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THESIS

**ANNEALING PROTOCOL AND FINITE ELEMENT MODEL
FOR RECOVERY OF RADIATION-DAMAGED
ELECTRONICS**

by

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June 2023

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**ANNEALING PROTOCOL AND FINITE ELEMENT MODEL FOR RECOVERY
OF RADIATION-DAMAGED ELECTRONICS**

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Captain, United States Army
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ABSTRACT

Technological advancements in electronic device scaling has led to the use of smaller spacecraft that can travel at higher speeds and lower costs associated with launch weight and propulsion. Traditional counter-radiation methods for space electronics involve hardened chip designs that negate the benefits of using smaller, lighter spacecraft. A self-healing counter-radiation approach, using a micro-heater to thermally anneal commercial-off-the-shelf (COTS) chips, is an attractive alternative due to performance enhancement and reduced cost and weight. In this research, the degradation of COTS transistors via gamma radiation and their subsequent recovery in the laboratory is experimentally proven. Through an iterative process, an annealing protocol is developed that successfully recovered damaged bipolar junction transistors (BJT) exposed to 5–10 Mrad radiation doses in approximately two hours at 200°C. Additionally, finite element modeling is used to create an annealing micro-heater, adjust heater parameters to optimize performance, and explore heater integration with a ceramic chip package, lid, and transistor. The annealing protocol and model results in this research provide the foundation for future self-healing efforts using more complex electronics, such as logic units. Furthermore, this research can serve to enhance the robustness of space electronics for future space missions executed by the DOD and subordinate organizations, such as the U.S. Space Force.

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List of Acronyms and Abbreviations

BJT	Bipolar Junction Transistor
CMOS	Complementary Metal-Oxide-Semiconductor
COTS	Commercial-Off-The-Shelf
DIP	Dual-In-Line Package
DoD	Department of Defense
EDS	Energy Dispersive Spectroscopy
ELDRS	Enhanced Low-Dose-Rate-Sensitivity
eV	Electron-Volt
FET	Field Effect Transistor
GAA	Gate-All-Around
GS	Gate-to-Source
IC	Integrated Circuit
KAIST	Korea Advanced Institute of Science and Technology
LLNL	Lawrence Livermore National Laboratory
MEMS	Micro-Electronic Mechanical Systems
MOS	Metal-Oxide-Semiconductor
NASA	National Aeronautics and Space Administration
NIEL	Non-Ionizing Energy Loss
NPS	Naval Postgraduate School
RH	Radiation Hardened

SEE	Single-Event Effect
SEL	Single-Event Latch-Up
SOT	Small Outline Transistor
TID	Total Ionizing Dose

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CHAPTER 1:

Introduction

1.1 Motivation

Recent technological advancements in electronic device scaling has driven efforts towards the use of miniaturized spacecraft that can explore near and far regions of the galaxy. While 10-centimeter-sided cube-shaped satellites, called CubeSats, have been in use since the early 2000s, even smaller satellites continue to emerge through aerospace efforts. For example, 3-centimeter-sided cube-shaped satellites, called Femto-Satellites, are currently under development and have the same technological capacity as the first CubeSats despite their decrease in size [1]. Nano-spacecraft, also called ChipSats, are even smaller spacecraft made up of a set of integrated circuits (IC). These tiny spacecraft, measuring only 3.2 centimeters in length and 5 grams in weight [1], lower launch weights and propulsion costs for space missions [2]. Their small size also allows them to accelerate to speeds one-fifth the speed of light, significantly decreasing interstellar exploration times. At this speed, the spacecraft could reach the closest stars to Earth, such as Alpha Centauri, in only 20 years [3], [4]. This is significantly less than the approximately 18,000 years it would take a conventional spacecraft to reach this region of space [2], as shown in Figure 1.1. This decrease in exploration time pushes the boundaries of space exploration and can lead to amazing new discoveries within the galaxy.

However, maintaining the functionality of small, complex spacecraft in the space environment is a challenging task. Throughout a spacecraft's lifespan, it can be exposed to various damaging aspects of the natural space radiation environment. Such aspects include energetic particles trapped by the magnetic fields of Earth or other planets, cosmic rays, and heavy nuclei produced through energetic solar events, such as solar flares [5]. Radiation exposure from these sources can lead to high levels of ionization, single-event effects, or displacement damage that can cease the functionality of semiconductor devices in a spacecraft and lead to mission failure [2]. These sources of space radiation and their effects are explored in further detail in Chapter 2.

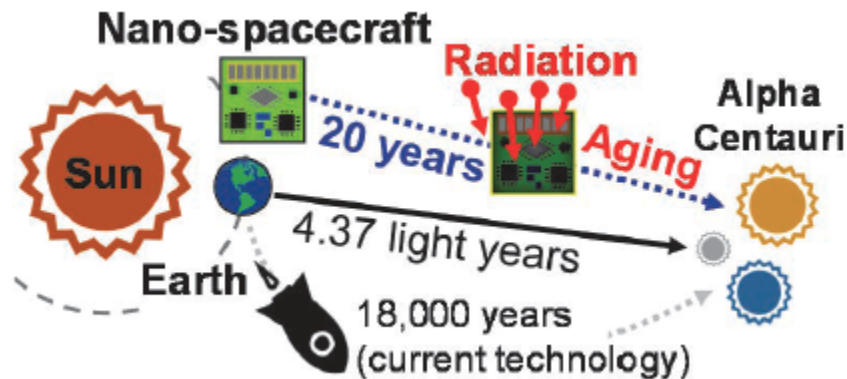


Figure 1.1. Nano-spacecraft, such as ChipSats, significantly decrease the travel time to the nearest stars compared to conventional spacecraft. However, nano-spacecraft are still exposed to damage from radiation and device aging issues. Source: [2].

Several options for addressing the damaging effects of radiation in space have been utilized in the past. The use of radiation hardened (RH) or shielded components is one such solution. However, radiation hardening and shielding increases the weight and cost of the system. Furthermore, RH components are no longer widely available and even those that are available do not offer the same performance measures as commercial-off-the-shelf (COTS) components [6], [7]. For these reasons, there has been an increase in the use of COTS parts instead of RH or shielded parts in space systems. Another option for addressing space radiation is path selection through space that minimizes radiation exposure [3]. However, the issue with selecting paths that specifically limit radiation exposure is that it reduces the bounds of space exploration and also leads to longer flight times to the mission objective.

An alternative to the above options is the development of a radiation counter-measure approach that is conceptually similar to the human immune system. An electronic immune system could detect and recover the device characteristics in a way that will keep electronics performing within acceptable parameters without the extra weight and cost penalties that come with radiation hardening or shielding [8]. It will also allow the spacecraft to travel through regions of space containing significant amounts of radiation, thereby reducing the need for a selective flight path. The mechanism of self-healing is accomplished via a micro-heater fabricated on the electronic component to be protected. The micro-heater operates using Joule heating allowing for thermal annealing. The National Aeronautics and

Space Administration (NASA) has visually demonstrated this concept for a Gate-All-Around (GAA) Field Effect Transistor (FET), as shown in Figure 1.2.

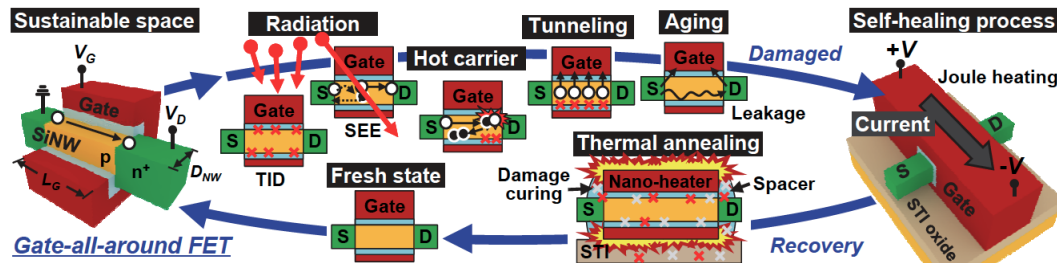


Figure 1.2. Concept of self-healing electronics. Radiation effects and aging cause damage to the device structure and functional characteristics. The self-healing process, through Joule heating and thermal annealing, can recover the device to its original condition, allowing for enduring performance in the space environment. Source: [2].

1.2 Research Objectives

The overarching goal of this research is to demonstrate that the functionality of an electronic component can be repaired on-the-fly when radiation damage is present. The successful demonstration of high radiation immunity can enhance the robustness of space electronics for future space missions. To that end, the first objective of this thesis is to use hands-on experimentation to demonstrate transistor defects due to radiation and their subsequent recovery in the laboratory. Three types of transistors are used as the test vehicles including NPN bipolar junction transistors (BJT), PNP BJTs, and metal-oxide-semiconductor (MOS) FETs. Using Cobalt-60 gamma radiation sources at Lawrence Livermore National Laboratory (LLNL), the above-mentioned transistors will be exposed to radiation levels seen in the space environment. The health of the devices will then be recovered via thermal annealing using a hot plate in the laboratory at Naval Postgraduate School (NPS) facilities. Through an iterative process, an appropriate annealing methodology will be developed to maximize device recovery.

Furthermore, this thesis uses finite element modeling to develop an annealing micro-heater. As a baseline and to verify the finite element model, micro-heaters provided to NPS by NASA will be modeled using COMSOL Multiphysics® software. The ways in which the

model is validated to represent the actual behavior of the micro-heaters are detailed in this thesis. The micro-heater model is used to adjust various device parameters, such as device geometry and materials, to achieve the desired effects.

1.3 Thesis Organization

This thesis is organized in five chapters and one appendix. Following this introduction, Chapter 2 discusses the space radiation environment and the effects radiation has on materials and devices commonly found in spacecrafts. The chapter then discusses some of the traditional methods used to mitigate the radiation effects of the space environment and their shortfalls. It concludes with a discussion of the physics underlying self-healing technologies. Chapter 3 outlines the experimental methods used to test, irradiate, and then recover BJTs and MOSFETs using radiation sources at LLNL and NPS facilities. This chapter also discusses the methods used to build and validate the COMSOL Multiphysics® model based on already fabricated NASA micro-heaters. Chapter 4 examines the results obtained from the experimental and modeling methods. This begins with a discussion of the radiation damage and subsequent recovery of the BJTs and MOSFETs exposed to radiation sources at LLNL. The second portion of the chapter presents the optimization results from the COMSOL Multiphysics® model. Chapter 5 presents the key research conclusions as well as recommendations for future research on this topic. Finally, the appendix provides a listing of the BJT and MOSFET recovery plots across all base currents and gate-to-source voltages, respectively, that are not explicitly shown in Chapter 4.

CHAPTER 2: Background and Theory

In order to understand the nature of self-healing technology for space applications, it is important to first understand the sources of space radiation, their effects on atomic structure and semiconductor devices, and the traditional methods used to mitigate these effects. After a discussion of these topics, the second portion of this chapter will cover emerging self-healing technology and the science behind them, including the physics of semiconductor conductivity, heat transfer, and Joule heating.

2.1 The Space Radiation Environment

One of the characteristics of the space environment is the presence of various sources and types of radiation. In short, the radiation environment observed in space consists of “a variety of energetic particles with energies ranging from kilo-electron volts (keV) to giga-electron volts (GeV) and beyond” [9]. Trapped particles, cosmic rays, and solar flares account for the majority of the radiation encountered in space [5], [9]. These three primary sources of space radiation are discussed in greater detail below.

2.1.1 Trapped Radiation

Trapped radiation consists of a broad range of energetic particles trapped in the magnetic field of the Earth. According to [9], “the field is basically that of a magnetic dipole and in those regions where the field lines are ‘closed’, charged particles become trapped in the magnetosphere.” These trapped, energetic particles form what are called radiation belts [9]. Earth’s radiation belts are made of electrons and protons with energies in the mega-electron volts (MeV) range. The electrons in Earth’s radiation belt have energies up to 7 MeV, with the highest energy particles located at higher altitudes (greater than 2.8 times the radius of the Earth) in a region called the outer zone. Conversely, the protons in Earth’s radiation belt have energies up to several hundred MeV. The most energetic protons in Earth’s radiation belt are found at lower altitudes in a region called the inner zone (less than 2.4 times the radius of the Earth) [9]. Understanding the radiation in these zones is important as spacecraft move through these regions on their way to outer space. Trapped radiation is

not exclusive to Earth, however, as this form of radiation also occurs around other planets and extraterrestrial bodies. For example, discoveries by the Galileo Spacecraft in the 1990s showed high levels of radiation around Jupiter. The spacecraft discovered that Jupiter's moon, Europa, is immersed in radiation trapped by Jupiter's magnetic field. This radiation has much higher energy levels than those around Earth and could certainly pose a threat to electronic components on spacecraft moving through that region [9].

2.1.2 Cosmic Rays

At the most basic level, cosmic rays are highly energetic atomic nuclei that are created through supernova explosions throughout the galaxy [5]. In [9], the authors describe the three sources of cosmic rays as galactic, solar, and terrestrial. Galactic cosmic rays are those which originate outside our galaxy and are a continuous source of radiation. Furthermore, in [9], the authors explain that these rays are composed of “about 85% protons, 14% alpha particles, and 1% heavier nuclei with energies extending to 1 GeV.” Solar cosmic rays, on the other hand, have a different origin than galactic cosmic rays. These cosmic rays are caused by solar material of low atomic weight being accelerated to a high velocity as a result of a solar flare. The overall energies of the rays are generally less than that of galactic cosmic rays [9]. Finally, terrestrial cosmic rays are produced as a result of galactic and cosmic ray interaction with the Earth's atmosphere. The transformation of these rays within the Earth's atmosphere produce secondary rays that are the main source of cosmic radiation at the Earth's surface [9].

2.1.3 Solar Flares

The final type of natural space radiation that will be discussed are solar flares. Solar flares are the result of energetic particles being emitted in bursts by the sun during solar storms. These energetic particles are mainly protons but also consist of lesser quantities of electrons and alpha particles [9]. The energy level of these particles is, in general, lower than trapped radiation but can certainly still impact the functionality of a spacecraft. For example, single flares in 1972 and 1989 dominated the solar cycle and, in the 1989 case, caused damage to several spacecraft solar arrays and disrupted onboard electronics [9]. Solar flares are also unpredictable, which poses a unique challenge in terms of a space mission's ability to adequately prepare for this type of radiation.

2.2 Space Radiation Effects

The study of the interaction between high-energy particles and photons with matter, called radiology, became prominent in the late 1950s when semiconductors became widely used in space and military applications [9]. The presence of radiation in space can lead to significant damage in semiconductor devices, which is naturally of great interest to manufacturers of electronics for space applications. Below is a discussion of the different effect's radiation can have on materials (atomic structure) and devices (such as semiconductors). In general, the final degradation depends on the radiation type, rate at which energy is entering the material, the type of material the radiation is entering, and how that material contributes to the overall function of the device in question [9]. Radiation effects in semiconductors can either be classified as destructive or non-destructive. Destructive effects are those that result in complete, catastrophic failure of the device. In other words, the device completely ceases to function. Non-destructive effects, on the other hand, are those in which the device can still function but not at full capacity. For example, data may be lost or complete control of the system may become infeasible [5]. The main radiation effects in materials and devices are ionization, single-event effects (SEE), and displacement damage. Since displacement events are of secondary concern for semiconductor devices [10] more attention will be paid to ionization and SEEs in this section.

2.2.1 Ionization

2.2.1.1 Overview

The first effect of radiation on materials and devices that will be discussed is that of ionization, also referred to as total ionizing dose (TID). This is the most significant source of radiation damage from the space environment in semiconductor devices. Radiation exposure from the trapped energetic particles, cosmic rays, and solar flares described above can lead to an accumulated TID of 10^5 rad, which is enough to cease functionality of semiconductor devices in spacecraft [5].

Ionization occurs when radiation enters a material (such as silicon in a semiconductor) with enough energy to create an electron-hole pair [10]. When the charged particles making up the radiation have a greater energy than the bandgap of the material, an electron in the valence band of the material is excited across the band gap and moves into the conduction

band [5]. This generates an electron-hole pair where the negatively charged electron is free to move about and the electron vacancy in the remaining atom, called a hole, acts like a positively charged particle. As an example, silicon has a band-gap of 1.1 electron-volt (eV). Therefore, when an energetic particle with more than 1.1 eV of energy penetrates the material, an electron-hole pair is created. Furthermore, when an electric field is present in the device material during normal operations, the electrons are swept away because their mobility in the material is greater than the mobility of the holes. The created electrons and holes then drift freely and diffuse in the material until they are recombined or trapped [5]. These additional electrons and holes change the value of the currents that are required for normal operation of the devices, which adversely impacts their operation.

2.2.1.2 Ionization in MOS and BJT Devices

In [10], the authors identify the three main components of ionizing radiation damage in the silicon dioxide layer of a MOS device as “the buildup of trapped charge in the oxide, an increase in the number of interface traps, and an increase in the number of bulk oxide traps.” When electron-hole pairs are created by the incident radiation, the electrons remain mobile and quickly move to the silicon and silicon dioxide interface. The holes, on the other hand, have lower mobility and may become trapped in the oxide. This leads to an overall net positive charge in the material. Some of the holes, however, may move to the interface between the silicon and silicon dioxide, where they will capture an electron and create an interface trap. Ionizing radiation may also break the chemical bonds in the silicon dioxide structure, which can lead to electric defects [10]. Both trapped charges and broken bonds can introduce their own electric field and potential in the device or modify the existing electric field or potential. This impacts the values of voltages and currents that are expected during normal operation, which adversely impacts the device. Figure 2.1 provides a schematic of a MOSFET before and after ionization of the gate oxide.

When this ionizing effect occurs, several performance parameters of the MOS device may be degraded. For example, there may be a shift in threshold voltage or decrease in gain which could cause the device to slow down. A negative shift in threshold voltage means a lower voltage would be required to turn the transistor on as a result of ionization [10]. This is problematic in that threshold voltage is a critical device parameter related to power consumption and speed. Shifting the threshold voltage can increase the supply current

which then disrupts the timing margins of the device [5]. A decrease in gain means a greater change in voltage is required to produce the same change in current as before the ionizing radiation. This is graphically depicted by a less steep I-V (current vs. voltage) curve for the device after ionization. High leakage currents can also occur, meaning that current may continue to flow through the transistor when no voltage is being applied [10]. This inability to shut off current between the transistor source and drain can lead to device failure [5]. The magnitude of the above effects depends on the amount of TID, rate at which the radiation is delivered to the device, temperature, and type of transistor [10].

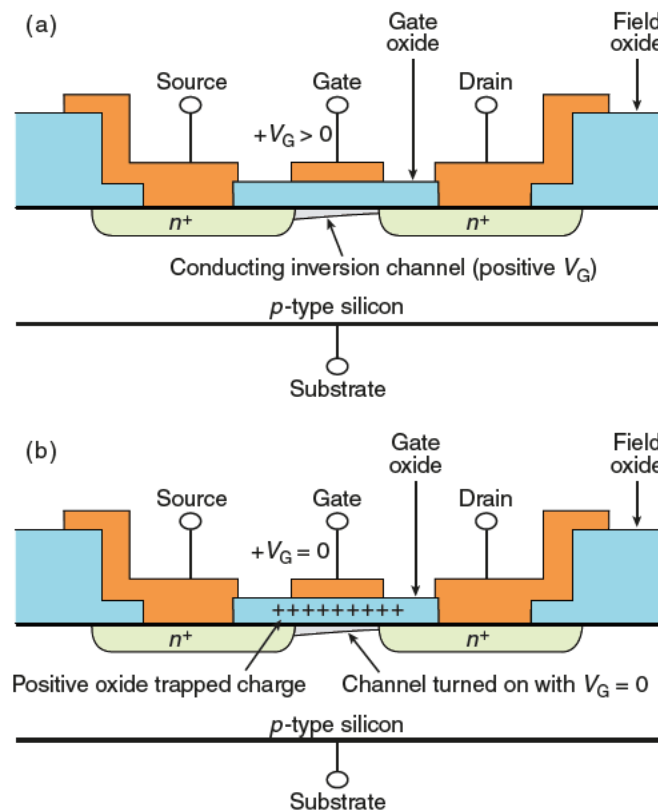


Figure 2.1. Schematic of MOSFET showing effects of TID of the gate oxide. Normal operation (a) and after ionization (b) shows residual trapped positive charges (holes) producing a negative threshold shift. Source: [5].

Research into the failure mechanisms in BJTs due to ionization can be traced back to the Telstar I communications satellite in 1962. A U.S. nuclear weapon detonation at high

altitude led to the enhancement of the Van Allen radiation belts and subsequently, the failure of the Telstar. It was found that gain degradation and leakage current caused the failure of a silicon diffused BJT on the satellite [11]. This established the understanding that degradation of gain and high current leakage are the two main impacts of ionizing radiation in BJTs. Through the same process as described in MOS devices above, trapped charges and interface traps are the main contributors to decreased gain. The trapped charges and interface states increase minority-carrier surface recombination velocity, reducing the ratio between collector current and base current, also known as emitter current gain. Ionization in the surface oxide of a BJT can also increase junction leakage currents, resulting in BJT device failure [9].

2.2.1.3 Enhanced Low-Dose-Rate-Sensitivity

One other type of ionization worth discussion is enhanced low-dose-rate-sensitivity (ELDRS). ELDRS has come about in the past three decades as a result of changes in integrated circuit fabrication that have made certain device components more sensitive to low dose rates of radiation. In other words, device degradation increases when the total dose is accumulated at a slower rate [11]. The physical explanation as to why this occurs deals with the space charge in the oxide of a transistor. In short, low dose rates lead to a lower space charge density in the oxide than at higher dose rates, which leads to more holes reaching the interfaces. This inherently increases the number of interface traps in the transistor [11]. While typical ground testing for TID occurs at roughly 50 rad/s, ELDRS testing needs to be done at rates of 10-100 millirad/s. This means that instead of accomplishing qualification testing in an 8-hour period (as is the case for TID), qualification testing for ELDRS can take weeks or even months [5]. This naturally has a significant impact on program schedule for space systems that may not be feasible. Industry has primarily handled this problem through radiation hardening (more on this in Section 2.3), which, while solving the schedule problems associated with ELDRS qualification testing, is still an expensive means to solve the problem.

2.2.2 Single-Event Effects

2.2.2.1 Overview

Another source of radiation damage in materials and electronic devices are called single-event effects (SEE) [5] or single-event phenomena (SEP) [9]. A SEE generally occurs when energetic particles from the radiation environment traveling through the electronic device lose energy by ionizing the material. The charge that is generated by this “single strike” produces a voltage on sensitive nodes that produce effects at the circuit level. The charge that is generated either recombines or gets collected at various nodes around the strike region. When the generated charge rises above the critical charge of the p-n junction, damage can occur [5]. Like ELDRS, SEE testing is generally not done by in-house facilities as is the case for TID testing. It requires the use of off-site particle accelerators, which inherently can increase the time and cost of the testing [5]. SEEs are broken down into several sub-categories: single-event latch-up (SEL), single-event upset (SEU), single-event burnout (SEB), single-event gate rupture (SEGR), single-event transients (SET), and single-event functional disrupts (SEFI). That said, single-event latch-up (SEL) is one of the most common SEEs discussed in literature and the most applicable to this thesis and, therefore, will be the focus of this section.

2.2.2.2 Single-Event Latch-Up

Single-event latch-up (SEL) is a type of SEE that occurs in ICs consisting of complementary metal-oxide-semiconductor (CMOS) architecture. The reason SEL is important for space applications is because, according to [5], “ICs fabricated with CMOS fabrication processes are very widely used in space electronics. “ When CMOS structures are located nearby one another, they form a parasitic BJT. No current is meant to flow through the base region of these formed parasitic BJTs under normal operating conditions [5]. However, single-event particle energy deposition can inject current into the parasitic base regions, forcing them into conduction [5], [9]. Positive feedback around the loop then causes the current to become larger and larger and, eventually, cause the voltage to drop below a threshold known as the holding voltage. When this occurs, the component can become damaged due to chip metallization failure or thermal runaway [5].

2.2.3 Displacement Damage

Displacement damage is the final radiation effect that will be discussed. It occurs when radiation causes atoms in a material structure to move from their original positions. When radiation enters a semiconductor material, such as silicon, a Frenkel defect pair is produced as a result of particle collisions. A Frenkel pair, in effect, is a displaced atom and the vacancy that is left by it. These are known as the intrinsic defects in the material. This dislocation disrupts the operation of semiconductor devices [9]. Figure 2.2 shows a schematic of atomic displacement and the resulting intrinsic defect (a vacancy and interstitial).

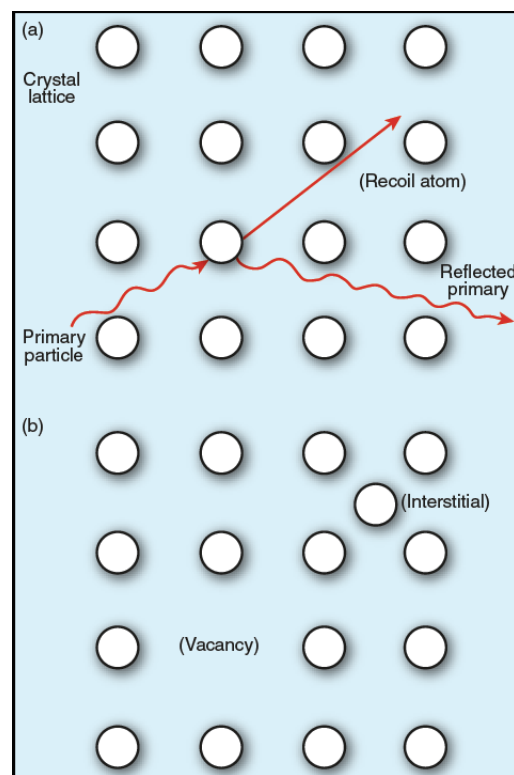


Figure 2.2. Schematic of atomic displacement. Atomic displacement event (a) and simple radiation-induced defects of a vacancy and interstitial (b). Source: [5].

Like TID, displacement damage is cumulative in that it compounds over time. Displacement damage is generally quantified using non-ionizing energy loss (NIEL). The NIEL coefficient is based on several factors such as the type of radiation, energy, and characteristics of the material the radiation is impacting. The most significant impact of atomic displacement

is the minority carrier lifetime in silicon is significantly reduced [10]. It can also lead to a change in the band-gap structure which, in turn, affects semiconductor properties. An example provided by [5] is that a deformation of the material structure in a solar array as the result of atomic displacement could lead to the solar array having less output power over the life of the spacecraft.

2.3 Traditional Solutions for Space Radiation

There are numerous efforts taken by manufacturers to mitigate the effects of radiation in materials and electronic devices. The most common solution is radiation hardening or shielding, however, other methods such as conservative circuit design have also been used. These approaches and their limitations were briefly discussed in Chapter 1 but will be analyzed in greater detail below.

2.3.1 Radiation Hardening

The term radiation hardening is rooted in military terminology [9]. Hardness, in the general military sense, means invulnerable to attack. Military and space hardening applications are similar in that they both analyze the ability to withstand the cumulative effects of ionization. Beyond that, military requirements are somewhat different than those seen in the space environment. For example, the military requirement for radiation survivability generally accounts for bursts of neutrons and gamma rays at a dose rate significantly higher than seen in space [9]. Therefore, not only does the military prepare for radiation bursts that are orders of magnitude higher than what is found in the space environment, but they also include neutron damage (such as those seen from a nuclear weapon). In the space environment, the term hardness refers to the tolerance of a material or device to radiation. Radiation hardening takes place at both the system and device levels. The system level looks at increasing the radiation tolerance of an entire piece of equipment consisting of many device level components. This predominantly includes large electronic systems [9]. The device level is comprised of increasing radiation tolerance at the semiconductor level, such as a MOSFET or BJT.

NASA has developed a programmatic methodology to hardening that takes a holistic approach. For example, they recommend an engineer be assigned as a lead specifically in

regards to radiation effects for each space flight project [6]. This engineer would serve as a single point of contact for all radiation issues related to the project to ensure performance in the space radiation environment. They also recommend this expert follow a programmatic guide from a systems perspective [6].

Radiation hardening, at the device level, is driven by a hardness methodology. Manufacturers want to use processes that are understandable and repeatable to produce components that respond well to radiation effects. Most hardening processes include robust simulation and physical analysis to proposed changes and evaluate the impacts on overall performance and other areas of the manufacturing process [9]. The manufacturing process includes several steps such as preparing and cleaning the material (ensuring the substrate material, such as silicon, is free of defects), oxide growth (volume of the oxide layer), oxide annealing (relieving stress at the oxide-silicon interface), application of gate electrodes and insulators, and application of an oxide mask. Therefore, manufacturer's must consider the impacts of a change on the most common performance characteristics of an IC, primarily, its speed, density, complexity, and power [9].

2.3.2 Radiation Shielding

Radiation shielding is a form of radiation hardening that involves essentially adding on material to armor or absorb radiation to protect the underlying device. This is done through fabricating a suitable material, typically a few millimeters in length, to the device, creating a barrier between it and the outside environment. Weight is a key consideration here. The more weight that is added to the system, the higher costs that will be associated with its operation. Larger weight can also effect performance parameters of the system, such as speed and propulsion. In order to keep the weight impact of shielding minimal, local or spot shielding may be used. In this case, the shield may be made more compact by applying it directly to a small area or single IC [9]. Other advancements in shielding materials have been made more recently. For example, tantalum and tungsten have been used for spot shielding for ICs. Both of these materials have high densities, approximately six times that of aluminum, allowing the shield material to be thinner [5]. Polyethylene composites have also been researched for their shielding capabilities. Unlike tantalum and tungsten, these materials have a density roughly one-third that of aluminum but provide similar shielding capability [12]. This makes them a good candidate for shielding in space applications since

their lower density has a lower impact on the cost to weight ratio of the system.

2.3.3 Limitations

There are two main limitations to radiation hardening and shielding. The first are design tradeoffs which impact the performance of the device. NASA points out in [6] that many RH devices used decades ago are no longer available and even those that are available are no longer considered state of the art. They provide a specific example in which semiconductor memory in RH devices are generations behind those used in COTS and the performance gap continues to grow. Given the limited control and frequent changes of COTS devices, there is more uncertainty surrounding how to effectively harden them from radiation [6]. Additionally, circuit designers are unable to keep up with new discoveries of radiation effects and, as a result, when a hardness methodology is undertaken, there are often last-minute changes or fixes which prove costly [6]. Additionally, there is an increased appetite for space exploration using miniaturized spacecraft. In [3], the author explains a joint venture between NASA and the Korea Advanced Institute of Science and Technology (KAIST) to deploy tiny spacecraft each composed of a single silicon chip. Shielding these chips, even with only a minimal weight impact, would completely nullify the advantage of having such a tiny spacecraft. The second major limitation to radiation hardening and shielding is the significant costs associated with it. As mentioned above, radiation hardening requires a robust methodology which takes a great deal of time, money, and expertise. NASA's approach discussed above includes a radiation expert with the sole task and responsibility of assessing hardness considerations for a program. Shielding is especially costly due to the price per weight penalty associated with it.

2.3.4 Other Solutions: Flight Path and Operating Conditions

It has been proposed that radiation damage can be mitigated by spacecraft utilizing selective flight paths that minimize travel through areas of high radiation [3]. This naturally makes sense because if high radiation areas are avoided, such as those discovered near Jupiter's moon Europa (discussed above in Section 2.1.1), then spacecraft have less chance of enduring damaging radiation. However, there are several downsides to a policy of radiation avoidance. For example, circumventing high radiation areas can lead to longer flight paths which in turn leads to longer mission timelines. Also, selective flight paths limit important

areas for space exploration [3]. Another downside to the selective flight path form of mitigation is the unpredictability of space weather. Solar flares, for example, are especially hard to predict [9], making this method of mitigation less compelling.

Selective operating conditions and device derating are final mitigations methods that have been proposed to reduce the effects of radiation. For example, some devices, after total dose testing, can be derated so out-of-specification parameters are not reached [5]. This is the case if the parameters will not affect the function of the circuit. In [5] an example is provided where a MOS-based operational amplifier with a very low input bias current was shown to be sensitive to TID. Radiation would increase the bias current by several orders of magnitude, however, the device could still operate successfully if modest value gain configuration resistors were used to minimize bias current drop. Other parts may also be used if they provide advantages such as low power consumption and high bandwidth while being less sensitive to radiation [5]. While this approach can be effective, like radiation hardening, it is a robust approach that requires a great deal of dedicated time and effort, which can increase the total cost of a space program. Also, relaxing tolerance margins on newer, state of the art technology inherently negates the performance benefits that come from using the state of the art technology in the first place [2].

2.4 Physical Theory Behind Self-Healing Technologies

As explained in Section 2.3, traditional solutions to mitigate the radiation effects of the space environment come with many limitations. NASA has pointed out in [6] that due to the simultaneous and competing requirements of increased data handling and other performance requirements, along with a decrease in spacecraft parameters such as power consumption, weight, volume, and cost, there has been a shift towards the use of COTS devices in emerging space technologies. The disadvantages of hardening/shielding, selective flight path, and other mitigation efforts have been detailed above. Dong Il Moon, of NASA, argues in [3] that a far better approach to these methods is to allow devices to sustain damage but design them so they can self-heal. Since 2016, NASA has been leading efforts in this field. In their previous works, they've proven the concept of self-healing in GAA FETs [2], both p-FETs and n-FETs [13], and at the die level [8]. The primary means of accomplishing this is through thermal annealing. Annealing, in a basic sense, is the restoration of a material or device to its original (pre-radiated) state by applying heat to the material or

device. For MOS systems, it was discovered that devices could be healed by removing trapped charges by heating to a temperature above 200°C [9]. Additionally, semiconductor device theory, heat transfer theory, and Joule heating are important in understanding how self-healing technologies work. These theories are discussed below and are incorporated in the experimental and modeling methodologies in the later chapters of this thesis.

2.4.1 Semiconductor Conductivity

Semiconductors, which have a conductivity between that of an insulator and conductor, are used in almost all modern electronics. One of the primary reasons for its wide use is that its conductivity can be controlled by a variety of methods. Such methods to alter the conductivity of a semiconductor include applying an electric field, varying the temperature, exposing to light, or introducing impurities, to name just a few. Due to these controls, semiconductors are used in nearly all electronic devices [14].

Conductivity (σ) can be calculated using

$$\sigma = \frac{1}{\rho} = \frac{J}{E}, \quad (2.1)$$

where ρ is resistivity, J represents current density, and E is the applied electric field [14].

The overall resistivity can be expressed as a function of the conductivity contributions of electrons and holes, which can be further expressed from the mobility and carrier concentrations, given by

$$\rho = \frac{1}{\sigma_n + \sigma_p} = \frac{1}{q(\mu_n n + \mu_p p)}, \quad (2.2)$$

where q is the charge of a unit carrier ($1.6 \times 10^{-19} C$), μ_n is the mobility of electrons, n is the concentration of electrons, μ_p is the mobility of the holes, and p is the concentration of holes [14].

The electrical resistance (R_E) of a semiconductor element is represented by

$$R_E = \frac{\rho L}{A}, \quad (2.3)$$

where L is the length of the resistor and A is the cross sectional area [14].

2.4.2 Heat Transfer

The three mechanisms through which heat transfer occurs are conduction, convection, and radiation. Conduction occurs when energy is transferred, in the form of heat through a material, from a hot region to a cold region. An example of conduction is given in [15] where the authors discuss the heat transferred to the handle of a metal fire poker whose opposite end is left in a hot fire. The atoms and electrons in end of the metal poker left in the fire will become excited from the hot temperature and pass their energy to neighboring atoms along the poker by colliding with them. The rate of conduction, or conductive power (P_{cond}), can be calculated using

$$P_{cond} = \frac{Q}{t} = kA \frac{T_H - T_C}{L}, \quad (2.4)$$

where Q is the heat, t is unit time, k is the thermal conductivity, A is the area, L is the thickness, and T_H and T_C represent the temperatures of the hot and cold reservoirs, respectively [15].

The thermal conductivity is a material property that changes with temperature. A material is considered a good thermal conductor if it more readily transfers energy. Thermal resistance (R_T) is another concept of note, given in [15] by

$$R_T = \frac{L}{k}. \quad (2.5)$$

In this case, the lower the thermal resistance, the better the thermal conduction. Conversely, if a material slab has a high thermal resistance, it is considered to be a good thermal insulator because it does not readily allow for heat transfer [15].

Convection, on the other hand, is the transfer of heat energy between a fluid (such as air) and an object when the object is at a higher temperature than the fluid [15]. Convective heat transfer is characterized by the heat flux at the interface, or wall, between the object and the fluid. The heat flux (q) is calculated using

$$q = h(T_0 - T_{env}), \quad (2.6)$$

where h is the heat-transfer coefficient, T_0 is the body temperature, and T_{env} is the fluid temperature [16].

Finally, radiation is when heat transfer occurs between an object and the surrounding environment via electromagnetic waves. Unlike conduction and convection, no medium is required for thermal radiation to occur (it can happen in a vacuum). The rate at which an object emits energy via radiation, also called the radiative power (P_{rad}), can be calculated using

$$P_{rad} = \sigma \varepsilon A T^4, \quad (2.7)$$

where σ is the Stefan-Boltzmann constant, ε is the emissivity of the object's surface, and T is the temperature in Kelvin [15].

Since objects both emit and absorb thermal radiation, it is also important to calculate the net rate of thermal energy exchange. The net power (P_{net}) is given in [15] and can be calculated using

$$P_{net} = \sigma \varepsilon A (T_{env} - T^4). \quad (2.8)$$

2.4.3 Joule (Ohmic) Heating

The physics underlying micro-heater technology is based on Joule heating of a resistor. Joule heating generates an increase in temperature. This temperature increase allows for the on-chip annealing of damages caused by TID radiation, hot carrier injection, and tunneling stress [2]. An overview of the joule heating process is described below with the relevant physical equations.

Joule heating is the term used to describe the process by which electrical energy is converted to heat energy. In other words, when a current flows through a semiconductor, energy is produced in the form of heat. This occurs due to collisions between current-carrying

electrons and the crystal lattice where some of the electron energy is passed to the atomic site. This increases the vibration of the site and increases in vibration are expressed via an increase in temperature. The theory begins with Joule's law, which is calculated using

$$P = I^2 R, \quad (2.9)$$

where P is the power, I is the electrical current flowing through the semiconductor, and R is the resistance [17].

Using the familiar form of Ohm's law ($V = IR$), Joule's law can be rewritten as

$$P = \frac{V^2}{R}, \quad (2.10)$$

where V is the voltage [17]. This equation makes it clear that, the higher the resistance of the resistor, more voltage is needed to produce the same amount of power. Furthermore, the amount of heat produced after a period of time can be calculated using

$$Q = Pt, \quad (2.11)$$

where Q is the amount of heat produced and t is unit time [17]. Finally, the rise or change in temperature can be found using

$$\Delta T = Qcm, \quad (2.12)$$

where ΔT is the change in temperature, c is the specific heat of the material, and m is the mass. These equations demonstrate how, during the conduction process, the collision of electrons transfer energy to semiconductors in the form of heat [17].

CHAPTER 3: Methodology

There are two distinct lines of effort pursued in this thesis. The first is an experimental effort to develop an annealing methodology to recover semiconductor device characteristics after they sustain damage from radiation, similar to the process followed by NASA in [2], [8] and [13]. The second is the building and validation of a finite element model using COMSOL Multiphysics[®] based on a micro-heater fabricated by NASA. This method will be used to continue design and optimization of later implementations of the micro-heaters. The methodologies used to accomplish these efforts are detailed below.

3.1 Self-Healing Experimental Proof-of-Concept

The methods and experiments used to measure semiconductor device health, damage the devices via radiation sources at LLNL, and subsequently heal the devices via thermal annealing on a hot plate are discussed in this section. The results of the experimentation are presented in Chapter 4.

3.1.1 Initial Measurements

The first step in this experimental process is to characterize the health of the devices. The FET devices used are 60V p-channel enhancement mode MOSFETs (part number: PJA3439) manufactured by Panjit Semiconductor. The NPN BJTs used are general purpose small signal amplifiers (part number: 2SC2412K) manufactured by Rohm Semiconductor. The PNP BJTs used are also manufactured by Rohm Semiconductor and are general purpose transistors (part number: 2SA1037AK). Previous work done by NASA used device parameters such as drain current versus gate voltage [2], [8] and shift in the device threshold voltage [8], [13] as acceptable device parameters for characterization. Based on this work and the data provided from the manufacturer data sheets, the collector current (I_C) versus collector to emitter voltage (V_{CE}) for the BJTs and the drain-to-source current (I_{DS}) and drain-to-source voltage (V_{DS}) for the FETs were chosen as the parameters to characterize device health. To gather pre-irradiation data, a Keysight B1500A semiconductor parametric analyzer was used to measure device I-V characteristics. In order to connect the transistor

to the parametric analyzer for measurement, the transistors were soldered to a small outline transistor (SOT) dual-in-line package (DIP) with six positions as shown in Figure 3.1.

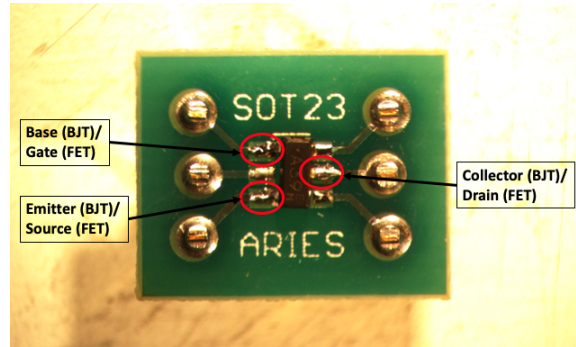


Figure 3.1. A transistor soldered to a SOT-23 DIP to enable measurement of device I-V characteristics on a semiconductor parametric analyzer. The soldered positions are circled in red.

Figure 3.1, shows that the transistors were soldered to the DIP at three positions. For the BJTs, these positions correspond to the base (top left), emitter (bottom left), and collector (middle right) of the transistor. For the FET, these positions correspond to the gate (top left), source (bottom left), and drain (middle right). Each position has a corresponding leg on the backside of the package, which can then be connected to the parametric analyzer via a red IC clip. The end of the clip opposite the transistor package was connected to the parametric analyzer in accordance with the emitter/gate, collector/source, and base/drain locations identified in the parametric analyzer software. Figure 3.2 is a picture of the semiconductor parametric analyzer system with a sample transistor connected.

The new devices produced I-V curves that reasonably agree with the data-sheets from the manufacturers [18]–[20] and were therefore classified as healthy. Figure 3.3 is an image of the data-sheet I-V curve for a PNP BJT from the manufacturer, Rohm Semiconductor, compared to the measured I-V curve for a sample PNP BJT. As seen from Figure 3.3, the collector current increases drastically between 0 and 0.5 volts (known as the linear region) and then tapers off for each given base current curve. This measurement process was repeated for each transistor. In total, two PNP BJTs, two NPN BJTs, and two FETs were. Due to limitations on the maximum drain current allowed by the parametric analyzer, only the linear region for the FETs was captured and compared to the data-sheet.

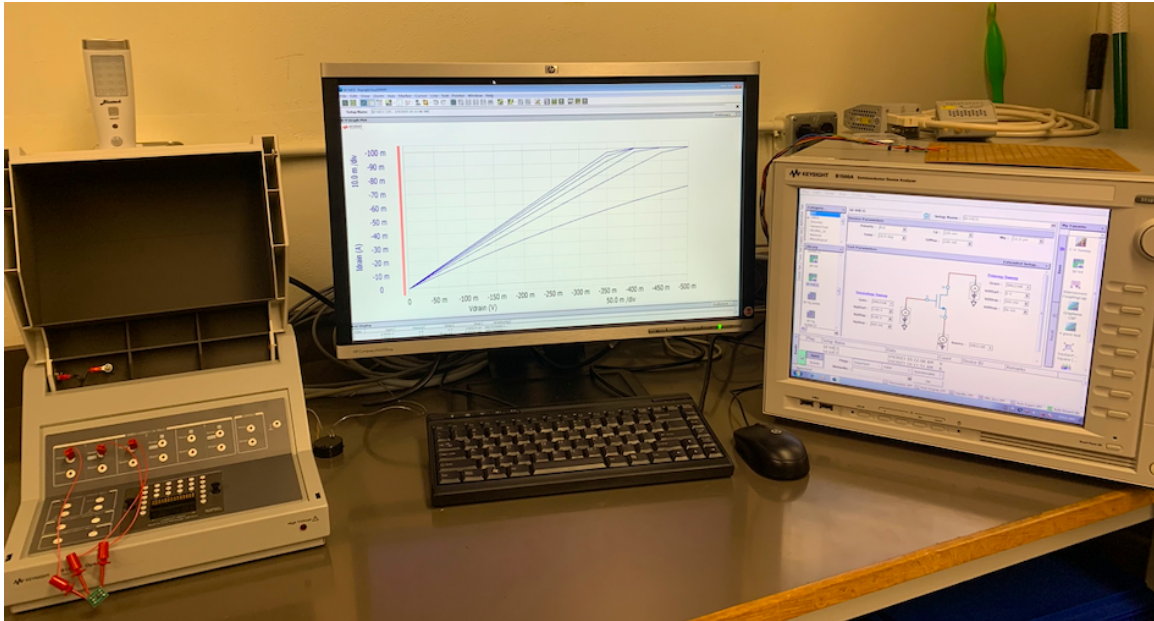


Figure 3.2. Keysight B1500A Semiconductor Parametric Analyzer with a sample FET connected.

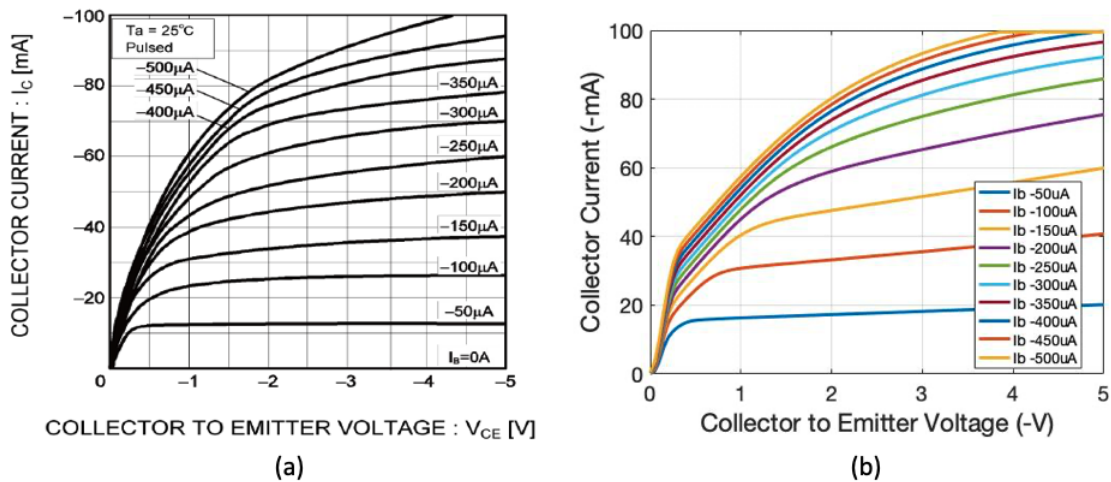


Figure 3.3. PNP I-V characteristics from the manufacturer data-sheet (a). Source: [19]. PNP BJT measurement using a semiconductor parametric analyzer (b). The curves show the Collector Current vs. Emitter Voltage at various Base Currents.

3.1.2 Radiation Damage

Facilities at LLNL were used to expose the healthy transistors to gamma radiation. Cobalt-60 was the gamma radiation source used. One of each transistor type (PNP BJT, NPN BJT, and FET) was exposed to a total dose of 5 Mrad, while the remaining three transistors were exposed to a total dose of 10 Mrad. This was to achieve the TID that can be experienced by space electronics when operating in space for extended periods [5]. Following their exposure to the radiation source, the devices were transported back to NPS where their I-V characteristics were measured. The resulting changes in transistor I-V characteristics post-irradiation will be discussed in Chapter 4.

3.1.3 Device Recovery

After capturing the changes in I-V characteristics for the transistors, recovery of the original device characteristics was attempted through thermal annealing on a hot plate in the laboratory at NPS. Figure 3.4 shows the hot plate with a sample device being placed on it. After the transistors are annealed, their I-V characteristics are remeasured. Figure 3.5 is a block diagram of the complete experimental setup to include the parametric analyzer components and hot plate.



Figure 3.4. Hot Plate used to thermally anneal damaged transistors.

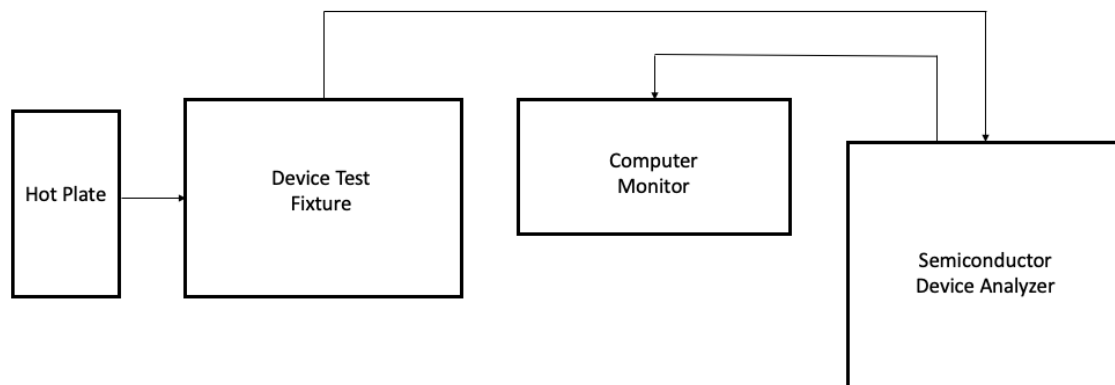


Figure 3.5. Block diagram showing the experimental setup for device measurement and recovery via thermal annealing. The device is annealed on the hot plate and then connected to the device test fixture at which point the parametric analyzer produces the I-V curves that are viewed on the computer monitor.

This was an iterative process through which changes in the annealing process were made after each iteration to develop an optimal annealing method. The first and second devices, a 5 Mrad damaged PNP BJT and FET, were placed on the hot plate at a temperature of 200°C. The devices were removed from the hot plate and measured every 10 minutes using the semiconductor parametric analyzer mentioned above. Subsequent iterations, including the 5 Mrad damaged NPN and 10 Mrad damaged FET, involved the devices being placed on the hot plate while still at room temperature to allow for a progressive heating up to 200°C. These later iterations also allowed for the devices to be slowly cooled down to room temperature prior to measurement. The reason for this change in annealing protocol was due to the I-V characteristic changes observed between when the device was still hot versus when it was allowed to cool. In other words, a temperature dependence was observed and, therefore, this change in annealing protocol serves to prevent thermal effects masking the true I-V curves of the devices. Final iterations, using the 10 Mrad damaged NPN and PNP BJTs, measured the device while still on the hot plate at various time intervals to capture the most realistic scenario for annealing on an actual space system. These final iterations also allowed for measurement after the devices cooled to best represent the final recovered condition. The results of these experiments are discussed in detail in Chapter 4.

3.2 COMSOL Multiphysics® Micro-Heater Model

The methods used to create and experimentally validate an annealing micro-heater finite element model are the subject of this section.

3.2.1 Creating the Model

COMSOL Multiphysics® version 6.0 is used for finite element modeling.

3.2.1.1 Model Geometry and Materials

As described in Chapters 1 and 2, NASA has done work on self-healing electronics to include fabrication of a prototype micro-heater design. NASA provided samples of their device to NPS, which are used as the baseline for this model. To build the model, several characteristics of the heater were measured. The horizontal dimensions of the heater to include the substrate and rectilinear, serpentine-style heater were measured using a AmScope microscope with an Omax digital camera attachment in the laboratory at NPS. Figure 3.6 is an image of the heater from the microscope with the dimensions annotated.

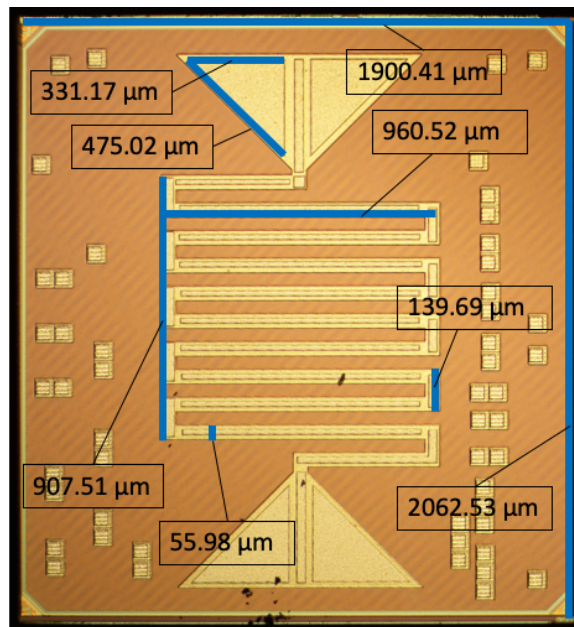


Figure 3.6. NASA micro-heater dimensions as measured with a microscope in the laboratory at NPS.

One of the limitations of using the microscope is that it cannot capture the thickness of the device layers. To measure the vertical dimensions, a FEI Inspect S50 Scanning Electron Microscope (SEM) was used. Figure 3.7 shows an SEM micrograph of the NASA heater, which was then used to measure the thickness of the micro-heater. Figure 3.7 shows various adhesion and electrical/thermal isolation layers of varying thickness for the rectilinear, serpentine portion of the heater. To simplify the model, only the thickness of the upper layer ($5.42\mu\text{m}$) was used in building the initial iteration of the model.

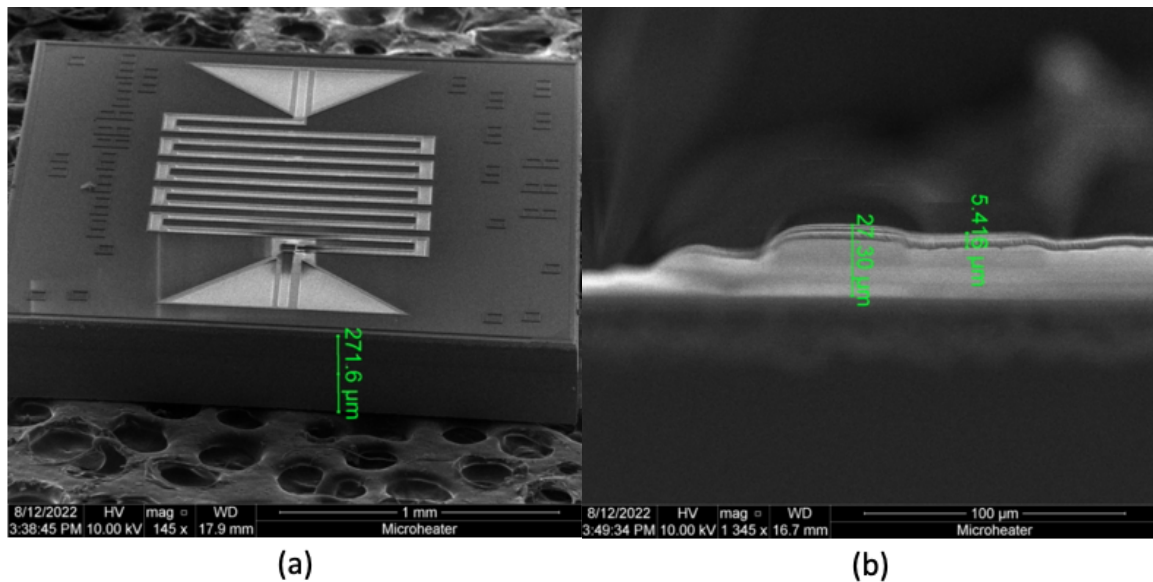


Figure 3.7. SEM micrograph of a sample NASA micro-heater as captured under a SEM (a) and a zoomed in, side-view of the micro-heater rectilinear region (b).

Using these dimensions, the model geometry was built in COMSOL Multiphysics®. This was done by creating a work plane in the model geometry and then building a simple block representing the substrate. Once the substrate was built to the correct length, width, and height, the rectilinear design was drawn to the given dimensions. The drawing was then extruded to give the heater the required thickness. The next step in the construction of the model was to select the various materials. An energy dispersive spectroscopy (EDS) attachment for the SEM is needed to determine the specific micro-heater materials. However, this particular attachment was not available for this research and, if possible,

should be incorporated in future work to further validate the model. Under the materials interface in COMSOL, silicon was selected as the substrate and gold was selected as the material comprising the rectilinear heater as these were considered the most likely materials to have been used and provided the closest match for measured resistance values.

3.2.1.2 Model Physics

Next, the COMSOL Multiphysics® modules were selected. The physics interfaces used for this model are the heat transfer in solids interface, the electric currents interface, and their coupling via the electromagnetic heating interface. The details of these interfaces and their underlying equations and variables are discussed below while drawing on their analogous equations from Chapter 2 as applicable.

Heat Transfer in Solids According to [21], “the heat transfer in solids interface is used to model heat transfer in solids via conduction, convection, and radiation. “ In its totality, the interface solves the following equation

$$\rho C_p \left(\frac{\partial T}{\partial t} \right) + \nabla \cdot (q + q_r) = Q, \quad (3.1)$$

where ρ is the density, C_p is the specific heat capacity, T is the absolute temperature, q is the heat flux by conduction, q_r is the heat flux by radiation, α is the coefficient of thermal expansion, and Q contains additional heat sources [21].

The interface is broken down into several sub-components that are used to solve the above equation. The first sub-component accounts for heat transfer via conduction. As discussed in Chapter 2, this is energy transfer in the form of heat from one object to another. The equation the interface uses to govern conductive heat transfer is

$$q = -k \nabla T, \quad (3.2)$$

where k is the thermal conductivity of the material and ∇T is the temperature gradient [21]. Furthermore, the model accounts for convective heat transfer. The equation the interface uses to govern the convective heat flux is

$$q_0 = h(T_{ext} - T), \quad (3.3)$$

where q_0 is the dot product between the normal vector (n) and the heat flux vector (q), h is the heat transfer coefficient, T_{ext} is the ambient temperature, and T is the temperature of the object [21]. This is analogous to Equation 2.6 from Chapter 2. The value for the heat transfer coefficient (h) was specified in the model as $20 \frac{W}{(m^2K)}$ which agrees with the values used in [13], [22]. The heat flux is an important boundary condition within the model and, as a default, all surfaces were selected to have a convective heat flux with the heat transfer coefficient value specified above. The external temperature was set to $20^\circ C$ (room temperature). Figure 3.8 provides a visual depiction of the heat flux boundary condition with all surfaces highlighted.

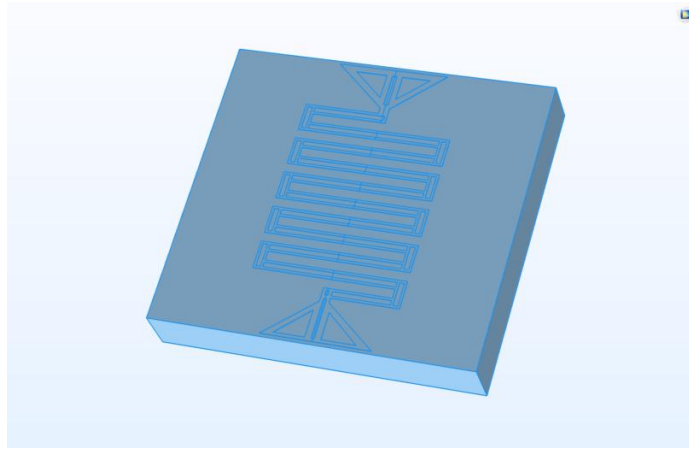


Figure 3.8. Heat flux boundary condition showing convective heat flux applied to all surfaces of the micro-heater.

Finally, the interface also accounts for surface-to ambient radiation losses. As described in Chapter 2, this is the heat transfer from a component to the outside environment, in this case, the air. The equation the interface uses to govern surface-to-ambient radiation is

$$-n \cdot q = \epsilon \sigma (T_{ext}^4 - T^4), \quad (3.4)$$

where n is the normal vector of the boundary, q is the conductive heat flux vector, ε is the emissivity, and σ is the Stefan-Boltzmann constant [21]. This is analogous to Equation 2.8 from Chapter 2. The surface-to-ambient radiation is another important boundary condition within the model. A separate surface-to-ambient radiation boundary was established for each material within the model. Default surface emissivities were initially assigned for gold and silicon, however, these values were adjusted later during the experimental model validation described in Section 3.2.2. Figure 3.9 provides a visual depiction of the surface-to-ambient boundary conditions for gold and silicon.

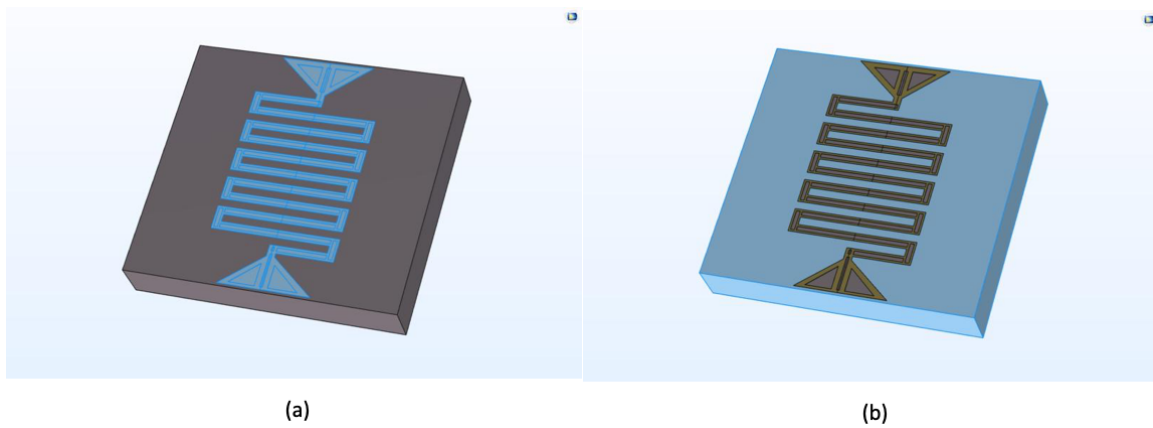


Figure 3.9. Surface-to-ambient radiation boundary condition for gold (a) and silicon (b). The areas highlighted in blue show the surface-to-ambient radiation boundary for each material with a unique surface emissivity value.

Electric Currents According to [21], the electric currents interface “is used to compute electric field, current, and potential distributions in conducting media under conditions where inductive effects are negligible.” Current conservation is the main node used in this interface and accounts for the equation for electric potential, which is defined by the relationship

$$E = -\nabla V, \quad (3.5)$$

where E is the electric field and ∇V is the electric potential gradient [21]. In addition to solving this equation, the current conservation node allows for defining the electrical

conductivity [21]. The electrical conductivity is related to the current density and electric field through the equation

$$J_c = \sigma E, \quad (3.6)$$

where J_c is the current density and σ is the electrical conductivity [21]. This equation is analogous to Equation 2.1 from Chapter 2. Furthermore, for the purposes of this model, the value for electrical conductivity (σ) is taken from the properties of the materials used. Finally, the current conservation node accounts for the electric displacement field and associated material property of relative permittivity. This is governed by the equation

$$D = \varepsilon_0 \varepsilon_r E, \quad (3.7)$$

where D is the electric displacement, ε_0 is the constant value for permittivity in free space ($8.854 \times 10^{-12} \frac{F}{m}$), and ε_r is the relative permittivity [21]. For the purposes of this model, the relative permittivity is taken from the properties of the materials provided by the COMSOL Multiphysics® library. Electric insulation is another node used in this interface and establishes electric insulation as a default boundary condition through the equation

$$n \cdot J = 0, \quad (3.8)$$

where n is the normal vector and J is the current density [21]. This boundary condition establishes that no current will flow through interior boundaries and, additionally, that electric potential is discontinuous across the interior boundaries. Figure 3.10 provides a visual representation of where the electric insulation boundary was established on the micro-heater.

After the electric insulation node, an initial values node is used to input the initial value for the electric potential [21]. The final nodes relevant to this interface in the model are the ground and terminal nodes. The ground node is used to select the model component where the potential is zero on the boundary. The terminal node is a floating potential node used

for a metallic electrode. This applies a constant voltage on the boundary and is governed by the equation

$$\int_{\partial\Omega} (-n \cdot J) dS = I_0, \quad (3.9)$$

where I_0 is a specific current and Ω represents the boundary [23]. Figure 3.11 shows where the terminal and ground boundaries were established on the micro-heater.

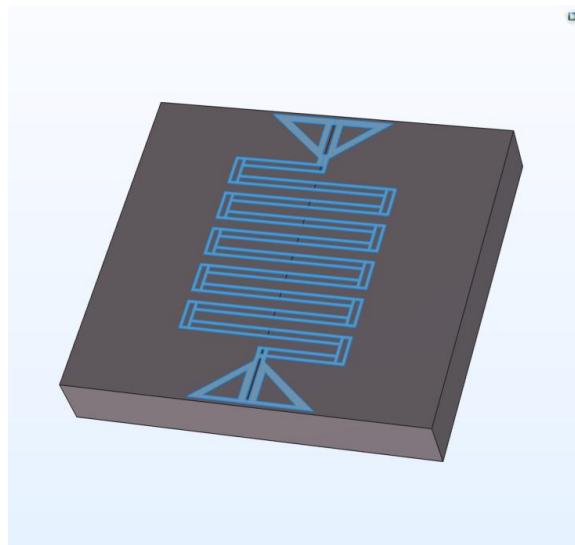


Figure 3.10. Electric insulation boundary on the micro-heater. This shows that current only flows through the highlighted blue regions.

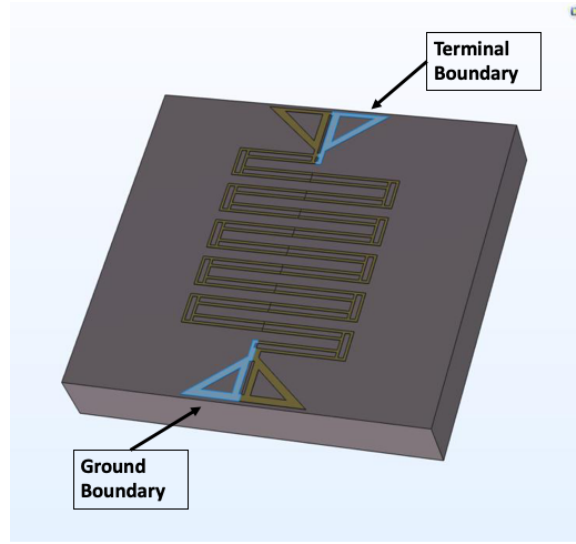


Figure 3.11. Terminal and ground node boundaries on the micro-heater.

Electromagnetic Heating One of the advantages of modeling in COMSOL Multiphysics® is the software’s ability to couple several types of physics simultaneously. In this case, the electromagnetic heating, or Joule heating, interface is used to combine the Heat Transfer in Solids and Electric Current interfaces. According to [24], “this multi-physics coupling accounts for electromagnetic losses in the Heat Transfer interfaces as well as for the temperature dependency of material properties in the Electric Currents interface.” The software accounts for this by adding a term to Equation 3.1 to account for resistive heating using

$$\rho C_p \frac{\partial T}{\partial t} - \nabla \cdot (k \nabla T) = Q_e, \quad (3.10)$$

$$Q_e = J \cdot E, \quad (3.11)$$

where Q_e is the resistive (ohmic) heating due to an electric current [21].

Upon completion of building the micro-heater geometry, selecting materials, and establishing the physical interfaces and boundary conditions, initial simulations were run. These simulations showed the temperatures the micro-heater could achieve at various input cur-

rents. Figure 3.12 shows the basic micro-heater model in COMSOL with the surface temperatures achieved at an input current of 0.9 Amps. In this case, a maximum temperature of 603 Kelvin, or 329.85°C, was achieved.

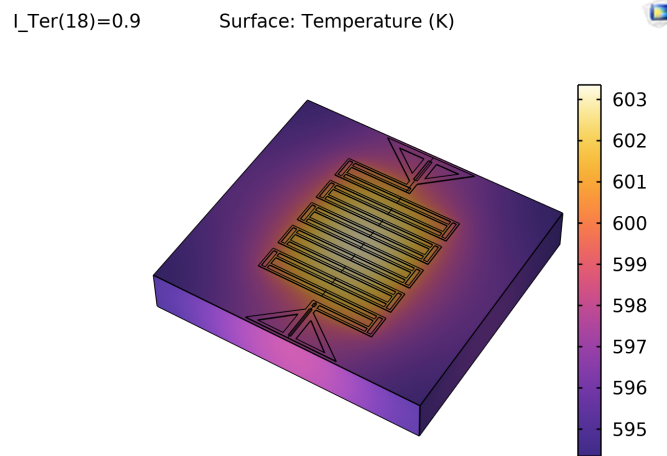


Figure 3.12. Example micro-heater simulation. The surface temperatures achieved are shown on the right hand side for an input current of 0.9 amps.

3.2.2 Validating the Model

Section 3.2.2 details the building of the micro-heater model. However, in order to validate that the model performs in accordance with the actual micro-heaters from NASA, the model needed to be validated experimentally. In order to experimentally measure various characteristics of the NASA heaters to ensure the accuracy of the model, the heaters were fabricated to a lead side brazed ceramic package with 28 nodes. Three heaters were secured to the package using a COTS epoxy. Once secured, the heaters dual-contact pads were wire bonded to the package at specified nodes. In total, five wire bonds were used for each dual-contact pad. The purpose for using multiple wire bonds was to improve current flow from the power supply to the heater and also to create redundancy in the event a single wire bond melted as the current applied, and subsequently temperature, increased. Figure 3.13 shows an image of the wire bonds created between the heater pads and package nodes as well as a zoomed in view of the wire bonds on a single heater secured to the package.

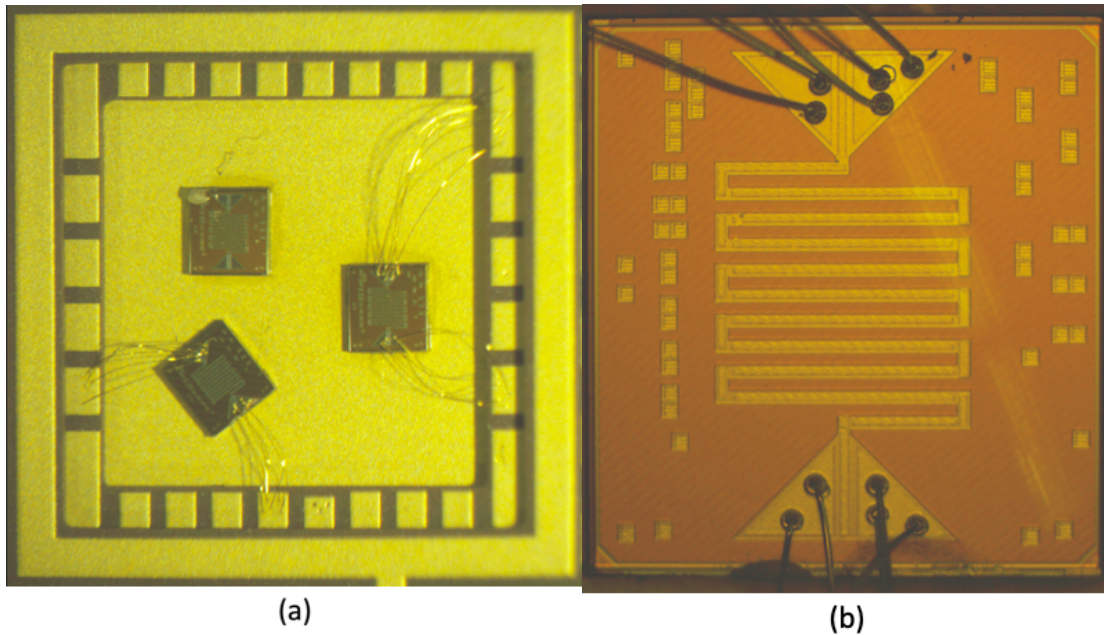


Figure 3.13. Image of three NASA heaters fabricated to a lead side brazed ceramic package (a) and a zoomed in view of a single NASA heater on the ceramic package (b). The heaters were secured to the package surface using a COTS epoxy and then wire bonded from the heaters' dual-contact pads to package nodes.

3.2.2.1 Heater Resistance and Thickness

The first parameter requiring validation was that of the heater's resistance. To measure the resistance of the heater experimentally, two heaters were connected to the same semiconductor parametric analyzer used in Section 3.1 to generate a plot of the current vs. voltage of the heaters as shown in Figure 3.14.

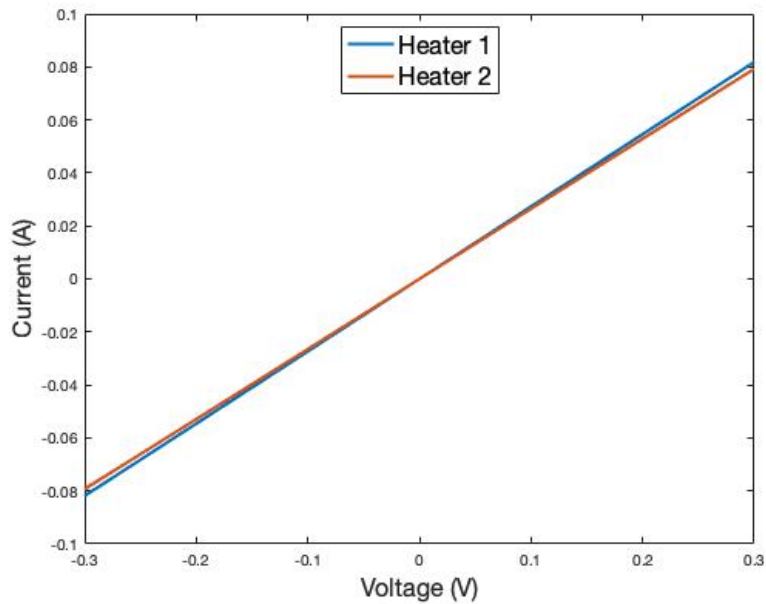


Figure 3.14. Current vs. Voltage for two sample NASA heaters as measured using a semiconductor parametric analyzer.

As seen from Figure 3.14, the current vs. voltage curves for the heaters are almost identical. Using the above curve for heater one (the blue line) and Ohm's law, the resistance of the heater was calculated as

$$R = \frac{V}{I} = \frac{150mV}{41mA} = 3.65\Omega.$$

However, this resistance accounts for the resistance of both the heater and the wire bonds used to bond the heater to the ceramic package. Therefore, the resistance of the wire bonds must be subtracted from the total resistance calculated above to give the resistance of the heater alone. The resistance of the wire bond alone was measured as 1.01Ω . Subtracting this from the total resistance calculated above yields

$$R_{Heater} = 3.65\Omega - 1.01\Omega = 2.64\Omega.$$

With the resistance of the experimental heater now being known, the rectilinear heater height was adjusted in the model until a resistance of 2.64Ω was achieved. This was accomplished using a parametric sweep of the heater thickness. This experimentally measured resistance was achieved in the model when the rectilinear heater height was set to $2.73\mu m$. As described in Section 3.2.1.1, the varying adhesive and isolation layers seen via the SEM required simplifying the rectilinear heater thickness for the initial model build. Therefore, slightly altering the rectilinear heater height was determined a reasonable method to achieve the experimentally measured resistance.

3.2.2.2 Surface Emissivities

Next, the emissivity of the surfaces of the heater materials required validation. To accomplish this, a Forward Looking Infrared (FLIR) camera was used to measure the temperature at specific locations on the device. A thermocouple was connected directly to the rectilinear heater to show the temperature of the surface. The emissivity was then adjusted using the FLIR software until the reading from the FLIR camera matched the reading from the thermometer. The emissivity for the rectilinear heater surface was found to be 0.3. For the silicon substrate, ceramic package metallized surfaces, and ceramic package non-metallized surfaces, the emissivity's were found to be 0.8, 0.9, and 0.99, respectively. These emissivity values were then incorporated into the model under the surface-to-ambient radiation nodes of the heat transfer in solids interface.

3.2.2.3 Temperature

The next parameter of interest was the model temperature at given voltages and currents. To experimentally determine the temperature of the heater, the ceramic package with the fabricated heaters was connected to a power supply. An Ammeter was incorporated in the loop to ensure the accuracy of the current value displayed on the power supply. Figures 3.15 and 3.16 are a block diagram and image of the experimental setup, respectively. These figures, specifically Figure 3.15, show how the power supply flows current to the heaters, whose temperature is captured via the FLIR camera which then provides a display of the temperature output on the laptop.

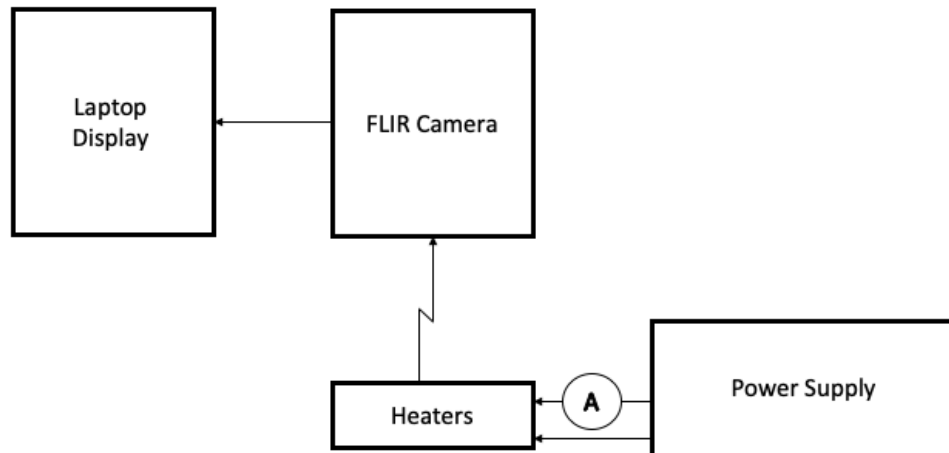


Figure 3.15. Block diagram of the experimental setup used to validate the temperature vs. current relationship of the heaters. The power supply applies a bias to the heaters, whose temperature is measured by the FLIR camera, which produces an output on the laptop display.

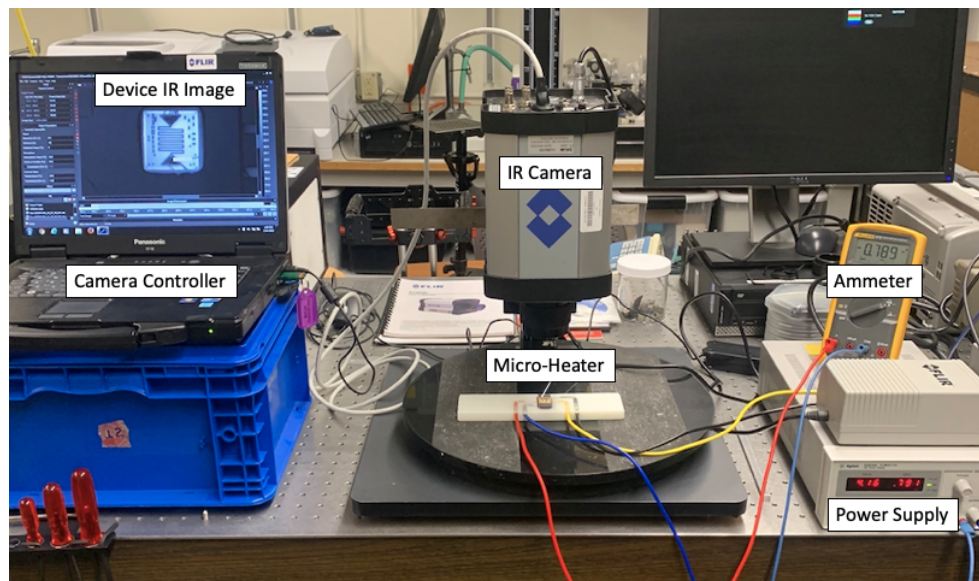


Figure 3.16. Experimental setup to measure the heater temperature vs. current relationship.

With the experimental setup complete, the process of measuring heater temperature at given currents began. The current was increased on the power supply in 50 mA increments until a steady state temperature was achieved. This generally occurred between five and ten minutes after the current on the power supply was set to a specified value. The current, corresponding voltage, and temperatures were then recorded. This process was then repeated for a second heater. For both heaters, the experiment ended when the heater reached approximately 300°C due to the heater sustaining damage. Upon completion of the experiment, the temperature was plotted against the current and compared to the temperature vs. current from the finite element model. Initially, the model produced much higher temperatures than the experimental data. However, it was quickly observed that modeling the heater alone would not be sufficient. The ceramic package and epoxy used to fasten the heaters to the package must also be included in the model as they were serving as a large heat sink for the generated heat. To do this, the ceramic package dimensions were obtained from the manufacturing company, Spectrum Semiconductor [25], and built into the model. Figure 3.17 shows the geometry of the micro-heater on ceramic package concept.

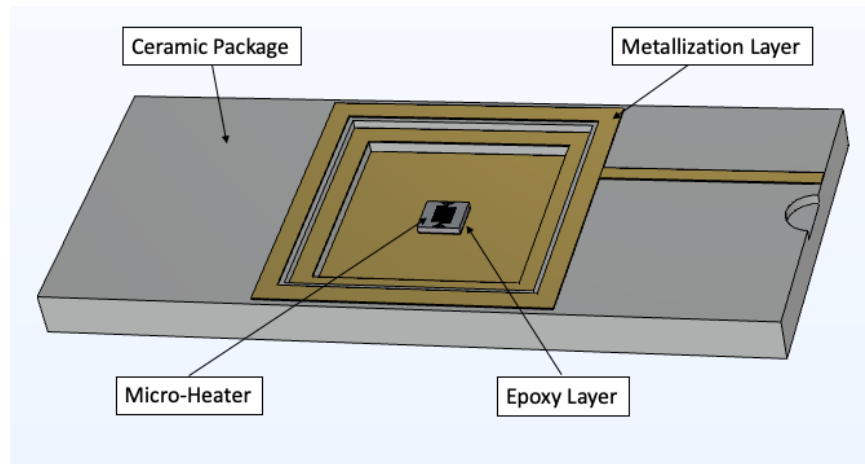


Figure 3.17. Model geometry of a micro-heater secured to a ceramic package using an epoxy layer.

The thermal properties of the ceramic package material, Alumina 440 (A440), was obtained from the Kyocera website and manually input in the model material properties [26]. An epoxy (cyanoacrylate) layer was also added with an estimated thickness of 35 μ m. From [27] the thermal conductivity of cyanoacrylate at room temperature is 0.11 $\frac{W}{mK}$ which was

manually input into the model material properties. Additionally, the material properties of silicon were confirmed to match the parameters used in previous NASA micro-heater modeling efforts [13]. Table 3.1 summarizes the key parameters used in the model. Once these additional geometries and material properties were incorporated into the model, a parametric sweep was executed to measure the temperatures achieved by the modeled heater at various currents. Figure 3.18 shows the graphs of temperature vs. current for the model and experimental heaters.

Table 3.1. Simulation Parameters for Model Materials

Parameter	Units	Silicon	Gold	Ceramic (A440)	Cyanoacrylate
Heat Capacity at Constant Pressure	$\frac{J}{kg \cdot K}$	700	129	780	1,470
Density of Material	$\frac{kg}{m^3}$	2,329	19,300	3,600	1,060
Thermal Conductivity	$\frac{W}{m \cdot K}$	130	317	14	0.11
Electrical Conductivity	$\frac{S}{m}$	$1 * 10^{-12}$	$45.5 * 10^6$	-	-
Coefficient of Thermal Expansion	$\frac{1}{K}$	$2.6 * 10^{-6}$	$14.2 * 10^{-6}$	$7.1 * 10^{-6}$	$8.0 * 10^{-5}$

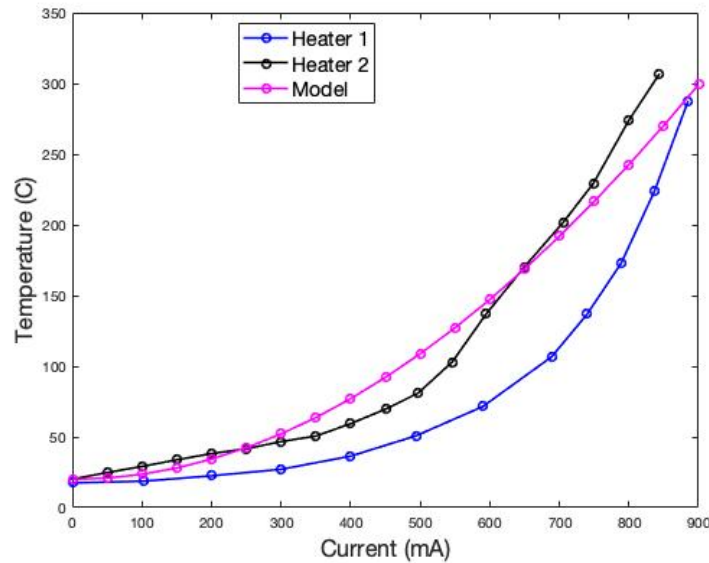


Figure 3.18. Temperature vs. Current for the two experimental NASA heaters and the model.

Figure 3.18 shows that the model exhibits behavior similar to that of the experimental heaters. In other words, the model produces comparable temperatures at given input currents. This model will be useful to adjust heater parameters of future iterations of the micro-heaters in order to optimize performance. Furthermore, this model also allows for the analysis of add-on features, such as a ceramic lid, additional heaters, and transistors to model the temperatures achieved given these changes. These parameters and the way in which the model behaves given their changes is the subject of the second part of Chapter 4.

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CHAPTER 4:

Results

4.1 Experimental Results

In this section, the experimental results from the thermal annealing of transistors damaged by gamma radiation is discussed. The amount of damage suffered by the transistors at 5 Mrad and 10 Mrad is covered first, followed by a discussion of the annealing process and recovery of each device. The recovery of the 5 Mrad exposed devices is discussed first, followed by the 10 Mrad exposed devices. This allows for a chronological account of the changes to annealing methods made throughout the experiment to achieve the greatest level of device recovery possible.

4.1.1 Device Damage

As discussed in Chapter 3, one of each type of transistor used in this experiment was exposed to a total dose of 5 Mrad from a Cobalt-60 gamma radiation source at LLNL. The remaining three devices (also one of each type) were exposed to the same Cobalt-60 gamma radiation source but for an additional two-weeks, allowing them to attain a total dose of 10 Mrad. In each case, all devices were damaged to levels that would impact their ability to function as designed. Figure 4.1 and Figure 4.2 show the damage sustained by the transistors at 5 Mrad and 10 Mrad gamma irradiation. For clarity, one base current curve was plotted for each BJT and one gate-to-source (GS) voltage was plotted for each FET. However, these figures are indicative of the damage sustained across all base currents for the BJTs and all GS voltages for the FETs. Figure 4.2 also includes the damage sustained for an FET at a lower GS voltage. This additional figure is included for the FET to demonstrate how, at 10 Mrad exposure and low GS voltages, the device gives no current reading for any drain-to-source voltage and potentially suffered catastrophic failure.

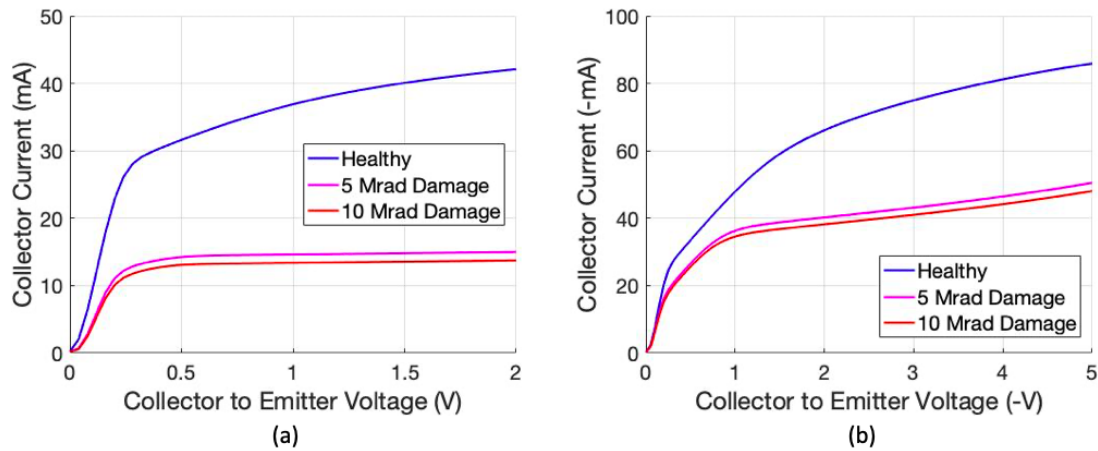


Figure 4.1. NPN BJT (a) and PNP BJT (b) device characteristics at $250\mu\text{A}$ base current when measured healthy, after exposure to 5 Mrad gamma radiation, and after exposure to 10 Mrad gamma radiation.

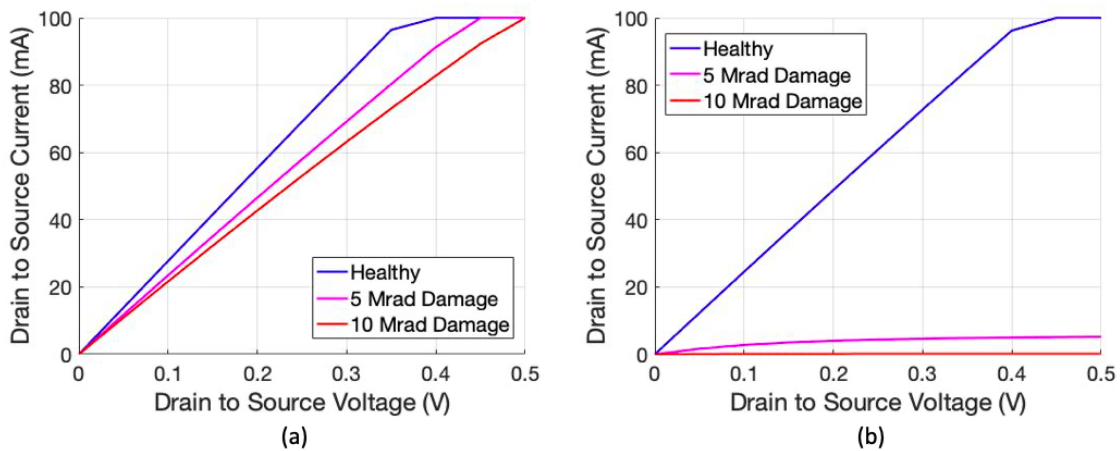


Figure 4.2. FET device characteristics at a 5V GS voltage (a) and 3.5V GS voltage (b) when measured healthy, after exposure to 5 Mrad gamma radiation, and after exposure to 10 Mrad gamma radiation.

Figure 4.1 and Figure 4.2 show that the collector current (BJTs) or drain-to-source current (FETs) measured at a given collector-to-emitter voltage (BJTs) or drain-to-source voltage (FETs) post irradiation decreased compared to measurements taken when the devices were healthy (pre-irradiation). As discussed in Chapter 2, Section 2.2.1.2, this is an example of

a decrease in device gain, meaning under their damaged condition, a greater GS voltage is required to produce the same pre-irradiation current, compromising the device functionality. This is an example of ionization occurring in each device as a result of their exposure to gamma radiation. Also, as expected, the devices exposed to 10 Mrad sustain more damage than those exposed to 5 Mrad. However, the difference in the amount of damage sustained is less between 5 Mrad and 10 Mrad than between the healthy device and 5 Mrad. After characterizing the damaged devices, the process of healing the devices via thermal annealing took place as discussed in following sections.

4.1.2 Recovery of Devices Exposed to 5 Mrad

The experimental results from thermal annealing the transistors exposed to a total dose of 5 Mrad Cobalt-60 gamma radiation are discussed in this section.

4.1.2.1 PNP BJT Recovery

The first device thermally annealed was the PNP BJT exposed to 5 Mrad gamma radiation. The device was placed onto an already heated hot plate at 200°C. The device was left on the hot plate for 10-minute time intervals. After each 10-minute interval, the device was removed and immediately measured (while still hot) and then returned to the hot plate. This process continued for a total of 3 hours. The measurements show that the device appeared to fully recover at lower base currents (specifically at 50μA) with less and less complete recovery observed at higher base currents. The next day, after the device had cooled to room temperature, the device was measured again. These measurements show that the device became less healthy at low base currents (from 50μA to 250μA) and healthier at higher base currents (from 300μA to 500μA). This demonstrates the temperature dependence of the device performance. Further annealing was then attempted by slowly heating up and cooling down the device, as opposed to placing the device on an already heated up hot plate and measuring the device while it was still hot. In this case, the device was heated to 200°C, remained in place for one hour, cooled down for 30 minutes, and then measured. This process was repeated, with the exception that the device was left on the hot plate for a 90-minute iteration at 200°C. Using this method, the device recovery was improved across all base currents. However, measurements taken the following day showed the device again relaxed and became unhealthier across lower base currents (from 50μA to 250μA). The

device health stayed roughly the same at higher base currents ($300\mu A$ to $500\mu A$). One final attempt at further annealing took place using the same progressive heat up and cool down method for two hours at $225^{\circ}C$, and then again for two hours at $250^{\circ}C$. This led to marginal recovery across all base currents. Figure 4.3 shows the progression of device recovery for the 5 Mrad exposed PNP BJT at $350\mu A$ and $50\mu A$, respectively. These plots are representative of the differences in recovery between lower base currents ($50\mu A$ to $250\mu A$) and higher base currents ($300\mu A$ to $500\mu A$).

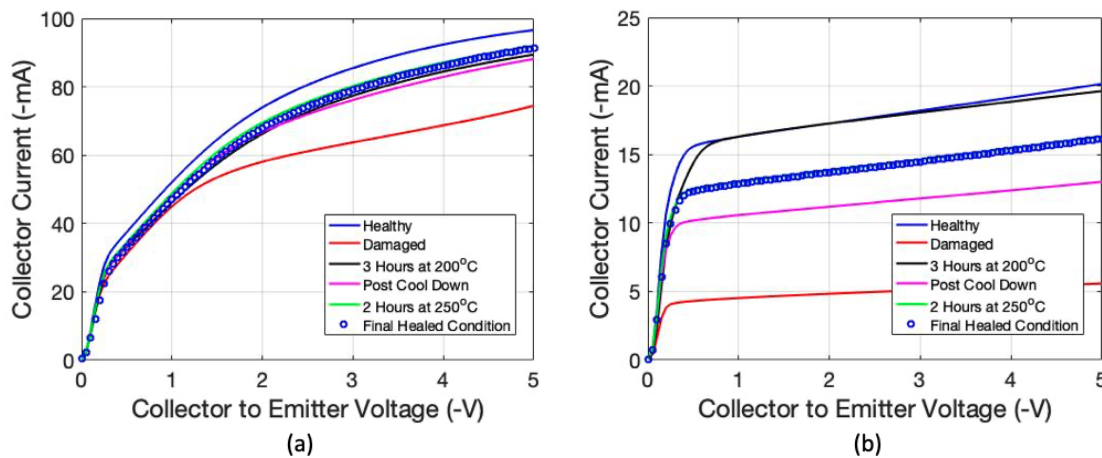


Figure 4.3. I_C versus V_{CE} characteristics at a $350\mu A$ base current (a) and $50\mu A$ base current (b) demonstrating device recovery for a PNP BJT after 5 Mrad gamma radiation exposure.

Figure 4.3 shows that the device never fully recovered. Higher annealing temperatures were not attempted due to the $300^{\circ}C$ heater limitation discussed in Chapter 3. Plots for the remaining base currents not pictured here are included in Figures A.1-A.8 in Appendix A.

4.1.2.2 FET Recovery

The second device thermally annealed was the FET exposed to 5 Mrad gamma radiation. The same method was used for this transistor as for the PNP BJT (where the device is placed on already heated up hot plate at $200^{\circ}C$) to see if the FET would produce a different recovery profile than the PNP BJT. Again, as with the PNP BJT, the device was removed and immediately measured (while still hot) at 10-minute intervals. Initially, the device

appeared to become unhealthier but then began to recover as time progressed. Annealing continued for a total of three hours, however, minimal recovery occurred after one hour and the device never approached its original healthy state. One final attempt was made to recover the device for 2 more hours at a higher temperature of 250°C , however, upon removal of the device from the hot plate for measurement, the device failed to record measurements. Upon further observation, the solder had melted, resulting in a poor connection between the transistor and package, resulting in the failed device measurement. Overall, the device failed to anneal to near its original healthy state, and in fact, showed no recovery at low GS voltages (2.5V and 3V). Figure 4.4 shows the I-V characteristics for a high GS voltage (4.5V) and a lower GS voltage (3V) before and after thermal annealing.

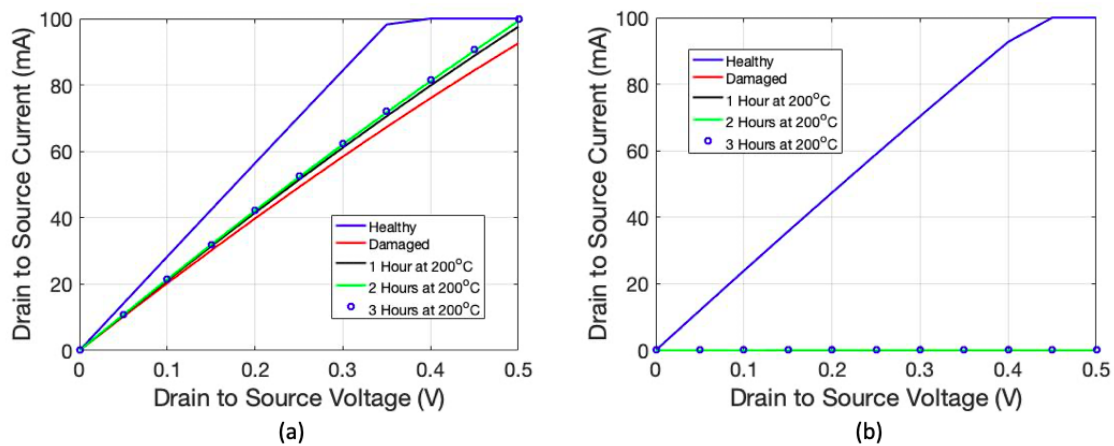


Figure 4.4. I_{DS} versus V_{DS} characteristics at a 4.5V GS voltage (a) and 3V GS voltage (b) demonstrating device recovery for a FET after 5 Mrad gamma radiation exposure.

Figure 4.4 shows that, at high GS voltages, some recovery occurs. However, the device recovers to only about 25% of its original characteristics, which is likely not enough to allow it to function within its designed parameters. At low GS voltages, no recovery occurs regardless of healing time and temperature, indicating the device suffered catastrophic damage from the 5 Mrad radiation. Also, this shows there was a shift in the device threshold voltage where 3V GS voltage was above the threshold before exposure, but the threshold was pushed to higher limits during exposure. Plots for the remaining GS voltages not pictured here are included in Figures A.9-A.12 in Appendix A.

4.1.2.3 NPN BJT Recovery

This device incorporated the progressive heating/cool down annealing method whereby the device was placed on the hot plate at room temperature and slowly heated up to an annealing temperature of 200°C . This is more accurate to how annealing would occur on a spacecraft since the heater (and subsequently, the transistor) would take time to heat up before reaching a temperature of 200°C . After annealing for a total of 3 hours (with measurements taken at 30-minute, 90-minute, and 3-hour time intervals), significant device recovery is observed. Additional healing was attempted at higher temperatures (225°C and 250°C for a period of 2 continuous hours each) in an effort to achieve potentially full device recovery. However, the higher temperatures led to minimal improvement in device health across all base currents. Figure 4.5 shows the I-V characteristics before and after thermal annealing of the 5 Mrad exposed NPN BJT at the highest ($500\mu\text{A}$) and lowest ($50\mu\text{A}$) base currents.

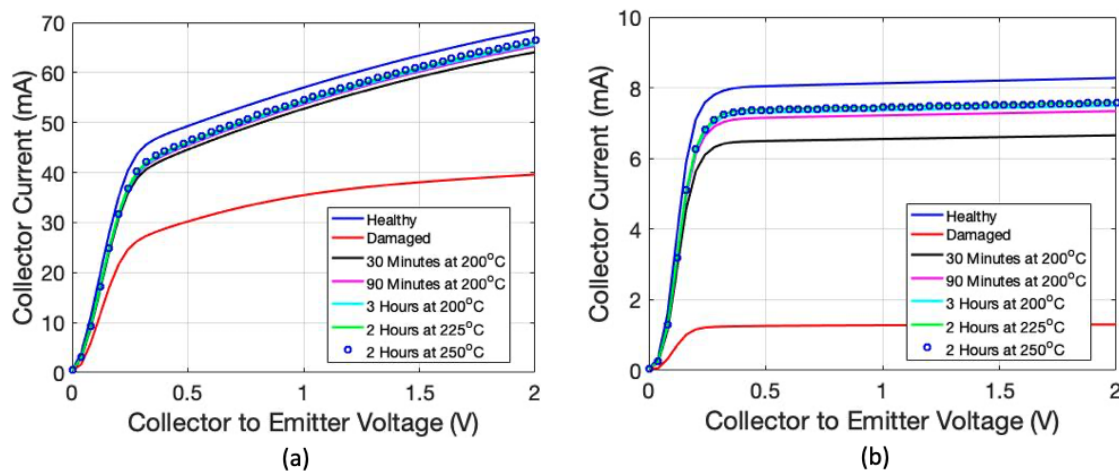


Figure 4.5. I_C versus V_{CE} characteristics at a $500\mu\text{A}$ base current (a) and $50\mu\text{A}$ base current (b) demonstrating device recovery for a NPN BJT after 5 Mrad gamma radiation exposure.

Figure 4.5 shows that at both high and low base currents, the healing behavior is the same in that a higher level of device recovery is achieved the longer the device is annealed. The 2 hours at 250°C (blue dots) plotted above represent the recovered device characteristics. This was confirmed after measurements taken one full day after annealing showed no change in the I-V characteristics of the device. Overall, at 200°C annealing, device health increased

by approximately 90% across all base currents. Since devices are designed to tolerate a roughly 10% parameter shift [8] this demonstrates adequate recovery and could allow the device to continue functioning as intended. Plots for the remaining base currents not pictured here are included in Figures A.13-A.20 in Appendix A.

4.1.3 Recovery of Devices Exposed to 10 Mrad

The experimental results from thermal annealing the transistors exposed to a total dose of 10 Mrad Cobalt-60 gamma radiation are discussed in this section.

4.1.3.1 FET Recovery

The first 10 Mrad exposed device thermally annealed was the FET. The method used to anneal this device was the progressive heating/cool down method due to the better results achieved for the 5 Mrad NPN BJT using this method. The device was annealed for 3 hours at 200°C and then for an additional 2 hours at 225°C. Figure 4.6 shows the recovery results for this FET at 4.5V and 3V GS voltages.

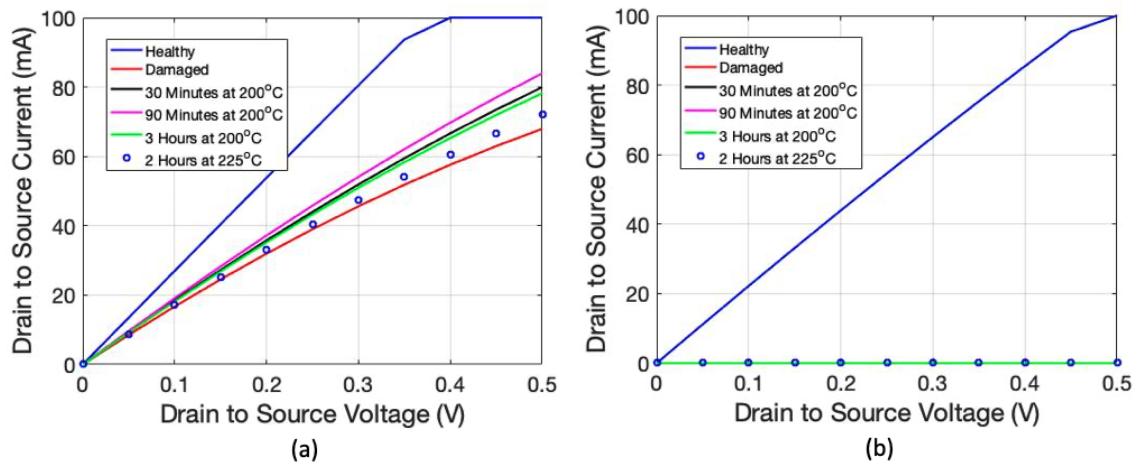


Figure 4.6. I_{DS} versus V_{DS} characteristics at a 4.5V GS voltage (a) and 3V GS voltage (b) demonstrating device recovery for a FET after 10 Mrad gamma radiation exposure.

Figure 4.6 shows no recovery for low GS voltages. The drain-to-source current continued to read zero regardless of the temperature or annealing time. As in the case of the 5 Mrad

exposed FET, this behavior indicates a shift in the device threshold voltage where 3V was above threshold before exposure, but the threshold was raised during exposure. It is clear that 10 Mrad TID damaged this device beyond repair at these lower GS voltages. For higher GS voltages, some recovery occurs after 30 minutes and 90 minutes of annealing at 200°C. Interestingly, beyond 90 minutes at 200°C, additional annealing appears to further damage the device. In fact, the device almost returns to its initially damaged state. Plots for the remaining GS voltages not pictured here are included in Figures A.21-A.24 in Appendix A.

4.1.3.2 NPN BJT Recovery

The next 10 Mrad exposed device thermally annealed was the NPN BJT. The method used to anneal this device was the progressive heating method, however, the device was measured while it was still on the hot plate. After 2 hours of annealing at 200°C, the temperature was increased to 225°C for 30 minutes and then 300°C for an additional 30 minutes in an effort to achieve maximum healing. Cool down occurred only after annealing was complete. A cool down measurement was taken 30 minutes after the device was removed from the hot plate as well as the following day. Figure 4.7 shows the recovery results for this NPN BJT at 500μA and 50μA base currents. These base currents were selected for consistency with the 5 Mrad NPN BJT figures included in this chapter.

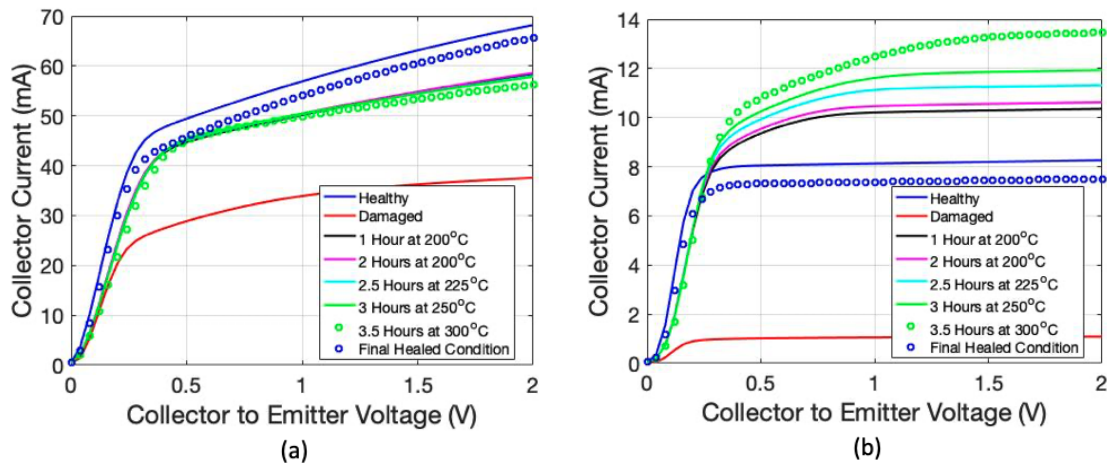


Figure 4.7. I_C versus V_{CE} characteristics at a 500μA base current (a) and 50μA base current (b) demonstrating device recovery for a NPN BJT after 10 Mrad gamma radiation exposure.

From Figure 4.7 significant recovery is observed after one hour of thermal annealing at 200°C . At high base currents (represented by the $500\mu\text{A}$ base current in the figure), minimal to no recovery occurs after one hour. At low base currents (represented by the $50\mu\text{A}$ base current in the figure), device recovery continues after one hour of thermal annealing and even begins to exceed the collector currents of the initial state. This is likely due to some thermal electron-hole pair generations. However, once the device is allowed to cool down, the I-V curves return to just below the healthy state at low base currents. At high base currents, the device continues to recover as it cools. Plots for the remaining base currents not pictured here are included in Figures A.25-A.32 in Appendix A.

4.1.3.3 PNP BJT Recovery

The final 10 Mrad exposed device thermally annealed was the PNP BJT. The same method was used as with the 10 Mrad exposed NPN BJT, with the exception that the experiment was concluded after 2.5 hours at 250°C due to observed damage of the IC clips used to connect the transistor to the semiconductor parametric analyzer. Figure 4.8 shows the recovery results for this PNP BJT at $500\mu\text{A}$ and $100\mu\text{A}$ base currents.

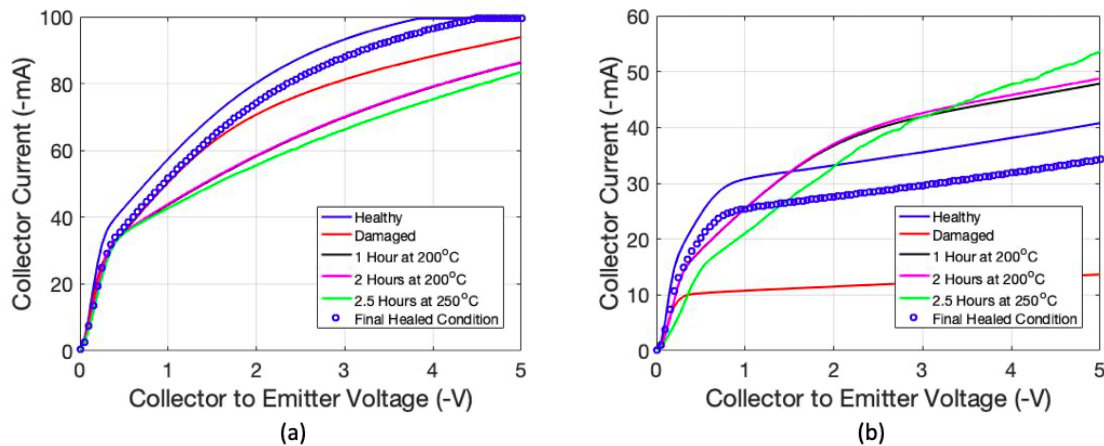


Figure 4.8. I_C versus V_{CE} characteristics at a $500\mu\text{A}$ base current (a) and $100\mu\text{A}$ base current (b) demonstrating device recovery for a PNP BJT after 10 Mrad gamma radiation exposure.

Figure 4.8 shows, for low base currents (represented by the $100\mu\text{A}$ base current in the figure), incremental recovery at each time interval and temperature increase occurred. However,

minimal device recovery occurs after the one hour time interval. Upon increasing the temperature to 250°C, it was observed the IC clips began to melt and started giving erratic measurements, such as the green line on the 100 μ A base current in the figure. At this point, the cooling process was initiated by lowering the hot plate temperature slowly to 0°C. Interestingly, and counter to what is observed for the NPN transistor, at high base currents (greater than 350 μ A) the device appears to become unhealthier as the temperature is increased. However, upon cooldown, significant recovery is observed. This relaxing behavior is also observed at low base currents when the curves lower to near pre-irradiation levels. Plots for the remaining base currents not pictured here are included in Figures A.33-A.40 in Appendix A.

Based on the above measurements taken for the BJTs, the suggested protocol to obtain the best device recovery is a progressive heating of the device, followed by a continuous 2-hour annealing period at 200°C, followed by a progressive cooling of the device to room temperature. More specifically, the progressive heating period should be 20-minutes and the cooling period should be 30-minutes. The additional cooling time allows for a 10-minute time period while the device is completely off the hot-plate to allow it to return to room temperature. This heating and cooling of the device should be accomplished by increasing (or decreasing for cooling) the temperature in 50°C increments every 5 minutes until the target temperature is achieved. This is represented graphically in Figure 4.9.

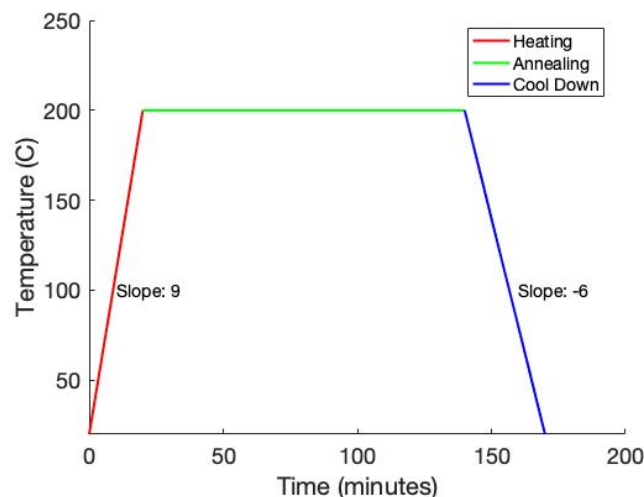


Figure 4.9. Suggested annealing protocol to achieve best device recovery.

4.2 Finite Element Model Results

The finite element model results are discussed in this section. This begins with a discussion of temperatures achieved using different heater materials and thickness dimensions. The later portion of the section discusses model outputs when adding additional features to the ceramic package, including a ceramic lid, an additional heater, a transistor, and a thermally conductive epoxy.

4.2.1 Heater Materials and Thickness

Using the developed model, the first parameter addressed is micro-heater material, specifically, the impact of heater material on the temperatures achieved by the heater at given voltages. In addition to gold, aluminum and tungsten are chosen as materials for comparison. Aluminum was selected since it is among the most common materials used in Micro-Electronic Mechanical Systems (MEMS) [14]. Likewise, tungsten was chosen due to its use in previous NASA experimental and modeling efforts involving self-healing electronics [13]. To model the effects of these materials on micro-heater temperatures, the micro-heater material in the finite element model was changed to aluminum (and then tungsten) and then a parametric sweep was executed across terminal voltages ranging from 0 to 2.5 volts. Figure 4.10 shows the results of this simulation.

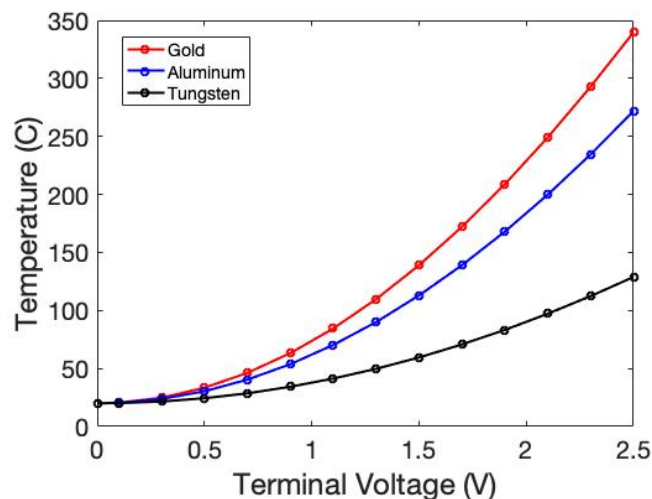


Figure 4.10. Temperature vs. terminal voltage for gold, aluminum, and tungsten micro-heaters.

From Figure 4.10, it is observed that as the voltage increases, the temperature of the micro-heater increases exponentially for all materials. This is the same behavior observed in Chapter 3 as the current was increased. Also, the model results show that gold achieves the highest temperatures of the three materials at a given voltage, followed by aluminum and tungsten, respectively. This justifies the use of gold, when compared to aluminum and tungsten, as a material of choice for the annealing micro-heater. This result is in accordance to the physical equations for conductivity and Joule heating discussed in Chapter 2. Gold, aluminum, and tungsten have thermal conductivities of $317 \frac{W}{mK}$, $237 \frac{W}{mK}$, and $175 \frac{W}{mK}$, respectively [21]. From Equation 2.1, a higher conductivity implies a lower resistivity, and consequently, lower resistance. Furthermore, lower resistance implies a greater dissipated power at a given voltage, as governed by Equation 2.10. Therefore, more heat is generated (Equation 2.12). This explains why tungsten, with the lowest thermal conductivity, produces the lowest temperatures at a given voltage.

The next parameter addressed using the micro-heater model is the impact of micro-heater thickness, specifically the rectilinear layer, on the temperatures achieved at a given voltage. This was required due to difficulties in measuring the thickness experimentally due to the presence of various adhesion and electrical/thermal isolation layers of unknown thickness. This was accomplished through executing a parametric sweep of heater thicknesses ranging from $0.5\mu m$ to $5\mu m$ at terminal voltages of 1V, 2V, and 3V. All other dimensions were kept fixed. Figure 4.11 shows the relationship between micro-heater thickness and the temperature achieved by the heater.

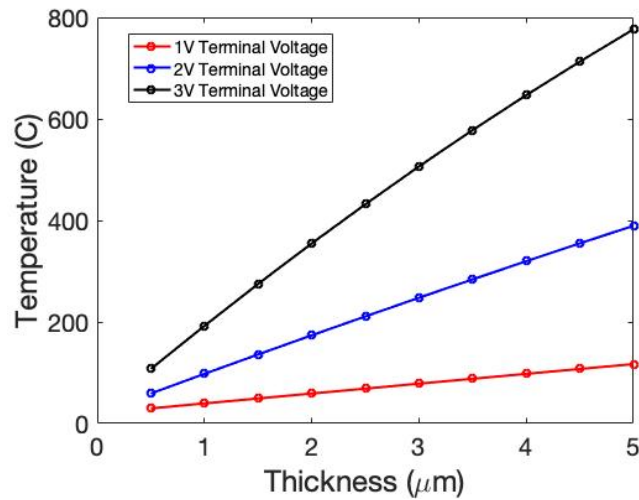


Figure 4.11. Temperature vs. micro-heater thickness at terminal voltages of 1V, 2V, and 3V.

From Figure 4.11, it can be seen that as the heater thickness increases, the temperature achieved increases at each terminal voltage. This result is expected since as the thickness increases, the resistance decreases and, consequently, the dissipated power increases. The thickness of the heater must be balanced with weight and space considerations of the entire system. As discussed in Chapter 1, cost and weight are major factors for space systems and thus, the size of various components must be considered when designing the micro-heater.

4.2.2 Temperatures Achieved with a Ceramic Lid

Next, the temperatures achieved with the incorporation of a ceramic lid is discussed. Investigating the use of a package lid is important as a lid can serve as a platform for a micro-heater to be printed on and integrated within the system. The dimensions for ceramic packages from Spectrum Semiconductor were measured using a micrometer gauge and, using these dimensions, a lid was built into the model. Additionally, instead of measuring the temperature of the heater, the temperature of the surrounding air around the heater was investigated. This is more important because the area immediately around the heater is where electronic components (such as BJTs and FETs) can be located and thermally annealed. Figure 4.12 shows how the lid was incorporated into the model with the lid depicted both transparently and as it would look in reality.

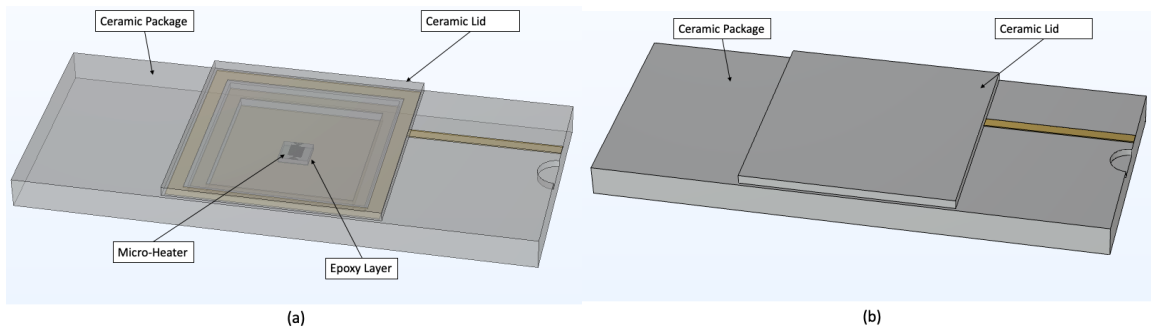


Figure 4.12. Model of micro-heater on package concept with a ceramic lid (a) and with the lid not set to transparent view (b).

Using this updated model geometry, simulations were run to determine the impact of the lid on the temperature achieved. Figure 4.13 shows the average temperature of the air surrounding the heater for the case of no lid versus the package having a lid. From Figure 4.13, it is observed that the temperature of the surrounding air is greater for the package with the ceramic lid. This supports the use of a ceramic lid in that it is useful for achieving the higher temperatures required for device recovery via thermal annealing.

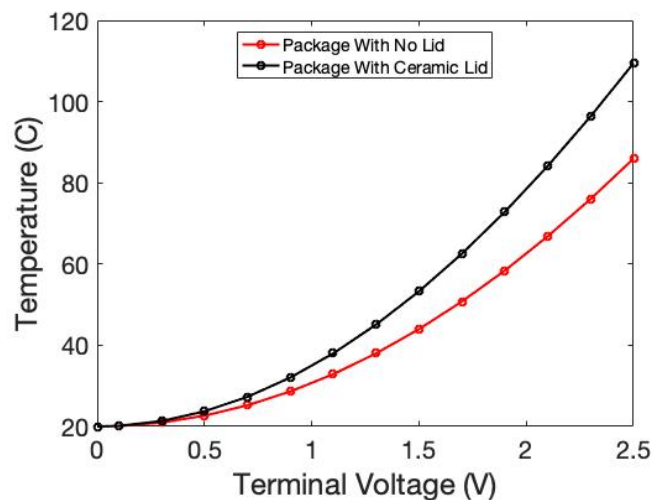


Figure 4.13. Temperature of surrounding air vs. terminal voltage for a ceramic package with and without a ceramic lid.

4.2.3 Temperatures Achieved with an Additional Heater

From the above analysis, the average temperature of the surrounding areas on a ceramic package was found. However, as seen in Figure 4.13, the temperature achieved with a ceramic lid at 2.5V was approximately 110°C, which is well below the target annealing temperature of 200°C used in the experimental efforts discussed earlier. Therefore, two options are available, the voltage can be increased or an additional heater can be added to the package. The latter option, adding an additional heater, is explored here. This was done in the model by simply duplicating the heater design and adding it onto the package near the first heater. Figure 4.14 shows how the additional heater was incorporated into the model.

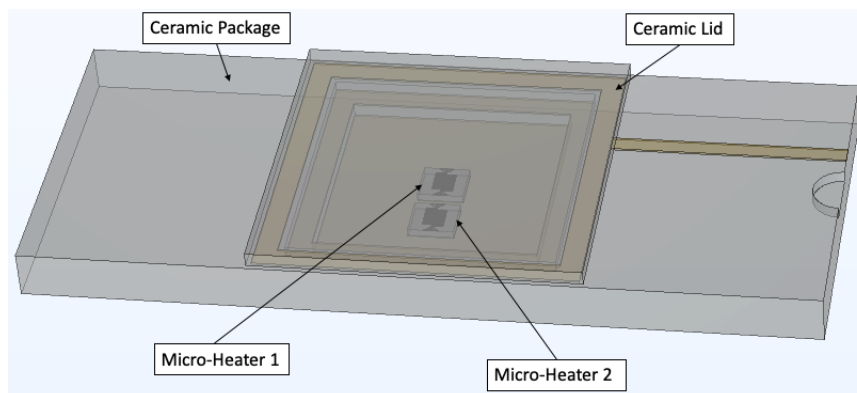


Figure 4.14. Model of two heaters on a ceramic package with a lid.

After adding terminal voltage and ground nodes to the second heater, simulations were run to see the temperatures achieved by the surrounding air, as seen in Figure 4.15. From Figure 4.15 it is clear that, as expected, the surrounding air temperature is higher with two heaters than with just one. In fact, the temperature now reaches 190°C, which is close to the 200°C target annealing temperature. To break the 200°C barrier, final changes are made to the model as discussed in the next section.

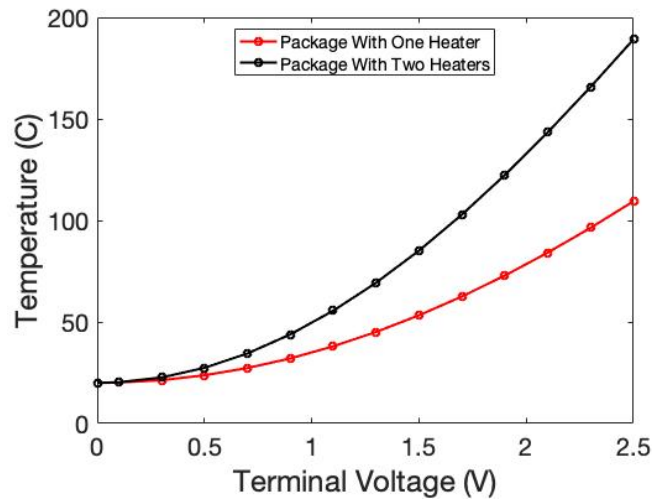


Figure 4.15. Temperature of surrounding air vs. terminal voltage for one heater and two heaters on ceramic package with lid.

4.2.4 Temperatures Achieved Using a Thermally Conductive Epoxy

The final application of the model is to explore the effects on temperature of changing the epoxy used to fasten the heaters to the ceramic package. Furthermore, instead of modeling the surrounding air temperature, the model was adapted to model the temperatures attained by a transistor on the ceramic package in the vicinity of the heater. This was done through building a block of silicon near the heater to the dimensions stated in the NPN transistor data-sheet. Simulations were run for both cyanoacrylate (used experimentally) as well as a thermally conductive epoxy available from Digikey Electronics [28] as the epoxy used to fasten the heater and transistor to the base of the package. The heaters and transistor were also connected to each-other along the base of the package via the epoxy. Figure 4.16 shows how the transistor was incorporated into the models using one heater and two heaters.

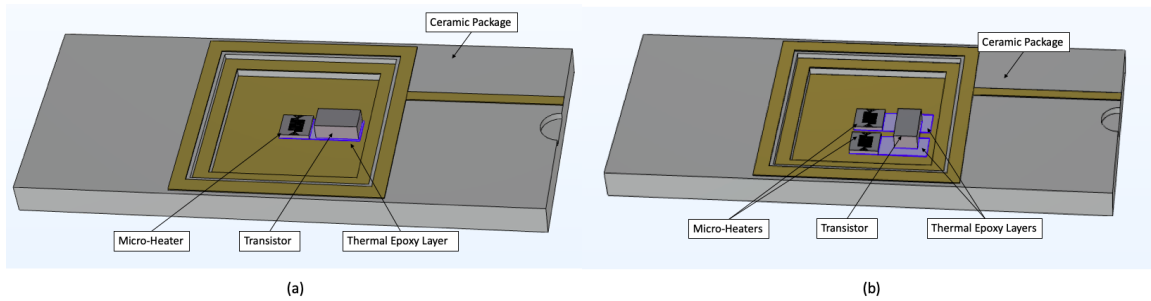


Figure 4.16. Models of one heater (a) vs. two heaters (b) and a transistor connected via a thermally conductive epoxy on a ceramic package.

The temperatures achieved by the transistor using this model are shown in Figure 4.17. As shown in Figure 4.17, the transistor achieves slightly higher temperatures when the thermally conductive epoxy is used when compared to cyanoacrylate. This is primarily due to the thermally conductive epoxy having a higher thermal conductivity ($1.40 \frac{W}{mK}$) than the cyanoacrylate ($0.11 \frac{W}{mK}$). A higher thermal conductivity means more energy is transferred in the form of heat from the heater to the transistor, as governed by Equations 2.4 and 3.2. Therefore, more heat is transferred from the heater element to the transistor through the thermally conductive epoxy than in the case using cyanoacrylate. This allows the system to achieve above the desired annealing temperature of $200^{\circ}C$ using two heaters with terminal voltages higher than $2V$.

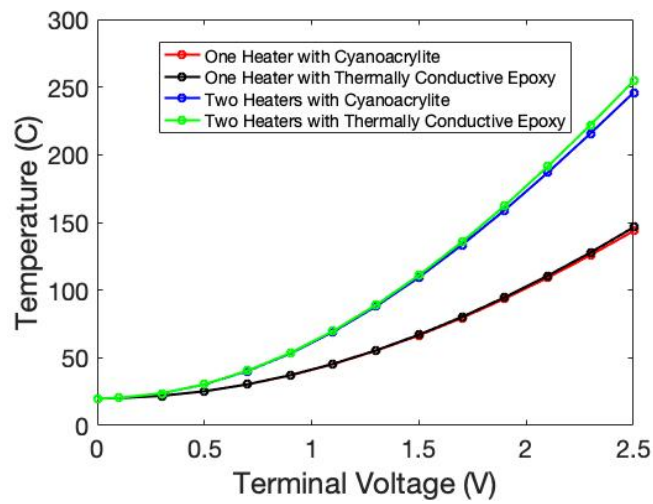


Figure 4.17. Temperature achieved for a transistor with different number of heaters and different epoxies bonding components to the ceramic package.

CHAPTER 5:

Conclusion

5.1 Conclusions

This research used experimentation and finite element modeling to explore the foundations of self-healing technology for space applications. Experimentally, transistors commonly found in electronic devices were exposed to gamma radiation sources and subsequently damaged. These transistors were then thermally annealed using a hot-plate in the laboratory to recover, to the greatest extent possible, their initial device characteristics. Using an iterative process, an annealing protocol was developed to achieve the maximum recovery possible. On the modeling side, an annealing micro-heater was built using COMSOL Multiphysics® based on a NASA micro-heater design from their previous work. The model was validated experimentally by measuring the temperatures achieved by the NASA heater at various input currents and comparing these results to those produced by the model. The model was then used to analyze the impact of various heater parameters and design configurations on the temperatures achieved. Device add-on features, including a ceramic lid, additional heaters, a transistor, and thermal epoxy were also investigated to determine the configuration to best achieve the desired annealing temperatures for device recovery.

Several conclusions are drawn from the experimental results. Through the experimental efforts, the concept of device recovery via thermal annealing is proven for BJTs. This is demonstrated through their significant I-V characteristic recovery close to their original states. On the other hand, the FET transistors (at both 5 Mrad and 10 Mrad doses) did not heal to near their original I-V characteristics. However, the FET results might be inconclusive. To fully capture I-V characteristics for the FET used in this work, a maximum allowed current of 1000 mA is required on the parametric analyzer. Since the parametric analyzer used in this work is limited to 100 mA, only the linear region of the FETs was captured. By not capturing the full I-V characteristics for the FETs, their recovery results are inconclusive. That said, using the results from the BJTs, an annealing protocol is suggested. This includes a 20-minute progressive heating of the device, followed by annealing at a constant temperature of 200°C for 2 hours, followed by a progressive cool down of the device

for 30-minutes back to room temperature. This healing protocol is suggested due to the diminishing returns achieved after annealing for longer time periods at higher temperatures.

The key conclusions from the model are that, first, when looking at common material used in MEMS, gold appears to be best suited for self-healing electronics due to the high temperatures achieved at given voltages compared to aluminum and tungsten. Furthermore, the model shows that greater micro-heater thickness increases the temperature achieved, however, this must be balanced by the size and weight constraints of the system. Also, higher thicknesses above those modeled in this work may eventually cause the maximum temperature achieved to drop as thermal mass increases. Another key conclusion from the model is that, if possible, a ceramic lid and multiple heaters should be incorporated to increase the temperature of the regions surrounding the heater. These higher temperatures will allow electronic components to reach the desired annealing temperature of 200°C. Finally, when possible, thermally conductive epoxy should be used in lieu of cyanoacrylate to fasten components to the package due to its higher thermal conductivity and subsequent higher temperatures achieved by nearby devices.

In summary, this work achieved the research objectives outlined in Chapter 1. Not only was device damage via radiation and subsequent recovery of BJTs via thermal annealing proven, but an annealing protocol was developed to achieve the best recovery results. Furthermore, after some adjustments, the annealing micro-heater created in COMSOL Multiphysics® demonstrated the same current vs. temperature behavior as heaters created by NASA. The model was then used to explore device parameters and add-on features to maximize performance. This work can have a significant impact on the Department of Defense (DoD). The DoD recently created a new service branch, the U.S. Space Force, showing their increased interest in ensuring a presence in space. The foundations for self-healing technology explored in this thesis can be built upon and incorporated in future space systems to enhance the robustness of space electronics for future space missions.

5.2 Future Work

In this section, recommendations to further research on self-healing electronics is discussed. As described above, the FET recovery results using a hot-plate and parametric analyzer proved inconclusive. To obtain conclusive results, future work can use different FETs

whose complete I-V characteristics are captured within the 100 mA current limit of the parametric analyzer. Alternatively, threshold voltage or drain current versus gate voltage can be analyzed as alternative measures of device health if these characteristics fall within the limits of the parametric analyzer. If future work is done using BJTs, a maximum total radiation dose of 5 Mrad will be sufficient as there is no significant further damage observed between 5 Mrad and 10 Mrad doses.

Besides transistors, future work can investigate the recovery of more complex electronics that suffer radiation damage. Logic devices, such as NAND or NOR gates and flip flops, are examples of electronics that are widely used in digital circuits and should be considered. As opposed to analyzing I-V characteristics, as was done with the transistors in this work, the actual functionality of the logic devices can be used as the standard for device health. Additionally, future work should look at the device's ability to recover at lower radiation doses. While the results from the BJTs in this work are promising, they did not achieve complete recovery (recovery was limited to approximately 90%). Future work should explore the effects of exposing electronics to a lower radiation doses and, subsequently, determine if they can achieve 100% recovery using the annealing protocols discussed in this work.

Future work should also explore micro-heater design and fabrication. Heater designs can be modeled using the same methods in this work and then printed directly on ceramic lids using a Voltera printer at NPS. The Voltera printer uses thermally conductive ink through which current can flow to heat up the ceramic package, air, and therefore the devices contained within. This system design, whereby the heater is located directly on the backside of a ceramic lid, can potentially negate the need for a micro-heater located on the package itself. If successful, this method could allow for more space on the package for other electronic components. These are all important steps that can continue to drive self-healing technology forward and, eventually, culminate in flight tests of a complete self-healing system in the space environment.

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APPENDIX A: Device Recovery Plots

A.1 Device Recovery for 5 Mrad Exposed Devices

A.1.1 PNP BJT

The below figures show device recovery at the base currents not shown in Chapter 4 for the 5 Mrad exposed PNP BJT.

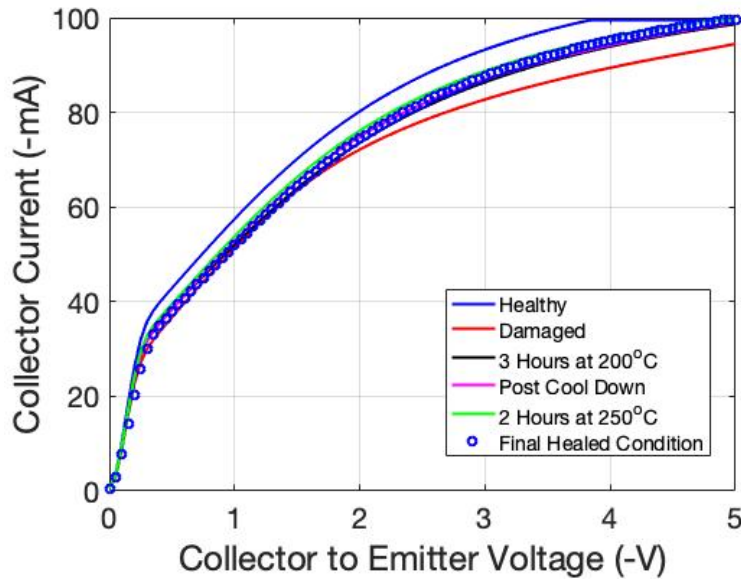


Figure A.1. I_C versus V_{CE} characteristics at a $500\mu A$ base current for a PNP BJT after 5 Mrad gamma radiation exposure and subsequent recovery.

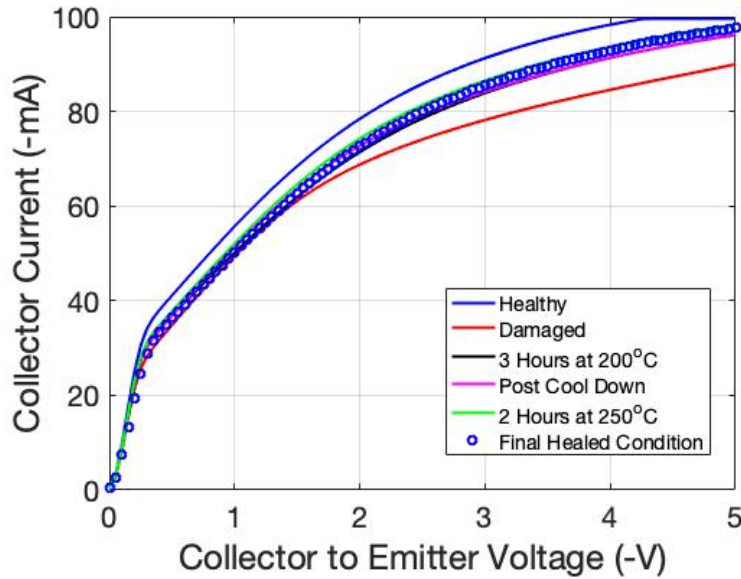


Figure A.2. I_C versus V_{CE} characteristics at a $450\mu A$ base current for a PNP BJT after 5 Mrad gamma radiation exposure and subsequent recovery.

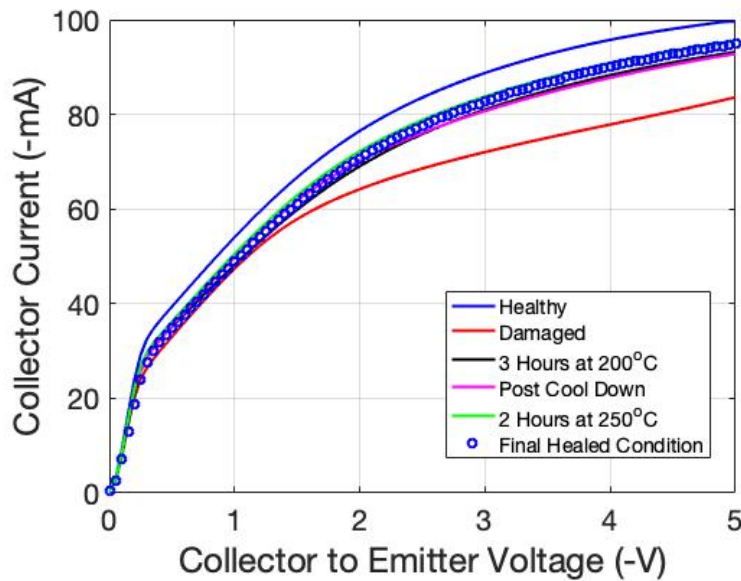


Figure A.3. I_C versus V_{CE} characteristics at a $400\mu A$ base current for a PNP BJT after 5 Mrad gamma radiation exposure and subsequent recovery.

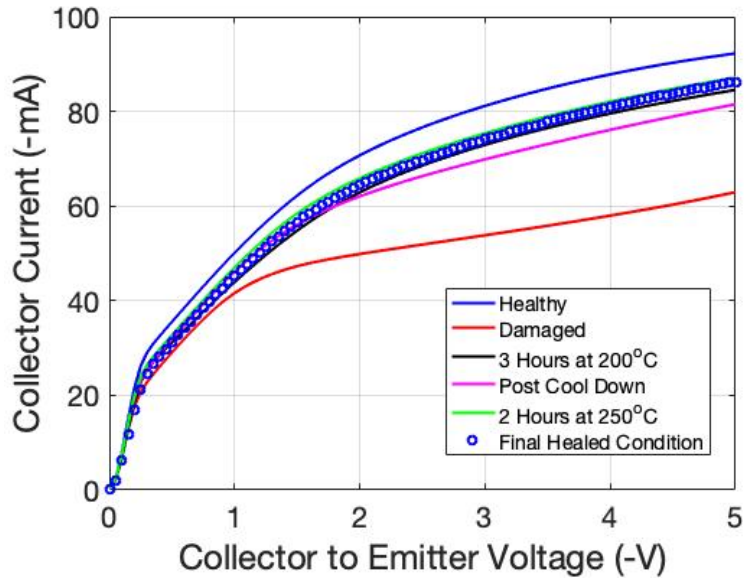


Figure A.4. I_C versus V_{CE} characteristics at a $300\mu A$ base current for a PNP BJT after 5 Mrad gamma radiation exposure and subsequent recovery.

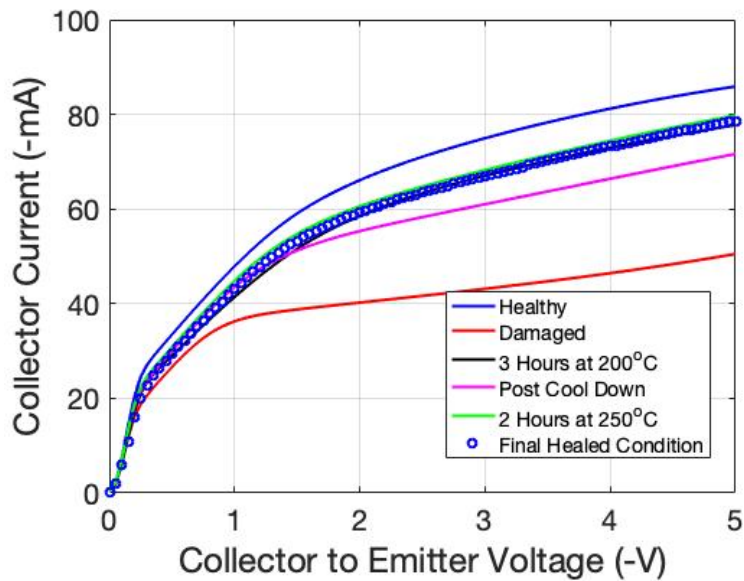


Figure A.5. I_C versus V_{CE} characteristics at a $250\mu A$ base current for a PNP BJT after 5 Mrad gamma radiation exposure and subsequent recovery.

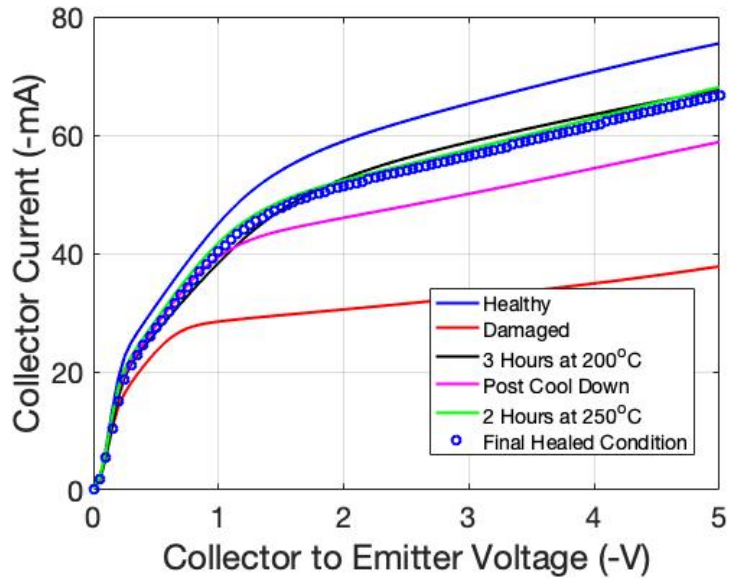


Figure A.6. I_C versus V_{CE} characteristics at a $200\mu A$ base current for a PNP BJT after 5 Mrad gamma radiation exposure and subsequent recovery.

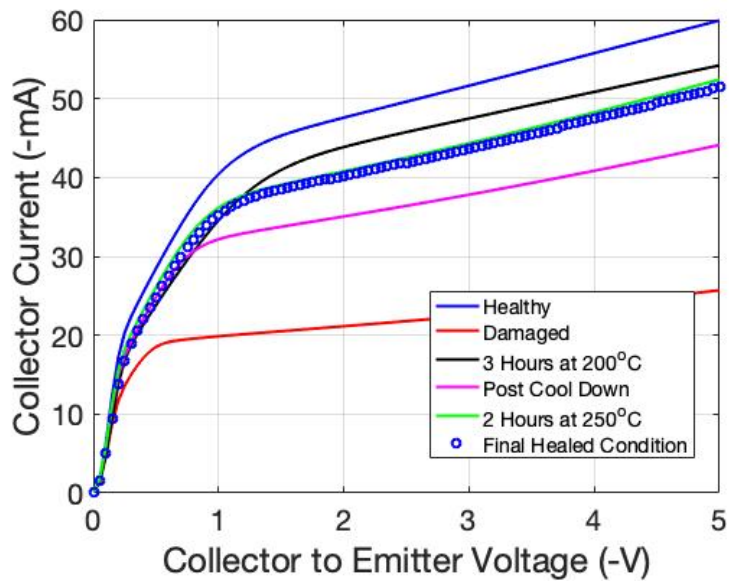


Figure A.7. I_C versus V_{CE} characteristics at a $150\mu A$ base current for a PNP BJT after 5 Mrad gamma radiation exposure and subsequent recovery.

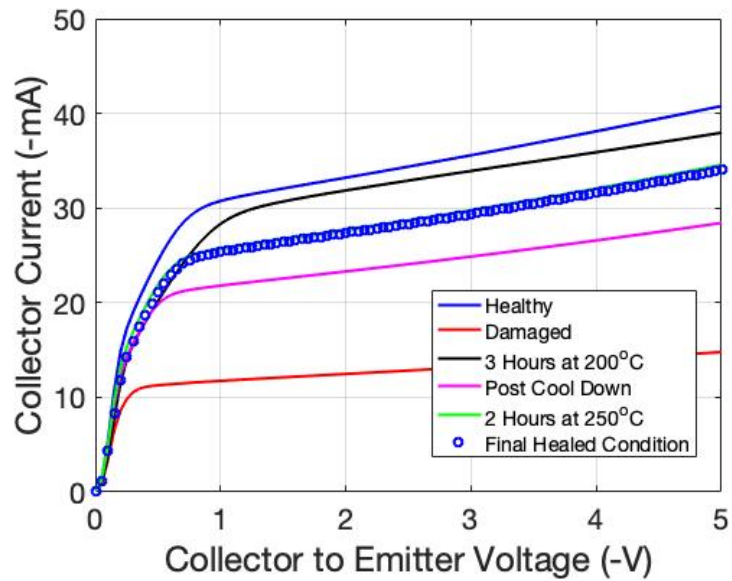


Figure A.8. I_C versus V_{CE} characteristics at a $100\mu A$ base current for a PNP BJT after 5 Mrad gamma radiation exposure and subsequent recovery.

A.1.2 FET

The below figures show device recovery at the GS voltages not shown in Chapter 4 for the 5 Mrad exposed FET.

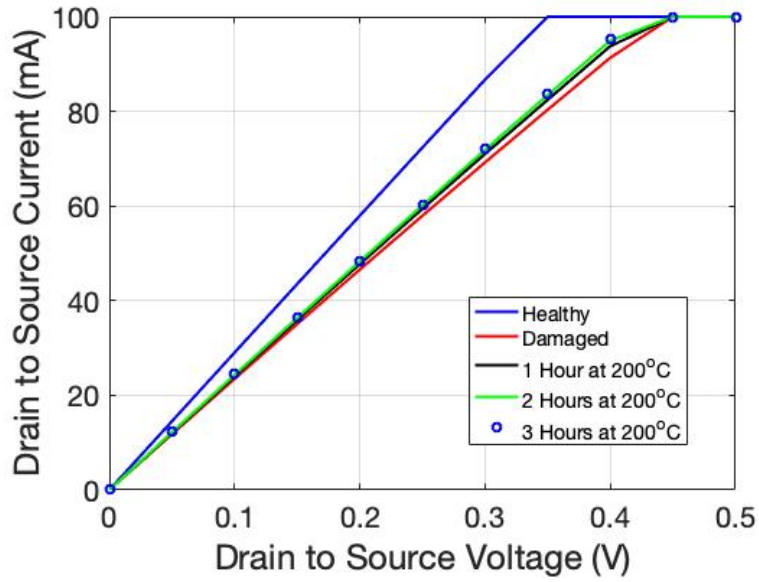


Figure A.9. I_{DS} versus V_{DS} characteristics at a 5V GS voltage for a FET after 5 Mrad gamma radiation exposure and subsequent recovery.

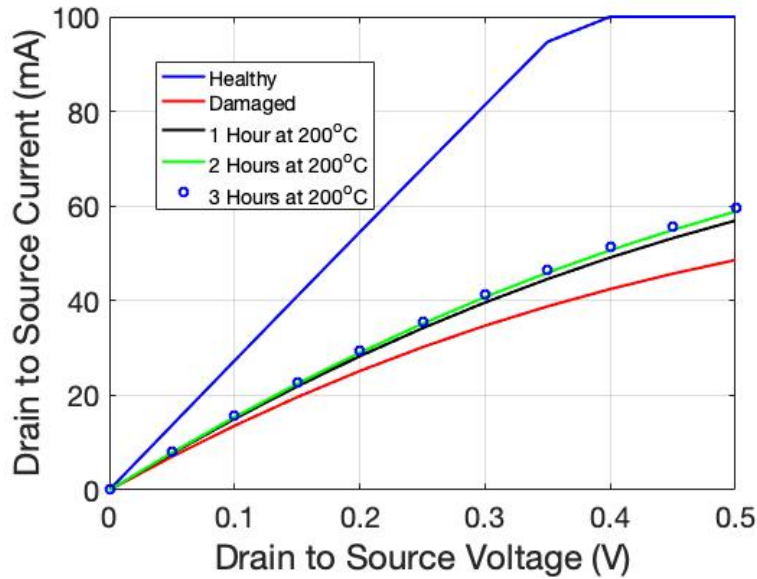


Figure A.10. I_{DS} versus V_{DS} characteristics at a 4V GS voltage for a FET after 5 Mrad gamma radiation exposure and subsequent recovery.

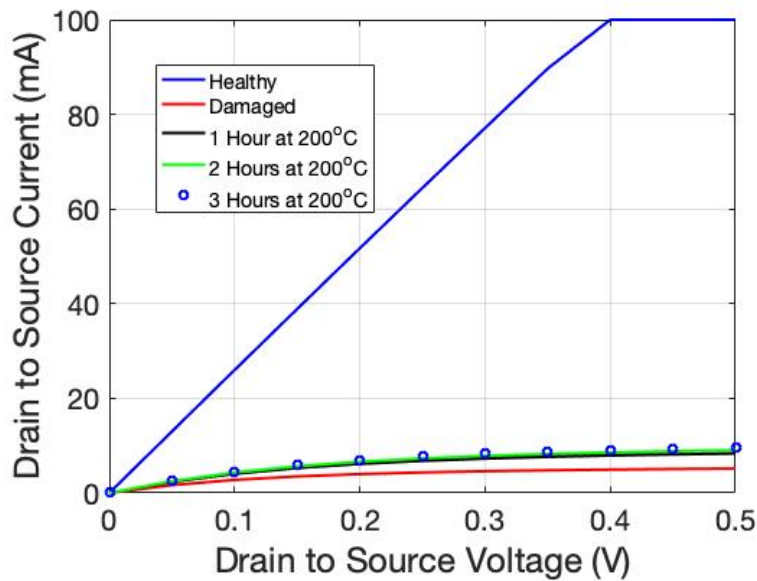


Figure A.11. I_{DS} versus V_{DS} characteristics at a 3.5V GS voltage for a FET after 5 Mrad gamma radiation exposure and subsequent recovery.

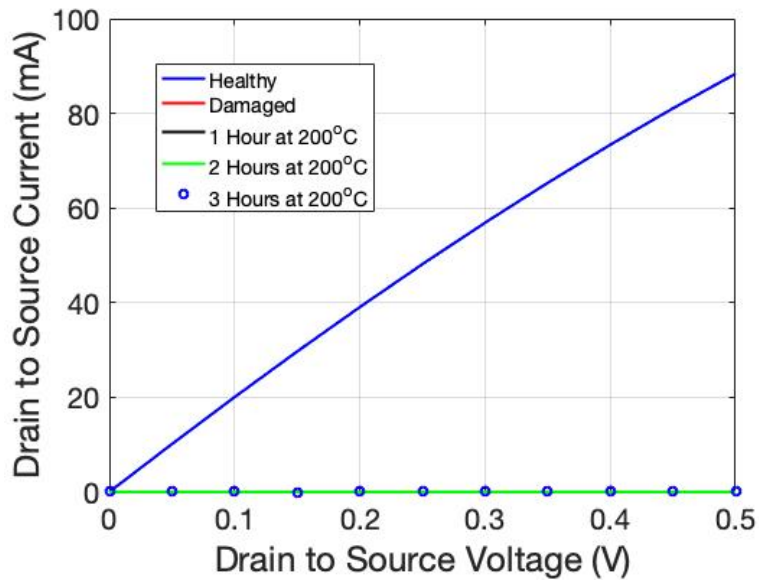


Figure A.12. I_{DS} versus V_{DS} characteristics at a 2.5V GS voltage for a FET after 5 Mrad gamma radiation exposure and subsequent recovery.

A.1.3 NPN BJT

The below figures show device recovery at the base currents not shown in Chapter 4 for the 5 Mrad exposed NPN BJT.

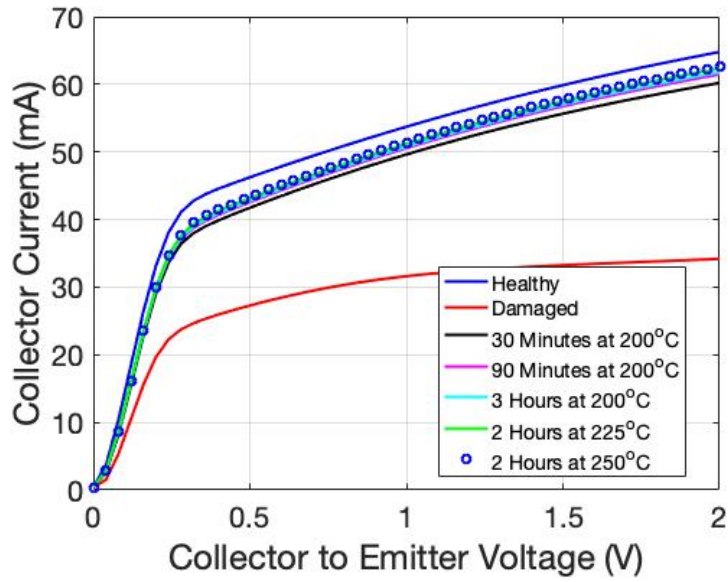


Figure A.13. I_C versus V_{CE} characteristics at a $450\mu A$ base current for a NPN BJT after 5 Mrad gamma radiation exposure and subsequent recovery.

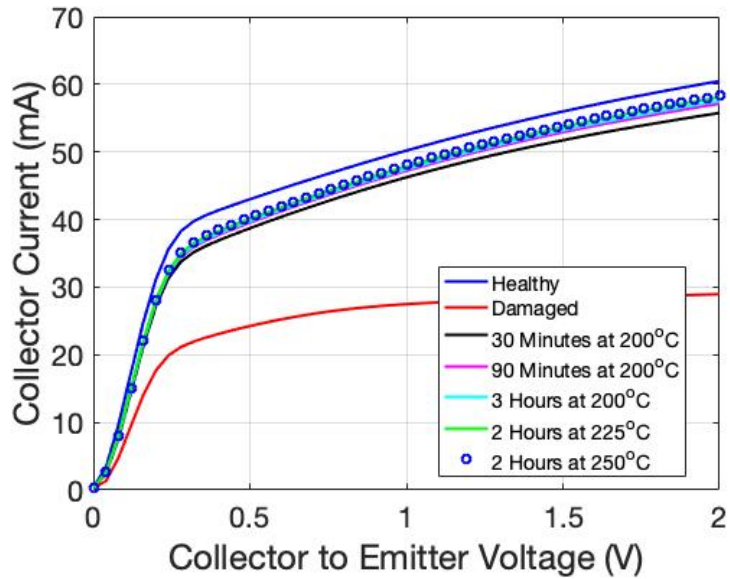


Figure A.14. I_C versus V_{CE} characteristics at a $400\mu A$ base current for a NPN BJT after 5 Mrad gamma radiation exposure and subsequent recovery.

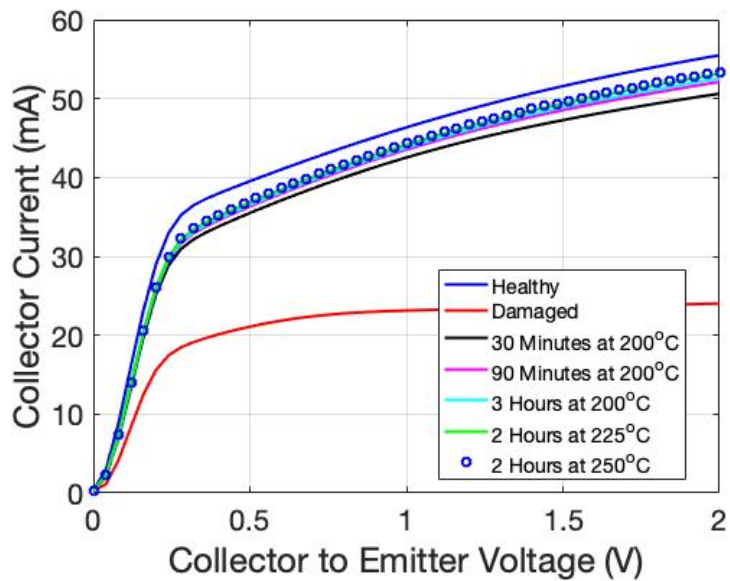


Figure A.15. I_C versus V_{CE} characteristics at a $350\mu A$ base current for a NPN BJT after 5 Mrad gamma radiation exposure and subsequent recovery.

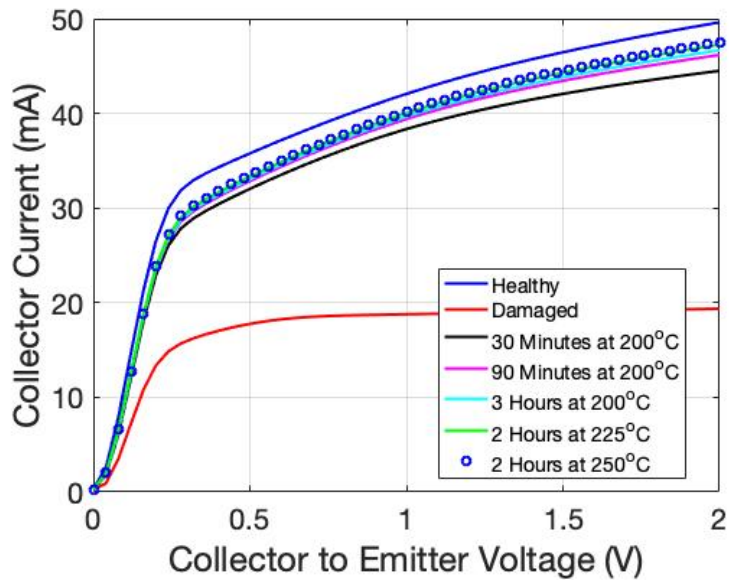


Figure A.16. I_C versus V_{CE} characteristics at a $300\mu A$ base current for a NPN BJT after 5 Mrad gamma radiation exposure and subsequent recovery.

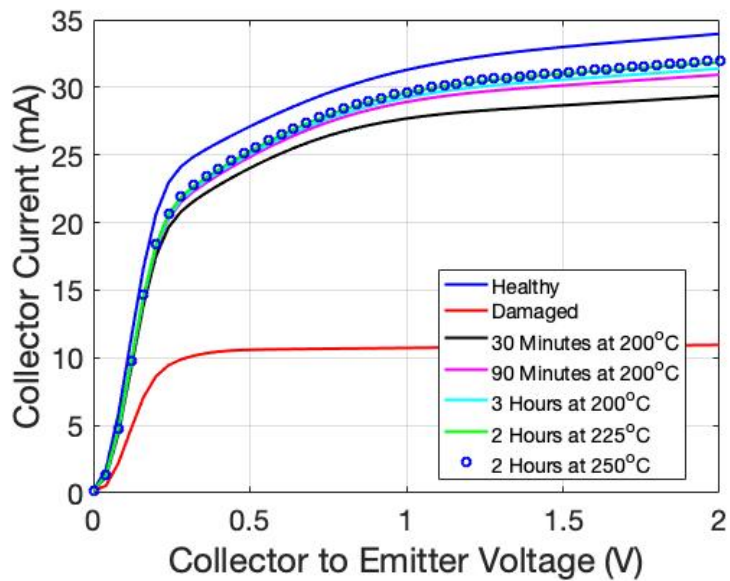


Figure A.17. I_C versus V_{CE} characteristics at a $250\mu A$ base current for a NPN BJT after 5 Mrad gamma radiation exposure and subsequent recovery.

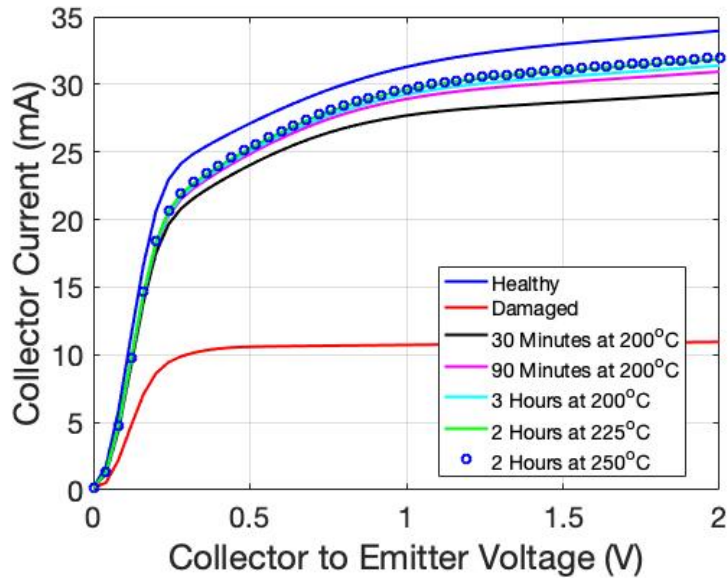


Figure A.18. I_C versus V_{CE} characteristics at a $200\mu A$ base current for a NPN BJT after 5 Mrad gamma radiation exposure and subsequent recovery.

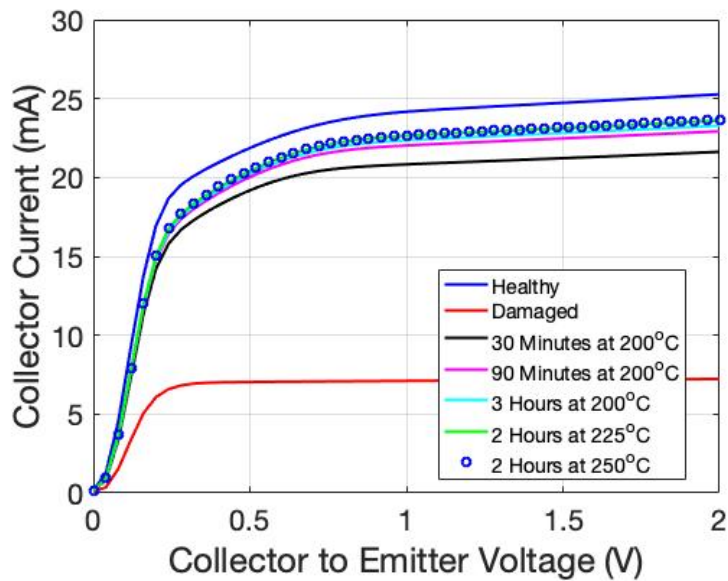


Figure A.19. I_C versus V_{CE} characteristics at a $150\mu A$ base current for a NPN BJT after 5 Mrad gamma radiation exposure and subsequent recovery.

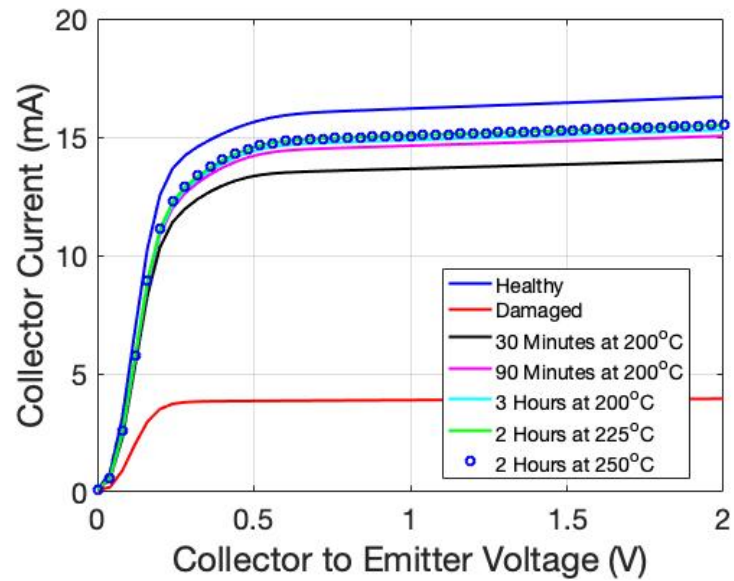


Figure A.20. I_C versus V_{CE} characteristics at a $100\mu A$ base current for a NPN BJT after 5 Mrad gamma radiation exposure and subsequent recovery.

A.2 Device Recovery for 10 Mrad Exposed Devices

A.2.1 FET

The below figures show device recovery at the base currents not shown in Chapter 4 for the 10 Mrad exposed FET.

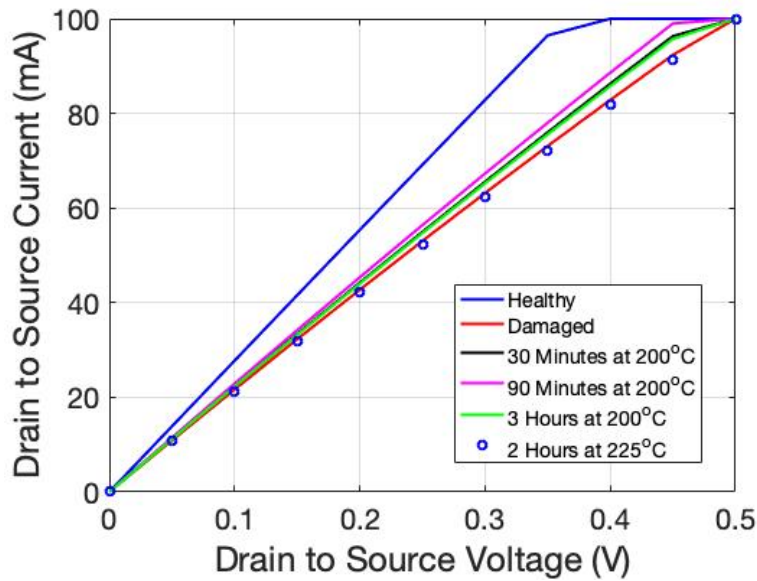


Figure A.21. I_{DS} versus V_{DS} characteristics at a 5V GS voltage for a FET after 10 Mrad gamma radiation exposure and subsequent recovery.

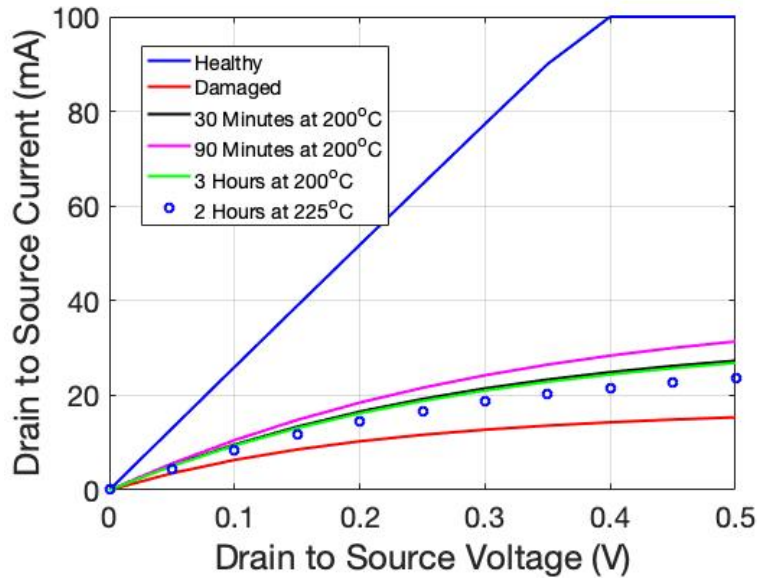


Figure A.22. I_{DS} versus V_{DS} characteristics at a 4V GS voltage for a FET after 10 Mrad gamma radiation exposure and subsequent recovery.

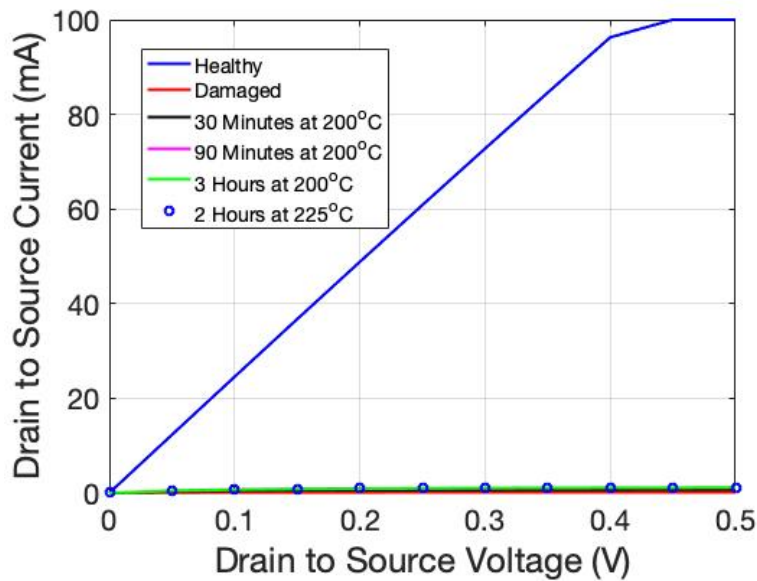


Figure A.23. I_{DS} versus V_{DS} characteristics at a 3.5V GS voltage for a FET after 10 Mrad gamma radiation exposure and subsequent recovery.

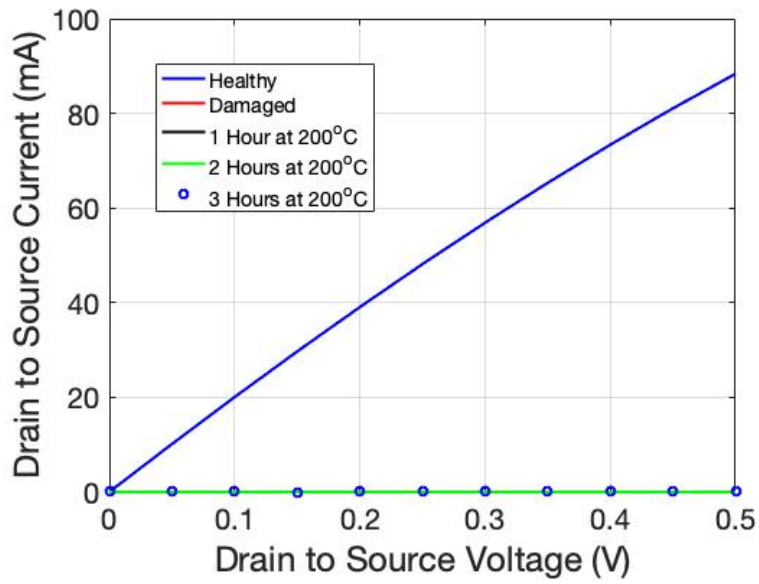


Figure A.24. I_{DS} versus V_{DS} characteristics at a 2.5V GS voltage for a FET after 10 Mrad gamma radiation exposure and subsequent recovery.

A.2.2 NPN BJT

The below figures show device recovery at the GS voltages not shown in Chapter 4 for the 10 Mrad exposed NPN BJT.

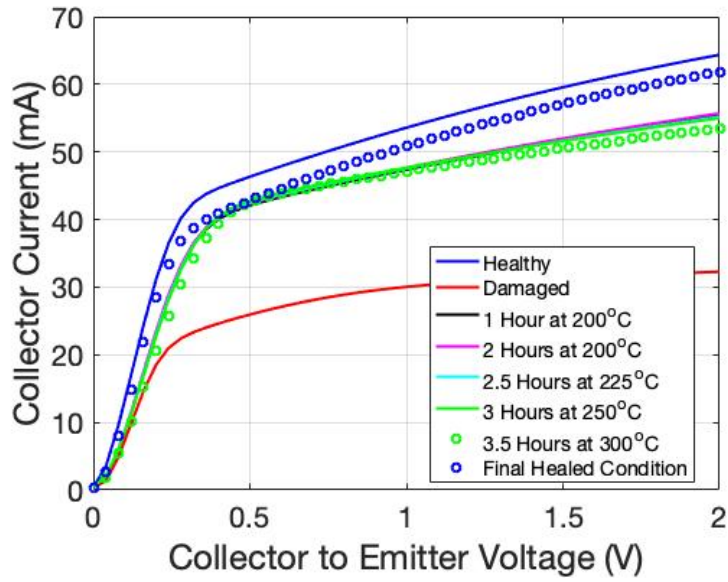


Figure A.25. I_C versus V_{CE} characteristics at a $450\mu A$ base current for a NPN BJT after 10 Mrad gamma radiation exposure and subsequent recovery.

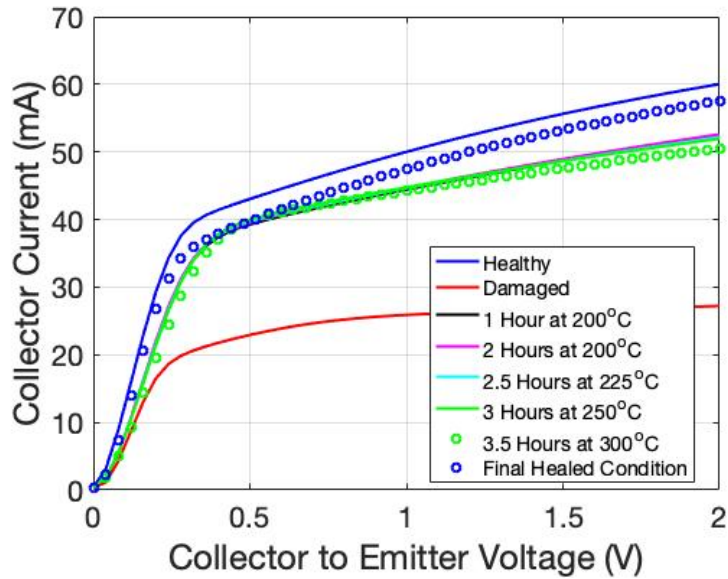


Figure A.26. I_C versus V_{CE} characteristics at a 400 μA base current for a NPN BJT after 10 Mrad gamma radiation exposure and subsequent recovery.

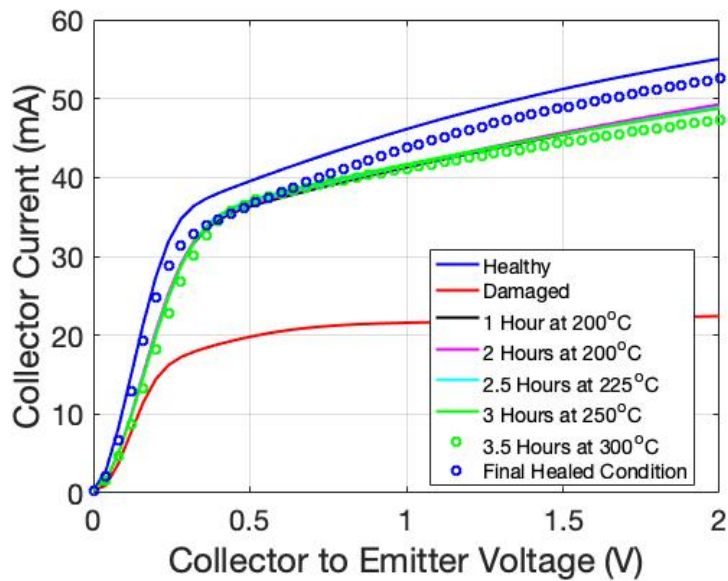


Figure A.27. I_C versus V_{CE} characteristics at a 350 μA base current for a NPN BJT after 10 Mrad gamma radiation exposure and subsequent recovery.

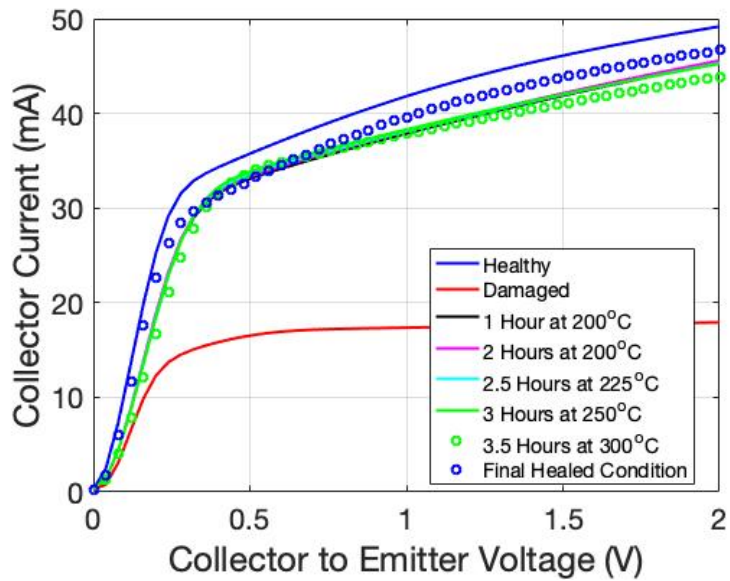


Figure A.28. I_C versus V_{CE} characteristics at a $300\mu A$ base current for a NPN BJT after 10 Mrad gamma radiation exposure and subsequent recovery.

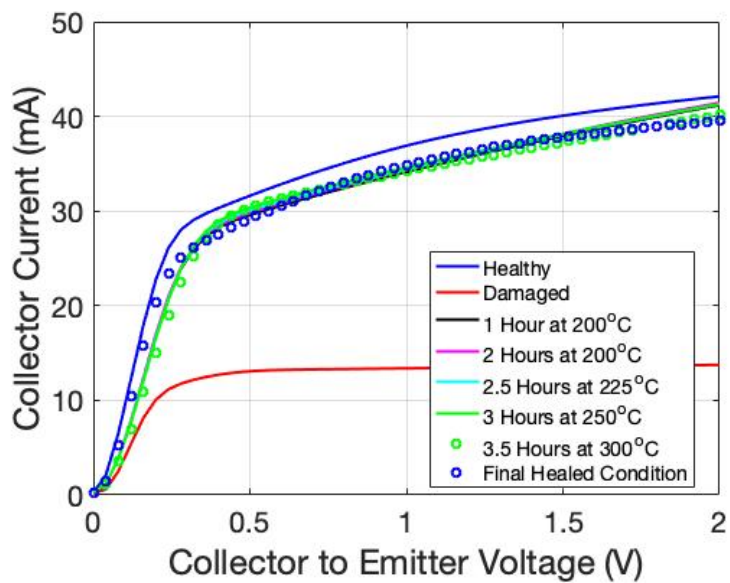


Figure A.29. I_C versus V_{CE} characteristics at a $250\mu A$ base current for a NPN BJT after 10 Mrad gamma radiation exposure and subsequent recovery.

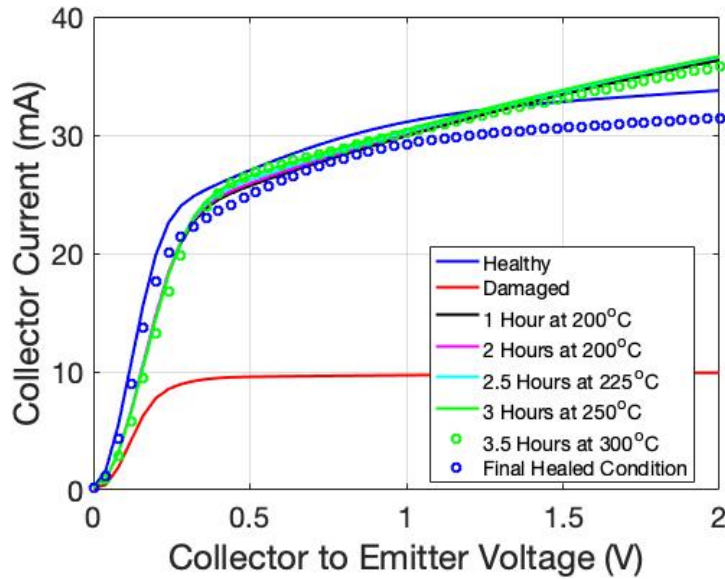


Figure A.30. I_C versus V_{CE} characteristics at a $200\mu A$ base current for a NPN BJT after 10 Mrad gamma radiation exposure and subsequent recovery.

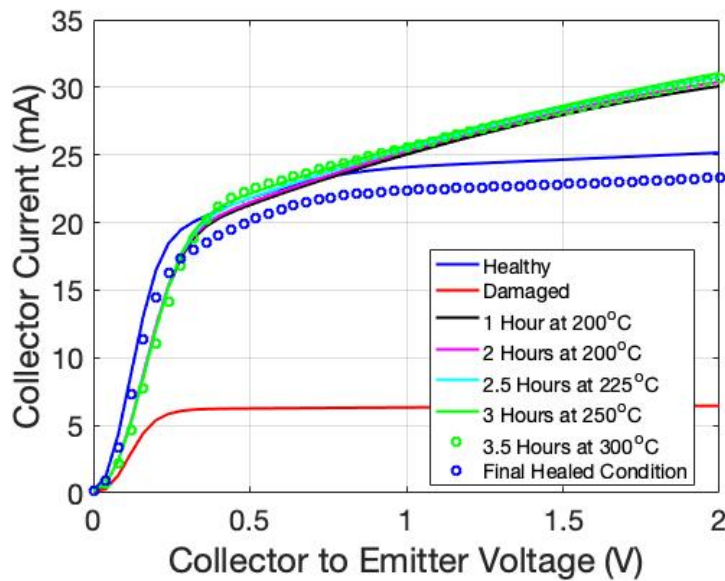


Figure A.31. I_C versus V_{CE} characteristics at a $150\mu A$ base current for a NPN BJT after 10 Mrad gamma radiation exposure and subsequent recovery.

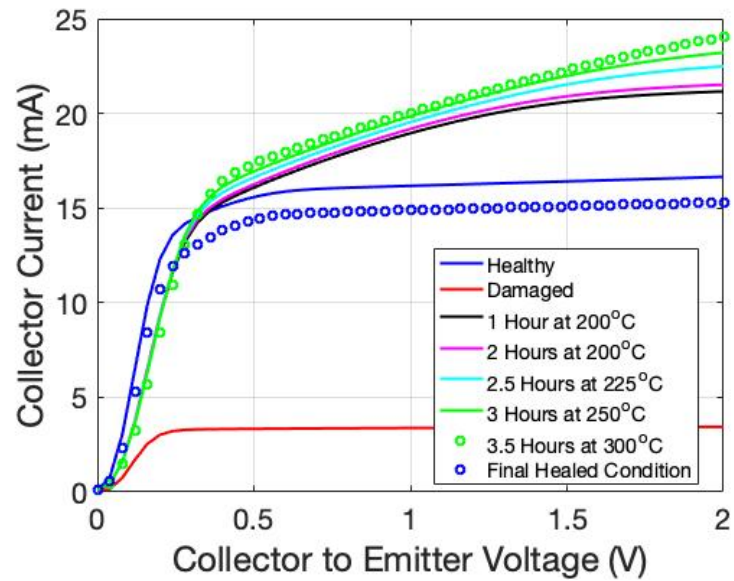


Figure A.32. I_C versus V_{CE} characteristics at a $100\mu A$ base current for a NPN BJT after 10 Mrad gamma radiation exposure and subsequent recovery.

A.2.3 PNP BJT

The below figures show device recovery at the base currents not shown in Chapter 4 for the 10 Mrad exposed PNP BJT.

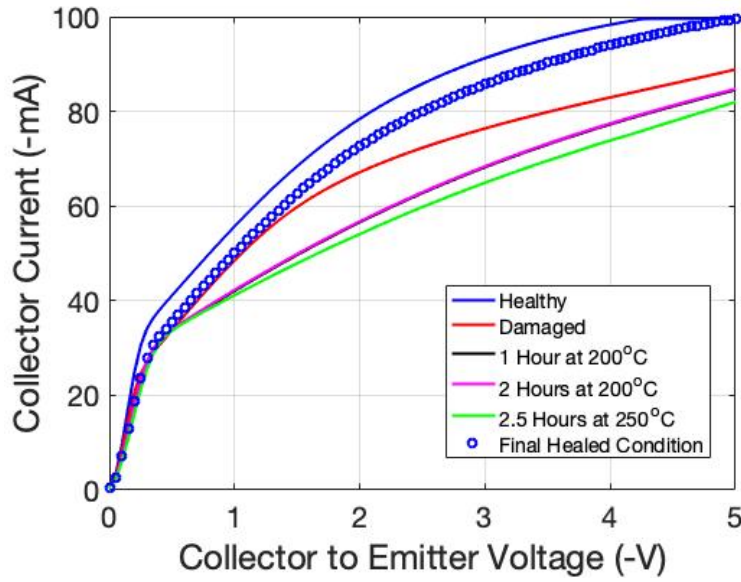


Figure A.33. I_C versus V_{CE} characteristics at a $450\mu A$ base current for a PNP BJT after 10 Mrad gamma radiation exposure and subsequent recovery.

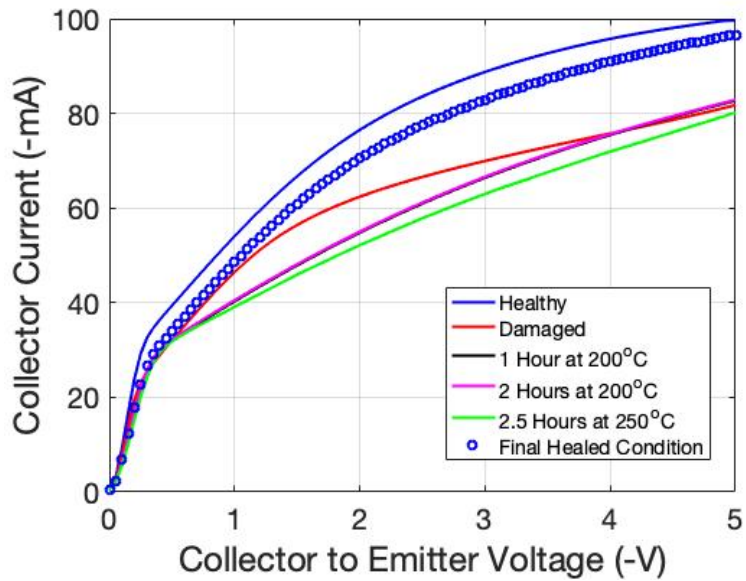


Figure A.34. I_C versus V_{CE} characteristics at a $400\mu A$ base current for a PNP BJT after 10 Mrad gamma radiation exposure and subsequent recovery.

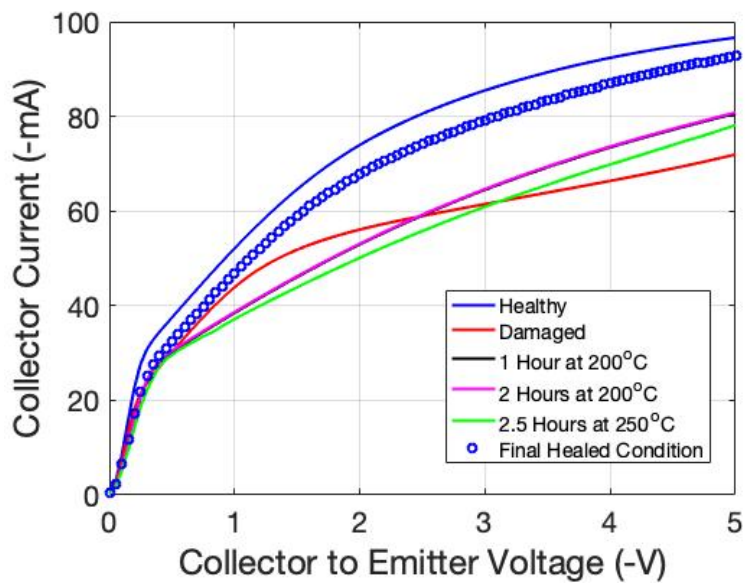


Figure A.35. I_C versus V_{CE} characteristics at a $350\mu A$ base current for a PNP BJT after 10 Mrad gamma radiation exposure and subsequent recovery.

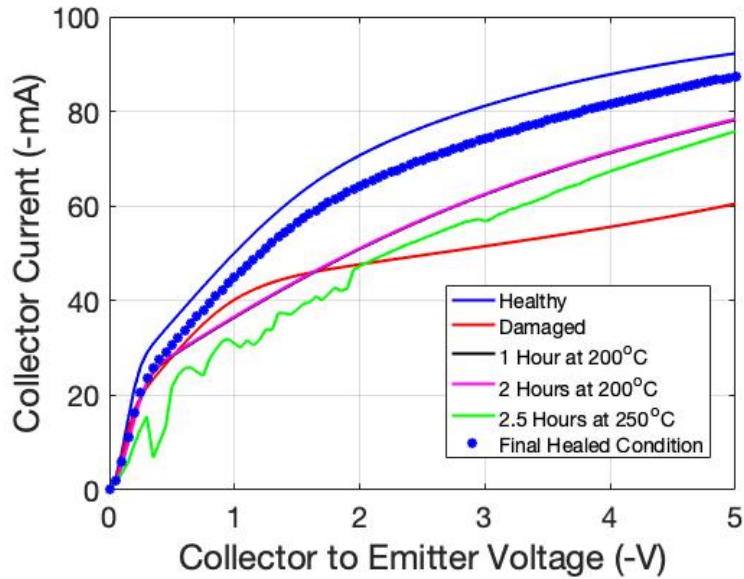


Figure A.36. I_C versus V_{CE} characteristics at a $300\mu A$ base current for a PNP BJT after 10 Mrad gamma radiation exposure and subsequent recovery.

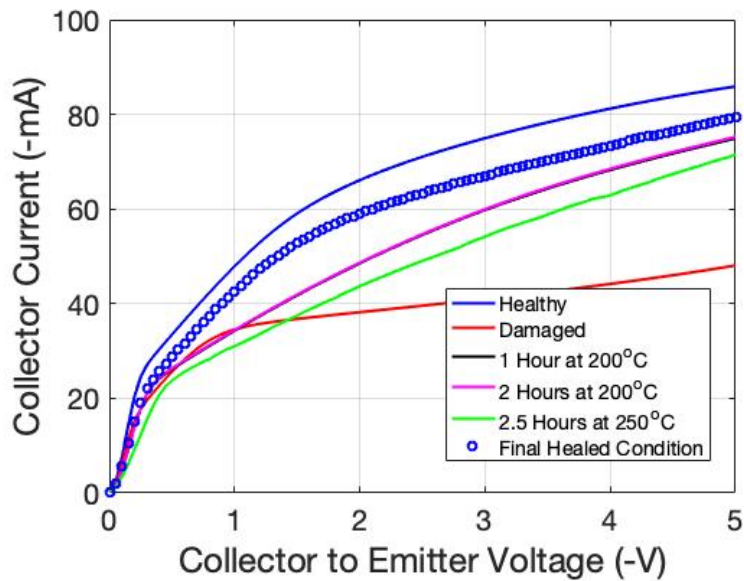


Figure A.37. I_C versus V_{CE} characteristics at a $250\mu A$ base current for a PNP BJT after 10 Mrad gamma radiation exposure and subsequent recovery.

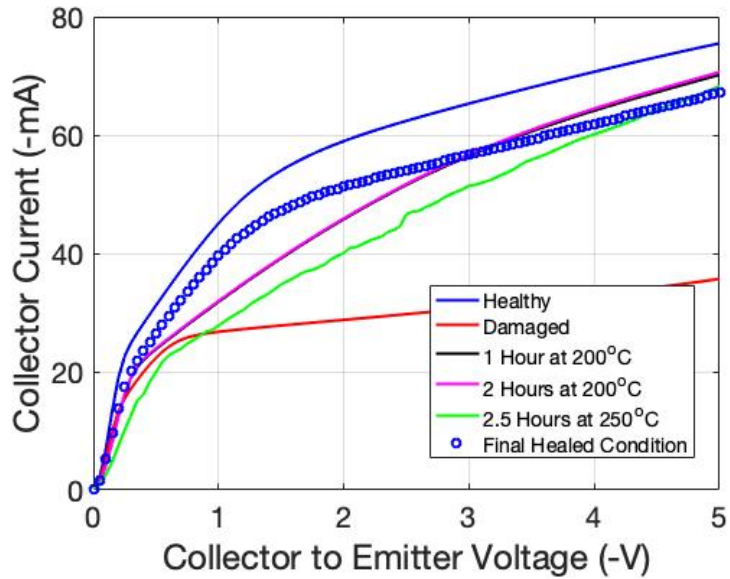


Figure A.38. I_C versus V_{CE} characteristics at a $200\mu A$ base current for a PNP BJT after 10 Mrad gamma radiation exposure and subsequent recovery.

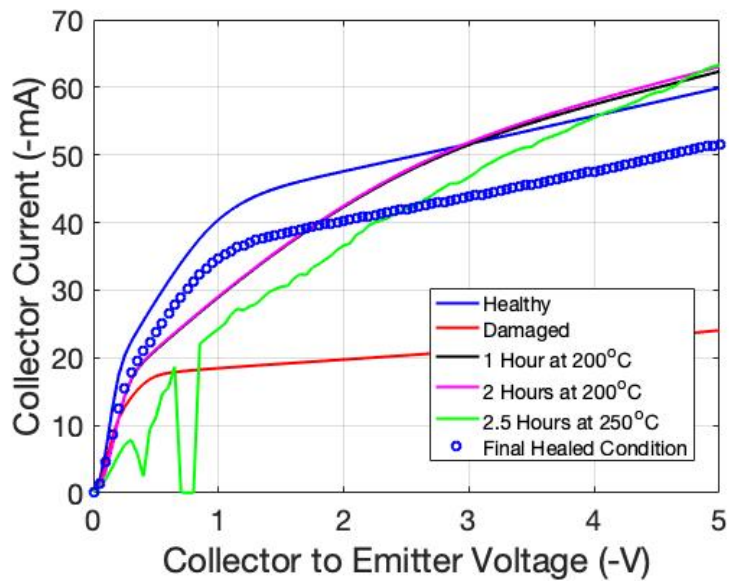


Figure A.39. I_C versus V_{CE} characteristics at a $150\mu A$ base current for a PNP BJT after 10 Mrad gamma radiation exposure and subsequent recovery.

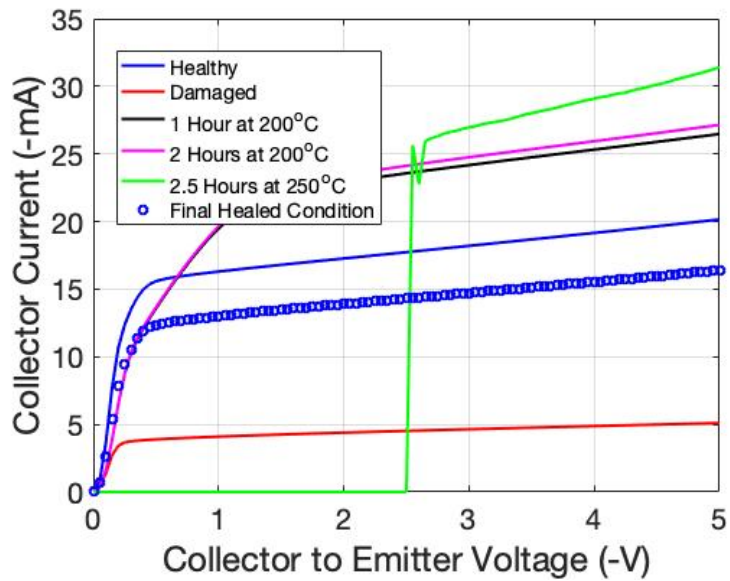


Figure A.40. I_C versus V_{CE} characteristics at a $50\mu A$ base current for a PNP BJT after 10 Mrad gamma radiation exposure and subsequent recovery.

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