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RADIATION EFFECTS ON MOSFET SEMICONDUCTOR DEVICES IN SUPPORT OF LEO OPERATIONS

by

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In this research, we exposed the Infineon BSC060N10NS3GATMA1 power metal oxide semiconductor field-effect transistor (MOSFET) to x-ray radiation and tested the device to failure by monitoring its voltage threshold. We found the MOSFET failed at approximately 7 krads under biased conditions versus 24 krads when held at ground (to simulate spare parts). Applying 2 mm of aluminum shielding to the MOSFET increased the survivability by roughly a factor of three. Based on the results from the radiation testing, we used the SPace ENVironment Information System (SPENVIS) to identify 5-year low Earth orbit (LEO) satellite orbits that would support the device's radiation tolerance. We recommend the Infineon power MOSFET be used for lower altitude LEO operations or shorter duration flights at higher LEO altitudes during solar minimum. Using SPENVIS, we did not observe a significant difference between the predicted total ionizing dose at solar minimum and maximum; however, further single event effect (SEE) testing needs to be completed to recommend the Infineon MOSFET during solar maximum when solar proton events reach their peak.

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RADIATION EFFECTS ON MOSFET SEMICONDUCTOR DEVICES IN SUPPORT OF LEO OPERATIONS

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LIST OF ACRONYMS AND ABBREVIATIONS

Al	aluminum
BJT	bipolar junction transistors
Co-60	Cobalt-60
CREME96	Cosmic Ray Effects on Micro-Electronics 1996
DC	direct current
DOD	Department of Defense
DUT	device under test
ESA	European Space Agency
ESD	electrostatic discharge
I_d	current drain
Km	kilometer
Krad	kilorad, unit of radiation
kVp	kilovolt peak
LEO	low Earth orbit
MOSFET	metal oxide semiconductor field-effect transistor
MPSMU	medium power source measure unit
PCB	printed copper board
PQFN	power quad flat no-lead
SEE	single event effect
Si	silicon
SMU	source measure unit
SPENVIS	SPace ENVironment Information System
TID	total ionizing dose
Vds	voltage drain to source
Vgs	voltage gate to source

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I. INTRODUCTION

A. PROBLEM STATEMENT

As the Department of Defense (DOD) and the intelligence community continue to leverage commercial satellites for imagery and communication, it is imperative to evaluate these systems down to the component level. Poor choices of electrical components, such as metal-oxide-semiconductor field-effect transmitters (MOSFETs), can affect the performance of spacecraft batteries, circuits used to control the satellites, and payload capabilities. The harsh space radiation environment caused by the Van Allen Belts, cosmic rays, coronal mass ejections, and solar flares puts a tremendous amount of stress on MOSFET devices, especially when they are not properly shielded or manufactured to handle the space environment. Research presented at the European Physical Journal Web Conference suggested eliminating poorly selected MOSFETs for space application by evaluating the device's external housing. It was determined that the thickness of the epoxy used for the external housing diminished performance of MOSFET devices when exposed to various doses of radiation [1]. While it is understood microelectronic devices are susceptible to radiation impacts, each device reacts differently based on its design and fabrication techniques. This generally means experimental tests are necessary to confirm the survivability of the device when exposed to radiation.

Radiation-hardened MOSFET devices are ideal for space applications since they use hermetically sealed packaging and low-temperature processing. Radiation-hardened MOSFETs are more radiation tolerant and experience fewer effects when exposed to the space environment [2]. However, competition from the commercial market has increased the lead-times for radiation hardened MOSFETs, impacting satellite manufacturers. The current semiconductor shortage has affected the availability of rad-hardened MOSFET devices, as well as standard MOSFETs. To meet production deadlines, companies are using standard commercial MOSFETs, which do not have the same level of radiation tolerance.

This thesis research used computer modeling and experimental testing to evaluate how different orbital inclinations, phases of the solar cycle, power conditions (biased

versus unbiased), and shielding impact the survivability of a MOSFET device in a low Earth orbit (LEO) orbit. We evaluated the radiation tolerance of the Infineon BSC060N10NS3GATMA1 power MOSFET to find the optimal orbit considering total ionizing dose (TID) effects. Of note, this device is being considered for the lithium battery power protection circuit in the Space System Academic Group (SSAG) high altitude balloon (HAB) project.

B. RESEARCH QUESTIONS

Our research question asks, "What risk is the DOD taking by leveraging commercial companies for space missions?"; specifically, when companies utilize non-radiation-hardened MOSFET devices in their satellites. To answer this question, we analyzed whether MOSFETs are affected more under biased conditions (simulating operation) or unbiased conditions (simulating spare circuits/parts). Second, we considered how shielding affects the radiation dose and verified this by testing the MOSFET to failure (no longer within manufacturer specifications) using an x-ray chamber in TID testing. Third, we simulated the radiation environment over a wide range of LEO orbits during solar maximum and minimum.

C. METHODOLOGY

To perform the radiation testing, we first designed and fabricated a bias board that enabled us to irradiate multiple MOSFET devices in both biased and grounded configurations. This allowed us to track the degradation of the devices during TID x-ray testing until the device failed. We determined the failure point by tracking the voltage threshold of the irradiated devices when it exceeded the manufacturer's specification. We used modeling to determine what space environment the power MOSFET could survive using the SPace ENVironment Information System (SPENVIS). SPENVIS calculates the radiation environment for different scenarios based on inclination, shielding, altitude, and phases of the solar cycle. Through testing we determined the minimum TID threshold to cause parts to fail, which allowed us to identify orbits the device could survive during solar maximum and solar minimum scenarios.

D. THESIS OVERVIEW

Chapter II provides an overview of MOSFETs and their applications in satellites. Chapter III covers the design and fabrication of our bias board and supporting apparatus, as well as TID results for the MOSFET devices. Chapter IV provides an overview of the SPENVIS model used to characterize the radiation environment in which the MOSFET would be used. The thesis concludes with Chapter V, which covers future work and recommendations for use of the MOSFET device in LEO.

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II. BACKGROUND

A. MOSFET DEVICES

A MOSFET device can act as a signal amplifier, an electronic switch in a circuit, a voltage regulator, or as a direct current relay. MOSFETs are commonly selected over their counterpart, the bipolar junction transistor (BJT), because they consume less power and can be made significantly smaller than BJTs, which makes them ideal for digital circuits. MOSFETs are highly recommended for use in integrated computer circuits and high-speed switching applications [3]. While MOSFETs excel in these applications, they are susceptible to high temperatures, radiation exposure, electrostatic discharge (ESD), and high currents. Passive or active cooling techniques are typically implemented to mitigate the device from failing due to high temperatures. Shielding is used to minimize radiation exposure to prevent damage to the device. Good grounding techniques and clean rooms are used to prevent inducing ESD damage to the MOSFET. A load resistor can protect the MOSFET from high currents when bias is applied to the circuit. Utilizing these techniques will protect a MOSFET device in the testing, fabrication, and operational phases of its life cycle.

1. P-Channel vs. N-Channel MOSFET

There are two categories of MOSFETs: p-channel (or PMOS) and n-channel (or NMOS). The term "channel" refers to the channel that is created between the source and drain terminals when the MOSFET is powered on. In an n-channel MOSFET, the channel current is composed of electrons (negatively charged), whereas, in a p-channel MOSFET, it is made up of holes (positively charged) Figure 1 introduces the basic components of a MOSFET; they include the "source," "gate," "drain," and "bulk" [4]. Other terminologies that may be used to reference the "bulk" include "substrate," "base," and/or "body." The image on the left in Figure 1, represents an n-channel MOSFET. The body, source, and drain layers of an n-channel MOSFET are doped [4]. Doping is a process in which impurities are injected into the material to create the p-channel or n-channel layer [5]. In

the n-channel MOSFET the doped areas act as donors (donating electrons) and typically are doped with elements such as phosphorus, arsenic, or bismuth.

The image on the right in Figure 1 shows a p-channel MOSFET [4]. In a p-channel MOSFET the source and drain layers are electrically neutral with doped acceptors (accept electrons) [5]. Boron, gallium, or indium are typically used as doping materials to create a p-channel MOSFET [5]. The gate terminal in both types of MOSFETs is the conductive metal, which is how the MOSFET got its name; however, there has been a switch in the industry to used doped polysilicon material to separate the nonconductive gate oxide layers typically silicon (Si), SiO_2, SiGe, or SiC. The device tested in this thesis was an n-channel MOSFET and used the new doped polysilicon material for the gate and a pure Si oxide layer.

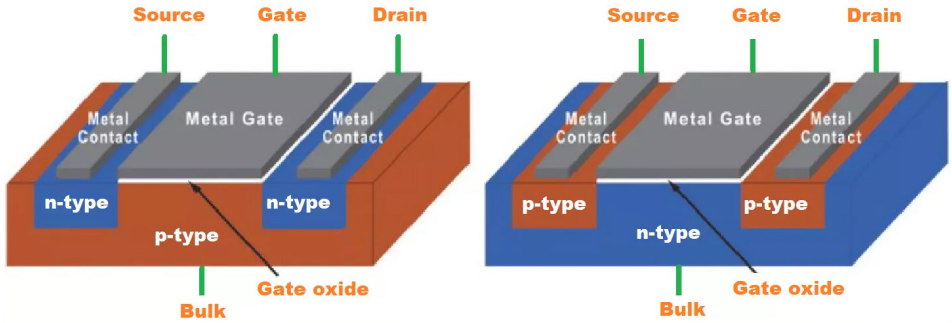

Figure 1. N-Channel vs. P-Channel MOSFET. Source: [4].

In n-channel MOSFETs, electrons act as the charge carrier in the current channel between the source and drain terminal when the device turns on. The carrier mobility of a n-channel MOSFET is approximately two to three times higher than that of a p-channel MOSFET for the "same resistance drain-to-source on" value, which means a p-channel device must be two to three times the size of an equivalent n-channel MOSFET [6]. For this reason, n-channel MOSFETs are often the preferred choice for a high current application.

2. MOSFET Package Types

To accommodate an array of applications and circuits, MOSFETs are packaged in different form factors, the most common being the thru-hole, surface mount, Power Quad Flat No-lead (PQFN), and directFET as seen in Figure 2 [7]. The surface mount, PQGN and directFET packages are typically used in integrated circuits where the MOSFET is soldered onto the printed copper board. In the surface mount and thru-hole package configuration, the leads typically act as the source, drain, and gate terminals; however, best practice is to reference the manufacture's data sheet to identify the correct terminals. Although there are four terminals, most often you will only see three terminal connections points for the (source, drain, and gate) because the body is connected internally to the MOSFET source terminal.

Reviewing the specification sheet is more imperative when using PQFN and directFET package MOSFETs, in which the drain, grate, and source pins/contacts can be interconnected to provide the user a better experience when soldering and help with heat dissipation to protect the MOSFET. In the thru-hole package the MOSFET can be affixed to the printed copper board by drilling and screwing the device onto the circuit; metal leads make it easy to conform to the circuit.

The device tested in this thesis used a unique package developed by Infineon Technologies called the PG-TSDON-8. This MOSFET package is wider than the PQFN to allow for more contact with the heat sink, which helps dissipate heat across the drain pins. In addition, three of the four pins are connected across the source, leaving one pin for the gate terminal. An excerpt from the manufacturer's data sheet showing the device is provided in Appendix A.

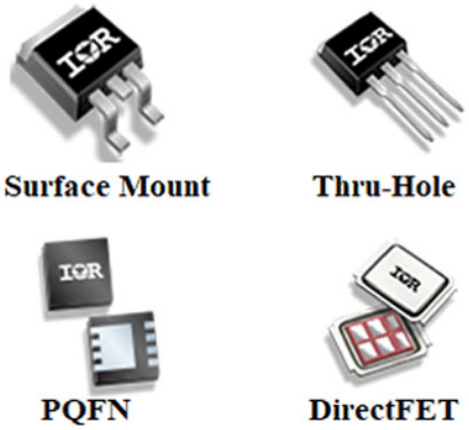

Figure 2. Commonly Used MOSFET Package Types. Source: [7].

3. Infineon BSC060N10NS3GATMA1 Power MOSFET

The MOSFET tested in this thesis is part of the Infineon OptiMOS 3 line of products that is "specifically designed for power conversion and power management applications that require high efficiency and power density", which is why it was selected for the SSAG battery power protection circuit [8]. The manufacturer claims the SuperSO8 footprint "reduces the on-state resistance by up to 50 percent compared to other MOSFETs in its class" and "enables faster switching while minimizing switching and gate-drive losses, higher power densities, and less heat generation in the driver" [8]. Table 1 outlines key specifications for the Infineon MOSFET that informed the board design and radiation testing [9]. Additional details are provided in an excerpt from the manufacturer's data sheet in Appendix A.

For our radiation testing we were limited to purchasing 17 MOSFET devices due to availability. Three devices were used for preliminary testing to verify current limits and fabrication methods. The other 14 devices were used to conduct the TID radiation test at Prairie View A&M, with two of those devices used as controls. This reduced the number of tests we could conduct. With additional devices we would have also tested different angles from the source x-ray, operating at a different frequency for bias conditions, and using different shielding thickness and materials.

Table 1. Key Parameters of the Infineon MOSFET Device. Source: [9].

Channel:	N-channel	
Package:	PG-TSDON-8	
Voltage Threshold (V_{th}):	2.7 V avg.	2.0 V min
Gate to Source Voltage (V_{gs}):	+/- 20 V	
Power dissipation:	125 W	
Continuous Drain Current:	90 A	

B. RADIATION TESTING

TID is the measure of the energy absorbed during exposure to radiation; it is measured in rads, where 1 rad = 0.01 J/kg. The goal of TID testing is to measure key device characteristics as the part is exposed to radiation. We monitor the degradation of the device until it eventually fails by exceeding specifications prescribed in the manufacturer's data sheet. In the space environment, degradation of a part can be caused by ionizing radiation sources such as trapped electrons and protons, gamma and x-rays, solar energetic particles, and cosmic rays [10]. A single solar event can generate enough radiation to cause permanent damage to a MOSFET device; this is called a single event burnout or a single event gate rupture. Radiation testing to simulate these types of events is known as single event effect (SEE) testing. However, TID testing involves just enough radiation exposure to accelerate the degradation process to replicate the total dose a device will receive during its mission lifetime. The dose rates used in TID testing are not high enough to induce SEEs. We conducted a TID test at 1.08 krad/min using x-rays.

TID failures in MOSFETs are typically caused by the accumulation of trapped charges in the oxide gate, which increases the threshold voltage and leakage drain currents [11]. After conducting several TID tests of both n-channel and p-channel MOSFETs, Dr. Lauenstein's research at NASA Goddard determined MOSFETs typically show failure in the degradation of the voltage threshold and leakage drain current [12]. Based on the NASA results, we monitored the device voltage threshold (Vth) for signs of failure. Voltage threshold is the minimum gate voltage needed for current to flow from the source to the drain in the MOSFET. Yang et al., irradiated MOSFETs at different frequencies; their research showed more stress was placed on the device as the frequency

increased on the biased gate terminal during irradiation [13]. Based on this, we expect the biased MOSFET without any shielding should show the most TID degradation.

1. X-Ray vs. Gamma Radiation

Two common forms of ionizing radiation used for TID testing are gamma rays and x-rays. When x-ray or gamma-ray photons interact with the Si bond in a MOSFET, hole trapping can occur, which can significantly increase the charge in the device and cause it to fail. Sometimes a failed device recovers after being removed from the radiation. In this phenomenon, the device (which can either be in a biased or unbiased state) heals itself after a period of time known as the "annealing period". Our testing used an annealing period of 24 hours; however, annealing sometimes requires weeks to see the effects.

X-ray and gamma radiation are similar, but gamma rays typically require nuclear sources, such as Cobalt-60 (Co-60), while x-rays can be produced mechanically from an x-ray tube, like the X-RAD IR160 shown in Figure 3 and used in this research [14].

Figure 3. X-RAD IR160 X-Ray Chamber with Power Supplies Configured

X-ray and gamma radiation can be further differentiated by their frequency, wavelength, and energy [15]. Gamma-rays have the highest frequency and shortest wavelength, which corresponds to greater energy and penetration capabilities. Gamma-rays from Cobalt-60 have energies of roughly 2.5 MeV, while the X-RAD IR160 produces x-rays up to 160 kilovolt peaks (kVp), or 160 keV. The higher energy of Co-60 gamma rays require more shielding than x-rays [15].

X-ray testing has become more appealing because it can be used to irradiate parts without having to worry about a dangerous radioactive material like Co-60. In the government sector, Co-60 is still the standard for radiation testing because they have the clearance and facilities required to store radioactive material. Educational institutions and private companies often choose x-rays because they are less dangerous, don't require special shipping procedures, and do not require special shielding and security to house radioactive material. Although special training is required to conduct x-ray radiation testing, using Co-60 requires background checks, specialized equipment, and monitoring for radioactive leakage from the chamber. Working with x-rays is also quicker and safer than Co-60 because once the machine turns off, the x-ray emissions stop. When working with Co-60 the user must wait until radiation levels have been deemed safe before entering the chamber. In addition, Co-60 has a half-life of 5.27 years, so disposal can be costly and require additional safety procedures for the facility and its operators [15].

2. Guidelines for TID Testing

For purpose of conducting our TID radiation testing we adopted the guidance outlined in MIL-STD-750D Method Number 1019.4, "Steady State Total Dose Irradiation" [16]. This guidance states:

1. All electrical measurements must be taken within one hour after the completion of one radiation cycle. [16]
2. After all electrical measurements have been taken, the devices must be returned for the next irradiation dosage. The time to place the device for the next cycle of irradiation must not extend past two hours. [16]
3. Electrical test instruments must be calibrated prior to irradiation testing e.g., power supplies and parameter analyzer. The test instruments used for electrical measurements will be configured to ensure they are stable. [16]

4. Test circuit board(s). The irradiated device shall be configured to ensure it is secure while maintaining circuit integrity during irradiation. It shall have connected all its bias for the proper functionality of the circuit while irradiating or testing device characterization. To ensure the integrity of the irradiating procedure no terminals, connections, or inputs shall be left floating. During irradiation, the circuit and support structure shall allow for uniform coverage considering the geometry and materials the devices will be tested on. An ideal apparatus will avoid oscillations when on a stable platform, reduce the chance of leakage currents, reduce the chance of electrical damage, and collect accurate measurements during irradiation and measuring. In between test setups, the bias board will be checked for functionality, looking for loose wires, connection points, and test bias from the power supply. [16]

3. Reducing Radiation Effects

The most effective way to reduce radiation effects in MOSFETs is to use a device optimized for radiation. The devices are hermetically packaged and sealed to provide an air and watertight seal, preventing escape of gases and vapors from the electrical components of the MOSFET. This protects the devices against corrosion, environmental, and space radiation. Most MOSFET devices are packaged using a hermetic glass-to-metal or ceramic-to-metal seal [17].

The next best alternative to using a rad-hard device is to use a commercial MOSFET and then apply either aluminum (Al) or lead shielding around it. However, in the future NASA and DOD are planning to adopt a lead-free policy because lead is considered a hazardous material for space application and produces secondary radiation effects [18]. The advantage of using lead over aluminum is that since it is a denser material thinner sheets achieve comparable shielding results. The major downfall to using lead is it is not as rigid as aluminum, which can necessitate thicker sheets, adding weight. In most cases a size and weight requirement for a mission may ultimately determine which material is used to mitigate radiation effects. Advancements in computer aided design and 3D printing allows material engineers to maximize the shielding when using aluminum to satisfy both size and weight requirements. This enables them to use the dimensions of the circuit or parts and to make precision cutouts where the components are placed, which ensures maximum shielding for the device.

A final way to mitigate impacts caused by radiation effects is to include spare parts and circuits that can be substituted through a command link if required. It is a common practice, especially in digital electronics, when a part is believed to have failed due to radiation effects to send an error correction command. This system of troubleshooting is important because the MOSFET is a single component of a circuit. However, this strategy will not work if the spare parts or backup circuits also experience significant radiation damage, which is the main reason for testing parts in the unbiased condition. If the unbiased state (simulating a spare part) performs worse than the biased state (simulating an operational part), then the device should not be used as a spare part.

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III. ENGINEERING DESIGN AND TESTING

A. SCHEMATIC OF BIAS BOARD

Figure 4 illustrates the schematic that was designed to fabricate the bias board for TID radiation testing. The bias board allows six MOSFETs to be tested simultaneously: three under bias and three unbiased with all the pins connected to a common ground. A function generator, represented by the alternating power supply, allows the MOSFETs to turn off and on by setting the voltage to 0 and 5 volts respectively, using a square wave form. We set the frequency to 1 kHz with a duty cycle of 50 percent, which helped ensure the device did not overheat. The higher the duty cycle the more the circuit acts as a constant on power supply. An ammeter placed between the drain and direct current (DC) power supply was used to confirm the maximum amount current to the device before overheating. All three devices turned on simultaneously because they were placed in parallel with the power supply across the gate terminal.

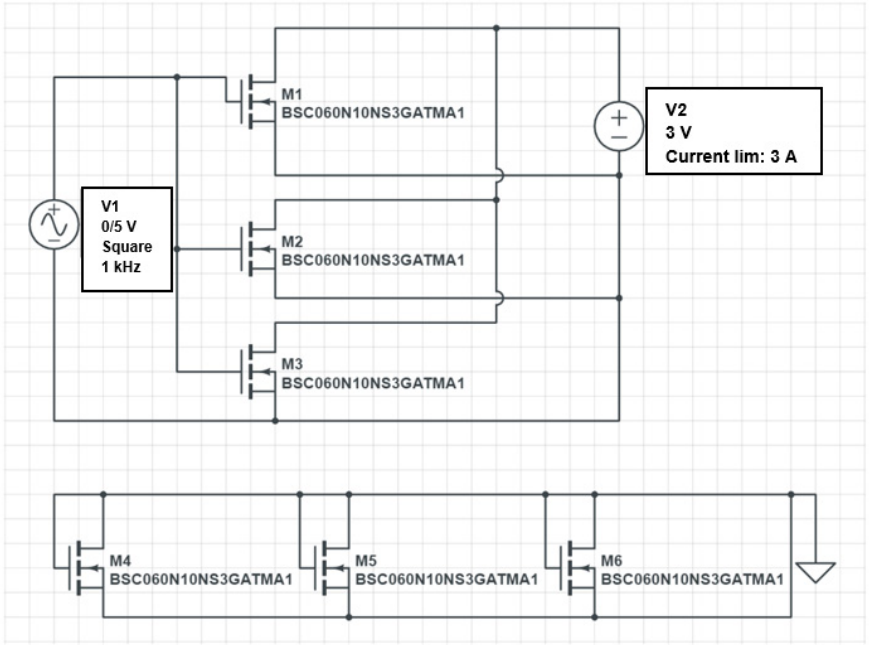


Figure 4. Schematic of Bias Board for Radiation Testing

A second DC power supply was applied across the source to drain (V_{ds}) at 3 volts to enable current to flow from the drain to the source. All three of these MOSFETs were connected in parallel to the DC power supply. During preliminary testing, the device failed when the voltage reached 3.8 volts, with visible damage across all drain, source, and gate pins. The first sign of stress was observed at 3.5 volts when the device started to get hot and then eventually started to smoke at 3.6 volts. To mitigate this, we could have placed a load resistor in series with the DC power supply and drain pin; instead, we simply used the internal resistance and limited the current through the DC power supply to 3 A. If the goal were to test the device as an amplifier, we would have included passive or active cooling to ensure the device could operate in the "saturation region."

The bottom of Figure 4 shows three MOSFET devices in an off state with all pins grounded. This was accomplished by connecting the source, drain, and gate pins to a common ground. These three devices represent the unbiased, spare parts, while the three devices at the top of the figure represent the active parts under power.

Figure 5 illustrates one of the first relationships taught when learning about MOSFETs: the I_d versus V_{ds} curve [19]. The figure shows the drain current (I_d) measured as a function of the voltage applied across the drain to source (V_{ds}) for different values of the gate to source voltage (V_{gs}). The specific V_{gs} relevant for any given device is provided in the manufacturer's data sheet.

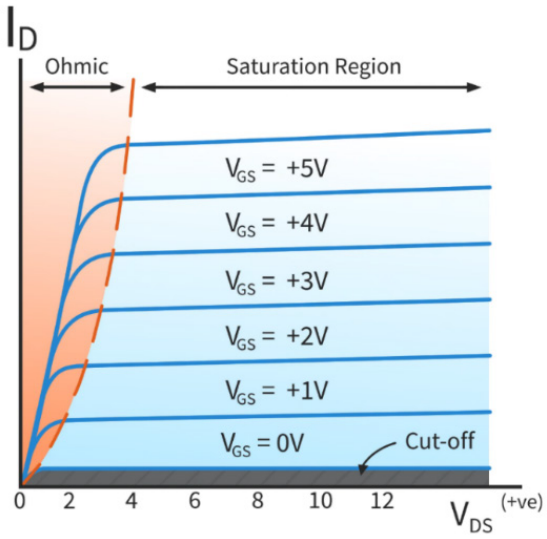


Figure 5. MOSFET: I_d vs. V_{ds} Curves. Source: [19].

I_d/V_{ds} curves are used to confirm the functionality of a MOSFET device, especially after fabrication. The curves can be broken into three regions: cutoff, ohmic, and saturation. When the device is powered off, or the applied voltage is less than V_{th}, the device is in the cutoff (or pinch-off) region, shown in Figure 5 as the grey region. In the cutoff region the device does not respond to an applied V_{ds}.

As V_{gs} increases beyond V_{th}, the device enters the ohmic region (also called the linear or triode region), shown in Figure 5 as the orange region. In this region, increasing V_{ds} causes a linear increase to I_d, which allows the MOSFET to be used as a switch. As V_{ds} increase further, such that $V_{ds} > V_{gs} - V_{th}$, the MOSFET enters the saturation region, shown as the blue region in Figure 5. In this region, increases to V_{ds} do not produce much change in I_d [19]. Our testing employed the MOSFET as a switch to support the battery design of the HAB battery circuit, so we designed the circuit to keep $V_{gs} > V_{th}$ and $V_{ds} < V_{gs} - V_{th}$.

B. BIAS BOARD FABRICATION

The first stage of fabrication involved converting the device from a surface mount into an 8-pin dip connection so the parts could be moved quickly from radiation testing to parameter testing. We used the Chip Quik Inc. model IPC0051 board, which was made specifically for power MOSFETs with an integrated heat sink to take advantage of the

device's aluminum pad. Compared to a standard print copper board (PCB) 8-pin dip adapter, the IPC0051 board was able to handle roughly 0.5 amps more current before overheating. The increased performance by the IPC0051 board over the standard PCB 8-pin dip adapter might have been contributed due to the design the implementation using the integrated aluminum heat sink and epoxy glass board on the IPC0051.

To convert the device into an 8-pin dip, we first applied solder paste to the IPC0051 board using the thinnest tip on the solder gun. This prevented spillage of the solder onto the adjacent pins that could have caused a short. Next, we used a hot plate for 20 seconds to seal the solder paste, then placed the board onto an Al bar to cool. A thermal microscope allowed for visual confirmation to verify the solder had been applied correctly. Using solder flux prevented the solder from balling up and allowed it to flow uniformly by removing oxide films on the metal contacts of the IPC0051 board. After the chip has cooled, "best practice" is to remove the flux residue to ensure the board stays clean and prevent dust from settling onto the flux residue, which protects the device from ESD damage. We then conducted a visual inspection, followed by a pinout test using a multimeter. Finally, we tested the device on a parameter analyzer to verify it produced the correct I_d versus V_{ds} curves. Note that using the IPC0051 board added two extra pins, one on each side, for a total of ten pins. These pins are available to connect an external heat sink but were not used in our test configuration.

Next, we fabricated the bias board using two stereo PCB connectors for each biased MOSFET, for a total of six, as illustrated in Figure 6. One connected to the function generator (V_{gs}) and the second supplied power for the DC power supply (V_{ds}). We used threaded 20-gauge copper wire to support the three amps of current flowing through the circuit. Position header connectors were used to swap out the devices in between radiation testing and parameter analyzer testing to measure the voltage thresholds. Two separate wire colors were used to help distinguish between the positive and ground connection points. To comply with the "Steady State Total Dose Irradiation" guidelines, the wires were cut and soldered to the shortest possible length, preventing current leakage, and reducing the chance of shorting out the circuit. For the grounded devices, all the pins were connected using a piece of wire and solder. Figure 6 shows the final assembled bias board and

supporting apparatus in a top-down view. The pair of black and red wires connect to the two power supplies, while a fifth yellow wire connects all the pins to a common ground.

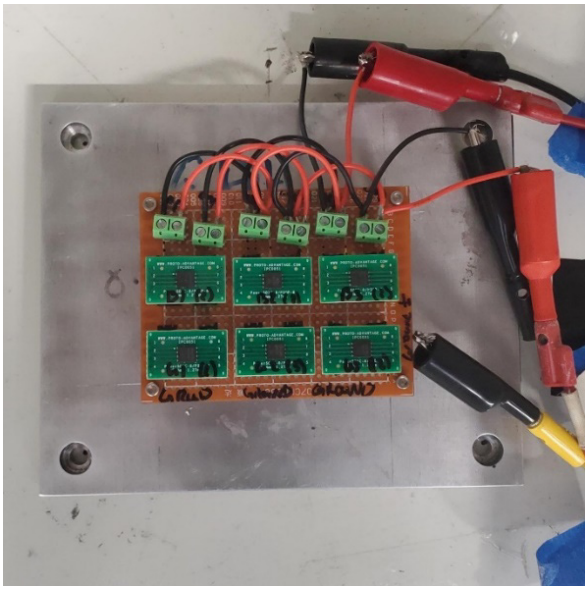


Figure 6. Bias Board Fabrication Top-Down View Test Configuration

The final stage of the fabrication was to construct a stable platform for the bias board; we used a ½ inch thick piece of aluminum as the base. Spacers were added to prevent the bias board from shorting out through the base. The bias board was then held into place using a washer and hex screw on top.

C. PARAMETER ANALYZER TESTING AND RESULTS

A critical part of the radiation testing was having access to a parameter analyzer to characterize the device. We used the Keysight 1500A; the Keysight offered many advantages over other parameter analyzers as it uses a Windows operating system, which made transferring and accessing data simpler and provided a better user interface. In addition, it came with pre-built test configurations for a multitude of devices, which simplified setup.

On the back of the Keysight are various source measuring units (SMU) modules. The image on the left side of Figure 7 shows how the testing setup utilized a medium power

SMU (MPSMU) and ground modules, which have two output readings: force and sense. The force terminal gives the user the ability to source and measure the device with a two-wire connection. Sense readings use a four connection terminal, which allows it to be used as a feedback loop in the case of cable loss across the force line [20]. The image on the right in Figure 7, shows how the SMU cables are connected to the device gate, drain, and source pins. When the SMU cables are connected properly the user can set up the test parameter for SMU 1 "gate", SMU 2 "drain", and SMU 3 "source" on the Keysight 1500A to record the reading of the V_{th}.

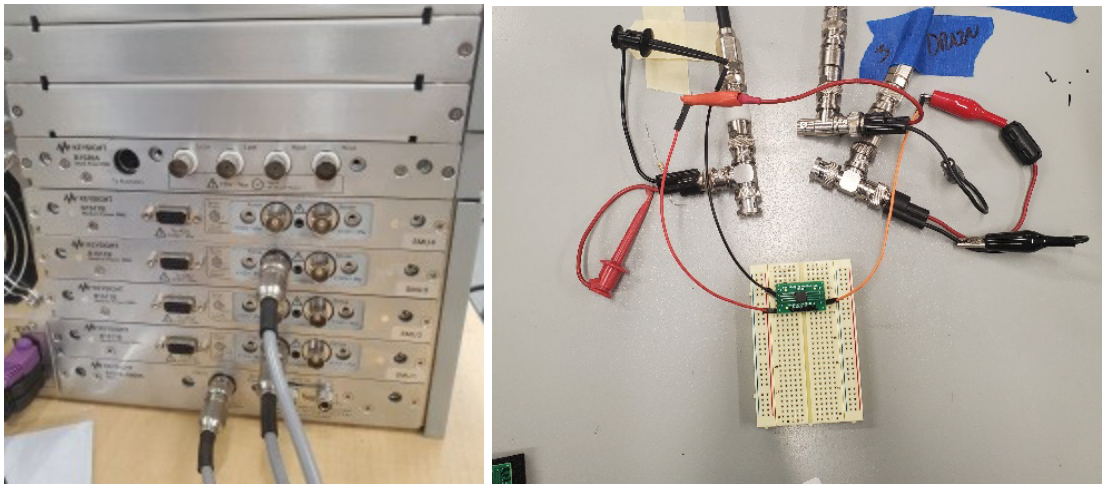


Figure 7. Keysight 1500A Parameter Analyzer SMU Cabling setup

Our application required just two of the supplied MPSMU modules in the force configuration for the gate and drain terminals. The third SMU was connected to a ground module referencing the source terminal. Within the Keysight we used the pre-configured settings to measure V_{th}: "V_{th} Constant 3 PowerDevice" (indicating power MOSFET). SMU1 was set to test the device across the gate from 0 to 5V, starting at 0. SMU2 was set to 3V to exceed the threshold voltage of 2.7 V (per the manufacturer's data sheet). SMU3 was grounded in accordance with the "V_{th} Constant 3 PowerDevice" test settings. The Keysight settings are summarized in Table 2.

Table 2. Device Test Parameter for Characterization

SMU1: Gate	**SMU2: Drain**	**SMU3: Source**
Base offset V: 0V	V_d: 3V	Grounded
V_g Start: 0V		
V_g Stop: 5V		
V_g Step: 500 mV		

Once the device was connected to the parameter analyzer, we collected pre-radiation data. To measure V_{th}, the Keysight generates an I_d versus V_g plot, which represents a variant of the I_d versus V_{ds} plot shown in Figure 5. In this case, V_{ds} (SMU2) is held fixed while sweeping across V_{gs} (SMU1). Figure 8 shows the raw data recorded from the Keysight during a pre-radiation test. The blue and orange lines show the current as the gate voltage sweeps from 0 to 5V. The vertical purple line indicates the voltage threshold (V_{th}) of the device being tested and represents the most critical test parameter. Devices were deemed to be "within spec" when the measured V_{th} exceeded the manufacturer's specification of 2V. All 17 MOSFET devices were tested in this manner prior to irradiation and found to be within the manufacturer's specifications. Figure 8 shows the pre-radiation test results for part B3 while under bias. In this case, the threshold voltage was measured to be 2.81201V, above the 2V minimum.

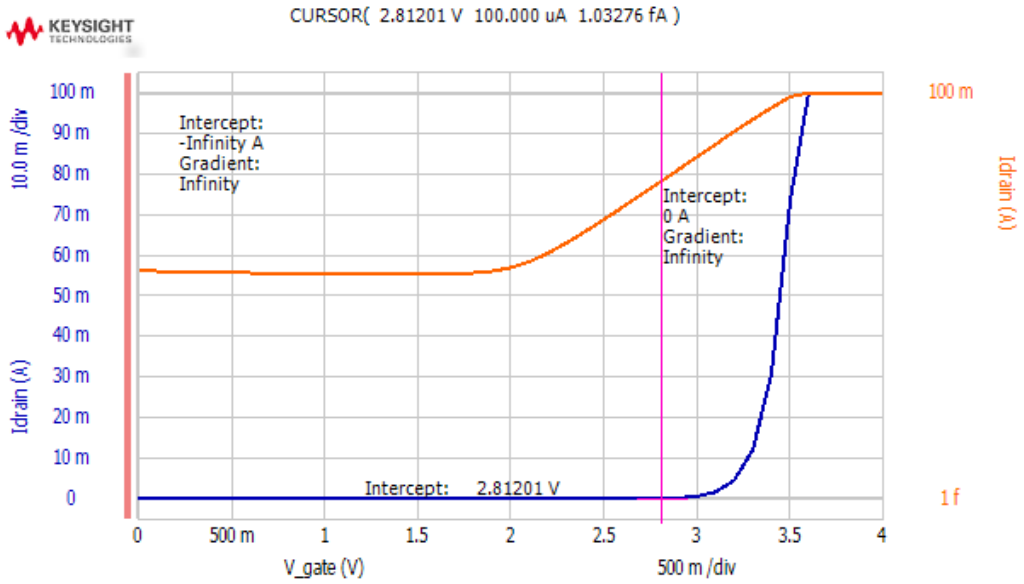


Figure 8. MOSFET Pre-radiation: Voltage Threshold Biased Condition at 0 krad

Figure 9 shows how the x-ray TID degraded the performance of the same device (B3). The figure shows the same I_d versus V_{gs} curve as Figure 8, but after exposure to 10 krad of radiation while in a biased configuration. As shown in the figure, V_{th} was measured to be 1.53685V, which falls below the 2V minimum indicated by the spec sheet. Figures 8 and 9 are intended to illustrate the raw data collected after each test using the Keysight 1500A parameter analyzer. A full report for all devices is provided in the next section.

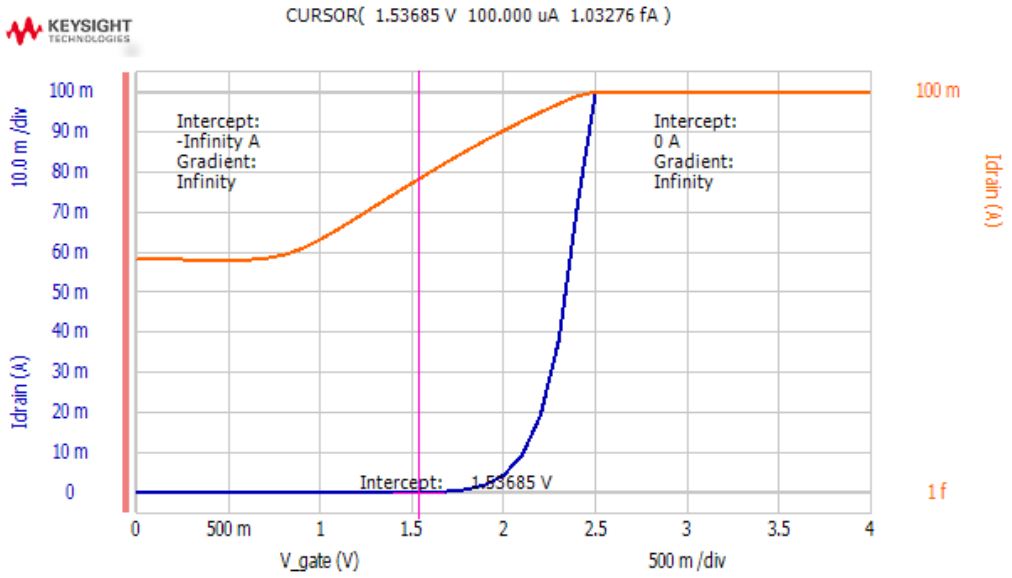


Figure 9. MOSFET Post-radiation at Failure: Voltage Threshold Biased Condition at 10 krad

D. RADIATION TESTING SETUP AND RESULTS

We conducted the TID test at Prairie View A&M University using their x-ray chamber. The devices were irradiated roughly at 1080 rad/min, but the received dose depends how far the device is from the source. As seen in Figure 5, our bias board apparatus was located approximately 70 cm from the source at 160 kVp (160 eV) to achieve this dose rate. During testing, V_{th} measurements were taken after achieving a cumulative dose of 1.08, 6.7, 10, 15, 20, 25, 30, 35, 40, 45, 50, and 55 krads. The test was conducted at room temperature for all cycles. A total of 12 devices were irradiated over two days with two of the devices used as controls. Each bias board tested three of the devices in a dynamic on-state configuration using a function generation supplying 0 to 5V with a 50 % duty cycle at 1 kHz across V_{gs}., then applying a static 3V across V_{ds}. Three other devices were tested with all pins grounded across the source, drain, and gate pins. The following test equipment was used: function generator- Agilent 33220A, DC power supply- Agilent E361A, parameter analyzer- Keysight 1500A, x-ray chamber- X-Rad IR-160.

The first day of radiation testing examined the performance of unshielded MOSFET devices. Table 3 provides a record of the radiation test condition and times for each cycle

of testing until the devices failed. Three devices were grounded to represent spare parts (G1, G2, G3) and three were biased to represent operating parts (B1, B2, B3). An additional control device was used as a control and not subject to any radiation.

Table 3. Unshielded Radiation Test Conditions

Dose Rate (rads/s)	**Cumulative Dose (krads)**	**Irrad. Time (sec)**	**Total Irrd. Time Elapsed (sec)**	**Temp (ºF)**
18	1.08	60	60	69
18	6.7	332	392	69
18	10	224	616	69
18	15	278	894	69
18	20	278	1172	69
18	25	278	1450	70
18	30	278	1728	69

Figure 10 shows the voltage threshold (V_{th}) recorded for the six devices as a function of the radiation dose; the black line in the figure depicts the control device. The failure point for each device is shown when V_{th} drops below 2V indicated by the red line. After each stage of irradiation, the control was used to confirm the accuracy of the Keysight before testing the other MOSFET devices. The final data point after each line shows the V_{th} measured after a 24-hour annealing period.

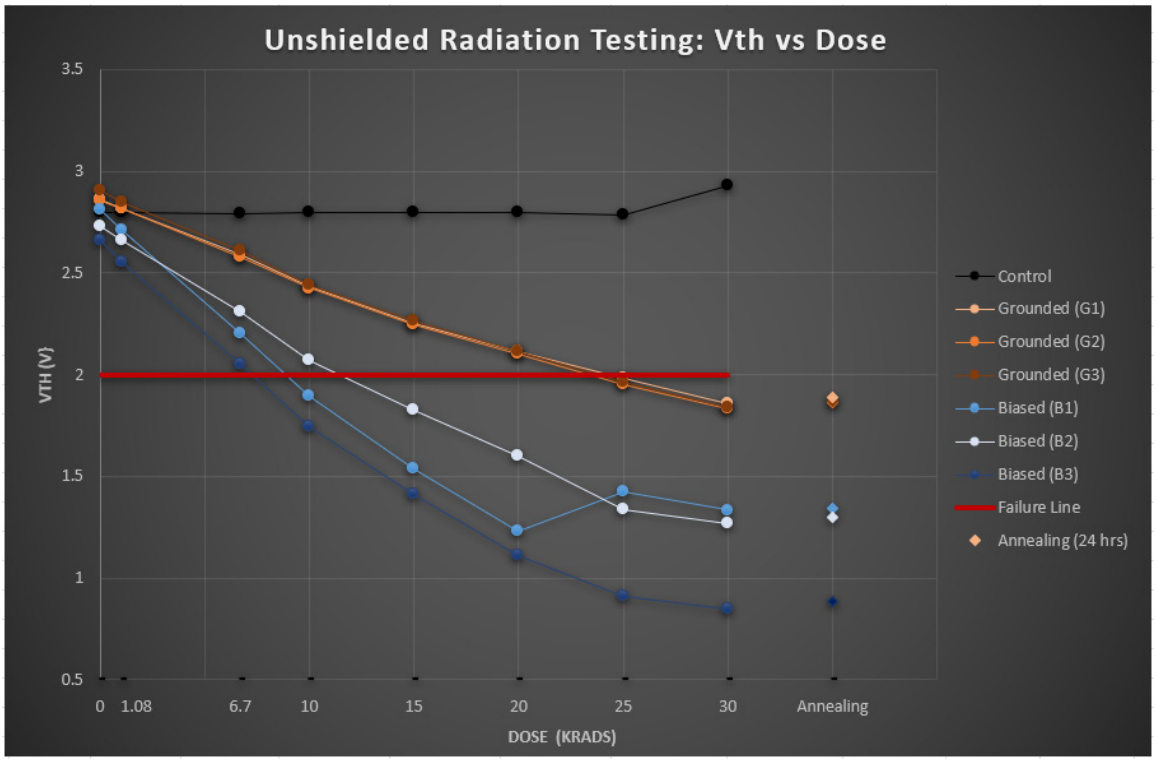


Figure 10. Unshielded Radiation Test Results V_{th} vs. Total Dose

Devices under bias showed the fastest decline, with devices B1 and B3 failing after the 10 krads test cycle. The trapped particles stored within the gate oxide eventually caused the device to fail by going below the 2V minimum V_{th} indicated by our spec sheet. Linear interpolation of the data between the dosage values at 6.7 krads and 10 krads suggests the devices would have failed at approximately 7 krads for B3 and 8 krads for B1. B2 was the most resilient, failing after 15 krads of TID; interpolation suggests this device would have failed at approximately 12 krads. Devices not under bias (G1, G2, and G3) showed less susceptibility to radiation, enabling them to survive until approximately 24 krads. All the grounded devices degraded at roughly the same rate. The fact our biased devices failed before the grounded devices suggest the Infineon MOSFET can be used for spare parts. The unshielded test results suggest devices under bias fail sooner than grounded devices, answering the first research question of the thesis.

None of the devices recovered after the 24-hour annealing period. It is possible the devices may have recovered after a longer annealing period, but we were unable to anneal

for longer than 24-hours due to time limitations. It was reassuring to see that the grounded devices, which simulated spare parts, survived longer than those under bias. Note that even though all the devices eventually fell below the manufacture's voltage threshold specification (indicating failure), they all continued to respond to the parameter analyzer while being tested, so didn't fail completely. Corresponding values of total dose and annealing from Figure 10 have been included in the first table in Appendix B.

The second day of testing examined the performance of shielded devices. Table 4 provides a record of the radiation test conditions and times for each cycle of testing until the devices failed in the shielded scenario. Three were grounded to represent spare parts (G1, G2, G3) and three were biased to represent operating parts (B1, B2, B3). An additional control device was not subject to radiation.

Table 4. Shielded Radiation Test Conditions

Dose Rate (rads/s)	Cumulative Dose (krads)	Irrad. Time (sec)	Total Irrd. Time Elapsed (sec)	Temp (°F)
18	1.08	60	60	69
18	6.7	332	392	69
18	10	224	616	69
18	15	278	894	70
18	20	278	1172	71
18	25	278	1450	71
18	30	278	1728	71
18	35	278	2006	71
18	40	278	2284	71
18	45	278	2562	70
18	50	278	2840	71
18	55	278	3118	70

Figure 11 shows how the devices were configured in the radiation chamber along with the Al filter that was used to shield the devices from the x-rays. The image on the right is the Al filter that was inserted near the source of the x-rays; this filter was not used in the unshielded test. The Al filter was placed 70 cm from the device for all radiation cycles.

The radiation dosage referenced in Table 4 and Figure 12 represents the exposed dose, not the dose received by the device because of the application of the Al filter.

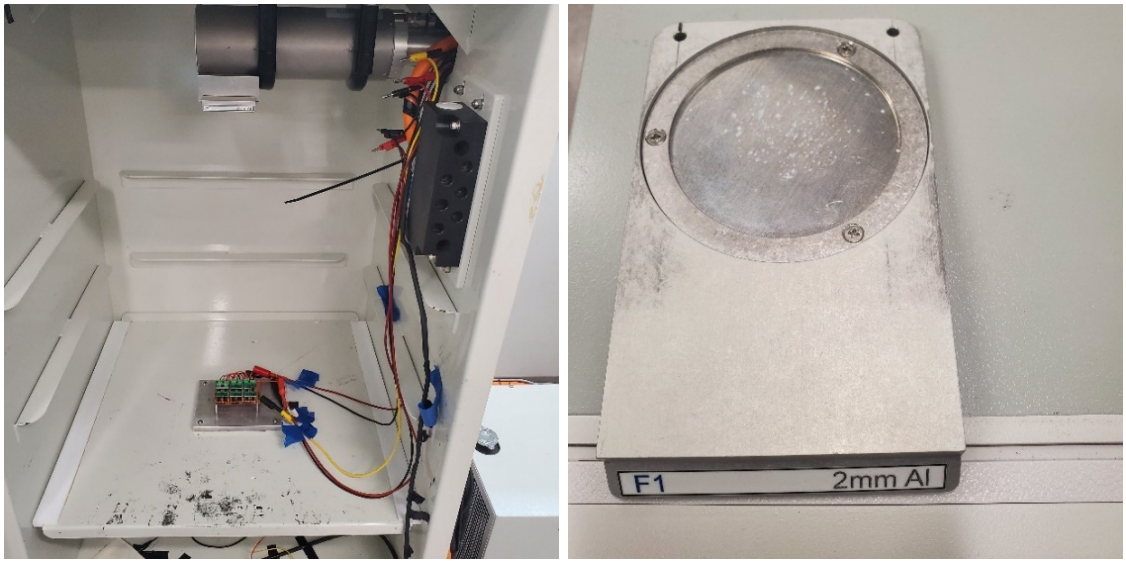


Figure 11. Biased Board Setup with Al Filter

Figure 12 again shows the measured V_{th} as a function of radiation exposure, but now the devices have a lower absorbed dose due to Al filter between the source and devices. The worst performing device was the biased device (B3), which failed at approximately 21 krads. This was also the only device that experienced a total failure and became unresponsive. There were no visible signs of failure; however, the device was unresponsive to the parameter analyzer, which indicates it most likely failed due to radiation exposure. Device B1 failed after being exposed to 30 krads of radiation; using interpolation the device likely would have failed at approximately 25 krads exposure. The best performing biased device (B2) failed after being irradiated to 55krads; interpolation suggests the device would have failed at approximately 50 krads. This made B2 an outlier of the three biased devices; however, the Al shielding caused a greater variation in the data. This variation is likely because the x-rays were scattered while penetrating through the shielding. The variation is also apparent when comparing the grounded devices in, the shielded and unshielded tests.

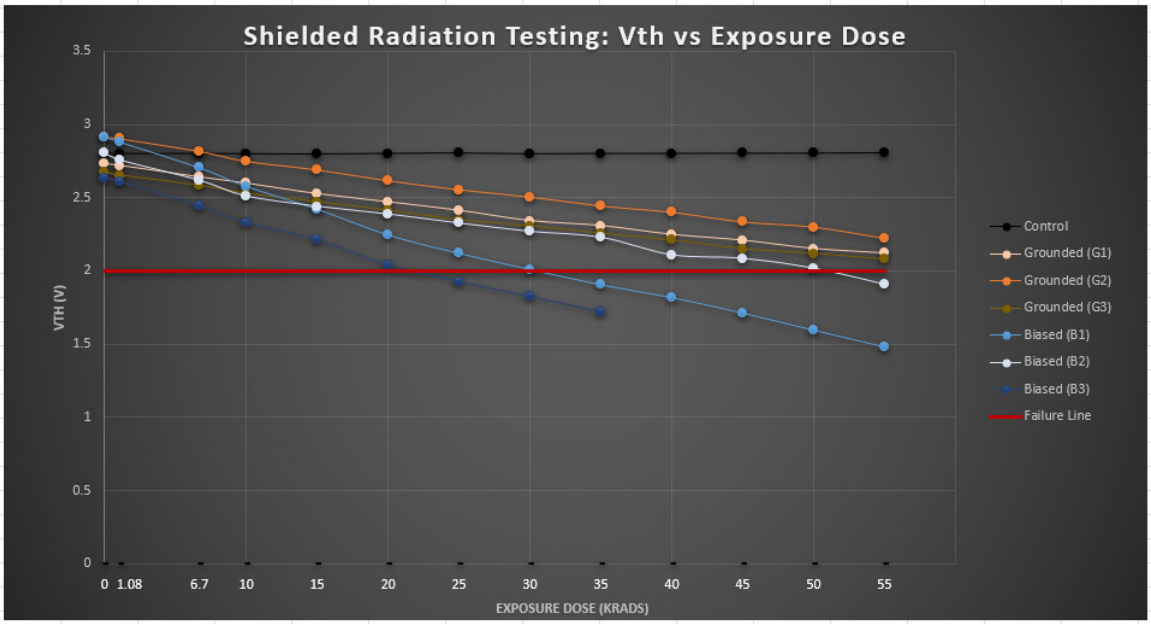


Figure 12. Shielded Radiation Test Results
V_{th} vs. Exposure Dose

All grounded devices stayed within the manufacturer's specification through 55 krads of radiation exposure. Time limitations prevented us from exceeding 55 krads of exposure; however, a linear curve fit of the data suggests the grounded devices could stay within specs until roughly 65-75 krads, which is consistent with the differences found between biased and unbiased devices in the previous unshielded test results. These results indicate that 2mm of Al shielding improved the survivability of the biased MOSFET devices by roughly a factor of 3. Corresponding values of exposed dose in Figure 12 have been included in the second table of Appendix B.

IV. SPACE RADIATION MODELING

A. SPENVIS OVERVIEW

The SPace ENVironment Information System (SPENVIS) is a web-based interface to a suite of space environmental models provided by the European Space Agency (ESA) [22]. SPENVIS is built off the Cosmic Ray Effects on Micro-Electronics (CREME96) model, a legacy radiation tool that incorporates galactic cosmic rays, solar energetic particles, radiation belts, and plasmas [23]. In addition, SPENVIS includes a tool to visualize the results together with the respective geomagnetic and solar indices. SPENVIS offers an updated user interface and models to provide a clearer understanding of the radiation environment. This research used SPENVIS (version 4.6.11.) to simulate a spacecraft trajectory in LEO at various altitudes and inclination angles to calculate the resulting radiation dose and damage equivalent fluences for a silicon (Si) MOSFET.

The next section covers the five subcomponent models and parameters used in SPENVIS to find the optimal LEO for the Infineon MOSFET device. Five subcomponent models were used to calculate the TID in SPENVIS: coordinate generator, trapped proton and electron fluxes, solar particle mission fluences, galactic cosmic ray fluxes, and ionizing dose for simple geometries. Each of the subcomponent models will be discussed further in association with the parameters used to calculate the TID for various orbital characteristics. Figure 13 shows the SPENVIS user interface and available subcomponent models used to calculate the TID, the effects of charged particles on a spacecraft, SEE, and potential hazards from space debris [21].

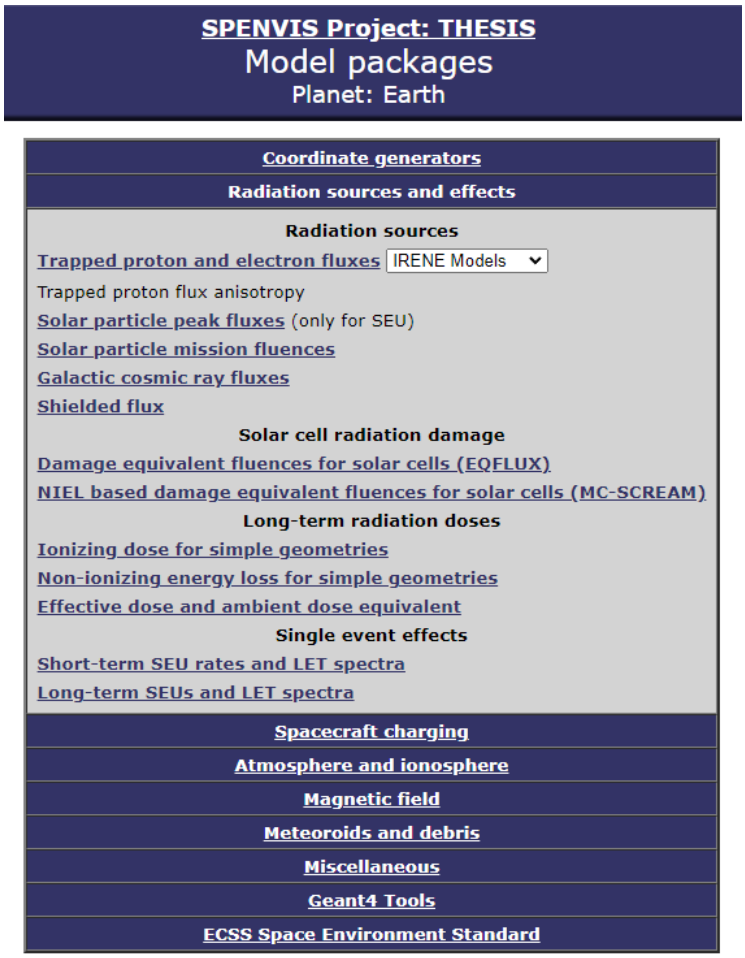


Figure 13. SPENVIS User Interface. Source: [21].

B. OVERVIEW OF APPLICABLE MODELS AND PARAMETERS

The first subcomponent model is the coordinate generator. Within this subcomponent, a user sets the mission start date and duration for the mission flight plan. Once completed the user then specifies characteristics of their orbital parameters: altitude, inclination, perigee and apogee, eccentricity, and semimajor axis. These inputs are used by SPENVIS to generate a 3D representation of the orbit as well as the mission report with the characteristics of the user's defined orbit. An example mission report is shown in Figure 14 [21].

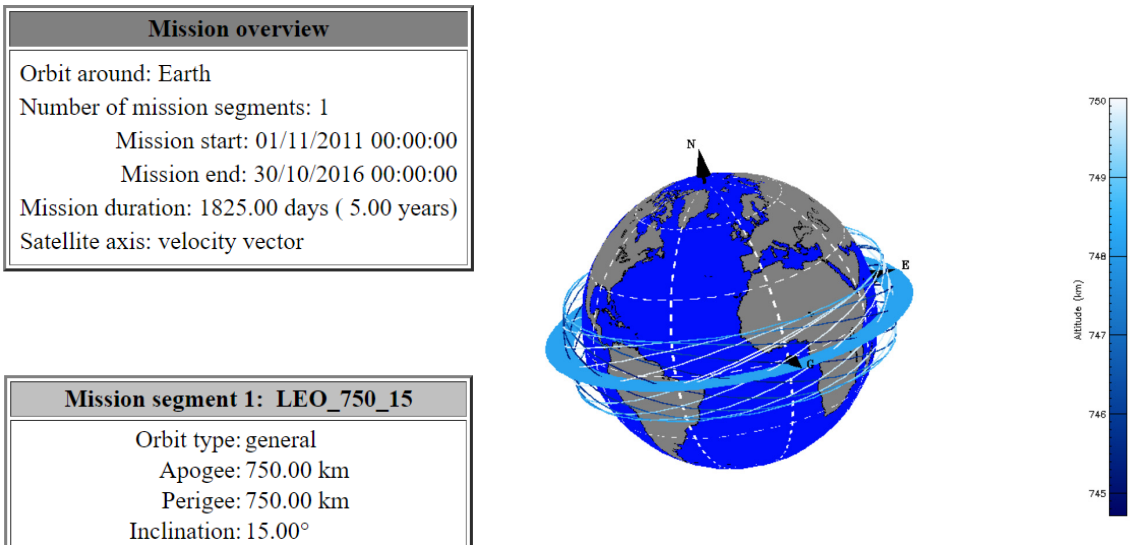


Figure 14. Orbital Parameter Report and 3D Graphic of Orbit at Altitude 750 km and Inclination 15°. Source: [21].

Figure 14 shows the mission overview on the left, indicating a circular orbit of 750 km and 15° inclination [21]. The image on the right is a 3D representation of the satellite's trajectory based on its orbital parameters. Table 5 lists the parameters set in the model to create the various orbits used to evaluate the TID at solar minimum and maximum.

Table 5. Coordinate Generator Model Parameters

Mission Start Date Solar Min:	01/06/2017
Mission Start Date Solar Max:	01/11/2011
Mission Duration:	5 years
Altitudes:	350, 500, 750, 1000 km
Inclinations:	0°, 15°, 30°, 45°, 60°, 75°, and 90°

The second subcomponent model calculates the trapped proton and electron fluxes in the radiation belts. We used the updated IRENE model (AP9/AE9) developed by the Air Force Research Laboratory; it incorporates over 60 years of satellite data from 45 different sensors [22]. The IRENE model predicts higher dose rates than previous radiation models (e.g., AP8/AE8) and is considered a more accurate representation of the radiation belts. A limitation of the earlier AP8/AE8 model was its inability to include trapped electrons in

the total ionizing dose calculation. Figure 15 shows the sunspot number from the last three solar cycles dating from March 1990 to March 2023, which indicates the phases of the solar cycle [23]. We used this graphic to select mission start times to represent the solar maximum and minimum periods. For solar maximum, we started the 5-year mission cycle on 1 December 2011, when solar activity was beginning to increase, and for solar minimum we started the 5-year mission cycle on 1 June 2017, when solar activity was nearing a low.

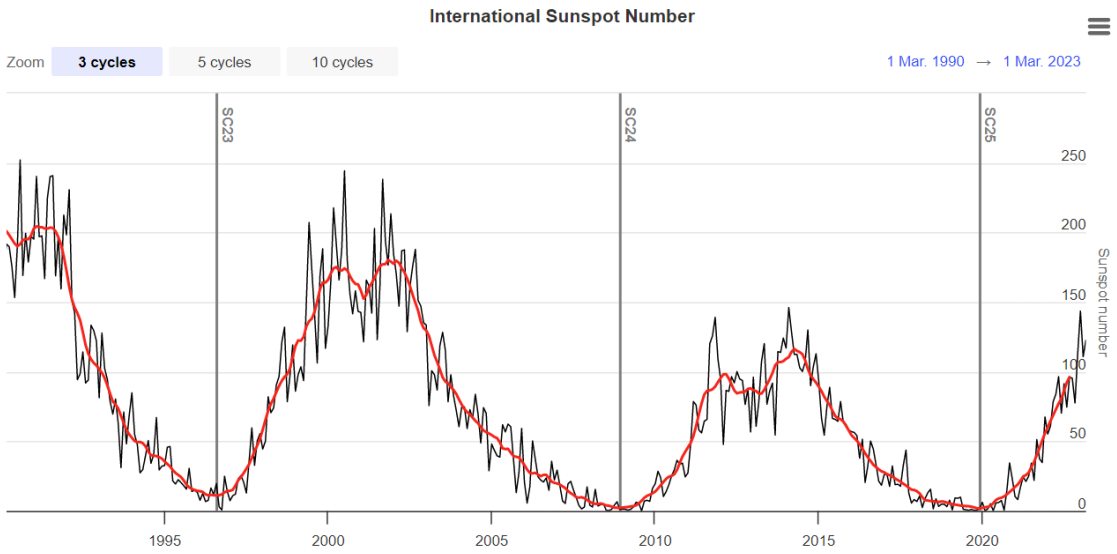


Figure 15. Solar Cycles Periods Evaluated in SPENVIS for Modeling TID Results. Source: [23].

For TID testing the IRENE model recommends using the "perturbed mean" feature, which runs multiple iterations from the orbital generator function as scenarios with the fluxes perturbed to account for uncertainties in measurements [22]. Table 6 shows the parameters used in the trapped proton and electron subcomponent model. As indicated, we used the latest version available in SPENVIS, "IRENE V1.5" with the default and Air Force Research Laboratory recommended settings.

Table 6. Trapped Proton and Electron Fluxes Parameters

Model:	IRENE
Model Version:	1.5
Model run mode:	Perturbed
Number. of runs (1-999):	20
Aggregate:	Mean
Energies:	Default SPENVIS Energies

The third SPENVIS subcomponent model calculates the solar particle mission fluences. The EPS-PSYCHIC model was developed specifically for integrated circuits and semiconductor parts to calculate the cumulative dose produced by solar heavy ions. The model allows the user to select a range of elements from the periodic table to include in the calculation; increasing the number of elements adds fidelity, but increases the model run time [24]. As indicated in Table 7, we included the full range from hydrogen (H) to uranium (U) and the rest of the settings were set to their default parameters.

Table 7. Solar Particle Mission Fluences Parameters

Solar Particle Model:	ESP-PSYCHIC (total fluence)
Ion range:	H to U
Prediction Period:	Automatic
Offset in solar cycle:	Automatic
Confidence Level:	95%
Magnetosphere:	Quiet
Shielding:	On
Directions:	All

The fourth subcomponent model calculates the effects caused by galactic cosmic rays (GCR). GCRs are energetic particles formed outside the solar system from space phenomena like supernovas [25]. The flux of GCRs reaches a peak during solar minimum, GCR particles have very high energies, but the probability of interacting with matter decreases with energy, so GCRs rarely contribute significantly to a satellite's total radiation dose [26]. The ISO 15390 model, developed by Moscow State University in 2004, was used because of its ability to estimate the radiation impact of galactic cosmic rays (GCR)

on semiconductor devices such as MOSFETs. Table 8 shows the settings used for the GCR subcomponent calculations.

Table 8. Galactic Cosmic Rays Parameters

Model:	15390
Magnetosphere:	Quiet
Shielding:	On
Directions:	All

The final SPENVIS subcomponent calculates the ionizing dose for simple geometries. It incorporates the results from the previous models to generate an estimate of the dose as a function of absorber thickness. Of the available options, we chose the ShieldDose-2 model because it is the newest model available in SPENVIS that is compatible with the IRENE models. This model only allows the user to choose Al as the shielding material; however, different materials, can be converted to an equivalent thickness of Al based on the material density [22]. Some examples of possible target materials include Si, GaAs, and SiO_2, which are useful for testing different types of MOSFETs with the referred gate oxides. Based on the target the user selects, the model calculates the absorption of radiation through the material. Table 9 lists the settings used to model the absorbed TID of a silicon device: 2mm thick Al spacecraft represents a bare part behind a typical spacecraft skin, while 4mm accounts for the spacecraft skin and an additional 2mm of Al shielding around the device.

Table 9. Ionizing Dose for Simple Geometries Model Parameters

Model:	ShieldDose-2
Target Material:	Si
Shielding Configuration:	Centre of Al
Material Thickness:	2mm, 4mm

C. OPTIMIZED ORBITS FOR INFINEON BSC060N10NS3GATMA1 MOSFET

The unshielded TID testing identified an absorbed radiation threshold of 7 krads for the Infineon MOSFET. This threshold applies, whether or not shielding is applied because the threshold refers to the absorbed dose. The SPENVIS model shows how shielding will impact the survivability of the device by predicting the TID absorbed in the material as a function of shielding thickness. The model generates a plot of "Dose in Si (rad) vs Aluminum Absorber Thickness." To correlate experimental results with a notional satellite mission, we assumed a baseline thickness of 2mm for the spacecraft skin. Thus, without shielding the radiation must penetrate 2mm of Al. To estimate the absorbed dose for a shielded device we included an additional 2mm of Al in the SPENVIS model, which resulted in a total thickness of 4 mm for the shielded scenario. The results from our earlier x-ray radiation test showed that adding Al reduced the degradation to the MOSFET, so we expected shielding would extend the survivability of the devices. SPENVIS allowed us to estimate the absorbed TID of the MOSFET for both the unshielded scenario and shielded scenario for various orbits.

Figures 16 shows the SPENVIS prediction of total absorbed ionizing dose as a function of satellite inclination for 5-year circular orbits ranging from 350 km to 750 km altitudes for an unshielded MOSFET. Solid lines indicate the result for solar minimum conditions while dashed lines represent solar maximum. Using these results, we can infer the ability of an unshielded Infineon MOSFET to survive under different orbital conditions. By overlaying the failure threshold of our worst performing device (B3) from the biased unshielded test, we can assess the altitudes and inclinations the Infineon MOSFET could survive for a 5-year mission life.

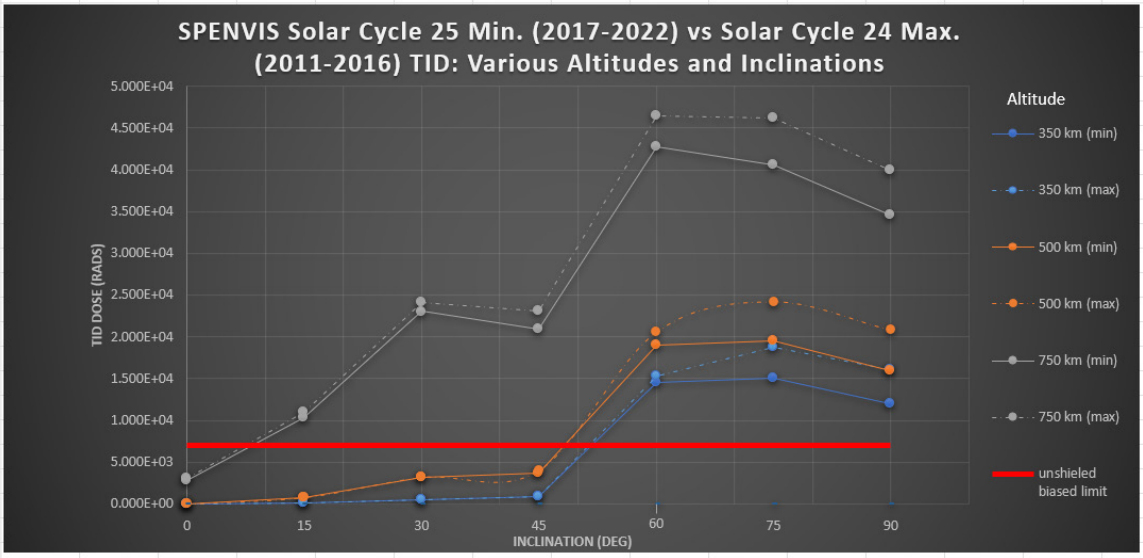


Figure 16. Total Ionizing Dose as a Function of Inclination Angle for Various Altitudes and Solar Conditions for an Unshielded MOSFET

The test results described previously saw an unshielded device fail after 7 krads of exposure; this threshold is indicated by a horizontal red line in Figure 16. Based on this threshold, we could expect an unshielded Infineon MOSFET to support 5-year missions up to 750 km altitude, but only for 0° inclination. At 500 km altitude, the device should support inclinations of 45° or less. These conclusions apply to both solar minimum and maximum.

The greatest factors in determining the cumulative radiation dose were the orbit altitude and inclination. The SPENVIS results show little difference between the cumulative dose at solar minimum and maximum. For all altitudes, the total dose increased between 0° to 30° inclination, likely due to the orbit spending more time in the South Atlantic Anomaly. This effect increased with altitude. Total dose increased again as the inclination reached 60°; this likely represents increased exposure in the high-latitude auroral oval. The dose for 90° inclination dropped slightly due to the lack of trapped particles over the poles.

Figure 17 shows the SPENVIS prediction of total absorbed ionizing dose as a function of satellite inclination for circular orbits altitude ranging from 350 km to 750 km with 2mm of additional Al shielding around the MOSFET. The same line styles and symbols were used as in Figure 16 to represent the absorbed TID for various orbits. Note

the y-axis in Figure 17 only extends to 14 krads, as opposed to Figure 16 which goes to 50 krads; this reflects the lower TID due to the additional shielding. As in Figure 16, the failure threshold of 7 krads is indicated by a solid red line.

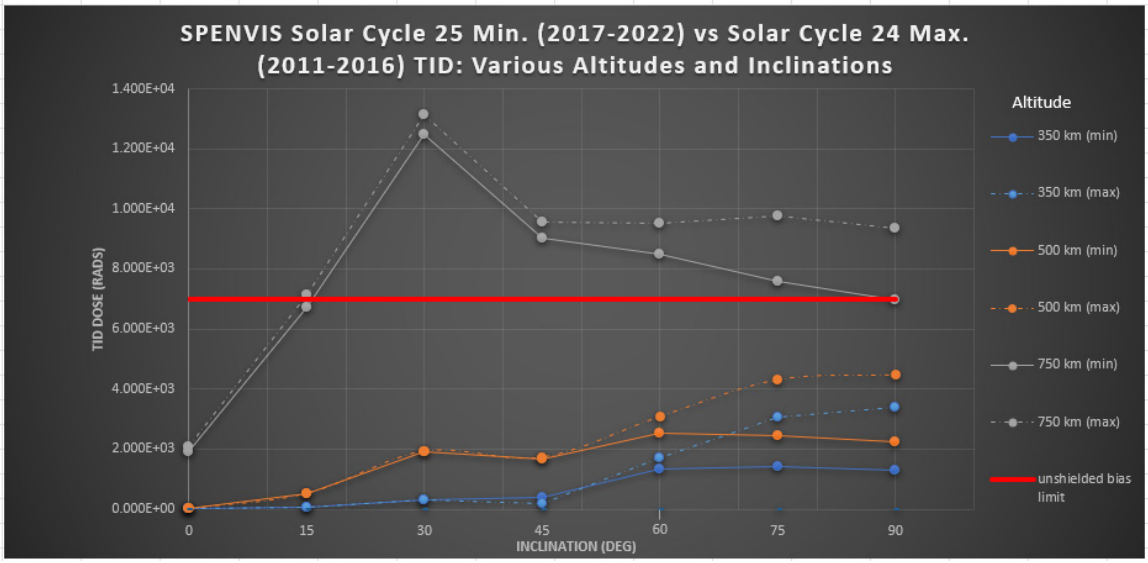


Figure 17. Total Ionizing Dose as a Function of Inclination Angle for Various Altitudes and Solar Conditions: Shielded MOSFET

Using the results shown in Figure 17, we can infer the ability of a shielded Infineon MOSFET to survive a 5-year mission under different orbital conditions. We could expect the Infineon MOSFET to survive orbits up 750 km at the equator for both solar minimum and solar maximum, and at 15°and 90° inclination during solar minimum. Orbits at altitudes of 500 km and below stayed below the failure threshold for all inclinations.

As expected, SPENVIS predicts a lower total absorbed dose as compared to the unshielded device; this difference ranges from a factor 1.5 to 4 depending on altitude and inclination. The largest reduction occurred above 45° inclination and at higher altitudes. Here the lower energy particles in the radiation belts and South Atlantic Anomaly are unable to penetrate through the increased Al shielding. Like the previous results in Figure 16, altitude was the most important factor to determining the absorbed TID; and again, little variation was observed between solar minimum and maximum.

As the orbit altitude and inclination increased, solar protons, and particles in the auroral oval were capable of penetrating through the Al, becoming the most important contribution to the cumulative dose. Although not shown in Figures 16 and 17, all orbits at 1000 km exceeded the failure threshold and would require additional shielding to survive a 5-year mission. The 1000 km results were not shown in order to focus on the altitudes and inclinations of where the MOSFET were predicted to survive, but the model results are tabulated in the third and fourth tables of Appendix B.

V. CONCLUSION

As LEO operations continue to grow it will be beneficial to conduct both TID and SEE testing of electronic parts. Although a MOSFET may operate without problems at one altitude and inclination, this does not guarantee it will survive at other orbits. SPENVIS modeling combined with the radiation testing reinforces this principle. We found that shielding is required for the Infineon MOSFET device to function at higher altitudes and inclination. The greatest factor in determining if a MOSFET will survive in a specific orbit was the altitude and the amount of shielding.

By analyzing a 5-year mission scenario in SPENVIS, our research showed that industries are taking more risks using commercial parts without accounting for the additional shielding required to support a mission's orbit. Our research indicates that the Infineon MOSFET device failed at extremely low TID, thus limiting where it could operate, even during solar minimum. Companies and government agencies should shift their focus towards the use of rad-hardened devices to ensure the long-term survival of their satellites or conduct the appropriate risk analysis if using commercial parts. By incorporating commercial parts, companies will need to account for the appropriate level of shielding to ensure parts do not fail. Our results suggest that 2mm of Al shielding would be insufficient for the Infineon MOSFET to operate at 1000 km altitude in any inclination over a 5-year mission life.

Our TID testing indicated the Infineon BSC060N10NS3GATMA1 power MOSFET with 2mm of Al shielding could support 5-years mission in orbits at 750 km at the equator for both solar minimum and solar maximum, and at 15°and 90° inclination during solar minimum. Orbits at altitudes of 500 km and below stayed below the failure threshold for all inclinations. However, further testing of the device’s susceptibility to single event effects is needed. Until SEE testing is complete, we cannot fully recommend this device during the peak periods of solar maximum. Facilities such as the Texas A&M Cyclotron could be utilized to conduct heavy ion testing to simulate an SEE. SEE testing can be paired with the Space Ionizing Radiation Environment and Effects (SIRE2) toolkit developed by Fifth Gait Technologies to model the space environment. NASA Goddard

gamma radiation facility can be used to compare the TID results to our x-ray testing. In addition, further research should expound upon the TID testing by evaluating the radiation effects at different V_{gs} biased frequencies and comparing the results of using gamma rays versus x-rays.

APPENDIX A. MANUFACTURER'S DATA SHEET EXCERPT

BSC060N10NS3 G

OptiMOS™3 Power-Transistor

Features

- Very low gate charge for high frequency applications
- Optimized for dc-dc conversion
- N-channel, normal level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC[1] for target application
- Halogen-free according to IEC61249-2-21

Product Summary

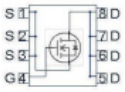
V_{DS}	100	V
$R_{DS(on),max}$	6	mΩ
I_D	90	A

PG-TDSON-8

RoHS

Halogen-Free

Type	Package	Marking
BSC060N10NS3 G	PG-TDSON-8	060N10NS



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C	90	A
		T_C=100 °C	66	
		T_A=25 °C, R_{thJA}=50 K/W[2]	14.9	
Pulsed drain current[3]	$I_{D,pulse}$	T_C=25 °C	360	
Avalanche energy, single pulse	E_{AS}	I_D=50 A, R_{GS}=25 Ω	230	mJ
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	125	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

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Source: [9]

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	1	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint	-	-	62	
		6 cm² cooling area[2)]	-	-	50	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=90 µA	2	2.7	3.5	
Zero gate voltage drain current	I_{DSS}	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C	-	0.01	1	µA
		V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=50 A	-	5.3	6	mΩ
		V_{GS}=6 V, I_D=25 A	-	6.6	11.5	
Gate resistance	R_G		-	1.6	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=50 A	43	85	-	S

[1)] J-STD20 and JESD22

[2)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3)] see figure 3

Source: [9]

APPENDIX B. TABULATED TEST AND MODELING RESULTS

	Figure 10. Unshielded Radiation Testing: Vth vs Dose								
	Absorbed Dose (krads)								
Vth (V)	0	1.08	6.7	10	15	20	25	30	Annealing
Control	2.8007	2.79687	2.79005	2.79899	2.7993	2.79748	2.78741	2.9274	2.8003
Grounded (G1)	2.8593	2.8188	2.58777	2.43203	2.2547	2.11618	1.98141	1.8588	1.88669
Grounded (G2)	2.8555	2.81557	2.58067	2.42487	2.24564	2.10381	1.95037	1.83237	1.8607
Grounded (G3)	2.9059	2.84564	2.60817	2.43961	2.2626	2.11176	1.96527	1.8417	1.87157
Biased (B1)	2.812	2.7093	2.20307	1.89432	1.53685	1.232333	1.42198	1.33367	1.34635
Biased (B2)	2.7322	2.662	2.30793	2.07126	1.8249	1.6017	1.33679	1.27097	1.30036
Biased (B3)	2.6606	2.5553	2.05213	1.74158	1.4115	1.11084	0.910378	0.849726	0.886913
Annealing	0 krad	60s= 1.08	332=6.768	224=10krad	278=15krad	278=20krad	278=25 krad	278=30 krad	

	Figure 12. Shielded Radiation Testing: Vth vs Exposure Dose												
	Exposure Dose (krads)												
Vth (V)	0	1.08	6.7	10	15	20	25	30	35	40	45	50	55
Control	2.80148	2.79991	2.80127	2.79792	2.7951	2.80157	2.8078	2.79688	2.80154	2.80229	2.80394	2.80558	2.81051
Grounded (G1)	2.73008	2.71893	2.64018	2.59726	2.52574	2.46974	2.41186	2.34136	2.30742	2.24693	2.20717	2.15048	2.11966
Grounded (G2)	2.91399	2.90203	2.8155	2.74822	2.68997	2.61625	2.55479	2.50539	2.4445	2.4011	2.33555	2.30027	2.224028
Grounded (G3)	2.67292	2.65425	2.58354	2.52953	2.47142	2.41275	2.34842	2.30701	2.25611	2.21033	2.1505	2.11892	2.07999
Biased (B1)	2.91505	2.88124	2.70511	2.57915	2.42311	2.24729	2.1214	2.01152	1.90733	1.81963	1.71427	1.59737	1.4832
Biased (B2)	2.80573	2.75723	2.61759	2.51044	2.44028	2.38693	2.32522	2.26803	2.22776	2.10719	2.0837	2.0161	1.90521
Biased (B3)	2.63258	2.61127	2.44386	2.33126	2.21191	2.04354	1.92895	1.8277	1.72268				

Figure 16. SPENVIS TID Predictions (Unshielded MOSFET)								
	Solar Min TID (rads)				Solar Min TID (rads)			
Inclination (deg)	350 km (min)	500 km (min)	750 km (min)	1000 km (min)	350 km (max)	500 km (max)	750 km (max)	1000 km (max)
0	9.967E-01	3.951E+01	2.813E+03	3.898E+04	1.043E+00	4.423E+01	3.083E+03	3.924E+04
15	7.796E+01	7.497E+02	1.031E+04	6.217E+04	8.396E+01	7.938E+02	1.092E+04	6.038E+04
30	4.868E+02	3.18E+03	2.303E+04	8.967E+04	4.883E+02	3.215E+03	2.413E+04	8.474E+04
45	8.965E+02	3.700E+03	2.091E+04	7.736E+04	8.662E+02	4.015E+03	2.310E+04	7.419E+04
60	1.456E+04	1.897E+04	4.277E+04	1.046E+05	1.530E+04	2.055E+04	4.642E+04	1.023E+05
75	1.507E+04	1.948E+04	4.056E+04	9.049E+04	1.873E+04	2.423E+04	4.623E+04	8.976E+04
90	1.202E+04	1.599E+04	3.454E+04	7.820E+04	1.608E+04	2.086E+04	3.996E+04	7.877E+04

Figure 17. SPENVIS TID Predictions (Shielded MOSFET)								
	Solar Min TID (rads)				Solar Min TID (rads)			
Inclination (deg)	350 km (min)	500 km (min)	750 km (min)	1000 km (min)	350 km (max)	500 km (max)	750 km (max)	1000 km (max)
0	7.017E-01	2.824E+01	1.896E+03	2.547E+04	7.338E-01	3.163E+01	2.077E+03	1.630E+04
15	5.404E+01	5.049E+02	6.724E+03	3.947E+04	5.806E+01	5.346E+02	7.121E+03	3.821E+04
30	3.093E+02	1.92E+03	1.250E+04	4.760E+04	3.126E+02	1.950E+03	1.312E+04	4.462E+04
45	3.757E+02	1.666E+03	9.038E+03	3.319E+04	1.800E+02	1.744E+03	9.557E+03	2.983E+04
60	1.322E+03	2.520E+03	8.497E+03	2.828E+04	1.723E+03	3.099E+03	9.540E+03	2.535E+04
75	1.404E+03	2.439E+03	7.573E+03	2.458E+04	3.059E+03	4.330E+03	9.757E+03	2.335E+04
90	1.306E+03	2.252E+03	6.965E+03	2.219E+04	3.395E+03	4.497E+03	9.375E+03	2.209E+04

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