NRL REPORT 3659

A VIDEO PULSE COUNTER

NAVAL RESEARCH LABORATORY

WASHINGTON, D.C.

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May 1, 1950

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ABSTRACT

As part of an investigation of the operation of a number of pulse sources on the same channel, a pulse counter has been designed which counts discrete video pulses. The maximum counting rate is two megacycles; the minimum counting rate is 25 cps. Each of six cascaded decade counter stages operates by storing pulse counts as capacitor charges. The counter operates for a crystal-controlled one-second interval, presenting the count it obtains on six panel meters. Each meter is calibrated from 0 to 9, there being one meter for each digit of the count.

PROBLEM STATUS

This is an interim report; work is continuing.

AUTHORIZATION

NRL Problem R07-29R
NR 507-290

A VIDEO PULSE COUNTER

INTRODUCTION

The pulse counter herein described was designed and constructed as part of a larger investigation of the operation of a number of pulse sources on the same channel. Two reports have already been written on this problem, one a mathematical analysis[1] and the second a description of the design and construction of a multiple video pulse generator[2] having 300 separate pulse sources of adjustable pulse length and recurrence rate, the pulses all being mixed and fed to one output. This generator, however, requires auxiliary equipment before it can be used to verify any mathematical analysis or analyze existing systems using a number of sources. The pulse counter described in this report is one of these auxiliary equipments.

The specifications on the output pulses of the multiple pulse generator are as follows:

Pulse length - 0.5 to 8.0 μ secs
Pulse rise time - 0.05 μ sec
No. of sources - 0 to 300
Recurrence rate - 20 to 400 cps per source

The counter, therefore, had to count approximately a total of 20 to 120,000 pulses per second (neglecting overlapping of pulses). In order to count all pulses it had to have a maximum counting rate greater than two megacycles, the reciprocal of the minimum pulse length, since nonoverlapped pulses will have random spacing down to zero time measured from the back of one pulse to the front of the next. A maximum counting rate of two megacycles also can be considered as a resolution time of 0.5 μ sec.

This problem might have been met by having each pulse draw a fixed charge through a meter calibrated in average recurrence rate, but with such an arrangement it is difficult to maintain a high degree of accuracy under the established recurrence rate and resolution time requirements. For this reason a pulse counter which could count in discrete numbers was decided upon.

Two types of such counters were considered: (a) the type which uses Eccles-Jordan circuits connected to form either a binary or decade counting system, and (b) the capacitor storage type, which has each pulse count stored as a capacitor charge.

Nearly all of the available literature discusses the first-named type, using Eccles-Jordan circuits. This system has reasonably high maximum counting rate, absolute accuracy within the limitations set by the resolution time, and, what is essential in so many cases, the ability to store a count indefinitely. However, it apparently is difficult to produce this type with a resolution time less than about two microseconds.

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[1] Ohman, G. P., "Average Pulse Relationships in High Pulse Density Systems," NRL Report R-3379, 4 November 1948 (Unclassified)

[2] Sheridan, J. P., "Multiple Pulse Generator," NRL Report R-3372, 21 October 1948 (Unclassified)

Since the counter to be used with the multiple pulse generator has only to sample pulses over short periods (in the order of a second or less) the indefinite storage time capabilities of the Eccles-Jordan type counter were unnecessary. Accordingly it was believed the resolution time requirements could probably be met more easily with a capacitor storage type counter, while maintaining the same absolute counting accuracy. A capacitor storage type counter was designed, built, and found to be capable of meeting the requirements.

GENERAL DESCRIPTION

Figure 1 is a panel photograph of the complete pulse counter. The upper section is the counter proper, the lower section containing power supplies and a monitor CR tube. The count obtained is read directly from the six panel meters.

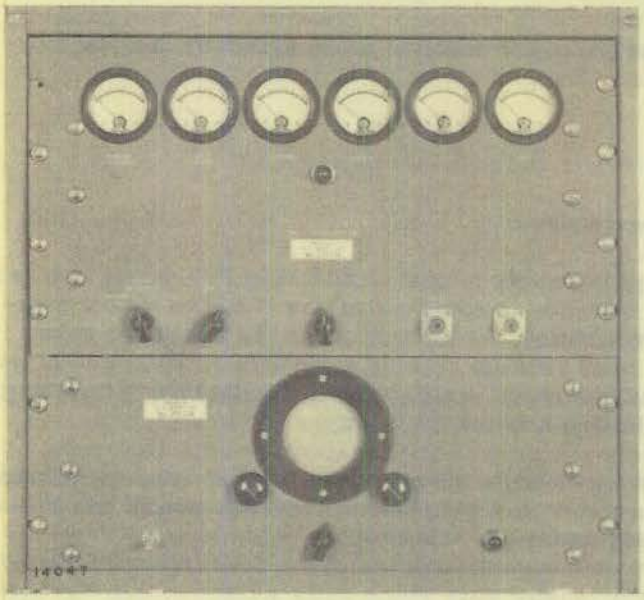

Figure 1 - Panel of pulse counter

Figure 2 is a block diagram of the pulse counter. The interval during which the circuit will count pulses is determined normally by a crystal-controlled counting interval timer. This interval starts shortly after the center panel switch marked CHECK-RESET-COUNT is thrown to the COUNT position. The interval is one second long with a percentage accuracy in the order of that of the crystal. No interval of less than a second is used since such an interval would aid little in speeding count measurements and would not allow as large a sample of pulses to be measured. Under the present requirement for minimum counting rate, longer intervals are not feasible. Provision is made for external pulse control of the counting interval, if this is ever desirable, rather than control by the crystal-controlled interval timer.

The output of the counting-interval timer is used to open a gate tube. This allows the input pulses that are to be counted to pass to the first of a cascaded series of six decade counters. The operation of each of the decade counters is basically the same.

Each of the randomly spaced input pulses to the first (or units) decade counter draws an approximately equal charge into a storage capacitor, building its potential up in jumps until the tenth pulse; the latter then discharges the capacitor to its initial zero-count condition. Each successive ten-pulse group repeats the process. Each time the first (or units) counter goes through a ten-pulse cycle it delivers a single pulse to the second (or tens) decade counter, this counter going through a similar cycle for every ten pulses fed it. Thus, the average recurrence rate is reduced by ten for each successive stage. All of the stages at any time during the count have a record of the total count at that time, the first stage the units, the second the tens (number of counts of tens), etc., to the last which counts the hundreds of thousands.

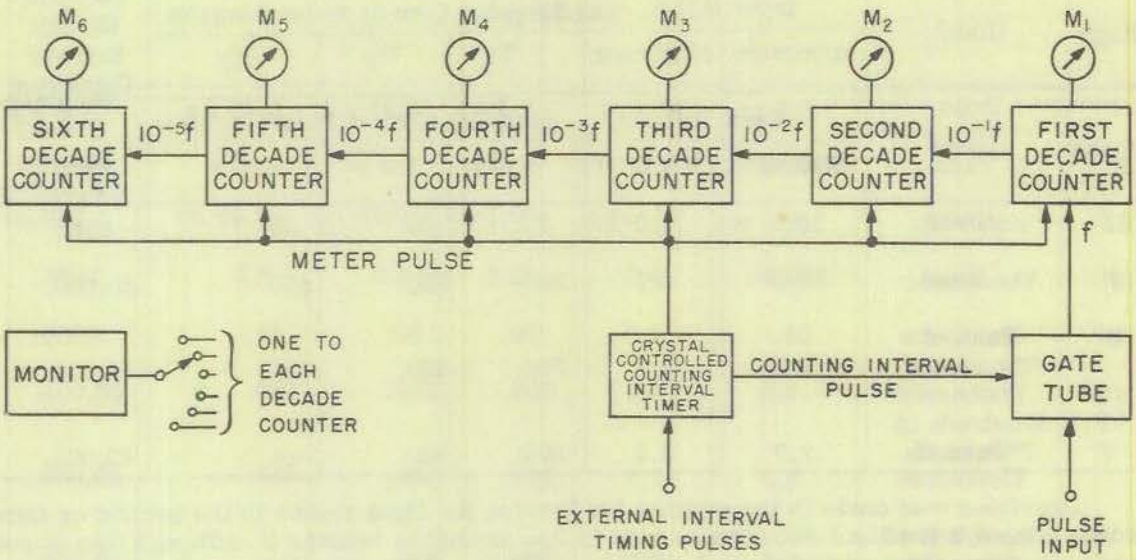

Figure 2 - Block diagram of pulse counter

In a counter using cascaded decade stages, the total maximum count is $C = 10^n$, where C = total count and n = number of cascaded decade stages. Therefore this counter is capable of counting 10^6, or one million pulses. This should not be confused with the maximum counting rate of 2 megacycles which is

$$F_m = \frac{1}{T_R}$$

where F_m = maximum counting rate and T_R = resolution time.

At the end of the counting interval, a pulse from the interval timer causes each meter circuit to measure the storage capacitor potential in the corresponding decade stage. There are six meters, therefore, calibrated from "0" to "9", which indicate the count obtained. At the end of a counting period the meters rise from zero to the count obtained and retain this reading for several minutes, even though the storage capacitors lose their charge.

To make another count, the main panel switch must first be thrown from COUNT to RESET in order to return the meters and storage capacitors to zero. Then, when the switch is thrown to COUNT, another counting period is started.

The maximum pulse recurrence rate which each decade stage can handle (the reciprocal of its resolution time) is listed in Table 1. In order to utilize the maximum counting rate capability of stage 1 the maximum counting rate of any stage must be

$$F_{m_N} \geq \frac{F_{m_1}}{10^N}$$

where F_{m_N} = maximum counting rate of Nth stage. Because of storage capacitor leakage current there is a minimum pulse recurrence rate each stage will handle. These figures are also listed in Table 1.

TABLE 1

Stage	Count	Input P.R.F.		Stepping Circuit Pulse Lengths			Stepping Circuit Storage Capacitor
		Maximum	Minimum	T_P	T'_P	T_d	
I	Units	2.0 mc	25. cps	0.3 μs	0.38 μs	0.45 μs	200. $\mu\mu$f
II	Tens	200 kc	1.5	3.0	3.8	4.5	2000.
III	Hundreds	20.	1.0	30.	38.	45.	6000.
IV	Thousands	2.0	0.7	300.	380.	450.	40,000.
V	Tens of Thousands	2.0	0.7	300.	380.	450.	40,000.
VI	Hundreds of Thousands	2.0	0.3	300.	380.	--	40,000.

Provision was made in the counter for feeding the input pulses to the second or third decade stages if the input recurrence rate is low enough to require it, although this is not necessary when the counter is used with the multiple pulse generator previously mentioned.

If the input pulses fed to the counter are from sources other than the multiple pulse generator and are shorter than the counter resolution time, there is a possibility the circuit will not count some of the pulses. In such a case the probable countdown or loss of pulses can be determined with the following equation:[3]

$$N_r = nF\,(1-FW)^{n-1}$$

where N_r = number of resulting pulses per second (after overlap),
n = number of pulse sources,
F = frequency of each source,
W = pulse length.

If this equation is used on completely random pulses, F must be set equal to the reciprocal of the counting interval with n equal to the total pulses to be counted in the interval.

W should be set equal to the counter resolution time and the equation solved first to give N_{rc}. N_{rc} alone will not be a true measure of countdown, however, since some of the original pulses will overlap in the source. The equation must be solved again for W set equal to the pulse length in the source to give N_{rg}, the actual number of pulses from the source in a second. Then,

$$\text{Countdown} = \frac{N_{rg} - N_{rc}}{N_{rg}} \times 100 \text{ percent.}$$

Percentage countdown increases as nF increases, and pulse length W decreases below the counter resolution time. If the pulse length W in the source is equal to or greater

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[3] Ohman, op. cit.

than the counter resolution time, $N_{rg} = N_{rc}$ and no countdown occurs. For purely random input pulses, the countdown probability is greater than if the pulses are not random. If the counting interval is increased, the countdown figure increases for random pulses and will decrease if the interval is reduced, providing nF is kept constant.

The main panel switch on the counter, when thrown to CHECK position, opens the gate which allows input pulses to feed through to the counter circuits. The counter stages run continuously in this condition and may be monitored on the 3FP7 CR tube which can be switched to any of the decade stages. The presentation, a vertical series of dots, is used in setting each stage to count ten and provides a quick and effective check on the proper operation of any stage. The CR tube can also be used in the same manner during a counting interval when the equipment is in COUNT position.

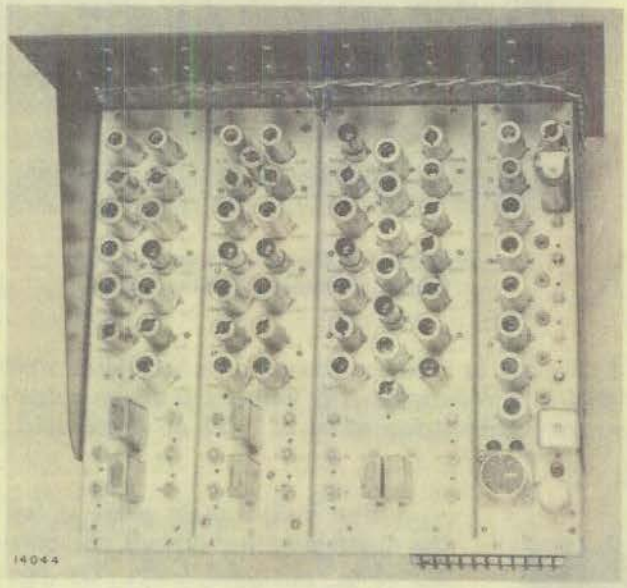

Figure 3 - Decade counters and interval timer, top view

Figures 3 and 4 are top and bottom views respectively of the decade counters and crystal-controlled counting interval timer. One sub-chassis contains the interval timer. Each of the other three sub-chassis contain two of the decade counters.

Figure 5 shows the chassis containing the power supplies and monitor unit. Around the CR tube is a double shield which is more than adequate protection against power supply fields. Three power transformers feed the positive and negative supplies. The main supply is regulated at +180 volts. Total power consumption of the unit is 400 watts.

CIRCUIT OPERATION

Decade Counters

All of the decade counter stages are fundamentally identical, Figure 6 being a block diagram of the basic decade state. Each of the randomly spaced input pulses triggers a single-shot multivibrator whose positive output pulse is held at a fixed amplitude and length for a given counter stage. Each successive positive pulse from the multivibrator (waveform (a) in Figure 6) charges a storage capacitor in a diode stepping circuit equally, thereby building the capacitor voltage up stepwise. After passing through two cascaded cathode followers, the step (waveform (b) in Figure 6) is fed to a second single-shot multivibrator which it keys on the tenth "step". The output pulse of this multivibrator fires a discharge tube across the storage capacitor in the diode stepping circuit, thus returning the capacitor voltage to zero. The discharge multivibrator pulse is also fed out to the following decade counter stage as a trigger pulse.

Thus, the typical decade counter goes through a repeating cycle in which ten randomly spaced input pulses produce one output pulse, there being a distinct capacitor voltage for each of the ten input pulses.

At the end of each counting period the input gate is closed, and a single 5000-microsecond pulse from the counting-interval timer operates the meter circuit, causing the meter to indicate the final count in that decade stage.

Since all of the decade counters are the same except for minor details, the operation of the third stage (Figure 8) may be taken as typical, the differences in the other stages being noted later. All six stages are shown schematically in Figures 7, 8, and 9. Waveforms in the third stage, typical of all stages, are shown in Figures 10a, 10b, and 10c. Table 1 lists waveform values for each decade stage, as well as other information discussed later.

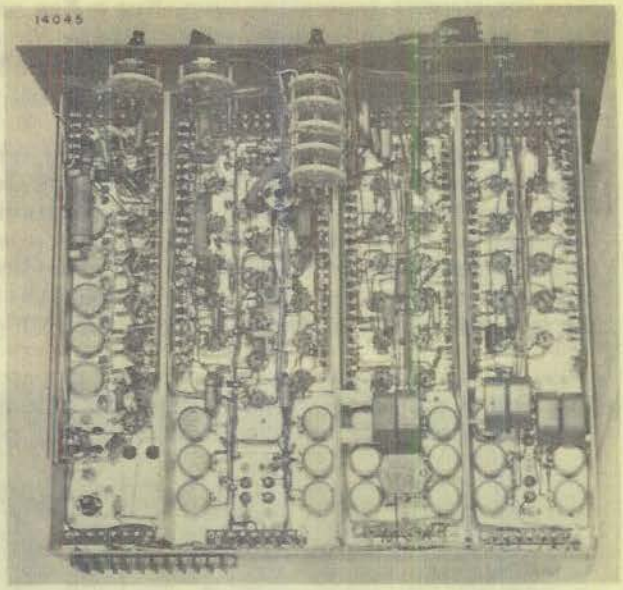

Figure 4 - Decade counters and interval timer, bottom view

The trigger pulses to the third decade counter, which are of constant amplitude and length, directly key the single-shot multivibrator V-21. The V-21B plate is held essentially at a regulated +105 volts between pulses by a V-22A. Since E_{bb} is a regulated +180 volts, a positive pulse of 75 volts is developed whose amplitude is essentially independent of V-21 or associated circuit component variations.

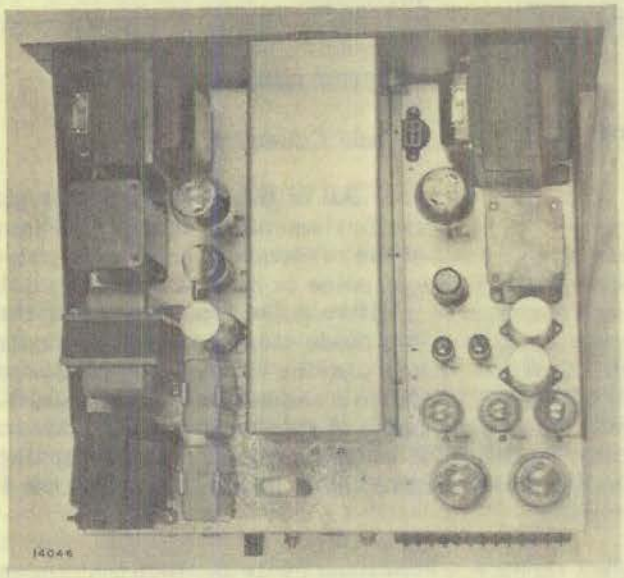

Figure 5 - Power supply and monitor chassis

The V-21B plate pulse is fed to the diode stepping circuit composed of V-23, V-24, and V-25. The operation of this circuit is illustrated in Figure 11. If a series of pulses of peak amplitude E_p is fed to the circuit at (a), the waveform at (b) will be produced across C_2. When E_p rises, C_1 and C_2 are charged through V_a, the charging time being designed to be less than the pulse length. The pulse voltage E_p is divided between the two condensers in inverse proportion to their capacitance. At the end of the pulse, C_1 will lose its previously gained charge through V_b, while C_2 retains its charge. On each succeeding pulse the process will repeat, except that the effective charging voltage will be $(E_p - E'_c)$. Thus, E'_c will have an envelope asymtotic to a value E_p.

The stepping circuit used in the pulse counter is the improved version

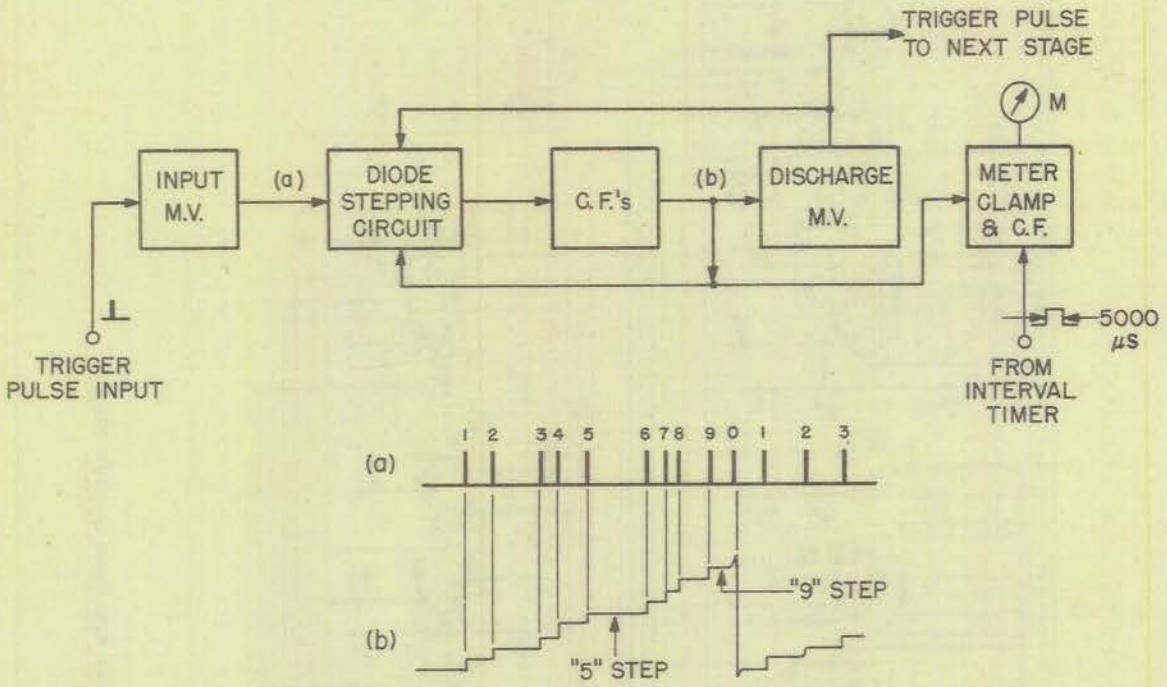

Figure 6 - Block Diagram of decade counter stage

shown at (c) with waveform at (d). The voltage E_c' in (a) cannot rise above E_p because the V_b plate is held at ground. In (c) the plate is made to rise simultaneously in nearly the same amount as E_c through the cathode follower action of V_c and V_d, thereby greatly increasing the value toward which E_c rises. Neglecting zero-bias limitations on the cathode follower action, the maximum voltage C_2 can have, or the value toward which the step voltage envelope will rise asymtotically, is

$$E_{cm} = \frac{E_p}{1-A}$$

where $A = \frac{dE_k}{dE_c}$ = constant,

providing $E_k = E_c$ when $E_c = O$. If E_k starts negative with respect to E_c, E_p is effectively reduced by this amount.

The gain, A, in (c) of Figure 11 can theoretically approach unity, under which conditions E_c would have an envelope with a very linear rise and could do so in that manner until the upper (zero bias) limit of the cathode follower were reached. With the circuit values used in the counter

$$A = 0.80$$
$$E_p = 75$$

$$\frac{E_p}{1-A} = \frac{75}{1.00-0.80} = 375V$$

In the third decade counter, V-23A is equivalent to V_a in Figure 11, while the 1N34 is equivalent to V_b. Two cathode followers are used, since the 1N34 peak current is high

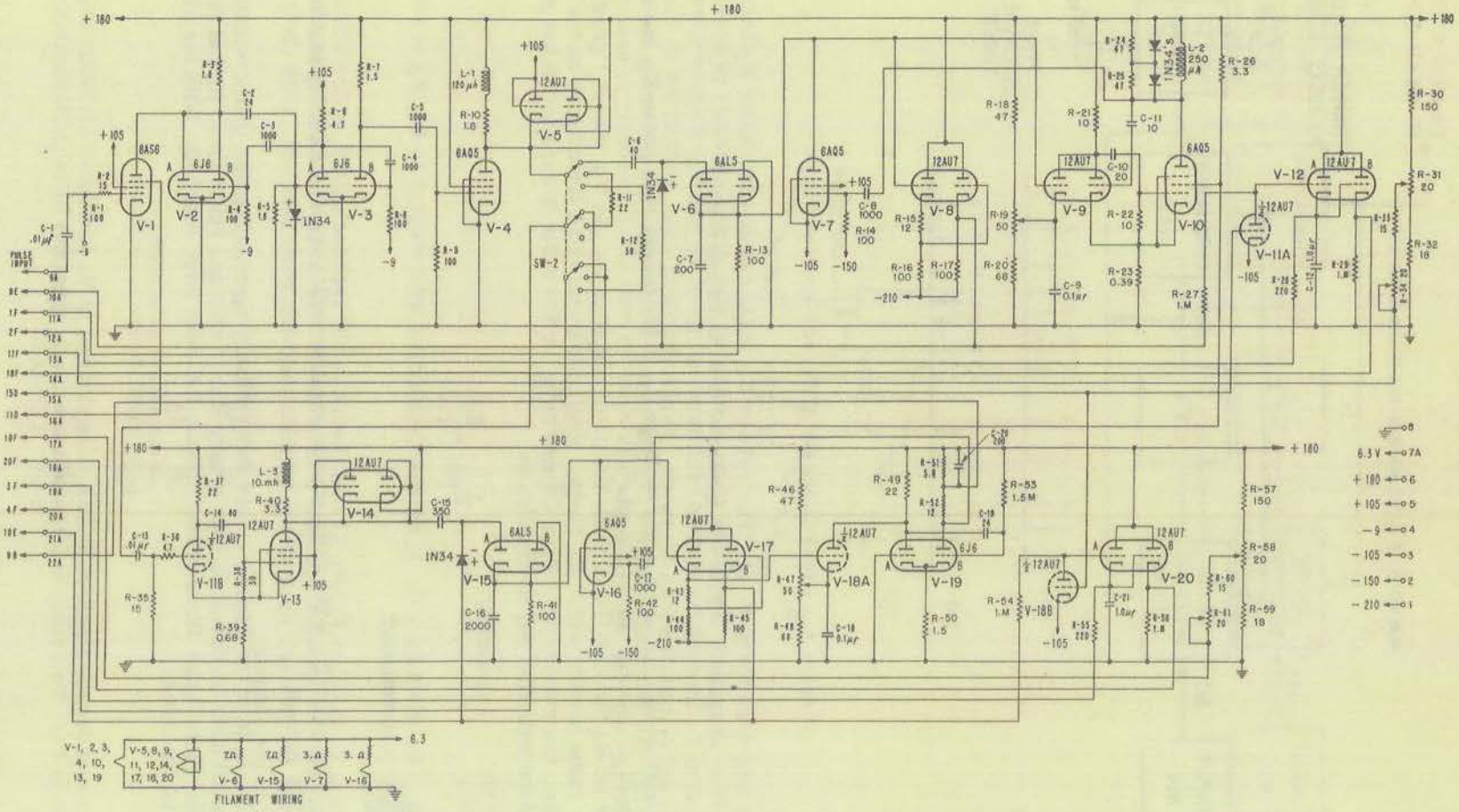

Figure 7 - Schematic of units and tens decade stages

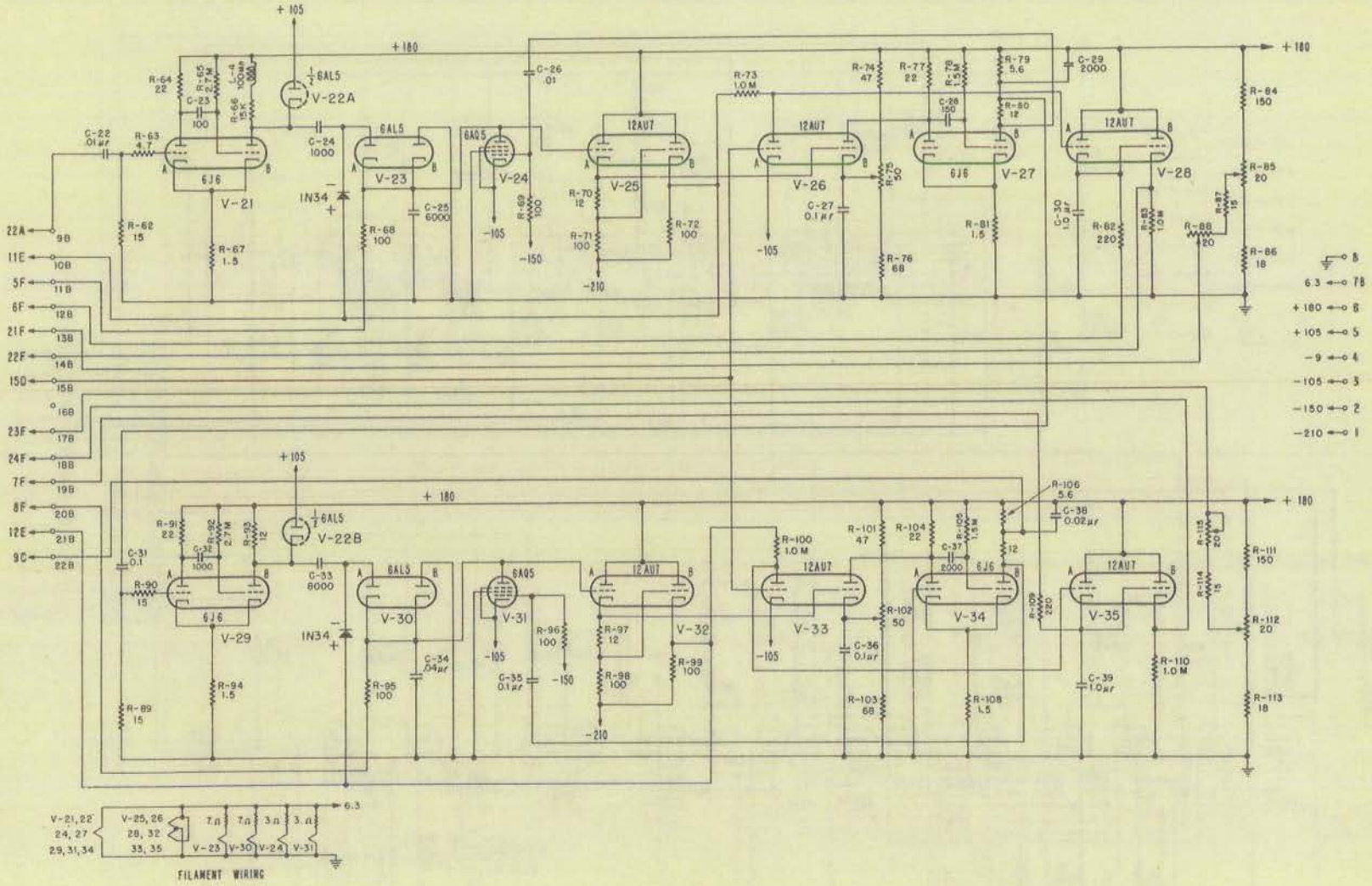

Figure 8 - Schematic of hundreds and thousands decade stages

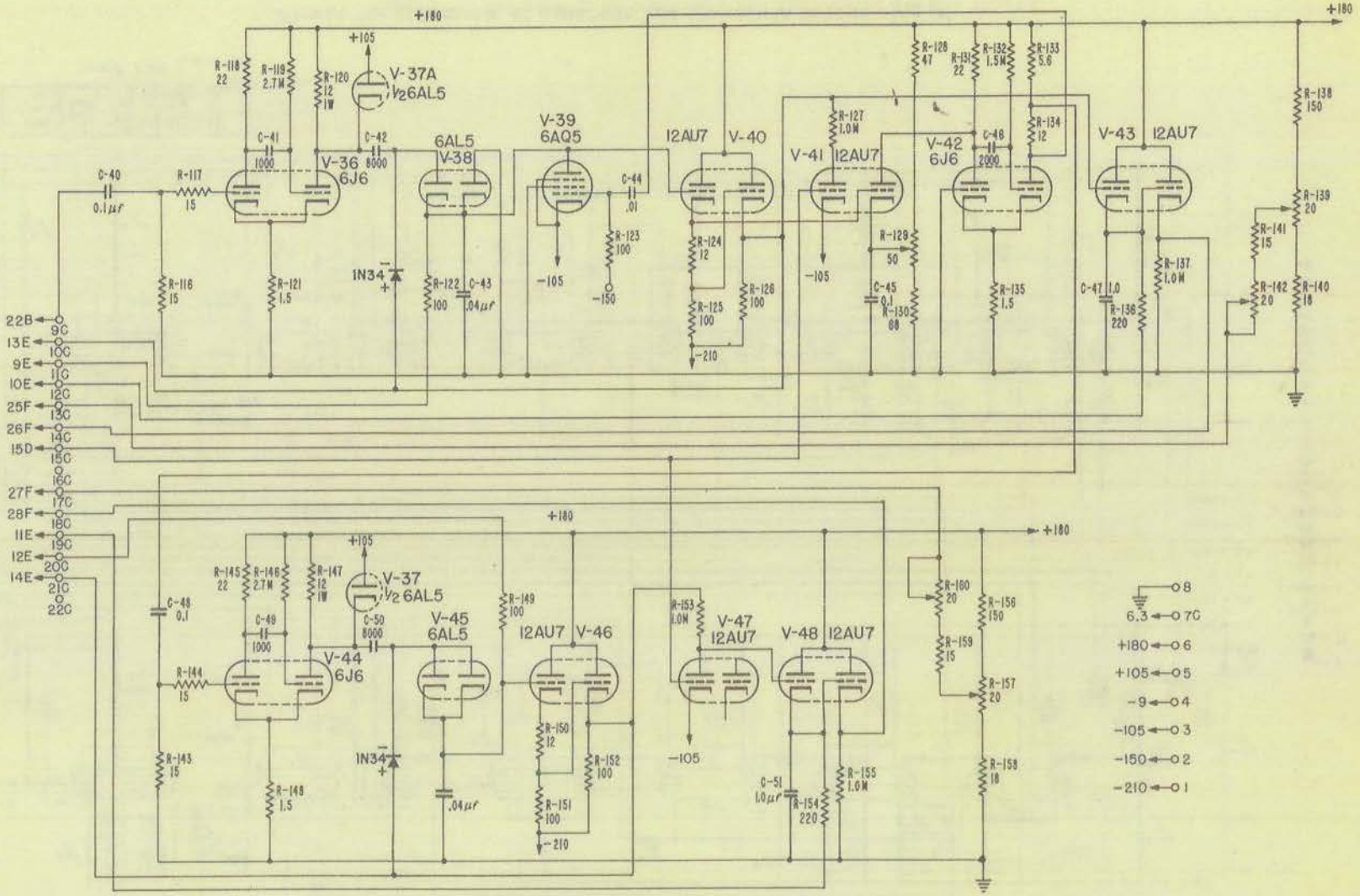

Figure 9 - Schematic of tens of thousands and hundreds of thousands decade stages

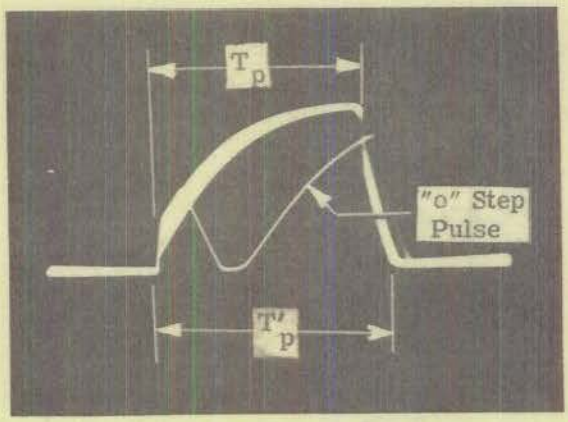

Figure 10(a) - V-21B plate waveform

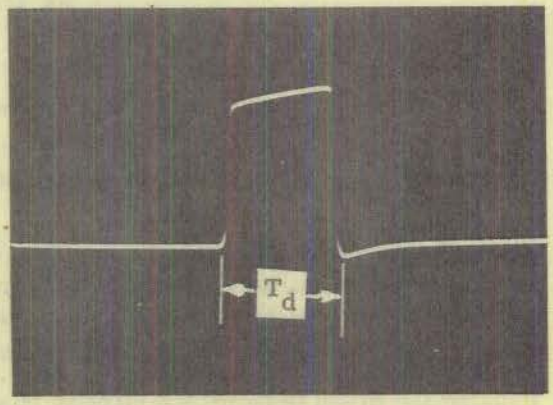

Figure 10(b) - V-27B plate waveform

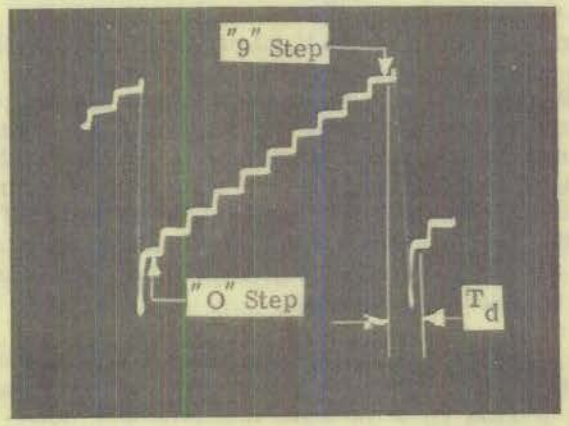

Figure 10(c) - V-25A cathode waveform

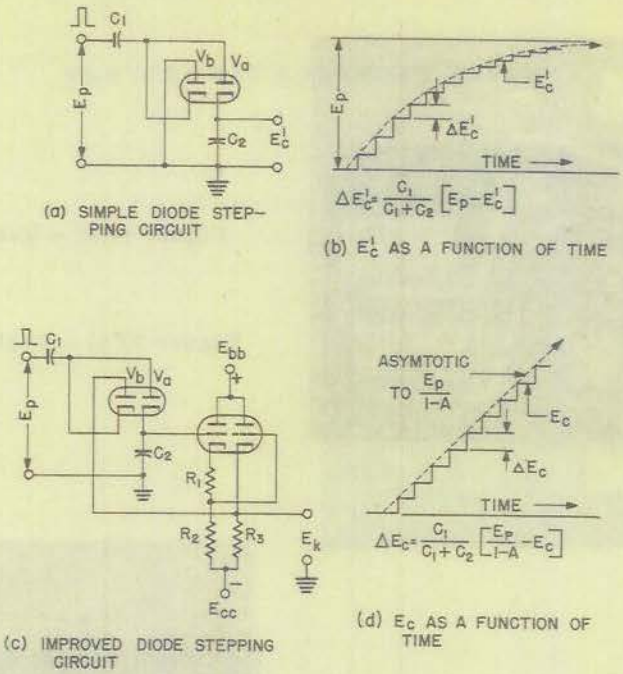

Figure 11 - Diode stepping circuit operation

enough to cause grid current flow in the cathode follower to which it is returned. If this were the first cathode follower V-25A, the storage capacitor charge would be upset. A resistor in series with the 1N34 would prevent this, but it would also increase the recharging or recovery time of the circuit. This would not be desirable since it would increase the resolution time of the decade counter stage. The relatively low cathode follower gain, while causing the steps to decrease slightly in size as the count goes from "0" to "9," is actually about ideal, as this nonlinearity is approximately balanced by a second tube nonlinearity in the meter circuits. This situation produces a desirable linear meter scale.

When the stepping circuit storage capacitor voltage at the V-23 cathodes rises to the tenth step, it causes V-26B to conduct. This in turn triggers the one-shot multivibrator V-27. The positive pulse output at the V-27B plate shown in Figure 10b drives discharge tube V-24 into conduction, allowing its plate current to discharge the stepping circuit storage capacitor C-25. The tenth step then is never realized but becomes the "0" step. This waveform is shown in Figure 10c. The storage capacitor discharge is at a constant current rate greater than necessary to obtain complete discharge in a time equal to the length of the discharge pulse. Diode V-23B prevents the discharge tube V-24 from pulling the storage capacitor C-25 potential much below the "0" step potential of ground. The C-25 potential recovers to ground when V-24 ceases to conduct plate current.

The waveform in Figure 10a is at the V-21B plate. The exponential rise time is due to the charging of the stepping circuit. All stages are so designed that the stepping circuit is greater than 98 percent charged during the period T_p of the input multivibrator pulse. Thus, any variation in pulse length T_p due to V-21 or associated circuit changes has negligible effect on the size of each step in the stepping circuit. The amplitude of the input multivibrator pulse in Figure 10a must be held constant to within 5 percent or the count in a stage will shift from the desired ten to nine or eleven.

The recovery time of the input multivibrator is (Tṕ-Tp) in (a) of Figure 11. This is the time during which the coupling condenser C-24 loses the charge it gained during the time Tp. The fall of the waveform (Figure 10a) has a sharp corner at the bottom because V-22A goes into conduction. V-22A thus not only stabilizes the amplitude value of the waveform but improves the recovery time of the input multivibrator circuit, a desirable feature since the maximum counting rate of the stage is equal to the reciprocal of Tp. The 100 K resistor at the V-23 cathode is connected to the CHECK-RESET-COUNT switch on the panel. It is grounded in the RESET position to return storage capacitor C-25 to "0" step condition. When in this condition the V-25B cathode is several volts less than ground, a condition necessary to prevent thermal energy diode current through V-23A and the 1N34, which would charge C-25.

The V-25B cathode potential is fed through a one-megohm resistor to the meter circuit composed of V-26A and V-28. Approximately 1000 microseconds after the end of a counting period a negative pulse of about 5000 microseconds duration is fed from the counting interval timer to the normally zero-biased V-26A grid. This pulse cuts off the V-26A plate current, unclamps the V-26A plate, and allows the V-28A grid to rise to the step potential of the V-26B cathode. V-28A charges the one-microfarad condenser C-30 in its cathode to a corresponding voltage, higher by an amount equal to the cutoff voltage of the tube. Thus, C-30 is charged to a voltage almost directly proportional to the final step voltage on C-25, the stepping circuit storage capacitor. Charging of C-30 is esstenially complete in 5000 microseconds. C-30 in the meter circuit in the third counter (and the other counters) has a leakage discharge time constant such that a "9" count decays to "8" in three minutes. The voltage across C-30 operates the cathode follower V-28B, while the V-28B cathode operates a one-milliampere meter as a voltmeter.

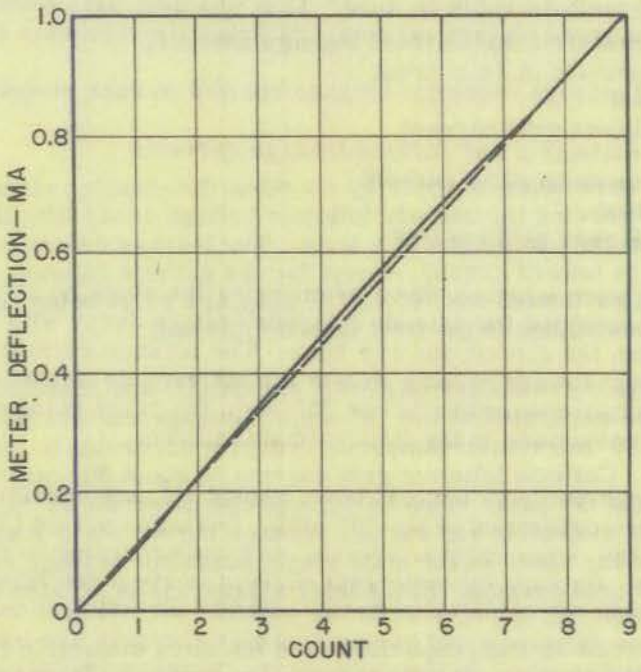

Figure 12 - Meter deflection vs. count

Two adjustments are provided, one a potentiometer for calibration of the meter at "0" count, the other a variable series resistor for calibration at the "9" count. Nonlinearity in the meter circuit tends to balance the stepping circuit nonlinearity and results in the curve of Figure 12.

All of the other decade counters have different input and discharge multivibrator pulse lengths, as indicated by Table 1. Also, as Figure 7 shows, the second decade counter input multivibrator uses different tubes than the later counter stages in order to produce a lower impedance pulse source to drive the stepping circuit.

In the units stage of Figure 7, the pulses to be counted are fed to the suppressor grid of V-1, a 6AS6 gate tube. The suppressor normally holds the tube cutoff, except during a counting interval when it is raised to zero bias. This allows the input pulses to operate the tube as a keyer for the multivibrator V-2/V-3A. Since conditions are possible where the input pulses would have a range of amplitudes, steps were taken to eliminate reproduction of any keying pulse existing in the multivibrator circuit when the input pulse was of insufficient amplitude to key the multivibrator. This was accomplished with clipper V-3B, which is biased beyond cutoff. Only pulses generated by the fully keyed multivibrator are large enough to drive V-3B into conduction. The V-3B negative plate pulse drives zero biased V-4 to cutoff to produce a positive 75-volt pulse at its plate to drive the stepping circuit.

As Table 1 shows, the period $T\acute{p}$, which is the resolution time of a decade stage, increases in each succeeding stage by a factor of ten. The fifth and sixth stages are exceptions, being the same as the fourth. Under the worst conditions possible, with pulses of a two-megacycle recurrence rate being fed to the pulse counter, each stage is able to operate on each pulse fed it. $T\acute{p}$ was made as large as possible in each of the first four stages so that large storage capacitors could be used. This was desirable since the greater the storage capacitance for a given leakage current, the lower the minimum counting rate possible.

The sources of storage capacitor leakage current in each stepping circuit are:

(1) Capacitor dielectric and surface leakage currents
(2) Discharge pentode plate current
(3) Diode current
(4) Cathode follower grid current.

Measurements were taken on these by charging the stepping circuit storage capacitor to the "9" step and observing the cathode follower voltage decay with the diode and discharge pentode removed from the circuit one at a time. The leakage currents discharge the storage capacitor in each stage toward ground, except for the cathode follower grid current which discharges the capacitor toward the "4" or "5" step, the value being controlled considerably by the total cathode resistance in the first cathode follower.

All of the leakage currents named above, except (1), are essentially the same in each decade stage and were calibrated at the "9" step. Leakage current (2) through each discharge pentode is roughly 150 micromicroamperes, varying according to the tube. Diode current is of the same order. Cathode follower grid current is about 800 micromicroamperes at the "9" step, with about the same value in the opposite direction at the "0" step or ground. The storage capacitor dielectric and surface leakage currents are least in the earlier stages, increasing with capacitor size. In the units stage, capacitor leakage current is much less than cathode follower grid current. In the later stages, (1) is greater than (2).

The stepping circuit storage capacitors are the mica dielectric type. A low-voltage capacitor is used in the first counter stage since the capacitor leakage current is small

compared to other leakage currents. In the last five stages, capacitor dielectric and surface leakage currents are a greater portion of the total leakage current; and these are minimized by the use of high-voltage mica stepping circuit storage capacitors.

The diode leakage current is a current flow from cathode to filament (electron flow from filament to cathode). Reduction of the diode filament potential from 6.3 to 4.4 volts reduced the diode leakage current to less than one hundredth of its former value without impairing the diode operation. Somewhat greater reduction could be realized by filament circuit isolation but was not considered worthwhile since the simpler filament voltage reduction brought the diode leakage current to a value reasonably small compared to other leakage currents.

Counting Interval Timer

A block diagram of the crystal-controlled counting interval timer is shown in Figure 13. The output of a 100-kc crystal oscillator is clipped to produce pulses spaced ten microseconds. These pulses are fed to a chain of five free-running multivibrators each of which delivers pulses at a recurrence rate one tenth of that of the synchronizing input pulses.

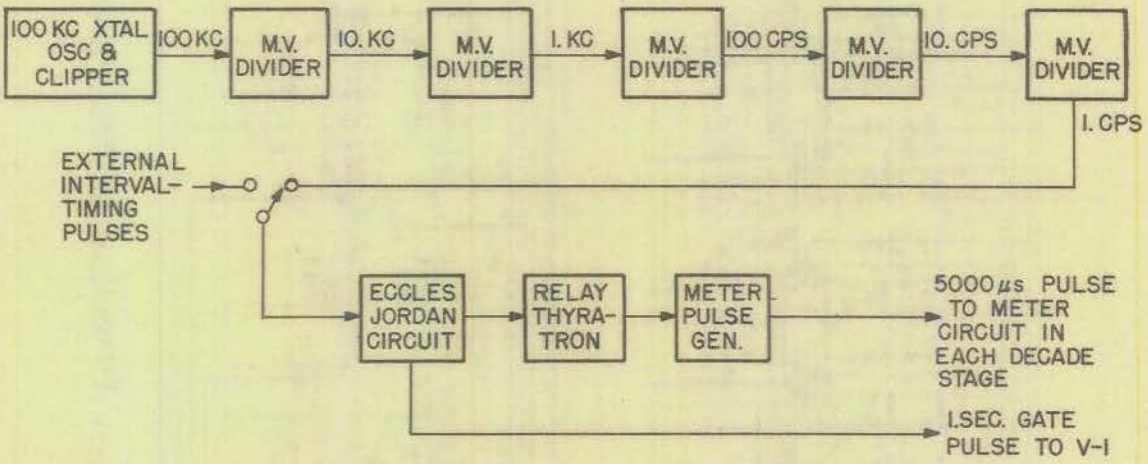

Figure 13 - Block diagram of counting interval timer

The last multivibrator divider delivers one pulse per second continuously to an Eccles-Jordan circuit. The CHECK-RESET-COUNT switch when in RESET holds the Eccles-Jordan circuit in the first of its two steady states. When the switch is thrown to COUNT, the next two pulses from the last multivibrator divider trigger the Eccles-Jordan circuit to its second steady state and then back to its first. This generates a single square pulse one second long which operates the gate tube V-1 in the first (or units) decade counter. The Eccles-Jordan circuit is prevented from being triggered by later divider pulses by thyratron operation of a relay at the end of the one-second gate pulse. The thyratron operation also triggers a single shot multivibrator which delivers a pulse to operate the meter circuits in each of the counter circuits.

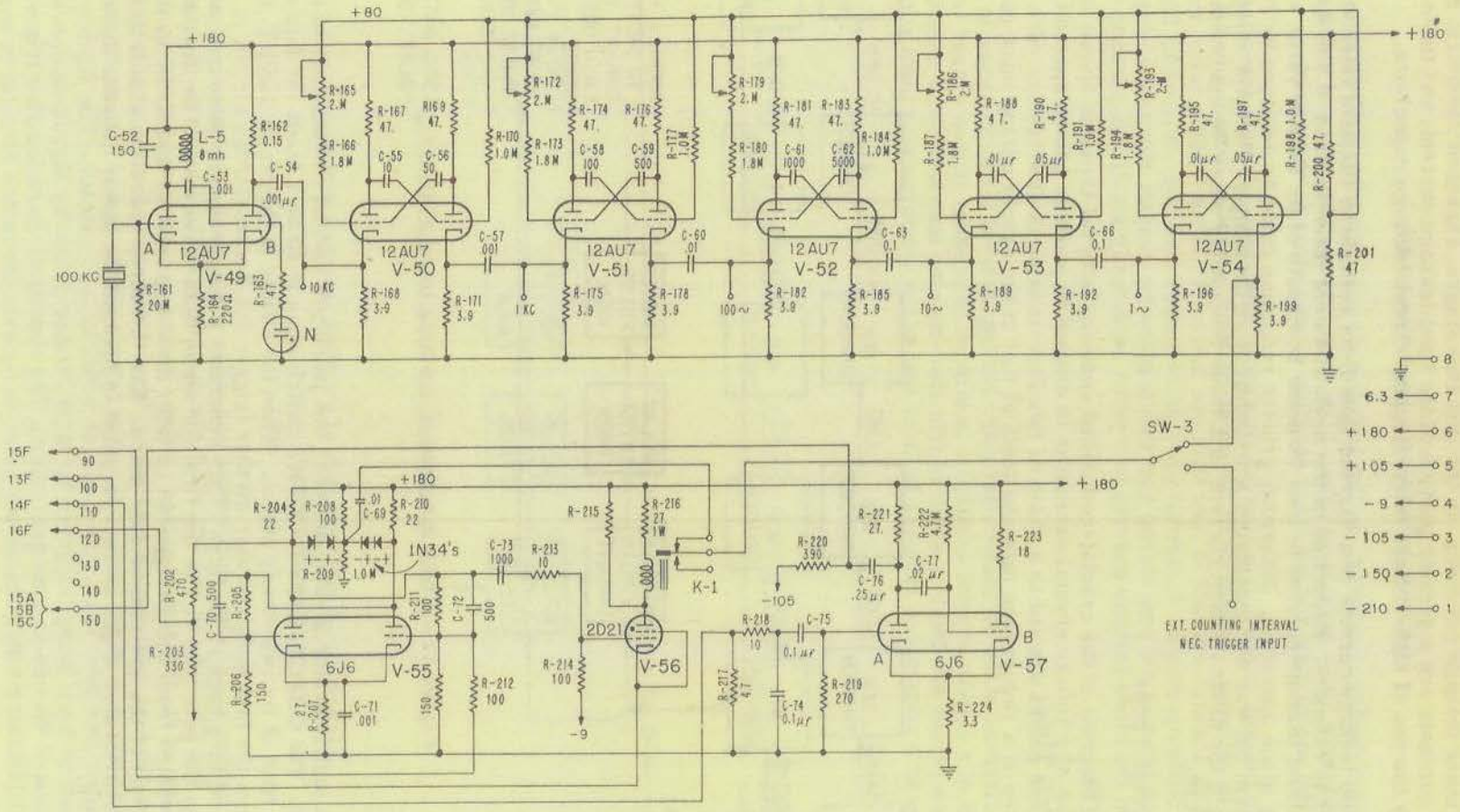

Figure 14 - Schematic of counting interval timer

The schematic diagram of the counting interval timer is shown in Figure 14. V-49A is a 100-kilocycle triode crystal oscillator whose r-f plate output drives V-49B as a class C amplifier. The V-49B grid current lights the neon bulb in the grid circuit. This bulb is mounted back of a panel jewel to indicate operation of the oscillator, since oscillator failure would produce inaccurate counting interval times. The plate waveform of V-49B due to class C operation is a series of negative pulses which are peaks of a sinewave. These are shown at (a) in Figure 15.

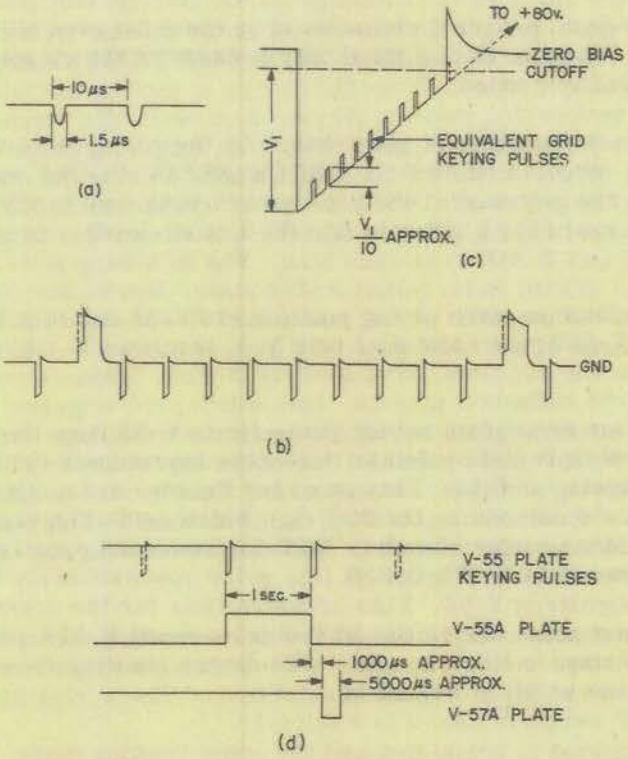

Figure 15 - Counting interval timer waveforms

All of the multivibrator dividers, V-50 to V-54 inclusive, operate alike and have identical circuit values except for the capacitors which determine the multivibrator frequency. The operation of a single divider is typical of all five.

Waveform (b), Figure 15, is that existing on the first cathode. The negative pulses are coupled capacitively from the previous stage for triggering. The wider positive pulses occur because of conduction of the first triode in the multivibrator. This period, determined in the second triode grid circuit, is slightly less than the period between successive triggering pulses. The first triode grid circuit period would be about 5 percent greater than ten periods of the input pulses were the latter not present. The negative cathode triggering pulses are equivalent to positive grid triggering pulses as shown in (c) of Figure 15. Grid circuit time constants and trigger pulse amplitudes are such that every tenth trigger pulse forces the first triode into conduction, ending the first triode grid circuit recovery slightly before it would naturally end itself. The trigger pulses are about one tenth the amplitude V_1 in (c) of Figure 15, which is about optimum. Smaller trigger pulse amplitudes would

allow values of grid time constants which would not be controlled by the trigger pulses. (The grid voltage would arrive at cutoff between trigger pulses.) Larger trigger pulse amplitudes would not improve the synchronization, but the percentage change in trigger pulse amplitude necessary to change the division from 10 to 9 or 11 would be less, which is undesirable.

The second cathode pulse of each stage provides triggering for the following stage. The division in each stage is initially adjusted with a variable grid resistor. This can be done most easily with the aid of an oscilloscope on the cathode test points. The stability of the dividers is very good, proper division being maintained even with large variations in the B supply. The +180 volts is regulated only because of the stepping circuit pulse generators in the decade counter stages.

V-55 is an Eccles-Jordan circuit plate-keyed by the pulses occurring once every second fed from V-58. When in RESET the CHECK-RESET-COUNT switch holds V-55B cut off by returning R-212 to ground. When the switch is thrown to COUNT, R-212 is ungrounded, allowing the next keying pulse to flip the Eccles-Jordan circuit to the stable state where V-55A is cut off and V-55B is at zero bias. The following plate keying pulse reverses this to place the circuit in its initial stable state. During the one-second period between these two pulses, the potential at the junction of R-202 and R-203 is raised, and, since it is tied to the suppressor of the 6AS6 gate tube V-1, it allows V-1 to pass pulses impressed on its control grid.

When the second effective plate keying pulse fed to V-55 flips the Eccles-Jordan circuit, the differentiated V-55B plate potential rise keys thyratron V-56 into conduction. Relay K-1 opens, preventing additional keying of the Eccles-Jordan circuit. The firing of V-56 produces at the V-56 cathode a potential rise which grid-triggers the single-shot multivibrator V-57 to produce an approximately 5000-microsecond negative pulse at the V-57A plate. The RC grid network in V-57A delays this pulse approximately 1000 microseconds after the firing of the thyratron V-56. This provides time for the counting stages to complete the count of the last pulse before the 5000-microsecond V-57A plate pulse operates each of the six counter stage meter circuits. Waveforms showing the operation of V-55, V-56, and V-57 are shown at (d) in Figure 15.

After a counting period is completed and the count reading made, the CHECK-RESET-COUNT switch can be thrown to RESET, which will extinguish thyratron V-56 and close K-1 to return the circuit to the initially described conditions. The wiring diagram for the CHECK-RESET-COUNT switch is shown in Figure 16.

Monitor Oscilloscope and Power Supplies

In order to provide a convenient check on the proper operation of any of the six decade counters, a monitor oscilloscope is included. The schematic is shown in Figure 17. A half-wave transformer supply provides positive and negative voltages to operate a 3FP7 long-persistence cathode-ray tube. The stepping circuit cathode follower waveform of any stage is fed to one "vertical" and one "horizontal" deflecting plate tied together to increase deflection sensitivity. No sweep is used, the presentation being a vertical series of ten dots or spots, one for each step, as shown in Figure 18.

When the monitor is used on the earlier counter stages the counting rate of these stages is usually high enough to allow ten spots to be seen at the same time without any need for a long-persistence P-7 screen. However, the later counter stages normally operate at such low counting rates that a long-persistence screen is needed.

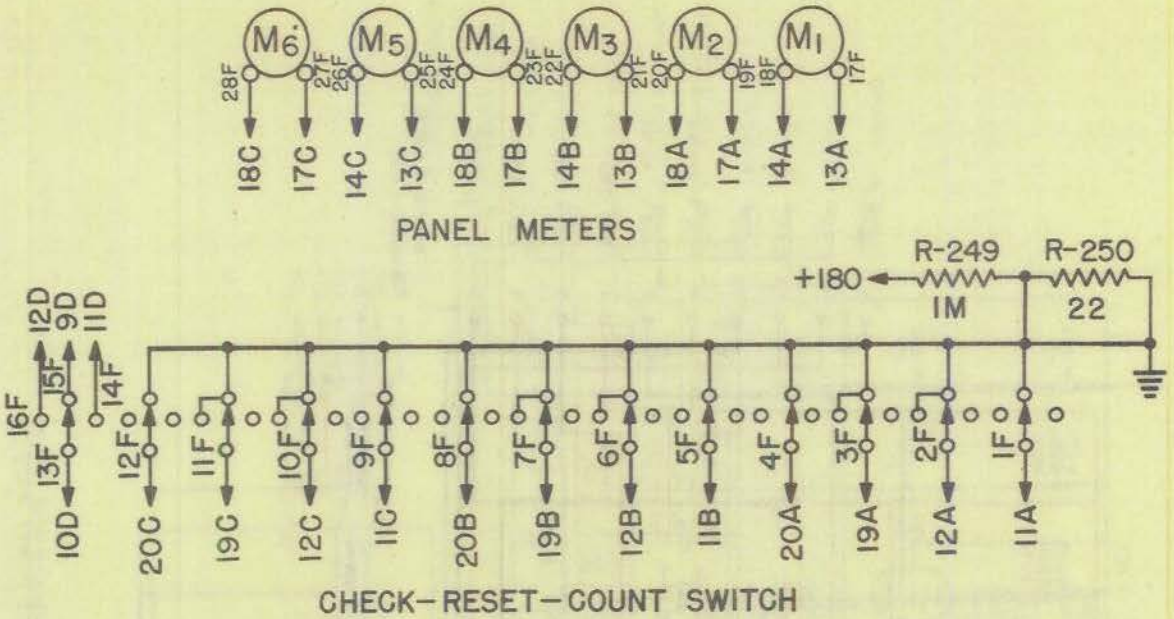

Figure 16 - Panel wiring

Brilliance and focus controls are on the front panel while a screwdriver-adjusted vertical centering control is on the back of the chassis. A portion of the step waveform is fed to the second anode to minimize defocusing due to unbalanced feeding of the deflection plates.

Figure 17, besides presenting the cathode-ray tube circuit, is also the schematic for the power supplies. Two power transformers, T1 and T2, feed two low-voltage rectifiers, filters, and series regulator circuits whose outputs are tied in parallel to deliver 265 milliamperes at a regulated +180 volts. A single 6SJ7 d-c voltage amplifier is used in the regulator circuit for both series regulators. Because T2, in addition to supplying V-64, also furnishes power to the negative supply, the V-63 series regulator is made to deliver more current than the V-64 regulator. Regulation of the negative supply is accomplished by two VR tubes.

T3 supplies filament power to the units and tens counter stages, the counting interval timer drawing filament power from T1 and T2.

CONCLUSIONS

It can be seen that the maximum and minimum counting rate capabilities of a capacitor storage type pulse counter are dependent upon the stepping circuit storage capacitor size, the storage capacitor leakage current, and the driving pulse generator impedance. For a low minimum counting rate large storage capacitance is desirable so as to make capacitor dielectric current (1) (p. 14) large compared to the external leakage currents (2), (3), and (4). The ultimate minimum counting rate depends, therefore, upon storage capacitor quality (capacitance times leakage resistance). If the storage capacitor is large enough, the external leakage currents will have neglibible effect on the minimum counting rate. Step waveform amplitude should have little effect on minimum counting rates.

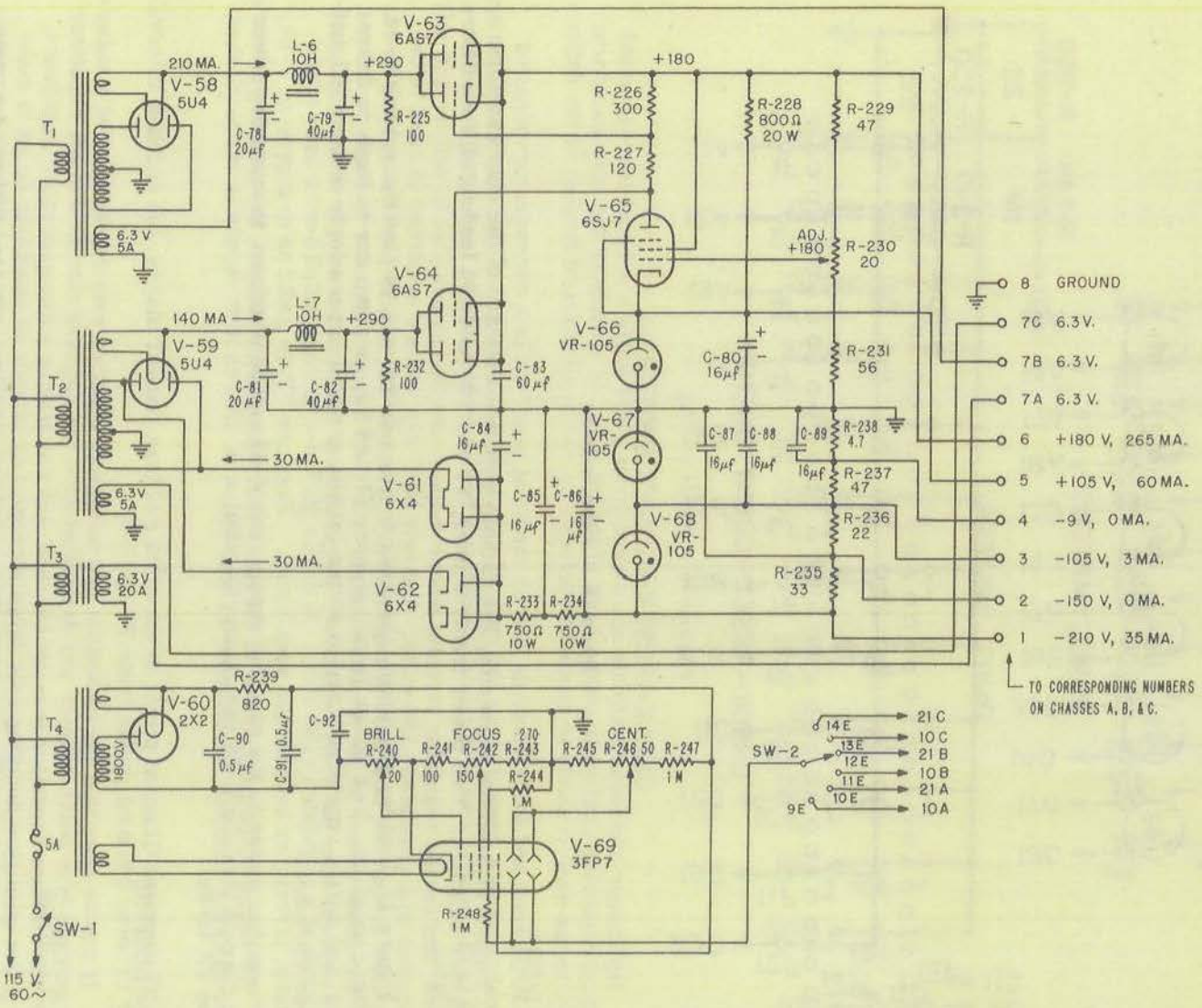

Figure 17 - Schematic of C.R. monitor and power supply

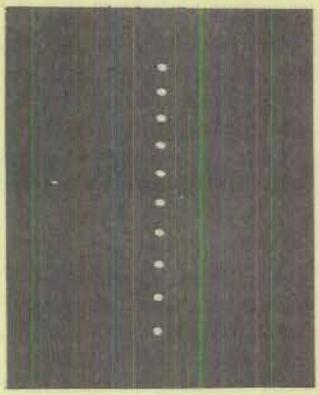

Figure 18 - Monitor presentation

The maximum counting rate of a stage depends upon the time required for the stepping circuit to charge the storage capacitor and recover for the following pulse. Small storage capacitance and a low impedance driving pulse generator are therefore desirable to attain higher counting rates. Small step amplitude is also desirable since this means a more easily generated smaller driving pulse.

The design of a storage capacitor type pulse counter involves a compromise if an attempt is made to maintain a low minimum counting rate. The counter described in this report was designed to count at a 2-megacycle rate and at the same time to have as low a minimum counting rate as was possible without unreasonable extremes of design. Possible improvements suggest themselves. A cathode follower after each amplitude-regulated m.v. pulse generator to drive each stepping circuit would provide a lower impedance pulse source and allow greater maximum or lower minimum counting rates. A smaller driving pulse amplitude could be used while maintaining the same step amplitude, the increased nonlinearity being offset by replacement of 12AU7's with higher $-\mu$ 12AT7's.

The counter described has a defect in that the stepping circuit storage capacitors are ungrounded when the panel switch is thrown to COUNT, but the counting period does not start until after an interval of up to one second. This is detrimental to the first stage only, where leakage current sometimes pulls the storage capacitor potential as high as the "1" step before the counting interval commences, giving an erroneous extra count. If a decade stage were used with less storage capacitance or greater external leakage currents than the first decade stage in the described counter, it would be desirable to have the storage capacitance ungrounded at the start of the counting interval.

It should be possible to design a decade counter stage with a maximum counting rate above the 2-megacycle maximum. However, the first decade stage of the present counter has a means of selecting, on an amplitude basis, which input pulses are counted and which are not. For those counted, pulses of constant amplitude are generated to drive the stepping circuit. This is done by V-2 and V-3, as already discussed. This feature would become increasingly difficult if the maximum counting rate were raised. However, the input pulses could be amplified, clipped, and used directly as a pulse source for the stepping circuit.

ACKNOWLEDGMENT

The author wishes to thank G. P. Ohman, W. L. Roberts, and J. W. Bryan for their valuable aid given during the development of this counter.

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