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AN AMPLITUDE-DISTRIBUTION ANALYZER

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ABSTRACT

Amplitude-distribution density, one of the important statistical properties of a signal, represents the relative probability of existence of different instantaneous signal levels. An automatic analyzer capable of rapid, moderately accurate computations was needed to determine this function for numerous recorded signal and noise samples and for quantitative comparison of their significant characteristics. Direct solution by any mechanical or electrical device involves scanning over the appropriate amplitude ranges with an integrating detector that has a response proportional to the total time that a given level is occupied by the signal. If results are to be absolutely accurate, integration must be performed for an infinitely narrow amplitude slice; but since this implies infinitely high detector sensitivity, all practical systems represent some compromise.

Because none of the techniques used in the past to obtain complete distribution densities appeared to fulfill present requirements, a new analog analyzer was developed. This equipment requires no storage devices or other special components and employs only standard receiving tubes to effect a comparison between the instantaneous signal level and a variable reference voltage. Distribution densities are computed and automatically plotted for any signal or noise voltage that can be applied to the input terminals at a 12-v level, or greater, peak-to-peak. Response is uniform for frequency components from dc to 1000 cps. When the input is a recorded signal sample repeated continuously at 1/3 cps, the total plotting time is about ten minutes. Plotted values for distribution densities are obtained by scanning the desired range of levels with an amplitude aperture that has a width of 1% of the peak-to-peak signal. Over-all accuracy of the system, including the output recorder, is about ± 5% when referred to that of an ideal device that employs the same finite aperture width. The inherent error in the use of the finite aperture depends upon the extent to which the density function varies within the aperture width and has been computed for the extreme case represented by a sinusoidal signal.

PROBLEM STATUS

This is an interim report on one phase of this problem; work on other phases is continuing.

AUTHORIZATION

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AN AMPLITUDE-DISTRIBUTION ANALYZER

INTRODUCTION

Whenever recent statistical theories of communication are applied to system design problems, statistical properties of signal and noise sources are of major interest. Two important functions are the amplitude-distribution function and the amplitude-distribution density. For a function of time, f(t), the amplitude distribution is defined as the probability that the instantaneous amplitude lies below the level x.

$$p(x) = \text{Probability}\ \left[f(t) \leq x\right]. \qquad (1)$$

The distribution density is the derivative of the distribution function or the relative probability that the signal amplitude lies within an infinitely narrow range of amplitudes centered about the level x.

$$p(x) = \text{Probability}\ \left[x < f(t) < x + dx\right]. \qquad (2)$$

The equipment described in this report is designed to evaluate and plot this second function automatically, and although the system was devised for convenience and speed rather than high accuracy, any proposed method to insure smaller errors would be extremely laborious by comparison.

A distribution-density plot is obtained simply by applying the signal at a level of about 12 v peak-to-peak to the input terminals and by starting the scanning motor and the output recorder. Within a period of ten minutes, the 1% amplitude slice or aperture is moved continuously through the amplitude range of the signal, and allows a maximum effective integrating time that approaches six seconds at a given level without loss of resolution. The equipment was designed for the analysis of low-frequency noise components and has been used exclusively for this purpose; in this application, the original signal has components from dc to about ten cps. A 1.5 minute sample is recorded on magnetic tape and played back as a continuous loop at a 30:1 increase in speed. The length of the sample is thus decreased to three seconds, and the maximum frequency is increased to 300 cps at the input to the distribution analyzer. The analyzer circuits, exclusive of the tape equipment, output recorder, and recorder amplifier, occupy a 10-in. rack-panel chassis.

REVIEW OF EARLIER TECHNIQUES

In addition to laborious hand-plotting methods, several different techniques were used in the past to obtain amplitude distributions. Nienburg and Rogers[1] used a storage tube to obtain a continuous display of the distribution density on an oscilloscope. The signal scans a single line of the storage area, and distribution is obtained by reading off the accumulated densities with a linear sweep. No data, however, were given on the accuracy of this method.

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[1] *Nienburg, R.E., and Rogers, T.F., "A Storage Tube as an Amplitude Distribution Analyzer," presented March 19, 1951 at the National Convention of the IRE*

In a brief review of early work on amplitude distributions, Knudtzen[2] mentions the technique of scanning an oscilloscope display with a photoelectric pickup and cites references to similar approximate methods used by various workers. Knudtzen then describes a more accurate technique whereby the distribution function of the envelope of filtered noise is obtained by counting electronically the number of times the instantaneous noise voltage exceeds a series of set levels and by comparing these counts, with the number of zero crossings for the same periods. Distribution densities are then computed from the points on the distribution function by the approximate equation

$$p(x) = \frac{\text{No. Counts } (x_1) - \text{No. Counts } (x_2)}{x_1 - x_2} \qquad (3)$$

where x_1 and x_2 are adjacent levels.

By modulating a sampling carrier with the signal, this method can be extended to investigate instantaneous voltages rather than envelopes. Using a maximum of 84 discrete levels about 0.5 v apart, Knudtzen states that three or four hours were required to run a distribution curve, but he points out that simultaneous observation of all or several levels is possible by duplicating equipment.

Davenport[3] used an analogous technique in obtaining directly points on the distribution-density curve for recorded samples of speech. Here a train of pulses at a repetition frequency of about 83 kc is modulated by the speech waveform in a linear modulator. These sampling pulses are then fed to a level selector that produces an output pulse each time the amplitude of one of the samples falls within a set amplitude interval or slice. During the measurement time, an electronic counter registers the number of selected pulses, and a second counter registers the total number of samples. The ratio of the two counts then gives the distribution density at the set level. Between 50 and 100 adjacent amplitude slices were used with a 1.0-v slice width which was referred to the level-selector input, and measurement times for each level were about five minutes.

THE NEW DISTRIBUTION ANALYZER

The unit described in this report was designed to produce rapid automatic plots of the distribution density for signal components from dc to 1000 cps. The basic principle is the same as that used in the previously mentioned storage tube and cathode-ray-tube scanning devices, in that an amplitude slice or aperture is moved continuously over the amplitude range of the input signal, while the relative amounts of time that the aperture is occupied by the signal are recorded. A precision potentiometer, driven by a constant-speed motor, is used to obtain an amplitude scan, and distribution-density data are extracted continuously by a circuit that applies a constant voltage or current to an integrator during the total time that the instantaneous signal amplitude lies within the aperture. By feeding the output of the integrator to a pen-and-paper recorder, an automatic plot of the distribution density is obtained.

The accuracy of the new method should be greater than that of the other analogue techniques mentioned, and if suitable experimental precautions were taken, it might approach that of the more laborious point-by-point methods. Where the effective measurement time at a given aperture level can be short (six seconds or less) the total plotting time is about ten minutes for an aperture which is 1% of the total amplitude range. This performance would represent a large gain in speed over the point-by-point techniques. When longer effective measurement times were needed, the advantage in speed would be smaller.

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[2] *Knudtzen, Nic, "Experimental Study of Statistical Characteristics of Filtered Random Noise," MIT Research Laboratory of Electronics, Technical Report No. 115, July 15, 1949*

[3] *Davenport, W. B., Jr.,"A Study of Speech Probability Distributions," MIT Research Laboratory of Electronics, Technical Report No. 148, August 25, 1950*

Elimination of the sampling carrier generator and the linear modulator, which are necessary when an instantaneous signal voltage is to be analyzed by the pulse-counting techniques, results in considerably simpler circuitry.

Aside from a possible loss in inherent accuracy, the principal disadvantage of the analogue technique lies in the difficulty of obtaining extremely long measurement times at a given amplitude level. Regardless of how slowly the amplitude scan is made, the effective measurement time can be no longer than the averaging time of the output integrator. For averaging times longer than a few seconds, an electronic integrator would be required to avoid bulky components. If an analogue device were used, another element of limited accuracy would be added to the system. An alternative method to obtaining effective integration for a long period of time would be to gate a high-frequency carrier with the unfiltered output of the analyzer. Counters would be used to count carrier cycles before and after gating. The count after gating would be proportional to the time that the amplitude aperture was occupied by the signal, and the ratio of the counts would be the distribution density. Use of this integration method would sacrifice the simplicity of the present equipment and make automatic plotting of results difficult; nevertheless, unlimited measurement times could be obtained.

EQUIPMENT DESCRIPTION

Circuit Principles

The general circuit techniques used in the distribution analyzer are indicated in a block diagram and a waveform sheet (Figures 1 and 2). The over-all function of the circuits is to produce a constant voltage or current output to the integrator when the instantaneous signal lies within a narrow range of amplitudes centered about the reference level. The output is zero at all other times.

The initial amplitude comparison is made in the level-selector circuit, which is a balanced stage where the differential output is zero when the signal is equal to the reference voltage. As the signal becomes positive or negative with respect to the reference, increasing outputs are produced, and a polarity reversal occurs as the output passes through zero.

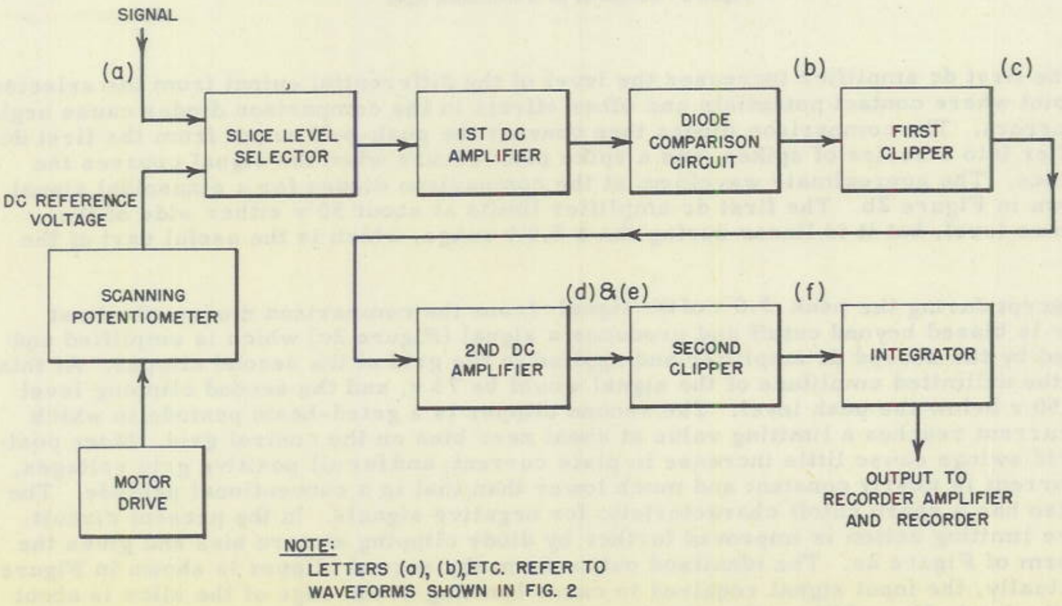

Figure 1 - Block diagram of the amplitude-distribution analyzer

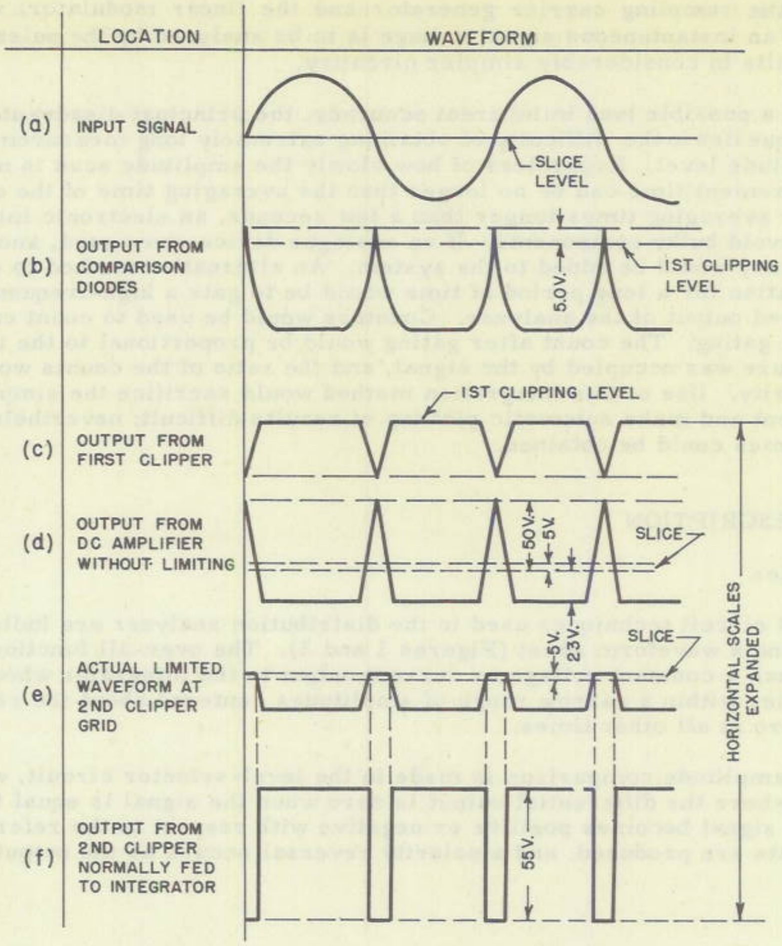

Figure 2 - Waveforms for a sinusoidal input

The first dc amplifier increases the level of the differential output from the selector to a point where contact potentials and other effects in the comparison diodes cause negligible errors. The comparison diodes then convert the push-pull output from the first dc amplifier into a series of spikes, and a spike peak occurs when the signal crosses the reference. The approximate waveform at the comparison diodes for a sinusoidal signal is shown in Figure 2b. The first dc amplifier limits at about 50 v either side of the reference level, but it is linear during the ± 5.0-v range, which is the useful part of the spike.

Except during the peak 5.0 v of the signal from the comparison diodes, the first clipper is biased beyond cutoff and produces a signal (Figure 2c) which is amplified and inverted by the second dc amplifier and applied to the grid of the second clipper. At this point, the unlimited amplitude of the signal would be 73 v, and the second clipping level is set 50 v below the peak level. The second clipper is a gated-beam pentode in which plate current reaches a limiting value at about zero bias on the control grid. More positive grid swings cause little increase in plate current, and for all positive grid voltages, grid current is nearly constant and much lower than that in a conventional pentode. The tube also has a sharp cutoff characteristic for negative signals. In the present circuit, positive limiting action is improved further by diode clipping at zero bias and gives the waveform of Figure 2e. The idealized output from the second clipper is shown in Figure 2f. Actually, the input signal required to cause limiting at the edge of the slice is about 5% of the total slice width so that the output pulses approach ideal rectangular slices rather closely. It should be emphasized that the slice shape is the over-all transfer characteristic between input and output and is not a function of time. The plot of the output vs. time shows rectangular, uniform pulses only for a periodic signal which crosses the amplitude aperture at regular intervals and at a nearly constant slope. The sine wave used for illustration is such a case.

The average signal value at the second clipper plate is a measure of the time the signal occupies the amplitude slice, and in the present equipment, this average is obtained continuously by a resistance-capacity integrator. This integrated output is applied to a pen-and-paper recorder, and as the motor drive slowly changes the reference level, an automatic plot of the distribution density is obtained.

Equipment Specifications

The following constants have been established:

Width of amplitude slice - 0.12 v at the input edges of slice.

Sum of rise and fall - 10% of the slice width.

Input impedance - 500,000 Ω shunted by 15 μμf.

Maximum signal input without loading of source - 20 v peak-to-peak for a slice width of 0.6%.

Frequency response for a 20 v-input level - flat to 1,000 cps and -3db at 2900 cps.

Reference-voltage scanning range - 0 v to + 25 v.

Reference scanning rate - 2.5 v/minute for a maximum of ten minutes.

Reference marker pulses - produced by a closing microswitch every 2.5 v.

Equipment Operation

The only operating controls are the input attenuator, the dc amplifier zero adjustment, the manual control knob for the scanning potentiometer, and the scanning motor switch.

When the components for the output filter have been chosen to give the desired integrating time, the equipment should be warmed up for at least 30 minutes to allow the dc amplifiers to stabilize. The front-panel bias meter is then set to the reference mark by the dc amplifier zero adjustment, and the equipment is ready to operate. The bias meter has a sensitivity of 50-v full scale, and a ± 5-v deviation from the mark which indicates a ± 10% change in the width of the amplitude slice. The zero adjustment must be made with the reference voltage set outside the signal range, preferably with the input grounded and the reference set a few volts above ground. When the signal lies within the amplitude slice, the bias meter will indicate zero. While a signal is swinging through the slice, the indications will vary between zero and the reference mark and roughly show the instantaneous distribution density.

The ten-turn reference-voltage potentiometer is provided with a geared-knob and dial assembly which indicates the setting as a fraction of the entire range. This dial rotates with the potentiometer during motor-driven scanning and also serves as the manual reference adjustment. A clutch between the drive motor and the potentiometer allows manual settings to be made without disengaging the motor drive, and it also protects the potentiometer stops by slipping at a safe torque value when either end of the range is reached. The motor drive is controlled by a three-position switch for clockwise rotation, motor off, and counterclockwise rotation. A microswitch is closed momentarily once in each potentiometer revolution to divide the scanning voltage into ten equal increments, and a voltage calibration may thus be indicated on the same recorder chart as the distribution-density function.

When the absolute reference-voltage level for a given dial setting is to be measured, a dc voltage should be applied to the signal input and adjusted until the bias meter drops to zero; this drop indicates that the input is centered in the amplitude slice. The voltage measured at the signal terminals is then the effective reference level at the particular dial setting and may differ slightly from the voltage at the reference grid of the level-selector stage because of unbalances in the push-pull stages. An internal balance adjustment could be provided, but it was considered unnecessary for present application of the equipment.

DESIGN CONSIDERATIONS IN DETAIL

The circuit schematic, power supply schematic, and a simplified drawing of the scanning potentiometer drive are given in Figure 3, Figure 4, and Figure 5, respectively.

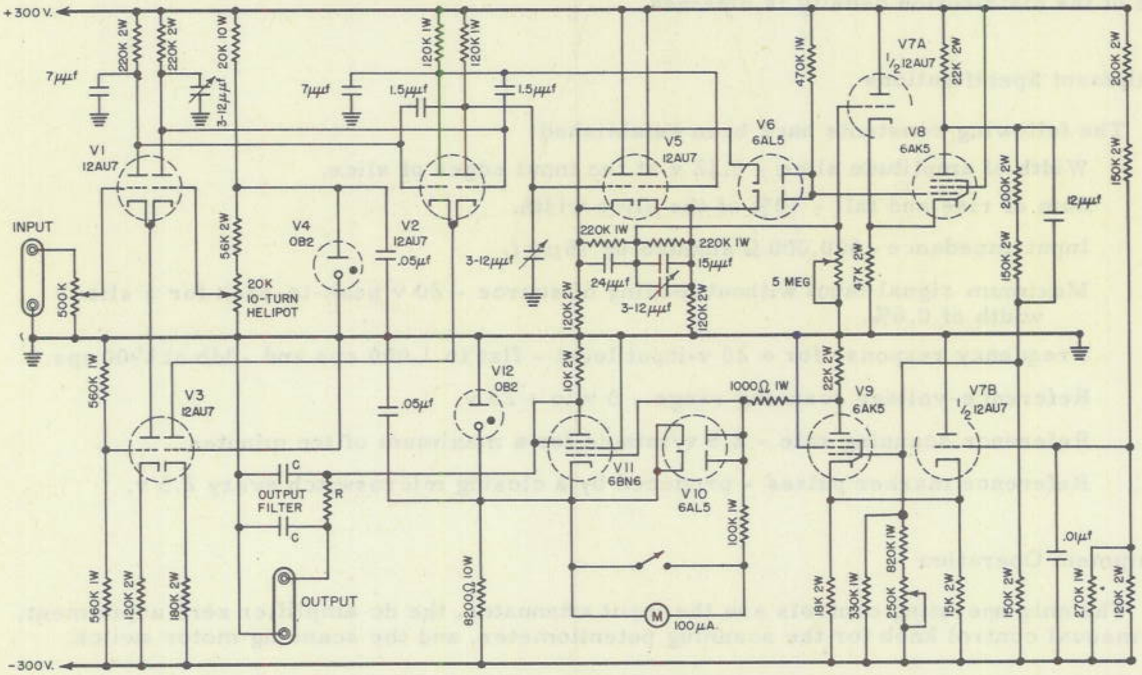

Figure 3 - Circuit schematic diagram for the amplitude-distribution analyzer

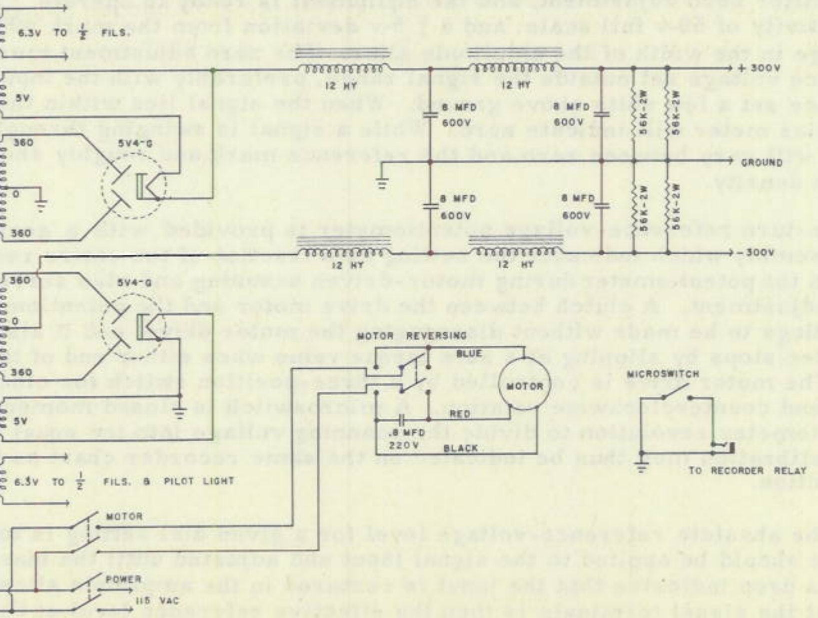

Figure 4 - Power-supply schematic diagram for the amplitude-distribution analyzer

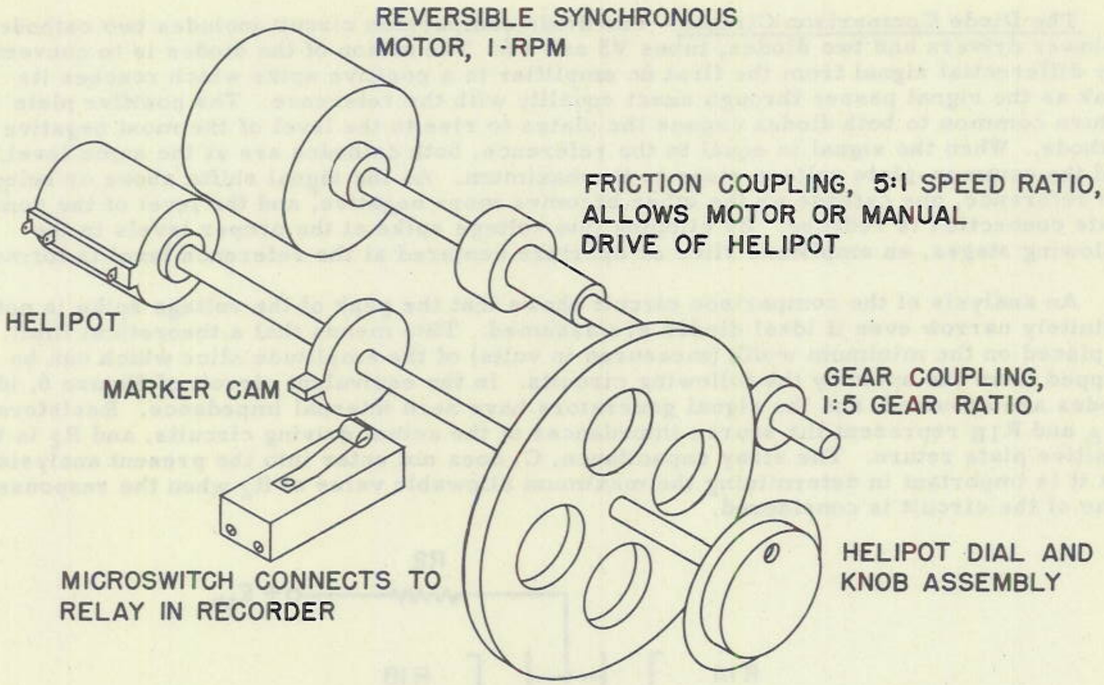

Figure 5 - Scanning-potentiometer drive

Circuit Details

The Level Selector - Formed by tubes V1 and V3A, the circuit used to indicate equality of the signal and a variable reference is a familiar type for amplitude comparison. When signal and reference grids are at the same level, the two plates are also at the same level if matched tubes and loads are assumed. Any difference voltage between the two grids appears amplified at the plates. This differential output is the one utilized by the following circuits to form the amplitude slice, but clipping points also depend on the push-push or common-mode output which should be kept as small as possible. Reference-voltage scanning over the desired range of signal amplitudes represents a common-mode input that may be as high as 25 v compared to a slice width of less than 0.2 v so that a large common-mode rejection factor is needed. By using a separate triode as a constant-current cathode load, a 20:1 reduction is obtained. An effective resistance of nearly 2.5 megohms is obtained while allowing normal plate-current levels in the amplifier sections. The maximum signal input that can be accepted without loading the signal source is 20 v peak-to-peak. However, a maximum variation in reference voltage of about 25 v peak-to-peak is available; it is obtained from a precision potentiometer (a ten-turn "Helipot" having 0.1% linearity) and is driven by a reversible motor. The reference level is stabilized by a VR tube, V4.

If instantaneous loading of the signal source can be tolerated, much higher input levels may be used since there are no bypass or coupling condensers to charge or discharge, and the amplification is always linear during the amplitude slice. A signal of 75 v peak-to-peak should be accepted without appreciable loss of gain or linearity during the slice, but a corresponding increase in the reference voltage would be needed to scan the entire signal in this case.

The First DC Amplifier - This circuit, consisting of V2 and V3B, provides further amplification of the differential signal at the input and further attenuation of the common-mode signal by a factor of about 60:1. The total gain from the signal input to one plate of the dc amplifier is about 85. The signal at one plate is limited at a maximum amplitude slightly under 100 v peak-to-peak, but during the amplitude slice, the only region of interest at this point and in all following stages, the circuit is linear.

The Diode Comparison Circuit - The diode comparison circuit includes two cathode-follower drivers and two diodes, tubes V5 and V6. The action of the diodes is to convert any differential signal from the first dc amplifier to a positive spike which reaches its peak as the signal passes through exact equality with the reference. The positive plate return common to both diodes causes the plates to rise to the level of the most negative cathode. When the signal is equal to the reference, both cathodes are at the same level, and the common-plate voltage rises to its maximum. As the signal shifts above or below the reference, one cathode or the other becomes more negative, and the level of the common-plate connection is reduced. By clipping this voltage spike at the proper levels in the following stages, an amplitude slice or aperture centered at the reference level is formed.

An analysis of the comparison circuit shows that the peak of the voltage spike is not infinitely narrow even if ideal diodes are assumed. This means that a theoretical limit is placed on the minimum width (measured in volts) of the amplitude slice which can be clipped from the spike by the following circuits. In the equivalent circuit of Figure 6, ideal diodes are assumed, and the signal generators have zero internal impedance. Resistors R_{1A} and R_{1B} represent the source impedances of the actual driving circuits, and R_2 is the positive plate return. The stray capacitance, C, does not enter into the present analysis, but it is important in determining the maximum allowable value of R_2 when the response time of the circuit is considered.

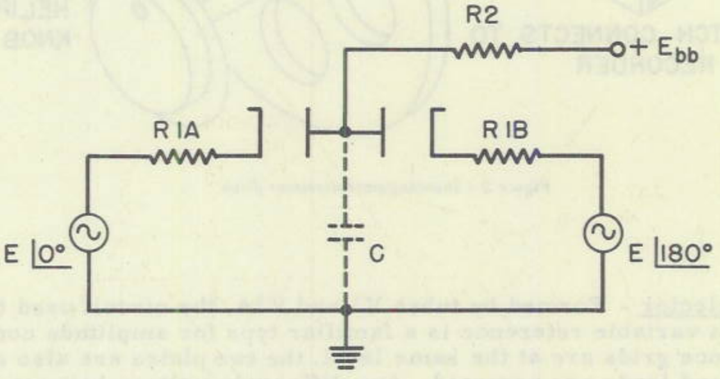

Figure 6 - Equivalent circuit for the comparison diodes

Let $R_{1A} = R_{1B} = R_1$, and let ΔE be the shift of each input voltage away from exact equality. Then, at the point where one diode just stops conducting, we have

$$(E + \Delta E) = (E - \Delta E) + \frac{[E_{bb} - (E - \Delta E)]\, R_1}{R_1 + R_2},$$

$$2\Delta E \left(\frac{R_1 + R_2}{R_1}\right) = E_{bb} - E + \Delta E,$$

$$\Delta E \left[\frac{2(R_1 + R_2)}{R_1} - 1\right] = E_{bb} - E,$$

$$\Delta E \left(\frac{R_1 + 2R_2}{R_1}\right) = E_{bb} - E, \qquad \text{and}$$

$$\Delta E = \frac{R_1\,(E_{bb} - E)}{R_1 + 2R_2}\,. \qquad (4)$$

Since the circuit is exactly balanced, no change in plate level occurs while both diodes are conducting, and the voltage spike has a flat top of width $2\Delta E$ v in terms of the signal on one cathode. In an actual circuit, the narrowest slice that can be clipped from the plate signal is thus slightly less than $2\Delta E$.

In the present case,

$$(E_{bb} - E) = 100 \text{ v},$$

$$R_1 = \text{cathode-follower output impedance + diode plate resistance},$$

$$R_1 = 2800 + 400 = 3200 \text{ cps},$$

$$R_2 = 470{,}000 \text{ ohms},$$

$$\Delta E = \frac{3200 \times 100}{3200 + 940{,}000}, \text{ and}$$

$$\Delta E = 0.34 \text{ v, at comparison diode cathode.}$$

Figure 7 shows the relationship between the signal input and the voltages at the comparison diodes.

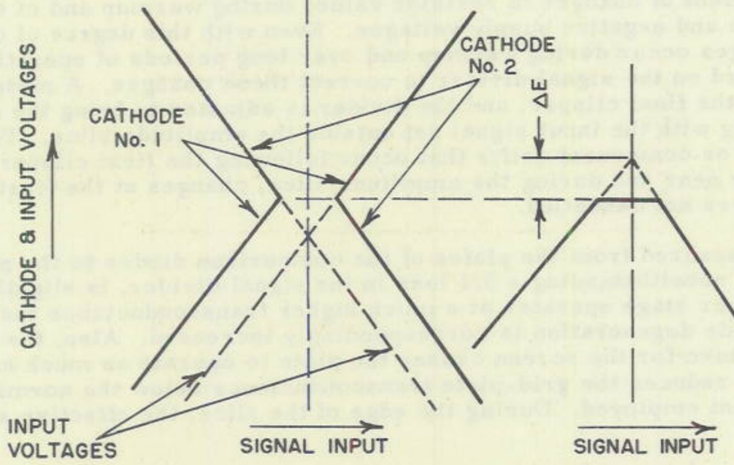

Figure 7 - Input-output transfer characteristic of the comparison circuit

The minimum slice width of 0.68 v is approximately 14 times as narrow as the slice actually used which is about 10 v at this point in the circuit so that a higher source impedance could be tolerated. However, the triode amplifiers alone would have an output impedance at least ten times as high as the cathode followers, and this would give a rather small margin between the theoretical limit and the desired width.

<u>The First Clipper</u> - Using tubes V7A and V8, the first clipper stage includes a pentode amplifier and a cathode follower which provide a low-impedance cathode return point for the amplifier. The utilization of a cathode-follower return has two important advantages over a VR tube or low-resistance voltage divider. First, the stability of the grid-cathode bias in the amplifier is increased. Instead of being equal to the difference between two relatively large and independently variable voltages, the bias is nearly equal to the operating bias of a cathode follower under constant voltage. The effects of common-mode shifts ahead of the comparison diodes are reduced by

$$\frac{1}{1 - G_{CF}}.$$

Cathode-follower gain should be at least 0.90 and should give common-mode rejection of 10:1. By returning the cathode-follower grid to an accurately center-tapped divider between the driver tubes, V5A and V5B, differential signal components are kept low while setting the correct dc level. Small bias adjustments are made by a variable bleeder to ground; the bleeder setting used reduces the cathode-follower compensation by a factor of only 0.98.

A second advantage of a cathode-follower tie point is the cancellation of changes in effective amplifier bias with heater supply voltage. If the cathode-follower and amplifier have identical cathode characteristics, compensation is theoretically perfect. In the present case, cathode characteristics undoubtedly differ, but 80 to 90 % compensation might be expected.

Plate current in the 6AK5 amplifier is normally cut off, and bias is set to allow conduction when the voltage spike on the grid rises within about 8.0 v of its peak. The edge of the amplitude slice is set about 5.0 v from the peak of the spike, and stage gain is relatively low because of cathode degeneration and operation near cutoff. The effective value at the start of the slice is about 6.

The Second DC Amplifier - Formed by tubes V9 and V7B, the second dc amplifier stage is almost identical in design to the first clipper stage, and a cathode-follower return point is used for the same reasons. This amplifier and the second clipper that follows are both operated below ground from a negative supply to provide an output with the same ground reference as the input signal. The use of physically similar voltage dividers for both the signal grid and the cathode-follower grid makes the grid bias of the amplifier stage more nearly independent of changes in resistor values during warmup and of dissimilar variations in positive and negative supply voltages. Even with this degree of compensation, noticeable bias changes occur during warmup and over long periods of operation; a vernier adjustment is provided on the signal divider to correct these changes. A meter indicates the grid-cathode bias at the final clipper, and the divider is adjusted to bring the meter to a predetermined setting with the input signal set outside the amplitude slice. This adjustment corrects for all tube or component drifts that occur following the first clipper. Since the clipper conducts only near and during the amplitude slice, changes at the first clipper or in preceding stages are not cancelled.

Over-all gain measured from the plates of the comparison diodes to the plate of the second dc amplifier, notwithstanding a 5:1 loss in the signal divider, is slightly greater than ten. The amplifier stage operates at a much higher transconductance than the first clipper, but the cathode degeneration is correspondingly increased. Also, the use of the convenient ground return for the screen causes the plate to operate as much as 125 v below the screen level, and reduces the grid-plate transconductance below the normal figure for the idling plate current employed. During the edge of the slice, the effective stage gain is between 8 and 9.

The Second Clipper - The second clipper stage consists of a gated-beam pentode, V11, and a diode limiter, V10; a VR tube, V12, provides a regulated cathode reference voltage. The gain from the signal input to the grid of this final clipper is approximately 830, and the transfer characteristic has the form shown in Figure 8. The actual amplitude aperture, represented by the shaded area of the diagram, is formed by the gated-beam tube which was chosen because sharp limiting action was required at both zero plate current and maximum plate current. The plate-current cutoff for negative grid-swings is somewhat sharper than that in a conventional pentode, and for a grid bias near zero, the plate current also reaches an upper limit. Further positive changes in grid voltage cause only small changes in plate current, and the grid current likewise limits at about 0.5 ma. The inherent positive limiting action is not as sharp however, as the plate-current cutoff, and was improved in the present circuit by clamping the grid at zero bias with a diode, V10. For the operating conditions chosen, the grid base of the tube is 5.0 v; the plate current limits at 5.5 ma and gives a -55 v signal across the 10,000-ohm plate load. The unlimited amplitude of the voltage spike on the grid is about 50 v from the edge of the slice to the peak that represents the center of the aperture where reference and signal voltage are exactly equal. The output voltage thus increases from zero to its upper limit in 5% of the slice width, and as the signal moves out of the aperture, it again decreases to zero in the same voltage increment.

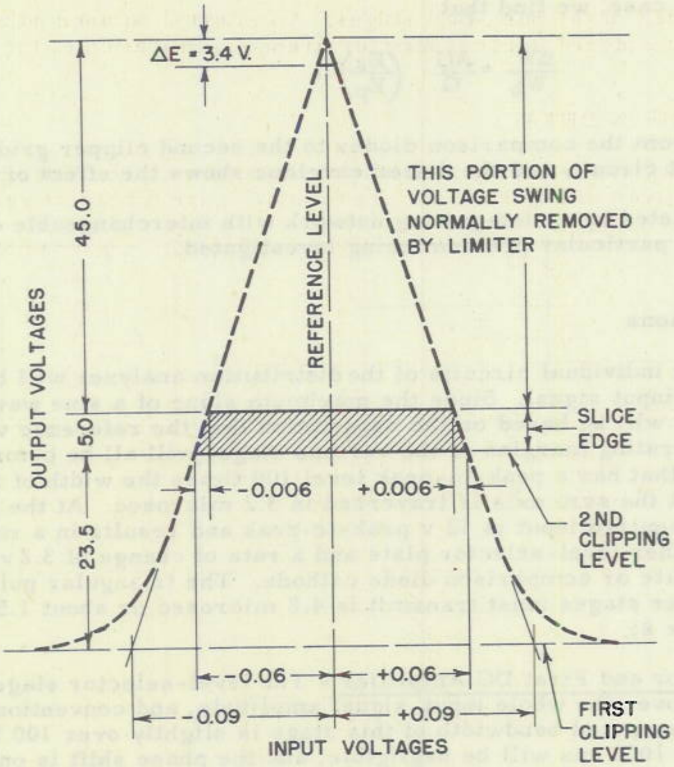

Figure 8 - Over-all transfer characteristic to grid of second clipper

Choice of the second clipping level relative to the base of the spike is a compromise between high over-all gain and stability of the slice width. Close to the first clipping level, the first clipper stage is operating near cutoff, and its gain is low, but changes in the gain of the clipper and second dc amplifier will have little effect on the slice width. As the second clipping level is moved away from the first, the gain of the first clipper improves, but the sensitivity of the slice width to gain changes also increases. The situation for an idealized triangular spike is shown in Figure 9.

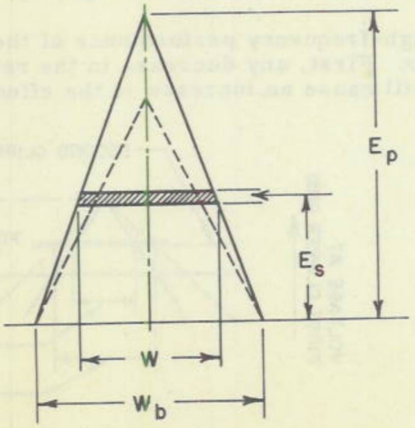

Figure 9 - Effect of second clipping level on sensitivity of slice width to grain changes

In this simplified case, we find that

$$\frac{\Delta W}{W_b} = \frac{\Delta G}{G} \left(\frac{E_s}{E_p}\right), \tag{5}$$

where G is the gain from the comparison diodes to the second clipper grid. The factor E_s/E_p is 0.47 for the present circuit, and the dotted envelope shows the effect of a gain decrease.

The unit is completed by an integrating network with interchangeable components which are chosen to suit the particular problem being investigated.

Bandwidth Considerations

Requirements for individual circuits of the distribution analyzer will be considered in terms of a sinusoidal input signal. Since the maximum slope of a sine wave occurs at the axis, all computations will be based on the assumption that the reference voltage is set at this level. The operating margins of the various stages will all be computed for a 1000-cps input signal that has a peak-to-peak level 100 times the width of the amplitude slice so that a slice at the zero axis is traversed in 3.2 microsec. At the levels used in the present circuit, the required input is 12 v peak-to-peak and results in a rate of change of 0.24 v/microsec at either level-selector plate and a rate of change of 3.2 v/microsec at either dc amplifier plate or comparison diode cathode. The triangular pulse that the clipper and second dc amplifier stages must transmit is 4.8 microsec or about 1.5 times as long as the slice itself (Figure 8).

The Level-Selector and First DC Amplifier - The level-selector stage normally acts as a linear amplifier over the whole input-signal amplitude, and conventional cw response theory applies. The computed bandwidth of this stage is slightly over 100 kc; thus the amplitude decrease at 1000 cps will be negligible, and the phase shift is only about 0.5°. The differential phase shift between signals at the two plates will be much smaller than this figure for matched loads.

The first dc amplifier stage operates as a linear amplifier over only about 10% of the level-selector plate swing, and it is most conveniently analyzed in terms of transient response. As operated here, the grid base of the stage is about 10 v from cutoff to zero bias and this 10-v range is covered by the grid signal in 40 microsec at an almost constant rate. If only the external plate loads of the stage are considered, the 10 to 90% rise time is under six microsec (T = 2.2 RC), and this means that the plate-rise times are less than 1% longer than the grid swings between zero bias and cutoff. The shunting effect of the tube plate resistance will cause some further improvement. As in the case of the level-selector stage, the differential change in rise time can be made much smaller by matching plate impedances. If tube plate resistance is neglected, the total time delay of the square-wave edges, as opposed to the change in slope or rise time, is about 2.5 microsec.

The high-frequency performance of these two stages alters the slice width and shape in two ways. First, any decrease in the rates of rise and fall at the comparison diode cathodes will cause an increase in the effective width of the amplitude slice (Figure 10).

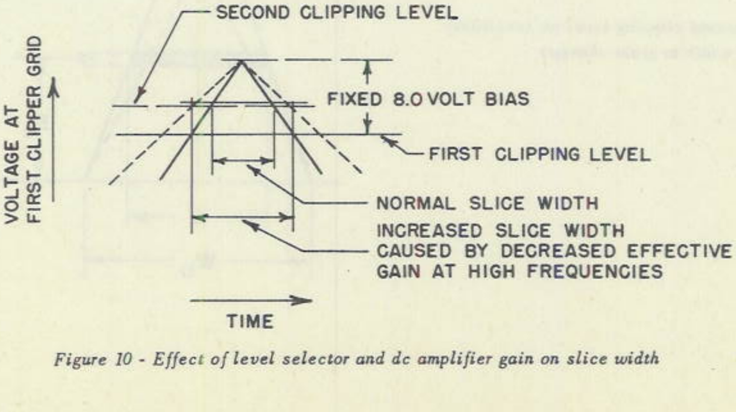

Figure 10 - Effect of level selector and dc amplifier gain on slice width

The 1000-cps data for the two stages indicate an increase of only 1% in width, and the slope of the slice edges increases proportionately so that no change occurs in the shape of the aperture.

The second source of error is the differential phase shift or time delay through the two channels (Figure 11).

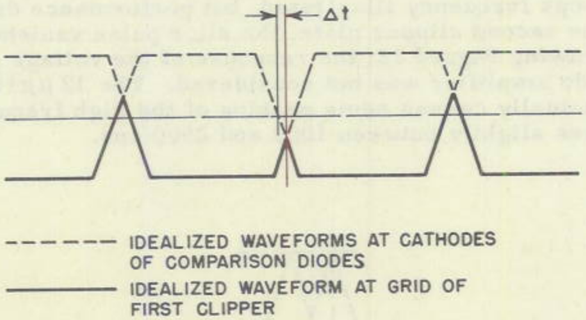

Figure 11 - Effect of differential phase shifts on slice width

Regardless of the absolute level, the peak of each voltage spike shown occurs when the two cathodes are at the same voltage; thus alternate peaks are formed above and below the normal comparison point. The effect of these shifts on the grid-cathode bias of the first clipper is reduced at least 10:1 by the associated cathode follower. The absolute time delay through the level-selector stage and the amplifier stage in cascade is estimated to be four microsec. If matching the two channels is 80% effective, the differential delay will be 0.8 microsec, and the shifts in the spike peaks will amount to ± 25% of the voltage swing through the complete amplitude slice. A 10:1 reduction by the cathode follower leaves ± 2.5% variations in slice width, and the slope of the slice edges does not change. For a symmetrical periodic signal, the average width for positive and negative crossings of the slice taken together will be unchanged, but errors will be introduced when the input is a time function that does not make positive and negative crossings at the same rate.

Trimmer capacitors for final phase adjustments are located at one plate of the level selector and at one plate of the first dc amplifier. Fixed padders are connected at the opposite plates. A third trimmer, located across one arm of the reference divider between driver cathode followers, allows adjustment for an accurate center tap at high frequencies. In this circuit, phase shifts have the same effect on the net signal to the first clipper as differential delays have in the push-pull stages.

The Comparison Diodes - The rate at which the common plate will follow a rising cathode, the most important consideration in this circuit, depends on the effective capacity to ground and the resistance and voltage of the positive return. For the circuit constants used, the maximum rate of rise is slightly over 8.5 v/microsec compared to the 3.2 v/microsec at the cathodes for a 1000-cps input. As the signal rate of rise approaches maximum, the condenser charging current rises, and the diode current falls by the same amount. This fall causes the diode plate to become more negative with respect to the rising cathode, and since the negative-going cathode intercepts the common plate at a level below its normal maximum, the whole voltage spike is shifted downwards. This shift is not reduced by the clipper cathode follower, and the decrease in slice width reaches about 10% when the signal rate of rise becomes equal to the maximum. The slice width decreases rapidly to zero for still higher input frequencies.

At high frequencies, a rounding of the spike top will take place because of the time constant formed by the output impedance of the driver cathode followers and the capacity at the diode plates. This effect should not appreciably alter the amplitude slice until the input frequency approaches 20 kc for a 1% slice.

The First Clipper and Second DC Amplifier - These stages both act as pulse amplifiers in which the signal is a triangular pulse with a length inversely proportional to the input frequency and input amplitude. For a 1000-cps input at the level required for a 1% slice, the length of the slice pulse is 3.2 microsec. The first clipping level is set somewhat below the slicing point on the grid-voltage spike, and at the plate, the triangular pulse is 4.8 microsec or about 1.5 times as long as the pulse formed during the slice. The approximate transient response of the two stages in cascade is shown in Figure 12. Negligible distortion of the slice occurs at the 1000-cps frequency illustrated, but performance deterioriates rapidly above 2500 cps, and at the second clipper plate, the slice pulse vanishes entirely between 3100 and 4000 cps. In drawing Figure 12, the response of the voltage divider between the first clipper and second dc amplifier was not considered. The 12 $\mu\mu$f compensating capacitor shown in the schematic actually causes some peaking of the high frequencies, and the relative output of the unit rises slightly between 1000 and 2500 cps.

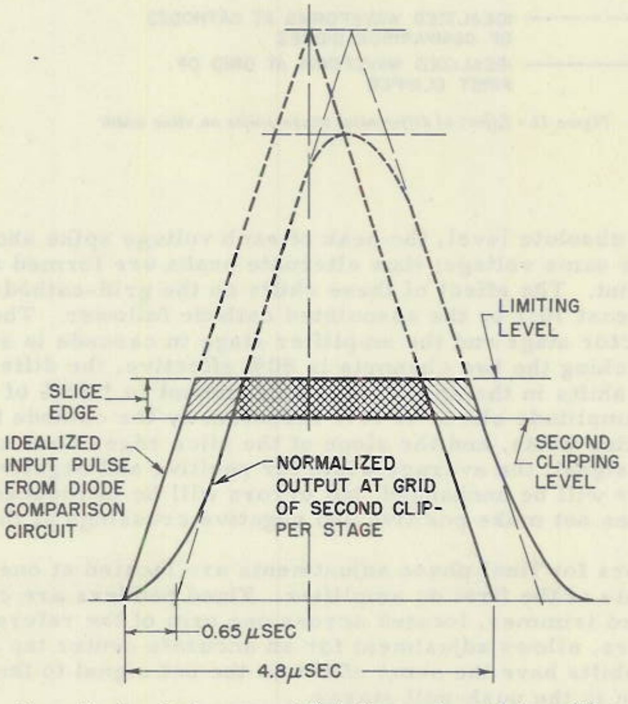

Figure 12 - Transient response of first clipper and second dc amplifier stages for a 1000-cps sinusoidal input at 12 v peak-to-peak

The Second Clipper - In this stage, the bandwidth of the plate load need not be considered when the output integrating device averages current rather than voltage. The network shown in the schematic diagram has this characteristic when the current impulses occur at a high enough frequency. The only disadvantage of this type of filtering is the small error introduced by the output tube. The plate characteristics of the 6BN6 gated-beam tube are similar to those of a standard pentode such as the 6AK5, but effective plate resistance is still low enough to cause a plate-current decrease of about 7% over the 55-v plate swing caused by maximum current in a 10,000-ohm load. This decrease means that high-distribution densities that result in a low-plate level will be recorded as lower than their true relative values.

The error caused by finite plate resistance may be eliminated by removing the input condenser of the integrating network and allowing the 6BN6 plate to follow each individual pulse of current. In this case, the integrator output is proportional to the average area (Σ Edt/T) under the output-voltage pulses, and the bandwidth of the plate load must be great enough to prevent distortion at the highest input frequencies of interest. For a 1% amplitude slice at 1000 cps, the output current pulse is 3.2 microsec long with rise and fall times of 0.16 microsec. With a 10,000-ohm load, the 10 to 90% rise time of the plate circuit is

0.15 microsec or faster, and the rise and fall times of the plate-voltage pulse will be increased to 0.22 microsec. This change represents only a small distortion of the pulse, and the change in area will be slight.

Experimental Data - Frequency-response measurements were made with the second method of integration in which the input condenser is eliminated. The input signal was a sine wave maintained at a level of 20 v peak-to-peak, and the reference voltage was set at the base line. A 20-v signal is the maximum that can be used without loading the signal source and results in an amplitude slice 0.6% of the peak-to-peak swing. Since relative output depends upon the product of amplitude and frequency rather than frequency alone, the data (Table 1) show a cutoff frequency about two-thirds as high as that for a 1% amplitude slice.

TABLE 1

Input Frequency (cps)	Relative Output (db)
0	0
1000	0
2500	+1.6
2900	-3.0
3100	-6.0

Extension of Frequency Range - No attempt has been made to determine the exact contributions of the various stages to the measured losses in output at high frequencies. Nevertheless, the discussion of operating margins at 1000 cps shows that the comparison diodes and the two following pulse-amplifying stages will contribute serious errors at frequencies five to ten times as low as the other portions of the circuit. The diode load resistor may be reduced by more than 10:1 and still permit a 1% amplitude slice to be clipped from the resulting voltage spike. This change, however, has been checked experimentally, and the high-frequency cutoff was not extended appreciably so that at present, the two pulse-shaping and amplifying stages apparently limit the response. Any useful extension of range would require the redesign of these stages with a tube having higher plate-current capabilities substituted for at least the second 6AK5.

PERFORMANCE DATA

Circuit Stability

The stability of the distribution-analyzer circuits must be defined in terms of the amplitude-slice position, the width of the amplitude slice, and the absolute level of the output signal.

Slice Position - Changes in slice position amount to errors in the reference voltage level and can be caused only by differential variation in the two halves of the balanced stages ahead of the comparison point. For perfectly matched tubes and other components, the errors caused by external disturbances are reduced to zero. However, any differences between the two channels in tube characteristics or plate loads will cause common-mode changes in plate-supply voltage, heater voltage, or grid-signal level, all to be partially converted to differential signals. In the present unit, no attempt has been made to select tubes, but resistors have been matched within 1%, and trimmer condensers are used to match plate-load impedances at high frequencies.

Slice Width - Variations in the width of the amplitude slice cause errors by changing the amplitude resolution of the system and by changing the effective gain. As long as the distribution density does not vary rapidly during reference-level changes comparable to the slice width, changes in resolution will cause small errors, but the accompanying gain changes may be serious. The integrator output that corresponds to a given distribution density is directly proportional to the width of the slice, and any variations in width that occur during a reference-voltage scan cause corresponding distortions of the plotted curve. Changes in slice width may result from random fluctuations in tube characteristics or from changes in supply voltages and dc signal levels. No estimate of the magnitude of random variations has been made, but the changes to be expected from plate-supply and heater-voltage fluctuations have been estimated from an approximate circuit analysis. These figures have been computed on the basis of a simultaneous change of + 1% in both positive and negative plate supplies and of a + 10% change in heater voltage. The data will thus be typical of operation from moderately stable regulated plate supplies with heater voltage obtained from an unregulated ac line. The present distribution-analyzer chassis does not incorporate regulated plate supplies, but it is operated from an ac line regulated within ± 1% so that deviations in plate supply should be comparable to those assumed, and heater-voltage changes should be ten times smaller.

The net change in slice width for a ± 1% plate-supply change is estimated to be +0.5%, which results from the partial cancellation of positive and negative shifts of +5.9% and -5.4% contributed by various parts of the circuit. When a change in operating point or stage gain occurs gradually and the resulting shift in the second clipper bias is corrected by resetting the bias meter to the reference mark, the situation is altered since changes at or before the first clipper stage do not contribute to the change in meter reading. For the + 1% supply change assumed earlier, a change in slice width of - 2% is fully corrected by bias reset and a net uncorrected change of +2.5% is left. For a + 10% heater-voltage change, the net change in slice width is estimated as - 2.5%.

Minor errors may be contributed by small changes in slice shape that accompany the width variations. Some of the contributing circuit variations cause corresponding changes in slice width and in the slope of the edges so that the shape of the amplitude aperture is not altered. Other variations cause a change in width without an equivalent change in the steepness of the edges. No distinction between the two types of variation was made in tabulating width changes.

In scanning the reference voltage over the signal-amplitude range, a common-mode change of over 20 v in grid level may occur in the level-selector stage. This change is a potential source of error in the following clipper stages, but the common-mode rejection of the balanced circuits is great enough to limit the resulting change in slice width to 0.03% (computed from approximate circuit theory).

Output-Level Changes - The only stage in which changes in operating level appear directly as variations at the analyzer output is the 6BN6 second clipper. The supply voltage for this stage is obtained from a VR tube, and during the slice, the plate current is limited at its maximum level, but this maximum will still change with variations in cathode emission. Slight changes in the operating voltage of the VR tube will also cause equivalent changes in output level. Over short periods of time, however, the errors in this stage should be small compared to those caused by lower-level stages.

Experimental Data - No measurements of individual-stage errors have been made on the analyzer circuits, but over-all stability data have been recorded. These figures include the effects of slice-width changes and slice-position or reference-voltage changes, and although it is not possible to separate them completely, a fairly accurate idea of stability in actual operation is obtained. The data were taken by grounding the signal input and setting the reference voltage just close enough to ground to place the operating points of all the stages at the edge of the slice where the maximum slope of the input-output transfer characteristic occurs. Under this condition, the variations in bias-meter reading may be interpreted in terms of either slice-width changes, slice-position changes, or both. A 1% change in line voltage (both plate and heater supply are changed by this percentage) caused a 10-v change in bias that could be accounted for by a 20% change in slice width or by a change in slice position of 0.012 v, which is 10% of the nominal slice width referred to the input. If earlier estimates of width sensitivity to supply voltage are assumed to be correct, only a

0.5% width change can be accounted for, and the remaining bias shift must be assigned to a change in effective slice position of almost the full 10%.

For nearly constant line voltage, bias-meter changes were also observed over a ten minute period which corresponds to the maximum amplitude scanning time. The largest fluctuations not correlated with line changes were ± 2 v, and this indicated ± 4% slice-width changes, position changes of ± 2% of the width, or a combination of both effects.

Theoretical Accuracy

The exact distribution-density function is obtained only when a signal is scanned in amplitude by an infinitely narrow aperture. Slices of substantial width used in practical circuits always cause a loss in accuracy, but this departure from the theoretical curve may be extremely small. A comparison for a sinusoidal signal has been made between the computed density functions for an infinitesimal slice and a series of ideal rectangular slices of finite width.

For an infinitesimal slice, the distribution-density function has been found to be

$$p(E) = \frac{1}{\pi\sqrt{(E_p)^2 - E^2}} \qquad (6)$$

where $E = E_p \text{ Sin } \omega t$.

In plotting this equation and the curves for finite slices, only relative values of the distribution density are shown, and a value of unity is assigned to the minimum density at the axis. The curves are shown for slice positions on only one side of the axis since the function is symmetrical about this point.

The curve for an infinitesimal slice and the points at the density maximums for several finite slices are shown in Figure 13. The values of E_s are measured to the center of a finite slice so that the maximums occur when E_s is less than E_p by one-half the width of the slice; the curves fall to zero when E_s exceeds E_p by the same margin.

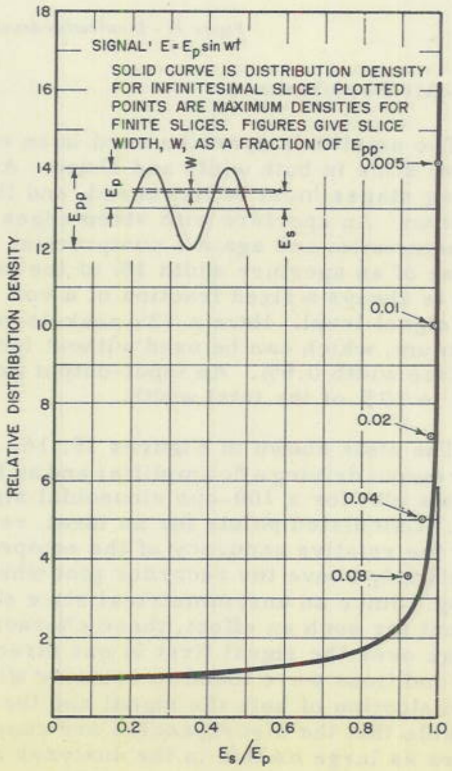

Figure 13 - Distribution density of a sine wave as given by an infinitesimal slice

Figure 14 shows an expanded plot of the region between $E_s/E_p = 0.95$ and $E_s/E_p = 1.01$. Here the complete curves for a 0.5% slice and a 1% slice are shown, and the maximums for 2% and 4% are plotted. The deviation of the 1% curve from that for an infinitesimal slice is seen to be small when E_s/E_p is as high as 0.97.

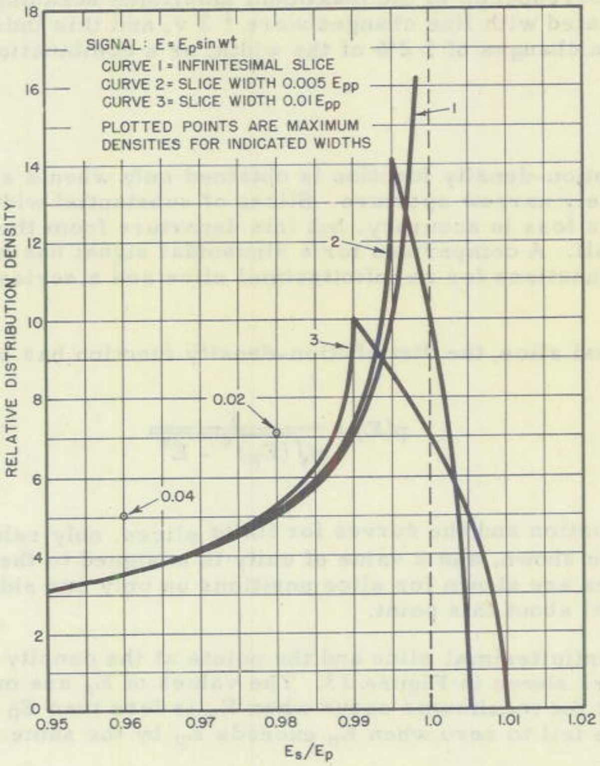

Figure 14 - Distribution density of a sine wave as given by finite slices

Over-All Performance

The amplitude aperture used in an actual circuit must fall short of the ideal infinitely narrow slice in both width and shape. As the aperture is narrowed, the bandwidth of the shaping stages must be increased, and the output indicating device must be made more sensitive. An aperture with steep edges implies high gain at those points on the transfer characteristic, and again a compromise must be made. The analyzer was planned to allow the use of an aperture width 1% of the peak-to-peak signal. Since the aperture or amplitude slice is always a fixed fraction of a volt referred to the input, the relative width depends upon signal level. Here a 12 v peak-to-peak signal gives 1% resolution, and the 20 v maximum, which can be used without increased input loading of the signal source, makes the slice width 0.6%. An input-output gain of over 9,000 makes the sum of the slice edges equal to 10% of the total width.

The plots shown in Figures 15, 16, 17, and 18 are actual recordings made with the analyzer output driving a dc amplifier and an Esterline-Angus Type AW recorder. Figure 15 shows a plot for a 100-cps sinusoidal signal at the level necessary for a 1% amplitude slice. Calculated points for an ideal, rectangular 1% slice are plotted on this sheet to show the relative accuracy of the equipment. Points for the theoretical curve are seen to fall slightly above the recorder plot when the latter is rising and slightly below when it is falling. Since an unsymmetrical slice shape or distortions of the sinusoidal signal might account for such an effect, these characteristics were checked by scanning the reference voltage over the signal first in one direction and then in the other. Plots obtained for the two conditions were found to coincide within less than the width of the inked line and prove that distortion of both the signal and the slice shape was negligible. It therefore seems probable that the discrepancies are caused by a lag in the recording system rather than by errors as large as this in the analyzer output voltage. The response of the recorder definitely accounts for the difference between the computed peaks and maximum amplitudes recorded. When the reference-voltage scanning motor was stopped and the level set manually to the peak density, the recorder pen was deflected to the full computed amplitude for a 1% slice (10.02 times as great as the zero-axis level). A slower reference-voltage scan would evidently give a more accurate plot for a function (such as a sine wave) with rapidly changing density. However, the present unit was designed for the examination of noise sources with more gradually varying densities, and a change in the drive speed could not be made conveniently. For this reason, no special tests were conducted at a low scanning rate.

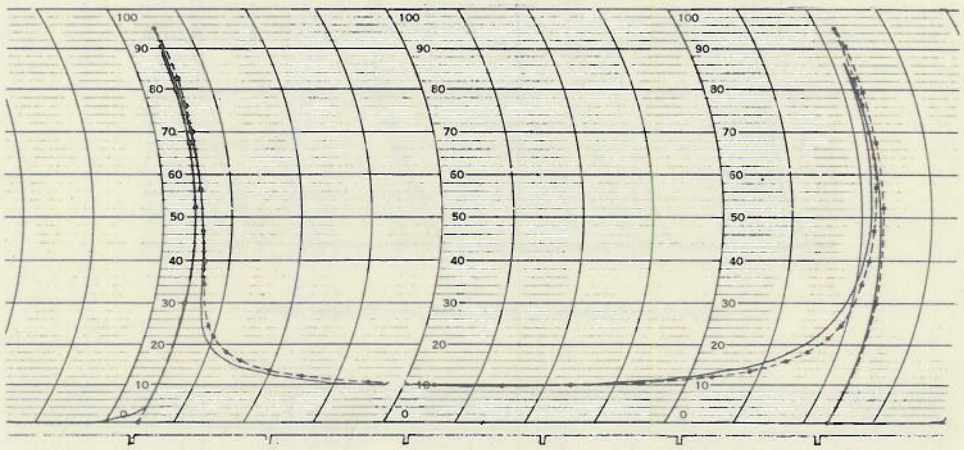

Figure 15 - Recorded distribution density for a sinusoidal signal

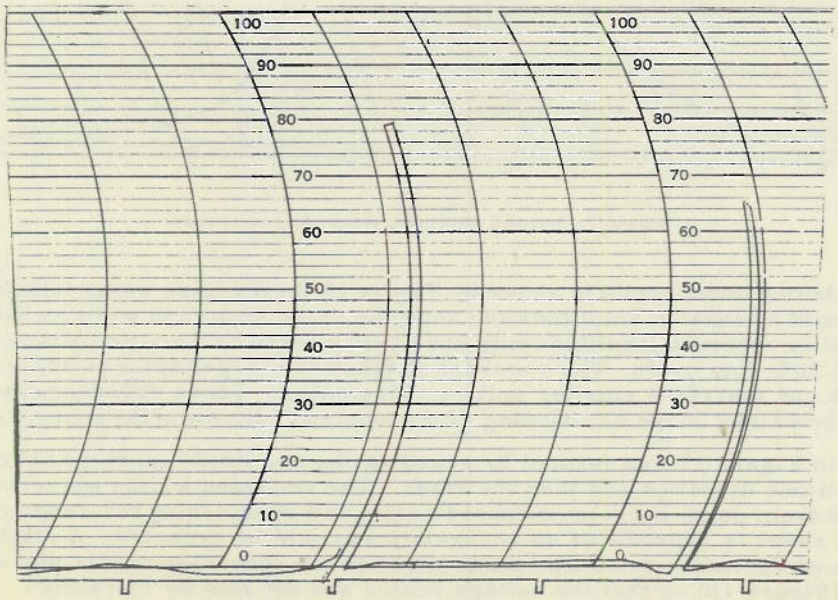

Figure 16 - Recorded distribution density for a square-wave signal

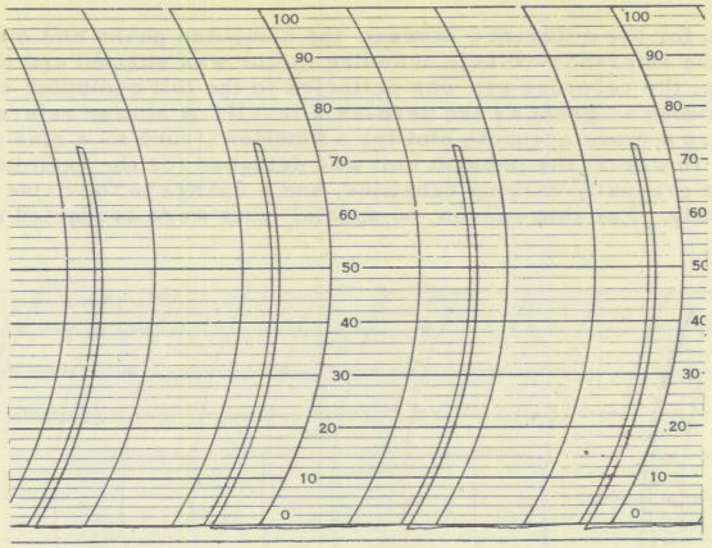

Figure 17 - Repeated recorder plots for a dc input signal

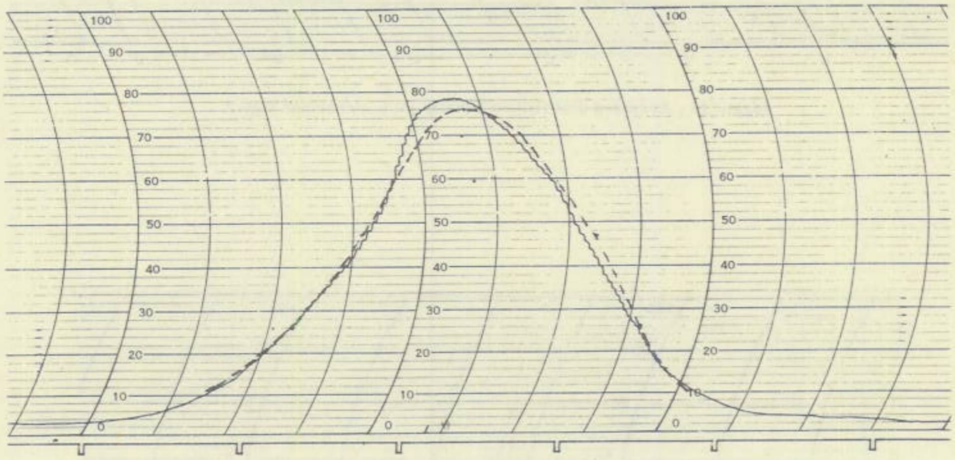

Figure 18 - Recorded distribution density for a noise source

The distribution-density plot is shown by Figure 16 for a square wave. Theoretically, the two spikes should be equal in amplitude and have the same shape and width as the slice itself. The difference in observed amplitude may have been caused by deviation of the square wave from an exact 50% duty cycle. The recorded width of the larger spike is 20% greater than the slice width and that of the smaller spike is 5% smaller. These differences are probably accounted for by a slight slope or rounding of the tops and bottoms of the square-wave half cycles.

The plot in Figure 17 was formed by scanning the amplitude aperture across a dc input voltage in first one direction and then the other. The recorded widths agree with the slice width obtained from point-by-point measurements, and considering the response of the recorder, the shape is reproduced as accurately as could be expected. A slight change in the gear ratio of the motor drive was made between the recording of this plot and the square wave (Figure 16) so that the voltage scales are not exactly the same.

Figure 18 gives the plot of distribution density for a noise source with a calculated Gaussian distribution shown as a superimposed dotted curve. The small ripples appearing on the recorded line occur at the repetition frequency of the signal sample and could be removed at the risk of a resolution loss by increasing the integration time.

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