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# THE ELEVATION ANGLE COMPUTER FOR THE AN/SPS-2 RADAR

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# THE ELEVATION ANGLE COMPUTER FOR THE AN/SPS-2 RADAR


E. E. Herman


November 19, 1951

Approved by:

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## ABSTRACT

The stacked-beam height-finding radar AN/SPS-2 requires as its elevation angle computer, a system capable of instantaneously reducing the signals from its seven beams to a single range-elevation-angle video signal. This reduction must be made in such a manner that elevation angle data is automatically and instantaneously determined from the distribution of echo energy among the seven beams.

The computer developed for this purpose operates by first selecting the pair of adjacent beams receiving the strongest returned echoes, then generating a pulse pedestal representing the beam pair selected, and finally, interpolating this pedestal, in accordance with the relative received echo strengths in the two beams, to the exact target elevation angle.

A novel peak selector circuit is employed which is capable of passing the strongest of several signals linearly while rejecting all signals more than 3 percent below the strongest one. The computer is expected to give accuracies of better than 1/8 beamwidth on signals 15 or more db above noise. Its minimum visible signal is expected to be about 3 db worse than that of a single channel, and it is expected to give about 1/4 beamwidth average accuracy on this minimum visible signal.

## PROBLEM STATUS

This report completes work on the computer phase of the problem. Work on other phases is continuing.

## AUTHORIZATION

NRL Problem R02-22
RDB NR 502-220

Manuscript submitted Sept. 27, 1951

# THE ELEVATION ANGLE COMPUTER FOR THE AN/SPS-2 RADAR

## INTRODUCTION

The radar AN/SPS-2 is a long-range search radar system of the stacked-beam height-finding type. It provides range coverage out to 300 nautical miles and height coverage up to 90,000 feet.

In the stacked-beam system, height finding is accomplished by using a number of separate receiving beams displaced vertically to form a stack and by computing target elevation angle from the distribution of the returned echo energy among these beams. In the AN/SPS-2 antenna system, a single reflector is fed by seven separate horn feeds. During transmission, all feed horns are excited in phase to provide a composite illumination pattern, while on receiving, the seven horns act independently to provide the required seven overlapping receiving beams shown in Figure 1. The problem of target elevation angle measurement is then one of converting incoming signals from the seven beams into a single range elevation-angle video signal.

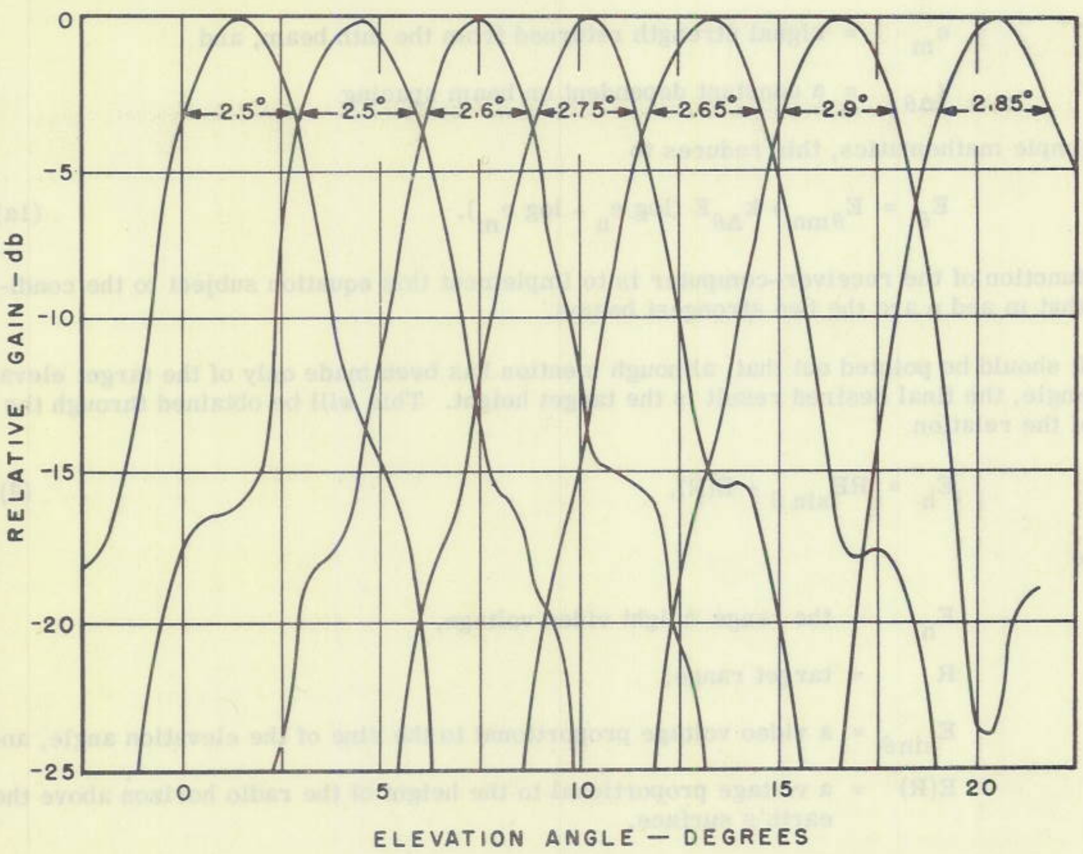


Figure 1 - Typical antenna vertical patterns

In the SPS-2, this is done by selecting the two beams in which the target is strongest, generating a voltage pedestal the amplitude of which is proportional to the crossover angle of these two beams, and interpolating to the exact elevation angle by modifying this pedestal in accordance with the relative received signal strengths. The antenna delivers to the two receivers associated with a particular pair of beams two signals whose amplitudes are such that the logarithm of their ratio is very nearly proportional to the deviation of the target elevation angle from the beam crossover angle. Interpolation, therefore, involves adding to the pedestal representing beam crossover angle the log of the ratio of input signal strengths multiplied by an appropriate constant. The elevation angle of a target is then

$$E_\theta = E_{\theta mn} + k_{\Delta\theta} E \log \frac{e_n}{e_m}, \tag{1}$$

where

$E_\theta$ = the range-elevation-angle video voltage,

$E_{\theta mn}$ = a pedestal voltage proportional to the crossover angle of the mth and nth beams ($n = m + 1$),

$e_n$ = signal strength returned from the nth beam,

$e_m$ = signal strength returned from the mth beam, and

$k_{\Delta\theta}$ = a constant dependent on beam spacing

By simple mathematics, this reduces to

$$E_\theta = E_{\theta mn} + k_{\Delta\theta} E (\log e_n - \log e_m). \tag{1a}$$

The function of the receiver–computer is to implement this equation subject to the condition that m and n are the two strongest beams.

It should be pointed out that, although mention has been made only of the target elevation angle, the final desired result is the target height. This will be obtained through the use of the relation

$$E_h = RE_{\sin\theta} + E(R), \tag{2}$$

where

$E_h$ = the range-height video voltage,

$R$ = target range,

$E_{\sin\theta}$ = a video voltage proportional to the sine of the elevation angle, and

$E(R)$ = a voltage proportional to the height of the radio horizon above the earth's surface.

Although, to facilitate this conversion, the actual computer will be set up to give as its output the voltage $E_{\sin\theta}$ (rather than the voltage $E_\theta$) we will, in the interest of simplicity, consider the computation of $E_\theta$. Since, for the range of angles involved (0 to 20 degrees) the sine differs from the angle by only a few percent, it is clear that with a slight readjustment of pedestal heights and interpolation gains, the output may be made to be $E_{\sin\theta}$ within a very minor error.

Before considering the actual computer circuitry, a few features of this computing method will be presented. It will be noted that target elevation angles are computed from two and only two beams. Thus, the loss in sensitivity to weak signals resulting from the mixing of videos will be only slightly more than is normally expected from the linear mixing of two videos even though there are actually seven received videos involved.[1] This is a very distinct advantage over the center-of-gravity type of computer[2] where all noise is mixed in a linear fashion. In addition to this weak signal advantage, the use of two-beam computing causes a more uniform distribution of the noise[3] over the face of the RHI (Range Height Indicator) scope. The center-of-gravity computer, on the other hand, gives an approximate Gaussian distribution of noise, centered around the center beams, so that weak echoes in this region are difficult to see.

Along with its weak signal advantage, the SPS-2 computer has a very definite advantage on strong signals. Since computing takes place only on the two strongest beams, the errors which would otherwise result from side lobes on the antenna pattern are eliminated.

## THE RECEIVER-COMPUTER

The r-f components and the mixers of the SPS-2 receiving system are, except for the complexity resulting from the high transmitted power (10 megawatts) and the number of receiving channels, perfectly straightforward. The i-f preamplifiers are unusual only because special attention has been given to their bandpass and linearity characteristics to insure correspondence of pulse shapes from different channels at all levels, and because they contain provision for a number of gain control and gating signal inputs.

The main i-f strips in the SPS-2 are specially designed to have a highly accurate logarithmic response[4] to facilitate the taking of ratios and to insure a wide dynamic range. The video outputs from these logarithmic receivers are combined in six video mixer units, each of which accepts signals from the log receivers for a pair of adjacent beams and delivers two outputs–the sum and the difference of these two inputs.

The sum outputs are provided for use in the selection of the pair of adjacent beams receiving the strongest signals, while the difference output is the interpolation voltage required by the parentheses of Equation (1a).

These six sum and six difference signals are fed to the computer where the elevation-angle video voltage is to be generated. The first operation performed by the computer is

[1] H. W. Lance, G. D. M. Peeler, and C. R. Randall, "Video Mixing Loss and Minimum Detectable Signal in the SPS-2 Radar," NRL Report R-3123 (Confidential), Sept. 1947

[2] Originally proposed for the Volscan and Volir Radars

[3] Actually six Gaussian distributions of approximately equal intensity centered around the six beam crossover angles

[4] T. H. Chambers, "The High Accuracy Logarithmic Receiver for AN/SPS-2," NRL Report 3848 (Confidential), Aug. 17, 1951

the selection, in two steps, of the correct pair of beams on which to compute. As a first step in this selection, the six sum signals are amplified and applied to the first peak selector as shown in the block diagram (Figure 2). The function of this selector is to identify (or "tag") instantaneously the sum signal having the largest amplitude.[5] When only noise is present, the tag outputs occur in random fashion among the six sum signals, simply denoting which one is receiving the greatest instantaneous noise level. When a signal is present near a beam crossover, the sum of the two beams encompassing the target will predominate, and the first selector will tag in the corresponding output line during the echo interval. If, however, a target lies near a beam tip, the first selector is unable to discriminate because the sum outputs of two adjacent pairs of beams are nearly alike, and two tag outputs will occur, denoting that the target lies close to both pairs of beams. Under these conditions, the discrimination provided by the first selector is insufficient and a closer selection is effected in a second selector on the basis of comparison of difference voltages.

When a target, not exactly on beam tip, is detected on two pairs of beams, the smaller difference output will occur in the pair lying closest to the target position. Making use of this fact, the second selector serves to identify the correct channel pair by comparing the amplitude of the difference signals. Before this comparison is effected, however, two manipulations are performed. First the difference outputs are selectively inverted so that regardless of the sign of the difference input, the output is always of one polarity. Second, this uni-polarity output is subtracted from a constant so that the result is a pulse whose amplitude is proportional to $K - |\Delta|$ where $|\Delta|$ is the absolute value of the difference signal. By applying these pulses to the second selector and choosing the larger, the one actually tagged will correspond to the channel pair having the smaller difference. The difference pulses are not continuously applied to the second selector but are gated-in only on those channels which were identified in the first selector.

Recapitulating, then, when only one tag occurs in the first selector, only one modified difference pulse is gated into the second selector which in turn merely tags and passes the information on. When two sums are tagged in the first selector, two inputs are gated into the second selector which, on the basis of comparison of difference amplitudes, chooses the correct beam pair. In the event that a target lies exactly on a beam tip, the sums are alike and the difference signals have the same absolute magnitude; the second selector then tags both pairs since they have data of equal merit.

Following the second selection, each tag output is used as a gating signal. This gating action accomplishes two purposes: the pulse pedestal, $E_{\theta mn}$ of Equation (1a) is generated, and the appropriate difference signal is gated-in to interpolate this pedestal to the exact target elevation angle. In the case of a beam-tip target where two selectors produce two tags, two pedestals will be produced, the lower one being interpolated upward 1/2 beamwidth and the higher one being interpolated downward 1/2 beamwidth, so that both channel pairs produce the same answer.

The final peak selector serves to combine the outputs of the six beam-pair channels into a single elevation-angle video output. The peak-selection principle is used here to prevent the generation of false target elevation-angle indications in the event that two beam-pair channels simultaneously give computed outputs. Since the peak selector is responsive only to the highest applied signal level, and passes this signal linearly, it will present the higher elevation angle target while the lower target will be discarded. Thus, an air target will be favored over ground clutter.

[5] A second function which may also be served by this selector is to furnish a nonlinear mixed video for intensity modulation of PPI and RHI scopes.

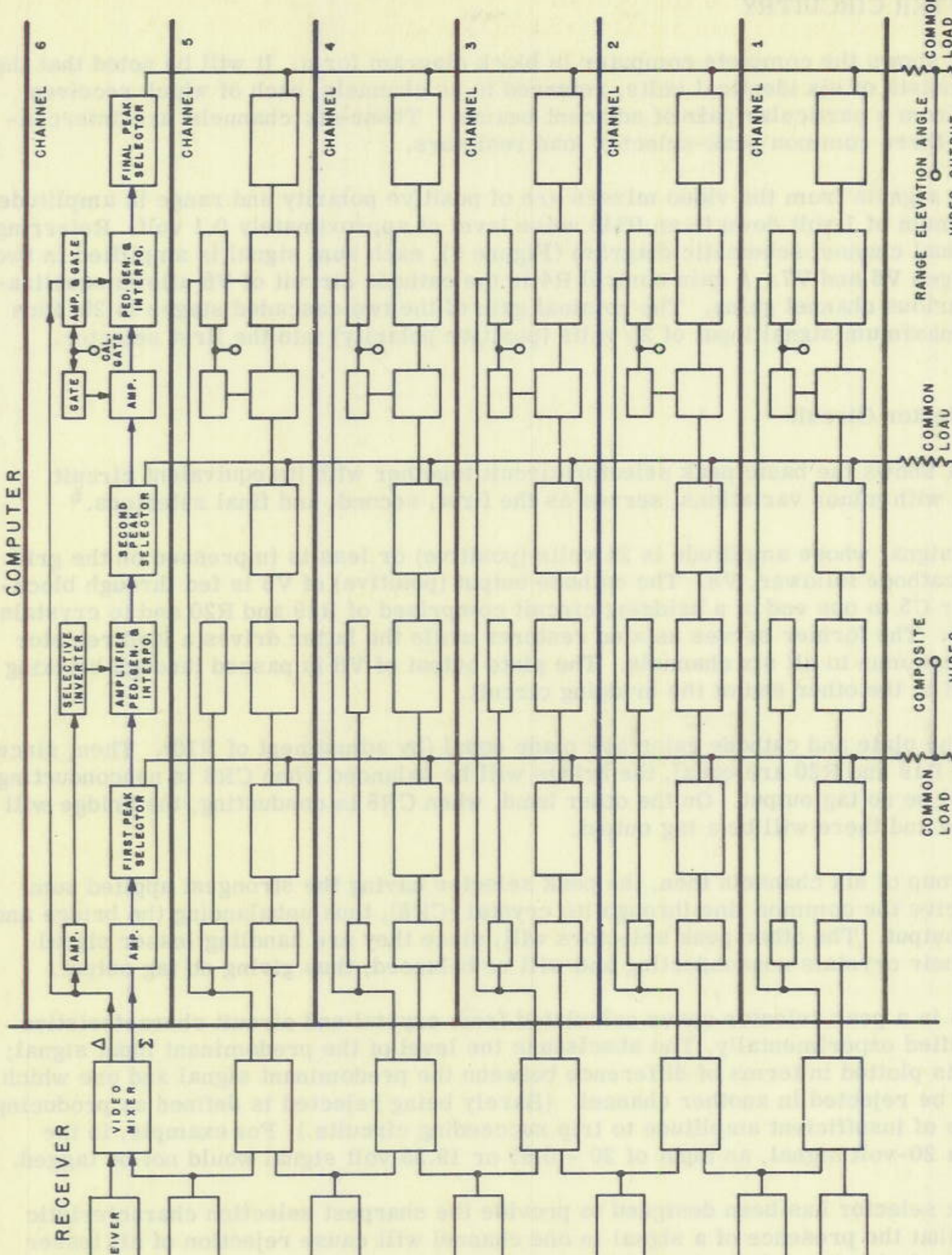


Figure 2 - Block diagram - receiver-computer for AN/SPS-2 radar

## THE COMPUTER CIRCUITRY

Figure 2 shows the complete computer in block diagram form. It will be noted that the computer consists of six identical units, referred to as channels, each of which receives information from a particular pair of adjacent beams. These six channels are interconnected at the three common peak-selector load resistors.

The sum signals from the video mixers are of positive polarity and range in amplitude from a maximum of 1 volt down to an RMS noise level of approximately 0.1 volt. Referring to the individual channel schematic diagram (Figure 3), each sum signal is amplified in two cascaded stages V6 and V7. A gain control R4 in the cathode circuit of V6 allows equalization of the various channel gains. The nominal gain of the two cascaded stages is 25, thus providing a maximum signal input of 25 volts (positive polarity) into the first selector.

### The Peak Selector Circuit

Figure 4 shows the basic peak selector circuit together with its equivalent circuit. This circuit, with minor variations, serves as the first, second, and final selectors.[6]

A video signal whose amplitude is 25 volts (positive) or less is impressed on the grid of the plate-cathode follower, V8. The cathode output (positive) of V8 is fed through blocking condenser C5 to one end of a bridging circuit comprised of R19 and R20 and to crystals CR7 and CR8. The former serves as a dc restorer while the latter drives a load resistor Ra which is common to all six channels. The plate output of V8 is passed through blocking condenser C6 to the other end of the bridging circuit.

In use, the plate and cathode gains are made equal (by adjustment of R10). Then, since the values of R19 and R20 are equal, the bridge will be balanced when CR8 is nonconducting, and there will be no tag output. On the other hand, when CR8 is conducting, the bridge will be unbalanced and there will be a tag output.

In the group of six channels then, the peak selector having the strongest applied sum signal will drive the common line through its crystal (CR8), thus unbalancing the bridge and giving a tag output. The other peak selectors will, since they are handling lesser signal level, have their crystals nonconducting and will be balanced, thus giving no tag output.

Figure 5 is a peak selector curve calculated from crystal and circuit characteristics and then verified experimentally. The abscissa is the level of the predominant input signal; the ordinate is plotted in terms of difference between the predominant signal and one which would barely be rejected in another channel. (Barely being rejected is defined as producing a tag, but one of insufficient amplitude to trip succeeding circuits.) For example, in the presence of a 20-volt signal, an input of 20 - 0.65 or 19.35 volt signal would not be tagged.

The peak selector has been designed to provide the sharpest selection characteristic possible, so that the presence of a signal in one channel will cause rejection of all lesser amplitude signals in other channels. There are three primary factors besides frequency response considerations entering into the efficiency of selection. When a tube drives the common load, the cathode gain is reduced slightly as compared to those stages not so loaded. This effect is minimized by using the highest possible $g_m$ in the driving stage, hence two parallel tubes. Another factor affecting the sharpness of selection is the voltage drop across the crystal during conduction. This drop is a function of crystal current

[6] In the schematic diagram, Figure 3, the corresponding tubes involved in these selectors are V8, V12, and V17

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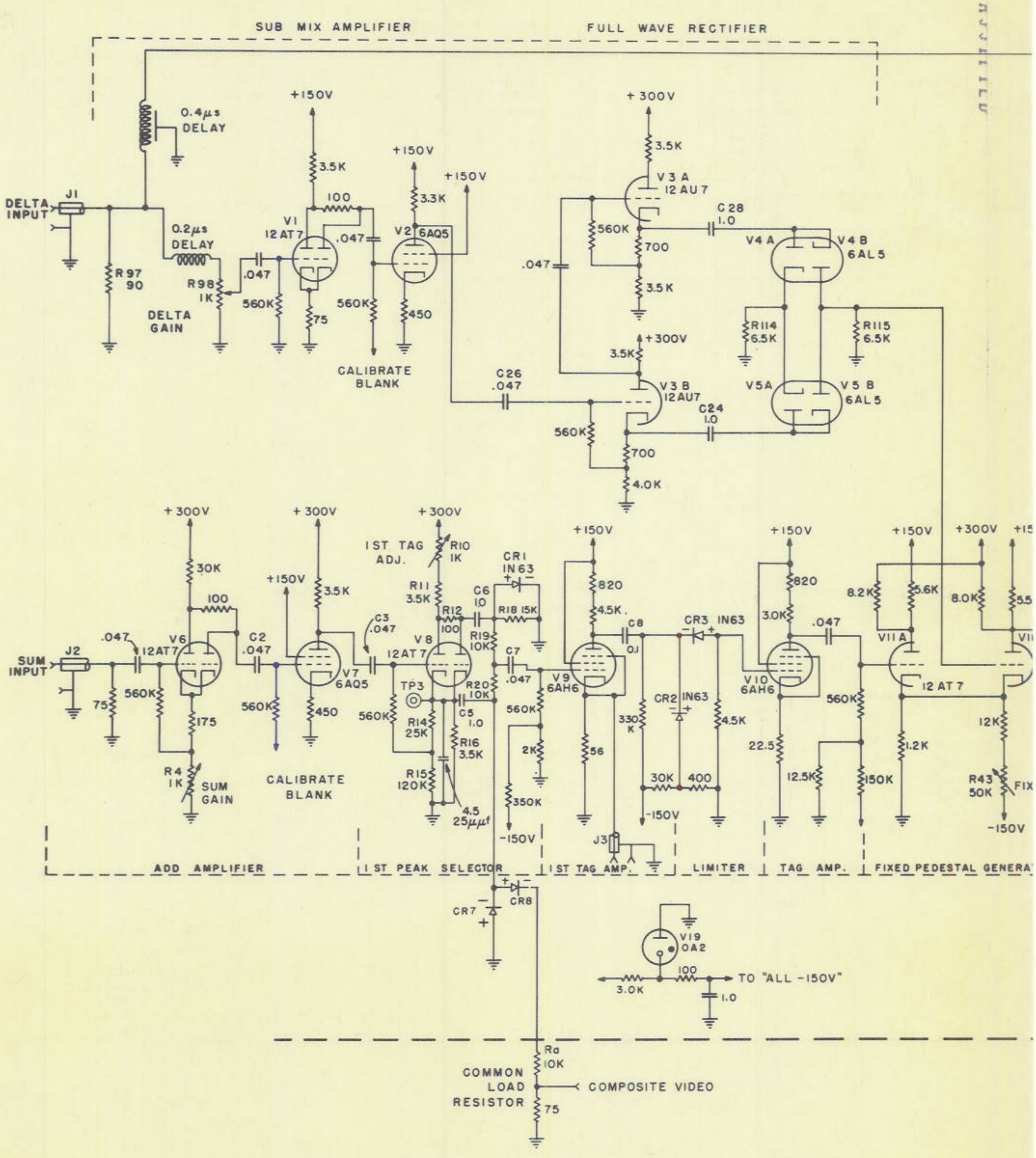


Figure 3 - Schematic diagram—one ch

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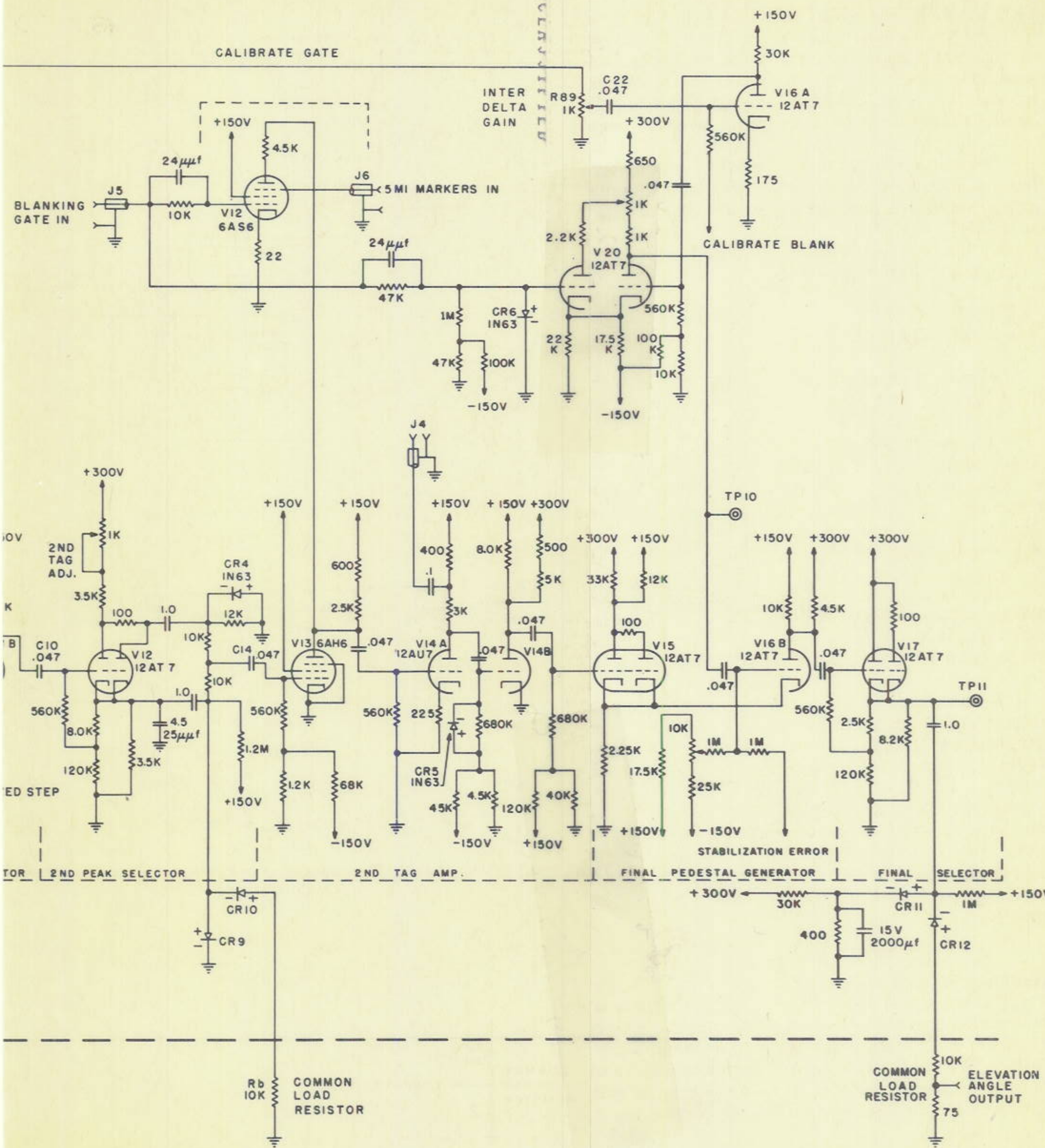
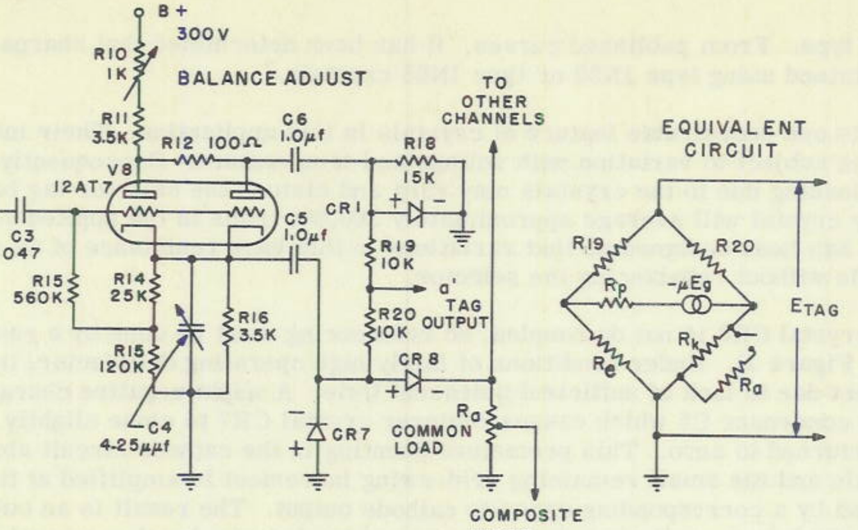



annel of computer for AN/SPS-2 radar




$$E_{TAG} = \frac{-\mu\, e_{in}\, R\,(R_e - R_k)}{2RR_k(1+\mu) + R_p(2R + R_k) + R_e(2R + R_p)}$$

where;

$R_e$ = R18 paralleled with series value of R10 and R11

$R_k$ = R16 when not tagging,
R16 paralleled with $R_a$ when tagging,

$R_p$ = The parallel dynamic plate resistance of two tubes, and

R19 = R20 = R

Figure 4 - The basic peak selector circuit and its equivalent circuit

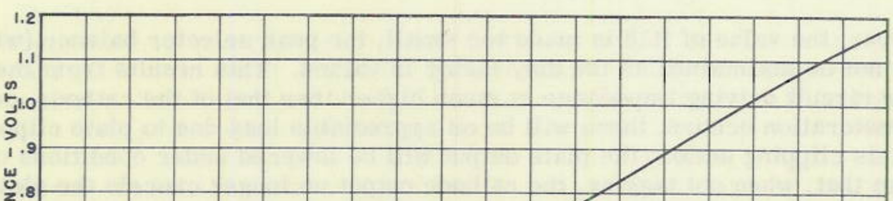



Figure 5 - Peak selector characteristics

and crystal type. From published curves, it has been determined that sharpest selection could be obtained using type 1N39 or type 1N63 crystals.[7]

There is one undesirable feature of crystals in this application. Their inherent back resistance is subject to variation with voltage and temperature. Consequently, the back resistance loading due to the crystals may vary and disturb the selector tag balance. A good quality crystal will average approximately 300,000 ohms in the applied voltage range. The circuit has been designed so that variations in this back resistance of as much as 50% are tolerable without rebalancing the selector.

Since crystal CR8 is not dc coupled, dc referencing must be done by a restorer crystal (CR7 in Figure 2). Under conditions of fairly high operating duty factor, the restoration is not perfect due to lack of sufficient quiescent time. A slight negative charge is retained on coupling condenser C5 which causes restorer crystal CR7 to close slightly before the input has returned to zero. This premature shunting in the cathode circuit abruptly raises the plate gain and the small remaining grid-swing increment is amplified at the plate and not cancelled by a corresponding opposite cathode output. The result is an output from the tag circuit which is opposite in polarity to normal tag but of a level comparable to typical tag amplitudes. This undesired output causes grid current and back biasing in the subsequent amplifiers with resulting paralysis.

In order to counteract this effect, a compensation circuit is employed in the peak selector plate output. Coupling condenser C6 feeds a load resistor R18 and a crystal CR1, providing a charging impedance comparable to the cathode circuit. It will be noted that the cathode-circuit charging impedance depends somewhat upon the probability of any one channel driving the common load Ra. Considering noise only, with six sum channels operative, any one channel is driving with approximately 16% duty factor. As channels are switched out, this probability increases. In spite of this nonconstancy of cathode loading, a compromise value of R18 is possible which causes the plate circuit to clamp (restore) at approximately the same time as the cathode restorer. Hence, the plate gain cannot rise and produce a spurious amplified output.

If, however, the value of R18 is made too small, the peak selector balance (when not tagging) will not be maintained as the duty factor is varied. This results from the fact that the plate circuit driving impedance is much higher than that of the cathode, so that when plate restoration occurs, there will be an appreciable loss due to plate clipping. Because of this clipping action, the plate output will be lowered under conditions of high duty factor so that, when not tagging, the cathode output no longer cancels the plate output and spurious signals result. The correct value of R18 must be empirically established after the system is placed in operation and receiver gain and noise settings established. Figure 6 shows typical tag outputs which result from various values of R18.

### The First Selector

The performance of the above described circuit as the first peak selector may be calculated from Figures 5 and 7 with the aid of certain general assumptions. It is assumed that the maximum signal input to any receiver will be no more than 60 db above noise and that with this maximum signal applied to two adjacent receivers the resulting sum input will be about 25 volts. It is further assumed that the output of a logarithmic receiver is directly proportional to the input in db. Therefore the sum of the video outputs of two

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[7] Tube diodes such as the 6AL5 did not provide as sharp selection; furthermore, Edison effect and capacity feed-through detract from performance

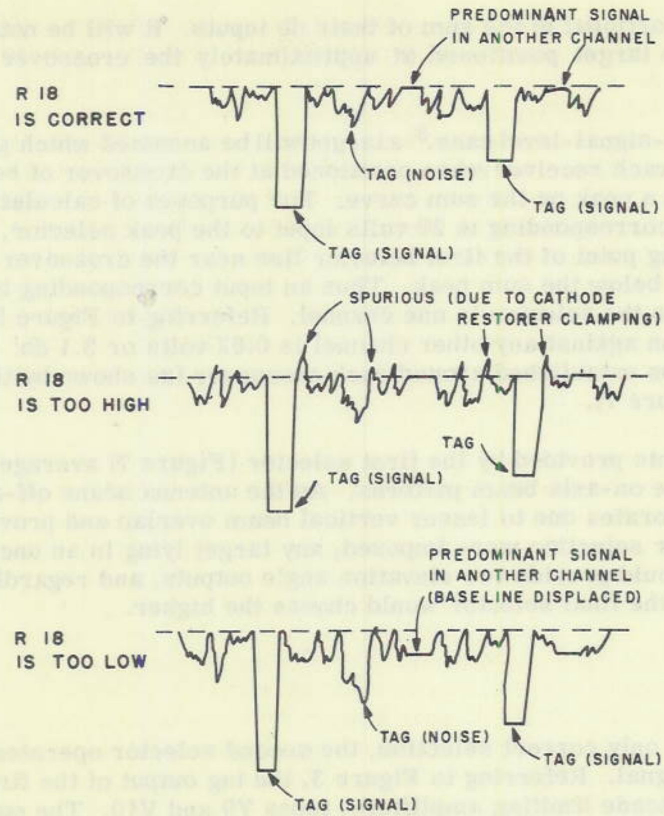


Figure 6 - Typical tag outputs for various values of R18

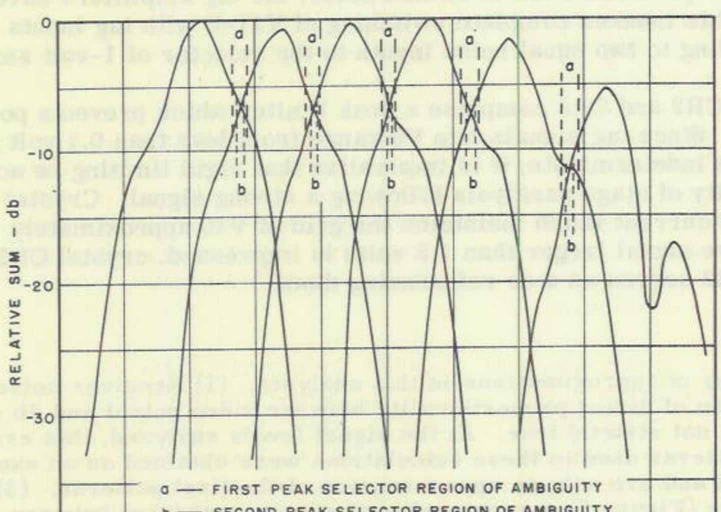


Figure 7 - Typical sum signal curves

receivers will be proportional to the sum of their db inputs. It will be noted that the maximum sum occurs for a target positioned at approximately the crossover of two adjacent beams.

In analyzing a high-signal-level case,[8] a target will be assumed which produces a 50-db (above noise) input to each receiver when positioned at the crossover of beams 1 and 2, a point corresponding to a peak on the sum curve. For purposes of calculation, 100 db sum input will be taken as corresponding to 20 volts input to the peak selector, or 0.2 volt per db input. The switching point of the first selector lies near the crossover on the sum curve or approximately 6 db below the sum peak. Thus an input corresponding to 94 db, or 18.8 volts, will be applied to the selector in one channel. Referring to Figure 5 for this input of 18.8 volts, the rejection against any other channel is 0.62 volts or 3.1 db. By this method, switching points may be established around each crossover (as shown by the dashed lines on the sum curve, Figure 7).

The switching points provided by the first selector (Figure 7) average approximately one degree wide for the on-axis beam patterns. As the antenna scans off-axis (in azimuth) the sum pattern deteriorates due to lesser vertical beam overlap and provides even worse selection. If no further selection were imposed, any target lying in an uncertainty region of the first selector would provide two elevation angle outputs, and regardless of which answer were correct, the final selector would choose the higher.

## The Second Selector

In order to insure only correct selection, the second selector operates on the more sensitive difference signal. Referring to Figure 3, the tag output of the first selector is passed through two cascade limiting amplifiers, tubes V9 and V10. The output of V10 in turn serves to cut off tube V11-A thus switching in, by cathode coupling, the associated gating tube and pedestal generator V11-B.

In order to allow peak selection down into noise, the tag amplifiers have a cascaded gain of over 400. This insures complete switching of V11-B with tag inputs of as low as 0.1 volt, corresponding to two equal noise inputs to the selector of 1-volt amplitude.

Crystal diodes CR2 and CR3 comprise a peak limiter which prevents positive overdrive into tube V10. Since tag signals into V9 range from less than 0.1 volt up to 4 volts and the duty cycle is indeterminate, it is imperative that rigid limiting be accomplished without any possibility of stage paralysis following a strong signal. Crystal CR3 normally passes a dc forward current which maintains the grid of V10 approximately 1.5 volts negative. When a positive signal larger than 1.5 volts is impressed, crystal CR3 ceases conducting. Crystal CR2 serves as a dc referencing diode.

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[8] There are a number of approximations in this analysis. (1) Receiver noise is neglected. Thus the assumption of direct proportionality between video output and db signal input to the receivers is not strictly true. At the signal levels analyzed, this error is minor. (2) The antenna patterns used in these calculations were obtained on an experimental scaled-down model and are only an approximation of the final patterns. (3) In using the peak selector curve (Figure 5), a mean value of signal input lying between the predominant and the minor signal was used rather than the true predominant signal. This approximation results in slightly narrower switching regions than is actually obtained; however, this error is less than graphical inaccuracies.

The cathode coupled stage V11-B serves two functions. As mentioned earlier, in order to effect the necessary comparison of difference signals, it is required to subtract the rectified difference voltages from a constant amplitude pedestal. Assuming no difference signal input to V11-B, the switching action causes a negative pulse pedestal to be produced at the plate output. This pedestal is adjusted to 15 volts amplitude in each channel. Individual adjustment is provided by variable resistor R43 in the channel shown.

The selectively inverted difference signal for interpolation of these pedestals is obtained as follows. The difference signal from each video mixer is passed through two cascaded amplifiers (V1 and V2 in Figure 3) which raise the input level from $\pm 0.5$ volt maximum up to approximately 10 volts. The difference signal is then phase-inverted in V3-A and V3-B and supplied at low impedance to two dual diodes V4 and V5.

When a negative difference input occurs, diode V5-B supplies the common load resistor R115. The inverted positive output feeds the dummy load R114 through V4-A. Conversely a positive difference input to the computer, being inverted by tube V3-A, provides a negative drive through diode V4-B. The corresponding positive output drives resistor R114.

Due to the bi-polar nature of the difference signals, dc referencing cannot be carried out in the conventional manner. In order to establish a zero dc reference at the center line of the difference inputs, symmetric impedances are employed in the rectification circuits following coupling condensers C24 and C28. Tube diodes V4-A and V5-A together with resistor R114 serve merely to make the diode load impedances symmetrical. By establishing this symmetry, the net charging currents in coupling condensers C24 and C28 are made zero. The negative rectified output from R115 is direct-coupled into the grid of V11-B and interpolates the associated pedestal downward from a 15-volt maximum to a minimum of approximately 8 volts.

These difference-interpolated pedestals are then applied to the second peak selector which, in choosing the highest input, actually chooses the channel having the smaller difference. The action of the second peak selector is identical in principle to that of the first, except that the polarity of inputs and of the crystal circuit are reversed. Figure 8 is a plot of the difference outputs calculated from the individual antenna patterns (Figure 1). The ordinate is shown in db since, due to the logarithmic receivers, the db difference corresponds directly to volts output from the video mixers. The switching points provided by the second selector are calculated on the basis of these difference plots and are shown by the dotted lines on Figure 7.

As a basis of calculation, the difference comparison gain is assumed to be 0.5 volt per db, thus 15 db of difference produces an interpolation of 7.5 volts on the pedestal. Since the switching points lie close to the difference maximums, the approximate signal level into the second selector is 8 volts. From Figure 5, the rejection at this level is 0.26 volt, or converting, 0.52 db. In terms of the difference plot (Figure 8), the switching region is defined by that region where the difference amplitudes are within 0.65 db (absolute magnitude) of each other.

## The Pedestal Generator and Interpolation

Following the second peak selector, the tag outputs are amplified and limited in three cascaded stages. An over-all gain of more than two hundred is provided. The negative output of tube V14-B (Figure 3) serves to cut off tube V15 which comprises one-half of the final pedestal generator. By cathode coupling, V16-B is gated on, therby generating a pedestal and allowing the difference input voltage to interpolate the pedestal to exact elevation angle (or sine thereof). Individual channel adjustment of the final pedestal amplifier is provided in each channel by a bias potentiometer (R81 in Figure 3). The pedestal voltages from the six sum channels are combined in the final selector. For convenience in calibration, and because a constant is clipped from each pedestal in the final selector, the amplitude settings of these pedestals are referred to the computer output rather than to the plate of the pedestal generator V16-B.

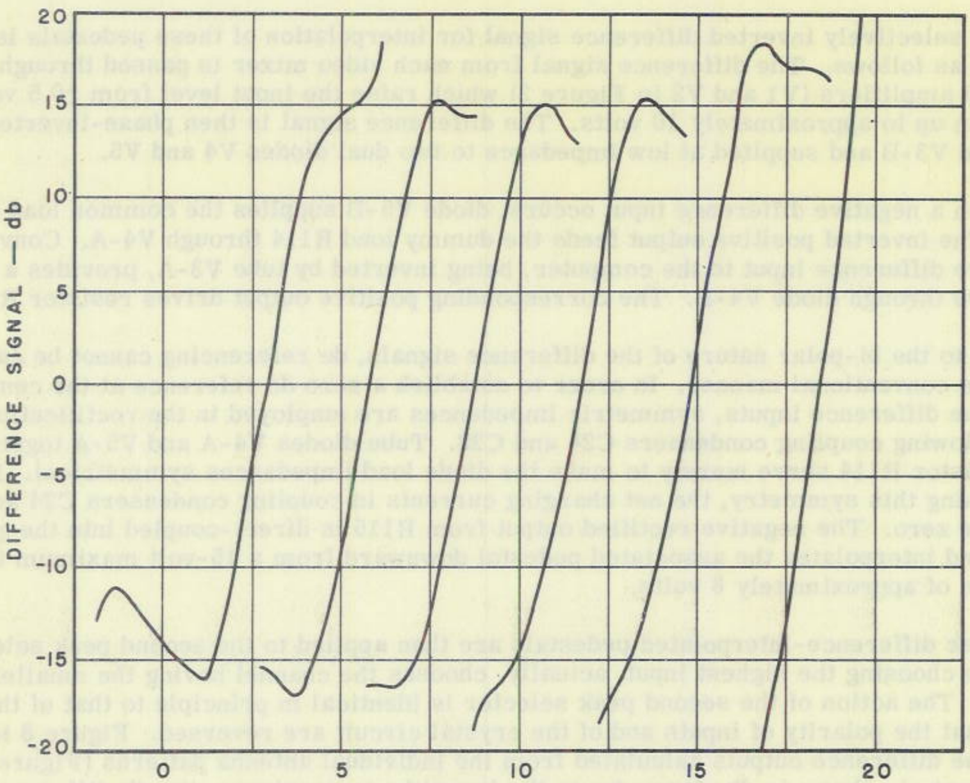


Figure 8 Typical difference signal curves

The beam crossovers of the antenna pattern determine the amplitude settings of the final pedestal generators. On the typical antenna pattern shown, these crossovers lie at 3.0°, 5.9°, 8.7°, 11.6°, 14.7°, and 18.5°. The pedestal voltages are set to correspond exactly to the beam crossover angles.[9]

The difference interpolation input which corrects the pedestal to exact elevation angle is applied to the grid of tube V16-B (Figure 3). The maximum interpolation required on any pedestal is slightly more than one-half of one beamwidth. Considering the lowest beam pair, the pedestal setting is 3.1 volts. One-half beamwidth higher or midway to the next higher pedestal is $3.1 + 5.9/2 = 4.5$ volts. Thus an interpolation of ±1.4 volts (plus reserve) is required. In order to provide this low level pedestal for the bottom beam crossover and still maintain the required linearity of interpolation, the actual pedestal

[9] When the computer is adjusted to provide the sine of the elevation angle, the pedestal amplitudes (as measured at the computer output) are set in accordance with the equation:

$$E_{\theta mn} = 57.25 \sin \theta_{mn}$$

generated in tube V16-B is set to a value higher than necessary by approximately 3 volts (plus a small additional increment to make up for the loss in the final selector) and the final selector crystal circuit is back-biased so that 3 volts are clipped from the base of each pedestal. By this technique, interpolation linearity may be maintained throughout the full interpolation range. Although this artifice is only required in the lowest channel, in order to allow all channels to be identical, the same technique is employed in all six channels.

Referring again to the final pedestal interpolation, the bi-polar difference signals required for interpolation are amplified in a single stage (V16-A in Figure 3) from ±0.5 volts up to approximately ±2 volts. The plate output of V16-A is fed through a coincidence gate V20-B whose sole function is in connection with calibration. During normal computation, this gating circuit merely passes the difference signals to the grid input of the final pedestal generator V16-B.

### The Channel Output Selector

The interpolated pulses from the six final pedestal generators are combined in the final selector to form a single elevation-angle output. This combination must be effected in such a manner that no errors result from two simultaneous sources of elevation data. When a target lies exactly at a beam tip on the antenna pattern, both the first and second selectors will tag in two channels, and two final pedestals will be generated. One will be interpolated upward one-half beamwidth and the other will be interpolated downward to the identical amplitude. The final selector is designed so that the maximum output error resulting from this condition is less than 17 minutes. This error decreases proportionally with elevation angle.

## CALIBRATION

Exclusive of the final stages of the computer, the primary requirement of calibration is to insure identical performance in all computing channels. The circuitry throughout the computer is designed to minimize errors resulting from tube changes and from drift. Since it is anticipated that only an occasional check will be required rather than a continuous monitor, a manual checking procedure is planned. This will involve two rotary switches with an associated test oscilloscope. In order to keep the discussion general, the calibration requirements and means of attainment will be described rather than specific details of the switching system.

The manual calibration of the computer makes use of pulses derived from a continuous monitor incorporated in the receiving system of the SPS-2 to provide a visual check of the receiver gains, slopes, and noise levels. Briefly, this continuous monitor employs a series of 5 r-f pulses which are timed to occur during the normal retrace period just prior to the next transmitter pulse. These pulses are applied to a monitor antenna which serves to illuminate uniformly all receiving beams of the antenna. The width of the monitor pulses is 7 microseconds with a spacing of 15 microseconds. Each of the five pulses is attenuated approximately 10 db below its predecessor with the first having a level of approximately 60 db above noise.

For purposes of manual calibration of the computer, the second of this series of five pulses is employed. This insures a test signal well below overload, yet relatively unmodulated by noise. Since all receiving beams are uniformly illuminated, a test pulse signal is provided at the computer with all sum inputs equal and the difference signals zero. Provision is also incorporated in the receiving system to reduce artifically the gain in either the even or odd receiving channels by a predetermined number of db. By introducing this "gain offset" prior to the log receivers, a known difference signal independent of r-f level is made available for computer calibration.

Within the computer itself, it is planned to incorporate a video pulse generator as part of the calibration system. This generator will be triggered just prior to the second of the 5 r-f monitor pulses, and will provide a pulse slightly longer than 7 microseconds to insure time coverage of the monitor signal.

The peak selector circuits of the computer provide a convenient means of checking relative pulse amplitudes. For this reason, the first step in calibration involves balancing the first peak selector. As mentioned previously, the tag output of the selector is adjusted for zero output when not shunted by the common load resistor (Ra). To provide this unloaded condition, the above mentioned video pulse is injected into the common load with positive polarity with an amplitude sufficient to insure that no sum channel will drive the common load resistor. Only one sum channel is activated at a time (cutoff bias is applied to all others during the calibration procedure) and any residual tag output is observed with the test oscilloscope.

After all channels of the first peak selector are balanced, the input to the common load can be reduced to a value comparable to that expected from the second monitor pulse input to the selector. Each channel will again be activated in turn and its gain adjusted until a slight tag output begins to show. Since the threshold region of the peak selectors is very narrow, a small change in sum gain will cause a wide variation in tag output.

In order to prepare the second peak selector for use in signal comparison, it is next balanced by injecting a negative video pulse into its common load resistor. Again only one sum channel is activated at a time, thus producing a tag in the first selector which in turn will generate a pedestal input for the second selector. Each pedestal is then set to correct value by using the second peak selector as a means of comparison against the video pulse injected into the common selector load resistor. During this step the receiver gain offset is not applied so that no difference signal occurs.

In order to set the difference comparison gains, the gain offset is now introduced, and the video comparison pulse into the second peak selector common load is reduced to the amplitude expected of the difference interpolated pedestal. Each difference gain is set for a slight tag signal showing.

A slightly different technique will be used to set the final pedestals corresponding to beam crossovers. A pulse measuring vacuum tube voltmeter will be employed for this purpose. In this pulse voltmeter, known dc voltages will serve to back-bias a diode in accordance with each pedestal amplitude required. The test oscilloscope will serve as an indicating means. The final pedestals must first be set to correct amplitude without any interpolation present, then the gain offset is introduced to provide a known interpolation whereupon the final interpolation gains can be set.

All parts of this calibration procedure will be set up by two rotary selector switches. The first of these, the function switch, will set up the correct conditions for the testing of a particular function. The second switch, the channel switch, will then connect the test signals and test scope to the desired channel.

There is one circuit incorporated in the computer which, although intended primarily to provide constant angle calibration marks for the range-height indicator, does serve as a partial check of the final circuits of the computer. In each channel a pentode is connected across the second tag amplifier to provide a means of injecting calibration pulses. Normally these pulses will be injected every 16th sweep to trigger the final circuits thereby producing pedestals corresponding to beam crossovers. In order to prevent any final difference interpolation of the pedestals during the calibration marks, coincidence gating tube V20 is interposed in each difference channel.

## COMPUTER PERFORMANCE

The performance of the basic computing method is shown graphically in Figure 9. This plot has been made on the basis of computing elevation angle (rather than the sine thereof) and includes lines showing error of ±1/4 degree.

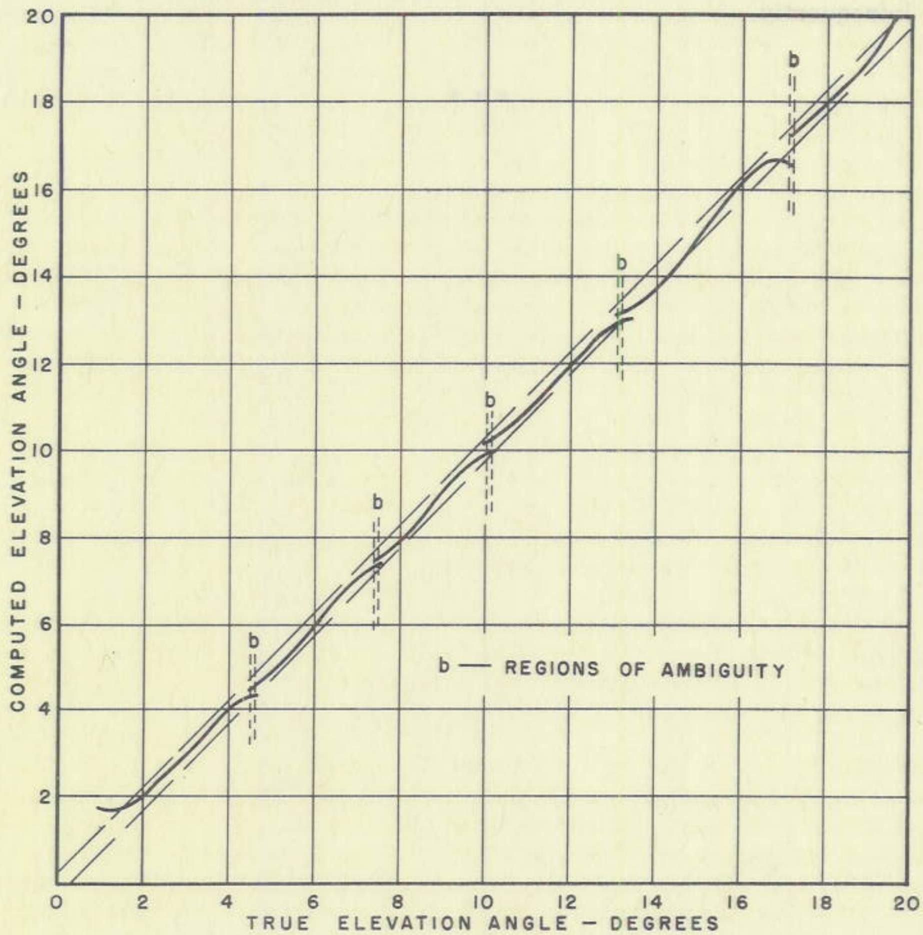


Figure 9 - Computer output characteristics

It will be noted that, with the exception of the range between 17.0 and 17.2 degrees, the method is capable of better than 1/4 degree accuracy. In a physical computer there will be additional errors (not included in Figure 9) which result from such factors as inaccuracies in log receiver response, nonlinearities in video amplifiers, lack of perfect balance in peak selectors, etc. These errors will, of course, lower computer performance. It is expected that, while peak errors in the complete system may run as high as 30 minutes, average errors will be considerably less, perhaps in the order of 10 to 15 minutes.

Although computer performance in noise has not been stressed at any length by this report, it is probably worthwhile to quote figures for expected performance in noise. The computer minimum visible signal is expected to be about 3 db worse than that of a single receiver channel. It is further expected that the computed elevation angle on this minimum visible signal will be accurate to an average error of about 40 minutes and a maximum error of about 1.3 degrees. As signal strength increases, accuracy is expected to improve rapidly, becoming the strong signal accuracy quoted above when the signal is about 12 db above noise.

The reliability of the computer is expected to be good. Although there are many circuits and numerous adjustments involved, the setup procedure is such that these adjustments may be made accurately, and circuit stability is such that readjustment need be made only infrequently.

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