Naval Research Laboratory
Washington, DC 20375-5320

NRL/6850/MR—2023/1

Memristive Neuromorphic Computing Elements

HANS S. CHO, PI
LAURA B. RUPPALT (FORMER EMPLOYEE)
FRANK K. PERKINS
CORY CRESS

Solid-State Circuits and Electromagnetic Materials Section
Electronics Science and Technology Division

ENRIQUE COBAS
ADAM FRIEDMAN (FORMER EMPLOYEE)

Magnetoelectronic Materials and Devices Section
Material Science and Technology Division

MARIO ANCONA (FORMER EMPLOYEE)

Nanoelectronics Section
Electronics Science and Technology Division

JOHN RODGERS (FORMER EMPLOYEE)

Vacuum Electronics and Advanced Materials Section
Electronics Science and Technology Division

ALEXANDER KOZEN
THOMAS LARRABEE

Jacobs, Inc.
Washington, DC

TIMOTHY WALTER

NRC Post-Doc
Washington, DC

December 5, 2023

DISTRIBUTION STATEMENT A: Approved for public release; distribution is unlimited.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing this collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports (0704-0188), 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number. **PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.**

1. REPORT DATE *(DD-MM-YYYY)*	**2. REPORT TYPE**	**3. DATES COVERED** *(From - To)*
05-12-2023	NRL Memorandum Report	01-10-2018 – 30-09-2020

4. TITLE AND SUBTITLE

Memristive Neuromorphic Computing Elements

5a. CONTRACT NUMBER
N0001419WX00060

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER
0602271N

6. AUTHOR(S)

Hans S. Cho, PI, Laura B. Ruppalt, Frank K. Perkins, Cory Cress, Enrique Cobas, Adam Friedman, Mario Ancona, John Rodgers, Alexander Kozen*, Thomas Larrabee*, and Timothy Walter

5d. PROJECT NUMBER

5e. TASK NUMBER
EL-271-016

5f. WORK UNIT NUMBER
6B53

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Naval Research Laboratory
4555 Overlook Avenue, SW
Washington, DC 20375-5320

8. PERFORMING ORGANIZATION REPORT NUMBER

NRL/6850/MR--2023/1

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)

Office of Naval Research
875 N. Randolph Street
Arlington VA 22203-1995

10. SPONSOR / MONITOR'S ACRONYM(S)
ONR

11. SPONSOR / MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION / AVAILABILITY STATEMENT

DISTRIBUTION STATEMENT A: Approved for public release; distribution is unlimited.

13. SUPPLEMENTARY NOTES

*Jacobs Inc., 601 New Jersey Avenue, N.W.4th Floor, Washington, DC 20001

14. ABSTRACT

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			**17. LIMITATION OF ABSTRACT**	**18. NUMBER OF PAGES**	**19a. NAME OF RESPONSIBLE PERSON**
a. REPORT	**b. ABSTRACT**	**c. THIS PAGE**			Hans Cho
U	U	U	SAR	16	**19b. TELEPHONE NUMBER** *(include area code)* (202) 767-0032

Standard Form 298 (Rev. 8-98)
Prescribed by ANSI Std. Z39.18

This page intentionally left blank.

CONTENTS

This page intentionally left blank.

EXECUTIVE SUMMARY

In this work, fundamental components of a neuromorphic system, including nanoelectronic equivalents of synapses and neurons with signal (spike) integration and generation functionalities, were demonstrated using oxide memristor-based devices. Both non-volatile and volatile memristors were demonstrated, with control over oxide stoichiometry, which corresponded to the electrical behavior. Circuits comprised of these devices were simulated and shown to exhibit behaviors analogous to those of biological spiking neurons. These devices and circuits form the basis of systems that can perform specialized computing tasks far more efficiently than conventional Si CMOS-based systems in terms of SWaP (size, weight and power) criteria.

This page intentionally left blank.

Final Report: Memristive Neuromorphic Computing Elements (Work Unit: 6B53)

1. INTRODUCTION

1.1 Background and Motivation

The program addresses the device hardware elements of neuromorphic (a.k.a., brain-inspired) computing, which has been proposed as an alternative to the dominant Von Neumann computing paradigm based on digital hardware. Complex and imprecise tasks such as image recognition and human speech acquisition may be processed more effectively and efficiently using neuromorphic computing devices. While reengineered digital hardware has been successfully employed in neuromorphic computing methods, such as deep learning neural networks, these have required large volumes of hardware and immense amounts of energy to perform tasks that humans perform routinely using brains consuming several orders of magnitude less space and energy. This becomes a significant barrier to deployment in various Department of Navy (DON) systems such as airborne, submersible, or space-deployed remote and autonomous systems, where size and power limitations are mission-critical. Furthermore, as outlined in the DON 30 Year Research and Development Plan (2017 version) [1], systems with advanced cognitive computing capabilities are forecast to increasingly become central to all DON systems fleet-wide. This transformation will not be possible unless supported by the development of a new scalable and projectable architecture. However, commercial interests are less incentivized to address these issues, instead focusing on the established approach of cloud computing based on connectivity to centralized datacenters. The orthogonal requirements of the DON to limit SWaP while offering orders of magnitude additional computational capabilities motivate efforts to develop a new paradigm for computing devices and architectures, independent of industry driving forces.

In analogy to the biological neural system and its components, a neuromorphic computing system can be modeled as a network consisting of nodes, or neurons, that are connected to other neurons by synapses, which may number several thousand per neuron. In this model, the synapses dynamically modulate electrical impulses (spikes) travelling between neurons, which integrate and synthesize the received impulses into a state response, which in turn triggers the axon hillock to fire a spike through the axon channel which propagates to neighboring neurons, again via synapses. Recently, nano-scale devices known as memristors [2] have demonstrated electrical response properties strongly analogous to those of synapses [3] that in a Si-based architecture would require circuitry consuming hundreds of μm^2 of die area to replicate. Hybrid circuits combining memristor synapses with neuron equivalents fabricated in CMOS have been developed [4-6]. Although a CMOS-based threshold switch is simple to realize, and has the advantage of being naturally compatible with the digital infrastructure prevalent today, its power consumption and circuit area footprint limits its scalability going forward, and the integrate and fire (IF) mechanism it reproduces is simplistic and incapable of resolving or generating complex temporal spiking behavior. The shortcomings of CMOS have motivated efforts towards using memristors to emulate spiking behavior, and simple spiking has been reported in Mott-insulator-based neuristors [7] and memcapacitive circuits [8]. These approaches utilize the mechanism of spiking by capacitor discharge and recharge modulated by a dynamically coupled resistance, or memristance. However, these are not fully integrated on a single substrate and have relied on large discrete passive components for significant parts of their circuitry.

Manuscript approved November 21, 2023.

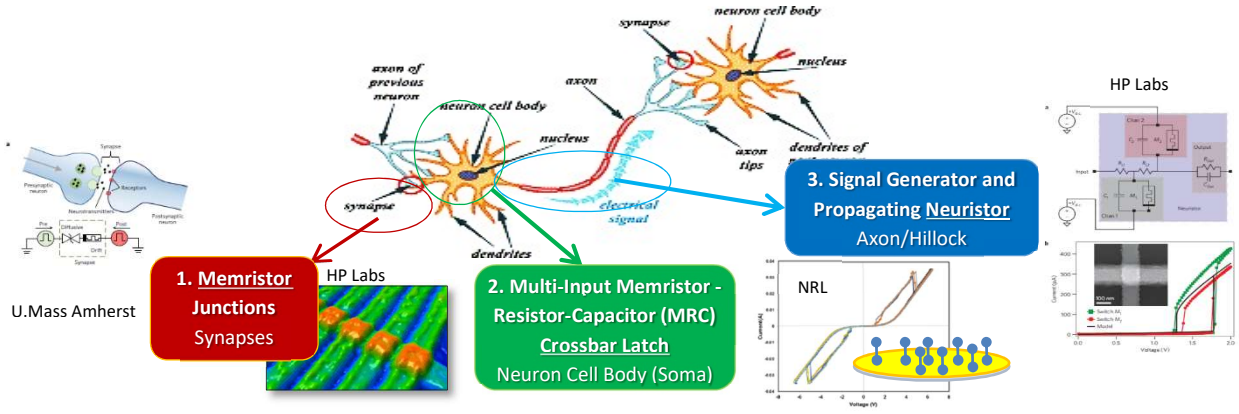


Fig. 1 — Neuromorphic devices and their biological equivalents.

1.2 Technical Goals

The central focus of this research program is the realization of a memristor-based neuron equivalent, along with its supporting device elements corresponding to synapses and the axon hillock, as depicted in Fig. 2. The ultimate goal is a unit cell demonstration of a device that forms the basis of devices that, fully realized, possess sufficient state storage and logic processing capability to process complex information contained in incoming spikes and convert it into a decision to generate a sequence of spikes that in turn encodes and transmits information. To this end, materials growth, device design and fabrication, and circuit modeling was performed, in order to obtain optimal oxide switching materials, non-volatile and volatile memristive devices, and spike-generating circuits, respectively.

2. APPROACH

2.1 Materials Growth and characterization

The basic materials system investigated was transition metal oxides (TMOs) deposited by atomic layer deposition (ALD). A critical advantage of ALD is its compatibility with semiconductor industry fabrication processes and with high-aspect-ratio device structures which are expected to become more common and important to future integrated electronic circuits. In this effort, materials, circuits, and their components were developed in parallel, with circuit results iteratively feeding back into the design and processing of the device components. Memristor devices were fabricated as single devices, coupled devices on a common bottom electrode, crossbar arrays, or complex combinations of these using both nonvolatile oxide films such as HfO_2, and volatile oxide films such as NbOx or VO_2. The optimization of memristor devices and materials progressed as needed throughout the duration of the program with input from the results of the ongoing program, “Electronic Transport and Switching in Oxides: An Alternative to FET Technology” (Work Unit 1C24). Memristive oxide materials developed in that program were screened and modified for optimal memristor switching characteristics such as threshold voltage, state retention, and dynamic switching kinetics.

2.2 Electrical device design, fabrication. and testing

Electrical testing of the various types of devices using 2-terminal DC and pulsed I-V measurements was conducted to determine basic switching modes and behaviors of TMO memristors. Similar electrical testing was applied to multiple terminals of memristor devices on a common electrode to characterize correlated switching behaviors between paired and larger aggregates of devices. The electrical

characteristics of various memristor devices were identified and screened to determine their suitability as specific components for neuronal circuits, such as synapses or firing gates.

Device electrical performance was measured and evaluated in terms of critical NVM performance parameters, including ON and OFF resistances, ON/OFF ratio, switching energy, electroforming energy, switching time, and maximum number of switching cycles. Electrical results were correlated to material properties, with a particular focus on TMO composition, crystal structure, and interfaces, in order to identify film and interface properties leading to optimal performance.

The electrical behavior of the Nb_2O_5 and NbO_2 memristors was evaluated using a Keithley 4200-SCS semiconductor parameter analyzer. Prior to measurement of a device, a high voltage bias sweep (typically above 10 volts) is applied through probes between two of the top electrodes repeatedly to electroform them, reducing the initial resistance of the NbOx films within those device areas to metallic levels. The probe connected to ground is left in contact with one of the top electrodes, while the other probe is moved to the top electrode of the device of interest, and a voltage sweep is applied.

2.3 System modeling and simulation

Electrical and physical modeling of the circuit elements were implemented as the elements are characterized physically and electrically. Basic spiking behavior was modeled with circuit element parameters derived from measured parameter values of memristor devices in combination with various passive and parasitic elements under pulsed and steady state DC input biasing conditions. Neuristors and latch devices are envisioned as the spiking element and logic integrator, respectively, within a future complex neuromorphic integrated unit.

3. EXPERIMENTS AND RESULTS

3.1 Materials Development

The materials deposition process development and characterization of resistive switching thin film transition metal oxides (TMOs) was continued from that conducted under Work Unit 1C24, as described in the final report submitted for that program and briefly recounted here.

3.1.1 Demonstration of non-volatile HfOx memristor films

Non-volatile hafnium oxide (HfO_2) memristor films were deposited by thermal atomic layer deposition (ALD) in an Oxford Flexal ALD chamber, located in NRL's Nano Science Institute (NSI) cleanroom facility. The hafnium precursor was tetrakis (ethylmethylamino)hafnium (TEMAH), and the oxidation occurred at temperatures of 200 – 300°C by reaction with water vapor. Modified versions of the ALD process, described more in detail in the next subsection, were performed on a Beneq TFS 200 ALD chamber using hydrogen plasma generated by a capacitively coupled plasma (CCP) generator.

The chemical composition of the grown films was determined by x-ray photo-spectroscopy (XPS), and the thickness determined by spectroscopic ellipsometry. An optimal thickness for switching of 5-13 nm was determined for fully oxidized HfO2 deposited by the Oxford ALD system.

3.1.2 Demonstration of Mott transition in NbOx films of tunable stoichiometry

The process development included modified atomic layer deposition (ALD) processes for fine in-operando stoichiometry control over TMO films and post-deposition processing of the films such as thermal annealing and plasma exposure for microstructure and composition evolution studies. Physical

characterization including x-ray diffractometry (XRD), secondary ion mass spectrometry, and cross sectional TEM was conducted on the films, as well as electrical I-V transport measurements on devices fabricated onto these films.

Atomic layer deposition (ALD) processes for thermal Nb_2O_5 and hydrogen plasma-reduced NbO_2 were developed using the Beneq TFS200 ALD reactor. NbO_2 is deposited by insertion of additional H_2 plasma steps into the conventional thermal ALD process, reducing the Nb5+ to Nb4+ and thus tuning the metal to oxygen ratios of the resulting NbOx films. The impact of plasma gas chemistry (Ar/H_2 ratios), plasma step duration, and the ratio of plasma step incorporation have been investigated in order to develop saturative conditions for deposition of amorphous ALD NbO_2. Additionally, the morphological and electronic properties of these mixed Nb_2O_5 -NbO_2 glasses have been studied as to their suitability for memristor devices. The hydrogen plasma modified ALD process resulted in tuning of the composition, ranging from fully stoichiometric Nb_2O_5 to reduced NbO_2. Tuning of the bandgap commensurate with the relative oxygen deficiency was also observed. The results of this section are reported in references [10] and [12].

As detailed in reference [10], the hydrogen plasma reduction process was implemented by varying the duration of hydrogen plasma exposure, the number of plasma steps per ALD cycle, and the hydrogen/argon ratio of the plasma. Each of these methods successfully resulted in reduced oxygen content relative to metal content in the deposited films, and could be utilized individually or in combination to achieve the desired NbO_2 stoichiometry. Physical characterization of these films is detailed in the following section.

3.1.3. Physical Characterization of Nb_2O_5 vs. NbO_2.

To more fully characterize the range of NbO_x films attainable using the in operando hydrogen plasma technique, we compared the optical and electronic properties of our most Nb-poor (deposited by conventional thermal process with no plasma exposure) and most Nb-rich (deposited using a single plasma step, with a 15% hydrogen plasma gas, and a 5 s plasma exposure time) NbO_x ALD thin films.

Figures 5(a) and 5(b) show measured XPS spectra of the Nb 3d core shell region for the Nb-poor and Nb-rich NbO_x thin films, respectively. In Figure 2(a), the single pair of peaks for the $3d_{1/2}$ and $3d_{3/2}$ doublet are attributable to Nb^{5+} and indicate that the Nb-poor film is nearly phase-pure Nb_2O_5. In Figure 2(b), however, the Nb-rich film has a second doublet, shifted lower in BE, which is attributed to Nb^{4+}. Notably, there is no evidence of any further reduced Nb (Nb^{2+}, Nb^0), suggesting that the Nb-rich film includes both Nb_2O_5 and NbO_2 phases, but no metallic Nb. As the optical properties of the Nb-rich films match well those reported for NbO_2, we believe the ALD films deposited with in operando hydrogen plasma exposures are nearly-fully reduced to NbO_2, with the Nb^{5+} detected via XPS derived from a surface oxide layer, as shown in Figure 2(c). NbO_2 is known to readily oxidize, with a thin Nb_2O_5 native oxide layer forming upon air exposure. Given the sampling depth of the Al Kα x-rays, the estimated surface composition of the Nb-rich sample, ~60% Nb^{5+} and 40% Nb^{4+}, is consistent with a ~2.5 nm Nb_2O_5 native oxide layer on the NbO_2 film. For the remainder of this report, the Nb-poor films will be referred to as "Nb_2O_5" and the Nb-rich films will be referred to as "NbO_2."

The direct bandgap of the Nb_2O_5 and NbO_2 films were extracted from the absorption measurements shown in the Tauc plot of Figure 3(a), and yields estimated energy gaps of 3.5 eV and 1.2 eV for Nb_2O_5 and NbO_2, respectively, in good agreement with literature reports for each material. The difference in optical properties is readily apparent from visual observation of 64 nm films grown on Al_2O_3 substrates, as shown in the photograph of Figure 3(b), where the wide band gap Nb_2O_5 is optically transparent and the narrower gap NbO_2 film is absorptive at visual wavelengths.

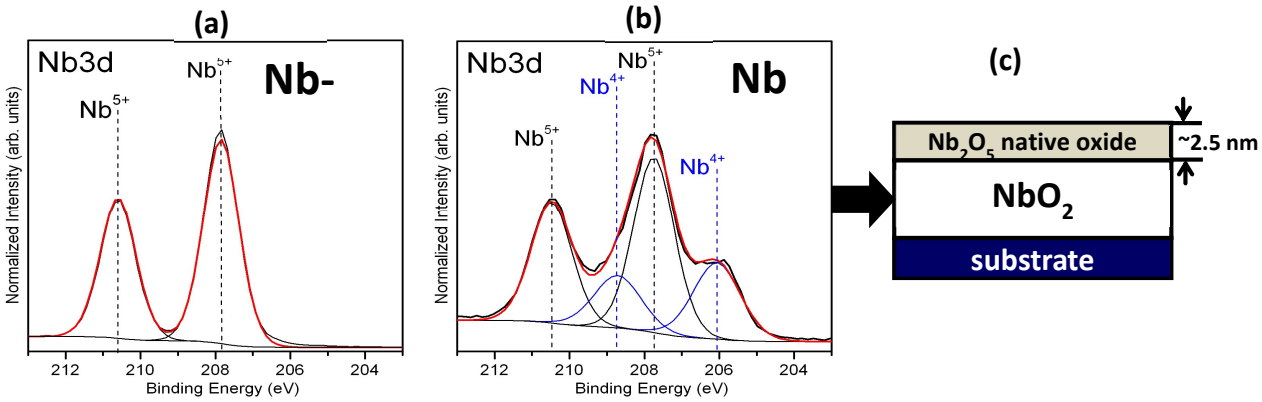


Fig. 2 — XPS spectra from (a) Nb-poor (Nb_2O_5) and (b) Nb-rich (NbO_2) films grown by ALD – showing peaks attributed to the presence of Nb^{5+} as well as peaks attributed to Nb^{4+}. (b) Schematic diagrams of cross section of NbO_2 film, showing hypothetical Nb_2O_5 native oxide formed on the surface of the reduced film upon exposure to air.

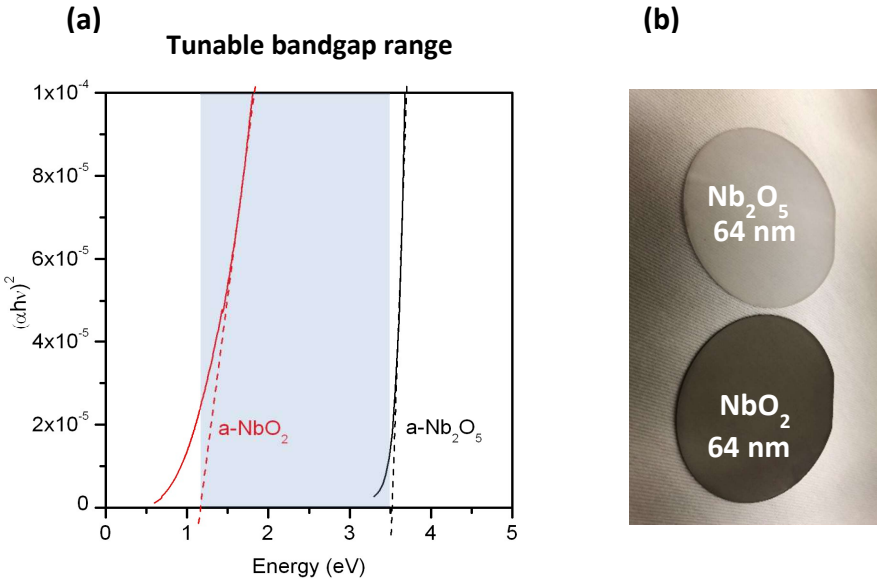


Fig. 3 — (a) Tauc plot of as-deposited a-NbO_2 and a-Nb_2O_5, with shaded intermediate area representing range of tunable bandgap attainable by intermediate process conditions. (b) True-color photograph of substrates deposited with Nb_2O_5 and NbO_2, showing the distinct optical properties of the two films.

Preliminary photoluminescence was performed at 2K on 65 nm-thick crystalline Nb_2O_5 and NbO_2 films grown in the NRL Beneq ALD reactor on c-plane sapphire substrates and then annealed in Ar gas and H_2/N_2 forming gas, respectively. PL was also obtained from the parent c-plane Al_2O_3 substrates. In particular, a very broad emission band with peak energy at ~ 2.5 eV was observed from the nearly transparent c- Nb_2O_5 film. In contrast, only very weak emission (likely from the parent c-plane sapphire substrate) was found in this spectral range from the nearly opaque c-NbO_2 film.

3.2 Device Stack Development

3.2.1. Memristor device design and fabrication

Memristive devices were fabricated from Nb_2O_5 films deposited using the conventional thermal ALD process (i.e., no plasma exposure) and from NbO_2 films deposited using a single 5 s, 15% hydrogen plasma step per ALD supercycle. Electrical test substrates used are of the type described elsewhere [10], and were constructed by a contract fab as follows: A dielectric SiO_2 film was deposited onto a film of tungsten (W), which functions as a common electrode layer. Vii of various diameters were patterned and etched into the SiO_2 film and titanium nitride (TiN) was embedded in the vii to contact the W layer. Nb_2O_5 and NbO_2 films of ~116 nm (as measured by ellipsometry) were deposited by ALD onto these substrates, and top electrodes consisting of Ti and platinum (Pt) were deposited by e-beam evaporation onto the vii. The memristor device therefore consists of the top electrode (25 nm Pt on 5 nm Ti), the NbOx films (117 nm), and the TiN via. The TiN vii connect to the W layer, which acts as a common electrode.

3.2.2. Memristor device characterization

Non-volatile Memristor Devices HfO_2 devices were fabricated by depositing HfO_2 films by ALD onto a continuous thin film layer of Pt/Ti or TiN (the bottom electrode), then selectively depositing a layer of Ti then a layer of Pt in a disc pattern of 50 microns by a lift-off process (the top electrode) onto the oxide film. The HfO_2 film is etched away in a selected location to expose the bottom electrode for probing contact. The resulting devices are equivalent to metal-insulator-metal (MIM - Pt/Ti/**HfO_2**/TiN or Pt/Ti/**HfO_2**/Pt/Ti) capacitor structures. The DC electrical response of the devices was measured using a 2-terminal continuous voltage sweep probing method. The current-voltage (I-V) plots over 20 voltage sweep cycles are shown in Figure 4, for individual devices measuring (a) 150 microns and (b) 300 microns in diameter respectively. Electrical behavior was consistent with bipolar memristive switching, with SET and RESET voltages averaging -1.3V and 1.2V, respectively, over 20 cycles, and a low bias resistance ratio (R_{OFF}/R_{ON}) greater than 10^3 observed for each device.

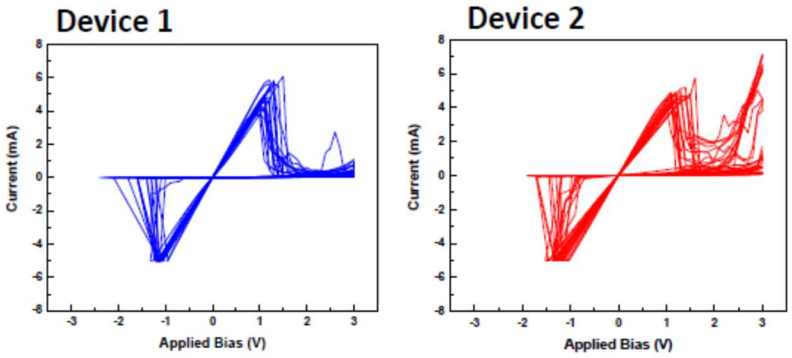


Fig. 4 — I-V characteristics of two typical HfO_2 memristor devices under DC sweep, 50 cycles.

Volatile Memristor Devices The devices fabricated from as-deposited NbO_2 (Fig. 5(d)) were initially 13.5 times more conductive than those fabricated from the standard as-deposited Nb_2O_5 (Fig. 5(a)), as measured at low bias conditions. To activate memristive behavior, devices were subjected to an initial voltage sweep, in which bias across device was increased from 0 V until a dramatic current increase was observed, typically termed "electroforming." During electroforming, joule-heating of the NbO_x film causes local crystallization of the film to NbO_2, which exhibits an intrinsic IMT at ~800°C. To prevent complete device breakdown, maximum current through the device was limited to below a preset level,

500 uA for the Nb_2O_5 (Fig. 5(b)) and 2.5 mA for the NbO_2 (5(e)) during the electroforming step. Electroforming occurred at above 8V for the Nb_2O_5 devices, but at significantly lower bias levels - about 2.5V – for the NbO_2 devices. After electroforming, devices fabricated in both material systems exhibited volatile memristive behavior, with the device switching into a low resistance state at higher current/voltage levels, etc. as shown in Figs. 5(c), 5(f). Notably, switching voltage was considerably less for NbO_2 film.

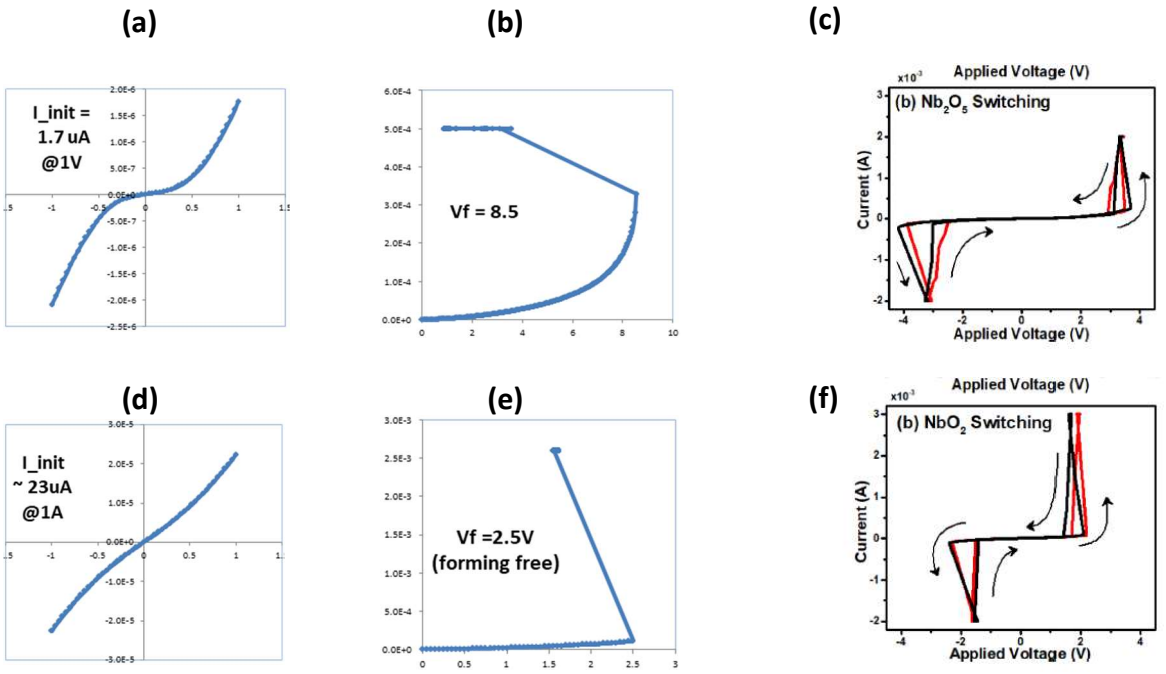


Fig. 5 Electrical characterization data from memristor devices fabricated using Nb_2O_5 (a-c) and NbO_2 (d-f). Initial I-V curves at low bias sweep (up to 1V) shows lower resistance in NbO_2 (d) than in the Nb_2O_5 (a) device. The electro-forming step shows a lower forming threshold for NbO_2 (e) than in the Nb_2O_5 (b) device. Finally, the threshold switching is observed to occur at a lower voltage for NbO_2 (f) than in Nb_2O_5 (c).

A summary of the results of electrical characterization are provided in Table 1, and the full details are reported in reference [10].

Table 1 — Switching characteristics of memristor devices using Nb_2O_5 and NbO_2

	Initial resistance	Forming voltage (Vf)	Switching threshold (Vth)
Nb_2O_5	588 kOhms	8.5V	3.5 – 4.2 V
NbO_2	43.5 kOhms	2.5V (forming free)	1.5 – 2.5 V

Finally, we have demonstrated a coupled memristor latch consisting of two anti-parallel HfO_2 memristors fabricated onto a common bottom electrode. The individual memristors are identical to those shown in Figure 4 earlier in this section. Figure 6 shows the current-voltage response over 3 cycles of the combined CRS device formed by contacting the top electrodes of the two individually electroformed and cycled devices and driving them in series through the bottom electrode. As the sweep voltage increases from the origin up to the switching SET voltage of one of the individual devices, the measured current remains at a negligible level, after which it rises exponentially then enters a linear regime at about 3.1V, at which point the current has risen to about 7 mA. When the bias is increased beyond 5V then decreased,

a switching event occurs at 5V in which the current abruptly increases from 21 to 32 mA, then subsequently decreases linearly. This linear regime is offset in the voltage axis from a line through the origin by about 1.1V, which is near the SET voltage of a single device, after which the current follows the path of the negligible current level observed at the beginning of the sweep. In the negative voltage sweep, the current follows the negative equivalent of the above switching, with negligible currents at low voltage and an abrupt switching event to a more conductive state occurring at around -5V. The voltage and current values cited in this analysis vary slightly from sweep to sweep, within 1V and 5 mA, respectively.

The current-voltage characteristics measured across two electrodes located 50 microns apart (edge to edge) are equivalent to the complementary resistive switching reported through a single crossbar junction comprised of a material stack roughly symmetrical in the vertical direction. As with the single crossbar version of the device, the CRS behavior is due to the voltage divider effect in which the current flows mostly across the lower resistance device. Any pair of bipolar memristors fabricated onto a common bottom electrode and measured through the top electrodes so that the devices are anti-serial is topologically equivalent to a single CRS device formed by a stack of anti-serial memristors separated by an intermediate electrode. To distinguish the two manifestations of CRS, CRS formed by paired discrete devices demonstrated in this work may be designated as “delocalized CRS”, or D-CRS. The apparent differences in the I-V curve slope with those from the previously reported CRS devices are the result of the different dimensions of the respective devices such as the electrode area and the thickness and width of the common electrode. It can be expected that reducing the size of the separate memristor junctions and narrowing the common electrode to a wire configuration will reduce the overall current level and bring the results more into agreement with single junction CRS devices.

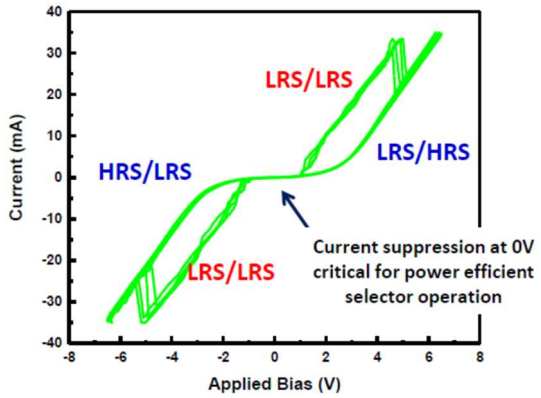


Fig. 6 Electrical characterization data from back-to-back HfO_2 memristor devices, exhibiting suppressed current at low bias and latching behavior above a threshold bias in either polarity.

As can be seen from the distinct regimes visible in the CRS curve of Figure 6, multiple discrete conductive states can be encoded in the CRS by the resistive state of the two constituent memristor junctions – that is, LRS-HRS, HRS-LRS, LRS-LRS, and HRS-HRS. These have been referred to as, in order, 0, 1, ON and OFF [13]. In addition to their utility for reducing sneak-path currents in cross-bar arrays, it has been noted that the threshold-like I-V behavior and implicit state register mechanisms of CRS devices enable the representation and memory of logic states and logic operations upon those states. Bistable crossbar latches [13] have been previously reported as having switching characteristics capable of generating a complete family of logic operations. Extending the concept to a multi-terminal configuration, and incorporating volatile as well as non-volatile memristor devices, we expect to develop devices capable not only of realizing externally readable logic functions, but also of integrating those

functions into a complex programmable spiking mechanism, thereby fulfilling the role of the neuron in the neuronal circuit.

4. MODELING

4.1 Neuron equivalent circuit design

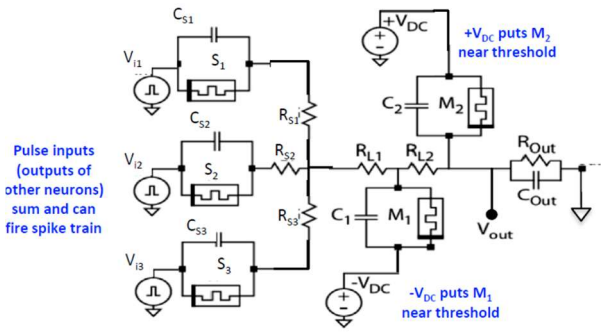
Circuits were designed according to the neuristor reported in reference [7], which is configured with an input and output, with opposing bridges consisting of volatile memristors and their respective parallel capacitors. In addition to the spiking apparatus shown in the reference, our circuits were designed with nonvolatile memristors to perform the function of "synapses", or variable resistance devices which modulate input signals by a "weight" or analog value. A voltage pulse traversing one such synapse would effect a current through the said synapse that is in proportion to the voltage multiplied by the resistance of the memristor device, according to Ohm's Law of resistance. The current pulses thus generated at each of the synapses are combined, or integrated, according to Kirchhoff's current law at the point of converging branches – the input of the spiking neuron. The modulated and integrated currents enter the spiking circuit, and if they build up sufficient charge at the parallel capacitors to exceed the threshold voltages of the volatile memristor devices, will trigger a Mott transition in one or both of them, discharging the capacitors such that a spike is emitted at the output. The circuit thus obtained is known in the literature as a leaky integrate-and-fire (LIF) neuron.

These circuits were designed according to parameters obtained from NbO_2 devices described in the above section and from reasonable extrapolations of values found in the literature for dielectric constants and resistances of NbO_2, TiN, HfO_2, and Pt films that would be utilized in its construction.

4.2 Neuron equivalent circuit simulation

Matlab simulations were performed on the neuristor equivalent circuit design shown in Figure 7(a). Varying the parameters in the model such as series resistance and parallel capacitance, the output characteristics of the neuristor circuit were measured as a function of time. Under an optimal set of parameters, the circuit exhibited voltage spiking when the input voltage exceeded a threshold of 1.5V. The spiking characteristics were shown to be temporally correlated to the resistance state of the two volatile memristor components in the circuit.

The time evolution of the two volatile memristors (RM1 and RM2) and the concurrent voltage spikes generated by the neuristor are shown in Figure 7(b). The output spiking is very sensitive to the values of the memristor resistances and the passive elements such as capacitance and series resistance, as shown with varying capacitances in Figure 8.



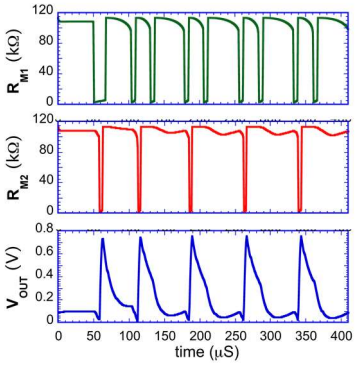


Fig. 7 – (a) Neuristor equivalent circuit diagram. (b) Time evolution plots of the resistance R1 of volatile memristor M1, resistance R2 of volatile memristor M2, and output voltage of neuristor.

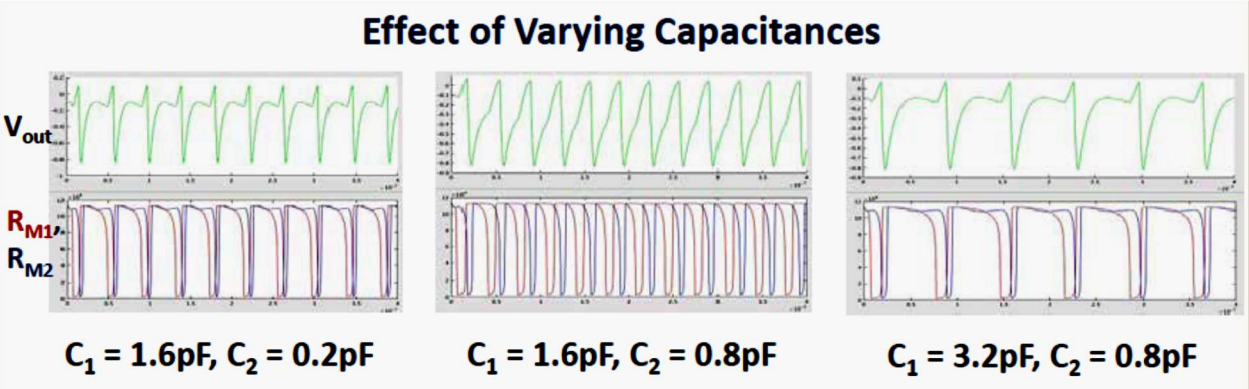


Fig. 8 – Time evolution plots of output voltage and memristor resistances at various capacitance values for the capacitors C1 and C2 respectively parallel to M1 and M2.

Spiking responses can also be triggered by electrical spikes entering the circuit from the input nodes. Furthermore, we have demonstrated in simulation that the output spiking is affected by the pattern of input spikes. For example, as shown in Figure 8(a), the neuristor circuit emits a spike in response to two input spikes within a given time interval (in this case 45 nsec). However, when the interval between the incoming spikes exceeds a certain delay time, the neuristor does not generate a subsequent output spike for the same input spike stimulus. This is a key attribute of leaky integrate and fire (LIF) spiking neurons, that is replicated in a simple memristor-based passive circuit. The effect of this device is that of a coincidence detector, by which the temporal proximity of two incoming spikes may be determined by the output spiking behavior.

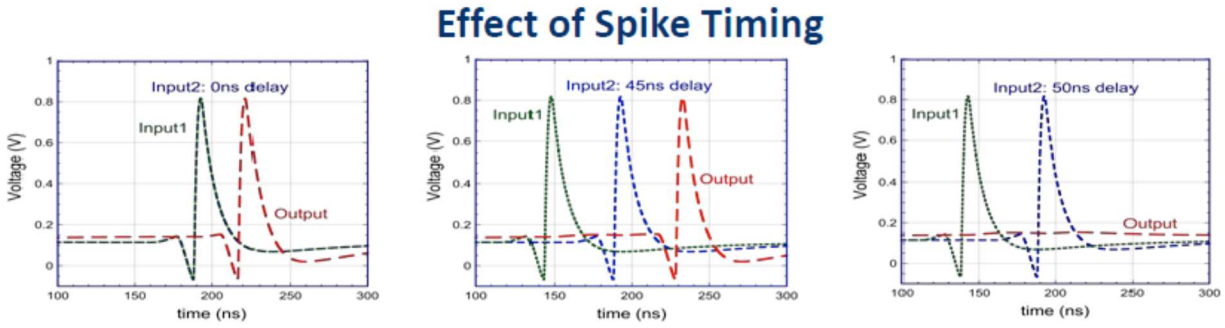


Fig. 9 Output spiking of neuristor as a result of two input spikes (a) with zero delay (b) with 45 nsec delay, and (c) with 50 nsec delay. The output spiking does not occur when the interval exceeds 45 nsec.

Conclusions

Memristor-based device elements for neuron circuits have been designed and fabricated using atomic layer deposition (ALD)-grown transition metal oxides (TMOs). Circuits that emulate neuron spiking were also

designed using these elements, and simulated using realistic physical parameters. Various spiking behavior was replicated in the simulations.

Physical realization of the circuits as designed and simulated, with all the components incorporated, could not be achieved due to unexpected constraints in our device processing capabilities and prolonged downtime of both the Beneq ALD and Oxford ALD tools, which limited the materials processing throughput needed to fabricate the component films in the devices. These issues were compounded by the frequent turnover in personnel, including two NRL scientists, a post-doc, and a contractor, during the course of the program.

Work Unit 6B53 has served as the basis from which multiple subsequent research program proposals in neuromorphic computing technology have been launched. Among those, the NeuroPipe ARAP program was successfully initiated in FY'21 under the funding of the Office of the Under-Secretary of Defense (OUSD) for Research and Engineering, and is engaged in developing neuromorphic devices and transferring the technology to the semiconductor fab environment, including efforts to realize a physical manifestation of the neuristor-based LIF circuit using oxide memristors.

REFERENCES

1. J.J. Burrow (DASN) and M. Winter (CNR), Department of the Navy Research, Development, Test, and Evaluation - 30 Year Research and Development Plan, Jan. 2017
2. D. Strukov et al, "The Missing Memristor Found", *Nature* Vol. 423, 80 (2008)
3. Z. Wang, J.J. Yang et al, "Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing", *Nature Materials* Vol. 16, 2017
4. M. Hu et al., "Memristor crossbar-based neuromorphic computing system: A case study," *IEEE TNNLS*, vol. 25, no. 10, pp. 1864–1878, 2014
5. D. Mountain et al, "Ohmic Weave: Memristor-Based Threshold Gate Networks", *IEEE Computer*, vol 48, no. 12 (2015)
6. M. Prezioso, et al, "RRAM-Based Hardware Implementations of Artificial Neural Networks: Progress Update and Challenges Ahead", *Proceedings of the SPIE,* vol. 9749, 974918 (2016)
7. M. Pickett et al, "A scalable neuristor built with Mott memristors", *Nature Materials* Vol 12, 2013
8. M. Ignatov, et al, "A memristive spiking neuron with firing rate coding", *Front. Neurosci.*, Vol. 9, 376 (2015)
9. G.A. Gibson, S. Musunuru, J. Zhang, K. Vandenberghe, J. Lee, C-C Hsieh, W. Jackson, Y. Jeon, D. Henze, Z. Li, and R.S. Williams, "An accurate locally active memristor model for S-type negative differential resistance in NbOx", *Applied Physics Letters* **108**, 023505 (2016)
10. Alexander C. Kozen, Zachary R. Robinson, Evan Glaser, Mark Twigg, Thomas J. Larrabee, Hans Cho, S. M. Prokes, Laura Ruppalt, "Composition Tuning of Atomic Layer Deposited Niobium Oxide Using In-Operando Hydrogen Plasma Exposure for Neuromorphic Computing", *ACS Chemistry of Materials*, 2019
11. Alexander C. Kozen, Thomas J. Larrabee, Mark E. Twigg, Hans S. Cho, Sharka M. Prokes, "Atomic Layer Deposition of NbOx Films with Tunable Stoichiometry Using Hydrogen Plasma Reduction", Invited Talk presented at ALD/ALE International Symposium, Incheon, South Korea, NRL/ON/6870-18-0051, July 2018
12. M. E. Twigg, A. C. Kozen, L. B. Ruppalt, S. M. Prokes, and H. S. Cho, "Transmission electron microscopy analysis of reduction reactions and phase transformations in Nb_2O_5 films deposited by atomic layer deposition", *J. Appl. Phys.* **129**, 025304 (2021).
13. P. Kuekes et al, "The Crossbar Latch: Logic value storage, restoration, and inversion in crossbar circuits", *Jour. App. Phys.* v97, 034301 (2005)

Recognition

In addition to the formal program participants, Thomas J. Larrabee, Alexander C. Kozen, and Timothy Walter, who were involved in ALD oxide growth as post-doctoral researchers, and Mark E. Twigg and Todd Brintlinger, who performed TEM analysis under other work units, contributed significantly to this work.

Contracts

This work was funded by the Office of Naval Research under NRL Base Programs 68-1C24 and 68-6B53.