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SYNCHRO-DATA QUANTIZER AND DIGITAL SERVO

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INTRODUCTION

Because of the close coordination required for the exercise of integrated command in modern warfare, there is need for a dependable method of transmitting shaft-position data by means of narrow-band communication facilities. Such equipment could be used for ship-to-ship or ship-to-air transmission of angle and range information from radar and sonar installations. As a part of its program in this field, the Bureau of Ships (Code 832) established a project at the Naval Research Laboratory in May 1949 to investigate the application of digital techniques to the data-transmission problem.

The immediate objective of the NRL project was to develope a Quantizer and Digital Servo for demonstrating a feasible approach to a digital data-transmission system. The Quantizer was to transform the shaft position of a synchro generator to a pulse-coded voltage. The Digital Servo was to accept this voltage and position a shaft to correspond with the synchro-generator rotor position. No radio link was used since it was known that transmission of the coded information could readily be handled by a standard Navy commumication facility. A model of the Quantizer and Digital Servo was set up to demonstrate one-speed transmission of shaft rotation at the Symposium on Electronic Systems Integration* held at the Naval Research Laboratory on 22 March 1950.

SYNCHRO–DATA QUANTIZER

The Quantizer for a single channel of one-speed synchro data is shown in Figure 1. The inputs to the Quantizer are the synchro-excitation voltage and the voltages on the three synchro-stator leads. To explain the operation of the Quantizer, it will be assumed that all of these voltages are sine waves having a fixed frequency (60 cps, for example). The excitation voltage serves as the reference signal for the system and may be drawn as a function of time (Figure 2, line A). The three stator voltages of the synchro are all of the same phase but vary in amplitude depending on the position of the synchro rotor. These voltages can be combined in a network to give a constant-amplitude sinusoidal voltage, the phase of which is directly equivalent to the shaft position of the synchro. The output of such a network (called the "Phase-Shift Network" in Figure 1) is illustrated on line B of Figure 2 for a phase lag of 30°, corresponding to a 30° rotor position for the synchro. The reference voltage is amplified and clipped to give a square-wave output from Squaring Circuit No. 2. This square wave is converted by Differentiator No. 2 to a series of positive and negative pulses occurring whenever the rate of change of voltage is a maximum (line C of Figure 2). The phase-shifted voltage is treated similarly in Squaring Circuit No. 1 and Differentiator No. 1 as shown on line D.

The phase difference between the two sinusoidal voltages is now represented by the time difference between two positive pulses. The negative pulses are eliminated since they are not used. This time difference can be readily quantized through the use of a clock-pulse generator, a Binary Counter, and

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* *NRL letter report 3950-24/50, Ser 7609, 22 March 1950, "Symposium on Electronic Systems Integration."*

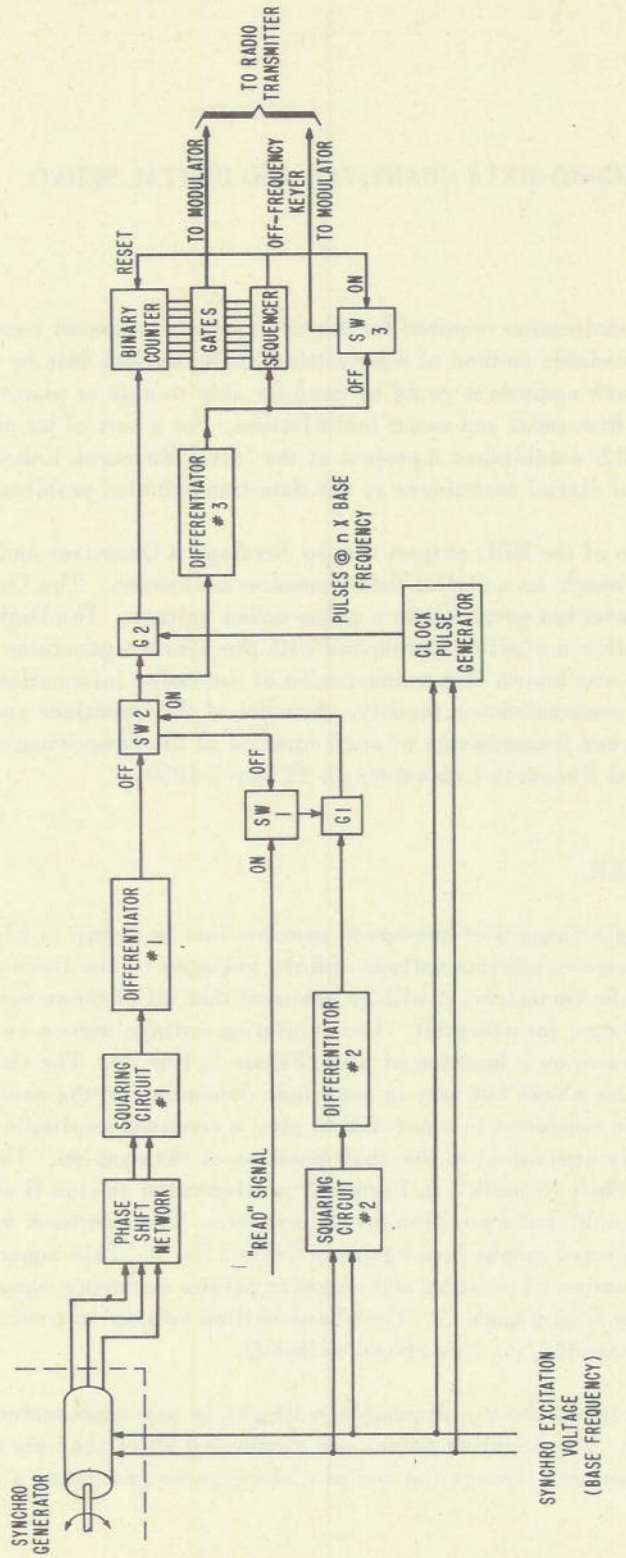

Figure 1 - Quantizer block diagram

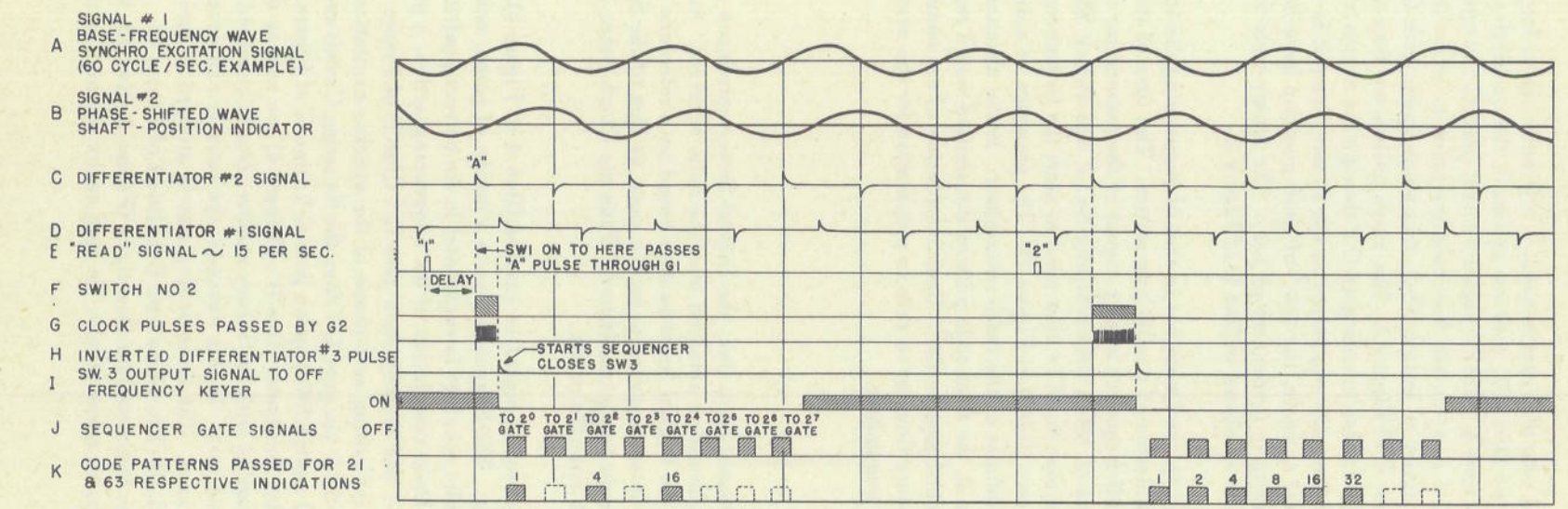

Figure 2 - Quantizer wave forms

appropriate gating circuits. If a reading rate of 15 per second, a reference signal frequency of 60 cps, and a clock-pulse frequency of 15,360 cps (256 x 60 cps) are assumed, the quantizing process is shown in lines E through K of Figure 2. Each time a "Read" signal occurs, gate G-1 is opened by the action of electronic switch SW-1. After gate G-1 is open, the first positive pulse to arrive from Differentiator No. 2 is allowed to pass. Through the action of switch SW-2, this pulse opens gate G-2 and closes gate G-1. This action is indicated on line E of Figure 2. The clock pulses are then allowed to operate the Binary Counter until the phase-shifted pulse closes gate G-2 through the action of switch SW-2 (line F and G of Figure 2). The number of pulses now registered in the Binary Counter is a measure of the synchro-shaft position. In this particular example, the 360° of shaft position have been divided into 256 divisions, thus giving a digital reading in increments of 1.4°. The binary code for approximately a 30° shaft position ($21 \times 1.4^{\circ}$) would be as shown in line K of Figure 2.

The problem remaining to be solved by the Quantizer is that of sequencing the information in the Binary Counter to allow pulse-code modulation of a radio transmitter. The time of the shaft-position reading is transmitted by stopping the off-frequency keying signal of the transmitter through the action of the phase-shifted pulse by way of switch SW-2, Differentiator No. 3, and switch SW-3 (lines H and I of Figure 2). The signal from Differentiator No. 3 is also used to start the Sequencer, which operates each of the eight binary-digit gates in turn (line J of Figure 2). The presence of a digit in the Binary Counter is indicated by pulsing the modulator of the radio transmitter. In the absence of a binary digit, no pulsing occurs. On line K of Figure 2, the first code pattern transmitted would represent a shaft position of $21 \times 1.4^{\circ} = 30^{\circ}$ and the second pattern 88°. Upon completion of the sequencing action, a pulse from the Sequencer resets the Binary Counter to zero in preparation for the next reading and turns on the off-frequency keyer of the radio transmitter.

DIGITAL SERVO

At the receiving end of the data-transmission link, the Digital Servo reproduces the synchro-shaft position on the basis of pulse-coded information obtained from the radio receiver. As shown in the block diagram (Figure 3), operation of the Digital Servo is also based on a reference sinusoidal voltage. Although the frequency of this voltage is not required to be the same as that of the Synchro-Data Quantizer, they are the same (60 cps) for the example being considered. Thus the Clock-Pulse Generator frequency for this example must be 15,360 cps (256 x 60).

When the transmitted off-frequency keying signal is stopped (line A of Figure 4), a pulse is sent from the radio receiver to the Sequencer. The Sequencer opens a series of gates, one at a time, so that each binary-digit pulse from the radio receiver is registered in its correct position in the Counter-Register (lines B and C of Figure 4). Upon completion of the sequencing action, a pulse is initiated by the Sequencer to operate switch SW-1 and thereby open gate G-1 (line D of Figure 4). Gate G-1 remains open until the positive pulse, indicating zero phase of the synchro-excitation voltage, has been transmitted to switches SW-1 and SW-2 via gate G-1 from the Squaring Circuit and Differentiator. Then switch SW-1 closes gate G-1, and switch SW-2 opens gate G-2 (line G of Figure 4). While gate G-2 is open, pulses from the Clock-Pulse Generator (line H of Figure 4) are sent to the Counter-Register, which accumulates pulses starting with the binary number already received from the Synchro-Data Quantizer, rather than from zero. In this example, the counter can accumulate pulses up to a total of 256 before returning to zero. The Counter-Register is stopped at zero by transmitting a zero pulse, which acts through switch SW-2 to close gate G-2 (line I of Figure 4). For the two cases of transmitting 21 and 63 from the Synchro-Data Quantizer (Figure 2, line K), the Counter-Register operates 234 times and 193 times, respectively. In both cases the total accumulation is 256.

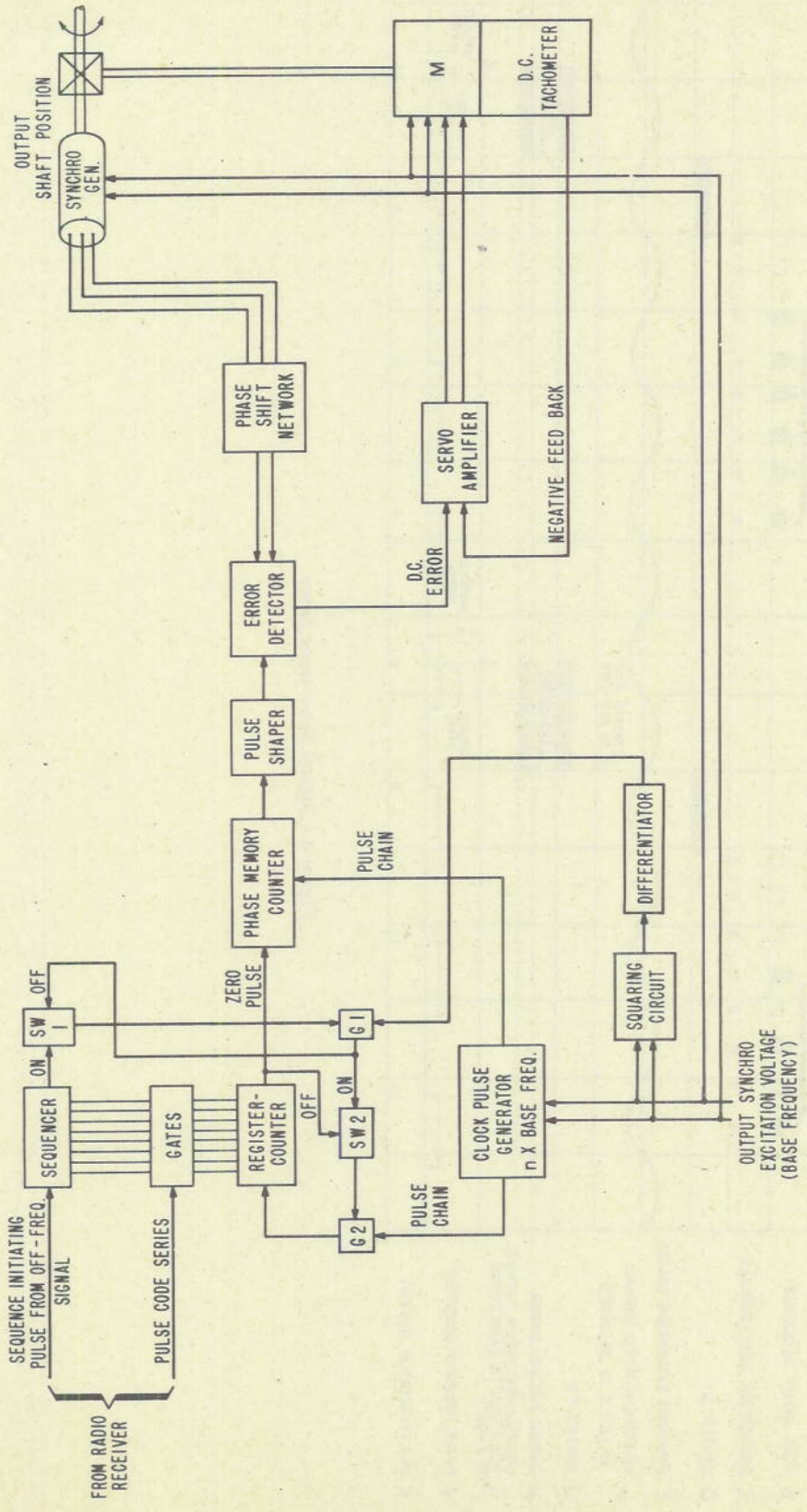

Figure 3 - Digital Servo block diagram

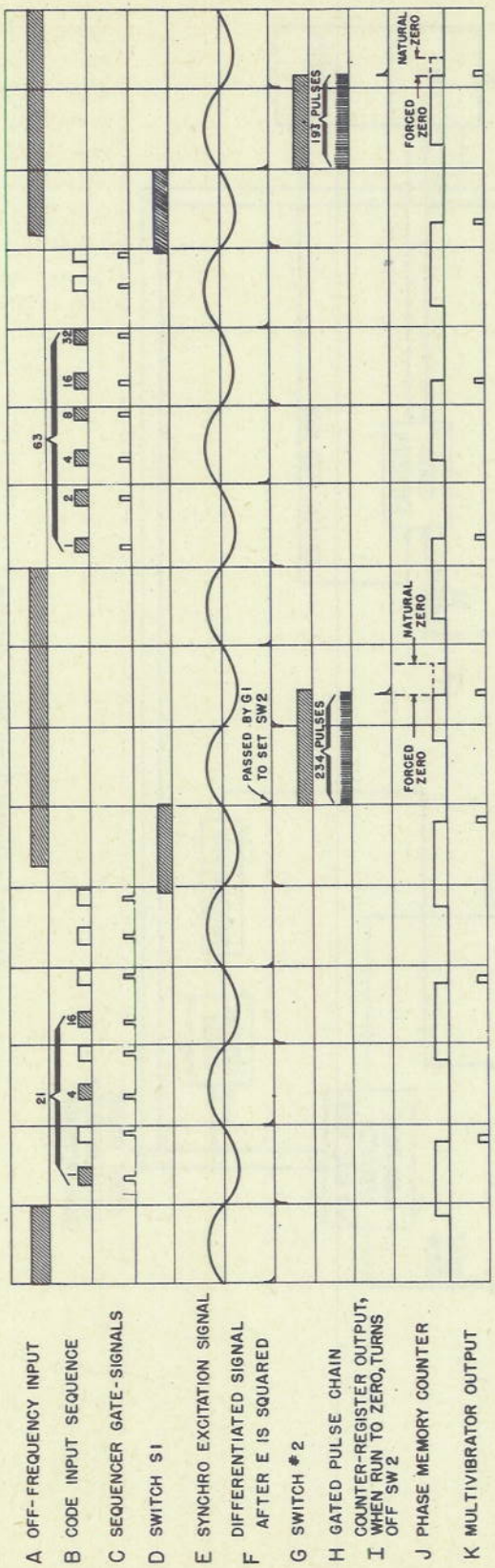

Figure 4 - Digital Servo wave forms

To produce a suitable phase-shifted alternating voltage, the Phase-Memory Counter and Pulse Shaper are used (Figure 3). In the present example, the Phase-Memory Counter is an eight-stage Binary Counter which is continuously cycled through a count of 256 by the output of the Clock-Pulse Generator. The zero-indication pulse from the Counter-Register forces the Phase-Memory Counter to zero as shown in line J of Figure 4. A zero-indication pulse generated by the Phase-Memory Counter is used to synchronize a multivibrator, the output of which is shown on line K of Figure 4. The square wave from the multivibrator is used as a reference in the Error Detector (Figure 3) for determining phase-position error indicated by the output-position device. It should be noted that the angle represented by the phase-memory voltage waveform varies in a sense opposite to that of the angle measured by the Synchro Data Quantizer. Thus to obtain the proper sense of output shaft rotation, the S1 and S3 leads to the synchro generator in the Digital Servo must be reversed.

DEMONSTRATION MODEL

The demonstration model of the Synchro-Data Quantizer and Digital Servo is illustrated in Figure 5. As shown in the block diagram for this equipment (Figure 6), not only have the radio link and sequential transmission of the pulse codes been eliminated, but several of the circuits have been connected to serve two purposes. This model is operated from a single source of 115-volt 60-cycle power, and only

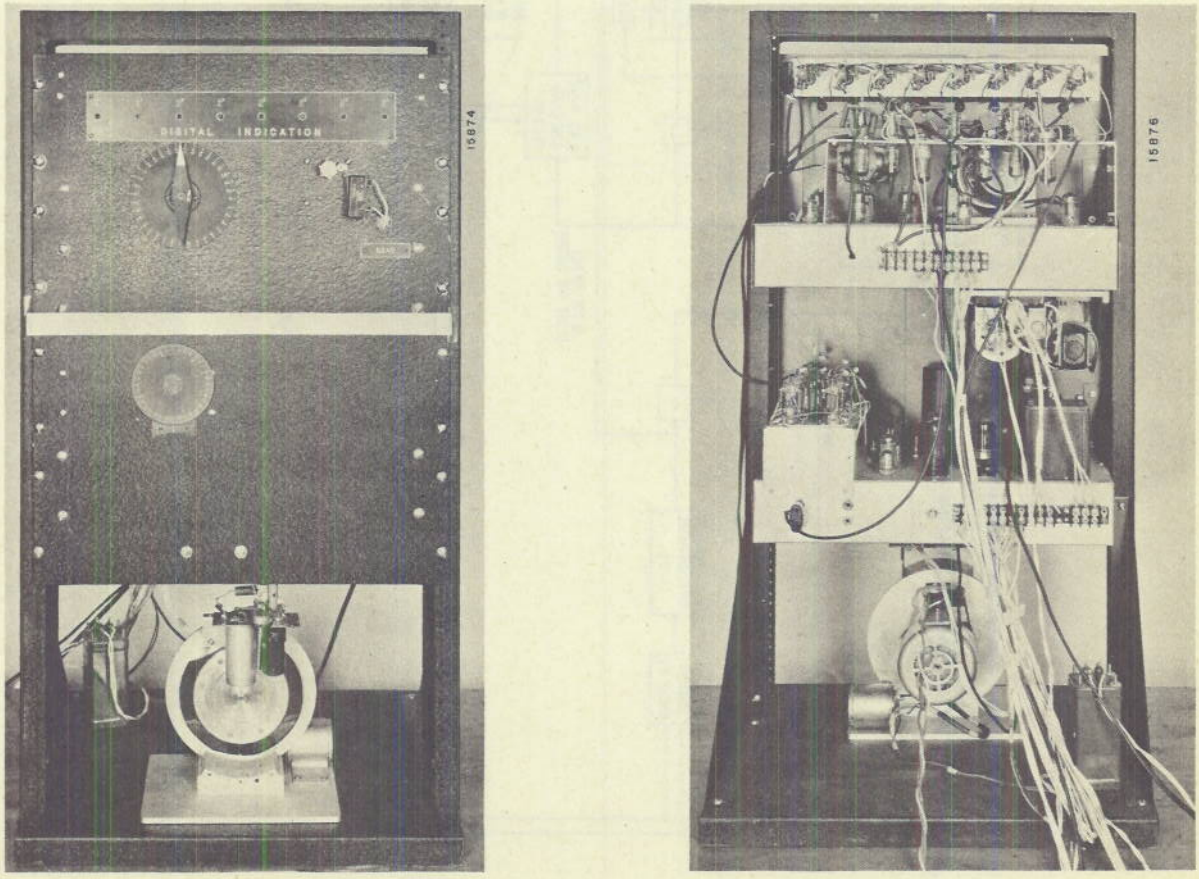

Figure 5 - Demonstration model of the Synchro-Data Quantizer and Digital Servo

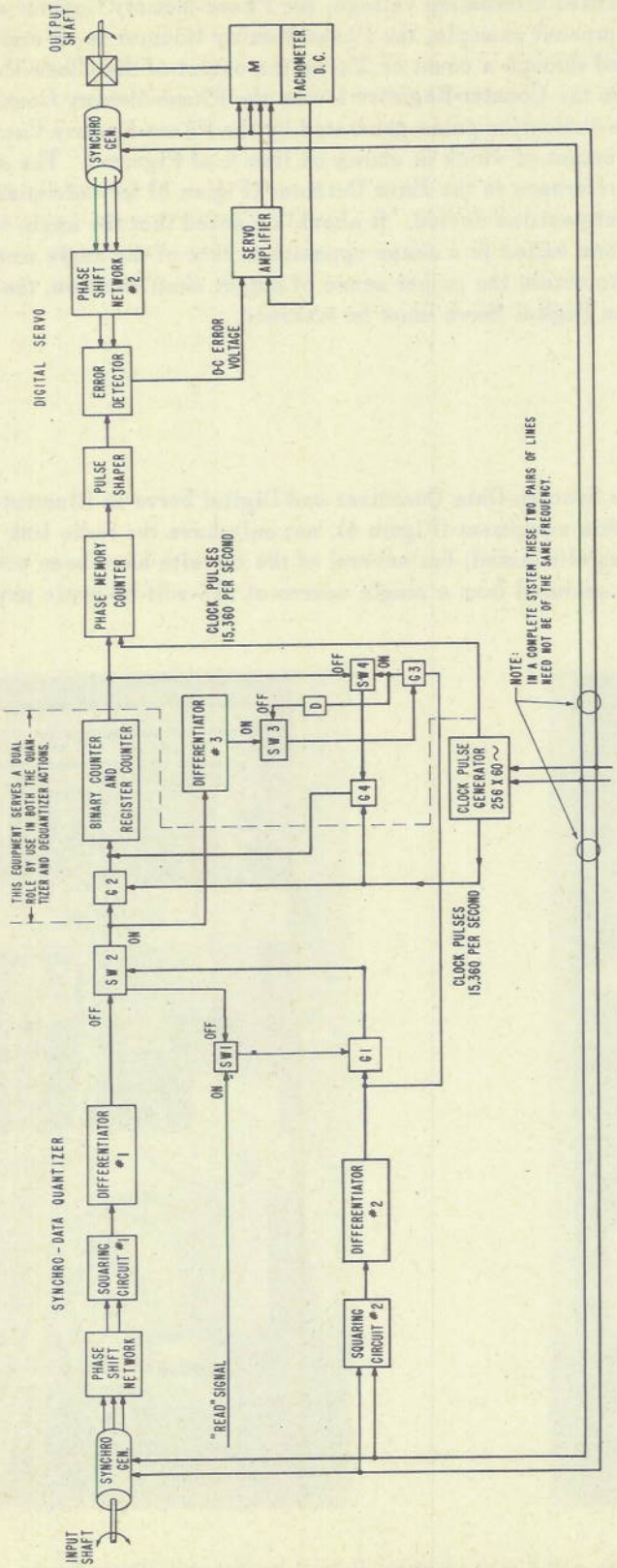

Figure 6 - Demonstration model block diagram

one Clock-Pulse Generator is used. The Binary Counter of the Synchro-Data Quantizer and the Counter-Register of the Digital Servo are the same counter. The "Read" signal is derived from a motor-driven cam operating a microswitch to produce pulses at the rate of 10 per second. The input and output shaft rotations have been divided into 256 parts, the same value as that used in the previous discussion of the more general system.

As ordered by a "Read" signal, the quantizer portion of the demonstration model (Figure 6) stores the synchro-shaft-position information in the Binary Counter in the manner previously described. The pulse from Differentiator No. 1 serves two purposes: (a) it completes the action of the Quantizer by closing gate G-2 (by way of closing switch SW-2), and (b) it opens gate G-3 (by way of switch SW-2, Differentiator No. 3, and switch SW-3) to allow the servo portion of the demonstration model to operate. The next zero-phase pulse from Differentiator No. 2 then passes through gate G-3 and opens gate G-4 through the "on" action of switch SW-4. After a short delay, gate G-3 is closed by way of switch SW-3. The Clock-Pulse Generator then transmits pulses through gate G-4 to the Counter-Register until the counter responds with a zero-indicating pulse to close gate G-4 by way of switch SW-4. At this point in the sequence, the Quantizer is ready for the next "Read" signal. The remainder of the operation of the servo portion of the demonstration model is the same as discussed for the Digital Servo.

The detailed circuit diagrams for the demonstration model are given in Figure 7 for the Quantizer and in Figure 8 for the Digital Servo. Figure 7A and 8A are functional diagrams to indicate which parts of the circuit serve the functions originally discussed (Figure 6).

As shown in Figures 7 and 7A, the input to the Quantizer is provided from the three synchro leads (S_1, S_2, and S_3), each carrying a 60-cycle sine-wave voltage identical in phase, but differing in amplitude as determined by the synchro-generator rotor position. Two sine-wave signals from the five-terminal network are applied to the grids of the cathode followers V1A and V1B. The voltage difference between these two input signals is obtained across the primary of the transformer T1, which is connected between the cathodes of V1A and V1B. From the secondary of T1, a constant-amplitude 60-cycle sine wave is obtained, shifted in phase an amount proportional to the synchro-rotor angular position. The wave is squared in a trigger circuit composed of the pentodes V2 and V3. The negative pulse obtained by differentiating this square wave is transmitted to flip-flop V10 (switch SW-2).

The "Read" signal is generated by the closing and opening of a microswitch, which causes flip-flop V4 to be set and reset. Lowering of the plate voltage of V4B generates a negative pulse that triggers flip-flop V5 so that the plate voltage of V5A becomes high. This, in turn, raises and maintains a high grid voltage on gate tube V7 (gate G-1 open). The first positive pulse of the reference signal occuring subsequent to the "Read" signal is transmitted from Differentiator No. 2 through gate tube V7. The leading edge of the negative pulse from the plate of V7 is used to set flip-flop V10 (switch SW-2), and the trailing edge of this pulse is used to close gate G-1 (V7 cut off) by action through a buffer tube (V6), and thus reset flip-flop V5 (switch SW-1). When flip-flop switch SW-2 (V10) is set by the signal from V7, the plate voltage of V10B raises the voltage on the first grid of gate tube V11 (gate G-2 open). Then pulses from the Clock-Pulse Generator can pass through V11, be amplified by V18, and accumulate in the 8-stage Binary Counter. Tube V11 is cut off (gate G-2 closed) by a positive pulse derived from the phase-shifted wave and applied to reset flip-flop V10. Then the binary number stored in the Binary Counter represents the shaft position of the synchro-generator, and the action of the Quantizer is completed until it is ordered to read again.

The operation of the digital-servo portion of the demonstration model will be explained by referring to Figures 7, 8, and 8A. In Figure 8A, the major components of the Digital Servo have been drawn in block form, and the functions have been indicated as previously described in connection with Figure 6.

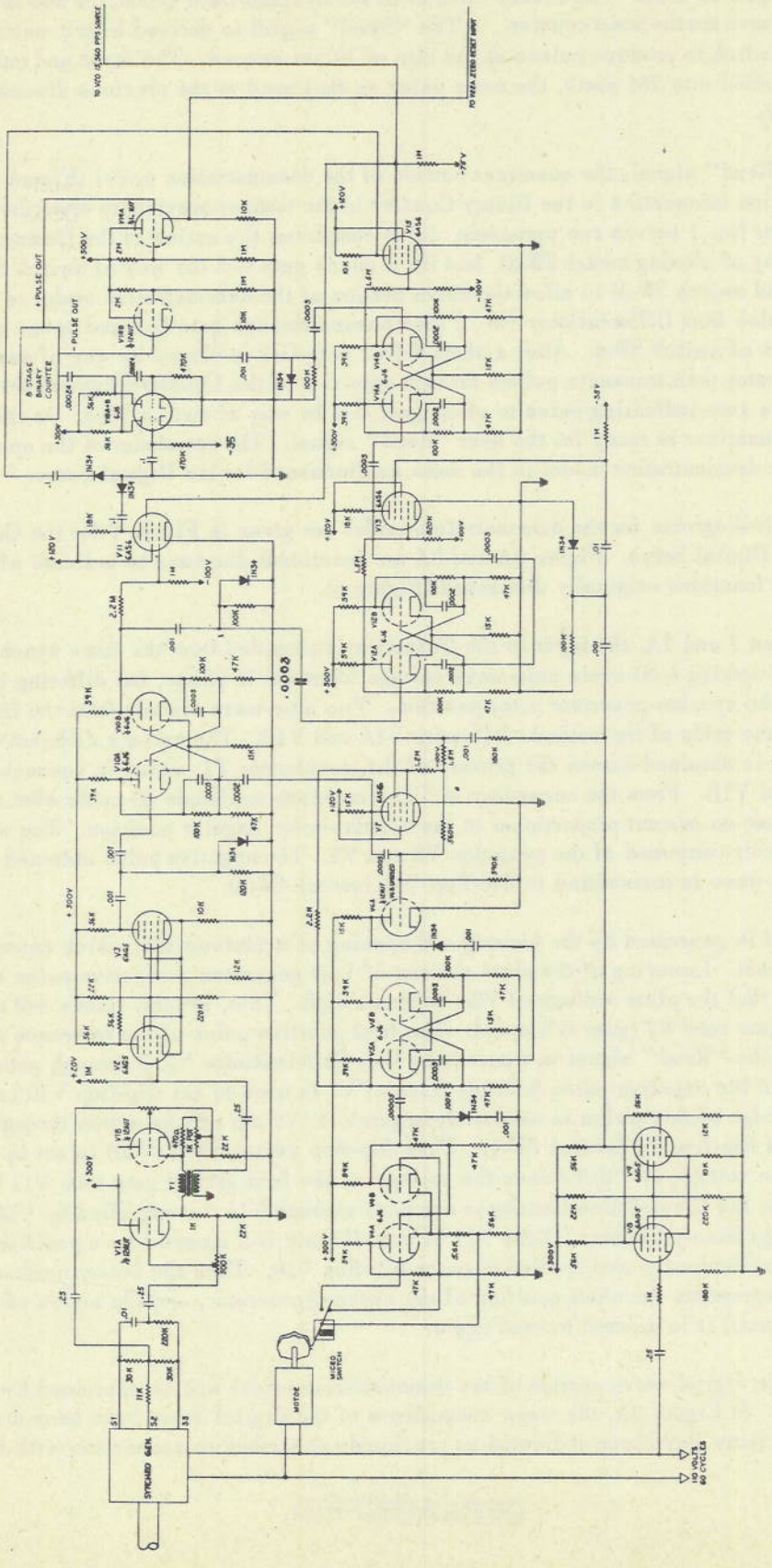

Figure 7 - Demonstration model Quantizer - schematic diagram

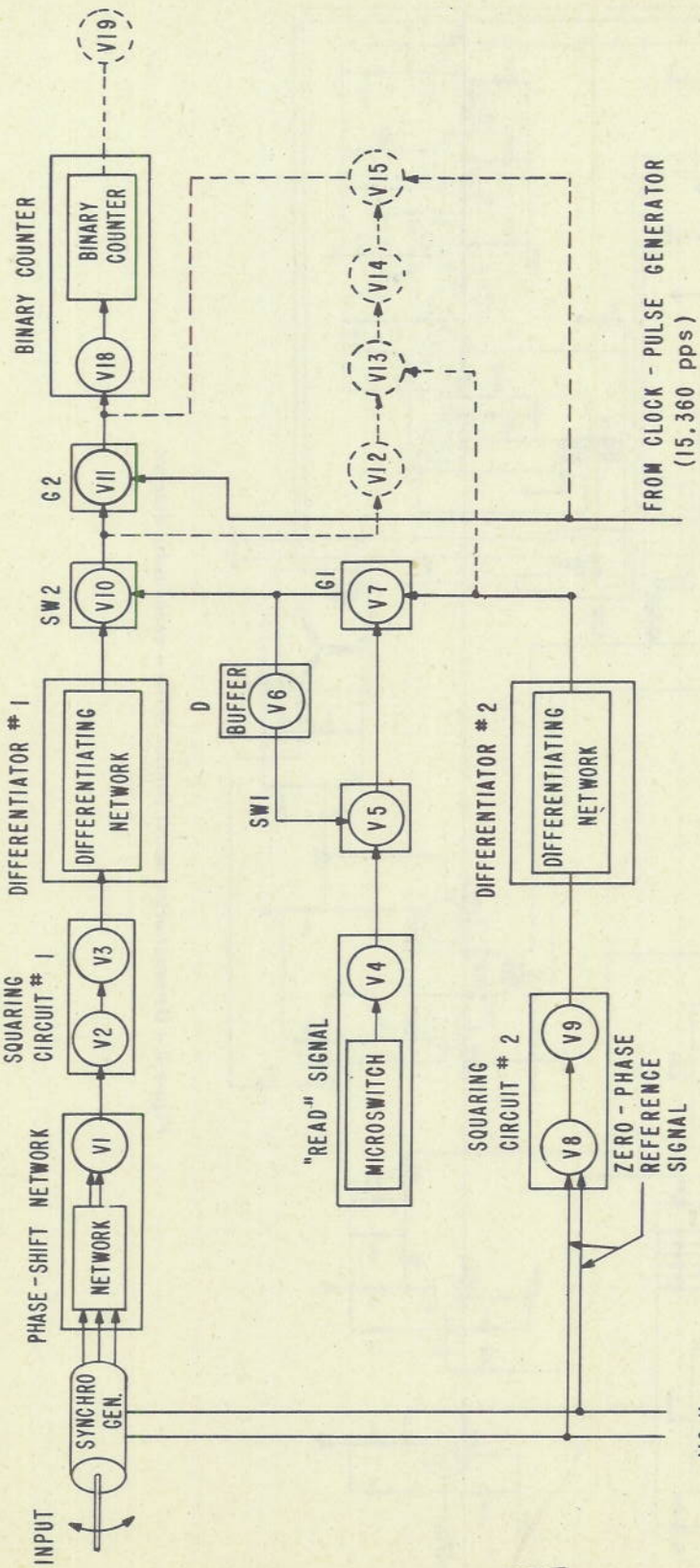

Figure 7A - Demonstration model Quantizer - functional diagram

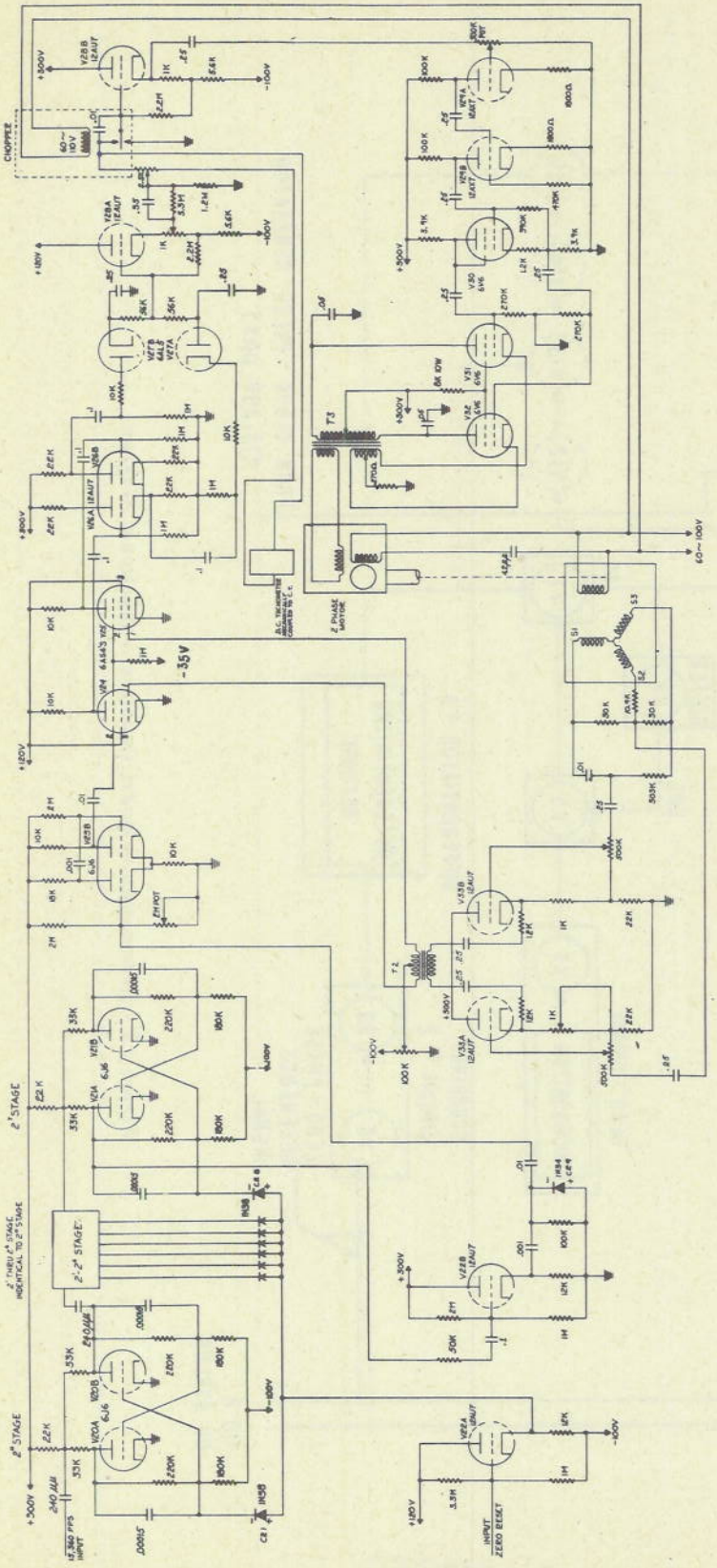

Figure 8 – Demonstration model Digital Servo – sechematic diagram

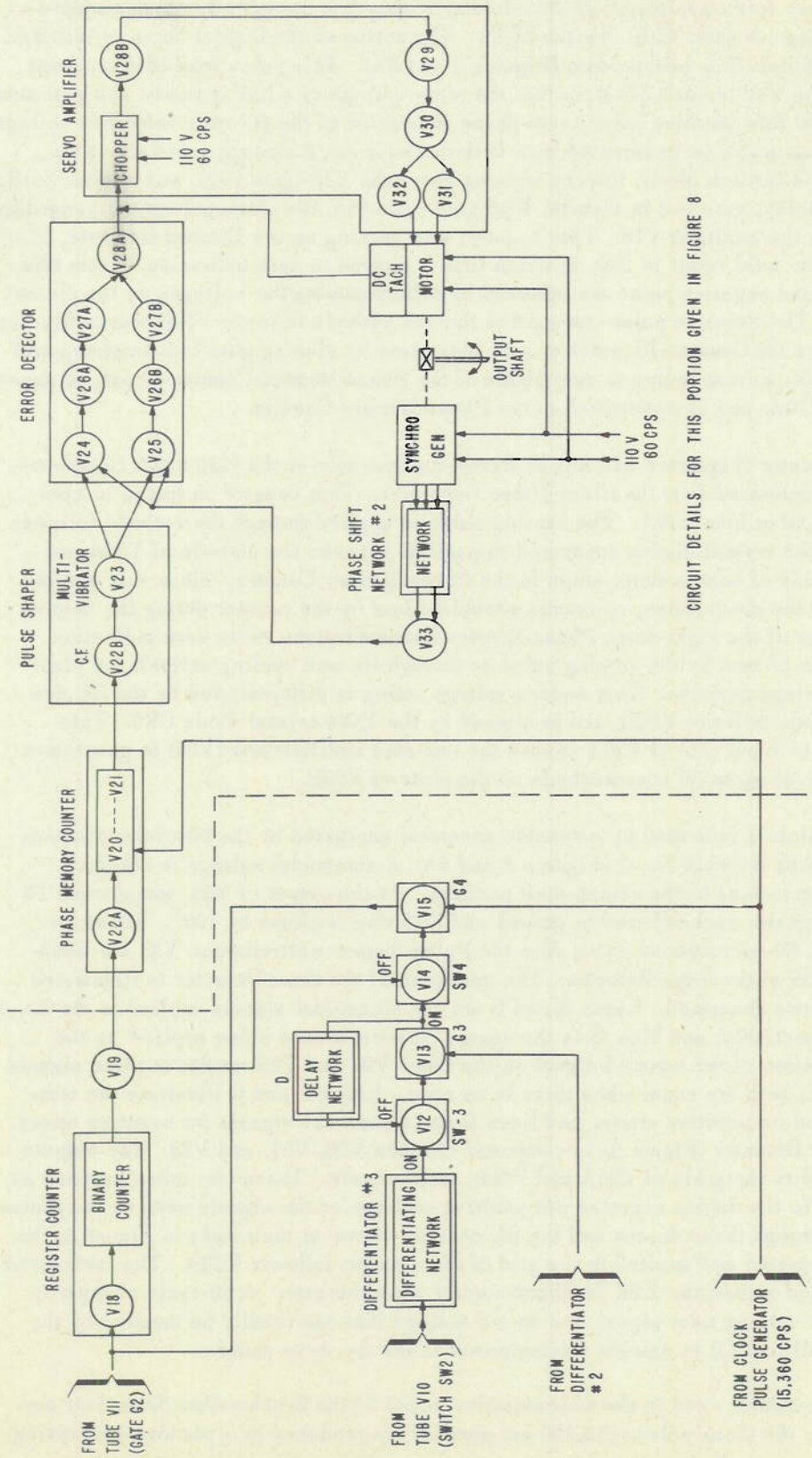

Figure 8A - Demonstration model Digital Servo - functional diagram

The quantizing sequence was completed with the closing of gate G-2 (tube V11), which resulted from the lowered plate voltage on tube V10B (switch SW-2). The action of the Digital Servo is initiated by a negative pulse derived from this voltage drop (Figures 7 and 8A). This pulse from Differentiator No. 3 is used to set flip-flop V12 (switch SW-3) so that the plate voltage of V12A is raised and gate tube V13 (gate G-3) opened. The first positive pulse (zero-phase indication of the 60-cycle reference voltage) subsequent to the quantizing action is transmitted from Differentiator No. 2 through gate G-3. This pulse then sets flip-flop V14 (switch SW-4), thereby opening gate tube V15 (gate G-4), and resets flip-flop V12 so that, after a short delay, gate G-3 is closed. With gate G-4 open, the clock pulses are passed to the Binary Counter through the amplifier V18. This counter, now serving as the Counter-Register, accumulates pulses until the total count is 256, at which time it returns to zero indication. From this zeroing action, a positive and negative pulse are obtained by differentiating the voltages on the plates of the last counter stage. The negative pulse transmitted through cathode follower V19B resets flip-flop V14 (switch SW-4) and stops the Counter-Register at zero indication by closing gate G-4 (lowering grid of V15). The positive pulse, corresponding to zero phase of the Phase-Memory-Counter output, is passed through cathode follower V19A and is transmitted to the Phase-Memory Counter.

The Phase-Memory Counter (Figures 8 and 8A) is driven continuously at the (256 x 60) 15,360-per-second rate by the pulses delivered from the Clock-Pulse Generator. This counter is forced to zero indication by the positive pulse from V19A. The zeroing pulse is applied through the cathode follower V22A and thence to the 1N38 crystal diodes connected in parallel between the cathode of V22A and the respective left-hand grids of each counter stage in the Phase-Memory Counter. Since this zeroing pulse is short compared to the clock pulse, no counts should be lost by the counter during the zeroing action. When the last stage of the eight-stage Phase-Memory Counter returns to its zero indication (either through being driven to zero by the zeroing pulse or through its own cycling action), the plate voltage of V21A rapidly swings positive. This sudden voltage swing is differentiated by the RC network on the output of cathode follower V22B, and is clipped by the 1N34 crystal diode CR9. This positive pulse applied to the input grid of V23A causes the one-shot multivibrator (V23) to generate a short positive square pulse of about 50 microseconds on the plate of V23B.

The output-shaft position is indicated by a synchro generator energized by the 60-cycle reference voltage. Through Phase-Shift Network No. 2 (Figures 8 and 8A), a sinusoidal voltage is obtained, phase-shifted an amount equivalent to the output-shaft position. At the output of V33, transformer T2 provides two sinusoidal signals, each referred to ground and differing in phase by 180°. These two sinusoidal signals and the 50-microsecond pulse from the Pulse-Shaper multivibrator V23 are transmitted to tubes V24 and V25 of the Error Detector. The operation of the Error Detector is illustrated in Figure 9 by the wave forms generated. Lines A and B are the sinusoidal signals applied to the No. 1 grids of V24 and V25, respectively; and line C is the square 50-microsecond pulse applied to the No. 2 grids. The gating action of the squared signal on the tubes V24 and V25 results in plate signals as shown on lines D and E; both are equal when there is no error. Lines F and G illustrate the combination of signals obtained for positive errors, and lines H and I show the signals for negative errors. The remainder of the Error Detector (Figure 8) is composed of tubes V26, V27, and V28. The outputs of V24 and V25 are applied to the grids of V26A and V26B, respectively. These two tubes function as phase inverters and apply to the diodes negative and positive replicas of the signals seen on the plates of tubes V25 and V24. Through these diodes and the RC network shown at their right in Figure 8, the impressed signals are integrated and applied to the grid of the cathode follower V28A. The tachometer negative-feedback is applied across the 2.5K feedback-control potentiometer. A 60-cycle chopper is used to convert the slowly varying error signal into an a-c voltage that can readily be handled by the servo amplifier (tubes V28B to V32) to provide driving power to the a-c drive motor.

Since the reference frequency used in the demonstration model of the Synchro-Data Quantizer and Digital Servo is 60 cycles, the clock pulses (15,360 per second) are produced by a photocell receiving

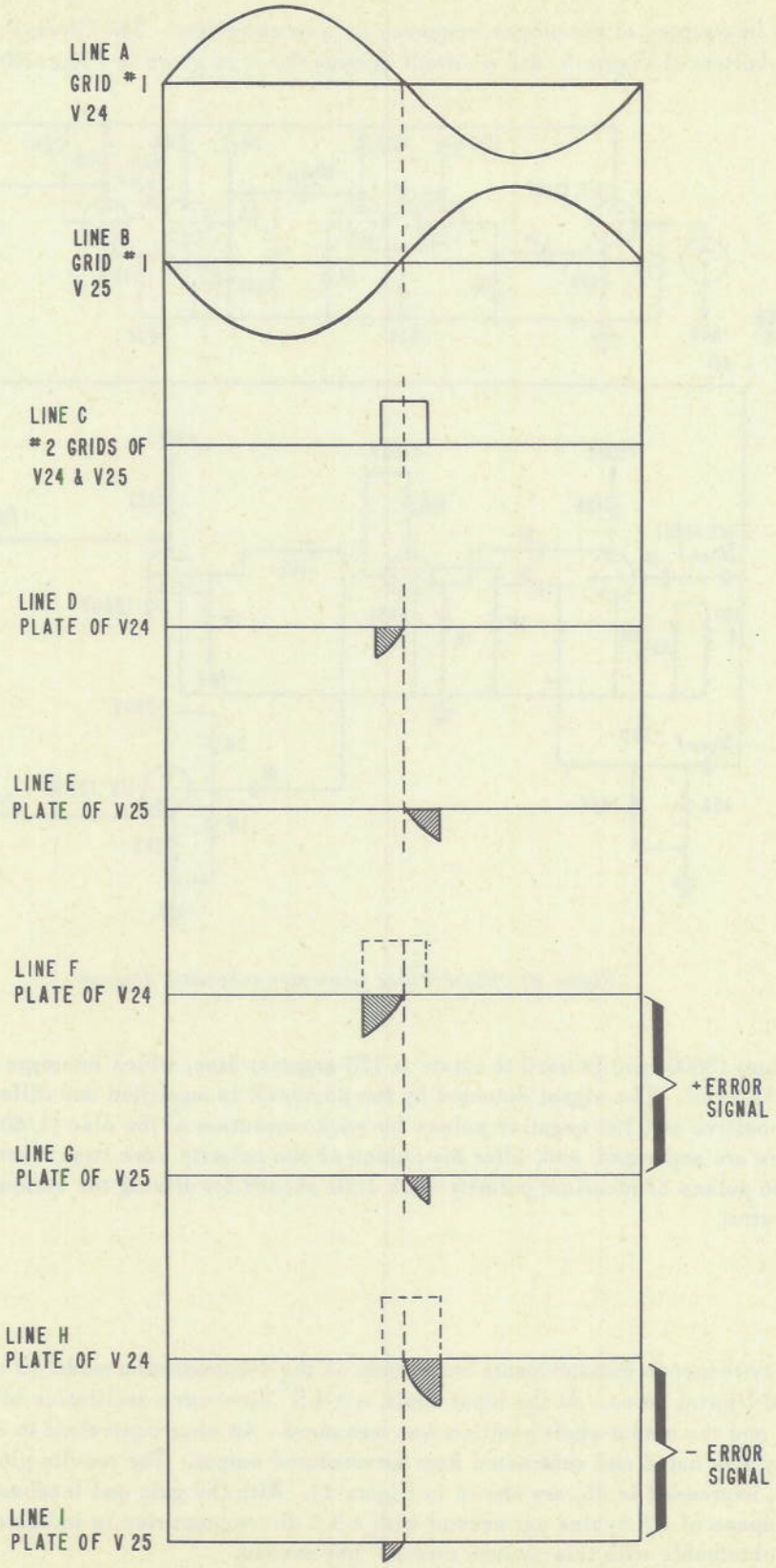

Figure 9 - Servo Error Detector wave forms

light which is interrupted at the proper frequency by a rotating disc. The Clock-Pulse Generator is visible at the bottom of Figure 5, and a circuit diagram for it is given in Figure 10. A synchronous

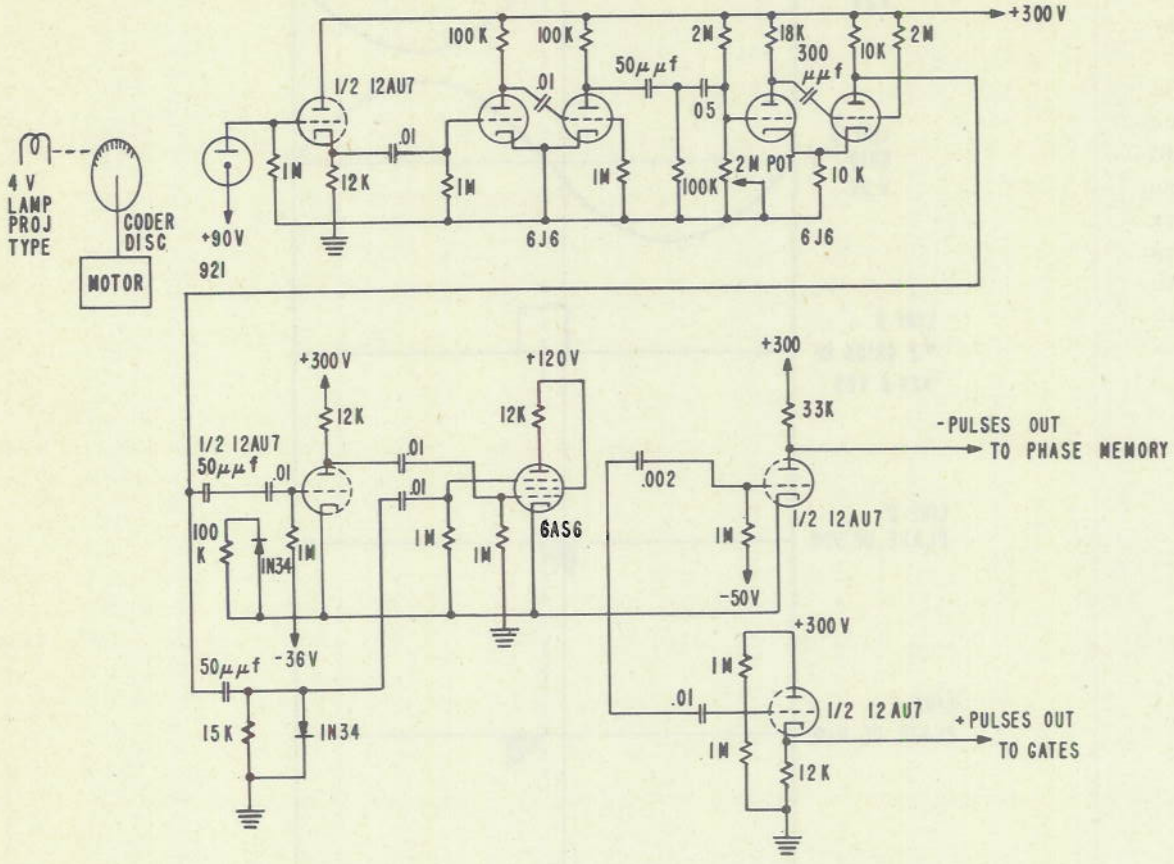

Figure 10 - Clock-Pulse Generator schematic diagram

hysteresis motor (3600 rpm) is used to rotate a 128-segment disc, which interrups the light falling on a Type 921 photocell. The signal detected by the photocell is amplified and differentiated to obtain a total of 128 positive and 128 negative pulses for each revolution of the disc (1/60 second). These voltage pulses are separated; and, after the pulses of one polarity have been inverted, they are mixed to provide 256 pulses of identical polarity each 1/60 second for driving the various counting units within the system.

DISCUSSION

Frequency-response measurements were made on the demonstration model of the Synchro-Data Quantizer and Digital Servo. At the input shaft, a $\pm 4.5^{\circ}$ sine-wave oscillation of varying frequency was applied, and the output-shaft position was measured. An error equivalent to a 1/30-second transmission delay was noted and subtracted from the measured output. The results plotted as ratio of output vs. input, expressed in db, are shown in Figure 11. With the gain and feedback settings used, an apparent bandpass of 1.5 cycles per second with a 3.5 db resonant rise is indicated. The maximum angular rate obtainable with this system was 30° per second.

The demonstration model was built to have an incremental reading accuracy of one part in 256; however, with the end-instruments used (synchro generators and Phase-Shift Networks), an accuracy approaching 1 part in 1000 could be obtained. This indicates that the reading increment could be reduced to 1 part in 512 or 1024. To accomplish this with the demonstration model, the number of stages in each counter and register would have to be increased by 1 for reading 512 points or by 2 for 1024 points. Also, the Clock-Pulse-Generator frequency would have to be increased by the proper ratio. For improved precision, either an indicating end-instrument with higher accuracy or two-speed position indicating systems can be utilized. Precision resolvers are capable of incremental accuracies of better than 1 part in 2000; however, these devices would have to be used as replacements for the position-indicating synchros in present equipment or would have to be positioned by servo systems directed by synchro signals.

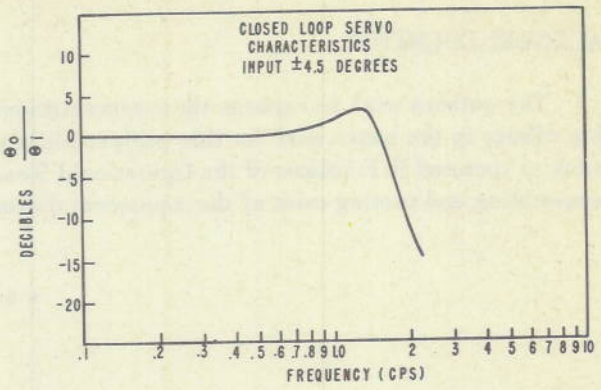

Figure 11 - Demonstration model servo response

A two-speed system offers improved accuracy used with either synchro- or resolver-end instruments. To instrument this system, two position-indicating devices are geared together in a ratio of $1/2^n$ (1/8, 1/16, or 1/32). Separate quantizing counters are used at the output of both the fine and coarse position-indicating devices, and dual Phase-Memory Counters are used at the receiver. The amount of equipment required for the two-speed system is about double that of a single-speed system.

Radio transmission of three, coded, shaft positions (10 pulses per reading on each channel) can readily be accomodated in a voice communication channel bandwidth. With a reading rate at 10 per second, this would require the transmission of 300 pulses per second. The amount of electronic multiplexing equipment required for handling additional channels is offset by the common usage of quantizing circuits in the over-all system; consequently; a three-channel multiplexed system would contain slightly less equipment than that contained in three single-channel systems.

One advantage of any system transmitting quantized data in a pulse-coded form compared with typical analog data-transmission systems, is the fact that no reference frequency or phase has to be transmitted with the data; only the presence or absence of pulses need be detected from the transmitted signal. Nevertheless, the relative sequence of the pulses received must be maintained at all times since the shift of a single pulse position in transmission or reception may halve or double the value of the indicated shaft position. In the system described in this report, a 60-cps base-frequency was used in both the Quantizer and Digital Servo. Such a frequency offers an advantage for internal-ship-data transmission. A ship quantizing on a 60-cycle base-frequency can readily transmit and be received by an aircraft having a Digital Servo operating at a 400-cycle base-frequency. The only requirement on both the Quantizer and the Digital Servo is that the Clock-Pulse-Generator frequency in each equipment be maintained at the same multiple (128, 256, 512, or 1024) of the available base-frequency.

It should be noted that the equipment described in this report represents an early effort in mechanizing a technique; consequently, it is to be assumed that improvement can be made by further component engineering and by a detailed study of the basic theory of sampling-type servo systems. Some consideration has been given to the theoretical aspects of this problem; these results will be issued as an NRL report.*

* *Stafford, B. H., "Frequency Analysis of Some Closed-Cycle Sampled-Data Control Systems," NRL Report 3910*

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