DECLASSIFIED

NRL Report 4619

[redacted]

UNCLASSIFIED

AN INSTRUMENT FOR ACCURATE MEASUREMENT OF PULSE PERIODS

[UNCLASSIFIED TITLE]

J.C. Holmes

Countermeasures Branch
Radio Division

DECLASSIFIED by NRL Contract Declassification Team
Date: 15 MAR 2017
Reviewer's name(s): A. THOMPSON, [redacted]
Declassification authority: NAVY DECLASS MANUAL, 11 DEC 2012, AS SERIES

UNCLASSIFIED

UNCLASSIFIED

October 28, 1955

[redacted]

DISTRIBUTION STATEMENT A APPLIES
Further distribution authorized by UNLIMITED only.

[redacted]

[redacted]

Naval Research Laboratory
Washington, D.C.

UNCLASSIFIED

[redacted]

DECLASSIFIED

CONTENTS

DECLASSIFIED

[redacted]

ABSTRACT

[redacted]

For some time there has been an operational need for a device to measure with an extremely high degree of accuracy the time interval between two pulses in a pulse train. Such a device should be capable of performing this operation over the pulse-period range from 50 μsec to 50,000 μsec, a range that includes low-repetition-rate loran pulses as well as high-repetition-rate radar pulses. Presently available multisweep pulse analyzers, such as the AN/SLA-2, are potentially capable of indicating such pulse periods to within one percent of full scale at best. For certain purposes it is operationally desirable to measure pulse periods to within 1 μsec regardless of the length of the pulse period. This specification dictates an accuracy of measurement to within 0.002% of the maximum period for the measuring equipment if it is to cover the specified range.

Equipment to be used in conjunction with an AN/SLA-2 pulse analyzer has been developed to meet these demands. It is capable of measuring pulse periods from 10 to 100,000 μsec and has provisions for greatly decreasing the effects of noise and unwanted signals. The pulse periods are read directly in microseconds from standard decade scalers. A unique mode of operation is provided whereby visual averaging of many independent readings is accomplished automatically. Descriptions of two previous devices offered as solutions to this problem are also given in detail. The final equipment is considered to be a satisfactory solution to the original problem.

PROBLEM STATUS

This is an interim report; work is continuing on this problem.

AUTHORIZATION

NRL Problems R06-04 and R06-16
Project Nos. NE 071-240- 2 & 4, NR 686-040, and
NL 460-076
Bureau Nos. S-1255.7 and EL-45002
NSA Task No. 332-5802

Manuscript submitted August 16, 1955

[redacted]

DECLASSIFIED

DECLASSIFIED

[redacted]

UNCLASSIFIED

AN INSTRUMENT FOR ACCURATE MEASUREMENT OF PULSE PERIODS [UNCLASSIFIED]

INTRODUCTION

Because of the ever-increasing interest in the measurement of various pulse parameters in radar, loran, and missile-guidance systems, countermeasures operational groups have felt the need for equipments capable of accurately determining spacing between the various pulses in such systems. The accuracy of measurement should be within 1 μsec for any pulse period within the range from 50 μsec to 50,000 μsec. Under optimum conditions, currently available pulse analyzers of the multisweep type (AN/SLA-2 and AN/APA-74) can only measure pulse periods to within 2% of full scale. At 50,000 μsec, this error amounts to 1000 μsec or 1000 times the error prescribed by the above limits.

When the above need became clearly apparent, work was initiated on the design of such equipment. The percentage accuracy of the measurements was to be controlled by a temperature-stabilized crystal oscillator whose drift could easily be held within the 0.002% limits. Such timing devices were commercially available but would have been completely inadequate for operation under field signal conditions. To be useful, moreover, such equipment would have to operate reliably on moderately noisy signals and reject interfering signals. Loran pulses offered a challenge; to measure the period of a given loran pulse required the elimination not only of the slave pulse but of the other loran pulses with periods differing by as little as 100 μsec from the one being measured. It was decided that the equipment should operate in conjunction with an AN/SLA-2 analyzer, but that as few modifications as possible should be made on the analyzer proper. The equipment should have a minimum of controls and should require no special skills on the part of the operator.

The detailed description is divided into three parts: The first section is a general description of the initial equipment which resulted from a preliminary investigation of the problem. The next section describes the final equipment, which differs in so few respects from apparatus built in the second attempt that it was thought advisable to treat it first. The third section discusses the reasons for the choice of some of the methods employed in the present design over the methods used in the second attempt.

GENERAL DESCRIPTION OF INITIAL EQUIPMENT

This equipment was designed for use in conjunction with an AN/SLA-2 pulse analyzer. In principle its operation is as follows: The signal whose period is to be measured is viewed on the AN/SLA-2 screen. A crystal-controlled time base is mixed with the incoming signal and appears on the display along with the signal. The time base can be adjusted in steps from 50 to 50,000 μsec. By visually comparing the length of this known time base with that of the unknown signal, the period of the signal can be determined.

If the lengths of two time bases are to be compared visually on such a display, there must be some means of assuring that the two time bases are initiated simultaneously. This is done by synchronizing the initial point of the accurate time base with that of the sweeps in the AN/SLA-2. Since all the indicator sweeps are initiated simultaneously (exclusive of lockouts) and since the duty cycle of operation of the accurate time base cannot be very high when measuring short pulse periods (as will become obvious later in the discussion), the synchronizing voltage that initiates the accurate time base is derived from the leading

[redacted]

DECLASSIFIED

DECLASSIFIED

edge of the 5000-μsec-sweep intensity gate. Thus every time the 5000-μsec sweep in the indicator fires, and provided the circuits in the measuring equipment are completely recovered and ready to initiate a new time base, the accurate time base is simultaneously initiated.

Provision is made to set the time-base length to any desired multiple of 50 μsec; all of these times are held to within 1 μsec by the controlling crystal oscillator. If the time base is set so that its duration exceeds that of the signal pulse period by not more than 50 μsec, then the trailing edge will appear (as a negative-polarity differentiated pulse) less than 50 μsec behind the signal pulse immediately following that signal pulse which simultaneously fired the 5000-μsec sweep and the accurate time base.

Because the 50-μsec sweep in the AN/SLA-2 is initiated about 60 times as often, on the average, as is the 5000-μsec sweep, the signal pulse (trailed by the back edge of the time base) will quite frequently initiate the 50-μsec sweep. Thus the trailing edge of the time base will appear on the 50-μsec sweep, and the distance between the initiation of this sweep and the termination of the time base can be read directly in microseconds from the 50-μsec scale. This time reading subtracted from the length of the time base itself gives the true period of the signal pulse to within 1 μsec.

Figure 1 is a display of a signal pulse with a repetition rate of 60 cps (a period of 16,666.6 μsec). The operator sets the time-base length to the approximate period of the signal pulse as read from the 50,000-μsec sweep on the indicator. By setting the time-base length slightly longer than the period of the signal pulse, he can make the trailing edge of the time base appear on the 5000-μsec sweep. He next shortens the time base by successive multiples of 50 μsec until the trailing edge of the time base is less than 50 μsec behind the signal pulse as seen on the 500-μsec sweep. He then reads on the 50-μsec sweep scale the amount (e.g., 34 μsec) by which the signal period is shorter than the time base. This figure subtracted from the length of the calibrated time base gives the pulse period. In this example the answer is 16,700 - 34 = 16,666 μsec. The jitter seen in the trailing edge of the time base is (assuming a jitterless signal pulse) due to the fact that the time base is initiated by the signal pulse but is terminated only after a predetermined number of pulses from a continuously running 1-Mc crystal clock have occurred. In general the time base will not be initiated simultaneously with a clock pulse. Thus the time between initiation and termination of the time base can vary up to a maximum of 1 μsec. If there is jitter present in the signal itself, it will show up as jitter in the reading on the 50-μsec scale, thus making the equipment an accurate device for measuring small-percentage jitter in a signal having a long pulse period.

CIRCUIT DETAILS OF INITIAL EQUIPMENT

A block diagram of the equipment is shown in Fig. 2. The output from a 1-Mc oscillator is sent through a pulse shaper which converts the 1-Mc sine wave into a square wave. These pulses are sent through a gating circuit to trigger a 1-Mc decade pulse counter. The output pulse from this counter (one output pulse occurs for every ten input pulses) triggers a second decade counter (100 kc) which in turn produces one output pulse for every ten entering it. Thus for every one hundred pulses emanating from the clock pulse circuit, one pulse is produced at the output of the 100-kc counter. One of these output pulses occurs every 100 μsec. Three cascaded preset counters follow the 100-kc counter. By means of pushbutton switches on each of the preset counters, a single pulse may be produced at the output of the last preset counter at any multiple of 100 μsec after the first pulse from the 100-kc counter enters the preset counters. By proper selection of pushbuttons, the operator

[redacted]

DECLASSIFIED

DECLASSIFIED

[redacted]

UNCLASSIFIED

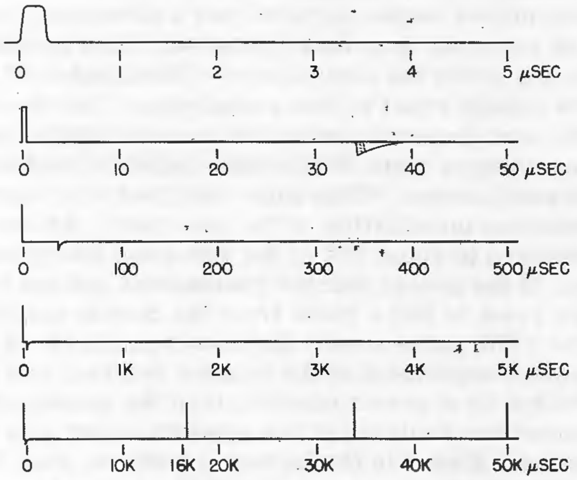


Fig. 1 - 60-cps signal and measuring gate on 5-gun analyzer

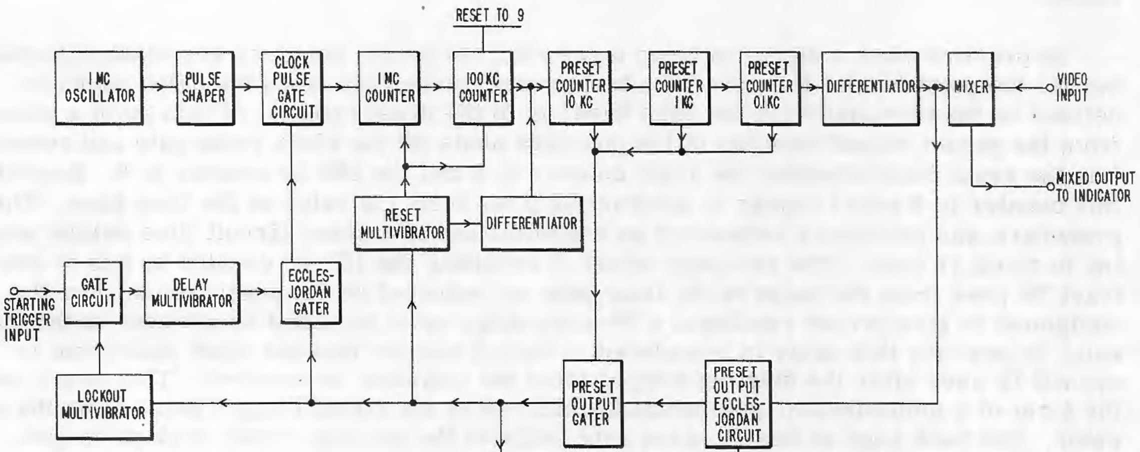


Fig. 2 - Block diagram of initial equipment

can adjust this delay in steps of 100 μsec throughout the range from 100 to 100,000 μsec. The output pulse from the last preset counter is differentiated and mixed with the video signal at the input to the indicator, and appears as a negative-polarity marker pulse (trailing edge of time base) on the indicator sweeps (Fig. 1). The time base is initiated by the first clock pulse to enter the counters after the clock pulse gate is opened. The opening of this gate is controlled by the signal pulse (initiation of the 5000-μsec indicator sweep). Both the process of initiation of the time base and the method of adjusting its length in steps of 50 μsec (rather than 100 μsec) are closely interrelated and will be discussed later.

[redacted]

DECLASSIFIED

DECLASSIFIED

The three preset counters are not operated in the conventional manner. The output pulse from the common preset output terminal has a slow rise time that would not be suitable for terminating an accurate time base. However if the pushbutton switches on the three preset counters are set to the complement of the number of 100-μsec periods desired, and if the counters are always reset to this complement, then the counters will count the desired number of 100-μsec intervals before the count of 000 is reached on the preset counters. As the count changes from 999 to 000 a pulse is produced at the decade output terminal of the last preset counter. This pulse has good rise time, and is used as the marker pulse to indicate the termination of the time base. An example will clear up this point. Suppose it is desired to count 777 of the 100-μsec intervals before the termination point of the time base. If the preset counter pushbuttons are set to read 223 (000 - 777), and if the counters are reset to 223 a pulse from the decade output of the last preset counter will be produced as the 777th pulse enters the preset counters. Furthermore, if after the counters are reset to the complement of the number desired, and if by some means one extra count is added to the first preset counter, then the numbered caps on the pushbutton switches may be removed and replaced in the opposite order with the 0 being placed in the former 9 position and the 1 placed in the former 8 position, etc. The desired count may now be set directly by pushing the buttons labeled with the desired count. Pushing the buttons labeled 777 activates switches formerly labled 222 instead of switches 223. The single extra pulse enables one, in effect, to subtract the desired count from 999 rather than 000 so that rearrangement of the buttons gives the proper count when that count is "dialed" on the pushbuttons. This single extra pulse is derived from the reset-pulse multivibrator described below.

In practice when a signal is being measured, the preset counters are allowed to count beyond the point 000 (at this count the last preset counter produces the pulse which is defined as the termination of the time base) up to the preset count. At this point a pulse from the preset output terminal of the counters shuts off the clock pulse gate and resets (via the reset multivibrator) the 1-Mc counter to 0 and the 100-kc counter to 9. Resetting this counter to 9 would appear to subtract 90 μsec from the value of the time base. This procedure was necessary because of an accumulation of various circuit time delays amounting to about 11 μsec. The resultant effect of resetting the 100-kc counter to 9 is to subtract 79 μsec from the value of the time base as indicated on the pushbuttons. For the equipment to give proper readings, a 79-μsec delay must be added somewhere in the circuit. In practice this delay is introduced in such a manner that the clock pulse gate is opened 79 μsec after the starting trigger from the indicator is received. This delay takes the form of a multivibrator gate which is initiated by the signal trigger pulse from the indicator. The back edge of this 79-μsec gate initiates the opening of the clock pulse gate. The true length of the time base (measured from the time of initiation of the indicator sweeps to the time a trailing-edge marker pulse appears on the indicator display) is now actually the reading that is selected by the pushbuttons.

To select gate widths in multiples of 50 μsec, a switch that controls the width of the delay multivibrator gate is switched from the 00 position to the +50 setting. With the switch in this position two circuit changes are effected. The extra pulse that normally advances by one the count on the first preset counter is eliminated. This effectively adds 100 μsec to the time-base period as read on the preset-counter pushbuttons. This delay when added to the inherent 11-μsec delay gives a total delay of 111 μsec. The resetting of the 100-kc counter to 9 effectively subtracts 90 μsec from this figure, leaving a net delay of 21 μsec. It is desired to have a total time delay amounting to exactly 50 μsec more than the indicated setting as read off the preset-counter pushbuttons. To accomplish this, the time-delay multivibrator gate width is switched to 29 μsec which, when added to the 21-μsec net delay, gives a total delay of exactly 50 μsec longer duration than is indicated on the pushbuttons.

[redacted]

DECLASSIFIED

DECLASSIFIED

UNCLASSIFIED

The preset counters used in this equipment have a disadvantage that requires the use of extra circuits for proper operation. After the preset output pulse occurs, several similar pulses (from the preset output) occur between the preset and the 000 count. These pulses must be prevented from reaching the circuits that are triggered by the preset pulse. A gating circuit and its associated Eccles-Jordan lockout multivibrator (Fig. 2) lock out these extraneous pulses by turning off the gate tube with the arrival of the first preset pulse and turning it on with the arrival of the 000 count pulse.

Another circuit that operates from the preset output pulse is the starting-trigger lockout multivibrator. On the arrival of the preset pulse, all circuits are reset and the lockout multivibrator opens the starting-trigger gate circuit only after all the circuits have had sufficient time to recover completely (about 60 μsec).

Operation of the equipment is simple. For example, suppose the operator sees on the indicator a pulse having a 60-cps repetition rate. He sets the pushbuttons to the approximate pulse period (170, indicating a pulse period of 17,000 μsec). The marker pulse indicating the end of the time base now appears on the 50-μsec sweep at 34 μsec. The operator simply multiplies the pushbutton reading by 100 and subtracts the reading obtained from the 50-μsec sweep. In the above example he finds that the pulse period is 16,666 ±1 μsec. (If the delay multivibrator switch is set to +50, the operator then adds 50 μsec to the final answer.)

The equipment described above has three major disadvantages:

(1) Deriving a sync pulse requires slight alteration of the indicator with which the equipment is to be used. A circuit change must be made and an extra cable connector installed on the indicator chassis.

(2) There is no provision for decreasing the effects of noise on a signal.

(3) When measuring signals having low repetition rates, the display on the 50-μsec sweep is of such low intensity that it is difficult to see the marker pulse. The reason for this is that the time base is not generated with every signal pulse. At best, the time base is only generated for one out of every two signal pulses. As a result, the practical operation of this equipment is limited to a semidarkened room.

GENERAL DESCRIPTION OF FINAL EQUIPMENT

Because of the above-mentioned deficiencies in the experimental equipment, new circuits were designed. The resulting equipment has none of the disadvantages listed above. It is much more versatile than previous equipment in that it has four separate modes of operation rather than one. The present equipment no longer requires the use of a visual pulse analyzer as did previous models; however, provision has been made for connecting the new interval-measuring equipment to a pulse analyzer (AN/SLA-2 or APA-74) so that the two may be used in conjunction. The pulse period of the signal being investigated is now entered on neon-bulb decimal indicators, and the operator can read the figures directly to an accuracy of 1 μsec. These new techniques for displaying the pulse-period information make the equipment easier to operate with a less confusing set of controls.

A block diagram of the most basic parts of the equipment is shown in Fig. 3. The video pulse signal to be examined is amplified to a level suitable for slicing. The noise on the baseline and tops of the pulses is then sliced from the pulse by a Schmitt slicing

[redacted]

DECLASSIFIED

DECLASSIFIED

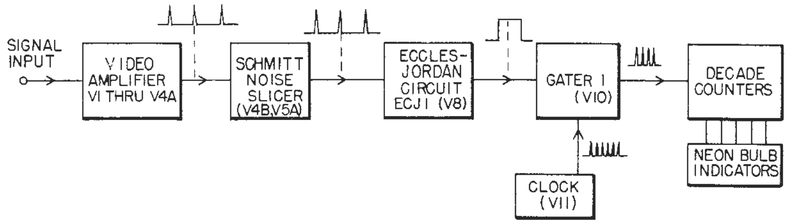


Fig. 3 - Basic block diagram of final equipment

circuit. These sliced pulses are sent to a symmetrically triggered Eccles-Jordan circuit, the first pulse causing the multivibrator to commutate in one direction and the next pulse returning it to its original state. (For purposes of simplification, this Eccles-Jordan circuit will be referred to as ECJ 1.) The width of the pulse produced by the Eccles-Jordan circuit is equal to the period of the incoming pulse waveform. The output pulse from the Eccles-Jordan circuit is sent to one input of a gating circuit (gater 1). To the other input is sent a continuous train of positive-polarity pulses, one pulse arriving every microsecond, the accuracy of their repetition rate being directly controlled by a crystal oscillator (clock). It is this clock that determines the absolute accuracy of the equipment. Only those clock pulses that are coincident with the duration of the positive-polarity gate from the Eccles-Jordan circuit pass through the gater to the decade counters. The counters register the total number of these pulses, and the final count which is displayed directly on neon bulbs is the period of the video signal pulse in microseconds. All the pulse-period information is displayed on these bulbs, and the operator has at his disposal four different modes in which this information can be displayed.

Figure 4 is a block diagram of the basic parts of the equipment used in the first mode (mode 1) of operation. To the block diagram of Fig. 3 have been added a start switch, a reset switch, and an automatic stop circuit. In this mode of operation, the sliced video signal is sent through a gating circuit (gater 2) to symmetrically triggered ECJ 1. The output from another Eccles-Jordan circuit (ECJ 2) is dc coupled to the remaining input terminal of gater 2. With the application of a starting pulse from the manually operated start switch, ECJ 2 commutates and opens the gating circuit. Signal pulses are then allowed to pass to ECJ 1. The first pulse to enter this circuit opens gater 1 and allows clock pulses to be passed on to the counters. The second pulse from gater 2 switches ECJ 1 in the opposite direction, thus preventing additional clock pulses from reaching the counters. The trailing edge of the positive-polarity gate from ECJ 1 is differentiated and used to trigger ECJ 2 so that it cuts off gater 2. The signal pulse period in microseconds remains displayed on the neon-bulb indicators. The counters may be reset to zero by actuating the reset switch. Another count may then be made by simply actuating the start switch. The decimal counter units register a total of 5 digits so that pulse periods of duration up to 999,999 μsec may be measured. Jitter in a signal pulse may be detected by measuring the period a number of times and recording the reading for each trial. The magnitude of the jitter can then be estimated from the amount of variation in the readings.

To save the time and trouble of writing down separate results of each trial and the subsequent time used to examine the data, a second mode (mode 2) of operation is available (Fig. 5). The automatic stop circuit ECJ 2 (Fig. 4) has been replaced by a multivibrator feedback loop; the reset thyratron is now triggered automatically from the multivibrators in this loop, and a circuit has been added to switch on and off the neon-bulb indicator lamps in the decimal counting units. The operation is as follows: With no signal input, gater 2 is

[redacted]

DECLASSIFIED

DECLASSIFIED

UNCLASSIFIED

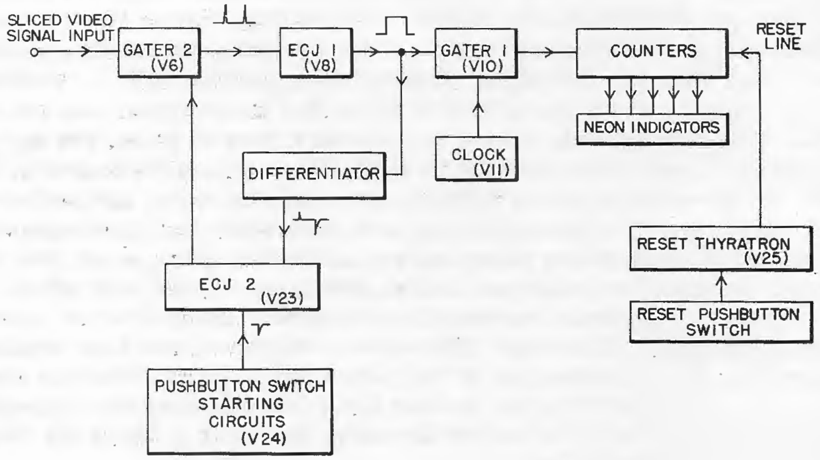


Fig. 4 - Block diagram of final equipment in mode-1 operation

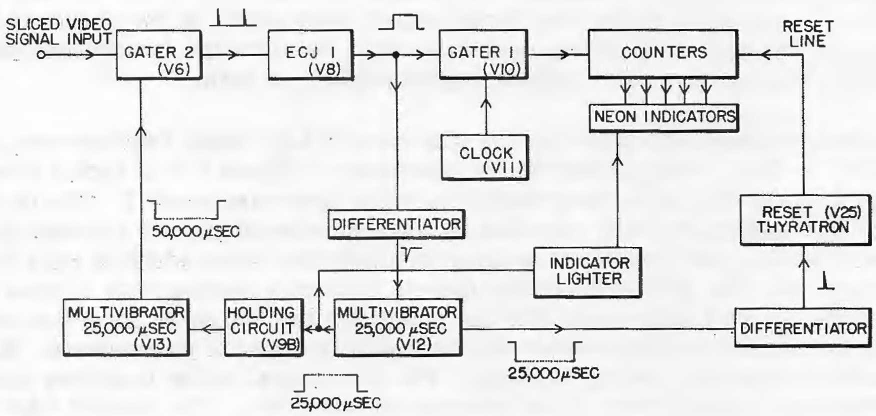


Fig. 5 - Block diagram of final equipment in mode-2 operation

normally open, and ECJ 1 has turned off gater 1. The counters have been reset to 00000, and the neon bulbs are turned off. At the arrival of a signal pulse, ECJ 1 opens gater 1 which allows clock pulses to pass on to the counters. The second signal pulse to arrive turns off ECJ 1, thus terminating the clock-pulse gate. The trailing edge of the ECJ 1 gate is differentiated to trigger a single-shot multivibrator having a gate width of about 25,000 μsec. This multivibrator gate lights the neon-bulb indicators so that the final count stored in the counters may be read by the operator. The count remains indicated throughout the 25,000-μsec gate of the multivibrator, at the termination of which the counters are automatically reset to 00000 and the indicator bulbs turned off. (If the bulbs were allowed to remain lit during the actual counting process, the operator would experience great difficulty in determining which of the flashing bulbs corresponded to the final count.) At the time of initiation of the 25,000-μ sec gate, a second multivibrator having a natural gate width of 25,000 μsec, is triggered. By the incorporation of a special holding circuit, the

[redacted]

DECLASSIFIED

DECLASSIFIED

output gate produced by this second multivibrator has a total width of 50,000 μsec, equal to the sum of the two individual gate widths. The leading edge of this 50,000-μsec gate, which is initiated at the time of occurrence of the second signal pulse, is used to turn off gater 2, thus preventing the next signal pulse from triggering ECJ 1. During the first half of the 50,000-μsec gate, the neon bulbs are lit so that the operator can see the actual count. The second 25,000-μsec interval allows the counters time to reset, the neon bulbs to be turned off before the next count, and the first 25,000-μsec multivibrator to recover. At the end of the 50,000-μsec gate, the circuits are ready to repeat the performance, during which time a second count is flashed on the neon indicators for approximately 25,000 μsec. In this manner, up to 20 separate pulse-period indications per second may be made. The operator simply watches the bulbs and notices which ones flash most often. The finite fall time of the operator's eye-brain combination effectively integrates the individual bulb flashes; those bulbs which flash most often appear brightest, and thus automatically leave the operator with a mental histogram of the pulse-period jitter about the mean pulse period. Thus the operator, after watching the display for a few seconds, can immediately write down a figure for the pulse period and at the same time give a figure for the amount of variation (jitter) about this period.

In the presence of noise, the amount of variation about the figure that seems to appear most often gives the operator some idea of the accuracy of this figure. In the presence of strong noise (atmospheric) or strong interfering signals with periods differing from that of the signal chosen for examination, both modes 1 and 2 of operation become less and less practical as the strength of the interfering signal increases. In the presence of such disturbances, the equipment reads the period between the first two pulses that come along, whether these signals are noise pulses, signal pulses, or both.

To alleviate these difficulties in the presence of high-level interference, another mode of operation has been incorporated in the equipment. Figure 6 is a highly simplified block diagram of some of the basic components used for operation mode 3. The basic block diagrams of Figs. 4 and 5 have been modified by the insertion of gater 3 between gater 2 and ECJ 1. In addition, a set of preset decimal counters has been added in parallel with the regular counters. The preset counters operate in such a manner that a pulse from their output terminal occurs coincident with the arrival of the nth pulse from the clock pulse generator, the number n being selected beforehand by a set of pushbuttons. In operation, gater 3 is opened by the starting circuits. The first signal pulse to arrive causes ECJ 1 to switch thereby opening gater 1 and starting the counters. The leading edge of the ECJ 1 gate is differentiated and sent to the gating circuits which in turn close gater 3 and shut out further signal pulses. After n pulses have entered the counters, a preset pulse occurs which is used to trigger the inclusion-gate multivibrator. At the arrival of the inclusion gate, the gating ciruits open gater 3 and hold it open until the termination of the inclusion gate. Thus after the arrival of the first signal pulse, no pulses can be passed to ECJ 1 until n clock pulses have entered the counters. As the nth clock pulse is generated, gater 3 is opened to signals for a period equal to the length of the inclusion gate. Any extraneous pulse signals occurring between the first pulse and a time n μsec later are prevented from actuating the equipment. Only if a pulse falls within the inclusion gate, is it able to pass through gater 3. For instance, suppose an operator suspects a signal pulse has a period in the vicinity of 2000 μsec (500 cps). If on his pulse analyzer he spots some very strong interfering signals having periods of 800 μsec, 1200 μsec, 1500 μsec, and 1800 μsec, he can eliminate them by simply setting the preset pushbuttons to read 1850 μsec. If he adjusts the inclusion gate width to a width of 200 or 300 μsec, he can then read the period of the desired signal pulse, all pulse periods between 0 and 1850 μsec having been eliminated.

DECLASSIFIED

UNCLASSIFIED

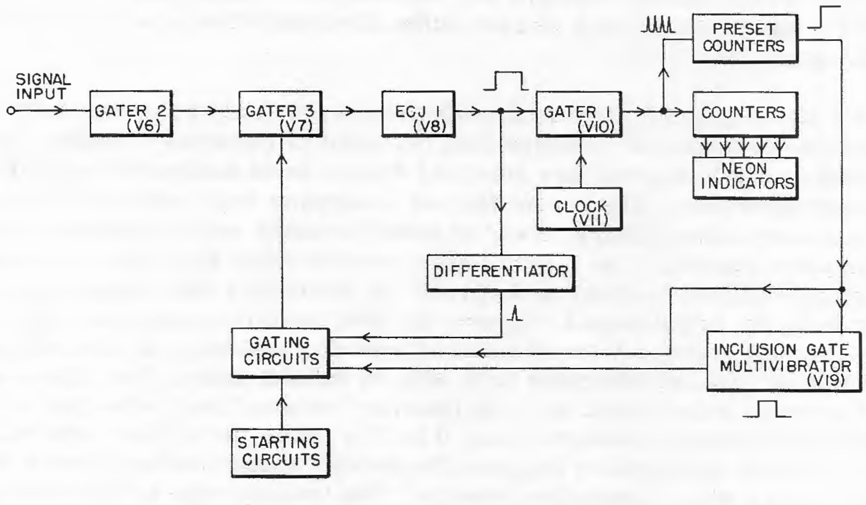


Fig. 6 - Basic block diagram of final equipment in mode-3 operation

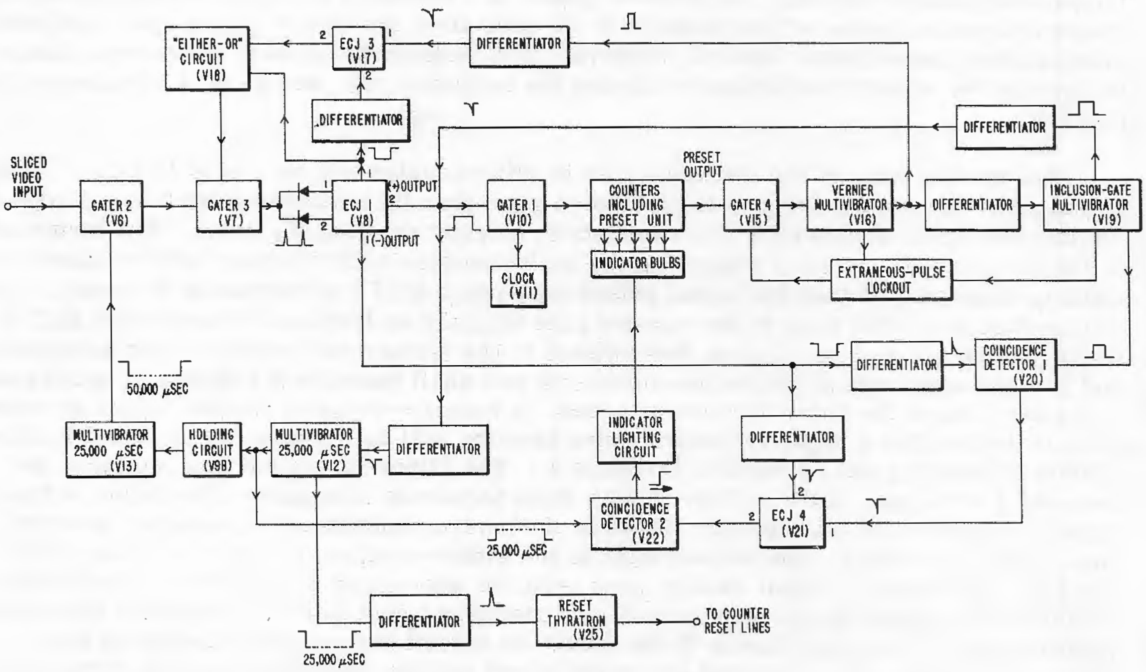


Fig. 7 - Detailed block diagram of final equipment in mode-3 operation

Figure 7 is a detailed block diagram of the components used for this third mode of operation. Several refinements have been added to the basic components described in the simplified block diagram (Fig. 6). In this mode of operation, the counters will perform up to 20 separate counts per second, and display them visually only if the pulses fall within the inclusion gate whose width may be arbitrarily set by the operator. If no pulses fall

DECLASSIFIED

within the inclusion gate, the counters are reset at the termination of the gate, and the process starts again. At no time are the bulbs lit except when a pulse is coincident with the inclusion gate.

Figure 7 shows gater 2, the two 25,000-μsec multivibrators, gater 3, ECJ 1, gater 1, and the counters in the same positions they occupied in previous simplified diagrams. The counters used in this equipment are standard decade units designed to operate at a 40-kc maximum repetition rate. The preset feature is already built into the units so that separate preset counters are unnecessary. Four of these counters were modified to operate at 100 kc (10-μsec pulse spacing). No 1-Mc preset counters were available, nor could any existing counters be modified to count at that rate. A standard 1-Mc counter is used to count the clock pulses; its output signal triggers the first modified preset counter. Consequently, preset pulses could ordinarily be obtained only after n multiples of 10 clock pulses had passed. It was considered desirable to be able to exclude interfering pulses up to within 1 μsec of the signal pulse itself, so an adjustable "vernier" multivibrator was connected to the output of the preset counters to add 0 to 10 μsec to the reading indicated by the push-buttons. The preset output pulse triggers the vernier multivibrator through a gating circuit (gater 4) which will be described shortly. The trailing edge of the vernier gate is differentiated and used to trigger the inclusion-gate multivibrator. Connections made to both the vernier and the inclusion-gate multivibrators go to a lockout circuit that closes gater 4 during the period when either multivibrator is producing a gate. Because of the nature of the preset-counter circuitry, extraneous pulses are produced at the preset output terminal. These pulses can occur at any multiple of 10 μsec after the desired preset pulse is produced, although they cannot occur before. However, it is undesirable to have extraneous pulses triggering the vernier multivibrator during the inclusion gate, and gater 4 eliminates this problem.

The trailing edge of the inclusion gate is differentiated and sent back to ECJ 1. If no signal pulse has arrived during the inclusion gate, then this differentiated trailing edge of the inclusion gate forces ECJ 1 to commutate, thereby stopping the count. The termination of the vernier gate, besides triggering the inclusion-gate multivibrator, also initiates the opening of gater 3 so that the signal pulses may reach ECJ 1 to terminate the count. The differentiated trailing edge of the vernier gate triggers an Eccles-Jordan circuit ECJ 3 which in turn sends a positive dc step voltage to the "either-or" circuit. (The numbers 1 and 2 at the terminals of an Eccles-Jordan circuit shall henceforth indicate to which plate of the dual triode the terminals are attached. A negative-polarity trigger signal on terminal 1 indicates that a negative-polarity step function will be produced at terminal 1 while a positive-polarity one appears at terminal 2.) The either-or circuit has two input and one output terminal. If the voltage at both input terminals is negative, the output voltage is negative and gater 3 is closed. However if either or both input voltages are positive, then gater 3 is opened. The second input to the either-or circuit is derived from ECJ 3. The ECJ 1 terminal-1 output voltage goes negative when gater 1 is opened. The leading edge of this negative-polarity gate is differentiated and sent to ECJ 3 to switch its output negative also. Thus, both inputs to the either-or circuit are negative during the time before the counters have reached the preset count and the subsequent arrival of the trigger from the trailing edge of the vernier multivibrator gate. With the arrival of this trigger, the either-or circuit opens gater 3 and leaves it in this condition until a signal pulse has passed through gater 3 to start a new cycle. The signal cannot, however, get through gater 2 until the counters have been reset and the 50,000-μsec gate has terminated.

The gate from the inclusion-gate multivibrator is sent to one input of a coincidence detector. To the other input is sent the differentiated trailing edge of the negative-polarity gate from ECJ 1. (The ECJ 1 gate will henceforth refer to that waveform which lies between

DECLASSIFIED

DECLASSIFIED

UNCLASSIFIED

the times of initiation and completion of the count.) If this trailing edge of the ECJ 1 gate arrives during the inclusion gate, a pulse is produced at the output of the coincidence detector. This pulse triggers ECJ 4 which in turn produces a positive-polarity output voltage step. (ECJ 4 had been triggered in the opposite direction by the leading edge of the ECJ 1 gate.) This positive-polarity signal is sent to one input of a second coincidence detector, the other input of which is connected to the positive-polarity signal from the first 25,000-μsec multivibrator. Positive-polarity signals must appear at both grids of coincidence detector 2 before the indicator lights can be lit, and if no signal arrives, the bulbs do not light at all. If this is the case, the differentiated edge of the inclusion gate terminates the ECJ 1 gate, the counters are reset to 00000, and the system is ready to try again as soon as the 50,000-μsec gate has terminated. If a video signal pulse does occur during the inclusion gate, the bulbs are lit for approximately 25,000 μsec, after which time they are extinguished and the counters are reset. The inclusion-gate width may be set at any value between 3 μsec and about 1600 μsec.

The fourth mode of operation is very similar to the first, in which the start and reset switches replace the automatic circuits. The fourth mode differs from the first in that the equipment counts pulse periods automatically over and over again until the pulse pair with the proper period (as set by the pushbuttons and inclusion gate width) arrives. When a pulse finally falls within the inclusion gate, the incoming signal is shut off, the indicator bulbs are lit, and the pulse-period reading remains on the bulbs until the reset switch is actuated. Like mode 1, mode 4 only produces one reading at a time, but it picks only those pulse pairs that fall within the set range on which to indicate a final count. This mode of operation has the advantage that one can list a number of separate counts one at a time so that the readings may be compared at some later date.

A block diagram of the components used for this mode of operation is given in Fig. 8. There are only two major changes from the block diagram of Fig. 7. Coincidence detector 2 is not used because once coincidence detector 1 detects a coincidence, the bulbs are to stay on indefinitely or until the reset switch is actuated. The other change involves the addition of a second either-or circuit and the reintroduction of ECJ 2. Either-or circuit 2 operates so that when both inputs are positive, gater 2 is opened, but when either or both inputs are negative, gater 2 is cut off. The equipment is started by actuating the start switch. This places a positive polarity on one input of either-or circuit 2. (The other input normally rests positive except during the 50,000-μsec gate.) Signal pulses are now allowed to pass through gaters 2 and 3 to initiate the ECJ 1 gate. If during the inclusion gate no signal pulse arrives to terminate the ECJ 1 gate, the trailing edge of the inclusion gate terminates it as before, and the counters are reset after 25,000 μsec. The indicator lamps do not light, and the negative polarity 50,000-μsec gate from the two 25,000-μsec multivibrators closes gater 2. At the termination of the 50,000-μsec gate, gater 2 is turned back on, and the cycle is repeated until a signal pulse falls within the inclusion gate. When this happens, the coincidence detector triggers ECJ 4 which lights the indicator lamps. The coincidence detector also sends a pulse to ECJ 2 which in turn sends a negative-polarity voltage to either-or circuit 2. This negative voltage prevents signal pulses from activating the equipment until the circuits are reset and the start switch is reactuated.

In the various block diagrams discussed above, some circuits have been omitted in the interest of simplifying the explanations. These omissions will be fully covered in the following section which describes all the circuits in detail.

DECLASSIFIED

DECLASSIFIED

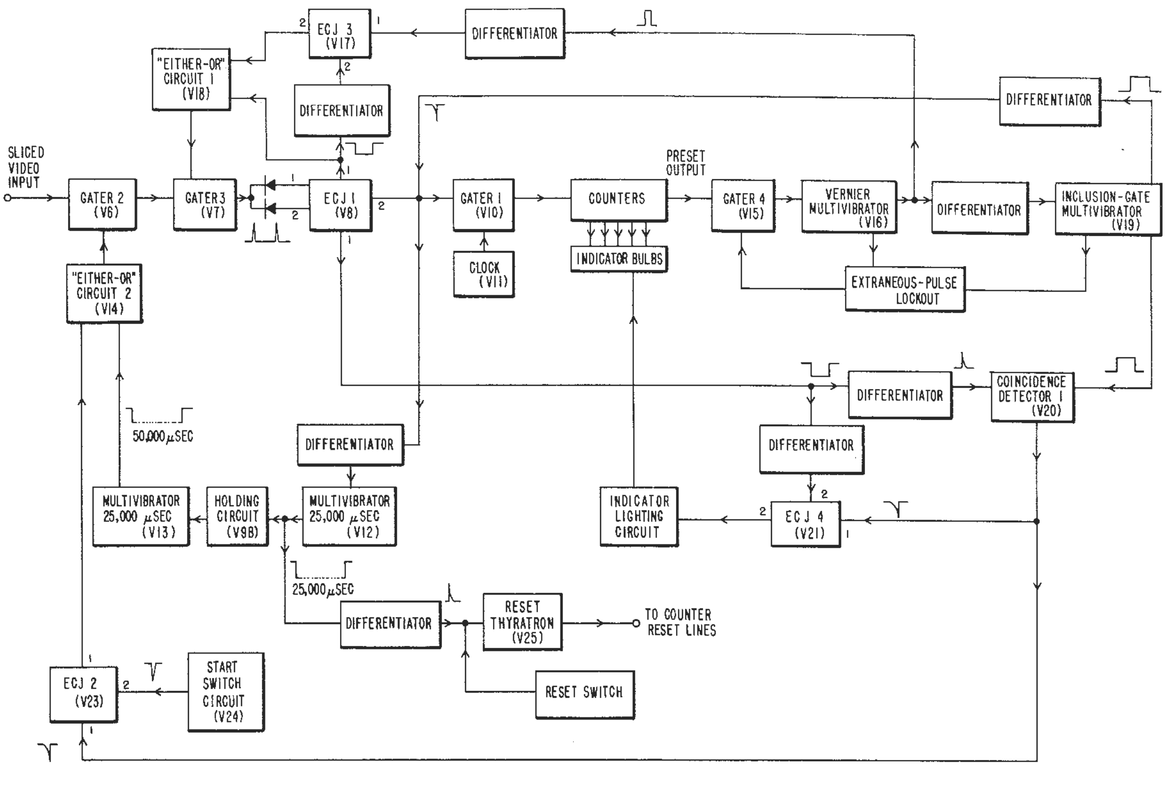


Fig. 8 - Block diagram of final equipment in mode-4 operation

CIRCUIT DETAILS OF FINAL EQUIPMENT

In order that this equipment may be used independently of any external apparatus, such as a slave sweep-pulse analyzer (AN/SLA-2 or APA/74), the incoming video signal must be amplified by an amplifier of suitable bandwidth. Incorporation of such an amplifier also allows operation of the equipment in conjunction with such an indicator without necessitating any modifications on the indicator itself. Figure 9 is a circuit of the three-stage amplifier incorporating two 404A's as amplifiers and a 5670 as a split-load amplifier which operates either as a cathode follower or as a phase inverter. Switch SW1 allows amplification of either positive- or negative-polarity video pulses so that positive-polarity signals are always produced at the plate terminal of V3. Cathode follower V4A provides a low-impedance output for the amplified signal. A portion of this signal is sent to one input of a dual-triode mixer, V26. To the other input of V26 is fed a portion of the inclusion-gate signal voltage. These two signals are added, and their sum may be sent to the pulse analyzer so that both the video signal and the pulse-inclusion gate will appear on the indicator sweeps.

The signal from the cathode of V4A is also sent to a Schmitt slicing circuit wherein both the top and bottom of the pulse are literally sliced away, leaving only a small portion of the pulse about half way between the baseline and the top of the pulse. In this manner noise that appears on the top or baseline of the pulse is eliminated, and only those noise spikes that traverse the slice region appear at the slicer output. Potentiometer R2 adjusts the input resting voltage to the slicer and thus determines the voltage level in the signal

[redacted]

DECLASSIFIED

pulse from which the slice is taken. In practice, the video gain control R1 is set to produce at the cathode of V4A an output pulse of approximately 20 volts amplitude. Potentiometer R2 is then set so that the slice is taken from a point about 10 volts up from the baseline.

In addition to slicing the video pulse signals, the Schmitt circuit performs one other very important function. In order to measure accurately the time interval between two pulses having leading edges of finite slope, it is necessary that the measuring interval begin and end at points of equal voltage on the slopes of the two pulses. Because the Schmitt circuit is amplitude triggered rather than slope triggered, it automatically triggers at the same voltage point on each pulse. The pulses produced by the Schmitt circuit have fast rise times (0.04 μsec) regardless of the rise time of the incoming signal, so that for equal-voltage points on the slopes of each pulse, a fast-rise-time pulse is automatically produced.

The square-output pulse from the Schmitt circuit is differentiated and sent to one grid of gating tube V6 (Fig. 10). This tube produces at its plate terminal a negative-polarity signal pulse whenever a positive-polarity voltage appears on both grids simultaneously. One grid is used for the incoming signal, and the other is used to turn this signal on or off by means of a gating pulse. The negative-polarity pulse from the plate of V6 is sent to amplifier-inverter V5B which in turn produces a positive-polarity pulse to drive one grid of a second gating tube, V7. The gating grids of both V6 and V7 must be positive for a signal to pass from the input of V6 to the plate of V7.

The negative-polarity signal from the plate of V7 drives the symmetrically triggered Eccles-Jordan circuit V8 (Fig. 11). This circuit, which was specially designed for use in this equipment, differs in several respects from standard circuits found in the literature. The plate supply voltage is quite low (180 volts), and the positive side is grounded. The two outputs from the circuit are used eventually to switch on and off the grids of two grounded cathode gate tubes, V7 and V10. Grounding the V8 plate returns allows the grids of V7 and V10 to be directly coupled (via cathode followers) to the V8 plates. This type of connection guarantees properly referenced gating voltages at the V7 and V10 grids, even if the plate supply voltage is varied over a relatively wide range. This stability could not be realized with conventional dc divider-network coupling circuits.

The use of neon-bulb coupling networks that form the multivibrator feedback paths made possible the low plate supply voltage of 180 volts. Unlike conventional dc divider networks, the full signal voltage at the plate of one tube is transferred to the grid of the other. The circuits can thus be designed for use with low plate supply voltages and still have sufficiently large grid signals to insure stability. The effective circuit-to-ground coupling capacity of these coupling networks has been kept as low as with conventional dividers.

The 430-$\mu\mu$f capacitors serve a dual purpose. First, they serve as low-impedance paths for transient voltages, and second, they act in combination with the 12K resistors as hash filters for neon-bulb noise. Considering for the moment the series circuit consisting of the two neon bulbs and the 12K resistor, the neon bulbs appear as a high inductive impedance, while the resistor has an impedance of 12K ohms. As long as the wire lead connecting the tube plate to the bulb and the lead connecting the resistor to the grid are kept short, the capacity to ground of the wiring between the bulbs and the resistor is of little consequence. The 430-$\mu\mu$f capacitors may be wired directly to the tube socket terminals so that their contribution to the stray capacity is kept at a minimum, The 470K resistors that shunt one neon bulb in each network are necessary to insure firing of the bulbs when the plate voltages are first applied. These resistors are not otherwise a functional part of the networks.

UNCLASSIFIED

DECLASSIFIED

[redacted]

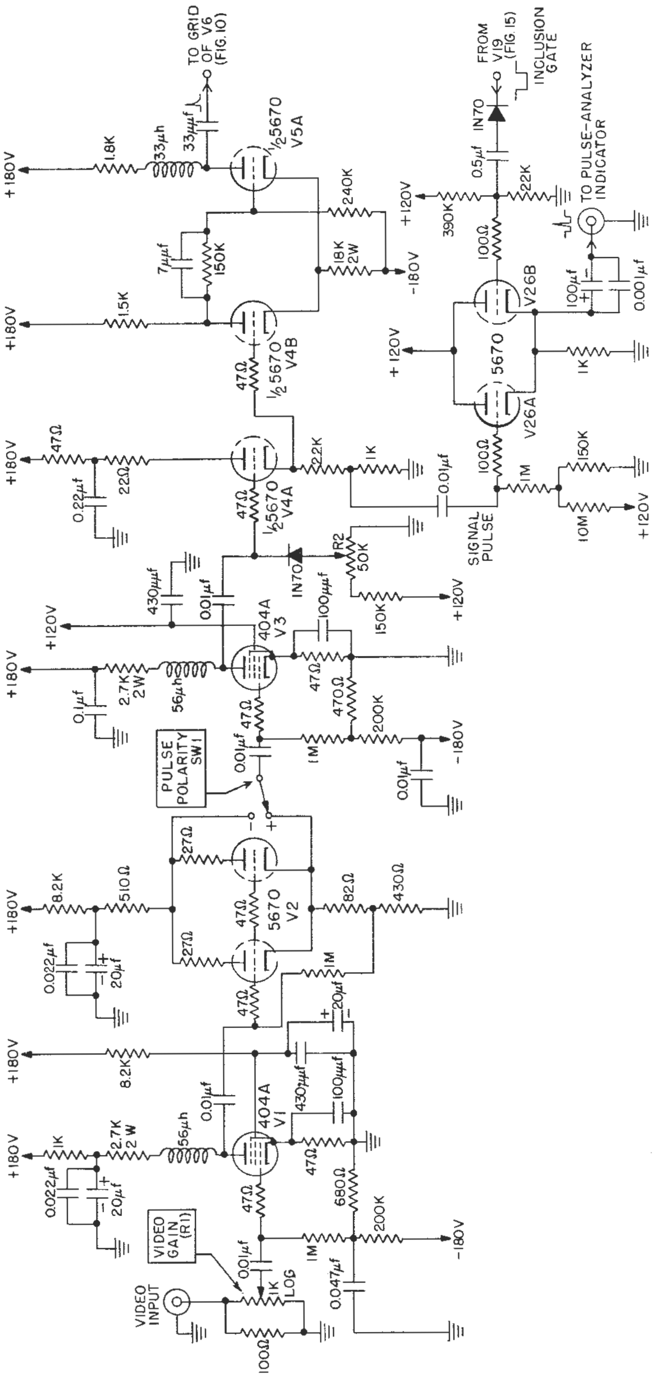


Fig. 9 - Video amplifier and noise slicer

[redacted]

DECLASSIFIED

DECLASSIFIED

UNCLASSIFIED

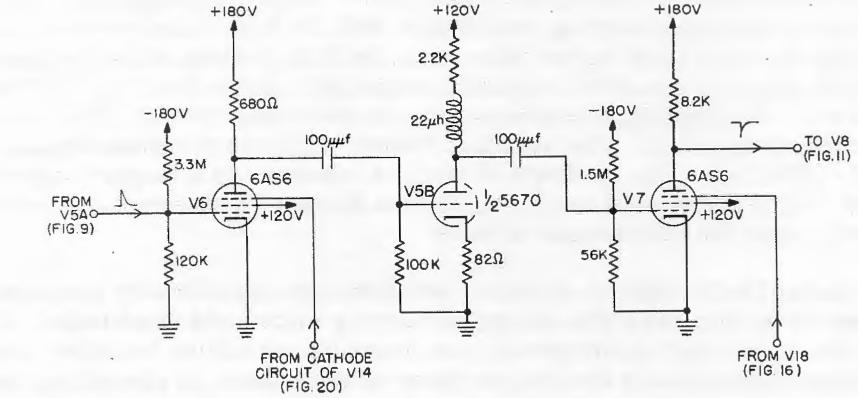


Fig. 10 - Gaters 2 and 3

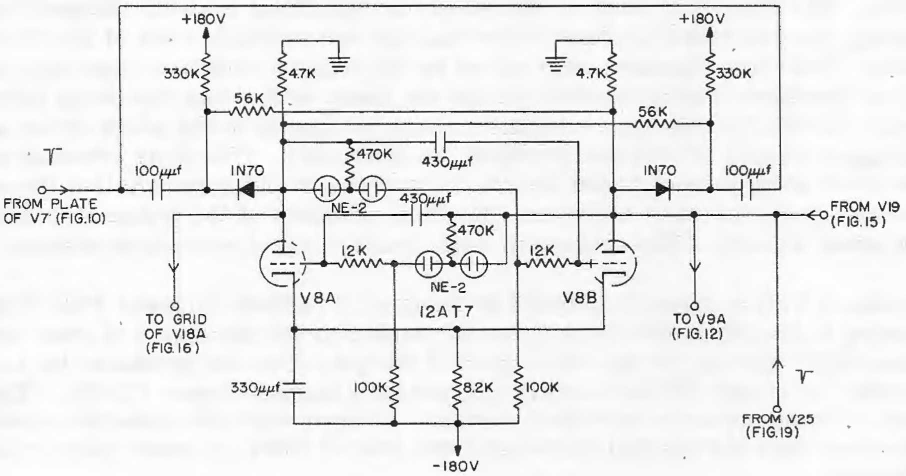


Fig. 11 - Eccles-Jordan 1 circuit

Conventional Eccles-Jordan circuits bypass the common cathode resistor to ground through a large capacitor. This practice allows the use of lower amplitude trigger pulses, and it speeds up the switching time by increasing considerably the internal feedback ratio. Trouble was encountered in the new circuit when much capacitance was introduced in the cathode. This difficulty was traced to tube unbalance; the cathode capacitor forced the cathode to remain at the normal "on" resting voltage for one of the tubes with the result that the cathode capacitor had insufficient time to discharge to the other level during the short trigger pulse. Compensation for this effect is an inherent part of the more

CONFIDENTIAL

DECLASSIFIED

DECLASSIFIED

conventional Eccles-Jordan coupling networks. Extra large compensating capacitors are placed across the plate-grid coupling resistor so that the initial amplitude of the switching signal appearing at a grid is of higher value than the final resting value for that tube. This initial overshoot allows the cathode capacitor sufficient time to discharge or charge to its new voltage level. The neon-bulb couplers have no overshoot, so that other means must be employed to correct this fault. The simplest method is to use a cathode bypass capacitor. of low capacity (330 $\mu\mu$f). The feedback is less, of course, and a larger trigger signal is required. The larger signal was available, and the Eccles-Jordan-circuit rise time was still sufficiently short for the purpose at hand.

In conventional Eccles-Jordan circuits, problems are occasionally encountered when the circuits are to be triggered with pulses of varying widths and amplitudes. A wide trigger pulse, or one of too high an amplitude, can cause the circuit to "misfire" because of an effective equal application of the trigger pulse to each plate. A circuit has been designed to eliminate this difficulty when using trigger pulses in a wide range of widths and amplitudes. A resistive coupling network connected between the plate of one tube and the trigger-diode cathode in the other plate circuit effectively places a reverse bias on the crystal which should not conduct with the application of the next trigger pulse. This bias is placed on one crystal at a time so that the trigger signal is sent only to one plate of the tube, whereas a wide trigger pulse in a conventional circuit is sent to both plates with almost equal amplitude. Separate coupling capacitors are employed to connect the trigger pulse to the diodes. The bias on a diode at the instant of switching is itself changed; however, this switching process takes a longer time than the commutation time of the Eccles-Jordan circuit itself. The time constant determined by the trigger coupling capacitor and the impedance of the diode bias network controls the speed with which the diode bias voltage is switched. As long as this time constant is long compared to the width of the widest expected trigger signal, the circuit functions as described. This time constant must, of course, be short with respect to the length of the shortest pulse period that the equipment is to measure. In the present equipment, the time constant of the trigger-coupling bias circuits is about 4 μsec. (The equipment will measure pulse periods as short as 10 μsec.)

The plate of V8B is directly coupled to the grid of cathode follower V9A (Fig. 12). The gate appearing at the V9A cathode is directly coupled to the third grid of gate tube V10. The clock pulses which are sent to the other grid of the gate tube are produced by a standard Pierce crystal oscillator (V11A) and are clipped by a biased clipper (V11B). The oscillator employs a temperature-controlled crystal. A small variable capacitor enables the operator to zero-beat the crystal frequency with that of WWV or some other reliable frequency standard.

Whenever a positive-polarity gate appears on grid 3 of V10, clock pulses are allowed to pass through the tube and on to the counters. Figure 13 shows one of the standard preset counters (Model 730 A - Berkeley Scientific Corp.) that has been rewired to operate in this equipment. The clock pulses from V10 run a 1-Mc decade counter (Model 1706 - Laboratory for Electronics) which in turn runs the first preset counter. Three more identical preset counters follow the first, giving five readout digits in all. These preset counters, being originally designed to operate at a maximum repetition rate of 40 kc, have been modified to operate at 100 kc (the 1-Mc counter puts out pulses every 10 μsec). The only parts of the counter circuit that needed redesign were the coincidence detectors which are responsible for producing a preset pulse after a given count as set on the pushbuttons. The preset-pulse coincidence circuits operate so that when all the grids of the coincidence triodes (V105 and V106) are driven negative, a positive-polarity pulse appears at their common plate terminal. Because of the finite time lags in the counter circuits, the waveforms associated with a certain count and those produced by the counter Eccles-Jordan

DECLASSIFIED

DECLASSIFIED

[redacted]

UNCLASSIFIED

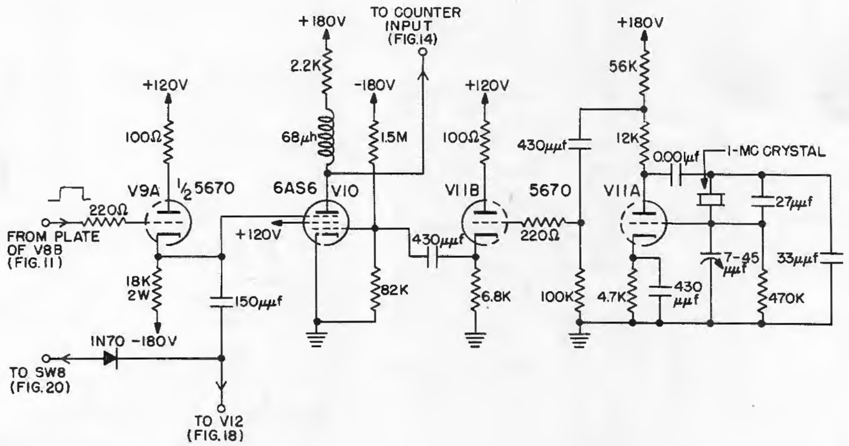


Fig. 12 - Gater 1 and clock circuits

circuits do not occur simultaneously. The time lags between such occurrences run as high as 1 μsec. It was found that for certain pushbutton settings, these time lags produced extraneous preset pulses that occurred before the desired one. For instance, suppose that pushbutton number 7 was depressed, thereby allowing the signal from the first and the last Eccles-Jordan circuits (V101 and V104) to operate the coincidence detectors. At the first instant when the grids of coincidence detectors V105A and V106B are both negative (count of 7), a positive-polarity step voltage appears at the common coincidence-detector plate terminal. However, suppose that at some time prior to the arrival of the desired count a situation existed in which one grid was positive and the other negative. Suppose that on the next count to arrive the relative voltages on these two grids are interchanged with the positive grid going negative and the negative one going positive. Furthermore suppose that the positive grid is sent negative a fraction of a microsecond before the negative one rises. During that period between transitions, both grids are negative simultaneously, thus producing a premature positive-polarity pulse at the common plate terminal of the coincidence detectors. This situation actually exists, and it is the purpose of the crystal-capacitor coupling circuits to minimize the length of this extraneous preset pulse. The capacitor acts to speed up the positive grid excursions, while the series crystal nullifies the effect of the capacitor on the downward swing. The extraneous pulses are made shorter, and a small amount of integration placed in the preset output lead destroys what is left. The only other change that has been made with respect to the coincidence detectors is that the negative grid-return voltage has been changed from 150 to 125 volts. This also helps the positive-going grid to get into the conducting region sooner than it otherwise would.

The other modification made in the preset counter circuit is the addition of four silicon diodes in the neon-bulb lighting circuits. As explained earlier (pages 6, 7, and 8) it is necessary to turn off the neon indicator bulbs during actual counting. The silicon diodes permit the bulbs to be turned off without affecting the normal functioning of the counter circuit itself.

[redacted]

DECLASSIFIED

DECLASSIFIED

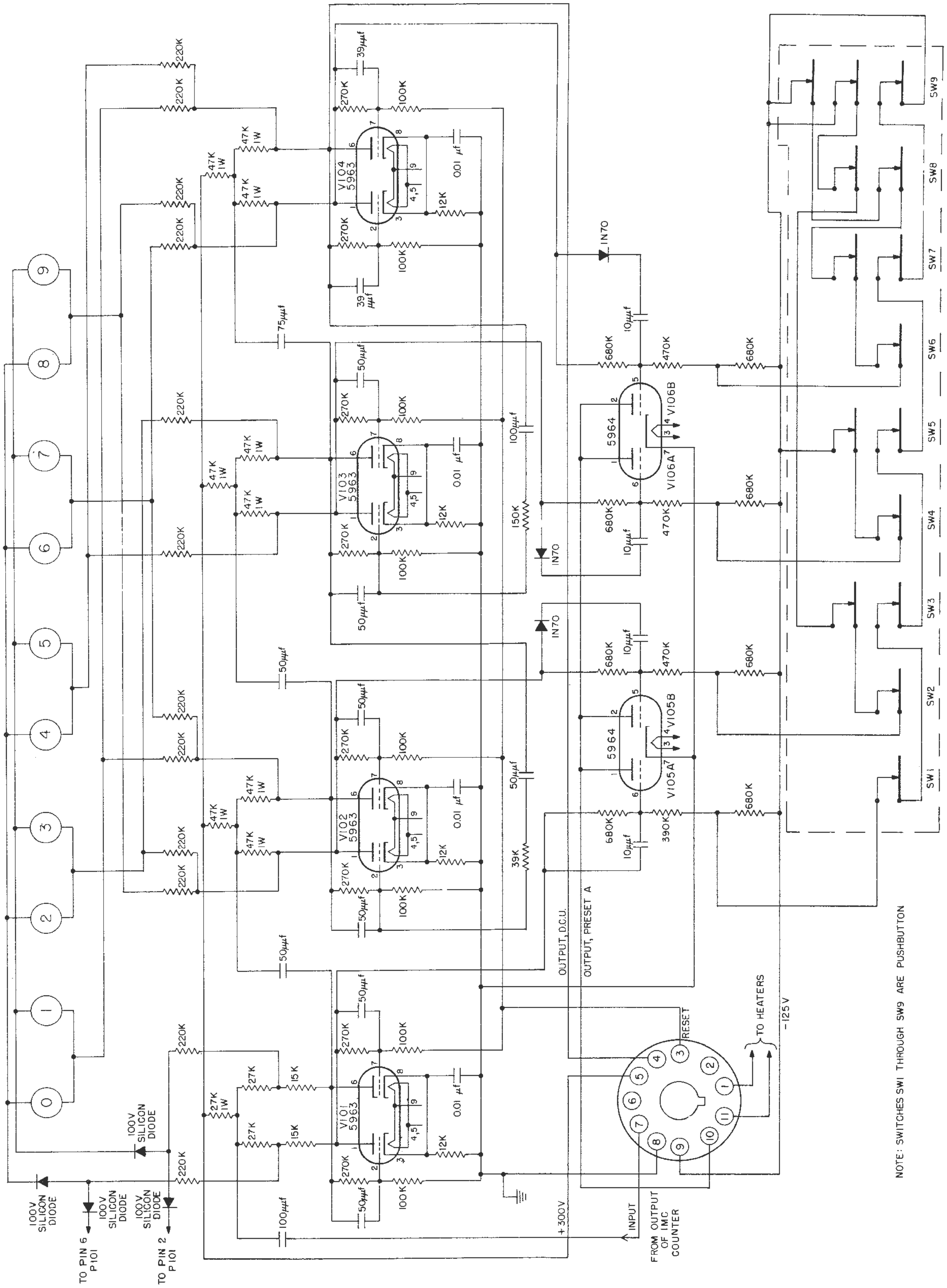


Fig. 13 - Modified circuit of Berkeley Model 730A preset counter

[redacted]

DECLASSIFIED

UNCLASSIFIED

Figure 14 shows the circuits that connect together the preset counters and provide the final preset output pulse. It also shows the mechanism used to switch on and off the neon-bulb count indicators. With respect to the preset pulse circuit, the preset output pulse from each counter is connected via diode to a common preset line. The diodes allow a positive step voltage to appear on this line if and only if the outputs from all the counters are simultaneously positive. This line is connected to the positive 180-volt supply through a load resistor; it is also clamped to the positive 120-volt line by a crystal diode. This clamping diode keeps a certain minimum current flowing in the load resistor at all times. When the preset line is negative with respect to 120 volts, and when a preset pulse is produced, this minimum current is supplied by the circuit capacities. The result is that the leading edge of the preset pulse has a nearly constant slope (the load resistor acts as a constant current supply) until it reaches the 120-volt level. The diode then clips off the top of the pulse, thereby eliminating the rounding off of pulse tops. Since these pulse tops are used to produce the trigger pulse for the vernier multivibrator, it is important that they be as square as possible. The integrating network mentioned above consists of a 100-$\mu\mu$f capacitor which shunts the 18K load resistor.

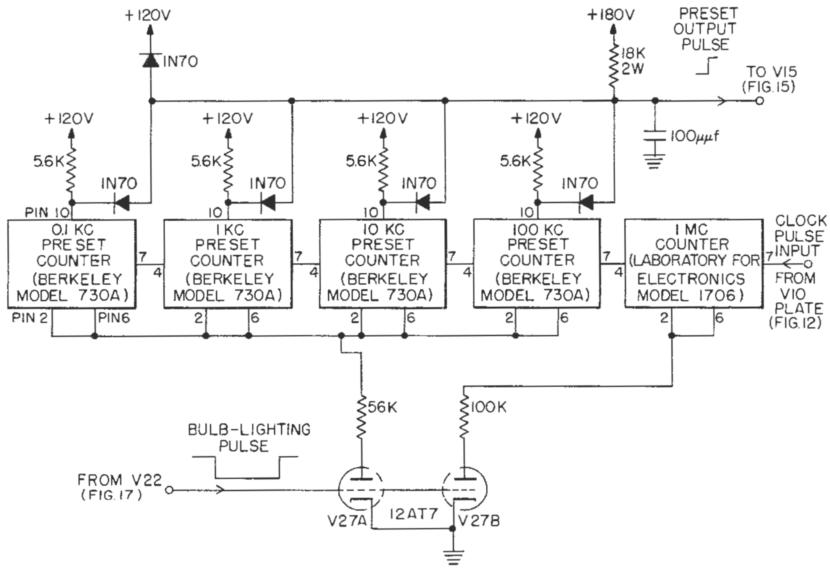


Fig. 14 - Combined counter circuits

It will be noted (Fig. 13 and 14) that all the lines running to the neon-bulb switching networks are joined together and connected to the plate of a triode switch tube V27A. Whenever the grid of this tube is positive (Fig. 14) the plate is pulled negative, cutting off the series diodes (Fig. 13) that supply the lighting current to the neon bulbs. The resultant voltage drop that appears across the series diodes does not affect the counter circuit because of the 220K series isolating resistors that connect the bulbs to the Eccles-Jordan plate circuits. A negative voltage (cutoff) on the V27A grid allows the bulbs to light in the normal manner, while a positive voltage on the grid extinguishes them. Because the voltages measured in the neon-bulb circuits of the 1-Mc counter are much higher than those present in the preset units, a separate neon-bulb switching tube V27B is used for the 1-Mc unit. This procedure precludes unnecessarily high voltages across the back impedances of the silicon diodes. It is necessary that the diode reverse current be kept as low as possible; this is the reason silicon diodes were used. The back impedance of germanium diodes is sufficiently low that the neon bulbs are able to light on the reverse current alone. Silicon diodes correct this fault provided their reverse-voltage ratings are not exceeded. The 1-Mc-counter neon-bulb circuitry is modified in a manner similar to that of the preset counters. However, two silicon series diodes already exist in the neon-bulb supply lines, so that all that is necessary is the addition of the two diodes that couple the series-diode plates to the V27B switching tube.

Figure 15 shows the circuit of gate tube V15 (gater 4), the vernier multivibrator V16, the inclusion-gate multivibrator V19, the preset lockout circuits, and Eccles-Jordan circuit V17 (ECJ 3). Positive-polarity pulses from the counter preset output are differentiated and sent to gating tube V15. A ringing circuit in the plate further differentiates the resultant negative-polarity pulse which is used to trigger the vernier multivibrator. The range of this multivibrator-gate width is from about 5 to 20 μ sec, the minimum gate width being set by potentiometer R3. The trailing edge of the vernier gate is differentiated and used to trigger both the V19 inclusion-gate multivibrator and the Eccles-Jordan circuit V17 (ECJ 3). The inclusion-gate multivibrator has two ranges of operation, one for narrow gate widths (3 to 100 μsec) and the other for wide (50 to 1600 μsec). The negative-polarity gate from the cathode circuit is sent back to the video mixer (V26) where it is added to the incoming video signal and sent to the slave-sweep analyzer. The positive-polarity V19B plate gate is sent to coincidence detector 1, and the trailing edge of the gate is differentiated and sent back to V8 where it serves to turn off the clock pulses in the case when no signal pulse fell within the inclusion gate.

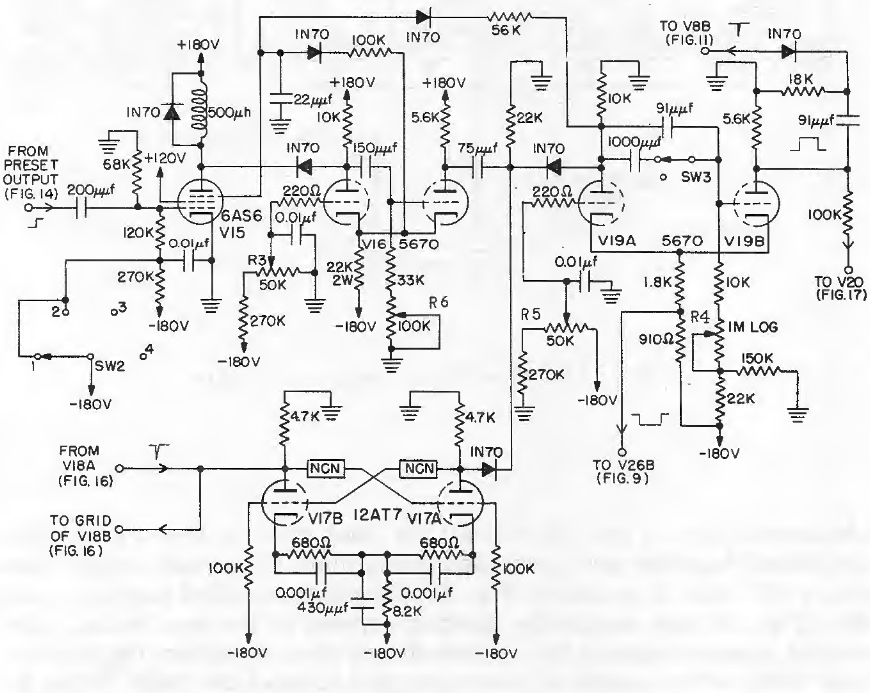


Fig. 15 - Circuit for gater 4, vernier multivibrator, inclusion-gate-multivibrator, preset lockout, and Eccles-Jordan circuit 3

DECLASSIFIED
UNCLASSIFIED

The cathode signal from V16, and the plate signal from V19A are added together in a crystal adder, and the resultant signal is dc coupled to the gating grid of V15. When either multivibrator V16 or V19 is producing a gate, the V15 gating grid is cut off so that none of the extraneous preset pulses (see page 10) are sent to the vernier multivibrator.

Switch SW2 has four positions, each corresponding to one of the modes of operation of the equipment: Position 1 corresponds to mode 1, etc. This switch cuts off the V15 signal grid so that, for modes 1 and 2 (where the preset features are not used), no preset pulses can trigger the vernier multivibrator and thus upset the circuits.

Eccles-Jordan circuit V17 (ECJ 3) uses the same type neon-bulb coupling networks (NCN) as were employed in the V8 circuit (Fig. 11). This circuit differs, however, from that of V8 in that separate RC networks have been installed in the cathode leads. These networks serve essentially the same purpose as do the overcompensated plate-to-grid coupling networks used in standard Eccles-Jordan circuits. During the conduction period of one of the triodes, a few volts of bias are developed across the 680-ohm resistor in the conducting-cathode circuit. This of course, is not true of the nonconducting triode, so that when commutation takes place, the formerly nonconducting tube automatically finds itself with less negative grid bias than the tube that was conducting. The 0.001-$\mu\mu$f capacitors keep the circuit in this state of unbalance until the voltage across the 8.2K common-cathode resistor has had time to reach its new resting voltage.

The signal from the plate of V17B is directly connected to one grid input of the either-or circuit V18 (Fig. 16). The other grid of V18 is directly connected to the plate of V8A (ECJ 1). The output terminal for this circuit is the common-cathode junction of the two crystal diodes in the V18 cathode circuit. The output voltage rests a little above ground level if either the grid of V18A or the grid of V18B, or both, remain at ground level. However, if both grids are negative, the output voltage is also negative. This output voltage is coupled to the gating grid of V7 (Fig. 10), so that V7 is cut off only if both grids of the either-or circuit are negative. The diode coupling network from the output of V18 to the V7 grid delays the negative-polarity signals at the plate of V7 (which are coupled back to the V7 gating grid through the either-or circuit) so that V7 will not cut itself off before V8 has had time to commutate. Switch SW4 is ganged to SW2 and is used to hold the gating grid of V7 positive for those modes of operation where the gating function of V7 is not utilized. The leading edge of the negative-polarity gate from the cathode of V18A is differentiated and sent to the plate of V17B so that ECJ 3 is reset each time that V8 (ECJ 1) opens the clock pulse gate. A similar pulse is sent to the plate of V21B (Fig. 17) so that V21 (ECJ 4) is reset at the same time. The trailing edge of the V18A cathode gate is differentiated and sent (as a positive-polarity pulse) to the grid of gating tube V20 (Fig. 17). (The inclusion gate is applied to the V20 gating grid.)

Coincidence of a video signal pulse with that of an inclusion gate produces a negative-polarity pulse at the plate of V20. This pulse triggers Eccles-Jordan circuit V21 (ECJ 4). Whenever a coincidence occurs in V20, V21A is triggered and a positive-polarity step voltage appears at the V21B plate and consequently at the V22 grid (coincidence detector 2). The application of the 25,000-μsec bulb-lighting gate (described on page 7) to the gating grid of V22 produces a negative-polarity gate at the V22 plate. This gate is dc coupled to the grid of V27 (Fig. 14), and the neon-bulb indicators are lit throughout the duration of this gate. For mode 3 of operation, the bulbs are lit only when both V22 grids are positive. If a coincidence of signal pulse and inclusion gate does not occur, the bulbs are not allowed to light. When a coincidence does occur, the bulbs are lit for the 25,000-μsec interval. Switches SW5 and SW6 are ganged to SW2 and SW4. For operating mode 1, these switches hold both V22 grids in their positive positions so that the neon-bulb indicators are

[redacted]

DECLASSIFIED

DECLASSIFIED

 [redacted]

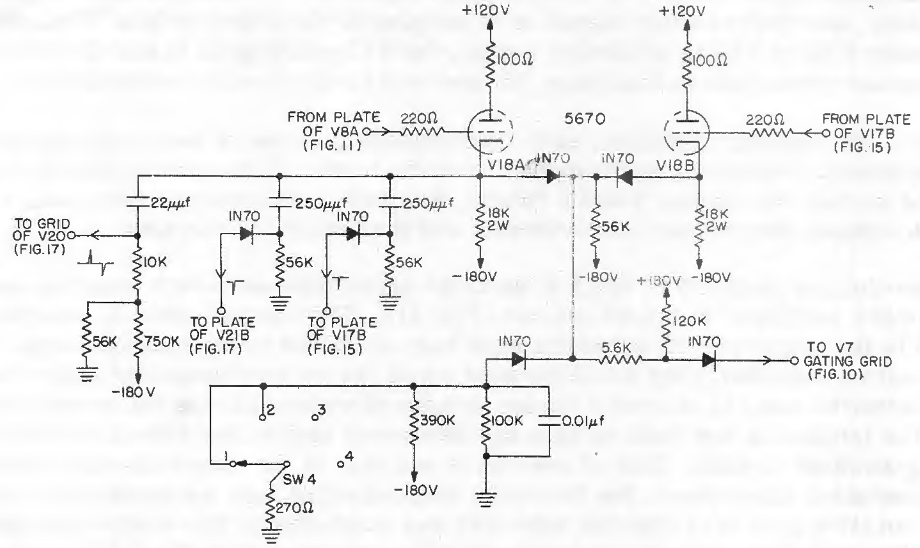


Fig. 16 - "Either-or" circuit 1

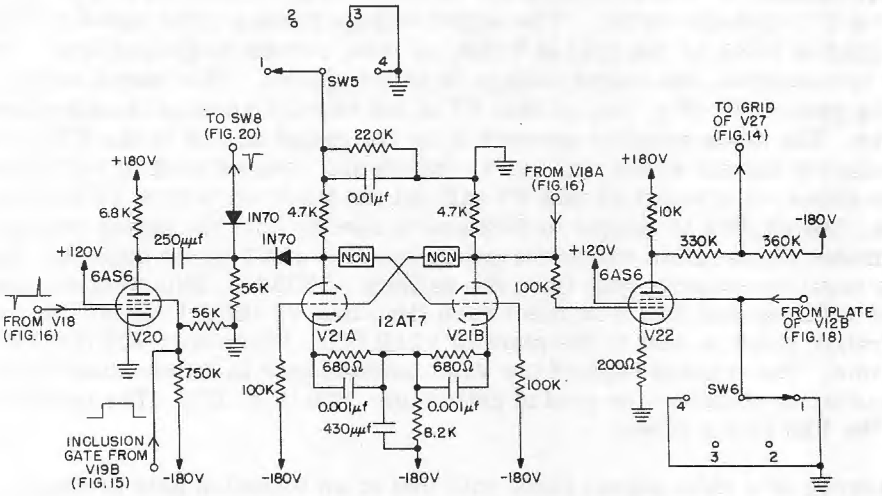


Fig. 17 - Coincidence detector 1, Eccles-Jordan 4, and coincidence detector 2

continuously lit. For operating mode 2, the V22 grid that is connected to V21B is held positive (SW5), and the 25,000-μsec gate alone has control over the neon indicators. Mode 3 has been described above. Mode 4 switches the V22 grid voltages so that the signal from V21B alone switches the neon indicators. (When, and only when, a coincidence occurs are the neon bulbs allowed to light. For mode 4 they remain lit until the start switch is actuated.)

[redacted]

DECLASSIFIED

The two 25,000-μsec multivibrators described on page 7 are shown in Fig. 18. The first multivibrator V12, which gates the neon-bulb switch tube V27 (Fig. 14) via V22 (Fig. 17), is triggered by the differentiated trailing edge of the clock-pulse gate as it appears at the cathode of V9A (Fig. 12). The positive-polarity output gate from the plate of V12B is dc coupled to the grid of the holding triode V9B. The plate of this tube is directly connected to the grid of V13B which is the normally conducting half of the second 25,000-μsec multivibrator. When the positive-polarity gate appears on the holding-tube grid, the plate of V9B and the grid of V13B are lowered from ground level down to a voltage well beyond the normal cutoff voltage for V13B. At the termination of the gate produced by V12, the capacitor which couples the plate of V13A to the grid of V13B is allowed to discharge through the 10-megohm grid resistor. After approximately 25,000 μsec, V13B begins to conduct, and the multivibrator commutates in the normal manner. The high-back-impedance silicon diode in the grid circuit of V13B shortens the multivibrator recovery time. The negative-polarity gate that appears on the V13B cathode has a total duration of 50,000 μsec (Figs. 7 and 8). Switch SW7 in the cathode circuit of V9B is ganged to switches SW2, SW4, SW5, and SW6. It disables the 50,000-μsec output gate when the equipment is operating in mode 1. This is accomplished by returning the V9B cathode to ground potential instead of to a negative voltage, with the result that the grid of V13B cannot be driven below ground. The 25,000-μsec switching gate for the neon indicator lamps is obtained from the plate of V12B and is directly coupled to the grid of V22 (Fig. 17).

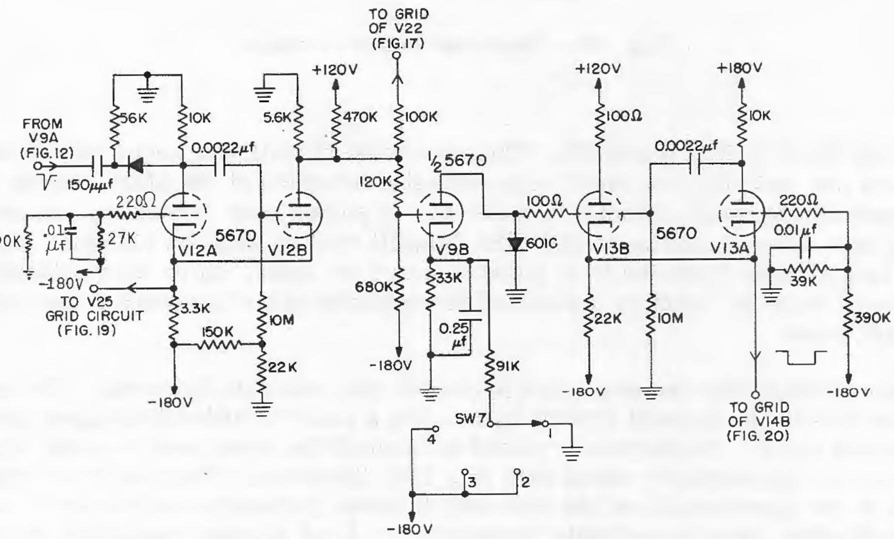


Fig. 18 - 25,000-μsec multivibrators and holding circuit

The start and reset circuits are shown in Fig. 19. Actuation of the start switch applies a negative-polarity pulse to the grid of a Schmitt circuit whose input grid is biased halfway between the two threshold levels. These levels are spaced about 20 volts apart, and a negative-polarity 15-volt pulse switches the circuit in one direction, while a positive pulse switches it in the other. A negative pulse at the input (actuation of start switch) produces a positive-polarity step current in the plate circuit of V24B. A damped ringing circuit differentiates this waveform and produces a narrow negative-polarity voltage pulse which

UNCLASSIFIED

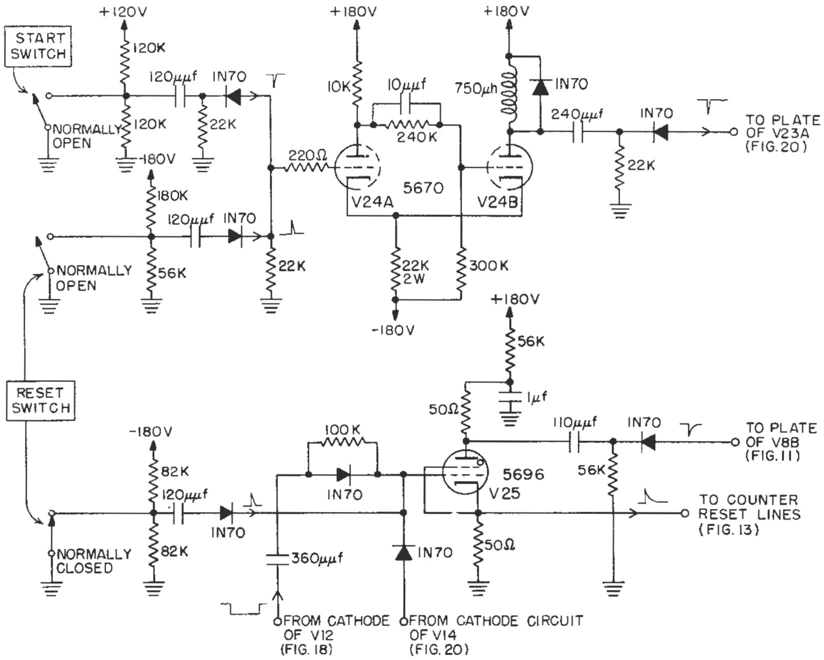


Fig. 19 - Start and reset circuits

is sent to V23 (ECJ 2, Fig. 4 and 20). This elaborate circuit was necessary to assure the production of one and only one start pulse with the actuation of the start switch. Manually operated switches normally produce a multitude of pulses upon actuation; this series of pulses may last several milliseconds. The Schmitt circuit with the clamped inputs produces one output pulse from the first pulse to enter its input. After commutation, the Schmitt circuit must be reset by a pulse of the opposite polarity before it can respond to another start pulse.

The reset switch has two poles and performs two separate functions. The normally open section resets the Schmitt circuit by sending a positive-polarity trigger pulse to the Schmitt-circuit input. The normally closed section of the reset switch sends a positive-polarity pulse to the normally cutoff grid of a 5696 thyratron. The positive trigger pulse on the grid of the thyratron fires the tube which draws instantaneously about 1 ampere through the 50-ohm cathode and plate resistors. A 1-μf storage capacitor in the plate circuit provides the necessary current. When this capacitor has been discharged, the thyratron grid regains control, and the 1-μf capacitor recharges to 180 volts through the 47K series resistor. The high discharge current through the thyratron produces 50-volt pulses across the plate and cathode resistors. The pulse from the cathode is used to reset the counters. The negative-polarity pulse from the plate is sent to the plate of V8B (Fig. 11) where it serves to close the clock-pulse gate in the case that all the circuits come to rest with V8 set in the wrong direction.

In the two automatic modes of operation, the reset trigger pulse is obtained from the trailing edge of the first 25,000-μsec multivibrator gate. The V12 cathode gate is differentiated and sent to the grid of V25. The crystals in the grid leads allow either type of reset signal to reset the thyratron without having to drive the source impedance of the other. Bias is derived from a tap on the V14A cathode resistor (Fig. 20).

DECLASSIFIED

[redacted]

UNCLASSIFIED

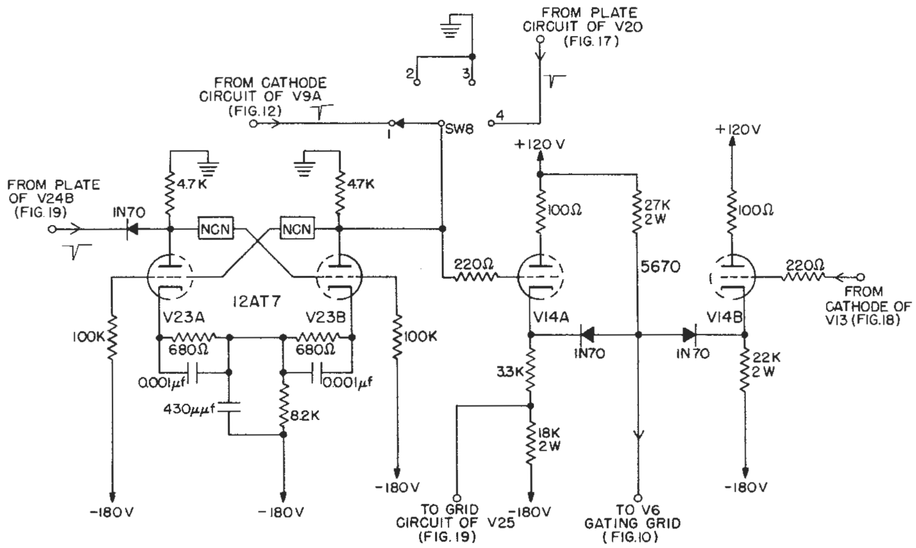


Fig. 20 - Eccles-Jordan 2 and "either-or" circuit 2

Figure 20 shows V23 (ECJ 2) and V14 ("either-or" circuit 2). The functions of these circuits were described in connection with Figs. 4 and 8. For operating mode 1, V23 is used to turn off V6 (gater 2) with the arrival of the second video signal pulse. For operating mode 4, both the V23 signal and the V13 cathode signal can cut off V6 through V14. "Either-or" circuit V14 is similar to that of V18 (Fig. 16), the only difference being that the crystals have been reversed. Thus a negative-polarity signal on either or both grids produces a negative-polarity signal at the output terminal, but both grids must be positive for the output to be positive. The negative-polarity 50,000-μsec gate from the cathode of V13 is directly connected to the grid of V14B, while the output signal from V23 is directly coupled to the grid of V14A.

For operating mode 1, V14A simply serves as a cathode follower to dc couple the output from V23B to the grid of V6. Under these conditions switch SW7 disables multivibrator V13 (Fig. 18) so that no signals reach the grid of V14B.

For operating mode 2 or mode 3, SW8 (ganged to SW2, SW4, SW5, SW6, and SW7) disables V14A, and V14B serves as a straight cathode follower to convey the V13 cathode signal to the V6 gating grid.

The tap from the V14A cathode resistor is directly coupled through a diode to the grid of the reset thyratron (V25, Fig. 19). This feature automatically provides lockout of the last thyratron grid trigger pulse when the equipment is operating in mode 4. As was described on page 11, the counter neon bulbs are not allowed to light until a video pulse falls within the inclusion gate. The circuits automatically count and reset themselves until a video pulse does fall within the gate. When this happens, the neon bulbs light and must stay lit until the reset and start switches are manually actuated. Thus the last reset pulse from the V12 cathode must be prevented from reaching the thyratron grid. This is accomplished by effectively raising the negative grid bias on V25 as soon as a signal pulse is

[redacted]

DECLASSIFIED

DECLASSIFIED

coincident with an inclusion gate. When the coincident signal pulse arrives, V23 is triggered to close gate tube V6. The cathode of V14A is simultaneously driven negative, with a consequent raising of the negative grid-bias value. When the differentiated trailing edge of the first 25,000-μsec gate arrives, it has insufficient amplitude to overcome the added negative bias on the V25 grid. As a result, the thyratron is not fired, and the final count remains on the neon-bulb indicators. However, the pulse from the manually operated reset switch has sufficient amplitude to override this bias so that the counters may be manually reset at any time.

Plate 1 at the end of this report is a complete schematic diagram of the final equipment.

EARLY EQUIPMENT

Prior to the construction of the equipment described above, another model was built upon which tests were run. It was quite similar in operation to that of the final model. The major difference was the method of generating the inclusion gate. No preset counters were used; the inclusion-gate delay was instead generated by multivibrators whose gate widths were manually adjusted by a potentiometer. A signal pulse initiated the delay gate, during which no additional pulses were allowed to enter the equipment. At the termination of this delay gate, the inclusion gate allowed pulses to enter until its termination.

Trouble arose in connection with the design of suitable delay multivibrators. Their stability left much to be desired, and the calibration of the gate-width potentiometer was not dependable to better than a few percent. Consequently, the inclusion-gate delay could not be set accurately without the aid of a slave-sweep analyzer display. It was found that with noisy signals, the position of the inclusion gate in such a display could not be read. Also the multivibrators were duty-cycle sensitive, their gate lengths changing as much as 2% with signal pulses of different repetition rates. For these reasons preset counters were advocated, and their incorporation has been fully justified. The inclusion-gate delay is now as stable as the crystal oscillator itself.

Other troubles occurred with respect to the many dc-coupling networks in the circuits. The Eccles-Jordan circuits of new design (Fig. 11) solved these problems. Certain troubles that were traced to crystal diodes have been alleviated by the installation of silicon-junction diodes, which were not generally available at the time the previous model was built. Use of silicon diodes also eliminated the necessity for four dual-triode vacuum tubes.

OPERATION OF FINAL EQUIPMENT

The control panel of the completed equipment is shown in Fig. 21. The panel controls from left to right are VIDEO GAIN (R1), VERNIER GATE (R6), INCLUSION GATE (R4), FUNCTION SWITCH (SW 2, 4, 5, 6, 7, 8), START switch, and RESET switch. The decimal counter units with their respective preset pushbuttons occupy the upper half of the panel. Two connectors are available at the rear of the chassis; one is the video input jack, and the other may be connected to the input of an AN/SLA-2 or APA-74 pulse analyzer.

Before attempting to operate the equipment, the operator should calibrate the visual pulse analyzer so that he can estimate the amplitude of the signal voltage entering the equipment. It will be remembered that for proper operation of the Schmitt noise-slicing circuit (see pages 12 and 13) the video input signal should have an amplitude of about 20 volts by the time it reaches the output stage of the video amplifier. The video gain control

[redacted]

DECLASSIFIED

DECLASSIFIED

CONFIDENTIAL

UNCLASSIFIED

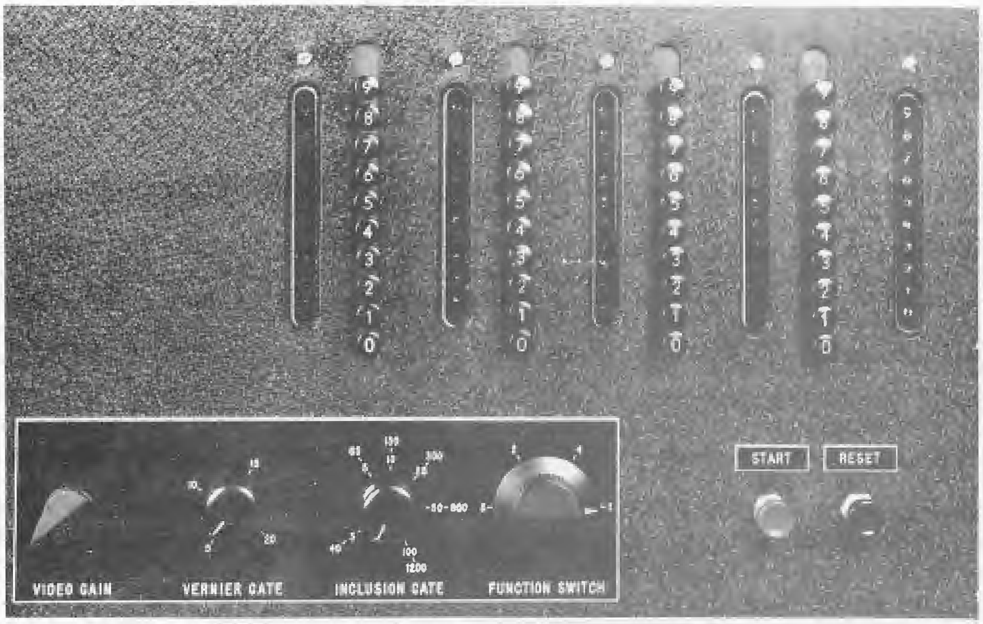


Fig. 21 - Control panel view

of the slave-sweep pulse analyzer should be set at about 3/4 maximum gain setting. With a video signal applied to the input of the pulse-measuring equipment, and with the slave-sweep pulse analyzer connected to the proper output connector, the signal amplitude appearing at the Schmitt circuit grid should be adjusted by means of the GAIN control until it reaches 20 volts in amplitude. (This voltage may be measured by connecting a calibrated oscilloscope to the input grid of the Schmitt circuit.) The slave-sweep analyzer gain control should then be adjusted so that the displayed signals have an amplitude of about 5/8 inches. The slave-sweep analyzer gain control is then locked, and the operator knows that if the GAIN control is adjusted to give a 5/8-inch deflection, the video signal will reach the Schmitt noise slicer with the proper amplitude.

For operation mode 1, the FUNCTION switch is set to position 1, and the VIDEO GAIN control is adjusted to give a 5/8-inch deflection on the pulse analyzer display. The reset button is actuated to "zero" the counters. The START switched is pushed. When the count is completed, the final count in microseconds may be read off the 5-decade scales. To take another reading, the operator resets the counters and again pushes the START switch.

If it is desired to have a continuously running display of the current count (mode 2), the FUNCTION switch is set to position 2. All the resetting and starting is done automatically, and the count is flashed on the scales at a maximum rate of 20 times per second. By noting which of the numbers flash consistently and which ones flash more or less randomly, the operator can quickly give an intelligent guess as to the percentage jitter in the signal pulse. If for instance the numbers in the first four columns (from left to right) flash consistently 3-3-4-6, and the last digit has a maximum variation between 2 and 8, then the maximum jitter would be about 6 parts in 33,460, or about 0.018%.

If the signal is very noisy, modes 3 and 4 will be used almost exclusively. To operate in mode 4, the FUNCTION switch is set to position 4, and the pulse analyzer display is examined to determine in what general range of pulse periods the signal pulse falls. Suppose

CONFIDENTIAL

DECLASSIFIED

DECLASSIFIED

 [redacted]

the operator suspects that a signal exists with a period in the vicinity of 2000 μsec. To set up a 500-μsec inclusion gate about this mean value, the operator depresses pushbuttons 0-1-7-5 and sets the inclusion gate to a width of 500 μsec. By pushing the start switch, a count may then be obtained. By listing several of these results, the operator may then examine the figures and see if there is any interval in the 500-μsec inclusion-gate range in which the readings were most numerous; if there is, the operator narrows down the inclusion gate to include only that interval in which a majority of the counts fell. If after the next series of readings there is a definite bunching of the readings about some point in the new interval, the inclusion gate may be narrowed to a new value and the process repeated. This procedure may be continued until the consistent bunching of the readings within the inclusion gate can barely be detected. When this point is reached, the operator can only say that the signal pulse lies somewhere in this inclusion-gate interval. In order to determine a figure for the jitter of the video-pulse signal in the presence of noise, more information is needed in addition to the histogram of individual readings. This matter will be discussed further in Appendix A.

Operating the equipment in mode 3 is accomplished by setting the function switch to position 3 and utilizing the pushbuttons as in mode 4. The readings will then be flashed on the neon-bulb indicators automatically at a maximum rate of 20 times per second.

It will be noted that the VERNIER GATE range is 5 to 20 μsec instead of 0 to 10 μsec. Because of inherent delays in the preset-counter circuits, the preset pulse may at times occur up to 5 μsec after the time as set on the pushbuttons. Thus if the operator wished to set a 5-μsec inclusion gate around a pulse having a period of 2003 μsec, he would find by pushing buttons 0-2-0-0 that the inclusion gate would open at 2010 μsec after the first signal pulse entered the equipment.* To have the signal pulse fall within the inclusion gate, the pushbuttons must be set to 0-1-9-9 and about 5 μsec added by the vernier multivibrator to the inherent 5-μsec delay. The 5-μsec inclusion gate would then be approximately centered on the 2003-μsec pulse.

CONCLUSIONS AND RECOMMENDATIONS

In several preliminary tests (Appendix B), this equipment has proved capable of measuring under conditions of extreme interference the repetition rates of pulse signals to within 1 μsec. It is the only known existing equipment that can accurately perform the pulse-period measurements under such adverse conditions.

It is recommended that this equipment be considered for applications which require the measurement of pulse periods with great accuracy. It is felt that the equipment represents a satisfactory solution to the original problem.

ACKNOWLEDGMENT

Acknowledgment is hereby made to William F. Hoffmann who designed, constructed, and tested the preliminary equipment described in the first section of this report.

---

*2000 μsec plus the 5-μsec delay plus the 5-μsec minimum width of the vernier gate gives a total of 2010 μsec.

* * *

[redacted]

DECLASSIFIED

[redacted]

DECLASSIFIED

UNCLASSIFIED

APPENDIX A
Statistical Theory of Individual Count Distribution

In order that the operator of this equipment be able to interpret the data he has collected, a short treatment of the method of handling such data follows. In this treatment it shall be assumed that, with the exception of repetitive interfering signals that can be eliminated by proper placement of the inclusion gate, all interference is in the form of random Gaussian noise. The signals that the equipment is to analyze are obtained at the output terminal of a wideband video receiver. The original white noise that entered the receiver has been first-bandwidth limited and then rectified by a detector or switch having the following transfer characteristic. $E_{out} = 0$ when $E_{in} < 0$; $E_{out} = E_{in}$ when $E_{in} > 0$.

The amplitude distribution of the peaks of pure white noise that has been bandwidth limited is Gaussian as shown in Fig. A1. Both positive and negative peaks are equally likely so that the probability-distribution curve is symmetrical about zero amplitude. The equation for this curve is

$$p = \frac{1}{\sigma\sqrt{2\pi}}\, e^{-E^2/2\sigma^2}$$

where E is the amplitude and σ is the standard deviation of the distribution. The probability that during a time interval $1/2W_0$ (where W_0 is the center frequency of the bandpass filter), the peak amplitude of the noise will lie in some amplitude region ΔE is found by integrating p between the upper and lower limits of ΔE.

If this Gaussian noise is then rectified by the switch having the above-mentioned transfer characteristic all negative-polarity peaks are eliminated and the positive ones remain unaltered. The probability-distribution curve for the peak amplitude of this rectified signal is simply the right-hand half of the normal Gaussian curve with a delta function of area 1/2 at the origin (Fig. A2). The delta function takes care of the fact that the rectified signal has a value of 0 half of the time. Suppose we now integrate this signal by passing it through a video amplifier of center frequency much lower than that of the circuits preceding the rectifier. In a typical receiver, the center frequency of the i-f strip is about 160 Mc. The effective center frequency of the video amplifier following the detector is of the order of 3 to 4 Mc. The video amplifier thus integrates out the 160-Mc carrier, and in doing so it changes the probability-distribution curve for the instantaneous amplitude of the noise. The resulting distribution curve is known as a Rayleigh distribution. If there is no signal present in the system, then the probability distribution appears as in Fig. A3. The most probable value of peak voltage no longer lies in the region near zero amplitude. Because the video amplifier has integrated the positive-polarity noise peaks, the envelope is all that is left, and the envelope rarely goes to zero. The most probable value of envelope voltage now lies in a region close to the rms value of the noise.

If there is a signal present in the receiver, then the probability distribution of the noise peaks about the instantaneous signal level is changed. The higher the signal-to-noise ratio, the more the Rayleigh distribution approximates that of a normal Gaussian distribution. Figure A4 shows the amplitude probability distribution of the envelope for five different signal to noise ratios.

With these figures in mind, let us consider the case of an actual signal situation. Suppose the signal to be examined has one of two characteristics (Fig. A5): either it has fast

[redacted]

DECLASSIFIED

DECLASSIFIED

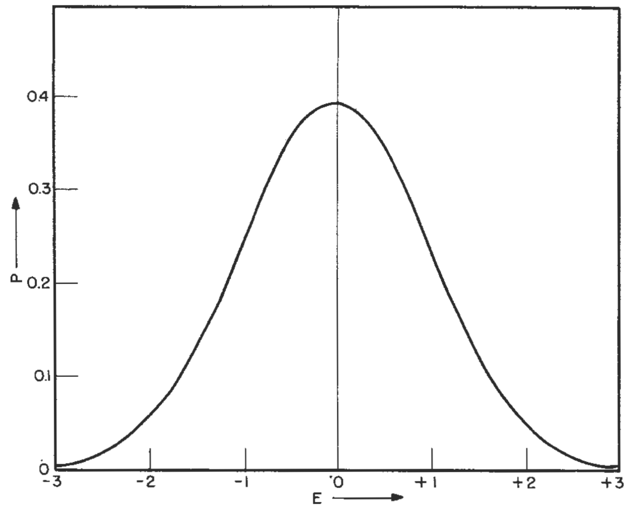


Fig. A1 - Gaussian noise distribution

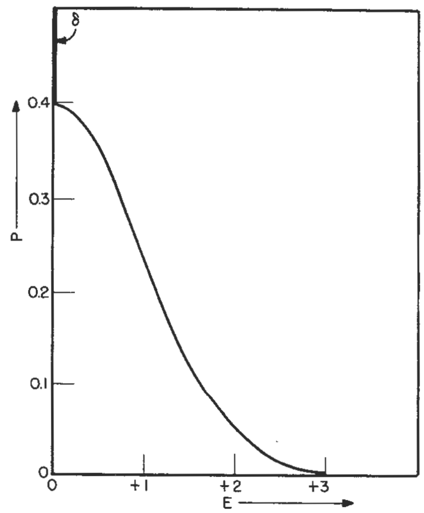


Fig. A2 - Rectified Gaussian noise distribution

rise time (of the order of the rise time of the video amplifier), or it has a slow rise time. If the signal of period T_0 is free from noise and jitter, the distribution of individual period counts in the inclusion-gate interval will appear as in Fig. A6. (There may be a quantum jump of 1 μsec, but never more than 1 μsec.) All the readings will be correct to within 1 μsec of the period T_0, regardless of the type of pulse. Next, suppose that a fast-rise-time pulse enters the system along with a certain amount of random noise. The histogram of the distribution (taken and normalized over many readings) might appear as in Fig. A7. The most likely reading may not be one corresponding to T_0, but because a signal pulse does enter the equipment at every T_0, there will be a sharp change in the distribution in the vicinity of T_0. The gradual distribution trend throughout the inclusion-gate interval

[redacted]

DECLASSIFIED

UNCLASSIFIED

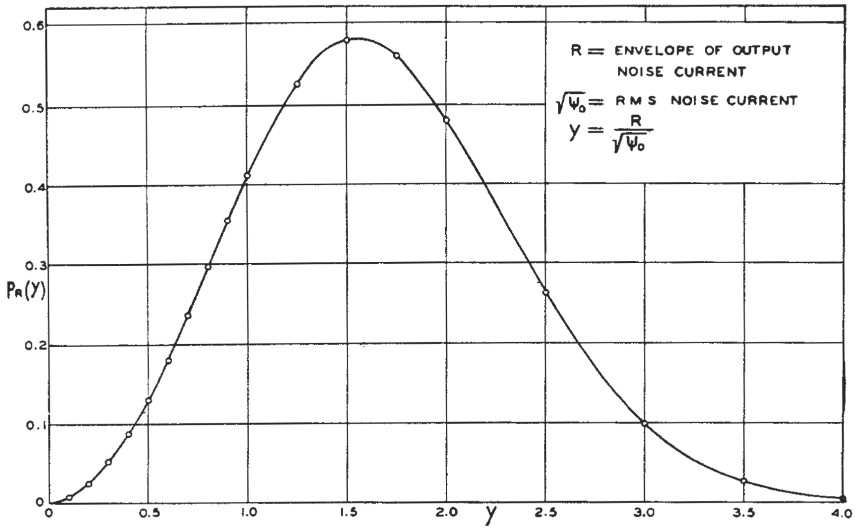


Fig. A3 - Distribution of maxima of envelope of noise current. Noise through ideal bandpass filter.
(taken from S. O. Rice, BSTJ, Vol. 24 (No. 1) p. 85, January, 1945)

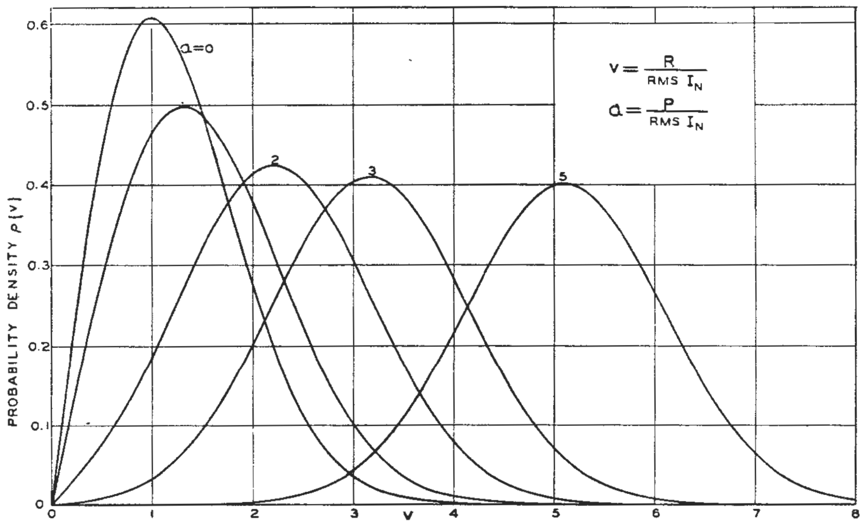


Fig. A4 - Probability density of envelope R of I(t) = P cos pt + I_N
(taken from S. O. Rice, BSTJ, Vol. 24 (No. 1) p. 102, January, 1945)

is determined by the nature of the noise and should be distinguished from the sharper peak in the distribution curve caused by the signal itself. With low-level noise (Fig. A7a), the distribution of non-signal counts will be relatively linear throughout each half of the inclusion-gate interval. (The existence of a regular pulse appearing at T_0 lowers the amplitude of the histogram throughout that part of the inclusion gate that follows the occurrence of the signal pulse.) With high-level noise (Fig. A7b), the non-signal counts will bunch nearer the beginning of the interval. In most cases the signal will produce a sharper hump than that produced by the noise distribution alone.

[redacted]

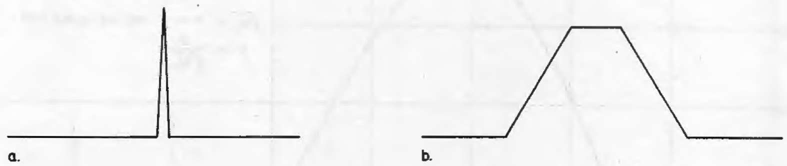


Fig. A5 - Typical pulse signals

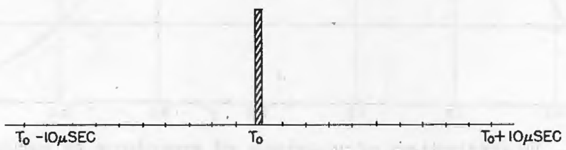
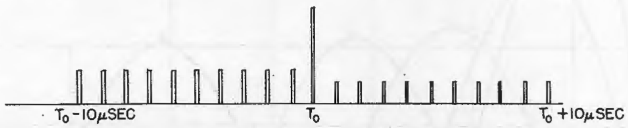
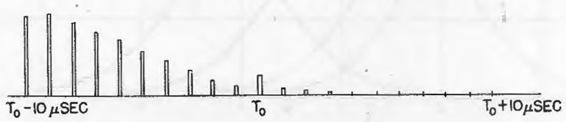


Fig. A6 - Histogram of measured period of noiseless signal



(a) - Low-amplitude noise



(b) - High-amplitude noise

Fig. A7 - Histogram of measured period of noisy signals

[redacted]

DECLASSIFIED

UNCLASSIFIED

Suppose that we have under noiseless conditions a repetitive pulse of one of the types shown in Fig. A5. If the pulse period is modulated with a random jitter, the pulse-period distribution curve might appear as in Fig. A8. Its maximum point is defined as T_0. Now if noise is added to the above picture, and if the pulse under examination has a fast rise time, the resulting distribution curve might appear as in Fig. A9.

Next let us assume that the signal to be examined consists of a fast-rise-time pulse followed by a slow-rise-time pulse (Fig. A10). Suppose it is desired to measure the time interval between the initiation of the fast-rise-time pulse and some point on the leading edge of the following slow-rise-time pulse. The noise-slicing Schmitt circuit triggers automatically at points of equal potential on the leading edge of each pulse. Assume that the level of the noise is sufficiently low so that the fast-rise-time pulse is able to start the count for most of the experiments. The question then arises as to what point on the leading edge of the second pulse the Schmitt circuit is most likely to trigger. The answer is not T_0, but a time interval shorter than T_0 whose length depends on the signal-to-noise ratio, the rise time of the pulse, and the bandwidth of the equipment. Figure A11 is a plot of the probability distribution of trigger points along the leading edge of a pulse having a rise time to normal trigger level of 10 μsec; the bandwidth of the video amplifier is about 4 Mc, the normal trigger voltage is 9 volts, and the rms noise voltage is 3 volts. This curve may be easily plotted by using a table of values for the integral

$$I = \frac{1}{\sqrt{2\pi}} \int_{-E}^{+E} e^{-\frac{\alpha^2}{2}} .$$

It will be noted that the probability of triggering at time T_0 or after is extremely small. In order to give an accurate figure for the time elapse between equipotential points on the leading edge of each pulse, the noise on the signal must be taken into account and an appropriate number of microseconds added to the answer given by the actual readings.

If the signal being examined consists of a repetitive pulse of slow rise time, the probability distribution of trigger points for the pulse which initiates the count must be taken into consideration as well as that for the pulse which terminates the count. If the noise is of low level, so that there is small likelihood of starting a count at any time other than with the arrival of a signal pulse, the distribution of the individual count readings will be a symmetrical curve with a maximum at T_0. The standard deviation of the resultant curve is approximately $\sqrt{2}$ times that of the curve shown in Fig. A11 for a single pulse of slow rise time. If the signals are being received under conditions of low noise, then the operator can decide from the plot of his readings whether there is jitter on the signal in addition to noise. If the standard deviation of his plotted curve is much greater than 1.414 times that of the corresponding theoretical curve (of which Fig. A11 is an example) then he assumes that there is jitter modulation on the signal itself. The square of the jitter standard deviation is equal to the square of the standard deviation of his plotted curve minus the square of 1.414 times the standard deviation of the theoretical jitterless curve for the existing conditions.

$$\sigma^2_{\text{jitter}} = \sigma^2_{\text{plotted}} - \sigma^2_{\text{theoretical}}$$

Of course, this type of calculation is not very useful for very noisy conditions. With high noise levels, the amplitude of the probability-distribution curve is much greater in the time region between pulses. The probability distribution for triggering on the first signal pulse is then quite different from that of triggering on the second pulse which is enclosed by an inclusion gate. The resulting histogram may be far from symmetrical, and

[redacted]

DECLASSIFIED

DECLASSIFIED

 [redacted]

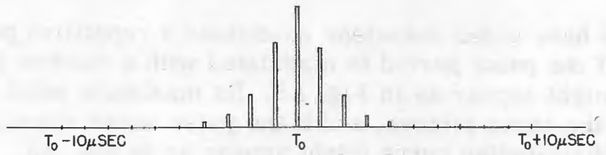


Fig. A8 - Histogram of measured period of noiseless jittered signal

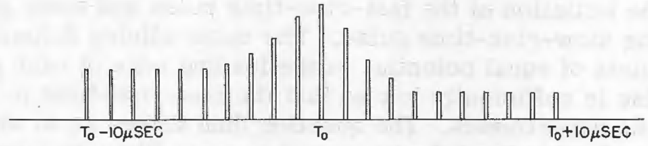


Fig. A9 Histogram of measured period of noisy jittered signal

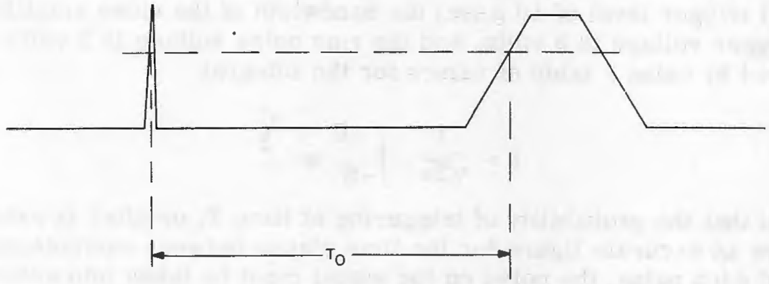


Fig. A10 - Typical two-pulse signal

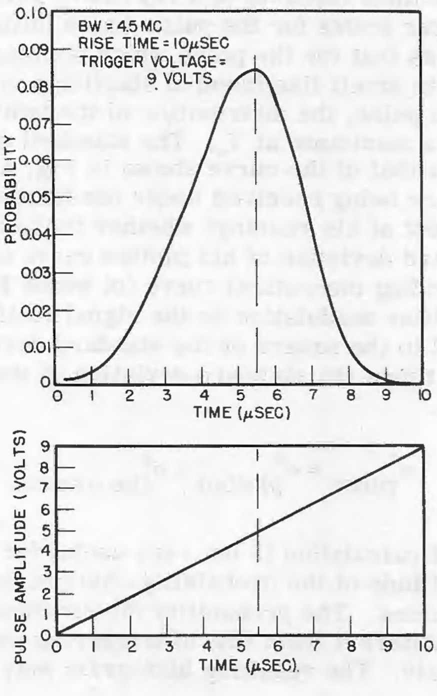


Fig. A11 - Trigger-point probability

[redacted]

DECLASSIFIED

DECLASSIFIED

UNCLASSIFIED

the resulting standard deviations will be quite meaningless. If the operator finds the individual readings bunching about some point in the inclusion gate, he should next shift or widen the gate a little and see if the readings bunch at the same point. If throughout the procedure of narrowing and widening the gate, the readings continue to bunch about the same point, then and only then is the authenticity of the signal proved. Bunching of readings may appear simply as a result of the noise distribution itself, but their points of high density will vary in time with adjustment of the width and delay of the inclusion gate. If, for instance, the operator finds that definite bunching of readings occurs within 50 μsec after the initiation of the inclusion gate for any arbitrary setting of the delay pushbuttons, then the bunching simply represents the fact that the occurrence of noise pulses in the above case is most likely within 50 μsec after the inclusion gate opens.

The above discussion is an attempt to predict the general behavior of the equipment under noisy signal conditions. Many simplifying assumptions were made for ease of explanation, but it is the opinion of the author that the assumptions made were not so far from reality that the over-all picture would be greatly changed. Extensive field testing will eventually be the critical test of the above conclusions.

* * *

[redacted]

DECLASSIFIED

DECLASSIFIED [redacted]

APPENDIX B
Preliminary Test Results

Below are the results of a few preliminary tests on actual loran pulse signals. A block diagram of the equipment used for this experiment is shown in Fig. B1. The source of loran signals was a modified National RA0-9 receiver. The receiver was tuned to the 2000-kc channel, and a photograph of the signals as they appeared on a 5-gun analyzer display is shown in Fig. B2. Loran pulses of periods 29,300, 29,400, 29,600, 29,800, and 30,000 μsec were identified immediately and logged within 1 μsec. The loran signal at 29,700 μsec was much weaker and subject to severe fading. A histogram of the pulse-period readings using mode 3 of operation is shown in Fig. B3a. A 100-μsec inclusion gate centered on 29,700 μsec was used. Bunching of the readings in the vicinity of 29,700 μsec was established, and the pushbutton delay was increased to 29,670 μsec, keeping the width of the gate constant. Figure B3b shows the resulting histogram with the bunching of readings still centered very close to 29,700 μsec. Figure B3c shows the results of a third set of readings using a 60-μsec gate which opened at 29,697 μsec. Figures B3d and B3e show two separate histograms representing 30-μsec gates approximately centered on 29,700 μsec. These histograms indicate a signal having a period between 29,698 and 29,701 μsec.

Thus a signal of whose existence the author was somewhat doubtful was found to be a reality and its period was pinpointed within very narrow limits. If one re-examines the photograph of Fig. B2 he must inevitably conclude that up to this time there has not been any general-analysis gear that could measure with such accuracy the periods of signals under conditions of such severe interference.

The equipment has been tested on several local radar signals with equally successful results. Use of the inclusion gate was found unnecessary because of the low noise levels encountered.

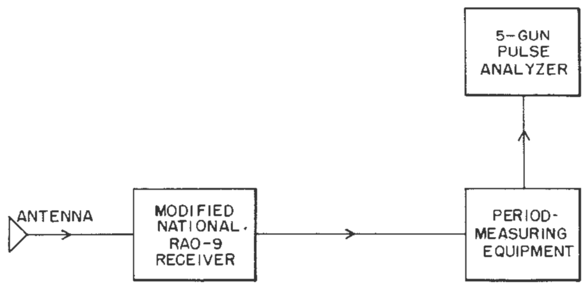


Fig. B1 - Equipment for measuring periods of loran signals

 [redacted]

DECLASSIFIED

DECLASSIFIED

UNCLASSIFIED

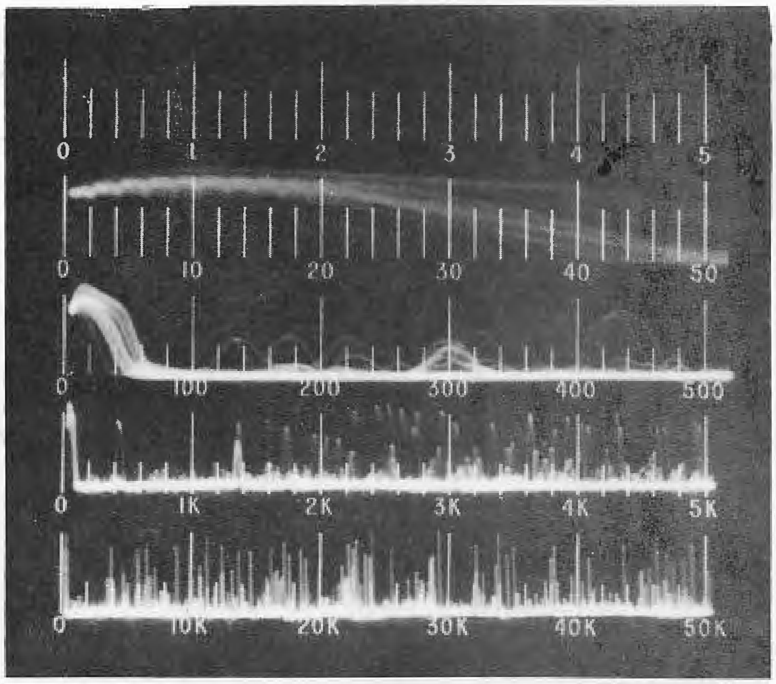


Fig. B2 - Typical loran signals on 5-gun pulse analyzer

[redacted]

DECLASSIFIED

DECLASSIFIED

 [redacted]

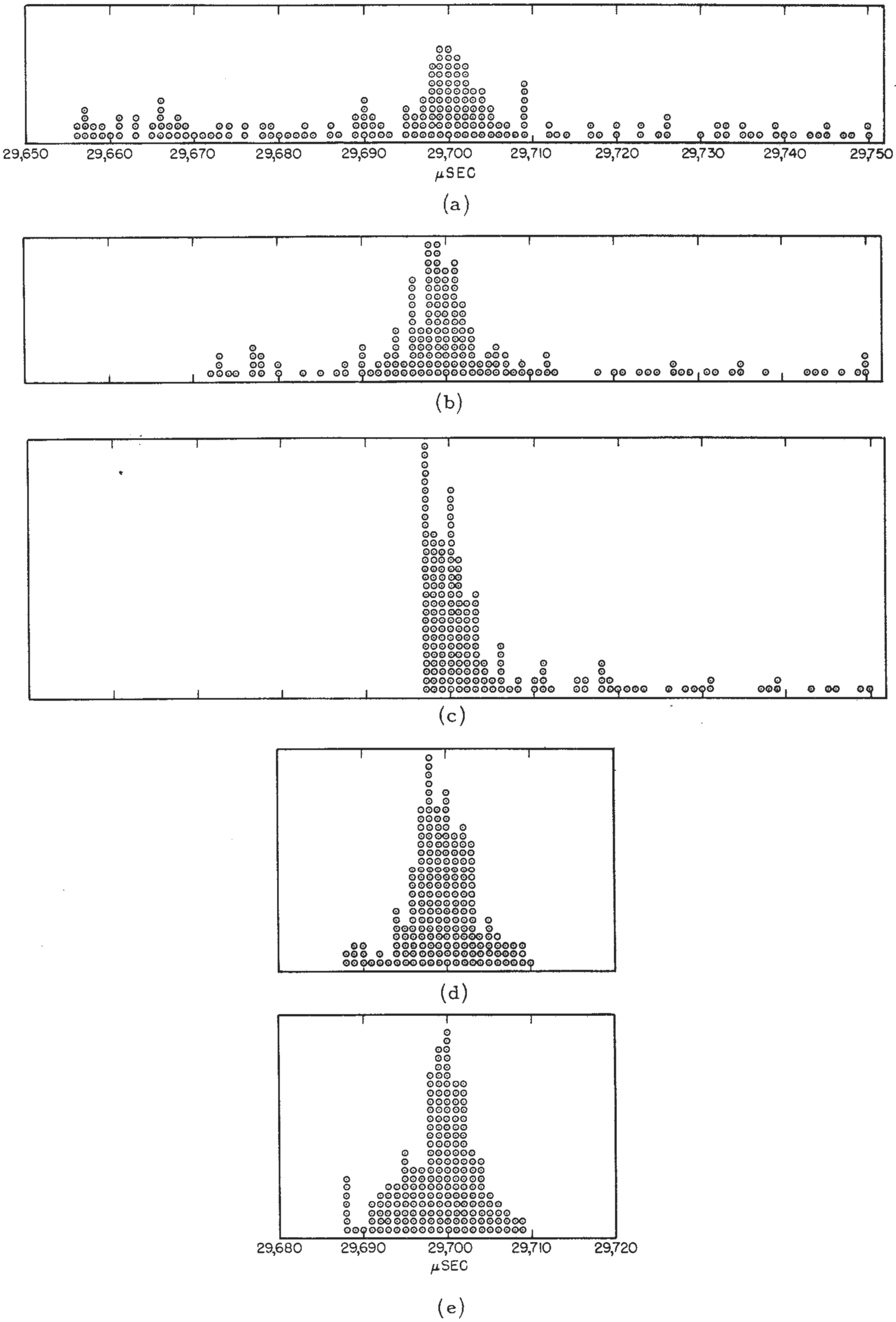


Fig. B3 - Histogram of pulse-period readings

[redacted]

DECLASSIFIED

UNCLASSIFIED

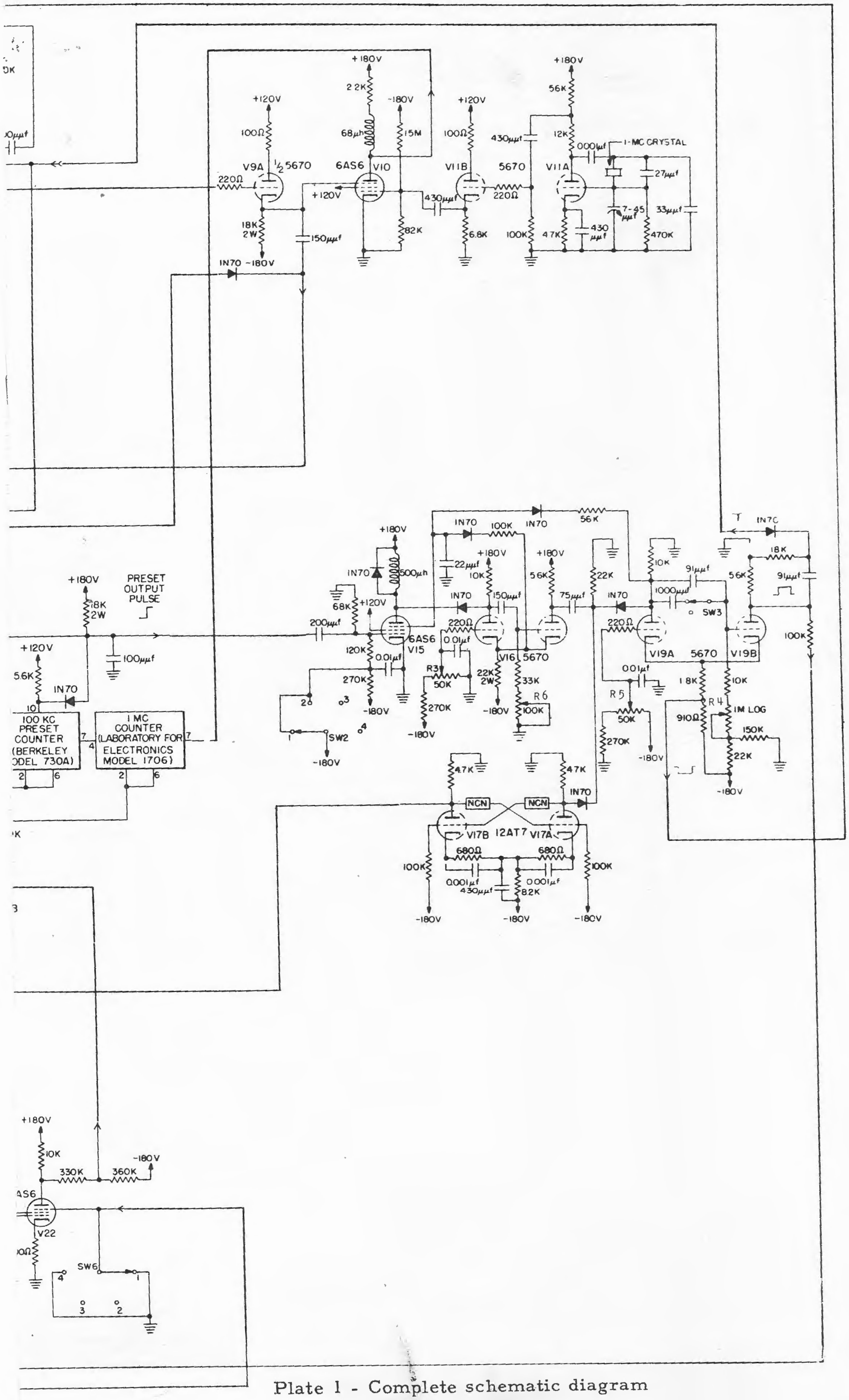
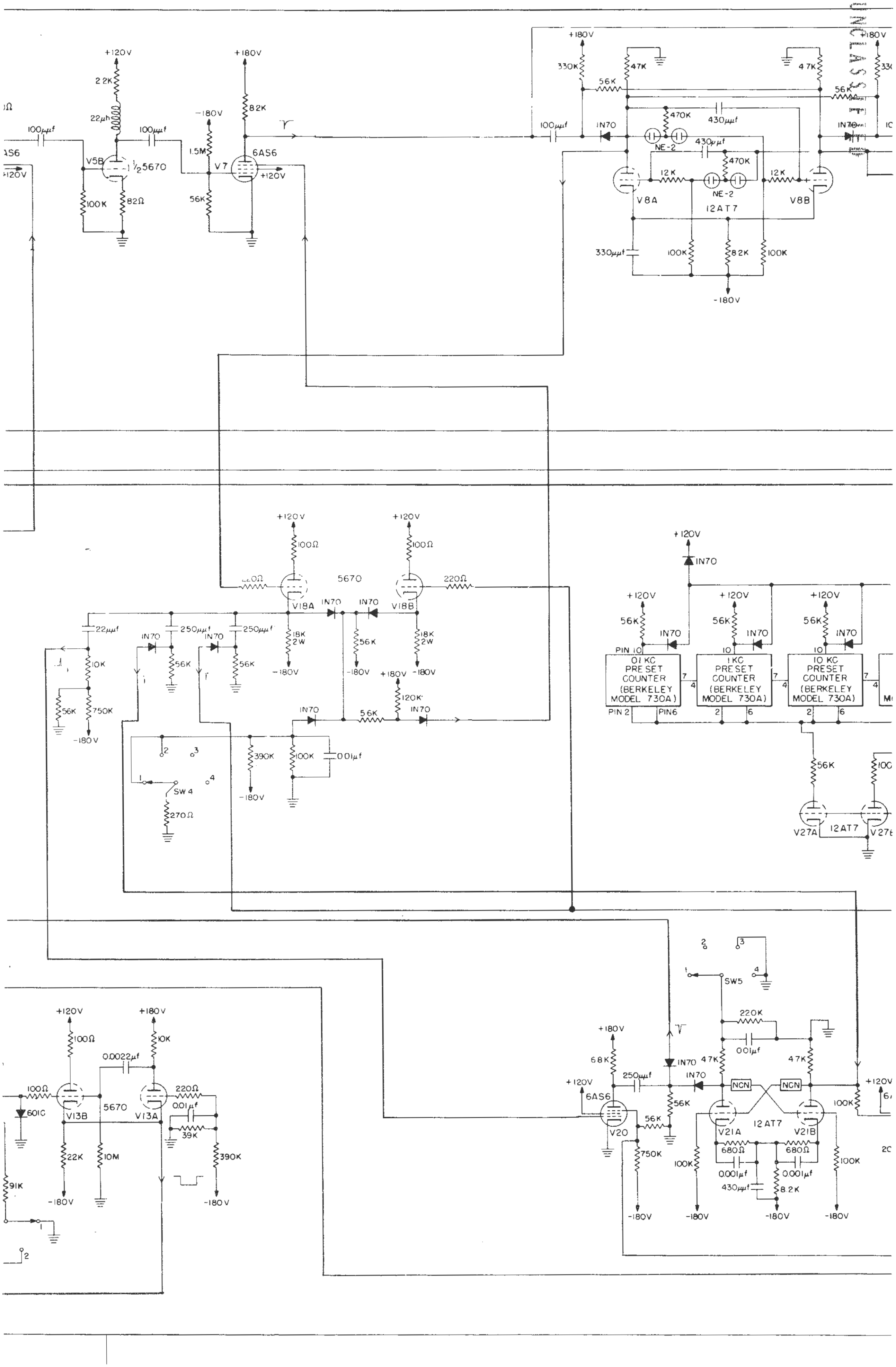


Plate 1 - Complete schematic diagram



+120V
2.2K
22µh
100µµf
V5B
1/2 5670
100K
82Ω
+180V
82K
-180V
1.5M
V7
6AS6
56K
330K
47K
56K
470K
430µµf
1N70
NE-2
12K
V8A
12AT7
V8B
330µµf
100K
82K
-180V
100Ω
5670
V18A
V18B
220Ω
22µµf
250µµf
18K 2W
120K
10K
750K
390K
0.01µf
SW4
270Ω
.01 KC PRESET COUNTER (BERKELEY MODEL 730A)
1 KC PRESET COUNTER (BERKELEY MODEL 730A)
10 KC PRESET COUNTER (BERKELEY MODEL 730A)
PIN 10
PIN 2
PIN6
V27A
12AT7
SW5
220K
001µf
6.8K
250µµf
NCN
V20
V21A
V21B
680Ω
0.001µf
430µµf
8.2K
V13B
V13A
0.0022µf
10M
22K
601C
91K
39K
390K

UNCLASSIFIED

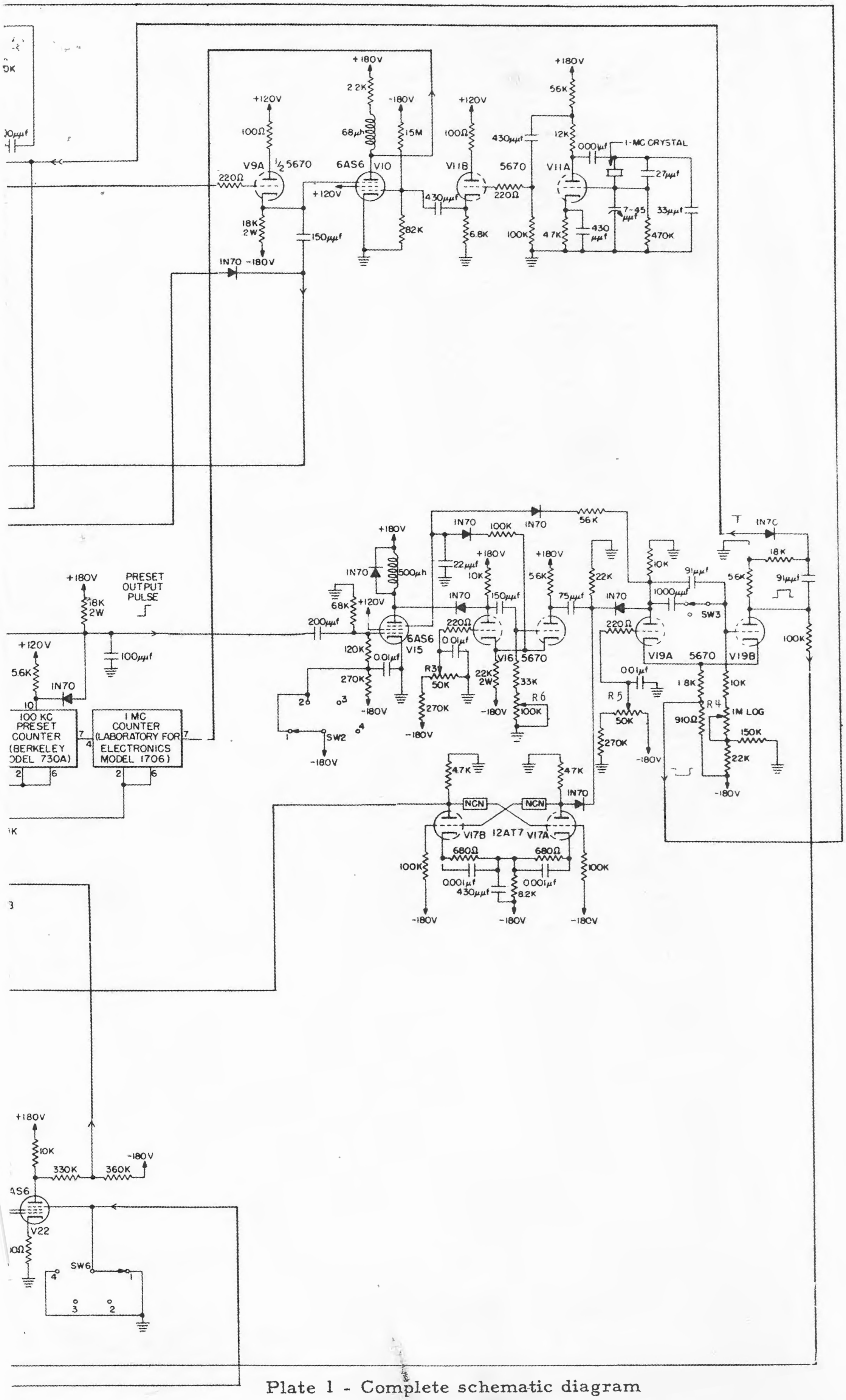


Plate 1 - Complete schematic diagram