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by

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B.S., Gordon College (2017)

Submitted to the Department of Electrical Engineering and Computer Science
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Abstract

Two-level-systems (TLSs) are identified as a major coherence-limiting factor that exist both within and at the interface of amorphous oxides found in current superconducting quantum circuits. Design improvements that reduce the spurious coupling to TLSs have led to significant improvements of superconducting qubit coherence over the past two decades. However, material and fabrication advancement that reduce the sources of TLSs has been relatively limited. Van der Waals (vdW) materials and their heterostructures are known for their extraordinary crystalline quality, versatile electronic properties, and flexible assembly that can be achieved with epitaxially-precise interfaces. In this thesis, we aim to explore and incorporate the advantages of vdW materials into the circuit quantum electrodynamics (cQED) platform of relevance to advancing quantum technologies. In particular, we fabricate and characterize high-quality, all-vdW Josephson junctions, a key component in superconducting quantum circuits. VdW heterostructures of 2-4 layers of hBN sandwiched between $NbSe_2$ superconductors demonstrate Josephson effect and the critical current increases exponentially with decreasing hBN layer number. Additionally, we observed a superconducting gap close to the bulk $NbSe_2$ gap, $\Delta = 1.1\,\text{meV}$ in all the vdW junctions, evidencing little degradation of superconductivity. We expect these efforts will lead to high-coherence all-vdW qubit devices with small footprints.

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Dedicated to my mother, Xiaomei.

Chapter 1

Why Care About van der Waals Materials in Quantum Computing?

1.1 Promise of van der Waals Materials for Superconducting Qubits

In the pursuit of building a quantum computer that could exponentially outperform classical computers on problems such as quantum simulations and factoring large numbers, superconducting qubits have emerged as a prominent platform for constructing large-scale quantum processors [1]. Superconducting qubits are lithographically defined electric circuits, composed of elements such as Josephson tunnel junctions, capacitors, inductors, and resonators. The current lithographic fabrication techniques provide superconducting qubits with great advantages of scalability and design flexibility, compared to other quantum computing modalities, such as electron/nuclear spins [2–4], trapped ions [5–7], and nitrogen-vacancies in diamond [8, 9].

Despite significant progress since their initial appearance, current state-of-art superconducting qubits, developed both by industrial leaders and academic pioneers, still suffer from two-level-systems (TLSs) that have been identified as a major source of noise and decoherence in superconducting quantum devices [10]. TLSs ubiquitously exist both within and at the interface of amorphous oxides commonly found in qubit devices. Improved circuit designs that reduce parasitic coupling of qubits to TLSs has contributed greatly to the five order-of-magnitude improvement of coherence time over the past two decades [11, 12]. This strategy works by making

the quantum circuit less susceptible to TLSs without reducing the TLSs concentrations in the materials. However, it has seemingly exhausted its potential. Further advancement of qubit coherence will need to incorporate advanced materials and fabrication techniques to mitigate the source of TLSs.

Two dimensional van der Waals (vdW) materials consist of individual atomic planes bonded by weak vdW attraction. They are known for their extraordinary crystalline quality, versatile electronic properties, and atomically flat interfaces [13]. Different vdW materials can also be assembled into heteorostructures with epitaxially precise and clean interfaces, which is made possible by the dry transfer techniques [14]. The family of vdW materials offers all the necessary building blocks to construct superconducting quantum devices: high-quality superconductors and dielectrics. Superconducting transition-metal dichalcogenides (TMDs) such as $NbSe_2$, NbS_2, TaS_2, and $TaSe_2$ exhibit well-defined superconducting gaps persistent down to a monolayer. Hexagonal boron nitride (hBN) is an insulator with a bandgap exceeding 5 eV and it has exhibited outstanding performance when serving both as ultra-clean protective layers and as robust tunneling barriers. With the crystalline vdW materials and the fabrication techniques, we are equipped to build Josephson junctions and capacitors with significantly reduced TLS density. Additionally, capacitors made with vdW heteorostructures can assume a compact parallel-plate form with much smaller footprint than current coplanar capacitors, which are selected primarily to avoid strong coupling to TLSs.

While vdW heterostructures have been well investigated via DC transport and optical techniques, experimental exploration in the microwave regime has heretofore been relatively limited. This has left an unexplored potential for incorporating the advantages of vdW materials into the circuit quantum electrodynamics (cQED) platform. On the other hand, the cQED platform can also offer a unique probe to investigate the rich physics of vdW materials.

1.2 Organization of This Thesis

The major goal of this thesis is to incorporate the material and fabrication advantages of vdW materials into superconducting quantum circuits. Specifically, we aim to realize and characterize all-vdW Josephson junctions, the critical component in superconducting qubits. These efforts will hopefully enable all-vdW superconducting qubits that host significantly less TLS with a reduced footprint.

This thesis begins with the theoretical background of Josephson junctions and superconducting qubits in Chapter 2. First, we introduce the theory of Giaever tunneling and Josephson tunneling that are needed to understand the $I-V$ characterisation of the devices. Then we discuss the role that Josephson junctions play in superconducting qubits, and consider the materials origins of superconducting qubit decoherence. The following Chapter 3 gives a brief overview of the macroscopic properties of vdW materials and specifically, the vdW superconductor and insulator of our choice, $NbSe_2$ and hBN. The fabrication procedures for realizing the vdW junction devices are documented in Chapter 4, along with the cooling system and measurement techniques employed to characterise the devices. In Chapter 5, we present the experimental results of three vdW Josephson junctions made with different tunneling hBN thickness. A well-defined superconducting gap is observed in all the junction devices, close to $\Delta = 1.1\,\text{meV}$, the bulk superconducting gap of $NbSe_2$. From the measured $I-V$ characteristics, we extract the critical current density J_c and find that it decreases exponentially with increasing hBN thickness. For junctions with 2 atomic layers of hBN, $J_c \sim 100\,\text{nA}\,\mu\text{m}^{-2}$ is comparable to the critical current density of modern Al-AlO_x-Al junctions. Here we also discuss the observed junction sub-gap resistance and potential aging effect of the junction. Finally, we conclude the thesis in Chapter 6 with an outlook for future directions of research and a plan for realizing proof-of-concept all-vdW transmon qubits.

Chapter 2

Basics of Josephson Junctions and Superconducting Qubits

2.1 Overview of BSC theory

In this section, we will briefly review some of the main assumptions and conclusions in the BCS theory in order to build a basic understanding of the microscopic model for superconductivity. In 1957, John Bardeen, Leon Cooper, and John Robert Schrieffer published their foundational paper [15], where they described how electrons can form a coherent bound state called Cooper pairs that would dramatically change the macroscopic behavior of the material, giving rise to perfect conductivity and flux expulsion. Cooper pairs originate from the slightly attractive interaction between a pair of electrons mediated by phonons. This attractive interaction between electrons results indirectly from the interaction between the electrons and the vibrating crystal lattice (the phonons).

The overview of BCS theory in this chapter mainly follows Michael Tinkham's treatment [16]. Readers can refers to Chapter 3 of *Introduction to Superconductivity* for a more in-depth discussions.

2.1.1 BCS Ground State

We can write the effective BCS Hamiltonian as

$$H = \sum_{\mathbf{k}\sigma} \xi_{\mathbf{k}} c^{\dagger}_{\mathbf{k}\sigma} c_{\mathbf{k}\sigma} + \sum_{\mathbf{k}\mathbf{k}'} V_{\mathbf{k}\mathbf{k}'} c^{\dagger}_{\mathbf{k}\uparrow} c^{\dagger}_{-\mathbf{k}\downarrow} c_{-\mathbf{k}'\downarrow} c_{\mathbf{k}'\uparrow} \tag{2.1}$$

where $c^\dagger_{\mathbf{k}\sigma}$ and $c_{\mathbf{k}\sigma}$ creates and annihilates, respectively, an electron with momentum $\hbar\mathbf{k}$ and spin σ. We define the $\xi_{\mathbf{k}}$ as the electron energy above the chemical potential $\xi_{\mathbf{k}} = \varepsilon_{\mathbf{k}} - \mu$. The second term describes the total attractive potential energy created by Cooper pairs. To make it clearer, we can also replace the single-electron operators by pair operators that create and destroy a Cooper pair made by two electrons of opposite momentum and spin:

$$\boldsymbol{b}^\dagger_k = \boldsymbol{c}^\dagger_{k\uparrow}\boldsymbol{c}^\dagger_{-k\downarrow} \tag{2.2}$$

$$\boldsymbol{b}_k = \boldsymbol{c}_{-k\downarrow}\boldsymbol{c}_{k\uparrow} \tag{2.3}$$

Then we can rewrite the effective BCS potential as

$$\boldsymbol{V}_{\text{eff}} = \sum_{k,k'} V_{kk'}\boldsymbol{b}^\dagger_k\boldsymbol{b}_{k'} \tag{2.4}$$

Now we employ the so-called Bogoliubov transformation to write the single-electron operators in terms of a set of new ferminoic operators, also called *Bogoliubons*, $\gamma_{\mathbf{k}\sigma}$, $\gamma^\dagger_{\mathbf{k}\sigma}$ that describe the quasiparticle excitations of the system.

$$\begin{aligned} c_{\mathbf{k}\uparrow} &= u^*_{\mathbf{k}}\gamma_{\mathbf{k}\uparrow} + v_{\mathbf{k}}\gamma^\dagger_{-\mathbf{k}\downarrow} \\ c^\dagger_{-\mathbf{k}\downarrow} &= u_{\mathbf{k}}\gamma^\dagger_{-\mathbf{k}\downarrow} - v^*_{\mathbf{k}}\gamma_{\mathbf{k}\uparrow} \end{aligned} \tag{2.5}$$

Note that the coefficients $u_{\mathbf{k}}$ and $v_{\mathbf{k}}$ satisfy the normalization condition

$$|u_{\mathbf{k}}|^2 + |v_{\mathbf{k}}|^2 = 1 \tag{2.6}$$

Substituting equation (2.5) into the effective Hamiltonian, we arrive at

$$H = H_0 + H_1 + H_2$$

with

$$
\begin{aligned}
H_0 &= \sum_{\mathbf{k}} \left[2\xi_{\mathbf{k}} \left| v_{\mathbf{k}} \right|^2 - \Delta_{\mathbf{k}} u_{\mathbf{k}} v_{\mathbf{k}}^* - \Delta_{\mathbf{k}}^* u_{\mathbf{k}}^* v_{\mathbf{k}} + \Delta_{\mathbf{k}} \left\langle \boldsymbol{b}_k \right\rangle \right] \\
H_1 &= \sum_{\mathbf{k}} \left[\xi_{\mathbf{k}} \left(\left| u_{\mathbf{k}} \right|^2 - \left| v_{\mathbf{k}} \right|^2 \right) + \Delta_{\mathbf{k}} u_{\mathbf{k}} v_{\mathbf{k}}^* + \Delta_{\mathbf{k}}^* u_{\mathbf{k}}^* v_{\mathbf{k}} \right] \left(\gamma_{\mathbf{k}\uparrow}^\dagger \gamma_{\mathbf{k}\uparrow} + \gamma_{-\mathbf{k}\downarrow}^\dagger \gamma_{-\mathbf{k}\downarrow} \right) \\
H_2 &= \sum_{\mathbf{k}} \left[\left(2\xi_{\mathbf{k}} u_{\mathbf{k}} v_{\mathbf{k}} - \Delta_{\mathbf{k}} u_{\mathbf{k}}^2 + \Delta_{\mathbf{k}}^* v_{\mathbf{k}}^2 \right) \right] \left(\gamma_{\mathbf{k}\uparrow}^\dagger \gamma_{-\mathbf{k}\downarrow}^\dagger \right) + \textbf{h.c.}
\end{aligned} \tag{2.7}
$$

Here **h.c.** represents the hermitian conjugate to simplify the expression. We define a new variable $\Delta_{\mathbf{k}}$, which later will turn out to give the gap in the energy spectrum.

$$
\Delta_{\mathbf{k}} = -\sum_{\mathbf{k}'} V_{\mathbf{k}\mathbf{k}'} \left\langle \boldsymbol{b}_k \right\rangle \tag{2.8}
$$

In order to diagonalize the total effective Hamiltonian, we can choose the coefficient $u_{\mathbf{k}}$ and $v_{\mathbf{k}}$ to satisfy the following condition so that the $\gamma_{\mathbf{k}\uparrow}^\dagger \gamma_{-\mathbf{k}\downarrow}^\dagger$ terms vanish in H_2.

$$
2\xi_{\mathbf{k}} u_{\mathbf{k}} v_{\mathbf{k}} + \Delta_{\mathbf{k}}^* v_{\mathbf{k}}^2 - \Delta_{\mathbf{k}} u_{\mathbf{k}}^2 = 0 \tag{2.9}
$$

Combined with the normalization condition (2.6), we can solve for $u_{\mathbf{k}}$ and $v_{\mathbf{k}}$:

$$
\left| u_{\mathbf{k}} \right|^2 = \frac{1}{2} \left(1 + \frac{\xi_{\mathbf{k}}}{\sqrt{\xi_{\mathbf{k}}^2 + \left| \Delta_{\mathbf{k}} \right|^2}} \right) \tag{2.10}
$$

$$
\left| v_{\mathbf{k}} \right|^2 = \frac{1}{2} \left(1 - \frac{\xi_{\mathbf{k}}}{\sqrt{\xi_{\mathbf{k}}^2 + \left| \Delta_{\mathbf{k}} \right|^2}} \right) \tag{2.11}
$$

We define a new variable $E_{\mathbf{k}}$, which will soon be shown to be the quasiparticle excitation energy of momentum $\hbar\mathbf{k}$,

$$
E_{\mathbf{k}} = \sqrt{\xi_{\mathbf{k}}^2 + \left| \Delta_{\mathbf{k}} \right|^2} \tag{2.12}
$$

Now we can use the above results to simplify the (2.7) Hamiltonian into:

$$H = \sum_{\mathbf{k}} \left(\xi_{\mathbf{k}} - E_{\mathbf{k}} + \Delta_{\mathbf{k}} \left\langle c^{\dagger}_{\mathbf{k}\uparrow} c^{\dagger}_{-\mathbf{k}\downarrow} \right\rangle \right) + \sum_{\mathbf{k}} E_{\mathbf{k}} \left(\gamma^{\dagger}_{\mathbf{k}\uparrow} \gamma_{\mathbf{k}\uparrow} + \gamma^{\dagger}_{-\mathbf{k}\downarrow} \gamma_{-\mathbf{k}\downarrow} \right)$$

$$H = E_0 + \sum_{\mathbf{k}\sigma} E_{\mathbf{k}} \gamma^{\dagger}_{\mathbf{k}\sigma} \gamma_{\mathbf{k}\sigma} \tag{2.13}$$

with

$$E_0 = \sum_{\mathbf{k}} \left(\xi_{\mathbf{k}} - E_{\mathbf{k}} + \Delta_{\mathbf{k}} \left\langle c^{\dagger}_{\mathbf{k}\uparrow} c^{\dagger}_{-\mathbf{k}\downarrow} \right\rangle \right) \tag{2.14}$$

It is evident now why $E_{\mathbf{k}}$ is the excitation energy since it is the energy required for adding a quasiparticle excitation, described by $\gamma^{\dagger}_{\mathbf{k}\sigma}$, from the BCS ground state. Additionally, from (2.12) we know even at the Fermi energy, when $\xi_{\mathbf{k}} = \varepsilon_{\mathbf{k}} - \mu = 0$, the energy spectrum has a gap size $|\Delta_{\mathbf{k}}|$. Thus we will need to supply an energy of at least $2|\Delta_{\mathbf{k}}|$ to create a pair of quasiparticles.

To better understand quasiparticles properties, we can rewrite (2.5) in the single-electron basis:

$$\gamma_{\mathbf{k}\uparrow} = u_{\mathbf{k}} c_{\mathbf{k}\uparrow} - v_{\mathbf{k}} c^{\dagger}_{-\mathbf{k}\downarrow} \tag{2.15}$$

$$\gamma^{\dagger}_{-\mathbf{k}\downarrow} = u^{*}_{\mathbf{k}} c^{\dagger}_{-\mathbf{k}\downarrow} + v^{*}_{\mathbf{k}} c_{\mathbf{k}\uparrow} \tag{2.16}$$

Now we can recognize the quasiparticle, or Bogoliubon, as a coherent superposition of an electron and hole. Referring back to (2.10) and (2.11), for $|\Delta_{\mathbf{k}}| > 0$ when $\xi_{\mathbf{k}} > 0$, $|u_{\mathbf{k}}|^2 > 1/2$ and $|v_{\mathbf{k}}|^2 < 1/2$, so the excitation is more *electron-like*; and vice versa, for $\xi_{\mathbf{k}} < 0$, the excitation is more *hole-like*, as shown in Figure 2.1. In the limit of $|\Delta_{\mathbf{k}}| \to 0$, we recover normal metal behavior: positive $\xi_{\mathbf{k}}$ gives rise to electron excitation and negative $\xi_{\mathbf{k}}$ excites holes.

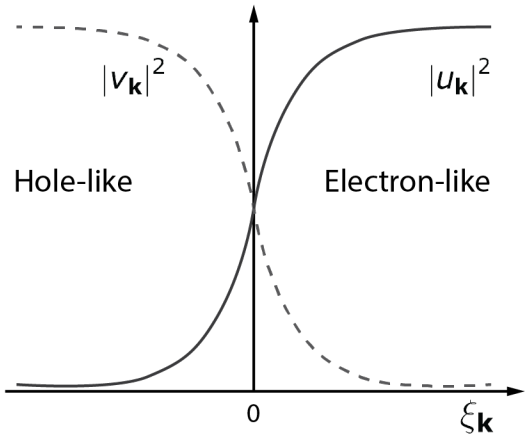


FIGURE 2.1: BCS quasiparticle excitation as represented in electron-hole space, as a function of $\xi_{\mathbf{k}}$. When $\xi_{\mathbf{k}} > 0 (< 0)$, the quasiparticle is electron-like (hole-like).

2.1.2 Density of States

Since the total number of states available in a material does not change due to a phase transition, we can find the superconducting density of states (DOS), $N_s(E)$, by equating

$$N_s(E)dE = N_n(\xi)d\xi, \tag{2.17}$$

where $N_n(\xi)$ denotes the normal-state DOS. In the limit $E_{\mathbf{k}} \gg \Delta$, $E_{\mathbf{k}} \approx \xi_{\mathbf{k}} = \varepsilon_{\mathbf{k}} - \mu$, which is just the electron energy of normal metal. Thus, at an energy well above the gap, the normal state energy spectrum of unpaired electrons is recovered. Therefore we can limit our focus to the vicinity of $\sim \Delta$ around the Fermi energy. Since $\Delta \ll E_F$, we can treat the normal metal density of states as constant $N_n(\xi_{\mathbf{k}}) = N_n(0)$. Then from equation (2.12) we can easily derive the relative superconducting density of states:

$$\rho_s(E) \equiv \frac{N_s(E)}{N_n(0)} = \frac{d\xi}{dE} = \begin{cases} \frac{E}{\sqrt{E^2-\Delta^2}} & E > \Delta \\ 0 & E < \Delta \end{cases} \tag{2.18}$$

As shown in Figure 2.2 (b), all the states within $|E| < \Delta$ are pushed out of the gap. Unpaired electrons fill the energy spectrum up to $-\Delta$ below the Fermi energy when

$T = 0$. In the following section, we will refer to this DOS diagram to obtain an intuitive understanding of electron tunneling between superconductors and normal metals.

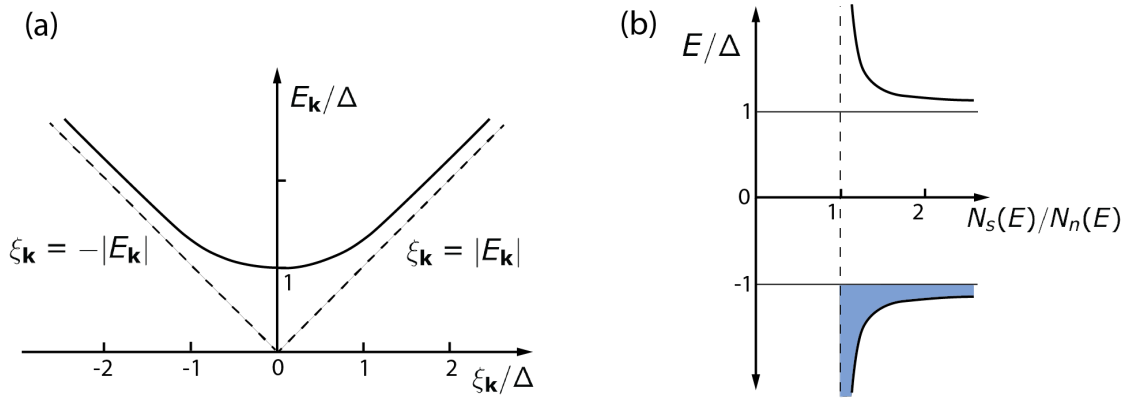


FIGURE 2.2: **(a)** Quasiparticle excitation energy as a function of $\xi_{\mathbf{k}}$. **(b)** Density of states of the quasiparticle in superconducting compared to normal state. In both figures, the dotted lines represent the normal state and the solid curves denote the superconducting state.

2.2 Tunneling in Superconductors

2.2.1 Giaever Tunneling

The superconducting density of states calculated from BCS theory was first experimentally examined by means of electron tunneling [17, 18]. When applying a small voltage V across the junction, the net tunneling current is proportional to the product of the DOS of the two normal metals or superconducting metals on each side of the junction, N_1 and N_2, separated by a thin insulating film:

$$I_{1\to 2} = A|\mathcal{T}|^2 \int_{-\infty}^{\infty} N_1\left(E+eV\right) N_2\left(E\right)\left[f\left(E\right) - f\left(E+eV\right)\right] dE \tag{2.19}$$

where A is a proportionality constant, $f(E)$ is the fermi-dirac distribution at energy E, and we assume the tunneling-matrix element $\mathcal{T}$ is constant. The direct correlation between the tunneling current and density of electron states provided a probe for investigating the superconducting DOS and energy gap. In 1961 and 1962,

Ivar Giaever published experimental results of the electron tunneling behavior of normal-insulator-superconductor (NIS) junctions [17], as well as superconductor-insulator-superconductor (SIS) junctions [18], and the I-V curve characteristics showed good agreement with the BCS theory.

An intuitive method that describes the electron tunneling current is the *semiconductor model*, in which electrons tunnel through *horizontal channels*, i.e., they occur at constant energy after accounting for the applied voltage across the junction by adjusting the different μ levels. At $T = 0$, electrons fill the available density of states of the material up to the Fermi level μ and tunneling can happen when the other side of the junction has available energy states. In this model, the normal metal is described by a continuous gap-less density of states distribution, while the superconductor is represented by a pair of symmetric electron bands about the Fermi level with the superconducting gap Δ, as seen in Figure 2.3 and 2.5.

Normal-Normal Tunneling

When both metals are in normal state and at a temperature $k_B T \ll E_F$ (which is always true for a metal since $E_F/k_B \sim 10^5$ K), equation (2.19) simplifies to

$$\begin{aligned} I_{nn} &= AN_1(0)N_2(0)|\mathcal{T}|^2 \int_{-\infty}^{\infty} [f(E) - f(E+eV)]\, dE \\ &= AN_1(0)N_2(0)|\mathcal{T}|^2 eV \equiv G_{nn}V \end{aligned} \tag{2.20}$$

The ohmic behavior of normal conductor is recovered.

Normal-Superconductor Tunneling

For the case where one of the metals is in superconducting state, let's first look at the *semiconductor model* pictured in Figure 2.3 to qualitatively describe the tunneling current behavior. At $T = 0$, tunneling is prohibited until the applied voltage reaches $eV > \Delta$. The current will increase sharply when the voltage is just above the gap, and then asymptotically approach the linear behavior as expected from normal-normal metal tunneling, as shown in Figure 2.4 (a). At $T > 0$, the occupation number depends on the Fermi function at T, which will create vacant states in the

electron and hole bands. Thus small current can flow at reduced voltage, giving rise to an exponential tail in the region where $eV < \Delta$, as shown in Figure 2.4 (b).

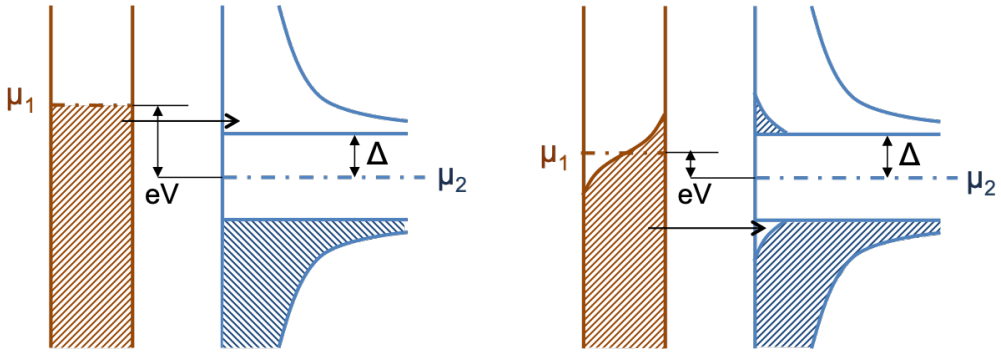


FIGURE 2.3: Semiconductor model description of electron tunneling in a normal metal-superconductor junction **(a)** At $T = 0$, no electron tunneling is allowed until applied voltage reaches $eV > \Delta$. **(b)** For $T > 0$, thermally activated electrons can tunnel at reduced voltage.

Analytically, we can now see equation (2.19) becomes

$$\begin{aligned} I_{ns} &= AN_1(0)|\mathcal{T}|^2 \int_{-\infty}^{\infty} N_2(E)\left[f(E) - f(E+eV)\right] dE \\ &= \frac{G_{nn}}{e} \int_{-\infty}^{\infty} \frac{N_{2s}(E)}{N_{2n}(0)} \left[f(E) - f(E+eV)\right] dE \end{aligned} \tag{2.21}$$

To more directly see the correlation between the tunneling current characteristics and DOS, we consider the differential conductance dI/dV as a function of applied voltage V across the junction.

$$G_{ns} = \frac{dI_{ns}}{dV} = G_{nn} \int_{-\infty}^{\infty} \frac{N_{2s}(E)}{N_2(0)} \left[-\frac{\partial f(E+eV)}{\partial(eV)}\right] dE \tag{2.22}$$

For finite temperature, the derivative of Fermi-Dirac distribution $-\frac{\partial f(E+eV)}{\partial(eV)}$ looks like a bell curve with width $4k_BT$. Therefore the differential conductance G_{ns} measures the convolution of the relative superconducting density of states $\rho_s(E)$, as defined in equation (2.18), and this bell-curve. As temperature drops, this derivative term becomes a delta function and at $T = 0$, $G_{ns}|_{T=0} = G_{nn}\frac{N_{2s}(e|V|)}{N_2(0)}$. We can compare the theoretical superconductor DOS shown in Figure 2.2 to the G_{ns} curve in Figure 2.4 (b) for the direct correlation.

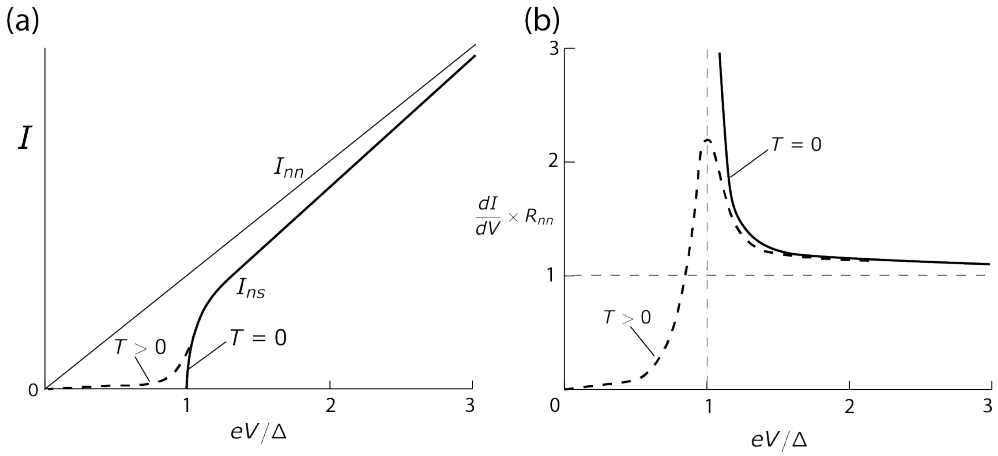


FIGURE 2.4: Normal-superconductor tunnel junction characteristics. (a) I-V curve (b) normalized differential conductance, which directly measures density of states at of the superconductor at $T = 0$. The solid curves indicate $T = 0$ case and dashed curves indicate the $T > 0$ case.

Superconductor-Superconductor Tunneling

Now for the case of our interest, superconductor-insulator-superconductor junction, the tunneling current characteristic is slightly more rich. As shown in Figure 2.5, at absolute zero temperature, electron tunneling won't happen until $eV \geq \Delta_1 + \Delta_2$. While at finite temperature, thermally excited electrons are allowed to tunnel and current will increase sharply at $eV = |\Delta_1 - \Delta_2|$, since at this bias voltage, the bottom gap edges of the two superconductors are aligned, and quasi-particles in superconductor 1 tunnel from the peak density of states to the peak of available states in superconductor 2. Then for $|\Delta_1 - \Delta_2| < eV < \Delta_1 + \Delta_2$, the tunneling current will decrease until it jumps again at $eV = \Delta_1 + \Delta_2$ because the density of states is infinite at the gap edges.

The tunneling current behavior described above is drawn in the IV characteristic trace in Figure 2.6. When taking a voltage-biased differential conductance measurement, we will expect to see a peak at $eV = |\Delta_1 - \Delta_2|$. However, this peak is non-stable and will not show up in current-biased measurement configuration, since for the same current value there exist multiple valid voltage values.

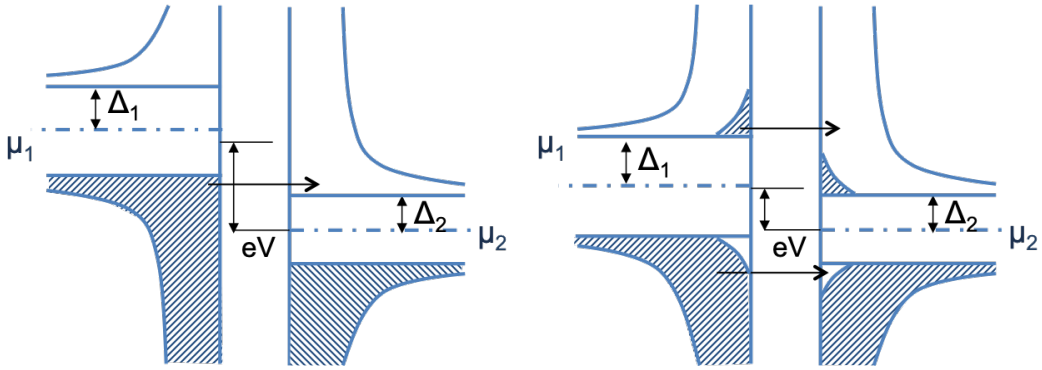


FIGURE 2.5: Semiconductor model description of electron tunneling in a superconductor-superconductor junction **(a)** At $T = 0$, there is no available energy state for tunneling until $eV \geq \Delta_1 + \Delta_2$. **(b)** For $T > 0$, thermally activated quasiparticles can tunnel at reduced voltage.

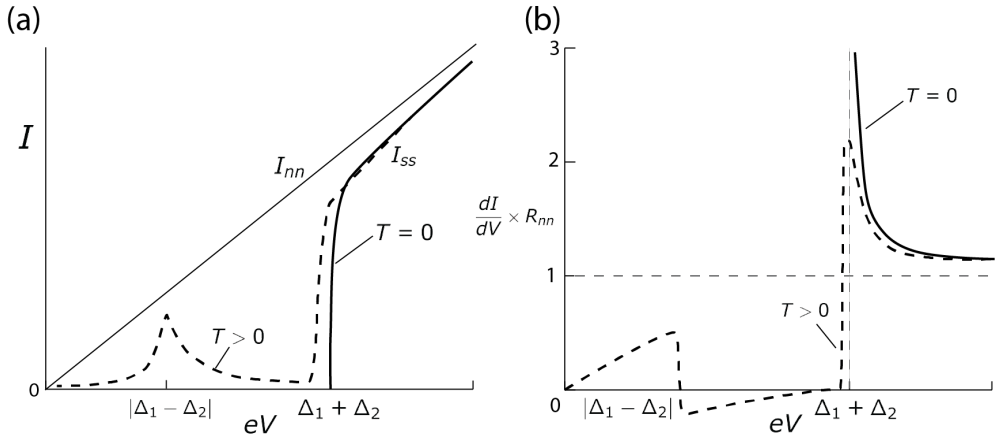


FIGURE 2.6: Superconductor-superconductor tunnel junction characteristics. (a) I-V curve (b) normalized differential conductance. The solid curves indicate $T = 0$ case and dashed curves indicate $T > 0$ case.

Again, let's take a look at the analytical solution for the tunneling current.

$$\begin{aligned} I_{ss} &= A \int_{-\infty}^{\infty} |T|^2 N_1(E) f(E) N_2(E+eV)[f(E) - f(E+eV)]dE \\ &= \frac{G_{nn}}{e} \int_{-\infty}^{\infty} \rho_1(E)\rho_2(E+eV)[f(E) - f(E+eV)]dE \end{aligned} \tag{2.23}$$

In our discussion later, we will focus on the case where we have $\rho_1 = \rho_2 = \rho_s$ (i.e. the superconductors on each side of the insulator are made with the same materials).

It is important to note that this *semiconductor model* greatly simplifies the details of the electron tunneling. One significant part missing in this model is the superconducting ground state. We will discuss another type of tunneling, Josephson tunneling, that involves the ground state condensed pairs in the next section.

2.2.2 Josephson Tunneling

In the same year that Giaever published his results on electron tunneling between two superconductors, Josephson made a remarkable prediction of another type of superconducting tunneling: at zero applied voltage, suppercurrent can flow between two superconductors separated by a thin insulating film. This current at zero voltage is a direct result of Cooper pair tunneling, which was regarded as nearly impossible before Brian Josephson changed the popular opinion in 1962 [19].

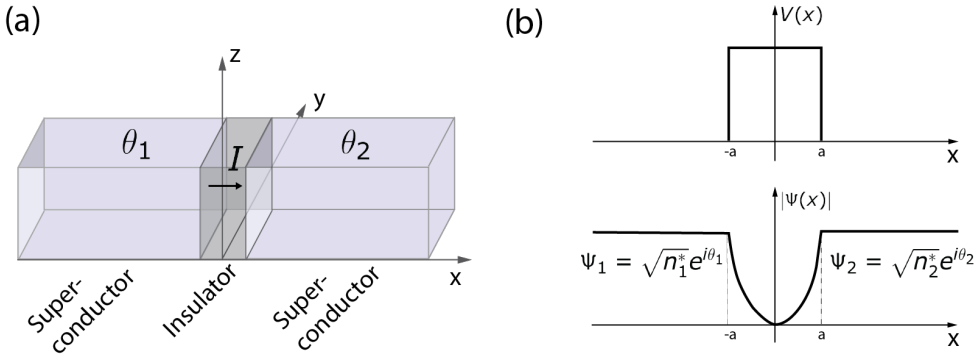


FIGURE 2.7: **(a)**A Josephson junction made of two superconductors (light blue) separated by a thin insulator (gray). θ_1 and θ_2 denote the superconducting phase parameters of the two superconductors. **(b)** Simple potential model of the *SIS* junction and the corresponding wave function magnitude for the two superconductors at $x = \pm a$. Note the superelectron density n^* and wavefunction phase θ can be different in the two superconductors.

In the macroscopic model of superconductivity, a quantum wavefunction $\Psi(\mathbf{r}, t)$ is used to describe the behavior of the entire ensemble of superelectrons in the superconductor.

$$\Psi(\mathbf{r}, t) = \sqrt{n^*}e^{i\theta(\mathbf{r},t)} \tag{2.24}$$

Here n^* denotes the superelectron density, and θ is a phase of the wavefunction. In a superconductor-insulator-superconductor (*SIS*) Josephson tunnel junction, as shown in Figure 2.7 (a), the insulating film can be simplified and modeled as a square potential barrier. For a thin insulating barrier, the wave functions of the two superconductors can have enough overlap to allow for suppercurrent to flow through the barrier. Along the x direction, we define the *gauge-invariant phase difference* between the two superconductors across the insulator:

$$\varphi(y,z,t) = \theta_1(y,z,t) - \theta_2(y,z,t) - \frac{2\pi}{\Phi_0}\int_1^2 \vec{A}(\vec{r},t)\cdot d\vec{l} \tag{2.25}$$

where Φ_0 is the flux quantum defined as $h/2e$. The two most fundamental equations describing the Josephson tunneling behavior can then be written in terms of the gauge-invariant phase φ.
The current-phase relation:

$$I = I_c \sin\varphi(t) \tag{2.26}$$

The voltage-phase relation:

$$\frac{d\varphi}{dt} = \frac{2\pi}{\Phi_0}v \tag{2.27}$$

Equations (2.26) and (2.27) tell us that when applying a DC current below the critical current I_c, we can sustain a constant phase difference φ across the junction and therefore obtain supper-current with zero-voltage. The critical current I_c is determined by the tunneling barrier material and geometry, and inversely proportional to the junction normal state resistance, known as the *Ambegaokar-Baratoff* formula [20]

$$I_c R_n = (\pi\Delta/2e)\tanh\Delta/2kT \tag{2.28}$$

At $T \to 0$, this relation reduces to $I_c R_n = \pi\Delta(0)/2e$.

Now with the current-phase and voltage-phase relation, the energy stored in the

basic Josephson junction can be derived by integrating the power

$$W_J = \int_0^{t_0} i(t)v(t)dt \tag{2.29}$$

$$= \int_0^{t_0} (I_c \sin\varphi')(\frac{\Phi_0}{2\pi}\frac{d\varphi'}{dt}dt) \tag{2.30}$$

$$= \frac{\Phi_0 I_c}{2\pi}\int_{\varphi_1}^{\varphi_2} \sin\varphi' d\varphi' \tag{2.31}$$

$$= \frac{\Phi_0 I_c}{2\pi}(1-\cos\varphi) = E_J(1-\cos\varphi) \tag{2.32}$$

where E_J is called the Josephson energy.

AC Josephson Effect

The above discussion focused on the DC current, zero-voltage dynamics. When a constant voltage V_0 is applied across a basic Josephson junction, the phase difference changes in time according to voltage-phase relation, and we see an ac current develops across the junction

$$i = I_c \sin\left[\frac{2\pi}{\Phi_0}V_0 t + \varphi(0)\right] \tag{2.33}$$

This effect is known as the *ac Josephson effect* and f_J the *Josephson frequency*, given by

$$f_J = \frac{V_0}{\Phi_0} = \frac{2e}{h}V_0 = 483.6\times 10^{12} V_0 \quad \text{(Hz)} \tag{2.34}$$

2.3 RCSJ Model with DC Current Drive

While equation (2.26) is sufficient to describe the tunneling current characteristics at zero voltage, for current larger than I_c, we need to consider a generalized Josephson junction which includes additional resistive and capacitive channels in parallel to the ideal Josephson junction, as shown in Figure 2.8 (a). The resistive channel originates from quasiparticle tunneling at finite temperature or impurities in the junction when the voltage is below the gap voltage $V_g \equiv 2\Delta/e$, and normal electron

tunneling when $V > V_g$.

$$R(V) = \begin{cases} R_{sg}(T) & \text{for } |V| < 2\Delta/e \\ R_N & \text{for } |V| \geq 2\Delta/e \end{cases} \tag{2.35}$$

Note that $R(V)$ is nonlinear near the gap voltage 2Δ as discussed in the previous section.

The capacitive channel is simply a result of the parallel-plate structure of the junction.

$$C = \frac{\epsilon A}{2d} \tag{2.36}$$

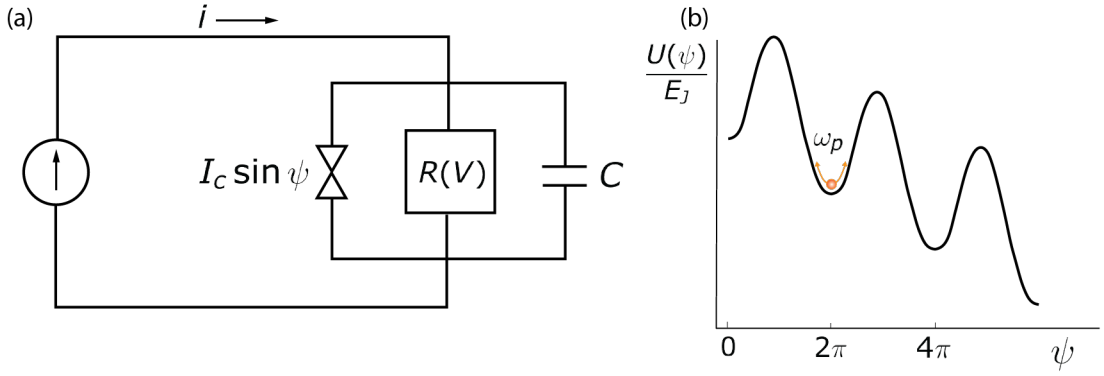


FIGURE 2.8: **(a)** The resistive and capacitive shunted junction model: an ideal Josephson junction is shunted by a resistive channel $R(V)$ and a capacitive channel C. **(b)** A general Josephson junction phase dynamics can be modeled by the classical analogy of a phase particle moving on a tilted washboard potential with a drag force. Local minima of the potential occur at every 2π, where the phase particle can oscillate with frequency ω_p.

Within the resistive and capacitive shunted junction (RCSJ) model, we can write down the total junction current from the three parallel channels

$$I = I_c \sin\varphi + \frac{V}{R(V)} + C\frac{dV}{dt} \tag{2.37}$$

Substituting in the phase-voltage relationship from equation (2.27), the time dependence of the phase φ can be derived as:

$$I = I_c \sin\varphi + \frac{1}{R}\frac{\Phi_0}{2\pi}\frac{d\varphi}{dt} + C\frac{\Phi_0}{2\pi}\frac{d^2\varphi}{dt^2} \tag{2.38}$$

We can re-organize the parameters so that

$$\begin{aligned} \left(\frac{\hbar}{2e}\right) C\frac{d^2\varphi}{dt^2} + \left(\frac{\hbar}{2e}\right)\frac{1}{R}\frac{d\varphi}{dt} + I_c(\sin\varphi - \frac{I}{I_c}) = 0 \\ \left(\frac{\hbar}{2e}\right)^2 C\frac{d^2\varphi}{dt^2} + \left(\frac{\hbar}{2e}\right)^2\frac{1}{R}\frac{d\varphi}{dt} + \frac{d}{d\varphi}\left[E_J(-\cos\varphi - \frac{I}{I_c}\varphi)\right] = 0 \end{aligned} \tag{2.39}$$

A closer look at equation (2.39) should reveal its classical analogy: a phase particle of mass $M = (\hbar/2e)^2 C$ moving on a tilted washboard potential

$$U(\varphi) = -E_J(\frac{I}{I_c}\varphi + \cos\varphi) \tag{2.40}$$

as shown in Figure 2.8 (b) and subjected to a viscous damping term $\eta = (\hbar/2e)^2/R$. At zero current, the potential has a sinusoidal profile with minima every 2π. As the current is increased up to I_c, the washboard potential starts to tilt but the phase particle remains trapped in a local minimum, and therefore maintains a zero voltage with static phase. When $I/I_c > 1$, the phase particle starts rolling on a continuously downward potential and thus develops a voltage across the junction, due to the time dependence of of the phase since $V = \frac{\hbar}{2e}\frac{d\varphi}{dt}$.

Now we parameterize this nonlinear differential equation (2.39) into a dimensionless one

$$\frac{d^2\varphi}{d\tau^2} + \frac{1}{Q}\frac{d\varphi}{d\tau} + \sin\varphi = \frac{I}{I_c} \tag{2.41}$$

where we introduced a dimensionless time variable $\tau = \omega_p t$, with

$$\omega_p = \sqrt{2eI_c/\hbar C} \tag{2.42}$$

the so-called *plasma frequency* of the junction. The effect of the damping term is determined by the "quality factor" Q of the junction, defined as

$$Q = \omega_p RC \tag{2.43}$$

In this RCSJ model, we will see how the IV curve characteristics of the junction vary for different amount of damping.

2.3.1 Overdamped Junction, $Q \ll 1$, at $T = 0$

When the damping is large, $Q \ll 1$, equation (2.41) reduces to a first-order differential equation

$$\frac{d\varphi}{dt} = \frac{2eI_cR}{\hbar}\left(\frac{I}{I_c} - \sin\varphi\right) \tag{2.44}$$

For $I > I_c$, we find that the rate of change for the phase, hence the voltage across the junction, is always positive and varies periodically with the phase. We can solve for the phase analytically:

$$\varphi(t) = 2\tan^{-1}\left[\sqrt{1-\left(\frac{I_c}{I}\right)^2}\tan\left(\frac{t\sqrt{(I/I_c)^2-1}}{2\tau_J}\right) - \frac{I_c}{i}\right] \tag{2.45}$$

with period

$$\Theta = \frac{2\pi\tau_J}{\sqrt{(I/I_c)^2-1}} \tag{2.46}$$

where $\tau_J \equiv \hbar/2eI_cR$ is the time constant for Josephson junction. The time averaged voltage can be found by integrating $V(t)$ over one period Θ and we obtain

$$\langle V(t)\rangle = \frac{1}{\Theta}\int_0^{\Theta} V(t)dt = IR\sqrt{1-(I_c/I)^2} \qquad \text{for } I > I_c \tag{2.47}$$

which smoothly interpolates the Josephson tunneling region when $I < I_c$ and the ohmic region when $I \gg I_c$ without hysteresis, as shown in Figure 2.9 (a). After taking into consideration the voltage dependence of the junction resistance, as shown in Figure 2.6 (b), the resulting IV curve characteristics for an overdamped junction

looks like 2.9 (b): voltage increases sharply from zero to 2Δ at I_c, and then curves smoothly into a straight line with linear resistance R_N.

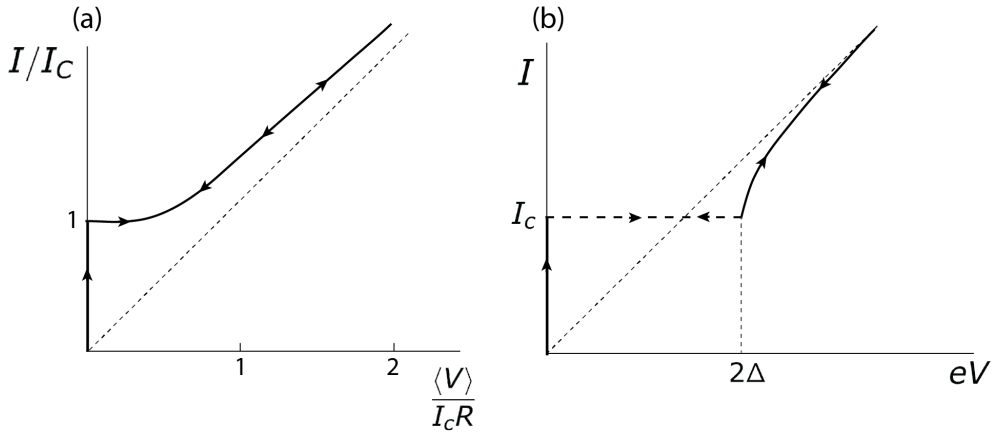


FIGURE 2.9: Representative IV curve characteristics for overdamped Josephson junction at zero temperature. **(a)** plots current normalized by critical current I_c vs. voltage normalized by $I_c R(V)$ **(b)** plots the typical IV characteristics after considering the voltage dependence of the junction resistance.

In the tilted washboard model, a heavily damped phase particle is dominated by the viscous drag force. When $I \gtrsim I_c$, the particle moves much slower through the almost horizontal inflection points than through the steeper drops. This process generates highly non-sinusoidal voltage. As current increases to $I \gg I_c$, the phase particle progresses at a constant pace, leading to sinusoidal voltage and the Josephson current averages to zero. Therefore the IV curve recovers the ohmic characteristics at large current.

2.3.2 Underdamped Junction, $Q \gg 1$, at $T = 0$

When the parallel channels R and C are large, leading to high quality factor, $Q \gg 1$, the junction is *underdamped* and the IV curve becomes hysteretic as Figure 2.10 illustrates. As current is increased from zero, the voltage remains zero until the current reaches I_c and it jumps to 2Δ at I_c. However, as current is swept down towards zero, the voltage does not go immediately to zero at I_c but rather stays at $\sim$

2Δ until below the retrapping current I_r. This hysteretic behavior can be intuitively explained in the RCSJ model as the inertia carrying the phase particle over the local minima when the tilted washboard is lifted. Alternatively, we can recognize that

$$Q = \sqrt{\frac{2eI_cR^2C}{\hbar}} = \sqrt{\frac{RC}{(\hbar/2eI_cR)}} = \sqrt{\frac{\tau_{RC}}{\tau_J}} \tag{2.48}$$

When $\tau_{RC} \gg \tau_J$, the RCSJ behavior is dominated by the RC resonator. Thus the time-averaged dc voltage is just $\langle V(t)\rangle = IR$. Note this solution assumes current is already flowing through the resistor, corresponding to non-zero voltage across the junction. So it only applies to when the current is swept down from above I_c.

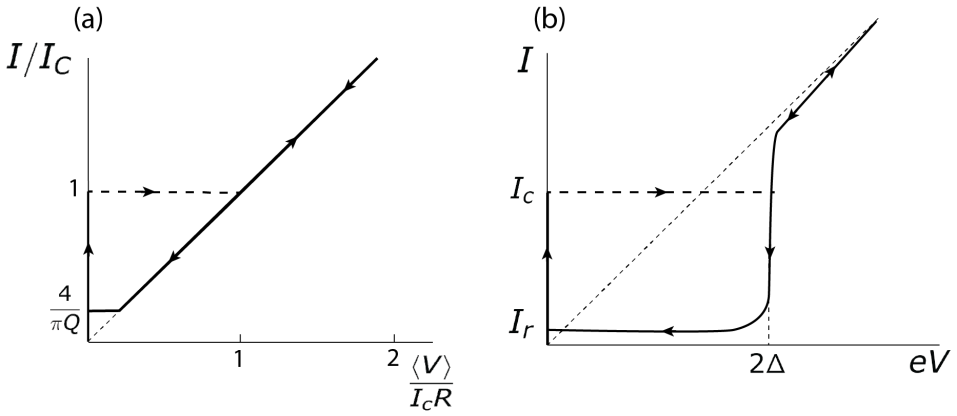


FIGURE 2.10: Representative IV curve characteristics for underdamped Josephson junction at zero temperature. **(a)** current normalized by critical current I_c vs. voltage normalized by $I_cR(V)$ **(b)** the typical IV characteristics after considering the voltage dependence of the junction resistance.

The retrapping current can be found by equating the dissipated energy when the phase particle advance one cycle, $\frac{1}{2}CV^2/Q$, to the energy supplied by the driving current source during the same period, $I^2R\tau$. I_r can then be found to relate to I_c by the quality factor Q

$$\frac{I_r}{I_c} = \frac{4}{\pi Q} \tag{2.49}$$

2.3.3 Effect of Thermal Activation

So far, we discussed the characteristic behaviors of Josephson junctions at zero temperature. In the tilted washboard model, thermal fluctuations cause the representative phase particle to oscillate in the potential well. For an **underdamped junction**, the phase point has opportunity of escaping the well with an attempt frequency ω_A when the current is smaller than I_c

$$\omega_A = \omega_p \left[1 - (I/I_c)^2\right]^{1/4} \tag{2.50}$$

Recall ω_p is the plasma frequency $\omega_p = 1/2\pi\tau_J$. Each attempt comes with success rate $\sim e^{-\Delta U(I)/k_B T}$ to escape to the next minimum. With small damping, the phase particle can continue to run down the washboard potential once it accumulates enough momentum. In terms of the IV characteristics, this process leads to *premature switching*. The barrier height ΔU depends on the current and can be approximated

$$\Delta U(I) \approx 2E_J \left(1 - I/I_c\right)^{3/2} \tag{2.51}$$

As the current is swept close to the critical current I_c, the likelihood of escape scales exponentially and this stochastic process leads to a distribution of measured switching current I_s. The relation between the mean switching current I_s and the critical current I_c is given by [21]

$$< I_s >= I_c \left\{1 - \left[(k_B T/2E_J) \ln\left(\omega_p \Delta t/2\pi\right)\right]^{2/3}\right\} \tag{2.52}$$

where Δt is the time interval one takes to sweep the interval of around I_s. From this distribution, we can see that the mean of the I_s is skewed to less than I_c as temperature increases, and significantly reduced from I_c when $k_B T > 0.05 E_J$

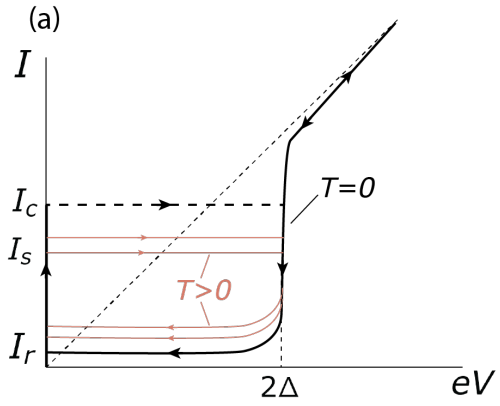


FIGURE 2.11: Effect of thermal activation on the IV curve characteristics for an underdamped junction. The thicker black curves indicate the case $T = 0$, and thinner orange curves represent the case $T > 0$.

For an **overdamped junction**, the phase point cannot just run away down the washboard potential from a single escape over the barrier like in the underdamped case. The heavy damping will bring it back into equilibrium over the next potential minimum. This process results in a diffusive movement over the barriers, and a finite nonlinear resistance R_0 even below the switching current I_s. In the Ambegaokar-Halperin theory [22], an important parameter that characterizes the activation energy is

$$\gamma_0(T) = \frac{2E_J(T)}{k_B T} = \frac{\Phi_0 I_c(T)}{\pi k_B T} \tag{2.53}$$

As $I \to 0$, this finite nonlinear resistance is related to the normal-state resistance by the modified Bessel function I_0:

$$R_0 = \lim_{I\to 0} \frac{\langle V \rangle}{I} = R_N \left\{ \mathcal{I}_0 \left[\frac{\gamma_0(T)}{2} \right] \right\}^{-2} \tag{2.54}$$

In the case of $\gamma_0 \gg 1$,

$$\frac{R_0(T)}{R_N} = \frac{\hbar I_c}{e k_B T} e^{-\frac{\hbar I_c}{e k_B T}} \tag{2.55}$$

We can see from figure 2.12, as γ_0 decreases from ∞ to 0, the IV curve for an underdamped junction shifts closer to resemble the linear ohmic curve as we would expect at high temperature.

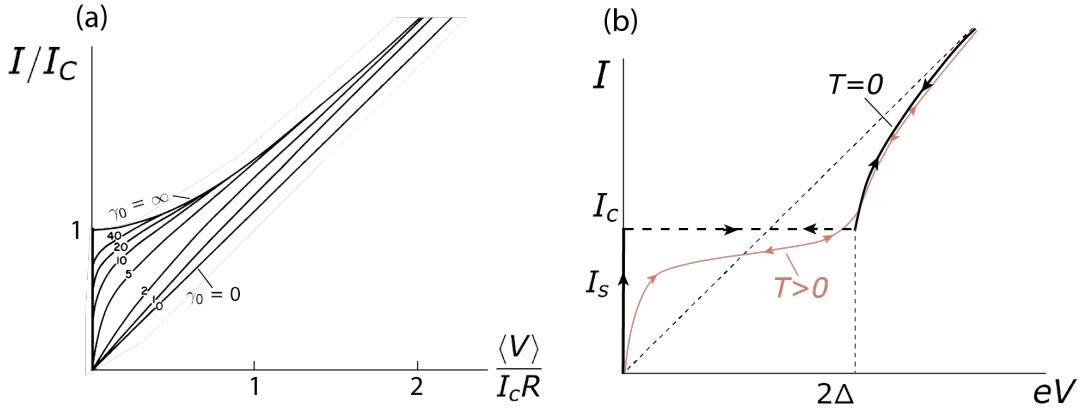


FIGURE 2.12: Effect of thermal activation on the IV curve characteristics for an overdamped junction. **(a)** Current normalized by critical current I_c vs. voltage normalized by $I_cR(V)$ for γ_0 of different values. Figure from Ref [22]. **(b)** The typical IV characteristics after considering the voltage dependence of the junction resistance. The black curve indicates the case $T = 0$, and orange curve represents the case $T > 0$.

2.4 Josephson Junction in a Transmon Qubit

In this section, we discuss the role that Josephson junctions play in transmon qubit, the most widely adopted superconducting qubit architecture today and the present workhorse of modern quantum computation.

2.4.1 Josephson junction as a nonlinear inductor

Let's first consider a simple quantum harmonic oscillator (QHO) made of a linear inductor L and a linear capacitor C, as shown in Figure 2.13 (a). We write down its

quantum-mechanical Hamiltonian:

$$\hat{H}_{\mathrm{QHO}} = 4E_c\hat{n}^2 + \frac{1}{2}E_L\hat{\varphi}^2 \tag{2.56}$$

where $E_C = e^2/(2C)$ is the charging energy for adding one electron to the island (the factor of 4 reflects Cooper pairs are the basic unit in superconducting state), and $E_L = (\Phi_0/2\pi)^2/L$ is the inductive energy. Here we work in the space of phase and charge number operator, which form a canonical conjugate pair $[\hat{\varphi}, \hat{n}] = i$. This Hamiltonian takes a quadratic potential energy that gives rise to eigenstates of equally spaced energy levels, i.e. $E_{k+1} - E_k = \hbar\omega_r$ with

$$\omega_r = \sqrt{8E_LE_c}/\hbar = 1/\sqrt{LC} \tag{2.57}$$

as shown in Figure 2.13 (c). The equal spacing of energy levels is problematic when we want to define a qubit with two computational states, $|0\rangle$ and $|1\rangle$, whose transition needs to be uniquely addressed, since the microwave tone $\hbar\omega_r$ can drive transition between arbitrary adjacent levels.

The solution for resolving the unwanted linearity in the QHO is by replacing the linear inductor with a Josephson junction. Let's recall the two equations governing the current and voltage dynamics of a Josephson junction, (2.26) and (2.27):

$$I = I_c \sin\varphi(t)$$
$$V = \frac{\Phi_0}{2\pi}\frac{d\varphi}{dt}$$

Combining these two equations with the definition of inductance $V = L(dI/dt)$, we can derive the Josephson inductance:

$$L_{\mathrm{J}} = \frac{\Phi_0}{2\pi I_{\mathrm{c}}\cos\varphi} \tag{2.58}$$

which is nonlinear with respect to phase φ due to the cosine function. When shunting a Josephson junction with a capacitor, we obtain an anharmonic oscillator, called a Cooper pair box. Similar to equation equation (2.56), we can write down its

Hamiltonian

$$H = 4E_{C_\Sigma}\hat{n}^2 - E_J\cos(\hat{\varphi}) \tag{2.59}$$

where $E_C = e^2/(2C_\Sigma)$, $C_\Sigma = C_s + C_J$ is the total capacitance including the intrinsic Josephson capacitance C_J and the shunt capacitance C_s, and $E_J = I_c\Phi_0/2\pi$ is the Josephson energy. After introducing the nonlinearity with the Josephson junction, we see that the potential energy is no longer quadratic but rather sinusoidal. This results in energy levels not evenly spaced (e.g. $\hbar\omega_{01} \neq \hbar\omega_{12}$), as shown in Figure 2.13 (b). In this case, the transition between the ground state and the first excited state can be uniquely addressed without significantly exciting higher level states. The ground and first excited levels therefore can form a computational subspace, representing the qubit $|0\rangle$ and $|1\rangle$ states.

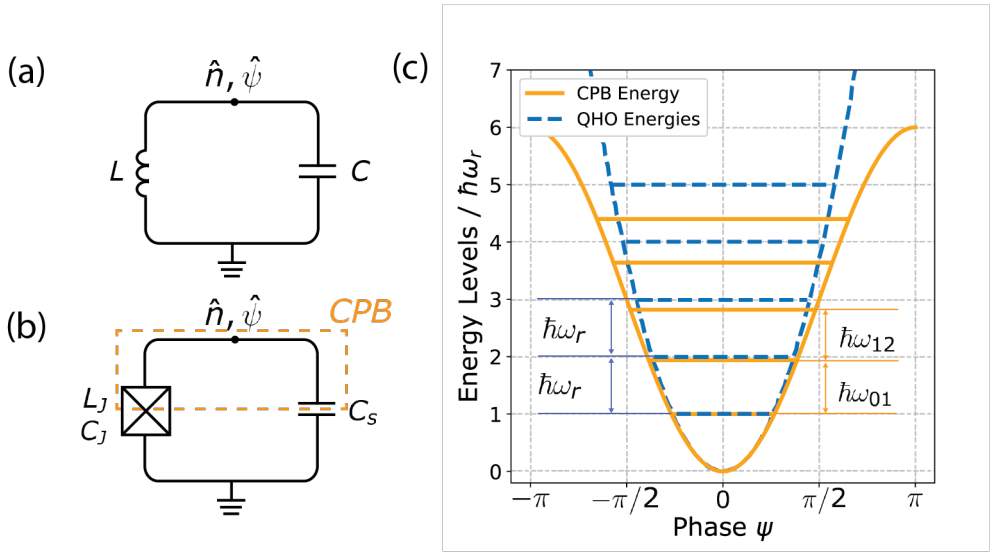


FIGURE 2.13: **(a)** Schematics of a quantum harmonic oscillator (QHO) made of a linear inductor and capacitor **(b)** Schematics of a Cooper pair box (outlined by the orange box), where the linear inductor in the QHO is replaced by a Josephson junction. **(c)** Comparison of potential energy and corresponding eigenenergy levels of QHO and the CPB.

2.4.2 Charge Qubit and Transmon Qubit

As we learned from the previous section the Josephson junction comes with intrinsic capacitance due to its parallel-plate geometry. Additional capacitors and inductors can also be added to modify the qubit energy spectrum and dynamics. The charge qubit operates in the regime $E_c \gg E_J$, whereas in the transmon architecture, the Josephson junction is shunted by large capacitor so that $E_c \ll E_J$. In this section, we will explore how E_J and E_c affect the qubit energy spectrum.

Let's first look at a **charge qubit**. Since it is in the limit $E_c \gg E_J$, charge fluctuation is relatively small compared to phase fluctuation. Therefore the charge number n is a good quantum number to work with. When applying a gate voltage V_g to qubit through a gate capacitor C_g as shown in Figure 2.14, the qubit Hamiltonian is slightly modified from equation (2.59)

$$\widehat{H} = 4E_{c_\Sigma}\left(\widehat{n} - n_g\right)^2 - E_\mathrm{J}\cos(\hat{\varphi}) \tag{2.60}$$

Here $C_\Sigma = C_J + C_g$ accounts for the total capacitance of the superconducting island, and n_g reflects the effective offset charge, $n_g = C_\Sigma V_\mathrm{g}/2e$.

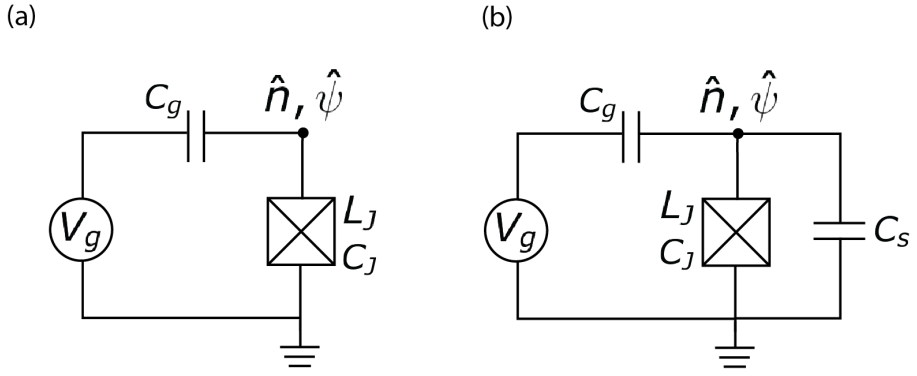


FIGURE 2.14: Circuit diagram for **(a)** charge qubit and **(b)** transmon qubit. Both qubits are coupled to an external gate voltage V_g by a gate capacitor C_g. Shunt capacitor C_s is zero for charge qubit, and a large value for transmon qubit.

By using the transformation between the canonical conjugate pair $\hat{n}, \hat{\varphi}$

$$|\varphi\rangle = \sum_{n=-\infty}^{\infty} e^{in\varphi}|n\rangle \tag{2.61}$$

$$|n\rangle = \frac{1}{2\pi}\int_0^{2\pi} d\varphi e^{-in\varphi}|\varphi\rangle \tag{2.62}$$

$$e^{i\hat{\varphi}}|n\rangle = |n-1\rangle \tag{2.63}$$

we can express the Hamiltonian fully in the charge number basis

$$\sum_n 4E_c\left(n-n_g\right)^2|n\rangle\langle n| - \sum_n \frac{E_J}{2}(|n\rangle\langle n-1| + |n-1\rangle\langle n|) \tag{2.64}$$

An example of charge qubit energy levels are plotted in Figure 2.15 (a) for the case $E_J = 0.1E_c$. Charge qubits are generally biased at the so-called sweep spots of $n_g = (2k+1)/2$ where the energy spectrum is first-order insensitive to charge noise. In order for the two-level system approximation of a qubit to be valid, we need to avoid regions close to integer n_g because $\hbar\omega_{01}$ and $\hbar\omega_{02}$ are degenerate at these points. Another advantage for setting the qubit at the sweet spots is that the qubit anharmonicity, i.e $\hbar\omega_{01} - \hbar\omega_{21}$, is the largest at these points as shown in 2.15 (b).

Transmon qubits, on the other hand, operate in the regime $E_J \gg E_c$. The most significant benefit of the transmon qubit is its insensitivity to charge noise as a result of a flattened energy spectrum. However, the immunity to charge noise comes at the cost of small anharmonicity. Figure 2.15 (c),(d) demonstrate an example of the flat transmon energy levels and the small anharmonicity for the case of $E_J/E_c = 30$.

In this limit, the phase spread is small compared to charge fluctuation, so phase φ is a good quantum number. We can expand the cosine term in the Josephson potential energy into a power series

$$E_J\cos(\hat{\varphi}) = \frac{1}{2}E_J\hat{\varphi}^2 - \frac{1}{24}E_J\hat{\varphi}^4 + \mathcal{O}\left(\hat{\varphi}^6\right) \tag{2.65}$$

With the first quadratic term alone we have a quantum harmonic oscillator, with resonant frequency $\omega_r = \sqrt{8E_JE_C}$. The 4-th order term can then be treated by

applying perturbation theory. After including the anharmonic correction, it can be shown

$$E_{01} = \sqrt{8E_C E_J} - E_C$$
$$E_{12} = \sqrt{8E_C E_J} - 2E_C \tag{2.66}$$

Therefore, the anharmonicity α is given by the expression $\alpha = E_{12} - E_{01} = -E_c$. In a transmon qubit design, one needs to balance E_c such that $E_c \ll E_J$ in order to suppress charge sensitivity while maintaining sufficient anharmonicity so it can still be effectively treated as a two-level system. Typically, for qubit frequency $\omega_{01} = (\sqrt{8E_C E_J} - E_C)/\hbar$ in the range of 3-6 GHz, E_c is designed to be 100-300 MHz.

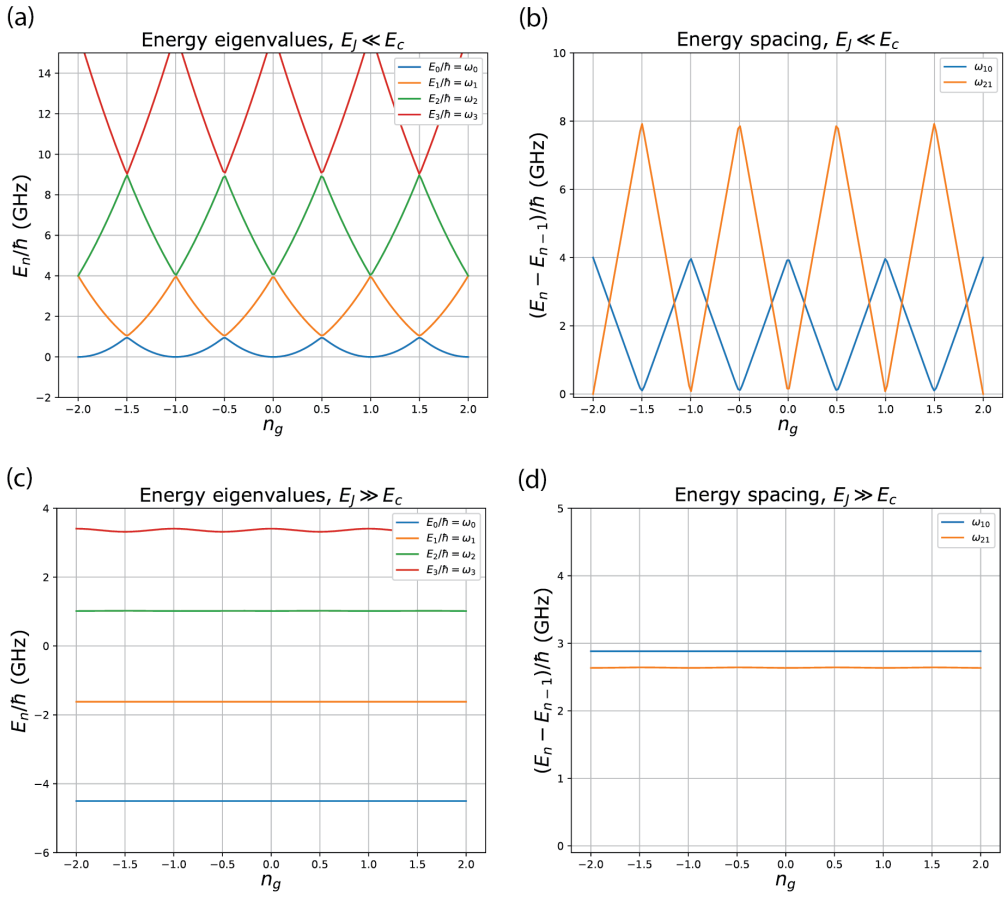


FIGURE 2.15: Energy spectrum for **(a)** Charge qubit regime, $E_J \ll E_c$ ($E_J = 0.1E_c$ plotted), energy level degeneracy appears at integer n_g **(c)** Transmon qubit regime, $E_J \gg E_c$ ($E_J = 30E_c$ plotted), the degeneracy is lifted at integer n_g, and energy spectrum is insensitive to charge fluctuations.

The coherence time for charge qubit [23] and its close variant, quantronium [24], is typically in the hundreds of nanoseconds range, which is mostly limited by environmental charge noise. The transmon coherence has improved significantly since it was first introduced by Schoelkfopf and colleagues [25] in 2007. For over a decade, advances in qubit design, fabrication techniques, and materials have all contributed to increasing the qubit coherence time to the range of 100-200 µs for fixed frequency transmons, and 50-100 µs in tunable transmons.

2.5 Materials Origin of Superconducting Qubit Decoherence

In the standard Bloch-Redfield picture, a quantum state of qubit can be represented by a Bloch vector

$$|\varphi\rangle = \alpha|0\rangle + \beta|1\rangle = \cos\frac{\theta}{2}|0\rangle + e^{i\varphi}\sin\frac{\theta}{2}|1\rangle \tag{2.67}$$

where $|\alpha|^2 + |\beta|^2 = 1$ for a pure quantum state, and $\theta \in [0, \pi]$ is the longitudinal angle, $\varphi \in [0, 2\pi)$ is the transverse angle, also the relative phase between $|0\rangle$ and $|1\rangle$ state components. This description of a quantum state can be visualized on a Bloch sphere as shown in Figure 2.16.

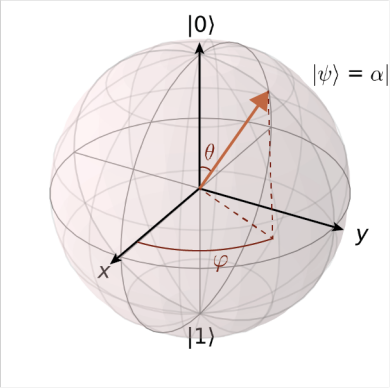


FIGURE 2.16: Bloch sphere representation of the quantum state $|\alpha|^2 + |\beta|^2 = 1$. The north pole and south pole of the sphere indicates pure quantum state of $|0\rangle$ and $|1\rangle$ respectively.

In isolation, the evolution of such a quantum state is deterministic and the qubit remains coherent. However, in an open system, superconducting qubits can interact with uncontrollable degrees of freedom either in the environment or from the control electronics. These interactions lead to qubit decoherence, that is, the qubit loses its defined phase relation between the two states $|0\rangle$ and $|1\rangle$. The main challenge for manipulating any quantum object, especially a large-scale quantum computer that consists of many individual smaller systems, is to keep the them isolated from the unwanted environmental noise while maintaining reliable interaction for control and readout purpose.

There are two decay rates that characterize the time scale over which qubit remains coherent:

$$\text{longitudinal relaxation rate } : \Gamma_1 \equiv \frac{1}{T_1} \tag{2.68}$$

$$\text{transverse relaxation rate } : \Gamma_2 \equiv \frac{1}{T_2} = \frac{1}{2T_1} + \frac{1}{T_\varphi} \tag{2.69}$$

The longitudinal relaxation rate Γ_1 describes qubit energy loss to the environment in the process of relaxing from the excited state to the ground state. Noise at the qubit frequency mediates a transition between the ground and excited states. Since the superconducting qubit is normally operated at dilution refrigerator temperatures ($\sim$20 mK) well below the transition energy (2-10 GHz), the qubit generally spontaneously emits energy to the cold environment in this process. For this reason, T_1 is also called the qubit excited-state lifetime, since it is the time scale over which the qubit excited state survives. The transverse relaxation rate Γ_2 is associated with the loss of the relative phase of a superposition state, which arises from two processes. First is pure dephasing characterized by $\Gamma_\varphi = 1/T_\varphi$. Second, longitudinal relaxation also leads to decoherence, because when it occurs, the superposition state loses the excited state component and the phase information is lost.

2.5.1 TLSs in Amorphous Oxides

Although there are many sources of noise in the environment, energy loss and fluctuations due to parasitic coupling to microscopic two-level-systems (TLSs) that exist ubiquitously in amorphous materials have been identified as the major culprit

of decoherence in superconducting qubits [26, 27]. Amorphous dielectrics are introduced to superconducting circuits either by design, as tunneling barriers, or unintentionally as the device surface oxidizes when exposed to air.

The microscopic mechanism of TLSs is often associated with atoms or electrons tunneling between two quantum states. These systems can originate from literal movement of dangling electronic bonds (such as OH-), hydrogen atoms and other defects in amorphous oxides, or collective motions of small atomic groups. Although the exact microscopic origins of TLSs are still elusive, we can still describe the physical dynamics of TLSs relatively well with the standard tunneling model (STM). In this model, TLSs exist in a double-well potential with two potential minima separated by a barrier. There exists two eigenstates of energy difference ΔE. Thermal energy can assist TLSs hopping between the two potential wells, and when temperature is sufficiently low quantum tunneling across the barrier becomes dominant at tunneling rate Λ.

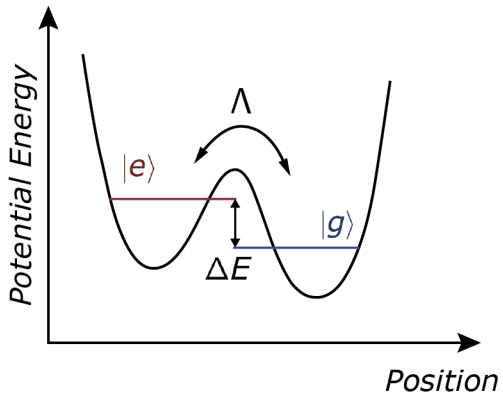


FIGURE 2.17: The standard tunneling model for TLSs, which is a double-well potential with two spatial eigenstates $|g\rangle$ and $|e\rangle$ in each of the potential wells. At low temperature, thermal activation is suppressed and quantum tunneling (at rate Λ) dominates the dynamics of the TLSs.

2.5.2 TLSs Interactions with Superconducting Quantum Circuits

Depending on how strongly TLSs couple to their own environment, they can exhibit either incoherent or coherent dynamics. Incoherent TLSs interact strongly

with their environment, which includes a number of different possible dynamical systems such as phonon modes, bath of other TLSs, and quasiparticles. These environmental processes can enable incoherent transitions between the TLSs eigenstates, as well as fluctuate their energy levels. As a result, incoherent TLSs often appear as fluctuators and contribute to low frequency noise, which leads to dephasing of the quantum devices [28]. When TLSs are isolated well from their own environment, they can coherently couple to their host quantum circuits and exchange energy with them. When the TLSs and qubit energy splittings become degenerate, they hybridize and are manifested as avoided level crossings in the qubit spectrum. This type of coherent interaction between TLSs and qubit have been shown to limit both qubit coherence and measurement fidelity.

For the scope of this thesis, we will limit our discussion to TLSs in Josephson junctions, even though TLSs at device interfaces are also a major source of noise and active area of research [29, 30]. There are two major mechanisms through which TLSs trapped in the tunneling barrier can interact with their host quantum circuit. In the first model, the electric dipole of charge-polarized TLSs can directly couple to the oscillating electric field between the two parallel plates of Josephson junction. Due to the small barrier thickness (normally ~ 10 Å), the electric field within a junction can reach several hundred V/m. Strong electric dipole coupling with TLSs leads to energy loss through resonance absorption by the TLSs. In the second model, the two eigenstates of TLSs are thought to be associated with different critical current values with difference δI_c. Fluctuations of the critical current directly couple to the Josephson energy $\delta E_j = \frac{\Phi_0}{2\pi}\delta I_c$ and hence modify the qubit frequency and result in qubit dephasing. This coupling to the critical current are often thought to contribute to $1/f$ noise measured in Josephson junction devices [31, 32].

2.5.3 TLSs Noise Mitigation

Since the first coherently-controlled Cooper pair box was developed in 1999 [23], significant progress has been made to improve superconducting qubit coherence time over five orders of magnitude. Advances in circuit design, device fabrication, and material science have all contributed to mitigating the impact of TLSs on qubit coherence.

Qubit Design Improvements

Here we briefly mention the two design modifications that considerably decreased qubit susceptibility to TLSs. The first change is to simply shrink the junction size so that the total number of TLSs trapped in the junction is reduced, even though the TLSs density has not changed significantly. Figure 2.18 shows an early work done by Martinis et al. [10] that demonstrated qubits with smaller-area junctions exhibited fewer TLSs and longer qubit coherence times. Another design philosophy that has notably increased qubit coherence is removing lossy dielectric wherever possible. The superconducting qubit community has come to favor coplanar capacitors in the form of two large electrode pads or interdigitated fingers where of the electric field is contained in vacuum. On the contrary, a parallel plate capacitor has almost all electric field contained inside the dielectric where TLSs is most concentrated. However, the trade-off of a coplanar design for shunt capacitor is a large footprint that often dominates the physical size of the entire qubit.

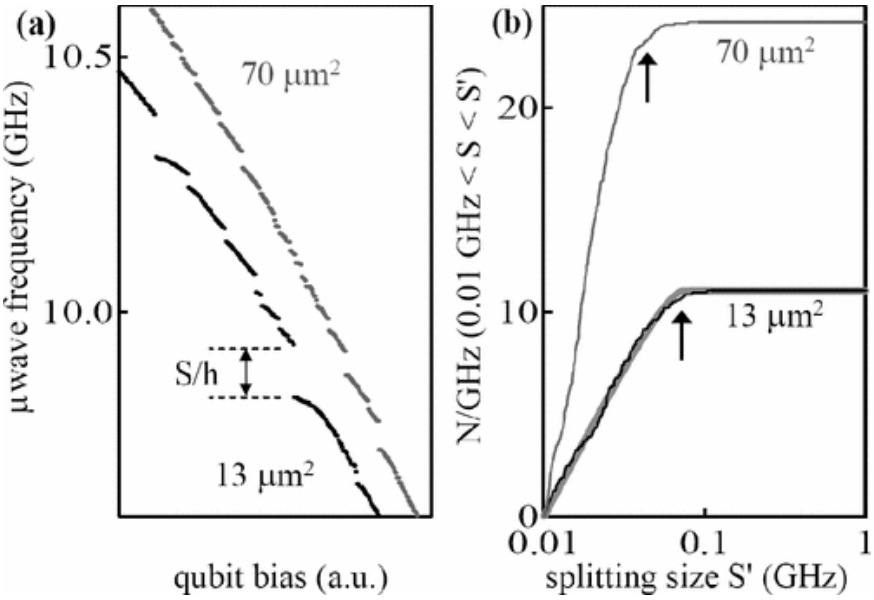


FIGURE 2.18: **(a)** Spectroscopy scan of Josephson phase qubit. By sweeping the bias current, qubit frequency can be adjusted. Avoided level crossings in the qubit spectrum show qubit hybridization with TLSs in the junction. Smaller-sized junction shows less avoided crossings with TLSs **(b)** Comparison of splitting size distribution for the small and large junction. Reprinted with permission from Reference [10].

Material & Fabrication Improvements

The conventional approach [33–35] for fabricating Josephson tunneling barriers over the past 40 years has been growing a few *nm* of native aluminum oxide AlO_x on top of an aluminum base layer. The controlled oxidation process happens in-situ between a double-angle shadow evaporation of aluminum. However, this amorphous AlO_x is known to display inhomogeneous thickness and surface roughness [36, 37], in addition to hosting measurable TLSs. A few attempts have been made to grow crystalline aluminum oxide [38–40] or build the entire tunnel junction with epitaxial materials [41]. These crystalline tunnel barriers displayed less TLSs density compared with their amorphous counterpart. However, qubits made with these types of junctions have often shown little or no improvement in terms of qubit lifetime and coherence time, likely due to less mature fabrication and design processes compared to the standard shadow evaporation.

Although the endeavor on material science front has so far been exploratory, for the purpose of scaling up quantum devices in the long term, it is of paramount importance to drive effort in search of new materials that intrinsically host fewer TLSs.

Chapter 3

Overview of Van der Waals Materials

3.1 Macroscopic Properties of Van der Waals Materials

Two dimensional van der Waals materials consist of crystalline planar layers that are held together by a weak van der Waals force. Therefore the layers can be easily separated by micro-mechanical cleavage. Since the first successful separation of graphene [42] (monolayer carbon atoms arranged in tight honeycomb structure), the interest in vdW materials has exploded with new discoveries coming out on a daily basis. Even though graphene attracted the most attention due to its very unique band structure and high electron mobility, people soon discovered that the vdW family hosts materials that span the full range of electronic properties, including superconductors, metals, semiconductors, and insulators, as shown in Figure 3.1. Although the electronic properties differ dramatically between different vdW materials, they are all known for their exceptional crystalline quality. The isolated layers are found to be atomically flat, free of dangling-bonds and intrinsic defects.

What makes vdW materials even more appealing is the freedom to mix and match different vdW flakes like LEGO® bricks and stack them into heterostructures that can achieve desired electronic characteristics. The development of dry-transfer techniques[14] allows vdW heterostructure assembly to be accomplished with pristine interfaces that best preserve the vdW materials' intrinsic properties.

Despite the flexibility and cleanness that the dry-transfer method offers, it is not scalable by nature because the manual assembly processes needs to be tailored for each different stack. On the contrary, bottom-up synthesis of vdW heterostructures

such as chemical vapor deposition (CVD) growth, combined with lithographic fabrication techniques, will ultimately offer the large scale possibility. Though currently limited by the sensitive growth condition, CVD grown vdW heterostructures have made significant advancement [43, 44] in the past decade, paving ways for long-term scalability of vdW electronics.

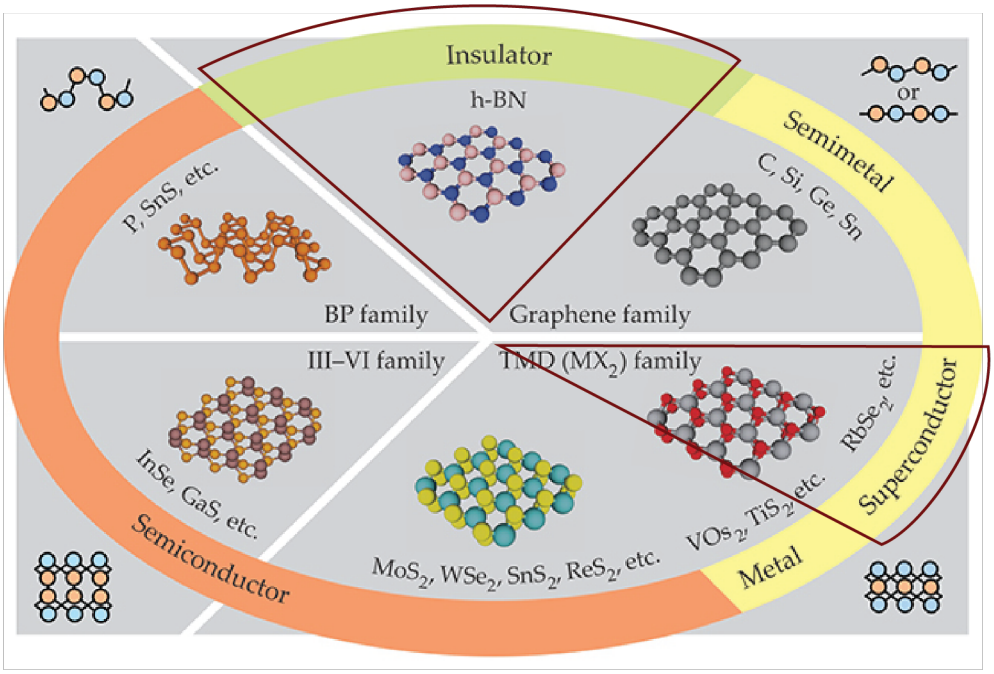


FIGURE 3.1: The world of van der Waals materials includes materials with vastly different composition and electronic properties. We are focused on vdW superconductors and insulators for the purpose of building superconducting quantum circuits. Adapted with permission from Ref [13].

The two necessary building materials for superconducting quantum circuits are superconductors and insulators. For example, Josephson junctions and parallel-plate capacitors can both be constructed with a superconductor-insulator-superconductor sandwich structure. So we will focus the discussion on suitable vdW superconductors and insulators in the following sections.

3.2 Van der Waals Superconductor – $NbSe_2$

The family of transition-metal dichalcogenides (TMDs) includes materials with the chemical formula MX_2, where M is a transition metal and X is a chalcogen such as S, Se, or Te. VdW TMDs are also layered materials consisting of a monolayer of transition-metal atoms sandwiched between two chalcogen atom layers, typically measuring $\sim$ 1 nm per combined MX_2 layer. TMDs have a wide range of electronic properties due to the many permutations of transition-metals and chalcogens. Among the TMD superconductors, niobium diselenide ($NbSe_2$) exhibits the highest superconducting critical temperature $T_c \approx 7.2$ K for the bulk material. Its superconductivity persists down to monolayer, although the T_c and superconducting gap decrease with the layer number[45], as demonstrated in Figure 3.2.

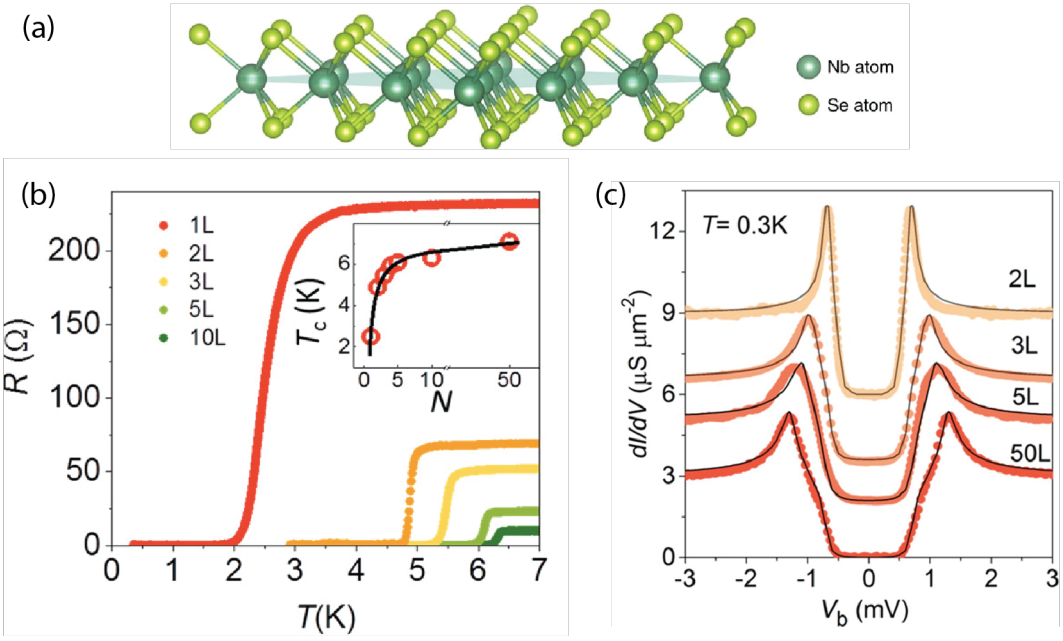


FIGURE 3.2: **(a)** Atomic structure of the two-dimensional superconducting NbSe2. Adapted with permission from Ref [46]. **(b)** Superconducting transition in few-layer $NbSe_2$ by transport measurements. **(c)** $NbSe_2$ tunneling conductance dI/dV as a function of bias voltage V_b, measured with electron tunneling spectroscopy. (b),(c) Adapted with permission from [45]. Copyright (2018) American Chemical Society.

It should be noted that $NbSe_2$, like all other TMD superconductors (NbS_2, $TaSe_2$,

TaS_2), oxidizes rapidly when exposed to ambient conditions [47]. Therefore extra protection should be applied when handling such oxygen-sensitive materials. Exfoliation and assembly of $NbSe_2$-based heterostructures should be performed in an oxygen-free environment. Encapsulation with hBN or graphene has also been shown to protect $NbSe_2$ from oxidation. There is some good news, however: transmission electron microscopy image has revealed that the surface oxidation would self terminate at a few nm, preserving the electronic properties of the crystalline materials inside [48]. Therefore, as long as the $NbSe_2$ flakes are thicker than 10 nm, we do not need to be overly concerned with oxidation once the important interfaces are sealed.

3.3 Van der Waals Dielectric – hBN

Hexagonal boron nitride (hBN) is a vdW dielectric that shares the same crystal structure as graphene. Each monolayer of hBN is $\approx$ 0.33 nm thick. Owing to its atomically flat structure that is also free of dangling bonds and surface charge traps, hBN has been widely used as encapsulation layers that protect vdW devices from environmental disorders. The extraordinary electronic properties of graphene was only truly revealed after it was paired with the hBN encapsulation just a decade ago [49, 50]. Moreover, hBN can also serve as a robust gate dielectric due to its large direct band gap of 5.97 eV [51]. All of these properties of hBN make it an ideal candidate as the tunneling barrier for Josephson junctions, and the dielectric for parallel-plate capacitors.

Chapter 4

Device Fabrication & Measurement Techniques

4.1 Fabrication of $NbSe_2$-hBN-$NbSe_2$ Tunnel Junctions

This section is dedicated to the hand-on process of fabricating vdW Josephson junction devices. Figuring out a set of working fabrication procedures for new materials involves many iterations of trials and errors and is actually the major challenge of the project. Hopefully this detailed documentation will be useful for those who follow a similar line of work.

The fabrication of a $NbSe_2$-hBN-$NbSe_2$ tunnel junction typically follow these steps:

1. Preparing substrates
2. Cleaving and selecting van der Waals (vdW) flakes
3. Assembling the heterostructure with dry transfer techniques
4. Examining the vdW stack structure with an atomic force microscope (AFM)
5. Defining the electrode patterns with e-beam lithography
6. Making the electrical contacts to the junction stack

Note steps 2 and 3 are completed in an argon-filled glovebox in order to minimize oxidation of $NbSe_2$. In the following sections, we will describe each of these steps in more detail.

4.1.1 Preparing Substrates

There are two types of substrates we use in the fabrication process. The first is simply a bare Si chip with 90 nm of SiO_2 on top for exfoliation purposes, and does not require any special cleaning steps before usage. The other kind of substrate is used to host the final Josephson junction device, and requires pre-deposited alignment markers so that later we can design the electrodes on top of the junction stack with e-beam lithography. The markers are defined with e-beam lithography (exposed to e-beam resist), and then a metal (Au or Pt) is thermally evaporated onto the Si substrate, followed by a lift-off process. Since these marker substrates are exposed to polymers and solution chemicals in the process, we treat them with 5 min of oxygen plasma before usage in order to minimize organic residue seen by the device.

4.1.2 Cleaving and Selecting vdW Flakes

The VdW flakes are prepared by mechanical exfoliation from bulk vdW crystals using adhesive tapes. Despite the seemingly primitive process, it still produces the best quality vdW devices to date due to the high intrinsic quality of the crystal, compared with their chemical vapor deposit (CVD) grown counterpart. A small piece of crystal is transferred to the tape, and copied a few times until the crystal reached the desired thickness. Then the flakes on the tape are deposited to a substrate by pressing the tape on top of the substrate and then slowly peeling away. Since $NbSe_2$ is highly reactive at elevated temperature, we avoid using heat treatment during the exfoliation process.

A candidate $NbSe_2$ flake for the junction device should be 30-50 nm thick, and uniform in thickness. We select $NbSe_2$ flakes by optical inspection and comparing the flake's color to a reference flake that has multiple steps whose thickness was determined with an AFM measurement. Figure 4.1 shows the optical image and the AFM measured step heights of the reference flake.

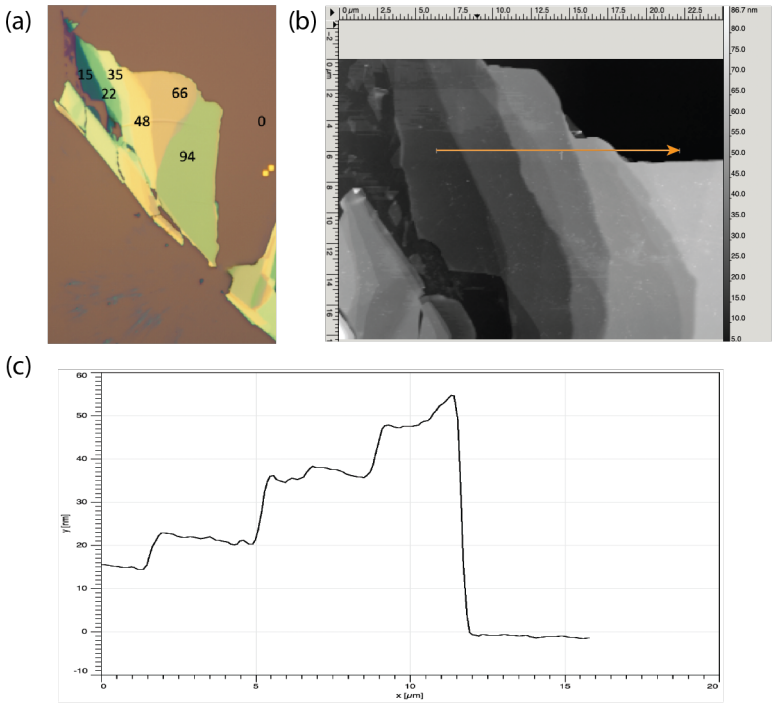


FIGURE 4.1: $NbSe_2$ reference flake. **(a)** Optical image of a reference flake that shows different colors in regions of different flake thickness. The number marks the flake thickness referenced to the substrate. **(b)** AFM image of the reference flake. **(c)** The AFM height profile of the line cut shown in (b). Arrow indicates the positive x direction.

It takes a little more work to hunt for a good tunneling hBN flake. Because our target thickness (0.6-1.5 nm for 2-5L hBN) is very small, flakes at this thickness are transparent in visible light and only faintly contrast with the SiO_2 substrate. A few optical tricks can be used to assist the identification process. First, we increase the optical contrast in the camera setting to make the thin flakes more obvious, as shown in Figure 4.2 (b). Then we use the red contrast of the flake to identify its layer number, inspired by the optical identification method described in Ref [52]. Using a reference monolayer hBN flake whose thickness had been identified by Raman spectroscopy, we determined that each hBN monolayer results in $\sim$ 2.5% reduction of red color value from its background, and this value increases linearly with number of hBN layers. This identification method provides a quick estimate of the hBN layer number and is reliable within the thickness range of our interest. Figure 4.2 (c) demonstrates an example flake shown in red-only image, which makes it easier to see areas of different thickness compared to the normal RBG image shown in (a).

From the red intensity profile in (d), we can calculate that the red optical contrast of the thinner area of the flake (the right half) is 9.8% reduced compared to its background, therefore it was estimated to be a 4-layer (4L) hBN flake. This flake was later used as the tunneling barrier for Josephson junction device 10, and the tunneling resistance measurement confirmed the hBN thickness to be 4L as detailed in section 5.2.1.

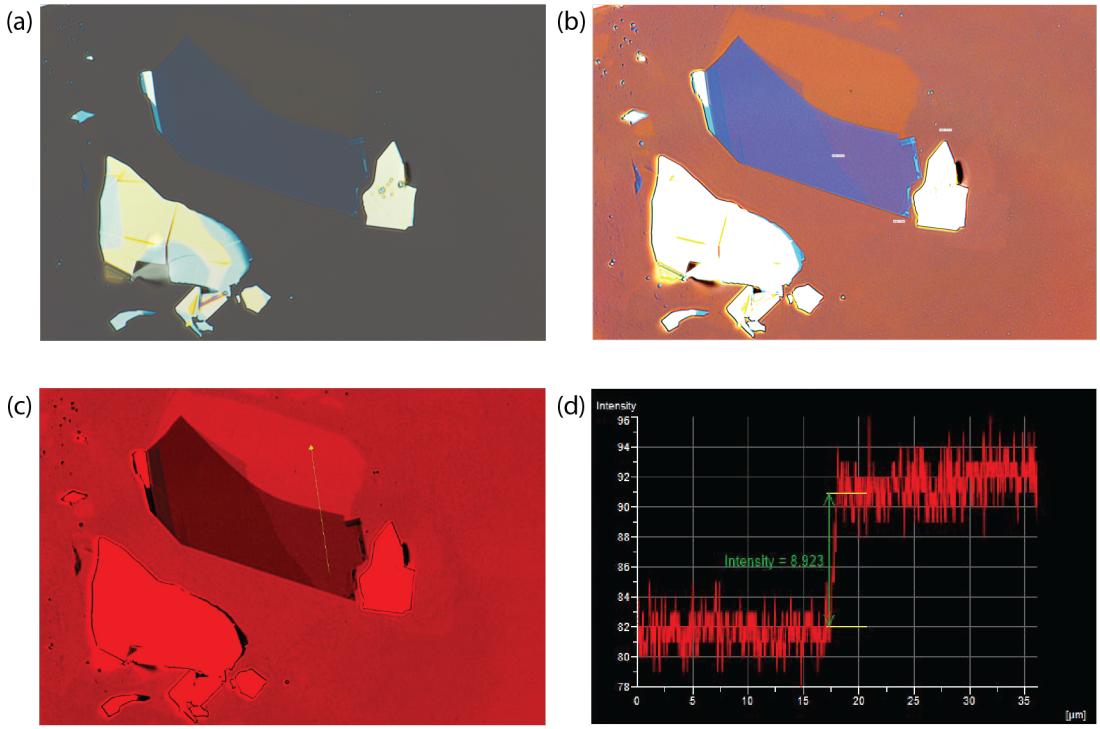


FIGURE 4.2: An example hBN flake shown in different optical settings. **(a)** Regular RGB image. **(b)** RGB image with enhanced contrast, which makes it easier to differentiate thin hBN flakes from their background. **(c)** Red-only image, which makes it easier to distinguish area of different hBN thickness. Dotted line outlines the 4L-hBN area that is later used in tunneling device 8. **(d)** The red intensity profile of the line cut shown in (c). The flake reflects a 9.8% contrast form its background, and therefore is estimated to be 4L thick.

4.1.3 Assembling vdW Heterostructure with Dry Transfer Techniques

The assembly of vdW heterostructures is the critical step where the junction interface is formed. Dry pick-up and transfer techniques [14] allow the interface to be free from polymer or chemical contamination. With the dry transfer method, we can directly pick up the thin hBN flake with a top $NbSe_2$ flake, which is made possible because the Van der Waals force between the $NbSe_2$ flake and the hBN flake is stronger than the adhesion between hBN and the rough SiO_2 surface.

The pick-up and transfer process utilizes a polymer "stamp", made with a small cushiony polydimethylsiloxane (PDMS) block and a polycarbonate (PC) film, as illustrated in Figure 4.4 (a). The PC film is the sticky surface used to pick up the top $NbSe_2$ flake and its adhesive strength increases with temperature until temperature reaches the melting point at 155°C. The PC film can be dissolved by rinsing in chloroform for 10 min.

Although the dry pick-up technique with PC film is widely used in the 2D materials community, it turned out that $NbSe_2$ flakes are especially difficult to pick up, which is suspected to result from their potential interactions with the SiO_2 surface that makes them stick stronger to the substrate. In order to successfully pick up the $NbSe_2$ flakes from the Si/SiO_2 substrate, it is important that we use flakes that are freshly exfoliated within a day. Another trick we discovered that increases the PC film adhesion is to treat the stamp with UV-ozone for a short period of time (90 seconds in our case). UV-ozone interacts with organic polymer and effectively makes the PC film surface rougher, which increases its stickiness. Using freshly exfoliated $NbSe_2$ flakes combined with UVO-treated PC has boosted our pick-up success rate to near 100%.

The transfer setup used for vdW heterostructure assembly is shown in Figure 4.3 (c), where the Si/SiO_2 substrate and PDMS-PC stamp are secured to the sample stage and transfer stage, respectively, by vacuum. We use two micro-manipulators to control the horizontal movement for the stack alignment and the vertical movement for engaging/disengaging the stamp and substrate. As illustrated in Figure

4.4, the stack assembly consists of three main steps. First, we pick up the top $NbSe_2$ flake with the PC film. Then we immediately proceed to picking up the tunneling hBN with the top $NbSe_2$, in order to quickly conceal the tunneling interface and minimize the $NbSe_2$ oxidation. The final step is depositing the half-stack on top of the selected bottom $NbSe_2$ on the Si/SiO_2 substrate prepared with alignment markers.

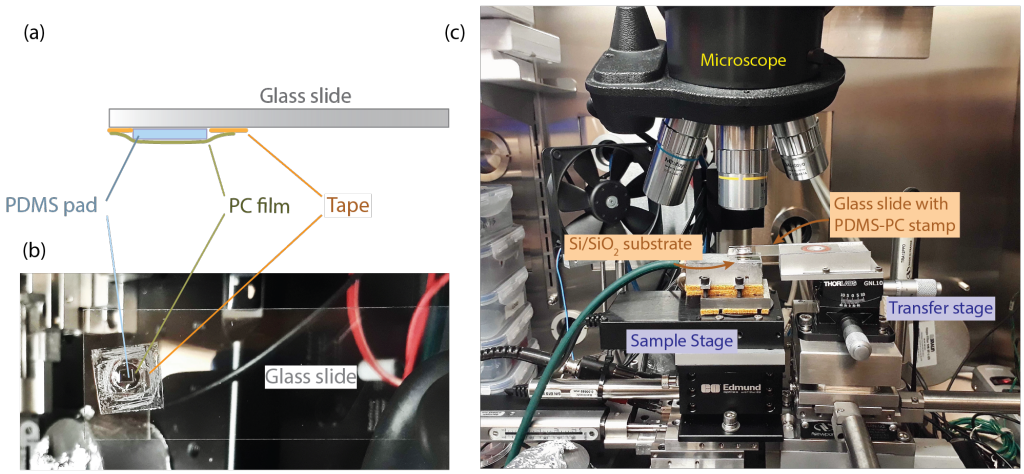


FIGURE 4.3: **(a),(b)** Illustration and picture of a PDMS-PC stamp on a glass slide. **(c)** Transfer setup for vdW heterostructure assembly inside an argon-filled glovebox. Micro-actuators are used to control the sample stage and the transfer stage movement both horizontally for alignment purpose and vertically for engaging/disengaging the stamp and substrate.

The detailed step-by-step recipe for assembling a complete $NbSe_2$-hBN-$NbSe_2$ stack is described as follow. Steps 2-4 are completed inside an argon-filled glovebox within 6 hours in order to minimize the $NbSe_2$ oxidation at the junction interfaces.

1. Treat PC-PDMS stamp with UV-Ozone for 90 second.
2. Pick up the top $NbSe_2$ flake
   (a) Heat the substrate to 60°C, and then use the micro-manipulator to slowly engage the stamp with the $NbSe_2$ flake on the substrate.
   (b) Heat the substrate to 90°C, and wait until the PC film fully conforms to the $NbSe_2$ flake.

(c) Keep the substrate temperature at 90°C, and slowly disengage the stamp by mechanically lifting up the transfer stage until the $NbSe_2$ flake is picked up.

3. Pick up the thin tunneling hBN flake

   (a) Carefully align the hBN flake with the top $NbSe_2$ flake by manipulating the transfer stage horizontally with the micro-actuator. Make sure the top $NbSe_2$ flake does not completely cover the hBN flake, which will lead to shorting between the two $NbSe_2$ flakes later.

   (b) Heat the substrate to 60°C, and slowly engage the top $NbSe_2$ flake with the hBN flake until the PC film fully conforms to both flakes.

   (c) Heat the substrate temperature at 90°C, and slowly disengage the stamp by mechanically lifting up the transfer stage until the hBN flake is picked up.

4. Drop the half-stack onto the bottom $NbSe_2$ flake

   (a) Carefully align the bottom $NbSe_2$ flake with the half-stack to define the junction area. Avoid shorting between the top and bottom $NbSe_2$ flakes.

   (b) Heat the substrate to 120°C, slowly engage the half stack with the bottom $NbSe_2$ until the wave-front moves past the stack. The reason we work at an elevated temperature in this step is to use more heat to force bubbles out of the junction area.

   (c) Heat the substrate to 160°C, slightly above the melting point of PC film. Then slowly lift up the stamp and the melted PC will stick to the substrate and release from the stamp.

5. Remove the PC film on the device substrate with a 3-step solvent clean

   (a) 10 min in chloroform

   (b) 1 min in acetone

   (c) 30 second in isopropyl alcohol (IPA)

   (d) Blow dry the chip with N_2

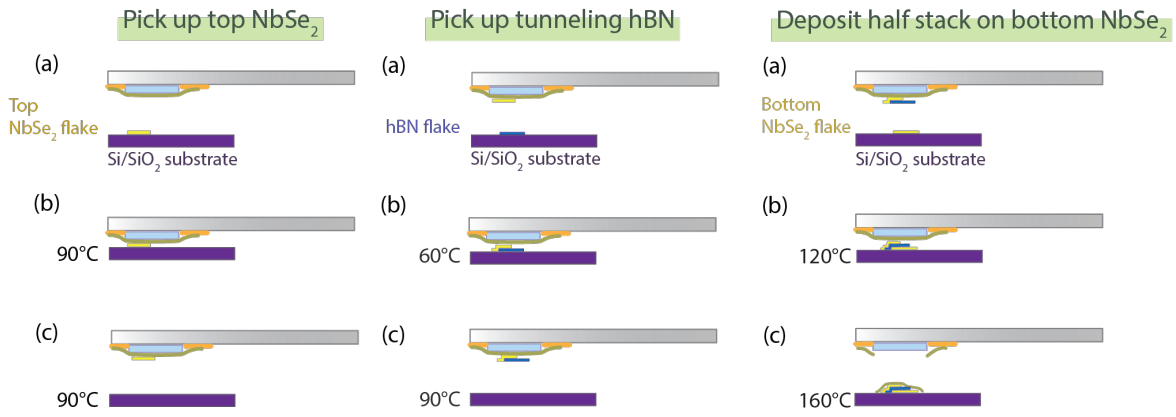


FIGURE 4.4: Illustration of vdW heterostructure assembly process. The three columns correspond to step 2-4 in the recipe. Note the size of vdW flakes are blown up for better visibility.

4.1.4 Examining vdW Heterostructure with an AFM

Before turning the assembled $NbSe_2$-hBN-$NbSe_2$ stack into a connected Josephson junction device, we need to check the junction quality with an AFM. There are three questions we would like to answer with the AFM measurement: (1) whether there is any shorting between the two $NbSe_2$ flakes, (2) if there is any notable structural defects within the junction area, and (3) whether the $NbSe_2$ flakes are thick enough (> 20 nm) to withstand the ion-milling process later. Figure 4.5 shows an example of the height and phase images from an AFM scan of a $NbSe_2$-hBN-$NbSe_2$ stack we made. In the phase image (b), we can see that hBN has a very smooth surface, compared with the more grainy surface of $NbSe_2$ and SiO_2, and thus can be easily distinguished. From the height image (a), we see a bubble of height $\sim$ 10 nm is present within the junction area. These types of structural defects are common, especially for junctions of a large area. We can also extract the thickness of the top and bottom $NbSe_2$ flakes to be $33(\pm 2)$ nm and $36(\pm 2)$ nm respectively.

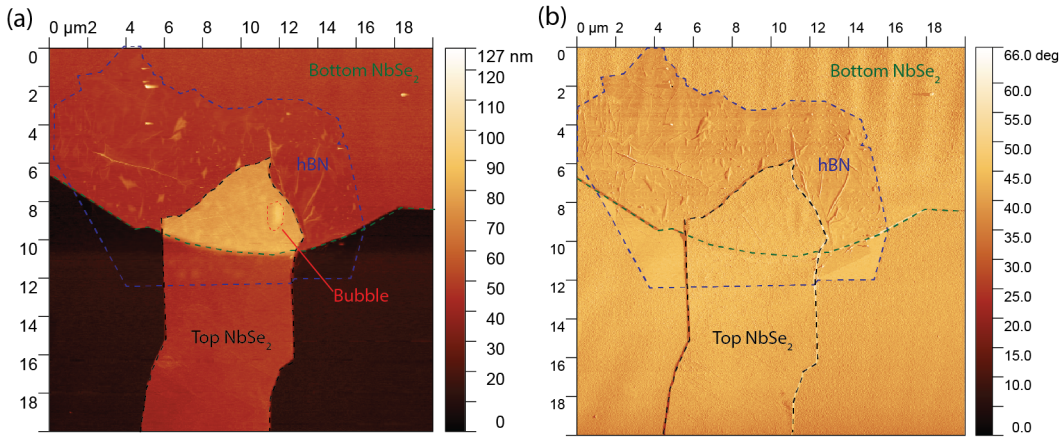


FIGURE 4.5: AFM scan of an example $NbSe_2$-hBN-$NbSe_2$ stack. **(a)** AFM height image. A bubble of height $\sim 10\,nm$ can be seen within the junction area. **(b)** AFM phase image. The outlines of the flakes are indicated by the dashed curves.

4.1.5 Ebeam Lithography

Now that our $NbSe_2$-hBN-$NbSe_2$ junction stack is examined, we proceed to patterning the electrodes for the stack. Here we use e-beam lithography for its design flexibility and nm-scale alignment accuracy. Because the e-beam lithography will be followed with an ion-milling step later, it is important that the resist is strong enough to withstand the etching. We choose to use a double-resist recipe that makes the resist extra thick and strong.

Spin Resist Two rounds of spinning PMMA 950 A5 at 3000 RPM for 45 second. Let the chip dry at room temperature for at least 5 minute between spins.

E-beam Lithography Use writing current $I = 10\,\text{nA}$, dose $= 3000\,\mu\text{C}\,\text{cm}^{-2}$, write field size = 500 µm, 50k dots per field, corresponding to dose time $= 0.3\,\mu\text{s/dot}$.

Cold Develop Use developing solution made with IPA:H_2O = 3:1 by weight. First keep the beaker with the solution in an ice bath for 2 min for proper thermalization. Then swirl the chip in the cold solution for 60 seconds and then blow dry with N_2.

After developing the e-beam patterns, chips are carefully examined under a optical microscope to check the pattern resolution. Figure 4.6 demonstrates an example

of well developed e-beam patterns: all edges and corners appear to be clean and sharp, without any smearing or misalignment.

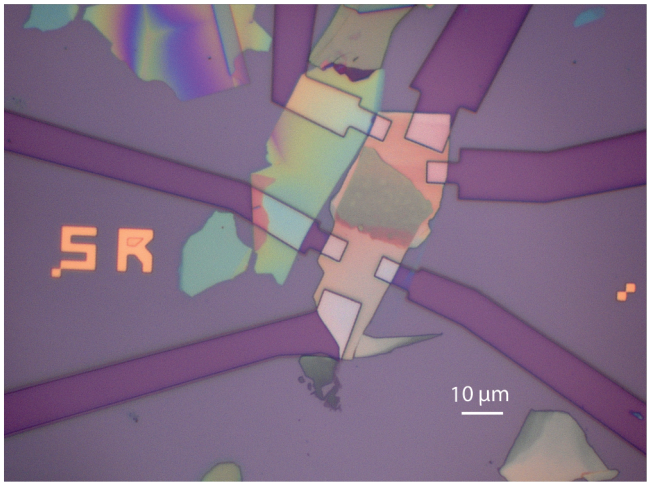


FIGURE 4.6: Microscopic image of an example junction stack with well developed e-beam electrode patterns. All edges and corners appear to be clean and sharp, without any smearing or misalignment.

4.1.6 Making Electrical Contacts

To make Galvanic contacts (i.e., electrical contacts without capacitive or inductive coupling) between the electrodes and $NbSe_2$ flakes, first we need to remove the top few oxidized $NbSe_2$ layers by ion-milling $\sim 10\,nm$ of the flakes, and then deposit superconducting Al in situ at $\sim 10^{-7}$ Torr vacuum. Finally, a standard lift-off process is followed to finish the process. Note since we used the double-resist recipe as stated in the previous section, the lift-off process requires a longer soak time and sometimes assisted peeling of the metal films. An example junction device with aluminum electrodes are shown in Figure 4.8.

The following ion-mill recipe has been calibrated to etch $\sim 10\,nm$ of $NbSe_2$. Figure 4.7 shows the AFM measurement of a calibration $NbSe_2$ flake after being etched with this recipe using a double-resist mask with 2 µm trench.

Ion Mill (With AJA system) Base pressure $1 - 3 \times 10^{-7}$ Torr, beam $400\,V/23.1\,mA$, accelerator $80\,V/4.3\,mA$, etching time 60 second.

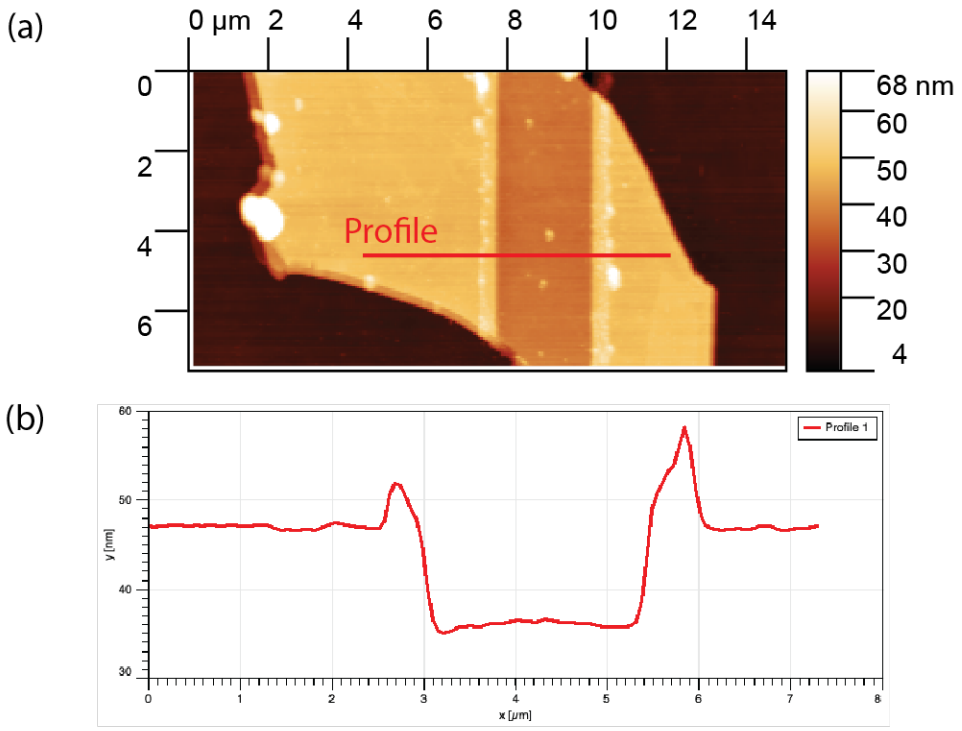


FIGURE 4.7: **(a)** AFM scan of a calibration $NbSe_2$ flake after 60 second of ion-milling using the recipe described in section 4.1.6. **(b)** AFM height profile of the line-cut indicated in (a). The $NbSe_2$ flake is etched by $11.2(\pm 1)\,nm$.

Immediately after the ion-milling is done, aluminum is deposited onto the chip with e-beam evaporation in the same system without breaking the vacuum.

E-beam evaporation of Aluminum Deposition pressure 10^{-7} Torr, current 47 mA, deposition rate 2 Å/s, Al thickness 100 nm.

Lift-off 6-8 hours in acetone. Squirt acetone on the chip with a squeeze bottle to gently peel away the Al films. Place the chip in a shallow watch glass filled with acetone. Check under an microscope for left over metal films while the chip is immersed in acetone in the watch glass. It is crucial to prevent the chip from drying before the lift-off process is completed, otherwise the films will collapse onto the chip and become very difficult to remove. Repeat the squirting process until all the unwanted metal films are lifted off.

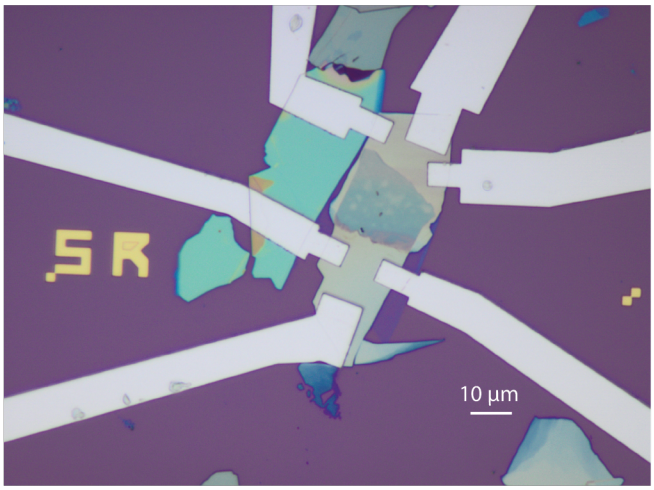


FIGURE 4.8: Microscope image of an example $NbSe_2$-hBN-$NbSe_2$ junction device with patterned Al electrodes that are made with the in-situ ion-milling and aluminum deposition processes.

4.2 Measurement Setup & Techniques

This section provides an overview of the cooling apparatus and electronic setup that is required to perform the Josephson junction measurement. We will briefly introduce where and how samples are mounted in the dilution refrigerator, and then move to more details about the electrical filtering and setup for the experiments.

4.2.1 Dilution Refrigerator

The experiments were performed in a BlueFors XLD dilution refrigerator (referred to as DR or *fridge* in the following text) system that provides an operating temperature well below the superconducting transition temperature of $NbSe_2$ ($T_c = 7\,\mathrm{K}$). A DR unit has different temperature stages that are limited by the different cooling mechanisms at each stage. The refrigerator mixing chamber (MXC) stage can be stably cooled to temperatures below 10 mK. The continuous cooling powder at low temperature is provided by the heat of mixing the two helium isotopes, ^{3}He and ^{4}He. Figure 4.9 shows the inside of the DR used in our experiments. The samples are mounted at the MXC stage, contained in two superconducting shields and a mu-metal shield.

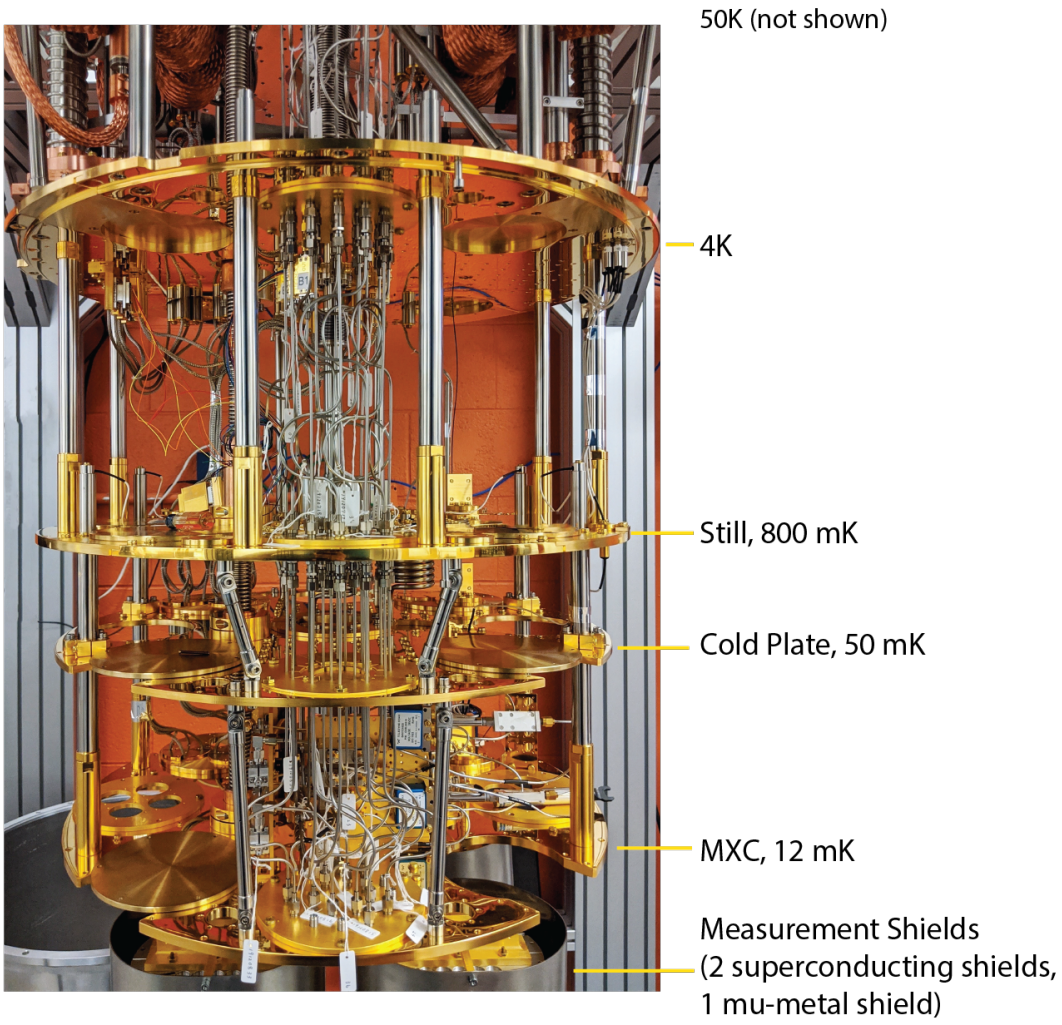


FIGURE 4.9: Picture of the BlueFors XLD DR unit we used to perform the experiments. Different temperature stages of the DR are shown in the image, as well as part of the measurement shields.

4.2.2 Device Wire-bonding & Mounting

To mount the sample chips, we use a dual in-line memory module (DIMM) board shown in Figure 4.10 (a). This DIMM board is designed to have 7 chip slots and each slot is equipped with 24 DC lines. We secure the sample chips onto the DIMM board with a drop of silver paste, and then make electrical connections by wire-bonding. The DIMM board mount is installed at the MXC stage of the DR, shown in 4.10 (b). It has the capacity to host two DIMM boards and therefore allows for as many as 14 chips to be measured simultaneously. On the mount, one micro d-sub

connector is allocated for each chip slot on the DIMM board to be connected to a DC loom. Currently there are 5 DC looms available for our experiments, although the capacity can be expanded in the future. Figure 4.10 (c) shows a complete setup with 5 chips wirebonded to the DIMM board and mounted on the DR.

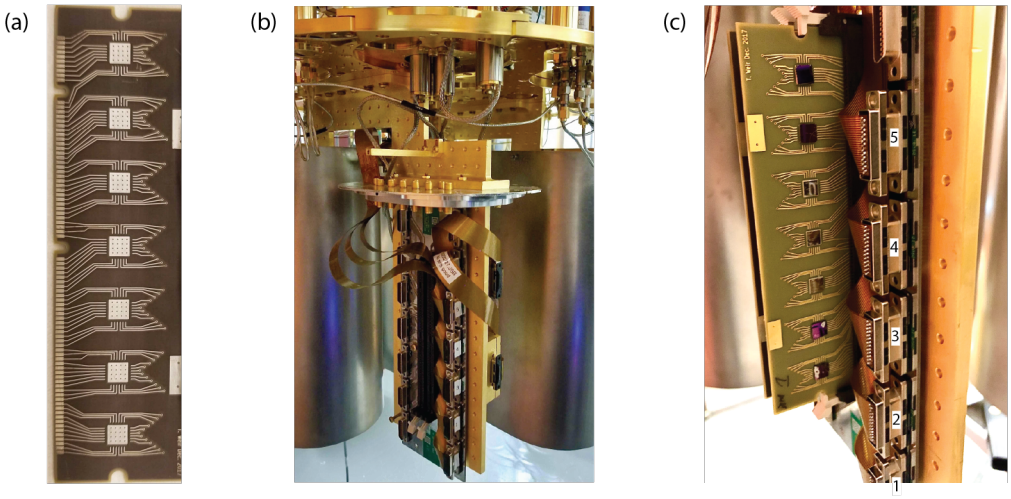


FIGURE 4.10: **(a)** Picture of DIMM board used to host the vdW Josephson junction sample chips. Each board has 7 available chip slots, with 24 DC lines for each chip. **(b)** Picture of the DIMM board mount secured to the dilution refrigerator MXC stage. Up to two DIMM boards can be installed on the mount, and each chip slot on the DIMM board can be connected to a 24-line DC loom. **(c)** Picture of a DIMM board with 5 sample chips installed on the mount. The top 2 chips on the DIMM board are blank place holders.

4.2.3 DC Line Filtering

Electrical wiring inside the DR is important not only because it provides electrical connections between the device under test and various measurement instruments, it also serves to thermalize the electrons that flow down to the device. The electron temperature is what actually sets the thermal activation level of the Josephson junctions, instead of the physical temperature at the device. Therefore special care should be taken to ensure the wires are properly thermalized and the thermal photons generated from high-temperature environments are filtered at various temperature stages in the DR.

There are typically two types of wiring insides a DR: RF and DC. We will limit

the discussion to DC lines here because RF lines are not used in our experiments. The BlueFors XLD DR we used is equipped with 8 DC looms, each containing 24 DC lines. Thermal anchors are placed at each temperature stage to secure and thermalize the looms.

A combination of cryogenic filters are installed along each DC loom to isolate the device form high-frequency noise, including a RC π filter at the 4K stage and a copper powder filter at the MXC stage. These two types of filters have complimentary filtering characteristics and a study [53] has shown that they offer an almost-ideal low-pass filtering when combined. Both types of filters are designed and built at the Lincoln Laboratory. The RC π filter utilizes a 50 Ω resistor and two capacitors of 30 nF, corresponding to a cut-off frequency $f_c = 53$ kHz. Typically, the attenuation of an RC filter decreases significantly beyond the 100 MHz range. Unlike RC filters, powder filters operate on the basis of the skin effect damping for strong attenuation at high frequencies above 300 MHz, where RC filters are less efficient. Therefore a broad-band low-pass filtering can be achieved when combining these two types of filters. We should also note that all filters are well thermalized at their respective bath temperature by having a large metal surface in contact with their host stage.

We discovered that with the $I - V$ measurements we performed, occasionally a voltage as high as 30 V could be applied between a DC line and the ground, when there is an open connection at the device end. Events like this could damage the RC filters. Therefore when it comes to choosing the RC filter cut-off frequency, although we would like to make it in the low kHz range, it is also necessary to consider the voltage limit of the capacitors used. Since smaller capacitors typically have higher voltage tolerance, we made the trade-off to increase the capacitor voltage limit to 35 V while still keeping the cut-off frequency at the 10 kHz range.

Before each cool down, it is important that we check the DC lines for any anomaly (open, short, or abnormal resistance) because it is almost impossible to locate and fix an issue once the fridge is sealed and cooled down. A well behaving DC loom should have all 24 lines well isolated from each other and ground. The end-to-end resistance of each DC line should be $\approx 50\,\Omega$, dominated by the resistance of the RC filter. Although a resistance measurement is straightforward, it soon becomes

very tedious and error-prone when we have 8x24=192 lines, and 192x192=36,864 potential shorting configurations to check. With the help of a Keithley 3706a switch matrix and a digital multimeter, we can automate the resistance measurement by programming the switch matrix to iterate through all the target DC lines and pairs of lines. Figure 4.11 shows a DC loom resistance map generated during a routine checkup, which revealed a few shorts between neighboring DC lines and ground.

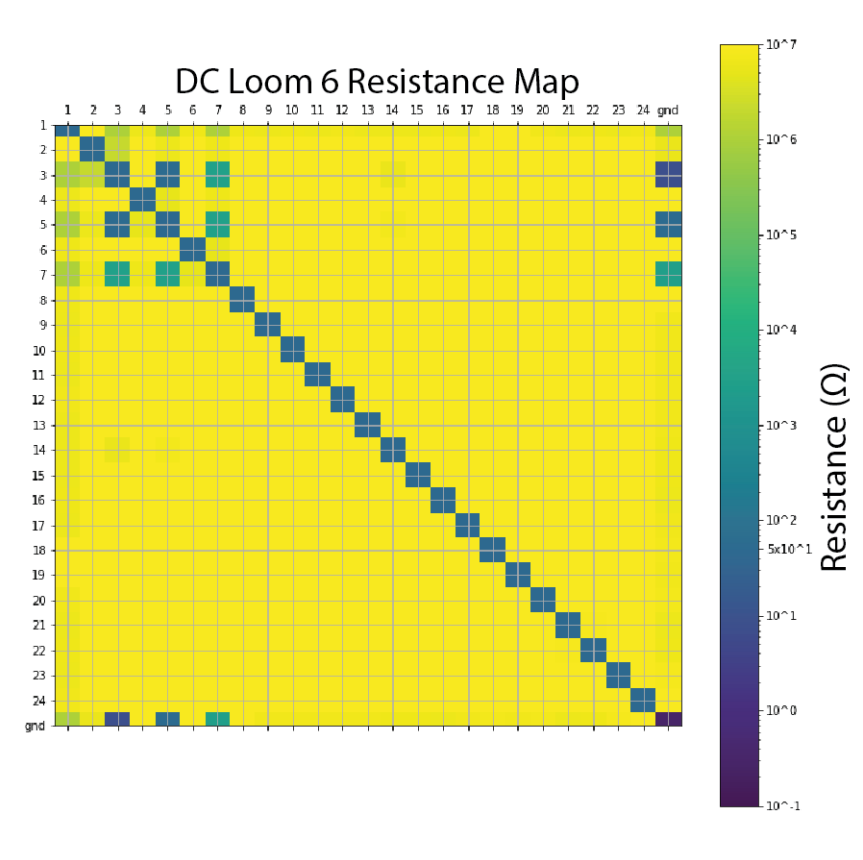


FIGURE 4.11: An example resistance map of a DC loom that reveals shorts between line #1, #3, #5, #7, and ground. The end-to-end resistance of a DC line is reflected by the corresponding diagonal element, which should be $\approx 50\,\Omega$. An off-diagonal element represents the resistances between two DC lines or a DC line and ground, which should be above $10\,\mathrm{M}\Omega$ for well-isolated lines.

4.2.4 Room Temperature Electronic Setup

All the Josephson junction measurements performed in this project utilize a four-terminal $I - V$ measurement setup with current bias, as illustrated in Figure 4.12.

The switch matrix (Keithley 3706a) at the center of the diagram provides multiplex channels for connections between the room temperature electronic instruments on the left, and the DC loom from the DR on the right. Up to 6 electrical connections can be made from the electronics to the switch matrix via BNC cables, and one DC loom can be connected to the switch matrix via a 24-pin Fischer cable at a time. So we measure one chip (connected by one DC loom) at a time, and keep the others grounded.

The reason for using a current biasing setup is that the Josephson tunneling happens in a regime of zero-voltage. A DC signal, provided by a Yokogawa 7661 DC source, and an AC signal, provided by an SRS 860 lock-in amplifier, are combined and sourced to the device through BNC cable 3, labeled as I+ in the diagram. The critical current for the vdW junctions we fabricate is in the range of 10 nA-10 µA. We choose $R_{bias}^{DC} = 1\,\mathrm{M\Omega}$ so that the DC source can work with appropriate voltage range settings of the instrument, 10 mV-30 V. The AC signal provided by the lock-in amplifier is used to directly measure the differential conductance of the junction device. In order not to significant broaden the conductance spectrum, we should keep the AC current around 1/10 of the critical current. However, the trade-off for having a small lock-in output signal is a low signal-to-noise ratio. We circumvent this problem by providing a large bias resistor $R_{bias}^{AC} = 2\,\mathrm{M\Omega}$. Now $I_{AC} = 5\,\mathrm{nA}$ corresponds to an output $V_{AC} = 10\,\mathrm{mV}$, at which the lock-in amplifier is comfortable operating. The frequency of the AC current is set to be 17 Hz, known to be a frequency sweet spot that avoids interference from power line harmonics (60 Hz in US), allows the signal to travel through the low-pass filters with little attenuation, and is still high enough for proper lock-in signal demodulation. As for the current drain (BNC 4, labeled as I- in the diagram) is set to ground in order to minimize noise.

To measure the DC voltage across the tunnel junction, the voltage signal is first amplified x10 with an SRS 560 low-noise voltage amplifier, which uses DC-coupling to filter out any AC components in the signal. Then an HP 34401A digital multimeter (DMM) is used to read the DC voltage. The AC voltage can be directly demodulated and amplified by the lock-in amplifier.

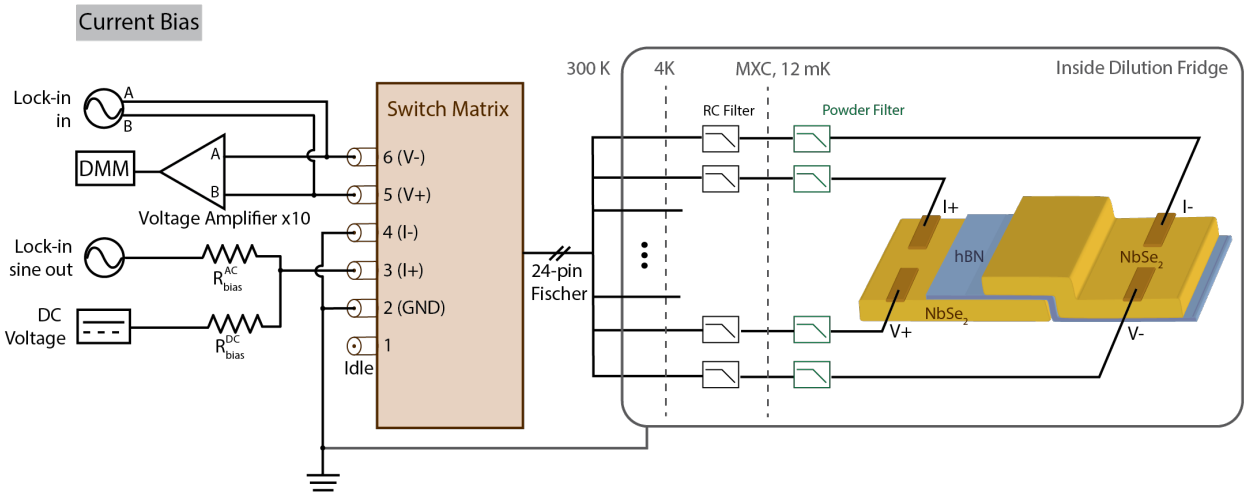


FIGURE 4.12: Diagram of the four-terminal $I - V$ measurement setup with current bias. The low-pass filtering on the DC lines inside the DR is described in section 4.2.3, and the room temperature electronic setup is detailed in section 4.2.4. All the instruments shown in the diagram share one common ground with the fridge. BNC 2 provides an access to ground for the DC loom when its not used in measurement. The current drain, BNC 4, is also connected to ground in order to minimize noise.

4.2.5 Grounding

Having a proper grounding is of great importance in our experiments for two major reasons. First, the vdW Josephson junction devices are sensitive to electrostatic discharges (ESD). Besides using ESD safe containers during transportation and keeping ourselves grounded whenever handling the devices, it is also crucial that the devices are properly grounded when they are not actively being measured but electrically connected to the environment. Second, without proper grounding the presence of ground loops allows electrical and magnetic interference to create voltage noise sources, hence contributes to the broadening of the measurement signals.

The first step towards a good grounding configuration is to ensure that the fridge shares one common ground with all of the measurement electronics. To begin with, we disconnect all electronics from the fridge and make sure the fridge is isolated ($> 10\text{M}\Omega$) from all electrical reservoirs, such as the power-line ground, instrument chassis, and the metal frames of the instrument rack. Then we make sure that all

electronic instruments that will be connected to the fridge are plugged into a single power source with a clean ground. The clean ground here refers to a separate ground reference that is isolated from the building ground, which is prone to ground noise. We also use a optical GPIB isolator to protect the instruments from the dirty ground that their control computer is connected to. Finally, we make the electric connections between the instruments and the fridge one by one, and checking that they still share the same ground.

Once a single ground reference is defined in the measurement setup, we take two additional steps to ensure the vdW junction devices are protected from ESD in the environment. First, the DC looms must be grounded before the the DIMM board with vdW devices are mounted, and they should remain grounded when the devices connected to the looms are not actively being measured. Second, the device that is being measured should also be grounded whenever a measurement is complete. BNC 2 on the switch matrix provides a connection to ground, so during the idle period all 24 lines in the DC loom should connect to BNC 2 and nothing else.

Chapter 5

Measurements & Results

5.1 Preliminary Measurements

Before committing to making Josephson junctions with $NbSe_2$ and hBN, we performed a few preliminary measurements to better understand their superconducting and dielectric properties.

5.1.1 $NbSe_2$ Superconductivity

As mentioned in section 3.2, $NbSe_2$ oxidizes easily once it is exposed to the atmosphere. Therefore we measured the temperature dependence of the flakes' resistance in two configurations: (1) unprotected $NbSe_2$ flake (2) $NbSe_2$ flake that is fully encapsulated by a top and a bottom hBN flakes. We expect the encapsulated $NbSe_2$ to be free of oxides and exhibit the material's intrinsic superconducting behaviors, while the exposed $NbSe_2$ flakes should show increased resistance or perhaps even loss of superconductivity.

$NbSe_2$ without encapsulation

First we patterned PdAu electrodes on a silicon chip with 285 nm of insulating SiO_2. Then the candidate $NbSe_2$ flakes were transferred on top of the electrodes. Finally, we cooled the devices down in a cryogenic refrigerator and measured the temperature dependence of its 4-point resistance (excluding contact resistance). With an atomic force microscope (AFM), device A shown in Figure 5.1 (a) was measured to be 25-36 ($\pm$2) nm thick (the flake has inhomogeneous thickness as can be seen in the flake color) and device B in Figure 5.1 (b) was 74 ($\pm$2) nm thick.

From the temperature-dependent resistance measurement in Figure 5.1 (d), we see that the resistance of both devices drops sharply around $T_c = 7K$, confirming that even with oxidation the flakes are still superconducting. To compare their resistivity, we make use of the sheet resistance, defined as $R_{sq} = R\frac{W}{L}$. Here W is the width of the flake, and L the length between measurement points. Device A, with the thinner flake, is estimated to have $R_{sq,A} \approx 3.5\Omega$, while for device B $R_{sq,B} \approx 14k\Omega$. These results agree with our expectation that thinner flakes are more resistive.

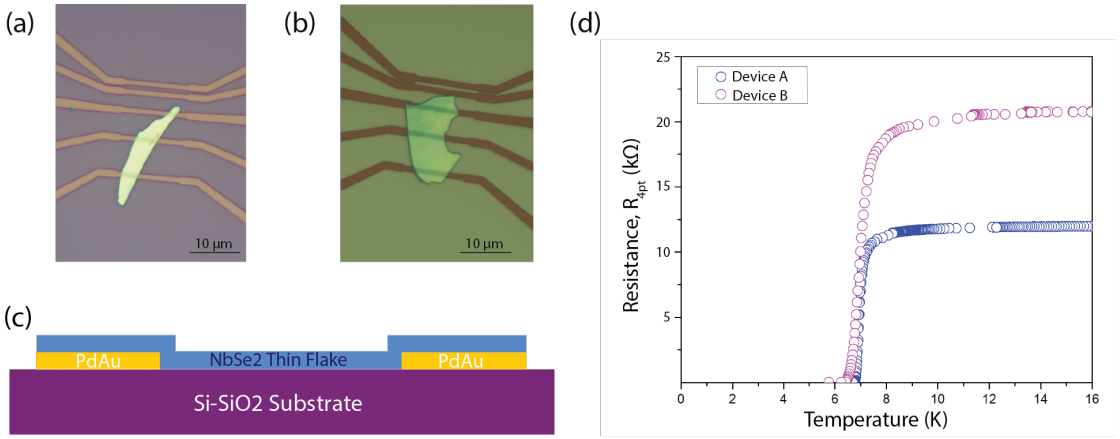


FIGURE 5.1: Unprotected $NbSe_2$ devices and resistance measurement. **(a) and (b)** Optical microscope images of device A and B, respectively, with PdAu electrodes underneath. **(c)** Cross-section diagram of unprotected $NbSe_2$ devices. **(d)** Temperature dependent measurement of device 4-pt resistance (excluding contact resistance). Resistance for both devices fall sharply around $T_c = 7K$.

Encapsulated $NbSe_2$

In order to better understand the electrical properties of $NbSe_2$ without the influence of oxidation, we encapsulated the $NbSe_2$ flake and the PdAu electrodes with a top and bottom hBN flakes, as the cross-section diagram depicts in Figure 5.2 (b). Since the encapsulation process was performed inside an argon-filled glovebox, we consider oxidation between the electrodes and the $NbSe_2$ flake to be minimal.

The encapsulated $NbSe_2$ flake shows a transition temperature around $T_c = 6.5(\pm 0.5)K$, similar to that of the un-encapsulated devices. However, its 4-pt sheet resistance

$R_{sq} \approx 25\Omega$ is two orders of magnitude lower than the unprotected $NbSe_2$ flakes. We see that although the oxidation of $NbSe_2$ does not destroy its superconductivity, it does significantly increase the flake resistance compared to the protected ones.

The nonlinear temperature dependence of the flake resistance observed in Figure 5.2 (d) is likely due to the temperature instability in the measurement process. This device was measured as the fridge warmed up rapidly, so the recorded temperature might not accurately reflect the local temperature of the device as heat needs time to equalize.

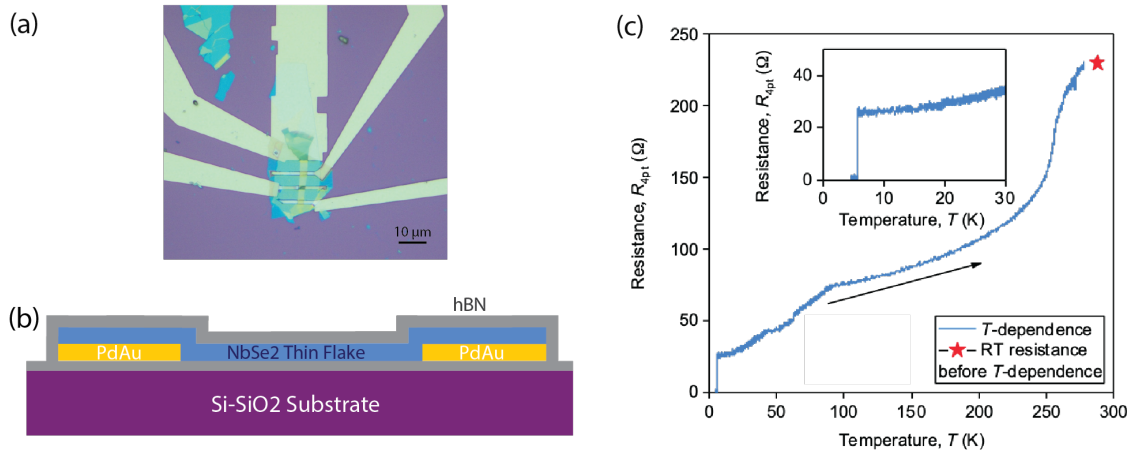


FIGURE 5.2: Encapsulated $NbSe_2$ device and resistance measurement. **(a)** Optical microscope image of the encapsulated $NbSe_2$ device. **(b)** Cross-section diagram of . **(c)** Temperature dependent measurement of device 4-pt resistance (excluding contact resistance). The star represents the 4-pt resistance measured at room temperature. The nonlinearity of temperature is likely due to temperature instability as the fridge warmed up quickly. Inset shows device resistance fall sharply around $T_c = 6.5(\pm 0.5)K$.

5.1.2 Characterizing hBN Microwave Properties

As discussed in section 2.5, the potential reduction of TLSs in high quality dielectrics is one of the major motivations that drive us to explore Van der Waals materials for fabricating superconducting quantum circuits. Megan Yamoah and Joel I. Wang et al. [54] led the work to characterize the microwave properties of

hBN using superconducting resonators.

The total measured resonator quality factor Q can be decomposed to the coupling quality factor Q_c and the internal quality factor Q_i,

$$\frac{1}{Q} = \frac{1}{Q_c} + \frac{1}{Q_i} \tag{5.1}$$

Here we are interested in Q_i because it quantifies the internal loss, and by incorporating hBN into the resonator we expect to observe a modified Q_i. The internal quality factor is also inversely proportional to the dielectric loss tangent,

$$Q_i = \frac{1}{\tan\delta} \tag{5.2}$$

The total loss tangent is a linear combination of all the contributing components' loss tangent multiplied by their corresponding participation ratio,

$$\frac{1}{Q_i} = \sum_n p_n \tan\delta_n \tag{5.3}$$

Here we incorporate hBN flakes into lumped-element resonators with two different methods as shown in 5.3: (1) by placing a thick (> 300 nm) hBN flake on top of a inter-digitated capacitor (IDC) and (2) by inserting a moderately thick (10-30 nm) hBN flake in a parallel-plate capacitor (PPC) made with a $NbSe_2$-hBN-$NbSe_2$ sandwich structure. The hBN participation ratio can be determined by electrostatic simulation using COMSOL. The hBN-on-IDC configuration leads to a smaller participation ratio $\sim$ 14%, compared with $\sim$ 66% for the PPC configuration. In order to compensate for the low participation ratio in the hBN-on-IDC configuration, an additional control resonator (labeled as "hBN Ctrl" in Figure 5.3 and 5.4) is added as a reference point to more accurately extract hBN material quality factor. This control resonator is designed with the same nominal L and C values as the resonator used to host the hBN flake.

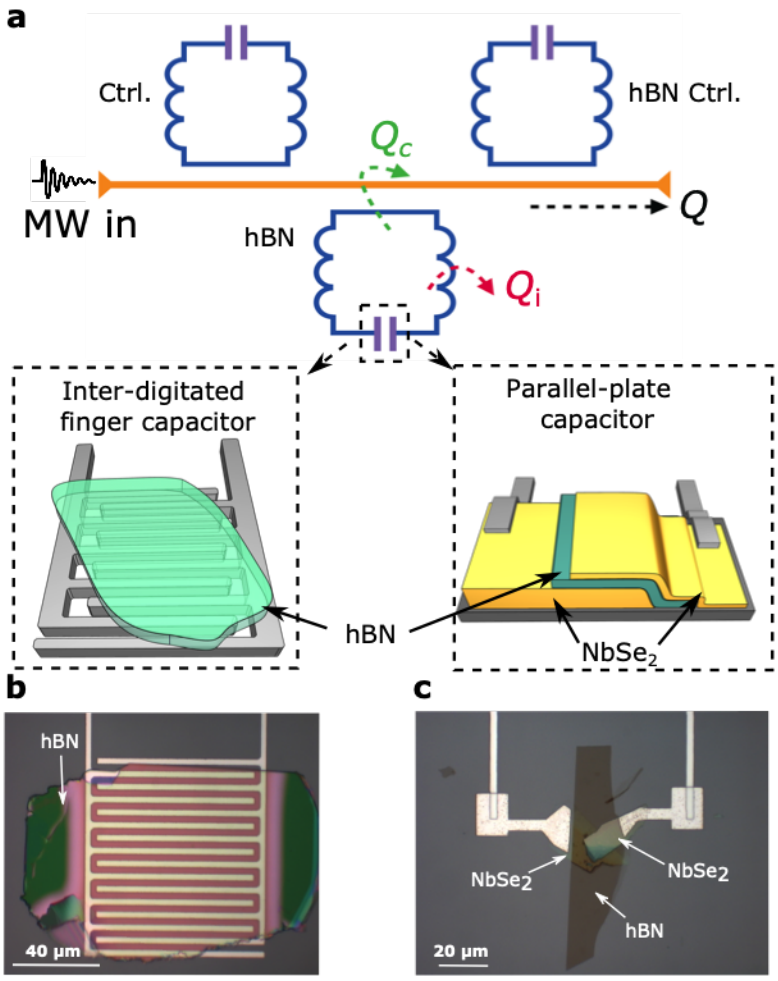


FIGURE 5.3: **(a)** Illustration of a hBN-integrated superconducting resonator (bottom one), along with two control resonators, coupled to the microwave read-out line. There are two different ways hBN flakes are incorporated into the capacitor: **(b)** on top of an inter-digitated capacitor **(c)** as the dielectric inside a $NbSe_2$-hBN-$NbSe_2$ parallel-plate capacitor.

By fitting the microwave reflection spectrum $S21$, we can extract the internal quality factor of the resonators and hence derive the hBN material quality factor using its participation ratio, which is further confirmed by the shift of resonance frequency from the control resonators. An example resonance shift of the resonator with hBN is shown in Figure 5.4.

The internal quality factor is extracted at different microwave drive power. The increase of quality factor with an increasing microwave power shown in Figure

5.4 (b) is a signature of TLSs induced loss, because TLSs predominantly interact with the resonator by absorbing and emitting energy but become saturated with increasing power. At the single photon level where we typically operate our quantum circuits, hBN material quality is determined to be $Q_{\mathrm{hBN}} > 5 \times 10^4$. Note this value is two orders of magnitude higher than the the amorphous AlO_x quality factor $\sim$ 500 reported by O'Connell et al. [55], which confirms our expectation and further motivates us to build superconducting circuit components with this material.

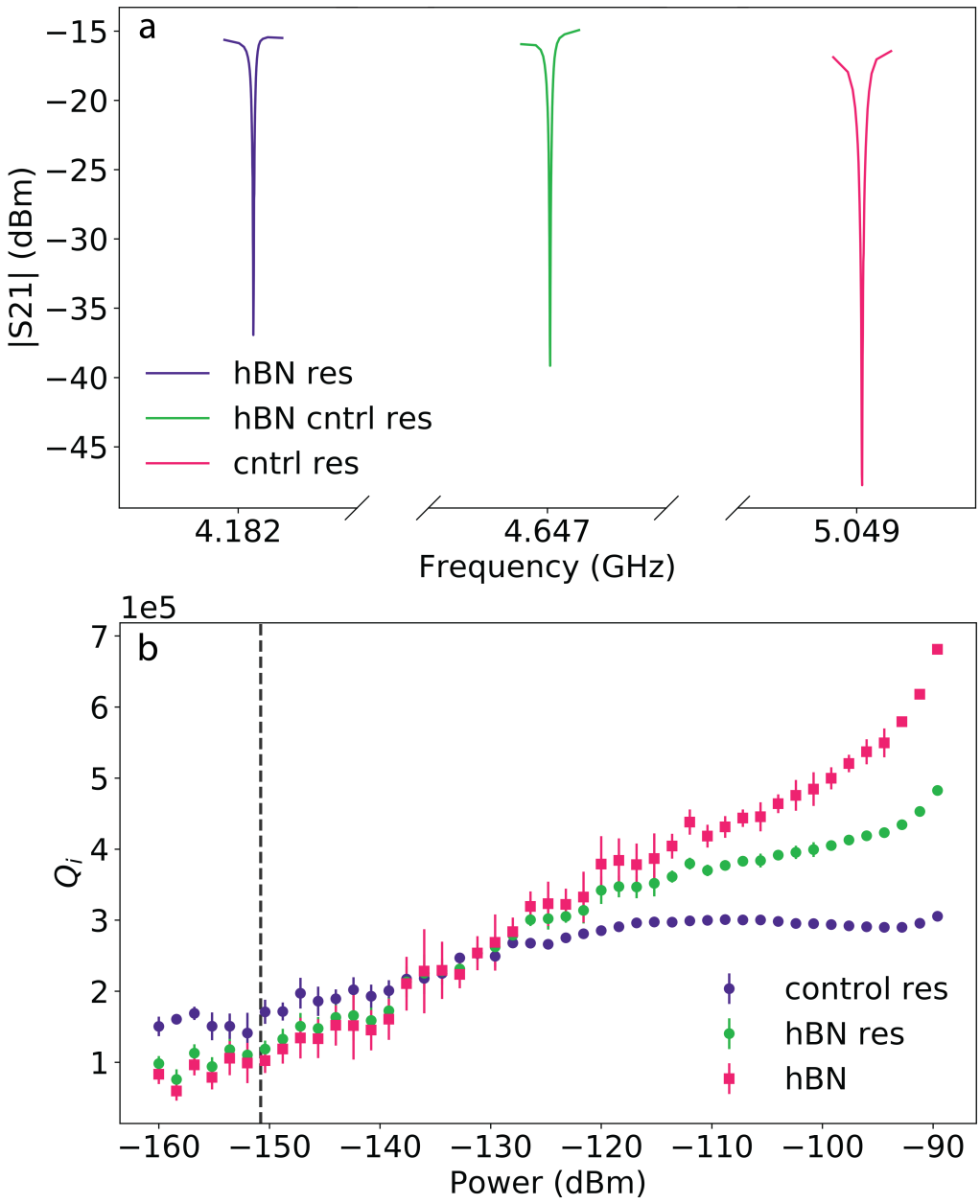


FIGURE 5.4: Microwave measurement results of an example hBN-incorporated resonator device. **(a)** Microwave reflection spectrum of the hBN resonator, hBN control resonator, and the control resonator. **(b)** The internal quality factor Q_i is extracted by fitting the reflection spectrum shown in (a), and shows expected power dependence for TLSs-induced loss.

5.2 All-vdW Josephson Junction Measurements

All-vdW Josephson junction fabrication requires manual stacking of vdW flakes which involve a myriad of uncertainties as mentioned in section 4.1.3. Out of the 14 complete stacks we fabricated, 3 of them successfully survived all the fabrication processes and demonstrated Josephson behaviors. Table 5.1 summarizes the important geometric parameters of these devices. Here the hBN layer number is determined by method of optical contrast described in section 4.1.2, and later confirmed with tunneling resistance measurement results. Figure 5.5 shows the microscope images of the three Josephson junctions with patterned electrical contacts.

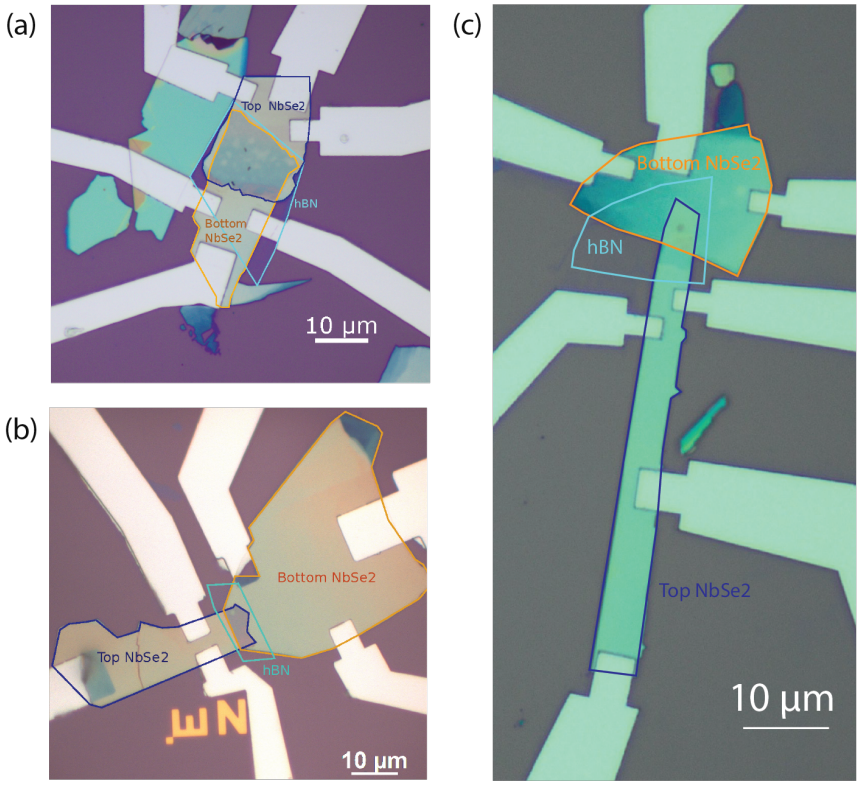


FIGURE 5.5: Microscope images for Josephson junction devices **(a)** Device 8 **(b)** Device 9 **(c)** Device 10. The outlines trace the $NbSe_2$-hBN-$NbSe_2$ flakes for better visibility.

Device Label	hBN Layer #	Junction Area (μm^2)
8	4	108 ($\pm$2)
9	2	34 ($\pm$1)
10	2	17.5 ($\pm$0.5)

TABLE 5.1: Summary of successful all-vdW Josephson junction devices.

5.2.1 $I - V$ Characteristics

Figures 5.6-5.8 present the current biased 4-point DC measurements of the all-vdW Josephson junction devices at temperature around 10 mK. From the hysteresis of the $I - V$ curves, we call tell that devices 8 and 9 exhibit behavior that is typical of underdamped junctions, while device 10 shows characteristics of an overdamped junction.

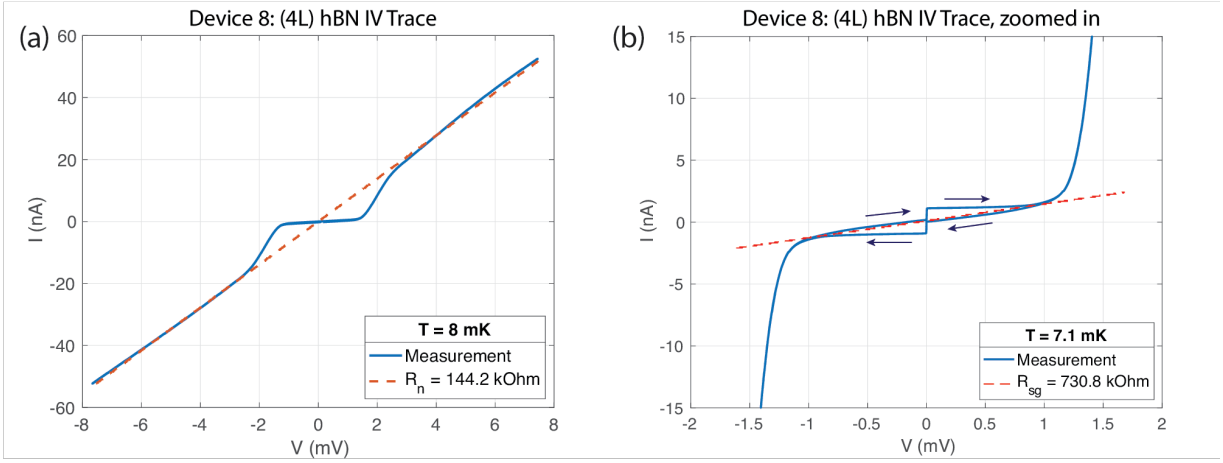


FIGURE 5.6: $I - V$ curves for the 4L-hBN device 8 from current biased 4-point DC measurement. **(a)** Overall $I - V$ **(b)** Zoomed into the current switching region.

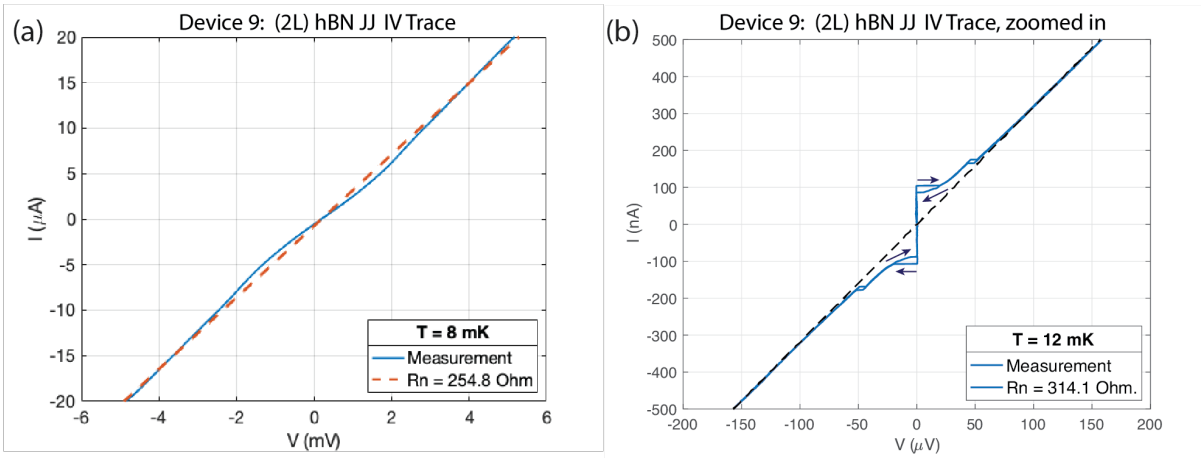


FIGURE 5.7: $I - V$ curves for the 2L-hBN device 9 from current biased 4-point DC measurement. **(a)** Overall $I - V$ curve. **(b)** Focused scan in the current switching region.

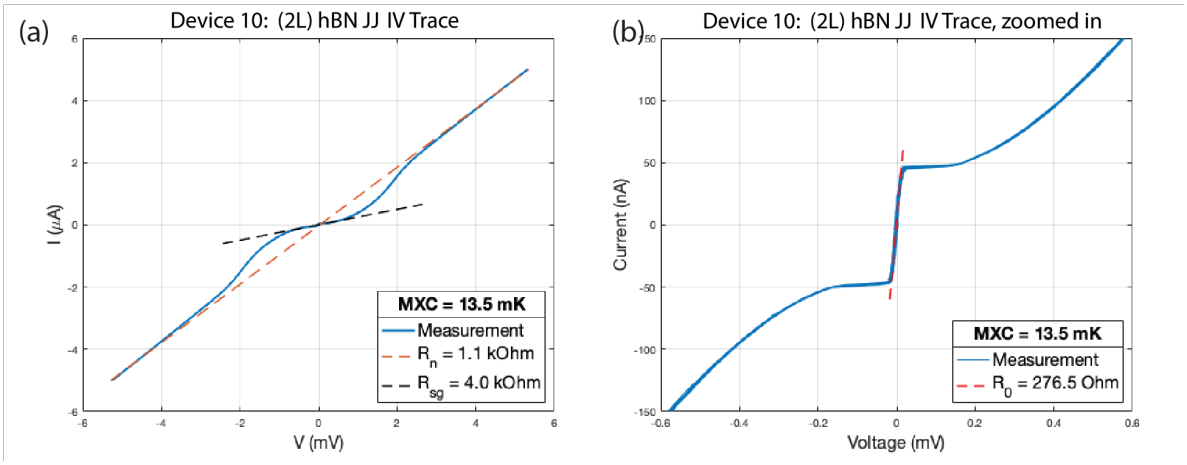


FIGURE 5.8: $I - V$ curves for the 2L-hBN device 10 from current biased 4-point DC measurement. **(a)** Overall $I - V$ curve. **(b)** Focused scan in the current switching region. Non-zero resistance is observed in the region before switching current, indicating that thermal noise is present.

Normal-state Resistance & Critical Current Density

The normal-state resistance of each junction can be extracted from fitting the linear region of the $I - V$ curves. After normalizing to the junction area, we plot the resistance as a function of hBN layer number and compare them to the reported

values of hBN tunnel resistance by Britnell et al. [56] Our results are in good agreement, even though Britnell and colleagues performed the electric tunneling measurements with a conductive atomic force microscopy at room temperature. From both of these measurements, we can see hBN tunnel resistance scales exponentially with increasing hBN layer number.

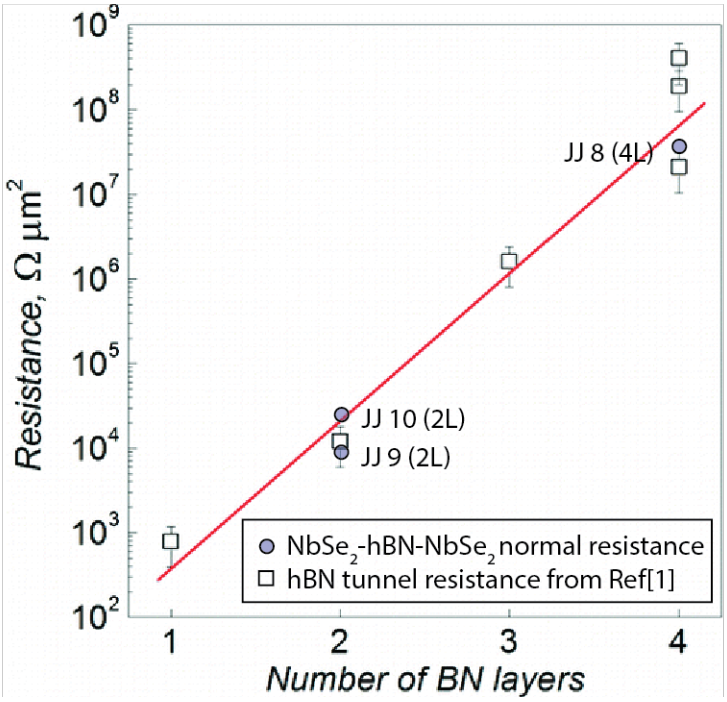


FIGURE 5.9: Normalized hBN tunnel resistance. Blue circles denote the normal state resistance extracted from the Josephson junction $I-V$ curves in this measurement. White squares represent data measured with conductive atomic force microscopy. Reprint with permission from Ref [56]. Copyright (2012) American Chemical Society.

Recall the Ambegaokar-Baratoff formula in 2.28 for $T \ll T_c$,

$$I_c R_n = \pi\Delta(0)/2e$$

We can then determine the critical current density for 2L hBN junctions is $\sim 100nA/\mu m^2$, and for the 4L hBN junction $\sim 10pA/\mu m^2$.

Subgap Resistance

Another parameter we are interested in is the ratio between sub-gap resistance and normal resistance, R_{sg}/R_n. Typically, we expect $R_{sg}/R_n > 10$ for high quality Josephson junctions, but for all the vdW junctions we measured, $R_{sg}/R_n < 5$. This relatively small sub-gap resistance indicates presence of leakage current that is normally associated with quasiparticle population and conductive defectives in the junction barrier. One potential source of conductive channels are fabrication imperfection of the vdW junction stacks. Figure 5.10 shows an example of junction area AFM image, where we can see bubbles trapped at the junction interface and surface unevenness.

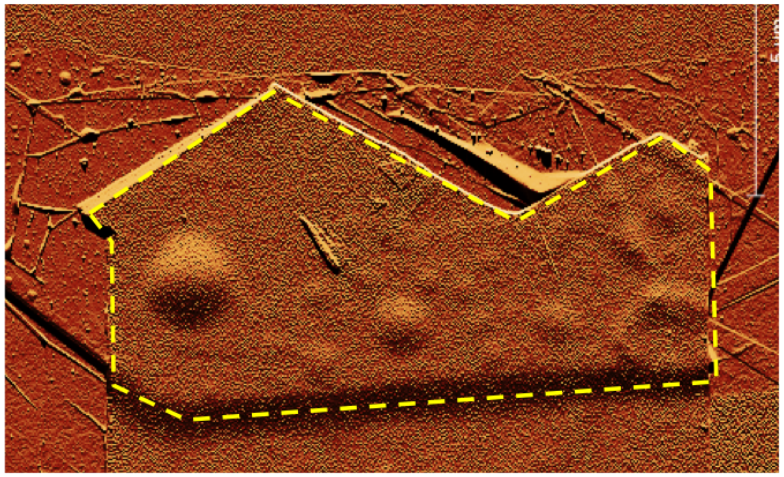


FIGURE 5.10: An example of $NbSe_2$-hBN-$NbSe_2$ junction AFM image. The dashed line outlines the junction area, where bubbles and surface unevenness can be seen.

Additionally, for the overdamped junction device 10, we observed non-zero resistance before the switching current is reached, as shown in Figure 5.8 (b). In section 2.3.3, we discussed how thermal activation gives rise to phase diffusion in a overdamped junction, leading to a finite resistance below the switching current. Therefore this observed resistance indicates presence of thermal noise during the junction measurement.

Junction Aging

It should be noted that $I-V$ curves in Figure 5.7 for device 9 showed abnormal behaviors. More specifically, the transition at the gap voltage is smeared out into an almost-linear curve, and the $R_{sg}/R_n = 1.2$ is also lower than the other two devices (5 for device 8, and 3.6 for device 10). In this section, we will discuss how these behaviors changed over time.

We had the opportunity to remeasure this device 63 days after the first measurement. The device was stored in a nitrogen-filled dry box during most of this period, and taken out in the atmosphere for 7 days in order for it to be re-packaged for the second round of cool-down. We noticed significant changes in its $I-V$ curve characteristics:

1. normal-state resistance increased ~10 times
2. conductance is more non-linear around the gap voltage
3. R_{sg}/R_n increased to 3.8, much closer to the value 3.6 for the other 2L-hBN device 10.

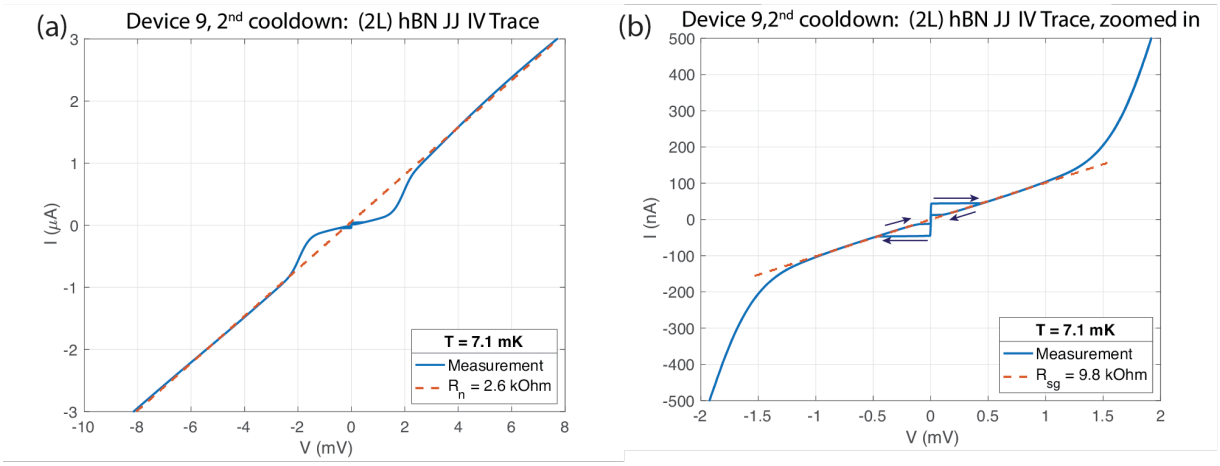


FIGURE 5.11: $I-V$ curves for the 2L-hBN device 9 from current biased 4-point DC measurement, 63 days after the first measurement shown in Figure 5.7. **(a)** Overall $I-V$ curve. **(b)** Focused scan in the current switching region.

A likely scenario that explains these changes is that over this time period, oxidation crept into the junction interface and increased the thickness of the insulating barrier, making the junction more resistive and the tunneling barrier strength higher.

5.2.2 Differential Conductance Measurements

We then measured the differential conductance of the vdW junctions using a lock-in amplifier. As discussed in section 2.2.1, differential conductance measures the superconducting density of states and is broadened by the thermal energy through the Fermi-Dirac distribution. However, the Fermi-Dirac distribution itself, especially when operated at low temperature ($\sim 10mK$ in our case), is not enough to account for all the broadening observed. Dynes [57] proposed a modified superconducting density of states equation from (2.18) to include the effect of quasiparticle recombination process,

$$\rho_s(E, T, \Gamma) = \mathrm{Re}\left\{ \frac{|E| - i\Gamma}{\sqrt{(E - i\Gamma)^2 - |\Delta(T)|^2}} \right\} \tag{5.4}$$

where Γ is the inverse of quasiparticle life-time, and gives rise to the smearing of the density of states around the superconducting gap. Note the quasiparticle recombination process also has a strong temperature dependence, even though not explicitly expressed here.

We numerically integrate equation (2.23) and take its derivative to find the theoretical solution for the differential conductance as a function of bias voltage. The temperature dependent superconducting gap can be approximated as

$$\Delta(T) \approx \Delta_0 \tanh\left(1.74\sqrt{T_c/T - 1}\right) \tag{5.5}$$

At the measurement temperature $\sim 10mK$, broadening due to quasiparticle life-time is the dominant effect and temperature only minimally modifies the fit results. Therefore we fix temperature at $10mK$, and use Δ_0 and Γ as the fit parameters. Figure 5.12 demonstrates an example of the differential conductance measurement and fit for junction device 9 (2^{nd} cooldown). The best fit for the superconducting gap is $\Delta_0 = 0.92(\pm 0.005)meV$, which is in reasonable agreement with the superconducting gap for bulk $NbSe_2$, $\Delta_{0,bulk} = 1.1meV$.

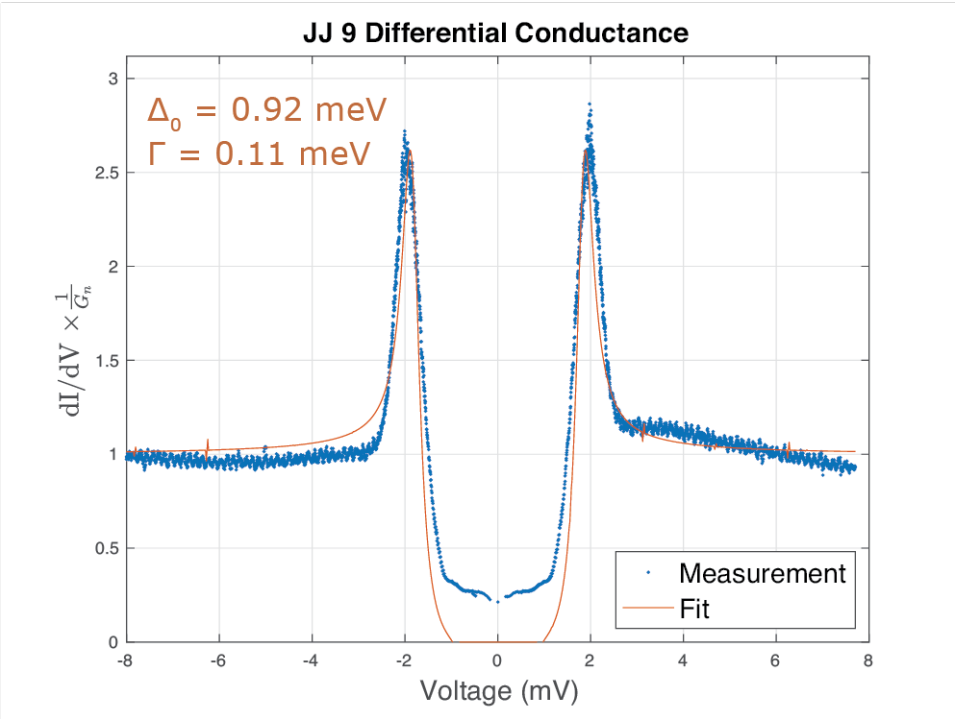


FIGURE 5.12: Normalized differential conductance of vdW Josephson junction device 9. The best fitting parameters found are $\Delta_0 = 0.92meV$ and $\Gamma = 0.11meV$.

Note even though the fit matches the data relatively well around the peaks, it does not account for the notable non-zero conductance in the subgap region. A more comprehensive model needs to be considered in order to capture all the details in the differential conductance measurement.

Chapter 6

Conclusion & Future Work

6.1 Conclusion

This research thesis demonstrated a new platform of van der Waals materials that could be used to build superconducting quantum circuits. We have successfully fabricated and characterized Josephson junctions made with vdW superconductor $NbSe_2$, and vdW dielectric hBN. Combined with the all-vdW parallel-plate capacitors characterized in the work led by Wang and Yamoah, et al., we now have access to the two building blocks for superconducting qubits. This work will hopefully enable all-vdW quantum devices in the near future.

The summary of parameters extracted from the $I - V$ characteristics and differential conductance measurements of the vdW Josephson junction devices is listed in Table 6.1. We confirmed that the normal-state tunneling resistance of hBN scales exponentially with the hBN layer number. Therefore the Josephson critical current density decreases exponentially with increasing hBN thickness. Junctions with 2L-hBN demonstrated $J_c \sim 100\,\mathrm{nA}\,\mu\mathrm{m}^{-2}$, which is comparable to the critical current density of modern Al-AlO_x-Al junctions. All devices showed a superconducting gap close to the bulk $NbSe_2$ gap, $\Delta = 1.1meV$, indicating there is little degradation of superconductivity in the vdW junctions.

However, both the R_{sg}/R_n ratio and quasiparticle lifetime parameter Γ indicate excess quasiparticle population, and potential conductive channels in the tunneling barriers. Further investigation of these junction properties requires temperature-dependent measurements. We should also consider improving fabrication techniques in order to reduce structural defects at the junction interfaces.

Device Label	hBN Layer #	R_n ($\Omega\mu m^2$)	J_c ($nA/\mu m^2$)	Δ_0 (meV)	Γ (meV)	R_{sg}/R_n
8	4	2.6×10^7	0.06 ($\pm$0.002)	0.93 ($\pm$ 0.005)	0.1	5.0
9	2	8.6×10^3	90 ($\pm$3.2)	0.92 ($\pm$ 0.002)	0.11	3.8
10	2	1.8×10^4	193 ($\pm$7.1)	0.95 ($\pm$0.006)	0.16	3.6

TABLE 6.1: Summary of all-vdW Josephson junction measurement results.

6.2 Future Work

6.2.1 Additional vdW Josephson Junction Measurements

To provide a complete characterization of Josephson junctions made with the $NbSe_2$-hBN-$NbSe_2$ structure, we need to fabricate and measure additional devices to obtain more data, especially for devices with 3L hBN. Additionally, we should perform temperature dependent measurements to quantify the impact of thermal activation and distinguish it from other potential defects that lead to the high sub-gap conductance we observed. Lastly, a systematic study could be performed to better understand the device aging rate and how it affects the junction properties. This would shed light on the long-term scalability of superconducting devices made with $NbSe_2$.

6.2.2 Fabrication Improvements

In section 5.2.1, we showed some examples of structural imperfections in the devices, such as bubbles trapped at the junction interface and ripples of the thin tunneling hBN flakes. These defects introduce local strain and disorder to the vdW junction devices which inhibit the advantage of vdW materials' low intrinsic disorder. A few recent studies proposed methods that could potentially help reduce these defects during the fabrication process. For example, Purdie et al. [58] reported less bubbles at the vdW interfaces with the "hot pick-up" techniques that utilize a higher temperature (>120°C) when picking up the vdW flakes. This method works

because the bubbles' mobility increases with temperature. Based on the same principle, they suggested another procedure to push out bubbles: laminating the vdW stacks onto a substrate at 180°C, with an ironing motion controlled by the microactuators. Without the use of extra heat, Kim et al. [59] proposed a AFM contact mode treatment to help remove bubbles with mechnaical force after the vdW heterostructure is completed. Since all of these methods were demonstrated with graphene-based heterostructures, some tweaking is required before applying them to the different vdW materials used in our project. They do, however, provide some plausible directions for fabrication improvements.

6.2.3 Towards All-vdW Transmons

Besides satisfying our scientific curiosity, the primary motivation for building and characterizing all-vdW Josephson junctions is to prepare for an all-vdW transmon. Here we limit the discussion to transmon qubits because of their relative simplicity, mature architecture, and long coherence time, but these vdW junctions can certainly be incorporated into other superconducting qubit architectures.

Recall that the transmon qubit design requires at least $E_J/E_C \approx 30$, as discussed in section 2.4.2. Traditionally, the high E_J/E_C ratio is achieved by shunting the Josephson junction with a large coplanar capacitor in order to avoid the high TLSs concentration in amorphous dielectrics. This leaves an extremely large footprint that dominates the qubit size. In section 5.1.2, we showed that parallel-plate capacitors made with the same $NbSe_2$-hBN-$NbSe_2$ heterostructures exhibit supreme quality, and significantly smaller footprint compared to coplanar capacitors. Combined with the vdW Josephson junctions, we now have all the necessary building blocks for all-vdW transmon qubits. Since these two components are made with the same vdW heterostructures, they can be combined in the fabrication process with a few specific requirements for the hBN geometry.

To take the first step towards all-vdW transmon qubits, we now consider the possibility of a simplified all-in-one design as a proof of concept. If a large enough capacitance can be obtained just from the Josephson junction without an additional

shunt capacitor, then it will greatly reduce the fabrication complexity. We can estimate the junction capacitance using the formula for parallel-plate capacitor,

$$C = \frac{\epsilon_r \varepsilon_0 A}{d}$$

Here the dielectric constant ϵ_r for few-layer hBN is 2.9 [60]. The thickness of the dielectric is $d = L * d_0$ where $d_0 = 0.33\,\text{nm}$ for monolayer hBN and L is the hBN layer number. Combined with the J_c reported in section 5.2.1 for different tunneling hBN layer numbers, we can now plot the E_J/E_C ratio as a function of junction area. It is clear from Figure 6.1 that junctions with 3L hBN match our target regime the best, with a reasonable junction size around a few μm^2.

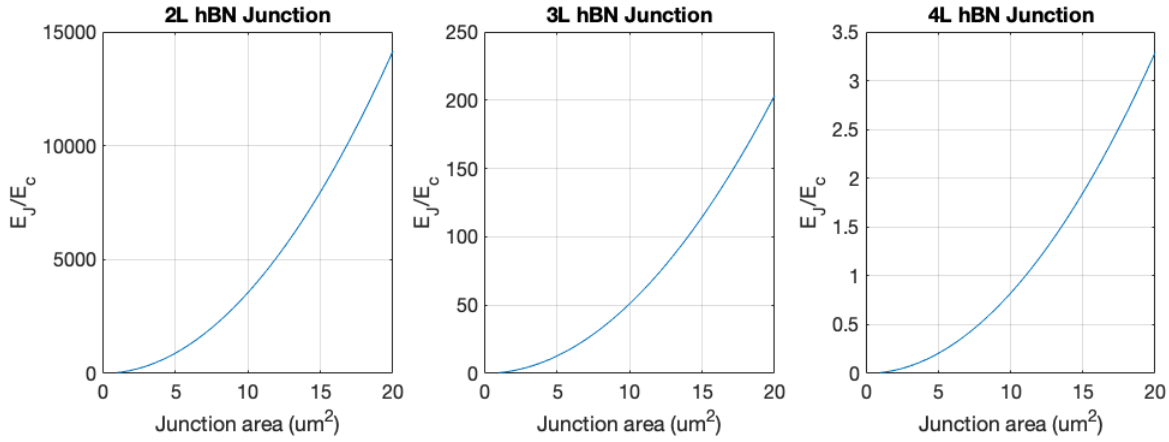


FIGURE 6.1: Simulated E_J/E_C ratio for vdW Josephson junction devices made with 2L, 3L, and 4L tunneling hBN, as a function of junction area size.

Next we plot the other two parameters that one cares about in a transmon qubit design: (1) the qubit frequency and (2) anharmonicty, as a function of the junction area. It can be seen from Figure 6.2 that with a junction area of 5-10 μm^2, we will be able to achieve a qubit frequency $f \sim 2.5\,\text{GHz}$ and qubit anharmonicty $\alpha = E_c \sim 200\,\text{MHz}$. Although the qubit frequency is on the lower side compared to standard transmon qubits we fabricate in the lab, it is still within the reasonable range of 2-10 GHz.

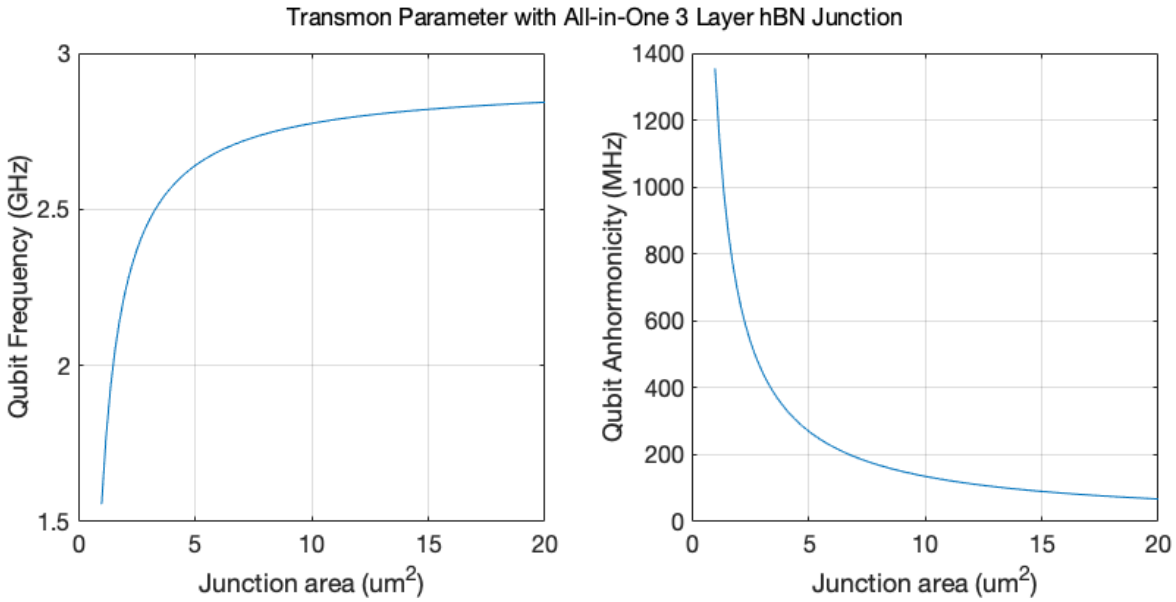


FIGURE 6.2: Simulated qubit frequency f, and qubit anharmonicity α as a function of junction area size, for vdW Josephson junction devices made with 3L tunneling hBN,

To make an all-in-one vdW transmon qubit, we first assemble a vdW Josephson junction stack with 3L hBN and an area size of 5-10 μm^2, following the same fabrication steps that are described in section 4.1. Then we simply transfer the whole stack to a pre-patterned chip that is designed with all standardized aluminum components. As shown in Figure 6.3 (a), a window area is cut out to host the vdW heterostructure. The superconducting quantum interference device (SQUID) loop is included to add flux tunability for the vdW transmon, and then the qubit is dispersively coupled to a meandering resonator for read-out. An additional step of ion-milling and aluminum evaporation will make Galvanic contacts between the vdW stack and the rest of the Al superconducting circuits. Figure 6.3 (b) shows the design of the entire qubit chip, which hosts two all-vdW tunable transmons and one Xmon[61] qubit as a control reference.

The spectroscopic and temporal measurements of this all-in-one vdW transmon qubit will provide the ultimate verification for our vision that was set at the start of the project: an all van der Waals transmon.

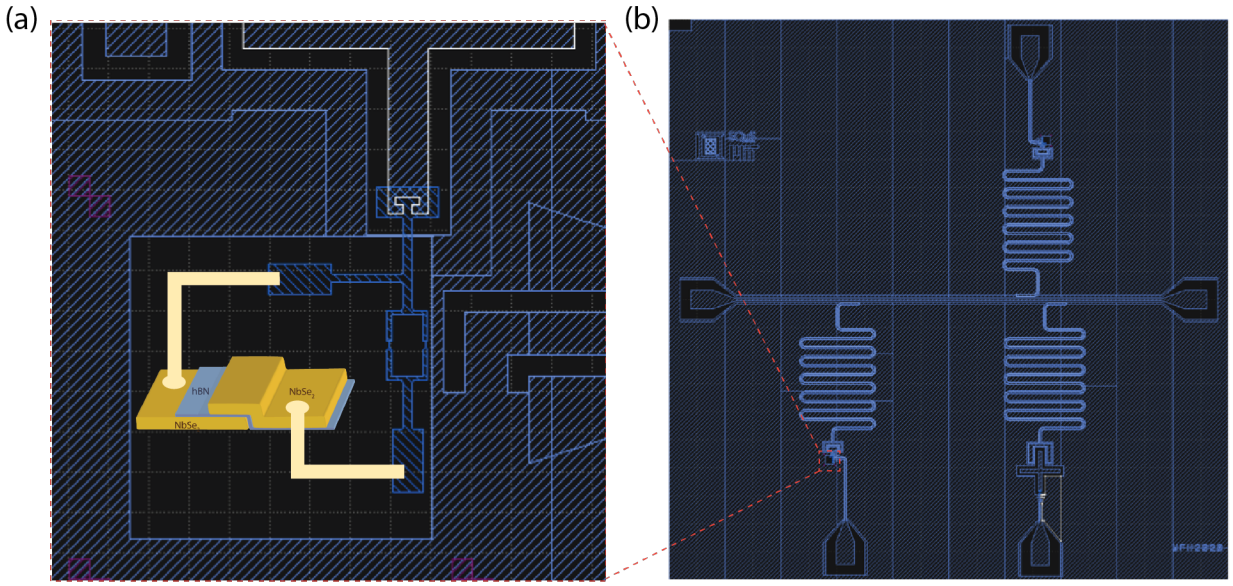


FIGURE 6.3: Design of the all-vdW transmon qubit chip. **(a)** A window area is cut out to host the vdW junction stack. The SQUID loop and flux line are included for qubit frequency tunability. After transferring the vdW stack onto the chip, Al contacts will be made to connect the stack to the result of the superconducting circuits. **(b)** A view of the whole chip design that has two all-vdW transmons and a standard X-mon qubit for reference. Each qubit is dispersively coupled to a resonator for read out.

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