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MAGNETIC TARGET LOCATOR (MATALOC)

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CONTENTS

ABSTRACT

[Confidential]

The proposed system is intended for installation in picket aircraft for automatically finding the center of a radar target, converting the center of target coordinates from polar to rectangular, providing temporary storage, and finally providing an output suitable for transmission over a narrow-bandwidth data link to a control ship. The design of the automatic detection and beam-splitting portion of the system is complete and described in detail. The system for conversion of coordinates is still under study; several methods are outlined and discussed.

PROBLEM STATUS

This is an interim report on one phase of a general study under a long term program.

AUTHORIZATION

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INTRODUCTION

The problem of handling large amounts of data rapidly has been the subject of many studies in recent years because of the increase in speed of aircraft and the advent of improved guided missiles. Many systems for data handling and presentation are now under construction or in proposal form. However, most of the effort has been directed toward large control centers on land or Combat Information Centers on board ship. Many of the proposed systems provide for a data relay between the main data handling facility and a remote search radar. It is of prime importance that the data link be of narrow bandwidth so as to reduce the burden on the already overloaded communication circuits. Consequently, a system is proposed to reduce raw radar data to a form suitable for transmission over a narrow-bandwidth data link and compatible with a central digital data handling system.

The proposed system is to be used to connect an airborne search radar to a shipboard control center. It is based on the premise that the control center will have computer facilities and excercise control of the complete tactical situation. This central authority will control intercepts, weapon assignments, threat evaluation, etc., and therefore, it is only necessary to provide an efficient and reliable system to send the early warning radar data to the control center.

The proposed Magnetic Target Locator, code named MATALOC, effectively reduces the raw radar information by automatically detecting the center of a target. The coordinates of the center of the target are then sent over the relay link. Prior to transmission, the target center coordinates are converted from polar to Cartesian and a temporary storage is provided as a buffer between the random rate of target acquisition and the even, slow rate of the information as relayed to the control center.

The proposed MATALOC system employs a digital video integration technique to enhance the signals in the presence of noise and to provide for automatic detection and beam splitting. Ferromagnetic techniques are exploited to obtain a cyclic magnetic core memory which will enhance the versatility and simplicity of the system. The system is intended to provide many of the facilities of the Lincoln Laboratory's Fine Grain Data System AN/FST-2 (Ref. 1) and, in addition, provide coordinate conversion as an aid for parallax correction. In general, the MATALOC system is less precise, and less complex than the AN/FST-2 and since the MATALOC proposal employs a magnetic core storage rather than a magnetic drum storage the MATALOC system may be synchronized to the radar rather than the converse as required by the AN/FST-2. The technique of beam splitting as employed in the MATALOC system offers an improvement in azimuth accuracy over the analog integration as used in the RAFAX system. This improvement in azimuth accuracy is of prime importance if the relayed data are to be used for computations of velocity and direction by the central computer. By using digital techniques throughout the detection logic, greater position accuracy may be expected than has been realized with analog systems such as the RAFAX (Ref. 2).

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THE DATA REDUCTION SYSTEM

The basic technique of the proposed system is to perform a digital video integration on a strobe-to-strobe basis using video quantized at range intervals of every half mile. The output from the integration is used to control counting circuits that function to determine the center of targets in units of one-half-mile range intervals and radar strobe intervals. These coordinates (polar in form) are then converted into the binary equivalent of Cartesian coordinates centered on the radar.

The heart of the data reduction system (Fig. 1) is a parallel magnetic-core memory describing 506 range intervals using 13 bits to store target information in each range interval. The 13-bit word is divided into three parts: four bits for strobe storage, two bits for target edge status, and seven bits for strobe counting in order to determine the center of the target.

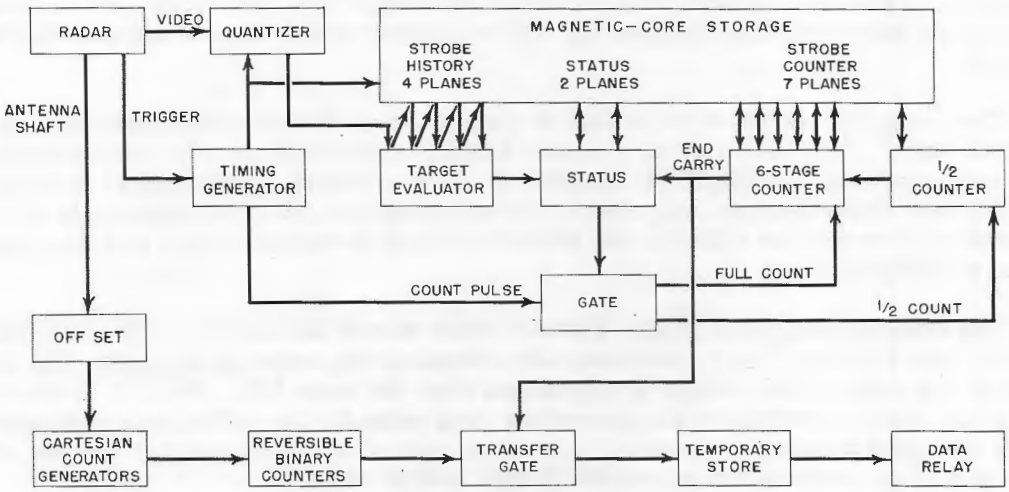

Fig. 1 - Block diagram of MATALOC

The memory is scanned with each radar strobe, and coincident with readout of the 13-bit word, the radar video is quantized for that particular range interval. Each word and the quantized video are read into a register, operated upon, and rewritten into the memory within every half-mile range interval. During the active portion of a radar strobe, the video output is quantized over every 6.1 μsec (1/2-mile radar range) and written into the strobe storage. The information stored is shifted during each radar strobe, resulting in the stored radar strobe shifting from the most recent bit to the next most recent bit, etc., until it is discarded after four strobes. The target evaluator is used to analyze the present quantized video and the quantized video from four previous strobes for leading and trailing edges of targets. After every half-mile range interval the target evaluator contains either a "one" in three or more of the five channels or a one in two or less of the channels. A leading-edge detected pulse is generated when ones are in three or more of the channels and a trailing-edge detected pulse is generated when two or less ones occur. Two bits are used to define the status of a target in each range interval. The first bit indicates a leading edge detected and the second bit a trailing edge detected.

Upon determination of a leading edge for a range interval, a leading-edge detected signal will set a status channel to "leading edge detected," and a count will be introduced in the "half count" digit of the strobe counter. For every additional radar strobe that three or more bits obtain, the strobe counter is changed by one-half count. When the trailing edge is determined, the main counter will contain a number of counts, equal to one-half the number of radar strobes subtending the target. A graph of the counting rate is shown in Fig. 2. It will be noted that if the target was present for X strobes, the count in the counting register will be X/2. That is to say, that two radar strobes are required for each count while the signal is present. When the trailing edge was detected, the center of the target had occurred X/2 strobes before. If it were not for the varying size of targets and the difficulty of providing for a variable offset, the position of the radar antenna minus the equivalent angle of X/2 strobes could be used to specify the azimuth of the center of a target. To circumvent this difficulty, the following artifice is used. Following receipt of a trailing-edge detection, the counter is changed to one count for every radar strobe regardless of target evaluator output until the full count S is obtained. At this time, the radar antenna will have scanned past the center of the target by an amount equal to

$$\left(\frac{X}{2}\right) + \left(S - \frac{X}{2}\right) = S \text{ strobes.}$$

However, S is equal to the total count of the register, which is a constant and hence the center of the target will always be displaced from the end-carry of the strobe counter by an angle equivalent to S radar strobes. Since this is a constant difference for all targets, a simple offset between the radar antenna shaft and the data pickup shaft may be used to synchronize the coordinate conversion unit to the antenna. The strobe counter end-carry is used to reset the status channels and to open a gate that will write the digit x and y coordinates of the center of the target into a temporary storage. An additional offset of two strobes is required since at least two and as many as four strobes may occur before a leading edge is detected. Likewise, the trailing-edge detection may be delayed from two to four strobes.

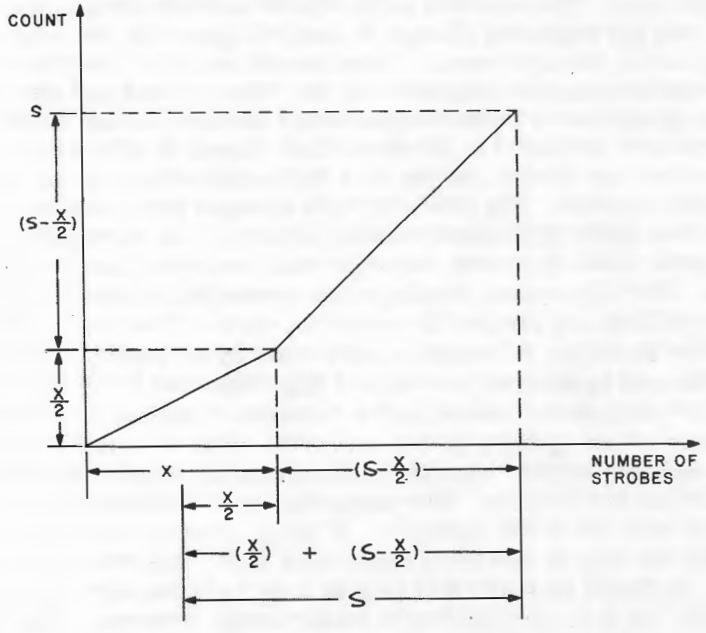

Fig. 2 - Counting rate vs radar strobes

CONVERSION OF COORDINATES

For ease of parallax corrections and subsequent compatibility with CIC data displays, the polar ρ and θ coordinates of the radar are transformed into rectangular x and y coordinates by coordinate conversion. The radar and the target center locator specify the polar coordinates of a target center. In place of range and angle counters, two reversible binary counters are used to accumulate count at rates proportional to cos θ and sin θ. The contents of these counters specify the instantaneous x and y coordinates of the radar strobe. The counters are reset during the radar dead time to either own radar location or to some off-centering for parallax correction. The pulses driving the x-range counter are derived from an x-count generator initiated by the radar trigger. These pulses occur at intervals of 6.1 cos θ μsec, corresponding to x-range intervals of one half-mile. The x-count generator is controlled by the radar data pickup shaft which has been offset by an angle required by the target center locator. Hence, when the center of a target has been determined, the end carry from the strobe counter will gate the x coordinate from the reversible binary counter into a temporary store. The temporary store serves as a buffer between the random rate of target acquisition and the uniform rate of target transmission over the data relay. In a similar manner the y coordinate is determined and transferred into storage.

MAGNETIC MEMORY

In Fig. 3 two magnetic shift registers are used to generate drive currents for biased magnetic switch cores which in turn generate drive currents for the storage cores. The X and Y shift registers each recirculate a single one and are shifted together every radar one-half-mile interval. Upon application of a shift pulse the ones are shifted to the next cores and the generated output pulses trigger blocking oscillators in each coordinate. The blocking oscillators generate enable pulses on the grids of driver tubes in each coordinate, and upon application of a read command pulse the driver tubes conduct heavily, generating currents in the switch core drive lines. The switch core at the intersection of the X and the the Y drive lines will be subjected to twice the current flowing through the windings of other cores on the drive lines. The selected core will be changed from negative to positive magnetic saturation, and the resulting change of flux will generate the read current pulse in the drive winding to the storage cores. When the drive to the switch core is terminated, the core is returned to negative saturation by the bias current and the resulting change in flux automatically generates a write current pulse for the storage cores. The 6578 magnetic storage cores are arranged in thirteen-digit planes of 506 cores each. In this system the storage cores are always driven by a full amplitude read current followed by a full amplitude write current. The drive is from a single turn winding that links one core in each plane. A four-turn digit-plane winding links all 506 cores of a plane and is used to sense the magnetic state of a core during a read cycle and may be used to inhibit during a write cycle. The digit-plane windings are connected to read amplifiers wherein the core output is amplified, and strobed to sense the state of the core. The one state of a core is indicated by an output pulse and a zero state by no output. The output from the read amplifiers is used to control the state of flip-flops that form the output register of the memory. After arithmetic operation the contents of the output register, in turn, controls inhibit drivers which operate during the write cycle to control whether a zero or one is written in the memory cores. The seven flip-flops associated with the strobe counter memory are also a binary counter. The sequence for this section is that during the read cycle the flip-flops are set by the momory. A count pulse is added either in the least significant digit or the next to the least significant digit, and then the new count is written into the storage. It should be noted that this is done very rapidly and the entire operation is completed within the 6.1-μsec half-mile radar-range interval. The flip-flops used in

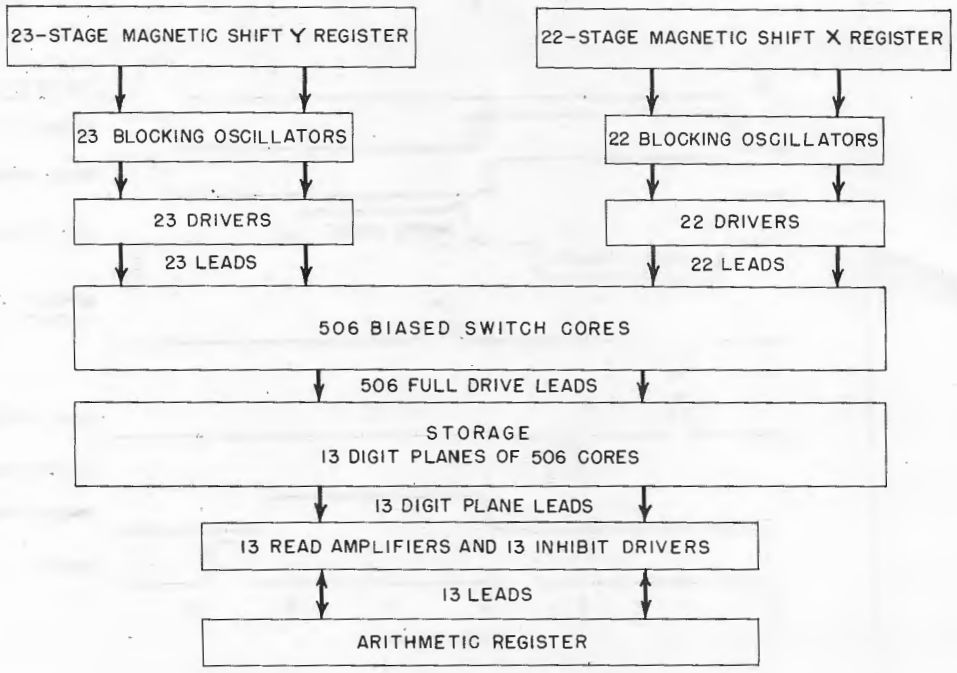

Fig. 3 - Block diagram of magnetic memory

the four strobe storage digit planes are connected such that the flip-flop connected to the quantized radar video will write in the first history digit plane; that of the first history plane will write in the second history plane, etc. In this section of the memory, data move from one plane to another with every radar strobe until after five strobes they are discarded. The status channel flip-flops operate gates to control the count pulses used in the strobe counter and control the writing of status information in the memory.

CIRCUIT DETAILS

Timing Generator

The timing cycle for the system and a block diagram of the timing generator are given in Figs. 4 and 5, respectively. The radar trigger is used to start a Miller (3) run-down circuit which generates a 3300-micro-second gate. This gate defines the active portion of the radar sweep and is used to start a shock-excited oscillator tuned to 163,929 cycles. This oscillator always starts with a negative-going cycle and is stopped by the end of the sweep gate. The nominal 164-kc oscillations are detected in Mulitar (4) regenerative amplitude comparator which emits a pulse every time the 164-kc oscillations pass from positive through zero to negative producing a train of pulses of 6.1-μsec intervals corresponding to a half-mile radar range. The pulses from the Mulitar trigger a blocking oscillator and its output consists of a train of pulses starting with the radar trigger and stopping at the end of the sweep gate. The pulse train is then sent through a multitapped delay line and the various delays required are selected. Single-shot multivibrators are used to generate the read and inhibit command pulses and a blocking oscillator is used to generate a 1/4-μsec read strobe.

Magnetic Shift Registers

The magnetic shift registers (Fig. 6) are used in the driving network for the magnetic switch cores. Starting with a delayed radar trigger the flip-flop associated with a gate will be reset and gated timing pulses will be passed to a shift pulse driver. The driver will

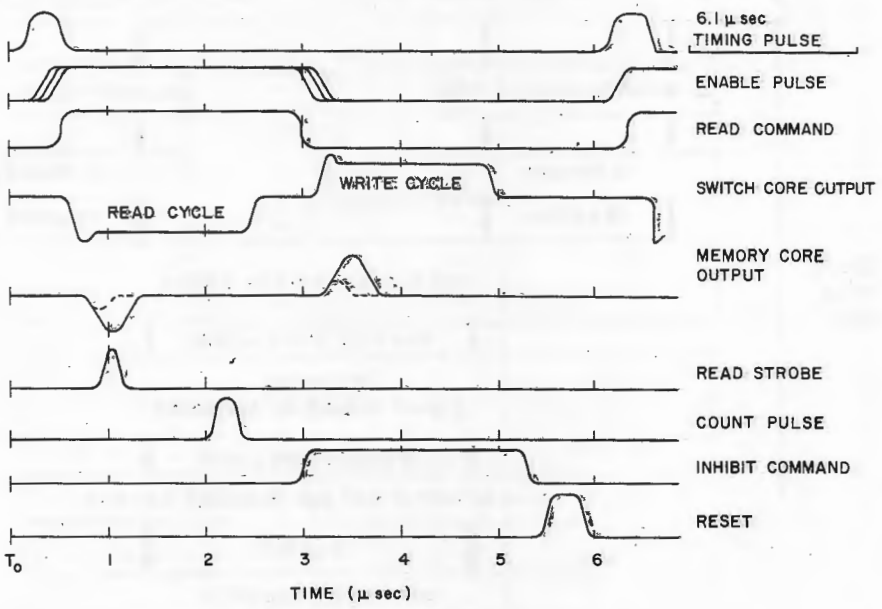

Fig. 4 - Timing cycle of typical range interval

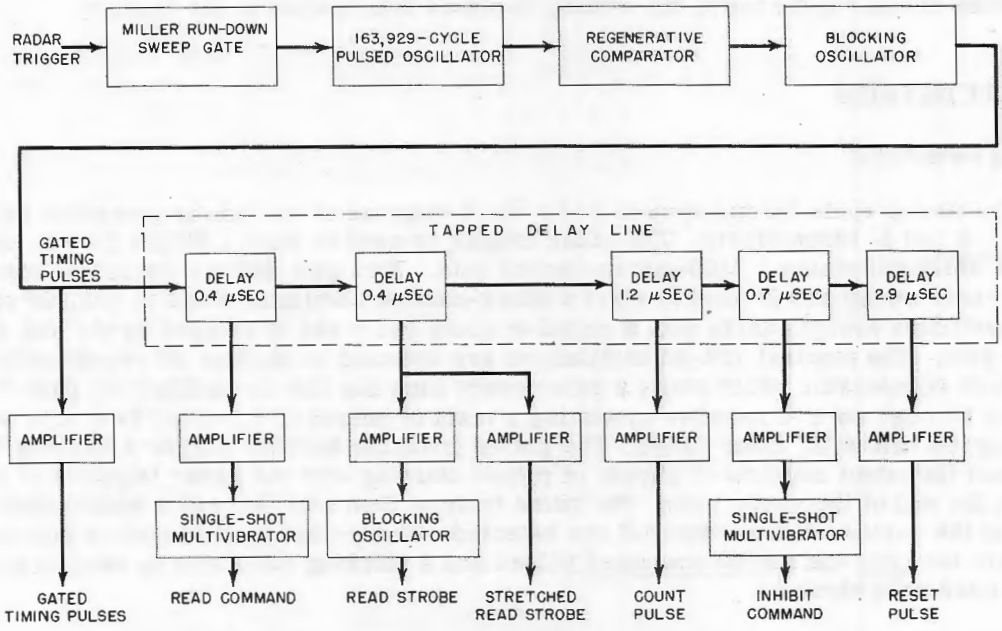

Fig. 5 - Block diagram of timing generator

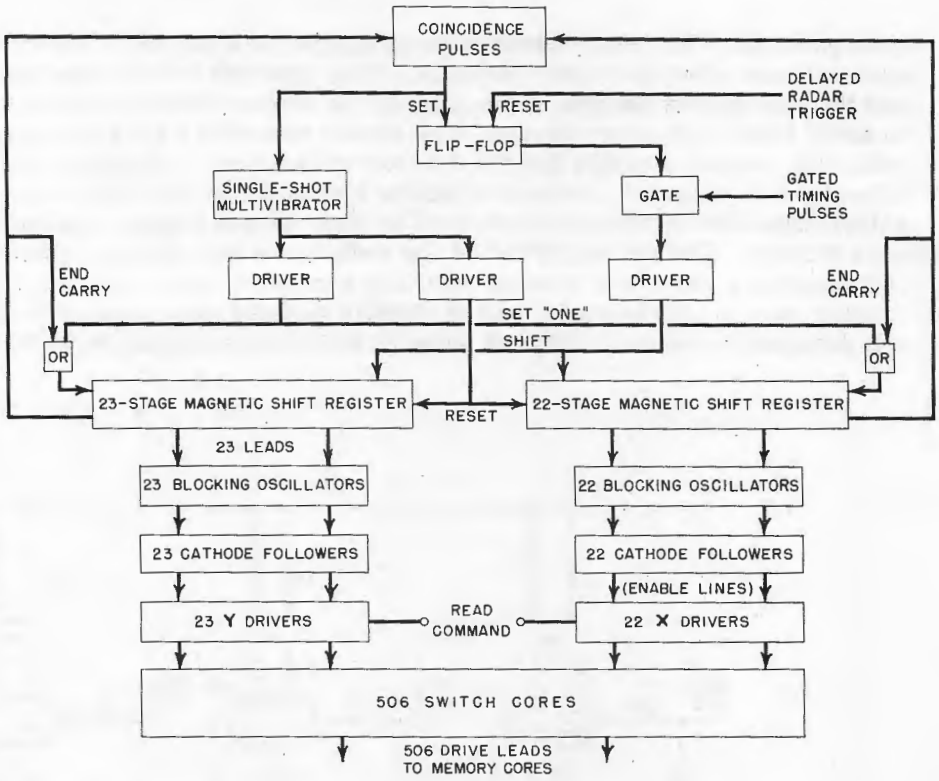

Fig. 6 - Block diagram of magnetic shift registers

shift the "one" stored in the first stage of each shift register to the next stage and this action continues until finally the one shifts from the last stage back to the first and the one is recirculated. It will be noted that one register has twenty-two stages, the other twenty-three. Thus, the end carries from the two counters will not occur at the same time except after twenty-two recirculations of the twenty-three stage register or 506 shifts. A coincident detector is used to determine when the end carries occur at the same time, and when coincidence is obtained the flip-flop is set and the gate prevents further shifts until after the reset. A single-shot multivibrator is also connected to the coincidence detector output. This circuit generates a long pulse which simultaneously feeds two drivers. One driver is connected to the shift windings of all but the first stage of each register. The other driver is connected through an "or" gate to the input winding of the first stage of both registers; thus, following the coincidence pulse the registers are reset to zero except for the first stages, which are set to one. Each stage of the shift registers is connected to a blocking oscillator and as the register is shifted one blocking oscillator in each coordinate is triggered. The pulse generated is coupled to grids of driver tubes via cathode followers and serves as an enable or selecting voltage for the driver tubes. The output of the magnetic switch cores is dependent upon coincident drive from the x and y shift registers. The result of the shift register cycle is to pulse the switch cores with a type of a diagonal television scan.

Switch Core Drivers

In the X or Y switch-core-driver circuit (Fig. 7) a type 5687 tube is cathode-driven to provide driving current for each drive line of the matrix of switch cores. The blocking oscillators controlled by the magnetic shift registers pulse the grids of one tube in each dimension to about eighty volts potential above ground. All other driver grids remain at

zero potential. The read command pulse applied to a parallel connection of type 6Y6 tubes causes these tubes to conduct strongly. Tube type 6Y6 is characterized by high perveance and the potential of the line connecting all the driver cathode resistors is rapidly reduced to about forty volts above ground. The driver tube with a grid potential held at plus eighty volts will conduct strongly for the duration of the read command, while the remaining tubes in each dimension have an effective bias of forty volts and are nonconducting. The rather high cathode resistors are used to improve the current regulation of the switch core drivers. The series circuit of the switch tube was chosen rather than a parallel circuit because a reduction of more than fifty percent of power required for the switch core drivers may be obtained at a cost of slightly reduced plate voltage swing. The drivers are designed to deliver a 300-ma pulse of 2-1/2 microsecond width to the switch cores.

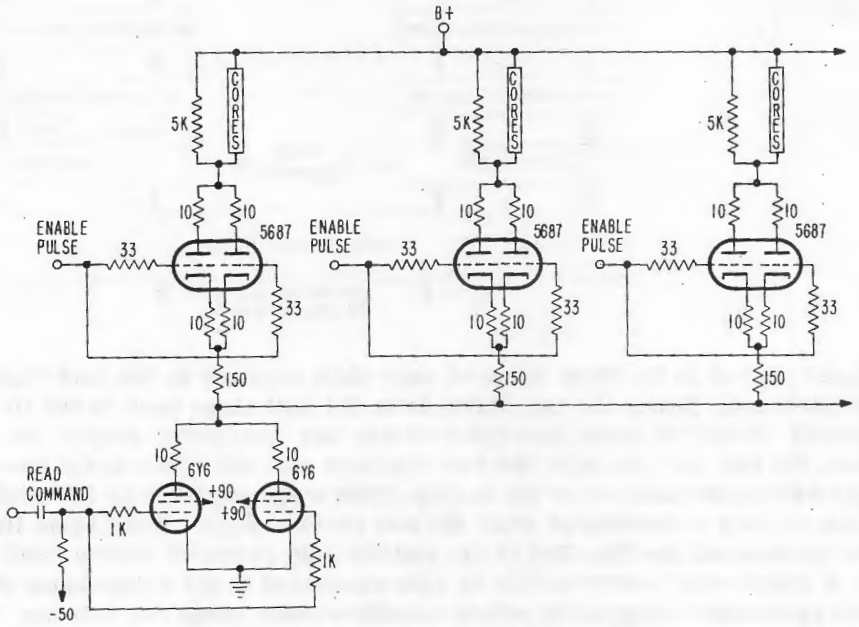

Fig. 7 - Schematic diagram of switch core drivers

Magnetic Switch Cores

The magnetic switch cores serve to select a single drive line out of the 506 for a read and write cycle. The cores are arranged in a two-dimension matrix (Fig. 8) with twenty-two cores connected in series on the X drive windings and twenty-three cores on the Y drive windings. Each core has two drive windings, a bias winding, and an output winding. The series connection of one drive winding forms the X drive line; the Y drive line is formed with the other winding. The switch cores are wound with 150 wraps of 1/8-mil-thick 1/8-inch-wide mo-permalloy 4-79 tape. This magnetic material has square hysteresis loop properties and rather fast switching time. The drive current of both X and Y lines and the bias current are all of equal magnitudes. The direction of current flow in the windings is such that the bias winding opposes the flux from current in the X or Y windings.

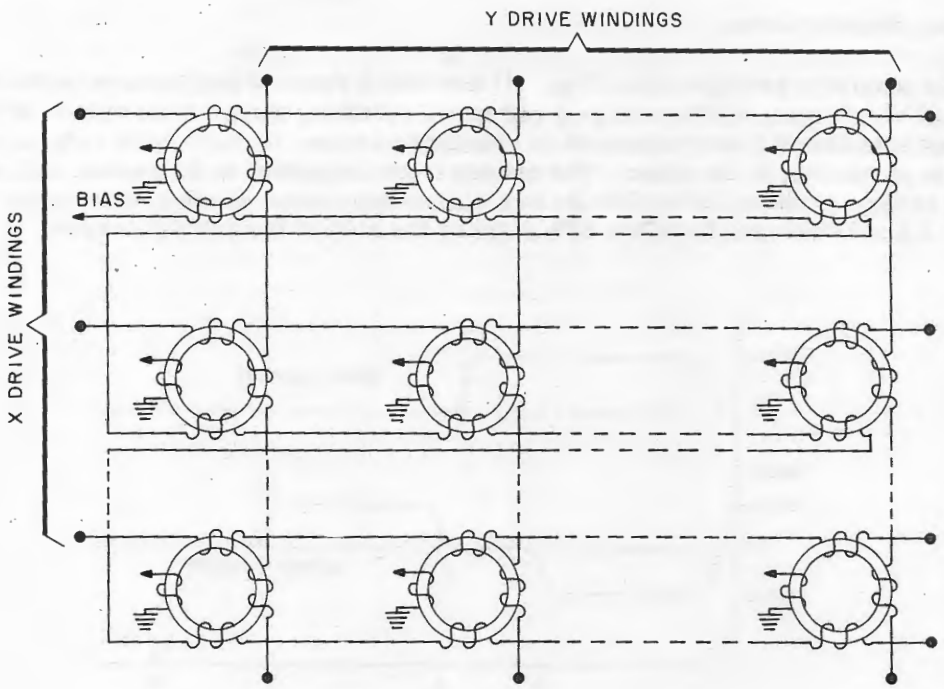

Fig. 8 - Switch core matrix

In Fig. 9, if current is passed in the X or Y windings the core is driven from the bias point 1 of negative saturation to point 2 near the knee of the hysteresis loop. This new point is still in the negative saturation region and there is very little flux change during the transition. However, if both windings are driven at the same time, the current in one may be thought to cancel the bias, the current in the other to drive the core to positive saturation point 3. The shift of the core from negative magnetic saturation to positive saturation results in a very large flux change within the core. The changing flux is coupled to the output winding and results in an output current. In this system the X and Y drive lines are pulsed at the same time. The core located at the intersection of the drive lines receives a coincident current and is driven to positive saturation for the duration of the drive pulse. At the end of the drive pulse the core is returned to negative saturation point 1 by the bias current. The other forty-three cores on the two active drive lines have only a partial drive and ideally would have zero output. Actually there is a spiked output owing to the lack of perfect squareness of the hysteresis loop. In practice this noise output is one seventh to one tenth the selected output. The switch core output (Fig. 10) is a pulse approximately two microseconds long and of eight volts amplitude across ten ohms load.

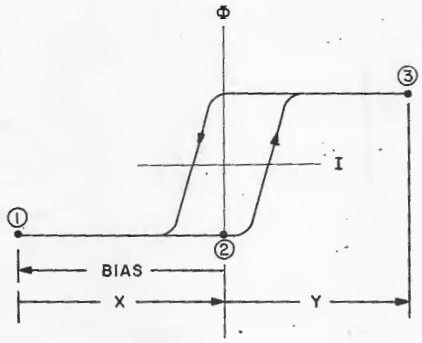

Fig. 9 - Operating path of switch core

Magnetic Storage Cores

The magnetic storage cores (Fig. 11) are small rings of magnetic material having properties of very square hysteresis loop and short switching time. A current of 800 ma for a time not less than 1.5 microseconds is required to drive the core from saturation in one sense to saturation in the other. The change from saturation to saturation will produce an output voltage of about 100 millivolts in a single-turn sense winding, said output occurring about 0.5 microsecond from the 90% point of the rise of the driving current.

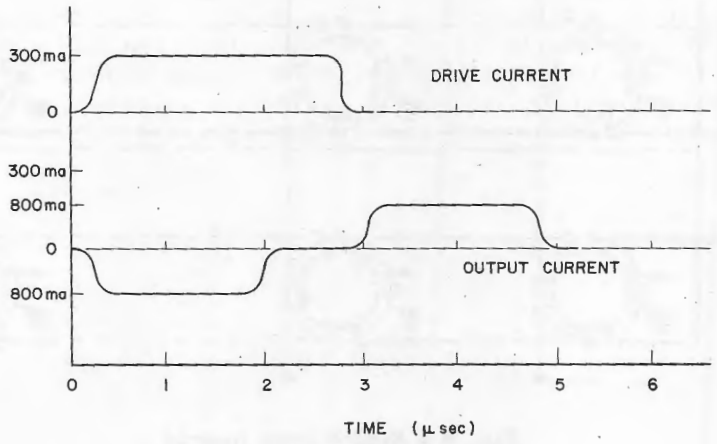

Fig. 10 - Switch core waveforms

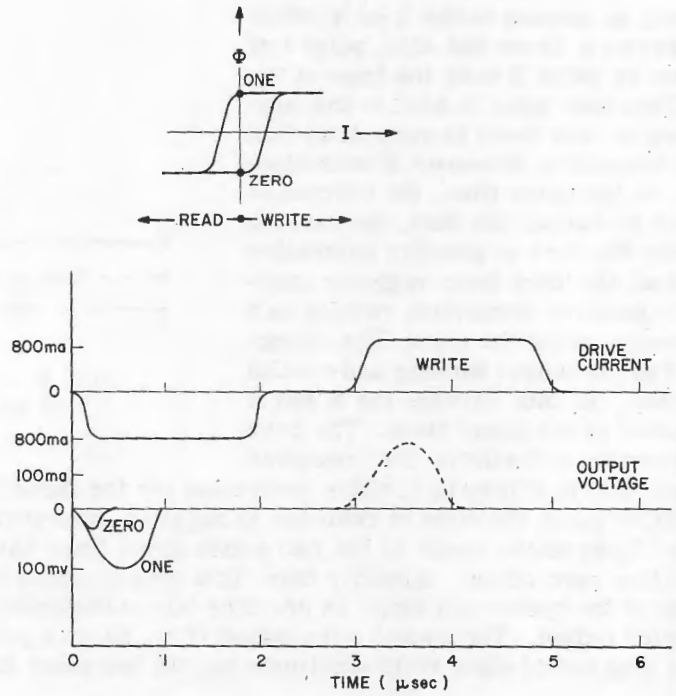

Fig. 11 - Storage core waveforms

In this system the storage cores are driven from a single-turn drive winding (5). The drive consists of a full-current (800-ma) pulse negative followed by a full-current positive pulse. The core output is taken from a four-turn sense winding that links all the cores of a digit plane. The same sense winding is used during the write cycle to inhibit the positive drive pulse from returning the storage core from negative saturation. Figure 12 shows the arrangement of the cores and windings on the frames. The entire storage is wound on eight frames, each frame holding 64 cores per digit and 13 digits. Figure 13 is a sketch of a single frame and Fig. 14 the complete storage.

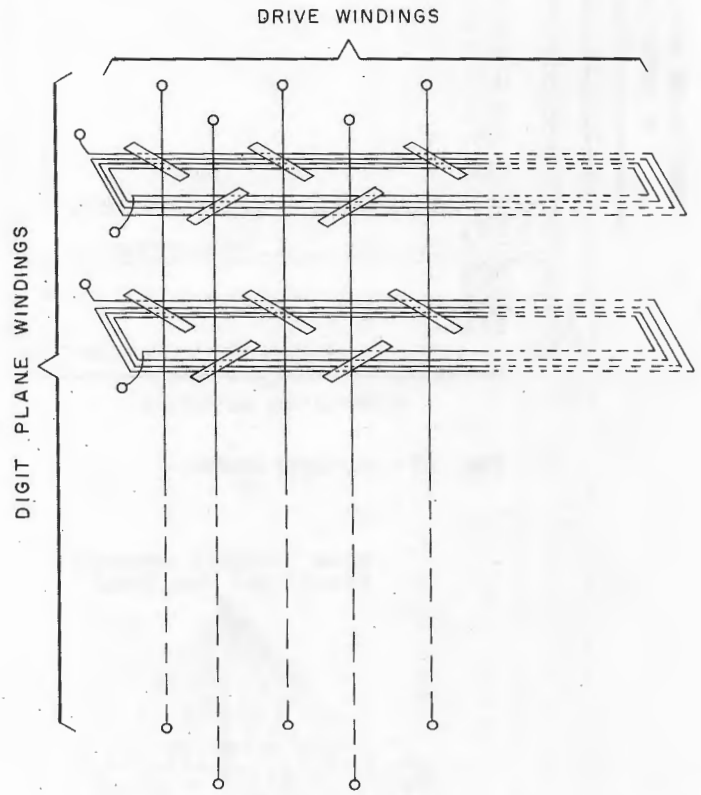

Fig. 12 - Memory array detail of digit plane windings

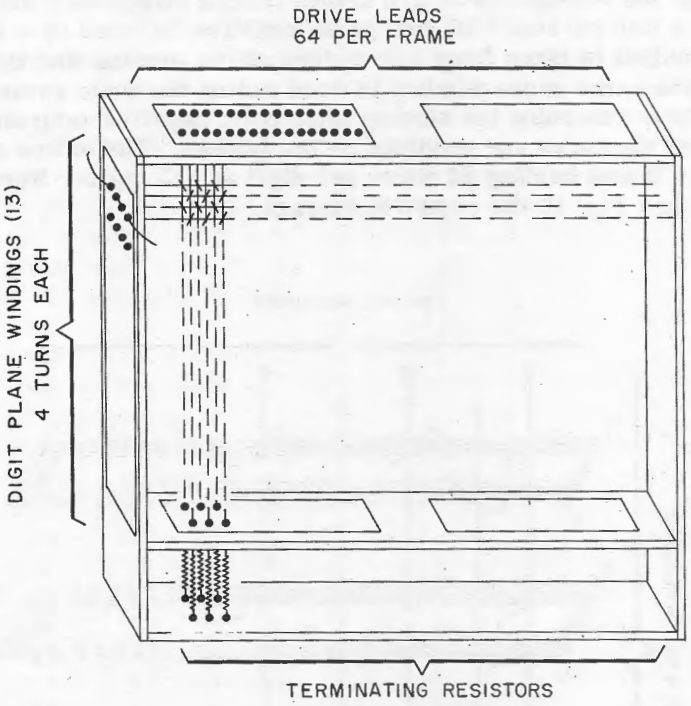

Fig. 13 - A single frame

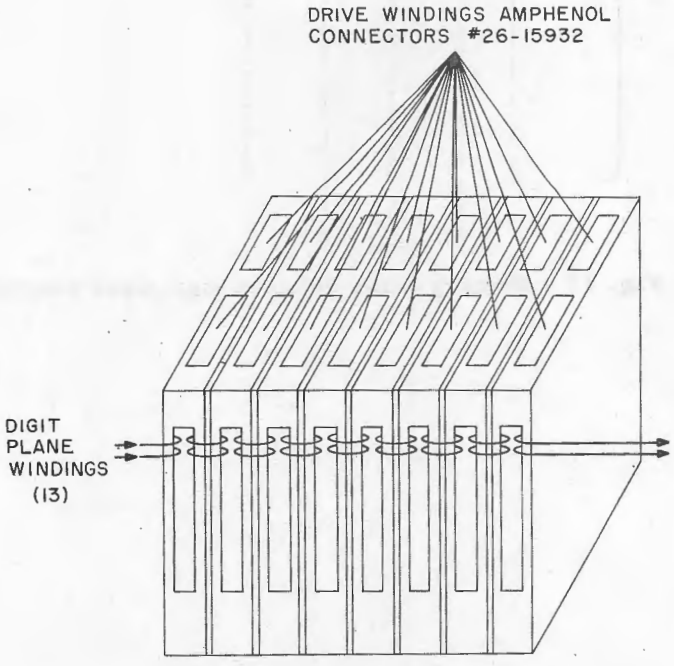

Fig. 14 - Complete storage, eight frames of 64 × 13 cores

Read/Write Amplifiers

The read/write amplifiers (Fig. 15) are used to amplify the output from the storage cores, determine the state of the core, and write information in the core. The storage core output is terminated in a transformer that provides an impedance step up for the read amplifier and step down from the inhibit driver. During the read cycle if a one has been stored a negative signal of approximately one volt will drive the grid of amplifier grid V2. This signal is amplified and inverted and becomes a positive twenty-volt signal on the suppressor grid of gate tube V3. At the proper time, a narrow strobe pulse is placed on the control grid of V3. Since both grids are near zero bias the tube conducts strongly and a "set" pulse is generated which will set the flip-flop. Setting the flip-flop to one will change the control grid of V1, the inhibit driver from zero bias to a large negative bias. An inhibit command pulse is sent slightly before the start of a write cycle and since the control grid is negative the inhibit driver will be cut off for the duration of the inhibit command. The inhibit driver will not conduct and the storage core will be returned to the one state during the write cycle. The flip-flop is always reset to zero at the end of a read/write cycle and if the storage core had contained a zero the noise signal to the suppressor grid of gate tube V3 would be too small for plate conduction during the read strobe. Thus, the flip-flop would not be set and the control grid of the inhibit driver tube V1 would be near zero bias. The inhibit command pulse will cause the inhibit driver to conduct and a current of one half the full drive current (i.e., 1/2 × 800 ma or 400 ma) flows in the digit plane winding. This current inhibits or opposes the drive current from the switch core and prevents the storage core being driven from changing to positive saturation or the one state. Also, since it is a one-half current drive it will not alter the state of any of the other 505 cores on the same digit plane winding. In other words, if the flip-flop is in the reset or zero state, a zero will be written in the storage during the write cycle and if the flip-flop is in the set or one state a one will be written in the storage.

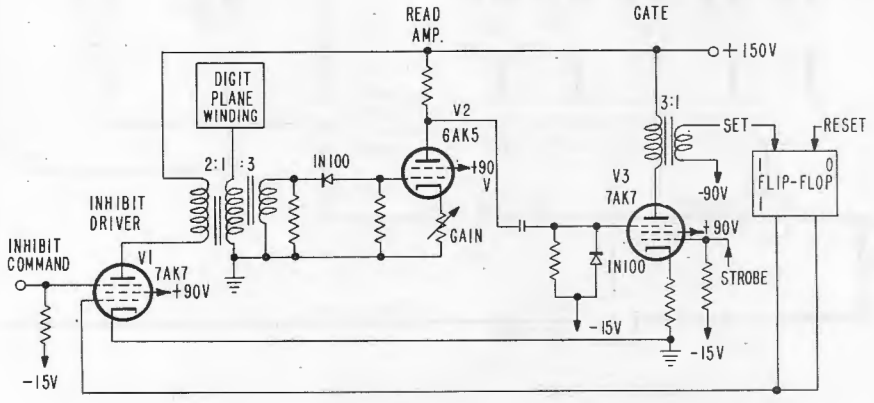

Fig. 15 - Simplified schematic diagram of the read/write amplifier

The flip-flops associated with seven of the read/write amplifiers are connected so as to form a binary counter as well as output register for the core storage. During the read portion of the cycle the counter is set as described above by the core storage. A count pulse may be added before the write cycle and the new value is then written into the storage.

Target Evaluator

The target evaluator (Fig. 16) is used to locate the leading and trailing edges of targets. For every range increment, the outputs of four previous strobes and the present quantized video are examined by the target evaluator. If three or more of the five channels contain ones, a leading-edge detected pulse is obtained and if two or less of the channels have ones, a trailing-edge detected pulse is obtained. The leading-edge detected signal sets a one in a status channel and this sets up gating circuits such that a count pulse is passed to the half-rate stage of the seven-stage counter. For every radar strobe that three or more ones are registered, the counter changes at the half rate. When two or less counts are registered, a trailing-edge detected signal is stored in a second-status channel. This changes the gating circuits so that now a count pulse is fed to the full-count-rate stage of the binary counter. Regardless of the number of ones in the target evaluator a full count rate will continue every radar strobe until an end carry is obtained from the counter. The end carry is used to gate the coordinates of the center of the target from the x and y counters into a temporary store and to reset the status channels to zero. The gating is such that with a zero in both status channels only a leading-edge detected signal will change the status and when a one is stored in the leading-edge status channel only a trailing-edge detected signal will change the status.

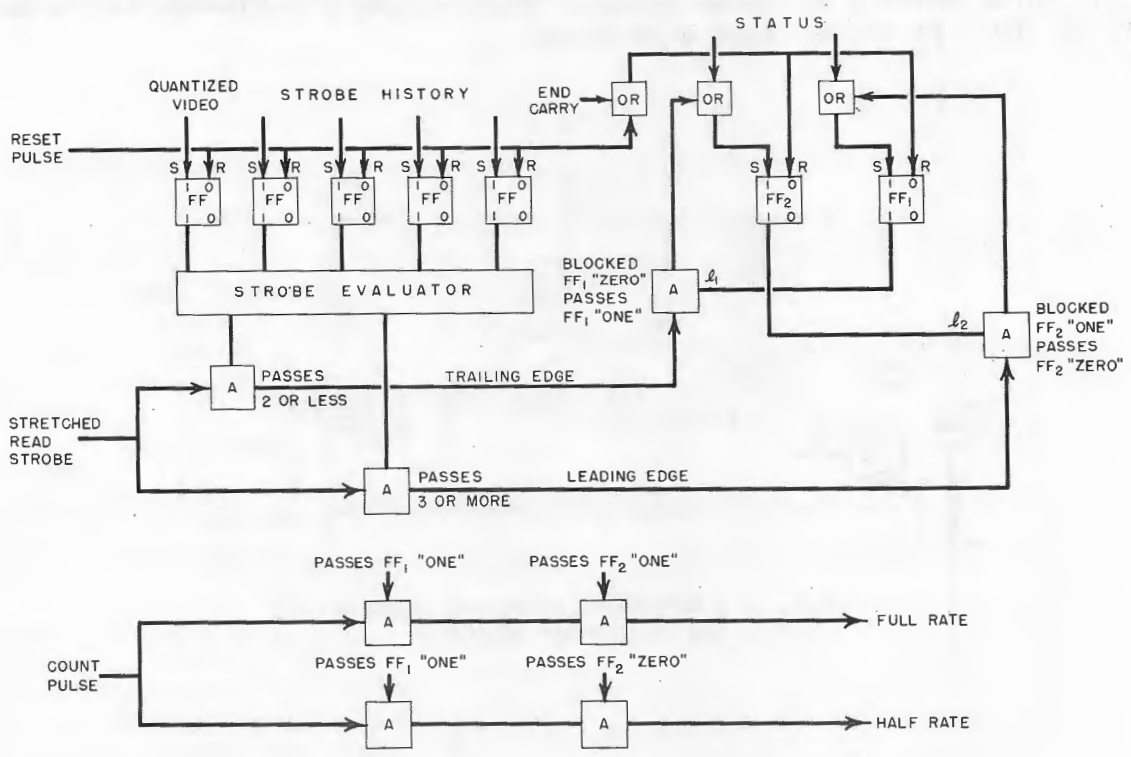

Fig. 16 - Block diagram of target evaluator

Coordinate Conversion

Figure 17 is a block diagram of method 1 for converting radar shaft rotation and radar ranges into Cartesian coordinates of binary x and y. The resolver is excited from a precision frequency generator and the amplitude is maintained constant by a feedback winding on the resolver. A characteristic of magnetic resolvers is that the outputs are either in phase or 180 degrees out of phase with the exciting voltage. It is therefore possible to strobe the output either in phase or out of phase with the excitation and obtain voltage samples that do not change polarity. In the system the output of the sin θ (or the cos θ) is fed to one side of a summing resistor. The other side is fed from an integrator and the summing junction is fed to a differential amplifier. Differences between the resolver and integrator outputs are amplified by the differential amplifier and fed to a current switch. The current switch is closed for a small strobe period during the crest of the resolver output. Thus, if the resolver carrier frequency is 1000 cycles a comparison between the resolver output and integrator output is made every millisecond.

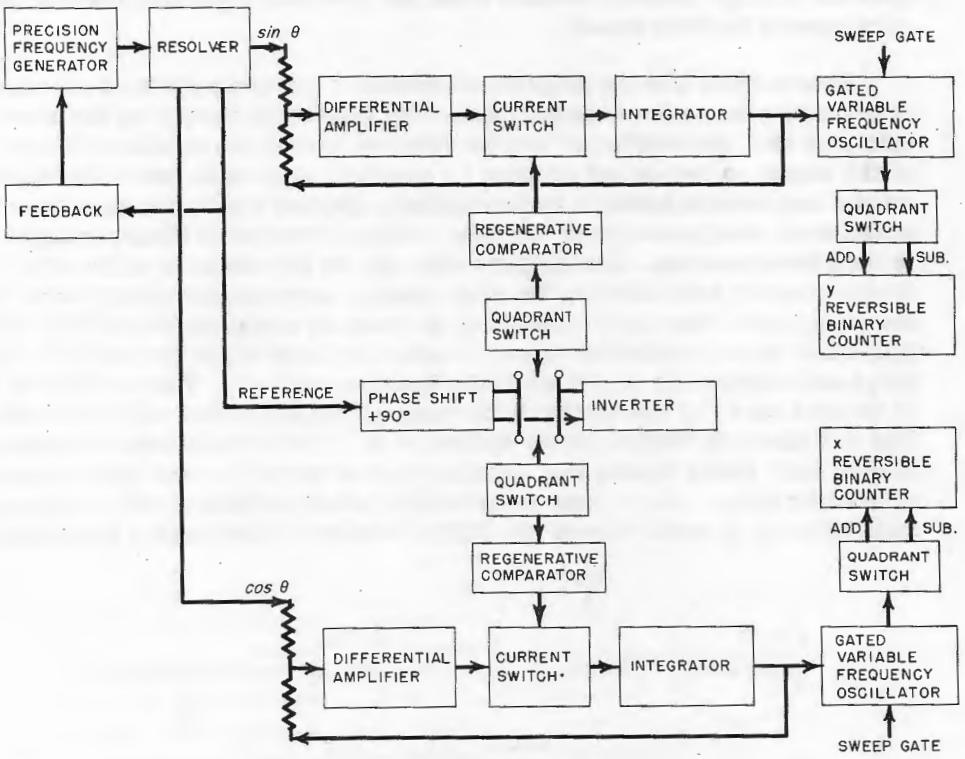

Fig. 17- Block diagram of coordinate conversion method 1

The strobe pulse is generated after shifting the phase of the exciting carrier 90 degrees. For one quadrant the phase-shifted exciting carrier voltage will just pass from negative through zero to positive voltage as the resolver output voltage is reaching its peak. As the resolver rotates and the phase between excitation and output inverts, the source for the strobe pulse must be inverted in order to keep the output polarity from changing. A quadrant switch is used to select the proper source and maintain output polarity. The zero crossing from minus to plus of the excitation voltage is detected by a regenerative amplitude comparator and a strobe pulse is generated on only the minus to plus transition. The action of the current switch is to charge and discharge the integrator capacitor so as to reduce to zero the difference between the resolver output and the integrator output. The outputs from the integrators are a slowly varying voltage equal in magnitude to sin θ (or cos θ).

A gated variable-frequency oscillator (6) is used to convert the variable voltage into pulse trains. The repetition rate of the pulses is proportional to the magnitude of the voltage from the integrator and the pulse train is operative only during a radar strobe. A reversible binary counter driven through a quadrant switch is used to count the pulses generated by the gated variable-frequency oscillator. The counters are reset at the end of every strobe period and will contain a binary equivalent of the Cartesian coordinates of the radar strobe during the live time of the radar.

A disadvantage of this system is that the counters may be changing at or during the time they are strobed for content. This means that some provision will have to be made to insure that the counters are not changing during the time the contents are being read out. Other disadvantages are the difficulty of determining the exact magnitude of the envelope of the resolver output and the exact point for quadrant change. The magnitude of the envelope ideally diminishes to zero and then increases. In the region of zero voltage variation, grid currents and zero adjustments tend to mask the actual magnitude voltage. The quadrant change likewise occurs when the function is passing through zero and the exact point cannot be determined.

Figure 18 is a block diagram of method 2 for conversion of coordinates. A code wheel is driven by the radar antenna shaft. The density of marks on the wheel has a sine distribution so that the number of marks detected in a given angular rotation varies as the sine of the angle. A two-stage counter (Δ counter) is used to count the number of sine (cosine) marks that occurs between radar strobes. During the radar dead time this Δ count is added to or subtracted from the sine (cosine) reversible binary counter. The Δ counter is then reset to zero. During the radar strobe the contents of the sine (cosine) reversible binary counter are added to the sine (cosine) accumulator every radar half mile. During the radar dead time the accumulator is reset to zero; the reversible binary counter is not. The value in the reversible binary counter is large when the function $\sin\theta$ or $\cos\theta$ is large and conversely small when the function is small. This results in the repetition rate of the end carry of the accumulator varying in accordance with the function $\sin\theta$ or $\cos\theta$. The end carry is used to drive another x or y reversible binary counter. Before the beginning of each radar strobe this counter may be preset to own radar coordinates or some off-center value. The x and y reversible binary counters will contain after every half-mile interval of radar sweep the digital number of the x and y coordinates for the interval.

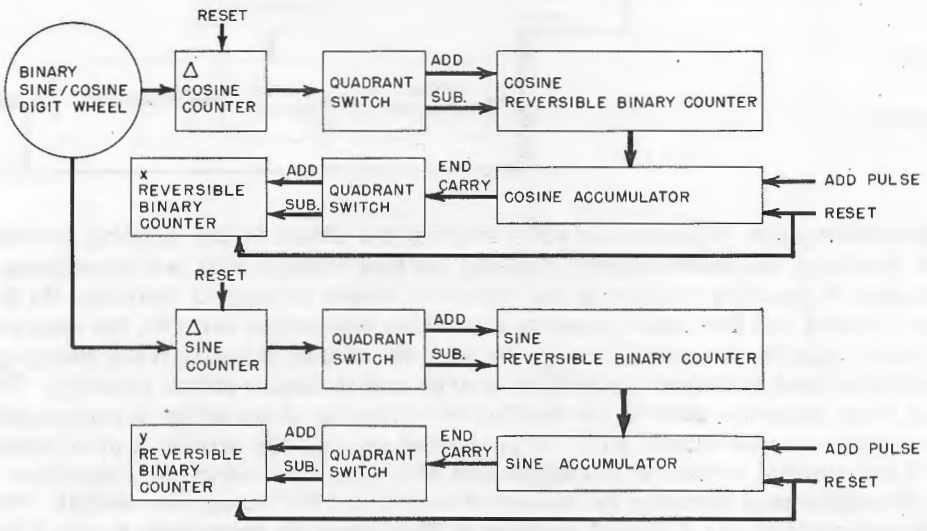

Fig. 18 - Block diagram of coordinate conversion method 2

An advantage of this system is that the x and y counters are in synchronism with the rest of the data reduction system and gating of the x and y coordinates into the temporary storage is simplified. Another advantage is that the accuracy of the system is readily predicted from the number of binary stages and the accuracy of the code wheel. It is estimated that an accuracy of one part in one thousand will be attainable easily.

The major disadvantage is the large number of tubes required. Further advances in transistor circuitry may alleviate this problem and more effort will be directed toward simplifying the circuit. Another disadvantage is the lack of synchronism between the strobe marks on the code wheel and the interval when the Δ counter is read out into the reversible binary counter. In addition, if the cosine (sine) reversible binary counter becomes in error it will carry this error until reset during a quadrant change-over.

Another method for coordinate conversion is shown in Fig. 19. This is similar to the method shown in Fig. 18 except that the addend for the cosine (sine) accumulator is obtained from a binary register. This register is set during radar dead time to a value proportional to the cosine (sine) of theta directly from a nonambiguous digit wheel driven by a mechanical motion resolver.

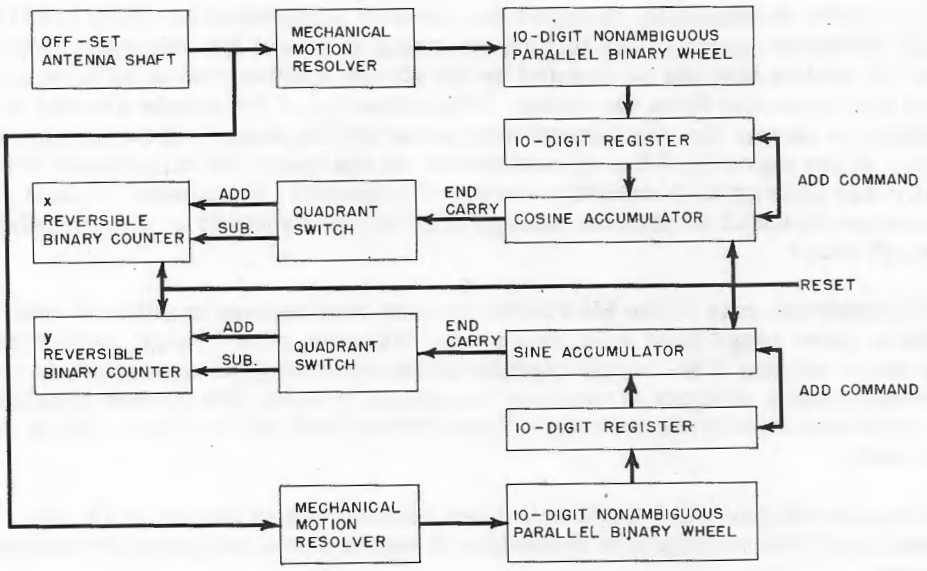

Fig. 19 - Block diagram of coordinate conversion method 3

The method provides advantages of simplicity and synchronism between range and the x and y coordinates. A disadvantage is a requirement of two mechanical motion resolvers, one for sine and one for cosine. However, it is believed that with proper design and construction the mechanical and electrical conversion from shaft rotation to electrical binary output may be accomplished with an accuracy better than one tenth of one percent.

DISCUSSION

The system has some immunity to light clutter owing to the rules for determining the leading edge of a target. The degree of clutter rejection, however, can only be ascertained after actual operational tests are performed. Additional clutter gating may be secured in heavy clutter areas by rejecting all targets in which a trailing edge was never detected, i.e., targets where the end carry from the strobe counter occurs even though a trailing edge was never detected. If desirable, a dynamic range-operated clutter gate may be added in the line between the quantized video and the strobe evaluator. The gate would be controlled by a flip-flop used to store the value of the preceding range interval and would allow only quantized video that does not immediately follow a signal in the preceding range interval to pass to the target evaluator. Neither system would enhance the signal in clutter areas, and in fact will tend to suppress the true signals as well as clutter.

The system is primarily designed for aircraft installation on early warning picket aircraft. However, many of the techniques would be useful for shipboard installations. The number of strobes that can be counted by the strobe counter should be determined by the hits per scan expected from the radar. If the capacity of the strobe counter is made too large there is danger that two targets may occur at the same range and only one would be detected. If the capacity of the strobe counter is too small the target may extend beyond the full count and result in detection error. Fortunately, the number of digit planes used in the system is small so that the number may be varied easily to accommodate almost any search radar.

The repetition rate of the MATALOC system may be synchronized to any radar that provides a radar range of at least 253 miles. However, short range, high-repetition-rate radars could be used if the range capacity of the system were appropriately reduced. In the present system azimuth errors are introduced if either the antenna rotation rate or radar repetition rate is not constant. These errors will not be large, and no compensation will be used.

It is expected that MATALOC will do an efficient job of reporting targets. However, if manual insertion of targets is desirable, it can be added with considerable expansion of equipment.

The leading edge selection rule of three hits out of five strobes is based on the following argument. In any detector there is a probability that noise will exceed a threshold during the detection interval. If the threshold-to-average-noise ratio is increased the probability that noise will exceed the threshold is decreased. Likewise, if signal and noise together appear at the detector there is a probability that signal plus noise will exceed the threshold in the detection interval. If the signal-to-average-noise ratio is increased the probability of detection is increased. The false alarm rate is defined as the number of times noise alone exceeds the threshold during the detection interval to the number of detection intervals. By adjusting the threshold level, it is possible to calculate and control the false alarm rate. Having established a false alarm rate and therefore the threshold level, it is possible to calculate the minumum signal-plus-average-noise to average-noise ratio

for some arbitrary detection probability, say 90%. One may reason that if the false alarm rate is held constant there is an optimum selection rule for the five strobes. If a rule of two out of five is chosen, the threshold level would have to be high to prevent false alarms and hence the signal would have to be strong to exceed the threshold. If a rule of five out of five is chosen, then the signal would have to be strong to insure that every strobe is quantized even though the threshold level is considerably lower than in the two-out-of-five case. Thus, one would guess that the best selection rule should be between two out of five and five out of five.

Results of calculations (Appendix A) would indicate that the most sensitive detector obtains with a rule of three out of five. This is an optimum simple selection rule regardless of the false alarm rate chosen as long as it is constant for all the detectors. Furthermore, the detector is relatively insensitive to false alarm rate as changes in the false alarm rate of several orders will not change the detector sensitivity over several decibels.

At the present time no active effort is being made to miniaturize. The large number of driver tubes required for exciting the switch cores have a filament dissipation of almost 400 watts. It would materially reduce wasted heat and power if the vacuum tubes could be replaced with power transistors. However, at present, the transistors capable of switching large currents cannot switch in a small enough time to operate in the system.

It is contemplated to construct the complete vacuum-tube driver system for the switch cores, but only one row and one column of switch cores will be used in the initial tests. This will enable tests of the driver circuits using only 55 switch cores rather than 506 switch cores. Also the storage cores will be so wired as to test a single-digit plane consisting of 506 cores rather than the complete memory. After successful operation of the single-digit memory system is obtained, the number of digits will be increased to thirteen and the number of storage cores per plane reduced to forty-six. This will allow testing of the timing and target splitting over a reduced range of twenty-three miles. It is believed that this reduced range will be sufficient to evaluate all of the principles of the system and that expansion to the complete system will be based upon results obtained at this stage.

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APPENDIX A
Analysis of Target Selection Rules

The best selection rule for the five-strobe target analyzer is the one that will detect a target with the smallest signal-power to average-noise-power ratio for a given detection probability and a given false alarm rate. The problem is to determine the best selection rule.

In the quantizer, there is a probability that noise alone in the absence of signal will exceed the threshold and be quantized. This probability is a function of video bandwidth to detection time and threshold power to average noise power. There is also a probability when both signal and noise are present, that the signal-plus-noise power will exceed the threshold and be quantized. The selection rules are really a calculation of the probability that an event will happen at least k times out of n trials if the probability of the event is p_1. Thus, a reasonably accurate first order approximation of the probability of detection can be made by considering the probability

$$P_d = p^n + {}_nC_{n-1}\, p^{n-1}\, q + {}_nC_{n-2}\, p^{n-2}\, q^2 + \ldots + {}_nC_k\, p^k\, q^{n-k} \qquad \text{(A1)}$$

where

P_d = probability of detection

p = probability of quantizing $(q = 1 - p)$

n = number of strobes analyzed

k = number of hits required for detection

${}_nC_k$ = number of combinations of "n" things taken "k" at a time.

Equation (A1) is plotted in Figs. A1 and A2. The graphs are the probabilities that at least two out of five, three out of five, etc., events will happen out of five trials. In our case, this corresponds to the probability that after five radar strobes, the target evaluator would indicate a target present based on selection rules of two out of five, three out of five, etc.

The probability that an event will happen in one trial, i.e., that the quantizer will contain a one, is a function of threshold-to-average-noise ratio in the absence of signal. In the presence of signal, it is also a function of the signal-to-average-noise ratio. In comparing the selection rules, it is necessary to maintain the same detection false alarm rate, i.e., some fixed number of false alarms per unit time or radar scans, regardless of the selection rule chosen. This may be accomplished by adjusting the threshold-to-average-noise ratio of the quantizer until the desired probability for quantizing noise alone is obtained. It is more convenient, however, to use the graph in Fig. A2 choosing the detection probability equal to the false alarm rate. The false alarm rate is defined as the number of false alarms detected to the number of quantizing intervals in the detection period. For scanning search radars of particular interest in this problem, a false alarm rate of about 10^{-6} corresponds to about one false alarm per scan. Thus, from Fig. A2 one may obtain values for the probability of quantizing, p_q, corresponding to each selection rule, holding the false

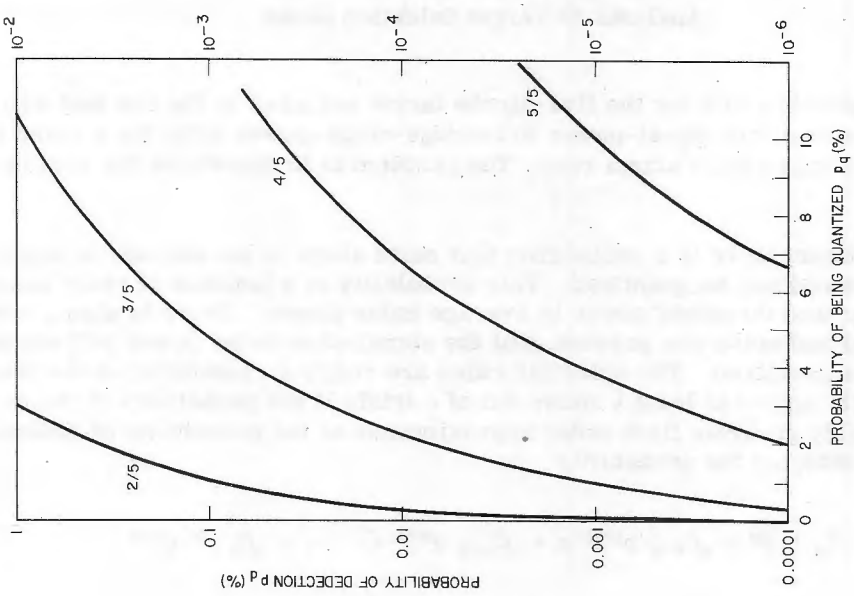

Fig. A2 - Probability of detection vs. small probability of being quantized

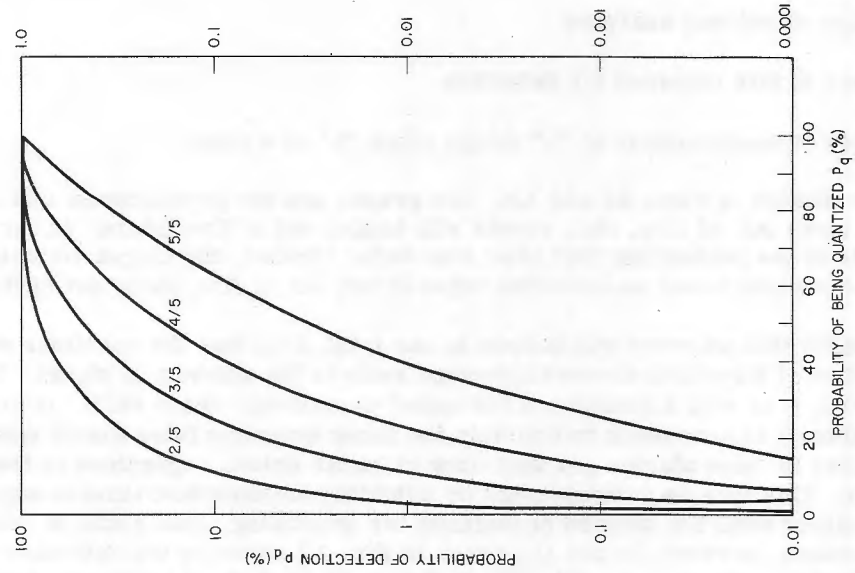

Fig. A1 - Probability of detection vs. probability of being quantized

alarm rate constant. In a similar manner, from Fig. A1 one may obtain values for the probability of quantizing, p_q, for a common probability of detection, say 90 percent, with a signal present. The threshold-to-average-noise power ratio for a given probability of quantizing may be determined from the graph in Fig. A3. The graph is plotted from the equation

$$p_q = e^{-Y_B} \tag{A2}$$

which is a special case of Eq. (A3) when there is no signal present.

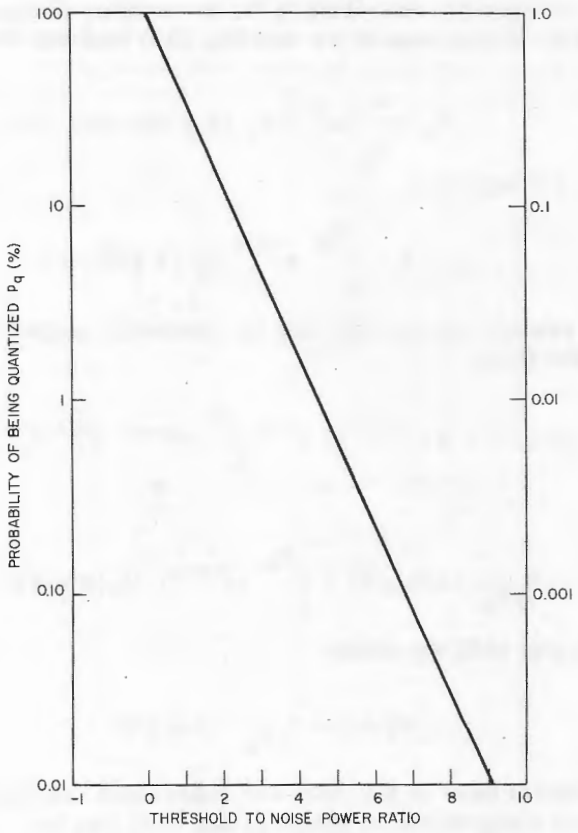

Fig. A3 - Probability that noise will be quantized vs threshold-to-noise power ratio

In order to compare the selection rules as a function of signal-to-noise power ratio one must compute the probability of being quantized as functions of signal-to-noise power and threshold-to-noise power. The probability that the quantizer will contain a one is given by Marcum* as

$$p_N = \int_{Y_B}^{\infty} \left(\frac{Y}{Nx}\right)^{\frac{N-1}{2}} e^{-Y-Nx} I_{N-1}\left(2\sqrt{Nx}\right) dY \tag{A3}$$

*Marcum, J. I., "A Statistical Theory of Target Detection by Pulsed Radar," Project Rand Research Memorandum RM-754, December 1947.

where

N = number of variates of signal-plus-noise integrated

x = signal-to-average-noise power ratio

Y = envelope-power to average-noise-power ratio

Y_B = threshold-power to average-noise-power ratio.

Equation (A3) is the cumulative distribution for N variates of signal-plus-noise following a square-law detector. In our case $N \equiv 1$ and Eq. (A3) reduces to

$$P_1 = \int_{Y_B}^{\infty} e^{-Y-x} I_0 (2\sqrt{xY})\, dY \tag{A4}$$

Changing the limits of integration

$$P_1 = 1 - \int_0^{Y_B} e^{-Y-x} I_0 (2\sqrt{xY})\, dY \tag{A5}$$

Equation (A5) is not readily solved, but may be treated as a special case of an incomplete Toronto function of the form

$$T_B (m,n,r) = 2r^{(n-m+1)} e^{-r^2} \int_0^B t^{(m-n)} e^{-t^2} I_n (2rt)\, dt \tag{A6}$$

In particular

$$T_{\sqrt{Y_B}} (1,0,\sqrt{x}) = \int_0^{Y_B} (e^{-Y-x}) [I_0(2\sqrt{xY})]\, dY \tag{A7}$$

Substituting Eq. (A7) into (A5) we obtain

$$P_1 = 1 - T_{\sqrt{Y_B}} (1,0,\sqrt{x}) \tag{A8}$$

Equation (A8) is a special case of Eq. (A3) and represents the distribution of signal-plus-noise when there is no integration. A graph of Eq. (A8) has been plotted in Fig. (A4) and from it the signal-to-average noise ratio may be determined in terms of probability of quantying and threshold-power to average-noise-power ratio.

A graph similar to the one in Fig. A5 may be prepared to indicate the variation of signal-to-average noise vs. false alarm rate for the selection rules. In Fig. A5 the detection probability is 90 percent, although other graphs may be plotted for different detection probabilities. It may be noted that the three-out-of-five selection rule is the optimum rule for the target analyzer.

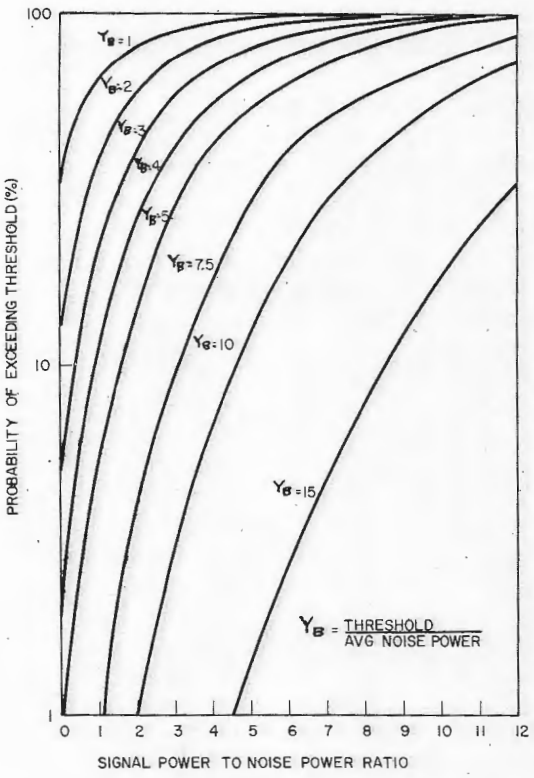

Fig. A4 - Probability that signal plus noise will be quantized vs. signal-to-noise power ratio and threshold-to-noise power ratio

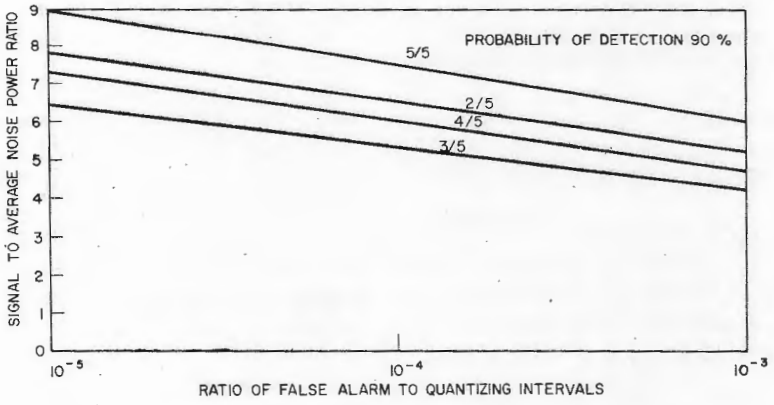

Fig. A5 - Comparison of selection rules

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