2027

DECLASSIFIED

NRL Report 4901

[redacted]

[redacted]

UNCLASSIFIED

SYNCHRONIZING EQUIPMENT FOR USE WITH THE COMPLEX-MODULATED-PULSE DEMODULATOR

[UNCLASSIFIED TITLE]

DECLASSIFIED by NRL Contract
Declassification Team
Date: 28 MAR 2017
Reviewer's name(s): [redacted]
[redacted]
Declassification authority: NAVY DECLASS GUIDE/ NAVY DECLASS MANUAL, 11 DEC 2012 08 SERIES

Julian C. Holmes

Countermeasures Branch
Radio Division

UNCLASSIFIED

UNCLASSIFIED

April 9, 1957

[redacted]

DISTRIBUTION STATEMENT A APPLIES.
Further distribution authorized by
UNLIMITED only.

NAVAL RESEARCH LABORATORY
Washington, D.C.

[redacted]

UNCLASSIFIED

DECLASSIFIED

[redacted]

CONTENTS

[redacted]

ABSTRACT

[redacted]

The need for a general system for the demodulation of complex pulse modulations has been felt for some time. Such a system has been developed, and has been described in NRL Reports 4463 and 4574. Since the publication of these reports operational groups have expressed the desire for auxiliary equipment to provide for synchronization of present equipment with certain types of pulse systems. Equipment existing until now demodulated only those signals having sync pulses of higher amplitude than the information pulses. A new Pulse-Width and Pulse-Group Synchronizer has been developed. Its purpose is to derive synchronization from sync pulses which differ from other pulses not in amplitude, but with respect to some other pulse parameter. Synchronization can now be derived from pulses that are wider than the signal pulses or from groups of two or three pulses with interpulse spacing of from 0.3 to 20 μsec. Recommendations are made for further improvement of existing circuits.

PROBLEM STATUS

This is a final report on the complex-pulse-demodulation portion of problem R06-04; work is continuing on other portions of this problem. This is the final report on problem R06-22.

AUTHORIZATION

NRL Problems R06-04 and R06-22
Projects NE 071-240-2-4 and NSA 332-5802
BuShips Problem S-1255.7 and NSA Task No. 332-5802

Manuscript submitted February 4, 1957

[redacted]

SYNCHRONIZING EQUIPMENT FOR USE WITH THE COMPLEX-MODULATED-PULSE DEMODULATOR
[Unclassified Title]

INTRODUCTION

During the past ten years much time and money have been spent in the field of pulse communication. Pulsed radio-frequency carriers are used today not only for land communication but also for missile guidance, ship-to-ship communication, and the various activities where telemetering is required. With the widespread use of this technique, it is natural to inquire into the ways in which an enemy might use this type of communication to his advantage. Present techniques enable him to produce simple types of pulse modulation with a very small amount of equipment. The various types of time-modulated pulses provide signals which are relatively noise-free when compared with AM signals. Pulse signals may be demodulated with ease at the receiving end, provided the receiver knows what sort of modulation to expect and, in the case of multichannel signals, the method of synchronization employed.

What makes these types of systems doubly attractive is that security of information transmitted by these means is easily kept by the parties involved, provided the enemy is not extremely well versed in such techniques. Encoding and decoding are relatively simple if the parties performing the respective functions are in collaboration. For the outside interceptor to decode such a signal, however, could be a task of mammoth proportions. Not only is decoding difficult, if the signal is coded at all, but the simple demodulation of the pulse modulations can easily be made very difficult. This can be accomplished by simply producing modulations of an order of magnitude too small to be detected on conventional pulse analyzers. Or it can be done in a multichannel setup by simply "hiding" the sync pulse from the enemy. Lastly, a sync pulse might not even be sent.

Thus, with the present state of the art, a reasonably clever enemy need use no coding at all to conceal what was being sent over his communication channel. It is this sort of thought that has prompted countermeasures people to investigate the general problem of pulse demodulation. As a result, equipment capable of handling pulse amplitude, width, position, period, and frequency modulations has been developed and is being used in the field.

Along with the actual production on a small scale of demodulation equipment for field use, requests have come in for special auxiliary apparatus to enable present demodulation equipment to demodulate certain special signals that are known to be used today. This equipment was needed so that sync pulses used in multichannel communication systems could be sorted out from the information pulses. The Complex-Modulated-Pulse Demodulator (CMPD) is capable of performing this operation only if the sync pulses in the signal are of higher amplitude than the information pulses in the various channels. Thus, sync pulses that are identified by their width, or grouped pulses which together make up the sync pulse are not recognized by the CMPD. It is the purpose of the Pulse-Width and Pulse-Group Synchronizer (PWGS) to recognize these two types of sync pulses and convert them to high-amplitude ones which are sent to the CMPD sync Schmitt circuit.*

---

*Holmes, J. C., "A Demodulator for Complex-Modulated Pulses," NRL Report 4463 ([redacted]report, Unclassified title), January 1955; and "Circuit Modifications for Complex Modulated Pulse Demodulator," NRL Report 4574 ([redacted] report, Unclassified title), August 1955

Provision also has been made to enable the operator of this equipment to examine a new signal visually before attempting demodulation of its channels. Conventional slave-sweep analyzers of the voltage or slope triggered type are generally incapable of displaying a steady pulse pattern when all signal pulses have equal amplitudes. In order to examine each pulse in detail, some sort of preliminary synchronization of the pulse train must be established. If this is not done, each successive sweep of the pulse analyzer trace is likely to be initiated by a different pulse in the train. Thus a sync pulse in the train will be shifting in the display, and the probability of locating it, identifying it as the sync pulse, and measuring its parameters so that the sync circuits may be properly adjusted is nil. Only if the pattern can be stabilized, can the characteristics of the sync pulse be accurately determined. Circuits to accomplish this task have been incorporated into the PWGS.

GENERAL DESCRIPTION

The major components of the presently existing CMPD are block diagrammed in Fig. 1. The amplified raw video signal from the video amplifier is ordinarily sent to a voltage-sensitive sync Schmitt circuit which produces a pulse at its output whenever the amplitude of the input pulse exceeds a certain threshold level. Figure 2a shows a multi-channel signal with a sync pulse of amplitude higher than all other pulses in the train. With the Schmitt-circuit threshold level properly adjusted, only the sync pulse passes through the Schmitt circuit. This pulse in turn triggers the pulse-selection-gate multivibrators which in conjunction with the pulse selector determine the particular channel that is to be demodulated.

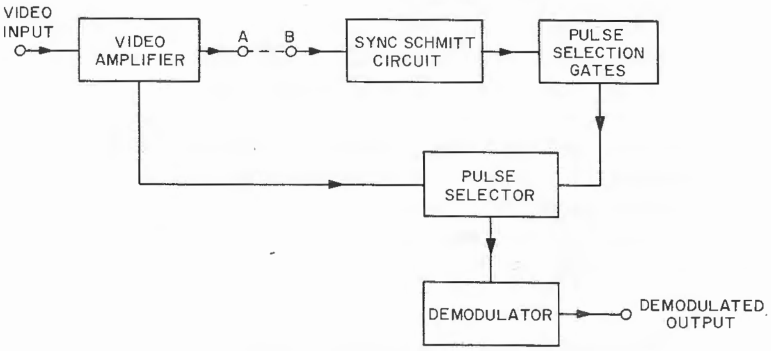


Fig. 1 - The basic diagram of the CMPD

If, however, the sync pulse in the raw video signal is of a different type, such as shown in Figs. 2b and 2c, a device of some sort must be placed between points A and B (Fig. 1) to produce from the sync pulse one that is suitable for triggering the CMPD sync circuit. The PWGS is essentially connected between these two points. In order that the PWGS can produce a suitable high-amplitude sync pulse from a sync pulse of a different type, some facility must be provided in order that the signal may be examined pulse by pulse so that the sync pulse can be located and identified. In the CMPD as it now exists are circuits (Fig. 3) which mix the output of the sync Schmitt circuit with the raw video signal and send the combination to a slave-sweep display analyzer of the AN/SLA-2 or the AN/APA-74 variety.

[redacted]

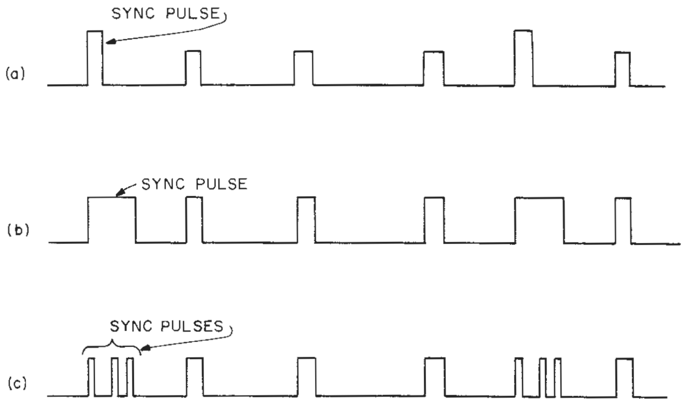


Fig. 2 - Multichannel signals with various types of sync pulses; (a) high-amplitude sync pulse, (b) wide sync pulse, (c) sync groups of three pulses

Thus the operator sees the actual signal with the sync signal superimposed. The signal is automatically synchronized on the screen when the sync pulse is of a higher amplitude than the rest. If the raw video sync pulse is indistinguishable in amplitude from the other pulses (Figs. 2b and 2c), the pattern on the screen will be unstable, with the Schmitt circuit synchronizing on every pulse or on no pulses, depending on the setting of the sync threshold control. In either case, any one of the channel pulses or the sync pulse is equally likely to trigger the display sweeps in the analyzer, so that the sync pulse will generally appear in a different position for each successive sweep. Identification of the sync pulse under these conditions is very difficult.

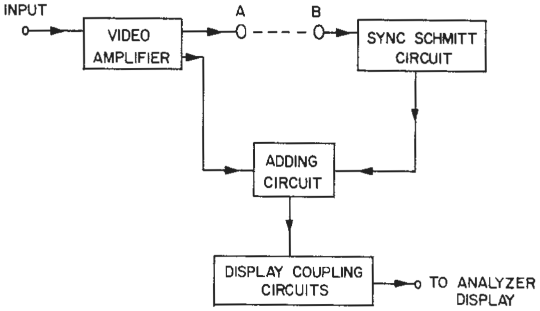


Fig. 3 - The CMPD display circuits

If it were possible to force a given channel pulse to trigger each successive sweep of the analyzer display, the pattern would stabilize regardless of which channel pulse is chosen. Suppose, for example, that a signal consists of 11 pulses, one for each of 10 information channels, with the 11th pulse being the sync pulse (Fig. 4). Assume that the average spacing between the sync pulse and any information pulse remains constant. Thus the average time elapse between two successive occurrences of the nth pulse ($1 \leqq n \leqq 11$) is the sum of all the pulse spacings, which is obviously the same for any n. If pulse 3 were allowed to trigger a sync circuit, and if a time base a little shorter than the sum of all the pulse spacings were initiated at the time of triggering, the time base would terminate just before the next occurrence of the number 3 pulse. If throughout the duration of this time base the sync circuit is prevented from operating, and if at the termination of the time base the signal is again allowed to trigger the sync circuit, output pulses from the sync circuit will occur simultaneously with and only with the number 3 pulse.

[redacted]

If this synchronizing pulse is sent to the CMPD sync Schmitt circuit, it will be superimposed on the video signal in the display circuits, and the analyzer sweeps will be initiated with the occurrence of the number 3 pulse. The signal as it would appear on an AN/SLA-2 screen is shown in Fig. 5a. This method of deriving stable pulse patterns has been incorporated into the PWGS and has been designated Pulse-Period Synchronization. Two controls on the PWGS enable the operator to vary the length of the time base from 3 μsec to 20,000 μsec in two ranges.

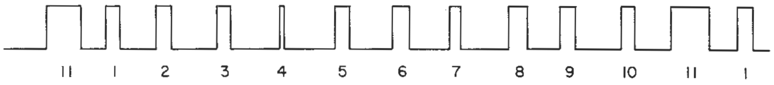


Fig. 4 - A ten-channel signal. The 11th pulse is the sync pulse

With a pulse pattern as shown in Fig. 5a, the operator can examine the signal in detail and will probably suspect the wide pulse appearing on the second (50 μsec) sweep as being the sync pulse. However, the fact that this pulse only appears on the second sweep makes accurate determination of its width difficult since it can be seen (Fig. 5a) that the suspected sync pulse is less than 5 μsec in width. If this pulse could be made to appear on the 5-μsec sweep the width could be measured to a much greater accuracy. This situation can be realized if the operator can shift the point of synchronization from the 3rd pulse to the 11th, so that the time base is initiated and the sync pulse is produced only with the arrival of the 11th pulse. Provision has been made to do exactly this. Once a stable pattern is obtained and a suspected sync pulse is located, the operator may shift the point of synchronization of the train one pulse at a time by simply pushing a button. If the button is pushed once, the pattern as shown in Fig. 5a is shifted to that shown in Fig. 5b with the sweeps synchronized with pulse 4. After seven additional actuations of the pushbutton, the pattern is shifted to one that is synchronized on the 11th or signal sync pulse, and this pulse now appears at the beginning of the 5-μsec sweep (Fig. 5c).

Noise may from time to time upset the synchronization scheme. This happens whenever a noise pulse of sufficient amplitude occurs between the termination of the time base and the arrival of the signal pulse that has been initiating the time base. This does not mean that the synchronization of the desired pulse is upset for more than one complete pulse train. Provided that the time base is set close enough to the pulse-train period, the desired pulse will ordinarily trigger the time base on the next trip around. If the noise is of opposite polarity from the signal pulse and has sufficient amplitude, its occurrence at the same time as the signal pulse may wipe out the signal pulse entirely. If signal pulse n is responsible for initiating the time base, synchronization will immediately jump to the (n+1)th signal pulse where it will remain until some further catastrophe occurs. However, if the signal is reasonably clean, the operator can keep the pattern synchronized by use of the pulse advance button.

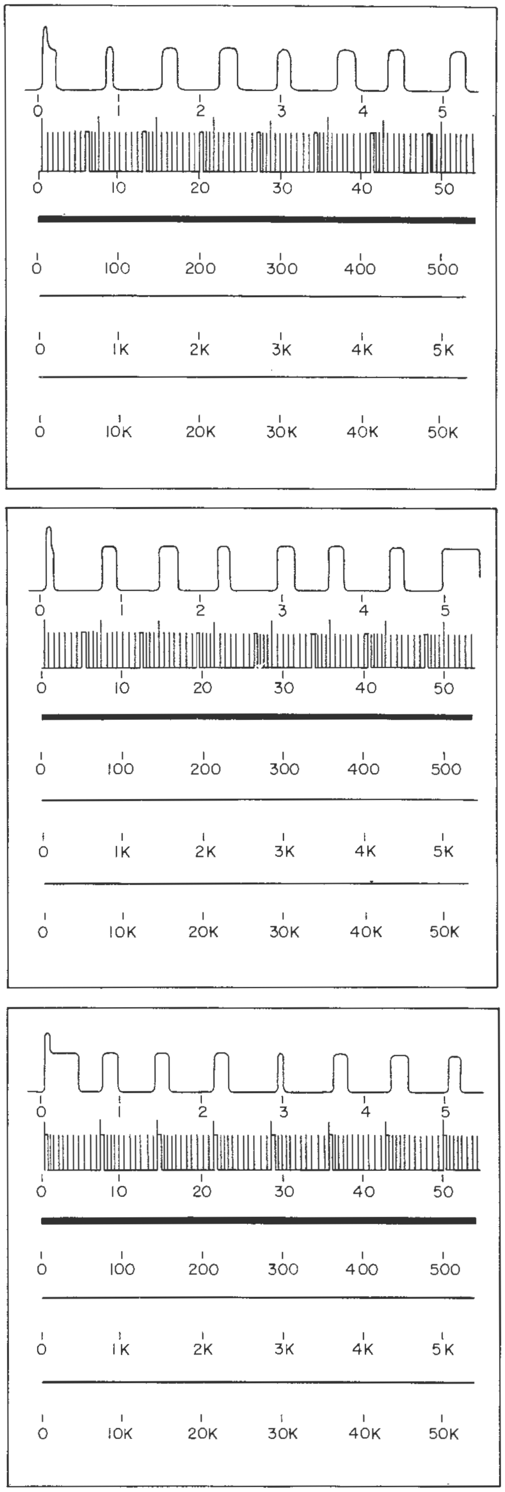
This method for examining a signal is good for any periodic signal regardless of the type of sync pulse used. Even if no pulse or group of pulses appears to have even a suggestion of any synchronizing properties, photographs of the stable pattern can be made and studied in more detail at the convenience of the operator.

[redacted]

[redacted]

DECLASSIFIED

UNCLASSIFIED



(a) Sweeps triggered on the number 3 pulse

(b) Sweeps triggered on the number 4 pulse

(c) Sweeps triggered on the 11th or sync pulse

Fig. 5 - The AN-SLA-2 analyzer display of a ten-channel signal

[redacted]

DECLASSIFIED

Once identification of a sync pulse is made, the operator can set up proper conditions in the PWGS for permanent synchronization on the particular type of sync pulse that has been identified. As mentioned before, the two types of sync systems that can be handled by this unit are wide pulses and grouped pulses. If a signal has been identified as a wide-sync-pulse type, the main SYNC SWITCH is then thrown from the PERIOD to the WIDTH position, and the WIDTH SYNC knob is advanced until the pattern on the analyzer restabilizes. If the knob has been advanced in the right direction, the signal is then automatically synchronized on the widest pulse. Further advancement of the WIDTH SYNC control produces artificial sync pulses from pulses other than the widest one, so that the pattern again becomes unstable. It is immediately obvious to the operator, therefore, when a signal is or is not properly synchronized. A properly synchronized signal of such description is shown in Fig. 6.

If upon examination of a signal it is suspected that the synchronization scheme is a group of two or of three pulses, then another procedure is used. A system of two delay lines is adjusted so that when and only when a pulse group having the proper interpulse spacing enters the pulse-group synchronizer circuit, a single output pulse of increased amplitude is obtained. Figure 7 is a block diagram of this circuit. The video signal is amplified and applied to the input of two delay lines, each having adjustable delay times from 0.025 to 20 μsec. The output of each line along with the undelayed signal is sent to an adding circuit which produces at its output the algebraic sum of the pulse signals. Figure 8a shows a three-pulse group as it leaves the amplifier along with the pulse group as it appears at the output of each delay line set to the desired delay times. If these three signals are applied to the adding circuit, a pulse three times the amplitude of a single pulse appears at the adding-circuit output at the time of occurrence of the undelayed pulse 3 (Fig. 8b). For the signal considered, there is no other time for which such addition occurs.

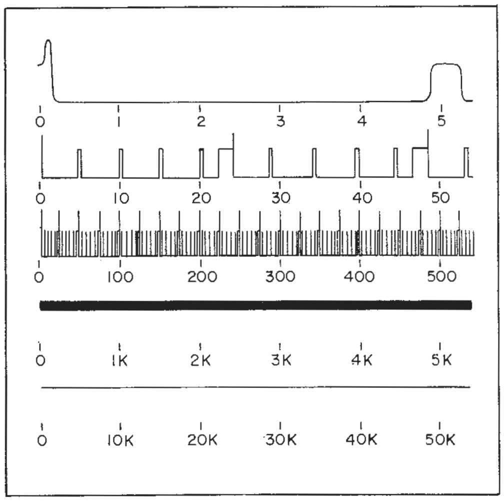


Fig. 6 - A multichannel signal properly synchronized on a wide pulse

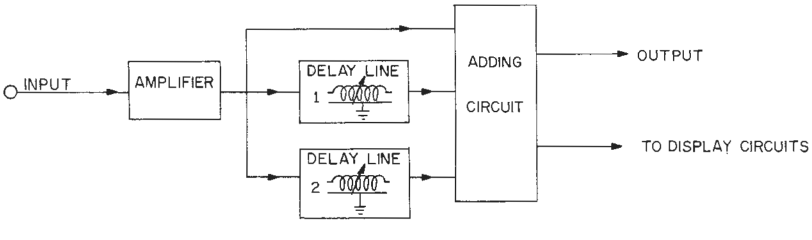
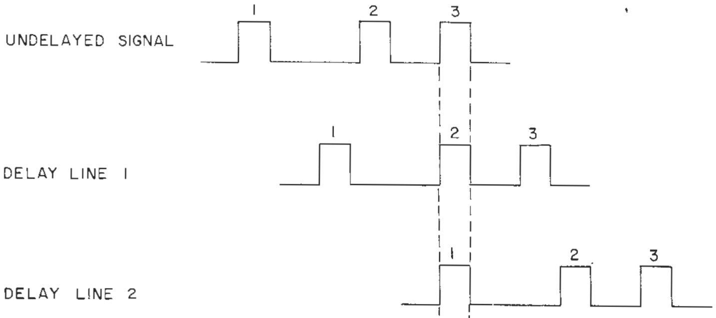
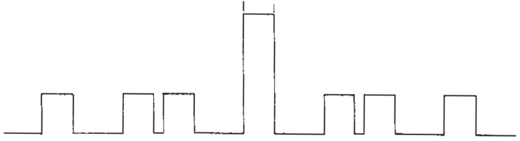


Fig. 7 - The basic diagram of the pulse-group synchronizing circuit in the PWGS

[redacted]



(A) ADDING CIRCUIT INPUTS



(B) ADDING CIRCUIT OUTPUT

Fig. 8 - The manner in which the pulse-group synchronizer produces a high-amplitude sync pulse from a three-pulse sync group

The CMPD Schmitt circuit, which follows the adding circuit, has its threshold level SYNC control adjusted so that no signals are passed unless they exceed the amplitude of at least a two-pulse coincidence. In this way a three-pulse coincidence will produce a sync signal in the CMPD, but a two-pulse one will not. If on the other hand a signal is suspected of having a two-pulse sync system, the pulse-group synchronizer may be used by simply setting the delay of one line equal to the pulse spacing. In this way an artificial three-pulse coincidence is produced, and the high-amplitude output pulse is coincident with the undelayed second pulse.

Visual aids have been incorporated to help in the proper setting of the delay lines. With the main SYNC SWITCH set in the PERIOD, DELAY LINE MONITOR position, and with the pulse pattern stabilized by properly setting the length of the time base, the output of the adding circuit is sent to a special connector on the CMPD chassis. (This connector and associated circuitry have been added to the CMPD since the publication of NRL Report 4574.) The signal at this connection is then added to the video signal in the display, so that the operator can visually adjust the delay lines to obtain coincidence of the pulses in the display. This method assures accurate adjustment of the delays because its success is independent of the calibration accuracy of the indicator display or the delay lines. Figure 9 shows an analyzer display of a signal when the delay lines are properly adjusted with the main SYNC SWITCH in the PERIOD, DELAY LINE MONITOR position. In this figure the first pulse of the three-pulse sync group has been selected to synchronize the analyzer. Three information pulses follow the sync group, and each information pulse appears in triplicate because of the adding circuit. The switch may now be turned to the DELAY LINE position for permanent synchronization of this signal (Fig. 10). Only the undelayed pulses and the added sync pulse will then appear in the display.

[redacted]

[redacted]

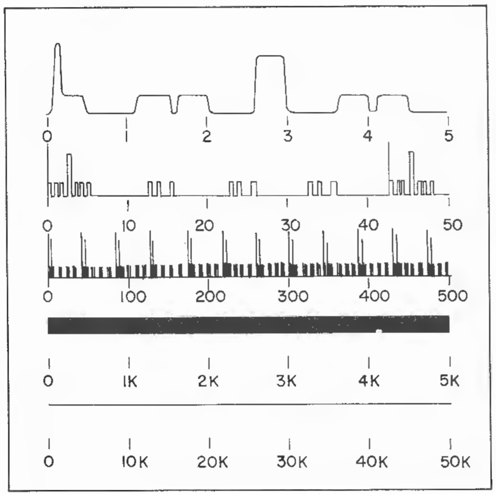


Fig. 9 - The proper visual adjustment of the delay lines for a three-pulse sync group

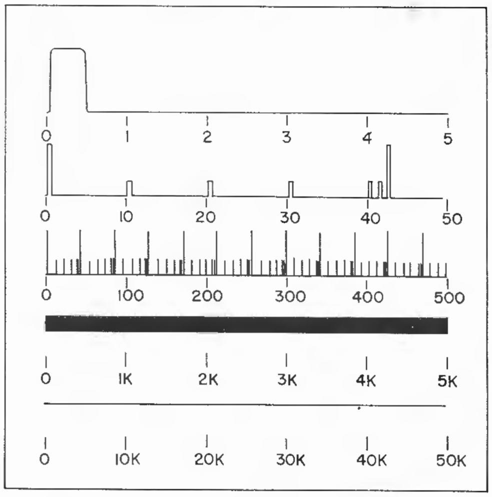


Fig. 10 - A three-channel signal properly synchronized on the three-pulse sync group

Figure 11 is a photograph of the front panel showing the positions of the various controls described above. The two delay lines are located at the bottom of the panel. Delays from 0.025 to 20 μsec in steps of 0.025 μsec can be selected by depressing the proper combination of pushbuttons. Although delay increments of 0.025 μsec may be selected, the minimum pulse spacing on which operation may be successfully performed is limited to 0.3 μsec because of rise times in the delay lines and multivibrators.

Fig. 11 - The front panel for the PWGS

[redacted]

[redacted]

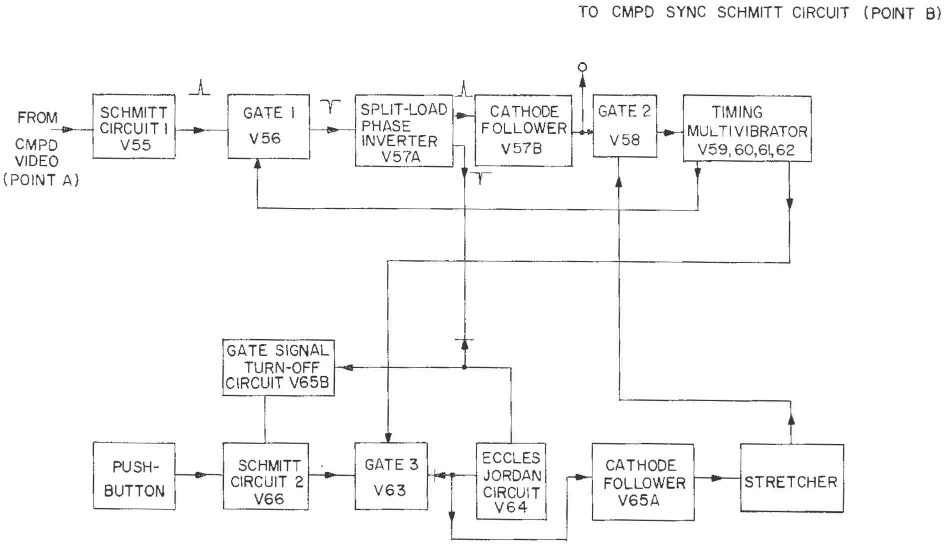


Fig. 12 - The basic diagram of the pulse-period synchronizer

CIRCUIT DETAILS

Pulse-Period Synchronizer

Figure 12 is a detailed block diagram of the pulse-period-synchronizing circuit. Pulses from the CMPD video amplifier are clipped by a Schmitt circuit and sent through a gate tube to a split-load phase inverter. The output of the phase inverter is sent via a cathode follower to a second gate circuit, the output of which triggers a high-duty-cycle one-shot multivibrator, the gate length of which is determined by the setting of the PERIOD switch and the PERIOD VERNIER control. This gate signal closes gate 1 and prevents pulses from passing beyond this point until the completion of the gating signal. If the length of the gating signal is set just short of the period of the incoming signal, the pulse that passes through gate 1 becomes the sync pulse that is sent to the CMPD sync Schmitt circuit.

If the above conditions are met, this sync pulse will always appear coincident with the nth pulse in an N-channel pulse train having a basic frame period slightly longer than the length of the multivibrator gate signal. If it is desired to shift the sync pulse from the nth pulse to the (n+1)th pulse, the PULSE ADVANCE button is actuated. This may be done any number of times with a resulting sync-pulse shift of one signal pulse each time the button is pushed. The block diagram of the circuit that accomplishes this occupies the lower portion of Fig. 12. When the pushbutton is actuated, Schmitt circuit 2 produces a step voltage which opens gate 3. The leading edge of the adjustable multivibrator gate is differentiated and allowed to pass through gate 3 to trigger an Eccles-Jordan circuit. The resulting commutation of this circuit serves two purposes. It turns off the Schmitt-circuit step signal which opened gate 3, and at the same time it closes gate 2 via a cathode follower and a pulse stretcher. (This pulse stretcher does not affect the shape of the signal that closes gate 2; it affects only the opening signal.) Gates 1, 2, and 3 are now closed. No video signals can trigger the adjustable multivibrator until gates 1 and 2 are opened. Gate 1, however, is opened as soon as the multivibrator terminates its gate, and

[redacted]

the first video signal pulse to pass through gate 1 (until now, this pulse has been the sync pulse) retriggers the Eccles-Jordan circuit to its original state. This would ordinarily reopen gate 2 and allow the signal pulse to trigger the multivibrator. However, the pulse stretcher delays the effective turn-on time of the gating signal for gate 2, so that this particular nth signal pulse is not allowed to retrigger the period-timing multivibrator. By the time the next signal pulse arrives, gate 2 has been opened so that the multivibrator is triggered this time by the (n+1)th pulse. Thus the sync pulse has been advanced by one signal pulse, or one channel.

At this point it might be asked how much the turn-on time of the gate 2 signal should be stretched, since pulse signals of various widths are to be treated with equal respect. The answer is that the pulse signals have been highly differentiated by the time they reach gate 2, so that all pulses are very short regardless of their original width, and only a very short stretch is needed.

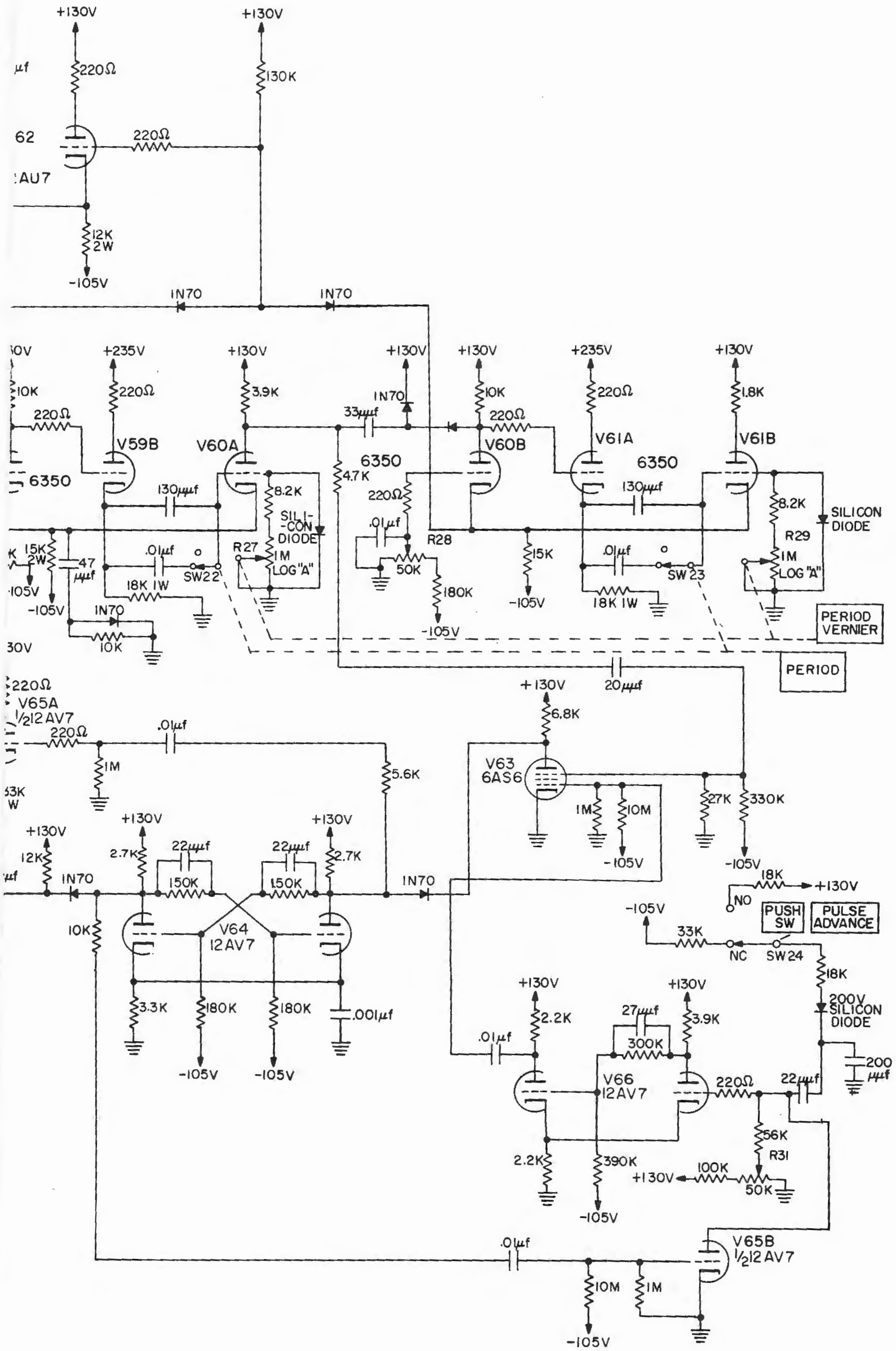
Figure 13 is a detailed schematic diagram of the pulse-period-synchronizing circuit. Schmitt circuit V55 slices all incoming signals to produce pulses of constant amplitude and slope. This signal is differentiated by the network which couples it to gating tube V56. The damped-ringing-circuit plate load of V56 followed by a short-time-constant coupling circuit serves to further differentiate the signal so that only very narrow pulses are applied to the grid of split-load phase inverter V57A. The positive-polarity output signal from the plate of V57A is sent via cathode follower V57B to the signal grid of gate tube V58 (gate 2), the plate load of which further differentiates the signal to trigger the period-timing multivibrator which utilizes tubes V59, V60, V61, and V62.

It should be remembered that it is the function of this multivibrator to produce a gate of length just short of a complete signal period. This necessitates duty cycles approaching 100 percent. Two multivibrators in tandem accomplish this task. Each is responsible for approximately one-half the total gate width, so that the maximum duty cycle for the individual multivibrators is only 50 percent. V59 and V60A compromise one multivibrator while V60B and V61 make up the second. Both multivibrators are designed for fast recovery to prevent gate width variations with change in duty cycle. Cathode followers V59B and V61A in conjunction with high-back-impedance clamping diodes are used for this purpose. The clamping diodes are Texas Instrument Company 620's that have been x-ray treated for fast recovery.* The two separate multivibrator gates are combined in a diode adding network and appear at the plate of cathode-coupled amplifier V62 as a single negative-polarity gate of length equal to the combined length of the individual multivibrator gates. This gate is coupled to the gating grid of V56 (gate 1) so that V56 is cut off throughout the length of the gating signal. Dual potentiometer R27 and R29 (PERIOD VERNIER) controls the length of the multivibrator gate. The PERIOD switch selects one of the two gate-length ranges, 3 to 250 μsec or 250 to 20,000 μsec.

When the PULSE ADVANCE button is depressed, a positive-polarity pulse is applied to the Schmitt-circuit-2 (V66) input grid. This produces a positive-polarity step at the Schmitt-circuit output which is coupled to the gating grid of V63 (gate 3). The differentiated leading edge of the first multivibrator gate can now trigger Eccles-Jordan circuit V64 which in turn dunks the input grid of V66 via dunking tube V65B. Thus the positive-polarity step at the V66 output is terminated, and V63 is cut off, thereby preventing additional pulses from passing through V63 to V64. However, when the Eccles-Jordan circuit is triggered by the one pulse allowed to pass through V63, V58 is cut off via cathode

---

*Future equipments should utilize fast-recovery silicon diodes which should soon be commercially available.


+130V
220Ω
62
AU7
220Ω
+130V
130K
12K 2W
-105V
IN70
IN70
+235V
220Ω
10K
220Ω
V59B
6350
+130V
3.9K
V60A
130μμf
8.2K
SILI-CON DIODE
R27
1M LOG "A"
SW22
.01μf
18K 1W
15K 2W
47 μμf
-105V
IN70
10K
+130V
IN70
33μμf
4.7K
6350
220Ω
.01μf
50K
R28
180K
-105V
+130V
10K
220Ω
V60B
+235V
220Ω
V61A
6350
130μμf
15K
-105V
.01μf
18K 1W
SW 23
+130V
1.8K
V61B
8.2K
SILICON DIODE
R29
1M LOG "A"
PERIOD VERNIER
PERIOD
20μμf
+130V
6.8K
V63 6AS6
1M
10M
-105V
27K
330K
-105V
220Ω
V65A ½12 AV7
220Ω
.01μf
1M
5.6K
+130V
12K
IN70
10K
+130V
2.7K
22μμf
150K
22μμf
150K
+130V
2.7K
V64 12AV7
IN70
3.3K
180K
180K
.001μf
-105V
-105V
18K
+130V
NO
PUSH SW
PULSE ADVANCE
-105V
33K
NC
SW24
18K
200V SILICON DIODE
+130V
2.2K
27μμf
300K
+130V
3.9K
.01μf
V66 12AV7
220Ω
22μμf
200 μμf
56K
R31
2.2K
390K
100K
+130V
50K
-105V
.01μf
V65B ½12 AV7
10M
1M
-105V

[redacted]

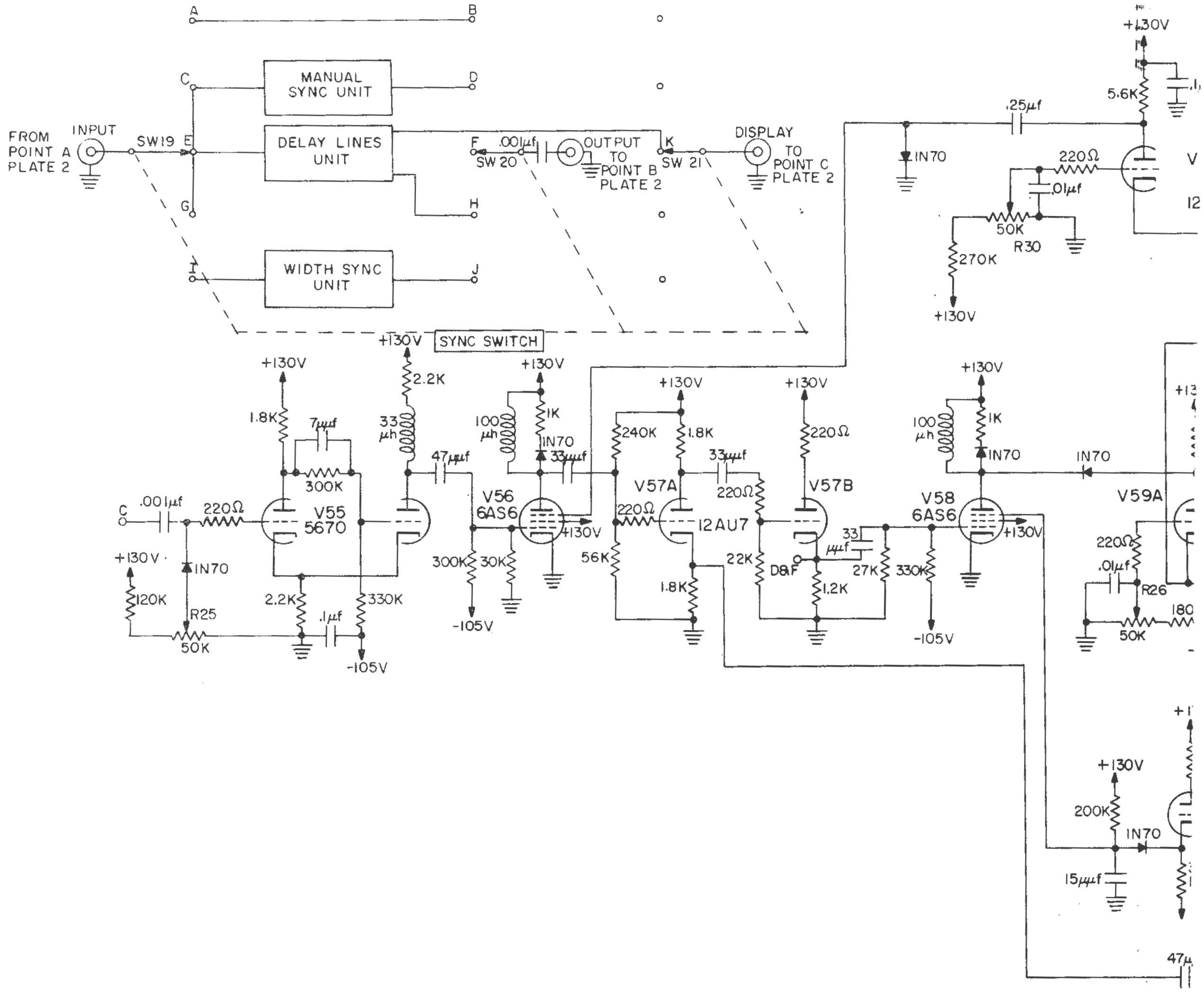


Fig. 13 - Schematic diagram of the pulse-period synchronizer

[redacted]

[redacted]

follower V65A. As soon as the multivibrator timing gate is terminated, the first synchronizing pulse that passes through V56 resets the Eccles-Jordan circuit, which terminates the negative-polarity gate on the gating grid of V58. This gate, however, is not terminated in time to let the sync pulse through to trigger the multivibrator. A stretching circuit connected to cathode follower V65A returns the V58 gating grid voltage to ground level in approximately 1/3 μsec. Thus the first pulse following the sync pulse is allowed to pass through V58 to trigger the timing multivibrator, and this pulse thereby becomes the new sync pulse.

Pulse-Group Synchronizer

Figure 14 is a schematic diagram of the Pulse-Group Synchronizer, which produces a sync pulse from a group of two or three specifically spaced pulses each time that particular group appears (Fig. 7). The high-current amplifier V67 is used to drive the two 1000-ohm delay lines. This high-powered driver was necessary to make up for the high attenuation of narrow pulses as they pass down the lines. All pulses are clipped in a unique adding circuit consisting of three modified cathode followers V68A, V68B, and V69A having a common plate-load resistor. The high-amplitude signals from the delay lines and amplifier drive the cathode-follower grids negative. The cathodes which are normally biased at about +135 volts follow the grids negative until the cathode crystals begin conduction at about +130 volts. The grids continue their negative excursion, but V68A, V68B, and V69A have become amplifiers since the cathodes are no longer free to move. The amplified signals appear at the common plate terminal across the 830-ohm load. Further negative excursion on the part of the grids simply cuts off the amplifiers, thereby slicing all pulses to the same amplitude provided they emerge from the delay lines with sufficient amplitude to cut off the adding-circuit tubes. If the delay lines are properly set, a synchronizing pulse of amplitude three times that of the other pulses will appear across the common plate-load resistor. This signal is fed via cathode follower V69B to the CMPD sync Schmitt circuit.

A third position PERIOD, DELAY LINE MONITOR of the main SYNC SWITCH allows the operator to adjust the delay lines to fit a certain pulse group by viewing the pulse pattern on the analyzer screen. A small portion of the V69B cathode follower output signal is sent via terminal K to a special jack installed on the main CMPD chassis. This jack is connected to the display circuitry, so that the actual output of the delay-line adding circuit may be viewed superimposed on the analyzer video display. After coincidence of pulses has been obtained, the main SYNC SWITCH may be set to the DELAY LINE position which establishes sync from the output of the delay line adding circuit.

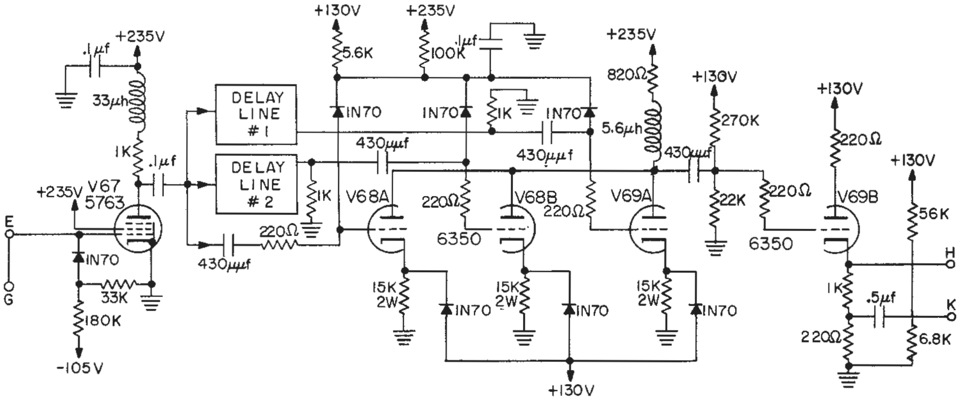


Fig. 14 - Schematic diagram of the pulse-group synchronizer

[redacted]

[redacted]

Pulse-Width Synchronizer

Figures 15 and 16 are block and schematic diagrams of the pulse-width synchronizer. Schmitt circuit V70 clips incoming pulses so that all signals entering inverter V71A will be of constant amplitude and slope. The negative-polarity square pulse from the inverter cuts off the grid of V71B which normally holds the tube in conduction. A constant-current generator in the V71B plate circuit produces a sawtooth waveform which is initiated at the beginning of the pulse and terminated at the end. The amplitude of the sawtooth is thus directly proportional to the width of the incoming pulse. The amplitude is also directly proportional to the available current from the constant-current generator. This current is controlled by R33 (Fig. 16) which is the WIDTH SYNC control on the front panel (Fig. 11). The sawtooth waveform is coupled to the number 1 grid of V72.

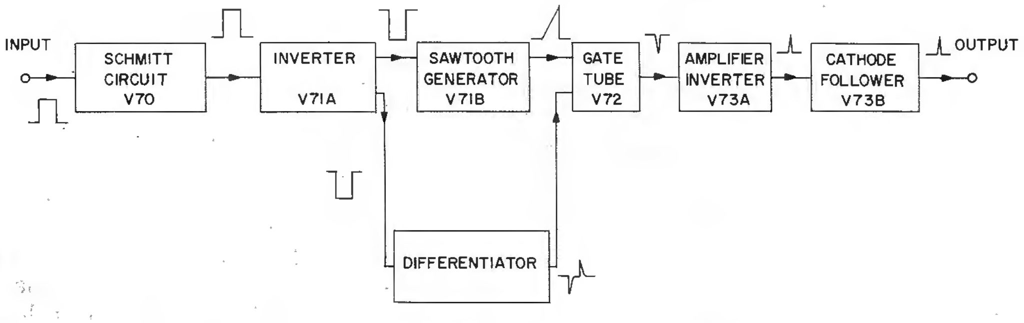


Fig. 15 - The basic diagram of the pulse-width synchronizer

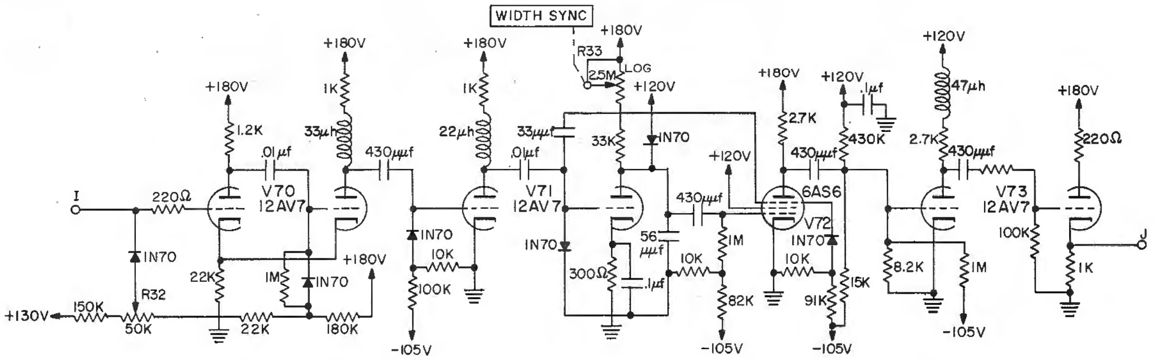


Fig. 16 - Schematic diagram of the pulse-width synchronizer

[redacted]

The input pulse to the sawtooth generator is differentiated and applied to the number 3 grid of V72. Both grids are biased to cut off in the absence of signal. However, if the sawtooth waveform is of sufficient amplitude to overcome the negative bias on the V72 number 1 grid, then the differentiated trailing edge of the input signal to the differentiator is allowed to pass through to the inverter amplifier V73A and on to output cathode follower V73B. Proper adjustment of R33 determines the minimum pulse width required to produce a sawtooth waveform of sufficient amplitude to turn on V72. Shorter pulses will produce no output. The sync pulse produced by this circuit is coincident with the trailing edge of the incoming pulse, which explains the nature of the particular pulse pattern shown in Fig. 6.

Switching and Interconnections

The PWGS essentially replaces the jumper which previously connected points A and B, the output of the CMPD video amplifier (V4, plate 2) and the input of sync Schmitt circuit (V5, plate 2). The output of the CMPD video amplifier is connected to the INPUT of the PWGS, and the OUTPUT of the PWGS is connected to the CMPD sync Schmitt circuit. These connecting jacks already exist on the CMPD chassis. A third jack has been added to the CMPD chassis in order that the delay-line adjustments can be made visually. Figure 17 shows the slight circuit modifications that have been made in the CMPD to accommodate this feature. A 1500-ohm resistor has been added between the cathode of V25 and the grid of V26. A crystal diode with ground return has been installed between the new jack and the V26 grid.

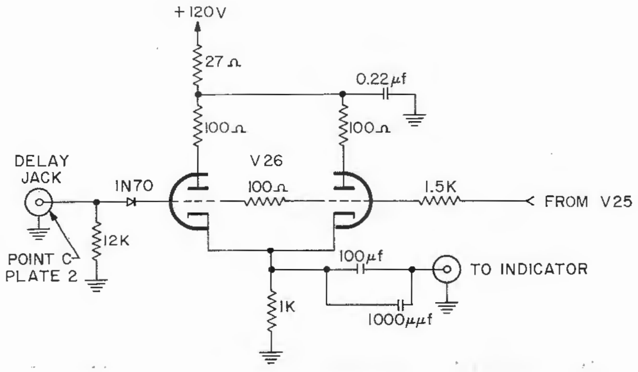


Fig. 17 - Circuit modifications in the CMPD

The main SYNC SWITCH (SW19, SW20, and SW21) connects the various sync units between the INPUT and OUTPUT jacks. It also connects a portion of the output of the delay line adding circuit to the display jack when the switch is in the PERIOD, DELAY LINE MONITOR position. In all other positions the 12,000-ohm ground-return resistor in the CMPD V26 grid allows the CMPD display circuits to operate in their normal manner.

Complete circuit schematics of the PWGS and the CMPD are Plates 1 and 2 of this report. Appendix A lists all changes made since publication of NRL Report 4574.

Power Supply

A regulated power supply to provide +235 and +130 volts is diagrammed in Fig. 18. An eight wire cable connects it to the PWGS chassis, and a six-wire cable connects it to the CMPD main-power-supply chassis. The six connections inside the main power supply are made to ground, to -105, +120, and +180 volts, and to the two 110-volt leads to the main switch. The relay in the PWGS power supply delays the application of positive voltages to the circuits until the -105-volt supply has come on.

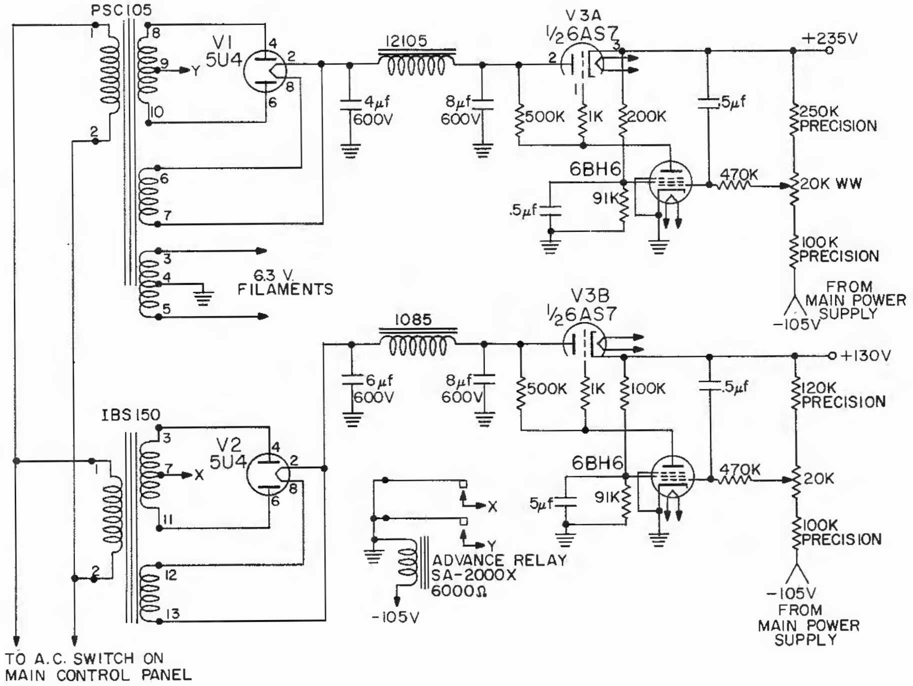


Fig. 18 - The power supply

ADJUSTMENT

With the PWGS properly installed and connected in the CMPD rack, the main SYNC SWITCH is set to the PERIOD position. A signal with pulses 1 µsec wide and a repetition rate of 100 kc is connected to the input of the CMPD, and the CMPD gain is set according to the instructions given in NRL Report 4463. Then R25 in the grid of Schmitt circuit V55 is set to properly slice the incoming pulse. The generator pulse-repetition rate is now dropped to 2 kc, the PERIOD switch is set to the 3-to-250 µsec position, and the PERIOD VERNIER is set to maximum. The threshold controls R26 and R28 are set so the gate produced by each multivibrator is approximately 135 µsec. Then R30 (V62) is set so that a clean negative gate of width equal to the sum of both multivibrator gates is obtained at the 3rd grid of V56. A narrow spike indicating the termination of the first multivibrator gate may appear in the center of the gate. This is normal and is of no consequence as long as the spike amplitude remains less than half the gate amplitude. Now with no signal applied, R31 is adjusted so that the input grid of V66 rests at a potential about halfway between the two threshold voltages. This may be done by connecting a voltmeter across the 2200-ohm output-plate load resistor (V66) and rotating R31, noting the approximate settings for plate current commutation.

The period synchronizing circuit is now ready for operation, and incoming periodic signals which cannot be stopped on the analyzer display screen may be synchronized by slowly adjusting the PERIOD VERNIER control until the pattern stabilizes itself. The SYNC control on the CMPD may require adjustment in order to accept the sync pulse produced by the PWGS.

Next the main SYNC SWITCH is set to the WIDTH sync position, and with the signal generator set for a 100-kc, 1-μsec signal, R32 is adjusted for best slicing of the signal as it appears at the V70 Schmitt-circuit output plate. Synchronization pulses can now be obtained from pulses of any width from 1/2 to 30 μsec by proper adjustment of the WIDTH SYNC control, R33.

RECOMMENDATIONS AND CONCLUSIONS

It is felt that there are still a number of circuit refinements that might well be affected in order to simplify the PWGS and better integrate it with the CMPD proper.

1. Improved layout of the PWGS chassis could result in eliminating the V70 Schmitt circuit with V55 serving both the period and the width synchronizing circuits.

2. The dual period-timing multivibrator, V59, V60, V61, and V62, was necessitated by the high-duty-cycle requirements. The high logarithmic resistance required for the R27 and R29 potentiometers cannot be met in anything but a rather unstable dual carbon control. At present an elaborate ball-bearing device is used to eliminate the undesirable backlash inherently present in such potentiometers. The division of the 3- to 20,000-μsec multivibrator range into 4 ranges would enable the use of lower resistance linear potentiometers.

3. Further simplification might be accomplished by making only one multivibrator continuously adjustable. The first fixed multivibrator would not be varied over any given range but would have its gate width switched between ranges. Thus only one vernier potentiometer would be required.

4. Direct coupling of the PWGS output to the CMPD sync Schmitt circuit V1 would eliminate the need for adjustment of the SYNC control on the CMPD for all types of synchronization with the exception of amplitude synchronization.

The fact that time has prevented the execution of the above recommendations in no way limits the immediate usefulness or reliability of the equipment as it now stands. It is, therefore, strongly recommended that the Pulse-Width and Pulse-Group Synchronizer be permanently incorporated into all Complex-Modulated-Pulse Demodulators now in existence. Any consideration given to production of CMPD equipment should include the PWGS as an essential component part.

DECLASSIFIED

[redacted]

APPENDIX A

Changes Made in the CMPD Circuit Since the Publication of NRL Report 4574*

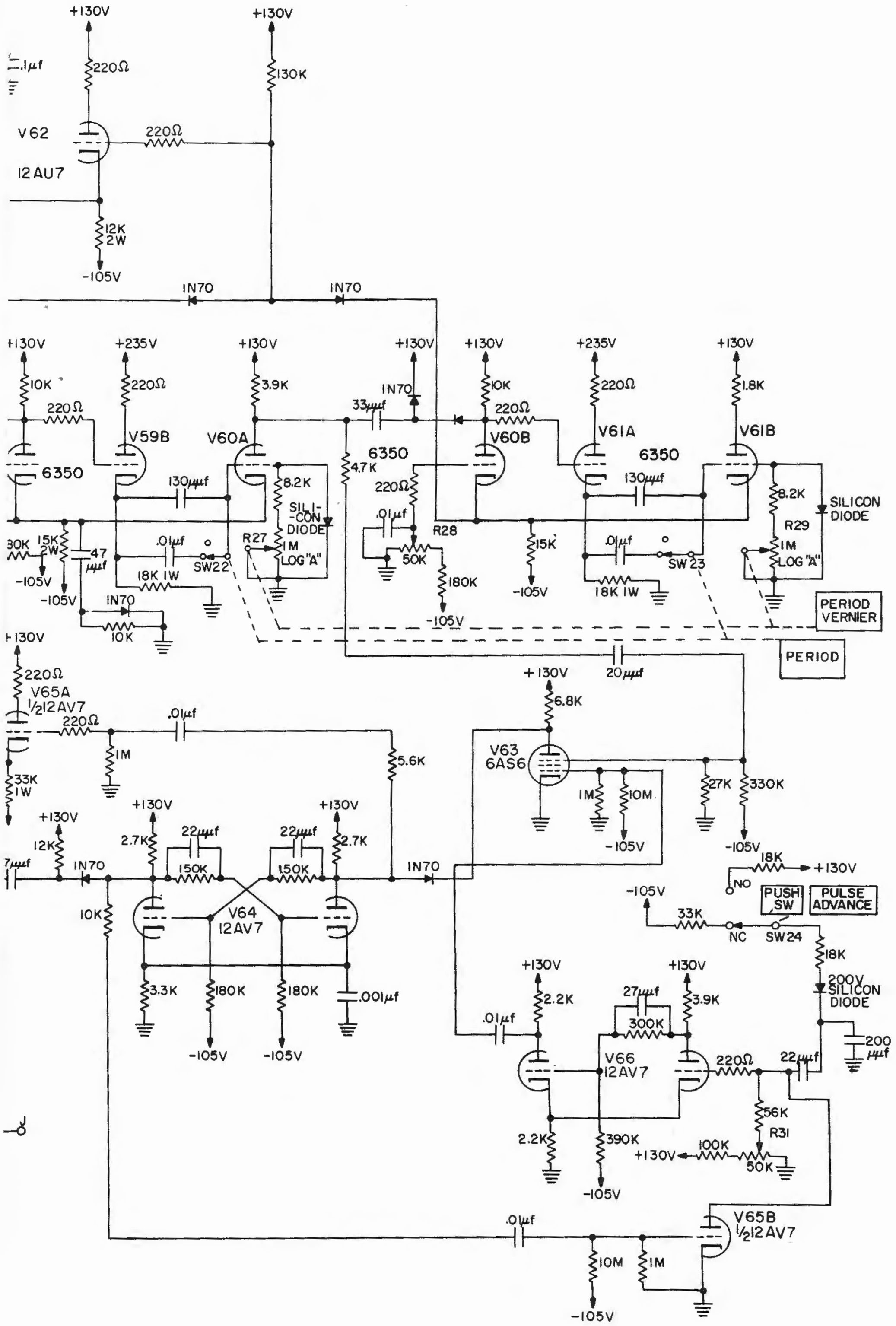
1. The inductors in the V1 and V3 plate circuits have been changed from 56 µh to 68 µh.
2. The R2 bias resistors (V5) have been changed from 91 and 200 kilohms to 68 and 130 kilohms.
3. The V7 and V10 timing capacitors have new values of 47 µµf, 910 µµf, and 0.02 µf.
4. The R4 and R7 resistors (V7 and V10) are returned to ground rather than to +120 volts.
5. The grid resistors in V7B and V10B have been changed from 22 kilohms to 5.6 kilohms.
6. The R13 bias resistors (V19) have been changed from 8.2 and 100 kilohms to 4.7 and 68 kilohms.
7. The R14 bias resistors (V19) have been changed from 27 and 100 kilohms to 18 and 68 kilohms.
8. The R16 bias resistors (V19) have been changed from 33 and 100 kilohms to 22 and 68 kilohms.
9. The R18 bias resistors (V21) have been changed from 22 and 68 kilohms to 10 and 120 kilohms.
10. The V24A cathode resistor has been changed from 300 ohms to 560 ohms.
11. The V20 compensating capacitors have been changed from 5 µµf to 10 µµf.
12. The V18B grid resistor has been changed from 68 kilohms to 30 kilohms.
13. The V32A plate resistor has been changed from 2.7 kilohms to 2.2 kilohms.
14. The cathode of V45B has been bypassed to ground by 0.01 µf.
15. The V47B bias resistor has been changed from 12 kilohms to 8.2 kilohms.
16. The V26B grid resistor has been changed from 56 ohms to 1.5 kilohms.
17. A 12-kilohms resistor and a 1N70 diode have been installed in the V26A grid circuit to provide coupling between jack C and V26.
18. Jacks A and B have been installed in the V4A cathode output line.

---

*Holmes, J. C., "Circuit Modifications for the Complex-Modulated-Pulse Demodulator," NRL Report 4574 ([redacted] report, Unclassified title), August 1955

[redacted]

DECLASSIFIED


+130V
220Ω
130K
.1μf
V62
12AU7
12K 2W
-105V
IN70
+235V
10K
220Ω
3.9K
IN70
33μμf
6350
V59B
V60A
V60B
V61A
V61B
1.8K
4.7K
8.2K
130μμf
SILI-CON DIODE
R27
1M LOG "A"
SW22
.01μf
18K 1W
15K 2W
47 μμf
50K
R28
180K
15K
SW23
R29
SILICON DIODE
PERIOD VERNIER
PERIOD
20μμf
V65A
½12AV7
.01μf
5.6K
1M
33K 1W
6.8K
V63
6AS6
1M
10M
27K
330K
12K
2.7K
22μμf
150K
V64
12AV7
3.3K
180K
.001μf
NO
NC
SW24
PUSH SW
PULSE ADVANCE
33K
18K
200V SILICON DIODE
200 μμf
2.2K
27μμf
300K
V66
12AV7
22μμf
56K
R31
100K
50K
390K
V65B
½12AV7
10M

[redacted]

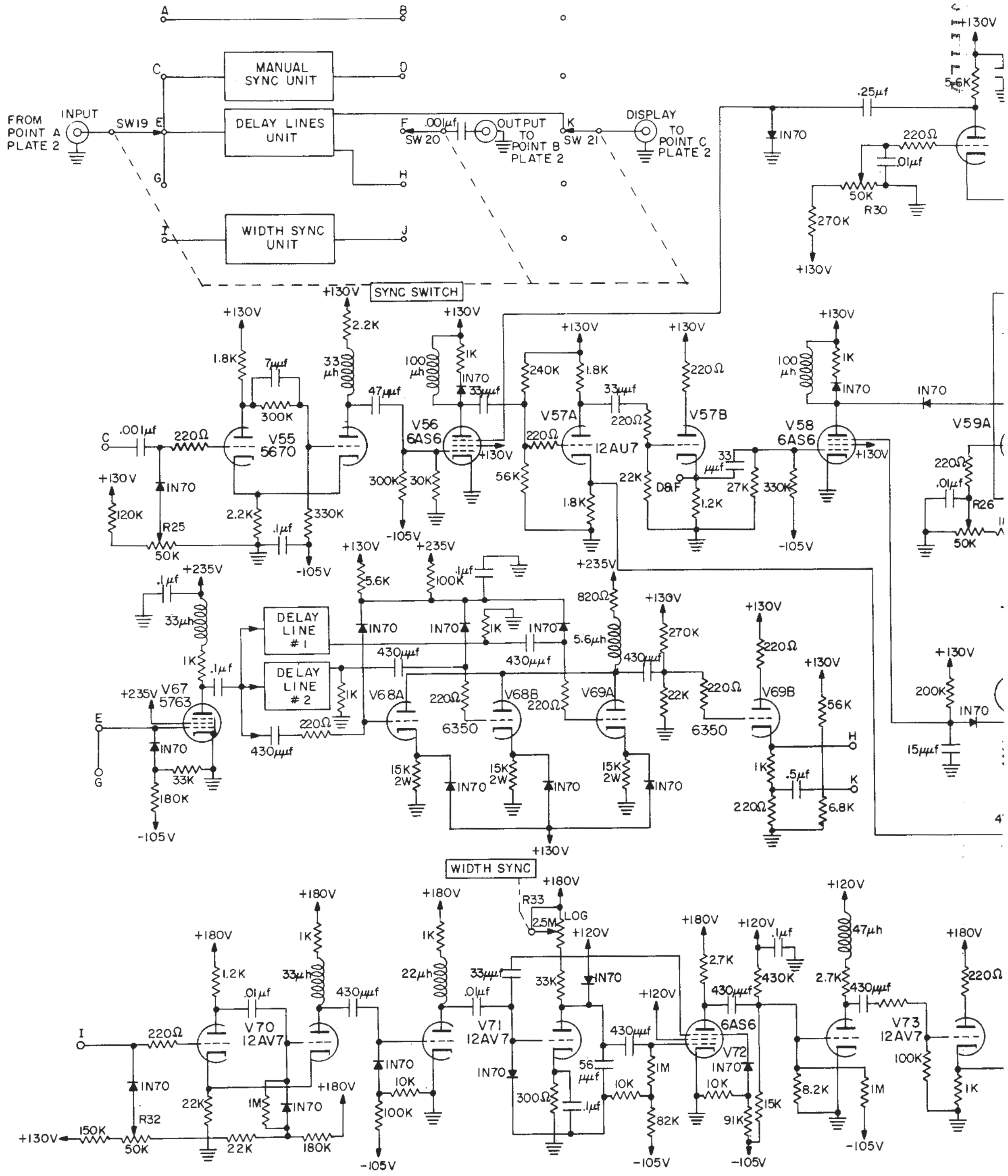
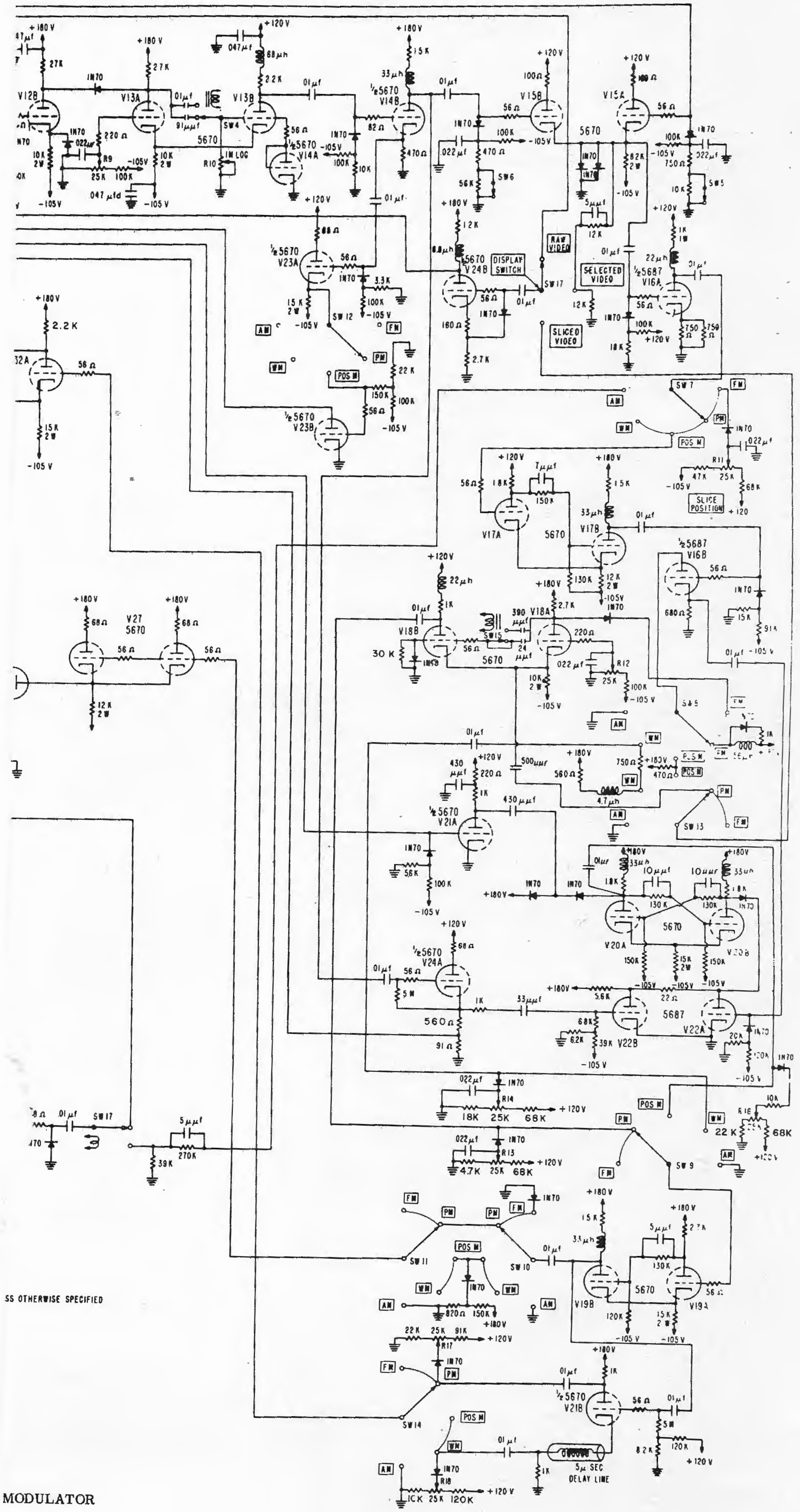


PLATE I

DECLASSIFIED

[redacted]



SS OTHERWISE SPECIFIED

MODULATOR

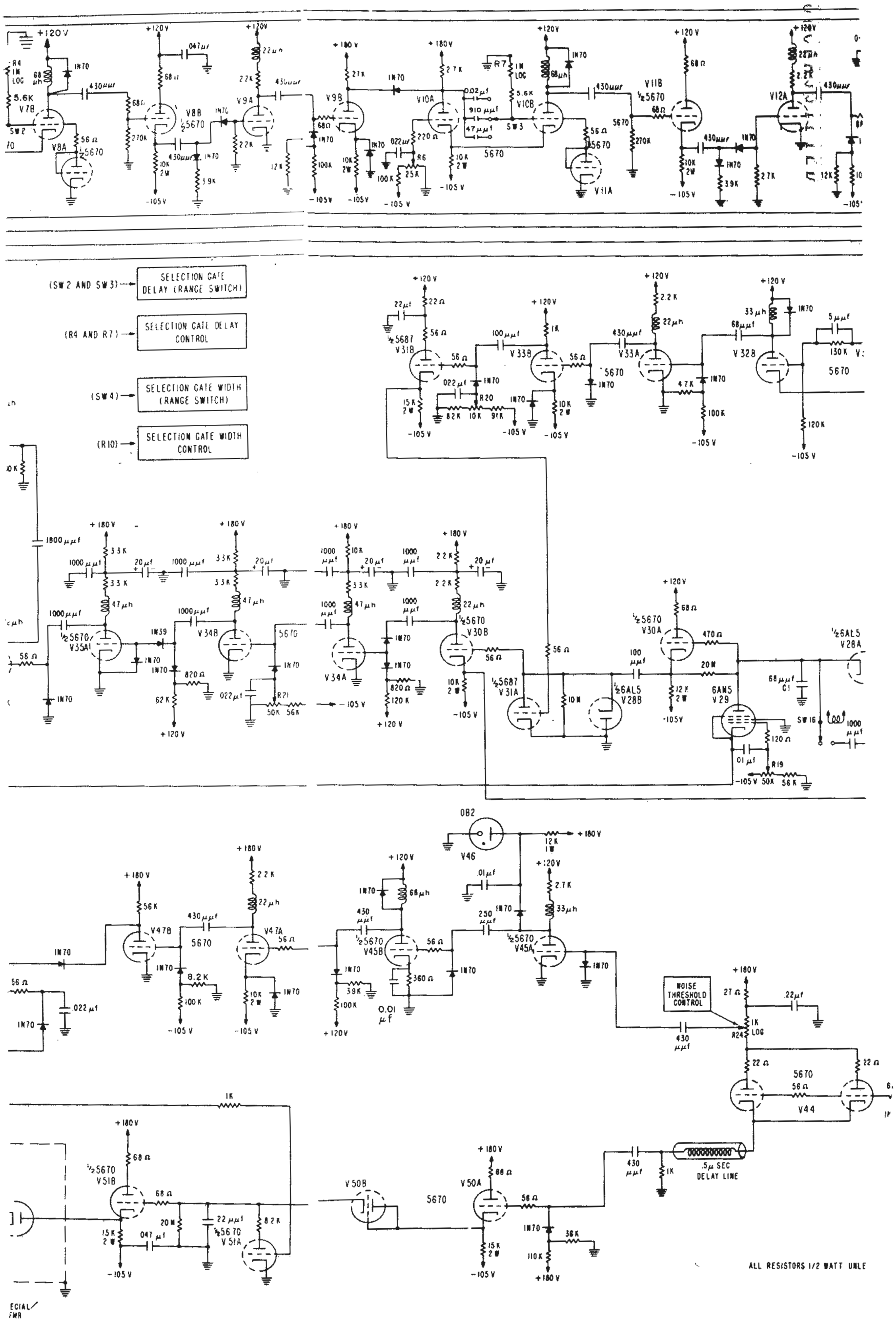
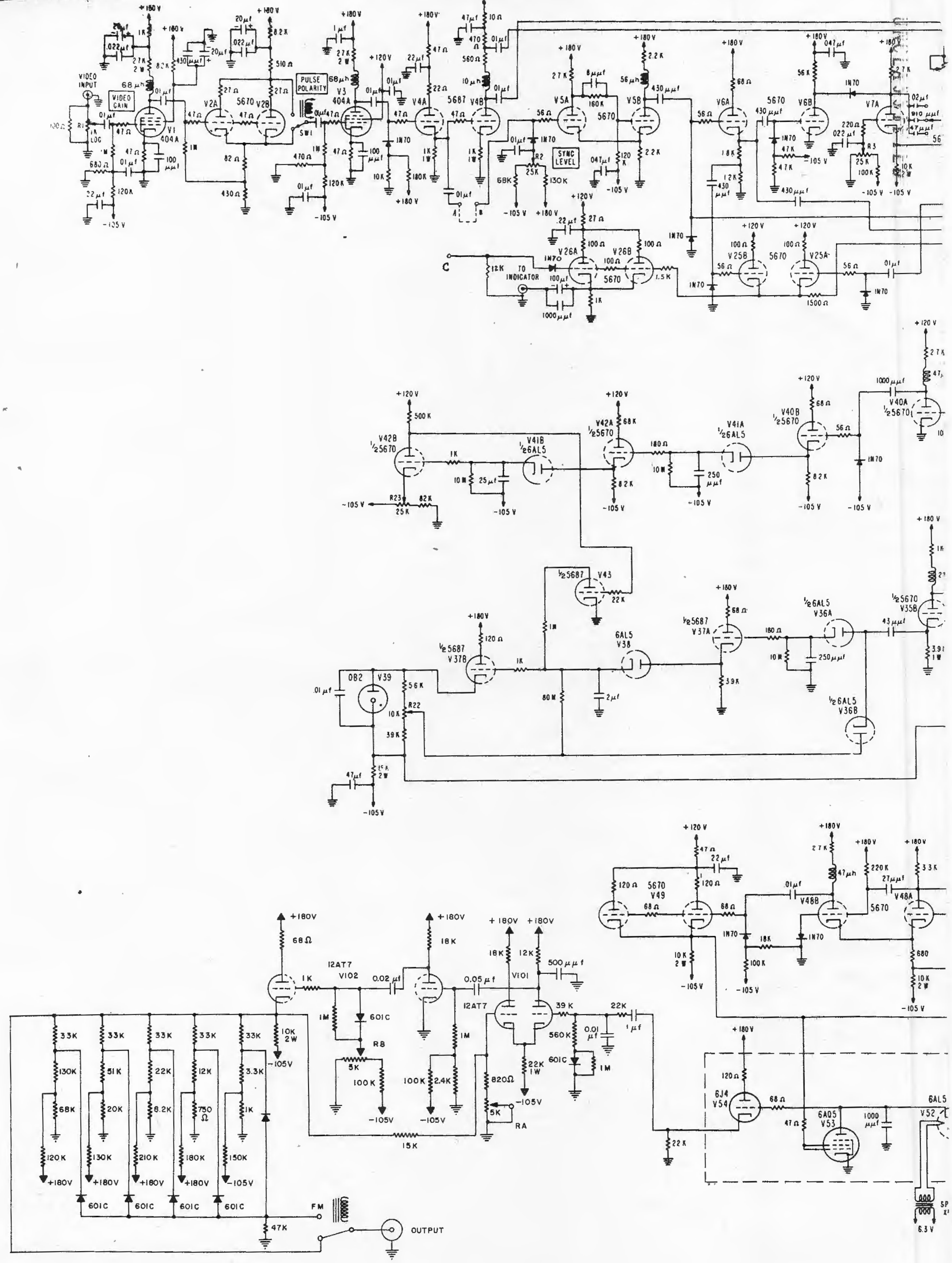


PLATE II - SCHEMATIC DIAGRAM OF COMPLEX-MODULATED-PULSE DE

[redacted]

DECLASSIFIED



[redacted]

DECLASSIFIED

NAVY-DPPO PRNC. WASH., D.C.