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# A COUNTERCEPT SYSTEM SIMULATOR

[UNCLASSIFIED TITLE]

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**ABSTRACT**  
[Unclassified]

In order to best utilize a previously reported time-series analyzer in the computation of countercept probability (the time-dependent probability of asynchronous countermeasures interception) a system simulator has been developed. This device simulates in real or scaled time the output of any given intercept receiver working against any given transmitter. The simulator takes into account all significant parameters — antenna patterns and rotation rates, transmitter power, receiver sensitivity, receiver bandwidth, receiver scan band and scanning rate, the position of the signal frequency in the receiver scan band, the nature of the transmitted signal (e. g., pulse width and pulse repetition frequency), the nature of the indicator and its coupling to the operator or other decision element (e. g., the minimum number of pulses required for the recognition of a pulsed signal or the minimum duration of signal recognizable as a communication), the statistical variation of receiver threshold introduced by the presence of a human operator, and the attenuation introduced by the propagation path (i. e., the effects of range and elevation).

The simulator has been completed and has been used in conjunction with the analyzer to solve one problem in receiver system design. It is hoped that the problem-solving program can be greatly expanded and that the computational facility can be made accessible to other activities.

**PROBLEM STATUS**

This is an interim report; work on the problem is continuing.

**AUTHORIZATION**

NRL Problem R06-07  
Project NR 417-000 and NR 417-002

Manuscript submitted May 17, 1957

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A COUNTERCEPT SYSTEM SIMULATOR  
[Unclassified Title]

GENERAL DESCRIPTION

The time-series analysis method of computing counterception\* probability described in a previous report† requires a source of simulated intercepts representing operating experience that would be obtained with a given transmitter, transmitting antenna, propagation path, receiving antenna, and receiver system. Although it would be possible to analyze the output of an actual transmitter-receiver combination, the analysis would be limited to existing systems and would likely require excessive time for completion. Thus, in order to take full advantage of the system, a high-speed electronic simulator was developed that is capable of reproducing the outputs of a wide range of possible transmitter-receiver combinations in a compressed time scale.

The parameters that determine whether or not a transmitted signal is detected by the receiving system may be divided into three categories — amplitude, time, and numerical requirements. The requirements are somewhat interrelated. For example, the amplitude requirements may be stated as follows: For interception to be possible the input power to the receiver must be greater than the detection threshold of the receiver where the former is determined by the transmitter power, the antenna gains and elevations, and the transmission paths. The antenna gains are, however, a function of time if the antennas are rotating. It is therefore possible that the amplitude requirement will be satisfied only intermittently. The simulator contains circuitry which produces an output whenever the amplitude conditions are satisfied. This will be generally referred to as the amplitude gate.

In order for interception to occur, not only must the amplitude requirements be satisfied, but there must also be a time coincidence of other conditions. The receiver must be tuned to the signal frequency, and the transmitter, if it is operating noncontinuously, must be radiating. Whenever the receiver is tuned to the signal frequency and the amplitude gate is also present, sufficient power is being delivered to the receiver to cause an output provided that the transmitter is actually radiating. The output of circuitry that is activated at the coincidence of the receiver tuning and amplitude conditions is called the "receiver + amplitude" or R+A gate.

The presence of the R+A gate in many cases fulfills the necessary conditions for an intercept. In some cases, however, other conditions must be considered. If the transmitter is operating noncontinuously, the transmitter modulation envelope must be simulated and must itself modulate the R+A gate. The output of this mixing process simulates above-threshold signals in the hypothetical receiver.

Two numerical requirements may also have to be imposed. If the transmitter is pulsing, a certain minimum number of pulses may have to be received before the intercept is recognized. Counting circuits in the simulator determine whether or not this condition is satisfied. Other receiving systems may require a certain minimum duration of intercept for recognition. Since the intercept is quantized in time and counted in order to determine its duration this is considered to be a numerical requirement. Figure 1 is a simplified block diagram of the simulator.

\*Defined as asynchronous countermeasures interception

†Wald, B., "Computation of the Probability of Countermeasures Interception," [U]  
NRL Report 4612 (Confidential) 5 October 1955

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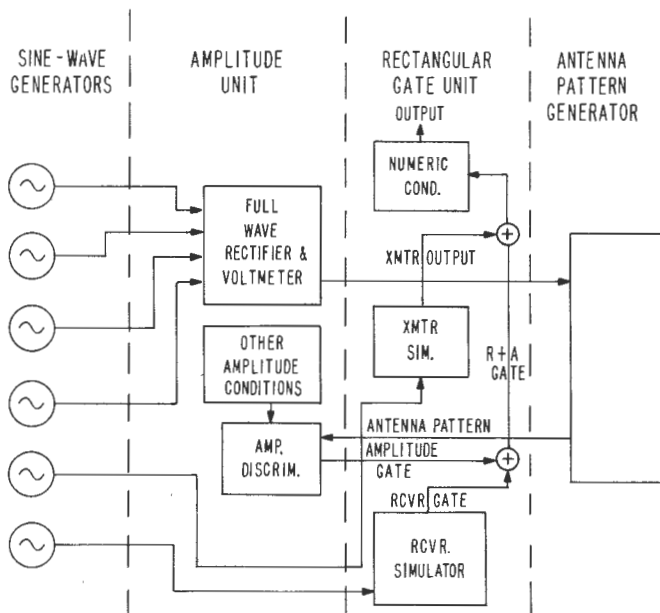


Fig. 1 - Simulator block diagram

Figure 2 is a photograph of the simulator. The lowest of the four front-panel units is the Antenna Pattern Generator. Above it is the Rectangular Gate Unit which simulates the time and numerical conditions, and combines these with the amplitude gate to produce the simulator output. The next unit up is the Amplitude Unit which feeds to the Antenna Pattern Generator the proper waveforms for the synthesis of antenna patterns, and receives from this generator simulated antenna patterns which it combines with the other amplitude conditions to produce the amplitude gate. The highest unit is a rack which contains six audio oscillators each of which can generate a frequency between 2 cps and 2 Mc. Frequencies above 20 kc are not generally used. Four of these frequencies are employed in the simulation of antenna patterns; the other two are connected to the Rectangular Gate Unit and are used to simulate the effect of receiver scanning and pulse repetition frequency.

#### DETAILED DESCRIPTION

In the circuit diagrams to follow, component numbers below 1000 refer to power supplies, numbers from 1001-1999 to the Antenna Pattern Generator, numbers from 2001-2999 to the Rectangular Gate Unit, and numbers from 3001-3999 to the Amplitude Unit. The following components are numbered: V- tubes; X- crystal diodes; R- potentiometers; C- decimal counters; and A- operational amplifiers. Table 1 lists the characteristics of the decimal counters and Table 2 the characteristics of the operational amplifiers employed in the simulator.

#### Power Supply

Figure 3, photographed through the back of the simulator cabinet, shows the Power Supply components, which are mounted on a hinged rack panel. Six commercially built



Fig. 2 - The countercept system simulator

power supplies are used to supply all but two of the dc voltages and part of the heater current. The two remaining voltages are supplied by the superregulator. Figure 4 is the circuit diagram of the power supply interconnection and the superregulator. Control is provided by the power supply of the digital analyzer.

TABLE 1  
Characteristics of Preset Decimal Counting Units

|            | Berkeley Model 732*                              | LFE Model 1723                   |
|------------|--|----------------------------------|
| Power      | 6.3 v at 3 a<br>300 v at 18 ma<br>-150 v at 1 ma | 6.3 v at 1.8 a<br>300 v at 15 ma |
| Max Speed  | 40 kc †  | 100 kc                           |
| Input Req. | -90 v for 2 μsec                                 | -90 v for 3 μsec                 |
| Reset Req. | 70 v for 15 μsec                                 | -70 v for 15 μsec                |

\*The 732 has two preset outputs; the 1723, one. At the preset count, the conductance to ground on the preset output bus falls to zero.

†The 732 will count to 100 kc but the preset outputs will ordinarily not be usable above 40 kc.

TABLE 2  
Characteristics of Philbrick Operational Amplifiers

|                | K2-W   | K2-X  | K2-P                                |
|----------------|--|---|-------------------------------------|
| Power          | 6.3 v at 0.6 a<br>+300 v at 4.5 ma<br>-300 v at 4.5 ma | 6.3 v at 0.75 a<br>+300 v at 7.5 ma<br>-300 v at 5.2 ma | 6.3 v at 0.45 a<br>+300 v at 2.4 ma |
| Gain           | 15,000   | 30,000  | 1,000                               |
| Rise Time      | 2 μsec   | 1 μsec  | 48 sec                              |
| Nominal Offset | 1.5 v  | 0.7 v   | 0                                   |
| Offset Stab.   | 10 mv  | 10 mv   | 10-100 μv                           |
| Output Max     | ±50 v at 1 ma  | ±100 v at 2 ma  | --                                  |

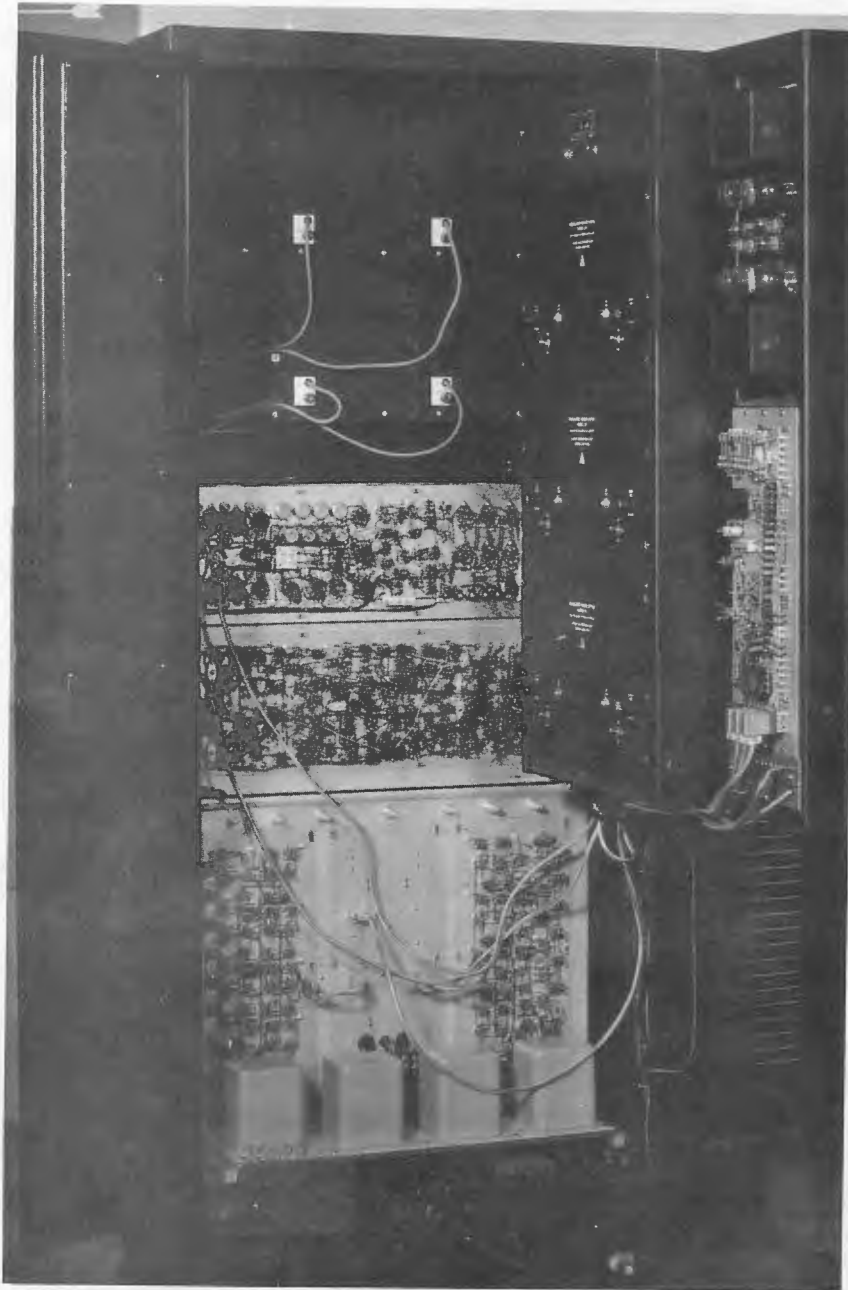


Fig. 3 - The countercept system simulator (rear view)

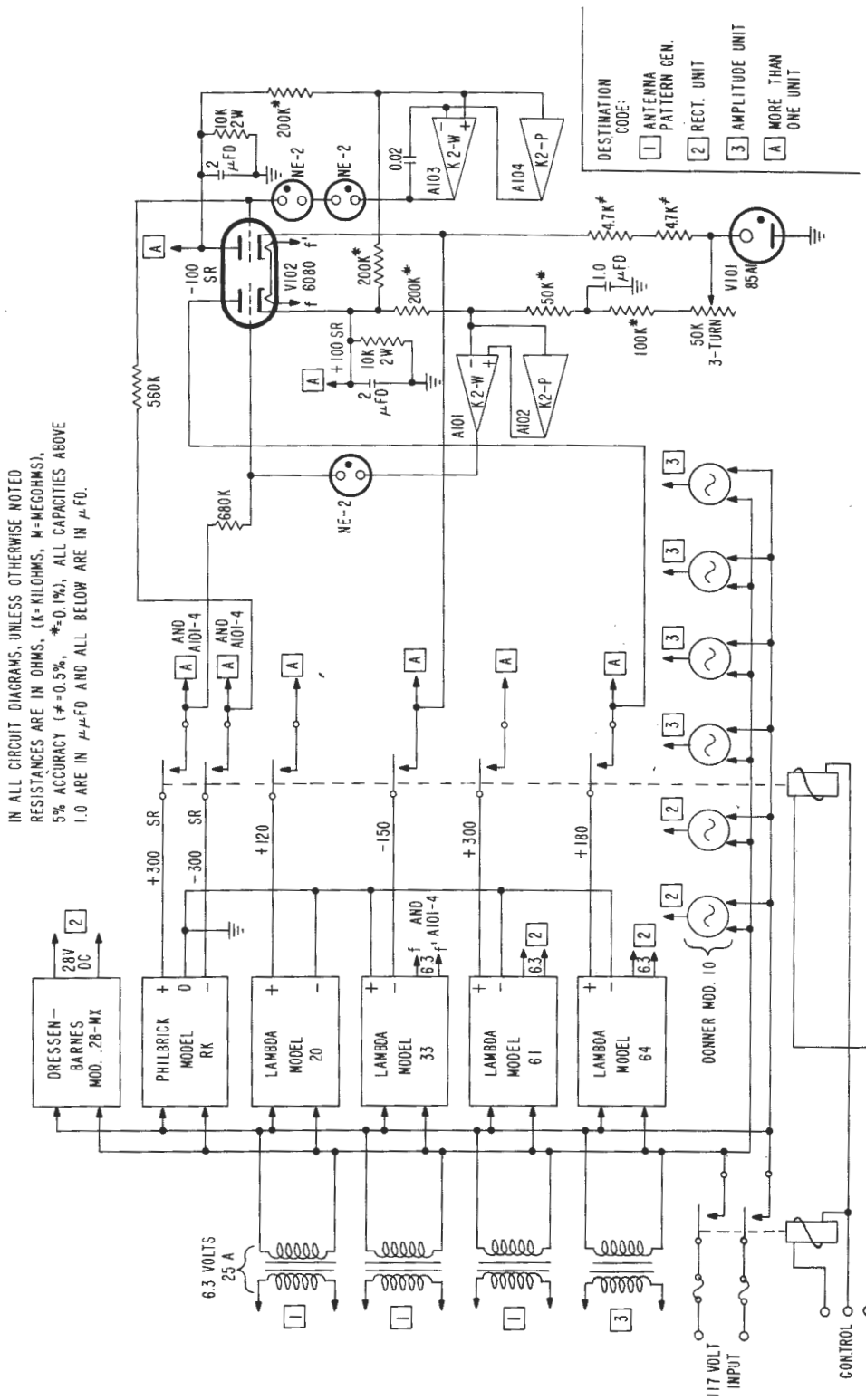


Fig. 4 - Power supply

The accuracy of the +100 volt SR\* output of the superregulator is determined by the stability of the 85A1 reference tube and hence can be relied upon to a very few parts per thousand. The -100 SR output tracks the +100 SR to an accuracy limited by the selected 0.1% divider resistors. Thus if the +100 SR output is assumed to be exactly 100 volts, even if R101 is not precisely adjusted or V101 drifts; the -100 SR will be at -100 assumed volts within the 0.1% tolerance that is standard for the simulator. All other waveforms are calibrated with respect to the +100 SR and -100 SR voltages. The circuitry is so arranged that the only necessary voltage decision is to determine whether or not certain voltages are above or below zero. Since these voltages are linear combinations of voltages calibrated against the +100 SR and -100 SR the decision will be correct even if the +100 SR is not at precisely 100 volts.

### Antenna Pattern Generator

The function of this unit is to produce a waveform which represents the combination of receiving and transmitting antenna gains to within a pair of constants which are supplied at the Amplitude Unit. The Amplitude Unit supplies to the Antenna Pattern Generator four waveforms, each a negatively full-wave-rectified sine wave of independently-controllable frequency held at exactly 20 volts peak amplitude. The pattern of each antenna is synthesized from two of these waveforms designated as the A and the B waveforms. Each antenna pattern is made up of four conditions which occur cyclically. For each condition the operator may control the number of cycles of the A waveform (and hence the duration of the condition), the amplitude of the A waveform, the amplitude of the B waveform, and the baseline of the waveform. The complete pattern is returned to the Amplitude Unit for combination with other amplitude conditions to produce the amplitude gate.

Figure 5 is a photograph of the front panel of the Antenna Pattern Generator. The components to the left of the center line, control the transmitting antenna pattern; those to the right, the receiving antenna pattern. Within each engraved box are found the potentiometers that set the amplitudes of the condition. The turns-counting dials on these potentiometers read directly in db's and tenths of a db. The time of transition from one condition to the next is controlled by the bank of preset counters which count cycles of the A waveform.

Figure 6 is a block diagram of the Antenna Pattern Generator, and shows the interconnection of the subassemblies. Note that all subassemblies except the output circuit are duplicated. The output circuit, is, of course, common to both the transmitter- and receiver-antenna simulation circuitry.

Figures 7 and 8 are circuit diagrams of Eccles-Jordan circuits, hereinafter referred to as EJ's, that are used throughout the simulator. Figure 7 is the standard EJ used for general locking and memory purposes. Its associated circuitry is usually arranged so that the switching time of the EJ is relatively unimportant. Figure 8 is a special EJ used where fast switching and a low-impedance output centered about ground are required.

Figure 9 is the circuit diagram of the antenna timer. Its operation can perhaps best be understood by first referring to Fig. 10. The clock-pulse generator produces pulses at the zero crossings of the sine wave which was full-wave-rectified to produce the A waveform. These pulses are counted by two paralleled banks of preset counters. In Fig. 10, A, B, C, and D refer to the counts which are preset on the counters. Assume that the count is less than A and that all EJ's are off. At the count of A (i. e., after A clock pulses) an output is produced on the A bus. Unfortunately, although the counters may operate up to 100 kc, this output is often considerably delayed. Therefore instead of

\*Denotes superregulated

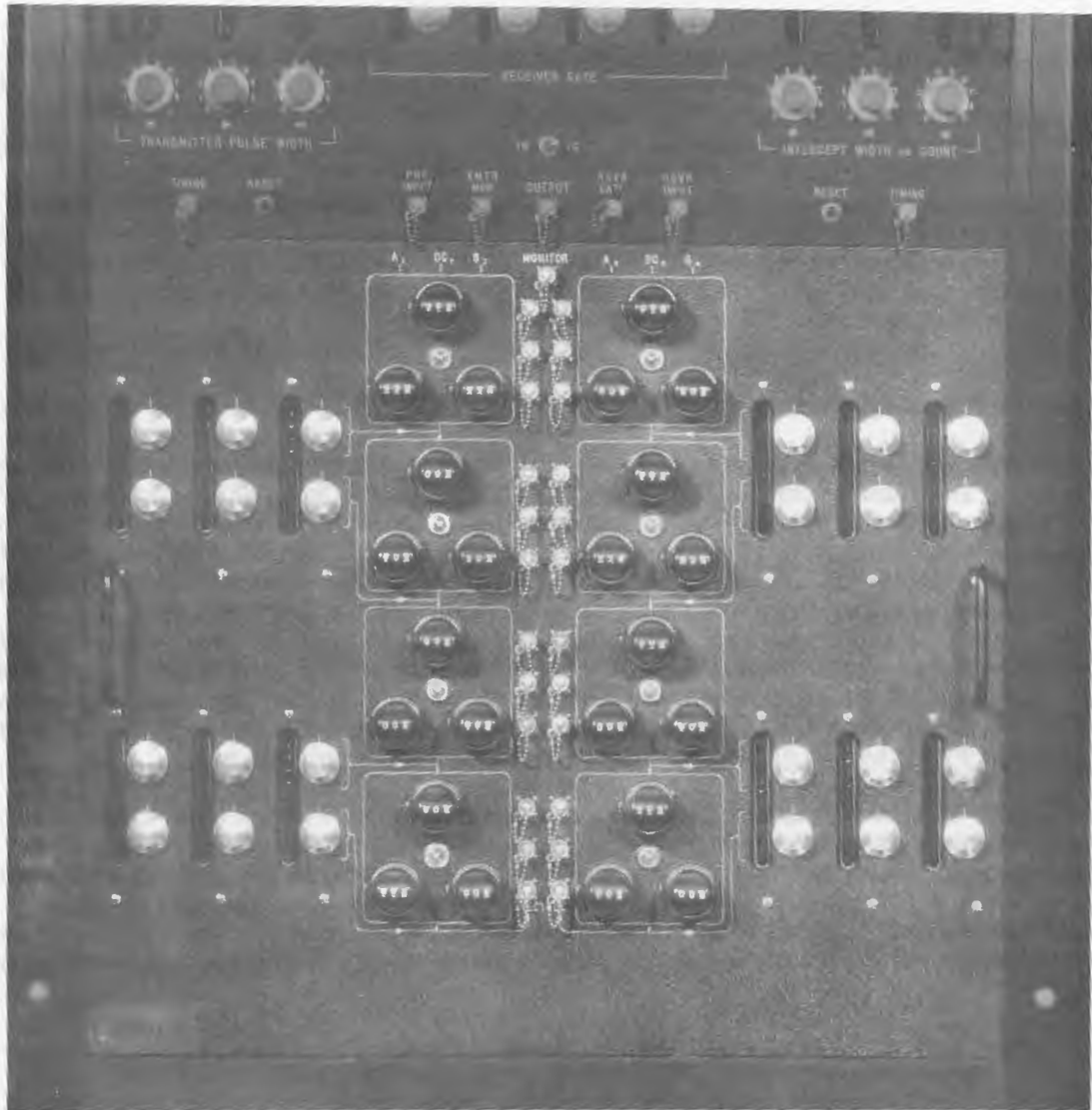


Fig. 5 - Antenna pattern generator (front panel)

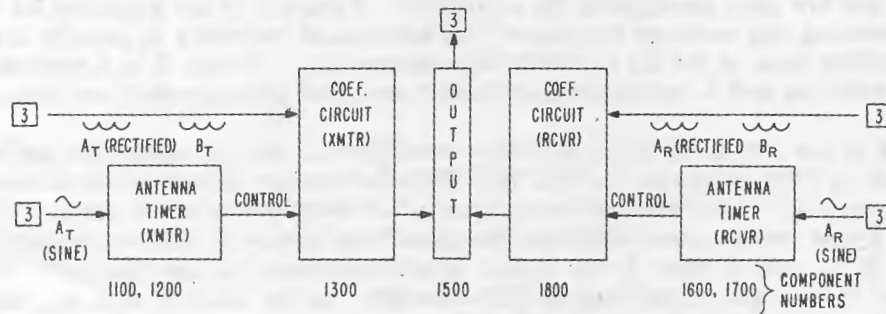


Fig. 6 - Antenna pattern generator (block diagram)

using it to control the antenna pattern directly, it is used to turn on an EJ. This opens a gate through a delay circuit allowing the A+1 clock pulse to turn on the SPEC EJ on the left. Similarly the middle SPEC EJ is turned on at the count of B+1 and the SPEC EJ on the right at the count of C+1. At the count of D an EJ is triggered and the counter is reset to zero. The next clock pulse, which occurs at the count of 1, operates a multivibrator which turns off all EJ's. Hence the left SPEC EJ is on from a count of A+1 to 1, the middle SPEC EJ from B+1 to 1, and the right SPEC EJ from C+1 to 1, where the 1's are of the next cycle, i.e., D+1's. Now let us define Condition I as being that period when the left SPEC EJ is off, Condition II as being that period when the left SPEC EJ is on but the middle SPEC EJ is off, Condition III as being that period when the middle SPEC EJ is on but the right SPEC EJ is off, and Condition IV as being that period when the right SPEC EJ is on. It then follows that Condition I occurs from the count of 1 to A+1; Condition II, from A+1 to B+1; Condition III, from B+1 to C+1; and Condition IV, from C+1 to D+1 (i.e., 1). Since in simulation of antenna pattern only the duration of the conditions interests us, the result is the same as would have been obtained if Condition I existed from a count of 0 to A; II, from A to B; III, from B to C; and IV, from C to D (i.e., 0). This is the mechanism that is implied in the engraving that may be seen in Fig. 5.

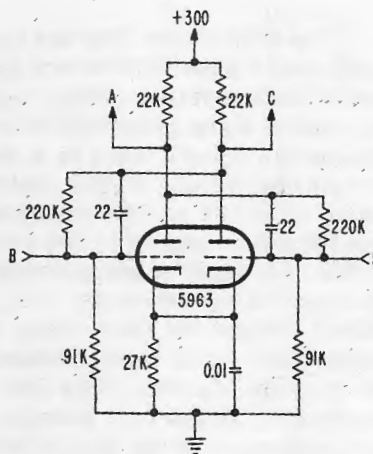


Fig. 7 - Standard EJ

We may now return to Fig. 9 and consider the operation of the antenna timer in detail. The components with 1100 (and 1600) prefixes are located just behind the front panel on the counter assembly, and may be thought of as constituting the clock-pulse generator. The components with 1200 (and 1700) prefixes are mounted in the rear of the Antenna Pattern Generator, and may be thought of as being the antenna timer itself.

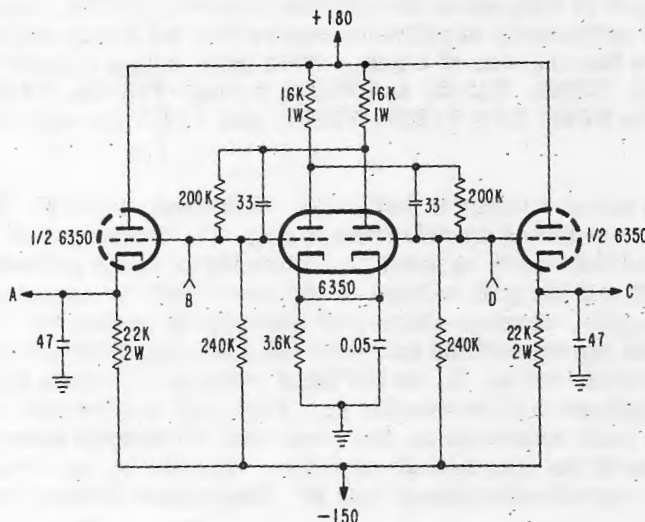


Fig. 8 - Special EJ

The sine waves that are used to produce waveform A are also sent directly to the clock-pulse generator where they are squared by X1101 and X1102. These silicon junction diodes have a voltage delay in forward conduction and hence require no bias. The resultant square wave is amplified by V1101 and passed to the Schmitt circuit, V1102. X1103 clamps the square wave to a voltage controlled by R1101 that is selected for proper Schmitt circuit operation. R1102 controls the Schmitt circuit sensitivity. The extremely square output of V1102 is differentiated and passed to the phase splitter, V1103a. The outputs of this tube are coupled to the grids of V1104, which are adjusted to a point beyond cutoff by R1103. A negative pulse occurs across the common load resistor of V1104 every half-cycle of the square wave, i. e., at the initiation of every lobe of the A waveform. These pulses trigger the monostable multivibrator, V1105, through X1104. R1104 controls the sensitivity of this multivibrator, and R1105 the duration of its output gate, which is usually set to about 5  $\mu$ sec. This gate is coupled to the cathode follower, V1103b, where it is clamped by X1105 to a voltage sufficiently negative to ensure that the output of V1103b will, in the absence of the multivibrator gate, cut off any grids to which it is connected. This output, referred to as the clock pulses, is fed to V1106, which drives C1101 and C1104. At the count of D, the positive signal on bus D causes V1107a to trigger the monostable multivibrator, V1108, through the coupling diode, X1106. The output of this multivibrator is fed to the cathode follower, V1107b. Normally V1107b is cut off, and its cathode is held at ground by X1107, which is conducting, thus assuring a low-impedance zero voltage on the reset bus, which is the combined grid return of half the tubes in the counters. The multivibrator gate raises the grid of V1107b well above ground, cutting off X1107 and resetting the counters.

In the antenna timer itself, V1202, V1209, V1215, and V1221 are the EJ's turned on at counts A, B, C, and D, through V1201a, V1208a, V1214a, and V1220a, respectively. By the counts of A+1, B+1, C+1, and 1; V1202, V1209, V1215, and V1221 have opened the gates V1203, V1210, V1216, and V1222 respectively through the RC delay networks. Thus the clock pulses occurring at these counts, respectively, turn on the SPEC EJ on the left, V1205; turn on the SPEC EJ in the middle, V1211; turn on the SPEC EJ on the right, V1217; and operate the monostable multivibrator, V1223, through X1201. V1204, V1206, V1212, and V1218 are the cathode followers associated with the SPEC EJ's. R1201 adjusts the sensitivity of V1223, and R1202 the duration of its gate, which is usually held within the range of 5 to 10  $\mu$ sec. This gate is coupled to the cathode follower, V1224, where it is clamped by X1202 to a voltage sufficiently negative to ensure that all grids connected to the output of V1224 are cut off in the absence of a gate. This gate, which occurs at the count of 1, resets the EJ's V1202, V1209, V1215, and V1221 through V1201b, V1208b, V1214b, and V1220b, and resets the SPEC EJ's V1205, V1211, and V1217 through V1207, V1213, and V1219, respectively.

The output of the antenna timer is fed to the coefficient circuits. The operation of these circuits can be understood by referring to Fig. 11. Suppose that three of the control points are negative and the fourth is positive. Then three of the cathode followers will be unconditionally cut off and the grid voltage on the fourth will be essentially determined by the output of the high-gain, chopper-stabilized operational amplifier. Since the loop is closed only through the fourth cathode follower and since the feedback resistor associated with this loop has the same value, R, as the input resistor, the gain from the input of this circuit to the fourth cathode will be exactly -1. Note that the crystals need not be perfect. If a crystal has finite back conductance, the error due to reverse current across R' will be reduced by the gain of the operational amplifier. Similarly, as long as the crystals have a forward impedance considerably lower than R', the proper cathode follower will remain cut off.



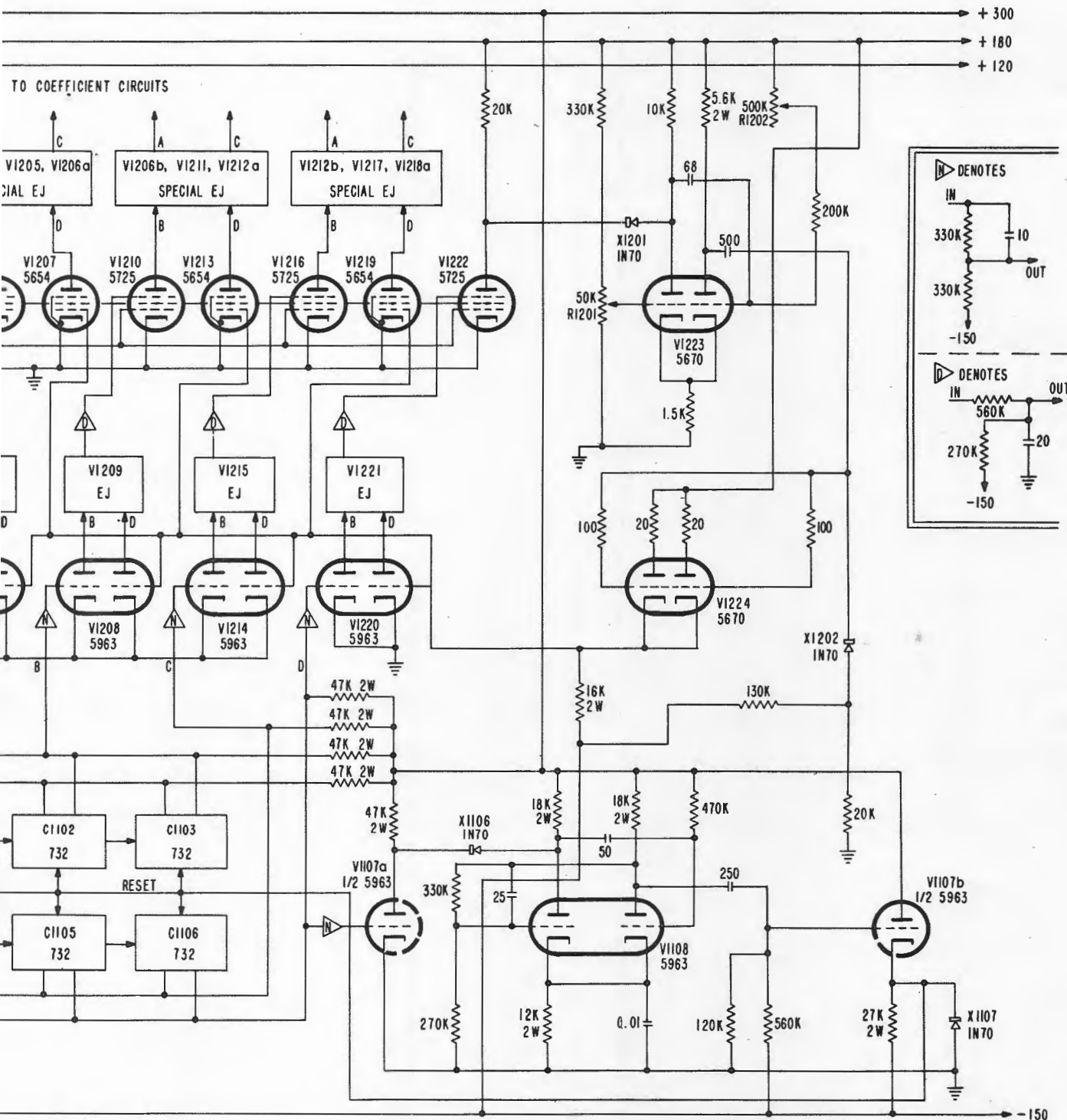


Fig. 9 - Antenna timer

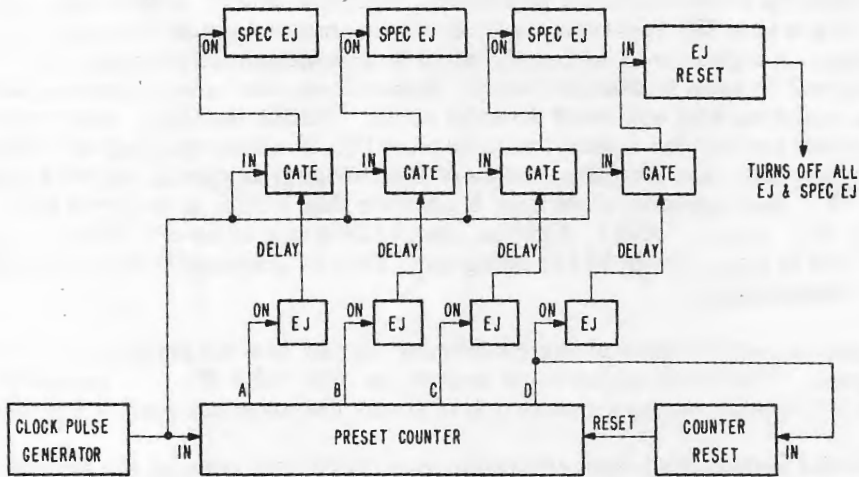


Fig. 10 - Antenna timer (block diagram)

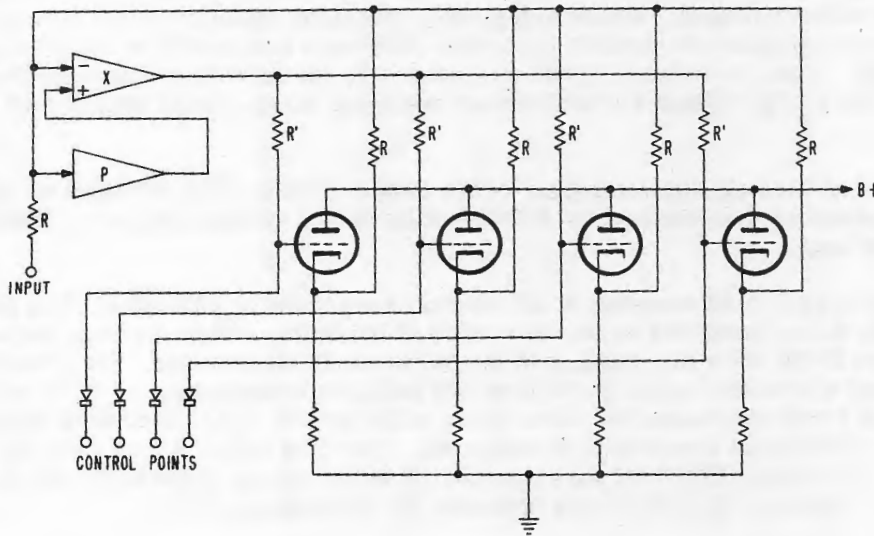


Fig. 11 - Basic coefficient circuit

The complete coefficient circuit is shown in Fig. 12. Figure 13 is a sketch of the front panel with the potentiometers identified. R1301 to R1312 replace the cathode resistors of Fig. 11. Each is a 2K, ten-turn, helical potentiometer tapped six turns from the counter-clockwise stop. A signal level of twenty volts is maintained across these six turns. A scale of 3 db/volt is used in this circuitry. Hence these six turns represent 60 db and a digital turns-counting dial will read directly in db. X1301 to X1318 carry out the specifications derived earlier for Conditions I through IV. In understanding the mode of connection of these crystals, use should be made of the theorem in circuit algebra that  $X + Y = \bar{X} \cdot \bar{Y}$ . For example, Condition II implies that V1205 is on and V1211 is off, and V1217 is off. Hence V1301a, V1304a, and V1305b are to be cut off either by V1205 being off or V1211 being on or V1217 being on. This is accomplished by X1301, X1310, and X1316, respectively.

The inputs to two sections of the coefficient circuit are the negative twenty-volt-peak A and B signals. The input to the third section is -100 volts SR. To maintain +20 volts on the selected cathode an input resistor five times the feedback resistor is employed.

The antenna pattern then appears as the sum of the voltages on the arm of the potentiometers. In general, only three potentiometers will have any voltage across them. During switching from condition to condition there is a slight problem. If the cathode followers are cut off before the next set are turned off, the voltage on the output of the operational amplifiers soars. If this voltage exceeds the dynamic range of the operational amplifier, the chopper stabilization loop is broken. Because of the slow rise time of the chopper amplifier it will take considerable time for the circuit to restabilize. If, however, two cathode followers in the same loop are operating, the sum of their cathode voltages will equal the negative of the input voltage and the sum of the voltages on the arms of the potentiometers (the output voltage of the circuit) will be some convex combination of the desired steady-state output voltages. Hence a desirable transient condition is brought about if, in the change from condition to condition, cathode followers are turned on before the others are turned off. This is assured by the condensers in the cathodes of the cathode followers of the SPEC EJ's (Fig. 8) and the well-known nonlinear large-signal behavior of a cathode follower.

Figure 14 is the schematic diagram of the output circuit. The voltages on the arms of all potentiometers are summed by A1501 and its output cathode follower, V1501. A1502 stabilizes the loop.

V1502 is used to hold one side of all monitor neon bulbs at +85 volts. The proper output of a SPEC EJ is connected to the other side of the bulbs. Thus the neon bulbs will indicate which SPEC EJ's are fired, and hence the condition existing. Since no diode matrix is used with these bulbs, more than one bulb per antenna may be lit at one time. The Condition I bulb is always lit. If no other bulbs are lit, i. e., if none of the SPEC EJ's are on, the existence of Condition I is indicated. The first SPEC EJ controls the Condition II bulb, the second SPEC EJ the Condition III bulb, and the third SPEC EJ the Condition IV bulb. Thus the lowest lit bulb indicates the condition existing.

The output of the Antenna Pattern Generator is taken from the cathode of V1501 and sent up to the Amplitude Unit. Notice that the output loop inverts the signal; i. e., increasingly negative output voltage simulates an increase in antenna gain.

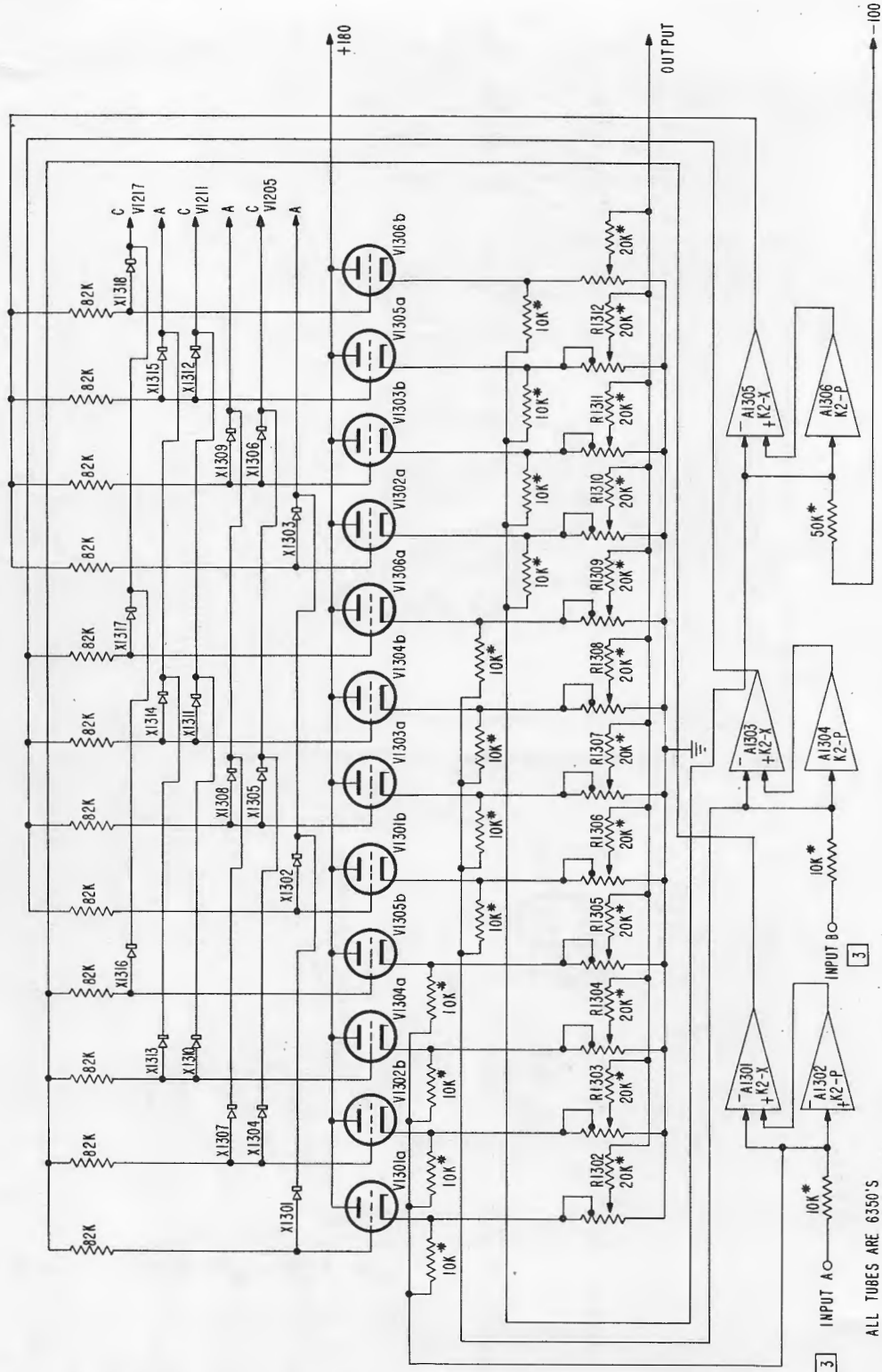


Fig. 12 - Coefficient circuit

ALL TUBES ARE 6350'S  
ALL CRYSTALS ARE IN305'S  
R1301-1312: SEE TEXT

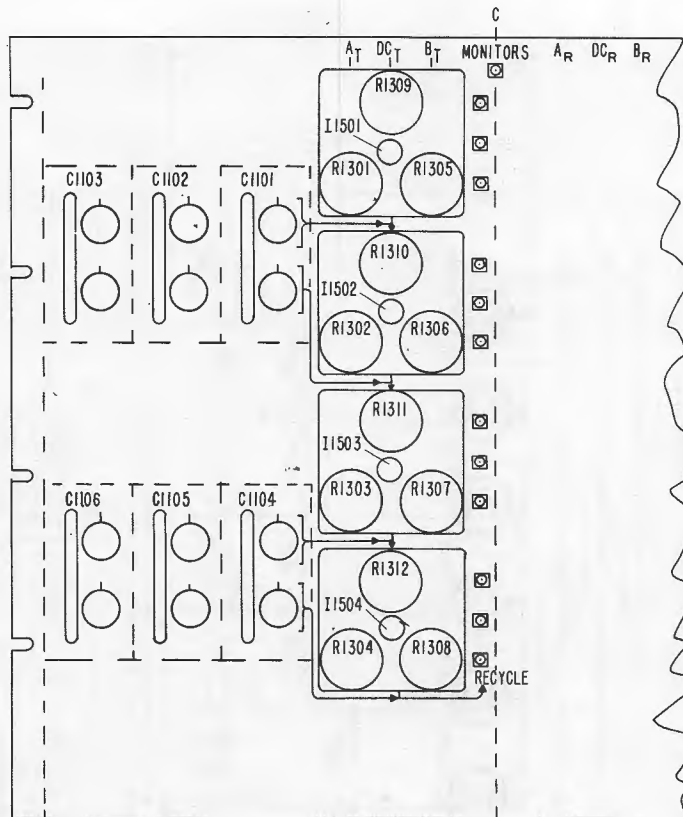


Fig. 13 - Antenna pattern generator (front panel sketch)

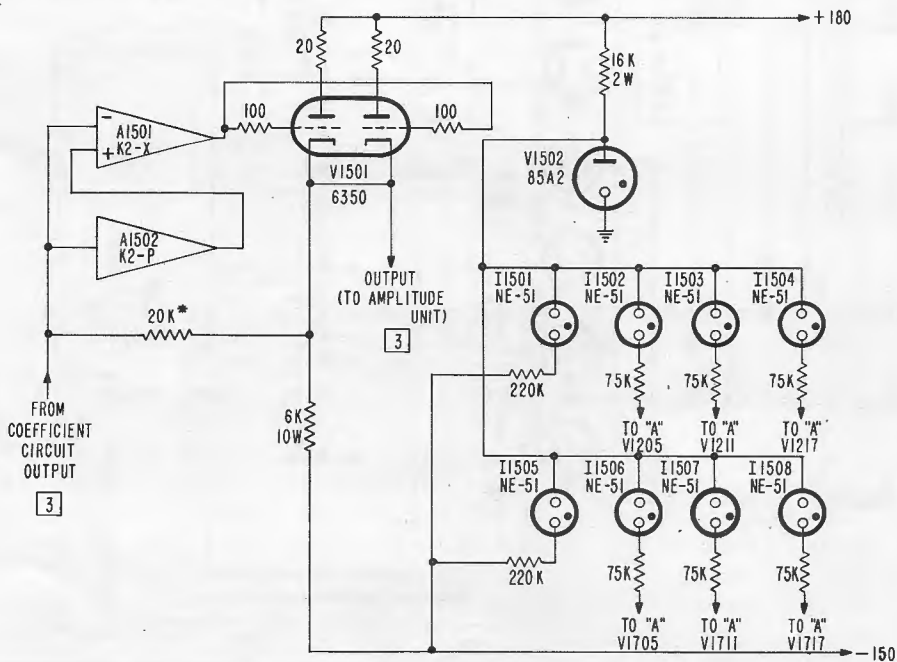


Fig. 14 - Antenna pattern output circuit

## Rectangular Gate Unit

The function of the Rectangular Gate Unit is to take the amplitude requirements which have been reduced by the Amplitude Unit to a rectangular gate, and to add rectangular gates to simulate the time and numerical requirements, producing an output at the coincidence of these gates. Figure 15 is a block diagram of this unit, and Fig. 16 is a photograph of its front panel.

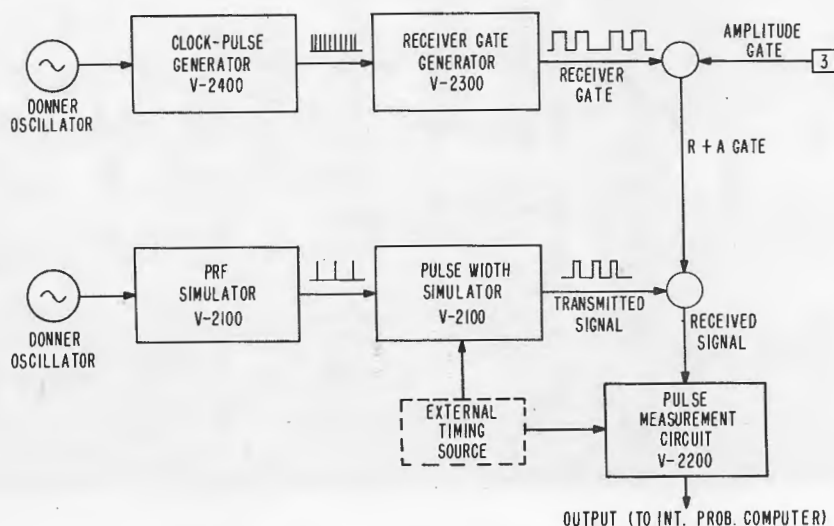


Fig. 15 - Rectangular gate unit  
(block diagram)

Sine waves from one of the oscillators mounted in the simulator are converted into timing pulses by the receiver clock-pulse generator. These pulses are fed into the receiver gate circuitry which produces a rectangular gate representing the fraction of time that the receiver is tuned to transmitter frequency. This gate is mixed with the amplitude gate, which represents the fraction of the time that the received power exceeds the receiver threshold. The combined gate, denoted as the R+A gate, simulates the fraction of the time during which operation of the transmitter would produce output from the receiver.

The transmitter simulator produces pulses at a rate determined by the sixth sine-wave oscillator. If continuous signal transmission is to be simulated, the prf is set to a very high value to assure that a pulse will get through any rectangular gate. If pulse width is significant, the duration of each pulse can be set at some multiple of an externally supplied timing period.

The output of the transmitter simulator is modulated by the R+A gate. A resulting output does not necessarily constitute an output. The pulse-measuring circuit takes into account the requirements of the operator or other decision element associated with the receiver. The pulse-measurement circuit can be made to indicate an intercept if a preset minimum number of pulses is received or if the intercept has at least a certain minimum duration. The assumption is that intercepts not meeting these requirements would be discarded by the operator or the decision circuit.

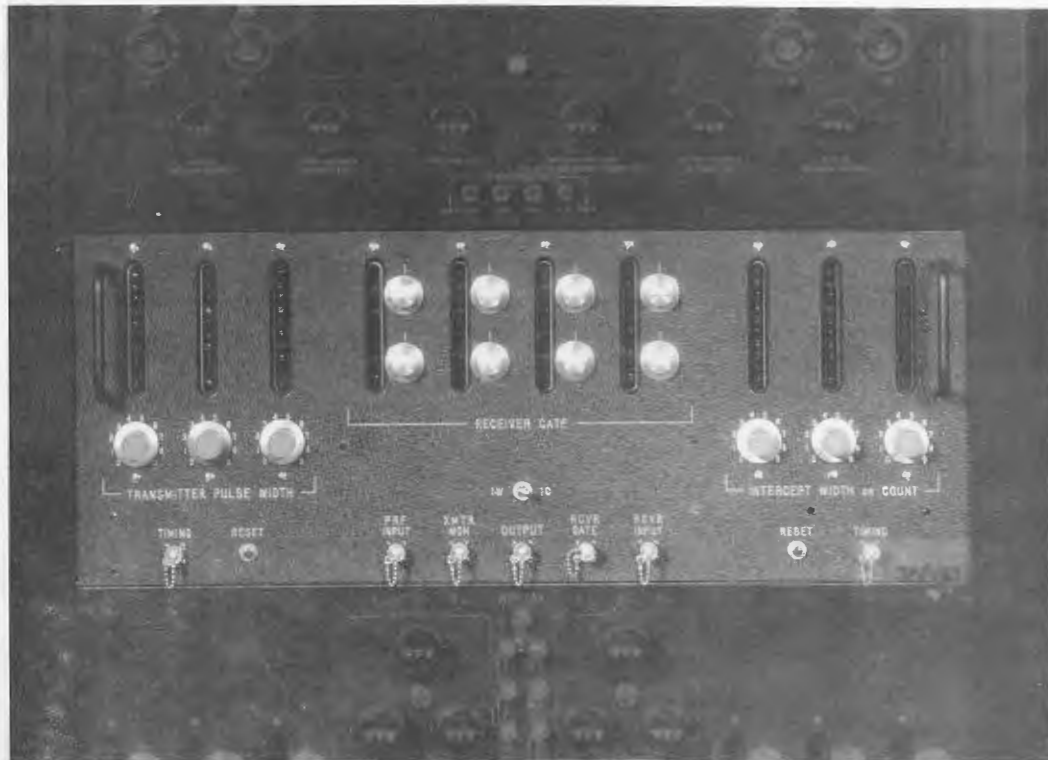


Fig. 16 - Rectangular gate unit (front panel)

Figure 17 is a more detailed block diagram of the transmitter simulator and pulse-measurement circuit. When the switches are in the P# (pulse number) position, it is assumed that the width of the pulses is unimportant. The transmitter simulator simply produces pulses at a rate determined by the sine-wave generator. These pulses are modulated in a gate tube by the R+A gate. The output of this operation is labelled "received signal." These pulses are amplified and counted by the preset P# and IW (intercept width) counter. After the preset number of pulses has been counted, the preset output of the counter, through its discriminator and an amplifier, operates a multivibrator which produces the simulator output. The counter is reset, however, by the trailing edge of the R+A gate. This assures that in order for the simulator to register an intercept, the preset number of pulses must occur within the duration of a single R+A gate. Thus if ten pulses are required before a signal can be recognized, these pulses must occur in a row — not five at one time and five a few minutes later — for an intercept to have occurred.

When the switches are in the PW (pulse width) position the transmitter simulator produces pulses of a controllable width. This is accomplished by using the prf pulses to turn on an EJ. The EJ opens a gate, allowing timing pulses from an external source to be fed to a preset counter. When the counter reaches its preset count the EJ is turned off, closing the gate, and the counter is reset to zero. Thus the EJ is on, at a repetition rate determined by the sine-wave oscillator, for a time equal to the product of the period of the timing source and the preset count.

The output of the EJ circuit, which represents the transmitted pulse, is now modulated by the R + A gate as before. The duration of the resulting simulated receiver pulse must now be measured. This is done by using it to control a gate which feeds pulses from an

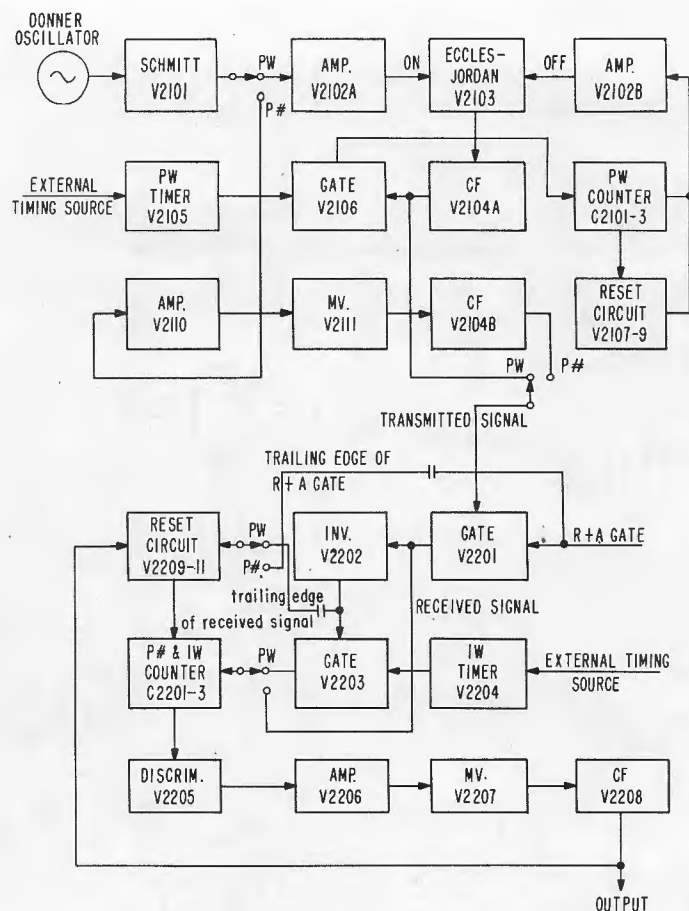


Fig. 17 - Transmitter simulator and pulse-measurement circuit (block diagram)

external timing source to the counter. The counter will reach its preset count and produce an intercept indication if the time duration of the coincidence of the transmitter pulse and the R+A gate exceeds the product of the period of the timing source and the preset count. The trailing edge of the coincidence is used to reset the counter in order to ensure that the width of but a single coincidence is measured.

It may be noticed that in either function the counter in the pulse-measuring circuit is reset whenever the circuit produces an output. In the intercept width case, this will mean that whenever the length of the coincidence exceeds the preset minimum intercept width, an intercept output will be produced after every minimum intercept width for the duration of the coincidence. This is of no consequence since the minimum intercept width should be narrow compared to the resolution with which probability information is required. In the pulse-counting function, however, this resetting action performs an important operation. If the prf of the transmitted signal is very low, and if the R+A gate remains on, there is essentially an intercept every pulse. It is therefore necessary to have each intercept reset the counter so that the next pulse will indicate an intercept.

Figure 18 is the circuit diagram of the transmitter simulator. The input sine waves used to control the prf are converted into square waves by the Schmitt circuit, V2101.

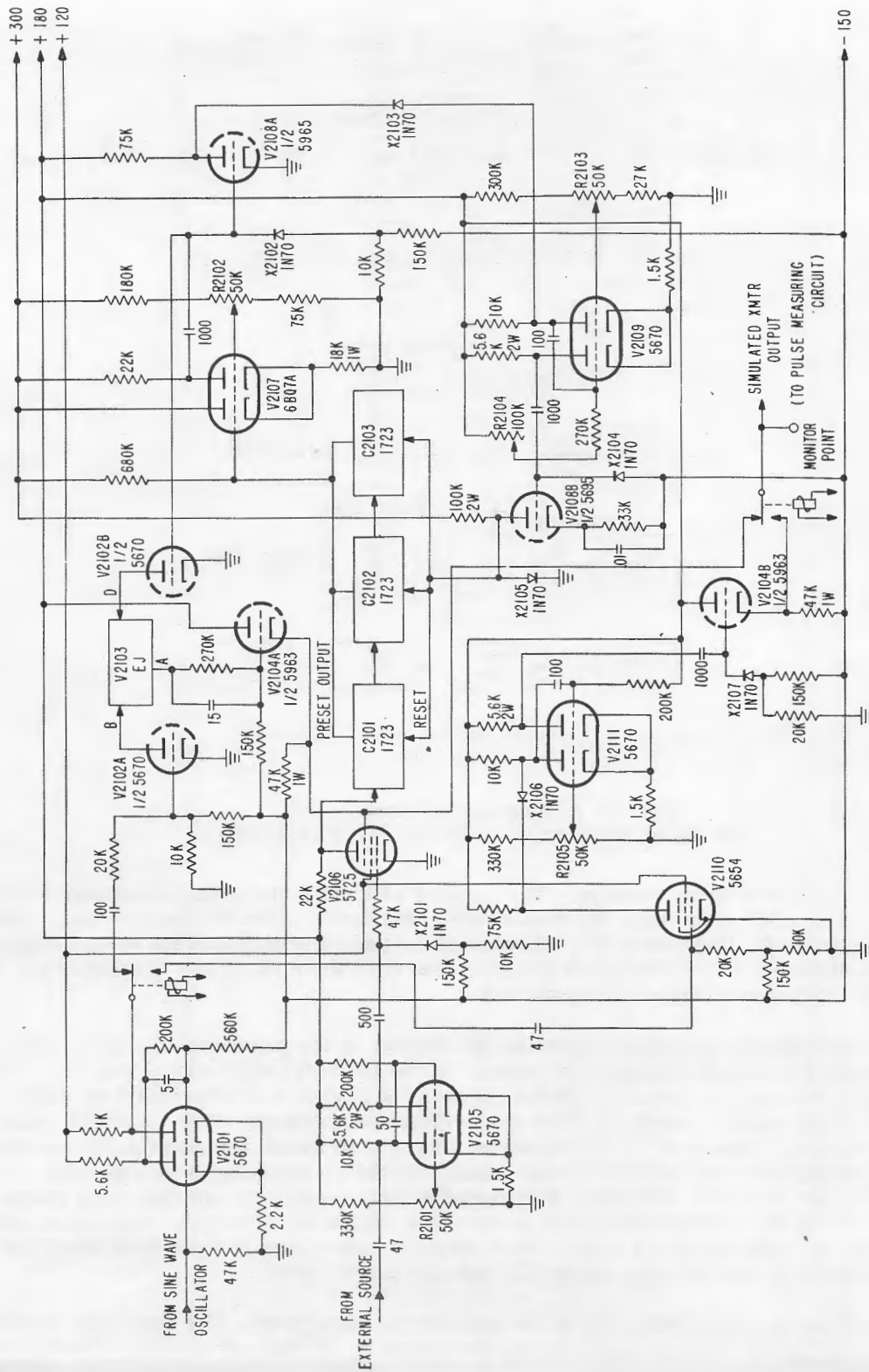


Fig. 18 - Transmitter simulator

Assuming the circuit is in the PW function, as in the drawing, the positive-going leading edge of this square wave raises the grid of V2102a above cutoff and turns on the EJ, V2103. The output voltage of the EJ rises and causes the voltage on the output cathode follower, V2104a, to rise from a negative to a positive value. As was previously mentioned, this EJ-controlled voltage represents the simulated transmitter output.

Meanwhile the external timing source is used to trigger the monostable multivibrator, V2105, whose sensitivity is controlled by R2101. The output of this multivibrator is negative-peak clamped by X2101 to a value below cutoff of the gate tube, V2106. The gate tube is controlled by V2104a. Thus, while the EJ is on, timing pulses will pass through the gate tube. The output of the gate tube is connected to the pulse-width counter string, C2101 to C2103. After the preset number of timing pulses, i. e., after the preset time has elapsed since the turning on of the EJ, the counter string produces a positive pulse on its preset bus. The cathode-coupled discriminator, V2107, which is controlled by R2102, is used to select this rise from smaller premature rises. The output of the discriminator is negative-peak clamped by X2102 below cutoff of V2108a which amplifies and inverts the preset pulse. This pulse is coupled through trigger diode X2103 to the monostable multivibrator, V2109, whose sensitivity is controlled by R2103, and whose gate is set with R2104 to the vicinity of 15  $\mu$ sec. This gate is clamped to the -150 bus by X2104. In the absence of the multivibrator gate, V2108b is conducting less than 3 ma. Its plate would therefore be above ground if not for the presence of X2105 which is conducting. When the grid of V2108b rises, the 33- $\mu$ sec time constant in its cathode prevents the cathode from following immediately, and plate current is drawn, cutting off X2105 and resetting the counters. While X2105 is conducting, however, the counter-reset bus is grounded through a low impedance.

The positive-going signal on the grid of V2108a is also fed to the grid of V2102b, which resets the EJ, V2103. Thus after the preset time the counter is reset, and the EJ (and therefore the simulated transmitter output) is turned off until the prf oscillator has gone through another cycle.

If, however, the switches (relays) are in the pulse-number position, the square-wave output of V2101 is differentiated and passed to V2110, whose grid is biased below cutoff. Thus there will appear on the plate of V2110 one negative pulse per cycle of the prf oscillator. This pulse is coupled through X2106 to the monostable multivibrator V2111, whose sensitivity is controlled by R2105. The output of the multivibrator is negative-peak clamped by X2107 to a voltage sufficiently low that the output of the output cathode follower, V2104b, will normally be well below ground, but will swing above ground for the simulation of the transmitter pulse.

The output of the transmitter simulator is fed to the pulse-measurement circuit shown in Fig. 19. The relays in this circuit work in synchronism with the relays in the transmitter simulator from the same front-panel toggle.

First let us analyze the action of the pulse-measurement circuit with the relays in the IW position as shown in Fig. 19. The output of the transmitter simulator is modulated by the R+A gate in the gate tube, V2201. V2202 is held full conducting through X2201 until V2201 can produce a sufficiently large negative output to cut off X2201. The plate of V2202 then rises, opening the gate tube, V2203. Meanwhile pulses from an external timing source are differentiated and fed through X2202 to the monostable multivibrator, V2204, whose sensitivity is controlled by R2201. The output of V2204 is negative-peak clamped below cutoff by X2203 and fed to the gate tube, V2203. The output of V2203 is fed to the counter string, C2204-6. After the occurrence of the preset number of pulses, i. e., after a sufficiently long coincidence between the transmitter pulse and the R+A gate, the voltage

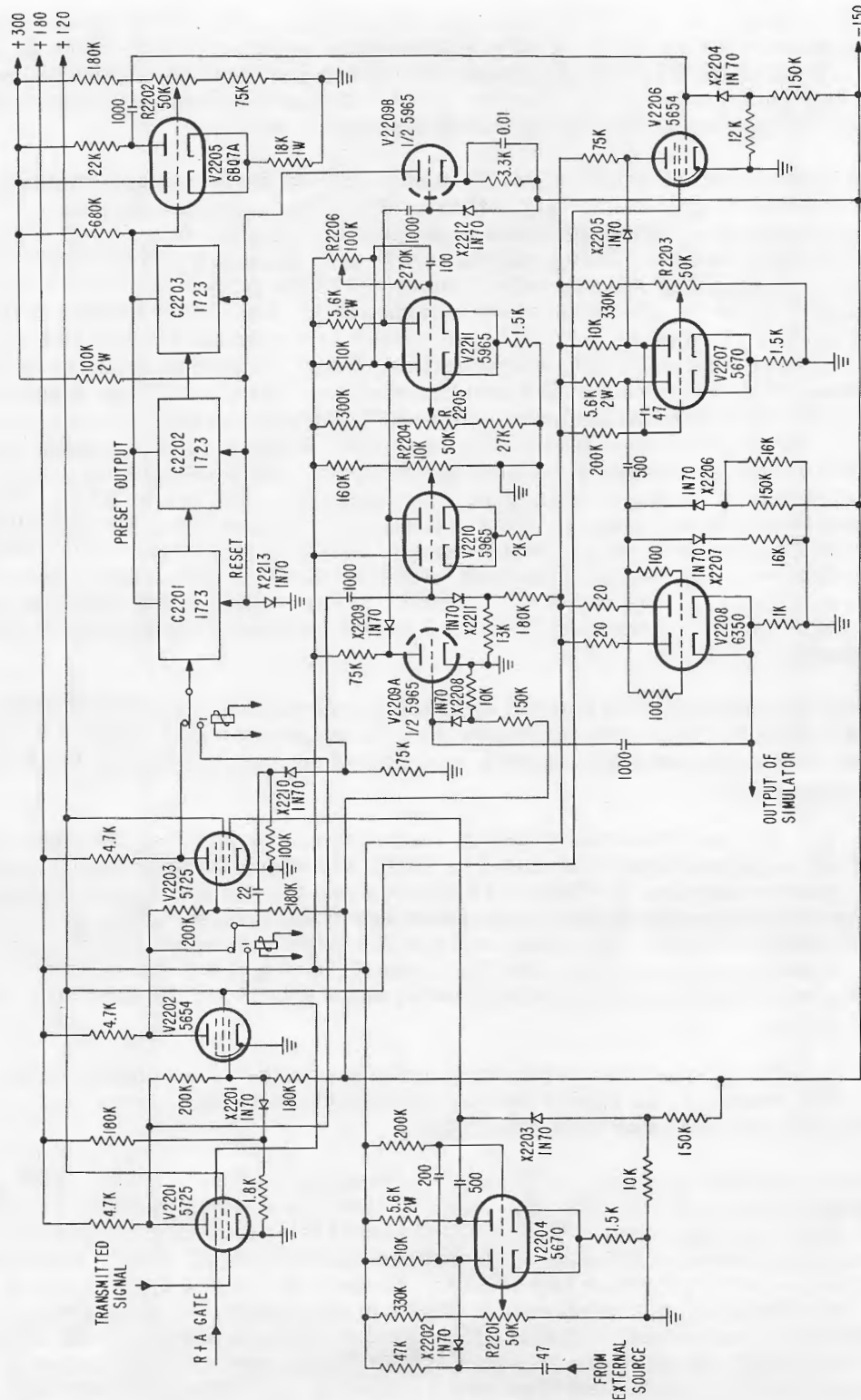


Fig. 19 - Pulse-measurement circuit

on the preset output bus of the counter string rises. The discriminator, V2205, which is controlled by R2202, amplifies this rise while disregarding any premature outputs of less amplitude. The output of the discriminator is coupled to the grid of V2206, which is negative-peak clamped below cutoff by X2204, producing a negative pulse on the plate of V2206, which is coupled by the keying diode, X2205, to the monostable multivibrator, V2207, whose sensitivity is controlled by R2203. X2206 and X2207 hold the output of V2207 between the proper levels to insure that the output cathode follower for the entire simulator, V2208, is normally cut off and produces a positive pulse of constant width and amplitude whenever an intercept is to be recorded.

Figure 17 indicates that the counters should be reset either by the intercept output or by the termination of the coincidence between the transmitter pulse and the R+A gate. The output of the simulator is capacity-coupled to the grid of V2209a and the negative-peak clamped by X2208 to a point below cutoff. An intercept then causes conduction in V2209a, and the resulting fall in its plate voltage is coupled through the keying diode X2209 to the monostable multivibrator, V2211. On the other hand, the plate waveform of V2202, which is the positive-going coincidence of the transmitter pulse and the R+A gate, is differentiated, and the negative spike marking its termination passed through X2210 to the grid of V2210, which is positive-peak clamped by X2211. R2204 is set so that with no signal the right half of V2210 is cut off. The termination of the coincidence will, however, cause conduction in V2210b and also trigger the monostable multivibrator, V2211. R2205 controls the sensitivity of this multivibrator, and R2206, its gate duration, which is set to about 15  $\mu$ sec. The function of X2212, V2909b, and X2213 in resetting C2204-6 is exactly the same as that of X2104, V2108b, and X2105 in resetting C2201-3 as already described.

Now let us consider the operation of the pulse-measurement circuit in the pulse-counting (P#) function. The input of C2204 is transferred to the plate of V2201, which contains the transmitter pulses modulated by the R+A gate. The input of the reset circuitry through X2210 is transferred to the R+A gate. Thus an intercept will be produced if the preset number of transmitter pulses occurs within the duration of a single R+A gate.

The desired form of the receiver gate is shown in Fig. 20. The "on-signal time" is the length of time required for the receiver passband to cross the signal frequency and is equal to the product of the time required for a one-way scan of the band searched and the ratio of receiver bandwidth to the width of the frequency band searched. It can also be expressed as the quotient of the receiver passband divided by the receiver scanning rate. The simulated on-signal time is controlled by the period of one of the sine-wave oscillators mounted in the upper portion of the simulator.

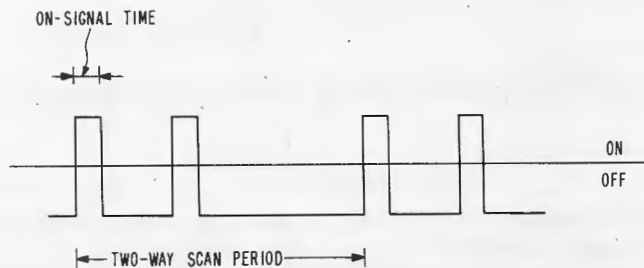


Fig. 20 - Receiver gate

If the receiver scan is sawtooth, i. e., if the receiver scans from one end of its band to the other and then very rapidly returns to its starting point, the receiver gate should consist of a positive pulse of duration equal to the simulated on-signal time occurring with a period equal to the simulated scanning time. If, however, the scan is a symmetrical sawtooth, i. e., if the receiver scans with equal speed in both directions, the receiver gate must be asymmetrical, with the degree of asymmetry depending on the location of the signal frequency in the search band of the receiver.

The method used to achieve the desired receiver gate is shown diagrammatically in Fig. 21. The clock pulses occur with a period equal to the simulated on-signal time. All other times are expressed as a multiple of this period. The clock pulses are fed to a dual preset counter string, which is preset to the length of the scan cycle and to the length of one of the subcycles. The complexity of Fig. 21 is largely due to the characteristics of the counter: that although the first output on the preset bus appears after the preset count, outputs may also appear at higher counts; and that the appearance of the output on the preset bus may be delayed a considerable and a variable fraction of a clock-pulse period after the occurrence of the preset clock pulse.

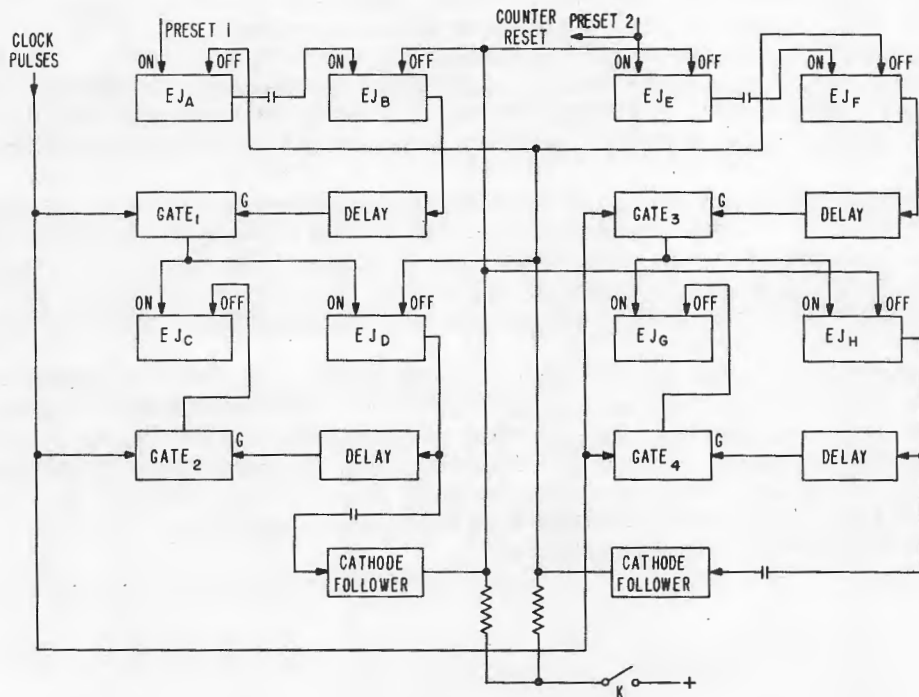


Fig. 21 - Receiver gate generator (block diagram)

In Fig. 21, all EJ's are assumed to have a positive output when on, and a negative output when off; gates are assumed to be opened by positive voltages at terminal G, and to produce positive outputs for positive inputs when open; EJ's are assumed to be turned on and off by positive signals at the appropriate input terminal; condensers are assumed to indicate differentiation; and the duration of all delays is assumed to be considerably greater than a clock-pulse width, but considerably less than a clock-pulse period. Figure 21 can perhaps be understood by perusing it in connection with Table 3.

TABLE 3  
Operation of Receiver Gate Circuitry

| COUNT                  | EJ <sub>A</sub> | EJ <sub>B</sub> | GATE <sub>1</sub> EJ <sub>C</sub> | ED <sub>D</sub> | GATE <sub>2</sub> EJ <sub>E</sub> | EJ <sub>F</sub> | GATE <sub>3</sub> EJ <sub>G</sub> | EJ <sub>H</sub> | GATE <sub>4</sub> RESET |
|------------------------|-----------------|-----------------|-----------------------------------|-----------------|-----------------------------------|-----------------|-----------------------------------|-----------------|-------------------------|
| Start                  | off             | off             | shut off                          | off             | shut off                          | off             | shut off                          | off             | shut off                |
| P <sub>1</sub> + ε     | on              | on              | shut off                          | off             | shut off                          | off             | shut off                          | off             | shut off                |
| P <sub>1</sub> + ε + d | on              | on              | open off                          | off             | shut off                          | off             | shut off                          | off             | shut off                |
| P <sub>1</sub> + 1     | on              | off             | open on                           | on              | shut off                          | off             | shut off                          | off             | shut off                |
| P <sub>1</sub> + 1 + d | on              | off             | shut on                           | on              | open off                          | off             | shut off                          | off             | shut off                |
| P <sub>1</sub> + 2     | on              | off             | shut off                          | on              | open off                          | off             | shut off                          | off             | shut off                |
| ⋮                      |                 |                 |                                   |                 |                                   |                 |                                   |                 |                         |
| P <sub>2</sub> + ε     | on              | off             | shut off                          | on              | open on                           | on              | shut off                          | off             | shut on                 |
| ε + d                  | on              | off             | shut off                          | on              | open on                           | on              | open off                          | off             | shut off                |
| 1                      | off             | off             | shut off                          | off             | open on                           | off             | open on                           | on              | shut off                |
| 1 + d                  | off             | off             | shut off                          | off             | shut on                           | off             | shut on                           | on              | open off                |
| 2                      | off             | off             | shut off                          | off             | shut on                           | off             | shut off                          | on              | open off                |
| ⋮                      |                 |                 |                                   |                 |                                   |                 |                                   |                 |                         |
| P <sub>1</sub> + ε     | on              | on              | shut off                          | off             | shut on                           | off             | shut off                          | on              | open off                |
| P <sub>1</sub> + ε + d | on              | on              | open off                          | off             | shut on                           | off             | shut off                          | on              | open off                |
| P <sub>1</sub> + 1     | on              | off             | open on                           | on              | shut off                          | off             | shut off                          | off             | open off                |
| P <sub>1</sub> + 1 + d | on              | off             | shut on                           | on              | open off                          | off             | shut off                          | off             | shut off                |
| P <sub>1</sub> + 2     | on              | off             | shut off                          | on              | open off                          | off             | shut off                          | off             | shut off                |

The manual reset button for C2101-3 also closes the contact K assuming that EJ<sub>A</sub>, EJ<sub>B</sub>, EJ<sub>D</sub>, EJ<sub>E</sub>, EJ<sub>F</sub>, and EJ<sub>H</sub> are initially off. The initial condition of EJ<sub>C</sub> and EJ<sub>G</sub> is immaterial. For this discussion we shall assume they are initially off. Let P<sub>1</sub> and P<sub>2</sub> be the two preset counts where P<sub>1</sub> is less than P<sub>2</sub>. Then at the count of P<sub>1</sub> + ε (where ε represents the fraction of a count the preset output is delayed by the counter), EJ<sub>A</sub> is turned on. The differentiated output of EJ<sub>A</sub> turns EJ<sub>B</sub> on. Because of the differentiation, subsequent outputs on the preset output bus can have no effect on EJ<sub>B</sub> as long as EJ<sub>A</sub> remains on. By the count of P<sub>1</sub> + ε + d, (where d is the delay expressed as a fraction of a count), gate<sub>1</sub> is opened. Thus the next clock pulse, which occurs at the count of P<sub>1</sub>+1 can turn on EJ<sub>C</sub> and EJ<sub>D</sub>.

The differentiating circuit attached to the output of  $EJ_D$  allows the act of turning on this  $EJ$  at the count of  $P_1 + 1$  to turn off  $EJ_B$ ,  $EJ_E$ , and  $EJ_H$ . By the count of  $P_1 + 1 + d$ , gate<sub>1</sub> is closed but gate<sub>2</sub> is open. Thus subsequent clock pulses can no longer try to turn on  $EJ_C$  and  $EJ_D$ , but the very next clock pulse which occurs at the count of  $P_1 + 2$  turns off  $EJ_C$  through gate<sub>2</sub>.

This state of affairs continues until the count of  $P_2 + \epsilon$  at which time the counter is reset to zero and  $EJ_E$  is turned on, turning on  $EJ_F$ , opening gate<sub>3</sub> by  $P_2 + \epsilon + d$ . The  $P_2 + 1$  clock pulse, which registers as the first clock pulse on the reset counter now turns on  $EJ_G$  and  $EJ_H$ . The act of turning on  $EJ_H$  turns off  $EJ_A$ ,  $EJ_D$ , and  $EJ_F$ . Note that it is now permissible to turn off  $EJ_A$  since the counter has been reset to a count less than  $P_1$ . It is necessary to turn off  $EJ_D$  so that gate<sub>2</sub> may be closed allowing  $EJ_C$  to be turned on later.

$EJ_H$  also turns on gate<sub>4</sub> by the count of  $1 + d$ . Thus on the count of 2,  $EJ_G$  is turned off. This state of affairs continues until the count of  $P_1$  at which time the cycle repeats.

The receiver gate is considered to be present when either  $EJ_C$  or  $EJ_G$  is on. Inspection of Table 3 shows that  $EJ_C$  is on between the counts of  $P_1 + 1$  and  $P_1 + 2$ , while  $EJ_G$  is on between the counts of 1 and 2. The cycle is  $P_2$  long. Thus in setting up the receiver gate, the clock-pulse period is set to the simulated on-signal time,  $P_2$  is set to the ratio of two-way scan time to on-signal time, and  $P_1$  is set to a number depending on the position of the signal frequency within the receiver frequency band. Since the numbering of the counts is immaterial, we can consider the circuit as producing a gate between the counts of zero and 1, and between  $P_1$  and  $P_1 + 1$ . This makes the set-up of a problem somewhat easier to visualize.

Figure 22 shows the circuit diagram of the receiver gate circuitry. It is somewhat more complicated than Fig. 21 as the polarity assumptions of Fig. 21 do not match the characteristics of gate tubes, necessitating several phase inverters. The output condition is that either  $EJ_C$  or  $EJ_G$  be on. The "C" lead on an  $EJ$  is positive when off, negative when on. Thus if either  $EJ$  is on, its "C" output will cut off V2326 and produce the positive output. Otherwise Fig. 22 is simply the translation of Fig. 21 into a schematic diagram.

Figure 23 shows the clock-pulse generator for the receiver gate and the mode of assembly of the subunits in the rectangular gate unit.

Sine waves of period equal to the simulated receiver on-signal time from one of the six oscillators are fed to the Schmitt circuit, V2401. Ordinarily this circuit would square sine waves, but the ringing and clipping circuit (consisting of X2401, the 33- $\mu$ h inductance, and circuit capacity), produces a single positive pulse for every cycle of the input sine wave. This pulse is coupled to the inverter, V2402, whose grid is clamped by X2402. The resulting negative pulse is coupled through the keying diode, X2403, to the monostable multivibrator, V2403, whose sensitivity is controlled by R2401. The resultant gate is negative-peak clamped by X2404 and fed to the cathode follower, V2404a. The positive-going output of this cathode follower can be fed directly to the receiver gate circuits, but must be inverted by V2405 in order to drive the receiver gate counters, C2401-4.

The receiver gate is mixed with the amplitude gate in the circuit consisting of X2505 and X2506. Like the receiver gate, the amplitude gate is positive when interception is possible, and negative otherwise. The combined R+A gate, which has the same polarity characteristic, is passed through the cathode follower, V2404b, and then to the pulse-measurement circuit.



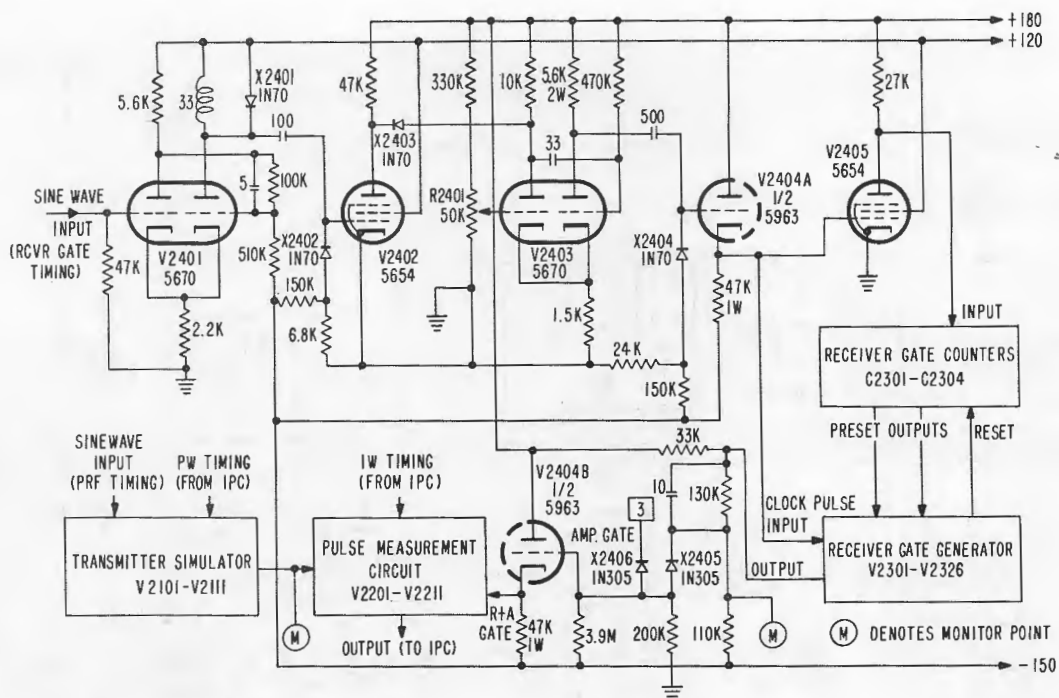


Fig. 23 - Rectangular gate unit assembly

Amplitude Unit

Figure 24 is the block diagram of the Amplitude Unit, and Fig. 25 is a photograph of its front panel. As can be seen in Fig. 24, the Amplitude Unit performs two more or less separate functions. This unit produces and monitors the "full-wave" components that are used to synthesize the antenna pattern, and also uses the antenna pattern and various reference settings to produce the amplitude gate.

Figure 26 is the circuit diagram of the full-wave rectifier. The input sine waves are inverted by A3101. Since this amplifier is not chopper stabilized, its offset voltage must be manually adjusted. This is accomplished by removing its input and adjusting R3101 for zero amplifier output as monitored by the microammeter. A3102 inverts the signal again. The offset of A3102 may be adjusted with R3102. If A3101 is properly offset, it should have zero output and hence zero input to the A3102 loop. Thus R3102 is adjusted for zero output on A3102 with no input to A3101. The negative halves of these out-of-phase sine waves are passed through X3101 and X3102 to the unity-gain cathode follower consisting of A3103 and V3101a. The offset of this circuit can be controlled by adjusting R3103 for zero output on the cathode of V3101a if R3101 and R3102 have first been adjusted. This output is the signal that is sent to the Antenna Pattern Generator.

At first it might appear that A3102 is unnecessary and that the cathode of X3102 could be connected directly to the sine-wave input. The resulting nonlinear load on the sine-wave generator would, however, cause an intolerable shift in the reference level.

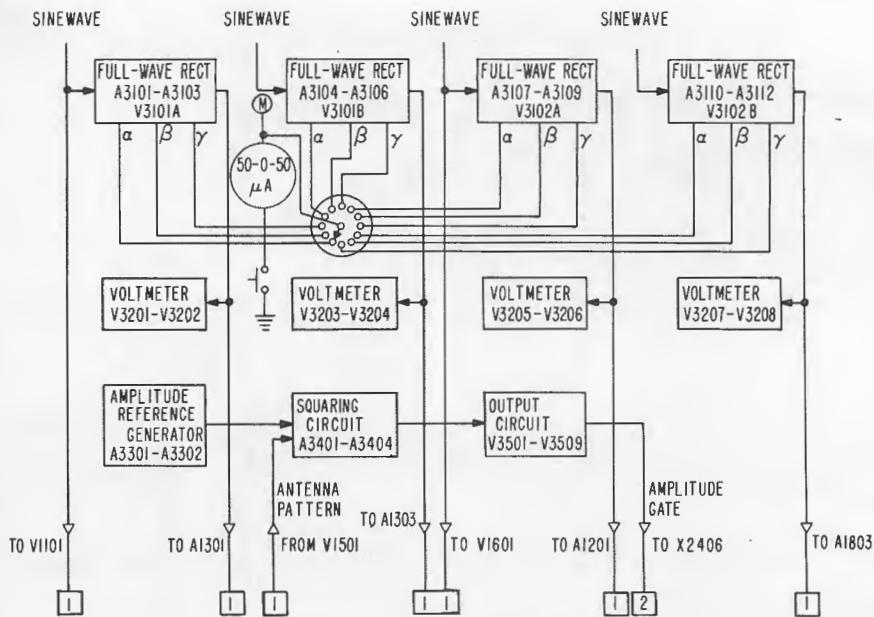


Fig. 24 - Amplitude unit (block diagram)

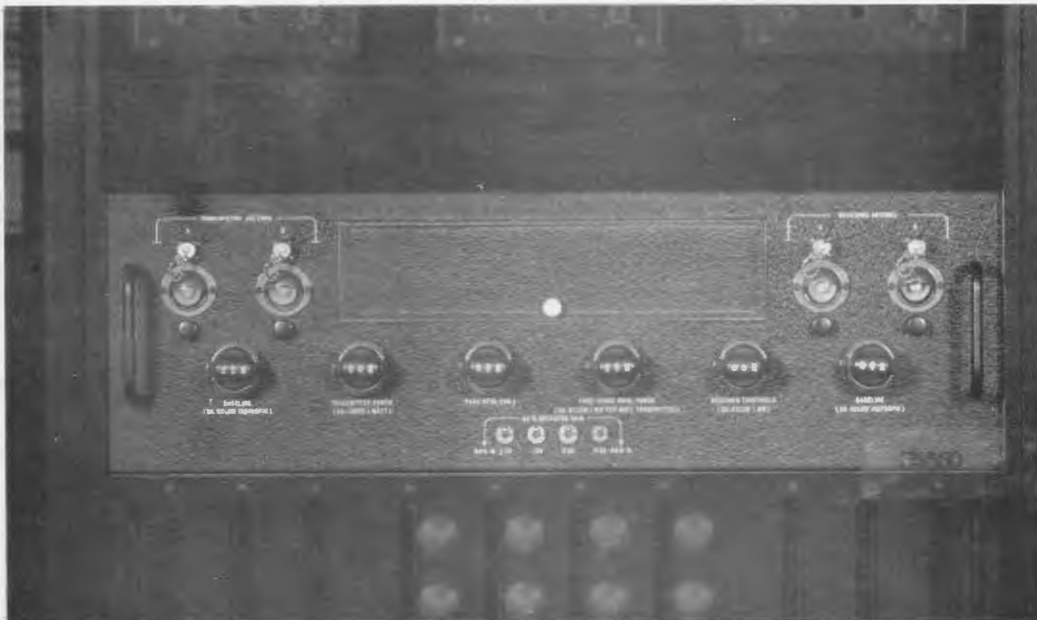


Fig. 25 - Amplitude unit (front panel)

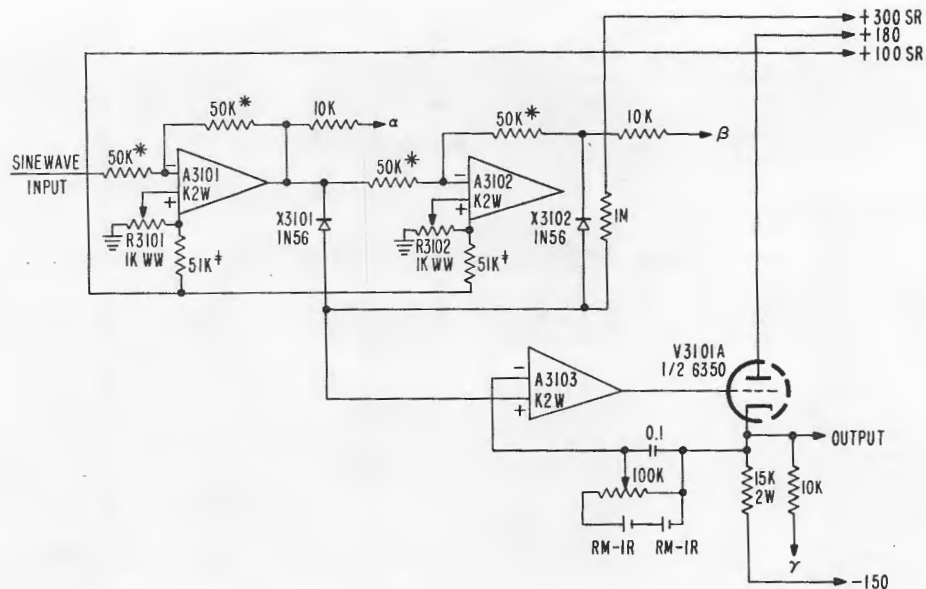


Fig. 26 - Full-wave rectifier

The peak of this output waveform is held to exactly -20 volts by adjusting the amplitude of the input sine wave. The output waveform is monitored by a peak voltmeter whose circuit diagram is given in Fig. 27. The junction of two precision resistors will be at ground potential when the instantaneous value of the input waveform is -20 volts; if the input is less negative, this junction will be above ground. Only if the peak value of the waveform is more negative than -20 volts, will the junction be negative. Note that at this point the ac waveforms are referenced to the +100 SR supply, which is a priori correct.

Temporarily neglecting X3201 and X3203, it appears from the previous discussion that if X3202 were perfect, an ac signal would appear on the anode of X3202 if, and only if, the peak negative value of the input waveform was more negative than -20 volts. Since X3202 does not have infinite back impedance, X3203 is necessary to eliminate the ac signal that would be caused by reverse current through X3202. Finally, X3201 is employed to prevent the appearance of a large signal on the cathode of X3202, which might be coupled to its anode through the relatively high capacity of a junction diode.

Any ac signal that appears on the anode of X3202 is amplified by V3201 and displayed as fuzziness on the face of V3202. R3201 merely adjusts the steady-state shadow angle. To use the voltmeter, the amplitude of the output of the sine-wave generator is advanced until fuzziness appears on V3202, and then retarded until it just disappears.

The remaining circuitry in the Amplitude Unit is concerned with the generation of the amplitude gate. The requirement for this gate is simply

$$P_r \geq R_p$$

where  $P_r$  = received power in mw, and

$R_p$  = receiver threshold in mw.

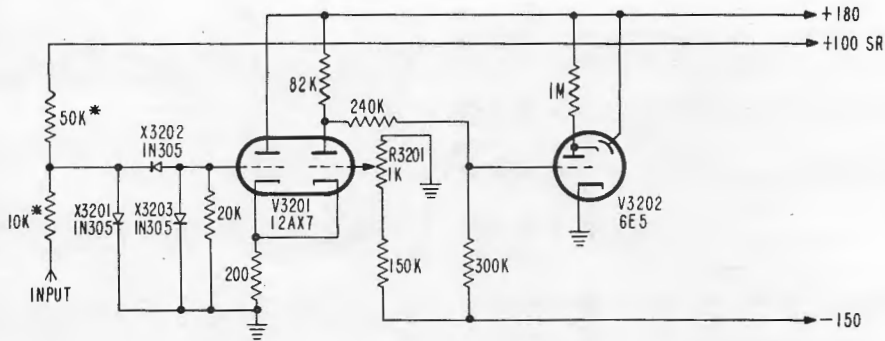


Fig. 27 - Voltmeter

We realize that

$$P_R = P_t \times FS \times P \times A_t \times A_R$$

where  $P_t$  = transmitted power in watts,

$FS$  = received power in mw per watt transmitted at the given range according to the free-space attenuation law, and assuming isotropic antennas,

$P$  = additional path gain not predicted by the free-space law,

$A_t$  = transmitter antenna gain relative to isotropic, and

$A_R$  = receiver antenna gain relative to isotropic.

If we now let lower case letters represent decibel quantities, the multiplications become additions, the amplitude gate requirement becomes

$$P_R \geq r_p$$

where  $p_R$  = received power in db above 1 wm, and

$r_p$  = receiver threshold in db above 1 mw.

$$P_R = p_t + fs + p + a_t + a_R$$

where  $p_t$  = transmitted power in db above 1 watt,

$fs$  = received power, in db above 1 mw, per watt transmitted, assuming the free-space law and isotropic antennas,

$p$  = additional path gain, in db, not predicted by the free-space law,

$a_t$  = transmitter antenna gain in db above isotropic, and

$a_R$  = receiver antenna gain in db above isotropic.

Reversing the sign of some of the quantities, and indicating this reversal by underlining, we have

$$-p_R = p_t - \underline{fs} - \underline{p} - \underline{a_t} - \underline{a_R}$$

and the threshold condition becomes

$$\underline{r_p} - \underline{p_r} \geq 0$$

which yields as the threshold condition utilized by the simulator

$$\frac{G(\theta)}{r} + \frac{G(\theta)}{r} + \underline{r_p} + (\underline{p_t} - \underline{f_s} - \underline{p} - \underline{a_t} - \underline{a_r}) \geq 0$$

where  $\underline{r_p}$  = receiver threshold in db below 1 mw,

$\underline{p_t}$  = transmitted power in db above 1 watt,

$\underline{f_s}$  = received power, in db below 1 mw, per watt transmitted, assuming the free-space law and isotropic antennas,

$\underline{p}$  = additional path attenuation in db,

$\underline{a_t}$  = transmitter antenna gain in db below isotropic, and

$\underline{a_r}$  = receiver antenna gain in db below isotropic.

positive voltage

negative voltage

Thus if the first two quantities are represented by positive voltages, and the last four by negative voltages, testing the sign of the sum of the six voltages will indicate whether or not the amplitude conditions are fulfilled.

It should be noted that  $\underline{a_t}$  and  $\underline{a_r}$  represent the gain of the deepest nulls of the antenna patterns. Therefore it is necessary to add to the sum of the six voltages the antenna patterns, which represents the instantaneous gains of the antennas relative to their nulls, before testing for fulfillment of the amplitude condition.

Figure 28 shows the circuitry which imposes the amplitude conditions. The time-independent conditions are set on R3301-R3306, each of which is a ten-turn helical potentiometer. A scale factor of 1 db/volt is used with these potentiometers, so a turns-counting dial reads directly in db. Increasingly positive voltages on these potentiometer arms imply fulfillment of the amplitude conditions. The sum of these voltages is inverted and divided by 3 by the loop consisting of A3301 and V3301, stabilized by A3302. Thus at the output of V3301 a negative voltage represents fulfillment with a scale of 3 db/volt.

Since this is the same scale as the output waveform of the Antenna Pattern Generator it can be directly added to the APG output in the squaring circuit as is shown in Fig. 29. The sum is amplified and inverted by A3401, which is stabilized by A3402. X3401 and X3402 prevent the dynamic range of A3401 from being exceeded, thus guarding against the accidental breaking of the stabilizing loop. At the output of A3401, a voltage above ground indicates the fulfillment of all amplitude conditions and the necessity of generating the amplitude gate.

Operating experience has tended to show that the threshold of a receiver is not a constant value but is itself a probabilistic matter. The threshold set in the circuit of Fig. 28 may be thought of as the sure threshold. At the scale of  $67 \mu\text{a/db}$  existing in Fig. 29, the toggle switches may be thought of as improving the threshold by an amount up to 7.5 db, controllable in 1/2-db steps. This "operator bias" represents the difference between the signal strength which assures operator recognition (set on R3305) and the signal strength which is detected 50% of the time. The biased signal is amplified and inverted by A3403, which is stabilized by A3404. X3403 and X3404 prevent the signal from exceeding the dynamic range of A3403.

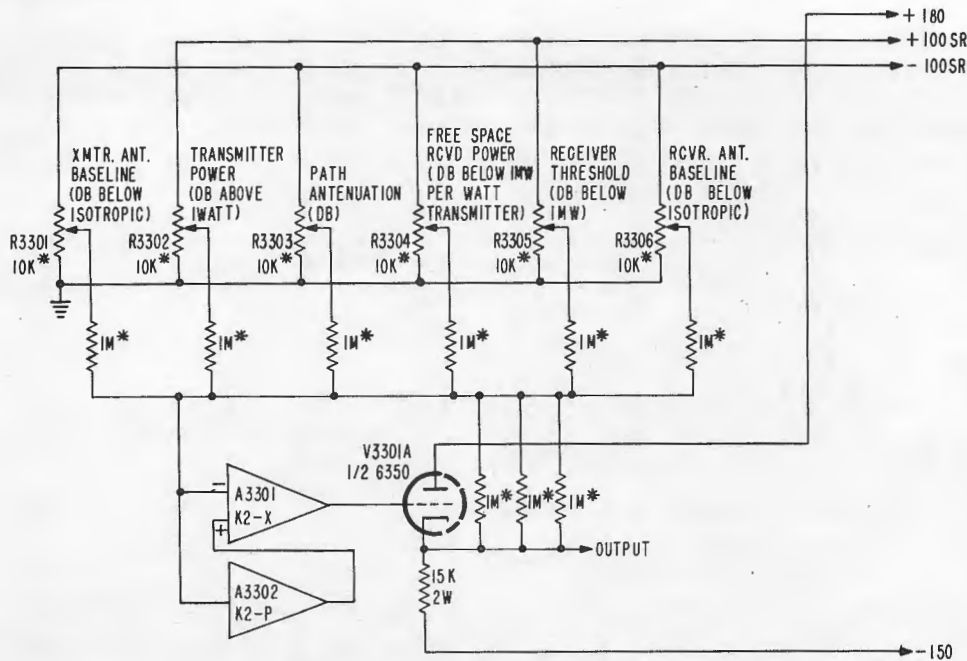


Fig. 28 - Amplitude reference generator

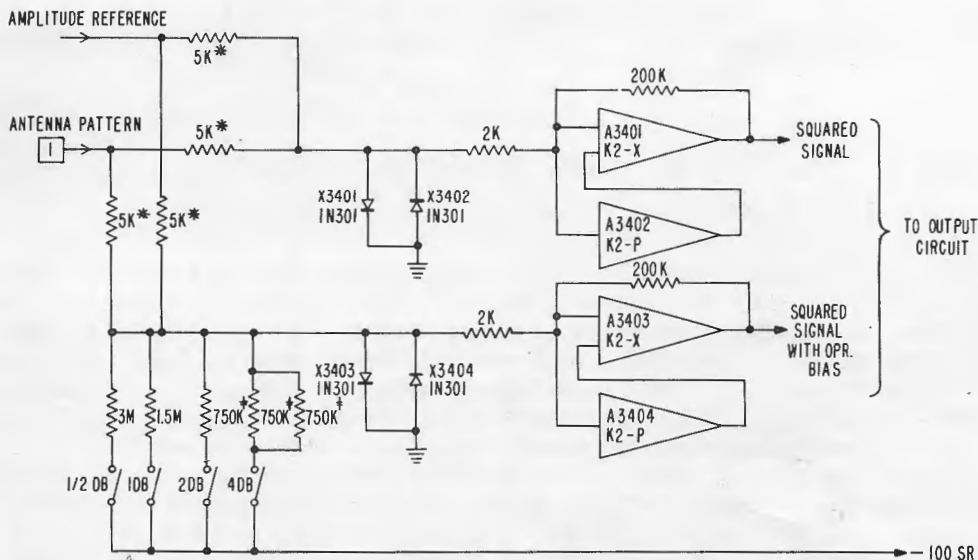


Fig. 29 - Squaring circuit



  
STATUS OF THE COMPUTER SYSTEM

With the completion of construction of this simulator in November 1956 there became available for the first time a means of rapidly and accurately computing countercept probabilities. As of this writing, one problem has already been analyzed by the computer system with significant results that are reproduced elsewhere.\*

The program for future use of the countercept computing system is being kept sufficiently flexible to allow consideration of interesting or urgent problems as they arise. Present plans call for two general types of computation — evaluating and optimizing specifications of proposed countercept systems, and gathering quantitative effectiveness data on existing systems for the formulation of operating doctrine.

Since the computing facility represents a considerable investment in funds and manpower and is sufficiently flexible to handle a wide variety of countercept problems, it is hoped that it will be possible to make the facility accessible to other activities.

In this connection it should be pointed out that, in common with all computers, this facility will give useful answers only if the proper questions are asked and if sufficient data are supplied. At the present time the most serious limitation in the utilization of the system is the lack of 360° antenna patterns. As these become more generally available, the range of problems amenable to computation will be correspondingly increased.

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\*Wald, B., and Christman, D. B., "A Comparison of Omnidirectional and Rotating Directional Antennas for Intercept" [U], NRL Report 4905 (Secret), 25 February 1957

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