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THESIS

CONTROL METHODS TO MITIGATE COMMON MODE EMI AND REDUCE SWITCHING LOSSES IN GRID-CONNECTED INVERTERS

by

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Three-phase four-leg voltage source inverters that use pulse density modulation achieve simultaneous commutation of the switching devices on each inverter leg. This switching scheme should result in the elimination of common mode voltage within the circuit; however, the presence of dead-time during the commutation of the switches results in the generation of some common mode voltage events. In this thesis, a software-based approach to compensate for the common mode voltage generated during dead-time has been simulated and experimentally validated. The novel compensation strategy reduces the amplitude of the common mode spikes and ensures robust compliance with the conducted electromagnetic interference requirements in MIL-STD-461G for naval ship applications. Benefits arising from this research are considerable as this software compensation method reduces electromagnetic interference and common mode voltage typically generated by three-phase power converters and drastically reduces the size of the common mode filter required to meet the limits in the military standard. By eliminating the common mode choke and reducing the need for filters, the power converter will have decreased weight and volume, which are critical for shipboard applications.

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CONTROL METHODS TO MITIGATE COMMON MODE EMI AND REDUCE SWITCHING LOSSES IN GRID-CONNECTED INVERTERS

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Three-phase four-leg voltage source inverters that use pulse density modulation achieve simultaneous commutation of the switching devices on each inverter leg. This switching scheme should result in the elimination of common mode voltage within the circuit; however, the presence of dead-time during the commutation of the switches results in the generation of some common mode voltage events. In this thesis, a software-based approach to compensate for the common mode voltage generated during dead-time has been simulated and experimentally validated. The novel compensation strategy reduces the amplitude of the common mode spikes and ensures robust compliance with the conducted electromagnetic interference requirements in MIL-STD-461G for naval ship applications. Benefits arising from this research are considerable as this software compensation method reduces electromagnetic interference and common mode voltage typically generated by three-phase power converters and drastically reduces the size of the common mode filter required to meet the limits in the military standard. By eliminating the common mode choke and reducing the need for filters, the power converter will have decreased weight and volume, which are critical for shipboard applications.

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List of Acronyms and Abbreviations

AZSPWM	active zero state pulse width modulation
AC	alternating current
CE	conducted emission
CM	common-mode
CMV	common mode voltage
CHiL	control hardware in the loop
DC	direct current
DER	distributed energy resource
DM	differential-mode
DOD	Department of Defense
DPWM	discontinuous pulse width modulation
EDM	electric discharge machining
EMI	electromagnetic interference
EUT	equipment under test
FET	field effect transistor
FPGA	field programmable gate array
HDL	hardware description language
IGBT	insulated-gate bipolar transistor
ILA	integrated logic analyzer

IO	input output
LISN	line impedance stabilization networks
MOSFET	metal oxide semiconductor field effect transistor
MPC	model predictive control
NPS	Naval Postgraduate School
NSPWM	near state pulse width modulation
PDM	pulse density modulation
PWM	pulse width modulation
SiC	silicon carbide
SVM	space vector modulation
SVPWM	space vector pulse width modulation
THD	total harmonic distortion
USN	U.S. Navy
VIO	virtual input output
VSI	voltage source inverter

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Gloria in Excelsis Deo

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CHAPTER 1:
Introduction

This chapter explains the historical motivation behind the research and why it is relevant for today. An outline of the thesis is also included with a brief discussion of the importance of power electronics.

1.1 Research Rationale

The Navy and the Marine Corps have continuously worked in tandem for hundreds of years to protect and serve the nation. This relationship will prove invaluable in the next armed conflict and will require further cooperation for planning and development of military equipment, strategy, and manpower. Based on recent Force Design guidance, the Marine Corps is preparing itself for the next fight through multiple courses of action. Such actions include an increased focus on amphibious warships, unmanned aerial vehicles, and on command and control of forces across a distributed landscape [1]. This emphasis requires renewed attention to the Navy and Marine Corps partnership and a full-fledged return to the amphibious roots of the Corps. This re-emphasis requires a complex capability set of technology that can make or break our ability to wage war and command and control at sea. If not properly accounted for, military technology can be degraded or even destroyed through interactions with electromagnetic interference (EMI). Notable examples of EMI affecting military equipment can be seen in the rocket detonation on the USS Forrestal and the sinking of the HMS Sheffield. Both situations represent the significant dangers of EMI and how it can affect naval forces. In the situation of the USS Forrestal, the presence of EMI resulted in the accidental misfire and rocket detonation of a F-4 Phantom that killed 134 personnel. In the case of the HMS Sheffield, the presence of EMI between satellite communications and radar equipment meant that only one or the other could operate at any one time. This was a critical vulnerability that led to its sinking during the Falklands War. During satellite communications, the ship disabled its missile radar system that left it vulnerable to incoming enemy missiles that led to its destruction and ultimate sinking [2]. Both of these examples represent a fraction of the EMI incidents that the U.S. Navy and allied navies have experienced. However, these historical examples highlight the dangers

of neglecting proper EMI mitigation measures that are necessary to keep our military and equipment safe from accidental mishaps. Like the Navy, the Marine Corps also understands the importance of EMI and how it affects communications and command and control of military units in a dense technological environment. The presence of increasingly sensitive and complex technology paired with similar mishaps as the ones previously described, has led to the problem of dealing with EMI. This EMI problem is particularly troublesome to Marine Corps communication equipment, which may degrade or jam friendly assets [3]. This problem is not strictly limited to one electronic equipment set over another. There exist numerous equipment assets from communication gear to power generation and transmission assets that may produce and/or experience the effects of EMI.

It is the author's personal experience in planning and establishing operating bases that emphasize the importance of electronic assets to leadership personnel. Communication equipment, power generation and storage, and even power transmission lines all represent sources of EMI and recipients of its interference from both military and civilian equipment alike. To compensate, additional spacial considerations are typically applied. However, this is not always feasible due to the physical space military equipment is capable or allowed to occupy. Thus, these restrictions that exist at a given location necessitate the co-location of equipment that has the potential to interfere with one another. This co-location may lead to the degraded ability of Marines to accomplish their mission in a distributed environment. As a result, it is imperative to plan with these EMI considerations in mind and ensure that the mishaps similar to the HMS Sheffield and USS Forrestal do not find their way onto Marine Corps outposts as well. These historical events and the author's personal experience inspired this research to mitigate EMI in hopes of advancing our war fighting capability, and minimizing this danger for future operations. This mindset is all the more important as the proliferation of capable electronic equipment becomes the mainstay to the battlefield of the future. As the Marine Corps continues to work with the U.S. Navy in a greater degree for the future fight, the need to mitigate EMI will continue to be a top priority to ensure that combat systems continue to function in a congested electromagnetic environment as well as a contested spacial environment on or off a ship. In this thesis, a software approach to mitigate EMI on a power inverter will be presented as a solution to reducing the interference of local power distribution systems.

1.2 The Importance of Power Electronics

Power electronic converters are electronic systems which control the conversion of electrical power from one form to another, such as alternating current (AC) to AC at different voltage and/or frequency, AC to direct current (DC), DC to AC or DC to DC at different voltages. This conversion process is extremely useful in shipboard power production and distribution, as well as microgrid applications that are more pertinent to Marine Corps basing operations in remote areas. For the Navy, ships require electrical power for their loads, electronics and military equipment, as well as lighting and signaling items aboard the ship. For these electrical loads there are various power requirements ranging from a few watts for a simple light bulb to hundreds of watts or kilowatts for high powered radar and other applications. Likewise, Marine operations have various power requirements in remote places to support their expeditionary facilities through various solar, wind, and traditional diesel power generation sources. Power electronics and more specifically power converters bridge the gap between the power generation sources and the loads that require the power. On a ship, large gas turbines are used to turn mechanical energy into electrical energy that is then converted from high voltage AC to lower voltage AC or AC to DC. Likewise, Marines require the use of power converters to manage the power that is generated from their diesel generators, solar panels, and/or batteries to produce the 120 V at 60 Hz required for the majority of their equipment.

Inverters are power converters that convert DC to AC and they can be single-phase or three-phase depending on whether their AC output is single-phase or three-phase respectively. Further, inverters connected to an AC distribution bus either on a ship or at the point of connection to the utility grid can be grid-following or grid-forming; the former operates in current control mode while following the grid voltage, while the latter operates in voltage control mode. This thesis focuses on grid-following three-phase inverters, which are widely used onboard ships as well as in land-based microgrids.

1.3 Research Principles and Outline

This thesis will focus on a software approach to mitigate EMI and common mode voltage (CMV) generation in a power converter. Power converters aboard Navy ships, as well as those used in microgrid applications require passive filters to mitigate the EMI and CMV

that they produce. As a result, this research will focus on the reduction of the CMV with a software based approach through the control hardware of a grid-following three-phase inverter. The principal goal of this research is to demonstrate a noticeable reduction of the CMV and subsequent EMI mitigation that allows the system to comply with MIL-STD-1399 and MIL-STD-461. Both characteristics will be discussed in the following chapter as well as their relationship with this principal goal.

In order to cover this software approach, this document has been divided into seven chapters. Chapters 1 (Introduction) and 2 (Background research) introduce the reader to the topic and a brief background into its origins and discussion into previous research made into the topic. Chapters 3 (System Architecture and Novel Dead-Time Compensation), 4 (Control Software and control hardware in the loop (CHiL) Simulations), and 5 (Hardware Implementation) discuss the method and rationale behind the software approach used to mitigate CMV and EMI as well as the software tools and physical equipment used to implement this approach into the circuit. Finally, Chapters 6 (Results) and 7 (Conclusion and Future Work) will cover the outcome of this approach and document the benefits of implementing this approach in similar power inverter circuits that may be used in Navy ships and/or Marine Corps microgrid equipment.

1.4 Thesis Goals

As the Marine Corps and the Navy continue to work in tighter cooperation with one another, the need to mitigate EMI will continue to be a notable concern. Methods that are effective in mitigating EMI will prove necessary to win the technology dependent fight of the future. To help win this fight, this thesis introduces a method to reduce EMI and CMV in three-phase inverters. The proposed method can reduce the cost and volume of power converter systems while enhancing their compliance with military standards. In short, it is the hope of this author to contribute to the field of study that prevents situations like those experienced on the HMS Sheffield and USS Forrestal from ever occurring again.

CHAPTER 2:
Background Research

In this chapter, EMI and CMV in power converters are introduced. Negative effects of CMV including physical damage to the electrical circuits are discussed. Previous work and the relevant military standards are also presented.

2.1 EMI and CMV

Power electronic equipment in the form of power inverters, converters, and motors are a prime source of EMI within a circuit. They can also be recipients of EMI and suffer from its negative effects such as decreased performance or physical damage to the circuit. EMI is typically categorized as either conducted or radiated and requires various shielding and filtering methods to mitigate its intrusive properties within the circuit [4]. Both forms of EMI are addressed in MIL-STD-1399 and MIL-STD-461 which will be discussed in detail later in this chapter. In regards to conducted EMI, there are two types known as differential-mode (DM) and common-mode (CM). DM refers to the noise relationship between each individual line, while CM refers to the noise relationship between the individual lines and a common ground. Both CM and DM can be with respect to voltage or current [4]. Equation (2.1) shows how the CMV V_{cm} is measured in a three-phase voltage source inverter (VSI) [5].

$$V_{cm} = \frac{V_a + V_b + V_c}{3} \tag{2.1}$$

In the equation, each voltage represents the phase voltage of each leg of the inverter with respect to ground. Ideally, designers of a power converter circuit would like this voltage term to be zero; however, this is impossible with a three-leg inverter, and the presence of CMV can introduce harmful effects in the circuit. There are other contributing factors to the generation of EMI within a circuit. The inverter itself experiences voltage and current transients from high to low and vice versa. These voltage and current transients depend on the characteristics of the switching devices and contribute to the generation of EMI within the circuit [6]. Switching semiconductor devices, such as the insulated-gate bipolar

transistor (IGBT) and the metal oxide semiconductor field effect transistor (MOSFET), are key components for the design and functionality of power converters. It is well known that each device has its respective trade-offs that make one device a better choice than the other depending on the application. For example, IGBT switching devices are capable of high voltage applications typically greater than 1000 V. Additionally, they operate at a relatively low switching frequency ranging from a few hundred hertz to a few thousand hertz due to their intrinsic high switching losses. On the contrary, MOSFET devices can work at a much higher switching frequency, e.g., tens or even hundreds of kilohertz, with the penalty of higher conduction loss especially at close to full load operation conditions. However, the performance of modern MOSFET devices, especially with the advanced wide bandgap materials, have improved considerably and are rated at higher voltages than previous generations of the same device. Thus, the MOSFET is a desirable switching device to be used in low power converter circuits based on its high switching frequency and conduction loss performance; however, it causes fast transition or high dv/dt which leads to common mode noise generation within the circuit [7].

The negative effects of EMI within a circuit have been known in the electrical engineering community for years and can affect various systems depending on the circuit and the associated components. As an example, inverters in motor drive applications cause large dv/dt transitions which lead to harmful common mode currents flowing through the motor windings, shaft, and bearing components. These large voltage transitions can increase in magnitude until they are capable of overcoming the resistance of the air and grease that surround these motor windings to cause a flash-over current. This current over time will perform a process known as electric discharge machining (EDM) which can cause pitting or fluting on motor components [8], [9]. Figure 2.1 and Figure 2.2 provide a visual depiction of an adjustable speed drive circuit connected to a pulse width modulation (PWM) inverter, as well as the mentioned damage caused by conducted EMI emissions.

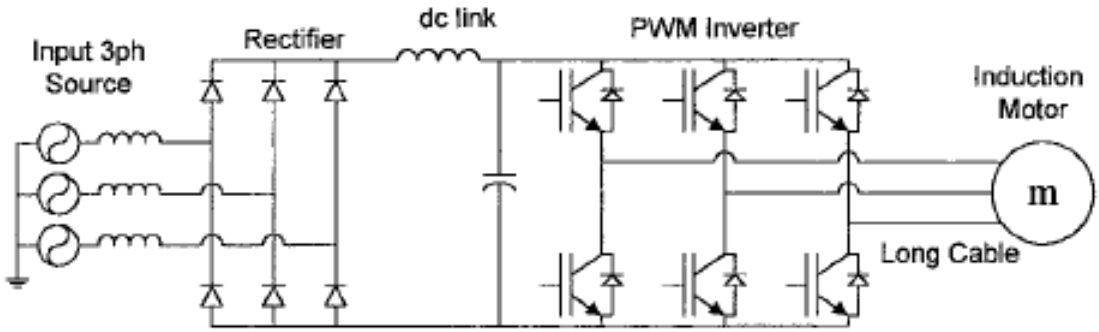

Figure 2.1. Typical adjustable speed drive system. Source: [8].

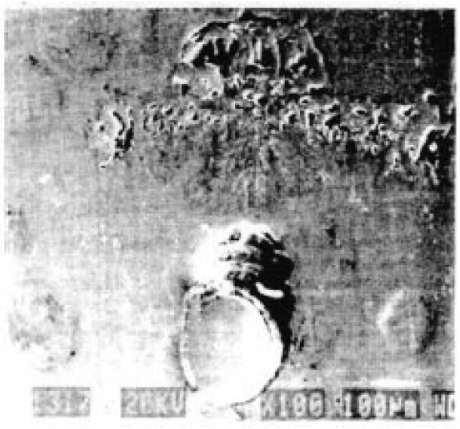

Figure 2.2. EDM pitting damage due to nearing current. Source: [10].

From the perspective of the Navy, these PWM inverters present a design challenge due to their generation of EMI as well as the size and weight of the filters that are necessary to attenuate interference. Technologies such as variable speed drives that may benefit Navy ships are unable to be widely implemented due to EMI generated from the power electronic

circuits associated with their use [11]. If the technology were to be implemented aboard U.S. Navy ships, they would face weight, space, and EMI obstacles that must be addressed. In an example application, a 450 hp electric motor would require a harmonic filter weighing 2700 lbs occupying nearly ten square feet of deck space just to meet military standards for EMI [11]. This represents a waste of valuable space and weight allocations on a ship that could be better addressed towards other military applications or needs. As a result, the use of passive filters alone is not the favorable solution to reducing EMI and represents a substantial area of improvement for reducing EMI and CMV. It does indicate that certain technology that might be beneficial to the Navy has been excluded from use due to the corresponding weight requirements of components needed to make that technology fit for use. In Table 2.1 we see the impact of the weight requirements necessary to meet the EMI requirements for the MIL-STD-461. In this table, the filter components when compared to the proposed EMI reduction method represent a significant increase in both space and weight requirements. As a result, it is critical to implement such methods in order to effectively meet the proposed military standards without said filters. The next section will focus on the methods that are currently used to address this problem as well as provide insights into the method proposed by this thesis.

Table 2.1. Inverter and weight ratings for EMI filters. Source: [12]

Inverter Rating (kW)	4th Pole Components		EMI Filter Components		% Size/Weight Reduction	
	cm^3	kg	cm^3	kg	% Size	% Weight
75	2323	5	2821	12	18	58
100	2999	11	3466	15	13	27
200	5703	17	11209	47	49	63
250	7055	24	13790	58	49	59
500	13770	80	26695	112	48	29

2.2 Common Mode Voltage Elimination Techniques

Multiple methods of eliminating EMI and CMV within a circuit have been studied with various results indicating respective tradeoffs that must be taken into account depending on the circuit applications. Nearly all methods involve the use of PWM, space vector

modulation (SVM) which is a type of PWM, and more recently, pulse density modulation (PDM) modulations methods that are implemented to improve characteristics of switching and control technology.

PWM is a well-known method used to control the switching devices within an inverter. It is typically accomplished through the comparison between a reference waveform which has the shape of the output that needs to be synthesized, and a carrier waveform which dictates the switching speed. The resulting PWM switching waveform is a train of pulses with the duty cycle determined by the comparison between the carrier and the reference signal. In a VSI, for each inverter leg, when the switching waveform is high, the top switch is turned on and the bottom switch is turned off, while the opposite happens when the switching waveform is low. An alternative to the carrier-based PWM is SVM which is accomplished in digital controllers through mathematical transformations. PDM is used in this thesis and will be presented in Chapter 3. It is important to note that while these different modulation strategies exist, there are similarities in performance that make the decision to use one method over another the choice of the designer and end user, as well as the specific constraints applied to the use of the circuit. For example, the use of PWM and SVM results in no difference between the two strategies that is the result of their innate qualities when regularly sampled [13]. Sampling of reference voltage and phase voltage can be a method to improve performance of either modulation strategy with respect to the technology used. The use of new technology such as the field programmable gate array (FPGA) allows the designer and user to vary the modulation method to improve performance. Such an improvement can be seen in Figure 2.3 where a digital implementation of SVM using an FPGA can be seen. In this example, a update scheme of approximately one update per chosen switching period that is normally associated with an SVM inverter is now sampled 20 times during the same period [14].

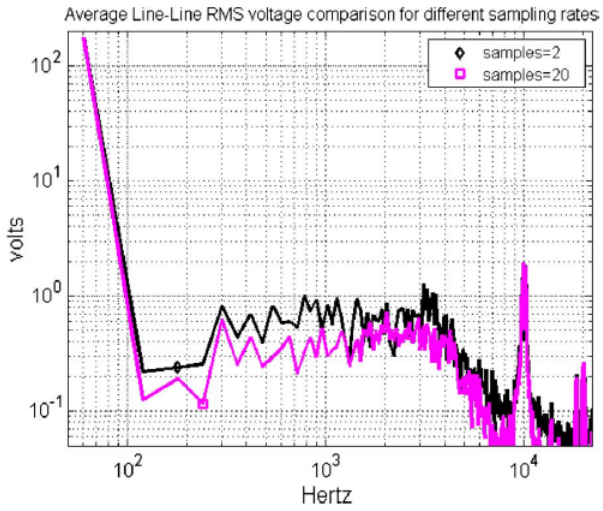

Figure 2.3. "Measured spectra of the line to line rms voltage." Black line denotes a total harmonic distortion (THD) of 2.54 percent with the magenta line having a THD of 1.71 percent. Source: [14].

This improvement in THD is the direct result of additional technology complimenting the use of pre-existing modulation methods to improve performance. In this example, the THD improvement is the result of the FPGA being able to sample the signal multiple times during a period in order to enact the desired change through the re-computation of the space vector timer [14]. The incorporation of a relatively new piece of technology, the FPGA, represents an approach to improving performance and reducing EMI using new tools and evaluation methods that were previously difficult to implement or imagine. Using hardware description language (HDL) to control the FPGA represents an inexpensive way to improve performance without increasing financial or material requirements.

2.2.1 Three-Phase Four-Leg Inverter Configuration

Typical three-phase inverter configurations have three legs as the one seen in Figure 2.1. The inverter output can be attached to three-phase balanced or unbalanced AC loads, a motor, or it can be connected to the main grid, in which case the inverter operates in current control mode. An alternative configuration for this three-phase inverter is the four-leg inverter in

which a fourth leg is added as shown in Figure 2.4. The addition of the fourth leg has the added benefit of delivering unbalanced currents away from the AC source, which causes the source to not see the unbalanced load [15]. Additionally, the presence of the fourth leg can eliminate the CMV through the switching of inverter legs in pairs to counteract each other, as was originally demonstrated in [16]. In a traditional three-leg inverter system, the odd number of legs will each occupy a voltage space that is inherently off balance with one or more legs of the system. One leg may be connected to the positive DC bus (top switch on) while the other two legs may be connected to the negative DC bus (bottom switch on), causing a non-zero CMV, which is expressed by equation (2.1). The CMV can drive circulating currents at the inverter switching frequency, which in turn cause EMI that can lead to damage in the circuit, as discussed in the previous section.

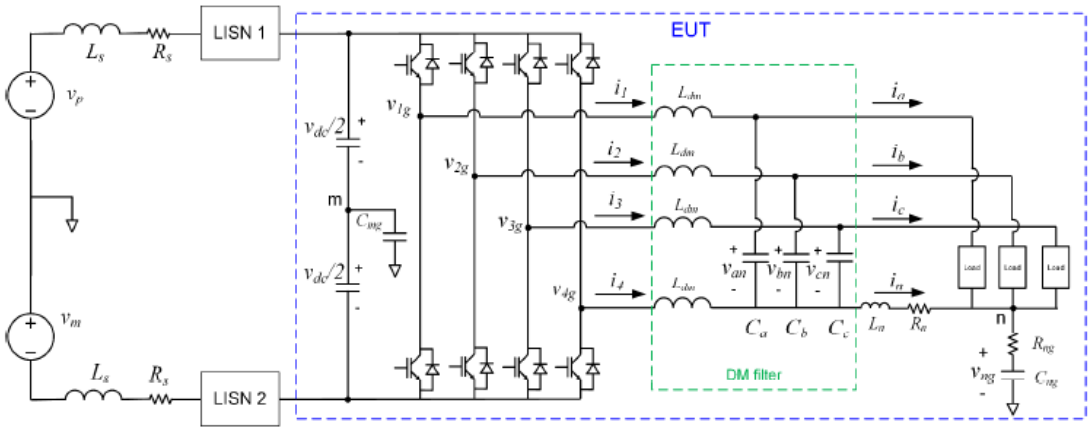

Figure 2.4. Three-phase four-leg inverter configuration. Source: [17].

Equation (2.2) defines the CMV V_{cm} for a four-leg three-phase inverter as a function of the pole voltages V_{xm}, with $x = 1, 2, 3, 4$, measured with respect to the midpoint of the DC bus m. When the top switch is on, the inverter pole voltage V_{xm} is equal to 0.5 V_{dc}, while V_{xm} is equal to -0.5 V_{dc} when the bottom switch is on. The CMV equation demonstrates that V_{cm} can be zero when two top switches and two bottom are on [15], [17]. This is further illustrated in Table 2.2.

$$V_{cm} = \frac{V_{1m} + V_{2m} + V_{3m} + V_{4m}}{4} \tag{2.2}$$

Table 2.2 demonstrates how the four-leg inverter generates the CMV based on the inverter switching states. If the top switch on a leg is on, then that leg is connected to the positive DC bus and the state for that leg is denoted by the letter p. In this case the leg voltage with respect to the midpoint of the DC bus V_{xm}, with $x = 1, 2, 3, 4$, is equal to half the DC bus voltage 0.5 V_{dc}. Likewise, if the negative leg of the inverter is connected to the negative DC bus rail, then the state of that leg will be denoted by the letter n and its voltage will be half of the negative DC bus voltage -0.5V_{dc}. Therefore, the switching states will result in some generation of CMV unless they are balanced. The desired states are those where no CMV is produced and involve switching states that balance one another out.

Table 2.2. Switching states for a four-leg inverter

State	nnnn	nnnp	nnpn	nnpp	npnn	npnp	nppn	nppp	pnnn	pnnp	pnpn	pnpp	ppnn	ppnp	pppn	pppp
CMV	$-0.5V_{DC}$	$-0.25V_{DC}$	$-0.25V_{DC}$	0	$-0.25V_{DC}$	0	0	$0.25V_{DC}$	$-0.25V_{DC}$	0	0	$0.25V_{DC}$	0	$0.25V_{DC}$	$0.25V_{DC}$	$0.5V_{DC}$

Any technique that would ensure a balanced switching event would, theoretically, eliminate the CMV generated. The elimination of the CMV generated by the inverter was demonstrated in literature with various modulation strategies, such as three dimensional PWM techniques including active zero state pulse width modulation (AZSPWM), near state pulse width modulation (NSPWM), space vector pulse width modulation (SVPWM), and discontinuous pulse width modulation (DPWM). These methods aim at reducing the CMV and the magnitude of the circulating currents within the inverter [18], [19].

AZSPWM utilizes active zero states, which substitutes (pnpn and npnp) for the zero state of the inverter and reduces the generated CMV by half [19]. Similarly, the use of the NSPWM and DPWM uses voltage states from "four neighbor active states (ppnp,pnnp,pnnn,pnpn)" in order to reduce the CMV output [19]. These methods work at the cost of higher switching losses, as a higher switching frequency is necessary to keep the same power quality. The use of these methods highlights the importance of the four pole topology of the inverter which makes effective use of the switching characteristics of the inverter to help mitigate the CMV output. However, most inverters have an additional issue that must be dealt with. Since

most inverters utilize a hard switching technique, the switches commute irrespective of the level or polarity of the current within the circuit. This will cause large voltage variations within the circuit that can generate conducted and radiated EMI [11]. To compensate, a current polarity measurement approach, as well as a purposeful control of dead-time of the switching events, can be used to improve CMV and EMI performance, as demonstrated in this thesis.

2.2.2 Dead-Time Compensation

Dead-time, or otherwise known as blanking time, is the time between switching events where both switches such as IGBTs or field effect transistor (FET)s are kept off to prevent a short circuit through the inverter DC bus. In this short circuit scenario, the upper switch and lower switch of the same leg would both conduct causing current to pass straight through the inverter. This can potentially damage or destroy the switches and the DC bus capacitors. To prevent this from occurring, dead-time is introduced so that when the state of the upper or lower switch changes, the corresponding switch on that leg is delayed slightly to block the current from passing straight through the inverter. A representation of dead-time can be seen in Figure 2.5 where the gate signals for switches T_A and T_B are separated by a purposeful delay or gap.

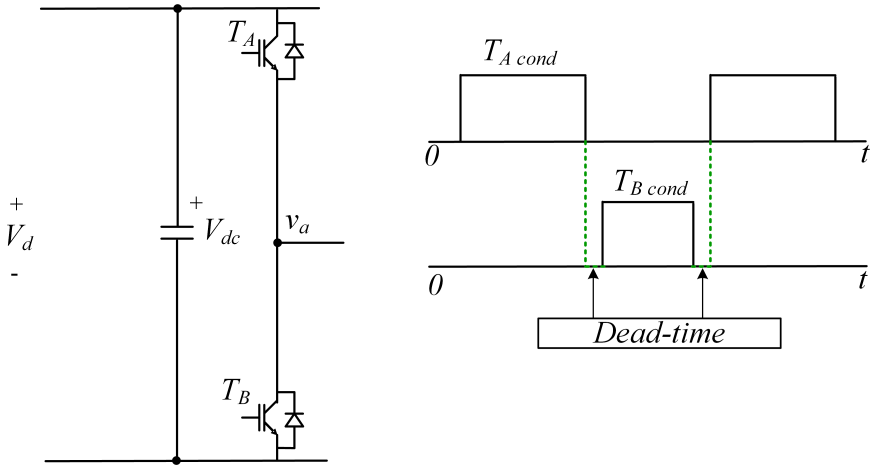

Figure 2.5. Dead-time representation.

Additional delays can also be introduced as well to allow for switching to take place at optimal moments of current direction that can reduce the generation of CMV. The use of current polarity sensing equipment and dead-time adjustment, needed in order to make switching decisions for the inverter, is another method to decrease CMV in PWM inverters [12], [20]. In [12] a four-leg multi-level inverter is studied with CMV and dead-time compensation based on the switching states of the converter, while in [20] the dead-time compensation is implemented using SVM on a three-leg inverter.

In this thesis dead-time compensation is proposed to reduce the inverter CMV using PDM, which, to this author's knowledge, has never been previously presented in literature. Additionally, the results of the proposed method are compared in the context of MIL-STD-1399 and MIL-STD 461 which consist of the stringent EMI rules that dictate tolerable limits and laboratory test conditions for evaluating EMI.

2.3 Military Standards

The military standards MIL-STD-1399 and MIL-STD-461G are referenced and utilized in this thesis. Both standards include requirements for electronic equipment to be utilized in military applications. Additional standards exist; however, for the purposes of this thesis only two will be discussed.

2.3.1 MIL-STD-1399

This standard encompasses the interface characteristics, tolerances, and test methods for electrical power systems that are used aboard military equipment [21]. Definitions for various terms associated with the testing of this equipment are also included in the description of "Type I Power" that is used aboard US Navy ships. Type I power as defined by this standard, is 440 or 115 V rms at 60 Hz and is interfaced with either three-phase or single-phase and is either ungrounded or solidly grounded [21]. Type II and Type III power also exist in this standard; however, they are not discussed or utilized in this paper.

2.3.2 MIL-STD-461G

This standard establishes the EMI testing and verification requirements as well as associated limits for electronic equipment [22]. This standard serves as the road map of how to set up

equipment for testing as well as provides limits that must be met for conducted and radiated emissions. For the purposes of this thesis, only conducted emission (CE) will be discussed. In Figures 2.6 and 2.7, the corresponding CE standards for current and voltage are displayed and will be used as the benchmark for evaluating the performance of the circuit to see if any measurable improvement is made using the current polarity and dead-time compensation method. Additionally, Figure 2.8 is used to demonstrate how the equipment must be setup in a laboratory for testing. Chapter 5 will present the laboratory setup for the equipment analyzed in this thesis, highlighting how it follows the guidelines in this military standard.

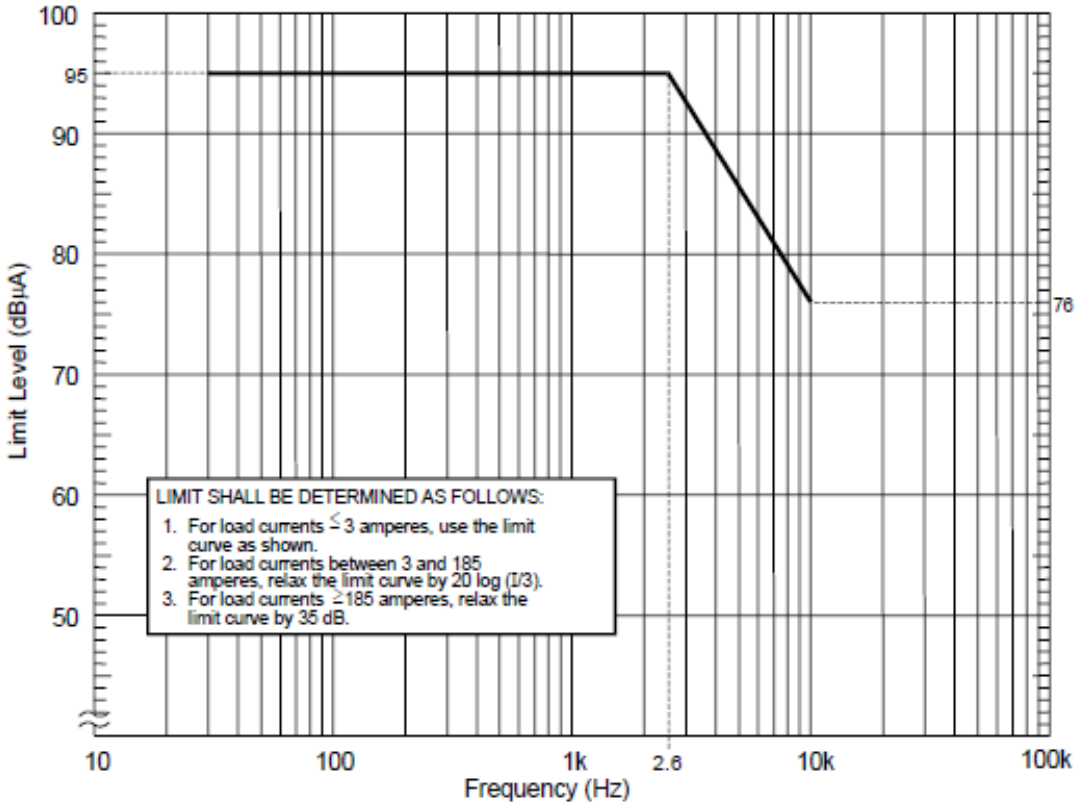

Figure 2.6. CE 101 limits. Source: [22].

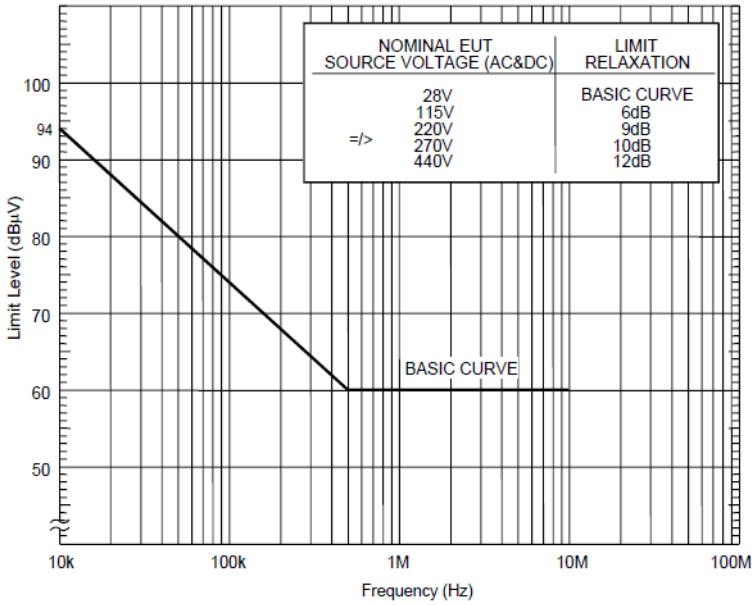

Figure 2.7. CE 102 limits. Source: [22].

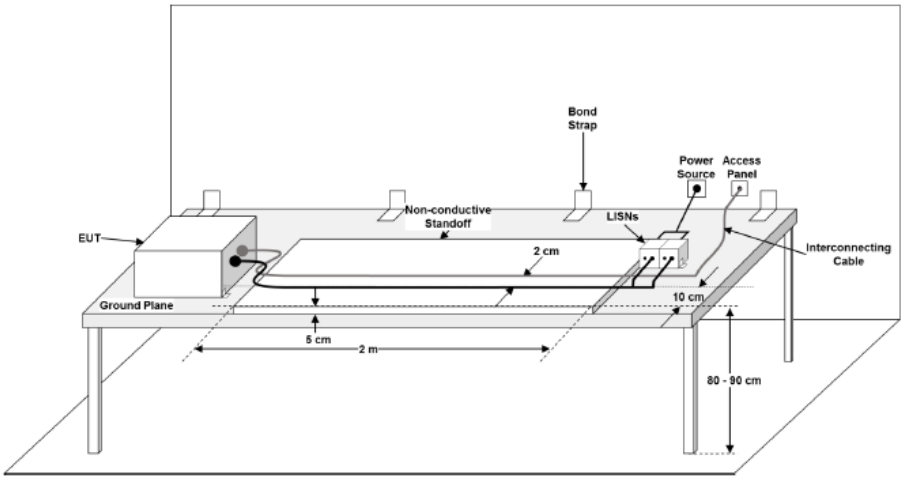

Figure 2.8. General setup of electronic equipment for testing. Source: [22].

CHAPTER 3:
System Architecture and Novel Dead-Time Compensation

This chapter includes the overview of the power converter architecture, control system, the CMV elimination method, and the novel dead-time compensation strategy.

3.1 System Architecture

The schematic in Figure 3.1 is a grid-connected three-phase four-leg VSI connected to a distributed energy resource (DER), which could be a renewable or conventional energy source or an energy storage system. The circuit includes a DM filter, but no CM filter, as the goal of this thesis is to demonstrate that the proposed CMV cancellation method eliminates the need for a CM choke. Four line impedance stabilization networks (LISN) are incorporated in order to comply with the requirements set in MIL-STD-461G [22]. Note the part highlighted as equipment under test (EUT) in Figure 3.1, is built to comply with the layout shown in Figure 2.8. The inverter modulation strategy and the specific CMV elimination are presented next.

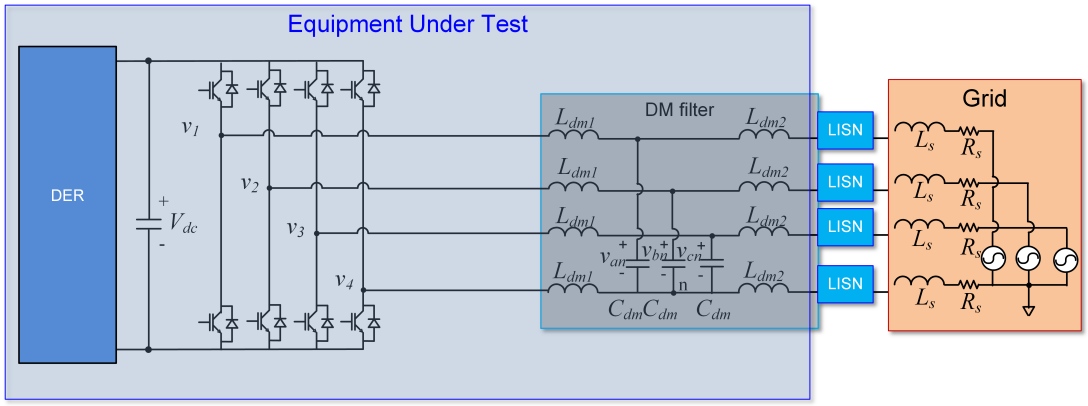

Figure 3.1. System architecture.

3.1.1 Controller and Modulation Strategy

The control system for the four-leg VSI is represented in Figure 3.2. PDM with delta modulation is used instead of PWM because the inverter is controlled in grid-following mode [15], [23]. In Figure 3.2, the four measured currents are compared to the reference currents and then the error signals are processed by the switch selection algorithm reported in [15]. While PWM uses pulses of different duty cycles to adjust the output voltage, the goal of PDM is to minimize the errors by selecting the appropriate switching states at each clock cycle. The benefit of using this method is the ability to eliminate CMV with the simultaneous switching of all the inverter legs [15].

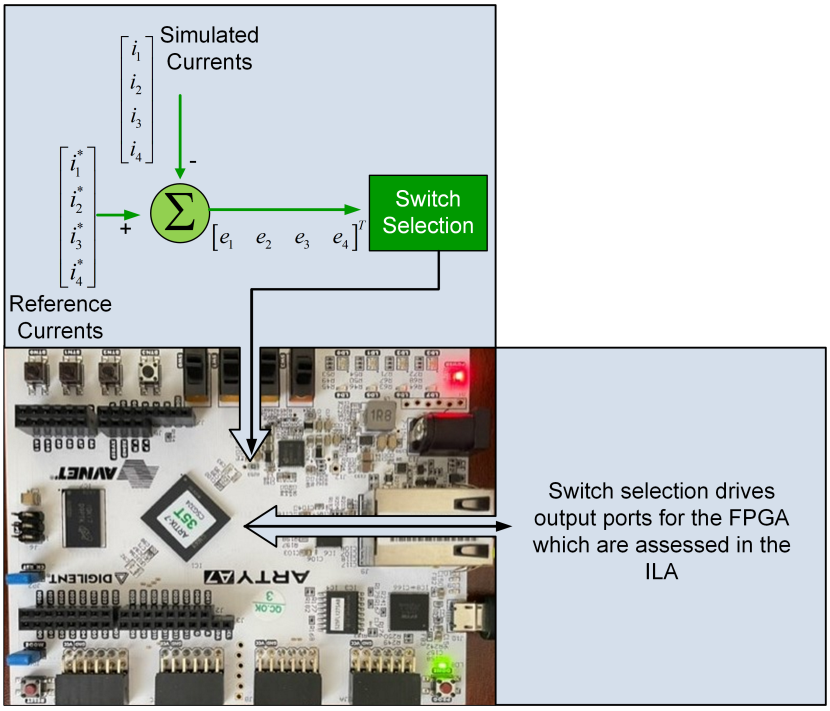

Figure 3.2. Control system for the four-leg VSI, implemented on an FPGA.

3.1.2 CMV Elimination

The use of PDM allows the VSI to switch in pairs simultaneously, so that two upper switches and two lower switches are always conducting. By switching the inverter legs in pairs, the voltages v_1, v_2, v_3, v_4 in Figure 3.1 ideally sum to zero. However, with the insertion of dead-

time as demonstrated in Figure 2.5, this momentary disruption in the commutation of the switches can lead to spikes in the CMV. This problem will be discussed in detail in the next section.

3.1.3 FPGA Implementation

The VSI control system is implemented into an FPGA without the need for additional control hardware, as depicted in Figure 3.2. When the FPGA board is connected to the laboratory hardware, the FPGA receives input from the current probes that measure the currents of each inverter leg. This measured current information is then compared to a specified reference current that is pre-programmed onto the board.

The proposed dead-time compensation method requires hardware validation; however, the control software can be first run and debugged through CHiL simulations to reduce the cost of the controller design process. During CHiL simulations, the board does not interface with current sensors and instead uses simulated currents from the physics-based model of the system implemented in the FPGA, as described in Chapter 4. This allows the user to check if the software has realized the designed switching algorithm.

Chapter 4 will discuss the process of CHiL development as well as the benefits with using the integrated logic analyzer (ILA) and virtual input output (VIO) components of Vivado. It is important to note that the use of the FPGA is conducive to the testing and evaluation of this method. Alternative control hardware for incorporating this method into VSIs include application specific integrated circuits that can be pre-programmed with the dead-time compensation method. These integrated circuits when produced in sufficient volume are cheaper than using an FPGA to accomplish the same task.

3.2 Novel Dead-Time Compensation Method

The dead-time compensation strategy is included in the diagram of Figure 3.3, where the four-leg inverter control system is illustrated. The entire controller is embedded into an FPGA and the dead-time compensation relies on the evaluation of the current polarity of each inverter leg to make switching decisions.

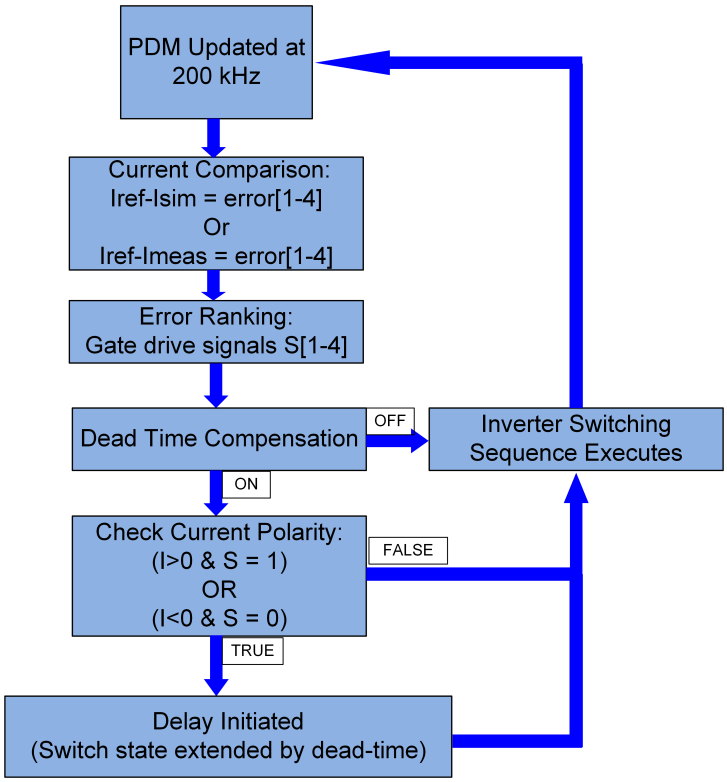

Figure 3.3. Dead-time compensation algorithm.

At the top of the diagram in Figure 3.3, 200 kHz is indicated as the PDM sampling rate, then the delta modulation controller is implemented in the following two steps where the current errors are computed and ranked from the greatest error to the least error, as described in the previous section. The outputs of the error ranking algorithm are the switching states for the four inverter legs; each can be either high or low depending on whether the top switch or the bottom switch is turned on, respectively.

In the next step, a flag is set to determine whether the user has enabled the dead-time compensation method. If the method is disabled, the switching signals will be sent to the gate drivers of the switch in order to correct the error. If the dead-time compensation is enabled, then the switching signals are used as inputs to the compensation algorithm, together with the current polarity for each of the inverter legs. If the current is positive (I>0), and the top switch is conducting (S=1), or the current is negative (I<0) and the top

switch is not conducting (S=0), the switch state will be extended by an interval of time equal to the dead-time. Alternatively, the FPGA will send to the gate driver of the switches the commutation signals as they were produced by the error ranking algorithm. By following these steps, the FPGA exerts control over the switching behavior of the inverter to ensure that the commutation of the switches occur with reduced CMV.

To visually demonstrate the inverter commutation process and how dead-time affects it, Figure 3.4 has been included to show four scenarios with different current polarities. The labels Ja4 and Ja3 represent the signals sent by the FPGA to the upper and lower switches of leg one of the inverters.

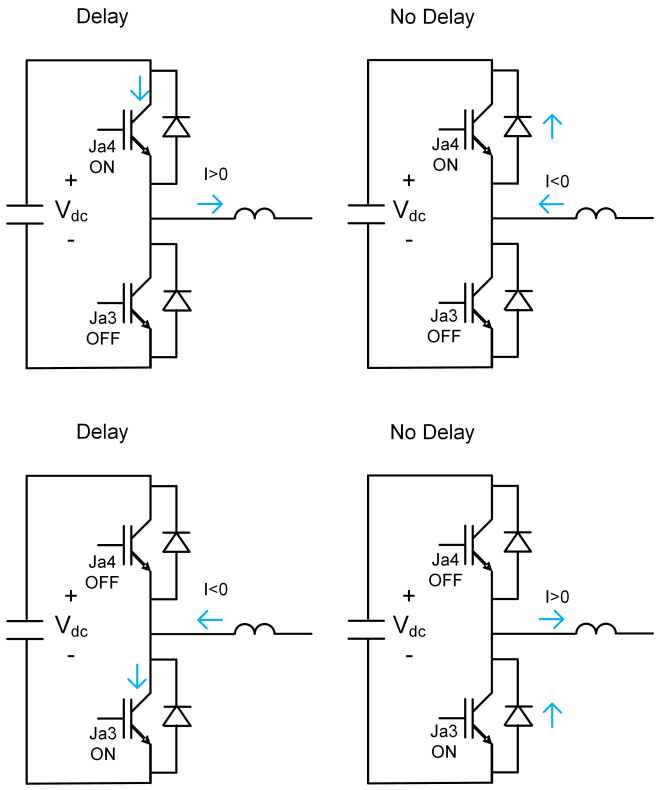

Figure 3.4. Leg one delay or no delay criteria.

In the first image located on the top left, the Ja4 switch is on and is conducting current while the Ja3 switch is off. The current flowing out of the inverter is positive, while it is

negative in the opposite case, shown by the image on the right. Using this information, the dead-time compensation portion of Figure 3.3 is implemented. Here, the delay condition is satisfied as the current is positive (I>0) and the switch state for the upper switch is on and conducting (S=1). This results in a delay equal to the dead-time being added to the signals sent from the FPGA to the gate drivers of the inverter.

On the top right of Figure 3.4, the current direction is flipped, making the current negative and flowing through the top diode. In this situation, the current is negative (I<0) and the upper switch is still on (S=1), which does not match the criteria necessary to initiate a delay. As a result, the delay is not required, and the switching signals are sent directly to the inverter.

The next example displayed in the bottom left-hand corner of Figure 3.4, has a negative current polarity (I<0) and the upper switch off (S=0) meaning it is not conducting. In this situation, the delay criteria are met and the delay is added in order to allow the current to commute through the switch.

The last image, depicted by the bottom right, does not meet the criteria for delay since the current is positive (I>0) with the upper switch being off (S=0). This results in current passing through the diode which does not require a delay in switching. Therefore, the switching signals are allowed to pass straight to the inverter.

The logic demonstrated in Figure 3.4, is applied to each leg of the inverter in order to ensure that the delay compensation method is initiated to allow current to commute through the switch before abruptly switching the leg. In Table 3.1, the explicit status of the switches and current is displayed to demonstrate its adherence to the dead-time compensation criteria and whether or not a delay should be initiated.

Table 3.1. Delay and leg criteria for VSI

Current Polarity	Upper Switch Status	Lower Switch Status	Compensation Criteria Met	Delay Initiated
Positive	On	Off	I>0 and S=1	Yes
Negative	On	Off	None	No
Negative	Off	On	I<0 and S=0	Yes
Positive	Off	On	None	No

To demonstrate how the compensation method affects the switching events, Figure 3.5 has also been included to display the timing of each switching sequence for two inverter legs. In this figure, the left two images show the results of the individual switching of two inverter legs and their switch commands without dead-time compensation. In this situation, the switching commands (swcmd3 and swcmd4) for legs 3 and 4 are plotted with purple lines. Once the command has been initiated through its transition from low to high for leg 3 and from high to low for leg 4, the voltage v_3 goes high on leg 3 and the voltage v_4 goes to zero on leg 4. This case meets one of the criteria for dead-time compensation in Figure 3.3 because the current is positive (I>0) and flowing through a switch (S=1) during the transition. The image on the right shows the effects of the dead-time compensation method for a similar switching scenario where the switching signal changes from low to high on leg 2 and from high to low on leg 4. Again, the criteria are met, so a delay is added on leg 4 since the current is positive and the upper switch is conducting. As a result of the dead-time compensation, the switching event for leg 4 is delayed in comparison with leg 2 pictured above to synchronize the two switching events. This delay reduces the CMV spike event and theoretically leads to increased compliance with the military standards. To test this method, a series of simulations and software development steps are performed, which will be covered in Chapter 4.

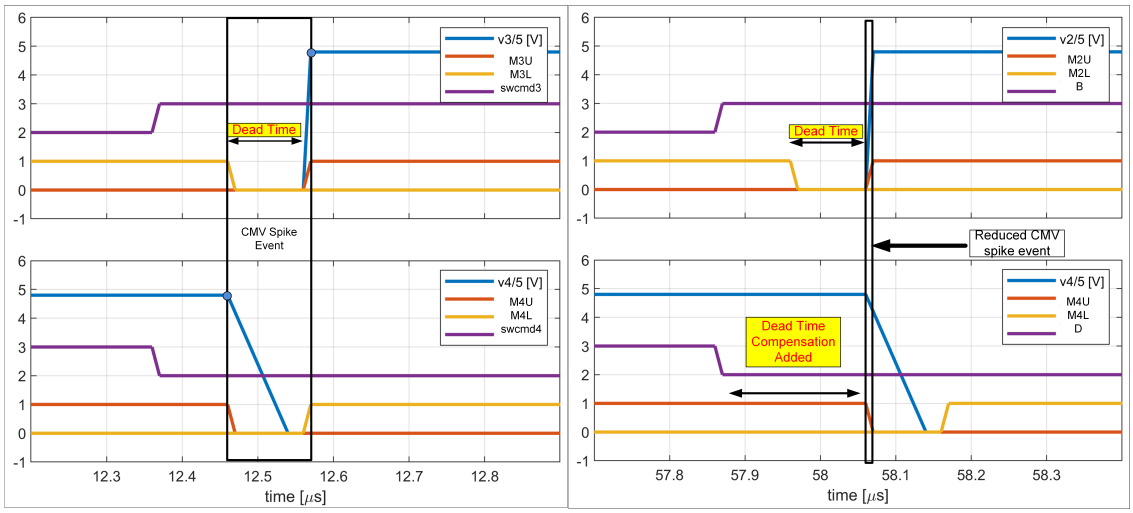

Figure 3.5. Timing diagram showing the effects of the dead-time compensation algorithm on switching behavior.

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CHAPTER 4:
Control Software and CHiL Simulations

This chapter presents the Verilog code and FPGA implementation for the controller of the three-phase four-leg VSI. Detailed information is provided to give the reader insight into the rationale and formulation of the code as well as a general overview of the controller implementation process. The use of CHiL is also discussed to demonstrate the progression of the dead-time compensation algorithm from theory, to simulated testing and verification, to laboratory hardware testing. By using CHiL, the timeline for verification and testing is shortened to leave more time for studying the results of the dead-time compensation method.

4.1 Switching Control Using an FPGA

To control the switches of the VSI, an ARTY A7 FPGA is used. This FPGA was chosen due to the 450 MHz internal clock speed which is sufficient to meet the 200 kHz switching requirement of the VSI [24]. Other FPGAs can be used, however, the author has experience with this device, making it ideal for the experiments performed for this thesis. Current probes are connected to the input output (IO) ports of the FPGA to convey the inverter output current measurements to the FPGA where they are subsequently compared to the reference currents that are either set by the user, or set by additional control systems. In the case of this experiment, the reference values are controlled by the user and can be changed depending on testing criteria or to the user's preference. The VIO functionality of Vivado, allows the user to input these commands to the FPGA in real time without the need to program and re-program the device. A discussion about the use of the ILA and VIO, will be included in the next section to give the reader context on what is being performed.

Figure 4.1 illustrates how the FPGA is integrated within the power electronics to give the reader a visual description of the FPGA within the system. In this case, the FPGA is connected to a computer through a USB cable and has IO ports connected to current probes, as well as to the four-leg silicon carbide (SiC) VSI to send the appropriate switching signals to the inverter. The FPGA acts as the control hardware that will perform the comparison necessary to determine which leg will commutate or not. As discussed in Chapter 3, delta modulation is used to control the switching of each inverter leg during operation [15].

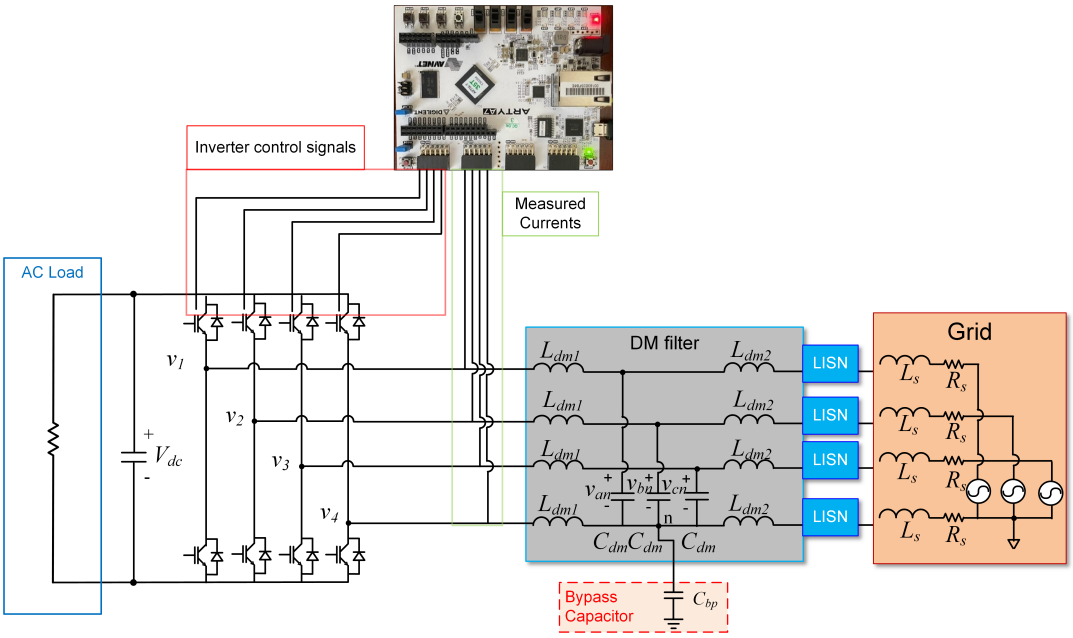

Figure 4.1. Generalized depiction of the FPGA interfacing with the inverter circuit.

The aforementioned control algorithm is implemented with Verilog HDL in the Vivado software. The error states of the measured and reference current values are first compared. The difference is used to rank each phase or leg of the inverter to determine which inverter legs need to switch and/or which legs need to remain the same. Figure 4.2, shows the Verilog code used to conduct this comparison from the measured and reference values. In this comparison, a reference current sine wave with amplitude set at 3 A is used and compared against the measured currents of the inverter. The difference is assigned to an error register. This register is then compared against the other error registers to determine the greatest error. Figure 4.3, depicts the error comparison code used to logically compare and rank errors between states and achieve the correct assignment of phases. This ranking system, determines the state with the greatest error which is then subsequently used to drive the switching of the inverter through intermediary variables in the Verilog code.

```
Isim1 =   $signed(Isim1[38:15])*K1   + sw1_mpc*K2; //  24.18 X 16.15 + 16.13 X 24.20 = 40.33 // uncomment this
Isim2 = $signed(Isim2[38:15])*K1 + sw2_mpc*K2; // added 8 to offset for bias in measurements
Isim3 = $signed(Isim3[38:15])*K1 + sw3_mpc*K2; // added 13 to offset for bias in measurements
Isim4 = - Isim1 - Isim2 - Isim3;
       Imeas_fil =   $signed(Isim1[39:8]) >>> 9;  // 32.16
       Imeas_fil_2 = $signed(Isim2[39:8]) >>> 9;
       Imeas_fil_3 = $signed(Isim3[39:8]) >>> 9; // phase 3 and 4 are switched on the board
       Imeas_fil_4 = $signed(Isim4[39:8]) >>> 9;

       error1 = ian_ref - $signed({Imeas_fil[21:0],18'b0});  // error is 40:34
       error2 = ibn_ref - $signed({Imeas_fil_2[21:0],18'b0});  // error is 40:34
       error3 = icn_ref - $signed({Imeas_fil_3[21:0],18'b0});  // error is 40:34
       error4 = idn_ref - $signed({Imeas_fil_4[21:0],18'b0});  // error is 40:34
    end
```

Figure 4.2. Verilog HDL code used to compare reference and measured current values

```
always @ (posedge slowclk2)// executed at 200 KHz
     begin
  sw1bUx_old = sw1bUx ; // need to save old state of x variables
  sw2bUx_old = sw2bUx ; // need to save old state of x Address_inx
  sw3bUx_old = sw3bUx ; // need to save old state of x Address_inx
  sw4bUx_old = sw4bUx ; // need to save old state of x Address_inx
            e1rank = error1;
            e2rank = error2;
            e3rank = error3;
            e4rank = error4;
            sw1rank = 2'b00; // will contain phase with largest error
            sw2rank = 2'b01;
            sw3rank = 2'b10;
            sw4rank = 2'b11;
            if (e1rank < e2rank) begin
                temp1z = e1rank;
                e1rank = e2rank;
                e2rank = temp1z;
                sw1temp = sw1rank;
                sw1rank = sw2rank;
                sw2rank = sw1temp;
              end
            if (e3rank < e4rank) begin
                temp2z = e3rank;
                e3rank = e4rank;
                e4rank = temp2z;
                sw2temp = sw3rank;
                sw3rank = sw4rank;
                sw4rank = sw2temp;
              end
            if (e2rank < e3rank) begin
                temp3z = e2rank;
                e2rank = e3rank;
                e3rank = temp3z;
                sw3temp = sw2rank;
                sw2rank = sw3rank;
                sw3rank = sw3temp;
              end
```

Figure 4.3. Verilog code of error ranking process.

In the uncompensated operation of this code, the sw1rank and sw2rank values would be compared, and the subsequent switch to high, low, or no switch would be assigned to the sw1bU through sw4bU switch. This signal would then ultimately be sent to the appropriate IO port of the FPGA to drive the inverter. This process is operated at a clock frequency of roughly 200 kHz and contains intermediate variables that are used to create delay through their assignment process to introduce dead-time to the system. This dead-time can be adjusted as necessary, and for the purposes of this experiment, both 100 ns and 300 ns dead time are used. In the physical lab configuration, the FPGA requires actual current measurements to compare against the reference values. To achieve a testing scenario that only involved the FPGA, a simulated value is used in place of the measured current values to verify the efficacy of the proposed changes in the Verilog code. In the next section, the use of the ILA will be discussed to show its usefulness in evaluating the switching waveforms to determine whether or not the inverter and IO signals are operating correctly.

4.2 Using The Integrated Logic Analyzer in Vivado

As mentioned previously, the Vivado software contains a useful ILA tool to evaluate waveforms of a specified variable. This tool enables the debug function to check if the signal outputs can achieve the designed functions. Ports such as the ones on the FPGA that control the switching operation, are crucial waveforms that can be evaluated using the ILA and the associated timing diagram. Figure 4.4 represents the code structure that is used to identify variables that the user needs to evaluate through the de-bugging procedure. In this case, the IO ports ja4 through jd3 from the FPGA are marked for debug since they are connected directly to the SiC-MOSFET switching devices of the inverter legs. They are specifically marked in order to evaluate their timing diagrams to see when each value goes high or low. Registers that contain decimal or hexadecimal information, may also be marked for debugging purposes. The IO port values, as well as the intermediate registers that are used to implement the delay necessary for the dead-time, can also be marked to verify the correctness of the delay and the respective output. This step is crucial to validate the software and implement the proposed compensation method discussed in Chapter 3. Figure 4.4, demonstrates the tag used to mark the items for evaluation using the ILA tool in Vivado. In this situation, the IO ports ja4 through jd3 are selected in order to verify that the signals sent to the inverter from the FPGA are correct.

```
(* mark_debug = "true" *) output reg ja4,  // phase1 U
(* mark_debug = "true" *) output reg ja3,  // phase1 L
(* mark_debug = "true" *) output reg jd10, // phase2 U
(* mark_debug = "true" *) output reg jd9,  // phase2 L
(* mark_debug = "true" *) output reg ja2,  // phase3 U
(* mark_debug = "true" *) output reg ja9,  // phase3 L
(* mark_debug = "true" *) output reg jd4, // phase4 U
(* mark_debug = "true" *) output reg jd3, // phase4 L
```

Figure 4.4. Ports ja4 through jd3 that are used to control the inverter.

Figure 4.5 demonstrates the output of the ILA including ja4 and ja3 ports, as well as intermediate register values to ensure the inverter legs are receiving the appropriate output switching signals with the correct timing sequence. Timing diagrams like this, prove to be instrumental in verifying the CHiL method implemented for testing the proposed dead time compensation method.

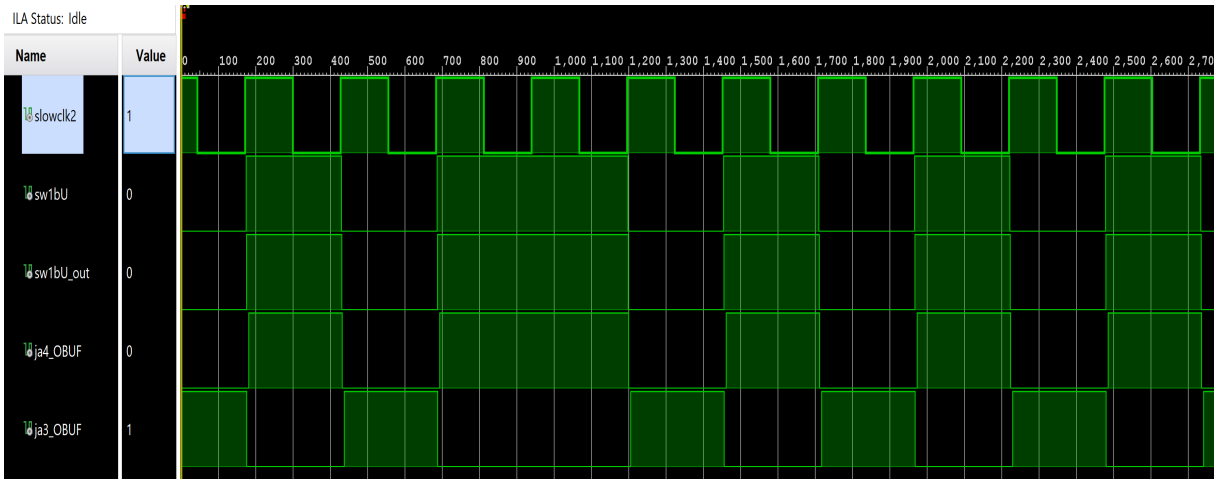

Figure 4.5. Ports ja4 through jd3 that are used to control the inverter.

4.3 Virtual Input Output Interface

In addition to the ILA tool, the VIO tool that Vivado offers allows the user to interact with the control hardware once the device has been programmed. It also incorporates an ability to

read off decimal, hexadecimal, or binary values from the circuit when configured correctly. Figure 4.6 shows the VIO interface that is presented to the user after successfully generating and programming the bitstream into the FPGA.

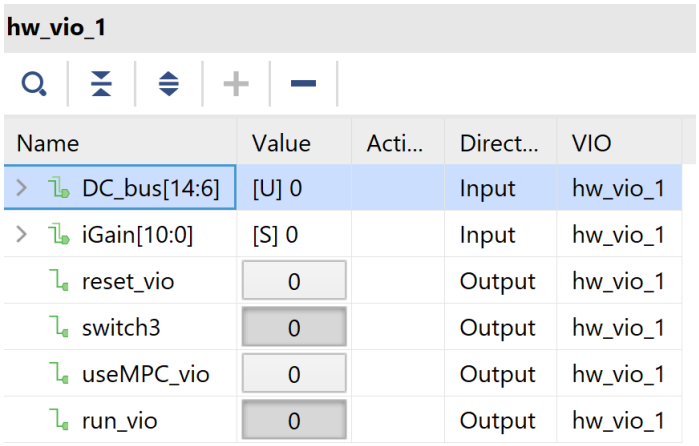

Figure 4.6. VIO interface with the user on the Vivado program.

The notable items from the Figure 4.6 include the DC bus voltage, reset vio, switch3, and the run VIO. As an example, the DC bus value measured and used by the controller can be visualized in this window, which can be further compared with the measurement results via physical voltage probes. Likewise, the reset VIO element allows the user to reset the FPGA as needed through the additional Verilog code that has been loaded into the device. Switch3 and the run VIO are the most useful or frequently used items for this thesis as they tie directly into the dead-time compensation process as well as the actual implementation of the Verilog code. When the run VIO is set to 0, the software does not implement the switching sequence. However, when the run VIO is set from 0 to 1, the Verilog code is active, and the switching sequence is implemented. This process is the same for the switch3; however, switch3 corresponds to the dead time compensation algorithm. When the switch3 value is a 1 then the compensation algorithm is enabled. Otherwise, it is disabled. The functionality of the VIO and its ability to interface with the user through a computer, allows the user to control the circuit directly without the need to constantly reprogram the FPGA. This provides an added safety benefit when operating the circuit at the 115 V parameters

called for when operating at the Type I power requirements stated in MIL-STD-1399 [21]. In short, these tools allow the user to evaluate, test, and operate the circuit using no physical switches or connections other than the ones provided by the control device and the laptop. Such an achievement allows future power electronic circuits to improve performance through the modification of software directly affecting the generation of CMV within the circuit. Software provides the template for not only simulation and testing, but also the means to directly impact performance of a physical circuit.

4.4 CHiL Simulation Implementation and Testing

The timing diagrams seen in the ILA tool in Vivado, provide a mechanism for determining the efficacy of the proposed algorithm. Prior to the laboratory implementation, the ILA tool is used to ensure that the correct output ports from the FPGA are signaling in sequence with their opposing portion of the inverter leg. For example, if the upper portion of the inverter leg for phase one is active meaning that the transistor is conducting, then the lower portion must be inactive. This ensures that there is no shoot through condition that will damage the inverter. Likewise, the upper and lower portions of each inverter leg must operate in sequence to ensure that each phase switches with a corresponding phase. This switching method is the basis of the PDM discussed in Chapter 3.

In Figure 4.7, the timing diagram from the ILA tool is inspected at a higher time axis resolution to ensure that the switching algorithm is functioning correctly and that each inverter leg is switching appropriately. On the left of the Figure, the individual legs and phases are broken down to their respective IO port for the FPGA. The IO ports, known as ja4 and ja3, correspond to the upper and lower devices of the phase one inverter leg while the subsequent legs have the same ordering with the top name corresponding to the upper switch of the inverter leg and the bottom name matching with the bottom switch of the inverter leg. From the Figure, it is apparent that each leg and phase are switching appropriately with no one phase remaining on causing a shoot through condition. On the right portion of the Figure, the time separation between switching events is also apparent. Each individual time delineation line denotes 20 ns for a total of 100 ns between switching events.

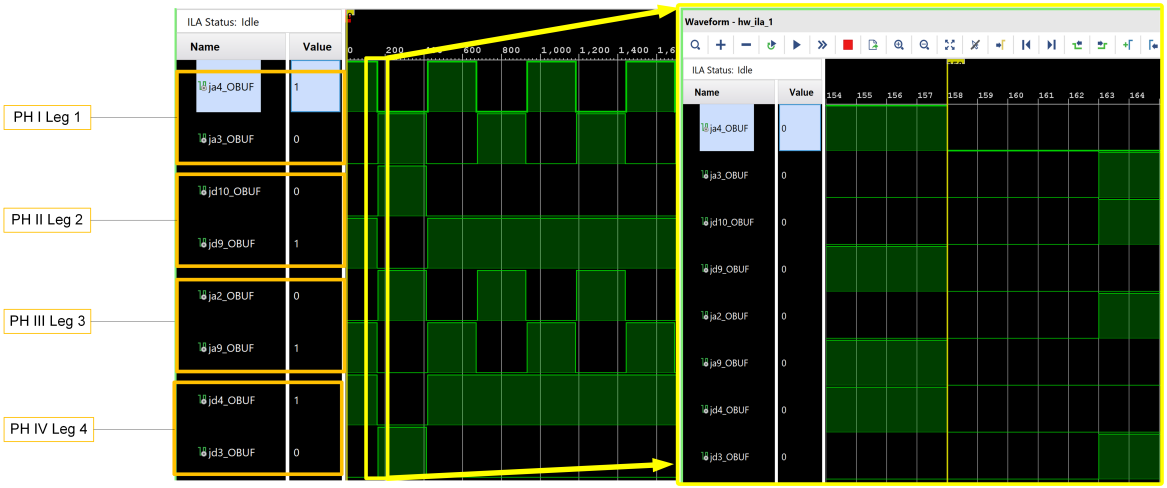

Figure 4.7. ILA timing diagram for IO ports.

This time period was chosen to produce the best possible results for eliminating CMV in the circuit, and can be adjusted as needed by the user for further evaluation. Reducing the dead-time below 100 *ns* results in the potential destruction of the inverter because the devices in the inverter cannot be fully turned off. The switching implemented in the FPGA, remains constant regardless of the current conditions when the algorithm is not enabled. In Figures 4.8 and 4.9 the switching event between phase one and three is demonstrated by the ja4, ja3, ja2, and ja9 waveforms. In this transition, phase one goes from a high voltage state to a low voltage state while that phase three goes from a low voltage state to a high voltage state. During this transition for both Figures, the registers sw1bUx, sw1bU, and sw1bU-OUT increment in a standard fashion in order to change the state of phase one from high to low. In both instances, these waveforms behave the same regardless of the current polarity within the transistor. This is indicative of the process where the switching events are taking place without the dead time compensation algorithm. As a result, there is the expected CMV generation caused by the interrupted current flow through the transistor. With the algorithm set in place, the waveforms change slightly with respect to Figures 4.8 and 4.9.

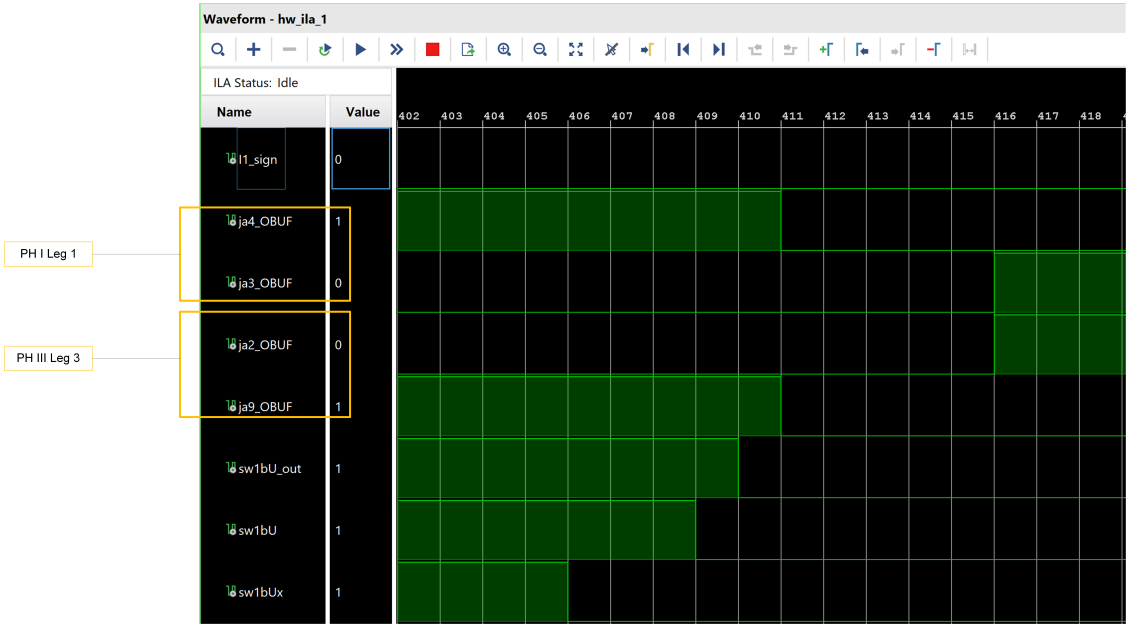

Figure 4.8. ILA timing diagram for negative current and algorithm inactive.

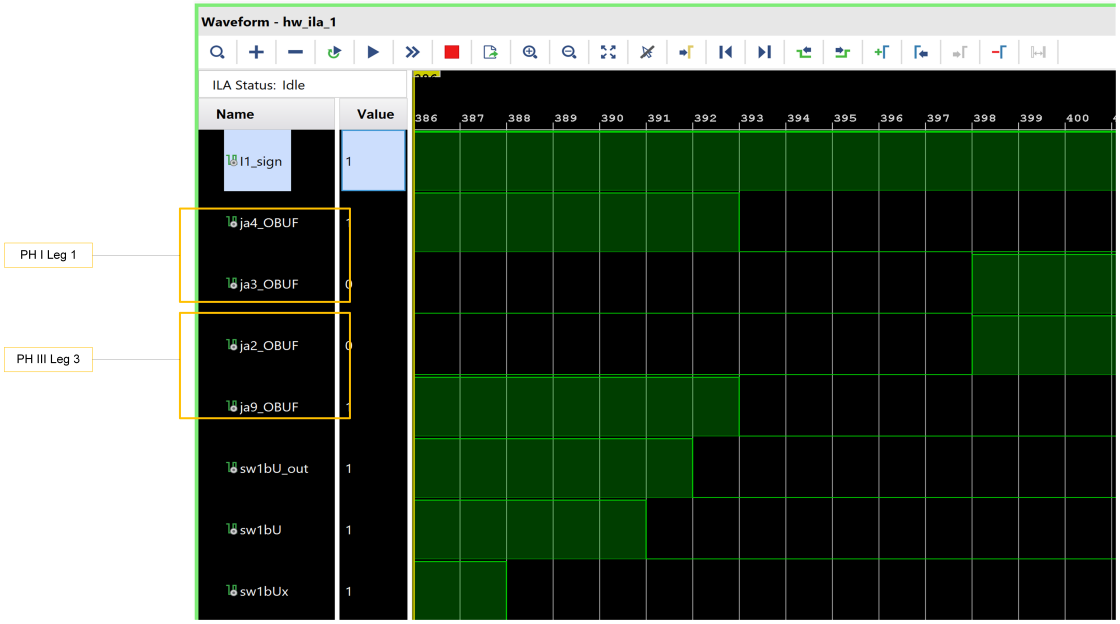

Figure 4.9. ILA timing diagram for positive current and algorithm inactive.

In Figures 4.10 and 4.11, the dead time compensation algorithm is active to demonstrate the effect of the method for both positive and negative current polarities. As seen in Figure 3.4, there is a delay that occurs in order to allow the commutation of the current through the transistor to occur. This delay is noticeable when looking at the sw1bUx registers of the previous four figures. In Figure 4.11, the sw1bUx waveform goes low five time cycles earlier compared to sw1bU_out in contrast to Figures 4.10, 4.9, and 4.8. This is to allow the current commutation through the transistor, which is achieved through the introduction of an additional 100 *ns* delay on top of the delay between when sw1bUx goes low and when sw1bU goes low. It is important to note that in the purposes of this code, sw1bUx is the output of the error ranking process for each phase while sw1bU and sw1bUout are the intermediate registers that are used to control the blanking time between the upper and lower portion of the inverter leg. In short, the use of these intermediate registers works in conjunction with the error ranking output to implement a delay long enough to allow sufficient time for the current to commute through the transistor. This delay only occurs when the conditions set forth in Figure 3.3 are met, meaning that the current polarity and state condition (conducting or not conducting) are met for that inverter leg. In the case of these previous figures, only one phase was shown. However, this algorithm applies to each individual phase and evaluates the current polarity and switching state simultaneously.

Based on the results from the ILA, the desired delay sequence according to the specified condition occurs as desired in the waveforms. As a result, the algorithm that was verified through the ILA can then be subsequently implemented into the hardware of the circuit for testing purposes. This ability to test and verify potential software changes before testing them in a laboratory, reduces the time necessary for testing and debugging.

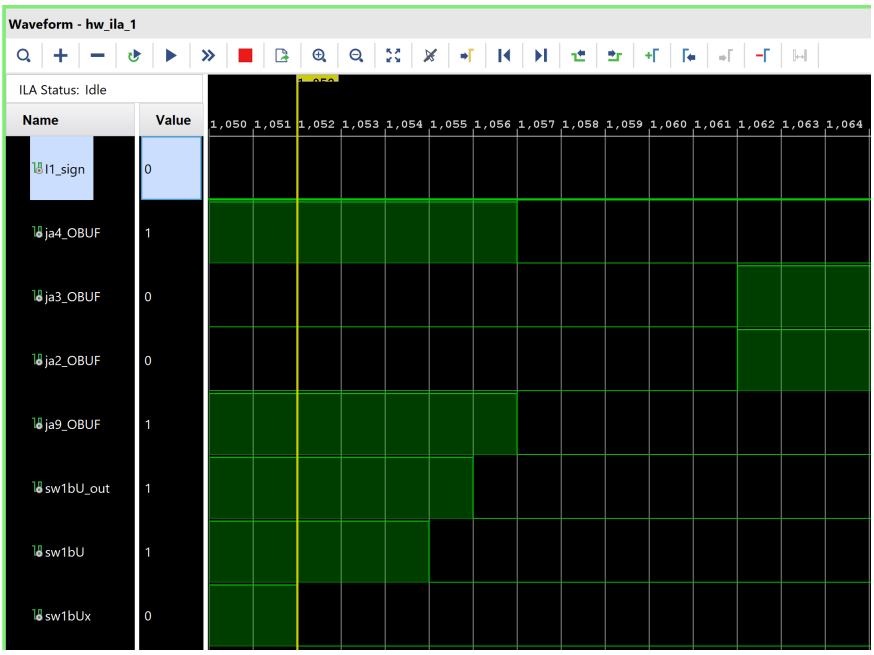

Figure 4.10. ILA timing diagram for negative current and algorithm active.

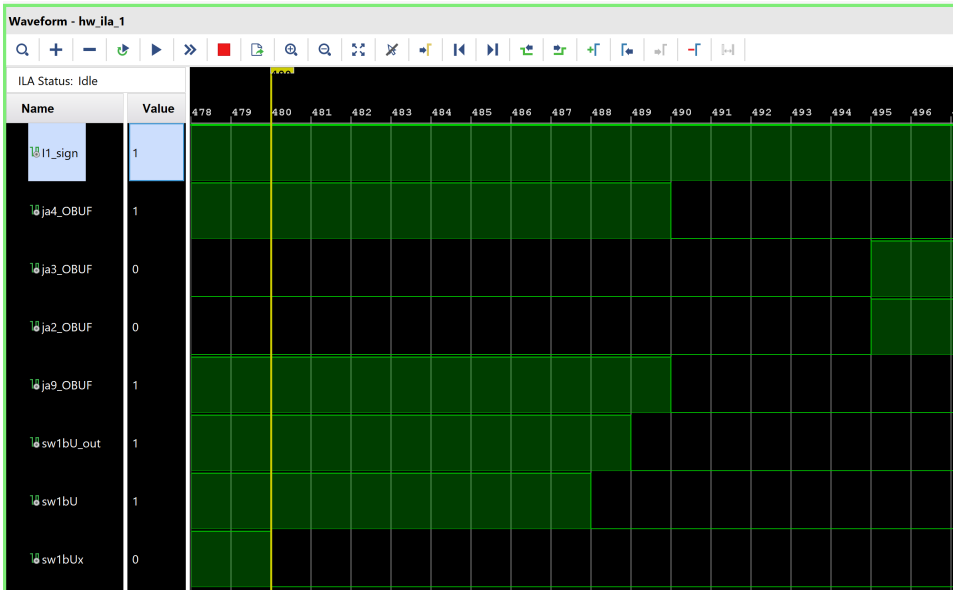

Figure 4.11. ILA timing diagram for positive current and algorithm active.

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CHAPTER 5:
Hardware Implementation

This chapter presents the integration of the control software discussed in Chapter 4 and the physical setup in the laboratory according to the requirements stated in the military standards.

5.1 Laboratory Setup

The laboratory setup for this thesis follows the guidelines in the diagram pictured in the military standard MIL-STD-461G for conducted EMI measurements, which is copied in Figure 2.8 [22]. The circuit schematic in Figure 5.2 and the photograph in Figure 5.1 show the laboratory setup for the four-leg three-phase VSI as required by [22] for conducted EMI testing of electronic equipment. In the laboratory setup, the four LISNs and the copper ground plane can be seen as well as the EUT.

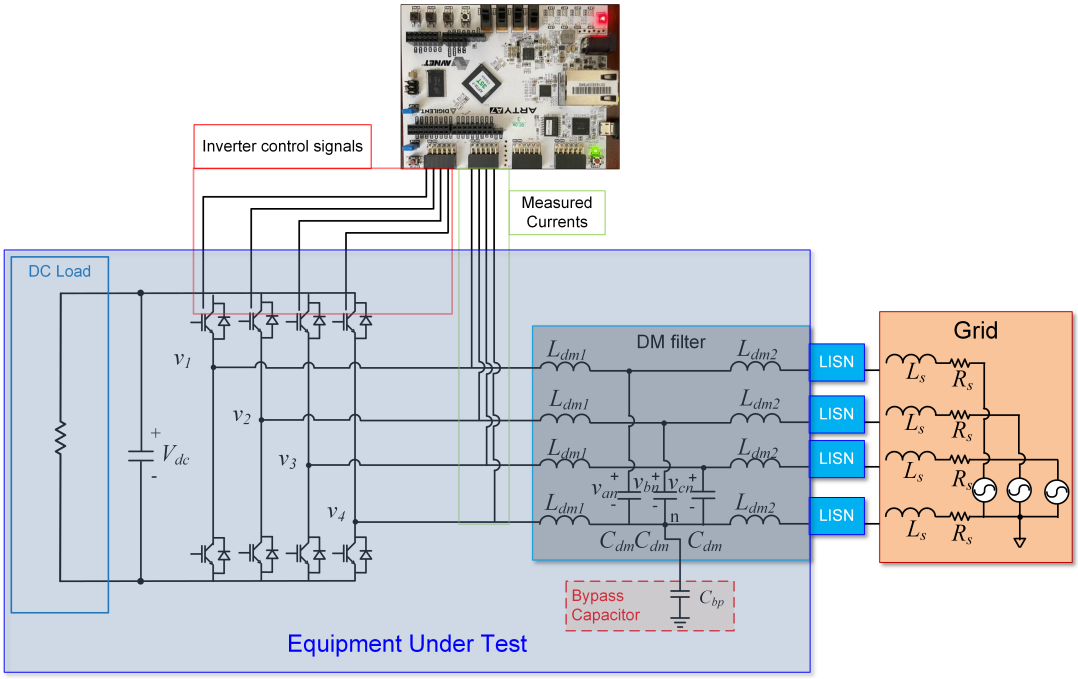


Figure 5.1. Circuit schematic of the laboratory setup.

There are four LISNs, for each leg and wire connected to the VSI. The LISNs as required by the military standard [22], standardize impedance control for the power leads and are necessary in order to ensure the experiment is repeatable and compatible with alternate testing laboratories. They are placed and connected between the DM filter and the grid power sources. The EUT includes the four-leg VSI built with SiC MOSFETs, the control hardware and the DM LCL filter. A resistor is connected to the VSI to represent a simple load. This is used in place of a DER as seen in Figure 3.1, to demonstrate the efficacy of the compensation method without the interference of additional power sources that may be connected. The control hardware consists of an FPGA board with voltage and current sensors connected to it. The FPGA board has a user interface, which is connected to a laptop for the experiments presented in this thesis.

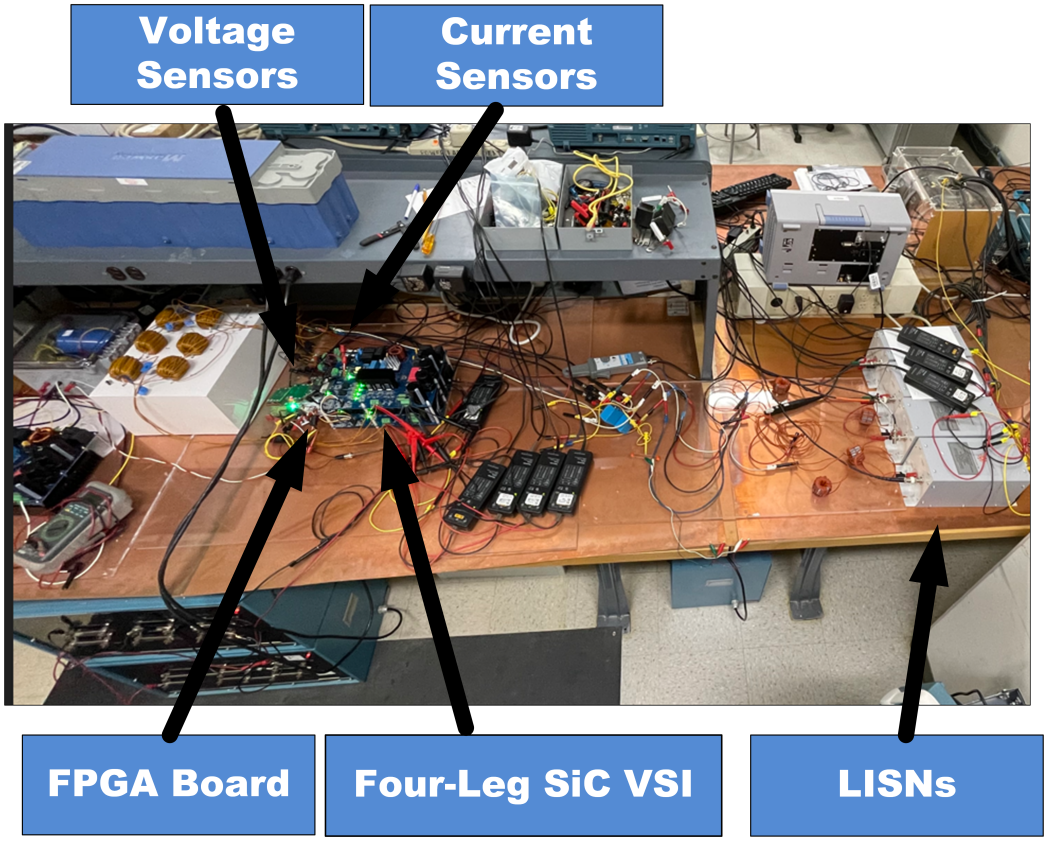


Figure 5.2. Laboratory setup.

Figure 5.3 displays the three-phase AC power source labeled *grid connection*, as well as the location of the laptop and resistive load connected to the DC bus of the four-leg VSI. It is important to note that laboratory settings contain external variables that are at times outside the control of the experiment being performed and must be accounted for. The power source contains harmonics that are the result of non-linear loads connected to the utility grid powering the building. As a result, these harmonics will be present in the measured voltage spectra presented in Chapter 6 and will be identified in order to demonstrate that they are not produced by the EUT.

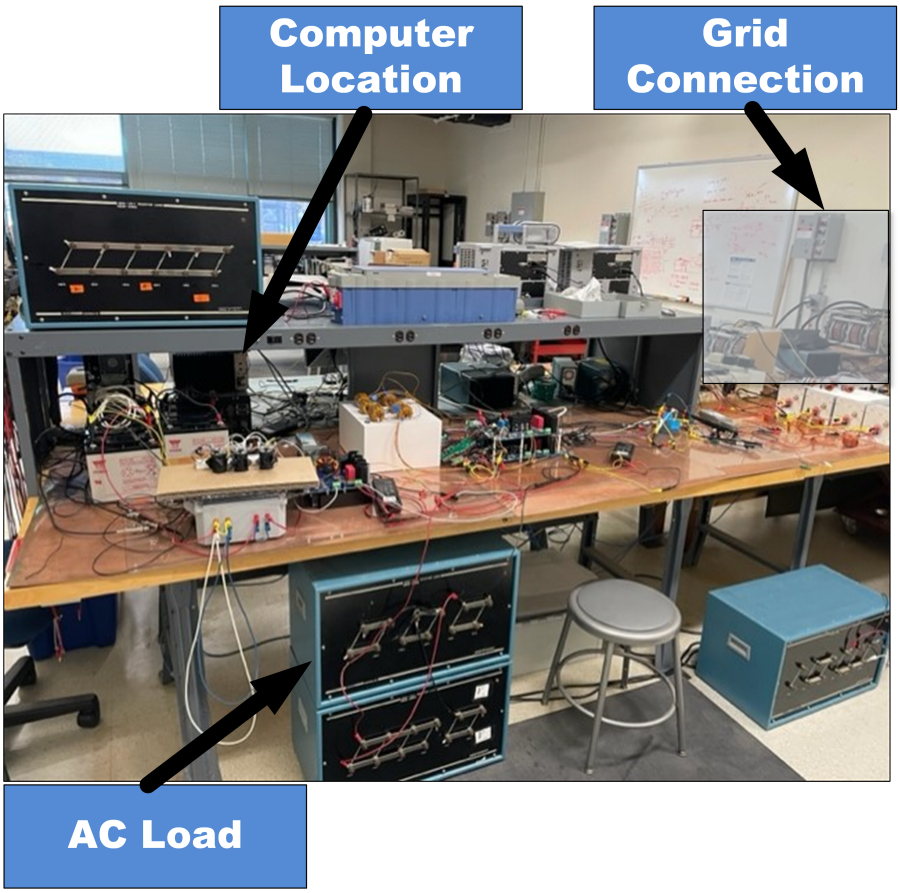


Figure 5.3. Setup in the lab additional view.

5.1.1 Laboratory Equipment

The equipment used to measure the voltage, current, switching, and frequency waveforms required for this thesis are listed in Table 5.1. This list, while not all inclusive, is meant to give the reader context to the most used equipment that was necessary to conduct the laboratory experiments for this thesis. Additionally, it is important to note the significance of each piece of equipment and how it is used in the experiments. For the Diligent Pmod current sensors, additional code not shown in this thesis was required to evaluate current data through the IO ports of the FPGA. Also, the two oscilloscopes were essential in validating the success of the work performed during the simulation of the dead-time compensation method. The MSO4034 scope was used to measure the dead-time and delays of the VSI switching events, while the RTE1024 performed the Fourier transform of the voltage to the frequency domain to compare against the CE 102 limits in [22]. This oscilloscope can project the CE 102 limit on the screen to measure the compliance of the VSI to the military standard in real time.

Table 5.1. Laboratory equipment

Equipment Name	Model Number	Purpose
Diligent Pmod	ISNS20	Current sensor used to interface with the FPGA
High Voltage Differential Probe	P5200	Measure voltages for oscilloscopes
Tektronix Mixed Signal Oscilloscope	MSO4034	Show switching events of the VSI
Rohde and Schwarz Oscilloscope	RTE1024	Preform FFT of voltage and show CE 102 limits
Solar LISN	9629-50-BP-25-BNC	Standardize impedance to meet military standards

5.2 From CHiL Simulation to Laboratory Testing

The overall process for validating the dead-time compensation method can be summarized in the block diagram seen in Figure 5.4. First the Verilog code is placed into the Vivado software and loaded into the FPGA. Next, the user can perform CHiL simulations and subsequently evaluate and modify the compensation method in order to ensure the simulated waveforms match the expected outcome. Once the code has been verified through the use of the ILA as described in Chapter 4, it can then be altered to take in the input from the current and voltage sensors connected to the physical hardware. Figure 5.5 illustrates the

process of commenting the simulation component of the code and the activation of the code that interfaces with the FPGA and current sensors.

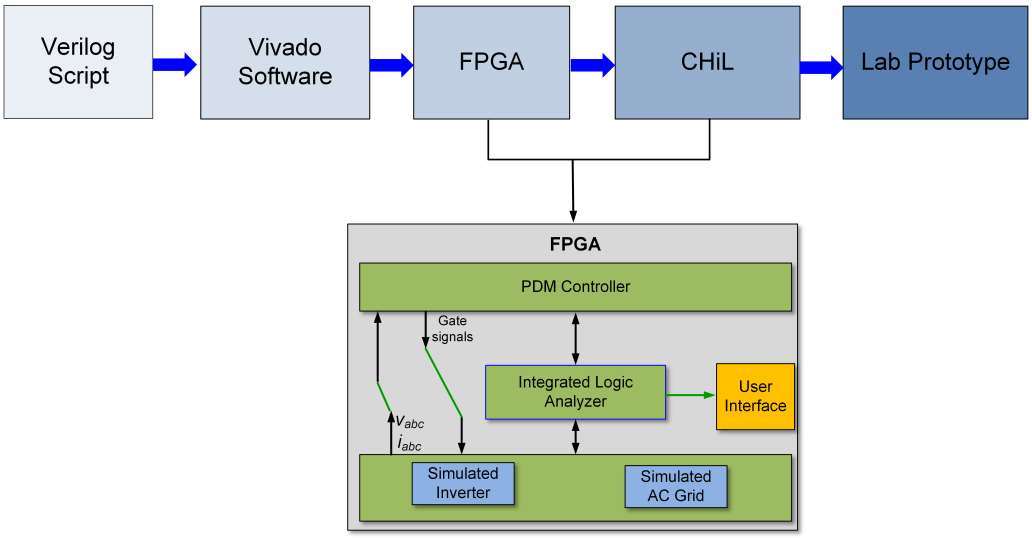


Figure 5.4. Block diagram for design and execution process.

In the final step towards validation, the FPGA receives input from the current sensors and implements in the hardware the control method discussed in Chapter 3. This step demonstrates the simplicity from going to a strictly simulation environment, to a testing scenario in a laboratory. Additional troubleshooting will be needed to ensure hardware such as the current and voltage sensors communicate with the FPGA and the connections are secure and functioning correctly. Additionally, the code can also be adjusted to meet supplemental objectives the user may have. In this thesis, additional code was implemented to increase the dead-time from 100 ns to 300 ns to test the effects of the dead-time increase on the inverter. The results of this increase are displayed in Chapter 6 along with the 100 ns results. Likewise, this dead-time increase was also implemented and tested through the ILA prior to the hardware implementation, which saved time when conducting the laboratory experiments.

```
  Imeas = (datainput16-$signed(16'h3fd8))*oneby89p95; // added 5 to offset for bias in m
  Imeasx = Imeas-Imeas_fil;
  Imeas_fil = Imeas_fil + alpha_dT*$signed(Imeasx[26:11]);  // phase 1
  Imeas_2 = (datainput16_2-$signed(16'h3fc8))*oneby89p95; // added 7 to offset for bias
  Imeasx_2 = Imeas_2-Imeas_fil_2;  // phase 2
  Imeas_fil_2 = Imeas_fil_2 + alpha_dT*$signed(Imeasx_2[26:11]);  // phase 2
  Imeas_3 = (datainput16_3-$signed(16'h3FA0))*oneby89p95; // added 12 to offset for bias
  Imeasx_3 = Imeas_3-Imeas_fil_3;                         // dec2hex((2048-12)*2^3)
  Imeas_fil_3 = Imeas_fil_3 + alpha_dT*$signed(Imeasx_3[26:11]);  // phase 3
  Imeas_4 = (datainput16_4-$signed(16'h3F88))*oneby89p95; // added 15 to offset for bias
  Imeasx_4 = Imeas_4-Imeas_fil_4;
  Imeas_fil_4 = Imeas_fil_4 + alpha_dT*$signed(Imeasx_4[26:11]);  // phase 4

 // Isim1 =   $signed(Isim1[38:15])*K1   + sw1_mpc*K2; //  24.18 X 16.15 + 16.13 X 24.20
 // Isim2 = $signed(Isim2[38:15])*K1 + sw2_mpc*K2; // added 8 to offset for bias in meas
 // Isim3 = $signed(Isim3[38:15])*K1 + sw3_mpc*K2; // added 13 to offset for bias in mea
 // Isim4 = - Isim1 - Isim2 - Isim3;
 // Imeas_fil =   $signed(Isim1[39:8]) >>> 9;  // 32.16
 // Imeas_fil_2 = $signed(Isim2[39:8]) >>> 9;
 // Imeas_fil_3 = $signed(Isim3[39:8]) >>> 9; // phase 3 and 4 are switched on the board
 // Imeas_fil_4 = $signed(Isim4[39:8]) >>> 9;

  error1 = ian_ref - $signed({Imeas_fil[21:0],18'b0});  // error is 40:34
  error2 = ibn_ref - $signed({Imeas_fil_2[21:0],18'b0});  // error is 40:34
  error3 = icn_ref - $signed({Imeas_fil_3[21:0],18'b0});  // error is 40:34
  error4 = idn_ref - $signed({Imeas_fil_4[21:0],18'b0});  // error is 40:34
end
```

Figure 5.5. Verilog Code for measured values with simulated values now commented out.

CHAPTER 6:
Results

This chapter covers the results of the dead-time compensation with respect to the military standard CE 102. Innate conditions of the grid power source, as well as the oscilloscope recorded time domain data points and CE 102 compliance will also be discussed.

6.1 Experimental Conditions

As mentioned previously, the voltage supplied by the utility AC grid in the laboratory contains harmonics that are not generated by the EUT. The voltage spectrum contains harmonics at the 30, 60, and 70 kHz values and are measured from the voltage at the LISN terminal for the first leg of the VSI. These voltage measurements undergo a Fourier transform operation by the Rohde and Schwarz RTE1024 oscilloscope which converts the time domain measurement of the voltage into frequency spectrum that can be compared to the limits in the military standard. Figure 6.1 displays the presence of these harmonics below the 100 kHz mark. These tones exist in all subsequent figures showing the harmonics of the voltage, but are not the result of the inverter operation. In the experiments presented here, these harmonics do not exceed the CE 102 limits in MIL-STD-46G [22].

The device used to take the measurements in Figure 6.1 is a Rhode and Schwarz RTE Oscilloscope which has the ability to pre-program the CE 102 limits from the military standard [22] onto the screen. Note that the CE 102 limit line was relaxed by 9 dB with respect to the benchmark in Figure 2.7, based on of the AC input voltage used for the experiments. The limit line itself is a straight line with a negative slope starting from 103 $dB\mu V$ ending at 69 $dB\mu V$ from 10 kHz to 500 kHz with a constant 69 $dB\mu V$ line from 500 kHz to 10 MHz.

All measurements were conducted with the EUT connected to the AC grid, through a VARIAC with the output voltage set at Type I nominal rms line to line voltage of 200 V [21]. The experimental parameter used for the following experimental measurements are listed in Table 6.1. It is important to note that a 6.8 nF bypass capacitor was added to the DM filter as shown in Figure 5.2, in order to meet the standard. However, as can be seen

in the following figures, the implementation of the dead-time compensation method does have a measurable effect on reducing the CMV generated from the VSI irrespective to the presence of the capacitor. Additionally, Table 6.1 presents two dead-time values, which will be alternatively used in the experiments although the 300 *ns* dead-time yields more significant results.

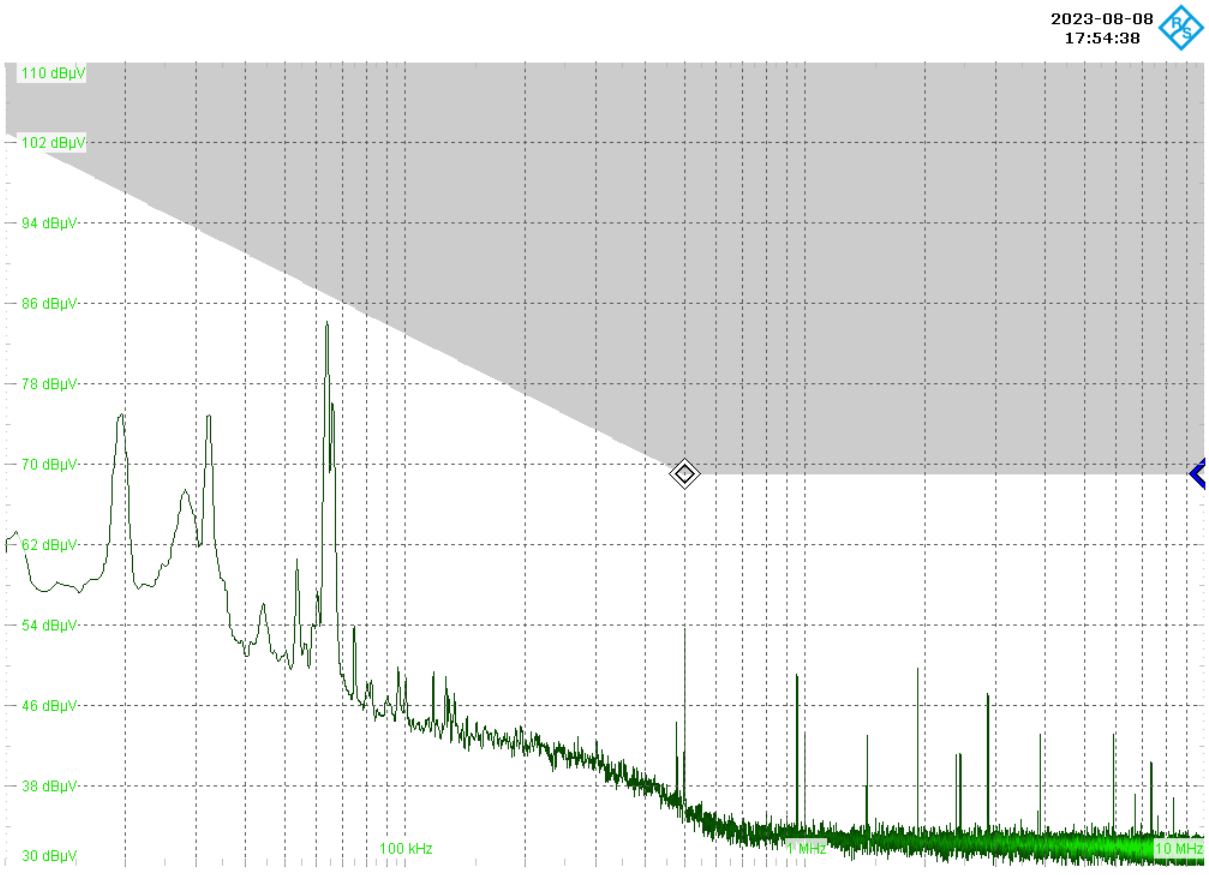


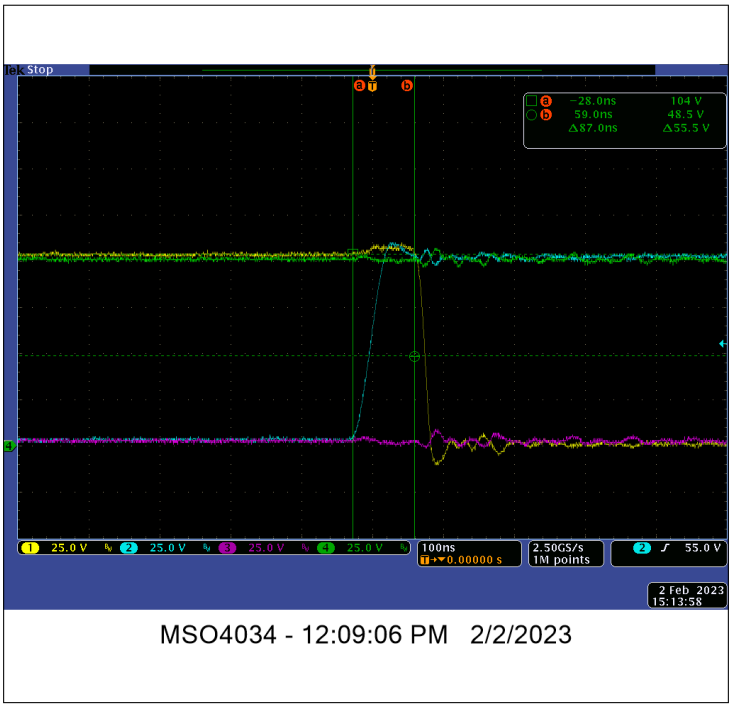
Figure 6.1. Harmonic representation of the grid without inverter operation.

Table 6.1. Experimental measurement parameters

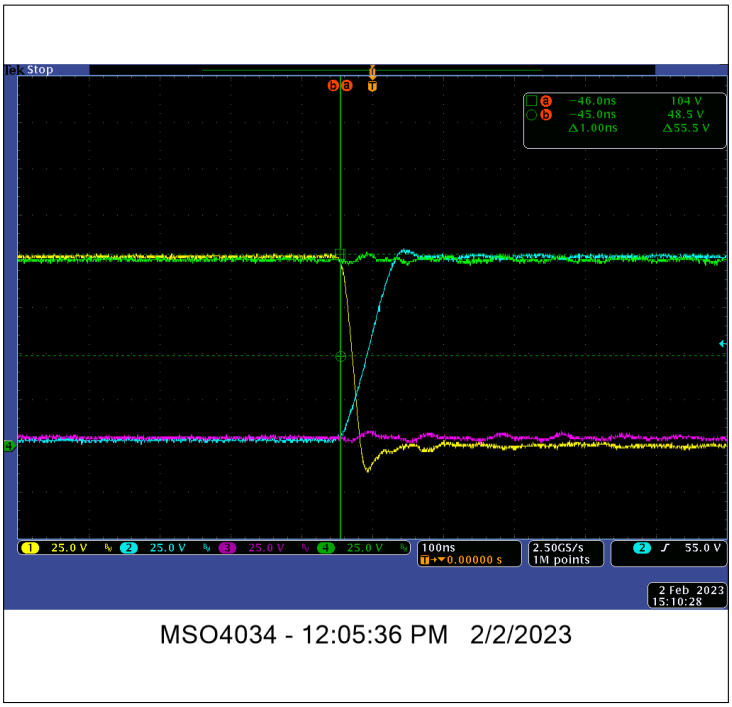
Symbol	Description	Value
C_{dc}	DC bus capacitance	1.2 mF
V_{dc}	DC bus voltage	350 V
V_{ll}	Grid line-to-line voltage	200 V
L_{dm1}	DM inductance 1	500 μH
L_{dm2}	DM inductance 2	400 μH
C_{dm}	DM capacitance	20 μF
R_{dcload}	DC load resistance	174 Ω
C_{bp}	Bypass capacitance	6.8 nF
t_{dead}	Dead-time	100 ns, 300 ns

6.2 Results with 100 ns dead-time

In this section, the CE measurements obtained with 100 ns dead-time are presented. This value was set by previous work [15] that determined that this was the minimum dead-time for the safe operation of the SiC-MOSFET used for the laboratory prototype. Figure 6.2 displays the measured switching events for both modes of operation: (a) with the dead-time compensation off and (b) with the dead-time compensation active. In Figure 6.2a, when the dead-time compensation is disabled, the voltage v_1 on the first inverter leg rises about 100 ns before the voltage on the other inverter leg falls. In Figure 6.2b the switching event is corrected by the dead-time algorithm which delays the commutation of leg 1 so that it happens at the same time as the other leg. These measured waveforms demonstrate that the dead-time compensation, previously validated with CHiL simulations, has in fact achieved the desired result in the laboratory hardware. The oscilloscope used for these measurements is the Tektronix MSO 4034.



(a) 100 ns dead-time compensation off



(b) 100 ns dead-time compensation on

Figure 6.2. Switching events for 100 ns dead-time implementation with the dead-time compensation method off (a) and on (b).

While the switching waveforms prove that the dead-time compensation achieves the desired effect in the laboratory, the voltage spectra acquired to verify the EUT compliance to CE 102 [22] show that the effect of the compensation method is minimal when 100 ns dead-time is used. In fact, the two figures are almost identical.

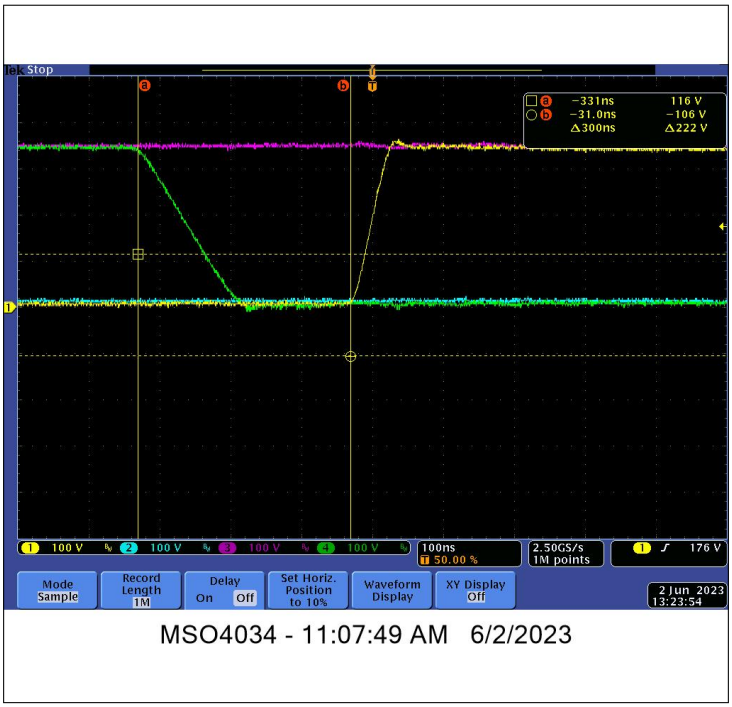
Figure 6.3. CE 102 compliance for 100 ns dead-time, 6.8 nF bypass capacitor, and with compensation method off.

Figure 6.4. CE 102 compliance for 100 ns dead-time, 6.8 nF bypass capacitor, and with compensation method on.

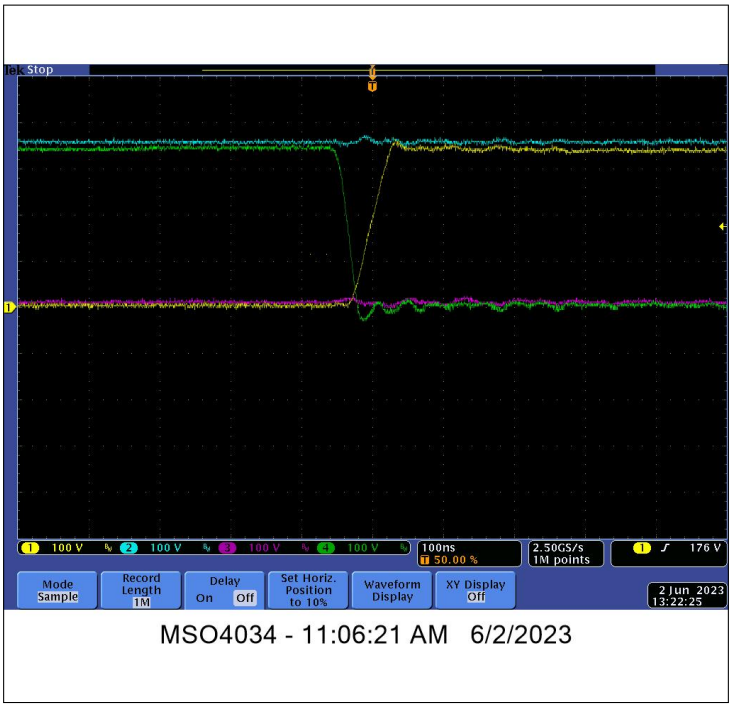
In Figure 6.4 the harmonics measured at 300 kHz and above are slightly larger than the ones seen in Figure 6.3. One hypothesis to explain this result is that noise in the current sensors may affect the measurements of the current polarity. If the FPGA is unable to distinguish the current polarity in the time necessary to accurately update the switching signals, then it is possible that a switching event can be omitted altogether. Further research will determine the cause of this result; however, once the dead-time has been increased to 300 ns, the effect of the compensation method becomes apparent.

6.3 Results with 300 ns dead-time

The measurements presented in Figure 6.5 are similar to those displayed in Figure 6.2, but obtained with a larger dead-time of 300 ns. The switching waveforms demonstrate the efficacy of the dead-time compensation method in the hardware implementation. The time between the two voltage transitions is different due to the increased dead-time value used. The true effect of the dead-time compensation method is seen in the LISN voltage spectra shown in Figure 6.6 and Figure 6.7 without and with dead-time compensation respectively. Both spectra show how the dead-time compensation method lowers the spectrum so that the EUT meets the CE 102 limits in MIL-STD-561G [22]. In Figure 6.6, the 164.5 kHz and 195 kHz harmonics exceed the CE 102 limit line imposed by the military standard. Additionally, there are noticeable harmonics at 200 kHz, the PDM frequency, and its harmonics. These harmonics are significantly reduced once the dead-time compensation method is enabled, as seen in Figure 6.7. The 164.5 kHz and 195 kHz harmonics now fall below the CE 102 limit, and all subsequent harmonics at 200 kHz and its multiples have been reduced by about 8 dB. This demonstrates that the software implementation of the dead-time compensation method reduces the EMI footprint of the inverter without additional CM filters, such as CM chokes. Overall, the compensation method decreased the harmonics by an average of 6 dB which is a significant reduction in the conducted EMI generated from this inverter. Table 6.2 displays the individual performance improvements for each of the LISN voltage harmonics for compensated and uncompensated measurements when the dead-time is set at 300 ns .



(a) 300 ns blanking time dead-time compensation off



(b) 300 ns blanking time dead-time compensation on

Figure 6.5. Switching events for 300 ns blanking time implementation with the dead-time compensation method off and on.

Figure 6.6. CE 102 compliance for 300 ns dead-time, 6.8 nf bypass capacitor, and with compensation method off.

Table 6.2. Improvements with compensation method (300 ns)

Frequency [kHz]	Uncompensated [dB]	Compensated [dB]	Improvement [dB]
164.5	80.5	76.6	3.9
195.5	80.28	71.85	8.43
390.6	68.7	62.2	6.5
586.1	66.5	60.0	6.5
781.1	67.11	61.1	6.01
976.5	65.5	57.9	7.6

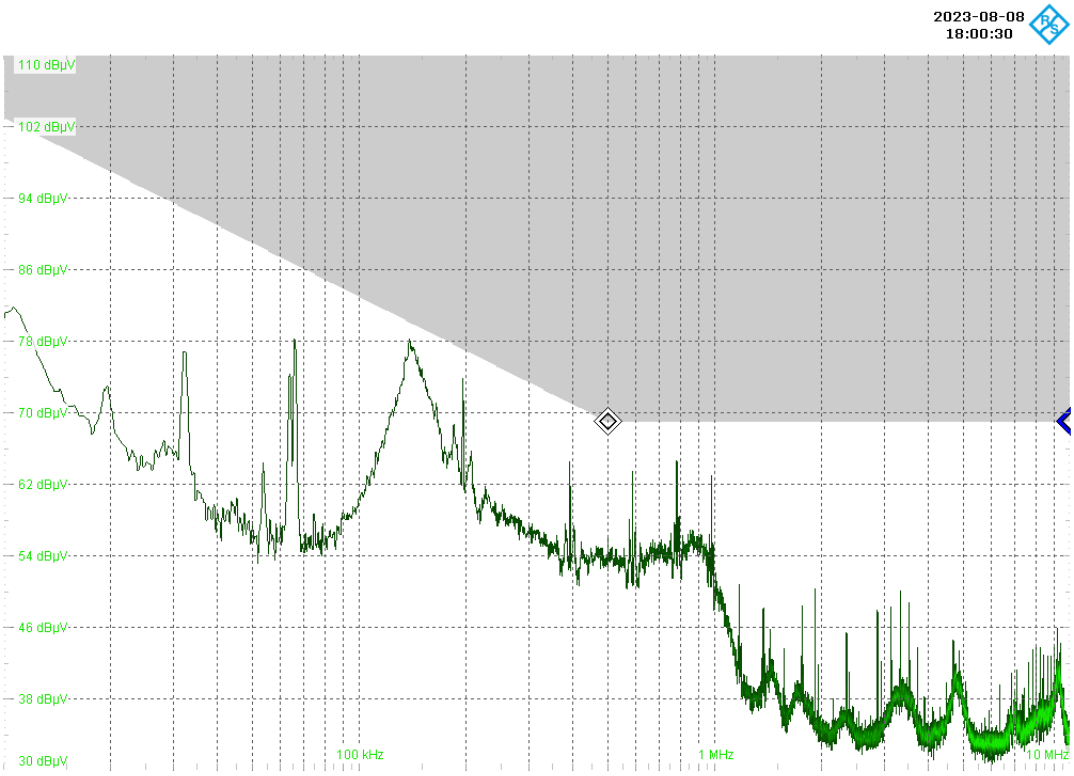


Figure 6.7. CE 102 compliance for 300 ns dead-time, 6.8 nf bypass capacitor, and with compensation method on.

6.4 Additional Analysis

In this section, an analysis is conducted on the presence of the bypass capacitor in the circuit and on the time-domain switching events with and without the compensation method. This analysis includes compliance with the CE 102 limit as well as time domain waveforms of switching events generated from data retrieved from the RTE 1024 oscilloscopes. MATLAB is used to generate the plots seen in the time domain sub-section.

6.4.1 Presence of the Bypass Capacitor

To test the effect of the dead-time compensation method on the inverter without the bypass capacitor, the 6.8 nF capacitor was removed and the inverter was tested with and without

dead-time compensation. The results of this experiment can be seen in Figures 6.8 and 6.9 without and with dead-time compensation, respectively. The spectra demonstrate once again that the compensation method reduces the peaks of the LISN voltage harmonics, although, the reduction is not enough for the EUT to meet the CE 102 limits.

Figure 6.8. CE 102 compliance for 300 *ns* dead-time with compensation method off without a bypass capacitor.

Figure 6.9. CE 102 compliance for 300 *ns* dead-time with compensation method on with a bypass capacitor.

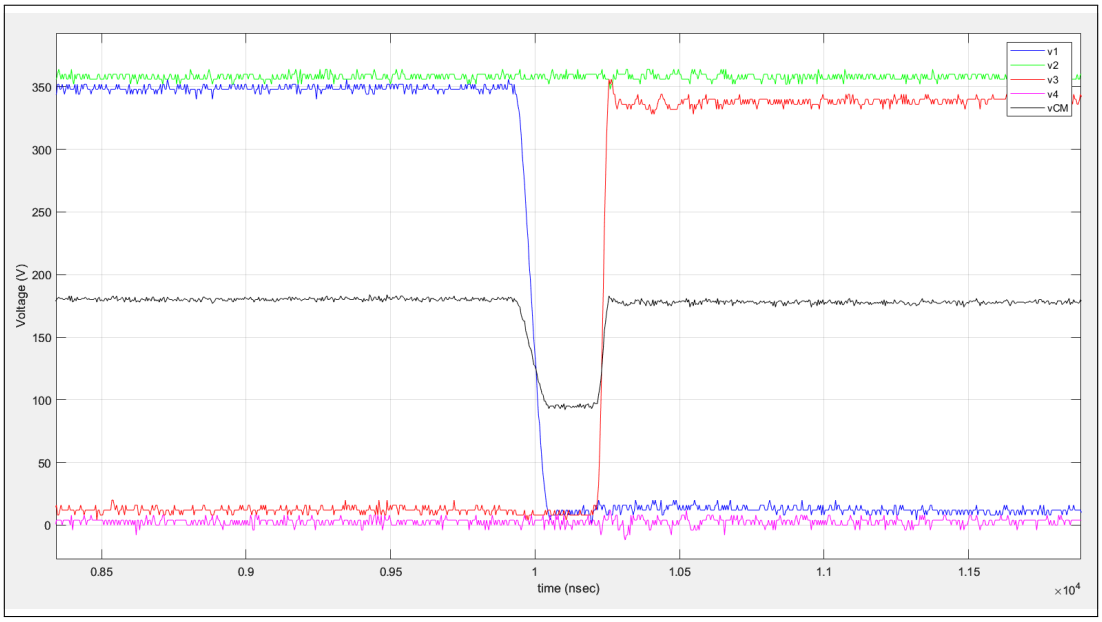
6.4.2 Switching Events Analysis

In order to better visualize the CMV generated from the inverter, the voltages at the inverter poles during commutation for the case with 300 *ns* dead-time were post-processed in MATLAB. Switching events were compared, as well as the CMV, which was obtained by summing the four inverter pole voltages. The results, shown in Figure 6.10a and Figure 6.10b, display the reduction of CMV not in terms of sheer magnitude but in duration of the event. For Figure 6.10a, the voltage magnitude drops from approximately 179 *V* to 94 *V* representing a spike of roughly -85 *V*. The duration of this event is for the whole 300 *ns* dead-time as the CMV remains constant during this entire time. Figure 6.10b on the other hand, achieves a similar negative magnitude, but a much smaller duration. The spike duration is not held constant over the whole 300 *ns* period and instead decreases almost

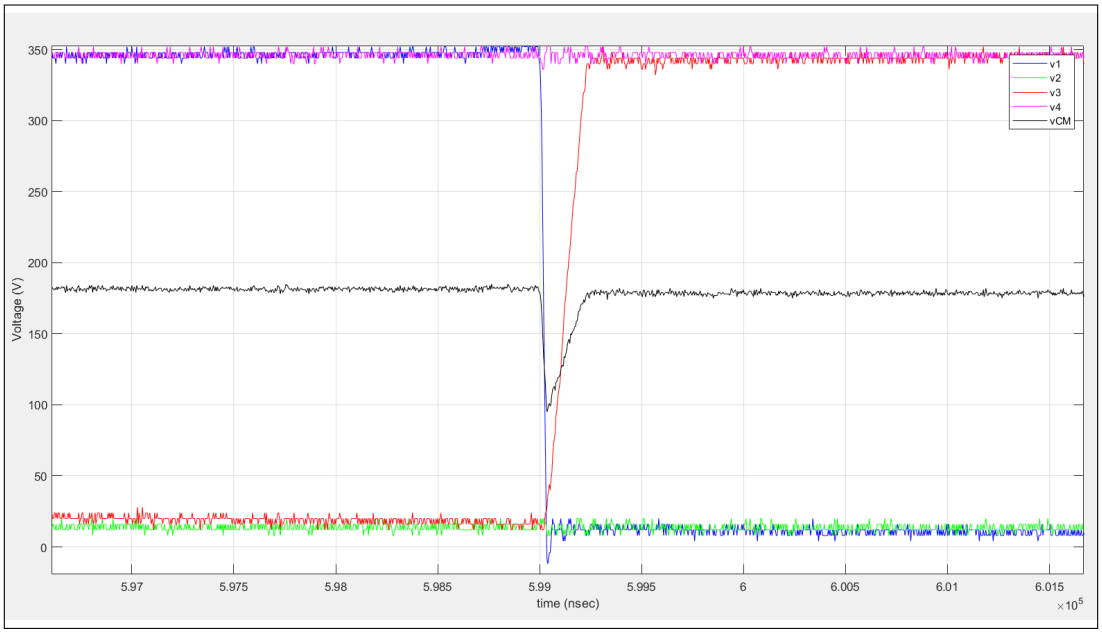
immediately after the spike has reached its maximum value. In this instance, the dead-time compensation method reduces the amount of time the CMV peaks and yields a shorter commutation resulting in a reduced EMI generation for the inverter.

However, Figures 6.11a and 6.11b display a switching event that when compensated leads to a complete reduction in the CMV generated during the switching event. This example compared with the two previous figures demonstrates that not all switching events achieve a zero CMV generation event, but that the compensation method does achieve the effect of reducing the event duration and or eliminating the event entirely. One potential cause of this discrepancy may be caused from the amount of dead-time that is used for each switching event. A 300 *ns* dead-time may be effective in eliminating the CMV for some switching events while not as effective in eliminating it from others. To remedy this, a commutation method that individualizes the dead-time necessary for each switching event may be necessary to eliminate all CMV generating events. Further analysis using the ILA function in Vivado will help identify and verify this cause and aid in determining the best method to solve this issue.

Overall, the implementation of the dead-time compensation method achieves positive results in reducing the severity of CMV events. Future work in refining the dead-time compensation algorithm may achieve further improvements as discussed in the following chapter.

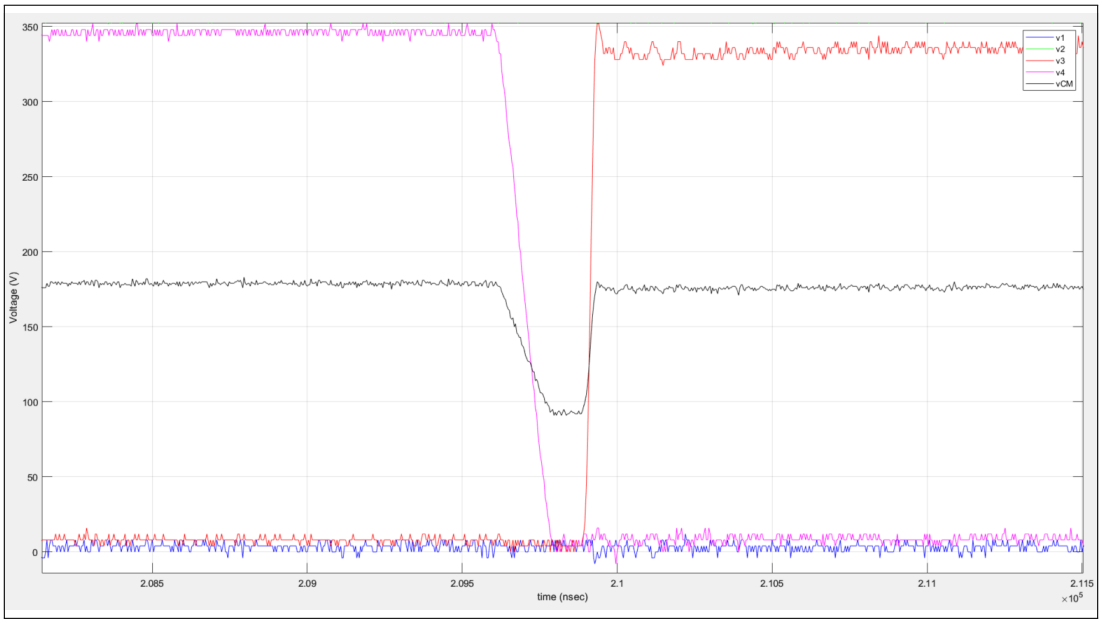


(a) Dead-time compensation off

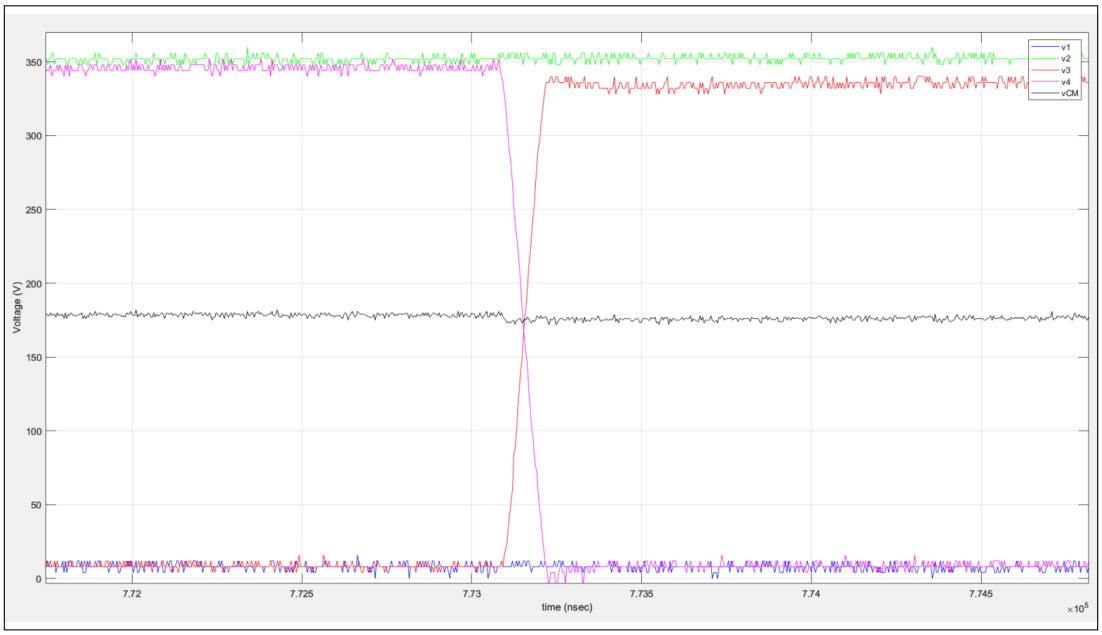


(b) Dead-time compensation on

Figure 6.10. Time compliance for 300 ns dead-time with compensation method off (a) and on (b).



(a) Dead-time compensation off



(b) Dead-time compensation on

Figure 6.11. Switching events for dead-time implementation with the 300 ns dead-time compensation method off (a) and on (b).

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CHAPTER 7:
Conclusion and Future Work

This chapter summarizes the findings of this thesis and presents avenues of future work that can progress this topic of research.

7.1 Conclusions

This thesis demonstrates that the proposed dead-time compensation algorithm achieved its desired effect of reducing the CMV of a three-phase four-leg VSI and improving adherence to military standards without the need for additional filters. It also demonstrates the effectiveness of using software and simulations to produce successful results without the need to work solely in a laboratory setting. The use of the ILA and VIO functions in Vivado demonstrated that software improvements can be fabricated without hardware and that CHiL can be used to estimate the CMV generation of a VSI in real time. By incorporating these software functions with the flexibility of the FPGA, troubleshooting, testing, and verification times were all significantly reduced.

Further refinements to the dead-time compensation algorithm can be accomplished using the same methods described in this thesis to achieve the individualized dead-times for switching events. In all, this research serves to benefit the Navy and Marine Corps branches in its efforts to reduce weight and costs and improve the safety and capabilities of the Sailors and Marines that are equipped with various power electronic systems across the globe.

7.2 Future Work

Future work can include various updates to the dead-time compensation algorithm to further reduce the CMV and ensure a consistent performance with different loads. Individualized delay times could be added to switching events with additional software, but first the code needs to be tested to verify the conclusions discussed in Section 6.4.2.

Testing the dead-time compensation method in a complete microgrid system is necessary to ensure the VSI operates correctly outside of this simple resistive load scenario. Additionally,

cost, weight, power loss, and reliability analyses can be conducted to see the savings that this algorithm can achieve when implemented on Navy and Marine Corps power systems. Specifically, the savings in cost, weight, and size from the elimination of most of the CM filter should be estimated, particularly for shipboard applications were the weight and size of EMI filters are a concern. The cost and performance of the algorithm can also be evaluated on an application specific integrated circuit to see if the cost of implementation could be reduced for large scale production.

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