AFRL-RY-WP-TR-2024-0011

MIXED-MODE CIRCUITS FOR EXTREME SPEED AND PRECISION

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APRIL 2024
Final Report

AIR FORCE RESEARCH LABORATORY
SENSORS DIRECTORATE
WRIGHT-PATTERSON AIR FORCE BASE, OH 45433-7320
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REPORT DOCUMENTATION PAGE

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1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED	
		START DATE	END DATE
April 2024	Final	17 September 2019	16 November 2023

4. TITLE AND SUBTITLE
MIXED-MODE CIRCUITS FOR EXTREME SPEED AND PRECISION

5a. CONTRACT NUMBER	5b. GRANT NUMBER	5c. PROGRAM ELEMENT NUMBER
FA8650-19-2-7931	N/A	62716E
5d. PROJECT NUMBER	**5e. TASK NUMBER**	**5f. WORK UNIT NUMBER**
N/A	N/A	Y20D

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8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)		10. SPONSOR/MONITOR'S ACRONYM(S)	11. SPONSOR/MONITOR'SREPORT NUMBER(S)
Air Force Research Laboratory Sensors Directorate Wright-Patterson Air Force Base, OH 45433-7320 Air Force Materiel Command United States Air Forces	Defense Advanced Research Projects Agency (DARPA/MTO) 675 North Randolph Street Arlington, VA 22203	AFRL/RYDI	AFRL-RY-WP-TR-2024-0011

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14. ABSTRACT
The aim of this project, in the phase 2, is to develop a high-frequency phase-locked loop circuit in GF 45nm RFSOI technology with a phase noise specification that is required to be lower than -100 and -120 dBc/Hz at 100 kHz and 1 MHz offset frequencies, respectively. A prototype circuit was designed and fabricated in the target technology, exhibiting -121 and -128 dBc/Hz, respectively, based on lab measurements. Some circuits for characterizing the technology were developed as well.

15. SUBJECT TERMS
RF mixed-mode devices, RF frontends, broadband mixed-mode circuits, phase-locked loop, SiGe BiCMOS circuits, low phase noise oscillators.

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES
a. REPORT	b. ABSTRACT	C. THIS PAGE		
Unclassified	Unclassified	Unclassified	SAR	97

19a. NAME OF RESPONSIBLE PERSON	19b. PHONE NUMBER *(Include area code)*
Aji Mattamana	N/A

PREVIOUS EDITION IS OBSOLETE.

STANDARD FORM 298 (REV. 5/2020)
Prescribed by ANSI Std. Z39.18

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1 OVERVIEW

The University of Utah has been one of the T-MUSIC performers. The main task of this team was to design very low-noise Phase Locked Loop circuits based on specifications that have been detailed in the program BAA. In addition, the team developed a few test structures to evaluate performance of transistors. In 2023, the team received some extra funding to commercialize the technologies that have been developed in the technical part of this project.

Two PLLs have been developed in this work, one per each Phase. In Phase I, a wide-band structure based on multi-phase phase detector circuits have been designed and fabricated in Tower Semiconductor 0.18 μm BiCMOS/SiGe technology. The PLL phase noise was measured to be -106 and -112 dBc/Hz at 100 kHz and 1 MHz offset frequencies, which passed the project requirements (-90 and -100 dBc/Hz at 100 kHz and 1 MHz offset frequencies). In Phase II, a double-edge sub-sampling PLL topology was developed. The PLL phase noise was measured to be -121 and -128 dBc/Hz at 100 kHz and 1 MHz offset frequencies, which passed the project requirements (-100 and -120 dBc/Hz at 100 kHz and 1 MHz offset frequencies). As a result, both designs could satisfy the defined specifications with enough margin.

As part of the commercialization effort embedded entrepreneurship initiative (EEI effort), an embedded entrepreneur was hired. His task was to evaluate the status of technology, communicate with potential customers and interested entities, and develop a proper business plan. In the context of this project, a company, named KratosIC was formed. Also, the team had meetings and discussions with a long list of companies, such as Analog Devices, Tower Semiconductor, Intel Labs, BAE, Microchip, Micron, Skywater, Synopsys, Renesas, Global Foundries, Analog Bits, Ripple Technologies, Silicon Technologies, Anikowave, Intel Foundry, and Texas Instrument. While almost all the companies agreed that our technology is outstanding, however their expectation was to have a more complete system (including transmitter and receiver components). Having said that, Intel Lab and Tower Semiconductor agreed to provide us test chip fabrication service, which will be critical for our STTR proposal. The team plans to submit a STTR project targeting a complete transceiver system in Intel 16nm and Tower Semiconductor 65 nm. In addition, the team has agreed to work with Synopsys on a test project, where a sample design will be designed, to demonstrate the efficiency of the algorithms developed by the team.

2 SUMMARY

The main objective of the T-MUSIC project is to enable disruptive RF mixed-mode technologies by developing high performance and high-speed analog integrated circuits together with advanced digital CMOS electronics on the same wafer. This approach will enable the implementation of the next generation RF mixed-mode interfaces with an unprecedented combination of wide spectral coverage, high resolution, large dynamic range, and high information processing bandwidth. Through the T-MUSIC program, DARPA seeks to: 1) advance RF and mixed-mode devices to support ultra-wide band RF frontends from HF to 100 GHz; 2) integrate those devices with high density digital CMOS electronics at the wafer scale to enable embedded digital intelligence; 3) develop and explore ultra-high resolution broadband mixed-mode circuit building blocks for DoD-relevant applications; 4) explore innovative device topologies and materials to implement THz devices in an advanced digital CMOS fabrication platform; and 5) establish a domestic ecosystem that facilitates enduring DoD access to differentiated capabilities for high performance RF mixed-mode SoCs.

Being part of the TA-1B program, the University of Utah's team has the responsibility to design, implement, and test a high speed PLL circuit with specified speed and phase noise characteristics, which are detailed in Table 1, shown for the Phase 1 and Phase 2 metrics. The scope of this project is to design very high-speed circuits and collaborate closely with TA1-A teams to assess the capabilities of their technology. Moreover, the goal is to develop new systems and circuit architectures that can expand the performance of key circuit building blocks, such as PLLs, beyond the state-of-the-art results.

Table 1: TMUSIC TA-1 Metrics

T-MUSIC		SOA Production	Phase 1	Phase 2
Objectives		FinFET CMOS, RF CMOS, SiGe BiCMOS	•Develop >350GHz transistors •Co-integration with CMOS •PDK development	•Develop >600 GHz transistor with ≤ 12nm CMOS •Ultra-broadband circuits
TA-1: Ultra-broadband Mixed-Mode Foundry Platform				
TA-1A Technology	Transistor f_T/f_{max} [a]	300/360 GHz (GF-US) 320/370 (ST-FR)	≥ 350/500 GHz	≥ 600/700 GHz
	Embedded Digital CMOS [b]	90nm CMOS (GF-US) 55nm CMOS (ST-FR)	≤ 90nm node ≥ 200 mm wafer	≤ 12 nm node ≥ 300 mm wafer
	PCM Yield Per Wafer [c]		50%	90%
TA-1B Building Blocks	Demo Circuit #1: ***PLL*** [d]	Phase Noise @ 30GHz (TowerJazz-US) < -91 dBc/Hz @ 100kHz offset < -97 dBc/Hz @ 1MHz offset	Phase Noise @ 30GHz < -90 dBc/Hz @ 100kHz offset < -100 dBc/Hz @ 1MHz offset **(Measurement)**	Phase Noise @ 30GHz < -100 dBc/Hz @ 100kHz offset < -120 dBc/Hz @ 1MHz offset **(Measurement)**
	Demo Circuit #2: ***ADC*** [d]	32 levels (5 ENOB[d]) @ 64 GSps , 20 GHz IBW[d] (20nm FinFET TSMC-TW)	Architecture simulation and building block demo **(Demo 16ENOB 1GSps ADC)**	≥ 256 levels (8 ENOBs) @100GSps, 50 GHz IBW **(Measurement)**
	Demo Circuit #3: ***Frequency Divider***	94 GHz input clock (Infineon-DE)	100 GHz **(Measurement)**	200 GHz **(Measurement)**
	Demo Circuit #4: ***Direct Digital Synthesizer***		***N/A***	≥ 256 levels (8 ENOBs) @50GSps, SFDR: 55dBc **(Measurement)**
	Circuit Yield Per Wafer [e]		50% (of divider)	90% (of ADC)

(a) *Proposal must define the test structure for extrinsic f_T and f_{max} to include practical parasitics of the gate and interconnect. f_T and f_{max} will be extracted from >20 GHz measurement*
(b) *The advanced CMOS node requirement for embedded digital circuits*
(c) *PCM: foundry-defined Process-Control Monitor (i.e. testers, transistors, 59-stage ring-oscillators)*
(d) *PLL: Phase-Locked Loop; ENOBs: Effective Number of bits; IBW: Instantaneous Bandwidth; ADC: Analog-to-Digital Converter; THA: Track-and-Hold Amplifier*
(e) *Within-wafer yield with more than 10 demo circuits per wafer*

		SOA Lab Demo	Phase 1	Phase 2
Objectives		SiGe BiCMOS, InP	•Develop new device structure	•Scale device and materials
TA-2: Fundamental: Advanced THz RF Mixed-Mode Devices				
	Transistor f_T/f_{max} [a]	500/720 GHz (IHP-DE)	≥ 600/600 GHz	≥ 1000/1000 GHz

In this context, the main Phase 2 tasks envisioned for the University of Utah's team includes design, implementation, and test of the following circuits in 45nm CMOS RFSOI technology provided by the Global Foundries (GF):

1) A 32 GHz PLL with a phase noise performance better than -100 dBc/Hz and -120 dBc/Hz at 100 kHz and 1 MHz, respectively.
2) Collaborate with the Global Foundry team to implement some process monitoring circuits, to evaluate technology performance parameters, mainly focused on device speed and noise. The test circuits include three different types of ring oscillators, all designed to oscillate at 1 GHz, where their specific operating points are different.

2.1 Overview

The main goal of this project is to explore advanced circuit and architecture techniques to improve capabilities of the modern clock and signal generators using PLL systems. Operating speed, as well as phase noise are the two main key design specifications for this research work. PLL-based clock and signal generators are widely used in RF transceivers, as LO (Local Oscillator) generators. The specifications envisaged for this project are targeted for advanced applications such as 5G wireless systems.

Table 2. Critical Metrics to Define Success (Phase 1 and Phase 2)

	Phase 1	Phase 2
PLL	Frequency 30 GHz PN < -90 dBc/Hz @ 100kHz offset PN< -100 dBc/Hz @ 1MHz offset	Frequency 30 GHz PN < -100 dBc/Hz @ 100kHz offset PN< -120 dBc/Hz @ 1MHz offset

Table 2 summarizes the main specifications targeted for this project. To achieve these specifications, a modified PLL architecture with proper circuit design schemes are being proposed:

- Use matrix PLL architecture that increases the granularity of the feedback correction rate in time. This technique allows to have a more adequate phase error correction at higher bandwidth. The extra available bandwidth can be traded with some other design parameters such as lower jitter peaking (jitter amplification) and higher loop phase margin, if needed.
- Sub-sampling phase detector is to eliminate the phase noise of feed-back dividers.
- A programmable multi-phase phase comparator, that can be adjusted based on target specifications (e.g., low phase noise, or high bandwidth)
- Optimal loop design, to minimize the phase noise coming from the loop filter components, at a desired bandwidth.
- Use C/IDS design methodology to minimize power dissipation of the PLL building blocks for the given speed and phase noise targets. C/ID design methodology was developed by the University of Utah's team to optimally design CMOS and FinFET circuits to optimize their power dissipation when a specific noise and speed is targeted [1].

The two major tasks of this project are:

T1: Design and test of the demo circuit #1: Phase Locked Loop (PLL).

A complete PLL system, including input buffer stage, sub-sampling phase detector (PD) array, charge-pump circuit (CPC) and/or transconductor array, loop filter, voltage-controlled oscillator (VCO), frequency lock assist (FLA) with its frequency dividers, and output buffers for monitoring and measuring the VCO and PLL outputs, will be designed, implemented, and tested in the target process technology node. A combined transconductor/PD array will be developed that can operate at 1 GHz speed using 45 nm RFSOI technology. Also, the transconductor/CPC array will be used to implement the target multi-phase array PLL. The programmable transconductor/CPC will allow us to compare the performance of PLL in two different configurations: (1) conventional single-edge structure, (2) double-edge array phase detector topology. Figure 1a illustrates the Phase 1 implementation, while Figure 1b shows the detailed block diagram of the proposed Phase 2 PLL.

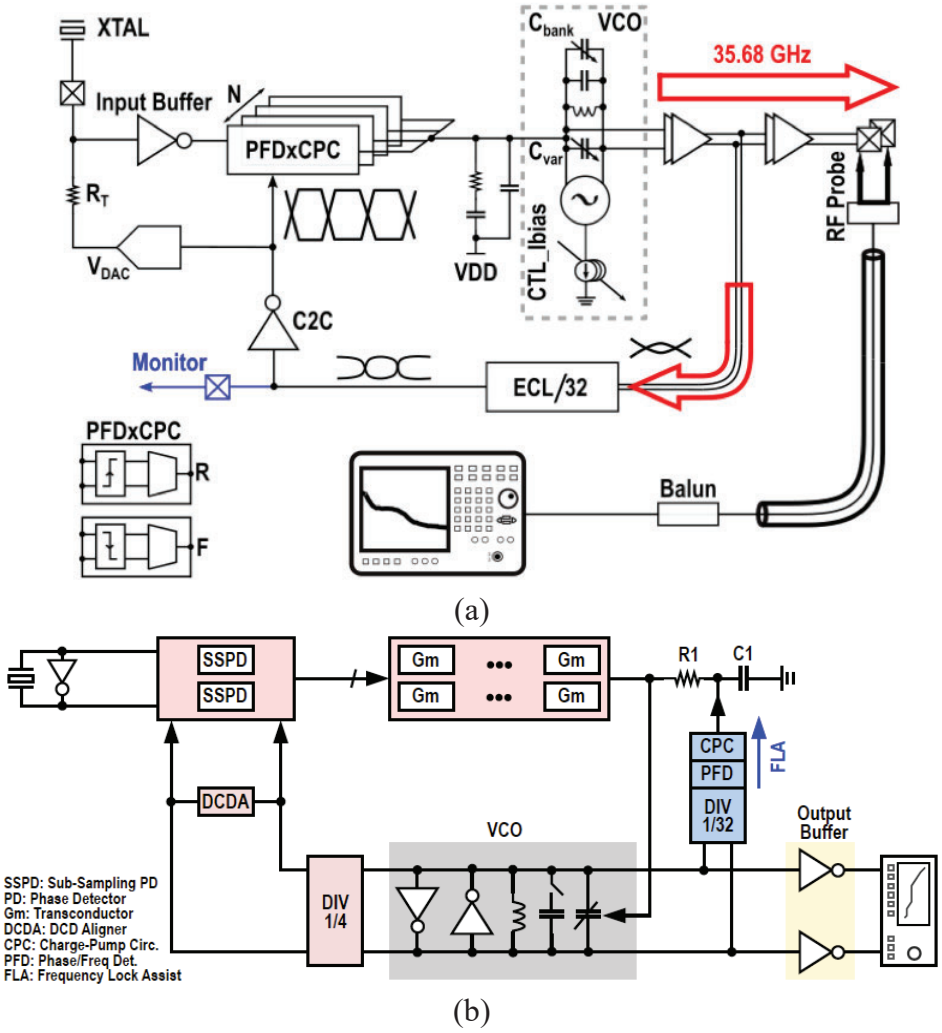


Figure 1: (a) Detailed Block Diagram of the Phase 1 PLL Circuit, An Array of PFD/CPC Blocks was Designed to Implement Both Single- and Double-edge PLL Topologies, (b) The Proposed Phase 2 PLL Architecture, Including the FLA Block

T2: Design process control monitor Circuits (PCMs) in collaboration with TA-1A team, GF. The aim of this task is to explore the maximum operating speed (f_t and fmax) of devices in the target technology. Different types of oscillators will be implemented for this study, such as CML ring oscillators, to study the speed of FET devices.

A high-speed and low-noise PLLs, using sub-sampling matrix phase-detector concept, will be designed, and tested. An array of ring oscillators, based on different topologies, and different types of devices (NMOS, PMOS, NPN), with and without inductive peaking, will be designed and implemented. Extensive lab experiments will be performed to measure the performance of the building blocks, and analyze their speed, noise, and sensitivity to process variations.

The period of the Phase 2 project is determined to be 24 months, with 3 extra months for reporting. The University of Utah's team, including the PI and two graduate students to design, model, simulate, prepare layout, provide test plan, run lab experiments, and prepare final report. To achieve the target specifications for the PLL circuit, an LC PLL circuit using matrix phase detector was developed in Phase 1. Based on the proposed approach, the phase correction occurs multiple times in each reference clock period and thus the noise of VCO and the loop filter can be corrected more accurately. To enhance the performance of Phase 1 PLL, and satisfy Phase 2 requirements, the architecture of the existing double-edge sampling PLL will be used as a basis, while the topology of the phase detector will be modified to a sub-sampling structure to eliminate the noise of feedback dividers. This modification has been proposed after lab experiments and transistor level simulations showed that divider circuit is the major source of phase noise in the Phase 1 design.

Table 3 summarizes the main architecture level choices for Phase 2.

Table 3: Summary of the Phase 2 Architecture Details

Item	Proposal/Target
Type of VCO	LC VCO, using SiGe transistors for lower phase noise
Feedback Architecture	Matrix feedback topology, to increase the time domain granularity, expand the PLL bandwidth, and minimize the phase noise of the forward path components.
Phase Detector	Sub-sampling phase detector, aiming to minimize the phase noise coming from the feedback divider circuits.
Charge-Pump/Transconductor	A low-noise discrete-time transconductor
Output Buffer	High-speed, inductive peaking buffer stages will be used to probe the 30 GHz output signal.
Frequency Lock Assist	To assist the PLL with initial lock achievement, a PFD based PLL will be employed.

During the technical performance period, Utahs' team completed the following efforts:

(i) Design and model the PLL architecture.
(ii) Circuit design (PLL and test VCO circuits).
(iii) Layout and verification of the circuits (PLL and test VCOs).
(iv) Taping out the designs (two designs) for fabrication.

(v) Developing the necessary PCBs for testing the chip.
(vi) Preparing foot-print and bonding diagram for the chip-on-board process, communicating with company who will do the chip on board,
(vii) Communicating with companies who will provide the rental equipment,
(viii) Working with the company which has fabricated our RF probes to make some fine adjustments.
(ix) Running the test and lab experiments.
(x) Analyzing the experimental data.

3 METHODS, ASSUMPTIONS, and PROCEDURES

3.1 Fundamental Concepts

To address the project requirements within the expected margins, we propose the following design methodologies:

1. PLL:
    - Matrix sub-sampling phase detector-based architecture, combined with optimally designed loop filter, that can suppress the low-frequency circuit noise and high frequency XTAL (reference) noise.
    - Extensive high-level behavioral modeling and simulations to find an optimal design.
2. PCM:
    - Design and implement a set of ring oscillators, designed for a target speed, with different methodologies to evaluate effectiveness of the proposed approach. Three oscillators were design to oscillate at 1 GHz, with different operating points (high, low, and optimum gm/ID values).
    - A methodological design procedure is being proposed to maximize the circuit bandwidth and speed for a given power budget. This approach can be exploited to estimate device speed in the target technology node.

As performance of the target circuits directly depends on device model, the PCM circuits acts as a very good measure to evaluate precision of device modeling (e.g., noise, parasitic elements, device inherent speed, etc.)

3.1.1 Top-Level PLL Topology:

The schematic of the proposed PLL is shown in Figure 1b. At the heart of this PLL lies a double-edge sub-sampling PD that enables implementing a matrix structure. The multi-phase PD is supported by an array of transconductor/CPC circuits, which are programmable. The rest of the system is very similar to the conventional PLL topologies, including an LC VCO, feedback divider chain (part of divider, not a full divide-by-32), the loop filter, as well as an input buffer circuit, with tunable duty-cycle. The circuit will include multiple observation (probing) points, e.g., at the output of VCO (32 GHz), and after the dividers (4 GHz).

Figure 1a shows the top-level PLL circuits, including the phase detector, VCO, output buffers, and the FLA circuit. RF probes have been utilized to measure the output of the PLL (the VCO output), after buffering that. The oscillation frequency of the PLL was measured to be 29 GHz.

3.1.2 Sub-Sampling Phase Detector

Sub-sampling PLLs (SS PLL) were developed to minimize the noise contribution from electronic components in the feedback path (i.e., feedback dividers). The existing sub-sampling phase detectors are mainly based on transmission gates. This project aims to develop a very high-speed sub-sampling phase detector (SS PD), that can compare the reference clock phase directly with the VCO output phase, operating at 32 GHz. This way, the entire divider path together with their phase noise will be eliminated. The schematic of such a SSPD operating at the rising edge and falling edge is showing in Fig. 2 and its layout with input AC couple is detailed in Fig.3.

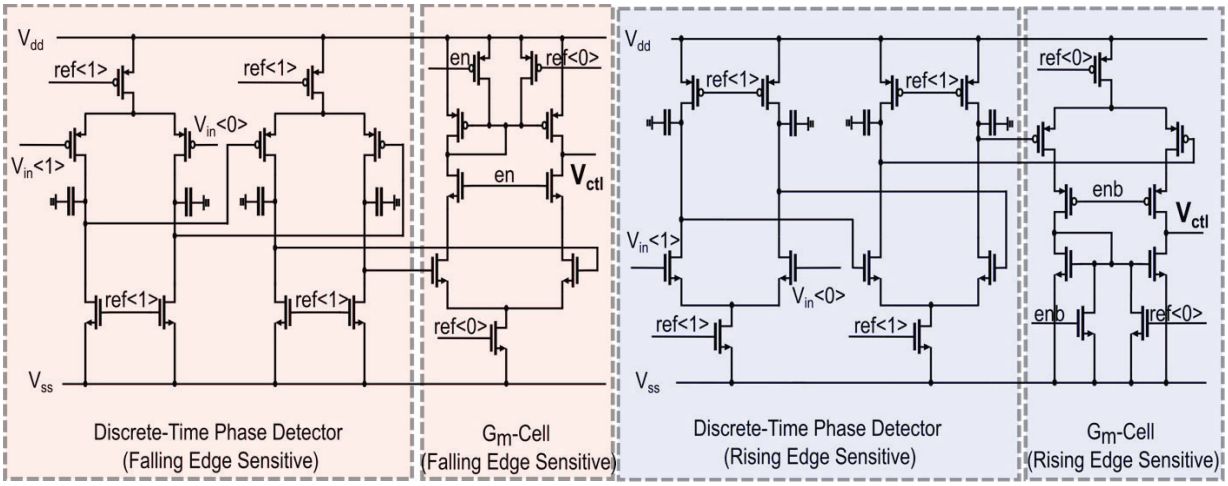


Figure 2: Circuit Diagram of the Discrete-Time Phase Detector

The discrete time operation consists of two different modes: (i) Reset mode and (ii) Mission mode. In the reset mode, all the transistors are reset so that no memory/hysteresis effects are retained, and the phase detector gets ready for a phase comparison for the next cycle. In the mission mode, the phase detector converts the phase difference between VCO signal and reference signal to a fixed voltage difference. The major attractive part of the discrete time design is that the two operation modes prevent direct rail-to-rail current flow and thus the overall consumption of the phase detector can be greatly reduced. A gm cell is attached at the output of the phase detector cell which reads the voltage difference provided by the phase detector and generates current output accordingly. This current is finally pumped to the loop filter and control voltage of VCO gets corrected according to the phase mismatch.

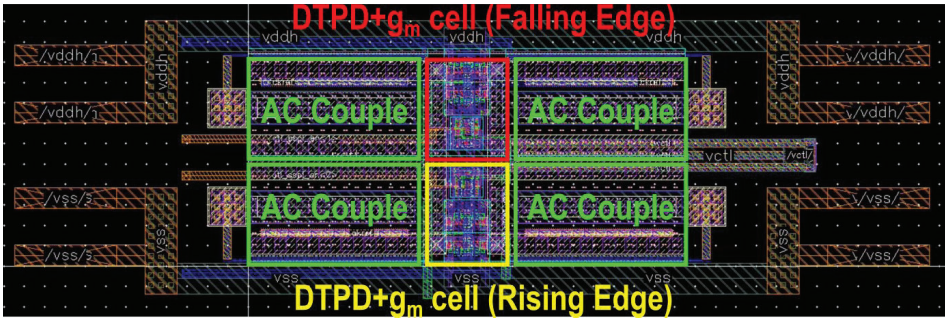


Figure 3: Layout of the DTPD & Gm Cell Incorporating AC Couple

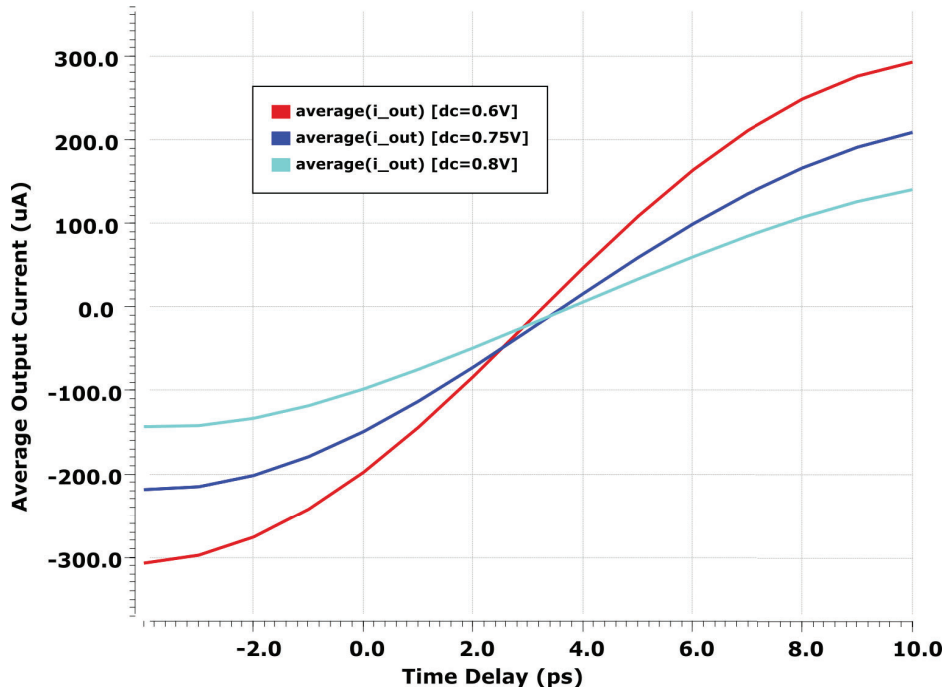


Figure 4: DTPD and Gm Combined with Transfer Function at Different DC Bias Values

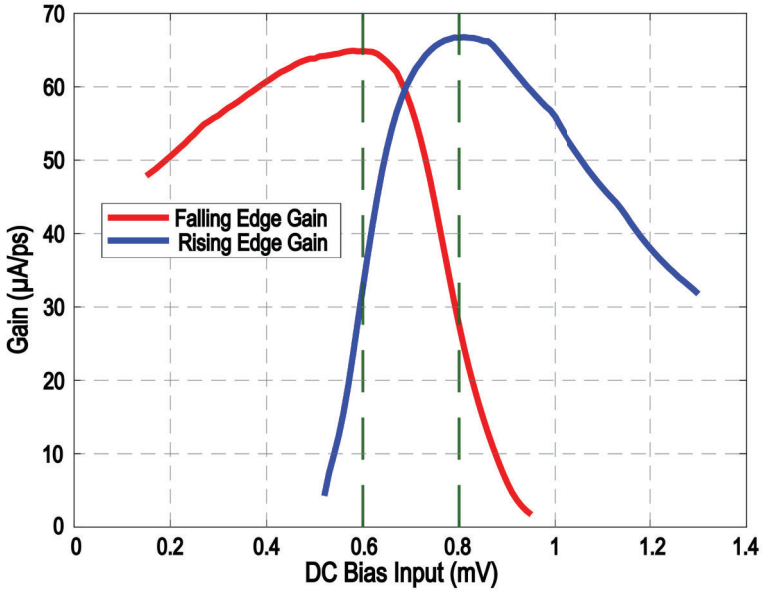


Figure 5: Rising/Falling Edge DTPD Gain with Respect to the DC Bias Input

Fig. 3 shows the layout of the DTPD and Gm cell. For internal power grids, BA and BB layers have been used. For the AC couple, ndsilresx and mimhdx have been used. Fig. 4 and Fig. 5 shows the wide tunability for gain adjustment from the DTPD and Gm cell with a requirement of DC enforcing DAC at the input of DTPD.

3.1.3 Voltage Controlled Oscillator

An LC VCO with BJT/SiGe cross couple devices was designed. Resonating with a single turn coil is a bank of capacitors for fine tuning the center frequency and a varactor for continuous fine control. SiGe devices are used to reduce the PN and loading, allowing the coil to have a larger capacitor budget. To minimize PN, a tail resistor bank is used a with a MOSFET switch for bias current control.
Schematic:

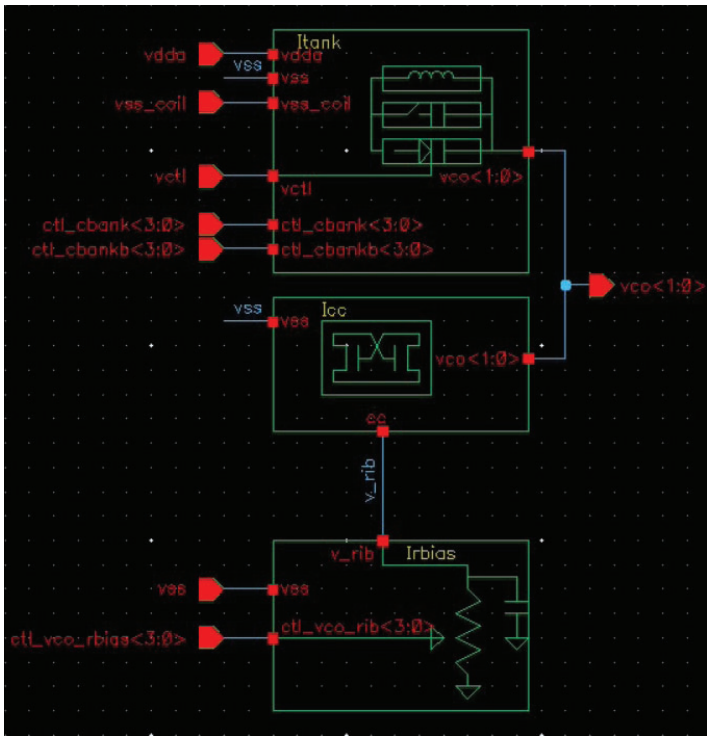


Figure 6: VCO schematic

- Uses BJT cross-coupled devices.
- Bias current controlled using a resistor network.
- "Symmetric Parallel Rectangular Spiral Inductor" from PDK used for the coil.
- Center frequency of tank is programmable (4b) with bank of "High Q MiM" capacitors.
- "Hyper-Abrupt Varactor" diodes used with DC biasing network for fine frequency control.

Layout:

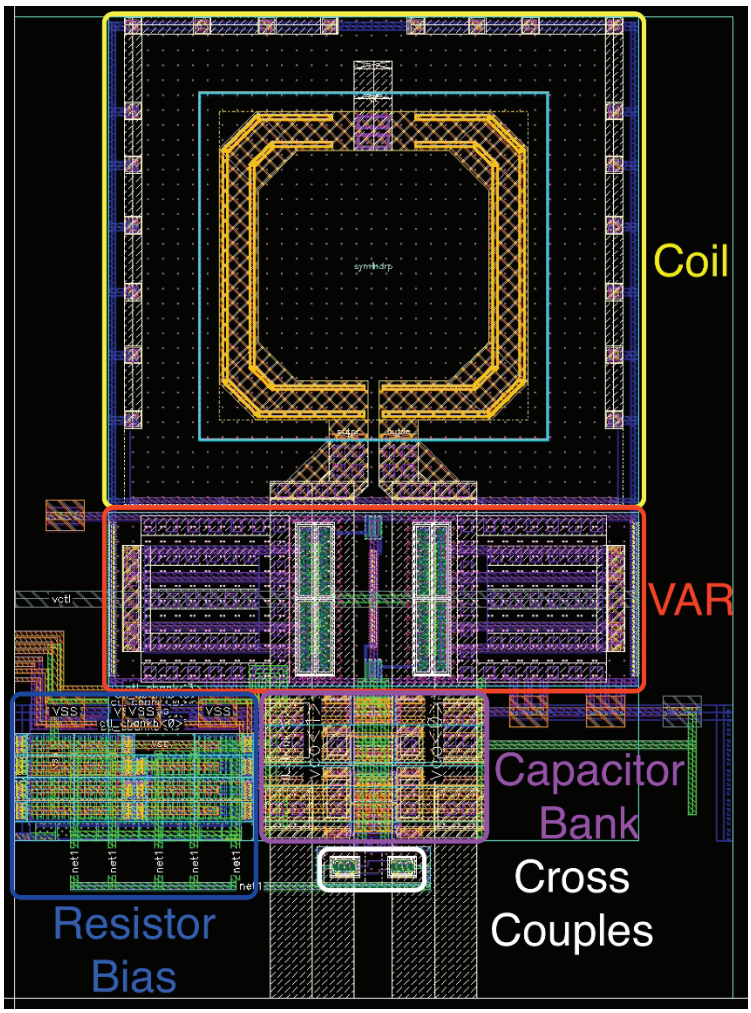


Figure 7: VCO Layout

Resistor Bias:

- Bias current controlled using resistors to reduce close-in noise.
- Control range: 4b [2.4mA to 9.6 mA]
- Smallest resistance slice made static without control/switch to remove largest source of noise at 100 kHz from VCO.

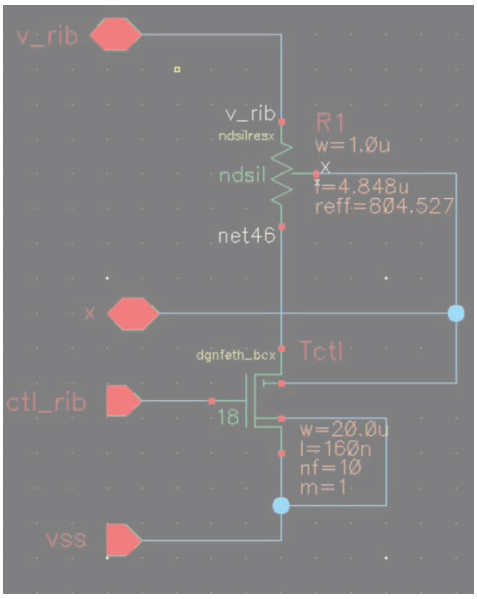


Figure 8: Resistor Bias Cell

Cross Couples:

- BJTs used as Cross Couple devices.
- "npnhp" BJTs devices used.

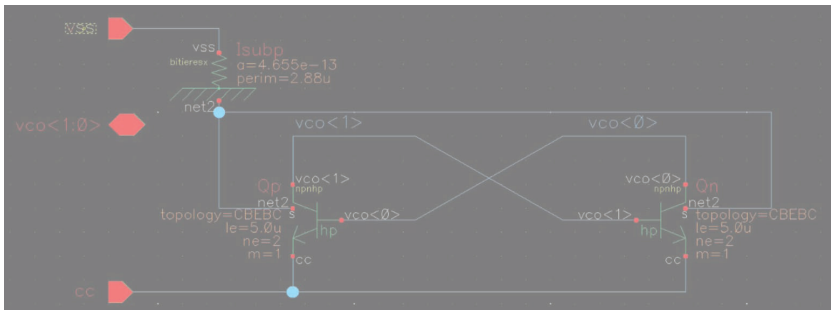


Figure 9: VCO Cross Couple

Coil:

- Inductor: "symindrpx"

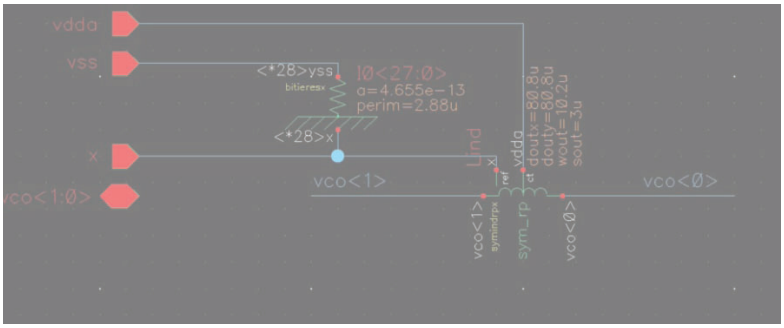


Figure 10: VCO Coil

Capacitor Bank:

- Capacitor Bank: “mimhqx”
- x2, x4 and x8 cells made with multiple copies of x1 block [shown in Fig. 12].
- Respectively adding up to 10fF, 20fF, 40fF and 80 fF to the 270 fF.

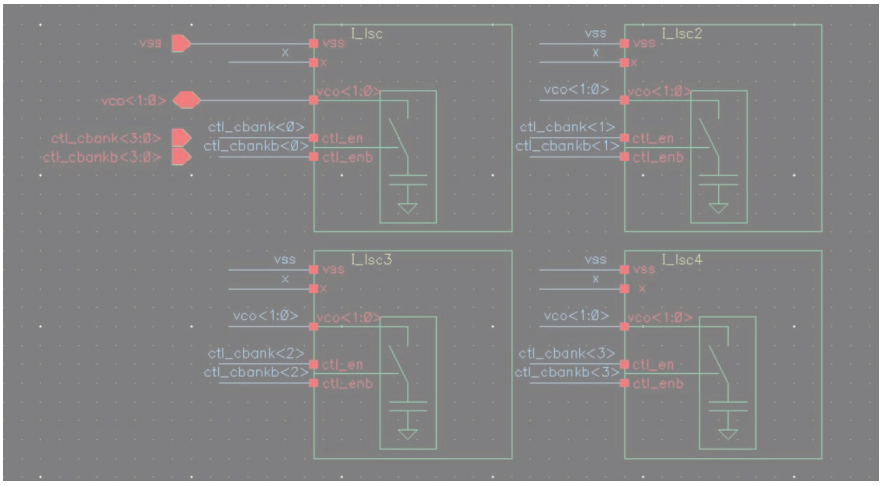


Figure 11: VCO Capacitor Bank

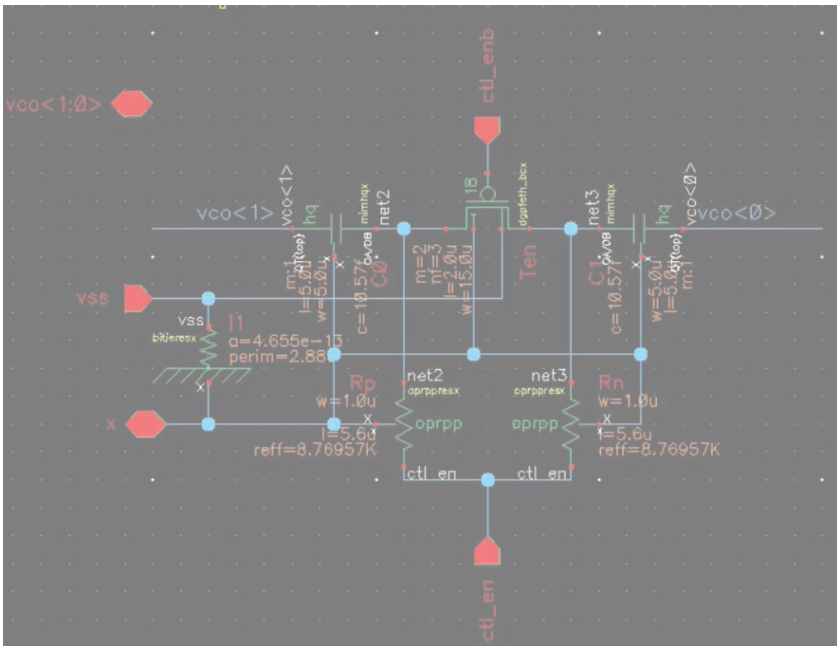


Figure 12: VCO Capacitor Bank Cell

Varactor:

- Varactor: “havarx”
- Additional DC Biasing added to improve linearity range of VCO.
- VSS chosen as DC biasing voltage.

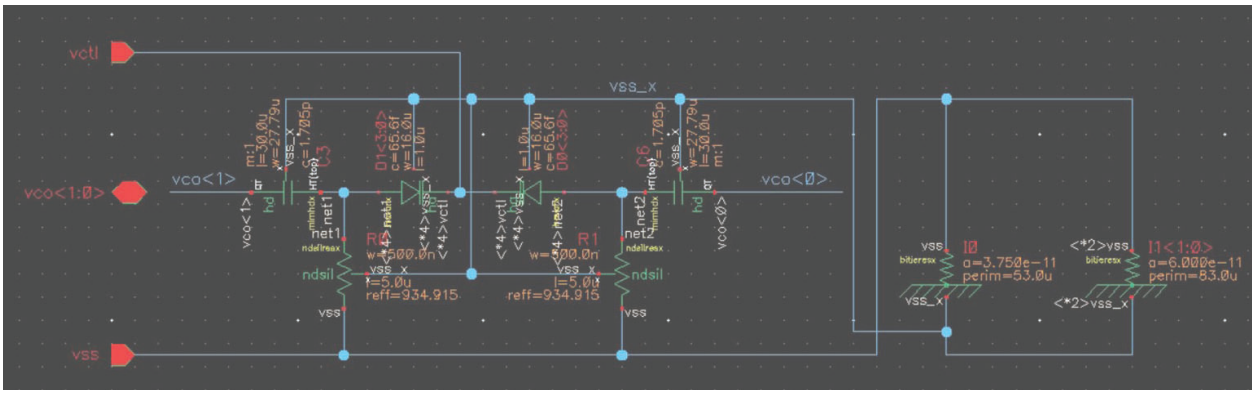


Figure 13: VCO Varactor

Performance:

VCO	Schematic Simulation		Post-Layout Simulation		Measurement	
Frequency Range	28 GHz – 36 GHz		30.75 GHz – 32.88 GHz		25 GHz – 29 GHz	
Offset Frequency	100 KHz	1 MHz	100 KHz	1 MHz	100 KHz	1 MHz
Phase Noise	-81.74 dBc/Hz	-101.6 dBc/Hz	-79.43 dBc/Hz	-99.44 dBc/Hz	-80 dBc/Hz	-102 dBc/Hz
Output Swing	1.23 Vppd (for best Phase Noise)		1.18 Vppd (for best Phase Noise)		- (cannot measure without buffer)	
	0 mVppd - 1.6 Vppd (full control range)		50 mVppd – 1.45 Vppd (full control range)			
I consumption	5.73 mA (Best PN)		6.5 mA (Best PN)		6.41 mA (Best PN)	
Kvco	4.8 GHz/V		3 GHz/V		2 GHz/V	

Figure 14: VCO Performance Simulation and Measurements

3.1.4 Loop Filter

The loop filter is required to have two operation points, one for the SS-PLL and one for the standard PLL loop during startup, Frequency Lock Assist. For this reason, the loop filter had to be made programable.

- Configurable Loop Filter designed with 2 effective R1 values.
- Enables PLL to remain stable both SSPLL only and FLA only operation modes.

Schematic:

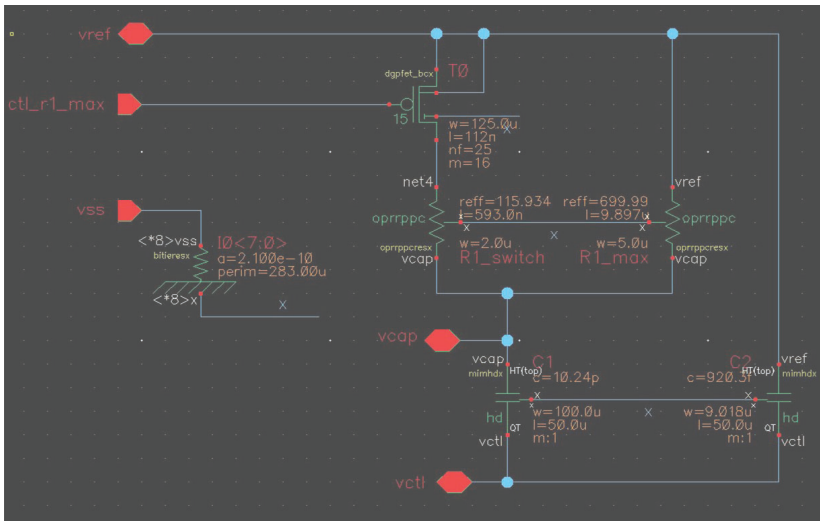


Figure 15: Loop Filter Schematic

Layout:

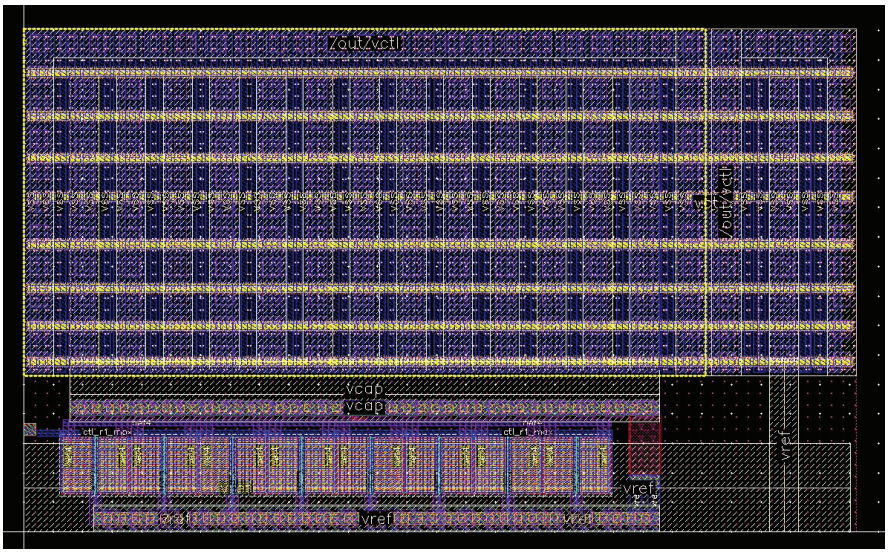


Figure 16: Loop Filter Layout

3.1.5 Frequency Lock Assist

In general, any SS PLL suffer from very limited frequency lock range. Thus, a frequency lock assist (FLA) circuit will be required for the initial lock acquisition process. The plan of record for this project is to design a second loop, assisting with frequency lock, with an adequate dead-zone. The FLA circuit includes a set of dividers and charge-pump circuits to bring the initial value of the VCO control voltage to the right value. Fig. 1 from section 2.1 shows the simplified block diagram of the FLA circuit.

3.1.6 High-Speed Buffers

High-speed buffers have been developed to probe the VCO outputs at 32 GHz. A three-stage buffer has been implemented to drive the external 50-Ohm loads. DC blockers will be used on the test board to avoid deteriorating the biasing point of output buffers during measurement process.

3.2 PCM Circuits:

Multiple CML ring oscillators have been designed based on C/IDS methodology to demonstrate the fundamental capabilities of the FET devices in GF 45nm RFSOI technology.

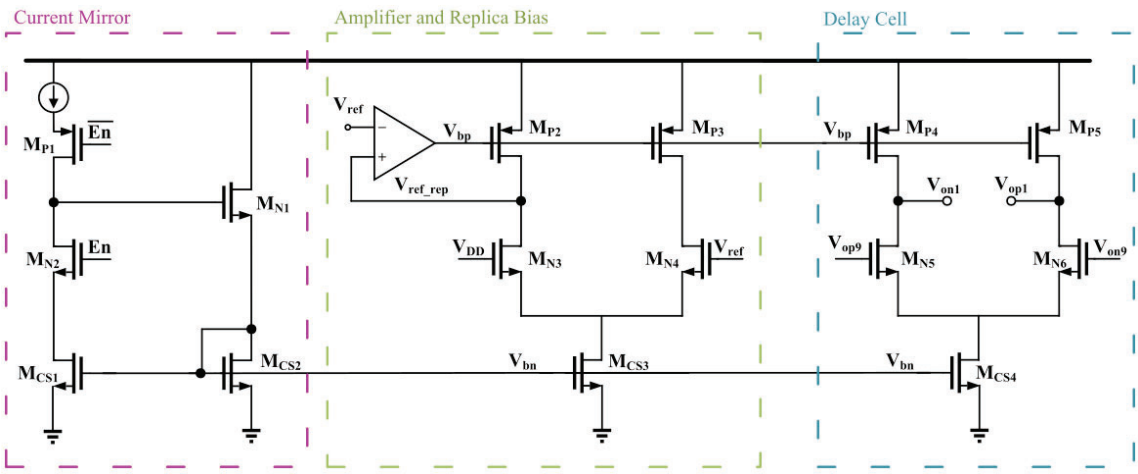


Figure 17: Biasing and the Delay Cell of the PCM Circuit

Three different oscillators have been implanted with different Kgm settings (High Kgm, Low Kgm and Optimal Kgm).

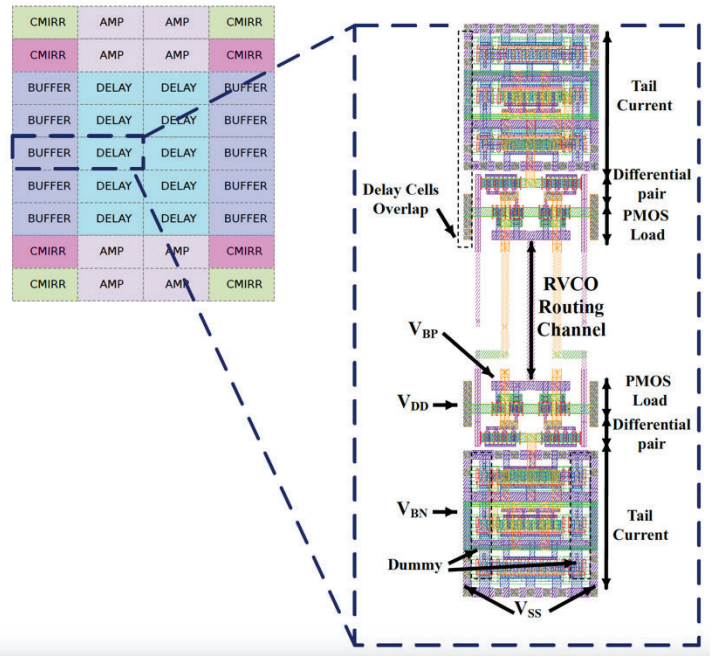


Figure 18: Layout of the Delay Cell and its Buffer

3.3 Top-Level Test Chip:

Fig. 2 shows the top-level block diagram of the target test chip. Different building blocks, including SSPLLs (different versions) and the ring oscillators have been placed on the test chip, as depicted in Fig. 19. It features the SSPLL with calibration (or wire bonded, WB-PLL) and without calibration (or stand alone, SA-PLL) along with the PCM blocks.

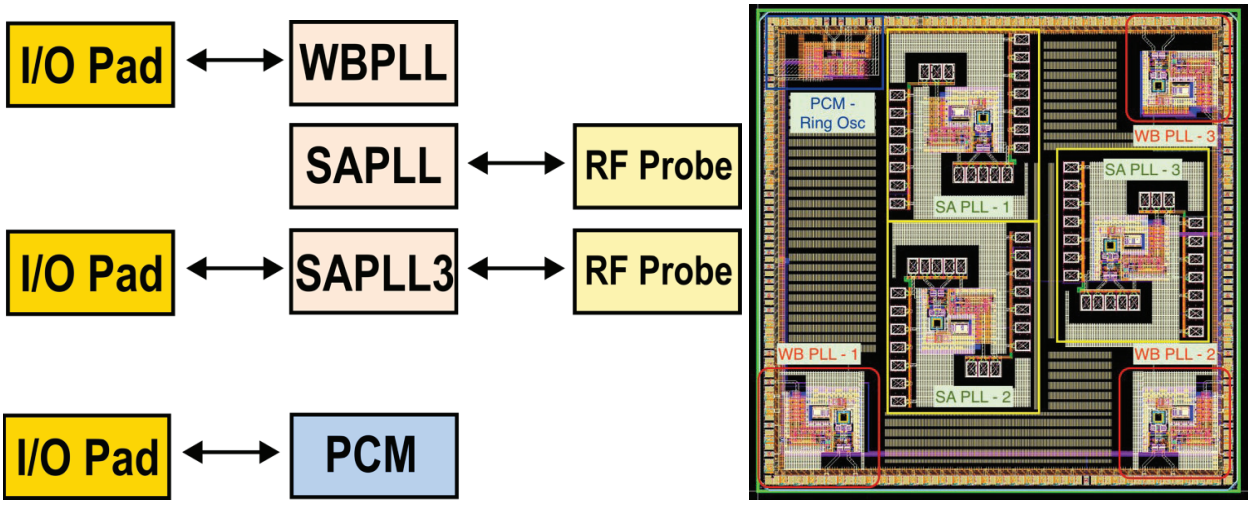


Figure 19: The Top-level Block Diagram of the Test-chip, Including Building Blocks Measured either Through I/O Pads, or RF Probes

4 RESULTS AND DISCUSSIONS

The fabricated samples were used to run lab experiments with the top-level of the test structure shown in Fig. 20. To perform the target tests, the die was mounted on a small PCB (called daughter board), using chip-on-board (CoB), technique. This approach allows to apply bias and control voltages directly from board, and at the same time use an RF probe to measure the high-speed output signals of the PLL. Moreover, there is no need to package the dies when CoB technique is used. A main board, called mother board, is used to deliver the bias and control signaling, including the supply voltages, calibration, and control signals. Also, there is the possibility to measure some of the critical on-chip analog signals, such as bias current and bias voltages. The calibration signals are generated using custom protocol through an Analog Discovery board, which is level converted in the mother board. A separate PCB was used to generate the reference current, specifically for the RF probe card. Below provides more details regarding the test structures and test results.

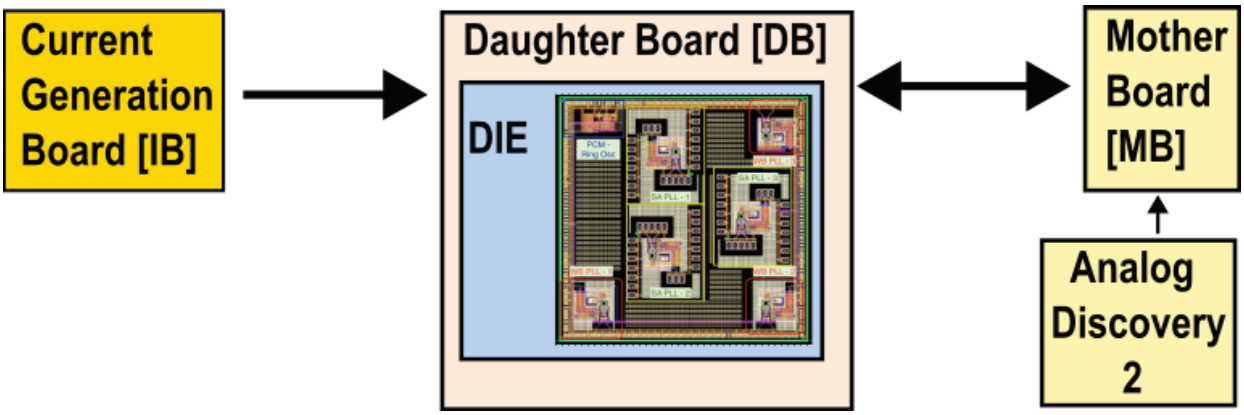
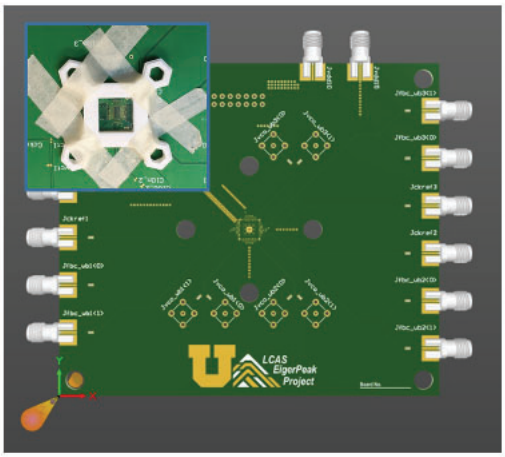


Figure 20: Test Setup Overview

4.1 Daughter Board

A high-speed and well-designed board is required to run the core tests for PLLs and the ring-oscillators. Fig. 21 illustrates the board that has been designed for this project. The core chip will be mounted over PCB using Chip-on-Board (CoB) technique. The plan is to have two different types of wire-bonding: with and without glob-top. The boards where chip is mounted without glob-top can be used with the RF probe station to monitor some high-speed signals. The boards which include dies without glob-top need a special protection. A plastic cover, implemented using 3D printers, will be utilized to protect the die and bond-wire from any intervention. The board needs to be designed very carefully having all signal integrity requirements in mind. All high-speed signals will be fed or monitored using SMA connectors.



- RF 4 GHz board
- Chip on board (CoB)
- Can be tested using RF probe (a plastic fixture will be added)
- Will be used for debugging, phase noise measurements
- Signal integrity requirements

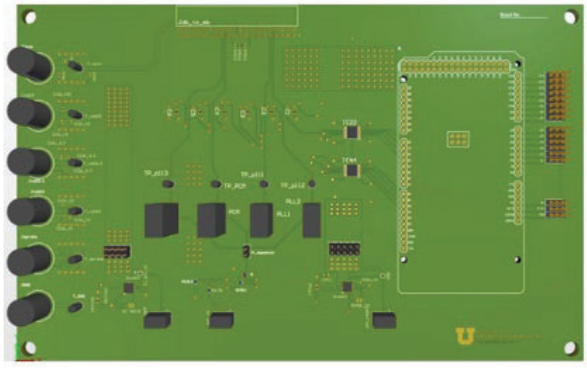
Figure 21: Top View of the Daughterboard Developed for this Project

4.2 Motherboard

While the test chips will be mounted on daughter boards, a single motherboard will be used to produce the necessary biasing and controlling signals. All supply signals are also provided by the mother board. Tunable regulators have been employed to produce the required supply levels. All bias currents are also produced using accurate resistors and are tunable. A microcontroller is used to enable communication with the test chip, and program it. The chip can be placed in different modes, such as ring-oscillator tests, PLL tests, leakage current measurement mode, among others. Also, each mode includes several sub-sets, in which the details characteristics of the circuits can be configured and programmed. Examples are different types of ring-oscillators or PLLs, loop filter control, bandwidth control.

The Daughterboard's key feature is the Chip-on-Board (COB) design. This PCB has the test die positioned at the center which is secured using a conductive epoxy to the exposed metal of the PCB. The test die is then further connected to PCB metal traces via wire-bonding. This bonding diagram allows proper control on test structures, located on the test dies. One distinguishing detail is the option for multi-wire bond the test dies High Speed outputs located within the I/O ring of the die. Three rings of wire-bond pads surround the test die and are arranged to permit a smaller distance of wire-bonds to the high-speed inputs and outputs, which terminate in either an SMA or SMB connection. Supply Filter Capacitors are used to minimize exterior noise and are located on the underside of the PCB as close to the test die as possible. Control Voltages (Supply and Digital) Currents and IO clocking is managed through a single bus header that connects to the Motherboard. Additionally, a 3D printed shield can be placed over the exposed test die without crushing the wires for easier handling. This shield will need to be removed for RF

testing, however. A 3D printed bottom plate ensures a smooth surface and protection, while allowing grip utility for a vacuum platen on probe stations.
Though motherboard will include only biasing and low-speed signals, the PCB layout has been made very carefully to avoid any noise coupling through crosstalk, and IR drop effects. Fig. 22 shows the top-view of the designed motherboard.



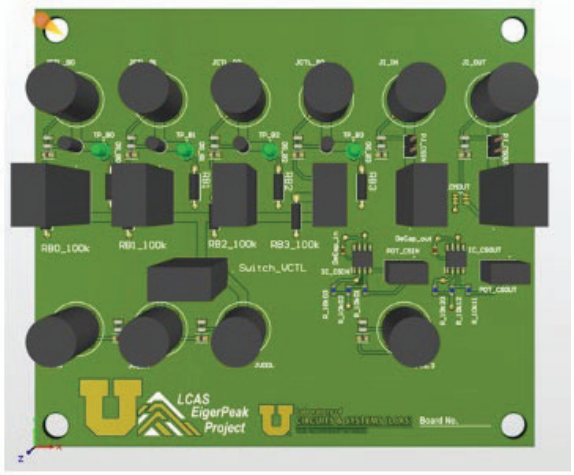
- Main board
- Micro controller
- Bias generator
- Control signal for the test chip
- Supply generator (controllable supply)

Figure 22: Top View of the Motherboard, to be used for Biasing and Controlling the Components on Daughter Board
An Adafruit Grand Central M4 Express featuring the SAMD51 will be used to produce the controlling signals.

4.3 RF Board

A dedicated PCB is needed for RF Probe Station based measurements. The stand-alone blocks on each die need low-noise supplies, bias current, as well as a few controlling signals. High-speed RF probes will be used to feed the input reference clock to PLLs, and measure (observe) the PLL outputs. The goal of these experiments is to measure the phase noise of PLL at the speed, i.e., 32 GHz. Fig. 23 shows the top-view of the designed PCB board, that has tunable bias current, control logic signal generators, and supply voltages. The signals will be fed into an L-shape probe card using SMA connectors.

The RF Probe PCB controls the immediate inputs surrounding the interior test die landing pads. This board provides control voltages and currents to a pair of RF pico-probe needle arrays. These control features consist of a double level voltage supply, four-bit digital control outputs and a pair of adjustable reference current outputs. The current outputs are distinguished by the direction of current provided, i.e., toward the test chip or taken out. The tuning range for the reference currents runs from |50μA – 1mA|. Each output has a toggle switch and indicator light for the benefit of the end user.



- RF 32 GHz board
- Measurements using RF probes
- Generates bias / control signals

Figure 23: Top-view of the RF Board to be used for Probe-Station Based Experiments

4.4 Chip-on-Board and Bond-Wire

Most of the debugging and the preliminary measurements will be performed using the daughterboard, explained in Section 4.9.9. To mount the dies on PCB, a CoB approach has been selected. Fig. 24 illustrates the bonding diagram and the footprint of the CoB scheme. The details of the bonding diagram have been checked with the company who is going to do CoB. The material at the interface to the PCB, footprint on the PCB, all have been designed and checked with the corresponding manufacturing parties. As both test chips have the same pin-out, one PCB and one bonding diagram will be sufficient for the corresponding experiments.

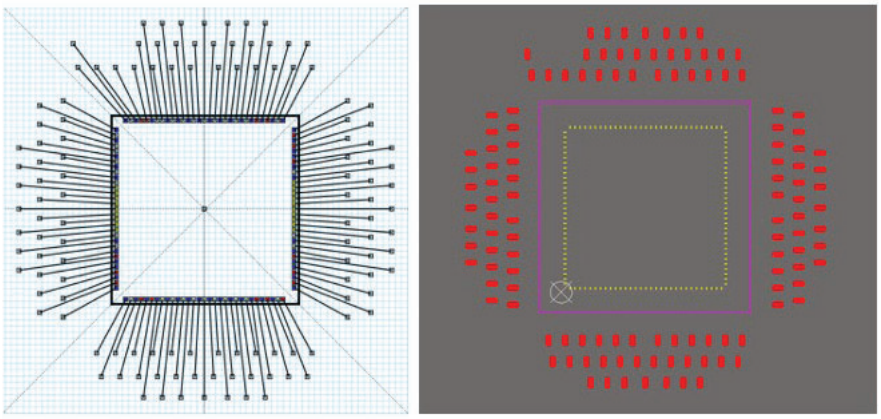


Figure 24: Bonding Diagram (left) and Footprint and Landing Diagram of the die (right)

4.4.1 Daughter Board

The daughter Board was ordered and verified. A bug in the daughter board was observed. The daughter board is to sit on the probe station and be held in place with a vacuum. As the board has soldered components, a flat surface was not available for the vacuum to work. To resolve this, a 3D printed base was made in-house at the University of Utah, to hold the board in place while offering a flat surface for the vacuum to work.

4.4.2 Mother Board

The Mother Board was tested and exhibited a couple of bugs for usage. The SMD components used proved to be very small for soldering by hand and the oven available was not able to solder the components satisfactorily. In addition to this the control mechanism planned to use a microcontroller proved to be complicated. Developing new tests showed to have a time significant overhead cost, which is predicted to be at a premium once testing is in full swing. To resolve both issues, a new motherboard was designed with easier to solder components as shown in Fig. 25. This board was redesigned to work with the Analog Discovery module. The Analog Discovery is a waveform and pattern generator and with its companion GUI, enables very quick modifications to the calibration code sent to the PLL during testing. Following this the new version of the mother board was ordered and verified to be satisfactory.

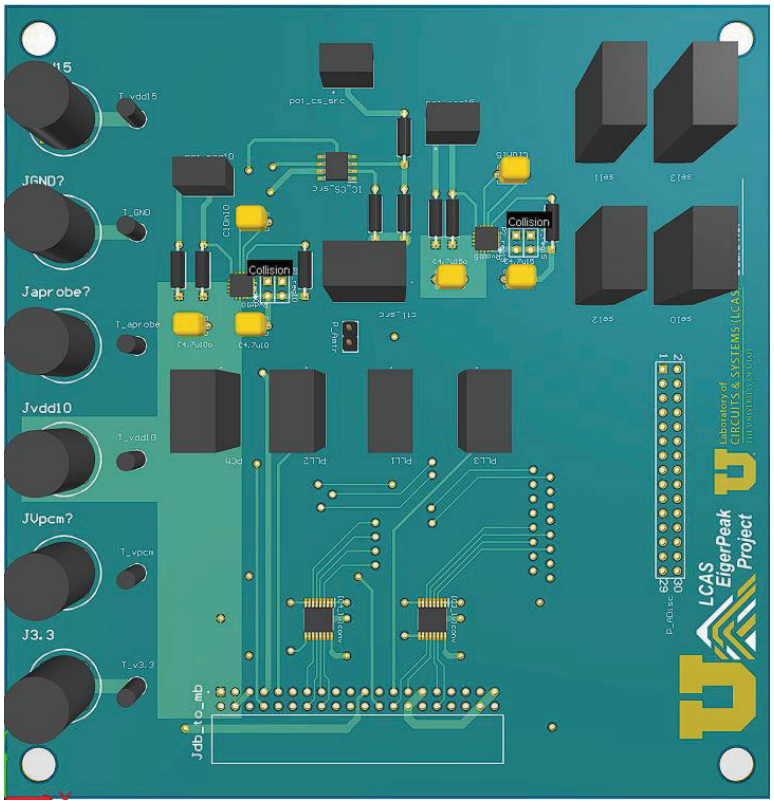


Figure 25: Redesigned Mother Board to Work with Analog Discovery

4.5 Test Equipment Rental

The PLL designed was simulated to exhibit the ability to lock to several reference frequencies and synthesize at very low PN. For verifying this in measurements, an equally low noise reference and phase noise analyzer was required. The R&S SMA 100 B signal generator with the B711 low noise option was selected to fit in this category and the R&S FSWP 50 with B60 option was chosen as the PNA. To rent these for a month, several companies were contacted as one was not available at the UofU. Together as their monthly rental was above the $10,000 limit, purchasing department of UofU was involved and a bidding conducted. Completing the documentation and procedure, the equipment necessary was arranged for the time the test samples get delivered.

4.6 Probe Modifications

The RF probes available were tested and a complication was predicted. During testing, the sample is planned to the chip-on-boarded and calibrated using a digital control bus. Once calibrated, RF probes are to be used to measure the performance of the PLL. But landing the RF probes with the calibration bus connected implies the probes will require a large angle of attack to make space for the other wiring. To resolve this, the RF probes were sent back to the manufacturer and the angle of attack was increased as shown in Fig 26.

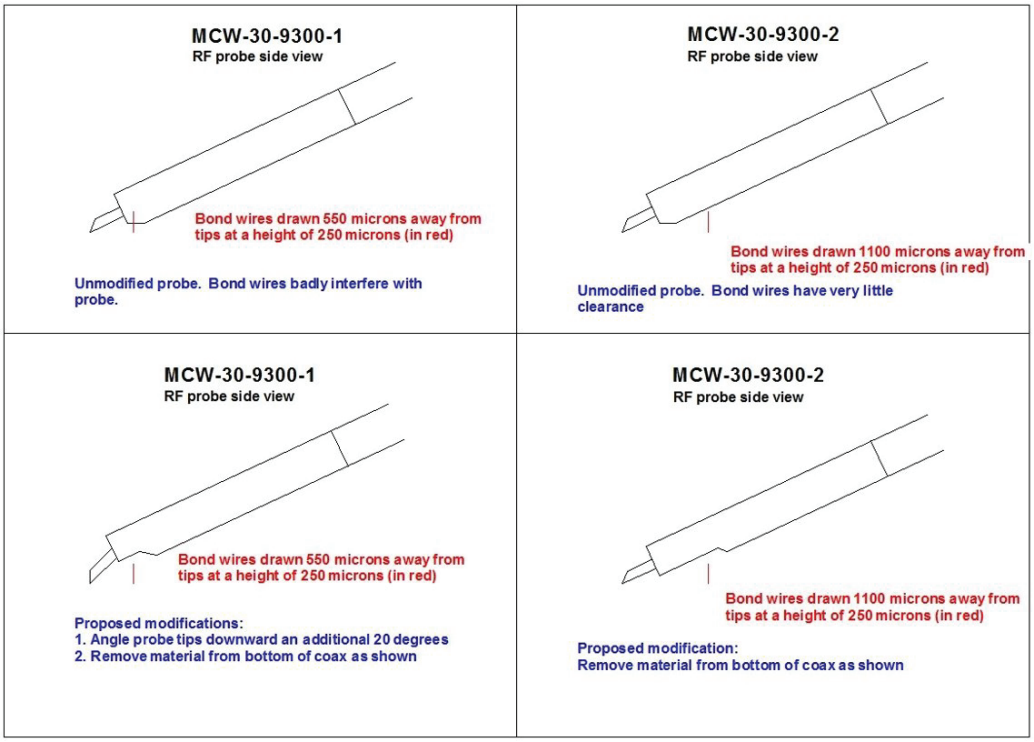


Figure 26: Proposed Modifications to the Probes to Increase the Angle of Attack

4.6.1 Soldering PCBs

Once the PCBs were tested and verified to be satisfactory to be used in the measurements, the components were soldered on all the manufactured PCBs.

4.6.2 Verifying Probes

The modified probes were verified to be satisfactory by landing them on substrate with all additional cables connected simulating the actual testing environment.

4.6.3 PLL Test Planning.

Extensive planning was done to test the PLL and measure all desired metrics as detailed in Fig. 27.

	Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Reference Characteristics	Input Frequency Range		-	-	-	-	CCSO-914X-1000.000 product has been used for test setup of the PLL
	Single Ended Mode		-	1		GHz	Single ended sinusoid is converted to CMOS rail-to-rail wave through an input buffer
	Temperature Range		-40	40	85	℃	
	Input Voltage		4.75	5	5.25	V	
	Frequency vs Temperature		-	150		PPM	
	Input Current		-	25	35	mA	
	Output		-	-	-		True Sine Wave
	Output Power		-	8		dBm	50 ohm load
	Start Up Time		-	2	10	ms	
	2nd Harmonic		-	-20	-15	dBc	
	DC		-	-	-	-	DC to be set internally, coupling capacitor required to decouple internal and external DC voltages.
Control Inputs	Voltage Domain		0.9	1	1.2	V	All control codes are connected to 1V domain
Power Supplies	Digital Control Power		0.9	1	1.2		Supply used by digital control unit only
	Analog Power		1.3	1.5	1.8	V	Both FLA and SSPLL operate at 1.5V domain. The VCO requires 1V which is generated internally through a regulator
VCO Characteristics	VCO Frequency Range		30.75	32	32.88	95.63	Fundamental VCO Range (With Varactor alone)
			29	32	34	GHz	Fundamental VCO Range (With Varactor+Cbank)
	VCO Sensitivity, Kv		1	3	3	GHz/V	K_vco drops below 800 mV
	Output Swing		0.4	1.18	1.45	Vppd	For best PN
	Current Consumption		2.4	6.5	9.6	mA	For best PN
	Control Voltage Requirement		0	600	1.45	mV	For best PN
Noise Characteristics	PLL Phase Noise Performance			-110		dBc/Hz	100 kHz offset from 32 GHz carrier [Single Edge Mode]
				-122		dBc/Hz	100 kHz offset from 32 GHz carrier [Double Edge Mode]
				-120		dBc/Hz	1 MHz offset from 32 GHz carrier [Single Edge Mode]
				-128		dBc/Hz	1 MHz offset from 32 GHz carrier [Double Edge Mode]
	Integrated Jitter (XTAL only)			4.5		fs-rms	Reference XTAL rms jitter integration bandwith (10 kHz-100 MHz)
	Integrated Jitter (SSPLL only)			20.95		fs-rms	In mission mode, FLA is turned off; rms jitter integration bandwidth (10 kHz-100 MHz); reference is considered noiseless
	Integrated Jitter (Total)			21.42		fs-rms	Integration bandwidth (10 kHz-100MHz)
SSPLL Bandwidth	Single Edge			235		MHz	Phase detection and correction happens only in a single edge [either rising/falling]
	Double Edge			380		MHz	Phase detection and correction happens both edge [rising & falling]
Jitter peaking	Single Edge			6.9		dB	Increased Peaking due to sub sampling action in the PLL transfer function
	Double Edge			6.4		dB	Increased Peaking due to sub sampling action in the PLL transfer function
Current Consumption	SSPLL			20		mA	In mission mode, only SSPLL operates
	FLA			120		mA	At startup, FLA is required to reach the target frequency
	Divider			80		mA	Divider used only in FLA Mode
	PFD			5		mA	PFD used only in FLA Mode
	CPC			15		mA	CPC used only in FLA Mode, including up/down calibration amp, all programable current mirrors and draining current paths.
	Fast Buffer			20		mA	2 stage output buffer, second with 50 Ohm loading to drive to pad.
	VCO			10		mA	Core of VCO
	Discrete-Time Phase Detector			1		mA	2 stage Integrators working as Phase Detectors
	Input Buffer			15		mA	2 Stage CMOS Input buffer and DAC for Duty Dycle Control
	Bias Block			2		mA	Universal Bias Current Generation Block
	Regulator			10		mA	Dedicatd Voltage regulator for VCO to isolate supply induced noise and bias first stage of output buffer
	DAC (Falling DTPD)			3		mA	DAC to set common mode of Falling edge sensitive Phase Detector
	DAC (Rising DTPD)			3		mA	DAC to set common mode of Rising edge sensitive Phase Detector

Figure 27: PLL Test Plans

4.6.4 Setting up Analog Discovery and Generating Calibration Codes

The Analog Discovery module was ordered, and testing was done on it to get familiarized with it. All possible planned scenarios for testing the PLL were listed, and calibration codes needed for all situations were generated and verified.

4.6.5 Chip-on-Board Structure

Once the fabricated sample was delivered, the appropriate variants were chosen and sent out to be Chip-on-boarded. Once this was done, the rest of the components were soldered onto the daughter board to finish preparing it for testing.

4.6.6 Test Setup

Testing of the PLL was performed in a combined RF-calibrated mode. Supply and calibration signals were provided through custom designed PCBs and the RF signals probed using high speed probes. Fig. 28 shows the setup used with some real-world pictures for reference.

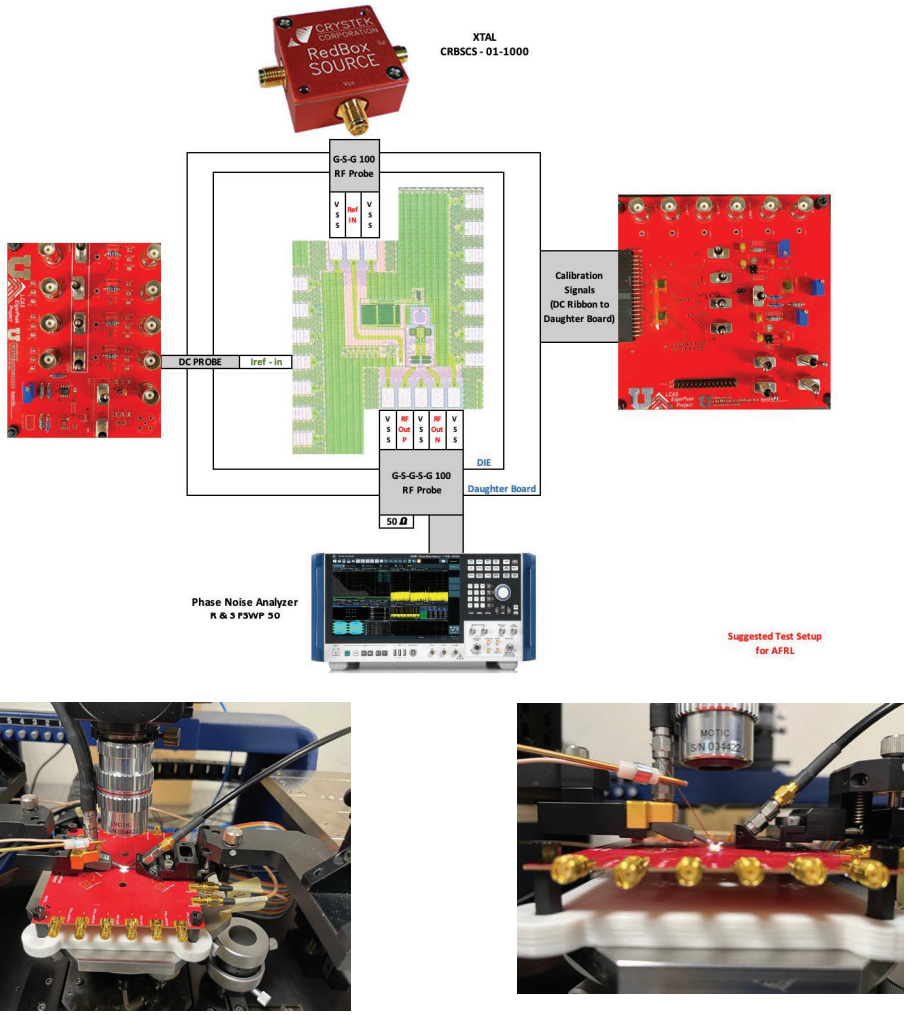


Figure 28: Test Setup

Test Setup Overview:

- Unit-Under Test (UUT) mounted on the daughter board PCB with chip-on-board connections for supply and calibration.
- Standard SMA cables connected to the daughter board used for supply connections, additional connections, shorted internally, for low resistance connection to supply.

- Mother board used in tandem, through ribbon, for calibration and additional supply connection.
- DC Needle used to supply reference current as shown in Fig. 29.
- RF Probes used to send-in reference clock and tap VCO signals as shown in Fig. 29.

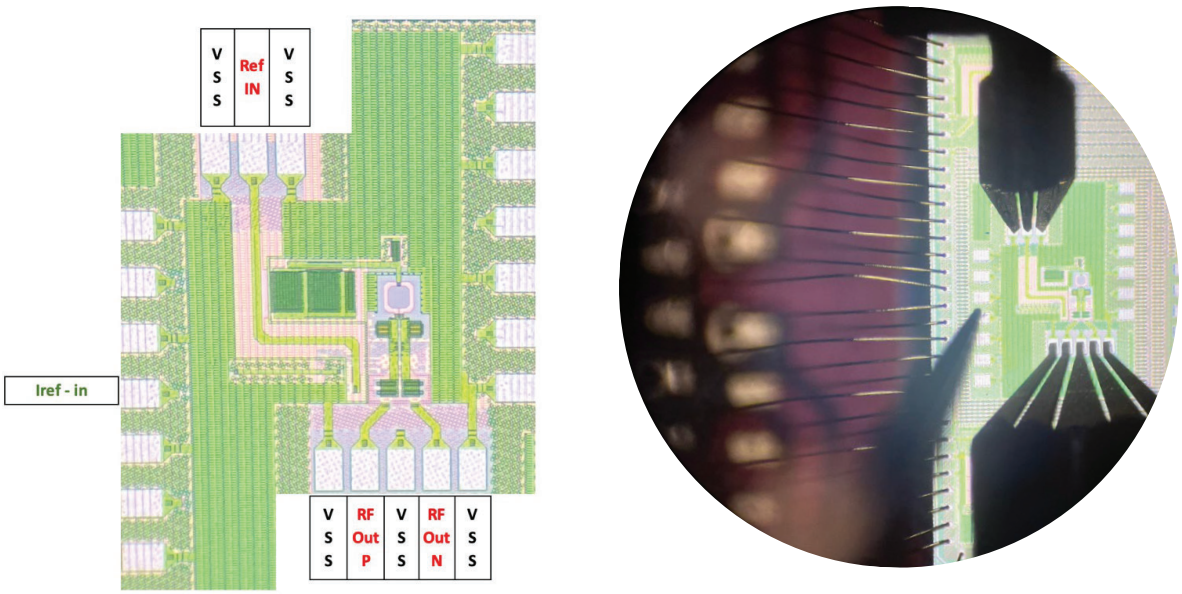


Figure 29: Probe Connections and RF Signals

4.6.7 Components:

- UUT, PLL die:
  - Bare Die sample
  - Chip-on-board sample [daughter board]
- Test PCBs
  - Daughter Board (DB)
  - Mother Board (MB)
  - Reference Current Generation Board (IB)

4.6.8 Unit-Under Test (UUT):

Fig. 30 shows the full fabricated die with the PLL in multiple test configurations. For the main PN and spectral measurements the highlighted PLL offering calibration capability and RF pads will be used.

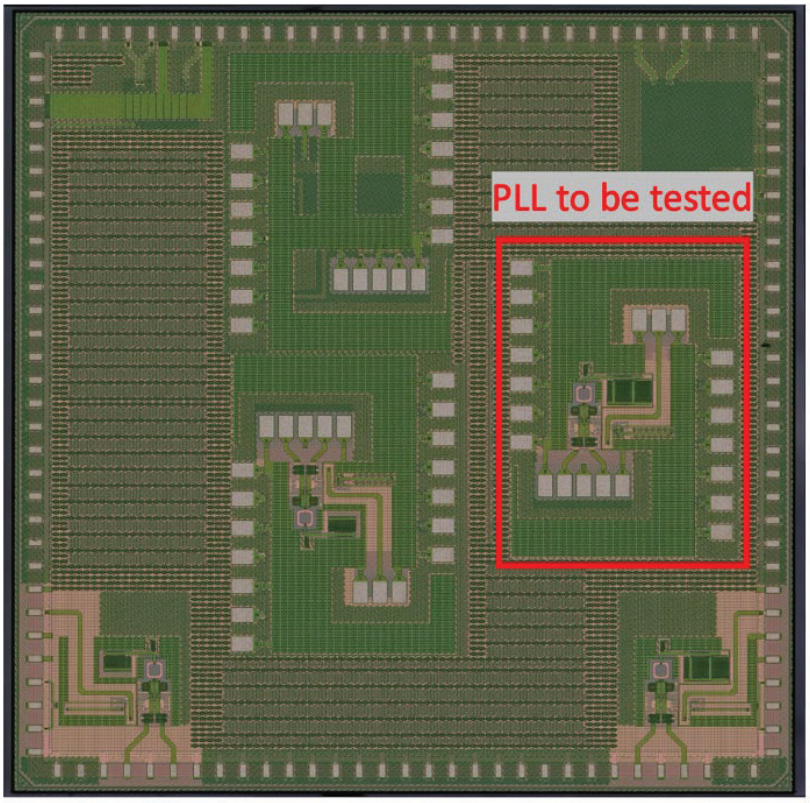


Figure 30: Full Die showing PLL to be Tested

4.6.9 Daughter Board (DB):

Contains the mounted UUT only with corresponding I/O. Necessary connections for testing are as the following:

- Supply; Jvdd10 = 1 V [North Right].
- Supply; Jvdd15 = 1.5 V [North Right].
- Ground; shielding and calibration bus.
- Calibration Bus [North Left]

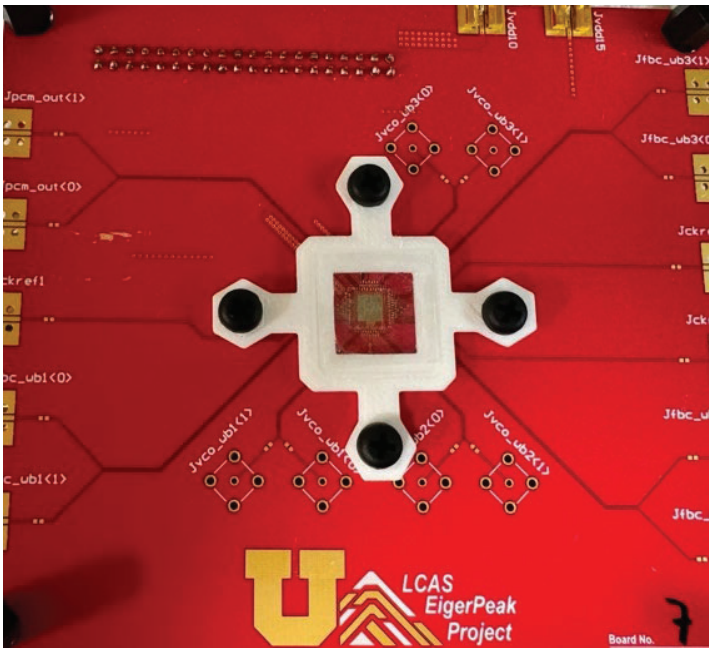


Figure 31: Daughter Board

4.6.10 Mother Board (MB):

Used to interface with the Analog discovery device, including the level shifter required, that controls the UUT. Includes switches to choose the PLL to be tested.
Necessary connections for testing are as the following:

- Supply; Jvdd10 = 1 V [North]
- Supply; Jvdd15 = 1.5 V [North Right]
- Supply; J3.3 = 3.3 V [North Left]
- Ground; Jgnd [North Right]
- Digital Bus-in [South Left]
- Calibration Bus-out [West]

Switch Configuration; 0011 [South Right]

- Sel12: Switch off, toggle Left (vss, 0)
- Sel11: Switch on, toggle Right (vdd, 1)
- Sel10: Switch on, toggle Right (vdd, 1)
- Sel13: Switch off, toggle Left (vss, 0)

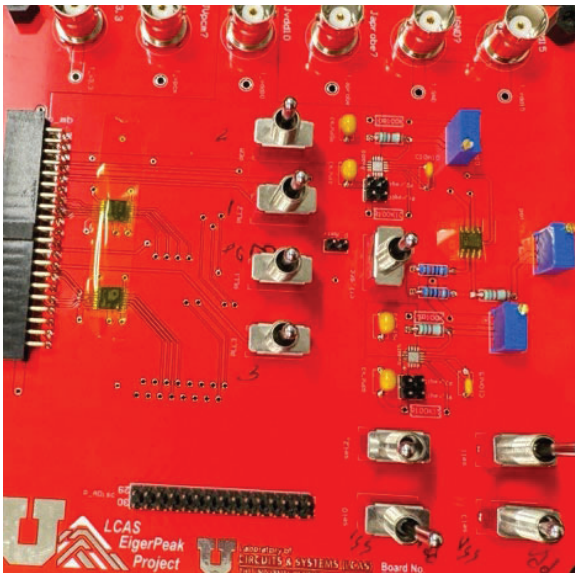


Figure 32: Mother Board

4.6.11 Reference Current Generation Board (IB):

Used to generate the reference current required and delivered through the DC needle.
Necessary connections for testing

- Supply; J3.3 = 3.3 V [South Right]
- Ground; Jgnd [South Left]
- Current Output; Jisrc [North Right]

- Pot used for tuning; “pot_cs_src”
- Necessary Selection for testing
- Switch Configuration: ctl_src [Toggle Left]
- Ammeter can be attached in series between the switch and the Jisrc BNC port using the provided hooks.
- If hooks are unused, they need to be shorted.

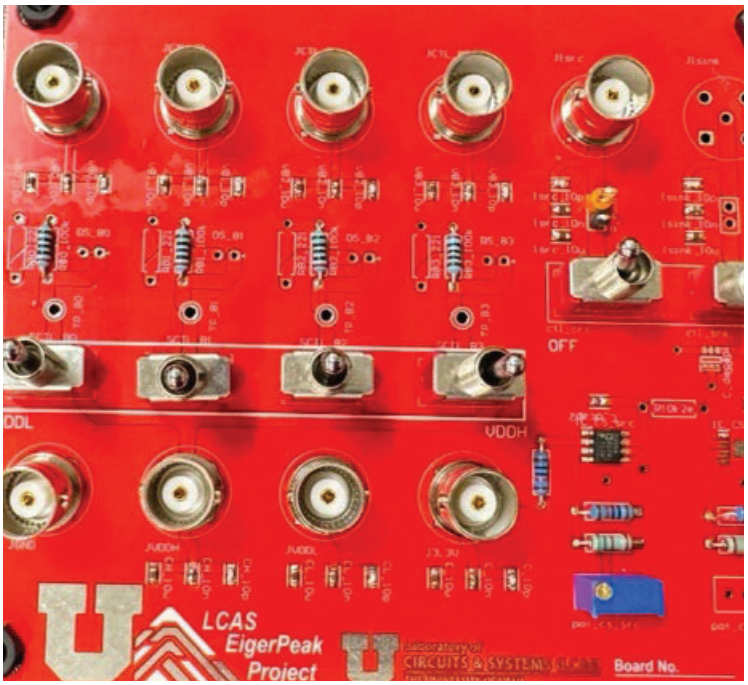


Figure 33: Reference Current Generation Board

4.6.12 Equipment List:

List of all equipment, connectors, and cables to be used.

Probes

- Pc: Custom L – Shaped probes [Same as Phase 1]
- Ps: G-S-G 100 um pitch probs; x1
- Pss: G-S-G-S-G 100 um pitch probs; x1
- Pdc: DC Probe, 20 um – tip; x1

- SMA Cables
  - W1: 2.92 mm 40 GHz cables (M-M); x3 [Same as Phase 1]
  - W2: Standard SMA cables, > 4 GHz (M-M); x1
  - W3: Standard SMA cables (M-M); x2
  - W4: Standard BNC cables (M-M); x6
- Converters
  - C1: 2.92 mm (F) – to – 1.85 mm (M); x1
  - C2: 2.92 mm (F) – to – Standard SMA (F); x2
  - C3: Standard SMA – to – BNC; x5
  - C4: BNC – to – Banana; x9
  - C5: BNC – to – BNC; x1
- Other Components
  - Cdc: 2.92mm DC Block (F-F); x3
  - C50: 2.92mm 50 Ω cap (F); x1 {or SMA 50 Ω cap with C2}
- Calibration Bus
  - D1: Digital Bus jumpers
  - D2: Calibration Bus Ribbon
- AD: Diligent Analog Discovery

- XT: CRBSCS-1000 XTAL [Standard SMA (F)]

PNA: FSWP-50 Phase Noise Analyzer with B-61 low PN option [1.85 mm (F)]

4.6.13 Connections:

Fig. 34 shows all the connections needed for performing the testing with the equipment and connectors previously listed and labeled.

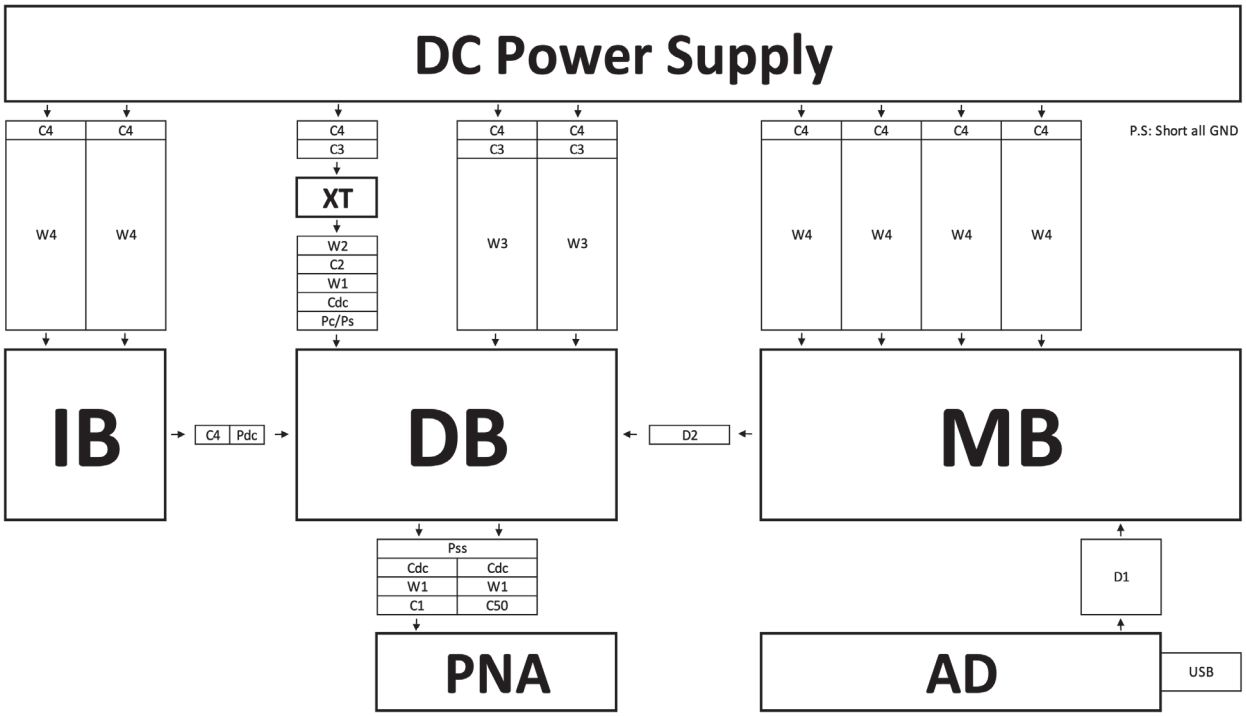


Figure 34: Full Setup Connections

4.6.14 Test Set-up Flow:

1. Connect the XTAL to the power supply using C4-C3.
2. Connect the XTAL to the probe using W2-C2-W1-Cdc.
3. Connect one of the outputs of Pss to the PNA using CDC-W1-C1 and terminate the other output using CDC-W1-C50.
4. Feed the XTAL signal using probe Ps on to the pad as shown in Fig.34.
5. Probe the RF output of the PLL using Pss with the pads as shown in Fig. 34.
6. Make Supply connections to MB using C4-W4 as shown in Fig. 34.
   3.3V, 1.5 V, 1V, GND.
7. Make Supply connections to DB using C4-C3-W3 as shown in Fig. 34.
   1.5 V, 1V.
8. Make Supply connections to IB using C4-W4 as shown in Fig. 34.
   3.3V, GND.
9. Connect the calibration bus from MB to DB using D2.
10. Connect the output of the IB using W4 and probe using Pdc to the pad as shown in Fig. 29.

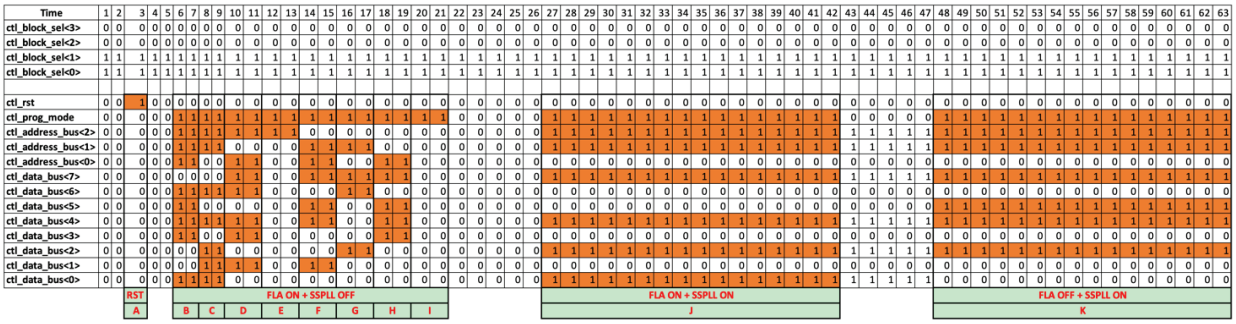
4.6.15 Digital Control:

Control of the UUT is done through an analog discovery module and its companion GUI. The UUT is designed with an 8-bit register bank that controls all the calibration points of the PLL. Upon receiving a high on the "ctl_rst" line, these registers are set to a default state where all blocks are turned off on all PLLs. To perform calibration, the register controlling the intended block is selected using the 3-bit address bus, the code to be fed into the register is enforced on the 8-bit data bus and the control block is put in the program mode by raising "ctl_prog_mode" compelling it to read the data in. Depending on the 4-bit "ctl_block_sel" the desired PLL is programed. Fig. 35 below shows for example the full PLL start-up sequence. Starting with a reset, all blocks are programed on by one, the PLL runs in FLA mode to acquire the frequency lock and the PLL is moved to the SS-PLL mode.

All the required control lines are produced using the digital I/O signals of an analog discovery module shown in Fig. 36. Fig 37 shows how each of the signals are mapped to the address/data bus and prog_mode/rst flags.

PLL control procedure:

- Download the software from the following link: https://digilent.com/reference/software/waveforms/waveforms-3/start.
- Reset and start up files for testing provided.
- Open the provided file, select the connected AD device and hit "RUN" on the GUI.



A	reset everything to the default codes so that everything is turned off			
B	if(ctl_prog_mode == 1) writes group 7-q7	ctl_data_bus<7:0>=<01111001>	ctl_cbank<3:0> = <0111>	ctl_vco_rbias<3:0> = <1001>
C	if(ctl_prog_mode == 1) writes group 6-q6	ctl_data_bus<7:0>=<01010111>	ctl_sspll_en<1:0> = <01>	ctl_fla_enb = 0	ctl_icpc<2:0> = <101>	ctl_r1_max = 1	ctl_div_en = 1
D	if(ctl_prog_mode == 1) writes group 5-q5	ctl_data_bus<7:0>=<11011010>	ctl_vreg_en = 1	ctl_vreg <5:0> = <101101>	ctl_fbuff_enb = 0
E	if(ctl_prog_mode == 1) writes group 4-q4	ctl_data_bus<7:0>=<00000000>	ctl_aprobe<6:0> = <0000000>	-
F	if(ctl_prog_mode == 1) writes group 3-q3	ctl_data_bus<7:0>=<10110010>	ctl_vdc_dtpd_f_en = 1	ctl_vdc_dtpd_f<5:0> = <011001>
G	if(ctl_prog_mode == 1) writes group 2-q2	ctl_data_bus<7:0>=<11000100>	ctl_vdc_dtpd_r_en = 1	ctl_vdc_dtpd_r<5:0> = <100010>
H	if(ctl_prog_mode == 1) writes group 1-q1	ctl_data_bus<7:0>=<10111000>	ctl_rbuf_en = 1	ctl_rbuf_dc<5:0> = <011100>
I	if(ctl_prog_mode == 1) writes group 0-q0	ctl_data_bus<7:0>=<00000000>	ctl_ibias<7:0> = <00000000>
J	if(ctl_prog_mode == 1) writes group 6-q6	ctl_data_bus<7:0>=<10010101>	ctl_sspll_en<1:0> = <10>	ctl_fla_enb = 0	ctl_icpc<2:0> = <101>	ctl_r1_max = 0	ctl_div_en = 1
K	if(ctl_prog_mode == 1) writes group 6-q6	ctl_data_bus<7:0>=<10110100>	ctl_sspll_en<1:0> = <10>	ctl_fla_enb = 1	ctl_icpc<2:0> = <101>	ctl_r1_max = 0	ctl_div_en = 0

ctl_block_sel<3:0> = <0011> for 1 SA PLL
only group 6 controls the lock handover.

Figure 35. PLL Start-up Sequence

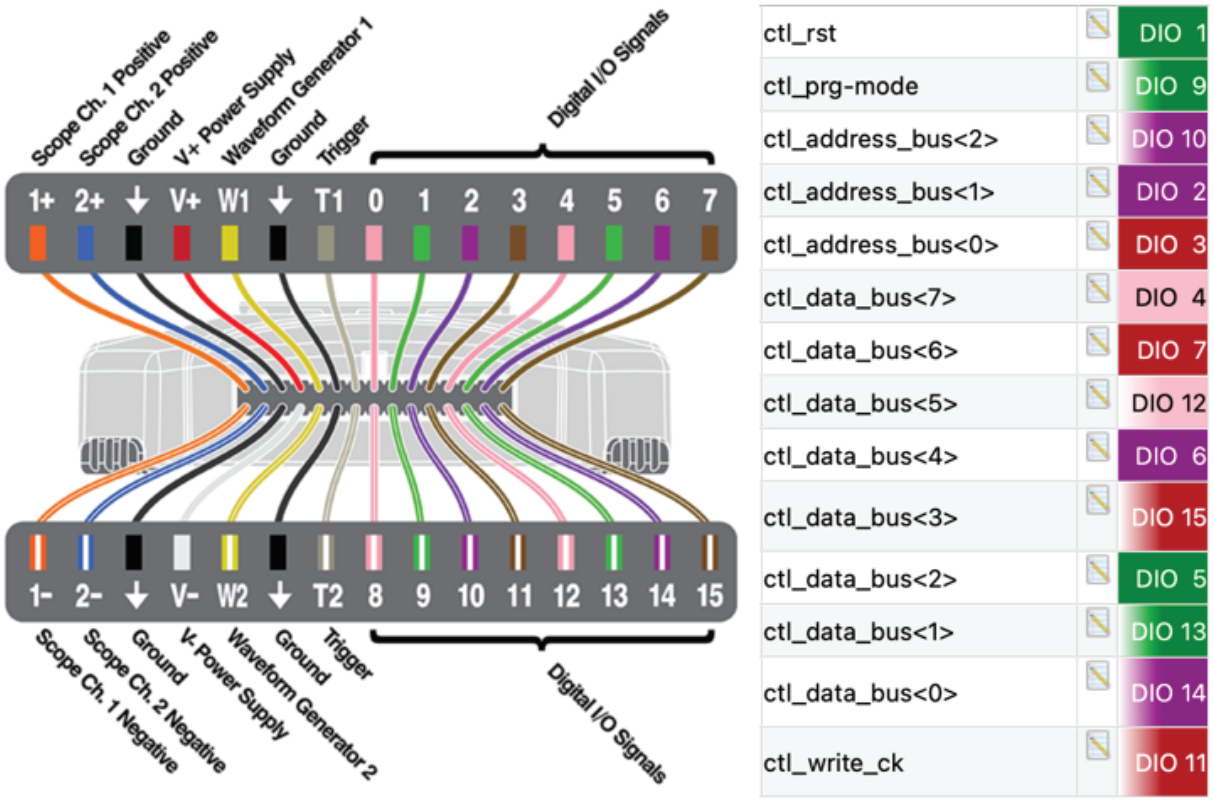


Figure 36: Calibration Signals

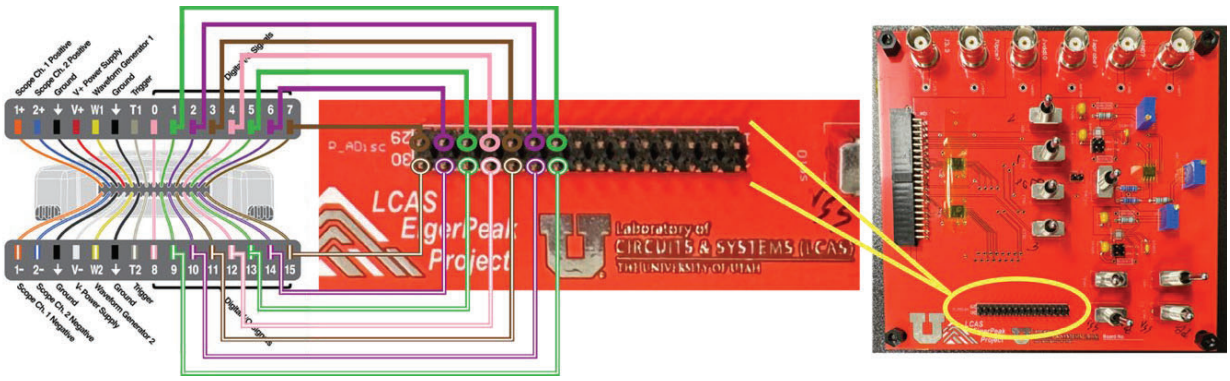


Figure 37: Calibration Connections

4.6.16 Test Check Offs

Initial Check Offs for PCBs:
This check off is to ensure all connections to the IB board are correctly done and the reference current is properly generated.

1. Make Supply connections to IB using C4-W4 as shown in “Full Setup” Slide.
   3.3V, GND.
2. Connect the output of the IB using W4 to the positive terminal of an ammeter. The negative terminal of the ammeter is to be grounded. Ensure the shielding of the wire W4 is to be grounded as well.

3. Turn on the 3.3 V supply.
4. Measure the current pushed to ground and ensure it is 100 µA.
5. If the current is not 100 µA, it can be adjusted using the pot in the south right, "pot_cs_src". {anti clockwise to increase}

4.6.17 Initial Check Offs for XTAL:

This check off is to first ensure the reference power is not too high for the PLL to handle as it feeds directly to a CMOS reference buffer. The check is also for the PNA; to ensure the PNA can measure low PN values with the expected PLL output power.

1. Connect the XTAL to power supply using C4-C3.
2. Connect the XTAL to the PNA using W2-C2-W1-Cdc- C1.
3. Turn on the power supply, slowly ramping up the supply voltage.
4. Around 2.5 V, the XTAL should begin to produce 1 GHz oscillations.
5. Continue ramping up till the swing of the sinusoid is measured to me 1.45 Vpp or ~7 dBm. {DO NOT allow this to go above 1.6 Vpp}
6. Make a note of the supply voltage (Vdd_ref) used and ensure this is not exceeded when connected to the test sample.
7. As an additional check, the noise floor of the PNA can be checked:
    a. With the lowest output swing from the XTAL, measure PN of the 1 GHz oscillation.
    b. The floor (> 1MHz offset) should be close to < -165 dBc/Hz in order to faithfully measure PLL PN.

4.6.18 Test Procedure:

Following is the procedure to be followed for locking the PLL. Once this is done, PN/spectral/power measurements can be performed.

1. Make all connections as detailed in the Test Setup section.
2. Perform all check as detailed in the "Initial Check Offs" section.
3. Connect AD to a computer with the companion software using the provided USB cable. Make sure the AD is recognized and selected as the target device.
4. Land the probes on the pads.
5. Turn on all the supplies, except that of the XTAL.
6. Run the "LCAS_PLL_RST" code to put the full chip on the reset mode.
7. Measure the current consumption by the die to be around 20 mA. This is the static draw from the termination resistances.
8. Measure the voltage on the IB connection to be around 1 V, this can have a 400-mV range. This is to only ensure a good contact; ideal value is 1.05 V. {lower implies better contact}.
9. Turn on the XTAL Supply and ramp up to previously noted Vdd_ref, there should be a 1-2 mA jump in consumption.
10. Run the "LCAS_PLL_STARTUP" code.
11. The PLL should run through the full startup and calibration process and lock to 29 GHz, consumption jumping to around 60 mA.
12. As the SSPLL will be locked stand alone with this test, it may lock to 28 GHz or 29 GHz. Lower PN is seen when oscillating at 29 GHz.
13. Rerunning the "LCAS_PLL_RST" and "LCAS_PLL_STARTUP" code will allow the PLL to lock to the desired frequency.

14. Once locked the PLL will hold the frequency and the PN can be measured.

4.6.19 Bare Die Measurements

The first measurement of the PLL was done on the bare die using the setup as in Fig. 38. The L-Shaped probes, with the RF and DC connections, were landed. Using these, the reference was fed in and the PLL output was taken out while also providing the supply. The PLL locked satisfying the specification without the need for any calibration as shown in Fig. 39, but the high frequency jitter peaking was a bit too high and showed potential of reduction with calibration.

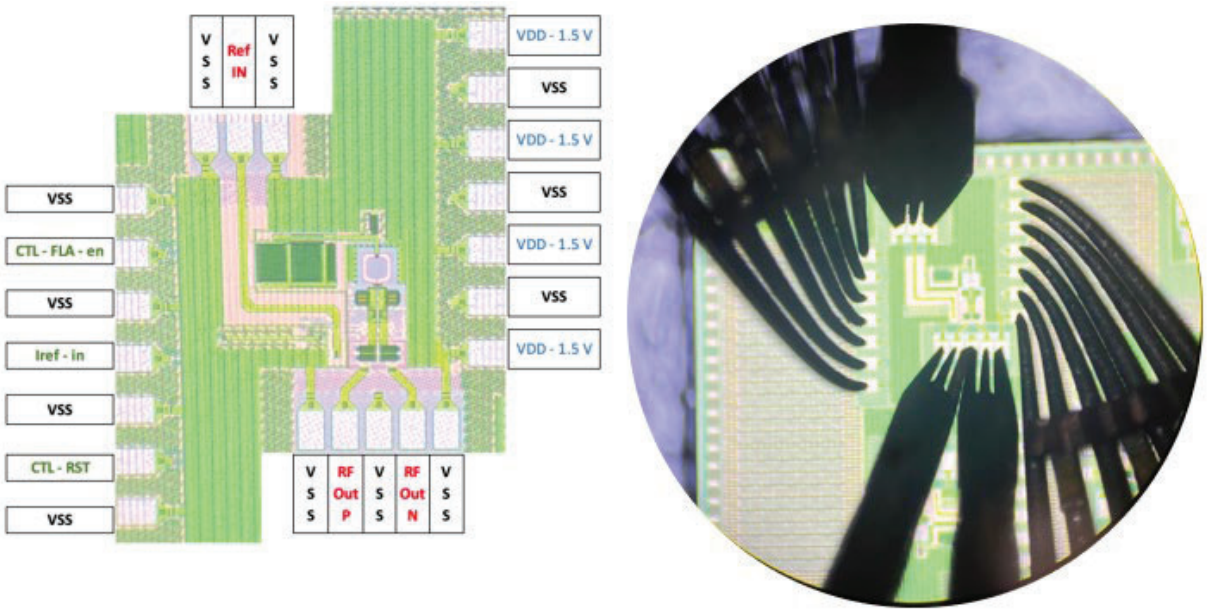


Figure 38: PLL Bare-Die Setup

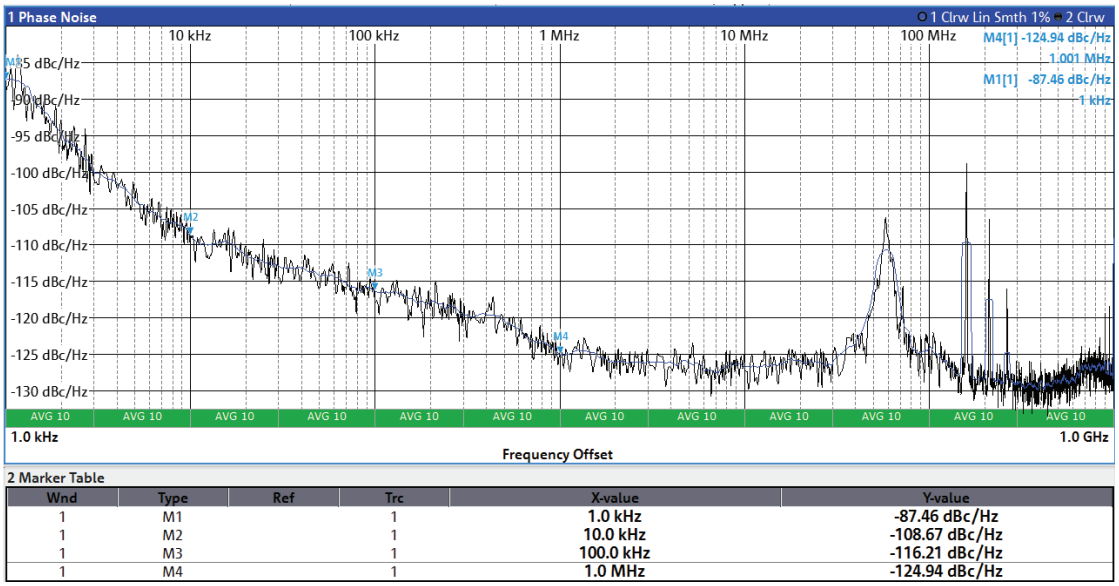


Figure 39: PLL Bare-Die PN Measurement

4.6.20 Calibrated Measurements

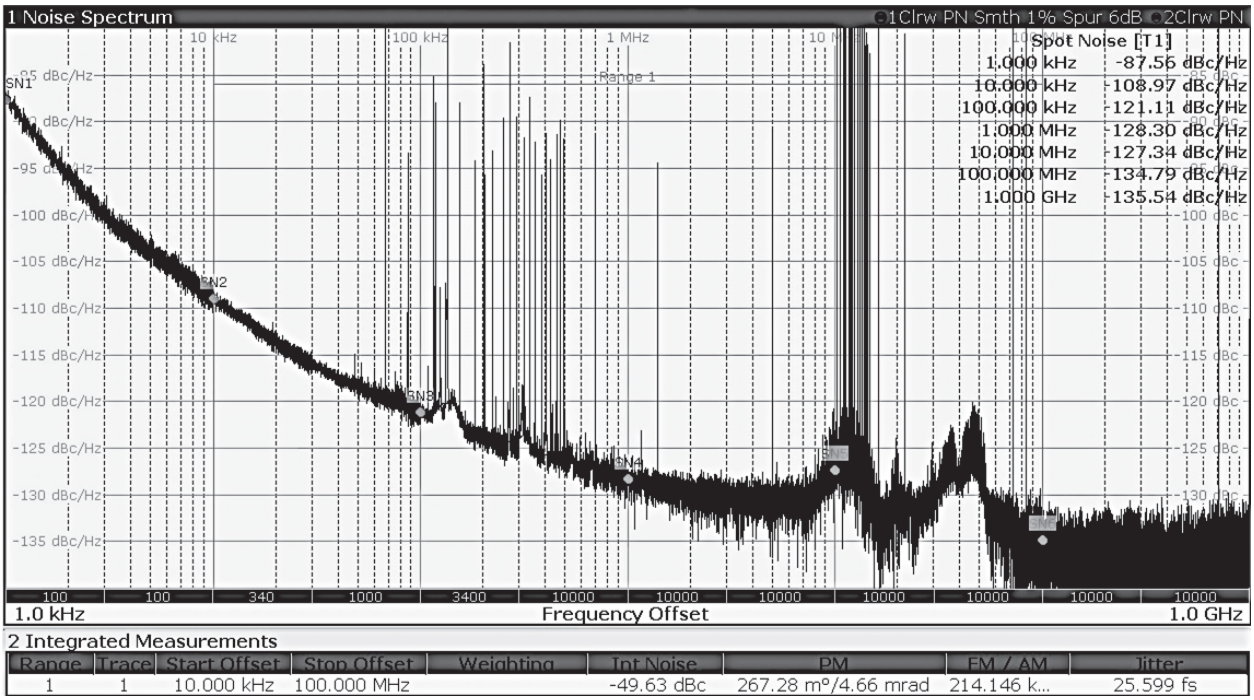


Figure 40: PLL PN Measurement

The bare die measurements showed that there is potential for calibrating the PLL. Especially the jitter peaking seen could be greatly reduced using calibration. To check this all the planned tests were performed and the PLL was tested to place it in the optimum calibration point and the measurements were repeated, using the setup shown in detail in Figure 38. The PN measurements of the PLL once the PLL is calibrated are shown in Fig. 40. The PLL was locked to 29 GHz using a 1 GHz, CRBSCS-01-1000, reference for the PN measurement shown in Fig. 40. The calibration sequence was used to set the duty cycle of this to minimize Phase Noise, PN, the double phase mode of operation. Further calibration was used to set the VCO and VCO-buffer in the lowest PN and jitter setting. Fully calibrated, the output PN is -128 (-124) dBc/Hz at 1 MHz offset, in double- (single-) phase modes. This achieves the target spec of -110 dBc/Hz at 100 kHz offset and -120dBc/Hz at 1 MHz offset comfortably with 8 dB of margin. Further, the total equivalent random jitter of the PLL output, integrated from 10 kHz to 100 MHz is 25.6 fs-rms, in the double-phase mode, making it one of the lowest published in literature as detailed in Table 4.

Variation of PN with reference: The PLL owing to the fact of being an SS-PLL has the capability of synthesizing the same 29 GHz, with different reference frequencies. The DTPD in the double phase mode allows the forward path to produce enough correction to hold the frequency, this enabling the PLL to operate with a wide range of reference frequencies. Consequently, the influence of reference frequency on PN in the same PLL post fabrication could be performed. The PLL was made to lock to an R&S SMA 100 B signal generator at multiple frequencies and the PN at 1 MHz was measured compared in Fig. 41. It shows that the reference frequency has a direct influence on the PN reducing by almost 13 dB.

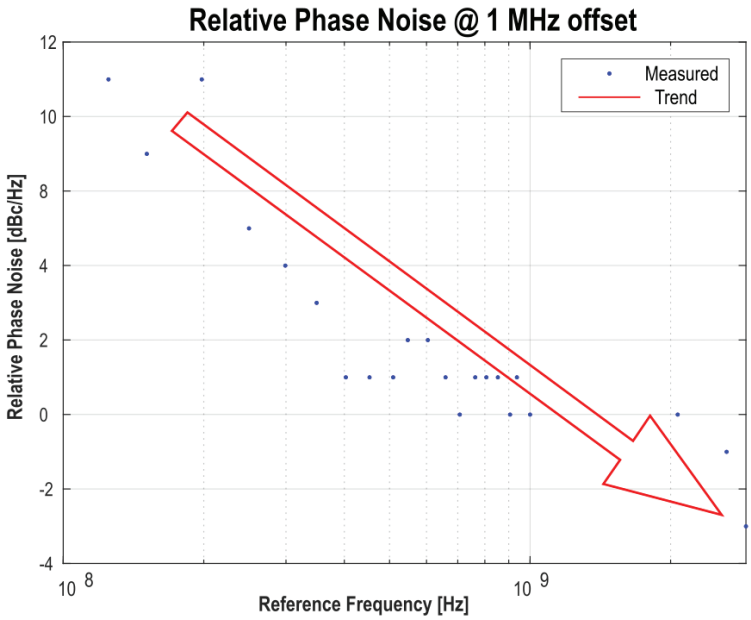


Figure 41: Variation of PN at 1MHz offset with Range of Reference Frequencies

A second test was performed to replicate this and the PLL was locked to the exact same reference but at 250 MHz reference and the PN measurements are compared in Fig. 42. The PN goes up by 9 dB as seen with the signal generator, showing the quality of reference had little influence.

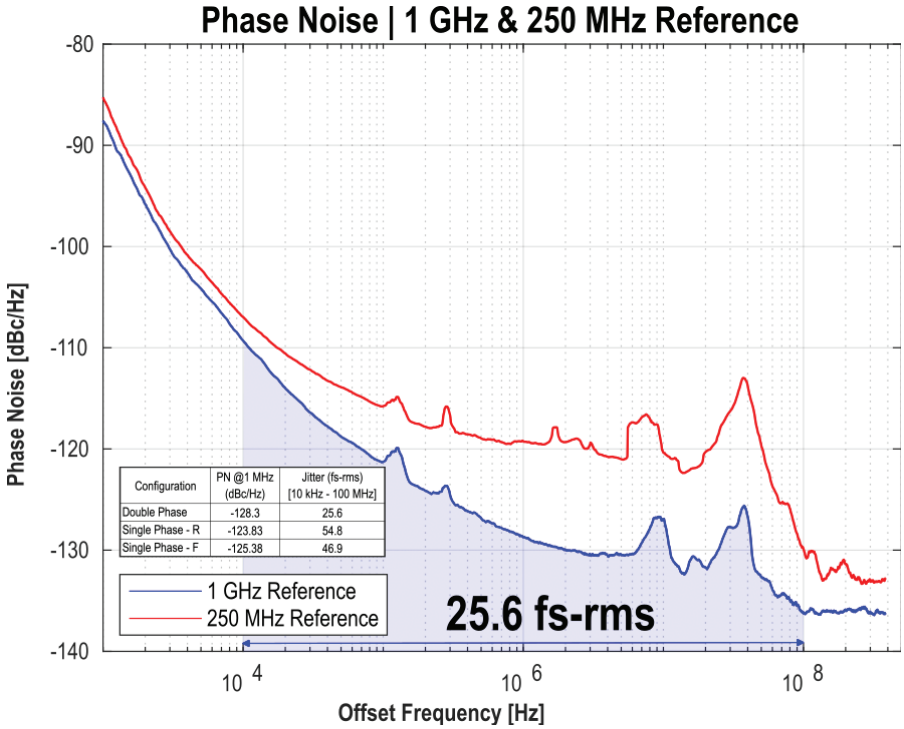


Figure 42: PN with 1 GHz Reference Crystal vs 250 MHz Reference Crystal

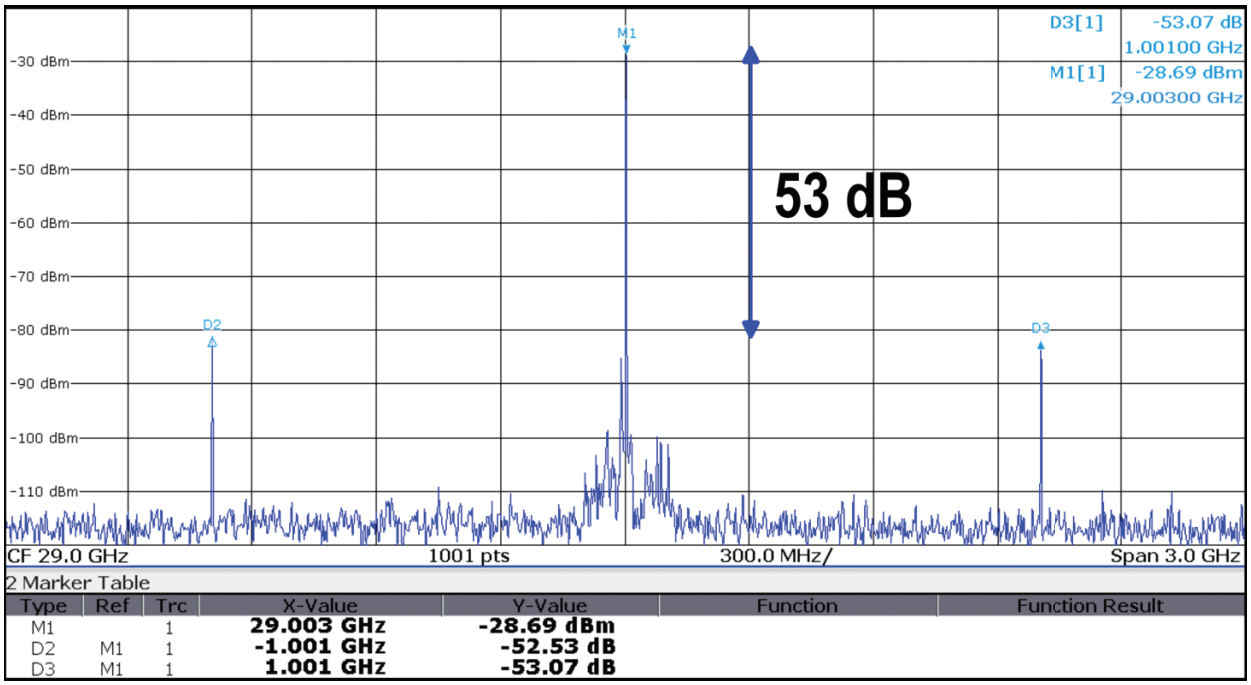


Figure 43: Calibrated PLL Spectral Measurement

The PLL was locked to 29 GHz using a 1 GHz, CRBSCS-01-1000, reference for the spectral measurements shown in Fig. 43. The calibration was used to set the VCO and VCO-buffer in the lowest PN and jitter setting. This implied the power output was not the highest possible by the buffer. In addition to this, owing to about -16 dB of loss along the line and -3 dBm signal driven was attenuated to -19 dBm in the best case and -28 dBm in the lowest PN configuration. The locked PLL exhibits a -53 dB reference spur after duty-cycle correction with this output power. A fully detailed PLL measurement is provided in Table 4, detailing the PLL operating in all modes.

		Single Phase - R	Single Phase - F	Double Phase
Spot Noise (dBc/Hz)	10 kHz	-105.56	-107.35	-108.97
	100 kHz	-113.25	-113.34	-121.11
	1MHz	-123.83	-125.38	-128.3
	10MHz	-124.19	-126.21	-127.34
	100Mhz	-131.7	-133.82	-134.79
Jitter [10 kHz - 100 MHz] (fs-rms)		54.8	46.9	25.6
Spur (dBc)		-47	-51	-53
Peaking	Magnitude (dB)	8	8	1.67
	Frequency (MHz)	13.86	12.76	25.82
Bandwidth (MHz)		46.77	43.68	65.86
Jitter-Power FoM (dB)		-251.91	-253.26	-258.52

FOM = 10*log[(σ/1s)^2 * (P/1mW)

Table 4: PLL Measurements in Single and Double Phase Modes

Power Consumption Distribution:

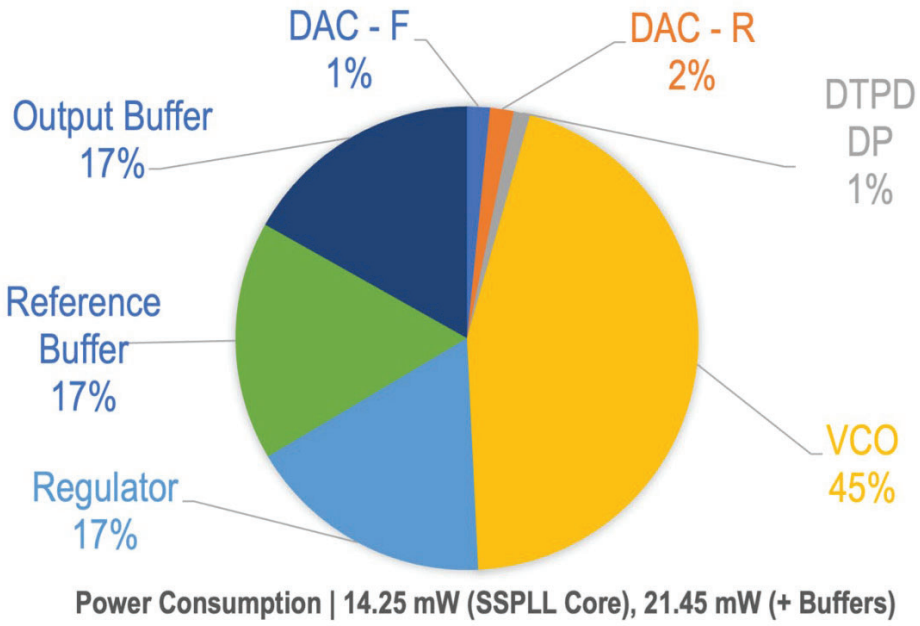


Figure 44: Power Consumption Distribution

The PLL consumes 14.25 mW at its core and 21.45 mW along with the output buffers and distributed as shown in Fig. 44. At start up, the PLL consumes an additional 156 mW in the frequency lock acquisition, which is turned off in all operation modes. The DTPD with a very efficient integrator design consumes less than 0.5 mW working at full rate. In fact, the biasing of DACs for the DTPD consume almost 10x the power of the DTPD, this was done to minimize noise added by the bias of DACs. The majority of the power drawn for the reference buffer is from the DAC with the 50 Ω matching input impedance used for controlling the input common mode, which in turn controls the duty cycle. The VCO with its regulator is the highest consumption point consuming > 50% of the total consumption.

4.6.21 Comparison to the State-of-the-Art

Table 4 compares the performance of the proposed PLL to the state-of-the-art, selected designs in both CMOS and SiGe technologies. Owing to the DTPD speed of operation, all components from the feedback path have been removed, thus improving the overall PN and the power consumption significantly. As a result, a performance comparable or better than the state-of-the-art has been achieved, even compared to the designs made in finer technology nodes. The advantages offered by the high-speed DTPD has led to a FoM of -258.5 dB including all the buffer stages, with the overall consumption of the core circuit being 14.25 mW, drawn from a single 1.5V supply.

Table 5: PLL Performance Comparison

	Y. Hu, ISSCC '20	H. Wang, TCAS '21	A. Bhat, TCAS '22	W. Chen, RFIC '22	Y. Zhao, JSSC '23	Y. Zhang, ESSCIRC '20	M. Hickle, BCICTS '21	R. Bindiganavile, RFIC '22	This Work (DP)	
Technology Node	28 nm CMOS	65 nm CMOS	65 nm CMOS	40 nm CMOS	28 nm CMOS	0.18 µm SiGe BiCMOS	90 nm SiGe BiCMOS	0.18 µm SiGe BiCMOS	45 nm SiGe RF SOI	
Reference Frequency [MHz]	250	100	50	100	250	250	100	1000	250	1000
Center Frequency [GHz]	21.71 to 26.49	40.5	24.4 to 29.2	21.8 to 41.6	20	25 to 30.5	25.3 to 28	33.89 to 37.46	25 to 29	
Phase Noise (100 kHz) [dBc/Hz]	-103.7	-95	-95	-104.1	-134.6	-116	-97	-109.9	-116	-121.1
Phase Noise (1MHz) [dBc/Hz]	-110.41	-100.5	-95	-110.3	-137.6	-117.3	-107	-113.3	-119	-128.3
Reference Spur [dBc]	-45	-43.5	-41	-46.1	-66	-57	-96	-48.56	-28	-53
Jitter [fs-rms] (10 kHz - 100 MHz)	75.8	192	330	62.7	20.9 (10 kHz - 40 MHz)	47.92	94	59.5	95	25.6
Total Power [mW]	16.5	9.1	18.2	23.6	12	46.8	850	194.6	21.4	
Figure of Merit * [dB]	-250.2	-244.6	-237	-250.3	-262.8	-250	-231	-241.6	-247	-258.5

*** FoM = $10\log(\sigma_j^2 * P_T)$**

4.7 PCM – Ring VCO

A set of ring oscillators have been designed to study process characteristics and its variations. In these measurements, three types of ring oscillators were designed and tested. These have been designed at low K_{gm}, optimal $K_{gm,}$ and high K_{gm} ($K_{gm} = g_m/I_d$ or transconductance efficiency). The optimal K_{gm} refers to the transconductance efficiency that results in the lowest power consumption. The two other circuit have been designed to have somewhat higher and lower transconductance efficiency compared to the optimal one. Elaborated below are the experimental results, where the conclusion can be summarized as:

In these measurements, three different types of ring oscillators were designed and tested. These have been designed at low K_{gm}, optimal $K_{gm,}$ and high K_{gm} ($K_{gm} = g_m/I_d$ or transconductance efficiency). Elaborated below are the experimental results, where the conclusions can be summarized as:

- **Conclusion 1:** Variability of all the 3 oscillators, over 7 boards measured, is approximately the same and about +/- 36%. [Considering the fact these are ring oscillators, high variation is expected but not as much as 36%. This could be from the floating body core devices among other process variations.]
- **Conclusion 2:** Phase Noise of all the three oscillators are consistent, with the VCO having high K_{gm} showing low Phase Noise.

In the following, the detailed experimental results are provided:

The proposed RVCO is designed for three various transconductance efficiencies and a center frequency of 1GHz. RVCOs are classified based on their operating transconductance efficiency to high, optimum, and low. Table 5 presents the simulation results of each RVCO, based on the optimization method, compared with the measurement results. For the V_{ctl} corresponding to 1GHz, Table 5 shows a good matching between the simulation results and measured parameters. The designed RVCO with high K_{gm} shows better Phase Noise, PN, in comparison with two other RVCOs.

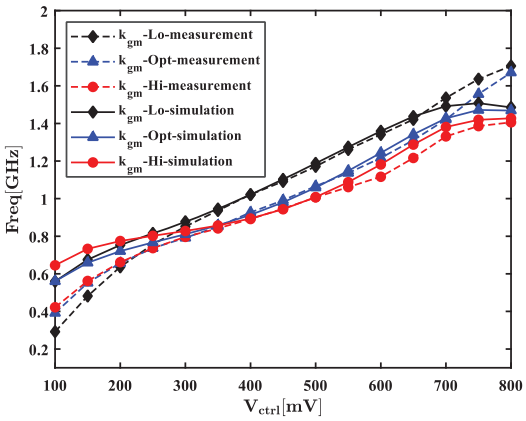


Figure 45: VCO Frequency vs Reference Voltage
Simulation vs measurement

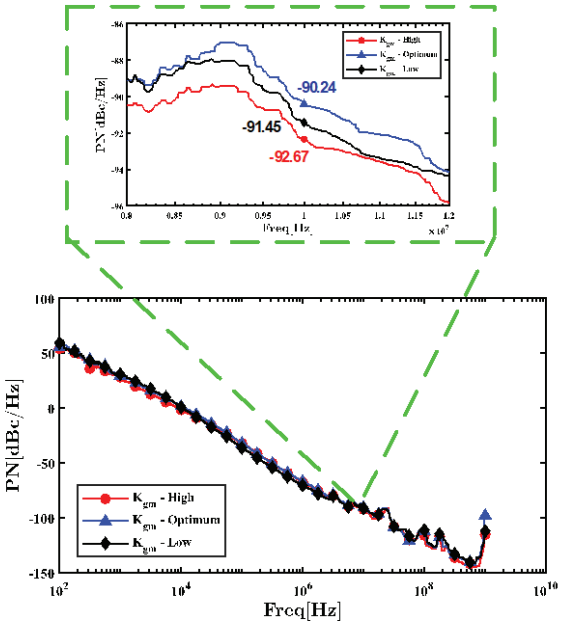


Figure 46: Phase noise of VCO at 10MHz for different Kgm

Fig. 46 illustrated for supporting the measured PN of the RVCOs presented in Table 5. Fig. 45 demonstrates the sensitivity of the RVCOs against control voltage, V_{ctl}, based on both simulation and measurement results. For the identical range of V_{ctl}, from 100mV to 800mV, the frequency of the oscillation has been changed from 600MHz up to almost 1.4 GHz for all RVCOs at transistor-level simulation. However, the frequency range variation for the measured results is from 400MHz to 1.7 GHz. As can be seen, $RVCO_{Low}$ shows more linear behavior compared to $RVCO_{High}$ and $RVCOO_{pt}$. In addition, $RVCO_{Low}$ has higher K_{VCO} according to Fig. 45.

Table 6: PCM Result Summary and Comparison

RVCO	Simulation		Measurement	
	V_{ctrl} [mV]	Freq. [GHz]	V_{ctrl} [mV]	Freq. [GHz]
High	510	1.036	510	1.016
Opt	480	0.994	480	1.036
Low	400	1.135	400	1.021

4.7.1 Control Codes for PCM Oscillators with different Kgm

The following tables show the default codes for operating the three different PCM oscillators (kgm_hi, kgm_opt, kgm_lo). vref_pcm shows the voltage required to sustain 1GHz oscillation in simulation for three oscillators. While one of the three oscillators (kgm_hi, kgm_opt, kgm_lo) are turned on, the remaining two oscillators are turned off.

Table 7: Default Control Code for PCM – kgm_hi

kgm_hi					
ctl_i_dist	**ctl_kgm_hi**	**ctl_kgm_opt**	**ctl_kgm_lo**	**ctl_fbuff**	**vref_pcm (1GHz Osc)**
0 V	0 V	1.5 V	1.5 V	0 V	510 mV

Table 8: Default Control Code for PCM – kgm_opt

kgm_opt					
ctl_i_dist	**ctl_kgm_hi**	**ctl_kgm_opt**	**ctl_kgm_lo**	**ctl_fbuff**	**vref_pcm (1GHz Osc)**
0 V	1.5 V	0 V	1.5 V	0 V	480 mV

Table 9: Default Control Code for PCM- kgm_lo

kgm_lo					
ctl_i_dist	**ctl_kgm_hi**	**ctl_kgm_opt**	**ctl_kgm_lo**	**ctl_fbuff**	**vref_pcm (1GHz Osc)**
0 V	1.5 V	1.5 V	0 V	0 V	400 mV

4.7.2 Programming Sequence for the digital blocks

The control codes of the overall chip are divided into eight groups. The control codes associated with pcm oscillators have been assigned to group 0 - q0. Out of the eight data bus, three data bus <2:0> has don't care (X) condition.

Grp 0 - q0							
ctl_data_bus<7>	ctl_data_bus<6>	ctl_data_bus<5>	ctl_data_bus<4>	ctl_data_bus<3>	ctl_data_bus<2>	ctl_data_bus<1>	ctl_data_bus<0>
ctl_kgm_lo	ctl_kgm_opt	ctl_kgm_hi	ctl_i_dist	ctl_fbuff	ctl_pcm<2>	ctl_pcm<1>	ctl_pcm<0>
					X	X	X

Figure 47: Data Bus representation for Group 0 - q0

The timing sequence of the programming for the control codes of the PCM is shown in the following pages. In every programming sequence, a reset pulse (ctl_rst) is sent initially to make sure all the blocks are turned off.

			R			kgm_hi on															
ctl_rst	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_prog_mode	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ctl_block_sel<3>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_block_sel<2>	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ctl_block_sel<1>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_block_sel<0>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_address_bus<2>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_address_bus<1>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_address_bus<0>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_data_bus<7>	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ctl_data_bus<6>	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ctl_data_bus<5>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_data_bus<4>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_data_bus<3>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_data_bus<2>	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
ctl_data_bus<1>	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
ctl_data_bus<0>	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Figure 48: Timing sequence for digital control (kgm_hi)

			R			kgm_opt on															
ctl_rst	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_prog_mode	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ctl_block_sel<3>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_block_sel<2>	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ctl_block_sel<1>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_block_sel<0>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_address_bus<2>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_address_bus<1>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_address_bus<0>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_data_bus<7>	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ctl_data_bus<6>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_data_bus<5>	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ctl_data_bus<4>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_data_bus<3>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_data_bus<2>	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
ctl_data_bus<1>	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
ctl_data_bus<0>	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Figure 49: Timing Sequence for Digital Control (kgm_opt)

R-Reset operation for the PCM

			R			kgm_lo on															
ctl_rst	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_prog_mode	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ctl_block_sel<3>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_block_sel<2>	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ctl_block_sel<1>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_block_sel<0>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_address_bus<2>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_address_bus<1>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_address_bus<0>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_data_bus<7>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_data_bus<6>	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ctl_data_bus<5>	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ctl_data_bus<4>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_data_bus<3>	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ctl_data_bus<2>	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
ctl_data_bus<1>	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
ctl_data_bus<0>	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Figure 50: Timing Sequence for Digital Control (kgm_lo)

4.7.3 Board #1 Measurement

Board #1 results are summarized in the following Tables (10,11,12). In Table 9, vref is chosen according to simulation for 1 GHz Oscillation frequency. The center frequency varies by 4.8%, 37.4% and 35.5% for kgm_hi, kgm_opt and kgm_lo respectively in measurement. In the next step, vref is tuned to achieve 1 GHz oscillation frequency in measurement and the results are shown in Table 11. Table 12 shows the phase noise results for the three oscillators @1GHz oscillation frequency.

Table 10: Board #1 - Frequency, Peak and Consumption of PCM (Default vref)

kgm_hi				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
510	952	-9.25	9.16	31
kgm_opt				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
480	1374	-10.25	9.118	31
kgm_lo				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
400	1355	-10.48	8.98	31

Table 11: Board #1 - Frequency, Peak and Consumption of PCM (Tuned vref)

kgm_hi				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
548	1000	-9.6	9.195	31
kgm_opt				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
280	1000	-9.61	8.638	32
kgm_lo				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
236	1000	-9.54	8.44	32

Table 12: Board #1 – Phase noise

Offset Frequency	**Phase Noise @1GHz Oscillation Frequency**		
	kgm_hi	**kgm_opt**	**kgm_lo**
1k	30.66	29.63	30.02
10k	-1.15	0	0.33
100k	-32.96	-33.25	-32.84
1M	-68.76	-68.54	-68.76
10M	-76.73	-76.99	-78.34
100M	-119.16	-112.8	-116.9

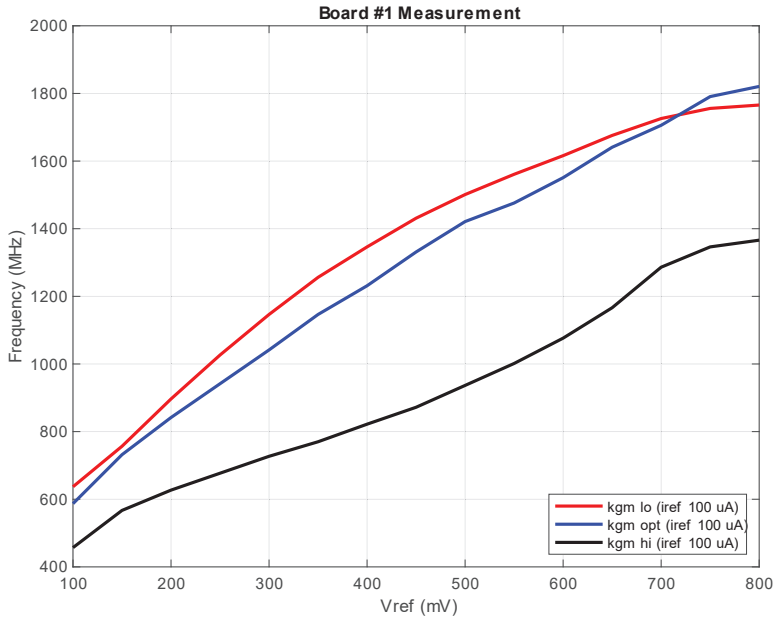


Figure 51: Board #1 - Oscillation Frequency vs. vref (iref 100 uA – all kgm)

Fig. 51 shows the variation of oscillation frequency with respect to the change in vref. The three different oscillators show different sensitivity with respect to vref in measurement. In this experiment, iref is fixed at nominal 100 uA.

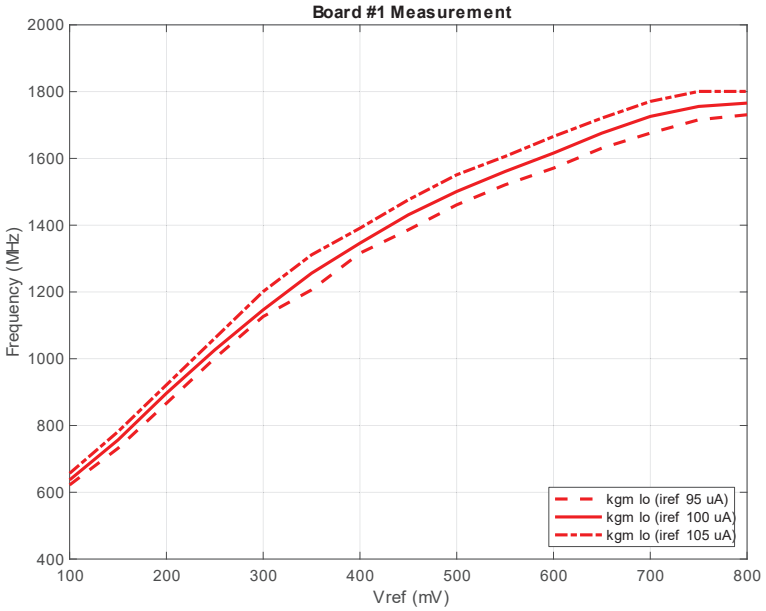


Figure 52: Board #1 - Oscillation Frequency vs. vref (iref varied 5% – kgm_lo)

Fig. 52 shows the variation of the sensitivity curve with 5% variation in the bias current (i.e. iref). The figure shows the variation of kgm_lo only.

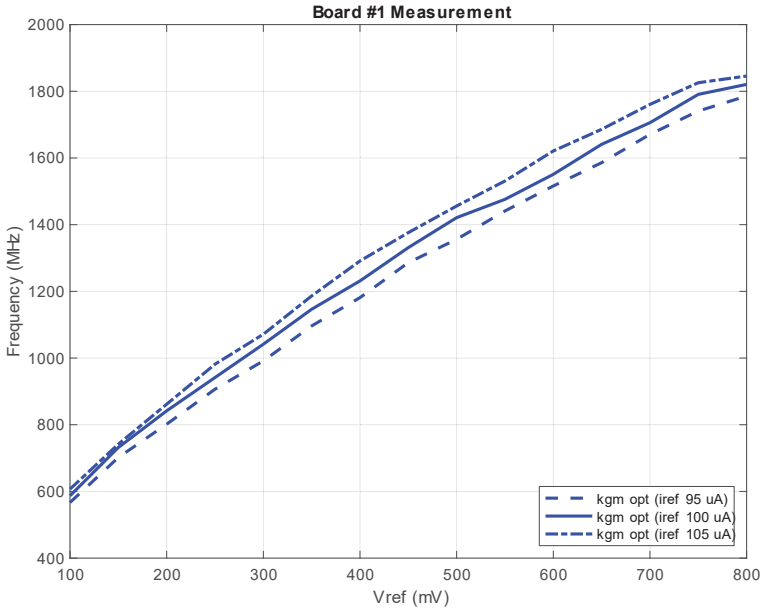


Figure 53: Board #1 - Oscillation Frequency vs. vref (iref varied 5% – kgm_opt)

Fig. 53 shows the variation of the sensitivity curve with 5% variation in the bias current (i.e. iref). The figure shows the variation of kgm_opt only.

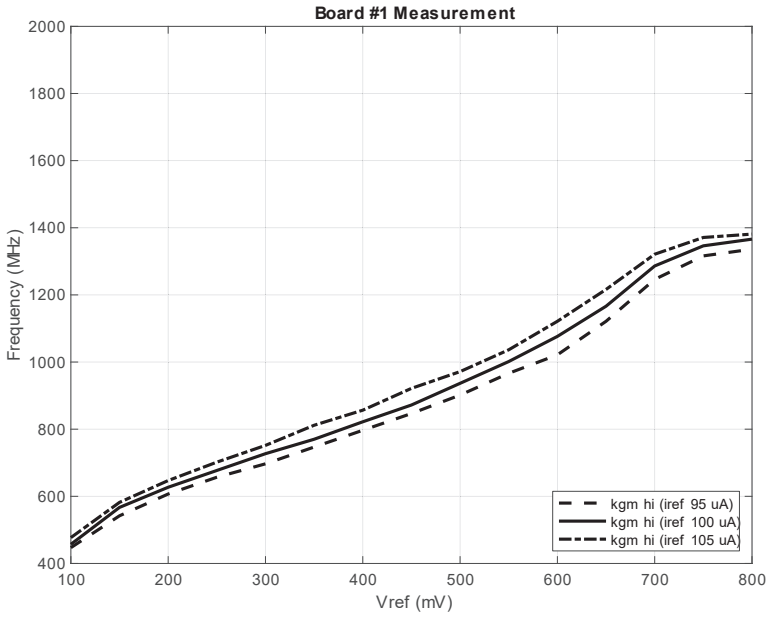


Figure 54: Board #1 - Oscillation Frequency vs. vref (iref varied 5% – kgm_hi)

Fig. 54 shows the variation of the sensitivity curve with 5% variation in the bias current (i.e. iref). The figure shows the variation of kgm_hi only.

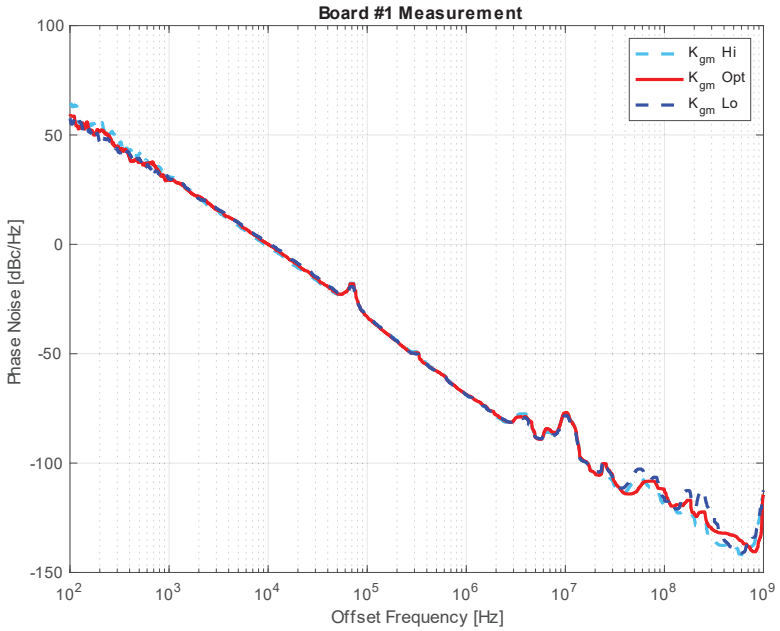


Figure 55: Board #1 – Phase Noise at 1GHz Oscillation Frequency (all kgm)

Fig. 55 represents the phase noise profile for all the oscillators in board #1. The three oscillators show close phase noise profile in lower offset frequencies. There are some bumps on the phase noise profile due to measurement artifacts.

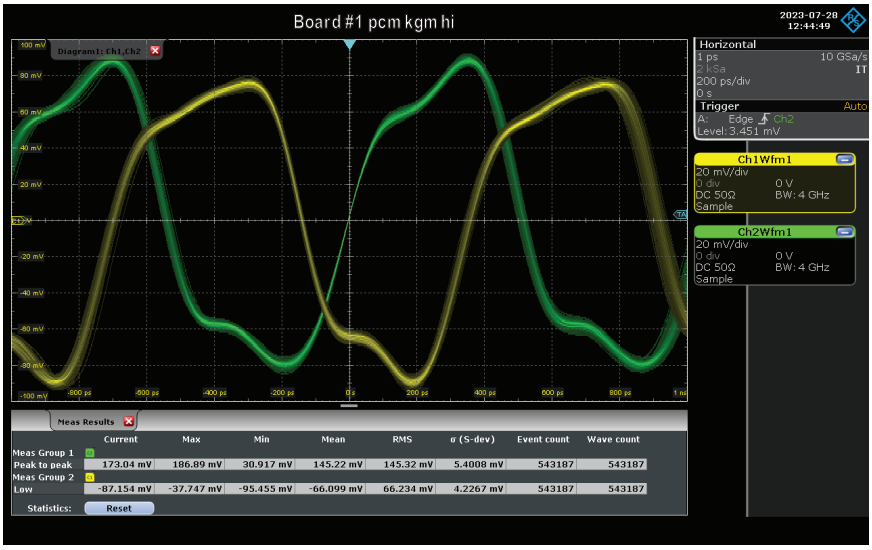


Figure 56: Board #1 – Transient Output from kgm_hi

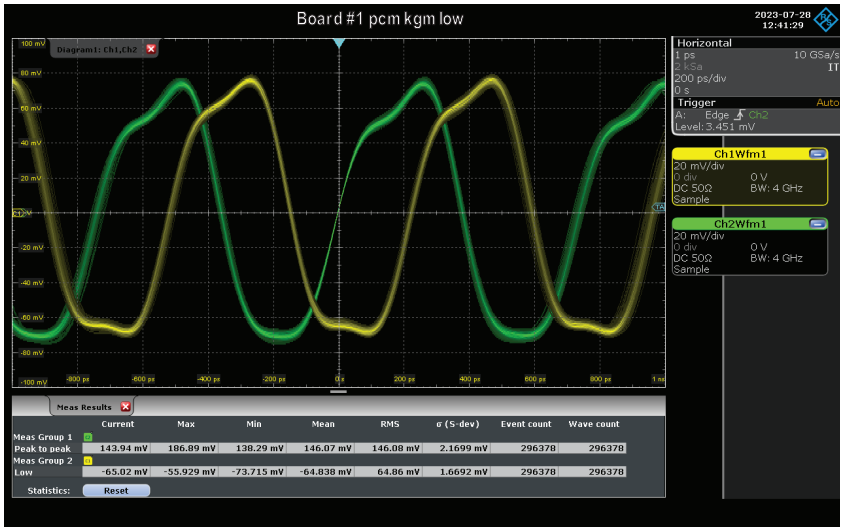


Figure 57: Board #1 – Transient Output from kgm_lo

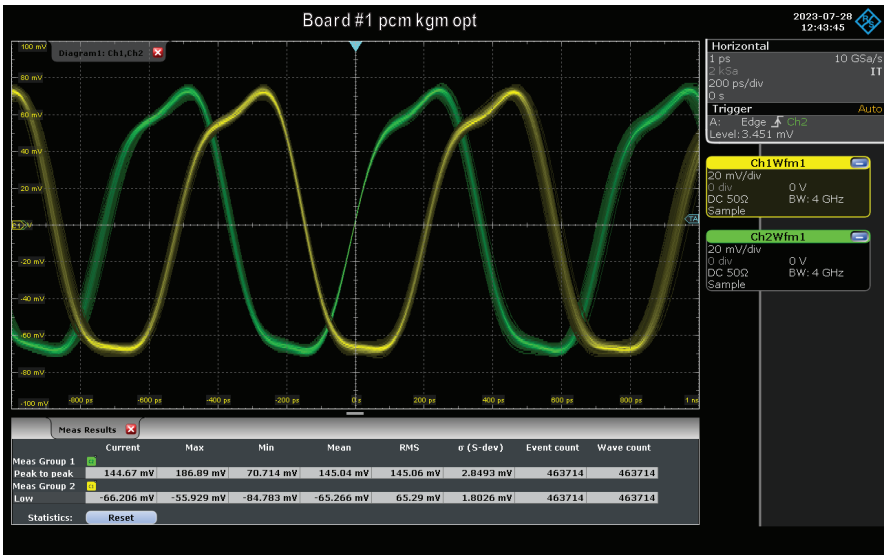


Figure 58: Board #1 – Transient Output from kgm_opt

Fig. 56 to 58 shows the transient measurement of the three oscillators output.

4.8 Board #2 Measurement

The results on board #2 are summarized in the following Tables (13,14,15). In Table 13, vref is chosen according to simulation for 1 GHz Oscillation frequency. The center frequency varies by 11.64%, 31.12% and 8.34% for kgm_hi, kgm_opt and kgm_lo respectively in measurement. In the next step, vref is tuned to achieve 1 GHz oscillation frequency in measurement and the results are shown in Table 14. Table 15 shows the phase noise results for the three oscillators @1GHz oscillation frequency.

Table 13 Board #2 - Frequency, Peak and Consumption of PCM (Default vref)

kgm_hi				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
510	1116.4	-10.01	8.165	32
kgm_opt				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
480	1311.2	-9.86	8.109	31
kgm_lo				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
400	916.6	-9.37	7.94	32

Table 14: Board #2 - Frequency, Peak and Consumption of PCM (Tuned vref)

kgm_hi				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
418	1001.5	-9.25	7.983	32
kgm_opt				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
316	1001.5	-9.49	7.651	32
kgm_lo				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
460	1001.5	-9.16	8.08	32

Table 15: Board #2 – Phase Noise

Offset Frequency	**Phase Noise @1GHz Oscillation Frequency**		
	kgm_hi	**kgm_opt**	**kgm_lo**
1k	28.17	31.62	26.25
10k	-1.53	3.5	-0.6
100k	-32.27	-33.33	-33.4
1M	-67.59	-69.58	-64.69
10M	-92.35	-91.57	-90.93
100M	-116.11	-110.22	-108.38

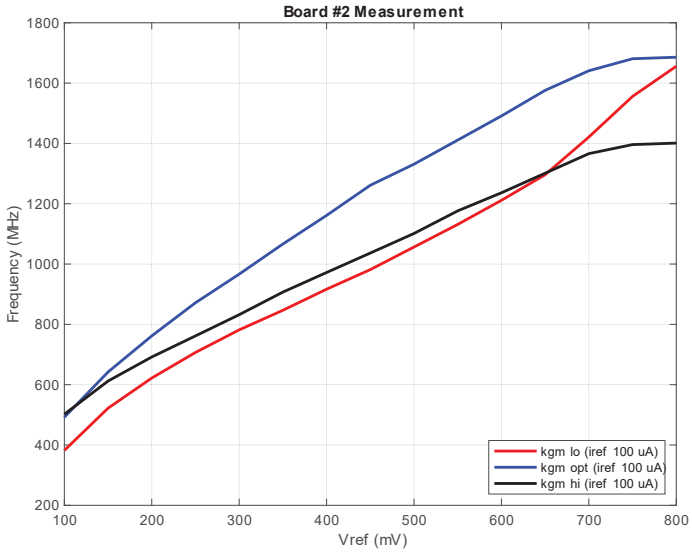


Figure 59: Board #2 - Oscillation Frequency vs. vref (iref 100 uA – all kgm)

Fig. 59 shows the variation of oscillation frequency with respect to the change in vref. The three different oscillators show different sensitivity with respect to vref in measurement. In this experiment, iref is fixed at nominal 100 uA.

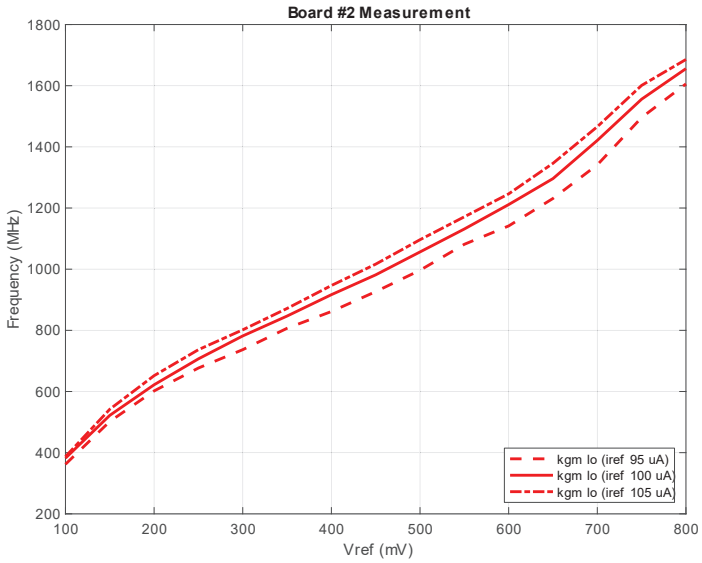


Figure 60: Board #2 - Oscillation Frequency vs. vref (iref varied 5% – kgm_lo)

Fig. 60 shows the variation of the sensitivity curve with 5% variation in the bias current (i.e. iref). The figure shows the variation of kgm_lo only.

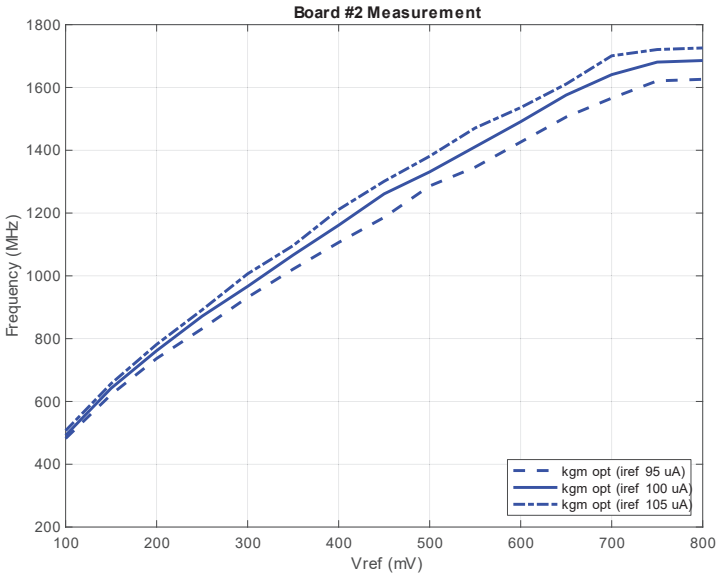


Figure 61: Board #2 - Oscillation Frequency vs. vref (iref varied 5% – kgm_opt)

Fig. 61 shows the variation of the sensitivity curve with 5% variation in the bias current (i.e. iref). The figure shows the variation of kgm_opt only.

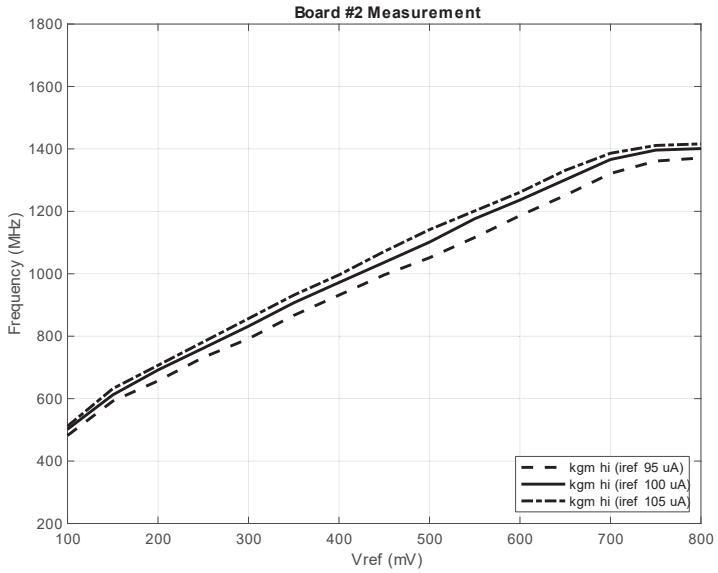


Figure 62: Board #2 - Oscillation Frequency vs. vref (iref varied 5% – kgm_hi)

Fig. 62 shows the variation of the sensitivity curve with 5% variation in the bias current (i.e. iref). The figure shows the variation of kgm_hi only.

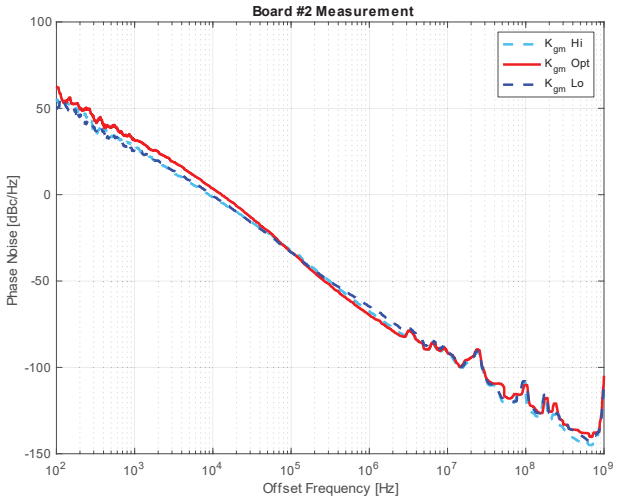


Figure 63: Board #2 – Phase Noise at 1GHz oscillation frequency (all kgm)

Fig. 63 represents the phase noise profile for all the oscillators in board #2. Unlike board #1, board #2 shows variation in the phase noise profile at lower offset frequencies. There are some bumps on the phase noise profile due to measurement artifacts.

4.8.1 Board #8 Measurement

The board #8 results are summarized in the following Tables (16,17,18). In Table 16, vref is chosen according to simulation for 1 GHz Oscillation frequency. The center frequency varies by 1.65%, 3.65% and 2.15% for kgm_hi, kgm_opt and kgm_lo respectively in measurement. In the next step, vref is tuned to achieve 1 GHz oscillation frequency in measurement and the results are shown in Table 17. Table 18 shows the phase noise results for the three oscillators @1GHz oscillation frequency. **Board #8 shows the closest match of measurement data with simulation.**

Table 16: Board #8 - Frequency, Peak and Consumption of PCM (Default vref)

kgm_hi				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
510	1016.5	-9.43	7.817	32
kgm_opt				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
480	1036.5	-9.92	7.77	32
kgm_lo				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
400	1021.5	-9.74	7.586	32

Table 17: Board #8 - Frequency, Peak and Consumption of PCM (Tuned vref)

kgm_hi				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
493	1001.5	-9.73	7.798	32
kgm_opt				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
452	1001.5	-9.52	7.719	32
kgm_lo				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
388	1001.5	-9.68	7.551	32

Table 18: Board #8 – Phase noise

Offset Frequency	**Phase Noise @1GHz Oscillation Frequency**		
	kgm_hi	**kgm_opt**	**kgm_lo**
1k	25.53	28.5	27.65
10k	-0.11	0.35	-1.11
100k	-34.46	-30.44	-34.87
1M	-71.25	-67.01	-69.69
10M	-91.93	-90.12	-91.3
100M	-113.45	-112.39	-107.83

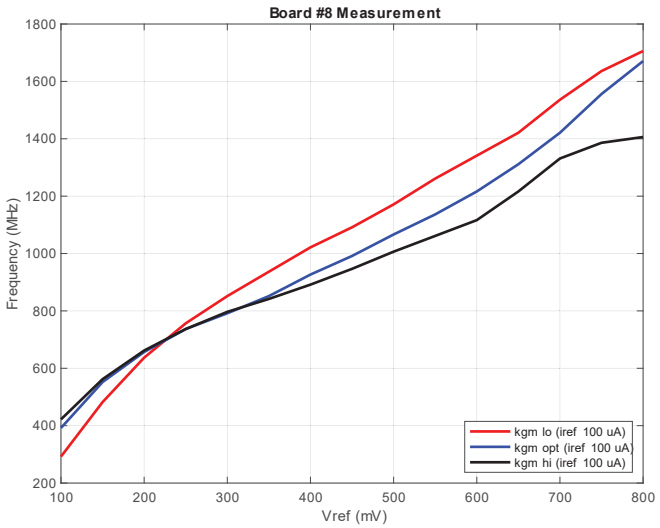


Figure 64: Board #8 – Oscillation Frequency vs. vref (iref 100 uA – all kgm)

Fig. 64 shows the variation of oscillation frequency with respect to the change in vref. The three different oscillators show different sensitivity with respect to vref in measurement. In this experiment, iref is fixed at nominal 100 uA.

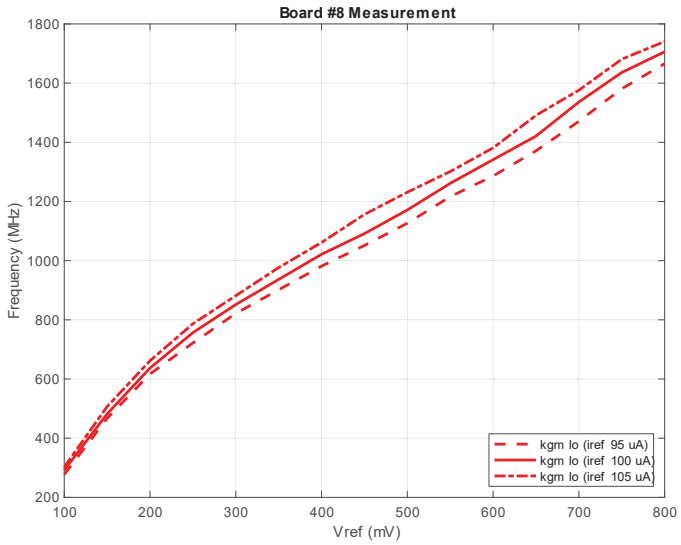


Figure 65: Board #8 – Oscillation Frequency vs. vref (iref varied 5% – kgm_lo)

Fig. 65 shows the variation of the sensitivity curve with 5% variation in the bias current (i.e. iref). The figure shows the variation of kgm_lo only.

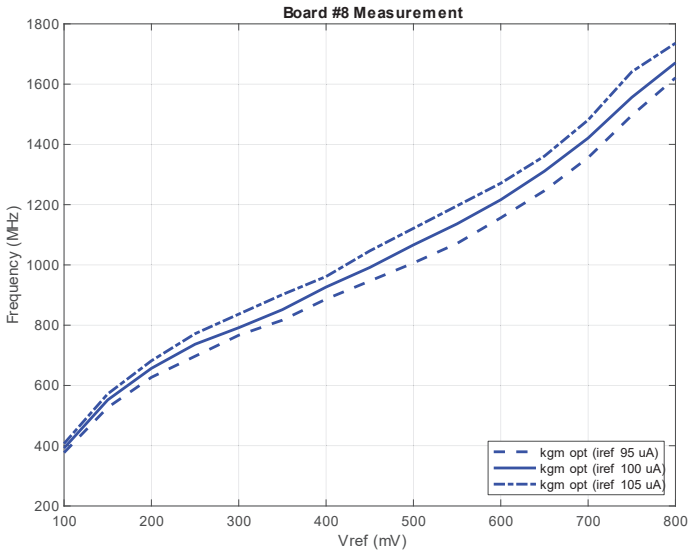


Figure 66: Board #8 – Oscillation Frequency vs. vref (iref varied 5% – kgm_opt)

Fig. 66 shows the variation of the sensitivity curve with 5% variation in the bias current (i.e. iref). The figure shows the variation of kgm_opt only.

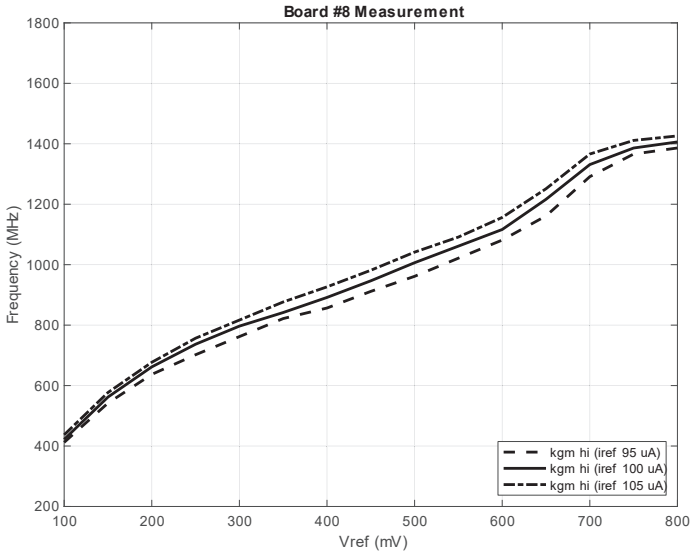


Figure 67: Board #8 – Oscillation Frequency vs. vref (iref varied 5% – kgm_hi)

Fig. 67 shows the variation of the sensitivity curve with 5% variation in the bias current (i.e. iref). The figure shows the variation of kgm_hi only.

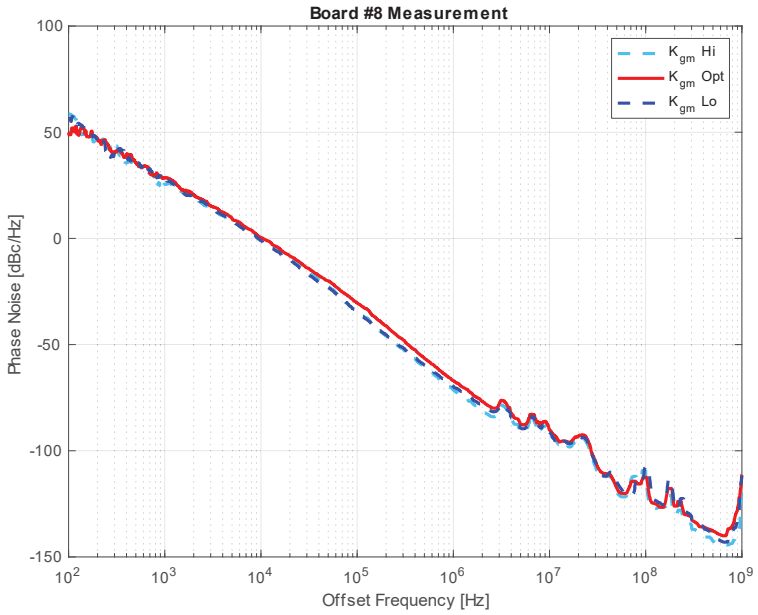


Figure 68: Board #8 – Phase Noise at 1GHz Oscillation Frequency (all kgm)

Fig. 68 represents the phase noise profile for all the oscillators in board #8. Lower than 10kHz offset frequency, the three oscillators show same phase noise profile. From the mid-band offset frequencies (10kHz ~ 1MHz), kgm_opt has higher phase noise. There are some bumps on the phase noise profile due to measurement artifacts.

4.8.2 Board #9 Measurement

The board #9 results are summarized in the following Tables (19,20,21). In Table 19, vref is chosen according to simulation for 1 GHz Oscillation frequency. The center frequency varies by 1.85%, 22.13% and 36.1% for kgm_hi, kgm_opt and kgm_lo respectively in measurement. In the next step, vref is tuned to achieve 1 GHz oscillation frequency in measurement and the results are shown in Table 20. Table 21 shows the phase noise results for the three oscillators @1GHz oscillation frequency.

Table 19: Board #9 - Frequency, Peak and Consumption of PCM (Default vref)

Kgm_hi				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
510	981.5	-9.65	8.423	33
kgm_opt				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
480	1221.3	-9.84	8.379	33
kgm_lo				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
400	1461	-9.69	8.208	33

Table 20: Board #9 - Frequency, Peak and Consumption of PCM (Tuned vref)

kgm_hi				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
530	1001.5	-9.81	8.451	33
kgm_opt				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
350	1001.5	-9.59	8.076	33
kgm_lo				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
209	1001.5	-9.61	7.339	33

Table 21: Board #9 – Phase Noise

Offset Frequency	Phase Noise @1GHz Oscillation Frequency		
	kgm_hi	kgm_opt	kgm_lo
1k	27.03	28.21	27.39
10k	-3.46	-1.85	-1.41
100k	-33.29	-33.12	-35.52
1M	-67.41	-69.82	-69.52
10M	-91.26	-91.33	-92.02
100M	-110.95	-111.75	-108.19

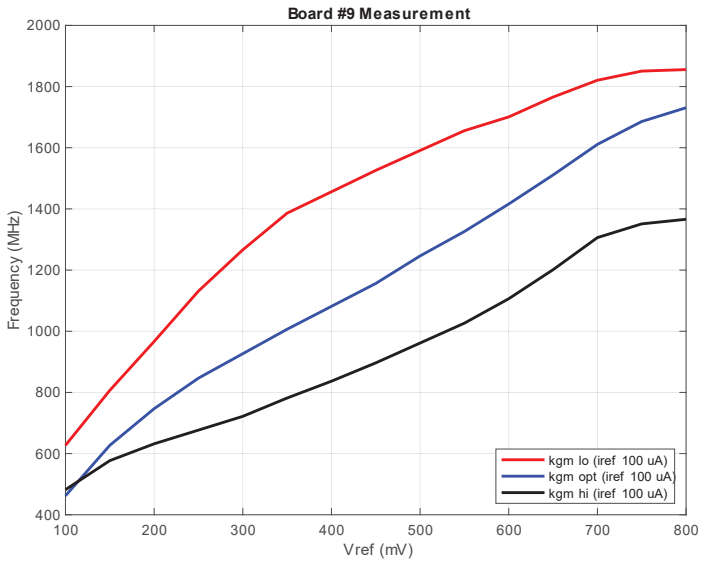


Figure 69: Board #9 – Oscillation Frequency vs. vref (iref 100 uA – all kgm)

Fig. 69 shows the variation of oscillation frequency with respect to the change in vref. The three different oscillators show different sensitivity with respect to vref in measurement. In this experiment, iref is fixed at nominal 100 uA.

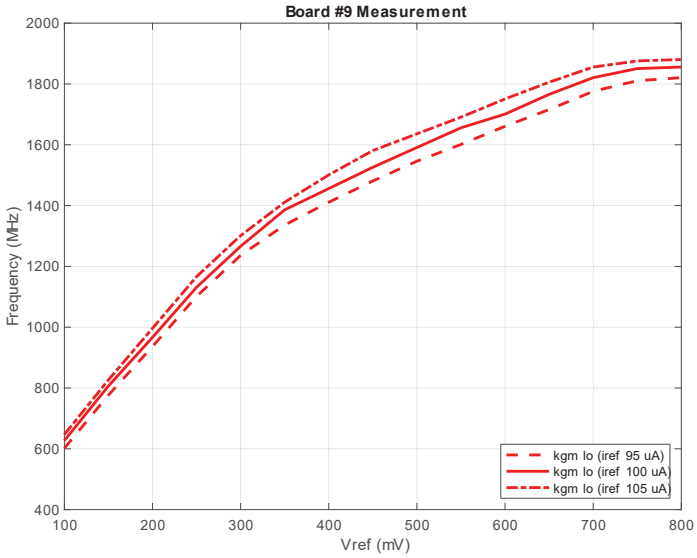


Figure 70: Board #9 – Oscillation Frequency vs. vref (iref varied 5% – kgm_lo)

Fig. 70 shows the variation of the sensitivity curve with 5% variation in the bias current (i.e. iref). The figure shows the variation of kgm_lo only.

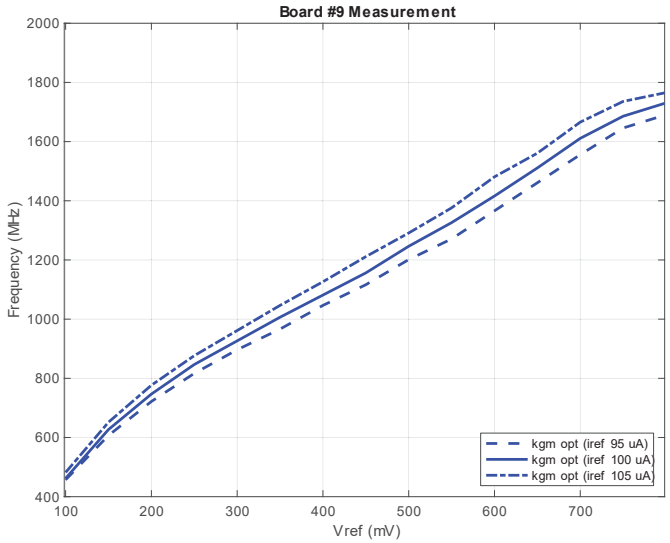


Figure 71: Board #9 – Oscillation Frequency vs. vref (iref varied 5% – kgm_opt)

Fig. 71 shows the variation of the sensitivity curve with 5% variation in the bias current (i.e. iref). The figure shows the variation of kgm_opt only.

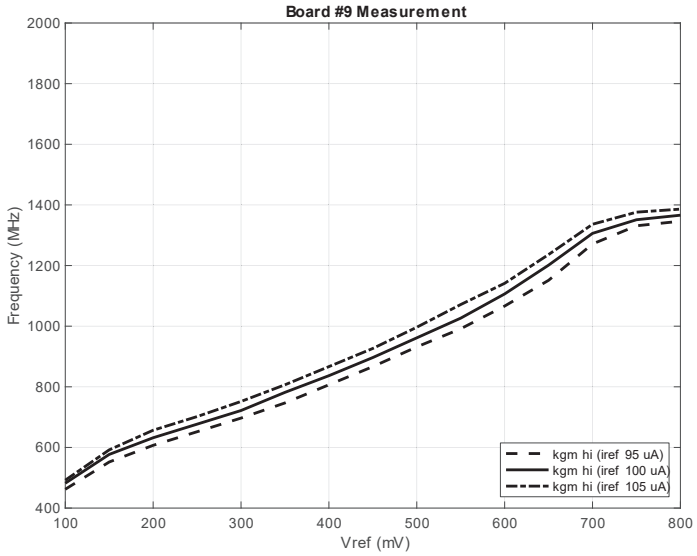


Figure 72: Board #9 – Oscillation Frequency vs. vref (iref varied 5% – kgm_hi)

Fig. 72 shows the variation of the sensitivity curve with 5% variation in the bias current (i.e. iref). The figure shows the variation of kgm_hi only.

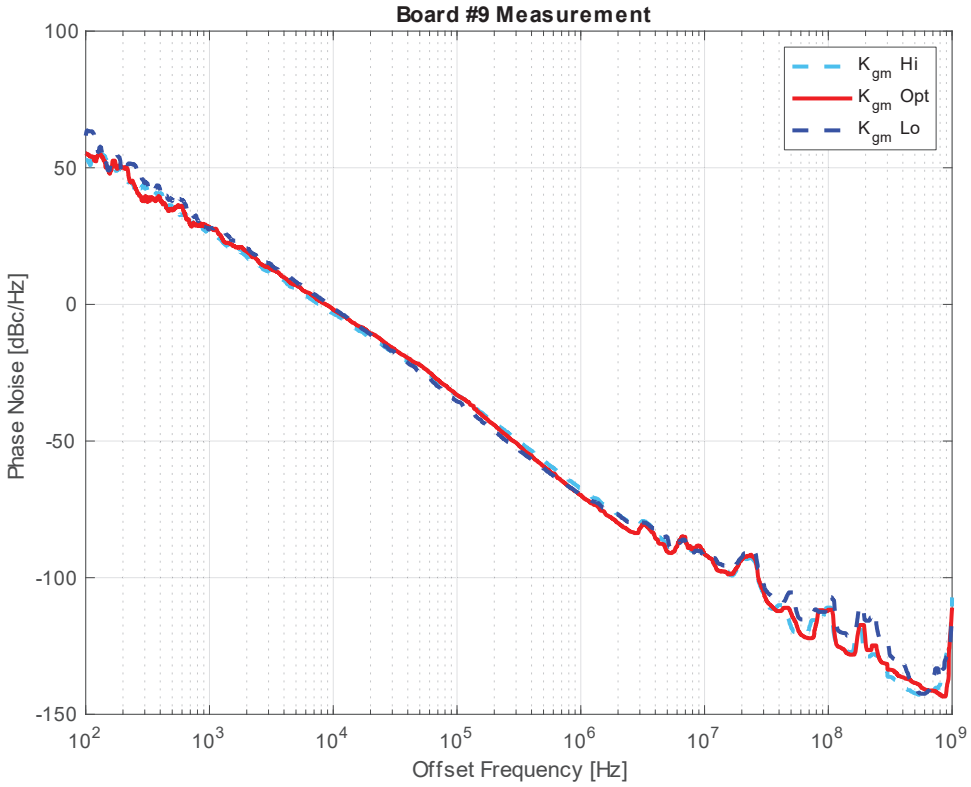


Figure 73: Board #9 – Phase Noise at 1GHz Oscillation Frequency (all kgm)

Fig. 73 represents the phase noise profile for all the oscillators on board #9. From 1kHz ~ 10 MHz the oscillators show similar phase noise profile. There are some bumps on the phase noise profile due to measurement artifacts.

4.8.3 Board #10 Measurement

The board #10 results are summarized in the following Tables (22, 23, 24). In Table 22, vref is chosen according to simulation for 1 GHz Oscillation frequency. The center frequency varies by 5.14%, 1.15% and 24.13% for kgm_hi, kgm_opt and kgm_lo respectively in measurement. In the next step, vref is tuned to achieve 1 GHz oscillation frequency in measurement and the results are shown in Table 23. Table 24 shows the phase noise results for the three oscillators @1GHz oscillation frequency.

Table 22: Board #10 - Frequency, Peak and Consumption of PCM (Default vref)

Kgm_hi				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
510	1051.4	-10.22	7.575	32
kgm_opt				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
480	1011.5	-9.93	7.54	32
kgm_lo				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
400	1241.3	-9.95	7.39	32

Table 23: Board #10 - Frequency, Peak and Consumption of PCM (Tuned vref)

kgm_hi				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
465	1001.5	-9.92	7.509	32
kgm_opt				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
468	1001.5	-9.81	7.519	32
kgm_lo				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
290	1001.5	-10.11	7.048	32

Table 24: Board #10 – Phase Noise

Offset Frequency	Phase Noise @1GHz Oscillation Frequency		
	kgm_hi	kgm_opt	kgm_lo
1k	24.3	29.8	33.4
10k	-4.66	1.79	2.43
100k	-35.66	-32.09	-36.34
1M	-68.75	-66.89	-70.34
10M	-92.26	-90.39	-92.97
100M	-109.84	-112.01	-107.93

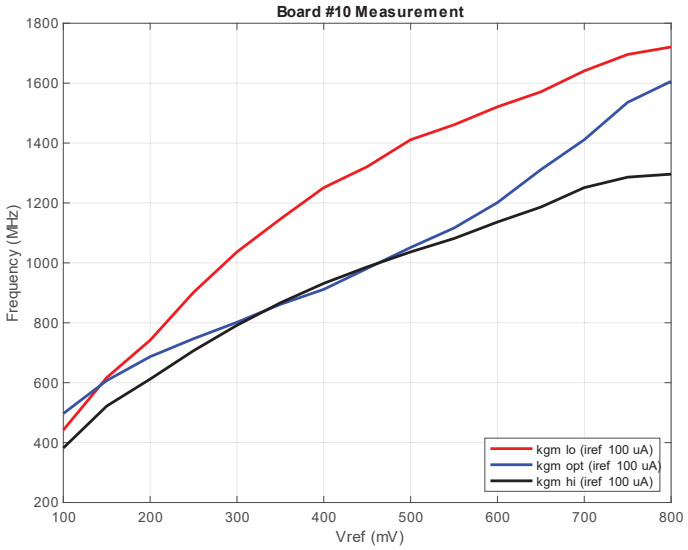


Figure 74: Board #10 - Oscillation Frequency vs. vref (iref 100 uA – all kgm)

Fig. 74 shows the variation of oscillation frequency with respect to the change in vref. The three different oscillators show different sensitivity with respect to vref in measurement. In this experiment, iref is fixed at nominal 100 uA.

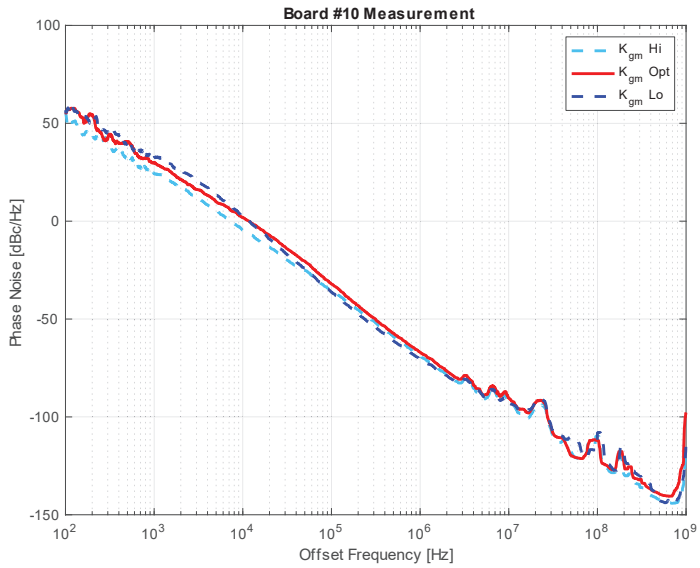


Figure 75: Board #10 – Phase Noise at 1GHz Oscillation Frequency (all kgm)

Fig. 75 represents the phase noise profile for all the oscillators in board #10. At lower offset frequencies, there is considerable variation of phase noise in board #10. There are some bumps on the phase noise profile due to measurement artifacts.

4.8.4 Board #11 Measurement

The board #11 results are summarized in the following Tables (25,26,27). In Table 25, vref is chosen according to simulation for 1 GHz Oscillation frequency. The center frequency varies by 11.14%, 24.13% and 27.62% for kgm_hi, kgm_opt and kgm_lo respectively in measurement. In the next step, vref is tuned to achieve 1 GHz oscillation frequency in measurement and the results are shown in Table 26. Table 27 shows the phase noise results for the three oscillators @1GHz oscillation frequency.

Table 25: Board #11 - Frequency, Peak and Consumption of PCM (Default vref)

kgm_hi				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
510	1111.4	-10.23	8.139	35
kgm_opt				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
480	1241.3	-10.04	8.102	35
kgm_lo				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
400	1276.2	-10.05	7.968	35

Table 26: Board #11 - Frequency, Peak and Consumption of PCM (Tuned vref)

kgm_hi				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
431	1001.5	-9.64	8.024	35
kgm_opt				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
354	1001.5	-9.61	7.85	35
kgm_lo				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
267	1001.5	-9.74	7.54	35

Table 27: Board #11 – Phase Noise

Offset Frequency	**Phase Noise @1GHz Oscillation Frequency**		
	kgm_hi	**kgm_opt**	**kgm_lo**
1k	25.61	28.23	30.03
10k	-3.19	0.71	-2.55
100k	-32.31	-33.82	-36.35
1M	-66.33	-68.85	-68.96
10M	-92.13	-91.93	-93.44
100M	-115.08	-113.37	-105.68

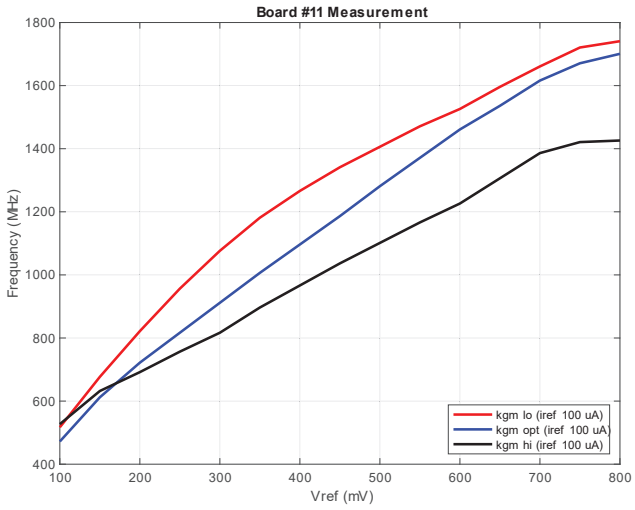


Figure 76: Board #11 – Oscillation Frequency vs. vref (iref 100 uA – all kgm)

Fig. 76 shows the variation of oscillation frequency with respect to the change in vref. The three different oscillators show different sensitivity with respect to vref in measurement. In this experiment, iref is fixed at nominal 100 uA.

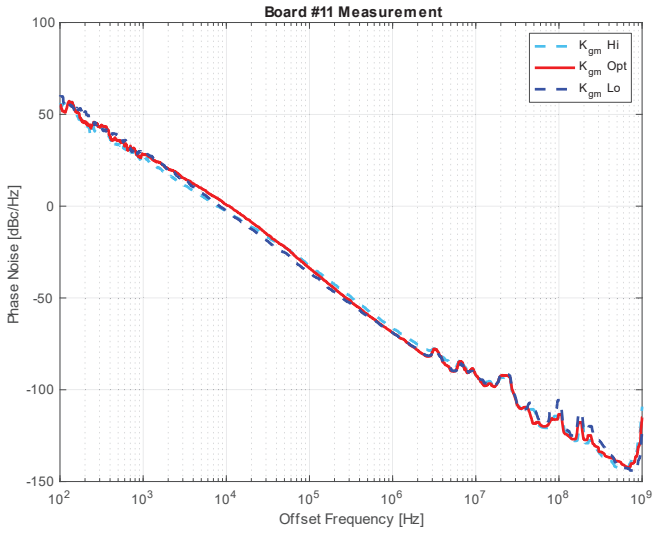


Figure 77: Board #11 – Phase Noise at 1GHz Oscillation Frequency (all kgm)

Fig. 77 represents the phase noise profile for all the oscillators in board #10. There are some bumps on the phase noise profile due to measurement artifacts.

4.8.5 Board #12 Measurement

The board #12 results are summarized in the following Tables (28,29,30). In Table 28, vref is chosen according to simulation for 1 GHz Oscillation frequency. The center frequency varies by 2.65%, 24.13% and 2.65% for kgm_hi, kgm_opt and kgm_lo respectively in measurement. In the next step, vref is tuned to achieve 1 GHz oscillation frequency in measurement and the results are shown in Table 29. Table 30 shows the phase noise results for the three oscillators @1GHz oscillation frequency.

Table 28: Board #12 - Frequency, Peak and Consumption of PCM (Default vref)

Kgm_hi				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
510	1026.5	-10.05	7.64	35
kgm_opt				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
480	1241.3	-10.03	7.603	35
kgm_lo				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
400	1026.5	-10.57	7.456	35

Table 29: Board #12 - Frequency, Peak and Consumption of PCM (Tuned vref)

kgm_hi				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
492	1001.5	-9.51	7.612	35
kgm_opt				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
341	1001.5	-9.35	7.314	35
kgm_lo				
vref (mV)	**Frequency (MHz)**	**Peak (dBm)**	**idd10 (mA)**	**idd15 (mA)**
376	1001.5	-9.27	7.4	35

Table 30: Board #12 – Phase Noise

Offset Frequency	**Phase Noise @1GHz Oscillation Frequency**		
	kgm_hi	**kgm_opt**	**kgm_lo**
1k	31.47	27.86	30.91
10k	-2.04	-0.82	0.78
100k	-35.45	-35.19	-36.28
1M	-68.09	-69.65	-70.46
10M	-90.68	-91.92	-91.43
100M	-112.43	-110.69	-111.3

Figure 78: Board #12 - Oscillation Frequency vs. vref (iref 100 uA – all kgm)

Fig. 78 shows the variation of oscillation frequency with respect to the change in vref. The three different oscillators show different sensitivity with respect to vref in measurement. In this experiment, iref is fixed at nominal 100 uA.

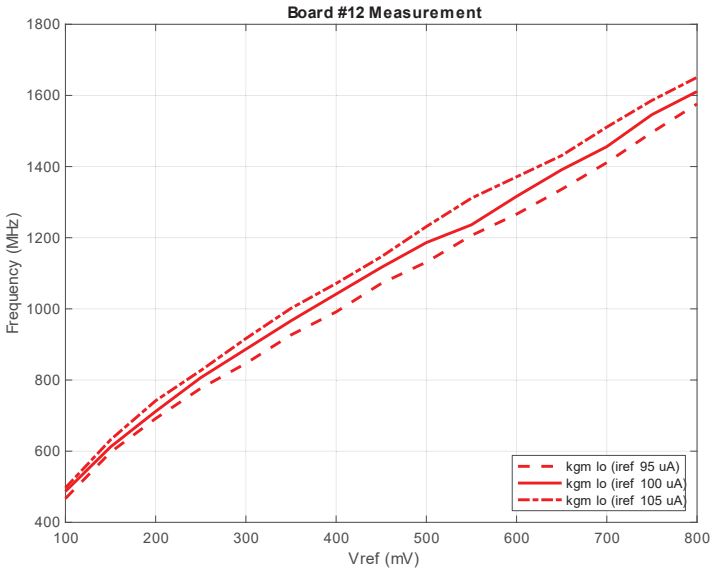


Figure 79: Board #12 - Oscillation Frequency vs. vref (iref varied 5% – kgm_lo)

Fig. 79 shows the variation of the sensitivity curve with 5% variation in the bias current (i.e. iref). The figure shows the variation of kgm_lo only.

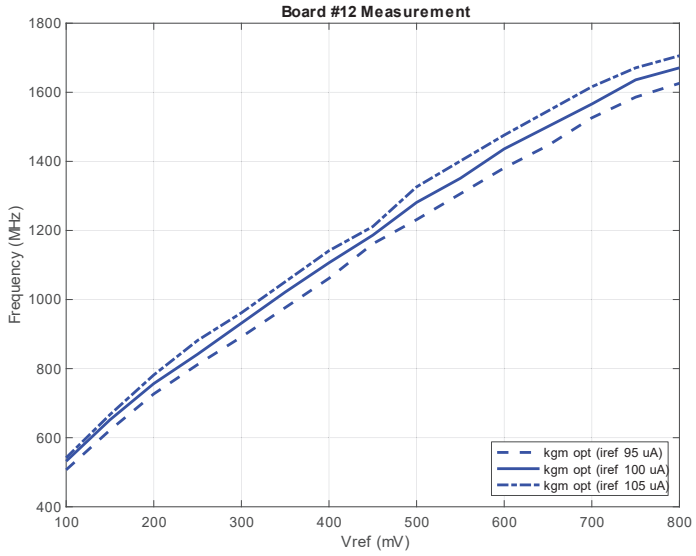


Figure 80: Board #12 - Oscillation Frequency vs. vref (iref varied 5% – kgm_opt)

Fig. 80 shows the variation of the sensitivity curve with 5% variation in the bias current (i.e. iref). The figure shows the variation of kgm_opt only.

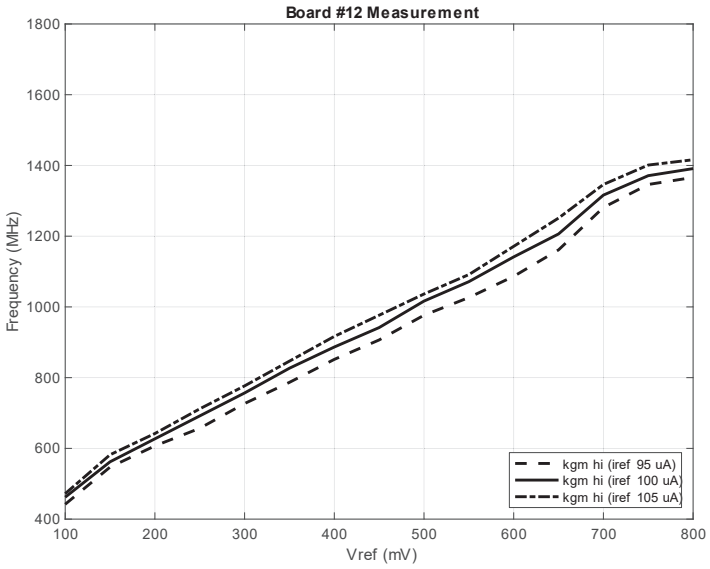


Figure 81: Board #12 - Oscillation Frequency vs. vref (iref varied 5% – kgm_hi)

Fig. 81 shows the variation of the sensitivity curve with 5% variation in the bias current (i.e. iref). The figure shows the variation of kgm_hi only.

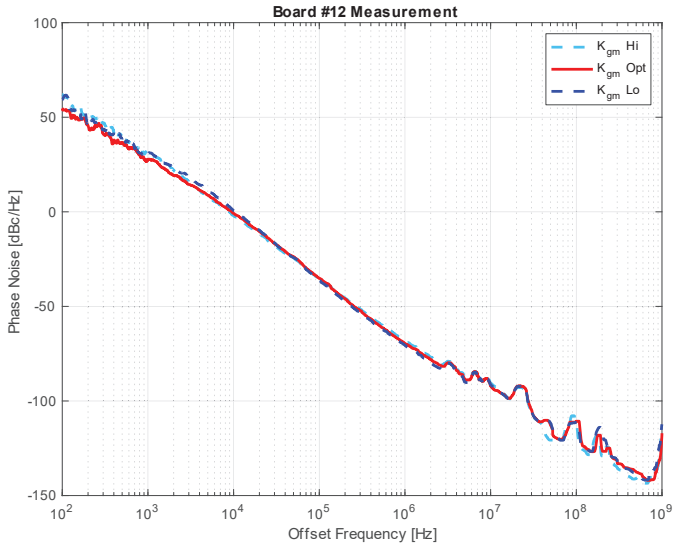


Figure 82: Board #12 – Phase Noise at 1GHz Oscillation Frequency (all kgm)

Fig. 82 represents the phase noise profile for all the oscillators in board #12. In the mid-band offset frequencies, the three oscillators phase noise profile show similar behavior. There are some bumps on the phase noise profile due to measurement artifacts.

4.8.6 Conclusion:

Based on the experimental results above, the following conclusions can be made in this section:

- **Conclusion 1:** Variability of all the three types of oscillators, measured using 7 different dies mounted on PCBs, is approximately the same with a maximum deviation of +/- 36%. This variation is rather high. Considering the fact these are ring oscillators, high variation is expected but not as much as 36%. This could be from the floating body core devices among other process variations.
- **Conclusion 2:** Phase Noise of all 3 oscillator are consistent, with the VCO having high K_{gm} showing the lowest Phase Noise.

5 High Bandwidth PLL Study

A study was conducted to see the effect of high frequency reference and high bandwidth on the phase noise and jitter of a synthesized tone in a PLL.

5.1 Design Approach

Synthesis of high-frequency tones in electrical systems is performed by the oscillator and any practical oscillator needs to be a VCO. Such an oscillator is in turn controlled by a feedback loop such as a PLL for two main reasons. Firstly, to ensure the tone produced is the desired frequency, and secondly has the purity required. The purity is stipulated by the final use case of the produced tone and is quantified using PN as the metric. To satisfactorily meet both targets, the PLL design can follow two approaches.

The burden in the first approach will be mainly on the design of a very low PN VCO exhibiting very good frequency selectivity ensuring the tone produced itself shows high purity. Following this, the VCO will be employed in a low-bandwidth PLL. In such an approach the PLL is responsible for maintaining only the desired frequency of the generated tone across all expected process, voltage, and temperature (PVT) variations. In addition, an adequate loop design is required to find a proper balance among different constraints, such as jitter transfer from reference, jitter peaking, bandwidth, and noise generation to not deteriorate the generated tone.

The second philosophy, targets achieving the same goals in a different manner. A wideband PLL is implemented that can adequately clean the noise produced by the VCO and other blocks on the forward path. This approach relaxes the design constraints of the VCO, CPC, and suppresses the supply-induced noise over a wider frequency range. Therefore, the main design target will be to expand the loop bandwidth to suppress a major part of the low-frequency noise with minimal jitter peaking and yet maintain a stable operation.

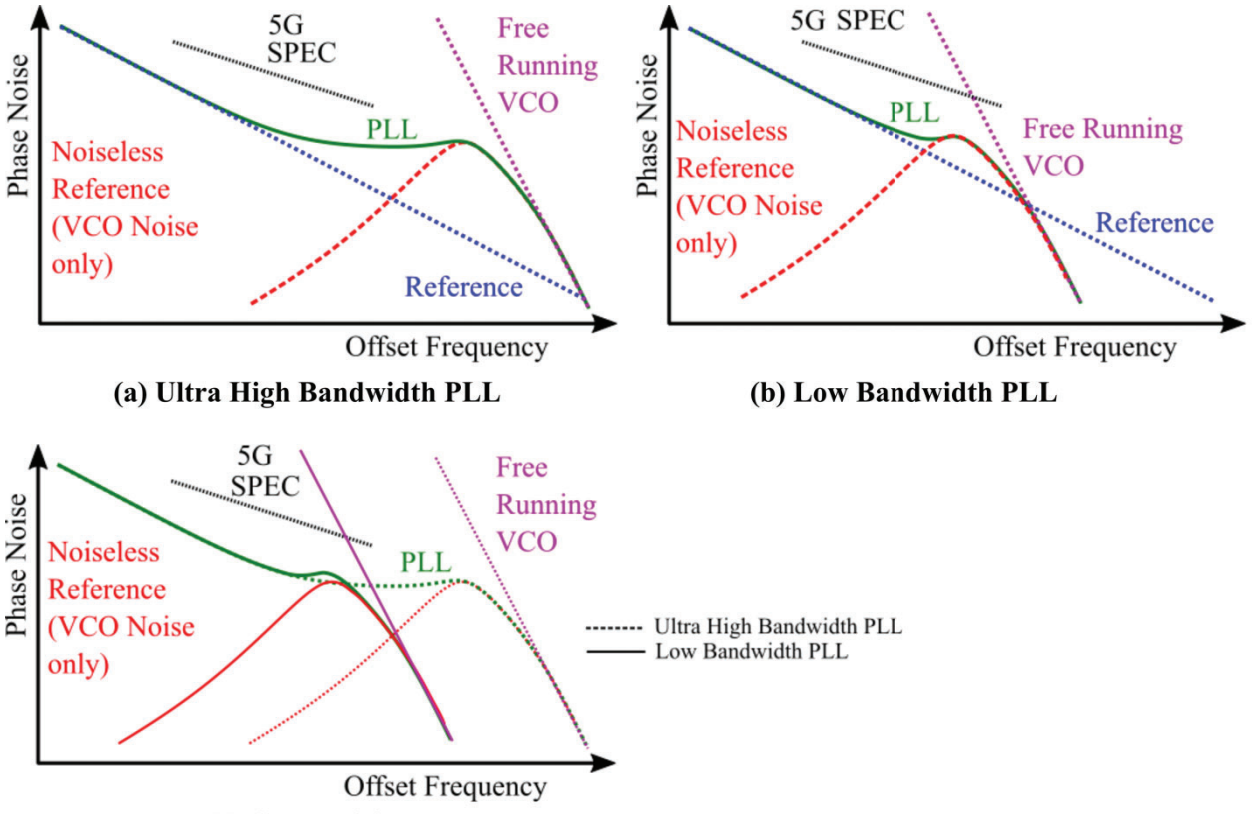
5.2 Strain on VCO

In the low bandwidth PLL approach the VCO is required to support two main requirements. Firstly, the VCO must have a wide frequency range such that it can service all the sub-channels used and allow the PLL to track PVT variations. To achieve a wide frequency range, a major portion of the capacitor budget resonating with the coil should be allocated to the controlled components such as capacitor banks and varactors. Indirectly, all parasitic elements on the main resonating nodes of the VCO must be reduced. Some of these are design choices, such as loading from the subsequent stages and cross couple devices. But a part of the parasitic elements is also intrinsic to the components and routing used which are hard to minimize, here a simpler layout and structure will help. Secondly, throughout this wide frequency range, the tones produced by the oscillator should exhibit high purity satisfying the PN requirement at higher offset frequencies. This translates to having complex resonating arrangements for the coil to exhibit the required high selectivity. Designing high-quality factor tanks, carefully simulated using advanced electromagnetic (EM) tools, is essential to implement such VCOs. The device parasitic elements and routing render the two requirements mutually exclusive translating to a strict trade-off, that scales exponentially with frequency.

The high bandwidth PLL approach simplifies the trade-off by decoupling the requirements passed on to the VCO. The VCO in this approach is required to only produce oscillations across the full required range. This allows the design to be simplified using a simple tank structure. An additional advantage of this is that the design can also be easily ported from one technology to another. Finally, the PLL is assigned the decoupled PN specification. By operating the PLL with a higher bandwidth, any PN from the VCO oscillations is sufficiently suppressed to meet the requirements.

5.3 Implications on Loop Dynamics

The detailed two approaches have characteristic differences in the requirements imposed on the loop of the PLL as detailed in Fig. 83. In the first case Fig. 83 b with the implemented highly selective tank, the free-running VCO can satisfy the PN specifications. The PLL loop is therefore required to only provide frequency corrections and make sure the VCO is always oscillating at the desired frequency. Following this, the phase corrections to be provided by the feedback loop of the PLL can have low bandwidth but need to be very stable to ensure robust operation. The low bandwidth operation ensures the reference noise and secondary noise sources do not degrade the generated clean oscillations.



(a) Ultra High Bandwidth PLL **(b) Low Bandwidth PLL**

(c) Comaprision

Figure 83: Comparison of the Phase Noise Profile in a Low Bandwidth and High Bandwidth PLL

In the second case Fig. 83 a, the VCO relies on the PLL loop to suppress the PN produced. To enable satisfactory suppression, the feedback loop gain of the PLL needs to have sufficient magnitude across the frequency band of interest. This high magnitude will have to be maintained well past the band of interest stipulated by the specification. One consequence of this is that noise is accumulated from a larger band, therefore additional care is to be taken in the design of the PLL components. For a second-order control loop given the natural frequency, choice of bandwidth and stability presents a trade-off. This is carried over to the PLL loop as well, a higher damping factor reduces peaking in the transfer function but reduces bandwidth. A lower damping factor increases bandwidth but also increases peaking in addition to making the loop unstable. This peaking in the transfer function manifests as an amplification of the jitter present. Therefore, the PLL loop damping factor must be carefully chosen after maximizing the natural frequency keeping the minimization of the total integrated jitter as the target.

5.4 Choice of Frequency of the Input Reference

The choice of reference frequency is one of the most important design decisions that can help in reducing the jitter accumulated. The chosen frequency of reference has a direct implication on the phase noise targets enforced on the VCO. This jitter accumulated by the PLL at the system level has two main sources: the VCO itself at a relative frequency much larger than the loop bandwidth and the reference well within the bandwidth of the PLL. The band of interest in which the jitter accumulated is independent of the reference frequency used and is defined for the frequency of tone generated. Therefore, the phase noise profile of the reference must be scaled with the proper division factor to estimate this contribution to the jitter within the bandwidth of the PLL. When a low frequency reference is used this division factor will be high and thus the scaling factor used is also high.

Shown in Fig. 84 is the phase noise profile of two ultra-low phase noise reference crystals, scaled to the same VCO frequency along with that of a state-of-the-art class-c VCO designed to exhibit as low phase noise as possible with 3rd harmonic resonance. For a low frequency reference, the phase noise at a relative frequency >10 MHz is worse than that of the free ruining VCO. This dictates the bandwidth of the PLL be «10 MHz to minimize the propagation of this phase noise to the output. At the same time, owing to its low scaling factor, the phase noise contribution from the higher frequency reference never goes above that of the free running VCO. This allows the PLL to as high bandwidth as needed, in fact as it is much lower than the free running VCO the higher the better. Fig. 83 also shows the phase noise profile of two PLLs designed with low and high bandwidth using the low frequency reference and high frequency reference respectively. As the low bandwidth reference exhibits a scaled phase noise much larger than the high bandwidth reference for any relative frequency >10 kHz, a PLL designed with this will accumulate more jitter in any band > 10 KHz. Additionally, as the high frequency reference allows the PLL to have a much higher bandwidth, the PLL can track the cleaner reference up to a higher relative frequency reducing the jitter accumulated further. The area highlighted in Fig. 84 shows this reduction and for a band from 1 kHz to 100 MHz is computed and shown above, estimated at 20 fs-rms for the same VCO.

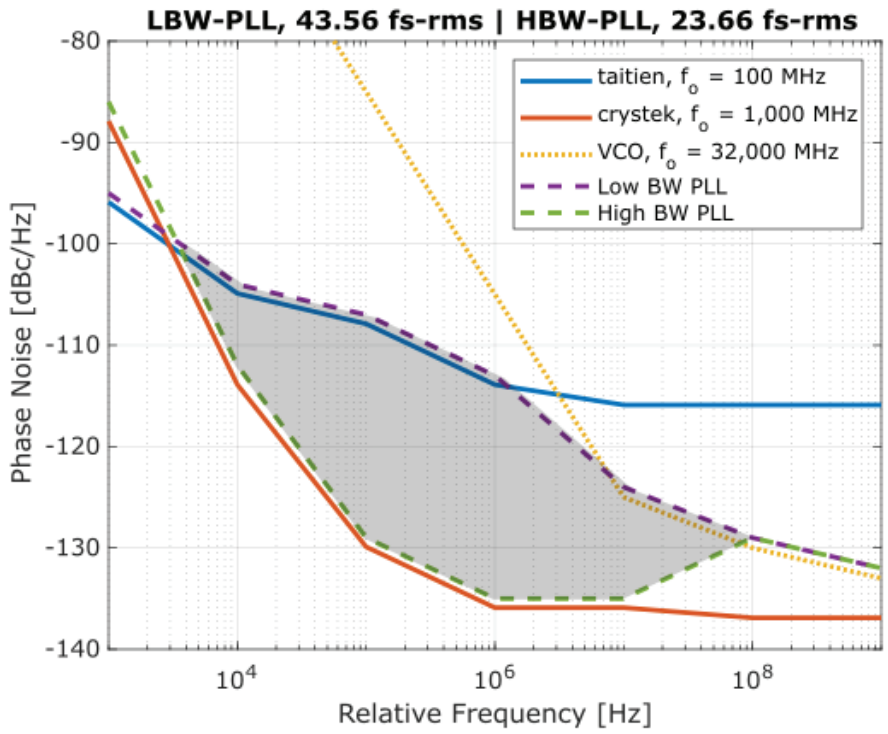


Figure 84: Phase Noise Comparison of a HBW PLL with High Frequency Reference and LBW PLL with Low Frequency Reference Operating with the Same VCO

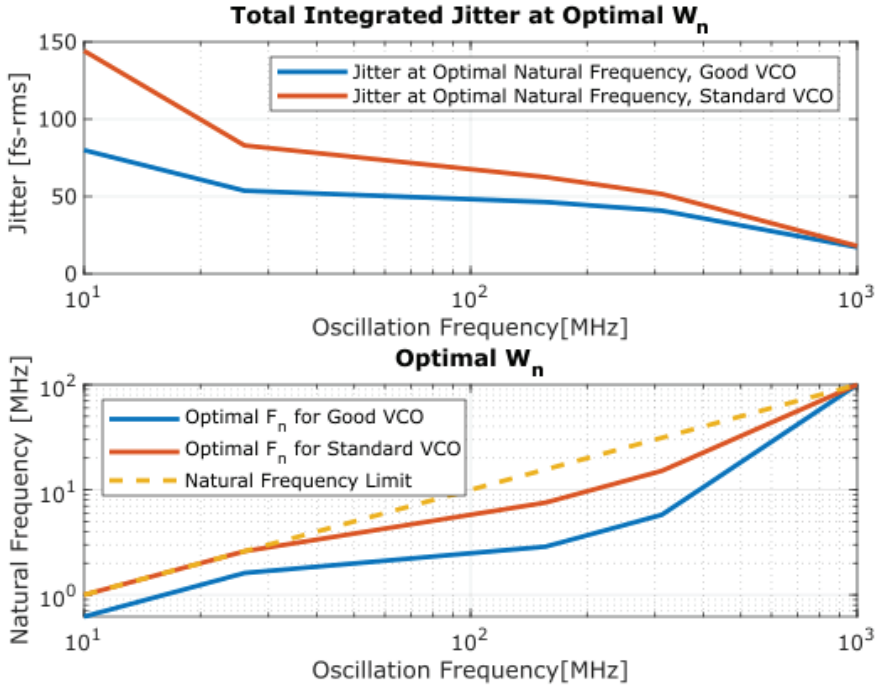


Figure 85: Comparison of Optimal Natural Frequency Resulting in the Lowest Jitter with Respect to the Reference Frequency and the Lowest Jitter Achieved

It follows that the optimal bandwidth for a PLL with minimizing jitter as the main objective is a function of the reference frequency. When the reference frequency is low, the bandwidth of the PLL must be reduced to minimize the contributions from the reference towards the jitter at the output. As the reference frequency increases, this optimal bandwidth should also increase linearly assuming all references produce the same amount of noise, which is rarely the case. The bandwidth for minimizing the jitter might not increase linearly if the phase noise from the reference increases. The point at which the jitter is minimized is when the contribution from the VCO is lower than that of the reference. The point can be lower for references which are noise. This relies on the VCO to have very low phase noise, as illustrated in Fig. 67 if the VCO is very clean the optimal point will be higher. In Fig. 85, the effect of increasing the reference frequency on minimizing the total integrated jitter in the band from 1 kHz to 100 MHz is visualized. For this, a set of ultra-low phase noise crystals at different oscillation frequencies are curated. The optimal natural frequency is chosen as the frequency for which a second order critically damped PLL loop transfer function produces the lowest jitter. Both the lowest jitter achieved, and optimal natural frequency chosen are plotted for each of the crystals. Clearly, for a VCO that is cleaner, the optimal natural frequency is lower than for the roughly 20dB worse. The more useful inference from Fig. 85 can be that the minimized jitter reduces with a higher frequency reference regardless of the phase contributed by the VCO and the effect of lower phase noise offered by the VCO on the jitter is reduced.

6 EEI Effort

Figure 86 provides an overview on EEI effort and its subtasks, based on SOW.

		2023						
		January	February	March	April	May	June	July
Task 1	Hire EE							
Task 2	Research Mkt Opportunities, Interview Stakeholders							
Task 3	VoC Dirven IP Library Requirements and Priorities							
Task 4	Preliminary Business Plan							
Task 5	DARPA Toolbox Support							
Task 6	Company Formation							
Task 7	Fundraising Preparation							
Task 8	ProspectiveCustomer Engagement							
Task 9	MVP Proposal							
Task 10	Program Management							

Figure 86: Project Schedule

6.1 Task 1 – Embedded Entrepreneur: Identify, propose, and hire an Embedded Entrepreneur (EE)

Working with Noble Reach company, few candidates were identified and interviewed. Eventually, Mr. Tom Rueckes was hired as an EE for this project. Mr. Rueckes engaged two other people in the project with the goal to cover technical and admin aspects of the work: Mr. Lee Cleveland and Mr. Greg Schmergel). The team was active till the end of project, i.e., November 15, 2023.

6.2 Task 2 – Market Strategy: Research Market Opportunity by Interviewing Prospective Stakeholders

We interviewed the companies listed in the SOW (Foundries/Fabless) and their unified response was that the only engagement model of interest is via government projects:

- Ongoing discussion with Tower and Intel Foundry regarding government projects and shuttle run:
    - Foundries suggested to talk to their customers to see if they want to buy our IP but fabless companies showed no interest in our IP (new startup without track record)
    - GlobalFoundries and SkyWater did not follow-up
- Established fabless and system companies from the SOW (ADI, Microchip, TI, and a few more) viewed us as competitors and did not want to engage. **Note:** SOW include a short list of companies as a suggestion to be interviewed.

Figure 87 shows the main outcomes of our discussions with different companies mentioned in the SOW.

Company	Date	Contact	Status / Outcome
Intel Foundry Services	04/25/23	Tao Zhou (Director, IFS)	1. IFS will make intros to their customers who could potentially use our IP 2. IFS interest is in high performance 60GHz+ / low jitter analog for Intel18A 3. is considering joint meetings with DARPA when time is right
Intel Labs	05/19/23	Narayan Srinivasa (Director, Machine Intelligence Research Programs)	1. Working through DARPA or Micro-Electronics Commons ($1.6B ChipsAct fund from DOD) is the best approach to get business with Intel/Intel Labs. Would be Intel Labs prototyping project on Intel16 process using our designs and would give us access to Intel technology and advanced packaging 2. Intel Labs is interested in discussing DARPA/DOD funded projects using our technology 3. Intel Labs avoids using design services from startups unless required by DOD restrictions (in case Intel internal resources are international) 3. pursue NDA & BU sponsorship for our tech
Tower	06/29/23	David Howard (Exec. Dir./Fellow)	Recommended to talk to Tower customers
GlobalFoundries	05/02/23	Julio Costa (VP RF Technology), Jack Pekarik (Fellow, RF TD), Joe Alvin (Sr. Fellow)	1. GF is interested in RF reference design from us which has been optimized to utilize benefits of GF technology so they can attract foundry customers 2. Julio recommended to pursue very high frequency apps, incl fiberopticspace (Cisco, ADI & also smaller fiberoptic-specific companies which need RF designs) 3. GF is interested in DARPA/DOD funded projects requiring our designs 4. GF aggregator program is in the works to provide portal for startups like us to engage with GF (timeline TBD)
SkyWater	06/13/23	Terry Danzer (Sr. Director, Platform Marketing); Rory Buchana (Sr. Director IP & Design support)	- follow-up meetings planned with A&D Bus Dev and Heteregoneous Integration - interested to work with us on a project; DARPA/DOD funding important
Skyworks		Mark Thompson (SVP, Mixed Signals)	Sent meeting request. No response
Qorvo		Craig Callahan (VP, Quality)	Sent meeting request. No response
Analog Devices	05/25/23	Dimitry Goder (Sr. Director, Design)	Recommended that we should prepare presentation on system level benefits for our ultralow jitter designs and approach system customers and their chip suppliers to identify specific use cases where it provides product benefits. This is a great suggestion and we will pursue it aggressively.
TI	04/12/23	Rinn Cleavelin (TI/Sematech COO)	1.Highest frequencies analog of interest 2.TI Lehi/UoUtah workforce education important
Broadcom			Discussed with Stan Reiss (Matrix) & Ralph Schmitt regarding PLL clock startup with ex Broadcom Executives
Microchip		Mark Reiten (VP, Licensing)	not interested in meeting
Xilinx			not good product fit
Altera			not good product fit
Qualcomm		John Han (SVP, Licensing)	Sent meeting request. No response.
Raytheon	04/26/23	Jim Rooney (Analog Engineer)	1. Highest frequencies analog of interest (radar)
Lockheed Martin			No contact
Northrup Grunman		Paul Feinberg (GM, Ext. Tech. Partnership)	Sent meeting request. No response.
BAE Systems	05/11/23	Steven Turner (Chief Scientist, Mixed-Signal IC Research), Greg Flewelling (Product Director, Mixed Signal Integrated Circuits)	1. BAE radhardening of our IP might be possible engagement scenario. BAE would be storefront for our radhardened designs then for their customers (large defense contractors) 2. BAE might be interested in SERDES from us (and maybe data converters; no interest in PLL as they are strong internally). BAE will check internally on BU interest and then go to NDA next. Main issue for BAE with existing SERDES IP is high cost. BAE suggested to work through DARPA for a potential SERDES engagement. 3. direct sampling of lower interest to BAE due to wideband noise concerns (in contrast to Raytheon, TI and Intel)
National Labs			Will contact once business plan is fixed

Figure 87: Company List Based on SOW

We discussed also with various additional companies (beyond the ones listed in the SOW) regarding IP blocks. The outcome is the following (the summary can be found in Fig. 88):

- Analog Bits
  - No interest in mmWave IP
- Anokiwave
  - Already has existing designs which are sufficient for advanced 5G smart antennas.
- Renesas
  - The CTO and his staff reviewed our IP and concluded that our PLLs are state-of-the-art, but that Renesas has no business needs.
- Ripple Technology
  - Wanted DAC/ADC IP but decided to go with existing IP instead of our custom design proposal.
- Silicon Technologies
  - Needs mmWave PLL designs from design services contractor, but work must be performed by US citizens (we do not have this staffing)
- Product drivers for mmWave PLLs
- 6G: ultralow jitter PLLs have value for Massive MIMO/6G; current 5G does not need improved PLLs.
- Radar: more precise with lower jitter PLLs but no volume market needs for better radar (existing radar tech good enough for autonomous driving).

- Potential niche government applications possible

Company	Meeting Date	Contact	Status / Outcome
Rambus		Phuong Le (Architect)	Most IP business for PLL taken over by EDA companies. SERDES products still can be done by small companies
Black Forest / UMI	06/01/2023	Jon Faue (former CEO)	practical pointers how to market and build design services company
Analog Bits	06/19/2023	Mahesh Tirupattur (EVP)	Focus on 1 fab initially; FinFet is good tech for new RF IP; consider ultrahigh performance ADC & SERDES + ultralow jitter PLL for clock applications; no interest in our PLLs for his company
Ripple	06/29/2023	Charles Hu (Director, Design)	Requested business proposal for ADC design but decided to go with other vendor who already had IP ready to go
ON Semiconductor	07/03/2023	Verne Hornback (Director, New Products)	Suggested to talk to the acquirer of ON's Radar BU regarding PLLs for high precision, short range radar; could not get contact
Synopsys	07/06/2023	Rob Aitken (Technology Strategy, Distinguished Architect)	Interested in our high precision PLL etc. designs for backporting to older nodes & our analog design automation techniques; project is being kicked off
Micron	07/12/2023	Tim Hollis (Fellow, Interface pathfinding)	Potential interest in fast wake-up time PLLs but no follow-up; not good fit
Micron VC	07/19/2023	Andrew Byrnes	Maybe interested in analog design startup
Sipex/Exar (former CEO)	07/21/2023	Ralph Schmitt	Good market for differentiated clocks if part of bigger designs; SerDes too difficult
Matrix Partners	07/25/2023	Stan Reiss (VC)	Difficult to commercialize PLL clocks themselves. Mixed-Signal (ex Broadcom executives) are trying but branched out to radar as it's difficult to build the PLL clock business. Radar application makes sense for PLLs but radar startups not VC investable. Macro environment not suitable for radar startups as existing radar tech is good enough for autonomous driving (main product driver). Lots of VC investment a decade ago for autonomous driving radar development mainly failed. SerDes, Broadband too difficult. PLL needs to be commercialized as part of a bigger chip. Made intros to Skyworks and Anokiwave
Anokiwave	07/31/2023	Rob McMorrow (VP, Engr)	6G might have need for more precise PLLs; PLLs need to be commercialized ir bigger designs

Figure 88: Additional Companies Interviewed

6.3 Task 3 – Voice of the Customer driven IP library content requirements and development prioritization

The strategy of developing IP based business was also considered as part of this project. The goal is to build IP library via immediate term funded projects:

- PLL
  - GF22nm via Synopsys – Mar '24 (design verification)
  - Intel16 via DOD MPW – Dec '24 (silicon verification)
- Complete RF beamforming system via STTR – Sep '25 (silicon verification)
  - low-noise front-end receiver circuit (incl. amplifier, demodulator, ADC, frequency synthesizer
  - efficient power amplifier, modulator, digital-to-analog converter
  - Fab will be Intel or Tower Jazz
- Target specifications and documentation will be developed as part of the projects.

IP Name	TSMC 40nm	GF 22nm	TJ 0.18um	GF 45 RFSOI	TSMC 28nm	Specifications
PLL Ring Oscillator	X	X				3.125 to 6.25 GHz
PLL LC			X	X	X	Range: 27-32 GHZ, RJ = 30 fs-rms, Phase noise -125 dBc/Hz @1MHz
LVDS Transmitter / Receiver		X				800 Mb/s
SerDes Analog PHY		X				16 Gbps
SerDes Analog PHY	X					12.5 Gbps
SerDes Analog PHY	X					6.25 Gbps
ADC SAR					X	7b 500 MSps

Figure 89. List of Current IP Building Blocks

6.4 Task 4 – Preliminary Business Plan

The key business objectives were identified to be:

- Phase 1: Design Services, Government Projects & strategic commercial projects to build IP portfolio.
- Phase 2: IP licensing (list of IP blocks provided in Figure 89).

KratosIC has silicon-proven designs and expertise in mmWave designs with competitive figures of merit (ultralow jitter, area, power):

- KratosIC also has analog design automation techniques for cost effective design porting.
- Current Solution Providers for mmWave IP is predominantly Synopsys and the analog fabless companies have their own designs.
- There are specialized providers mainly for government applications, such as Silicon Technologies

One key observation was that the mmWave IP is crowded field and KratosIC will specialize on projects for which specific design IP is needed and which is not serviced by Synopsys. KratosIC has a novel analog design automation approach which is more universally applicable than prior approaches. US Government is securing critical designs and large number of RF design porting projects are expected over the next few years and KratosIC is intending to pursue this business.

KratosIC will pursue the IP roadmap outlined in the Task 3 deliverable report. Government funded and strategic corporate project will be used to build IP portfolio. Resources will be staffed as permitted by the amount of funding available from the projects.

Current active projects will be used to build out IP library and for getting traction, so the company becomes financeable for Venture investments; active projects include:

- Synopsys
    - Synopsys JDP for porting GF 45nm to GF 22nm using KratosIC analog design automation techniques.
    - Synopsys makes EDA resources available for free to KratosIC.
    - Once this initial Synopsys project has been completed, the plan for the next phase will be worked out. Options are design services for Synopsys porting projects or commercialization of the KratosIC analog design automation software as EDA tool.
- Intel Foundry
    - DOD approval for Intel16 MPW looks promising. MPW will be used for building out reference designs.

- STTR (Intel or Tower)
    - Complete RF beamforming system via STTR – Sep ‘25 (silicon verification)
    - low-noise front-end receiver circuit (incl. amplifier, demodulator, ADC, frequency synthesizer
    - efficient power amplifier, modulator, digital-to-analog converter
    - Fab will be Intel or Tower Jazz
- Once these projects are more advanced, we can develop a detailed go-to market plan and funding requirements.

6.5 Task 5 – DARPA Toolbox Support

All the Toolbox/IP Vault deliverables are in a directory and ready to upload once the NDA transfer agreement with University of Utah is signed. University of Utah will sign the transfer agreement/NDA in the next few days. The following data is ready for upload:

- Circuit Tower Jazz 180nm
- Circuit GF 45nm
- GDS Tower Jazz 180nm
- GDS GF 45nm
- Information 180nm PLL.xlsx
- Information 45nm PLL.xlsx
- KratosIC Marketing Slide.pptx
- Circuit Characterization and Qualification Plan.xlsx
- Datasheet 45nm (V1).docx
- Datasheet 180nm (v1).docx
- 45nm PLL Testing Report.pptx
- 180nm PLL Testing Report.pptx
- Results Phase 1.pptx
- Information.xlsx
- Layout and Simulation Setup.pdf
- Importance of Porting.docx
- Results Phase 1.pdf
- Results Phase 2.pdf

6.6 Task 6 – Company Formation

Company Formation done – Delaware C Corp – KratosIC, Inc. UoU provided draft agreement for IP licensing terms (license option). Terms of license will be negotiated after this option has been exercised. Projected revenue can be determined once concrete business opportunities have materialized. Prof. Tajalli will have part time role in the company compatible with his Professorship position at the University of Utah.

6.7 Task 7 – Fundraising Preparation

We are planning to get initial funding for KratosIC via STTRs to build up IP portfolio as outlined previously, including DOD MPWs, Intel16/GF22nm and complete RF beamforming system (low-noise front-end receiver circuit incl. amplifier, demodulator, ADC, frequency synthesizer and efficient power amplifier, modulator, DAC). In addition, we are starting a project

with Synopsys on design porting using KratosIC analog design automation software. Upon completion of these projects in 2024/25, KratosIC should be in a VC fundable state.

6.8 Task 8 – Prospective Customer Engagement

Synopsys wants to evaluate KratosIC analog design automation via porting of our GF45nm PLL to GF 22nm:

- Synopsys will provide all required design tools to KratosIC
    - 2 Custom Compiler Front End
    - ICV
    - StarRC
    - PrimeWave
- Status: Synopsys is preparing site ID for KratosIC and then send Cloud Service Evaluation Agreement (CSEA) as next step
- Once Synopsys sees value in KratosIC technology then they will consider details regarding Phase 2 engagements.

The next possibility is to apply for a STTR proposal. The fabrication options are Tower and Intel Foundry.

6.9 Task 9 – Develop Proposal for DARPA Minimum Viable Product (MVP) Funding

KratosIC is working on 3 projects towards the MVP proposal:

- STTR Phase 1 project to result in commercially attractive IP library, significantly broadened beyond current offering:
    - Complete RF beamforming system
        - low-noise front-end receiver circuit (incl. amplifier, demodulator, ADC, frequency synthesizer)
        - power amplifier, modulator, DAC.
    - Customer feedback will be used for MVP proposal to include custom modifications of existing designs to fit customer needs.
- Synopsys Phase 1 automated design porting project so that Synopsys commercialization path is clear:
    - Synopsys commercialization options include KratosIC design services and KratosIC EDA tool development for analog design automation.
- Foundry MPW projects with Intel and Tower to build out KratosIC portfolio and port STTR RF beamforming system to different nodes and modify according to customer requirements.

6.10 Task 10 – Program Management

KratosIC's IP portfolio was presented to various foundries, IDMs and fabless companies in the RF/analog space.

- No commercial traction materialized as described in Deliverable 2 (explained under section 6.2. Task 2):
    - KratosIC portfolio was not broad enough but very focused on PLLs.
    - Foundries only interested in product designs resulting in wafer sales and not interested in IP from unproven startup.

    - Analog IDMs and Fabless companies perceived KratosIC as competitor and were not interested in engaging.

Based on customer discussions it became clear that the following 3 application areas are the commercial drivers for our ultralow jitter mmWave PLLs

- 6G: needs very low jitter PLLs for Massive MIMO (5G does not need improved PLLs)
- Radar: precision can be improved with lower jitter PLLs.
- Details are described in Deliverable 3 (see Section 6.3. Task 3).

Current active projects will be used to build out IP library and for getting traction, so the company becomes financeable for Venture investments; active projects include:

- Synopsys
    - Synopsys JDP for porting GF 45nm to GF 22nm using KratosIC analog design automation techniques.
    - Synopsys makes EDA resources available for free to KratosIC.
    - Once this initial Synopsys project has been completed, the plan for the next phase will be worked out. Options are design services for Synopsys porting projects or commercialization of the KratosIC analog design automation software as EDA tool.
- Intel Foundry & Tower
    - DOD approval for Intel16 MPW looks promising. MPW will be used for building out reference designs.
- STTR (Intel or Tower)
    - Complete RF beamforming system via STTR – Sep ‘25 (silicon verification)
    - low-noise front-end receiver circuit (incl. amplifier, demodulator, ADC, frequency synthesizer
    - efficient power amplifier, modulator, digital-to-analog converter
    - Fab will be Intel or Tower Jazz

Plan details are explained in Section 6.4.

Company Formation, DARPA toolbox, fundraising preparation, customer engagement and MVP funding tasks was completed as explained in Deliverables 5, 6, 7, 8, and 9 (Sections 6.5, 6.6, 6.7, 6.8). The projects established during the EIR project, Synopsys Phase 1 collaboration + STTR beam forming system design + Intel/Tower IP library buildouts should be completed, to create sufficient commercial traction for pursuing VC and MVP funding:

- STTR Phase 1 project to result in commercially attractive IP library, significantly broadened beyond current offering.
    - Complete RF beamforming system
        - low-noise front-end receiver circuit (incl. amplifier, demodulator, ADC, frequency synthesizer)
        - power amplifier, modulator, DAC.
    - Customer feedback will be used for MVP proposal to include custom modifications of existing designs to fit customer needs.
- Synopsys Phase 1 automated design porting project so that Synopsys commercialization path is clear.

- Synopsys commercialization options include KratosIC design services and KratosIC EDA tool development for analog design automation.

Foundry MPW projects with Intel and Tower to build out KratosIC portfolio and port STTR RF beamforming system to different nodes and modify according to customer requirements.

7 CONCLUSIONS

The primary focus of the second phase of this project (Phase II) was on design, analysis, implementation, and test of a set of Phase-Locked Loops (PLLs) and some other test circuits (i.e., ring oscillators). A sub-sampling PLL architecture was developed to satisfy the phase noise requirements of this project. A novel sub-sampling phase detector also was developed to enable high-speed and low-noise operation, simultaneously. Supported by experimental data, the phase noise of the PLL was shown to be within the spec defined for this project. Measurement data for three different types of ring oscillators was provided to evaluate their performance and study the process variation in GF 45 RFSOI technology.

In parallel to the technical tasks, a commercialization activity also was performed. As part of this activity, some target companies were interviewed and a company was formed, and a minimum viable product strategy was developed.

8 REFERENCES

[1] A. Tajalli, "Power-Speed Trade-Offs in Design of Scaled FET Circuits Using C/IDS Methodology," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 2, pp. 631-640, Feb. 2021, doi: 10.1109/TCSI.2020.3036683.

APPENDIX A – Publications and Presentations

The team has submitted the following articles for publication:

(i) Presented in GOMACTech conference: A 59-fs-rms 35-GHz PLL with FOM of -240 dB in 0.18 µm BiCMOS/SiGe Technology, March 2022.

(ii) Presented in IEEE RFIC conference: A 59-fs-rms 35-GHz PLL with FOM of -240 dB in 0.18 µm BiCMOS/SiGe Technology, June 2022.

(iii) Published in the IEEE TVLSI: Optimal Design of Loop Circuit Topologies Using C/IDS Methodology, August 2022.

(iv) Accepted (minor modifications) in IEEE TCAS-II: Noise-Aware Circuit Design Using C/IDS Methodology.

(v) Accepted in IEEE ISCAS 2023: Complexity Analysis of Different Analog Design Methodologies.

(vi) Accepted in IEEE CICC 2024: A 29 GHz Sub-Sampling PLL with 25.6-fs-rms RJ based on a Discrete-Time Integrating PD in 45nm RF SOI.

APPENDIX B – Publications Used for Comparison

- Y. Hu *et al*., "**17.6 A 21.7-to-26.5GHz Charge-Sharing Locking Quadrature PLL with Implicit Digital Frequency-Tracking Loop Achieving 75fs Jitter and −250dB FoM**," *2020 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2020.
- H. Wang and O. Momeni, "**A Charge Pump Current Mismatch Compensation Design for Sub-Sampling PLL**," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 6, pp. 1852-1856, June 2021.
- A. Bhat and N. Krishnapura, "**A Reduced-Area Capacitor-Only Loop Filter with Polarity-Switched G_m for Large Multiplication Factor Millimeter-Wave Sub-Sampling PLLs**," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 1, pp. 160-171, Jan. 2022.
- W. Chen *et al*., "**A 21.8-41.6GHz Fast-Locking Sub-Sampling PLL with Dead Zone Automatic Controller Achieving 62.7-fs Jitter and −250.3dB FoM**," *2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Denver, CO, USA, 2022.
- Y. Zhao, M. Forghani and B. Razavi, "**A 20-GHz PLL with 20.9-fs Random Jitter**," in *IEEE Journal of Solid-State Circuits*, vol. 58, no. 6, pp. 1597-1609, June 2023.
- Y. Zhang *et al*., "**A Sub-50fs-Jitter Sub-Sampling PLL with a Harmonic-Enhanced 30-GHz-Fundemental Class-C VCO in 0.18µm SiGe BiCMOS**," *ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC)*, Grenoble, France, 2021.
- M. D. Hickle, K. Grout, C. Grens, G. Flewelling and S. E. Turner, "**A Single-Chip 25.3–28.0 GHz SiGe BiCMOS PLL with −134 dBc/Hz Phase Noise at 10 MHz Offset and −96 dBc Reference Spurs**," *2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, Monterey, CA, USA, 2021.
- R. Bindiganavile, A. Wahid, J. Atkinson and A. Tajalli, "**A 59-fs-rms 35-GHz PLL with FoM of −241-dB in 0.18−µm BiCMOS/SiGe Technology**," *2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Denver, CO, USA, 2022.

LIST OF SYMBOLS, ABBREVIATIONS, AND ACRONYMS

ACRONYM	DESCRIPTION
3D	3-Dimension
BAA	Broad Agency Announcement
BUF	Buffer
CoB	Chip on Board
CPC	Charge Pump Circuit
CMOS	Complementary MOS
CML	Current Mode Logic
DIV	Divider
ECL	Emitter Coupled Logic
FLA	Frequency Lock Assist
GUI	Graphical User Interface
I/O	Input/Output
IR	Voltage drop across a resistor due to current flow
LO	Local Oscillator
LF	Loop Filter
MPLL	Matrix PLL
MOS	Metal-Oxide-Semiconductor transistor
MVP	Minimum Viable Product
PA	Power Amplifier
PFD	Phase Frequency Detector
PLL	Phase Locked Loop
PCB	Printed Circuit Board
PCM	Process Control Monitor circuits
PN	Phase Noise
PTM	Predictive Technology Model
RF	Radio Frequency
SMA	Sub-Miniature version A
SMB	Sub-Miniature version B
SMD	Surface Mounted Device
SOW	Statement of Work
UofU	University of Utah
UUT	Unit Under Test
VCO	Voltage Controlled Oscillator
XTAL	Crystal oscillator
DCDA	DCD Aligner