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Operation of HTS Digital Circuits at Elevated Temperatures: Beating Thermal Activation

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14. ABSTRACT
Based on the calculations and simulations of digital SFQ and RSQ circuits, which included the kinetic inductance of the circuit, show that a 1-layer technique with HIB-JJs would not work at elevated temperatures. Instead, a 2-layer technique allows to significantly reduce the influence of the kinetic inductance and a 3-layer technique would even allow superconducting wiring with vias. Since the latter is not available, the design proceeded with the 2-layer technique. Combining this 2-layer technique with an additional insulated normal conducting layer (e.g. Au-layer) allows for the design of RQL and SFQ circuits. These circuits have been simulated and will be combine into a test circuit consisting of a dc-toSFQ converter, followed by a JTL, a 2 stage shift register, another JTL and a SFQ-to dc converter.

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Operation of HTS Digital Circuits at Elevated Temperatures: Beating Thermal Activation

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Design Considerations

As shown in a previous report [1], the kinetic inductance of very thin films as used for Helium Ion Beam Written Josephson Junctions (HIB-JJs) [2] is quite large. For these YBCO-films with a penetration depth of $\lambda \approx 300\ nm$, one expects a kinetic inductance per length of 1pH/µm for a 3 µm wide line. A superconducting square loop of 13 µm x 13 µm outer dimension and 3 µm conductor width has a magnetic inductivity of about $L_g = 7$ pH – if it is made from the 40 nm thick YBCO film, the kinetic inductance is $L_k = 4 \cdot 10$ pH $= 40$ pH, significantly more than the magnetic inductance. A 400 nm thick film in contrast has only a kinetic inductance of 0.1 pH/µm, resulting in only a small contribution to the total inductance of the square loop.

The activation rate *R* can be selected and determines the thermally-activated error rate. The selection determines the ratio I_c/T and thus the minimum critical current I_c of the Josephson junction for a given temperature.

$$R = \Gamma \exp -\frac{E_J}{E_T} = 10^{12} s^{-1}\ exp -\frac{\Phi_0 I_c}{2\pi\ kT}$$

A high activation rate makes a digital circuit unreliable. For the following discussion, we select a medium activation rate of $R = 10^{-6}$ and an operating temperature of 77 K.

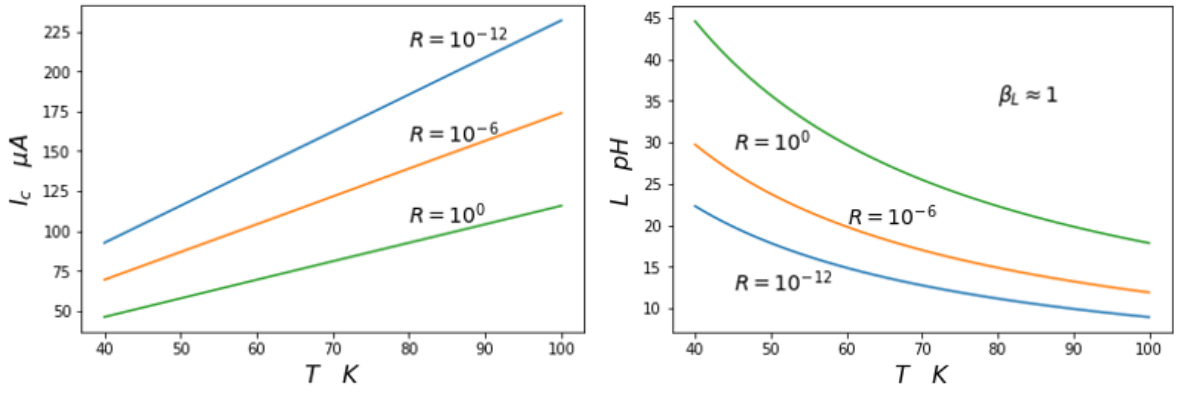

Figure 1: Minimum critical current and resulting inductance for an SFQ-loop as function of temperature.

The resulting values for the critical current and the loop inductance for an SFQ-loop with $\beta_L = LI_c/\Phi_0 \approx 1$ are listed in table 1:

Table 1 : Kinetic and magnetic inductance of a square loop of 13 um length and 3um conductor width for a 40 nm and 400 nm thick film.

t	$L_k/\,l$	$L_g\square$	L	$I_{c,min}$	L_{max}
40 nm	1 pH/µm	7 pH	47 pH	140 µA	17 pH
400 nm	0.1 pH/µm	7 pH	11 pH	140 µA	17 pH

It is obvious that for the 40 nm film the loop inductance *L* will be much larger than the maximum allowable inductance L_{max}. For smaller thermal activation rates, the mismatch will only become larger. In contrast, with the 400 nm thick film there is even some room for design decisions: the total inductance of 11 pH for the square loop is significantly smaller than the maximum loop inductance of 17 pH. It would even allow to increase the critical current by more than 50%.

This design restriction means that for the HIB-JJs a 2-layer process is absolutely necessary! The conductor, in which the HIB-JJ has to be written needs to be deposited as last layer. A thinning of a layer would damage the film too much and significantly reduce the critical temperature of the film.

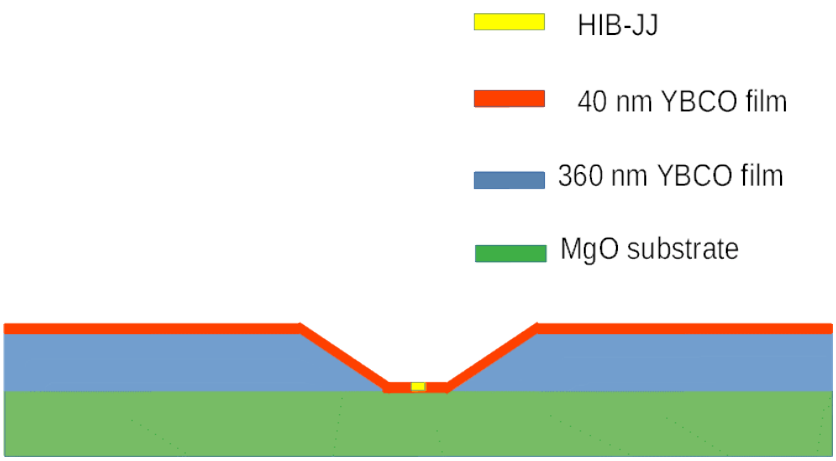

Figure 2 : Schematic drawing of the 2-layer preparation of a HIB-JJ in-line with a conductor.

The preparation of these 2-layer structures proceed in the following way:

(1) Clean and prepare the substrate, if necessary deposit a buffer layer.
(2) Deposit the 360 nm YBCO film (A).
(3) Structure the film for the base wiring.
(4) Structure the areas where HIB-JJs will be written with sloped angles (< 35dg to prevent low critical current density grain boundaries).
(5) Deposit the 40 nm film (B) on top.
(6) Structure the film like the base wiring of film A, but do not structure the HIB-JJ areas.

(7) Write the HIB-JJs in the prepared 40 nm HIB-JJ area.

Step (4) is especially important to achieve coverage of the slopes without creating low critical current grain boundary junctions. These would be in series with the HIB-JJs and clutter the IV-characteristics the junctions and inhibit regular function of the superconducting circuit.

Preparation of vias in a 2-layer technique

For non-trivial superconducting digital circuits at least a 2-layer technique is necessary. It differs from the one described for the preparation of HIB-JJs in that the two layers are insulated from each other. A typically sequence of deposition/structuring would be:

(1) First deposit a 400 nm base YBCO layer.
(2) Structure the base layer for the base wiring or alternatively keep it as a ground plane.
(3) Deposit an epitaxial insulating oxide layer on top.
(4) Structure windows into the insulating layer where contacts between the base layer and the top layer are needed. The windows need to have angled side (about 25 deg) and a typical size of the window sides is 3 µm to 10 µm at the base. Etching about 200 nm deep into the base HTS layer is needed for a high critical current density contact.
(5) Deposit the second HTS layer on top. A typical thickness is 150 nm.
(6) Structure the top HTS layer for wiring.

The resulting structure is depicted in Fig. 3.

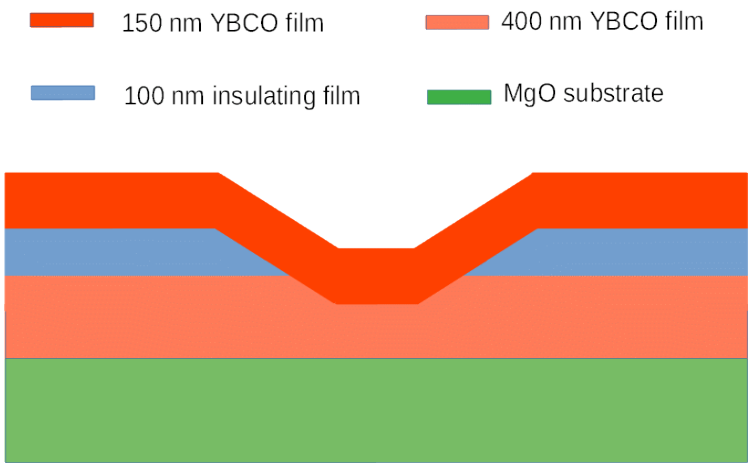

Figure 3 : Schematic cross-section through HTS via section

The angled approach has the advantage that the contact between upper and lower base works like a ramp-type junction without barrier – it is a contact with a current density typically in the range of 100 kA/cm^2 at 77K. If one intends to use HIB-JJs, the 40 nm HTS layer deposition follows the last step (6) of the deposition sequence with subsequent structuring and writing of the HIB-JJs. This would be already a 3-layer technique, in which all layers, including the insulating layer, have to be grown epitaxial on each other.

Principle Layout of an RSQ shift register and Josephson Transmission Line (JTL)

Assuming being limited to the 2 layer process for the HIB-JJs (thus no vias), the layout options become very limited. Nevertheless, it is possible if one uses normal conducting clock lines. Fig 4 shows a basic RSQ-cell for a shift register [3].

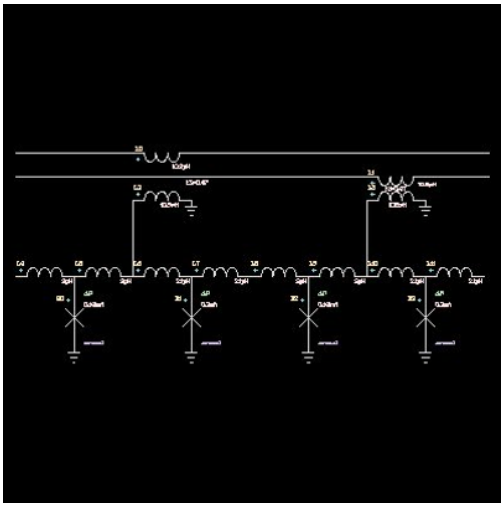

Figure 4 : Basic RSQ-cell for a shift register.

Using the above described 2-layer technique for the HIB-JJ preparation and a normal conducting (Au) layer on an insulator, a symmetric and an asymmetric design of the RSQ shift register is possible. These designs have been simulated for 77 K and 65 K operation.

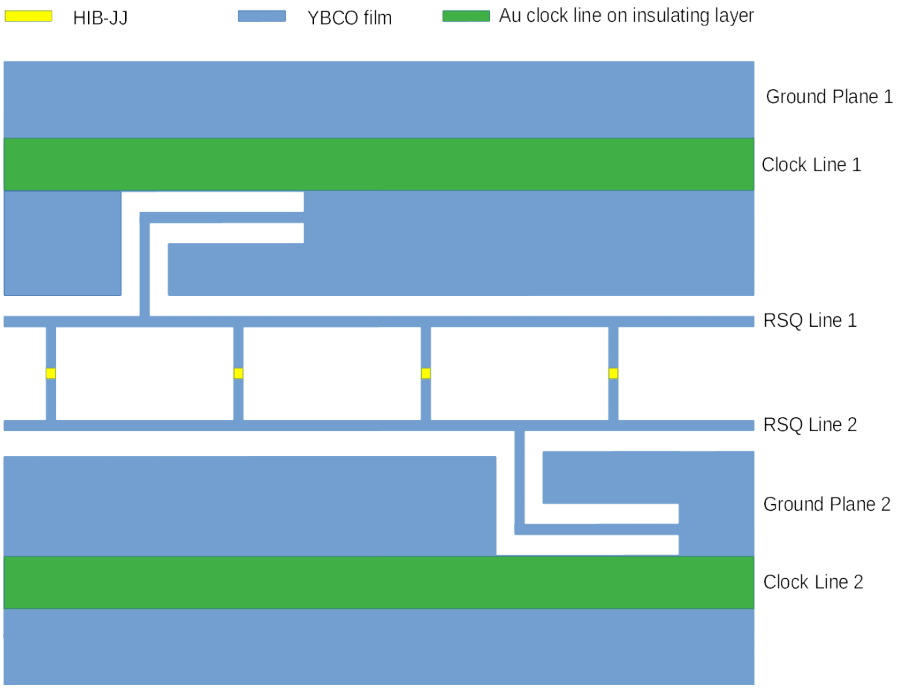

Figure 5 : symmetric design of an RSQ shift register.

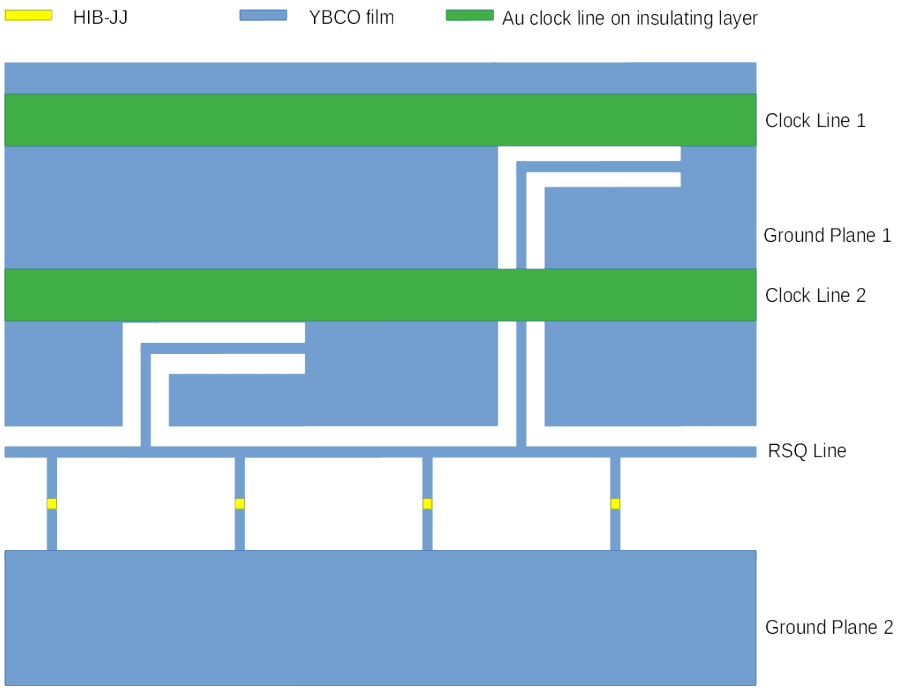

Figure 6 : Asymmetric design of an RSQ shift register cell.

Additional normal conducting connections between the two ground planes have been left out for clarity. In a similar way, an asymmetric Josephson transmission line has been designed and simulated (see Fig. 7).

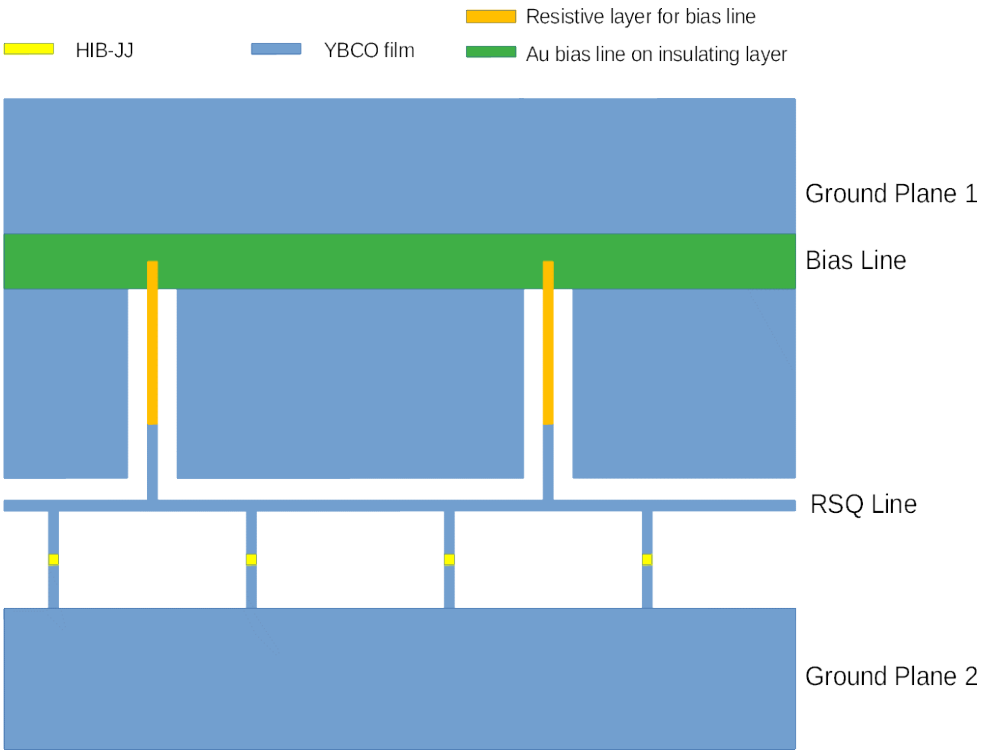

Figure 7 : Asymmetric design of a Josephson Transmission Line (JTL).

Other circuits, like a dc-to-SFQ- and a SFQ-to-dc-converter can be designed in a similar way.

HTS Digital-to-Analog Converter (DAC)

The work on the pulse-drive HTS Josephson Quantum Voltage DAC [4] at NIST continued using grain-boundary junctions [5] on an MgO bi-crystal, since a HIB-JJ device was not yet available. The test chip contains individual junctions and series arrays of 2 and 3 junctions (see Fig. 8), in part connected to the pads via coplanar waveguides, that allow to apply microwave signals to the connected junctions.

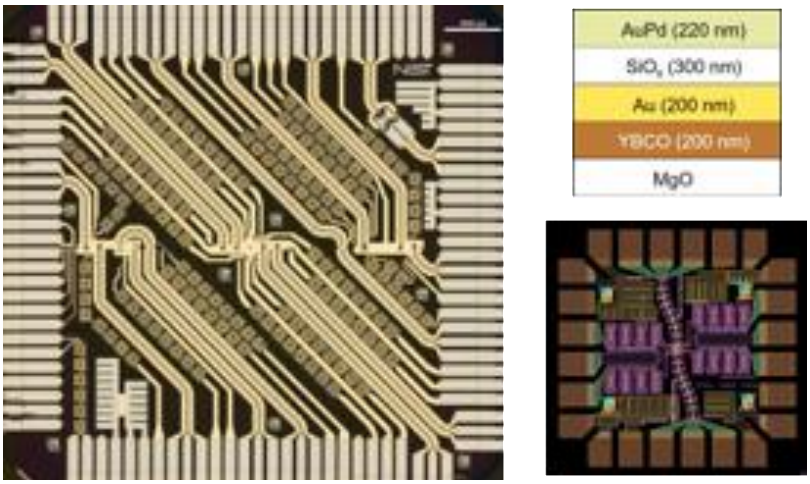

Figure 8 : (a) Microscope image of a recent 10 mm chip for testing of microwave-driven arrays of YBCO grain-boundary junctions. Junctions are located on the MgO substrate's 24˚ grain boundary line. (b) Design of a quantum voltage circuit based on HIB-JJs..

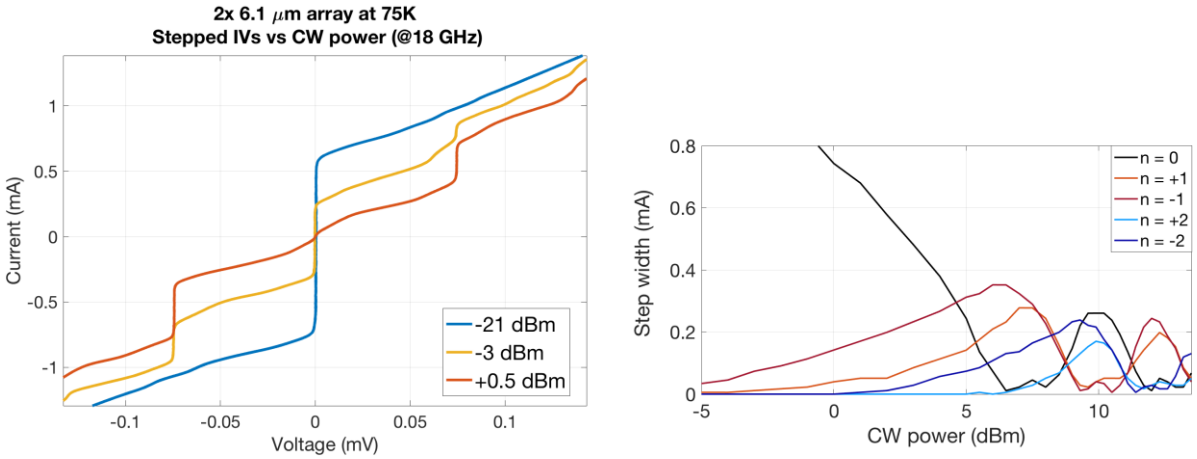

*Figure 9 : (a) Shapiro steps observed in a two-junction array of 6.1 μm-wide grain-boundary junctions at 75 K. Drive frequency was 18 GHz and drive powers are shown in the legend. Two-junction votlage steps are observed at the expected 2*hf/2e = 74.5 μV, with widths up to approximately 400 μA. (b) As a function of microwave power, the width of Shapiro steps modulates according to the usual Bessel function behavior, albeit with some asymmetry between equivalent steps at positive and negative dc currents.*

The measurements show, that these devices can be used for quantum voltage sources. Hopefully, a circuit based on HIB-JJs will become available soon.

Conclusion

Based on the calculations and simulations of digital SFQ and RSQ circuits, which included the kinetic inductance of the circuit, show that a 1-layer technique with HIB-JJs would not work at elevated temperatures. Instead, a 2-layer technique allows to significantly reduce the influence of the kinetic inductance and a 3-layer technique would even allow superconducting wiring with vias. Since the latter is not available, the design proceeded with the 2-layer technique. Combining this 2-layer technique with an additional insulated normal conducting layer (e.g. Au-layer) allows for the design of RQL and SFQ circuits. These circuits have been simulated and will be combine into a test circuit consisting of a dc-to-SFQ converter, followed by a JTL, a 2 stage shift register, another JTL and a SFQ-to dc converter.

In the intermediate step for the development of a Josephson Quantum Voltage DAC, we used HTS grain boundary junctions and were able to show that the design of these circuits was successful: double-voltage Shapiro steps at 18 GHz have been measured at a device temperature of 75 K.

The Quantum Voltage Project is primarily a NIST project that uses some results from the AFOSR project and vice versa to the benefit of both projects.

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