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Flexible Sensor Network and Its Embedded Integrated Circuits for Structural Health Monitoring

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14. ABSTRACT

Structural Health Monitoring (SHM) is a novel technology that can be used to perform on-line health monitoring of any type of structures (Metal or composite) with minimal human involvement and at reduced cost compared to traditional non-destructive inspection (NDI) methods. SHM involves the use of NDI principles coupled with in situ sensing to allow for rapid, remote, and real-time condition assessments. The sensors record certain signatures, within deviations from such signatures may indicate a mechanical issue that needs to be addressed. Alternately, the sensors may deterministically detect a flaw, thus indicating the type of damage and location for further assessment. Such a system can be used to conduct nondestructive inspections for areas of the structural platform which have been traditionally difficult to access. SHM systems may either be used to supplement normally scheduled inspections or provide continued monitoring of a given structure. The goal is to reduce operational costs and increase lifetime of structures by:
- Continuously monitoring critical areas
- Overcome accessibility limitations, complex geometrics, depth of hidden damage
- Eliminate costly and potentially damaging disassembly
- Minimize human factors using automated data analysis
- Move towards Condition Based Maintenance (CBM) for the structure, as opposed to scheduled maintenance.

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Flexible Sensor Network and its Embedded Integrated Circuits for Structural Health Monitoring

Contract #FA9550-18-C-0009

Ninth Report
Phase II

January 18, 2021

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1. Background

Structural Health Monitoring (SHM) is a novel technology that can be used to perform on-line health monitoring of any type of structures (metal or composite) with minimal human involvement and at reduced cost compared to traditional non-destructive inspection (NDI) methods. SHM involves the use of NDI principles coupled with *in situ* sensing to allow for rapid, remote, and real-time condition assessments. The sensors record certain signatures, wherein deviations from such signatures may indicate a mechanical issue that needs to be addressed. Alternately, the sensors may deterministically detect a flaw, thus indicating the type of damage and location for further assessment. Such a system can be used to conduct nondestructive inspections for areas of the structural platform which have been traditionally difficult to access. SHM systems may either be used to supplement normally scheduled inspections or provide continued monitoring of a given structure. The goal is to reduce operational costs and increase lifetime of structures by:

- Continuously monitoring critical areas
- Overcome accessibility limitations, complex geometries, depth of hidden damage
- Eliminate costly and potentially damaging disassembly
- Minimize human factors using automated data analysis
- Move towards Condition Based Maintenance (CBM) for the structure, as opposed to scheduled maintenance.

Over the past decade, several sensing solutions have been developed for SHM. Sensors including strain gages, fiber-optic gages, piezoelectric transducers, MEMS, etc. are all being used for SHM. Acellent Technologies has developed an SHM system that utilizes a network of distributed sensors and actuators embedded on a thin dielectric carrier film called the SMART Layer to query, monitor, and evaluate the condition of a structure. A portable diagnostic hardware unit processes signals obtained from the sensors bonded to the structure. With appropriate diagnostic software, the signals can be analyzed to ascertain the integrity of the structure being monitored. The SMART Layer technology has both active and passive sensing capabilities using piezoelectric sensors (PZT). Other types of sensors such as temperature, strain gauges, and fiber optics can also be added into the SMART Layer network to provide additional sensing functions. In the “active” sensing mode, the diagnostic hardware automatically instructs actuators to generate pre-selected diagnostic signals and transmits them to neighboring sensors whose response can then be interpreted in terms of damage location and size or material property changes within the structure. In the “passive” sensing mode, the SMART Layer sensor network is continuously monitored to “listen” for any impact events. Both modes permit real-time structural analysis and evaluation along with constant collection of structural data and information while the structure is in service. Acellent has developed SHM systems to monitor several different applications in a number of industries.

Current SHM systems (comprised of sensors, hardware, and software) can perform the required functions, but they are heavy, bulky, and difficult to integrate with the structure to provide on-board real-time structural integrity assessment. Structural integrity monitoring is a critical safety factor for a wide variety of aerospace assets to prevent accidents due to structural fatigue and impact damage. Use of newer, lightweight materials such as composites introduces new failure mechanisms such as delamination that require additional vigilance with respect to structural integrity. Embedding the currently available sensors and electronics used by these systems into composite structures can be a challenge. Novel SHM capabilities are therefore necessary to meet the challenges of future autonomous aircraft that are planned to be used by the Department of Defense in combat and surveillance/reconnaissance missions.

Flexible hybrid electronics (FHEs) based on application-specific integrated circuits (ASICs) can conformably distribute sensors, actuators, and electronics over very large aircraft components, enable availability of instantaneous information on the structural integrity of the vehicle, and measure environmental conditions for optimum performance while adding minimal weight.

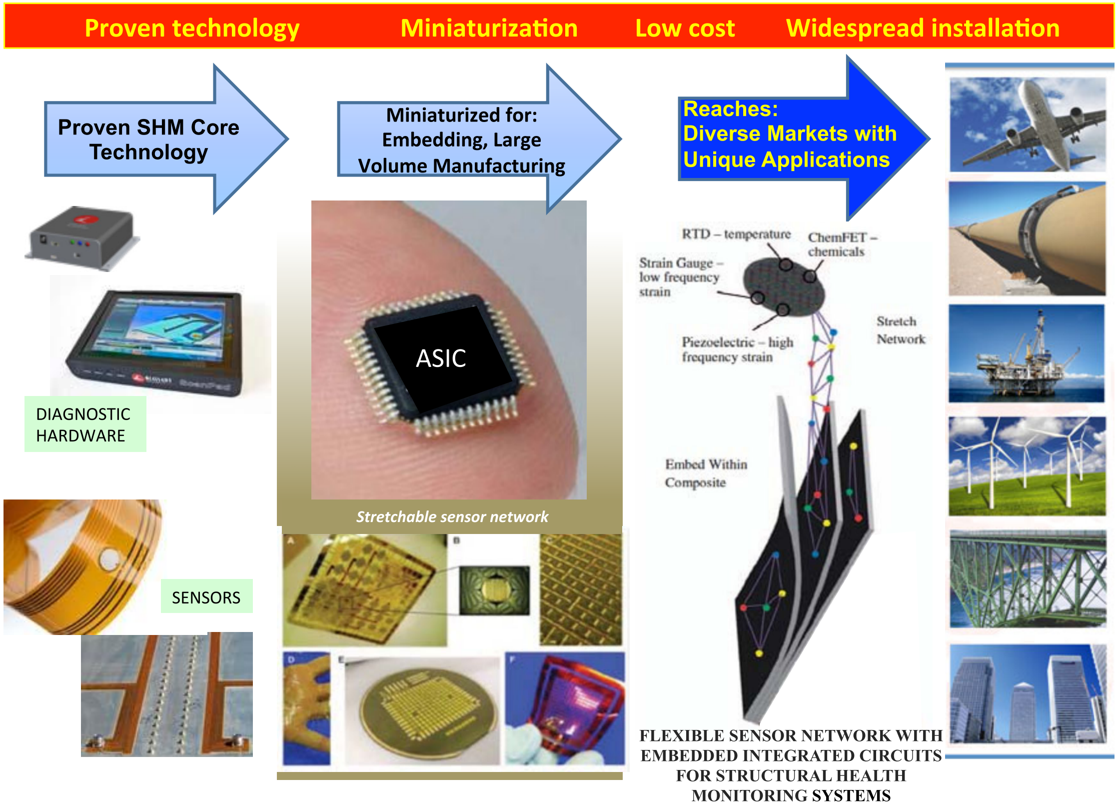


Figure 1: Schematic of proposed innovation

Acellent Technologies, Inc. has proposed to develop an SHM system using a flexible stretchable sensor network along with embedded integrated circuits that will serve as a platform to all types of sensors including strain gauges, piezoelectric sensors, etc. The proposed program, shown in Figure 1, will utilize previous work done at Acellent Technologies, Inc. and Stanford University as a basis for the development. Ongoing and completed work at Stanford focused on developing sensor networks with miniaturized sensors, which, along with Acellent's current SHM systems, will be used as a basis for this effort. Our proposed effort addresses the challenges remaining regarding development of ASIC electronics, robustness, integration, and manufacturability of stretching/folding substrates, micro-wire sharing, mechanical optimization, electronics integration, sensor signal addressing, and algorithm development.

The goal will be to enable large-scale manufacturing of robust and reliable flexible stretchable multi-modal micro-sensor networks that can be integrated with flexible substrates for SHM.

2. Proposed Work

Phase I focused on performing proof-of-concept analysis and experiments to demonstrate the feasibility of a highly expandable, lightweight, and flexible sensor network and its embeddable application-specific integrated circuit (ASIC). The Phase I work of this project focused on the development of a working board-level prototype of the future ASIC built using discrete components and interfaced with the flexible stretchable sensor network. Since a lot of effort has gone into development of the flexible stretchable sensor network by both Acellent and Stanford, the major focus in Phase I was on the development of the ASIC electronics. Feasibility in Phase I was demonstrated using Acellent's current flexible sensor networks and a prototype board-level design developed in this program. During the development of the proposed ASIC circuitry, Acellent and Stanford ensured that all the required challenges were overcome to ensure the successful development of a compact system.

The technical approach for the analog sub-system for the ASIC had two main elements:

1. Breadboarding to study system integration and inform ASIC translation.
2. Study of advanced signal conditioning/equalization algorithms that will help reduce the transmitter voltage requirements.

The concept of discrete PCB breadboarding is a widespread approach taken by industrial players to mitigate the risks in ASIC development. Acellent leveraged Phase I to emulate the complete target system using discrete components. This will help solidify the system specifications and prevent systematic design problems before undertaking a costly mask design for a CMOS ASIC in Phase II.

In addition, Acellent and Stanford investigated advanced techniques that can help reduce the transmit voltage requirements in the system. For example, a reduction to less than 10 V would mean that the ASIC can be realized with significantly lower-cost technology and higher power efficiency. The drawback to reduced transmit voltage is that the amplitude of the received waveform will be proportionally smaller and thus more difficult to collect and extract information from. An analogy for this can be found in the world of sound. Currently, the system is analogous to person talking over a loud speaker to ensure everyone can understand them. This, unfortunately, requires high voltage to provide the amplification, which is a complex problem to address on the ASIC. A better solution is to improve everyone's hearing. In this case, less amplification is required, lowering voltage and simplifying circuit design; however, the transmitted signals are more susceptible to being drowned out by noise (poor signal-to-noise ratio). Fortunately, a similar problem is found in the world of wireless signal transmission where significant advances have been made in improving signal-to-noise ratios utilizing improvements on existing filtering techniques such as finite impulse response (FIR). By studying these techniques and applying them to the problem of wave propagation in a plate, the team believes it will be possible to significantly reduce the output voltage, thus simplifying ASIC design and increasing power efficiency.

Based on this, the specific objectives of the Phase I work that were accomplished include the following:

- **A. Define a system architecture for the ASIC interfaced with the flexible sensor network**
- **B. ASIC development with focus on Analog and Digital circuits**
- **C. System integration, testing and demonstration**

For reference, the Phase I work plan is given in Table 1 below.

Table 1: Phase I Work Plan

Project Task	Month									Milestones
	1	2	3	4	5	6	7	8	9	*(Gold Stars Denote Milestones)*
Task 1: Project Kickoff	★									Kick-off meeting, revisions to project plan
Task 2: Define SHM System Architecture	🟥★									SHM architecture for team identified
Task 3: Analog System Development	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	Analog circuit development
Task 3.1: Development of Data Acquisition Circuitry	🟥	🟥	🟥	🟥						
Task 3.2: Integration of Analog Systems				🟦	🟦	🟦★				Analog circuit completion
Task 3.3: Study on Signal Conditioning and Digital Post-processing					🟥	🟥	🟥	🟥	🟥	
Task 3.4: Flexible sensor layer Interface Design						🟦	🟦			
Task 4: Digital System Development	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥		Digital circuit development
Task 4.1: Digital Control System	🟦	🟦	🟦★							Completion of Digital Controller
Task 4.2: Control and Communication			🟥	🟥	🟥★					Completion of Communication System
Task 4.3: Power Management				🟦	🟦	🟦				
Task 5: Electronics Integration						🟥	🟥	🟥★		Completion of Preliminary Prototype
Task 6: Sensor fabrication										Prototype flexible sensor layers fabricated
Task 7: Development of Interface Software					🟦	🟦	🟦	🟦		Interface software developed
Task 8: Feasibility Testing							🟥	🟥	🟥★	Feasibility testing on test-bed, Prototype Validated
Task 9: Reports and Deliverables	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	Progress reports

Phase I Summary of Achievements

The goal of this STTR program is to develop a highly expandable, lightweight, and flexible sensor network and its embeddable application-specific integrated circuit (ASIC). Previous work has already demonstrated a flexible sensor network; therefore, the current focus is on demonstrating capabilities to design and fabricate the ASIC, and then test the systems. The Phase I goal was to perform proof-of-concept analysis and experiments that demonstrate the feasibility of the flexible sensor network and its embeddable ASIC for usage with large composite or metal structures.

At this stage in the project, Acellent and Stanford have successfully completed the architecture and design portion of the ASIC work. The physical design of the 8-channel Phase I prototype system has been completed. The system was based on a Texas Instruments AFE5803 ultrasonic analog front-end and was designed to interface with a Xilinx KC705 FPGA. The system was designed for high tunability to enable easy design space exploration for Phase II, and the highly-parallel 8-channel configuration enabled faster data acquisition when compared to Acellent's existing multiplexer-based designs. A breakdown of this 8-channel prototype system development and its status can be seen in Figure 2.

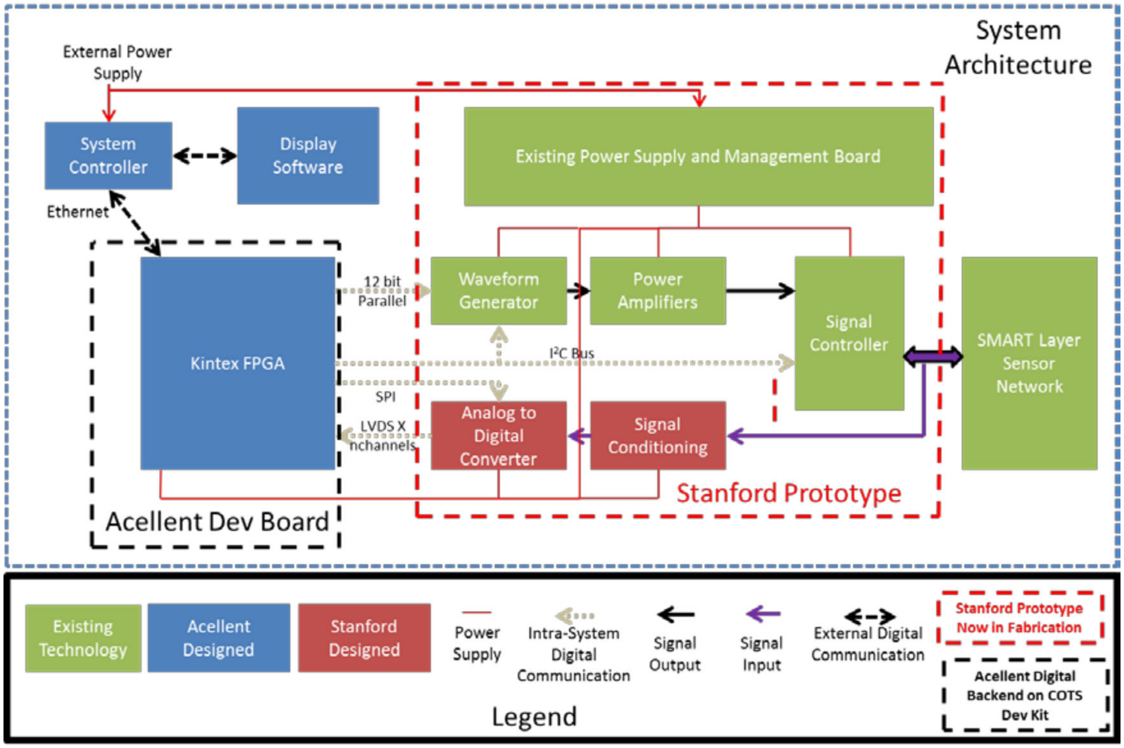


Figure 2: Block diagram for 8-channel hardware prototype

The ASIC hardware prototype is currently in the fabrication and testing stages. The fabrication will occur in two portions:

1. Fabricating a prototype of the analog system, including all components and power circuitry.
2. Developing the digital back-end for the system using the FPGA and Ethernet interfaces.

Both portions are in the development stage and will be combined in the upcoming period of the project, then tested with the flexible sensor network integrated on a composite or metal structure. The work by Acellent and Stanford in this project will culminate in development of a system that has improved functionality over the existing ultrasonic interrogation system while reducing the number of discrete components in the system. Furthermore, Acellent and Stanford are able to demonstrate that the future system can be miniaturized and even reduced to an ASIC design by leveraging existing IC technology to replace many of the current discrete components, minimizing the future design risk. This proof-of-concept approach reduces the risk and costs of developing a completely integrated embedded flexible sensor network technology.

3. Proposed Work

The overall goal of the proposed Phase I and Phase II effort is to develop and implement an SHM system consisting of a flexible sensor network with embedded ICs. The goal will be to turn this concept into a commercially viable product that will be available for widespread trial and adaptation within 30 months of the project. The new proposed technology will have the following benefits:

- Increased safety, minimal structural downtime
- Reduced life-cycle costs
- Increased productivity due to reduced downtime and reduced inspection time.

Phase II will refine the design concepts for application with composite structures used in the aerospace industry, as well as other critical structures. A manufacturing plan for fabricating expandable structures with integrated SHM systems, along with a framework and plan for integrating SHM data into the structural design process will be developed during Phase II to enable potentially significant reductions in structural weight. The Phase II deliverables will include a prototype of the flexible sensor network and its embeddable ASIC along with the required hardware and software. The feasibility of autonomous health monitoring in a simulated operational environment will be determined and methodologies for integration into actual aircraft will be developed.

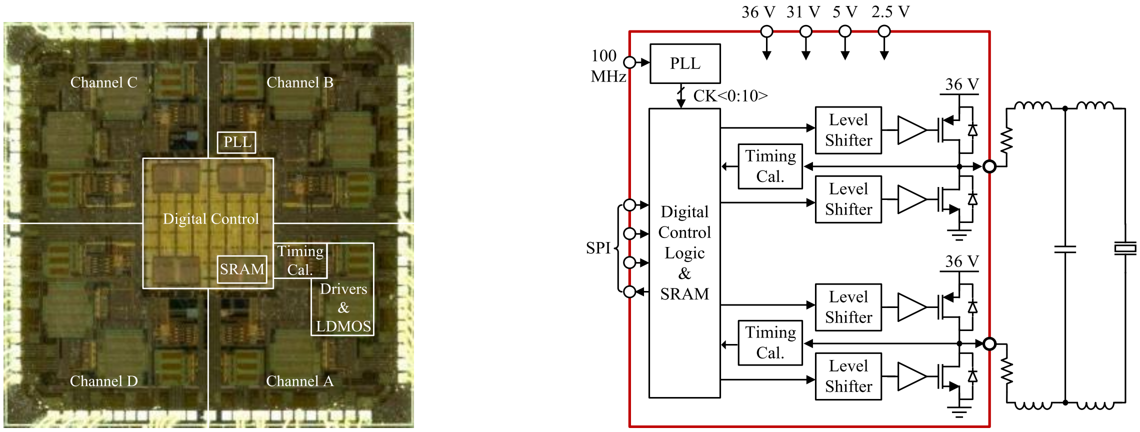
In Phase II, the project goal is to design, fabricate, and test a prototype flexible sensor network and its embeddable interface electronics as well as their accompanying software. At the end of the project, tests shall be conducted on the prototype system in a simulated operational environment to demonstrate the feasibility of autonomous health monitoring as well as to validate system performance. Another key outcome of the project will be the development of baseline methodologies for integration into an actual aircraft.

Stanford will be primarily responsible for the development of the analog and mixed-signal interface electronics required by the prototype. In doing so, the team at Stanford aims to leverage results from work that they have already done towards developing a custom ASIC for state-sensing applications. In particular, in 2014, Stanford, in collaboration with Acellent, demonstrated a four-channel, ±36 V, 780 kHz PZT-driver IC for driving the PZT wafer transducers used in SHM applications. Furthermore, in Phase I of the STTR, Stanford and Acellent specified and developed a 32-channel PCB-based state sensing system that couples Acellent's current actuation electronics with the receive capabilities of the Texas Instruments AFE5803 ultrasonic analog front-end to achieve highly parallel data-acquisition capabilities.

Going forward, the targets for the interface electronics are the following:

- First, the results that will be gathered from a series of experiments during the testing phase of the 32-channel PCB-based system will be used to define the specifications for the integrated receive electronics of the Phase II prototype. These specifications shall then guide the implementation of a receiver front-end that is optimized for state-sensing purposes. Key specifications to be defined include front-end architecture, amplifier gains, filter cut-off frequencies, analog-to-digital converter resolution, sampling frequency, and the required digital signal processing blocks.

- Second, reducing the form factor of the electronics to a degree that is compatible with integration in a sensor network mounted on an aircraft requires both the actuation and receive electronics to be integrated. Although an integrated PZT-driver IC, shown in Figure 3, has already been demonstrated, the large amount of burst power that it needs to deliver necessitates the use of high voltage (±36V and ±31V voltage rails). The presence of such high driving voltages results in large chip areas, high power system complexity, high fabrication costs, and limited channel count. However, the current PZT-driver IC is a significant step-up from previous PCB-based approaches for actuation. Therefore, starting with an implementation that leverages the current integrated PZT-driver IC, the aim is to reduce the footprint of the transmit electronics.



(a) (b)

Figure 3: Existing 4-channel PZT-driver ASIC: (a) Die Photo (b) Block Diagram

- Third, as outlined in the Phase I proposal, an avenue towards further reducing the footprint of the PZT-driver IC is the use of pulse compression together with dispersion compensation. This would enable the use of lower voltage actuation waveforms (e.g., ±5 V rather than ±36 V), thereby greatly simplifying the power supply requirements of the chip as well as allowing the use of more mainstream process technologies which have lower fabrication costs. Exploration of these pulse compression and dispersion compensation techniques is ongoing and if the results of the analyses are promising, incorporating these techniques into the design of both transmit and receive interface ICs will be a huge focus of Phase II.

- Finally, to ensure the successful integration of the interface electronics with the rest of the prototype system, Stanford's Mixed-Signal Group shall work closely with Acellent and Professor Fu-Kuo Chang's Structures and Composites Laboratory (SACL) to complete the following system integration tasks:

  1. The first integration task will be the redesign of the system's power supply and distribution network. Key areas of focus in the redesign will be area reduction, reducing interference with the signal path, and eliminating superfluous high voltage supplies. As discussed previously, the goal of reducing the power supply's area footprint will be greatly aided by the successful implementation of a low-voltage actuation scheme. As shown in Figure 4, another pathway to achieving lower area will be the use of very high frequency, soft-switched power converters with air cores. Stanford University's Power Electronics Research Laboratory is doing extensive

work in this area and we plan to consult with them to incorporate such converters in the redesign. Having an end-to-end view of the system's design will also allow employment of techniques to limit power supply interference in the signal path as well as to identify alternatives for parts requiring high supply voltages such as the current analog multiplexers.

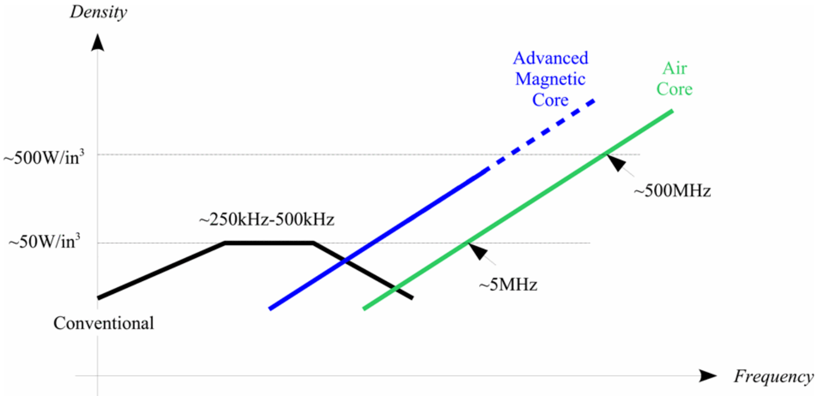


Figure 4: Plots showing the improvement in power density with frequency for DC-DC switching power converters

2. Integration of the interface ICs with the digital control and processing electronics will also be critical to the successful delivery of the prototype system. Following Acellent's leadership, Stanford will provide the documentation and other inputs necessary for developing the software and hardware required to integrate the transmit and receive electronics within the overall system prototype. Furthermore, the flexible sensor network within which the electronics are going to be embedded shall be developed by the SACL, and Stanford shall work closely with both the SACL and Acellent to integrate this sensor network and the prototype's interface electronics.

3. Finally, the prototype's reliability and robustness are critical factors given the future vision of integrating state sensing systems on in-service aircraft. Therefore, with Acellent's guidance, Stanford shall select components and employ design techniques to maximize system reliability and robustness over the course of this project.

Specific objectives for the Phase II are therefore to:

- ✓ Design the final flexible sensor system with embeddable ICs
- ✓ Develop a prototype of the system
- ✓ Perform the testing to validate the developed system and prove the survivability in operational environments
- ✓ Integrate the final deployable system with sample aircraft structures
- ✓ Collaborate with industrial partners for beta testing of the system (As indicated in the attached letter of support, Boeing is very interested in the proposed technology and has agreed to help with any testing and commercialization efforts.)
- ✓ Develop a user's manual and training guide for the proposed system
- ✓ Develop commercialization plan for Phase III implementation and usage.

The availability of test articles for actual trials to collect *real-time* test data is critical in ensuring a reliable and robust system. The partnership with Boeing will undoubtedly help ensure this.

3. Phase II Project Status

Scope: Phase II work will focus on developing and testing a complete system prototype and demonstrating its capabilities in operational environments.

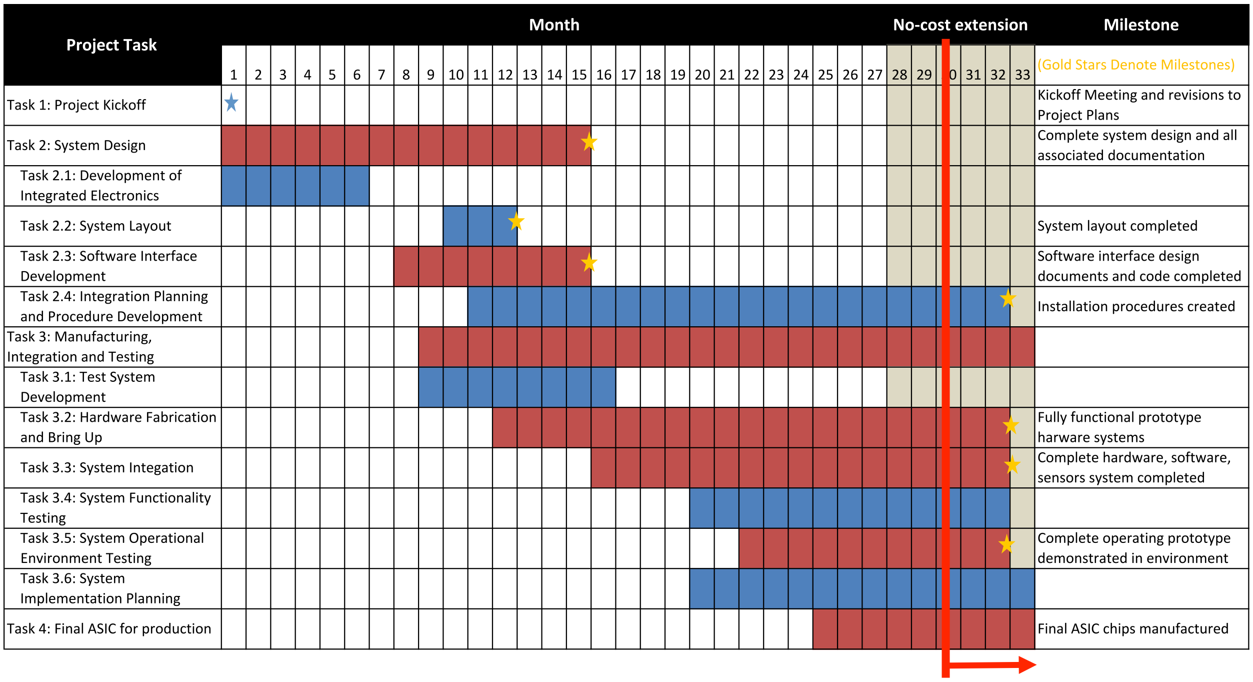
Goal: The motivating goal of the research work conducted during Phase II of this project is to develop a working prototype integrated circuit design that represents a significant miniaturization and weight reduction compared to existing ultrasonic guided-wave SHM systems like Acellent's ScanGenie line of diagnostic hardware. Once design and development of this prototype has been completed, the complete prototype system will be tested in both laboratory and real-world operational environments and assessed on its ability to accurately perform damage detection, localization, and quantification on a variety of structural materials.

Key tasks and timeline for Phase II are provided in Table 2.

No cost extension: Due to the COVID-19 situation, a no-cost extension for the program has been requested to extend the duration till April 2021.

The revised timeline and tasks are given below.

Table 2: Phase II Task and Milestone Schedule



Project Task	Month																											No-cost extension						Milestone
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	0	31	32	33	(Gold Stars Denote Milestones)
Task 1: Project Kickoff	★																																	Kickoff Meeting and revisions to Project Plans
Task 2: System Design	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥 ★																			Complete system design and all associated documentation
Task 2.1: Development of Integrated Electronics	🟦	🟦	🟦	🟦	🟦	🟦																												
Task 2.2: System Layout										🟦	🟦	🟦 ★																						System layout completed
Task 2.3: Software Interface Development								🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥 ★																			Software interface design documents and code completed
Task 2.4: Integration Planning and Procedure Development											🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦 ★		Installation procedures created
Task 3: Manufacturing, Integration and Testing									🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	
Task 3.1: Test System Development									🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦																		
Task 3.2: Hardware Fabrication and Bring Up												🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥 ★		Fully functional prototype harware systems
Task 3.3: System Integration																🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥 ★		Complete hardware, software, sensors system completed
Task 3.4: System Functionality Testing																				🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦		
Task 3.5: System Operational Environment Testing																						🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥 ★		Complete operating prototype demonstrated in environment
Task 3.6: System Implementation Planning																				🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	
Task 4: Final ASIC for production																									🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	Final ASIC chips manufactured

Tasks: Prior to the kick-off of Phase II, the goal was broken down into the following tasks:

1. Redesign of waveform generator and amplification circuitry for weight reduction and miniaturization.
2. Experiment with reduction of waveform peak-to-peak output voltage while maintaining current signal-to-noise ratio.

3. Work on power supply and distribution redesign.
4. Work on design integration.
5. System component selection for reliability and robustness (15-20 year lifespan, meeting applicable military specifications).
6. Integration of electronics with stretchable layer.

Section 3.1 will summarize the research and design work completed during this reporting period, explaining the conclusions in light of the overall project schedule. Section 3.1.1 – Section 3.1.4 will present and discuss the details of research, simulations, and experiments that were conducted during this reporting period in order to address critical design challenges. Finally, Section 3.1.5 – Section 3.1.6 will describe the next steps and lay out a roadmap for the rest of the project.

3.1 Summary of Phase II Project Status

This section summarizes the work that has been done on this project so far.

1. STTR Phase I System Software Development and Testing (October 2018 – March 2019)

At the beginning of Phase II the physical design of the 8-channel Phase I prototype system was complete, but the system was yet to be tested. To recap, the Phase I system was based on a Texas Instruments AFE5803 ultrasonic analog front-end and was designed to interface with a Xilinx KC705 FPGA. The system was designed for high tunability to enable easy design space exploration for Phase II and the 8-channel configuration enabled faster data acquisition when compared to the existing multiplexer-based designs. To wrap up this phase of the project, the firmware and software necessary to test the system were developed in tandem with Phase II activity. The prototype system successfully actuated, recorded, processed and digitized diagnostic signals which were subsequently used to successfully localize defects. This prototype system also served as the foundation of a system developed at Acellent.

2. STTR Phase II Activity

Listed below is the work that has been accomplished in Phase II thus far. The comments below summarize work which was described in more detail in previous reports.

i. Assessment of candidate low-voltage actuation techniques (Jun. 2018 - Sept. 2018)

As outlined in the statement of work, the key design challenge for Phase II of the project is to lower the voltage at which the piezo-electric transducers that are used for SHM are actuated to enable system miniaturization and weigh reduction. The actuation voltage must be lowered while maintaining a high enough signal-to-noise ratio (SNR) to enable accurate defect detection and localization. For a fixed noise floor, just reducing the actuation voltage while maintaining the same tone-burst waveform actuation and recording scheme does not achieve this goal because signal power is proportional to the square of the voltage amplitude. As such, the SNR penalty for reducing the actuation voltage would be too high and the resulting degradation in signal quality would render recorded waveforms useless for defect localization and detection.

To get around this amplitude voltage and SNR trade-off, we did some analysis and ran simulations to assess two signal processing techniques that exploit longer actuation times to improve signal to noise ratio. The first technique is pulse-compression, a technique that uses chirp actuation signals and matched filtering to improve SNR while lowering actuation voltages. The second technique is accurately measuring the frequency spectrum of the paths between pairs of PZT transducers through the structure under test using a vector network analyzer (VNA) like system. This improves the SNR through the averaging effect and allows for a more favorable trade-off between the actuation voltage and the amount of time taken to measure the frequency spectrum. Time domain waveforms for use in detection and localization algorithms can then be obtained from the frequency spectra using the Inverse Fast Fourier Transform (IFFT).

Pulse compression was limited by its reliance on dispersion compensation algorithms which are still maturing and its applicability to pulse-echo SHM only. Therefore, at the conclusion of our assessment, we chose the frequency domain-based technique and decided to work on a SHM VNA-on-a-chip system instead of pulse compression.

ii. Conceptual development and design of a VNA-on-a-chip system (Sept. 2018 - May. 2019)

In light of the choice to pursue a frequency-domain-based S-parameter measurement approach to lower actuation voltages, tasks 1 and 2 changed from the redesign of the waveform generator and experimentation with the generator's peak-to-peak output voltage. Instead, they became the conceptual development and design of a system that can make S-parameter measurements for ultrasonic guided-wave SHM.

The conceptual development portion of this effort involved extensive experimental work that showed successful detection and localization of defects in aluminum and honeycomb carbon-fiber reinforced plastic (CFRP) coupons using very low actuation voltages in a wide variety of conditions. This work culminated in a paper *"Towards On-Chip Measurement of S-Parameters for Ultrasonic Guided-Wave SHM: Damage Localization in Aluminum Using S-Parameter Measurements"* that was published and presented at the 12th International Workshop on Structural Health Monitoring. This publication only covered the work done on the aluminum coupon because experiments in CFRP were still ongoing at the time of abstract submission. The architectural design of the VNA-on-a-chip system was done alongside the experimental work discussed above.

iii. Calibration Experiments – Improving Effective Directivity and Compensating for Errors (Oct. 2019 - Dec. 2019)

During the architectural design process, directional coupler design emerged as one of the major design challenges due to the 10 kHz to 5 MHz target frequency range and the directivity degrading effect of the frequency-dependent impedance of the PZT transducers. Commercial VNA systems compensate for directivity and other measurement non-idealities using calibration procedures based on standardized loads. To confirm that we could yield similar improvements in effective directivity and other measurement non-idealities in our system, we prototyped a PCB-level one-port VNA (reflectometer) with similar specifications as our proposed system and ran some calibration experiments on it.

As the results presented in our December 2019 report showed, calibration was successfully carried out in this system and reflection coefficient measurements that were made using it closely matched those of the benchtop VNA. The measurements that were compared were made on both the standard loads and PZT transducers. These results gave us confidence that once we have developed integrated directional couplers and the VNA-on-a-chip system, we would be able to use standard calibration protocols to increase effective directivity and compensate for other measurement non-idealities.

iv. Signal-to-Noise Ratio Quantification Experiments (Oct. 2019 - Dec. 2019)

These experiments were carried out to quantify the signal-to-noise ratio (SNR) of the proposed VNA-on-a-chip system. This was a key step in the design process because there is a significant reduction in actuation voltage in the proposed system and it is important to ensure that the necessary SNR performance to successfully detect and localize defects is maintained at these lower actuation voltages. Furthermore, quantifying performance enabled the identification of key design knobs and provided a basis for the comparison of the proposed system to existing systems. Through consultation with Acellent engineers, we established that the ScanGenie time-domain based systems that Acellent produces were designed with a receiver SNR spec of 60 dB. Therefore, this was the target SNR specification that we set to achieve in the experiments that we conducted.

The experiments were run using a prototype VNA system consisting of a function generator and high-precision 4-channel oscilloscope. The results showed that the target SNR value can be met and exceeded in our proposed system. Furthermore, they revealed that the design of the intermediate frequency (IF) digital filter is a key factor influencing the SNR performance. The detailed procedure and results of these experiments were presented in the December 2019 report.

v. Aerospace Journal manuscript preparation and publication (January 2020 to March 2020)

Our IWSHM conference paper was invited to an IWSHM 2019 Special Issue of the Aerospace Journal. We dedicated most of the first quarter of the year to performing additional experiments and preparing this manuscript which was published on 20 March 2019. In this paper we showed the success of the S-parameter method in an anisotropic high-density carbon-fiber reinforced polymer (CFRP) test structure in addition to the previous results from an aluminum test structure that we presented at IWSHM last September. The paper also provides some comprehensive background on how VNAs work and why the method achieves good quality results using very low actuation voltages. The paper goes into more detail on how the new test structure was prepared, how the new measurements were taken and processed, and the additional insights that the new results reveal.

vi. Addressing outstanding VNA-on-a-chip design challenges (January 2020 to March 2020)

In the first quarter, we also invested some time into coming up with solutions to design challenges that needed to be addressed before proceeding with the design of an VNA-based SHM system. One such challenge was finding a directional coupler design that was compatible with CMOS implementation at the low frequencies that we operate at. To address this challenge, we selected the integrated directional bridge technology that was patented by Keysight Technologies in 2006 (US Patent No. US 7,309,994 B2). We also explored the use of matching networks to minimize reflection losses at the interface of the measurement ports and the PZT transducers. Finally, we extended the work on VNA calibration and system SNR quantification that was started in late 2019.

vii. *Introduction of an OFDM-based transfer function measuring method to address VNA-on-chip challenges (March 2020 to September 2020)*

In this reporting period, we spent much of our effort pursuing alternative methods to measure the transducer-to-transducer transfer functions through the structure. This was a consequence of the advent of the COVID-19 pandemic in March that impacted our implementation plans for the VNA-on-a-chip as initially projected. As part of these efforts, measuring the transfer functions using an orthogonal frequency division multiplexing (OFDM) approach like the one used in multi-carrier communication systems yielded very promising results. Firstly, it led to a drastic reduction in measurement times from the 85 second per transfer function time scale that was used in the VNA proof-of-concept experiments to 4 ms per transfer function. Furthermore, the interface electronics required by the OFDM approach have a lower component count and simpler designs allowing for more ports and hence more parallel measurement which leads to shorter aggregate measurement times when all the paths in the structure are measured. Attempts to address the high peak-to-average power ratio (PAPR) that is characteristic of OFDM systems were made. This was important because high peak amplitudes, though very sparse in the entire OFDM signal, would need to be accommodated in the design of the electronics thereby limiting how low the operation voltage can be made. In this vein, a tone-reservation technique was tested yielding moderate improvements in PAPR.

3. Goals for October 2020 to January 2021

The following were the project goals for the previous reporting period as per the project roadmap.

i. Validation of time-domain waveforms generated using frequency-domain (VNA and OFDM) measurements against direct measurements made on Acellent's commercial ScanGenie Mini hardware.
ii. Validation tests were to include more complex and realistic test structures in addition to the aluminum and CFRP coupons that had been used thus far.
iii. Hardware development: Schematic design and board layout.

The first item was originally not on the roadmap and was added after follow-up discussions that happened after the Multi-functional Materials for Defense Workshop that was held in September 2020.

4. Progress report for October 2020 to January 2021

i. Validation of waveforms generated using frequency-domain methods against direct ScanGenie Mini measurements.

As of September 2020, frequency-domain measurement gathered using the VNA and the newer OFDM approach had been successfully used to detect and localize defects in relatively simple aluminum and CFRP structures. At this point it was decided that an important next step before the hardware implementation of the proposed frequency-domain measurement systems was to validate the time-domain waveforms generated using these methods against those generated by a commercial system. Furthermore, to better emulate the complex structures that are found in aerospace structures and other realistic built environments, this validation process was required to include structures with more complex geometries and more challenging material properties. The hardware that was used for validation purposes was the latest version of Acellent's ScanGenie Mini together with the SHM Pro-SHM Patch software package.

The first set of experiments were conducted in the composite coupon SS55 IC shown in Figure 1. This is a 762 mm × 610 mm × 3 mm complex composite frame provided by Acellent for these experiments. The shaded area represents the 6 transducers that were used for these tests. To validate the waveforms generated from frequency-domain methods with those measured with the ScanGenie Mini, all five paths emanating from PZT 1 (starred in Figure 5) were measured in the frequency domain using the VNA and time-domain waveforms were generated from these measurements using methods that are detailed in our previous reports and publications. These generated time-domain waveforms were normalized and plotted alongside corresponding measurements made using the ScanGenie Mini. Slight time shifts were applied to the waveforms to account for the minute time differences (~ 5 μs) between due to signal path differences in the measurement systems. The plots showing the results are shown in Figure 6. A notable difference between the waveforms is the presence of significant crosstalk in the ScanGenie signals. If the observed crosstalk trends carry over to the prototype hardware under development, it will be an additional advantage of the frequency-domain based approach. Aside for differences due to crosstalk, the results show that the waveforms are closely matched across all the paths in this reasonably complex and highly attenuative structure. This strongly points to the fact that the frequency-domain methods accurately capture the physical interactions between the Lamb waves and the test structures including boundary interactions such as reflections, mode-conversions and interference.

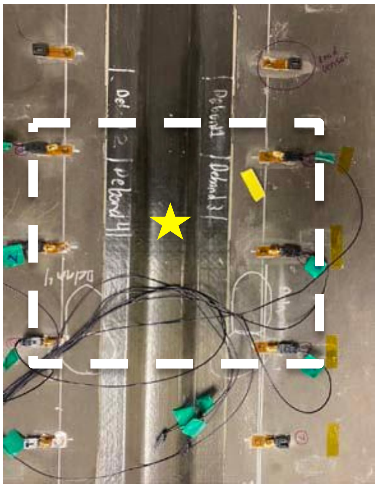
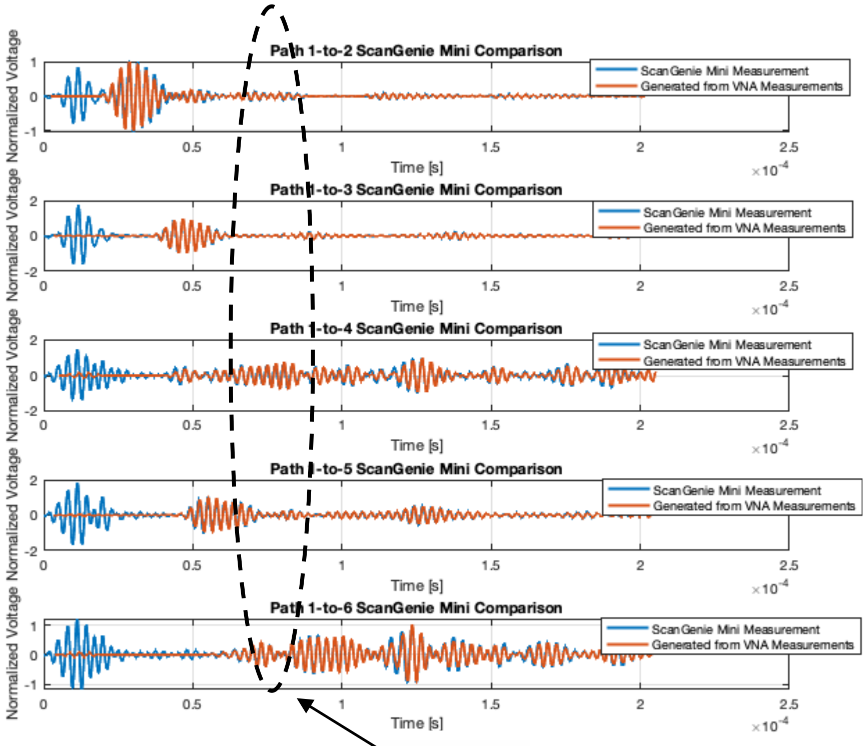


Figure 5: Composite coupon SS55 IC



Crosstalk

Figure 6: Comparison of ScanGenie measurements and generated waveforms

The other aspect of the frequency-domain measurements that was in question was the repeatability of the measurements. This was tested in four coupons which included one made of aluminum and three made of different kinds of composite. These coupons are shown in Figure 7. In each material, three paths were selected and for each path 10 frequency-domain spectrum (using both the VNA and the OFDM setup) measurements were taken in succession. These were subsequently processed to yield time-domain waveforms as before. The RMS error signal amplitude was then calculated and used as a metric to assess the repeatability of the measurements. Due to its higher frequency-domain measurement accuracy, the VNA outperforms the OFDM method. Therefore, for brevity only the OFDM results are presented below since they represent the worst-case results.

Aluminum - 457 mm × 457 mm × 3 mm

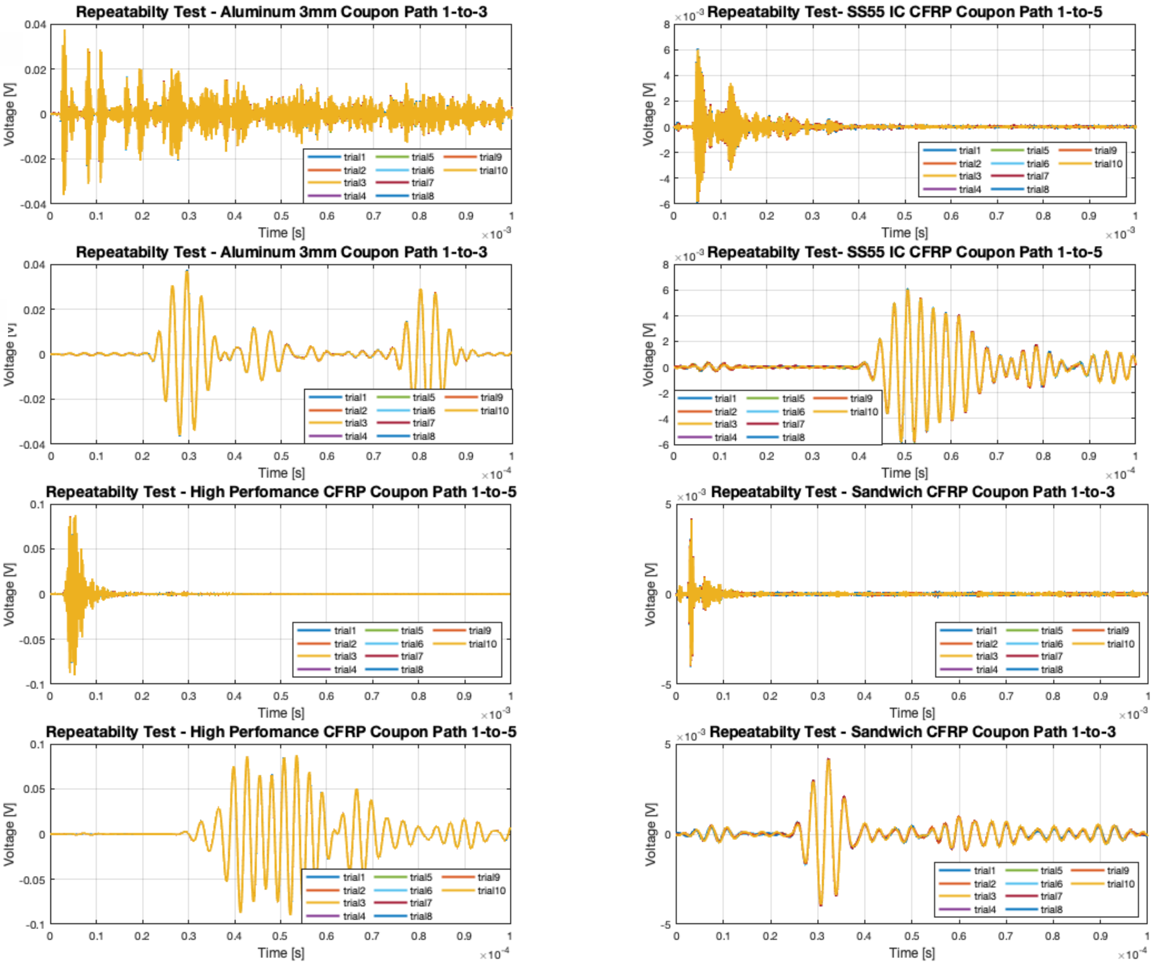
SSIC 55 - 762 mm × 610 mm × 3 mm

Ultra-strength CFRP - 305 mm × 305 mm × 3 mm

Sandwich CFRP - 305 mm × 305 mm × 10 mm

Figure 7: Coupons tested in repeatability tests

Exemplary plots for the time-domain waveforms generated for each material using the OFDM method are shown in Figure 8. As the plots show, the time domain waveforms display good repeatability both on the long and short time scales with very negligible deviations from trial to trial. In quantitative terms, the RMS error signal amplitudes were calculated to be between 0.1% and 1% of the values of their respective signals. This means that we see good repeatability from trial to trial. In addition to assessing repeatability, after it was observed that crosstalk is suppressed using the frequency-domain approaches, peak crosstalk values were also compared to the peak first-arrival signal values across all the coupons. It was found that peak crosstalk never exceeds 20% of the peak amplitude of the first-arrival wave when the highest crosstalk paths are included. More typically, crosstalk is below 5% of the peak amplitude of the first arrival wave. This points to very good crosstalk performance in the frequency domain methods.


Long time frame

hort time frame

Repeatabilty Test - Aluminum 3mm Coupon Path 1-to-3

Repeatabilty Test- SS55 IC CFRP Coupon Path 1-to-5

Repeatabilty Test - Aluminum 3mm Coupon Path 1-to-3

Repeatabilty Test- SS55 IC CFRP Coupon Path 1-to-5

Repeatabilty Test - High Perfomance CFRP Coupon Path 1-to-5

Repeatabilty Test - Sandwich CFRP Coupon Path 1-to-3

Repeatabilty Test - High Perfomance CFRP Coupon Path 1-to-5

Repeatabilty Test - Sandwich CFRP Coupon Path 1-to-3

Figure 7: Exemplary plots showing repeatability results in all tested coupons

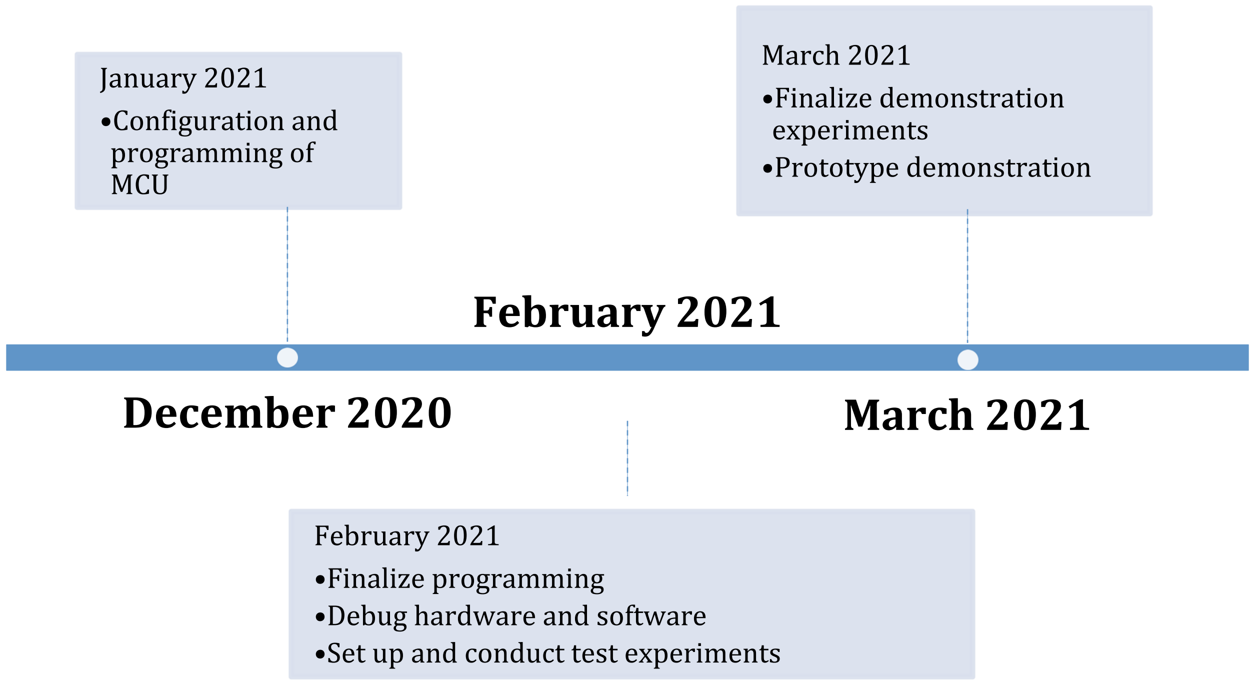
ii. Hardware development

After the validation of the frequency-domain methods against commercial hardware and confirmation of their good repeatability, we decided to implement the prototype system based on the OFDM method rather than the VNA-on-a-chip concept. The OFDM approach was picked over the VNA method because it allows for faster measurement times, a relatively simpler design and the capacity to accommodate more channels as discussed previously.

The initial plan was to develop a custom hardware to make the OFDM-based frequency domain measurements. However, after exploring the landscape for commercially available chips, we found that the ST Microelectronics STM32F303VE mixed-signal microcontroller offers the necessary functions (DACs, multi-channel ADCs, amplifiers, on-board memory, 32-bit processing and communications infrastructure) that fit our requirements in a compact 10 oz. development platform that can be leveraged for a faster development cycle and rapid iteration. This leaves programming, testing and demo preparation as the outstanding development tasks to be completed in the remaining 3 months on the project.

5. Project Roadmap

The projected roadmap of the project from now until completion is shown below.



January 2021
- Configuration and programming of MCU

February 2021
- Finalize programming
- Debug hardware and software
- Set up and conduct test experiments

March 2021
- Finalize demonstration experiments
- Prototype demonstration

6. Conclusion

In this reporting period, focus was placed on validating the proposed frequency-domain methods (VNA and OFDM based) against commercial SHM hardware, ensuring that the frequency-domain methods have good repeatability and advancing the development of a prototype design to showcase these novel methods. The validation experiments were conducted in test coupons that included coupons with more complex geometries and properties than those that have been used to demonstrate these frequency-domain based methods before. The results of the validation experiments show that the normalized waveforms generated using the frequency-domain methods are identical with those of direct measurements taken on the commercial ScanGenie Mini platform. This means that the lower voltage frequency domain measurements accurately capture the Lamb-wave physics and complex boundary phenomenon that occur when the waves are reflected by the structures' edges. Furthermore, the generated waveforms are characterized by markedly less crosstalk (at most 20% of the peak amplitude of the first arrival wave) and very good repeatability (at most 0.1% to 1% RMS error). Regarding hardware development, the OFDM method was chosen for implementation and the core of the design will be a ST Microelectronics STM32F303VE mixed-signal microcontroller. The remaining development time will be focused on configuration and programming, debugging, running experiments and setting up the final demonstration.