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(Quantum Accelerator) Superconducting-FET microwave amplifier for qubit readout

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14. ABSTRACT Superconducting parametric amplifiers are a key enabling technology for fast, high-fidelity readout of superconducting qubit processors. However, they have shortcomings such as limited power handling capacity, and need bulky auxiliary ferrite-based directional components which makes them difficult to integrate with large-scale qubit systems. We propose to build amplifiers that meet all the necessary performance metrics for qubit readout while also being directional and thus easy to integrate with quantum processors. Our approach is to exploit superconducting FieldEffect-Transistors (SFETs) built with recently developed superconductor-semiconductor hybrid heterostructures which we anticipate can achieve the ultra-low-noise performance of superconducting parametric amplifiers in combination with the attractive features of classic semiconductor amplifier designs such as simple DC biasing, large power handling and directionality. Success would make it possible to integrate qubits and readout devices thus bringing us closer to scalable next-generation quantum-computing hardware. (Approved for Public Release)					
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(Quantum Accelerator) Superconducting-FET microwave amplifier for qubit readout

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1 Accomplishments

1.1 Research objectives:

Superconducting parametric amplifiers are a key enabling technology for fast, high-fidelity readout of superconducting qubit processors. However, current state-of-the-art amplifiers, some commercially available, have shortcomings which make them difficult to integrate with large-scale qubit systems. The objective of this project was to make and characterize a Superconducting Field-Effect-Transistor (SFET) with the recently developed Aluminum-Indium Arsenide (Al-InAs) superconductor-semiconductor material platform. We would then use SFETs to build an ultra-low-noise microwave amplifier for the measurement of superconducting qubit processors. To achieve this goal, we proposed the following set of tasks over the course of this project.

- **Task 1:** Fabricate an optimized microwave transistor with the Al-InAs material platform.
- **Task 2:** Benchmark DC current-voltage characteristics of the transistor at room temperature.
- **Task 3:** Operate the transistor as an SFET at 20 mK and characterize its DC properties.
- **Task 4:** Measure the current shot noise produced by the SFET at targeted microwave frequencies to identify the conditions for lowest added noise and lowest static power dissipation.
- **Task 5:** Design and test an SFET amplifier for qubit measurement.

1.2 Accomplishments

Shankar group has successfully fabricated superconducting-field-effect-transistors (SFETs) on heterostructures provided by **Shabani** group (**Task 1**). We have also measured the DC current-voltage characteristics of the transistor at room temperature and in a dilution refrigerator at 20 mK (**Task 2** and **Task 3**). A key outcome of these objectives was to develop the fabrication recipes to make SFETs at UT Austin and to demonstrate that we can measure DC characteristics similar to those measured in **Shabani** group at NYU, thus spreading the expertise to work with the Al-InAs material platform.

One conclusion of the DC characterization was that, as expected, our device behaves as a gate-voltage tunable Josephson junction (JJ) for bias voltage below the superconducting gap of Al ($\sim 200 \mu\text{V}$). This feature can be exploited to make a quantum-limited superconducting parametric amplifier whose center frequency is tunable by the gate voltage bias. Such gate-voltage tuning is advantageous for scaling compared to conventional Josephson amplifiers, which are tuned by the magnetic field from a nearby current loop, as it reduces cross-talk between devices. We are therefore in the process of building an SFET amplifier (**Task 5**), using a parametric amplifier design principle, where the SFET acts as a gate-voltage tunable Josephson junction. We have completed an initial microwave design and are currently fabricating the device to be subsequently characterized and tested for qubit measurement.

An alternative amplifier design would be to use a circuit like in conventional semiconductor amplifiers such as the common-source FET amplifier. In FET amplifiers, the energy for amplification is provided by a simple DC current bias, unlike a parametric amplifier, which needs a pump drive from an microwave generator that is orders-of-magnitude more expensive. FET-style amplifiers would use the SFET like a conventional FET - with large bias voltages (above the superconducting gap $\sim 200 \mu\text{V}$), where the device current saturates as a function of voltage. This current saturation has not been observed so far, indicating that we need more fabrication and characterization cycles to optimize the SFET to behave as a conventional FET. Once, this optimization is complete, we will measure the current shot noise of the SFET (**Task 4**) and subsequently build a common-source FET amplifier with it.

We would like to highlight that the ongoing pandemic has hindered our access to nanofabrication facilities and for students to be trained on fabrication and characterization tools. It also slowed down the completion of the wiring of our dilution refrigerator. Nevertheless we are hopeful that with another six months of effort we will succeed in demonstrating a gate-voltage tunable Josephson parametric amplifier within the **Shankar** group. Prototypes of such an amplifier have been recently demonstrated with graphene Josephson junctions (see arXiv: 2204.02103 and arXiv: 2204.02175) and with Al-InAs Josephson junctions by the group of Andrew Higginbotham at IST Austria, indicating interest in the community to build such devices.

1.3 Dissemination of results

Shankar group: student **Zhuoqun Hao** presented an oral talk titled “Novel superconductor-semiconductor low-noise amplifier based on InAs-Al JJFET” at the APS March meeting in March 2022.

Shabani group: students **Mehdi Hatefipour** and **William Strickland** are preparing a paper on improving materials synthesis of InAs-Al structures.

2 Impacts

The impact of success in this project will be to make it possible to integrate a superconducting qubit processor together with its readout devices which would have implications for scaling up next generation quantum-computing hardware. More broadly, this project would establish that superconductor-semiconductor heterostructures can be closely integrated with superconducting quantum circuits which opens many new possibilities for processing of quantum microwave signals.

Beyond the research goals, our project also supported one graduate student at UT Austin, **Zhuoqun Hao** and two graduate students at NYU, **Mehdi Hatefipour** and **William Strickland**. These personnel were trained and successfully conducted the growth of the Al-InAs heterostructure by molecular beam epitaxy, cryogenic magneto-transport characterization of these heterostructures, and the fabrication of the SFET with nanofabrication processes such as e-beam lithography, etching of III-V materials, atomic layer deposition and e-beam deposition of superconducting metals.

3 Technical Updates

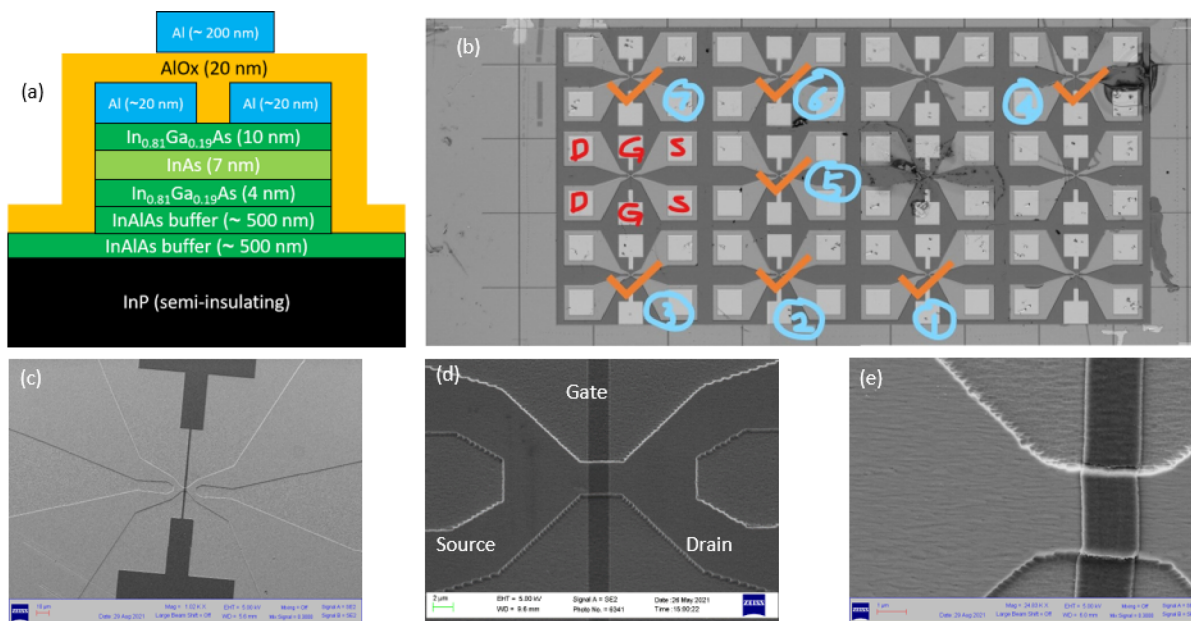


Figure 1: (a) Cartoon of device cross-section. (b) Optical micrograph of chip with 12 candidate devices with channel lengths ranging from 100 nm to 1 μm . Labelled devices were electrically characterized at 20 mK by **Shabani** group and subsequently at **Shankar** group (c), (d), (e) Scanning electron micrograph of a device at progressively higher magnification showing gate, source and drain electrodes.

A schematic of the device structure we are building, is shown in Fig. 1 along with optical and SEM micrographs of fabricated devices. The multi-layer heterostructure was grown by molecular beam epitaxy and then characterized by cryogenic magneto-transport measurements by students, Mehdi Hatefipour and William Strickland, in **Shabani** group. The heterostructures were then shipped to **Shankar** group for further nanofabrication. At UT Austin, **Shankar** group has developed the recipes for (i) defining the mesa via lithography and wet etch, (ii) defining the channel region and Al source and drain contacts via lithography and wet etch, (iii) atomic layer deposition (ALD) of aluminum oxide which acts as the gate dielectric, (iv) defining the Al gate, source and drain electrodes via lithography, e-beam evaporation and liftoff. Due to the small structures involved and need for precise alignment, e-beam lithography was performed with a Raith 30 keV e-beam writer. Unfortunately, the progress in developing these recipes was slowed by some unanticipated downtime on the writer. Nevertheless, we have successfully developed the recipes to that point that our student, **Zhuoqun Hao** is able to fabricate a chip containing multiple candidate devices within a week of work.

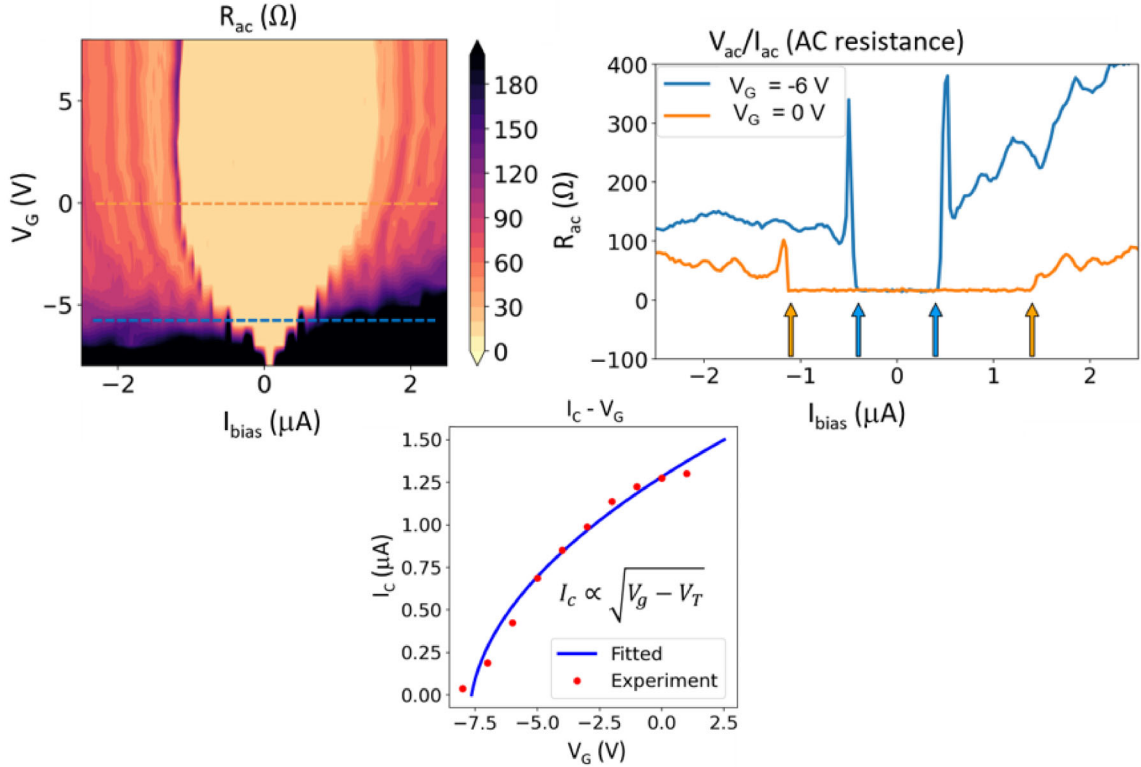


Figure 2: Small signal ac electrical characterization performed at **Shankar** group (a) Differential resistance versus drain current and gate voltage. (b) Line cuts at $V_G = 0$ V and -6 V. Arrows indicate the location of the switching current from superconducting to normal state which provides an estimate of the critical current, I_C . (c) Extracted critical current I_C versus gate voltage V_G shown with a fit to $I_C \propto \sqrt{V_G - V_T}$ dependence

To characterize SFETs in-house, **Shankar** group assembled the electronics, wiring and a home-built sample holder in our dilution fridge for low temperature DC electrical charac-

terization. The electronics setup consists of a lockin-amplifier, programmable voltage source and voltmeter, while the low temperature wiring contains cryogenic RC and LC filtering to reject noise arising from higher temperature fridge stages. Initial devices did not show any gate voltage dependence of the super-current. These non-idealities were surmised to be due to fabrication errors - in particular the wet etch process to define the channel was found to have partially etched the Al source-drain electrodes in these devices. In subsequent rounds of fabrication we optimized the etch process to define the SFET channel. We were then able to observe the signature of supercurrent expected for the device at low drain voltage bias in a differential resistance measurement (see Fig. 2). In this regime of bias voltage/current, we can treat the SFET as a gate-voltage tunable JJ. Such a regime of operation has been used by **Shabani** group to realize gatemon qubits. The extracted critical current shows the expected dependence on gate voltage of $I_C \propto \sqrt{V_G - V_T}$ where V_T is the threshold voltage of the device.

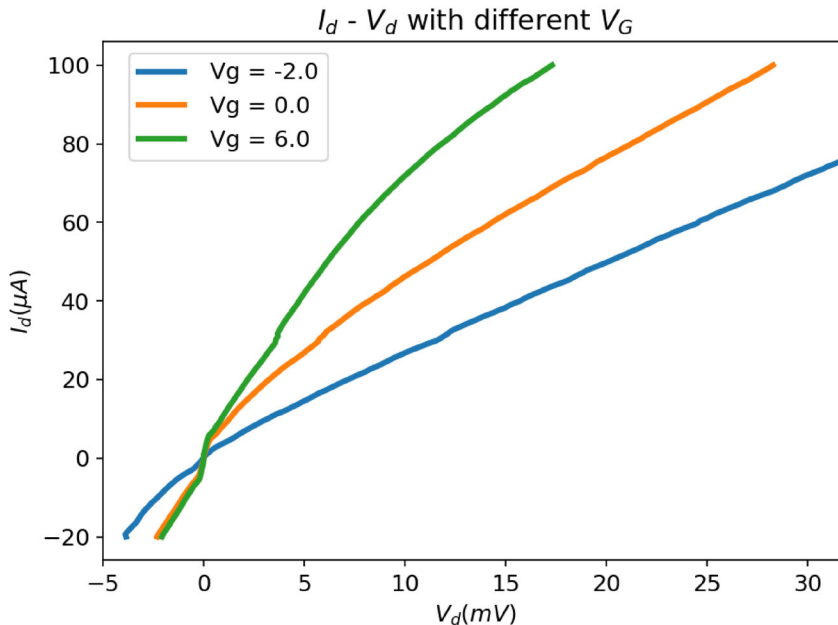


Figure 3: DC electrical characterization performed at **Shankar** group at drain-source bias voltage above 200 μ V. No saturation in drain current is observed at large bias voltage

One of our project goals was to design a common-source FET amplifier. In such an amplifier, the SFET would be operated in the so-called saturation regime where the drain-source current is independent of bias voltage. However, as shown in Fig. 3 we have not yet observed this saturation of drain current at high drain voltage bias in our SFET. Possible causes are the presence of parallel conducting channels in the heterostructure that are independent of the gate voltage or the presence of band-to-band tunneling which is present in low-band-gap semiconductors like InAs. These could be addressed using a so-called T-gate structure, which would require more rounds of device optimization.

We are currently focusing on building a gate-voltage pumped Josephson parametric am-

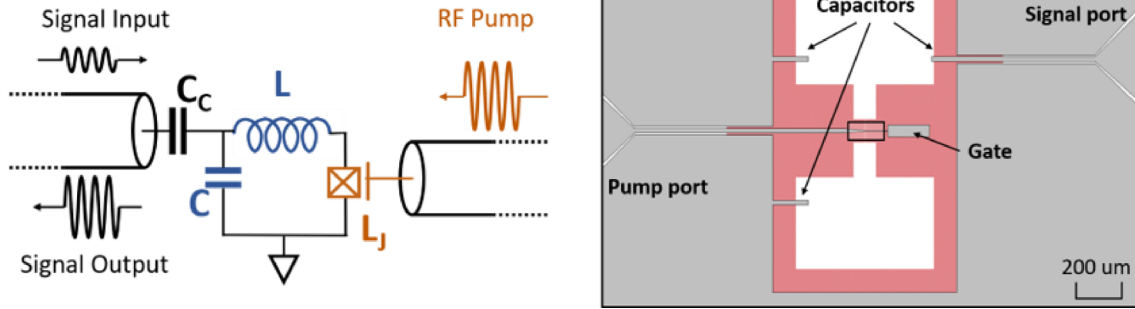


Figure 4: Gate voltage pumped parametric amplifier (a) Schematic circuit consisting of an LC resonator with an embedded gate-voltage tunable JJ. An RF pump is applied to the gate electrode and a small signal applied to the LC resonator is reflected with gain. (b) Layout of the chip

plifier with the SFET operated as a gate voltage tunable JJ. Fig. 4 shows a schematic circuit of a gate-voltage pumped Josephson parametric amplifier, along with the layout of the design to be realized with e-beam lithography, which is currently under fabrication. A key feature we are pursuing, unlike other groups in the community, is to apply the RF pump directly to the gate electrode. This separates the pump drive from port with the signal to be amplified, thus allowing us to protect the upstream sensitive qubit circuits from the strong pump signal

In parallel with work at UT Austin, **Shabani** has been in collaboration with Andrew Higginbotham at IST Austria (separate from this funding) to explore microwave properties of InAs-Al heterostructures. The exciting result, which benefits our project, is the demonstration of a quantum-limited amplifier using a SFET. Initial measurements show 20 dB of gain over a 4 MHz instantaneous bandwidth, with an operating frequency that is tunable over 2 GHz via the field effect. This is a promising new direction that combined with the goals of this project can add to the toolbox of quantum information processing.