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Development of a Photonic Field-Programmable Gate Array (pFPGA) for Software-Controlled Photonics

DIRK ENGLUND
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
77 MASSACHUSETTS AVE
CAMBRIDGE, MA, 02139
USA

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Dirk R. Englund

Massachusetts Institute of Technology

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Massachusetts Institute of Technology
77 Massachusetts Avenue
Cambridge, MA 02139

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Last Name, First Name: Englund, Dirk

Months worked: .2 summer month

Describe briefly how this person contributed to the project: Supervised experiments, theory, wrote manuscripts, etc.

Project Role: PI.

Additional Funding Source(s): UMD/NSF award (UMD Award: 28725-Z8401005), NSF award (NSF Award Number: EFMA1641064), AFOSR award (AFOSR Award Number: FA95501610391), NSF award: (NSF Award Number: CCF1640012), Harvard subaward/ARO MURI (Harvard subaward number: 134062-5093041, ARO Award Number: W911NF1510548), ARO MURI (ARO Award Number: W911NF1810432), NSF award (NSF Award Number: OAC1839159), MITRE award (MITRE Award Number: Research Agmt. 126508), NSF award (NSF Award Number: ECCS1933556), NSF award (NSF Award Number: CNS1946976), UMD/NSF RAISE-TAQS (UMD award number: 81350-Z3438201 NSF Award Number: OMA1936314), Stanford subaward/DOE (Stanford Subaward Number: 62267053-151086, DOE Award Number: DE-SC0020115), Harvard subaward/DARPA (Harvard Subaward Number:134371-5113608, DARPA Award Number: W911NF2010021), ARO award (ARO Award Number: W911NF2010084), AFOSR award (AFOSR Award Number: FA95502010105), Air Force Korea award (Air Force Award Number: FA23862014070), AFRL award (AFRL Award Number: FA87502021007), Harvard subaward/QuEra (Harvard Subaward Number: Agmt No. 218050-5116760), Photonspot award/NASA (Photonspot Award Number: STTR under 80NSSC21C0126).

International Business during Report Period.

1) Did the individual collaborate with individuals located in a foreign country? Yes: we collaborated with Prof. Peter O’Brien of the Tyndall National Institute in Ireland.

2) International Travel: No.

Last Name, First Name: Bandyopadhyay, Saumil

Months worked: 4.17 calendar month

Describe briefly how this person contributed to the project: Saumil has been developing the design & packaging for the 20x20 programmable many-mode interferometer (PMMI), as well as inventing a powerful error correction algorithm for the control of the device.

Project Role: PhD student.

Additional Funding Source(s): NTT Research (Research Collaboration Agreement), UMD/NSF C-Accel (UMD award number: 93943-Z3687203, NSF Award Number: OIA2040695), UMD/NSF RAISE-TAQS (UMD award number: 81350-Z3438201 NSF Award Number: OMA1936314) and NSF Graduate Research Fellowship (NSF Award Number: 1745302).

International Business during Report Period.

1) Did the individual collaborate with individuals located in a foreign country? Yes. Saumil has been working with our collaborator Prof. Peter O'Brien and his group at the University College Cork, Ireland, where he leads the Photonics Packaging Group. Dr. O'Brien is also deputy director of the Science Foundation Ireland, Irish Photonic Integration Centre (www.ipic.ie). Dr O'Brien is an Adjunct Professor at the College of Optical Science, University of Arizona, Tucson.

2) International Travel: No.

Last Name, First Name: Sludds, Alexander

Months worked: 2.35 calendar months

Describe briefly how this person contributed to the project: Alex has contributed to the packaging and testing of programmable photonic circuits developed in this program.

Project Role: PhD student.

Additional Funding Source(s): NTT Research (Research Collaboration Agreement), NSF EAGER (NSF Award Number: CNS1946976), AFRL award (Federal Award Number: FA8750-20-2-1007), ARO Award: (Federal Award Number: W911NF-17-1-0527) and NSF Graduate Research Fellowship (NSF Award Number: 1745302).

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1) Did the individual collaborate with individuals located in a foreign country? No.

2) International Travel: No.

1. Archival Publications (published) during reporting period:

1. Ryan Hamerly, Saumil Bandyopadhyay, Dirk Englund, ``Asymptotically fault-tolerant programmable photonics," *Nature Communications* **13** 6831 (2022)

2. Saumil Bandyopadhyay, Ryan Hamerly, Dirk Englund, ``Hardware error correction for programmable photonics," Optica Vol. 8, Issue 10, pp. 1247-1255 (2021)
3. Saumil Bandyopadhyay, Dirk Englund, ``Alignment-free photonic interconnects," ArXiv: 2110.12851 (2021)
4. Saumil Bandyopadhyay, Alexander Sludds, Stefan Krastanov, Ryan Hamerly, Nicholas Harris, Darius Bunandar, Matthew Streshinsky, Michael Hochberg, Dirk Englund, ``Single chip photonic deep neural network with accelerated training," arXiv:2207.06883 [cs.ET] (2022)
5. Ryan Hamerly, Saumil Bandyopadhyay, Dirk Englund, ``Accurate Self-Configuration of Rectangular Multiport Interferometers," Phys. Rev. Applied 18, 024019 (2022)
6. Ryan Hamerly, Saumil Bandyopadhyay, Dirk Englund, ``Stability of Self-Configuring Large Multiport Interferometers," Phys. Rev. Applied 18, 024018 (2022)
7. Alexander Sludds, Saumil Bandyopadhyay, Zaijun Chen, Zhizhen Zhong, Jared Cochrane, Liane Bernstein, Darius Bunandar, P. Ben Dixon, Scott A. Hamilton, Matthew Streshinsky, Ari Novack, Tom Baehr-Jones, Michael Hochberg, Manya Ghobadi, Ryan Hamerly, Dirk Englund, ``Delocalized Photonic Deep Learning on the Internet's Edge," Science, 378, 220 (2022)

2. New discoveries, inventions, or patent disclosures to report for this period?

The discoveries and inventions are reported in the papers above.

Patent Pending

Application Number: US 17/556,033

Filing Date: December 20, 2021

Publication Number and Date: *(Pending)*

Title: Error Correction for Programmable Photonics

Inventors: Saumil Bandyopadhyay, Ryan Hamerly, and Dirk Englund

Summary:

> **[0001]** If a unitary operation is realizable by an imperfect photonic circuit, it should not require optimization to deduce the required settings; rather, a small perturbation in the device behavior due to component deviation should translate directly to a small perturbation in the interferometer's phase settings to recover the original unitary. This insight has led us to consider a local error correction strategy, where circuit functionality

is restored by correcting hardware errors one at a time within each optical gate composing the circuit.

[0002] Here, we present a process to directly correct hardware errors for a programmable photonic circuit. Our process outperforms previous approaches in several key respects: 1) it is flexible, enabling a one-time device calibration to directly compute the hardware settings for any given unitary; 2) for sufficiently low hardware errors, the computed settings yield the exact unitary desired; and 3) our approach requires reduced or minimal overhead and does not make use of additional interferometers or internal detectors within every device. Our process can be used to correct fabrication errors in feedforward programmable circuits that implement arbitrary unitary matrices, as these systems have the most demanding requirements for fabrication precision. Our local error correction strategy individually corrects each optical gate within the circuit. It can be generalized to any programmable architecture making use of interferometers, including feedforward circuits with redundant devices and recirculating waveguide meshes.

[0003] Applying our approach to programmable photonics, such as optical neural networks and programmable coupled-ring systems, enables resilience to fabrication errors well beyond modern-day process tolerances. Error correction also greatly reduces the overhead for programmable photonics that require optimization to deduce the hardware settings, as it eliminates the need to retrain for each individual set of hardware with unknown fabrication errors. Current process tolerances suggest that our approach enables improved functionality for systems of up to hundreds of modes, providing a new avenue for scaling up programmable photonics.

Patent Pending

Application Number: US 17/711,640

Filing Date: April 1, 2022

Publication Number and Date: *(Pending)*

Title: Self-Configuration and Error Correction in Linear Photonic Circuits

Inventors: Ryan Hamerly, Saumil Bandyopadhyay, and Dirk Englund

Summary:

[0001] We disclose programming methods for multiport interferometers, based on measurement-assisted matrix diagonalization, that corrects for hardware errors in a near-optimal fashion without extra hardware complexity or pre-calibration. In addition, we present modified circuit architectures that further improve scaling: (1) a design based on modified tunable couplers to span a wider range of splitting ratios, and (2) a design based on the generalized FFT butterfly. These new architectures, coupled with error-tolerant programming methods, significantly relax the scaling constraints that hardware errors pose for linear photonic circuits.

Patent Pending

Application Number: US 17/470,803

Title: Self-Aligning Photonic Interconnections for Photonic Integrated Circuits

Filing Date: September 9, 2021

Publication Number and Date: *(Pending)*

Inventor(s): Saumil Bandyopadhyay and Dirk Englund

Summary:

[0001] A self-aligning photonic interconnect technology that is insensitive to misalignment can be used to connect PICs and other devices with photonic components. This technology uses the interaction created by two waveguides crossing at an angle, giving rise to efficient evanescent coupling at their intersection. Importantly, this coupler is invariant to translational misalignment, as two waveguides at an angle will still intersect after in-plane translation. Surprisingly, in addition to translational invariance, the coupling efficiency of this structure is far more insensitive to angular misalignment than more conventional approaches such as edge coupling. A cantilevered self-aligning coupler also relaxes tolerances for out-of-plane misalignment.

[0002] In addition to having large translational and angular misalignment tolerances, an inventive self-aligning photonic interconnect has several advantages over other PIC connectors. It can connect a single-mode waveguide on one PIC to a single-mode waveguide in the same PIC or another PIC. Its propagation loss can be extremely low, e.g., below 0.1 dB/cm. Its insertion loss can be less than 0.1 dB/facet. It can transmit almost arbitrarily many beams between two chips, without the need for single-mode waveguides or fibers—one self-aligning photonic interconnect can connect PICs with arbitrary waveguide pitches. It can be flexible and pliable and thus can conform to the surface of a PIC. A self-aligning photonic interconnect can be made using low-cost manufacturing techniques. And many two-dimensional (2D) self-aligning photonic interconnect can be layered or stacked on top of each other and molded together to enable 3D interconnect geometries.

3. Changes in research objectives (if any): No

4. Change in AFOSR Program Officer, if any: No

5. Extensions granted or milestones slipped, if any: N

6. SUMMARY

FPGAs (field programmable gate arrays) have revolutionized many areas of electronics, from dedicated circuit prototyping to machine learning accelerators. We are developing a new generation of photonic FPGAs (pFPGA) for programmable photonic circuits in this program. At the heart of the pFPGA is a packaged programmable many-mode interferometer (PMMI) capable of implementing arbitrary 20x20 linear optical transformations. This PMMI, developed in a collaboration with Elenion Technologies, was fabricated in a commercial silicon photonic foundry process. The chip couples twenty input and twenty output channels to standard telecom (SMF-28) fiber, incorporates 420 individually programmable phase shifters, and is bump-bonded for high-density interconnect packaging.

We completed the fabrication of this PIC several years ago and found the packaging to be the most difficult. The device is controlled by 20^2 =400 MZI phase shifters, for a total of 800 electrical connections once grounding wirings are taken into account (we use one ground per thermal phase shifter to reduce electrical crosstalk). Working with Tyndall for over two years, our collaborative team was able to complete a full prototype that we are currently testing. Furthermore, we created a core control interface and a novel error-correcting algorithm to enable programmable circuits with fidelity greater than 99.9%, as well as long-term stability enabled by in-situ feedback. We have held regular meetings with future users in the US photonics community to make the pFPGA available for AFOSR-relevant research activities.

Furthermore, due to COVID-imposed lab constraints, we delved two years ago into the problem of how to correct hardware errors during fabrication. This investigation yielded a number of surprising results, indicating tremendous algorithmic resilience when using local (algorithms) in material unit cells. And whereas last year we discovered a resource-efficient algorithm that eliminates errors ϵ or reduces them to $O(\epsilon^2)$, that scheme required time-consuming pre-calibration followed by error correction. We now have developed algorithms that correct errors right away in the calibration step, greatly simplifying calibration time and reducing residual errors [1]. Finally, we achieved major advances in in-situ trained machine learning on such circuits, including a novel device that includes engineered in-line nonlinearities [2].

7. INTRODUCTION

Motivation: The ultimate goal is to program complex optical systems to perform useful functions like high-speed communications, beam steering, photonic computing accelerators, displays, and advanced precision, navigation, and timing.
The vast majority of photonic systems are purpose-built for specific applications. However, just as many types of application-specific integrated circuit (ASIC) applications have been replaced by field-programmable gate arrays (FPGA), there is a compelling case for a new generation of photonic photonic FPGAs (pFPGAs) that promise improved performance while reducing development time and cost[3].

A pre-packaged pFPGA system with optimized control hardware and software would have far-reaching implications: research groups with no expertise in semiconductor packaging or nanophotonics would be able to jump right into projects with far-reaching implications in fields as diverse as neuromorphic computing, telecommunications, quantum information processing, sensing, and imaging. Large-scale pFPGAs raise fundamental questions about error propagation in coherent systems and the limits of hybrid reversible-irreversible computing. Simply put, the pFGPA could do for photonics applications what FPGAs have done for electronics.

State of the art: The core of the pFGPA is a universally programmable mode transformer, the most advanced of which has been realized in cascaded Mach-Zehnder

Interferometers (MZIs); we call this the programmable many-mode interferometer (PMMI).

Gap: However, there exists an open challenge in developing PMMIs with a minimum size of tens of input and output modes with sufficiently high-fidelity control and transmission.

Approach: Our approach is to develop a 20x20 - mode pFPGA, consisting of a foundry-based silicon photonic integrated circuit (PIC) with the requisite $20^2=400$ phase control degrees of freedom (plus additional phase shifters in the last switch layer) and built-in detectors and feedback, controlled with advanced 12-bit control electronics, and run via a new suite of control algorithms built from the ground up on advanced error correction for optimal control.

Goals: A) Development of a pFPGA built around a 20x20 universal optics. B) Demonstration of near-perfect large-scale optical transformations. C) Application of the pFPGA in photonic accelerators for artificial intelligence (AI).

8. RESULTS AND DISCUSSION

8.1. Goal A: Development of a pFPGA built around a 20x20 universal optics.

Summary: We completed packaging of our first PMMI chips in collaboration with Tyndall National Institute, which contains 420 active components and over 900 passive components and are bump bonded to high-density interconnect (HDI) packaging.

Fig. 1 shows our first-generation pFPGA. It uses a custom electronic interposer with 500 channels, bump-bonded to the PIC. The PIC consists of 200 MZIs as well as in-line photodetectors. The assembly is packaged in a custom housing for efficient and resilient coupling to a fiber array and precision control electronics (Qontrol).

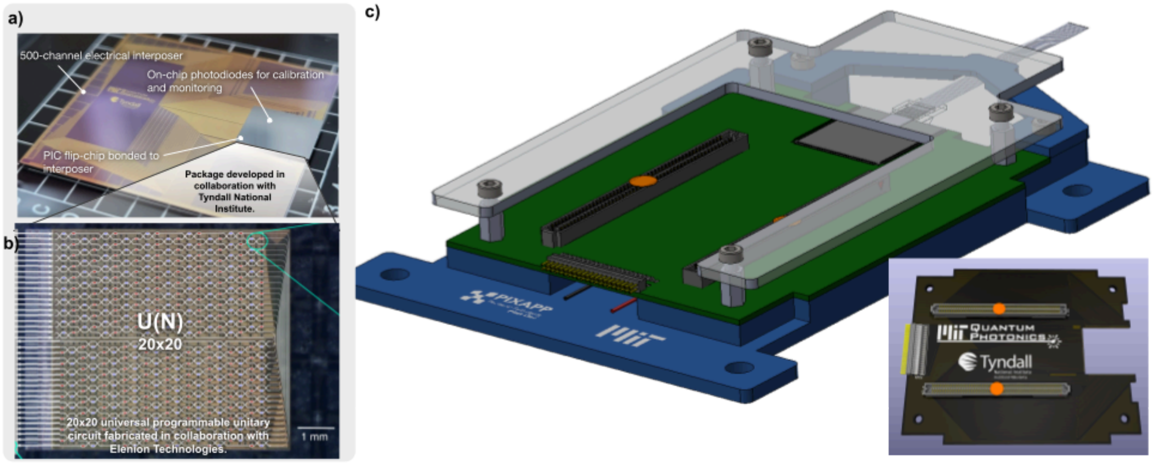

Figure 1. a) The electrical interposer developed in this program in collaboration b) The programmable U(20) SOI PIC, whose bump-bond-based packaging was just completed in an extensive MIT-Tyndall collaboration, has a broad operating range over several THz in the c-band, and uses thermal phase shifters with > 100 kHz response rate. c) Packaged system.

Figure 2. Photograph of the final packaged PMMI system. The 20x20 unitary photonic circuit is flip-chip bonded to a custom high-density silicon interposer, which is wirebonded to a high-resolution printed circuit board for easy interfacing

to control electronics. Optical signals are interfaced to the device through a fiber array glued to the PIC, enabling simplified coupling without micrometer alignment stages.

8.1.1. Alignment-free photonic interconnects

Next generation optoelectronic systems will require the efficient transfer of optical signals between many discrete photonic components integrated onto a single substrate. While modern assembly processes can easily integrate thousands of electrical components onto a single board, photonic assembly is far more challenging due to the wavelength-scale alignment tolerances required. Here we address this problem by introducing an alignment-free photonic coupler robust to x, y, z displacement and angular misalignment. This alignment-free coupler engineers a translationally-invariant evanescent interaction between waveguides by intersecting them at an angle, which enables a lateral and angular alignment tolerance fundamentally larger than non-evanescent approaches such as edge coupling. We show that our approach can function as a universal photonic connector interfacing photonic integrated circuits and microchiplets across different platforms. As a potential use case, we describe a new type of self-aligning photonic circuit board enabled by our approach that greatly simplifies assembly of complex optoelectronic systems.

Publication: Saumil Bandyopadhyay, Dirk Englund, ``Alignment-free photonic interconnects," ArXiv: 2110.12851 (2021)

Acknowledgement: S.B. was supported by a National Science Foundation (NSF) Graduate Research Fellowship under grant no. 1745302 and the Air Force Office of Scientific Research (AFOSR) under award numbers FA9550-16-1-0391 and FA9550-20-1-0113. D.E. acknowledges support from the Air Force Research Laboratory (AFRL) under award number FA8750-20-2-1007. The authors are grateful to Dr. Carlos Errando Herranz, Dr. Mohamed ElKabbash, Dr. Genevieve Clark, and Alexander Sludds for useful discussions.)

8.2. Goal B: Demonstration of near-perfect large-scale optical transformations.

Summary: We discovered a control algorithm that can fully cancel a great range of fabrication errors without device overhead and based on few measurements. Our hardware error correction for programmable photonics has no hardware overhead requirements.

Detail: Our work, which is detailed in our recent publication in Optica [4], tackles a central challenge in programmable photonic integrated circuits (PICs), whose proposed applications range from machine learning accelerators to fully-reprogrammable optical

FPGAs. Since Babbage demonstrated the first mechanical computing machine, the central challenge in analog information processors has been the rapid accumulation of errors. This problem manifests in programmable PICs primarily through component variation across the chip, which has been shown to significantly degrade performance for applications such as artificial intelligence and optical signal processing. Component errors can be reduced by optimizing the circuit settings with real-time feedback from the chip; however, these strategies require significant overhead, such as photodiodes within each device, and are inefficient.

Our error correction scheme corrects errors *locally* at each optical gate within the circuit. Unlike previous work, our approach requires only a one-time calibration of the device errors. Using our approach, we show that chip settings determined once in software can be deployed to arbitrary numbers of chips with unique fabrication errors. Thus, our hardware error correction scheme enables programmable photonics to scale up to hundreds of optical modes *without a corresponding increase in overhead for circuit optimization*.

Beyond the immediate application to silicon-PIC based PMMIs for this program, our algorithm applies to all leading programmable PIC architectures, including the feedforward architectures being studied for machine learning and the recirculating meshes being used for optical signal processing. Moreover, we rigorously prove that for low hardware error ϵ, our scheme can *reduce the error to zero.* Beyond that error bound, we prove that our approach enables in feedforward circuits an error reduction from ϵ to ϵ^2, as detailed in our paper.

8.2.1. Asymptotically-fault tolerant programmable photonics

Component errors limit the scaling of multiport interferometers based on MZI meshes. These errors arise because imperfect MZIs cannot be perfectly programmed to the cross state. Here, we introduce two modified mesh architectures that overcome this limitation: (1) a 3-splitter MZI for generic errors, and (2) a broadband MZI+Crossing design for correlated errors. Because these designs allow for perfect realization of the cross state, the matrix fidelity no longer decreases with mesh size, allowing scaling to arbitrarily large meshes. The proposed architectures support progressive self-configuration, are more compact than previous MZI-doubling schemes, and do not require additional phase shifters. This eliminates a major obstacle to the development of very-large-scale linear photonic circuits.

Publication: Ryan Hamerly, Saumil Bandyopadhyay, Dirk Englund, ``Asymptotically fault-tolerant programmable photonics," *Nature Communications* **13** 6831 (2022)

Acknowledgement: S.B. is supported by an NSF Graduate Research Fellowship. D.E. acknowledges funding from AFOSR (no. FA9550-20-1-0113, FA9550-16-1-0391). The authors thank Prof. David A. B. Miller and Sunil Pai for helpful discussions.)

8.2.2. Hardware error correction for programmable photonics

Programmable photonic circuits of reconfigurable interferometers can be used to implement arbitrary operations on optical modes, providing a flexible platform for accelerating tasks in quantum simulation, signal processing, and artificial intelligence. A major obstacle to scaling up these systems is static fabrication error, where small component errors within each device accrue to produce significant errors within the circuit computation. Mitigating this error usually requires numerical optimization dependent on real-time feedback from the circuit, which can greatly limit the scalability of the hardware. Here we present a deterministic approach to correcting circuit errors by locally correcting hardware errors within individual optical gates. We apply our approach to simulations of large scale optical neural networks and infinite impulse response filters implemented in programmable photonics, finding that they remain resilient to component error well beyond modern day process tolerances. Our results highlight a potential way to scale up programmable photonics to hundreds of modes with current fabrication processes.

Publication: Saumil Bandyopadhyay, Ryan Hamerly, Dirk Englund, ``Hardware error correction for programmable photonics," Optica Vol. 8, Issue 10, pp. 1247-1255 (2021)

Acknowledgement: National Science Foundation (1745302); Air Force Office of Scientific Research (FA9550-16-1-0391, FA9550-20-1-0113); Intelligence Community Postdoctoral Research Fellowship Program.)

8.2.3. Stability of Self-Configuring Large Multiport Interferometers

Realistic multiport interferometers (beamsplitter meshes) are sensitive to component imperfections, and this sensitivity increases with size. Self-configuration techniques can be employed to correct these imperfections, but not all techniques are equal. This paper highlights the importance of algorithmic stability in self-configuration. Naïve approaches based on sequentially setting matrix elements are unstable and perform poorly for large meshes, while techniques based on power ratios perform well in all cases, even in the presence of large errors. Based on this insight, we propose a self-configuration scheme for triangular meshes that requires only external detectors and works without prior knowledge of the component imperfections. This scheme extends to the rectangular mesh by adding a single array of detectors along the diagonal.

Publication: Ryan Hamerly, Saumil Bandyopadhyay, Dirk Englund, ``Stability of Self-Configuring Large Multiport Interferometers," Phys. Rev. Applied 18, 024018 (2022)

Acknowledgement: S.B. is supported by a National Science Foundation (NSF) Graduate Research Fellowship (grant no.1745302). D.E. acknowledges funding from the Air Force Office of Scientific Research (AFOSR) (grant no. FA9550- 20-1-0113 and FA9550-16-1-0391). Source code implementing the algorithms described in this paper is available in the Meshes package [39].)

8.2.4. Accurate Self-Configuration of Rectangular Multiport Interferometers

Multiport interferometers based on integrated beamsplitter meshes are widely used in photonic technologies. While the rectangular mesh is favored for its compactness and uniformity, its geometry resists conventional self-configuration approaches, which are essential to programming large meshes in the presence of fabrication error. Here, we present a configuration algorithm, related to the 2 × 2 block decomposition of a unitary matrix, that overcomes this limitation. Our proposed algorithm is robust to errors, requires no prior knowledge of the process variations, and relies only on external sources and detectors. We show that self-configuration using this technique reduces the effect of fabrication errors by the same quadratic factor observed in triangular meshes. This relaxes a significant limit to the size of multiport interferometers, removing a major roadblock to the scaling of optical quantum and machine-learning hardware.

Publication: Ryan Hamerly, Saumil Bandyopadhyay, Dirk Englund, ``Accurate Self-Configuration of Rectangular Multiport Interferometers," Phys. Rev. Applied 18, 024019 (2022)

Acknowledgement: S.B. is supported by an NSF Graduate Research Fellowship. D.E. acknowledges funding from AFOSR (no. FA9550-20-1-0113, FA9550-16-1-0391).)

8.3. Goal C: Application of the pFPGA in photonic accelerators for AI

8.3.1. Single chip photonic deep neural network with accelerated training

Abstract: As deep neural networks (DNNs) revolutionize machine learning, energy consumption and throughput are emerging as fundamental limitations of CMOS electronics. This has motivated a search for new hardware architectures optimized for artificial intelligence, such as electronic systolic arrays, memristor crossbar arrays, and optical accelerators. Optical systems can perform linear matrix operations at

exceptionally high rate and efficiency, motivating recent demonstrations of low latency linear algebra and optical energy consumption below a photon per multiply-accumulate operation. However, demonstrating systems that co-integrate both linear and nonlinear processing units in a single chip remains a central challenge. Here we introduce such a system in a scalable photonic integrated circuit (PIC), enabled by several key advances: (i) high-bandwidth and low-power programmable nonlinear optical function units (NOFUs); (ii) coherent matrix multiplication units (CMXUs); and (iii) in situ training with optical acceleration. We experimentally demonstrate this fully-integrated coherent optical neural network (FICONN) architecture for a 3-layer DNN comprising 12 NOFUs and three CMXUs operating in the telecom C-band. Using in situ training on a vowel classification task, the FICONN achieves 92.7% accuracy on a test set, which is identical to the accuracy obtained on a digital computer with the same number of weights. This work lends experimental evidence to theoretical proposals for in situ training, unlocking orders of magnitude improvements in the throughput of training data. Moreover, the FICONN opens the path to inference at nanosecond latency and femtojoule per operation energy efficiency.

Publication: Saumil Bandyopadhyay, Alexander Sludds, Stefan Krastanov, Ryan Hamerly, Nicholas Harris, Darius Bunandar, Matthew Streshinsky, Michael Hochberg, Dirk Englund, ``Single chip photonic deep neural network with accelerated training," >cs>ArXiv:2208.01623 (2022). Currently under review.

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8.3.3. Experimental quantum speed-up in reinforcement learning agents

As the field of artificial intelligence advances, the demand for algorithms that can learn quickly and efficiently increases. An important paradigm within artificial intelligence is reinforcement learning1, where decision-making entities called agents interact with environments and learn by updating their behavior based on obtained feed- back. The crucial question for practical appli- cations is how fast agents learn2. While various works have made use of quantum mechanics to speed up the agent's decision-making process, a reduction in learning time has not been demon- strated yet. Here, we present a reinforcement learning experiment where the learning process of an agent is sped up by utilizing a quantum com- munication channel with the environment. We further show that combining this scenario with classical communication enables the evaluation of such an improvement, and additionally allows for optimal control of the learning progress. We im- plement this learning protocol on a compact and fully tuneable integrated nanophotonic processor. The device interfaces with telecom-wavelength photons and features a fast active feedback mechanism, allowing us to demonstrate the agent's systematic quantum advantage in a setup that could be readily integrated within future large- scale quantum communication networks.

Publication: Valeria Saggio, B. Asenbeck, A. Hamann, T. Strömberg, P. Schiansky, V. Dunjko, N. Friis, N. C. Harris, M. Hochberg, D. Englund, S. Wölk, H. J. Briegel, and P. Walther , ``Experimental quantum speed-up in reinforcement learning agents," Nature 591 (2021)

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7113) and Research Group (FG 5), and Red Bull GmbH. The MIT portion of the work was supported in part by AFOSR award FA9550-16-1-0391 and NTT Research.

8.3.4 Delocalized photonic deep learning on the internet's edge

Abstract: Advanced machine learning models are currently impossible to run on edge devices such as smart sensors and unmanned aerial vehicles owing to constraints on power, processing, and memory. We introduce an approach to machine learning inference based on delocalized analog processing across networks. In this approach, named Netcast, cloud-based "smart transceivers" stream weight data to edge devices, enabling ultraefficient photonic inference. We demonstrate image recognition at ultralow optical energy of 40 attojoules per multiply (<1 photon per multiply) at 98.8% (93%) classification accuracy. We reproduce this performance in a Boston-area field trial over 86 kilometers of deployed optical fiber, wavelength multiplexed over 3 terahertz of optical bandwidth. Netcast allows milliwatt-class edge devices with minimal memory and processing to compute at teraFLOPS rates reserved for high-power (>100 watts) cloud computers.

Publication: Alexander Sludds, Saumil Bandyopadhyay, Zaijun Chen, Zhizhen Zhong, Jared Cochrane, Liane Bernstein, Darius Bunandar, P. Ben Dixon, Scott A. Hamilton, Matthew Streshinsky, Ari Novack, Tom Baehr-Jones, Michael Hochberg, Manya Ghobadi, Ryan Hamerly, Dirk Englund, ``Delocalized Photonic Deep Learning on the Internet's Edge,'' Science, 378, 220 (2022)

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8.4. D. Other research advances to which the above advance contributed

8.4.1. Triggered single-photon generation and resonance fluorescence in ultra-low loss integrated photonic circuits

A central requirement for photonic quantum information processing systems lies in the combination of nonclassical light sources and low-loss, phase-stable optical modes. While substantial progress has been made separately towards ultra-low loss, ≤1 dB/m, chip-scale photonic circuits and high brightness single-photon sources, integration of these technologies has remained elusive. Here, we report a significant advance towards this goal, in the hybrid integration of a quantum emitter single-photon source with a wafer-scale, ultra-low loss silicon nitride photonic integrated circuit. We demonstrate triggered and pure single-photon emission directly into a Si3N4 photonic circuit with ≈1 dB/m propagation loss at a wavelength of ≈920 nm. These losses are more than two orders of magnitude lower than reported to date for any photonic circuit with on-chip quantum emitter sources, and >50 % lower than for any prior foundry-compatible integrated quantum photonic circuit, to the best of our knowledge. Using these circuits we report the observation of resonance fluorescence in the strong drive regime, a milestone towards integrated coherent control of quantum emitters. These results constitute an important step forward towards the creation of scaled chip-integrated photonic quantum information systems.

Publication: Ashish Chanana, Hugo Larocque, Renan Moreira, Jacques Carolan, Biswarup Guha, Vikas Anant, Jin Dong Song, Dirk Englund, Daniel J. Blumenthal, Kartik Srinivasan, Marcelo Davanco, ``Triggered single-photon generation and resonance fluorescence in ultra-low loss integrated photonic circuits," physics > arXiv:2202.04615 [see scirate page for discussion] (2022)

Acknowledgement: Acknowledgements We thank Edward Flagg from West Virginia University for helpful discussions regarding the resonance fluorescence results. A.C. acknowledges support under the Cooperative Research Agreement between the University of Maryland and NIST-PML, Award no. 70NANB10H193. J.D.S. acknowledges the program of quantum sensor core technology through IITP (MSIT Grant No. 20190004340011001). Author Contributions M.D. performed electromagnetic design of the hybrid devices. J.C., D.E., R.M., D.J.B., K.S. and M.D. conceptualized the hybrid chip pick-and-place assembly method. J.D.S. provided the molecular beam epitaxy-grown quantum dot sample. R.M. designed and fabricated the Si3N4 photonic circuit chip. H.L. devised and performed post-fabrication adjustments to the Si3N4 on-chip devices. B.G. fabricated the GaAs devices. J.C. and H.L. performed pick-and-place assembly of the hybrid device. V.A. provided superconducting nanowire single-photon detectors. A.S. performed the waveguide propagation loss and single quantum dot characterization measurements, analyzed the data and produced figures for the manuscript. A.S. and M.D. wrote the manuscript, with input from all authors. M.D., K.S., D.J.B., D.E and J.C. supervised the project. All the authors contributed and discussed the content of this manuscript. Additional Information Correspondence and requests for materials should be addressed to M.D. Competing financial interests The authors declare no competing financial interests. D.E. and H.L. acknowledges support from NSF (1936314QII-TAQS) and AFOSR program FA9550-16-1-0391.

8.4.2. Controlled-Phase Gate by Dynamic Coupling of Photons to a Two-Level Emitter

We propose an architecture for achieving high-fidelity deterministic quantum logic gates on dual-rail encoded photonic qubits by letting photons interact with a two-level emitter (TLE) inside an optical cavity. The photon wave packets that define the qubit are preserved after the interaction due to a quantum control process that actively loads and unloads the photons from the cavity and dynamically alters their effective coupling to the TLE. The controls rely on nonlinear wave mixing between cavity modes enhanced by strong externally modulated electromagnetic fields or on AC Stark shifts of the TLE transition energy. We numerically investigate the effect of imperfections in terms of loss and dephasing of the TLE as well as control field miscalibration. Our results suggest that III-V quantum dots in GaAs membranes is a promising platform for photonic quantum information processing.

Publication: Stefan Krastanov, Kurt Jacobs, Dirk R. Englund, Mikkel Heuck, ``Controlled-Phase Gate by Dynamic Coupling of Photons to a Two-Level Emitter," to appear in NPJ Quantum Information (2022)

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9. CONCLUSION

We are developing a new generation of photonic FPGAs (pFPGA) for programmable photonic circuits. At the heart of the pFPGA is a packaged programmable many-mode interferometer. The device is controlled by 20^2 =400 MZI phase shifters, for a total of 800 electrical connections including grounds. This program realized the following advances:

1. Development of the first deterministic error correction algorithms for programmable photonics, self-configuration algorithms that realize these error bounds, and new architectures for programmable photonic meshes that enable asymptotic decreases in error with larger photonic mesh sizes.
2. Development of a universal programmable many-mode interferometer that realizes arbitrary unitary operations on twenty optical modes. The development of this system also enabled new advances in packaging, including the integration of these systems with high-density silicon interposers for efficient electrical interconnects.
3. Development of the first single-chip, end-to-end silicon photonic system for implementing deep neural networks optically, using programmable many-mode interferometers as the core processor for optical matrix-vector algebra. The development of this system realized additional advances in packaging and the development of new algorithms for *in situ* training of machine learning models on programmable photonics.
4. Demonstration of a novel optical edge computing scheme using integrated silicon photonic transceivers, enabling the deployment of large-scale, state-of-the-art machine learning models on low-power edge hardware.

The results from this program have further advanced our work towards realizing "algorithmically error-correcting, intelligent optical materials."

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