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INVESTIGATION OF TECHNICAL PROBLEMS IN
GALLIUM ARSENIDE

Fred H. Eisen, et al

Rockwell International Corporation

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progress made during the six-month period are described in separate sections. Future plans for the next reporting period are also included. This work is being carried out in cooperation with the California Institute of Technology, Cornell University, Stanford University, and the University of Southern California.

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INVESTIGATION OF TECHNICAL PROBLEMS IN GaAs
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1.0 INTRODUCTION

The widespread application of GaAs devices in microwave systems is yet to be realized despite their superior performance characteristics. The lag of reproducibility and reliability in these devices has resulted in low yield and high unit cost. These drawbacks overshadow the advantages in performance, some of which are unique to GaAs devices. For instance, the high electron mobility in GaAs permits the fabrication of FET's operating in frequencies far beyond the cutoff of the bipolar transistor. The combination of high electron mobility in the low field region and the large difference in electron and hole ionization coefficients recently led to the realization of very high efficiency (>30%) GaAs IMPATT devices. In addition, the transferred electron device, which is made possible by the negative differential mobility, is just unattainable from other better-known semiconductors such as silicon or germanium. The urgent need of improved microwave devices for high data rate communication is approaching due to the advent of the digital computer. The currently-available frequency spectrum allocated for communication is nearly filled. It is certain that an improvement in GaAs technology will help to alleviate many device and system difficulties in microwave frequencies beyond X-band and perhaps well into the mm-wave frequencies.

A joint program between the Science Center and several leading universities was conceived and initiated in 1973 to investigate and solve the technological problems in the development of GaAs devices. The IMPATT diode and the Schottky barrier field effect transistor were chosen as the experimental vehicles for the studies of GaAs material and technology. The areas of research relevant to these devices are:

1. Quality evaluation of semi-insulating substrates in terms of electrically active trap densities and crystal dislocations.
2. Growth of ultra-thin epitaxial layers.
3. Formation of low resistivity ohmic contacts.
4. Formation of semi-insulating areas by proton bombardment.
5. Ion implantation to form n-type layers on insulating substrates or device structures.
6. RF measurement on GaAs devices for material characterization and technology evaluation.

The above activities are carried out at the Science Center closely coordinated with the participating universities. Improvement in reliability and yield of microwave devices is anticipated as a direct result of this GaAs technology program.

2.0 PROGRAM GOALS AND TECHNICAL APPROACH

The original program goals and the technical approach were described in Section 2.0 of Report No. SC563.4SATR under Contract No. F19628-74-C-0038. The activities include material growth and characterization, using device structures as experimental vehicles for information extraction.

2.1 Epitaxial Material Growth and Characterization

The goal is to establish material and processing technology required to enhance the yield, the performance, and the reliability of devices.

2.1.1 Ultra-Thin Layer Growth

Methods of growing submicron liquid phase epitaxial GaAs films with rigid tolerance on layer thickness and carrier concentration is to be developed. Initial growth rate of liquid phase epitaxy is retarded by a reduction of the volume of As-saturated Ga between the substrate and the GaAs source.

2.1.2 High-Resistivity GaAs Layers

The objective of this work is to investigate the growth conditions leading to high-resistivity epitaxial GaAs films with low compensation using liquid phase growth. The effect of hydrogen flow rate, dopants, and bakeout temperature of the source material on the carrier concentration and the compensation ratio of the epitaxial films is being studied systematically.

2.1.3 Multi-Layer LPE

Techniques for growing multi-layer device structures with simultaneous control of film thickness and carrier concentration in each layer are the prime objectives of this work. The resulting multi-layer structures will be used in conjunction with preferential etching techniques to form high-power microwave devices. Initial experiments are carried out using special LPE boats with multi-reservoirs.

2.1.4 Material Characterization--Theoretical and Experimental Investigation of the Effect of Material Properties on Device Performance

Schottky barrier gate FET, IMPATT, and Gunn effect devices are to be fabricated using materials prepared during the course of this contract. The information derived from electrical measurements performed on the resulting devices is used as a measure of the quality of the material and the processing technology.

2.2 Semi-Insulating Material

The goal is to establish methods to evaluate semi-insulating GaAs crystals, with the emphasis placed on the effect of deep traps on MESFET's fabricated on such substrates. An n-i-n structure is being considered for experimental investigation of electrically-active trap densities. The effect of various impurities and growth conditions on semi-insulating GaAs is to be investigated by a combination of photoconductivity, resistivity, and thermal activation measurements.

2.3 Ion Implantation

The goal is to investigate the effect of ion beam energy, dosage and species of impurities on the carrier concentration profile of ion-implanted GaAs substrates under various annealing conditions. The effectiveness of the protective caps for the substrate surface during the annealing process is being investigated. A method for control anodization of the GaAs surface for precision stripping has been successfully developed. The controlled stripping technique has added considerably to the ability to characterize the implanted layers.

3.0 RESULTS

3.1 Progress of Epitaxial Material Growth and Material Characterization

3.1.1 Growth of Ultra-Thin Films

3.1.1.1 Progress in the Growth of Ultra-Thin Films. In previous reports we have discussed the necessity of slowing down initial growth rates of films grown from liquid gallium. Figure 3.1-1 shows curves of thickness of epitaxy grown as a function of time in a liquid gallium system where the amount of gallium is approximately 2 cc and the saturation temperature is approximately 660°C to 675°C. Included in this figure are the ranges of thickness grown for fixed-duration times of growth at that temperature in a new system designed and developed under this contract. It is seen that the new system allows a growth time of 60 seconds to obtain epi-layer thickness of approximately 0.25 μ m to 0.5 μ m. The range of variation for that 60-second growth period is due to a number of factors some within our control, others not. For instance, imposed temperature gradient at the liquid-solid interface (presently quantitatively measured by the cooling gas flow) has a marked effect, but so also does the substrate, for substrates from different sources have apparently different influences on growth rate. This is a subject presently slated for investigation.

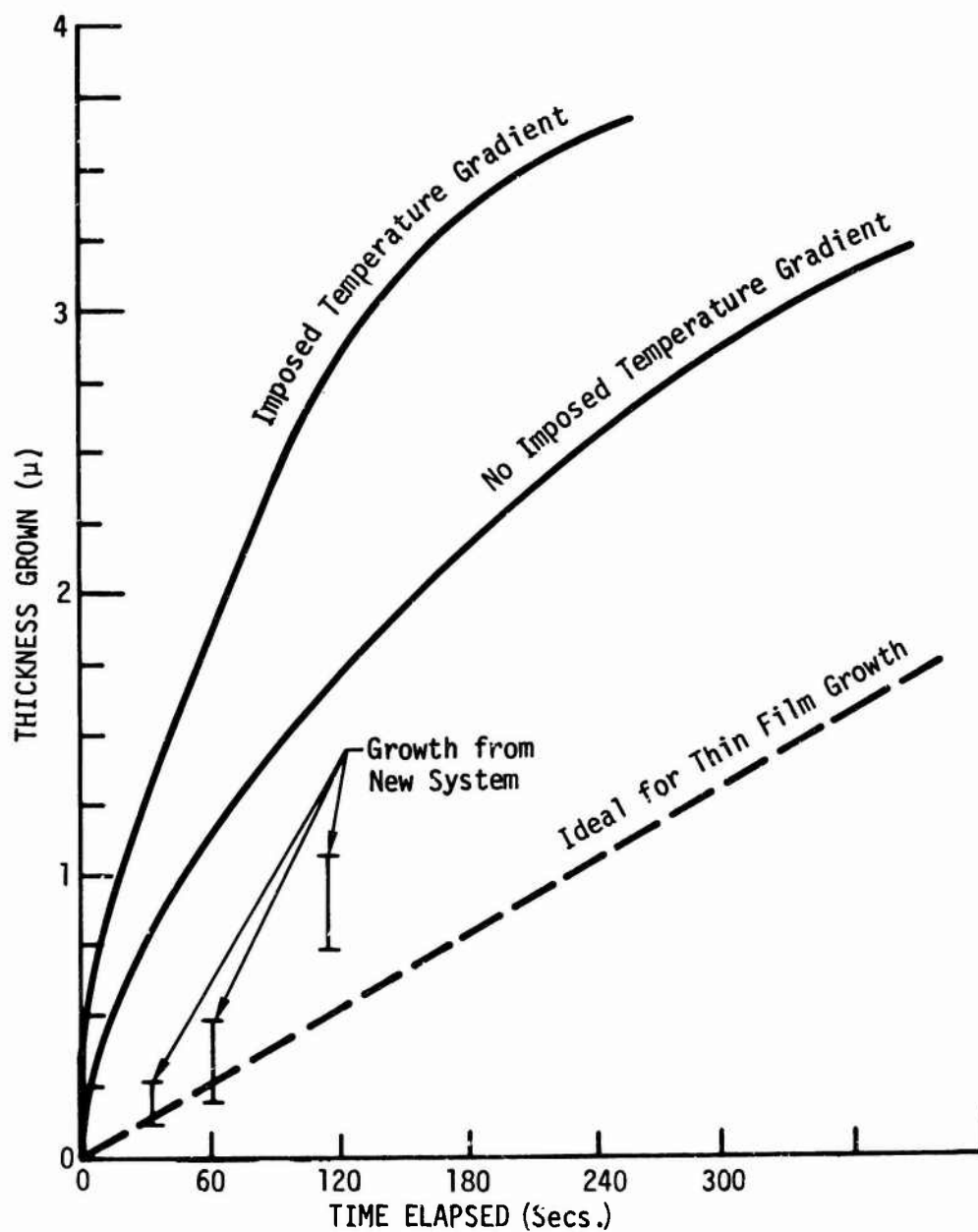


Fig. 3.1-1 Approximate growth rate-time elapsed nature of epitaxial lay deposition.

Figure 3.1-2 shows the carrier concentration versus depth for a layer typical of those grown in the new system. Background impurity of this system has been measured at approximately $1 \times 10^{16}/\text{cm}^3$. While this is not a very pure material, the reason is most probably in the fact that thick graphite walls are present in the boat design since emphasis was on the growth rate rather than the impurity level. However, newer boat designs will contain much less graphite and be easier to clean up. While $1 \times 10^{16}/\text{cm}^3$ is not particularly low, it is below the minimum level contemplated for power GaAs MESFET's--an application for which these layers (of carrier level ≈ 2 to 3×10^{16} and thickness 0.4 to 0.5 μm) are intended. Uniformity of thickness in the layers has improved. It is found to be dominantly influenced by differences locally in the temperature gradient at the growth interface. Figure 3.1-2 also illustrates the degree of uniformity over a layer $1/2" \times 3/4"$ in area.

One final note on results deals with an interesting effect seen in a couple of crystals (out of approximately 25) of a sharp rise in carrier level at the interface of the high conductivity layer and the semi-insulating substrate. It is felt that this is not due to the particular properties of the substrate, but, rather, to the substrate temperature being too far below the gallium temperature upon initial contact. GaAs MESFET's are being made from this layer to investigate the effects of the unusual profile.

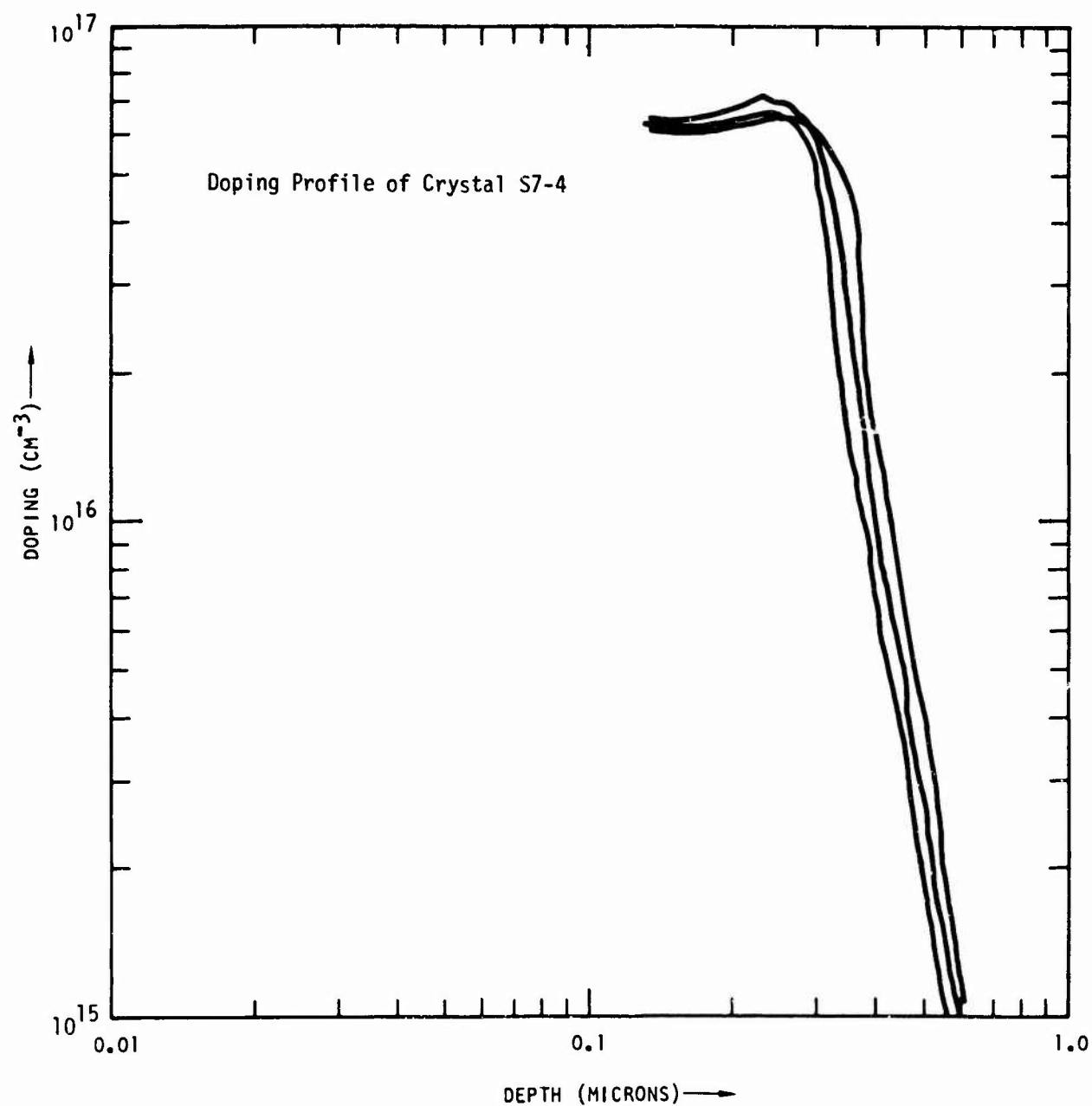


Fig. 3.1-2 Figure illustrating the as-grown doping profile of an FET layer. This layer was grown in a special liquid phase growth system for the growth of ultra-thin layers. The layer took 60 seconds to grow.

3.1.1.2 Factors Affecting the Growth of Thin Layers. In what follows, there is a brief review of some of the basic phenomena occurring in LPE and some basic growth system principles. From this we will build arguments for modification aimed solely at decreasing growth rate.

In Fig. 3.1-3(a) the two full lines show the saturated content of As in gallium at two slightly different temperatures. The system has just dropped in temperature from T_1 to T_2 , and onto the right-hand interface a layer of solid GaAs is growing because of the degrees of super-saturation. The content of arsenic in the gallium drops rapidly at the growth interface and nearby, but drops only slowly out far from the growth interface as shown by the dotted line. If given enough time it would drop to the new saturation level throughout the solution and the system would be in equilibrium. Convection currents shown in the figure aid in the transport of As and the reversion to equilibrium. But, as shown, it is not in equilibrium as the arsenic content is above the level specified by the new temperature. Generally, in growth systems where the growth stimulus is supplied by a drop in temperature, there exists this super-saturated state and this is particularly true for systems where the growth is stimulated by a continuing drop in temperature with time. Only in the case where the rate of temperature drop is very slow is super-saturation and its effects of causing the surface to be non-smooth not observed.

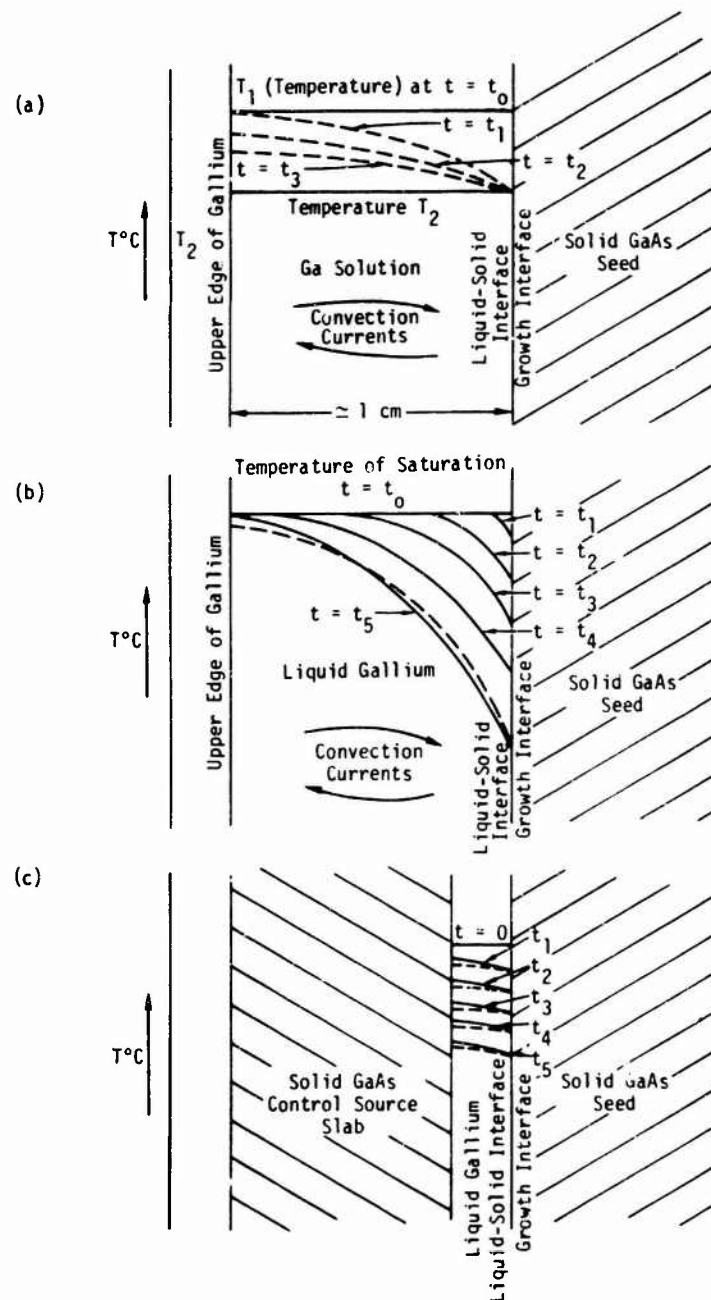


Fig. 3.1-3 The actual temperature profile and liquidus temperature profiles in growth systems: (a) no temperature gradient; (b) a system with imposed temperature gradient; (c) the new modified system for thin layers.

If one imposes a spatial temperature gradient on the growth system at the liquid-solid interface, as in Fig. 3.1-3(b), one immediately obtains some benefits. In Fig. 3.1-3(b) the solid lines are the temperature (local) in the solution. For time $t = t_5$ a dashed line shows the saturation temperature corresponding to the local concentration of arsenic in the gallium melt and this is a sharply decreasing function close to the interface having the same value at the interface as the actual local temperature. Because of the upward gradient of temperature into the solution (away from the interface), there is very little super-saturation in the body of the melt and hence stability. In addition, nucleation density of growth sites on the seed crystal (at time $t = t_1$) is very much more dense than without a temperature gradient and this makes possible extremely smooth layers.¹ Thus stability and smooth, densely-nucleated layers come from the imposition of a temperature gradient and these advantages are accompanied by the not-so-advantageous fact that growth occurs more rapidly as seen in Fig. 3.1-1. The more rapid growth stems from the fact that any attempt to impose a gradient sufficient to ensure stability must cause the overall system temperature to drop rapidly precipitating a lot of GaAs. In addition, convection currents are stimulated or enforced by the temperature gradient speeding the transfer of arsenic to the growth interface.

When one wishes to grow thin films, one has to: (1) slow down the growth rate; (2) maintain a high nucleation density; (3) make sure the solution never gets super-saturated, and (4) reduce the convection currents or at least cause them to be smaller in extent transporting arsenic over much smaller distances. The obvious way to accomplish need (4) provides the way to accomplish all of the above objectives in the manner described in what follows.

Figure 3.1-3(c) illustrates the modification. The thickness of the gallium solution over the seed is drastically reduced from about 1 cm to 1 mm or less.

When considering initial growth rates in thick solutions, the remote parts of the melt are quasi-infinite sources of arsenic which give rise to the arsenic gradients which necessitate the temperature gradients for stability. When the solution is very thin and the volume small, then there is a rapid usage of the arsenic in all parts of the melt, and there is, therefore, no arsenic gradient and, therefore, in turn, no need for high temperature gradients to avoid constitutional instability. Thus, one of the biggest sources of the very rapid growth (e.g., the means to implement a thermal gradient) is greatly reduced but not eliminated altogether as it is necessary in a reduced form to ensure dense nucleation. Thin melts do, in their own way, ensure a dense nucleation because there is a greatly-reduced movement in the

liquid gallium because of the reduction of large-scale convection currents. The initial growth rate is then reduced because of:

- (1) a greatly-reduced temperature gradient at the liquid-solid interface;
- (2) greatly-reduced convection currents, and
- (3) smaller total volume.

Finally, as a second modification, also shown in Fig. 3.1-3(c), the boundary of the solution on the upper side should also be GaAs. This has the following effects: (1) it ensures that the solution is never super-saturated even in that period of cooling down due to imposition of a thermal gradient (however small) before the seed is brought into contact with the melt; and (2) it provides an alternative nucleation site for arsenic atoms coming out of solution thereby diminishing the available GaAs, from an already small volume, for the seed face where we are interested in growing the thin film.

3.1.3 A Practical System. A practical system to accomplish the above has developed into what is essentially shown in Fig. 3.1-4. The sliding vat is stepped on the inside to support a slab of undoped GaAs. The Ga under this slab is of a thickness determined by the step height and this is less than or equal to one millimeter. The thermal gradient is applied through a gallium reservoir and a thick graphite piece being, therefore, a lot smaller than normal at

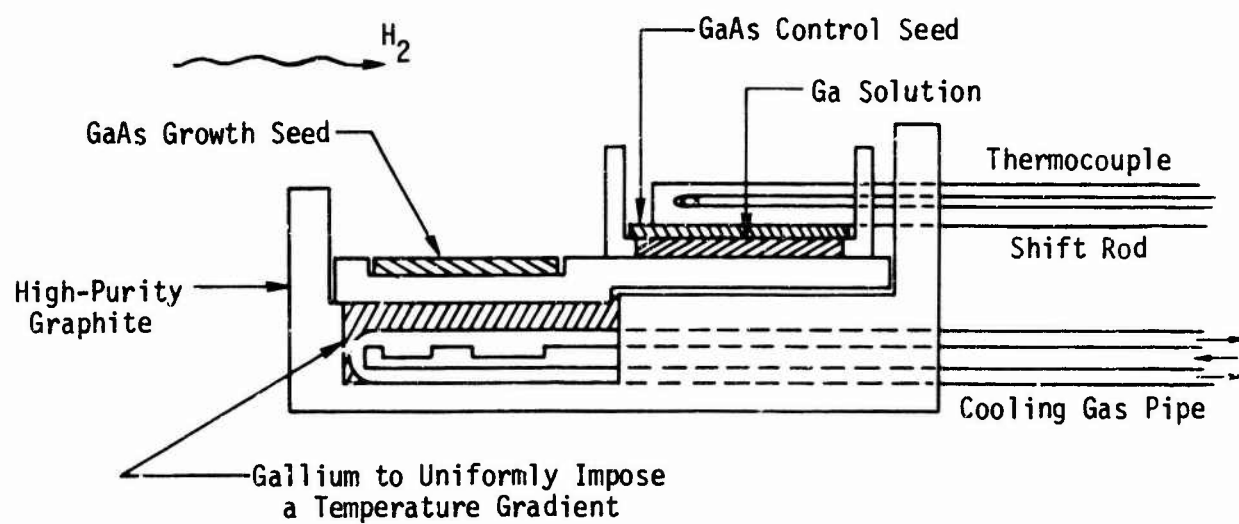


Fig. 3.1-4 A practical system incorporating a thin melt configuration for improving growth rate control.

the GaAs seed. The overall temperature drop due to the cooling is usually only about two or three degrees in a 60-second growth.

3.1.2 Growth of High-Resistivity GaAs Layers

Summary of Work: The following lists the aspects of growing epitaxial layers of GaAs that have been investigated during the six-month period reported:

1. The effects of chromium doping in the melt both as a function of activity (concentration) and of temperature of growth.
2. The effects of bakeout and bakeout temperatures and times upon the grown layers.
3. The effects of hydrogen flow rate on the properties of the grown layers.
4. The properties of oxygen-doped epitaxial layers.

3.1.2.1 Properties of Chromium-Doped Layers. During the first quarter, the work was concentrated on the finding of suitable growth conditions for growing Cr-doped SI epitaxial GaAs. Thirty-five GaAs layers were grown at initial growth temperatures ranging from 700 to 850°C, and with different concentrations of Cr in the Ga solution. The highest resistivity of the epitaxial layer obtained was 224 Ω -cm at a growth temperature of 775°C with 0.7% mole percent of Cr in the melt. All 35 layers were grown with 0.6 liter/min of hydrogen flow rate and 780°C/hr cooling rate except for growth number 419 which was grown with a cooling rate of 3300°C/hr.

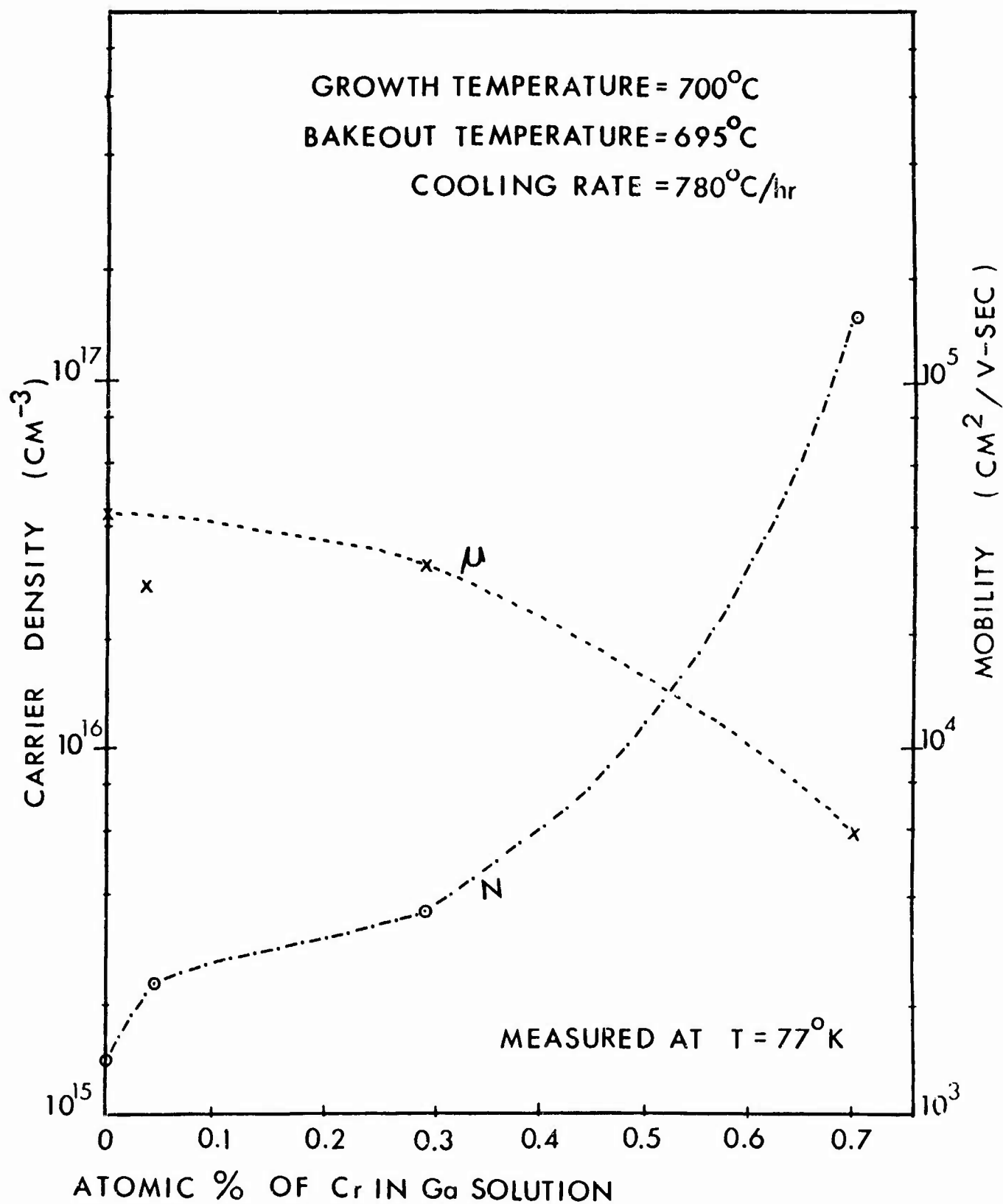


Fig. 3.1-5 Carrier density and mobility vs atomic percentage of Cr in the Ga melt for epi-layers grown at T = 700°C.

Table 3.1-1 Characteristics of Liquid Phase Epitaxial GaAs Prepared Under Various Growth Temperatures

Growth No.	Growth Temp.* (°C)	Mobility (cm ² /V-sec) at 300°K	Carrier Con. (cm ⁻³) at 300°K	Resistivity (Ω-cm) at 300°K	Conductivity Type
401	700	6350	1.14×10^{15}	0.86	n
402	750	7338	7.01×10^{14}	1.22	n
403	775	5140	1.64×10^{14}	7.41	n
405	785	300	3.99×10^{14}	26.9	p
404	800	369	4.6×10^{14}	36.8	p
303	700	3993	2.35×10^{17}	6.66×10^{-3}	n
310	750	2409	6.53×10^{14}	3.91	n
315	775	390	5.65×10^{13}	2.84	p
305	800	378	1.45×10^{14}	11.4	p
311	850	393	2.58×10^{15}	6.17	p

Undoped

0.7 atom percent of Cr in the melt

* Other growth conditions: H₂ Flow Rate: 0.6 liter/min.
Cooling Rate: 13°C/min.

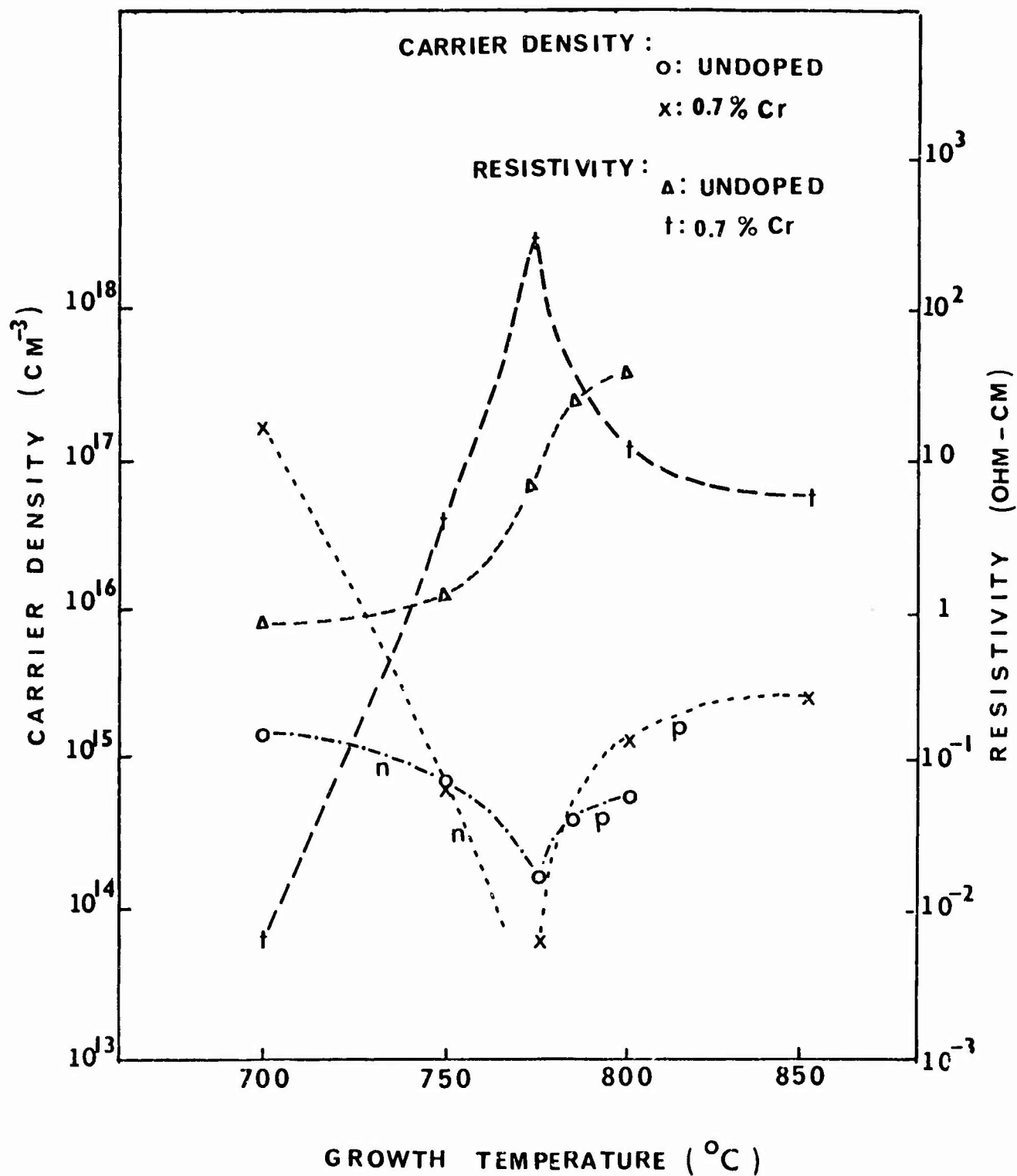


Fig. 3.1-6 Carrier density and mobility vs growth temperature for undoped epi-layers and epi-layers with 0.7 atomic % of Cr in the Ga melt.

For the first series of seven growths, the initial growth temperature was fixed at 700°C, and the mole fraction of Cr in the melt was varied from 0.05 to 0.7%. Under these conditions, the carrier concentration increased with the amount of Cr in the Ga solution (Fig. 3.1-5). Then, with a fixed concentration of Cr in the melt (0.7%), the growth temperature was varied from 700 to 850°C. The carrier concentration decreased from 10^{17} cm^{-3} at 700°C to 10^{14} cm^{-3} at 750°C. When the growth temperature was raised above 800°C, the layers changed to p-type, and the carrier concentration increased in the range of 10^{16} cm^{-3} . When the growth temperature was lowered to 775°C, a layer grown from the same melt appears to be semi-insulating with a carrier concentration of 10^{13} cm^{-3} and a resistivity of 284 $\Omega\text{-cm}$ (Table 3.1-1, Fig. 3.1-6).

In order to investigate the effect of Cr on the electrical properties of the GaAs epi-layers grown under these growth conditions, 10 layers were then grown at 775°C without Cr in the melt. For these layers, the carrier concentrations were all in the range of 10^{13} cm^{-3} and the conductivity type of the layers changed from n-type to p-type as the growth temperature was increased above 785°C (Table 3.1-1, Fig. 3.1-6).

From the above results, the highest resistivity layer was grown at 775°C; therefore, the growth temperature was then fixed at this

value and 10 layers were grown with different Cr concentrations in the Ga solution (0.02, 0.1, and 0.7%). The carrier concentration initially increased with Cr concentration, but then decreased during a series of growths at one value of Cr concentration as shown in Fig. 3.1-7.

Discussion: The amount of experimental work above is large and what emerges from it is summarized in what follows:

1. The first point is that the undoped layers pass through a point of almost complete compensation at 775°C becoming p-type at temperatures of growth above that.
2. Chromium doping has the effect of increasing the number of donors for low temperatures of growth but has little or no influence on the transition to p-type at a temperature of approximately 775°C.
3. From points (1) and (2) it is reasonable to ascribe to chromium a shallow donor behavior at low temperatures of growth with possibly a segregation coefficient greater than 1. But it is most probably not the source of the compensating acceptor which makes its presence felt at higher temperatures of growth. This could be oxygen as oxygen has been detected in these crystals in large quantities by mass spectrographic analysis (see Table 3.1-2), and oxygen has been found to behave as an acceptor in a previous study.

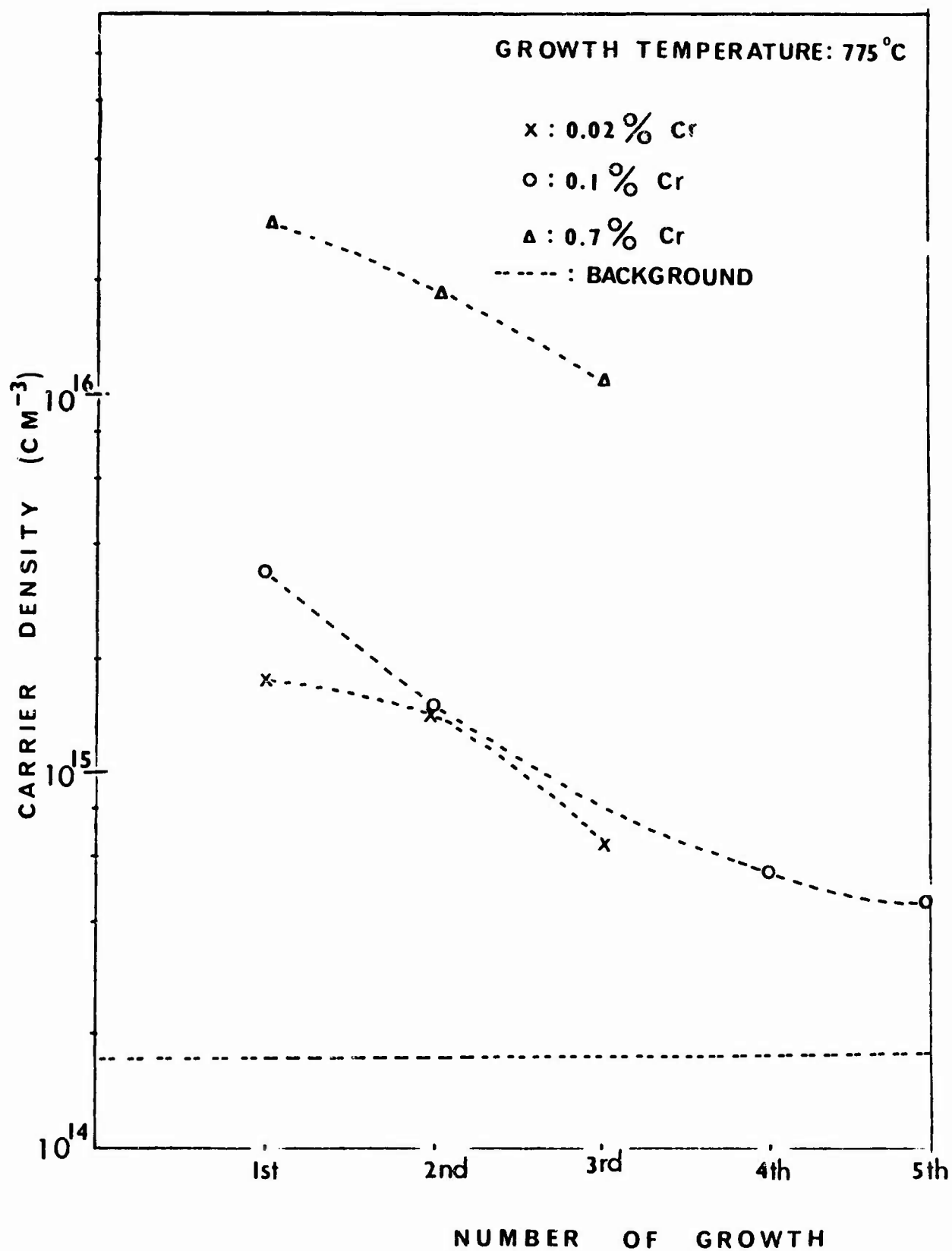


Fig. 3.1-7 Carrier density for three series of growth with different concentrations of Cr in the Ga melt.

Table 3.1-2
Bell & Howell Mass Spectrometric Analysis of GaAs
Source Material and Epi-Layers

Element ¹	GaAs Source	Growth #434 ² (ppm atomic)	Growth #435 ²
B	0.18	1.0	0.3
C	6.4	9.8	32.0
N	1.5	1.6	5.1
O	9.0	80.0	26.0
F	0.50	1.2	1.8
Al	0.76	2.5	3.6
Si	0.97	3.1	4.8
Pb	0.90	N.D.	N.D.
S	0.98	1.5	3.0
Cl	0.70	1.5	1.0
K	2.70	1.1	3.2
Ca	0.28	1.2	N.D.
Cr	0.22	2.1	2.6
Fe	0.60	1.3	1.2
TOTAL	26.0	107.9	84.6

¹GaAs spectrum interferes with Na lines

²Electrical properties at 300°/77°K

#434 6510/22,900 (cm²/v-sec); 7.2/5.5×10¹⁵ (cm⁻³)

#435 4420/12,200 (cm²/v-sec); 3.2/1.9×10¹⁶ (cm⁻³)

3.1.2.2(a) The Effects of Bakeout Times and Temperatures. From the results of the first quarter, it has been found that some of the electrical properties of the epitaxial layer are a function of the bakeout temperature.

The effect of bakeout temperatures at 600 and 800°C on the electrical properties of epitaxial layers, at a fixed saturation temperature, are shown in Table 3.1-3 together with other growth conditions.

In the results of Table 3.1-3, the changes in the electrical properties of the epi-layers are mainly due to the long period of bakeout. The saturation and growth temperature has little effect on these changes, since it appears to be equivalent to a short-term bakeout and is, anyway, the same in both instances. The incorporation of impurities into the solution is mainly determined by the bakeout conditions.

The incorporation of impurities into the solid and the role they adopt in the solid is a function of the bakeout history of the solution (i.e., its impurity content), and of the growth temperature as well.

3.1.2.2(b) The Measured Effects of Growth Temperature. A number of growths were performed on a gallium melt when the bakeout of the tube and contents was performed at the temperature of growth;

Table 3.1-3
The Effect of Bakeout Temperature on GaAs Epi-Layers

Growth No.	Bakeout Temp. (°C)	Saturation Temp. (°C)	H ₂ Flow Rate (ℓ/min)	Carrier Density (cm ⁻³) at 300°K	Mobility (cm ² /V-sec) at 300°K	(N _A + N _D) (cm ⁻³)	Resistivity (ohm-cm)
503	600	600	1.0	2.5 × 10 ¹⁵ (n)	5683	7.48 × 10 ¹⁵	0.44
504	800	600	1.0	1.21 × 10 ¹⁵ (p)	270	2.0 × 10 ¹⁷	19.5

Table 3.1-4
The Effect of H₂ Flow Rate on GaAs Epi-Layers

Growth No.	Bakeout Temp. (°C)	H ₂ Flow Rate (ℓ/min)	Carrier Density p (cm ⁻³) at 300°K	Mobility μ _{300°K} (cm ² /V-sec)	N _D /N _A	N _A + N _D (cm ⁻³)	Resistivity (ohm-cm)
409	775	0.6	3.5 × 10 ²⁴	383	0.96	1.5 × 10 ¹⁶	46.6
505	775	1.0		Depleted			
508	775	1.2	2.95 × 10 ¹⁴	227	0.999	5 × 10 ¹⁷	93.4
404	800	0.6	4.6 × 10 ¹⁴	369	0.96	1.7 × 10 ¹⁶	36.8
504	800	1.0	1.2 × 10 ¹⁵	270	0.994	2 × 10 ¹⁷	19.1

i.e., the saturation period was the only bakeout. By analyzing the free carrier density and Hall mobility data,^{2,3} the residual donor and acceptor concentrations (N_D and N_A) were obtained. The influence of growth temperature on N_A and N_D is shown in Fig. 3.1-8.

The important impurities in the growth system are Si, C, and O (as shown in Table 3.1-2). Both Si and C can enter the crystal lattice either as donors or acceptors. It is known that oxygen acts as a deep level impurity in melt-grown GaAs, and in LPE GaAs oxygen acts as a shallow donor when the temperature of growth is less than 750°C.⁴ From Fig. 3.1-8, the transition from n-type to p-type at 775°C may be due to the dependence of the relative compensation between these impurities on the growth temperature. Silicon is incorporated predominantly as an acceptor at low temperatures, whereas at high temperatures it is incorporated as a donor.^{4,5} Therefore, the amphoteric behavior of Si impurity cannot be used to explain this transition. The transition may instead be due to the amphoteric behavior of carbon or to reduced oxygen concentration at higher temperatures.

3.1.2.3 Effects of H_2 Flow Rate. Table 3.1-4 shows that as the H_2 flow rate increases, both N_D/N_A and $(N_A + N_D)$ increase. Therefore, by choosing the proper growth conditions (bakeout temperature and H_2 flow rate) we can, in principle, obtain a heavily compensated epitaxial layer with N_D/N_A close to unity, a very low

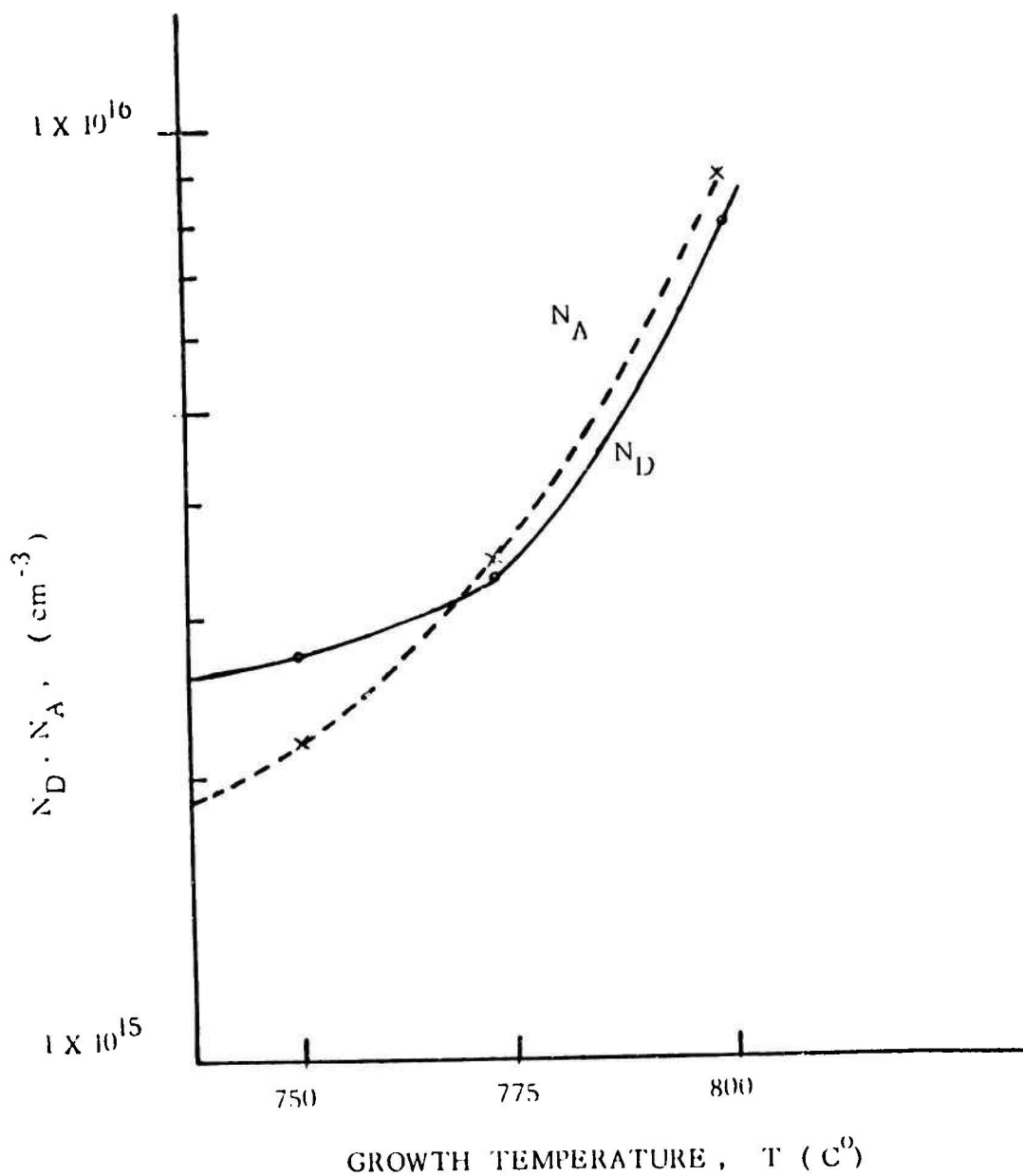


Fig. 3.1-8 Dependence of residual donor and acceptor concentration on growth temperature. Bakeout temperature = growth temperature. H_2 flow rate = 0.6 liter/min.

free carrier density, and a high-resistivity epi-layer.

The effect of H_2 flow rates at 0.6 l/min to 1.2 l/min is shown in Table 3.1-4. There seems to result from increased hydrogen flow a greatly increased density of impurities almost equally divided among donors and acceptors.

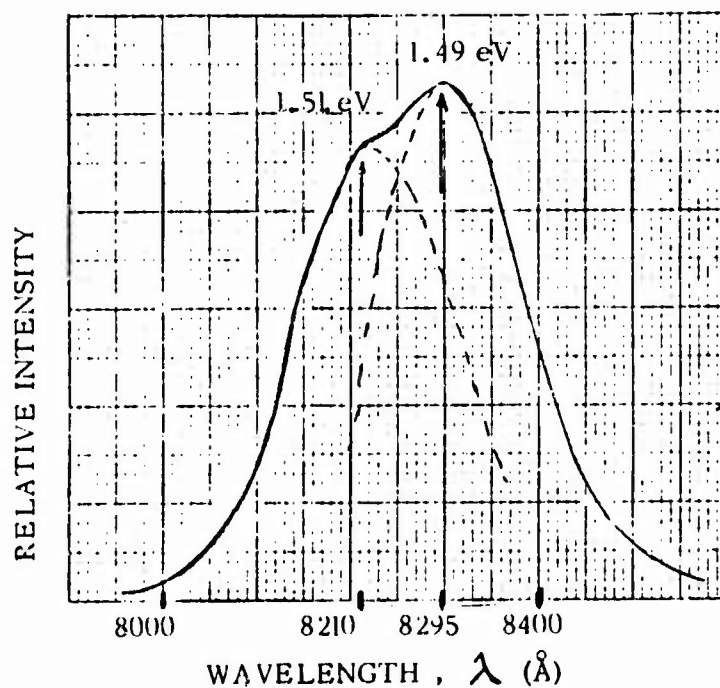
3.1.2.4 Properties of Oxygen-Doped Epitaxial Layers. For the study of oxygen doping, eight epitaxial layers have been grown thus far. Oxygen was added to the Ga solution by using 0.12 mole percent of Ga_2O_3 (99.9999%). The properties of these layers are shown in Table 3.1-5. Figure 3.1-9 shows the photoluminescence spectrum of an oxygen-doped epitaxial layer as measured at 77°K.

The effects of adding Ga_2O_3 to the Ga solution can be seen from Table 3.1-5 where both N_A/N_D and $(N_A + N_D)$ are decreased! From the ratio of $n_{300^\circ K}/n_{77^\circ K}$ and Fig. 3.1-9, it can be concluded that oxygen introduces a shallow donor level in LPE GaAs instead of deep level traps as in melt-grown GaAs. The photoluminescence spectrum shows that the donor level is about 50 meV below the conduction band. These layers have been grown at lower temperatures and the role of oxygen at higher temperatures of growth has yet to be established.

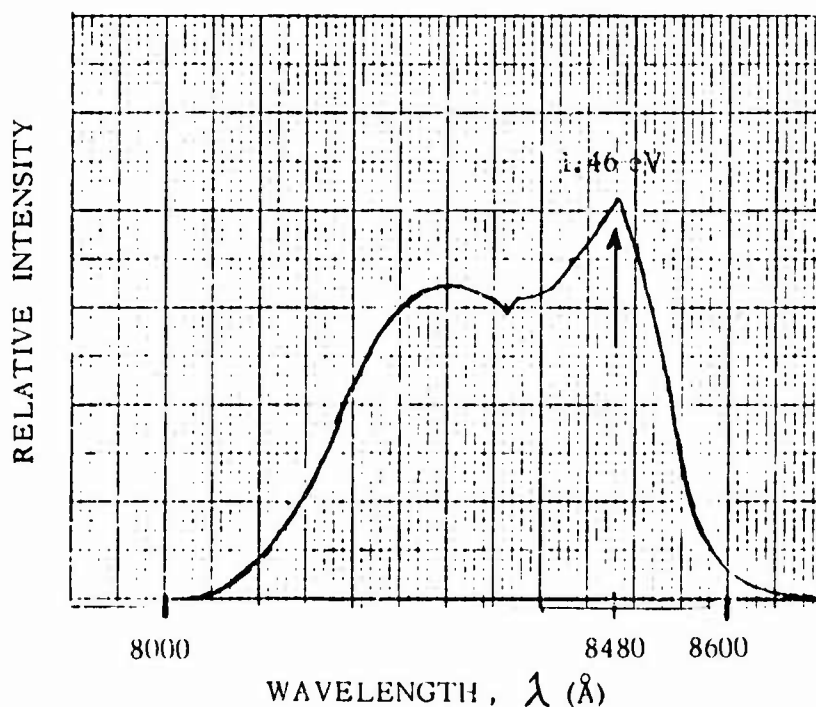
Table 3.1-5
Results of O₂ Incorporation in GaAs Epi-Layers

Growth No.	Dopant	Bakeout Temp. (°C)	Growth Temp. (°C)	Mobility $\mu_{300^\circ\text{K}/\mu_{77^\circ\text{K}}}$	Carrier Density $n_{300^\circ\text{K}}/n_{77^\circ\text{K}}$	N_A/N_D	$(N_A + N_D) (\text{cm}^{-3})$	Resistivity (ohm-cm)
702	Undoped	775	650	8558/62704	1.45×10^{15} 1.28×10^{15}	0.6	5.12×10^{15}	0.5
703	Undoped	790	775	6646/21241	8.5×10^{14} 5.58×10^{14}	0.89	9.47×10^{15}	1.1
704	Ga ₂ O ₃	700	700	8402/61895	1.13×10^{15} 9.7×10^{14}	0.38	2.15×10^{15}	0.66
705	Ga ₂ O ₃	700	700	8282/60733	1.09×10^{15} 9.86×10^{14}	0.37	2.2×10^{15}	0.69
706	Ga ₂ O ₃	775	700	7474/46149	1.95×10^{15} 1.59×10^{15}	0.41	3.8×10^{15}	0.43
707	Ga ₂ O ₃	800	700	8696/62665	6.58×10^{14} 6.51×10^{14}	0.39	4.25×10^{14}	1.09
708	Ga ₂ O ₃	800	700	9694/70100	1.18×10^{15} 1.05×10^{15}	0.21	1.63×10^{15}	0.55

* H₂ flow rate = 0.6 l/min.



(a) Typical undoped n - type layer (Growth No. 403)



(b) Oxygen-doped n-type layer (Growth No. 708)

Fig. 3.1-9 Photoluminescence spectra of GaAs epitaxial layers.
 (a) Typical undoped n-type layer (Growth No. 403)
 (b) Oxygen-doped n-type layer (Growth No. 708)

3.1.3 Multi-Layer LPE

A liquid phase epitaxial growth chamber was modified to accept a multi-compartment Ga bowl for the preparation of multi-layer IMPATT device structures. The apparatus was designed to enable the consecutive growth of n , n^+ , and p^+ layers in one run. Two samples with $n/n^+/n/p^+$ substrate structure were prepared. They are awaiting further evaluation of carrier concentration and the thickness of the active n -layer on the top surface.

3.1.4 Theory and Results in Device Measurement

3.1.4.1 Results in IMPATT Theory and Measurements. In the first quarterly report, the analysis of amplifier measurements was reviewed from the point of view of extracting from experimental data those diode properties directly related to material parameters. The theoretical development was developed sufficiently to show how the diode microwave admittance affected the amplifier performance. At this stage of development, however, it is not clear how to separate the parasitic elements of the diode mounting and of the amplifier circuit from the desired diode parameters. A very useful technique for separating these parasitic elements is that of perturbing the diode parameters.² For example, the amplifier characteristics may be measured as a function of the dc current or the microwave power level.

To illustrate in detail how the perturbation technique can be used for determining the effective width of the avalanche zone of the diode, consider the equivalent circuit of the diode shown in Fig. 3.1-10 since the amplifier yields the admittance more directly, consider

$$Y = \frac{1/r_d}{1+Q_d^2} + j \frac{\omega C_d}{1+Q_d^2} = G_d + jB_d \quad (1)$$

where the diode Q-factor is $Q_d^{-1} = \omega C_d r_d$. As one varies the diode current, for example, one obtains the quantities dB_d/dI and dG_d/dI . Taking these derivatives from the conductance and susceptance terms of Eq. (1) and considering the limit where $Q_d^{-1} \rightarrow 0$ one obtains the relation

$$\lim_{Q_d^{-1} \rightarrow 0} \left\{ \frac{dB_d/dI}{dG_d/dI} \right\} = \frac{d(C_o/C_e)/dI}{-\omega_o C_o (dr_d/dI)} \quad (2)$$

where C_o is geometrical capacitance, and C_e represents the electronic part. From the expression for the diode impedance the ratio of Eq. (2) can be shown to be

$$\lim_{\substack{Q_d^{-1} \rightarrow 0 \\ B \ll 1}} \left\{ \frac{dB_d/dI}{dG_d/dI} \right\} = \frac{\sin\psi + \frac{x_1}{w-x_1} \psi + (1-\cos\psi)|\cot\xi|}{(1-\cos\psi) - |\cot\xi| \left(\sin\psi + \frac{x_1}{w-x_1} \psi \right)} \quad (3)$$

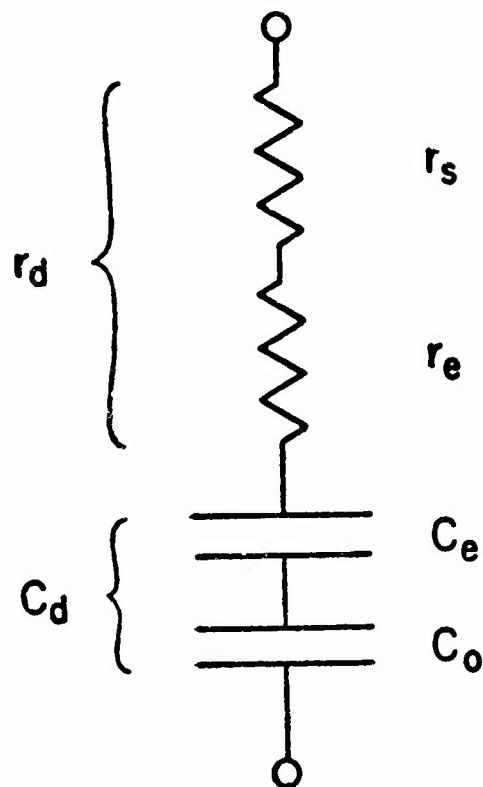


Fig. 3.1-10 Equivalent series circuit of avalanche diode with frequency-dependent electronic elements. C_o represents the geometrical capacitance, r_s is the series resistance, and the subscripts d and e stand for diode and electronic part, respectively.

where the transit angle $\psi = \omega(w-x_1)/v_s$ and $\xi \approx \omega M\tau_1$. Except for conditions high excitation or very low frequency $|\cot \xi| \ll 1$ and Eq. (3) reduces to

$$\lim_{\substack{Q_d^{-1} \rightarrow 0 \\ B \ll 1}} \left\{ \frac{dB_d/dI}{dG_d/dI} \right\} = \frac{\sin \psi + \frac{x_1}{w-x_1} \psi}{1 - \cos \psi} = Q_{P_0} \quad (4)$$

where Q_{P_0} is the Q referred to in the last report. Finally, the left side of Eq. (4) may be expressed in terms of the amplifier "Q" and the frequency "pushing":

$$Q_{P_0} = \frac{Q_x \frac{2}{\omega_0} \frac{d\omega}{dI}}{(d|Q_x/Q_a|dI)} = \frac{\sin \psi + x_1(w-x_1)^{-1} \psi}{1 - \cos \psi} \quad (5)$$

Equation (5) was derived by perturbing the diode parameters with varying bias current. Another and equally useful perturbation can be effected by varying the ac voltage or equivalently the microwave input power to the amplifier. The amplified power is related to the diode voltage by

$$\Delta P = P_o - P_{in} = V_d^2 G_d \quad (6)$$

and here P_o includes the circuit and parasitic losses as well as the power delivered to the load. In most cases, however, the circuit and parasitic losses will be small. Equation (5) may now be

given in terms of derivatives taken with respect to ΔP

$$Q_{P_0} = \frac{Q_x (2/\omega_0 [d\omega/d(\Delta P)])}{[d|Q_x/Q_a|/d(\Delta P)]} = \frac{\sin\psi + x_0 (w-x_1)^{-1}\psi}{1-\cos\psi} \quad (7)$$

A cursory examination of Eqs. (5) and (7) shows that an ideal minimum phase distortion amplifier (i.e., an amplifier with Q_{P_0} less than 1.0) cannot be made with any diode for which the avalanche zone width is greater than 20% of the drift zone. Therefore, it is advantageous to have a large asymmetry of the electron and hole ionization rates and, furthermore, large bandgap materials will also be advantageous. In the larger bandgap materials the field dependence of the ionization rates is larger because the ionization threshold tends to increase faster than the optical phonon energy requiring the carriers to diffuse upwards to ionizing energies.

Measurements taken on silicon avalanche diodes with uniformly-doped n-type active layers show that the avalanche zone occupies 40% of the depletion layer (see Fig. 3.1-11). A complementary p-type active layer would have an avalanche zone about half of this value with consequent improvement in amplifier performance.

Measurements on GaAs Schottky barrier diodes with uniformly-doped n-type active layers show contradictory behavior for the current and power perturbations instead of expected consistency. Data for

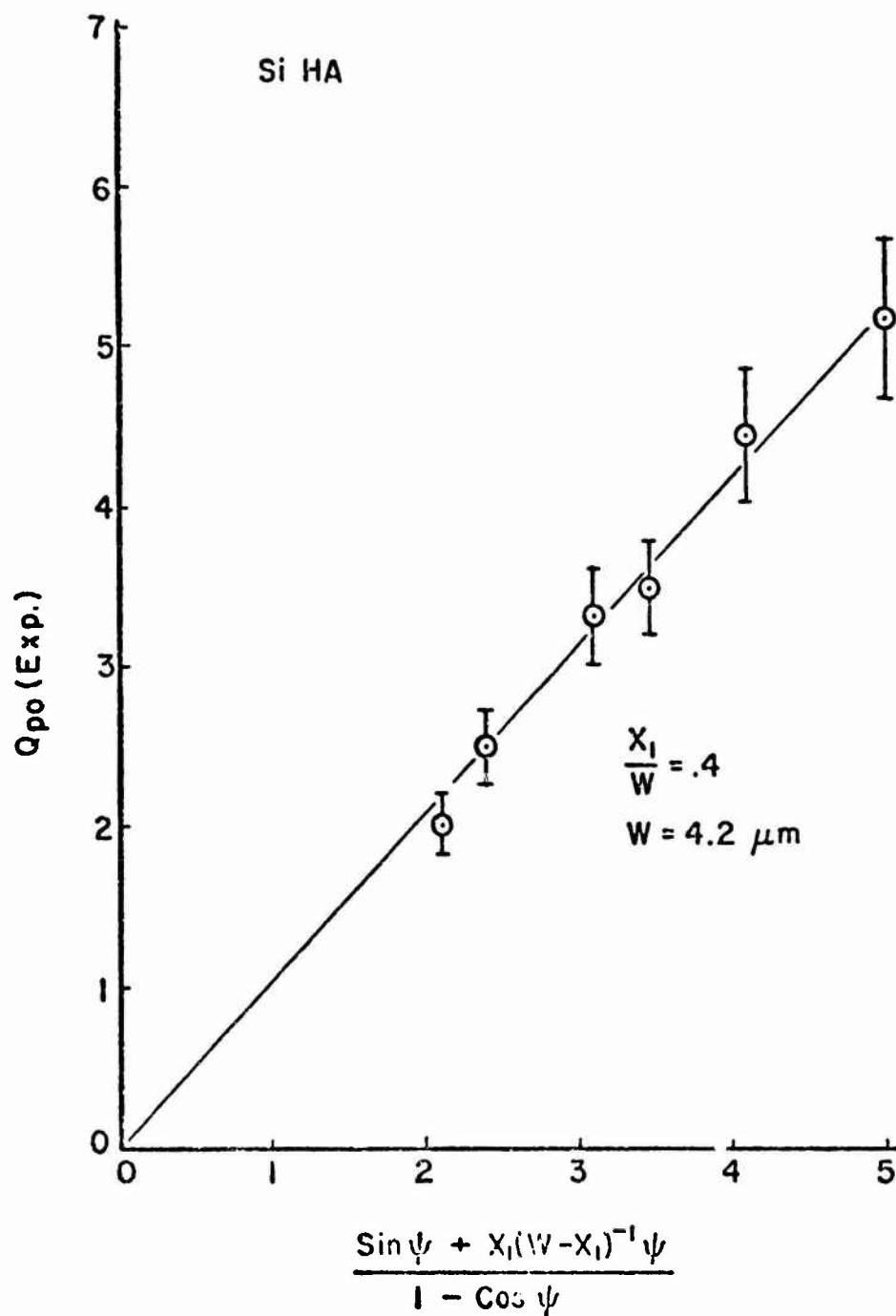


Fig. 3.1-11 Measurement of avalanche zone width in a silicon diode with an n-type active layer.

two GaAs diodes from Raytheon are shown in Figs. 3.1-12 and 3.1-13. These diodes have uniformly-doped n-type active layers and the junctions are Schottky barriers. In addition, these diodes have an undepleted region of the active layer of the order of $1\mu\text{m}$ at breakdown.

Considering that the current and power perturbations are found to give consistent results in silicon diodes, the first explanation should be sought in the obvious difference in the construction of the GaAs diodes; that is, the relatively large undepleted zone of the active layer. Additional complicating factors in the GaAs diodes are a greater variation of the breakdown voltage with temperature as well as a saturation velocity of the electrons that varies as $1/T^{1/2}$. This relatively large temperature variation of the saturation velocity is a consequence of the losses to acoustic phonons becoming comparable to intervalley scattering at higher energies.

The temperature variation of the breakdown voltage leads to a widening of the depletion layer as the current is increased. This increase in w may overcompensate the frequency variation of gain due to the current-dependent electronic reactance, thus yielding a net positive increase in frequency with current. Qualitatively this argument seems to be a valid one, but quantitatively the degree of current-frequency pushing observed as a function of

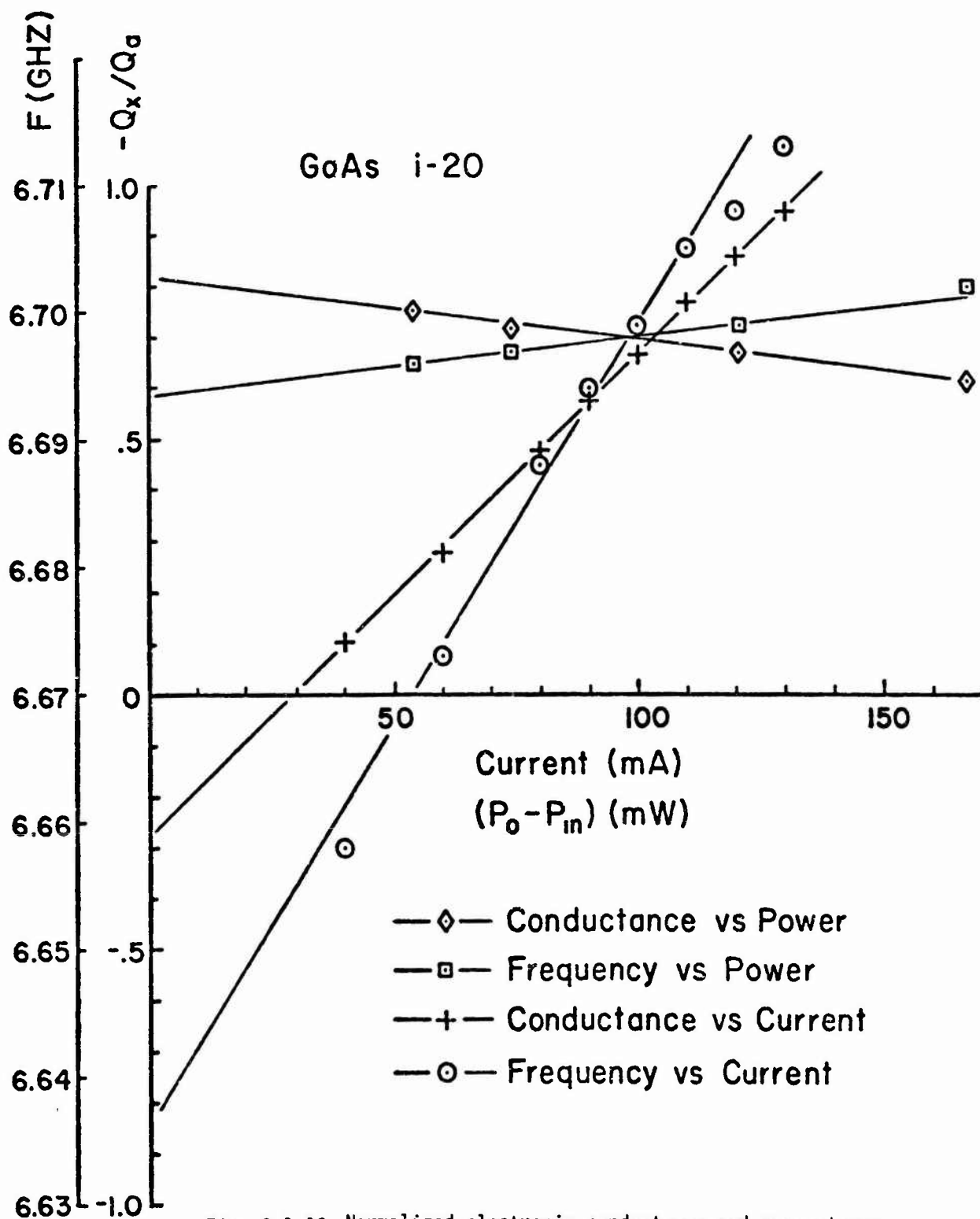


Fig. 3.1-12 Normalized electronic conductance and susceptance as a function of bias current and power level of an "N" GaAs diode.

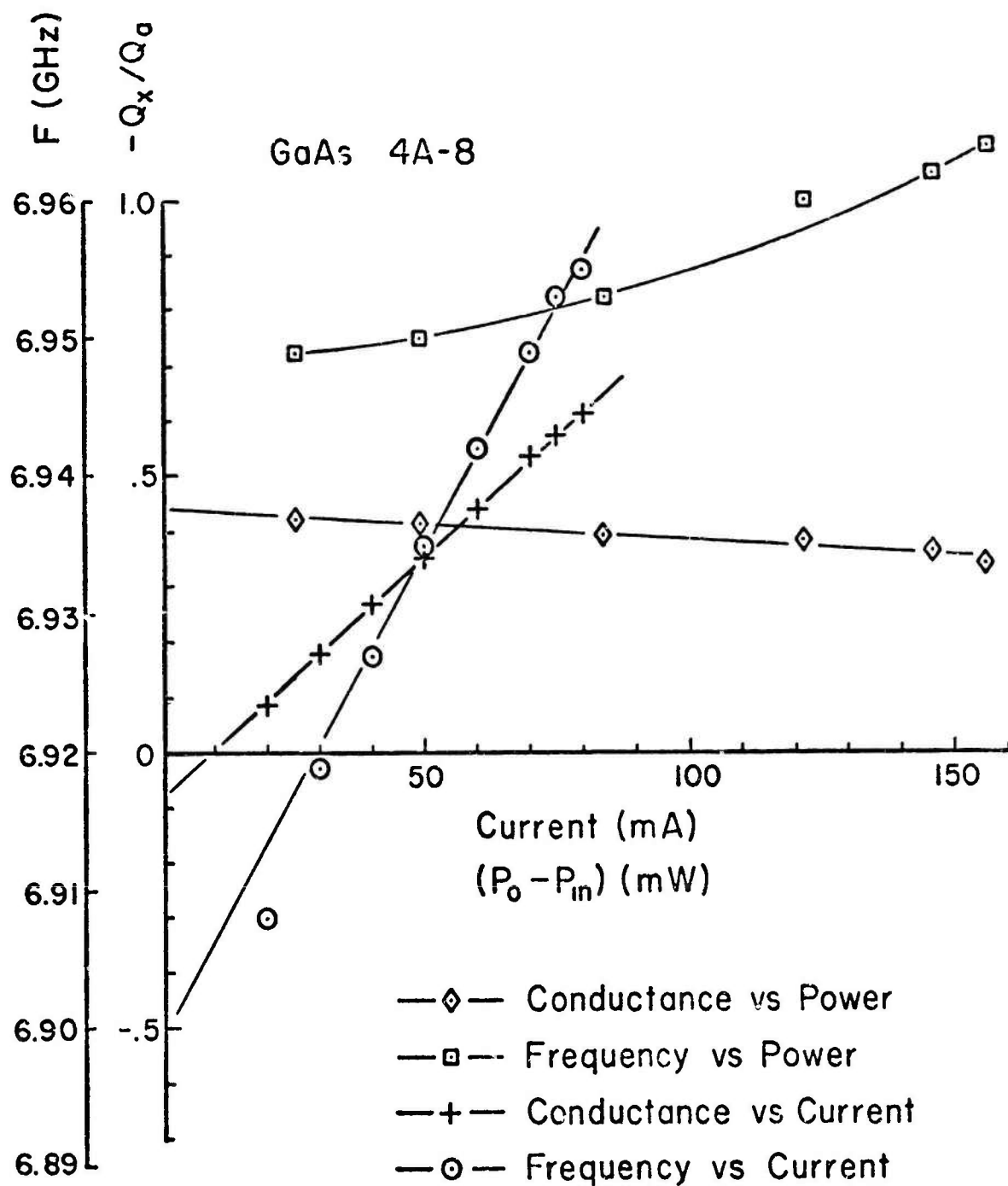


Fig. 3.1-13 Normalized electronic conductance and susceptance as a function of bias current and power level of an "N" GaAs diode.

current cannot be made compatible with the tuning effects observed as a function of the microwave power level. Thus the temperature variation of the depletion width does not by itself afford an explanation of the data. A further possibility to be examined is the impedance of the low field region of the active layer.

An attempt was made to eliminate the uncertainty that may be caused by the undepleted part of the active layer by fabricating some diodes in which the entire active layer was depleted. Although the material used had a buffer layer between the substrate and the active layer, a very sharp rise in saturation current was observed at "punch-through." This current rise did not permit taking the diodes to avalanche breakdown.

At this point it appears that the undesirable electrical properties of the interface present a major obstacle in the analysis of diode structures as well as in obtaining desirable system performance.

3.1.4.2 High Field Generation at Interface Defects. Non-punch-through IMPATT and Read structures are made because generation centers are commonly observed at the interface of the active layer and the substrate. Punch-through diodes tend to burn out more easily and the burnout mechanism is quite likely associated with localized generation at interface defects and filamentary instabilities. This interface problem has been observed in silicon avalanche devices and has been overcome by diffusing the electrical

interface between active layer and substrate out beyond the physical interface. It is felt that the same technique can be applied successfully to GaAs.

Outdiffusion is being tried both at the Science Center and Cornell on pieces of single wafers. The Science Center will encapsulate the wafer to avoid surface deterioration while the Cornell group has set up a closed tube equilibrium vapor apparatus for high-temperature annealing.

The effects of interface defects on punch-through diodes were mentioned in Section 3.1.4.1. Detailed measurements on those diodes are given in this section. The wafer used had been grown for LSA operation. A tin-doped buffer layer with a concentration in the range of $10^{18}/\text{cm}^3$ was grown on a substrate by liquid phase epitaxial growth. Then an active layer of $\sim 150\mu\text{m}$ is grown by constant temperature gradient LPE with a concentration ranging from $\simeq 4 \times 10^{14}/\text{cm}^3$ near the buffer layer to $\sim 2 \times 10^{15}/\text{cm}^3$ near the surface.

A set of dimples are etched in the active layer to within several microns of the buffer layer. Figure 3.1-14 shows the dimple-etched wafer with gold dots sputtered onto the dimples and in between to provide non-punch-through reference diodes. Figures 3.1-15(a) and 15(b) show the I-V characteristic of a non-punch-through



Fig. 3.1-14 GaAs wafer containing punch-through diodes (dimpled structure) and non-punch-through diodes. Diode numbering is by row-column.

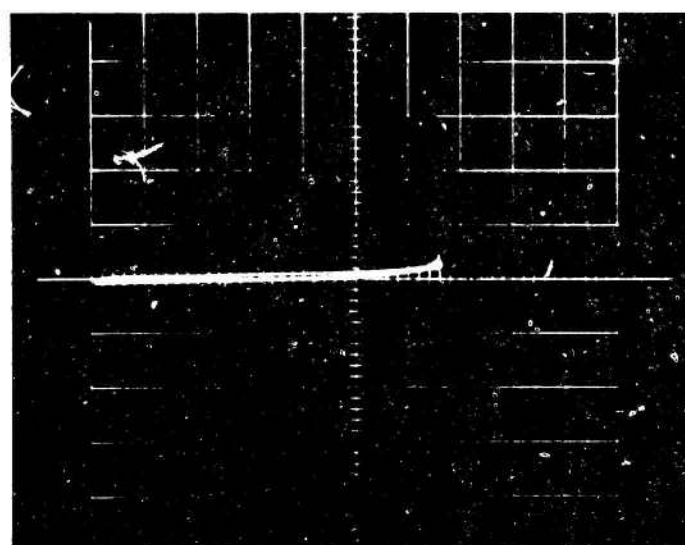
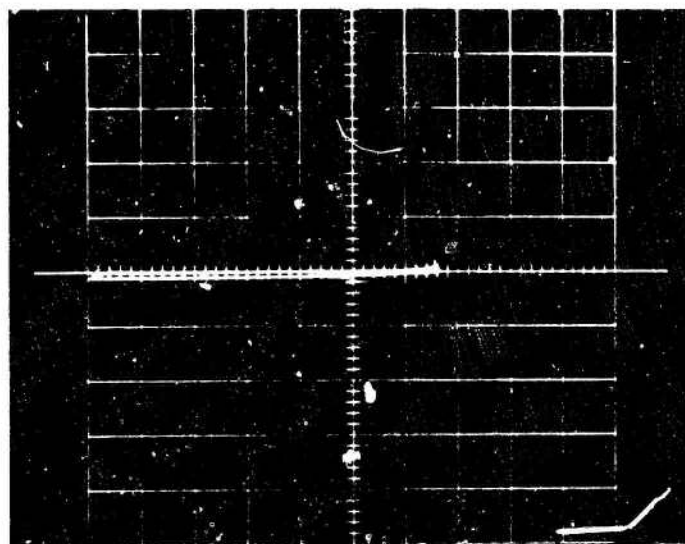


Fig. 3.1-15 (a) Current-voltage characteristics of non-punch-through Schottky barrier diode #6.5-2 without illumination.
 (b) Current-voltage characteristic of diode #6.5-2 with illumination.

Vertical scale: $10 \mu\text{A/cm}$; Horizontal scale: 5 V/cm .

diode without illumination (a) and with illumination (b). The saturation current is seen to remain small beyond 30 volts reverse bias with some slight multiplication evident in the illuminated diode beyond 30 volts. In contrast, Fig. 3.1-16 shows a dramatic increase in reverse bias current at only 6 volts. The capacitance versus voltage of these two junctions is shown in Fig. 3.1-17. The jog in the capacity curve of the punch-through diode at 2 volts corresponds to punch-through. The thickness of the active layer in the dimpled section of the diode is approximately $3\text{-}5\mu\text{m}$. Thus when the current increases drastically at 4 to 6 volts, the electric field at the interface should exceed 10^4 V/cm. Attempts will be made to view the spatial distribution of these generation centers by Bremstrahlung radiation from the junction.

3.1.4.3 High-Temperature Annealing of GaAs. To circumvent the problem of generation at the interface, wafers will be annealed at high temperatures in order to diffuse the electrical interface past the physical interface of the active and substrate layers. Since it is essential to maintain the integrity of the surface, a vacuum pumping station has been constructed for evacuating and baking quartz ampoules containing the epitaxial wafers to be annealed. Excess GaAs and As are also encapsulated with the sample to provide an equilibrium atmosphere at the annealing temperature. It is important that a high vacuum be attained with no traces of water

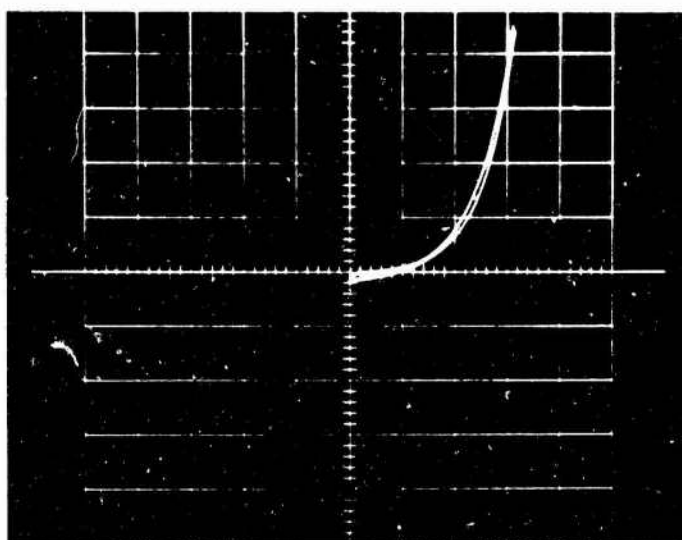


Fig. 3.1-16 Current-voltage characteristic of punch-through diode #7-1. Vertical scale: $10\mu\text{ A/cm}$; Horizontal scale: 2 V/cm .

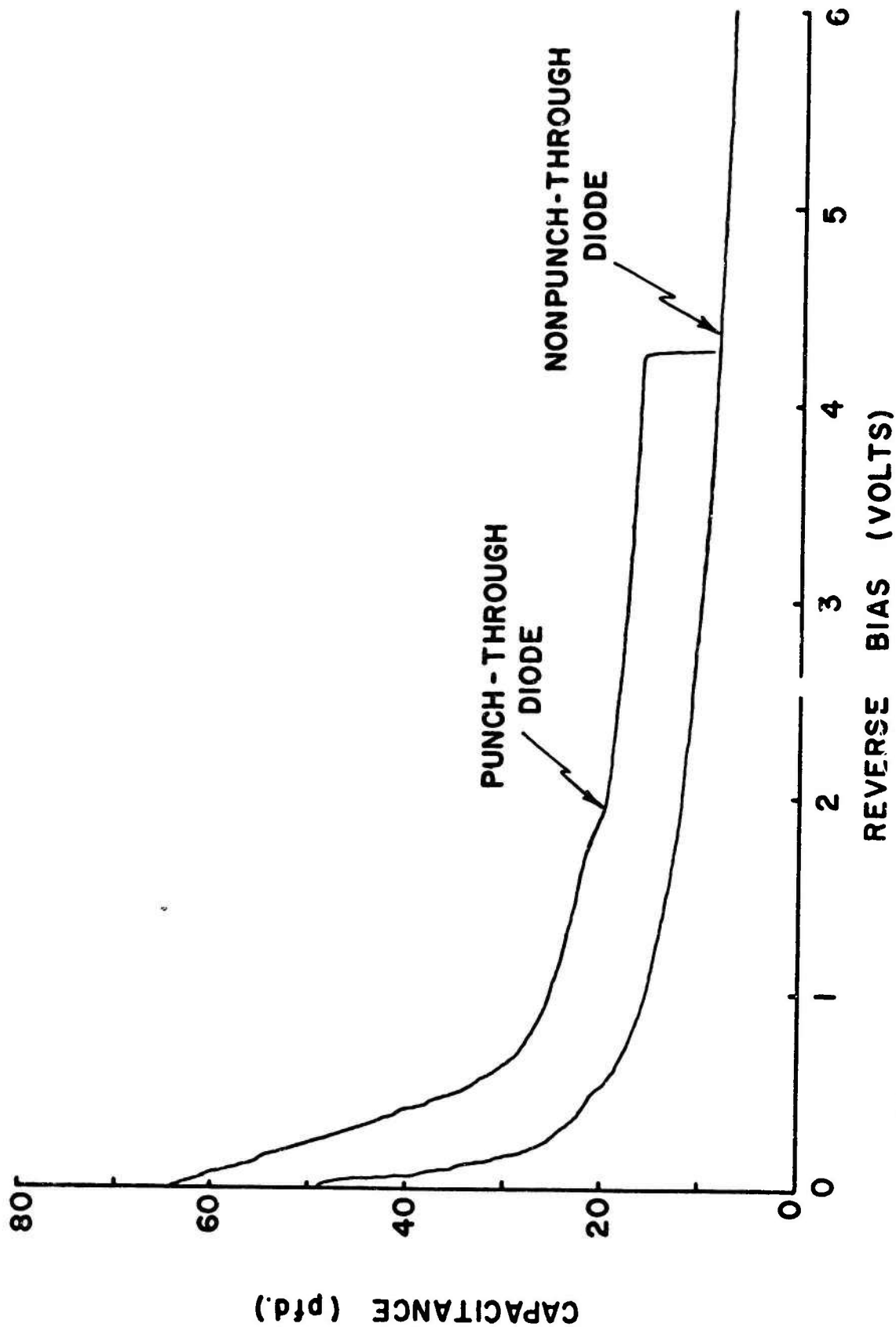


Fig. 3.1-17 Capacitance vs voltage traces of diodes #7-1 and #6.5-2. The jog in the capacitance curve of #7-1 corresponds to punch-through of the space-charge region to the buffer layer.

vapor that may act as a transporting agent within the capsule.

So far, with excess GaAs and sufficient As to maintain an atmosphere or so of As vapor pressure at 900°C, the original surface can be maintained to within 1/10 μ m or so.

Half of two epitaxial wafers of GaAs are being processed by the Science Center using an encapsulation technique and the other halves will be processed by Cornell. If the annealing is successful, then a significant improvement in the microwave diodes can be achieved and, furthermore, we may proceed with ionization rate measurements.

3.1.4.4 GaAs Operated in LSA Mode of TEO. When GaAs layers are grown under controlled conditions, it is possible to have transferred-electron oscillation in a repeatable manner. The most critical GaAs requirements for such oscillations are encountered when the efficient, limited space-charge accumulation (LSA) mode is used. The LSA mode requires that the GaAs active layer have a controlled donor concentration profile, uniform device area, low crystal strain, a low density of compensating acceptors, and planar high-performance interfaces with adjacent high-conductivity GaAs layers.

When devices are constructed from such material, they can be operated in the LSA mode in proper cavities, such as the multi-axis radial circuit.⁶ In such circuits the oscillation has a

portion of each cycle with the device voltage above the threshold voltage. The portion of each cycle spent above threshold is normally determined by microwave cavity resonance. Under proper LSA operating conditions, the only mobile excess space charge present is an electron accumulation layer that first forms at the negative electrode and then moves into the active layer with a velocity of approximately 1×10^7 cm/s during the portion of each cycle spent above threshold voltage. The electron depletion layer that forms in front of the accumulation layer to yield a high-field Gunn domain is kept negligible under LSA mode operating conditions. During the portion of each cycle spent below the threshold voltage, the accumulation layer is eliminated. The advantage of LSA operation is that it suppresses the electron depletion layer, allowing uniform fields from the accumulation layer to the positive electrode.

The LSA frequency of operation is not limited by transit time effects in the usual way. Devices can operate at a desired frequency even if the active layer is much thicker than the distance traveled by the electron accumulation layer during the portion of each cycle of the oscillation that the device spends above the threshold voltage. Even if the device is made thin enough for the accumulation layer to reach, or nearly reach, the positive electrode, there is no substantial change in the mode of

operation. If the device is made even thinner, the device voltage is quickly quenched to a value below the threshold voltage, each cycle, at the time that the accumulation layer reaches the anode. Thus the accumulation layer transit time determines the portion of each oscillation cycle that has device voltage above threshold voltage on ultra-thin devices.

The voltage swing during oscillation is from a value below threshold voltage to a value above the average, or bias, voltage by an amount nearly equal to the amount of microwave voltage swing below the bias voltage. During this voltage swing the amount of current swing is the important quantity for efficient operation. A parameter called the current peak-to-valley ratio determines this current swing. It is possible to apply very high pulsed bias voltage at low duty cycle to an LSA oscillator if no microwave output power is coupled out. During such unloaded oscillation at high pulsed bias voltage, the pulsed bias current nearly reaches the value of the instantaneous valley current. Thus a plot of pulsed bias current versus pulsed bias voltage yields the important current peak-to-valley ratio during unloaded oscillation.

It has recently been found that the pulsed, low-duty-cycle, current peak-to-valley ratio depends upon the device thickness and electron concentration even when the GaAs layers are nearly ideal.

Very thick LSA devices have a pulsed current peak-to-valley ratio that is nearly the velocity peak-to-valley ratio of 2.35 for X-band devices at room temperature. Thinner devices with the same electron concentration have lower pulsed current peak-to-valley ratios. Lower electron concentrations for a given thickness also yield lower pulsed current peak-to-valley ratios. Thinner devices yield lower peak power levels, but can be operated at higher duty cycle, or even continuously, so they are especially worthy of study for practical systems applications.

Figure 3.1-18 shows the pulse bias current versus the pulse bias voltage of an LSA device operated at X-band. It is $40\mu\text{m}$ thick, has uniform, $1.7 \times 10^{15}/\text{cm}^3$ electron concentration, and has a low-field resistance of about 2Ω . As expected for uniformly-doped layers, performance is substantially the same in both polarities and both polarities yield a current peak-to-valley ratio of just over 2, as shown.

When thinner devices are tested, they show pulsed bias current versus pulsed bias voltage like that of the commercial device shown in Fig. 3.1-19. Here there is a definite bias current minimum with a current peak-to-valley ratio of only 1.5, followed by a linear current rise. This device had about 25% more electron concentration on the positive electrode side of the active layer

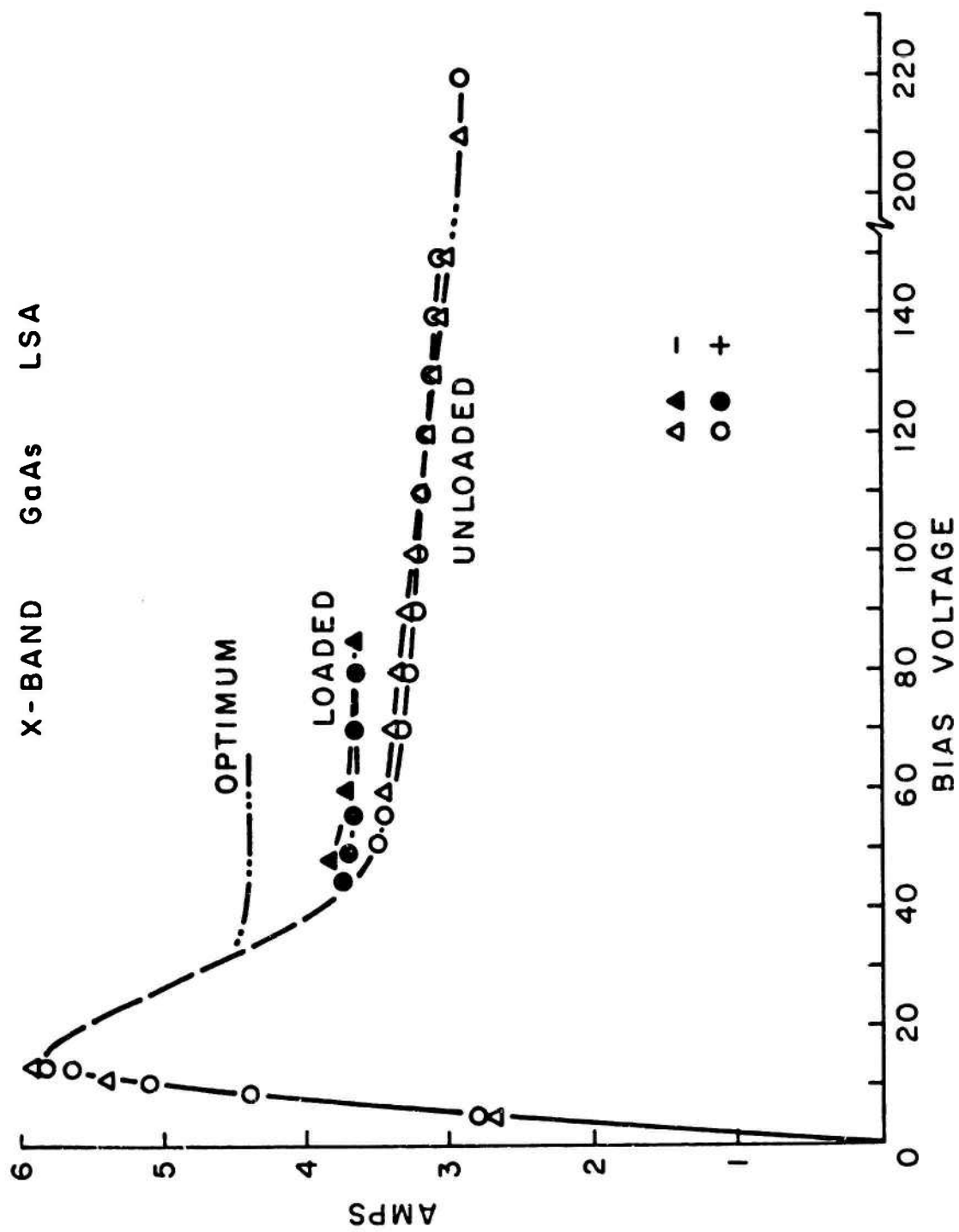


Fig. 3.1-18 Pulse bias current vs pulse bias voltage of an X-band LSA device.

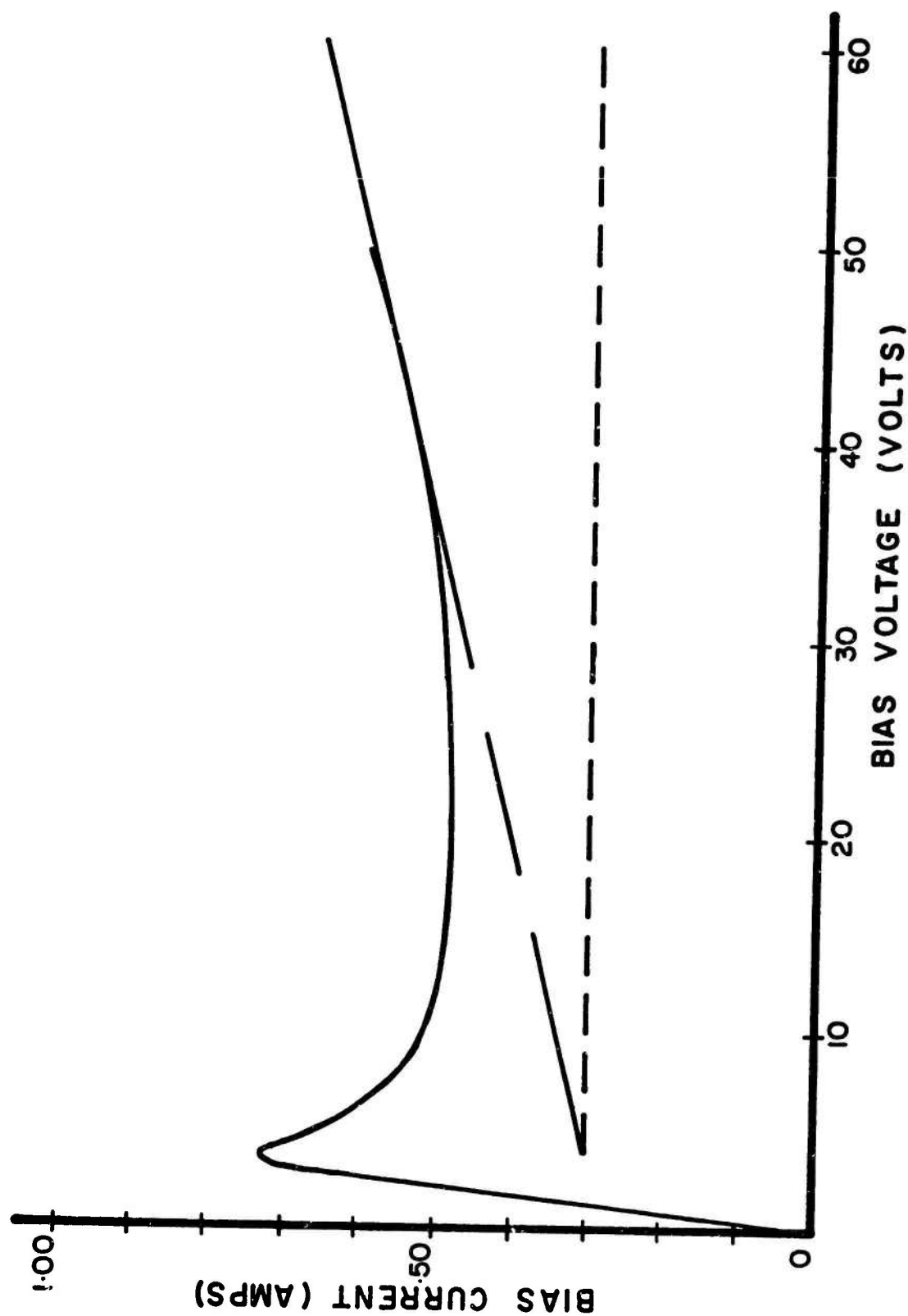


Fig. 3.1-19 Pulsed current-voltage characteristic of a thin LSA device.

than it did on the opposite side. It has about $11\mu\text{m}$ thickness and $1.5 \times 10^{15}/\text{cm}^3$ average electron concentration. This electron concentration gradient causes poor pulsed operation, with an avalanche breakdown, in the opposite polarity. If devices with uniform electron concentration were tested, a similar current-voltage characteristic would result, but with a well-behaved current peak-to-valley ratio of 1.75 or so in both polarities. A plot of data on the reciprocal of the pulsed current peak-to-valley ratio versus the reciprocal of the product of electron concentration and thickness of the device active layer is made in Fig. 3.1-20. Three devices with uniform electron concentration and device area are shown marked D. These devices operate efficiently in low-duty-cycle operation. The data for these devices fall along a straight line that intersects the axis at the reciprocal of the theoretical ratio of valley velocity to peak velocity. These uniformly-doped devices were grown by steady-state, temperature gradient LPE by David Woodard at Cayuga Associates. Commercial devices marked A, B, and C, from three manufacturers, are for moderately efficient "C.W." devices in pulsed operation. Device A is the one used to take the data of Fig. 3.1-19. Devices A, B, and C all have electron concentration gradients yielding lower pulsed current peak-to-valley ratios. If

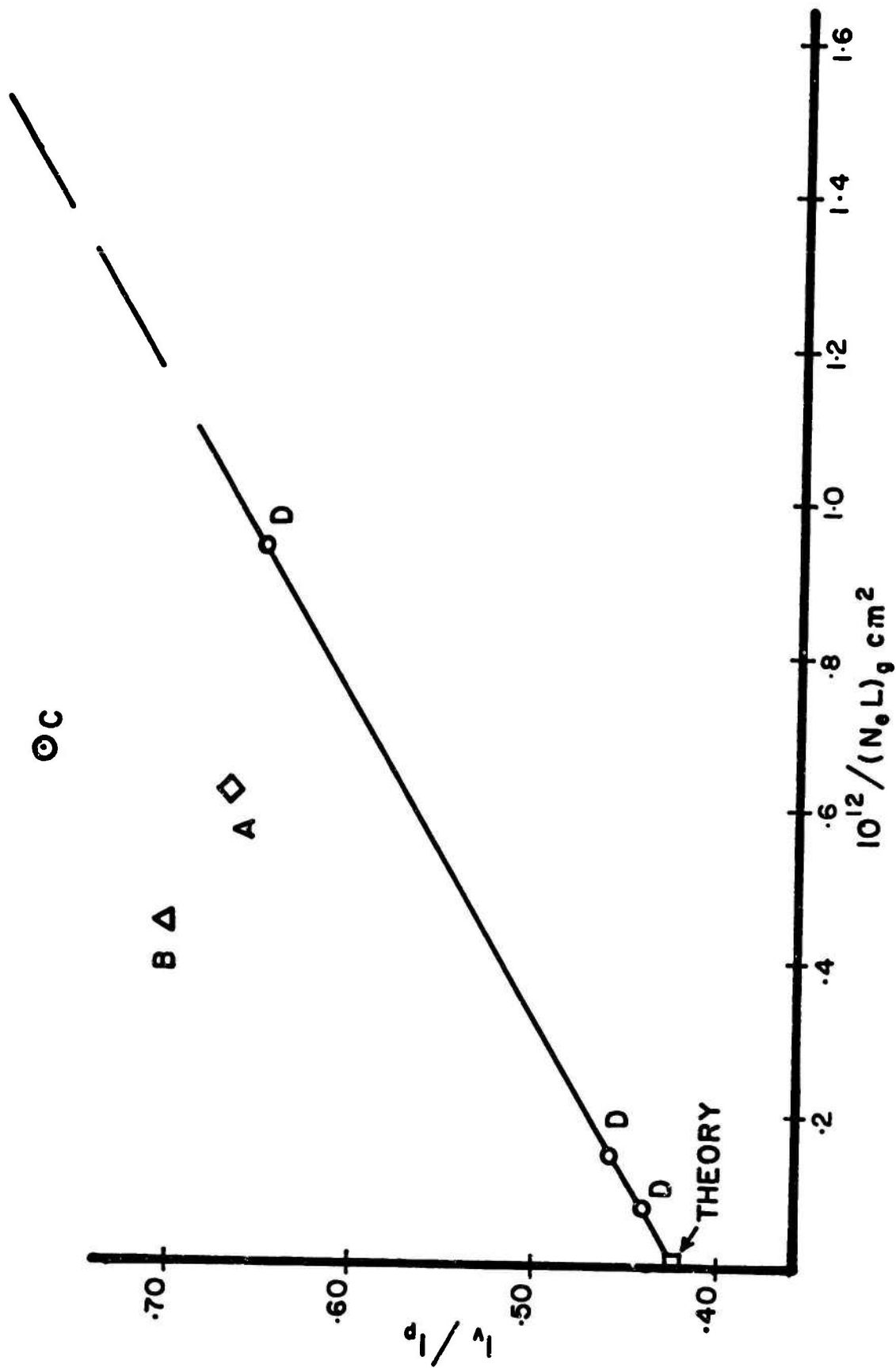


Fig. 3.1-20 Reciprocal of the pulsed current peak-to-valley ratio vs thickness of the active device.

controlled properly, these electron concentration gradients may be useful in C.W. operation where temperature gradients occur, but this aspect of the devices has not yet been studied on this program.

The consistent reduction of current peak-to-valley ratio with reduced product of the electron concentration times the length of the active layer can be easily explained. The accumulation layer size rises and falls in response to the voltage across the device and the resulting uniform electric field from the accumulation layer to the positive electrode. During the time that the accumulation layer is moving into the active layer, it induces a current in the electrodes applying the voltage, raising the value of the valley current. By Ramo's theorem, this induced current density is: $J = Q_u V_{AL} / L$, where J is the induced current density in amps/cm², Q_u is the accumulation layer (surface) charge density in coulombs/cm², V_{AL} is the velocity of the accumulation layer, and L is the thickness of the active layer separating the electrodes. This moderate induced current is in phase with the microwave voltage and thus counters the out-of-phase, negative resistance resulting from the bulk properties of the transferred-electron effect. Since the negative conductance per unit area is proportional to the electron concentration and the positive conductance associated with the induced current is reciprocally

proportional to the product of electron concentration times the length of the active layer. It is the ratio of the positive conductance to the negative conductance that raises the reciprocal of the current peak-to-valley ratio.

An alternate explanation involves the positive resistance properties of that region of the active layer, between the negative electrode and the accumulation layer that has electric field levels below the threshold value. As the total device voltage rises, the accumulation layer charge rises, and a higher current density is required in the positive resistance region, yielding resistive loss. In thin devices, a larger percentage of the active layer has positive resistance, and in devices with lower electron concentration more loss is present due to current in this region.

One important operating parameter is the asymptotic frequency, f_a . This frequency is the frequency at which the diode is resonant with the cavity only. $f_a = 1/2\pi\sqrt{LC}$ where L and C are the inductance and capacitance of the oscillator under no-load conditions. At this asymptotic frequency the time below threshold voltage is zero, resulting in an oscillation wave shape that is sinusoidal, with the minimum voltage equal to the threshold voltage.

Camp has shown that the time an LSA oscillator spends above threshold (τ_a) is nearly constant, whereas the time below threshold is a function of bias voltage, decreases as the voltage increases. Thus at infinite bias voltage, the time below threshold will be zero. The frequency then is $1/\tau_a$. To measure f_a , we use a lightly loaded circuit, and measure its operating frequency as a function of voltage. When $1/f$ is plotted against $1/[V_b/V_{th} - \frac{1}{2}] = 0$ (or $V_b \sim \infty$) is τ_a is shown in Fig. 3.1-21.

Experimentally, high efficiency approaching that predicted by theory has been obtained, depending on the current peak-to-valley ratio, I_p/I_v . It has been shown that when the bias voltage is adjusted to cause the bias frequency to be one-half the circuit resonant frequency, f_a , the efficiency is maximum and is given by:

$$n_o \cong b \frac{\left(\frac{I_p}{I_v} - 1\right)}{\left(\frac{I_p}{I_v} + 1\right)} \left[1 - \frac{V_{th}}{2V_B} \left(1 + \frac{I_v}{I_p} \right) \right] \quad (8)$$

where $b = 0.6$ for fundamental frequency only ($= 0.9$ with second harmonic tuning) and where V_B is the bias voltage and V_{th} is the threshold voltage. The bias current is nearly up to $(I_p + I_v)/2$, with second harmonic tuning. For $I_p/I_v \geq 2$ which is the case for

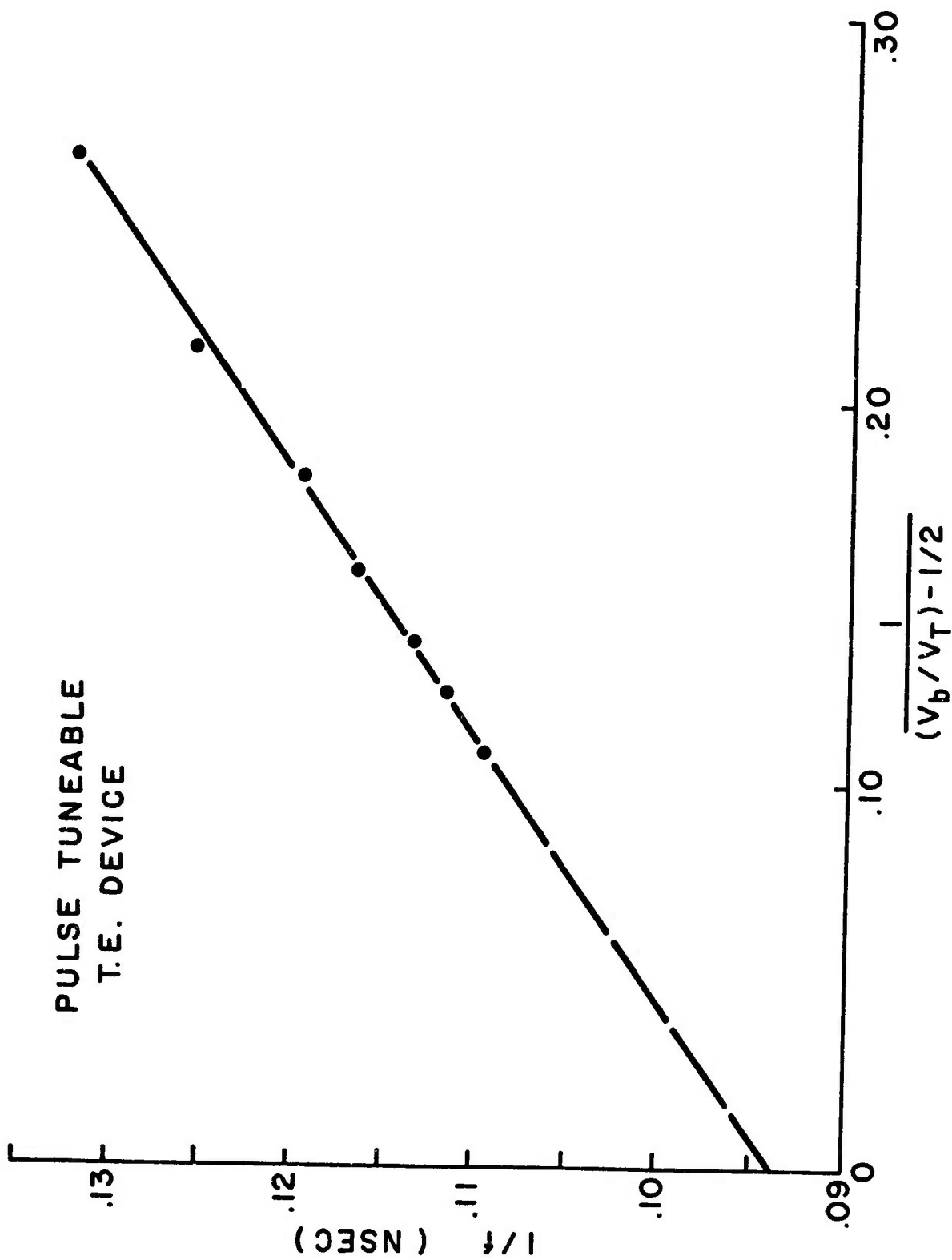


Fig. 3.1-21 Determination of time spent above threshold in an LSA oscillator determined as the intercept on the ordinate.

thicker devices, and $V_B \cong 4 V_{th}$ $\eta \cong 25$ or 17% depending on whether second harmonic has been tuned or not. It is clear, then, that the current peak-to-valley ratio plays a very important role in the efficiency of the dc to RF conversion.

Efficiency of around 12% is often obtained. With second harmonic tuning in the appropriate resonant cavity, efficiency as high as 19.6% has been achieved in experiments on this program near 3 GHz. This particularly high efficiency is obtained using a thick diode ($L \sim 100\mu m$, $N_e = \sim 1.0 \times 10^{15} \text{ cm}^2$) in a multi-axis radial cavity (MARC) earlier.* Second harmonic tuning is done by using the appropriate low-impedance slug, approximately 22Ω in the output coaxial line for the first $\lambda/8$ length. This causes the reflection of a small portion of the peak voltage swing, delayed by $90^\circ < \theta < 180^\circ$ so that it adds up to the voltage below threshold forcing the current to build up faster. Of course, the maximum efficiency occurs when the current is a square wave, having I_p for half a cycle and I_v for the other half cycle. See Fig. 3.1-22(a) and 22(b) for voltage and current wave shapes. The second harmonic tuning approximates this square wave efficiency.

Various methods for tuning the second harmonic have been tried: double slug tuning, double stub tuning, irises, and a slide screw tuner. In many cases these improved the efficiency but these

* L. Eastman and W. Wilson, Proc. Third Biennial Cornell Electrical Engineering Conf., August 17-19, 1971, p. 361.

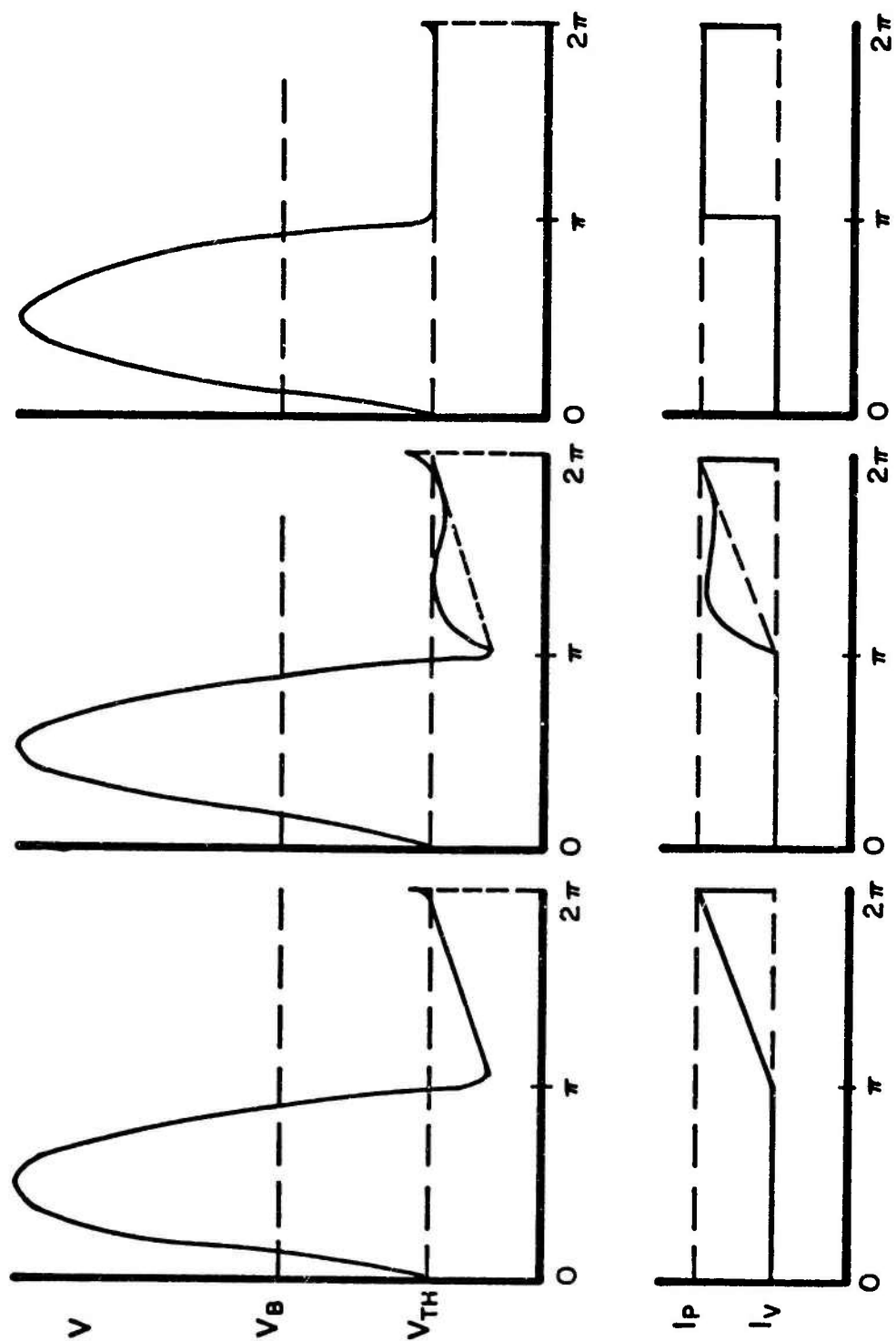


Fig. 3.1-22 Voltage and current wave shapes illustrating the use of second harmonic tuning to approximate the maximal efficiency square wave.

methods are more cumbersome and give less pronounced efficiency rise than the Marc type cavity with the $\lambda/8$ low impedance slug. With various slug impedance levels, optimum parallel circuit loading is possible and is

$$R_L \geq \frac{12 R_0 \frac{V_B}{V_{th}} - 1/2}{\frac{I_p}{I_v} - 1} \cong |R_N|_{opt} \quad (9)$$

where $|R_N|_{opt}$ is the optimum negative resistance that can be obtained for any bias V_B and low field resistance R_0 . The value is replaced by 8 when the second harmonic is tuned. Thus the loading at the second harmonic is important too. Carroll has shown that when the second harmonic is loaded heavily, it can seriously affect the oscillation, in some cases, could quench the oscillation. Camp has shown that the optimal loading for the second harmonic is that $(R_L)_2 \geq 4x(R_L)_1$ of fundamental. Much effort has previously been put into analyzing the optimum circuit, harmonic generation efficiency, and power output of LSA devices, and it is now possible with the appropriate resonant cavity and with second harmonic tuning, to achieve nearly the maximum efficiency predicted theoretically. This efficiency depends on the material itself through the I_p/I_v ratio determined by the product of electron concentration, N , times the device active layer length and by the

gradient of the doping profile. There is also the requirement that: $1 \times 10^5 < N/f_a < 2 \times 10^5$ sec/cm³ to control LSA starting transients and space charge instabilities at room temperature.

From the viewpoint of making an efficient oscillator, the ratio of peak current to valley current is the most important value, representing the important materials parameters. The higher this value, the greater the efficiency. From the viewpoint of space charge stability, the positive and negative differential mobilities become important. These two quantities specify the dielectric decay and growth rates of space charge instabilities in the crystal.

A large gradient of doping concentration or any device area variation may result in a domain which stops the desired oscillation and whose high field could damage the diode. The efficiency decreases as the slope of the doping gradient increases, so the best low-duty-cycle efficiency is obtained for a flat doping profile.

During the next working period, approximate theoretical treatment will be made to yield a prediction of the rise in valley current with lower $N \times L$ product and with higher bias voltage. In addition, the effects of ambient temperature and self-heating on peak-to-valley ratio and efficiency will be studied, especially from the materials properties point of view.

3.2 Semi-Insulating Materials

3.2.1 Crystal Growth

The program at USC was to grow bulk GaAs with low impurity concentration and low dislocation density.

The approach taken in the growth of GaAs crystals has been to minimize the sources of contamination during synthesis and growth. These crystals are grown in quartz boats using a horizontal gradient freeze system. Silicon is a prime impurity and is introduced at concentrations of $\sim 10^{17} \text{ cm}^{-3}$ if temperatures during synthesis and growth rise $\sim 100^\circ\text{C}$ above the melting point.

Lowering this maximum temperature presents problems; namely, control of the directionality of solidification decreases as the maximum temperature and corresponding temperature gradient decrease. Efforts were concentrated on improving temperature control as a means for maintaining freezing directionality with lower temperature gradients and hence lower maximum temperatures.

The first horizontal gradient freeze system was constructed and operated with temperature gradients typically used by others, $\sim 0.8^\circ\text{C}/\text{cm}$. Early problems such as strong FM radio interference in the control circuits and varying ambient conditions have been solved to a large degree. This system is now capable of producing 65 to 165 gm ingots. To date ten ingots have been grown to establish the ranges of growth parameters, such

as furnace gradients adjacent to the boat and the temperatures which control the arsenic pressure. Single-crystal yields of these unseeded ingots are within the range, 65-100%.

A second horizontal gradient freeze furnace system has been completed. It is an improvement over the first one in several significant aspects. Its arsenic control furnace is a USC design and has operated by itself at 600°C to within 0.003°C for a 24-hour period. The high-temperature furnace is a three-zone one, a Mini-Brute manufactured by Thermoco Products Corporation. Dimensions of this system are such that it can handle 500 gm ingots 15 cm long. This system is still under preliminary evaluation for stabilities of temperatures and their changes during growth cycles. It is expected to be in operation by August 1, 1974. Initially, it will be used in parallel with the first apparatus and then replace it.

The emphasis on establishing the degree of temperature control obtainable also relates to the feasibility for growing crystals in a vertical direction. Advantages of this would be higher stabilities of the solid-liquid interfacial region, much simplified control of the radial temperature gradients and the planarity of the interface, plus providing a more useful wafer shape for subsequent device use. Deliberate seeding is also greatly simplified with a vertical growth axis. Vertical systems have not been extensively used in the past because of slow equilibration rate of the liquid composition near the freezing interface

with vapor phase. This is due to the slow transport through the intervening liquid column. Tight temperature control is an obvious prerequisite to slowing the growth rate to accommodate this. It is believed that growth in a vertical direction is feasible, and such a system is currently being designed.

Supporting equipment built for this program include a vacuum pumping station for evacuating the growth and arsenic ampoules before sealing, an arsenic sublimation apparatus, precision bias supplies so that temperatures in the GaAs growth furnace and the arsenic furnace can be monitored on an expanded scale of a multi-point recorder with a range as small as 5°C . A quartz strip heater for alloying contacts has been set up to be used in a Pd-diffused H_2 atmosphere.

Since the beginning of this program, ten ingots of GaAs have been grown in the original apparatus. Typical weights of the 15-cm-long ingots are 65-90 gm. These are self-seeded and have useful single-crystal yields of 70-100%. Dislocation densities vary from $\sim 10^5$ to $3 \times 10^3 \text{ cm}^{-2}$. These have been grown from melts which have been varied in composition from being arsenic- to gallium-rich. The furnace temperature gradients have been varied from 8 to $0.8^{\circ}\text{C cm}^{-1}$ and growth rates were 0.6 to 5 cm/hr. Sticking or wetting of the GaAs with the boat is not a problem. This is in accord with the residual oxides in the sealed ampoules being relatively low.

The properties of the crystals vary but not in a manner inconsistent with the growth conditions. One crystal which had an exceptionally high dislocation density, 10^5 cm^{-2} , had an excellent mobility of $4800 \text{ cm}^2 \text{ v}^{-1} \text{ s}^{-1}$ or 20% higher than nominal for its carrier concentration of $2 \times 10^{17} \text{ cm}^{-3}$. The high dislocation density may have facilitated the condensation of Ga or As defects. This crystal had been grown at a slow rate, 0.55 cm/hr with a high gradient, $0.7^\circ \text{C cm}^{-1}$. The latter figure most likely accounts for the relatively high carrier concentration because of the necessity to raise the GaAs $\sim 100^\circ \text{C}$ above its melting point therefore enhancing its reaction with the quartz boat. Undoped crystals grown with smaller temperature gradients have lower carrier concentrations, $\lesssim 10^{16} \text{ cm}^{-3}$. These have presented problems in characterizing in part because of difficulties in making ohmic contacts and possibly because of inhomogeneities.

One ingot was grown from a melt weighing 165 gm. The single crystal yield was above average and sticking was not a problem. This lends confidence to the belief that 15-cm crystals weighing up to 500 gm can be grown in the new horizontal furnace system.

A semi-insulating crystal, USC-7, was grown from sections of the first four ingots. It was unique in that the GaAs was not first synthesized from the elements but, more significantly, the minimum temperature in the sealed ampoule was $\sim 1200^\circ \text{C}$ during growth. A section at a

distance of 1.5 cm of the nominal seed end was evaluated at the Science Center. In this section the carrier concentration varied from the mid- 10^{15} cm^{-3} range to a semi-insulating range. This section was reported to have a higher photoconductivity for photons with energies below the bandgap than at the gap energy, as compared to Cr-doped semi-insulating crystals. It is possible that the high extrinsic photoconductivity is due to a high density of deep levels. It is speculated here that the high resistivity in the above crystal is caused by the reduction in the Si concentration or its pairing with oxygen much in the manner observed at IBM.

It is believed that the initial goals have been established; namely, that single crystals can now be grown with moderate yields and with defect concentrations probably in the 10^{16} cm^{-3} range or possibly less. These can be grown as semi-insulating without intentional doping and are suitable for Cr-doping experiments. Crystals of the 65-165 gm size can be grown at the rate of one per week if this best serves the needs of the program. Efforts to obtain larger crystals have been described.

Other activities which relate to these efforts are the use of stabilized zirconia tubes to purify H_2 atmospheres and measure its water content in the range of H_2O mole fractions of 2×10^{-7} to 10^{-4} . This is presently directed towards lowering the growth temperature of liquid phase GaAs epitaxy down to $\sim 600^\circ\text{C}$. Earlier this effort had been directed

towards the development of a means for measuring oxygen in Ga solutions and in GaAs. The findings on a limited number of semi-insulating undoped samples and several deliberately grown under added oxygen was that the detected oxygen content was less than $5 \times 10^{16} \text{ cm}^{-3}$. It suggests that it may be difficult to introduce relatively large concentrations of oxygen in GaAs unless it is paired with a defect such as Si. As such our procedure would not detect it. Sensitivity for detecting oxygen in GaAs at concentrations above that of the Si can be increased to $\sim 10^{15} \text{ atoms/cm}^3$.

Problem areas associated with evaluating the electrical properties of the higher resistivity crystals involve difficulties in making reliable ohmic contacts. Towards this end, an apparatus for alloying doped gold wires using spark melting is being built. This has proven to be reliable in the past for n-type samples with electron concentrations of $\sim 10^{17} \text{ cm}^{-3}$ and mobilities between 3000 and 5000 $\text{cm}^2\text{v}^{-1}\text{s}^{-1}$. This method does not allow for the precise positioning of the contacts, a factor which is important if sample homogeneity is a problem. Homogeneity is a problem in most Cr-doped semi-insulating crystals and some undoped ones. In anticipation of this, we are assembling an apparatus to grow few-micron-thick n^+ or p^+ epi-layers on such samples from solution so that contacts can be made with precise positioning.

Dislocation densities are still not under adequate control. The crystal with the lowest average dislocation density, $3 \times 10^3 \text{ cm}^{-2}$, has regions $\sim 1 \text{ mm}^2$ in which the density was lower by an order of magnitude. We are encouraged by the existence of such regions in that it indicates that boat wetting is not a serious source of stress nor is the average curvature of the freezing interface. A likely cause for the regions of higher dislocation densities is cellular growth--a condition which can be improved in principle by adjusting the As pressure, temperature gradients, and crystal dimensions.

3.2.2 Material Evaluation

3.2.2.1 Quantitative Measurements. The goal for this group of measurements is to obtain quantitative results on the trap densities. The density of traps is expected to affect the properties of the junction between the semi-insulated substrate and epitaxial layers grown on top for device construction. Therefore, sample configurations involving that type of junction are best suited for the measurement of trap densities.

The approach initially taken was discussed in the first semi-annual report. Structures were built with a thin semi-insulating layer (typically 10μ) between an n-type epi-layer and an evaporated metal film. I-V characteristics of these n-i-m structures were measured when the n-type layer was negatively biased in order to

inject electrons. At low voltage, injected electrons start filling the insulator traps and build a trapped space charge that keeps the current low. all the traps are full when the voltage reaches the value⁷

$$V_{TFL} = \frac{qN_{ET}L^2}{2\epsilon} \quad (10)$$

where q is the electronic charge, N_{ET} the electron trap density, L the thickness of the semi-insulating material, and ϵ the static dielectric constant. At V_{TFL} there is a sharp current increase until it reaches a free carrier space-charge-limited regime. This sharp rise of current at V_{TFL} is equivalent to breakdown for all practical purposes. Similar measurements on p-i-m structures were expected to yield hole-trap densities.

As discussed in the first semi-annual report, breakdown measurements on commercial semi-insulating GaAs* yielded electron trap densities in the 10^{13} cm^{-3} range. These figures were several orders of magnitude lower than the concentration of Cr indicated by mass spectroscopy. Therefore, they were not considered reliable at that time, and it was believed that there was some failure of the model for the trapping effects. In particular, it was

* Supplied by Laser Diode Laboratory and Texas Instruments, Materials Laboratory.

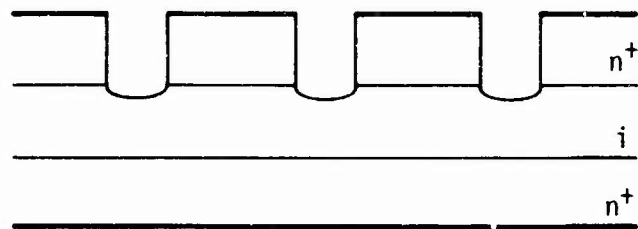
suspected that hole injection could take place from the metal side, leading to a double-injection type of breakdown. However, recent results, which will be discussed in this section, are now supporting the original low figure for the electron trap density as a real property of the material.

Indications in support of the low electron trap density arise from a reverse breakdown measurement. Some n-i-m structures with Ti as the metal were reverse-biased (the n side positive). The structures were made small (150 μ diameter) in order to reduce the probability of premature breakdown due to imperfections. Breakdown voltages of 600V were observed in structures with a semi-insulator thickness of 30 μ . The junction between the n-type epitaxial layer and the semi-insulating material can be treated as an abrupt p-n junction. When this junction is reverse-biased, the negative charge on the semi-insulating side (the p side) is built up by filling of electron traps. Assuming that breakdown is due to avalanche,⁸ an upper bound of electron trap density of 10^{15} cm^{-3} is obtained for the semi-insulating material. Still, this is an indication that the electron trap density may be indeed much lower than the density of Cr impurities which is in the middle of 10^{16} cm^{-3} range for the material discussed here. In order to simplify the interpretation of the breakdown effects, n-i-n structures were constructed.

An n-i-n structure had been studied by Haisty and Hoyt.⁹ However, in their experiment, one of the n-type contacts was actually an alloyed metal contact. Therefore, they were left with the same uncertainty which arose from the n-i-m structure discussed here; namely, whether the metallic contact may be responsible for double injection. The n-i-n structure constructed here is more difficult to build than the n-i-m structure or the structure of Ref. 9 because it requires double epitaxial growth. But this n-i-n structure excludes all possibility of double injection effects. It is considered here a step forward in the understanding of the breakdown effects and their use for the measurements of trap densities in semi-insulating GaAs.

The n-i-n structures are constructed by growing an epitaxial n^+ layer ($n \sim 10^{18} \text{ cm}^{-3}$) on one side of a semi-insulating substrate (see Fig. 3.2-1(a)). The other side is polished and etched down until the thickness of the semi-insulating material is reduced to 10-20 μ . After this, another n^+ film is grown on the other side. On one side a large Ti-Au contact is made (Fig. 3.2-1(a)) while on the other side small Ti-Au contacts (15 $\times$ 15 mil) are constructed. The structures are then separated by etching channels through the n-type layer.

(a)



(b)

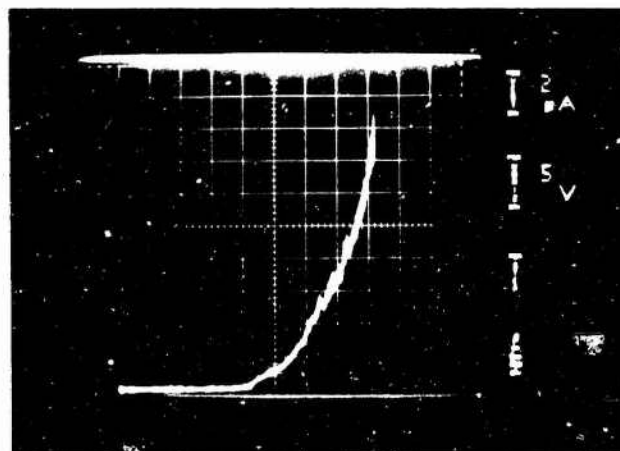


Fig. 3.2-1 (a) Schematic of an n-i-n structure.
(b) I-V characteristic of an n-i-n structure.
The measurement was made in a dc condition.

Figure 3.2-1(b) shows the I-V characteristic of an n-i-n structure. The insulator thickness was 27μ . Although shown as an oscilloscope trace, the measurement was made in a dc condition, photographing the slow motion of the point on the oscilloscope screen. Breakdown takes place at 20V. Assuming that breakdown occurs when the depletion region of the reverse-biased junction reaches the other junction and injection starts, namely, when a punch-through condition is reached, the electron trap density can be calculated from Eq. (10).^{*} For the sample of Fig. 3.2-1, it is $3 \times 10^{13} \text{ cm}^{-3}$. There is some preliminary indication that the breakdown voltage follows a square law dependence on the thickness, as expected.

The result from the n-i-n structure cannot be compared directly with those from the n-i-m structures because the data were obtained on different substrates, although they are from the same suppliers. However, the agreement on the order of magnitude of the electron trap density is very suggestive. It indicates that the measurements on n-i-m structures were reflecting actual low-electron trap densities.

* Notice that this is trap-filling by depletion while Eq. (10) was derived for an injection condition. However, the equation is valid because it derives directly from Poisson's equation.

In order to further support the conclusion that the model is correct and trap densities are low, an attempt is being made to measure the potential distribution across the structure by using Auger electron spectroscopy (AES) in an ultra-high vacuum scanning electron microscope (SEM) system. For this application of the AES-SEM system, a finely-focused 20 kV electron beam (primary beam) of $\sim 3/4\mu\text{m}$ diameter is stepped across the depletion region of interest in the sample which is a cleaved n-i-n structure with the side exposed. At each position of the primary beam the Auger peak for carbon is recorded. It has been determined that the energy of the C peak is a linear function of surface potential over at least a $\pm 40\text{V}$ range.¹⁰ It is hoped to measure with sub-micron spatial resolution the potential distribution across the n-i-n structure by this means. Preliminary results are promising, with further work needed for proper interpretation.

Although the measurements on the n-i-n structures are still preliminary, the evidence that the electron trap density is in the 10^{13} cm^{-3} range in some standard commercial material deserves some comment. What makes this low figure so striking is that mass spectroscopy analysis of the same material indicates concentrations of Si, O, and Cr in the 10^{16} cm^{-3} range, as shown in Table 3.2-1 of the first semi-annual report. Evidently, strong compensation

effects are taking place in the material. Oxygen is likely to be a key compensating impurity by introducing a deep donor level, as proposed by Blanc and Weisberg.¹¹ Their model for the compensation effect in material doped only with O requires that the number of shallow acceptors exceeds that of shallow donors, so that the deep O donors located near the middle of the gap can pin the Fermi level in this position. The role of Cr in semi-insulating GaAs would be to relax the requirement that there are more shallow acceptors than donors and to pin the Fermi level near the deep O donors and the deep Cr acceptors. This model would explain how the material can acquire high resistivity by the addition of both O and Cr impurities. However, considering that the number of electron traps is equal to the difference between the number of acceptors and the number of shallow donors, it is difficult to admit a compensation so perfect that the difference between those two densities is three orders of magnitude smaller than each of them. Therefore, the possibility of some natural pairing of impurities must be considered.¹² As to the presence of O as a deep donor, it will be tested by measurements of hole-trap concentrations on p-i-p structures. Measurements of breakdown voltages on p-i-m structures were made (see the first semi-annual report). Such measurements indicate breakdown voltages slightly larger than those of n-i-m structures, and, therefore, hole trap densities larger than the electron trap

densities, indicating that deep donors may indeed exist. But the measurements of electron and hole trap densities were made on different materials. Systematic studies are necessary in order to clarify the situation.

Some attention was focused on capacitance measurements. Transient capacity measurements at Schottky barriers and p-n junction yield concentrations of deep traps in n- or p-type semiconductors.¹³ When the time constants of the transients are measured as functions of temperature, the depth of the traps can be calculated. But for all those measurements a conductive material is required, as the capacity is usually measured with some conventional capacitance bridge at a frequency in the megahertz range. At this frequency, the deep traps cannot follow the excitation because their emission and recombination lifetimes are too long (of the order of seconds). The lifetimes referred to are functions not only of the ability of the deep center to capture and emit carriers, but also of the series resistance in the capacitor circuit.

A direct approach was attempted which consisted of measuring the capacity vs frequency. It was hoped that at sufficiently low frequencies it would be possible to measure the capacitance of the junctions. From here it would be possible, in principle, to determine depletion width and impurity densities. For a preliminary

study, the n-i-m structure was used. As a first approximation, the n-i-m structure can be represented by the equivalent circuit shown in the insert of Fig. 3.2-2. This circuit represents the structure under reverse bias (the n side positive). In the insert, C_0 represents the capacity between the n-layer and the metal, inversely proportional to the thickness of the semi-insulating layer. This is the high-frequency capacity measured by a capacitance bridge. R_I represents the resistance of the semi-insulating layer. C_1 is the capacity of the n-i junction, and R_1 is such that $R_1 C_1$ is equal to the lifetime of the traps. C_2 and R_2 are the analogs of C_1 and R_1 for the m-i junction. The admittance of this circuit is:

$$Y = \frac{1}{R} \frac{\omega^2 R^2 C^2}{1 + \omega^2 R^2 C^2} + j\omega \frac{C}{1 + \omega^2 R^2 C^2} + C_0 \quad (11)$$

where $R = R_I + R_1 + R_2$ and $1/C = 1/C_1 + 1/C_2$. Figure 3.2-2 shows the real and imaginary parts of Y calculated from Eq. (11) for typical values of $R_I C$ and C_0 . R_1 and R_2 are assumed negligible. Measurements of the real and imaginary parts of Y for n-i-m structures were made with a lock-in detector equipped with a current preamplifier. The samples were kept in the dark in order to avoid photoconductive effects. Results are shown in Fig. 3.2-3 for two samples with the thickness of the semi-insulating layer equal to

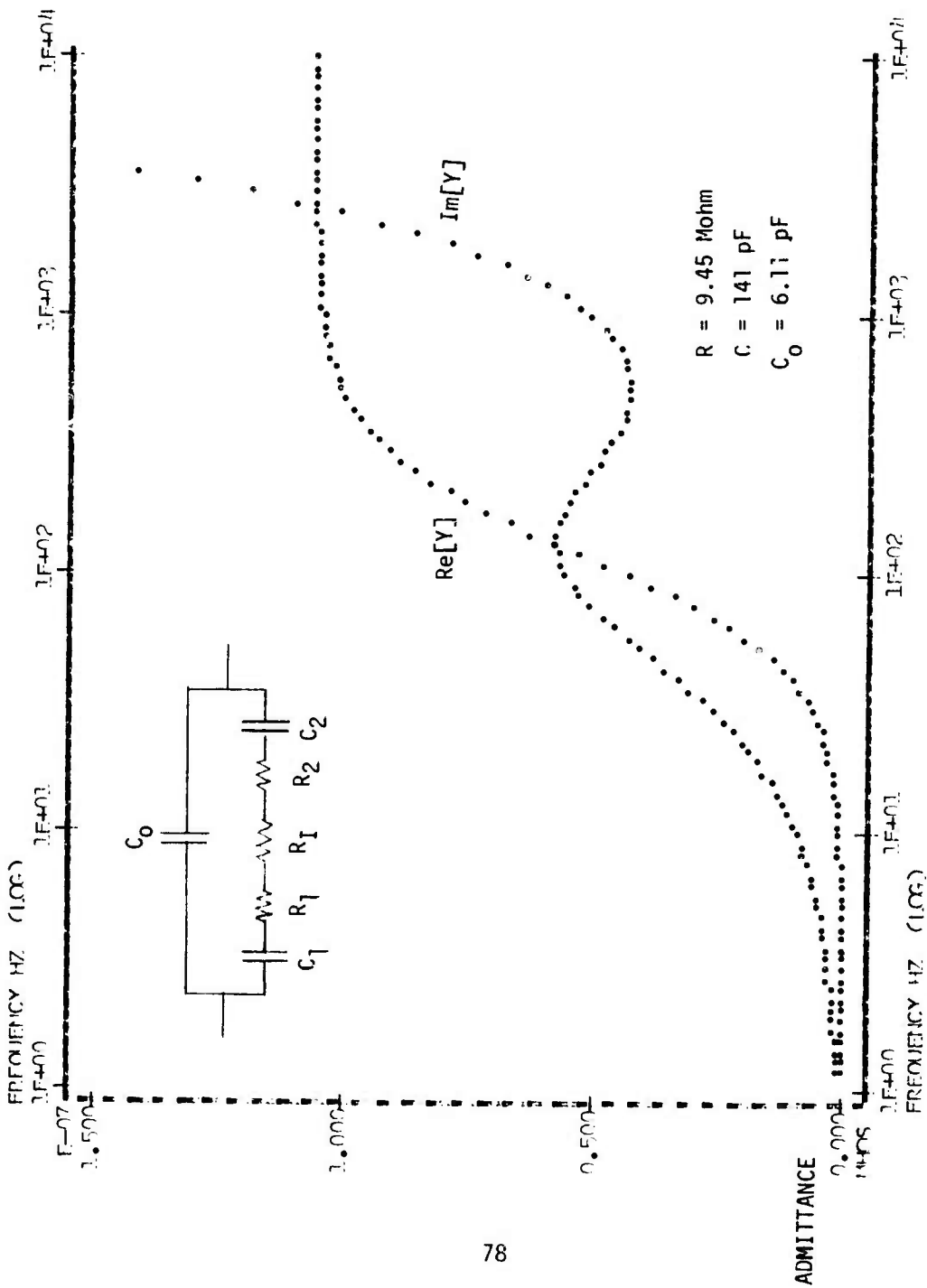


Fig. 3.2-2 Real and imaginary parts of the admittance of the equivalent circuit of an n-i-m structure under reverse bias.

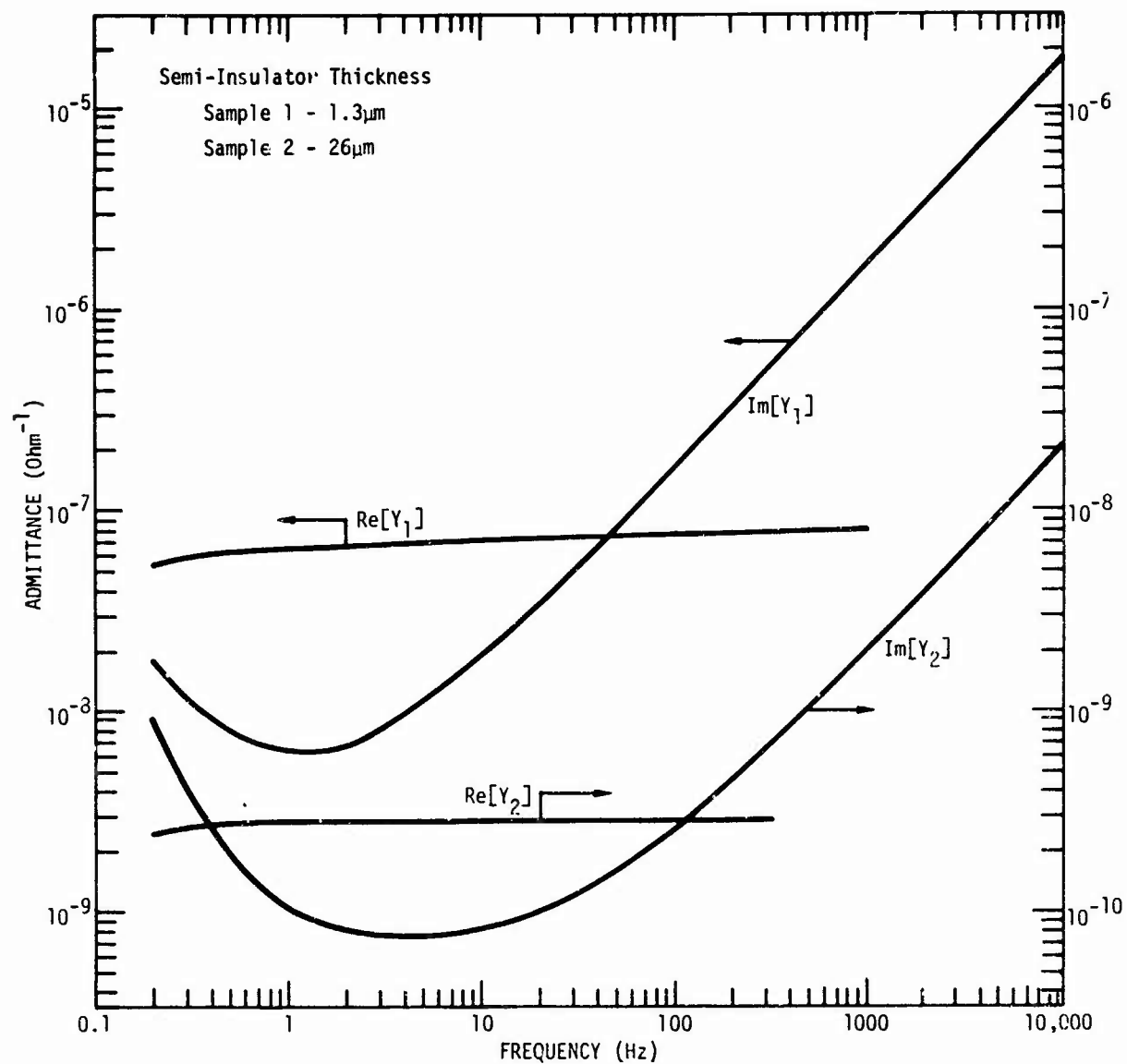


Fig. 3.2-3 Real and imaginary parts of the admittance of an n-i-m structure under reverse bias.

1.3 μ m and 26 μ m, respectively. The samples were not biased. The curves are insensitive to reverse bias. These curves are different from the ideal curves of Fig. 3.2-2. The real parts of the admittances are almost constant. The imaginary parts are straight lines in most of the frequency spectrum indicating a proportionality to ωC_0 . The capacity obtained from the slopes agrees with that measured with a capacitance bridge at 1 MHz. Only at very low frequency do the imaginary parts bend upward suggesting a behavior of the type of Fig. 3.2-2. However, the bend occurs in a noisy frequency range, where it can be attributed to experimental error. That the curves are insensitive to application of reverse bias suggests this possibility.

These results indicate that the capacities of the tested n-i and m-i junctions are only active at very low frequencies, below 1 Hz. This is probably due to the long emission lifetimes of the deep traps. These long lifetimes keep the depletion regions of these junctions "frozen." Measurements at higher temperatures, where the emission lifetime of the deep traps is reduced will be attempted.

The upper bound of 1 Hz for the frequency response implies that in practical devices, operating at room temperature, as long as bias voltages are either constant or pulsed at frequencies higher

than 1 Hz, there is no reason to be concerned about changes of the width of the depletion layer between the n-type epitaxial layer and the semi-insulating substrate.

3.2.2.2 Complementary Measurements. Preliminary results on photovoltaic effects at the junctions between semi-insulating GaAs and low-resistivity GaAs were discussed in the first semi-annual report. These studies were completed in this period. The purpose was to test the validity of treating junctions between semi-insulating substrates and epitaxial low-resistivity layers, and of metallic barriers on semi-insulating GaAs as normal semiconductor junctions, and simply placing the Fermi level in the semi-insulating material near the center of the gap. This test is important both in device applications and in the analysis of measurements of the type discussed in the former section.

The samples were n-i-m and p-i-m structures of the type discussed in the former section. These configurations are schematically reproduced in the inserts of Figs. 3.2-4 and 3.2-5 where n and p stand for n- and p-type GaAs, respectively, i for semi-insulating GaAs, and m for metal. The n- or p-type layers, with carrier concentrations of $\sim 2 \times 10^{17} \text{ cm}^{-3}$, were grown on semi-insulating GaAs substrates by liquid phase epitaxy. Ohmic contacts were made on the n- and p-type layers. The semi-insulating substrate was

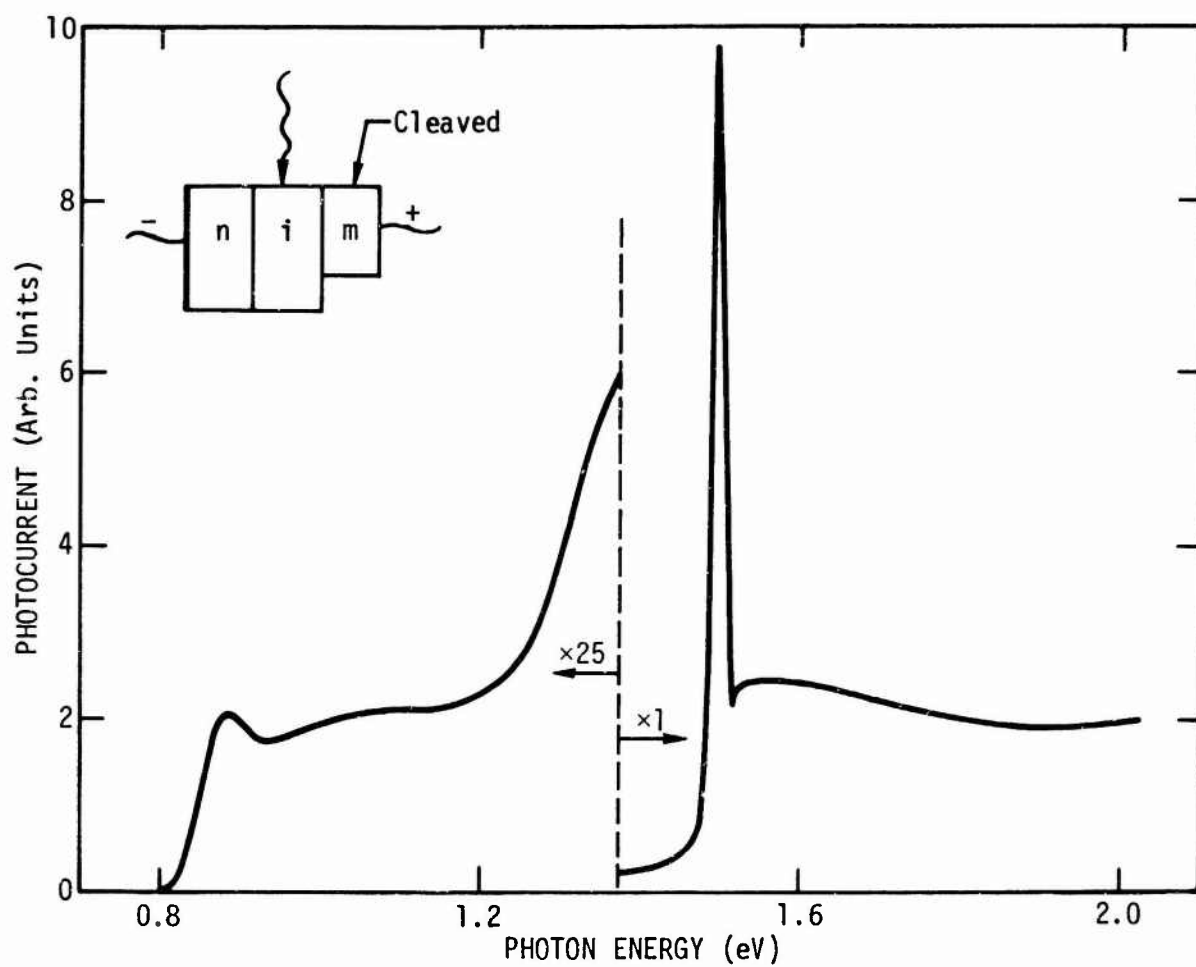


Fig. 3.2-4 Photocurrent spectrum at 4.2°K of an unbiased n-i-m sample illuminated from a cleared side.

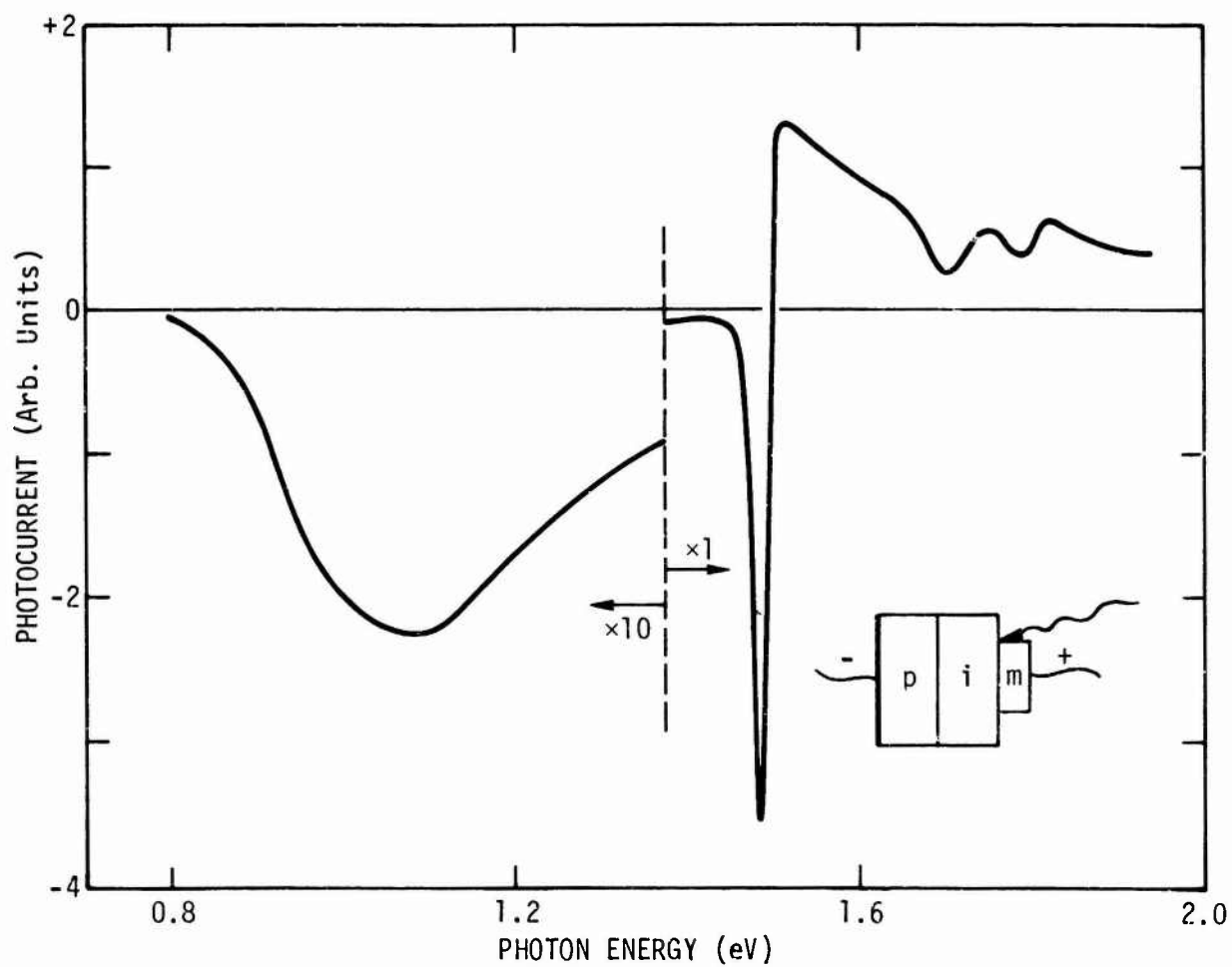


Fig. 3.2-5 Photocurrent spectrum at 4.2°K of an unbiased p-i-m sample illuminated from the metal side.

then polished and etched down to a thickness between 10 and 20 μ m. Aluminum dots were evaporated on the etched surface of the semi-insulating layer. Some n-i-m samples were cleaved exposing a cross section of the structure.

Light from a tungsten lamp was passed through a 0.3m McPherson monochromator and focused on the sample. On the cleaved n-i-m samples the light beam was focused on the exposed cross sections. On the n-i-m and p-i-m non-cleaved samples, the light beam was focused on the metal side. Since the metal dot was opaque for the incident radiation, care was exercised to illuminate the edge of the Al dots, at an angle of approximately 15° with the normal, to insure some penetration under the metal contact. The photocurrent was measured against photon energy with a Keithley 417 picoammeter, with no bias applied to the sample. Similar photocurrent spectra were obtained chopping the light beam at 150 Hz and measuring the photocurrent with a lock-in detector. With this arrangement, photon-energy-dependent phase shifts were observed due to changes in the lifetime of photocarriers. A pyroelectric detector was used for spectral calibration of the intensity of the incident beam. The spectra were corrected so that they represent photocurrent per incident photon. All the measurements were made at liquid He temperature. At room temperature, similar but much broader spectra are obtained.

Figure 3.2-4 shows the intensity of the photocurrent as a function of photon energy for a cleaved n-i-m sample. The sign convention is indicated in the insert. The spectrum shows a sharp photocurrent peak at the energy gap and a continuum at photon energies above the gap. Below the gap, the photocurrent shows some structure, which can be assigned to deep impurities.¹⁴ The spectrum has a sharp threshold at 0.8 eV in agreement with prior observations in Cr-doped GaAs.¹⁵ Non-cleaved n-i-m samples illuminated from the metal side yield similar spectra, except that the structures below the gap are not resolved and the threshold at 0.8 eV is less steep.

The photocurrent spectrum of a p-i-m sample illuminated from the metal side is shown in Fig. 3.2-5. The broad photocurrent structure below the gap is similar to that of the cleaved n-i-m structures. The most prominent feature of this spectrum is the change of sign that takes place at the energy gap.

In order to interpret the change of sign in Fig. 3.2-5, it must be considered that no photocurrent can arise from the bulk of the insulator because there is no applied bias to sweep the photocarriers. Only photocarriers generated at the junctions, where there are built-in electric fields, can give rise to photocurrent in our experiments. At photon energy above the gap, the incident

light has very low penetration, less than $1\mu\text{m}$.¹⁶ Therefore, when the sample is illuminated from the metal side, the above-gap portion of the photocurrent spectrum can only arise from the m-i junction. At photon energies below the gap, the optical absorption is low.¹⁷ Therefore, the incident light penetrates deep into the sample reaching the n-i or p-i junction with negligible attenuation. The change of sign of the photocurrent in the p-i-m sample (Fig. 3.2-5) occurs precisely at the energy gap. This indicates a competing effect between the m-i and the p-i junction, the effect at the p-i junctions being dominant. The effect at the m-i junction becomes dominant only above the gap where light cannot reach the p-i junction. That there is no change of sign in the n-i-m sample when illuminated from the metal side indicates that in this sample the effects of the two junctions are additive.

The band scheme shown in Fig. 3.2-6 is proposed for the n-i-m and p-i-m structures without bias. The Fermi level in Cr-doped GaAs is close to the Cr level (approximately 0.8 eV from the conduction band⁹). Considering that Al Schottky barriers on both n- and p-type GaAs pin the Fermi level at the surface 0.90 eV below the conduction band,¹⁸ presumably because of a high density of surface states, this can also be assumed to be valid for semi-insulating GaAs. This assumption leads to a curvature of the bands as shown on the right side of Fig. 3.2-6. Such band bending is in agreement

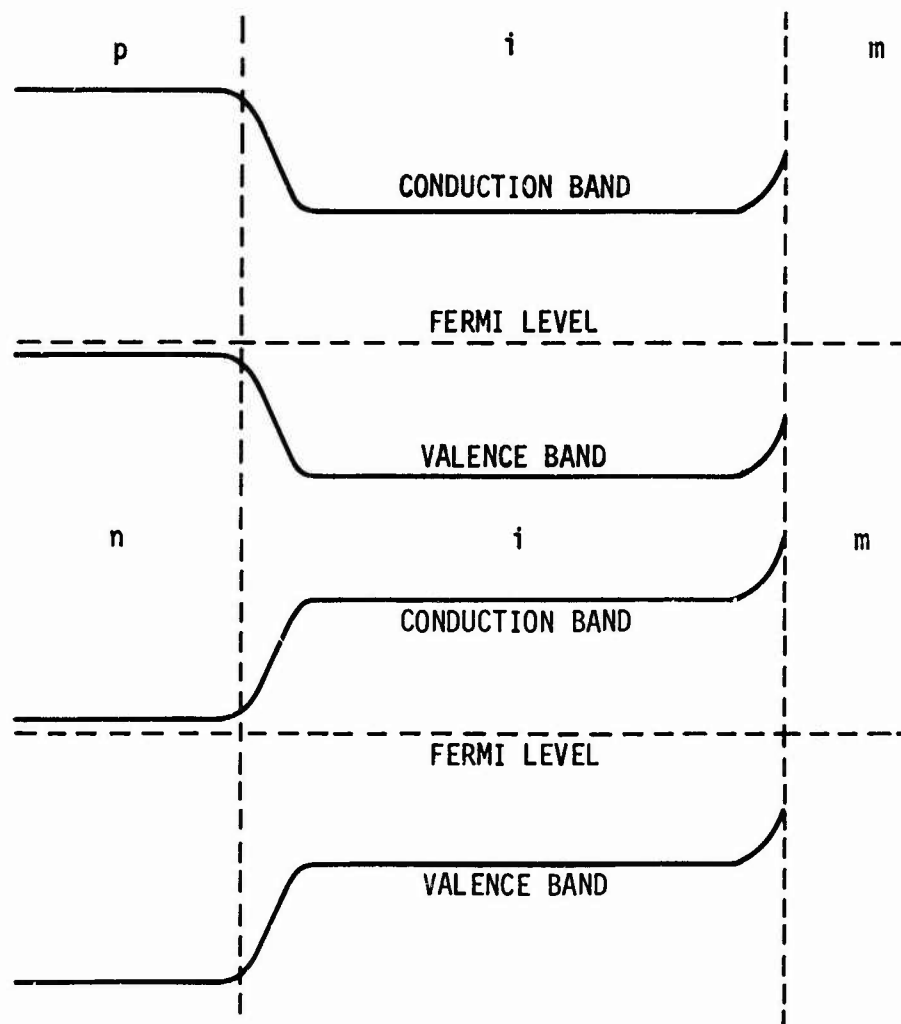


Fig. 3.2-6 Proposed band scheme of the n-i-m and p-i-m structures at zero bias.

with the polarity of the photocurrent excited by above-bandgap photons. It must be noticed that the proposed band curvature requires a positive space charge. Such charge can arise only from neutralization of acceptors which in the bulk are ionized by electrons supplied by background impurity donors.

The below-gap portions of the photoconductivity spectra are dominated by effects at the n-i and p-i junctions, as discussed above. The polarity of the photocurrent is in agreement with the band curvature shown in the left portions of the band scheme of Fig. 3.2-6. Here the n-i and p-i junctions are described by treating semi-insulating GaAs as a p-type material, with the Fermi level close to the C_r level, near the center of the gap.

As to the lack of resolution of spectral structures below the gap and the diminished sharpness of the 0.8 eV threshold when spectra from samples illuminated from the metal side are compared with spectra of cleaved samples (Fig. 3.2-5 vs Fig. 3.2-4), this may be due to filtering of incident light by the semi-insulating layer before the photons reach the n-i or p-i junction.

In conclusion, photovoltaic effects in semi-insulating GaAs can be understood by extension of the behavior of n- and p-type GaAs. In particular, the change of sign of the photocurrent in an unbiased p-i-m structure can be explained in terms of competing photovoltaic

effects at the m-i and p-i junctions. The sign of the effect at the m-i junction indicates that the bands bend at the junction in the manner predicted by assuming that the Fermi level is pinned by high-density surface states, as it is in Schottky barriers on n- or p-type GaAs.

3.2.2.3 Conclusions. Well-defined progress was made in the evaluation of semi-insulating GaAs. The main achievement is the development of n-i-n structures. This allows the determination of trap densities without ambiguities in the interpretation of the results due to the configuration of the sample. The preliminary measurements on the n-i-n structures indicate that trap densities are much lower than impurity densities determined from mass spectroscopy analysis. Some hypothesis in terms of the role of 0 impurities is advanced. Interpretation of photovoltaic effects at junctions between semi-insulating and low-resistivity GaAs, and at Schottky barriers on semi-insulating and low-resistivity GaAs supports the treatment of junctions which involve semi-insulating GaAs as if this material were a normal semiconductor, with the Fermi level near the center of the gap. This further supports the interpretation of the breakdown effect in the n-i-n structure as a "punch-through."

The program of substrate evaluation has matured to the point where evaluation techniques have been defined and are available. Table 3.2-1 shows the scheme of material analysis that will be used in the near future. This scheme is not exclusive of other techniques that may become necessary later on. Conditions are now given for interaction with crystal growth, which is in the spirit of this program.

Table 3.2-1 Scheme of Material Analysis Procedures

Measurements	Nature	Result
Resistivity vs Temperature	Preliminary	Verification of high-resistivity, Fermi level
Breakdown in n-i-n and p-i-n structures	Quantitative	Electron and hole trap densities
Photoconductivity	Complementary	Energy levels of impurities

3.3 n-type Doping of GaAs by Ion Implantation

The work in this area involves the combined efforts of Science Center and Cal Tech personnel. The sputter deposition of films for annealing caps, and subsequent ellipsometry measurements are done at the Science Center. The 2 MeV helium ion backscattering measurements, used to evaluate stoichiometry and density are done at Cal Tech. Implantation of tellurium ions in GaAs samples and annealing after capping are carried out at the Science Center. The

anodization technique used in determining the electron concentration and mobility profiles was developed at Cal Tech and the profiling measurements are performed there. C-V measurements for comparison purposes are sometimes carried out at the Science Center. Since each technique or measurement mentioned is available only at one location, this cooperation makes possible a more complete program than would be possible at either location alone.

3.3.1 Annealing Cap

In the preceding scientific report,¹⁹ results were presented on the annealing of tellurium-implanted GaAs samples using an AlN annealing cap. The AlN films were deposited by reactive sputtering using a general-purpose sputtering system. They contained approximately as much oxygen as nitrogen. In our current work, a new sputtering system used solely for the deposition of films for annealing caps has been used. In order to further explore the effectiveness of AlN as an annealing cap, an attempt was made to lower the oxygen content of the sputtered films. A ratio of oxygen concentration to nitrogen concentration as low as 6% was achieved and it was possible to consistently produce films whose oxygen content was less than 10% of the nitrogen content.

The energy spectrum of 2 MeV helium ions backscattered from a typical film is shown in Fig. 3.3-1. These data indicate that the oxygen content of the film was about 7.4% of the nitrogen content and that the ratio of nitrogen to aluminum in the film was .96. The density of

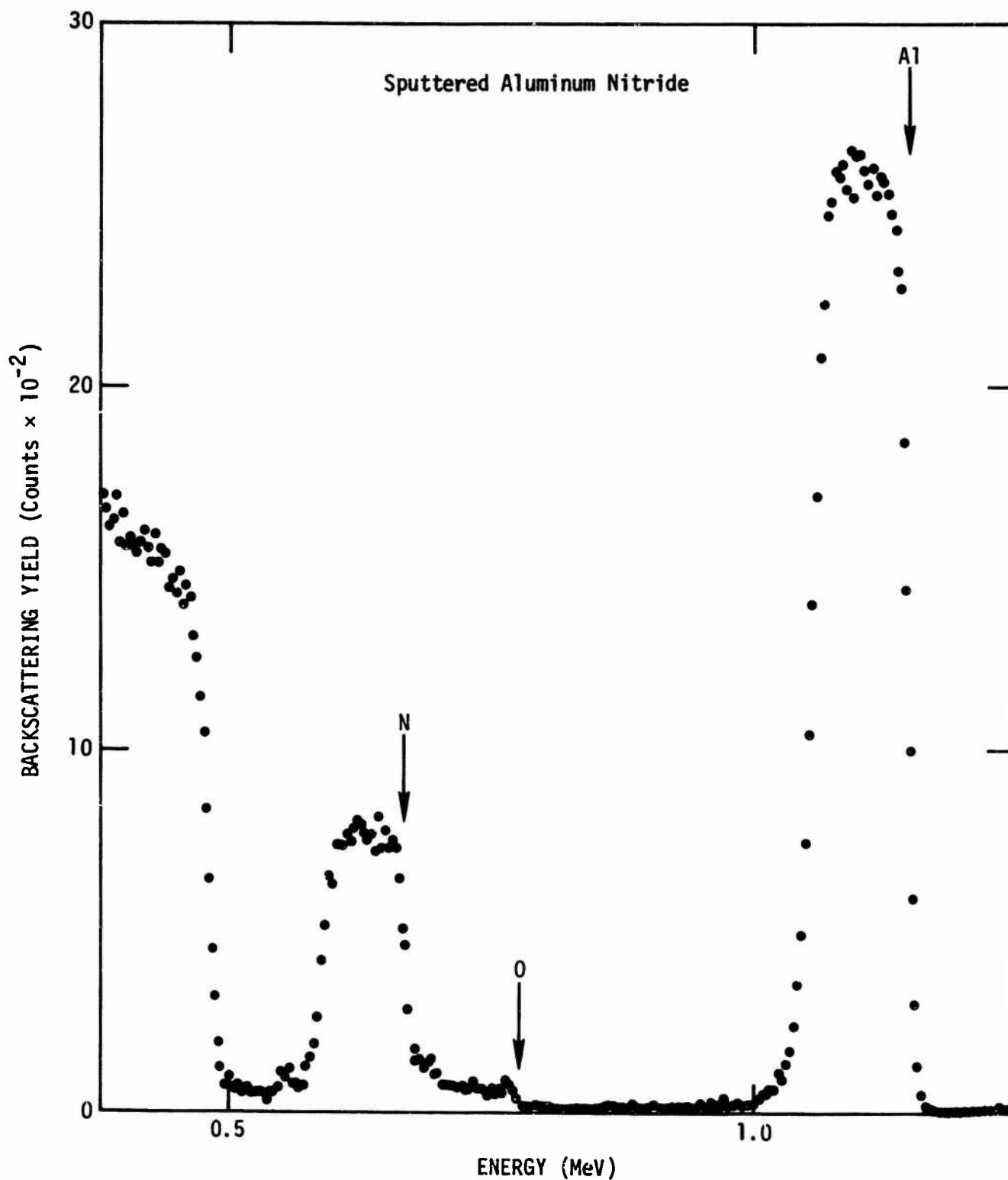


Fig. 3.3-1 Energy spectrum for 2 MeV helium ions backscattered from a sputtered aluminum nitride film.

the film, which was calculated from the backscattering data, and the thickness derived from ellipsometry measurements was 3.7 g cm^{-3} . The index of refraction of these AlN films was usually in the range between 2.05 and 2.10. The backscattering measurements did not detect any impurities in the films besides oxygen.

The decrease in the oxygen content of the sputtered films correlated with an improvement in the vacuum conditions in the sputtering system resulting from repair of several small leaks which were present in the system when it was delivered. This result suggests that a substantial amount of the oxygen content of sputtered AlN films may be due to oxygen in the background gas in the sputtering system.

The AlN film with low oxygen content did not adhere well when deposited on GaAs samples. The adherence appeared to depend on the temperature of the GaAs during film deposition. For temperatures in the range of 400° to 450°C , cracking of the nitride film was observed following deposition. This problem disappeared when the sputtering was carried out with the GaAs held at about 300°C . When GaAs samples were annealed with low-oxygen-content AlN caps, cracking or peeling of the films was usually observed for the annealing temperatures of 800 to 900°C . Several samples implanted with low doses of Te were annealed using these nitride films. C-V measurements made on the samples following annealing indicated that there was little if any electrical activity due to the implanted Te. These

results with low-oxygen-content films may indicate that the higher oxygen content of the previously-used AlN films was important to their success as an annealing cap. We feel that this point should be investigated in the future by introducing controlled amounts of oxygen into the sputtered AlN films.

Reactively-sputtered Si_3N_4 films have been extensively investigated during the past few months. Helium-ion backscattering measurements, ellipsometry measurements, and determinations of etching rate in HF have been carried out on these films. Sputtering conditions have been determined which allow the reliable production of uniform, high-density Si_3N_4 films having a low oxygen content, a low etch rate, and a high index of refraction. Typical values of the etch rate are about 4Å/sec in concentrated HF, with densities of about 3.1 gm/cm³, and values of the index of refraction of about 1.97 to 1.98. Oxygen contents are typically less than 3% of the nitrogen content of the film. These films are deposited at temperatures between 300° and 400°C. The films are somewhat nitrogen-rich with the nitrogen-to-silicon ratio typically lying between 1.5 and 1.6, whereas the stoichiometric ratio would be 1.33. The He-ion backscattering data obtained on one of these films is shown in Fig. 3.3-2.

Annealing experiments have been carried out with the sputtered Si_3N_4 films on unimplanted GaAs samples in order to evaluate the adherence

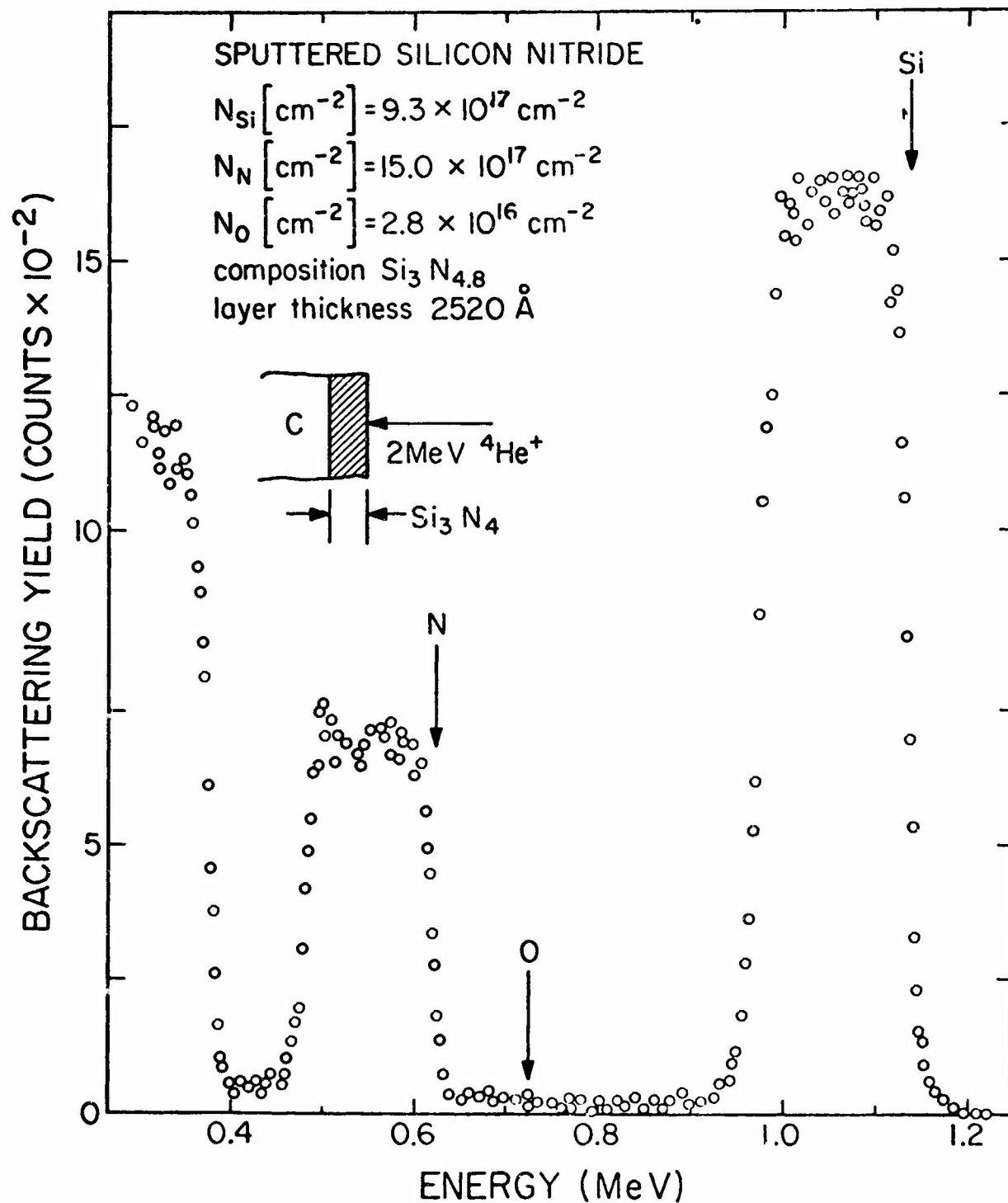


Fig. 3.3-2 Energy spectrum for 2 MeV helium ions backscattered from a sputtered silicon nitride film.

of the films was found to be best when annealing was carried out in a hydrogen atmosphere. Under this condition, good adherence has been observed at temperatures as high as 900°C. Experiments have been carried out in which n-type epitaxial GaAs was annealed using Si_3N_4 as a protective cap. Schottky barrier capacitance voltage measurements were made on the films before and after the annealing was done. Typical data for such an experiment are shown in Fig. 3.3-3. The results indicate that the nitride film was an effective annealing cap and that there was little if any change in the electron concentration in the film as the result of the annealing treatment. A number of Te-implanted GaAs samples have been annealed at various temperatures using 2500Å-thick Si_3N_4 films, with the characteristics described above, as the annealing cap. The results of electrical measurements on these films are described below.

3.3.2 Evaluation of Implanted Layers and Junctions

3.3.2.1 Development of an Anodization Technique for Profiling

Implanted GaAs Samples. Recently, several publications²⁰⁻²⁵ have reported on the possibility of anodic oxide growth on GaAs. In general, constant voltage sources were used and simultaneous film growth and dissolution occurred. In some cases, severe pitting was observed. In this report we describe a procedure which allows the use of a constant current source. N-methylacetamide, which is a common electrolyte for silicon,²⁶⁻²⁸ was found to be applicable to GaAs.

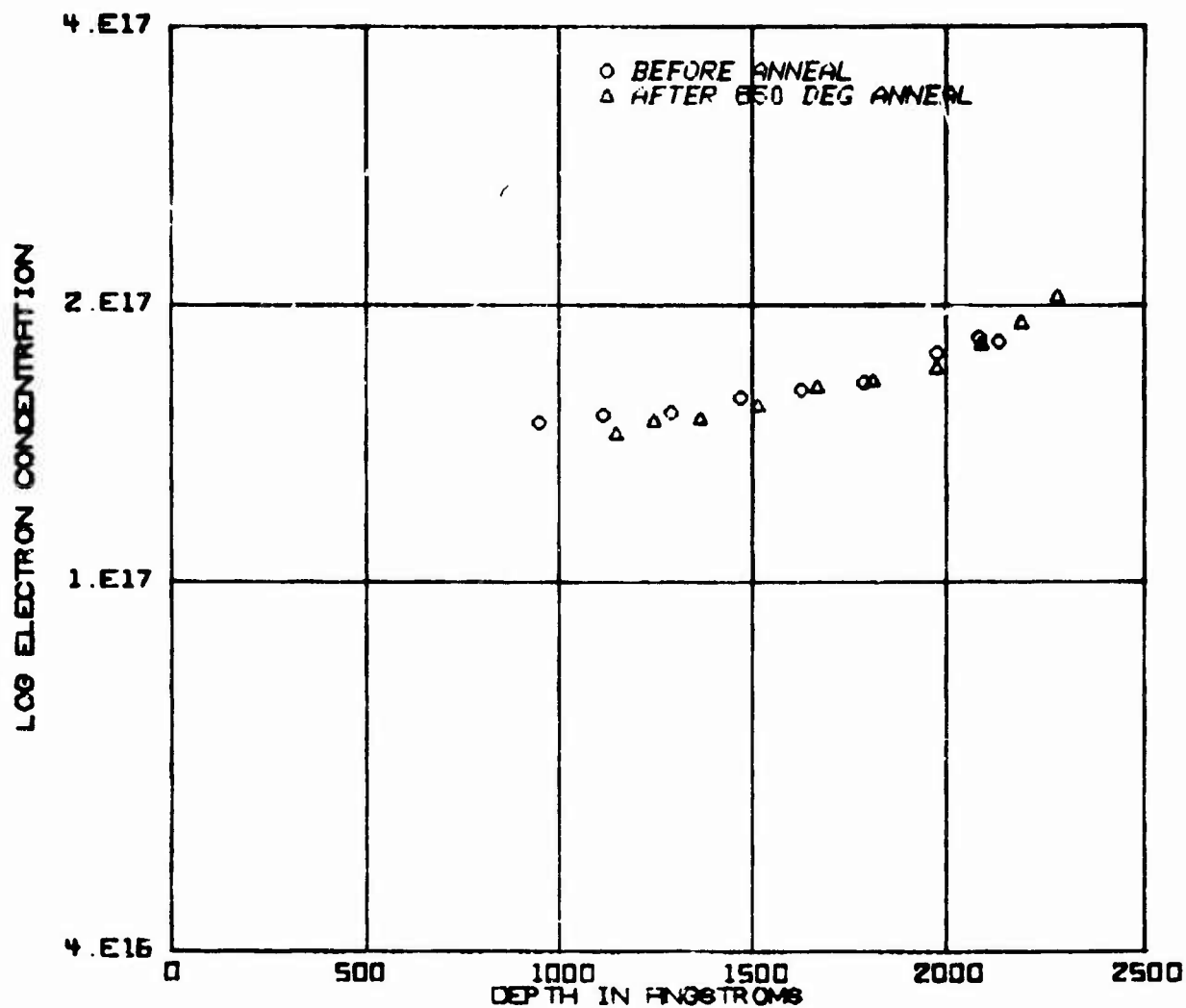


Fig. 3.3-3 Electron concentration vs depth for an epitaxial GaAs film before and after annealing with a silicon nitride cap. These data are based on Schottky barrier C-V measurements.

The material used for evaluation of the anodic oxidation process was generally $\langle 111 \rangle$ oriented, n-type GaAs, silicon-doped with a net donor concentration of 10^{18} cm^{-3} . Usually the anodizations were carried out on a chemically-polished A face. Other samples were etched in a solution of $3\text{H}_2\text{SO}_4:1\text{H}_2\text{O}_2:2\text{H}_2\text{O}$ at 0°C (etch rate $\sim 1000\text{\AA}/\text{sec}$) and about $1\mu\text{m}$ was removed. Growth rates were compared on a few samples of p-type material of $\langle 100 \rangle$ orientation with a net acceptor concentration of $3 \times 10^{17} \text{ cm}^{-3}$.

The anodizations were carried out in a Teflon beaker, described in detail elsewhere.²⁹ Its main features are a vinyl plate with a 5-mm-in-diameter opening which exposes part of the sample surface to the solution and acts as a seal between the sample and the Teflon beaker. A platinum cathode was used and the anode contact was achieved by a gold plate underneath the sample. Generally, the backsides of the samples were only lapped and no effort was taken with respect to back-contact preparation. For large area anodizations, samples were held by a stainless steel clamp and dipped into the solution close to the clamp. In these cases, both sides of the sample could be anodized.

The solution was N-methylacetamide ($\text{CH}_3\text{CONHCH}_3$ --J. T. Baker Chemical Co.) adjusted to various pH-values as described below in detail. A constant current source with a maximum open circuit

voltage of 300V was applied. The voltage increase as a function of time was monitored on a recorder. Generally, the cell voltage was used as a thickness reference and corrections were made by subtracting initial voltage drops.

Determination of the oxide thickness as a function of the forming voltage (i.e., cell voltage minus initial voltage drop) was done by ellipsometry, interferometry and by use of a Talystep. The amount of GaAs consumed in the oxide layer was determined by interferometry, Talystep measurements and He-backscattering. In the latter case a Te-implant was used as a marker³⁰ and the shift of the peak of the profile towards higher energies was used for calibration of the amount of GaAs removed.

Several aspects were considered with regard to the use of N-methylacetamide (NMA) as an electrolyte for anodization. A pure solution has a melting point of 27°C and it is common practice²⁶ to add small amounts of H₂O (5-10%) to lower the melting point. The specific resistance is also known to be high²⁵ and, therefore, in silicon anodization experiments, oxygen-containing electrolytes such as KNO₃ are added to increase the conductivity. It was found that these compounds are not involved in the mechanism of oxide growth.²⁵

On the other hand, it is known²⁰ that in contrast to silicon, native oxides on GaAs are soluble in all common acids (like H_3PO_4 , HCl , H_2SO_4) and that the oxide growth in case of H_2O_2 is sensitive to the pH-value of the solution; a similar behavior may be anticipated for N-methylacetamide. Therefore, in our application of N-methylacetamide to the anodization of GaAs, the pH-value of the solution was considered as an additional parameter when trying to obtain a proper low-resistivity solution.

In Fig. 3.3-5 the influence of H_2O on bath resistance for a given geometry and on the pH-value are shown. For small amounts of H_2O (sufficient to prevent crystallization) the pH-value is close to neutral and the resistance was found to be 23.8 k Ω . Resistance values were measured using two platinum electrodes with $\sim 20 \text{ mm}^2$ each separated about 1.5 cm. With increasing content of H_2O , the resistance can be lowered by almost a factor of 2 but simultaneously the pH-value of the solution decreases to an acidic character. Anodizations carried out on n-type GaAs at a current density of 0.5 Ma/cm² resulted in an oxide growth for a ratio of H_2O to NMA less than 1 but showed severe pitting. Worm-like craters about 50 μm deep were formed; areas between these showed homogeneous oxide growth. No relation to crystal orientation (preferential oxidation) or surface preparation of the samples could be found. The density

of the defects increased with increasing amounts of H_2O . For H_2O to NMA ratios >1 , the anodization turned into an etching process.

The results of Fig. 3.3-4 indicate that two competing mechanisms are involved at pH-values below 7. Oxide growth and thickness for a given reference voltage were found to be enhanced at increased current densities but simultaneous dissolution presumably due to the acidic character of the solution could not be suppressed. No reproducible thickness vs voltage relationship could be achieved.

Further experiments were performed at pH-values above 7. Figure 3.3-5 shows the bath resistance as a function of pH-value adjusted by NH_4OH . A decrease in resistance by a factor of 6 is observed when the pH is adjusted to 8.3. At this value very homogeneous layers could be obtained and no further influence of oxide thickness on current density was found, which suggests that dissolution of the oxide was suppressed to a very small amount. At pH-values above 10 a slight dependence of oxide thickness on current density was found due to the fact that the layers are soluble in NH_4OH .

For a pH-value of 8.3 the current density was chosen to be 0.5 Ma/cm^2 which results in a cell voltage increase of 9.5 V/min . A typical cell voltage versus time plot is shown in Fig. 3.3-6. The initial voltage drop is 3.5 volts and represents the total voltage

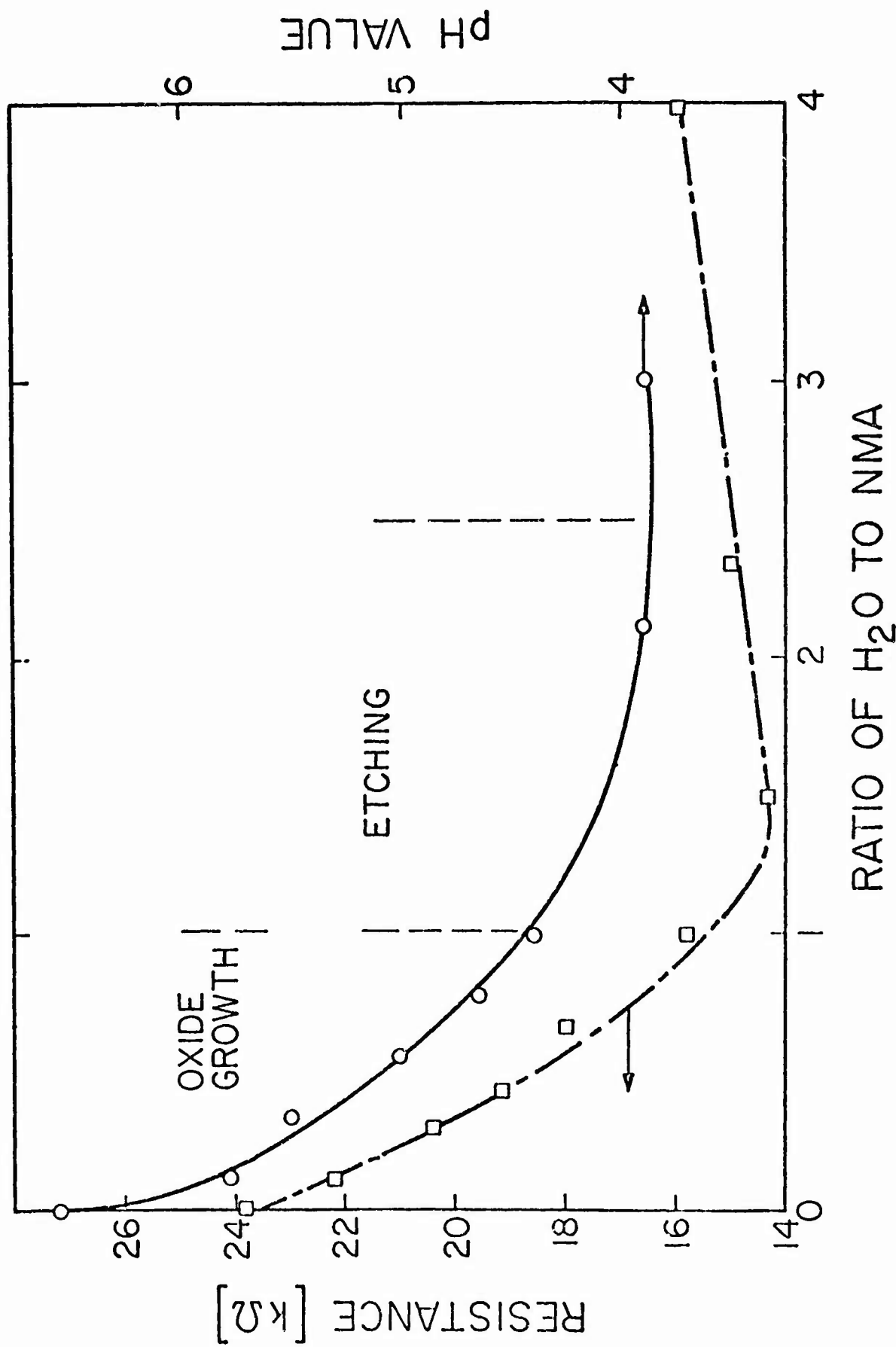


Fig. 3.3-4 Resistance and pH dependence of NMA-solution on H₂O content.

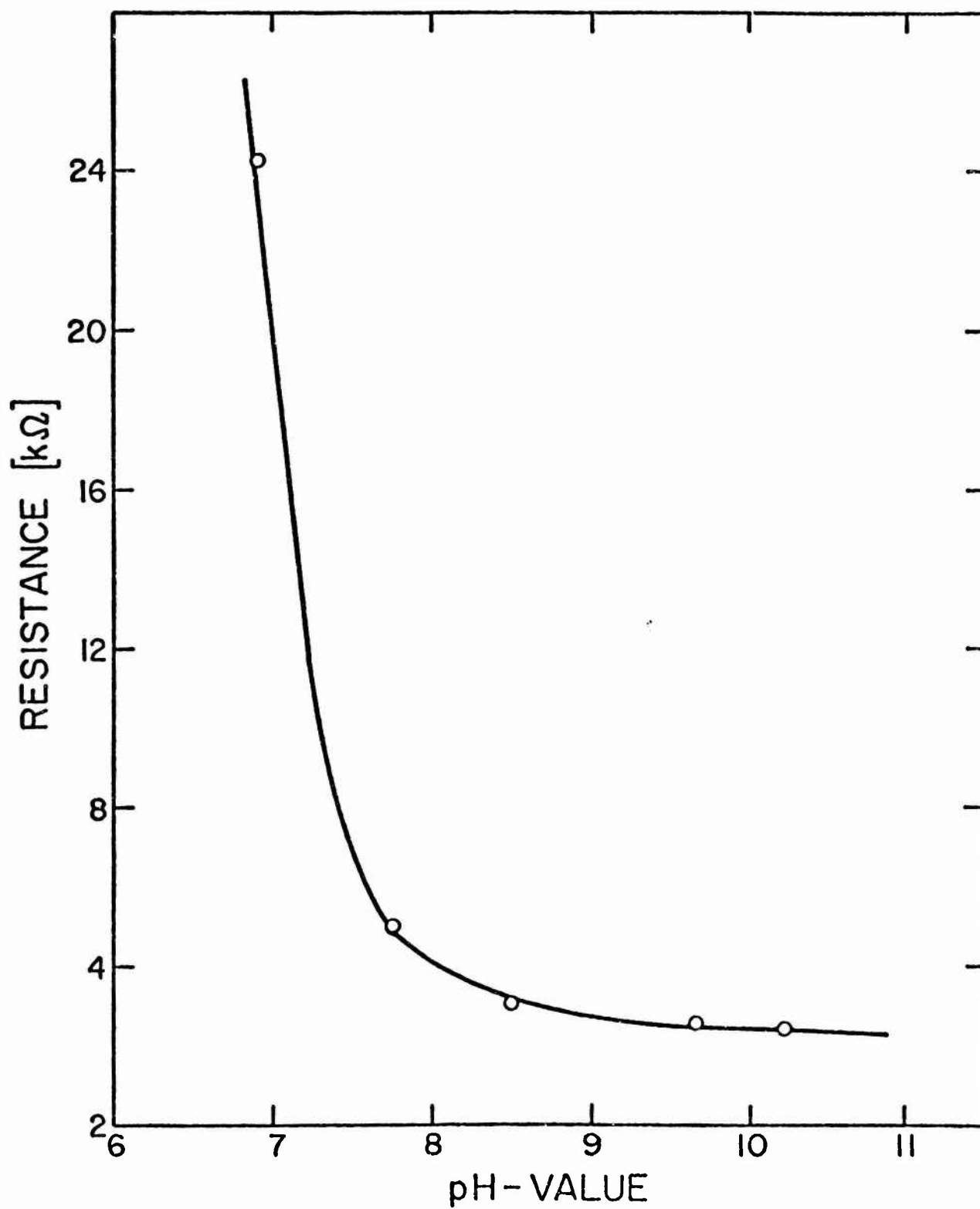


Fig. 3.3-5 NMA bath resistance versus pH-value adjusted by NH_4OH .

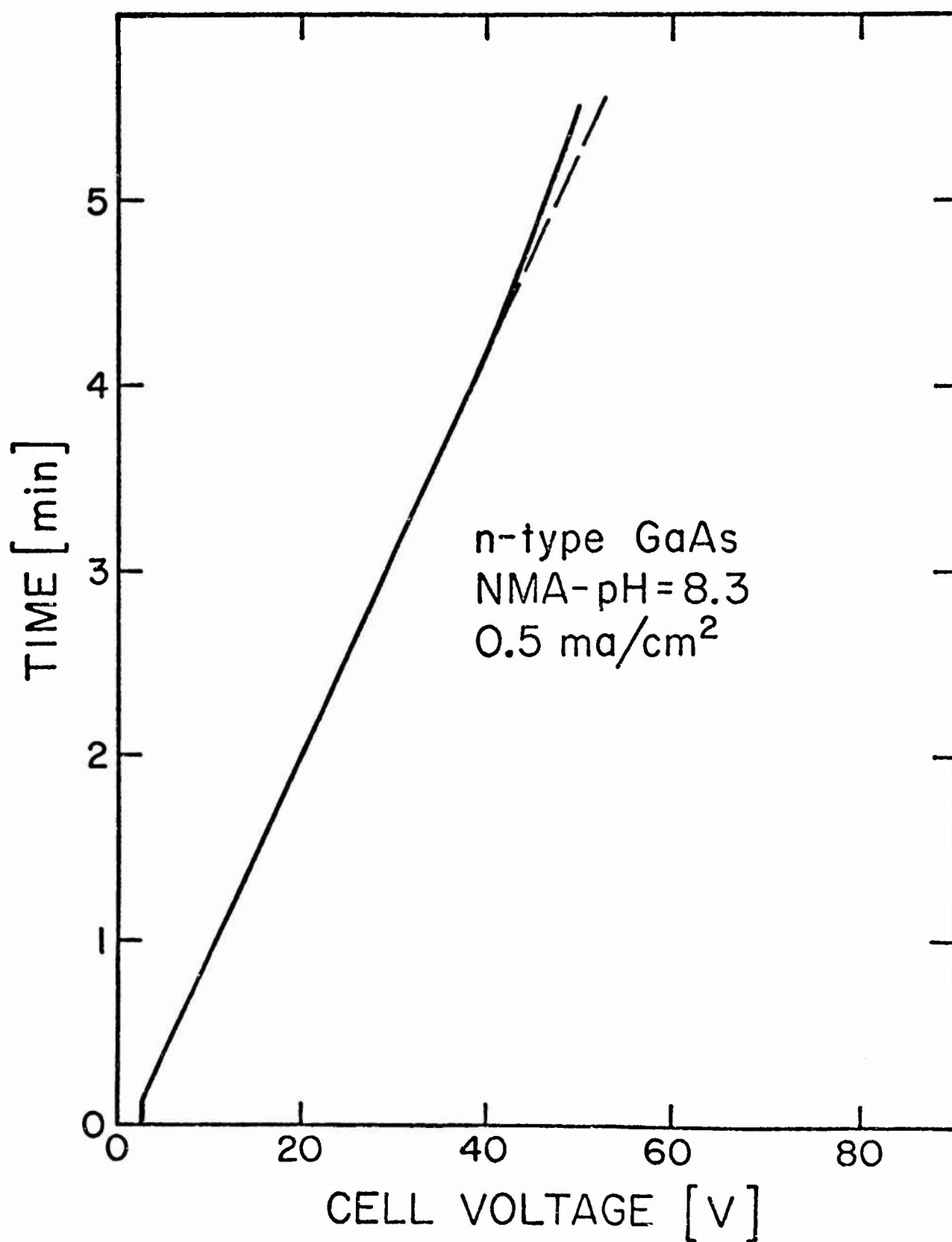


Fig. 3.3-6 Cell voltage vs time plot for anodization in NMA adjusted to pH = 8.3.

drop across electrolyte, semiconductor bulk and back-contact. Generally, for the first anodization of a polished surface a slightly higher voltage drop was observed than for following anodizations after layer removal. A light source was found not to be necessary for voltages up to 50V. In order to reproducibly approach a certain voltage, the reference voltage was chosen to be larger than the desired voltage and as soon as the desired voltage was reached, the current source was switched off. This determined the applied current density, which should allow a reasonably slow approach to a desired voltage value. For voltages above 40V a slight nonlinearity in the voltage time plot is observed, as can be seen in Fig. 3.3-6. The nature of this effect was not carefully investigated; however, it was found that using a light source and increasing the current density by a factor of 3 the deviation from a linear cell voltage versus time relationship occurs at about 80V. Since the main emphasis of this work is to demonstrate a technique which allows successive removal of thin layers (100-300Å), the voltage range above 40V was not investigated in detail.

A series of oxides was prepared on chemically-polished p-type surfaces, the cell voltage was used as a reference and the voltages were chosen between 20V and 60V. In all cases, an initial voltage

drop of about 3V was observed and subtracted from the cell voltage to give the forming voltage which defines the x-axis in Fig. 3.3-7. The solid line in Fig. 3.3-7 represents the average oxide thickness versus forming voltage for different techniques. The open circles were obtained from ellipsometry measurements. The refractive index of the oxide layers was found to be $n = 1.815 \pm 0.005$ over the entire voltage range similar to that found by Dell'Oca, et al.²² From the slope an oxide growth rate of 20.2Å/volt was obtained. For comparison, Talystep and interferometer measurements were performed on some of the samples. Photoresist processing was used to remove part of the oxide and to create a well-defined step. In the case of interferometer measurements, Al was evaporated on the samples to create a high reflecting surface. The observed growth rate agrees very well with results by Logan, et al.,²⁰ obtained on abrasively-polished surfaces. For comparison, p-type material with a carrier concentration of $3 \times 10^{17} \text{ cm}^{-3}$ was anodized. In a first approach, the colors of the oxide layers appeared identical to the colors obtained on n-type material. Ellipsometry measurement confirmed an identical 20.2Å/volt thickness to voltage relationship. The refractive index also turned out to be identical. Identical growth rates were obtained for both chemically polished and etched surfaces on n- and p-type material. Generally for the first anodization a somewhat higher initial voltage was found

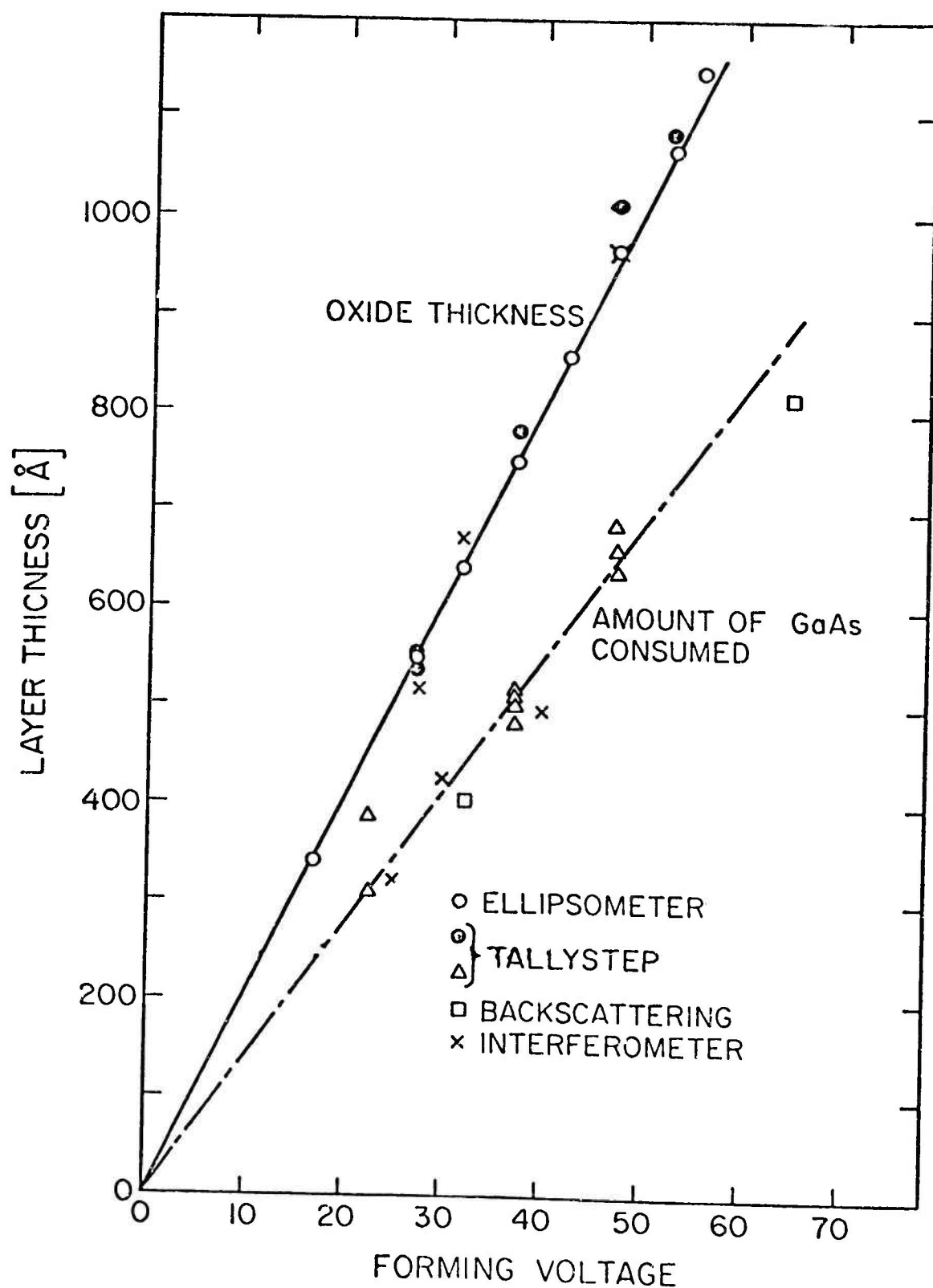


Fig. 3.3-7 Oxide thickness and amount of GaAs consumed vs forming voltage.

compared to following anodizations. This difference may be indicative of changes in surface appearance. Since the nature of this difference is not known, it is difficult to deduce a change in growth rates. Using the forming voltage as a reference for the oxide thickness, no change in growth rate was found on successively anodized samples. No preferential oxidation either due to surface roughness or changes in surface homogeneity was found for as many as 27 successive anodizations, ($\sim 1\mu\text{m}$ of GaAs removed).

The amount of GaAs consumed in the oxide layer was primarily measured by Talystep. For comparison, interferometer measurements were taken. In order to develop a step in the material which corresponds to the amount of GaAs consumed in the oxide, a first oxide was grown; then part of this oxide was removed by photomasking and a second oxide was grown on this area. The oxide thickness was measured on both areas after first and second anodization by ellipsometry in order to ensure that no further growth takes place on the original first oxide. Thus, the difference in oxide heights corresponds to the amount of GaAs consumed. From the dotted line in Fig. 3.3-7, the average amount of GaAs consumed in the oxide layer corresponds to $13.4\text{\AA}/\text{volt}$.

A slightly lower amount of material consumed was found by backscattering measurements as indicated in Fig. 3.3-7. A dose of $2 \times 10^{15} \text{ cm}^{-2}$ Te was implanted at 350°C into n-type GaAs at an energy of 400 keV. 2.5 MeV He^+ backscattering was used to determine the implanted Te profile. Energy-to-depth conversion³¹ of the backscattered spectrum allows the determination of the mean projected range of Te. After anodization and layer removal, the Te peak is closer to the surface and the shift corresponds to the amount of GaAs consumed in the oxide. It was found that the Te-profile is not changed by the oxide growth, which is a basic assumption for electrical profile determination by successive layer removal.

3.3.2.2 Electrical Profiles of Te-Implanted GaAs. Successive anodization and layer removal has been used to evaluate electrical carrier concentration profiles by sheet resistivity and Hall measurements. Semi-insulating, Cr-doped GaAs was implanted with 400 keV tellurium ions at 350°C . The sample preparation for "in situ" stripping and electrical measurements was done by the following procedure. First, four Au-Ge-Ni contacts were evaporated (diameter $\sim 1.5 \text{ mm}$) and alloyed at 450°C for 45 sec in forming gas. In a photoresist step (KMER) a van der Pauw-type pattern was defined and mesa-etched to $3.3 \mu\text{m}$. A sample holder described elsewhere in detail²⁹ was used to both perform Hall and sheet resistivity

measurements and for anodization of the exposed area. The main feature of this sample holder is a spring-loaded Teflon insert which seals the mesa pattern along the dashed line shown in the schematic of Fig. 3.3-8 and protects the electrical contacts against the solution. A platinum wire was used as the cathode and the four contacts were connected together to serve as the anode during oxide growth. After each anodization the oxide was removed in diluted H_3PO_4 (1:1 with H_2O) and the sample was rinsed in de-ionized H_2O and methanol and then dried in a dry nitrogen flow.

Using the technique described in the preceding paragraph, it was generally possible to profile implanted samples to a depth at which the remaining sheet electron concentration was about $5 \times 10^{10} \text{ cm}^{-2}$. This corresponded to a sheet resistivity greater than $10^5 \Omega/\text{square}$. Under these conditions of electron concentration and sheet resistivity, the ability to profile further was limited by the equipment used for the electrical measurements. It sometimes happened that one of the contact arms etched more rapidly in the region of the Teflon seal than the rest of the exposed sample area. In these cases, it was not possible to carry the profile measurements to a depth where they were limited by the ability to make the electrical measurements as described above. In

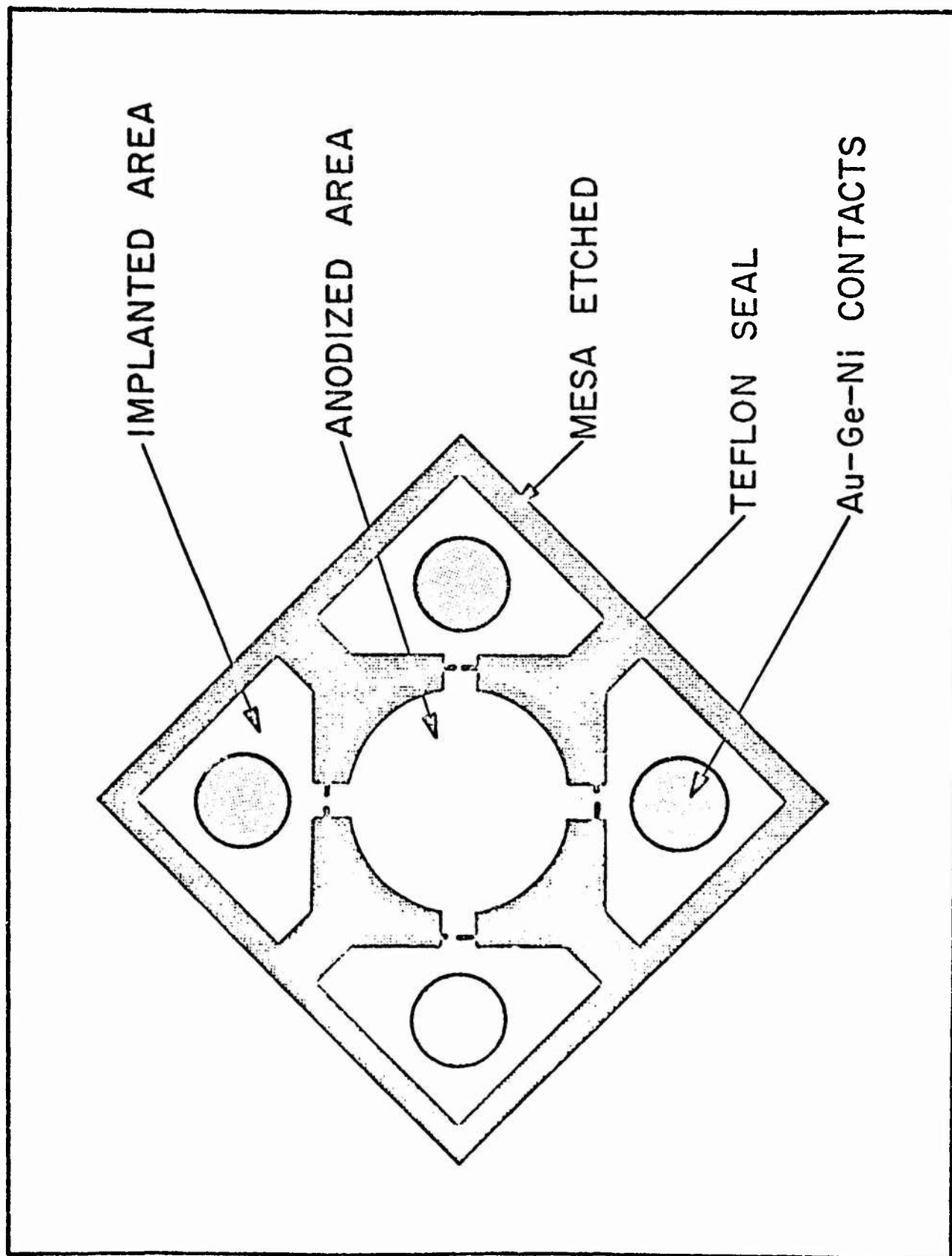


Fig. 3.3-8 Schematics of mesa-etched van der Pauw pattern employed for layer removal by anodic oxidation.

most cases, however, it has been possible to account for all but a few percent of the carriers introduced into semi-insulating GaAs by Te implantation.

Data for several samples implanted with 10^{13} Te ions/cm² and annealed for 10 minutes at different temperatures are shown in Fig. 3.3-9, along with the range distribution for 400 kv Te in GaAs calculated from the LSS³² range theory. The profile measured for the sample annealed at 850° is much deeper than those for the other two samples. The values of the remaining sheet electron concentration in the samples annealed at 800° and at 900° indicate that the electron concentration profile in these samples cannot be nearly as deep as that in the sample annealed at 850°. In all three cases the distribution is somewhat broader than would be predicted by the LSS range theory, and the peak electron concentrations are somewhat below the peak Te concentration predicted by this theory. The greater depth shown for the sample annealed at 850° and the fact that the carrier concentration in the region of the peak is higher than for the 900° anneal sample are not understood at present. It is possible that this is an anomalous result which will not be repeated in other samples annealed at 850°. The mobilities as a function of depth in these 10^{13} Te implants are shown in Fig. 3.3-10. These data indicate that for the 10^{13} Te

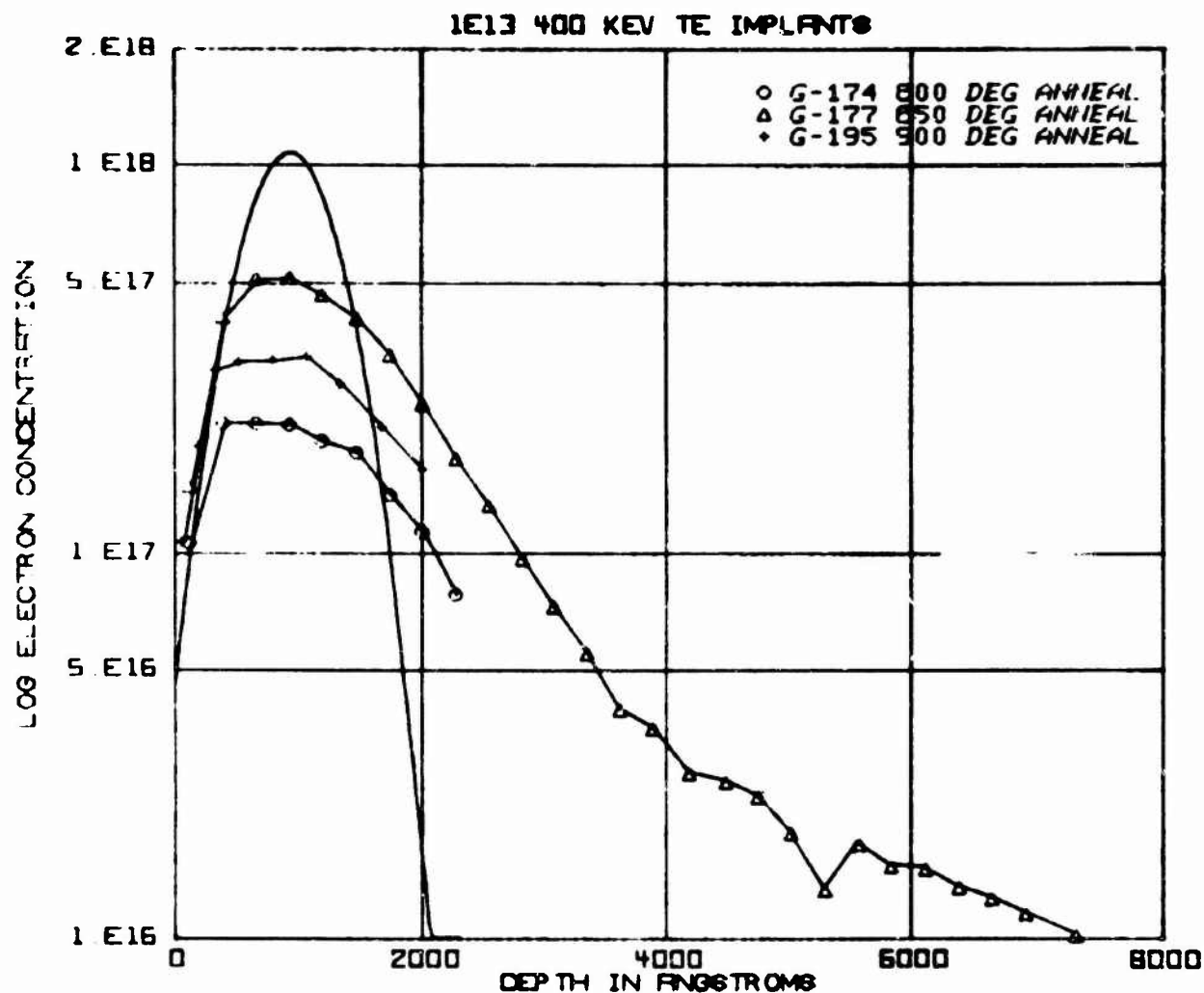


Fig. 3.3-9 Electron concentration vs depth for Cr-doped GaAs implanted with 1×10^{13} tellurium ions/cm² at 400 keV and annealed at the indicated temperatures for 10 minutes.

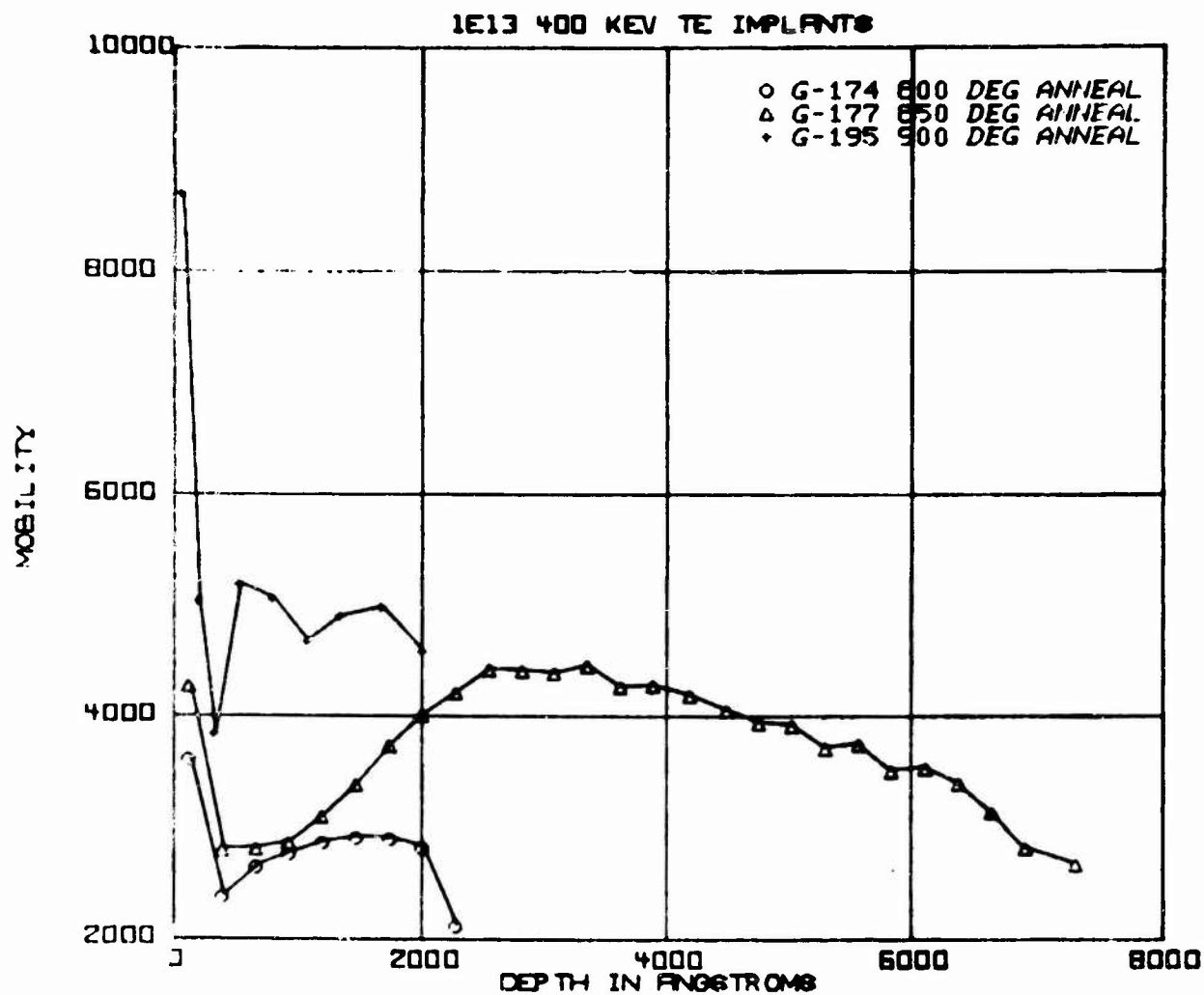


Fig. 3.3-10 Mobility vs depth for the samples of Fig. 3.3-9.

implants the mobility in the sample may be increased by increasing the annealing temperature. There is a tendency for the mobility to decrease at greater depths where the electron concentration is also decreasing. This is shown more explicitly in Fig. 3.3-11 where the mobility is plotted vs the log of the electron concentration. This figure also includes a curve derived from data on epitaxial GaAs samples which indicate approximately the maximum mobility to be expected as a function of the electron concentration.³³ It can be seen that for the 850° annealed sample in the vicinity of electron concentrations of $3 \times 10^{17} \text{ cm}^{-3}$ the mobility is nearly as high as would be expected as for the 900° anneal. Some of the points even lie above the curve for epitaxial samples. This indicates that good mobility values can be obtained for annealing temperatures in the range of 850 to 900° at doses of 10^{13} . It can also be seen that as the electron concentration decreases the mobility for the sample annealed at 850° falls significantly below the values for the epitaxial samples.

Electron concentration profile data for samples implanted with 10^{14} Te ions/cm² are shown in Fig. 3.3-12. The LSS range curve is not included on this figure, but the predicted Te concentration at any depth would simply be 10 times greater than that shown in the curve in Fig. 3.3-9. In contrast to the samples implanted with

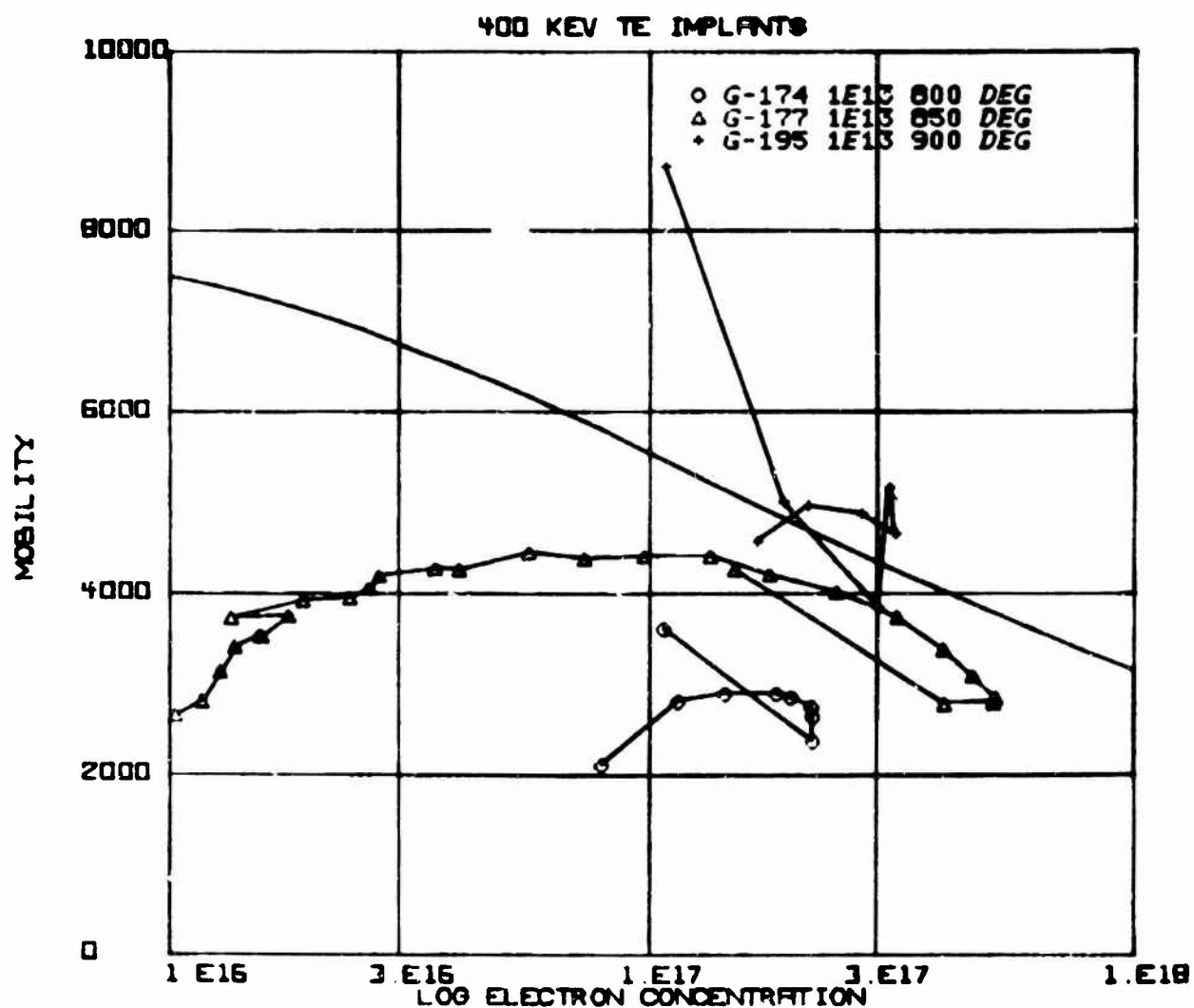


Fig. 3.3-11 Mobility vs electron concentration for the samples of Fig. 3.3-9. The curve without points is based on mobility data for high-quality epitaxial GaAs samples.¹⁵

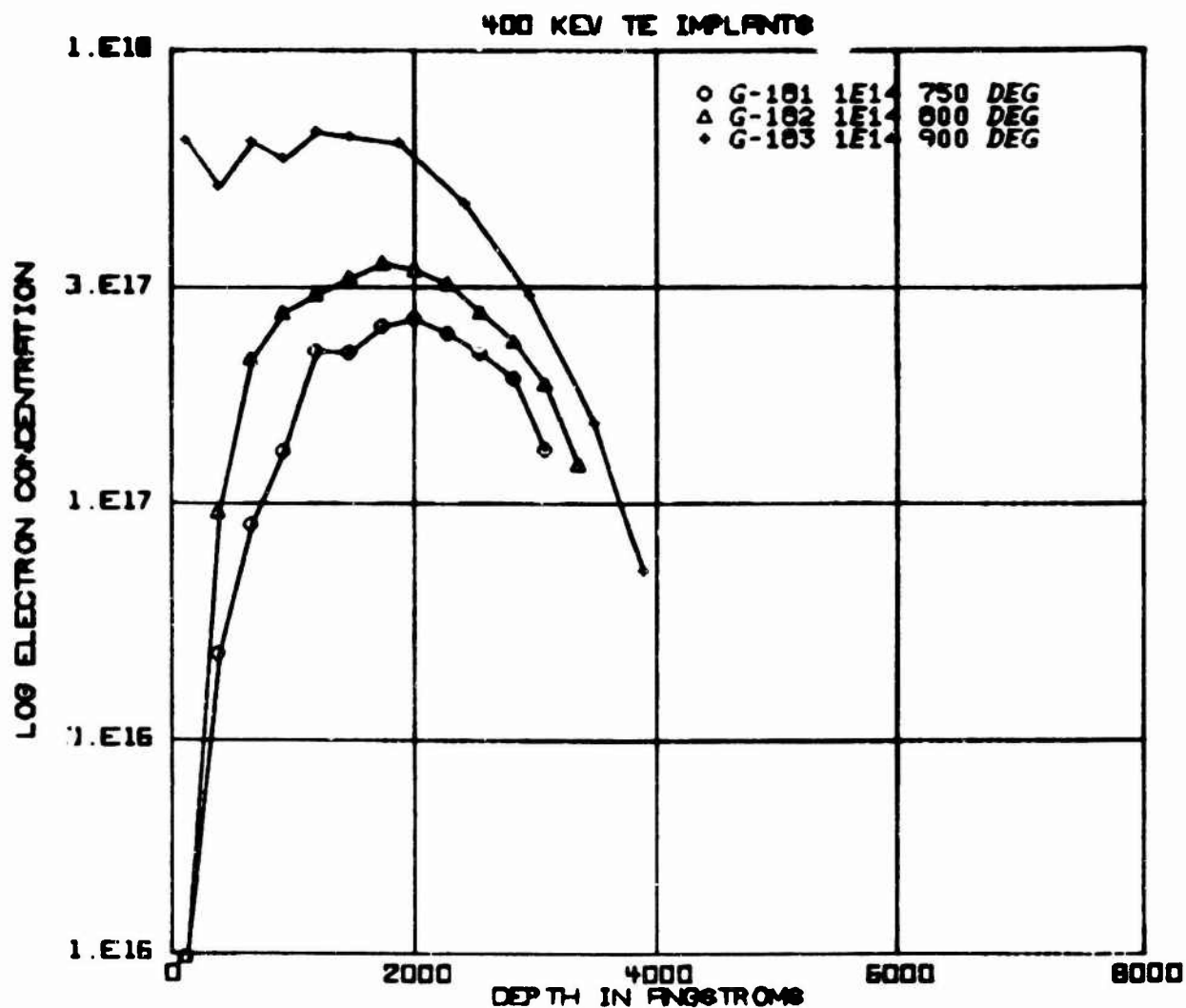


Fig. 3.3-12 Electron concentration vs depth for Cr-doped GaAs implanted with 1×10^{14} tellurium ions/cm² at 400 keV and annealed at the indicated temperatures for 10 minutes.

10^{13} Te ions/cm², the data shown in Fig. 3.3-12 exhibits no tendency for the electron concentration to peak in the vicinity of the projected range of the tellurium; i.e., the peak in the LSS range curve in Fig. 3.3-9. The electron concentration distributions are rather flat and extend to depths significantly beyond the LSS range curve. The corresponding mobility data are shown in Fig. 3.3-13. In this case, the mobility in the vicinity of the projected range of the tellurium, where the disorder produced during implantation would be greatest, is much lower than for the samples implanted with 10^{13} Te ions/cm². The mobility data for all three samples shows a very similar dependence on depth, increasing as the depth increases, except for the last point on each curve. The dependence of the mobility on electron concentration is shown in Fig. 3.3-14 where a comparison with the values from epitaxial material is again included. It can be seen from this figure that the low mobility values obtained at depths of about 1000Å to 2000Å are well below the best mobility values which might be expected at the electron concentrations observed at those depths.

There is considerable difference in the electron concentration profile measured for a dose of 10^{13} Te ions/cm² and those measured for a dose of 10^{14} Te ions/cm². In order to show this difference more

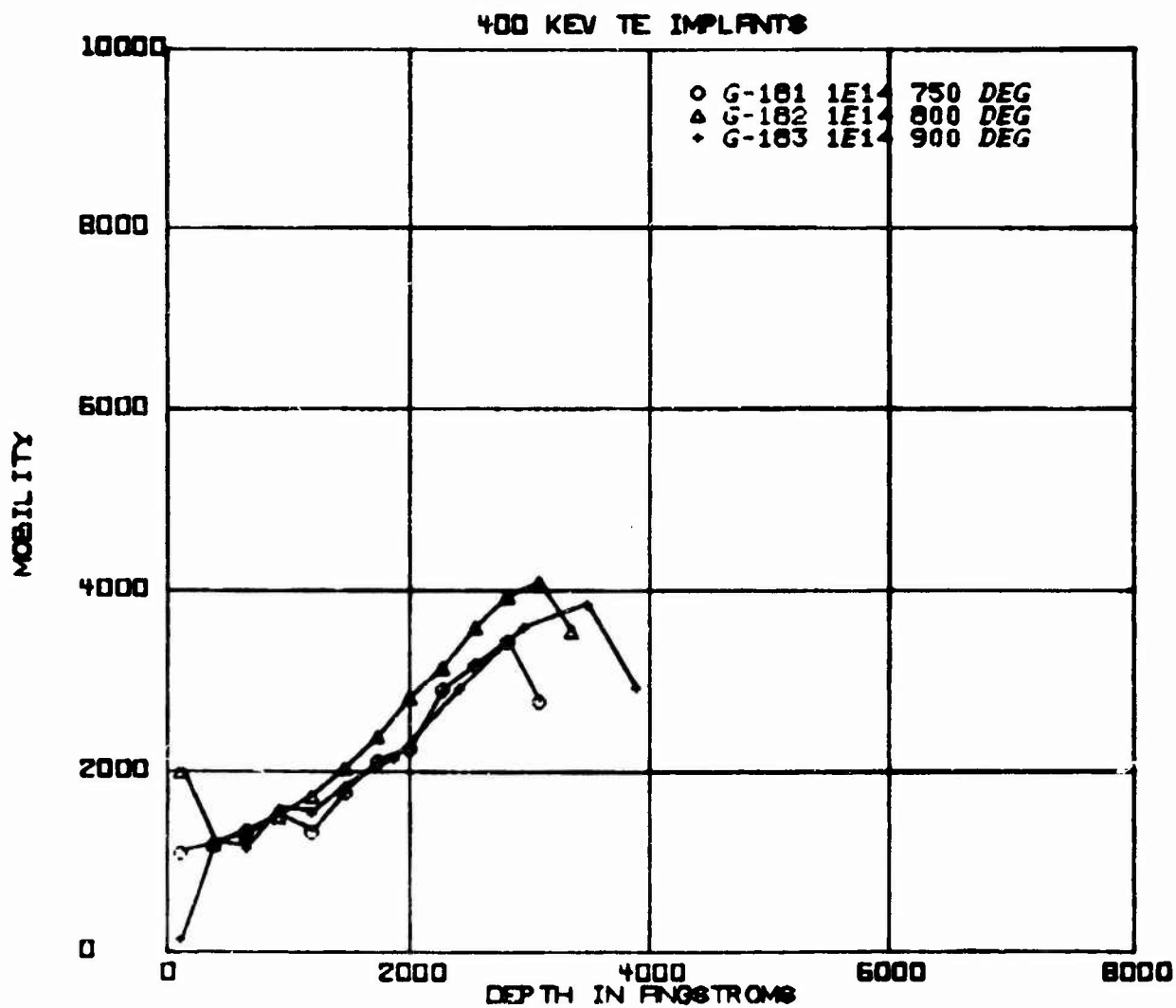


Fig. 3.3-13 Mobility vs depth for the samples of Fig. 3.3-12.

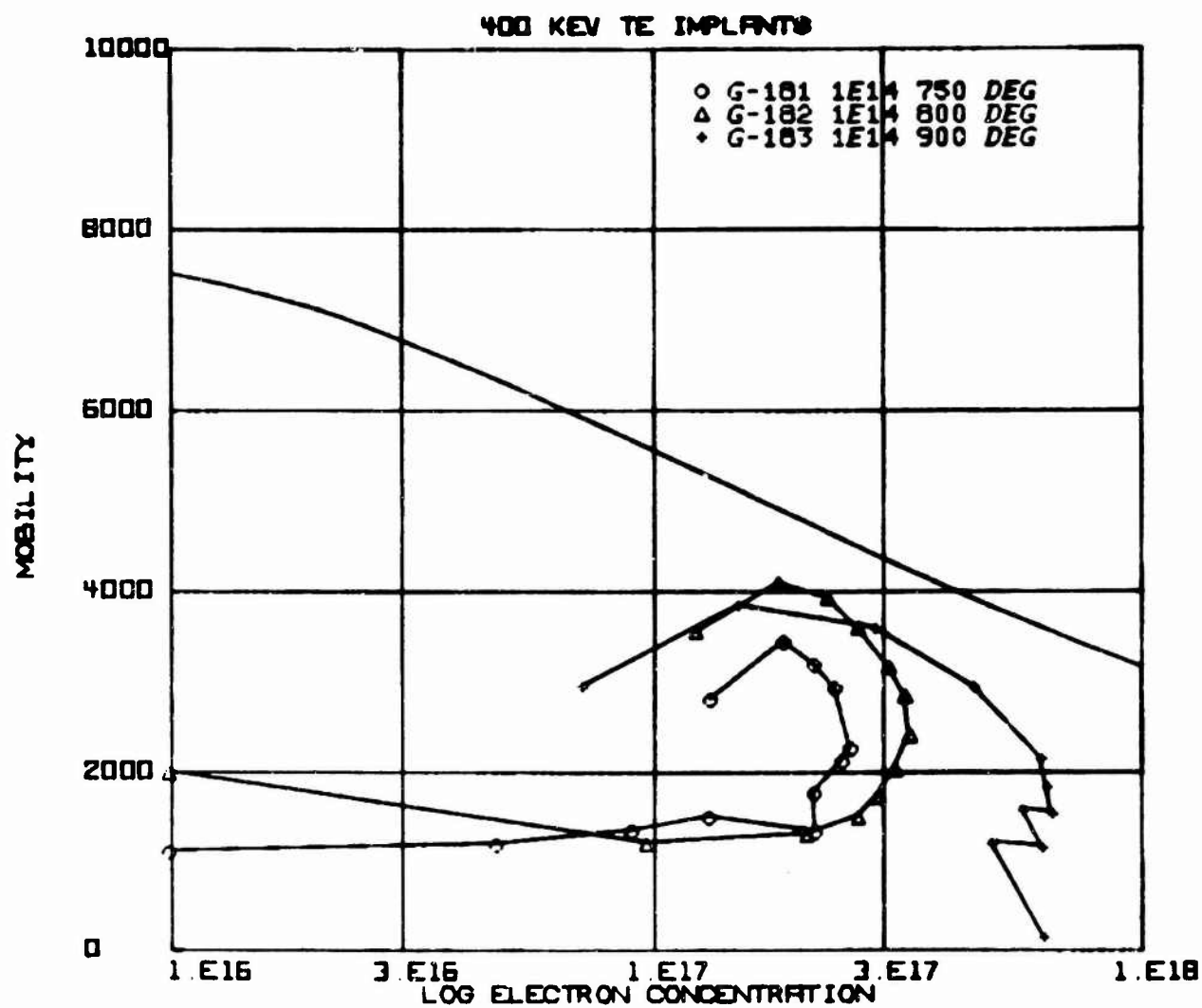


Fig. 3.3-14 Mobility vs electron concentration for the samples of Fig. 3.3-12. The curve without points is the same as in Fig. 3.3-11.

clearly, data for a 10^{13} implant and a 10^{14} implant annealed at 800°C are presented in Fig. 3.3-15. Near the surface of the sample the electron concentration is higher in the sample which was implanted with 10^{13} Te ions/ cm^2 than in the one which was implanted with 10^{14} Te ions/ cm^2 . At depths beyond about 600Å or 700Å, the higher dose sample exhibits a higher electron concentration, but the peak electron concentration obtained is only about one-and-one-half times that observed for the sample implanted with 10^{13} Te ions/ cm^2 . One possible explanation for the low mobilities and low electron concentrations observed in the samples implanted with 10^{14} Te ions/ cm^2 is that there has been incomplete annealing of the disorder produced during the implantation of the tellurium. This disorder should have its greatest value at a depth slightly less than the projected range of the tellurium; that is, at about 900Å. Incomplete annealing of this disorder could result in the presence of defect centers in the GaAs which might act both to compensate the implanted tellurium, and as scattering centers for the electrons, resulting in a lowered mobility. It is probable that the greater width of the electron distribution for the samples implanted with 10^{14} Te ions/ cm^2 is due to an enhanced diffusion effect. That is, that the tellurium diffuses to depths of several thousand Ångstroms as a result of the high defect concentration present near the surface of the implanted sample. Some indication

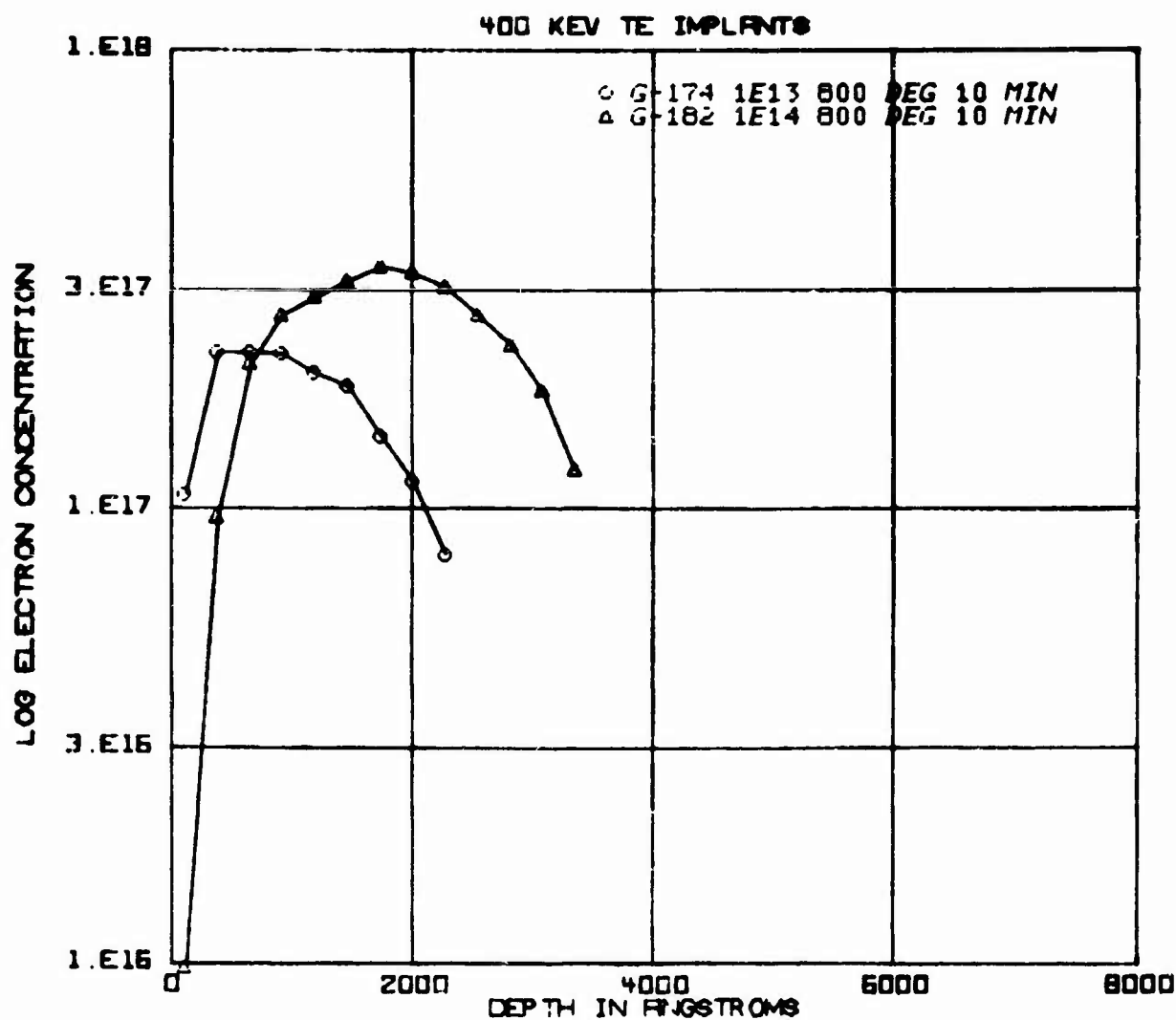


Fig. 3.3-15 Comparison of electron concentration profiles for samples implanted at 400 keV with 1×10^{13} or 1×10^{14} tellurium ions/cm² and annealed at 800°C.

of enhanced diffusion effects in the lower dose samples is also apparent since the profiles in this case extend somewhat beyond the predictions of the LSS range calculation. However, the effect appears to be much smaller than for the samples implanted with 10^{14} ions/cm². It should be pointed out that the penetration of tellurium beyond the depths predicted by the LSS range theory may also be due to channeling effects as well as to the possibility of enhanced diffusion. Future experiments are planned in an attempt to evaluate the possible contribution of channeling effects to this deeper penetration of the tellurium.

The profiles observed in the present work for samples implanted with 10^{14} Te ions/cm² are somewhat different from those reported in the preceding scientific report¹⁹ for similar doses of tellurium implanted into p-type GaAs and annealed with either a Si₃N₄ or an AlN cap. The implantation energy in this earlier work was 220 keV, and a peak in the electron concentration as high as 8×10^{18} /cm³ was observed at a depth corresponding approximately to the expected projected range of tellurium at this implantation energy. It is not clear why similar peaks have not been observed in the present work. It may be that the greater implantation energy plays a role through the greater total amount of disorder introduced in the GaAs. The use of Cr-doped semi-insulating substrates rather than p-type

may be important. Another possibility is that the Si_3N_4 caps are not acting as the perfect protection for the GaAs during annealing resulting in some loss of electrical activity near the surface. Further work will be required in order to understand these differences.

Another feature of the present data which deserves comment is the tendency of the mobility to decrease as the electron concentration in the sample is decreasing at depths of several thousand Ångstroms. This suggests that the concentration of charged defect centers in the sample is increasing with increasing depth, which would not normally be expected. The explanation for this effect is not clear at present. One possibility is that the centers responsible for the decreasing mobility involve the chromium doping of the substrate material in some manner. If this were established, it might provide a useful technique for studying chromium-doped, semi-insulating substrate material.

The results presented above show that useful profile data can be obtained in implanted GaAs samples using the anodization-stripping technique which has been developed. The data also suggest that the sputtered Si_3N_4 films currently being used as annealing caps are reasonably effective in this application.

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The results presented above show that useful profile data can be obtained in implanted GaAs samples using the anodization-stripping technique which has been developed. The data also suggest that the sputtered Si_3N_4 films currently being used as annealing caps are reasonably effective in this application.

3.3.3 Device Processing, Fabrication, and Evaluation

No new devices have been fabricated; however, a number of layers with characteristics suitable for FET fabrication have been identified, and fabrication of devices in these layers has been started. These include both tellurium-implanted layers, a portion of which will be profiled by the stripping technique, and some sulfur-implanted layers which were prepared under company-supported research. Fabrication of FET's in these layers will be carried to completion and measurements of the performance of the devices carried out, with an attempt to correlate the device performance with the measured characteristics of the implanted layers.

4.0 FUTURE PLANS

4.1 Epitaxial Growth and Processing

4.1.1 Ultra-Thin Layer Epitaxy

Further reduction of initial growth rate as a function of growth temperature and reactor geometry will be optimized. It is hoped that high-quality epitaxial films with a predefined carrier concentration can be reproducibly grown at a rate less than 5000Å per minute.

4.1.2 High-Resistivity Epitaxy

Optimum growth conditions to minimize residual impurities will be sought. The resulting high-resistivity layers will be investigated using a scanning electron microscope to determine the minority carrier diffusion

length. Thermally-stimulated current and capacitance measurements will be employed to study the density of deep levels in the epitaxial layers.

4.1.3 Multi-Layer LPE

Control of layer thickness and carrier concentration will be the prime objective. C-V measurement techniques will be used for profile determination. The extent of cross contamination between layers deposited consecutively is to be determined.

4.1.4 Processing and Device Measurements

Future measurements will be made mainly on devices fabricated on materials prepared during the course of the contract. Emphasis will be placed on material characterization. More experiments will be carried out to evaluate the interface states by measuring the saturation current of reverse-biased diode structure near punch-through.

4.2 Semi-Insulating Material

Our effort will concentrate on evaluating semi-insulating substrates grown under various conditions using the n-i-n and n-i-m structures. The use of Auger spectra to determine the potential distribution of a reverse-biased n-i junction will also be pursued. Our immediate goal is to reach a conclusion as to whether the density of electrically-active deep traps in semi-insulating substrates is high enough to cause degradation in devices fabricated on top. The next step is to determine the mechanism of impurity incorporation during the growth of GaAs crystals--especially the role oxygen plays in insulating GaAs. Semi-

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insulating crystals will be grown with or without Cr doping in both the horizontal gradient freeze furnace and a new vertical furnace.

4.3 Ion Implantation

Further work is planned to investigate the repeatability of results for a given implant dose, accelerator voltage and anneal temperature, and to investigate the effects of using semi-insulating substrates or epitaxially-grown layers from various sources. The possible contribution of planar channeling to the penetration of the implanted tellurium will also be studied.

Additional experiments will also be carried out to determine if better annealing caps than the materials currently in use can be obtained.

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