STUDY OF FIELD ASSISTED PHOTOCATHODES WITH DOUBLE HETEROJUNCTION STRUCTURE

A. G. Milnes, et al

Carnegie-Mellon University

Prepared for:

Advanced Research Projects Agency

June 1974

STUDY OF FIELD ASSISTED PHOTOCATHODES WITH DOUBLE HETEROJUNCTION STRUCTURE

Final Technical Report

A. G. Milnes D. L. Feucht P. K. Govil

412-621-2600

June 1974

CARNEGIE-MELLON UNIVERSITY
Electrical Engineering Department
Pittsburgh, Pennsylvania 15213

Sponsored by

ADVANCED RESEARCH PROJECTS AGENCY
ARPA ORDER NO. 2182
PROGRAM CODE NO. 2D10

CONTRACT NO. DAAK02-72-C-0206

Effective Date of Contract: 1 February 1972

Contract Expiration Date: 30 June 1974

Amount of Contract: $90,244.00

This research was supported by the Advanced Research Project of the Department of Defense and was monitored by the Night Vision Laboratory under Contract DAAK02-72-C-0206.

ABSTRACT

The concept of a double heterojunction structure, pGe-νZnSe-p^+GaAs (Cs) as a field assisted photocathode that would emit electrons from the GaAs following the photo-generation of electrons in the Ge has been studied.

Severe technological problems were encountered in fabricating the structure and efficient electron transport from the Ge into the ZnSe was not achieved. Strong trapping actions were observed at the Ge-ZnSe interface prepared by an HCl close-spaced transport process.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

1. Introduction

p^+GaAs with a Cs or Cs-O surface treatment is a high-yield photocathode that emits electrons for photons of energy equal to or greater than 1.4 eV. Since a condition of negative electron affinity exists with respect to electrons thermalized in the conduction band of the GaAs the quantum efficiency is high. Extension of this approach to ternary three-five compounds and to silicon has resulted in photocathodes with acceptable sensitivity thresholds down to about 1.1 eV.

For photothresholds of lower energy it is necessary that the photons create electrons in the conduction band of a semiconductor with a band gap of less than 1.1 eV, such as Ge (0.7 eV). A suitable surface treatment must be found which enables these electrons to be emitted directly into vacuum from the low-band-gap semiconductor or these electrons must be transferred through a heterojunction to the conduction band of a low-electron-affinity semiconductor such as GaAs (Cs-O) for emission. Examination of the heterojunction concept suggests that a three-layer structure, Ge/ZnSe/GaAs, will be necessary to prevent undesirable current flow under the required voltage-bias and doping conditions.

The basic idea is to retain the proven GaAs (Cs) or GaAs (Cs-O) negative electron affinity structure[1] and to achieve sensitivity at photon energies below 1.4 eV by the addition of a pGe-ZnSe junction. The energy band diagram expected (without external bias applied) would then be as in Fig. 1(a). Under normal operation the external bias would be as in Fig. 1(b) and the resulting band diagram as in Fig. 1(c)*. Incident

---

* The band diagram is discussed in more detail later, see Fig. 9.

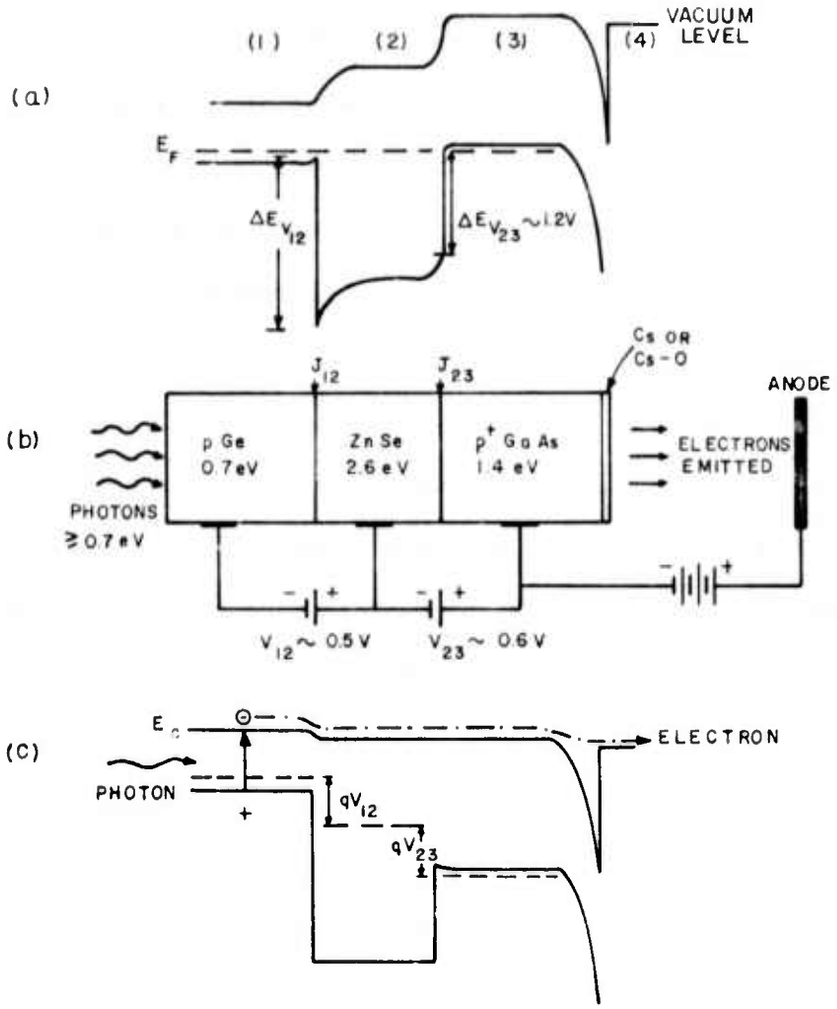


Fig. 1 pGe-νZnSe-p^+GaAs(Cs) electron-emitting photo-cathode: sensitivity to 0.7 eV (1.75μm) expected. (a) Energy diagram without bias voltages. (b) Bias circuit for operation of the structure. (c) Energy diagram with bias voltages applied.

photons, as shown, would create electron-hole pairs in the Ge.

A photoexcited electron has no energy barriers to its movement from the Ge through the ZnSe (∿2μm thick) conduction bands. However the barrier to hole flow from the Ge to ZnSe is desirably large. The valence band barrier between the ZnSe and the GaAs is also substantial even for the required bias condition on J_{23} and therefore there should be no hole injection from the p^+GaAs into the ZnSe that might represent undesirable current flow. (Undesirable, because it might reduce the electron lifetime in the ZnSe and because it would produce voltage drops and heating).

The Ge/ZnSe/GaAs combination is very attractive for several reasons. The lattice constants of the three materials are very similar (5.658, 5.667, 5.654 Å) and the thermal expansion coefficients are close enough that, with care, single-crystal uncracked layers of ZnSe may be grown on Ge or on GaAs. The electron affinity values are also very closely the same (viz. 4.13, 4.09, 4.07 eV) so there are no appreciable conduction band barriers. Heterojunction transistors of nZnSe/pGe/nGe, nZnSe/pGaAs/nGaAs, and n GaAs/pGe/nGe have been grown in our laboratory and examined. There is some evidence of interface recombination at the heterojunction interfaces, but at moderate current densities (a few A/cm^2) transistor alphas of greater than 0.9 are commonly obtained. Hence the pGe-nZnSe and the nZnSe-p^+GaAs interfaces can be characterized as moderately well behaved if skill is used in their fabrication. Therefore the structure proposed in Fig. 1 seems within the state of the present art without an excessive number of imponderables.

Quite a number of other heterojunction possibilities have been considered by us. In order to show reasonable promise we believe that they need to satisfy five conditions: (1) They must have an excellent lat-

tice match so that interface recombination will be low, (2) the energy band gap of the middle semiconductor (e.g., ZnSe in Fig. 1) must be sufficiently large so there is a barrier to hole flow from the electron-emitting semiconductor (e.g., GaAs), (3) the electron affinities should be nearly equal or increase as one proceeds from the material in which the carriers are optically generated (Ge) to the electron-emitting semiconductor (GaAs), (4) the interface states should not cause depletion regions that add to the conduction band barriers in ways that adversely affect electron flow, and (5) the electron diffusion lengths must be suitably long.

With the Ge/ZnSe/GaAs (Cs) structure proposed it seems reasonable to expect electron emission for photons down to the Ge absorption edge $\sim$ 0.7 eV. The device therefore should cover the important laser lines at 1.06μm (Nd), 1.15μm (HeNe), and 1.69μm (Ar). It should also operate comfortably in the atmospheric windows up to the 1.4-1.8μm window.

The work on the research grant is concerned with the general concept of double heterojunction field assisted photocathodes.

In order to accomplish this study the following three areas of investigation have been defined:

1. Design analysis to determine the required structure and the quantum yield for the double heterojunction field assisted photocathode.
2. Development of the materials and device fabrication techniques for the Ge/ZnSe/GaAs structure.
3. Measurement of the electron transport properties in Ge/ZeSe/GaAs structures.

2. Analysis and Design Calculations

The proposed heterojunction photocathode structure ought to be oper-

able in two different modes viz. (a) the transmission mode in which the photons are incident on the Ge side of the structure and (b) the reflection mode in which the photons are incident on the GaAs side of the structure. Figures 2 and 3 show the schematic representation of such a structure in the reflection and transmission modes. In both the modes, the electron emitting surface is the GaAs side. The analysis of these structures for computing the expected photoemissive yield (electrons emitted/incident photon) involve different considerations.

Operation under transmission mode (Fig. 3) offers convenience and simplicity of utilizing such photocathodes since the light input and the electron output sides are separated. Moreover, if the proposed three-layer structure is illuminated from the GaAs side, there will be at least three reflecting surfaces (and interfaces) resulting in multiple infrared reflections. Probably therefore operation in transmission mode, where the Ge surface can be suitably coated with antireflection film, is desirable from the viewpoint of minimizing reflection losses.

The photoemissive yield (η) of such structures is expected to be given by

$$\eta = (1-R)\ F_d\ T_{ZnSe}\ T_{GaAs}\ P \qquad (1)$$

where R represents the effective reflection loss, F_d is the fraction of the photogenerated electrons (in Ge) able to diffuse up to the Ge/ZnSe interface where the electric-field can sweep them into the ZnSe layer, T_{ZnSe} and T_{GaAs} represent the transport efficiency of the ZnSe and GaAs layers and P is the escape probability of electrons after reaching the GaAs (C_s-O) surface for emission into vacuum. In the following sections we relate these factors to the material and device parameters.

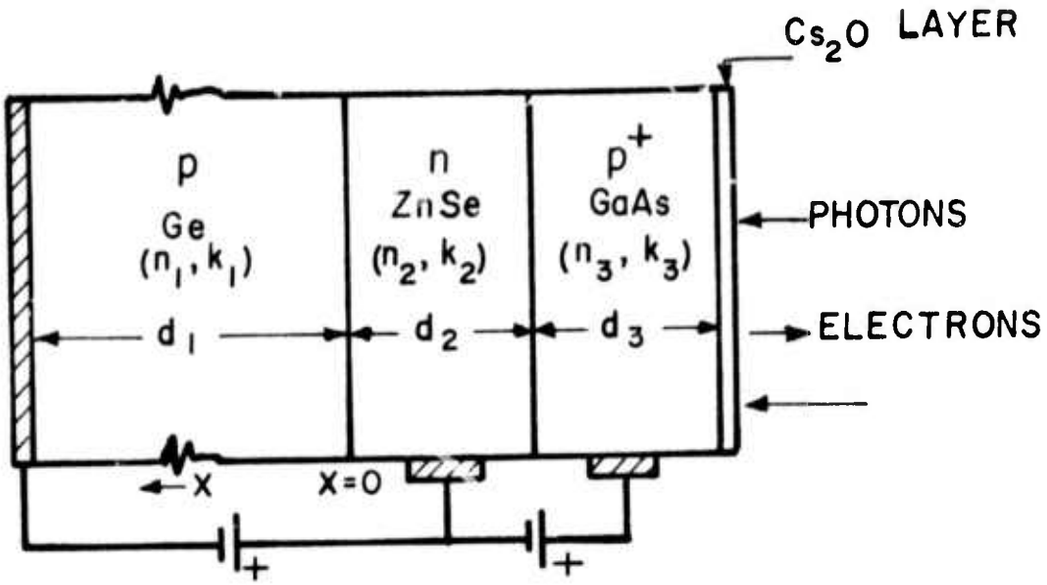


Fig. 2. Schematic representation of the proposed photocathode in reflection mode.

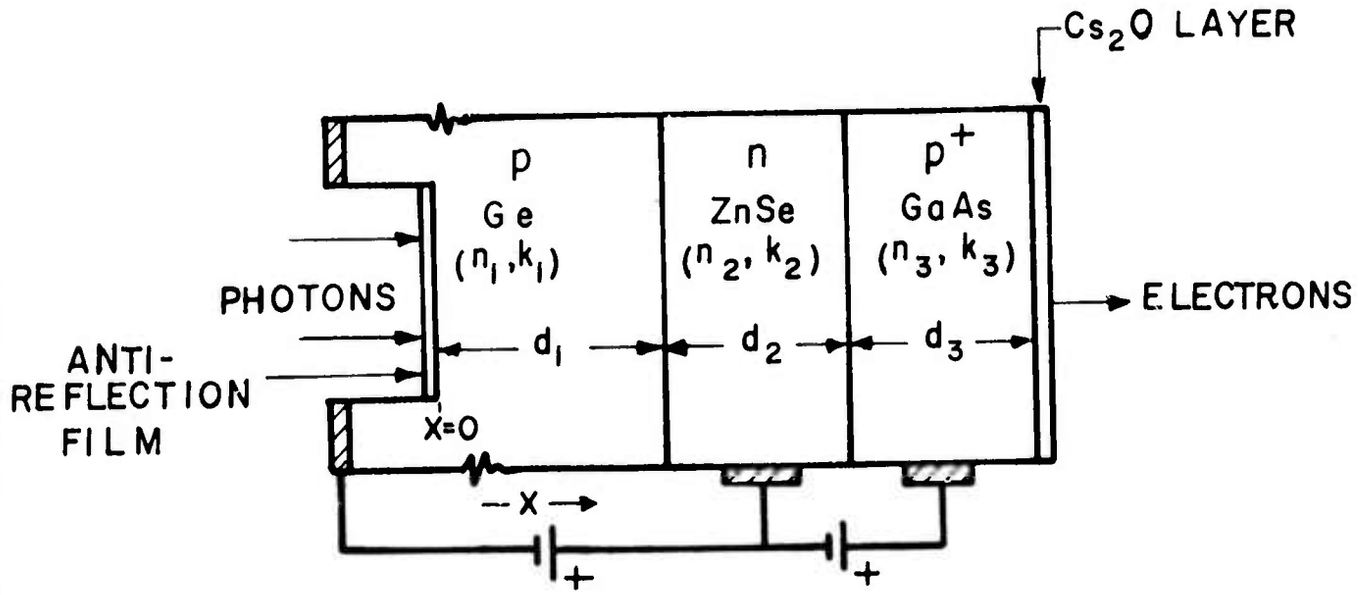


Fig. 3. Schematic representation of the proposed photocathode in transmission mode.

2.1 Estimation of Reflection Loss, R

2.1.1 Reflection mode:

In this case we do not have any control over the surface to minimize reflection. It will be assumed that the Cs_2O monolayer on GaAs surface does not affect the reflectivity of this surface and that GaAs and ZnSe layers are thick films ($d>5\lambda_o/2n$).

In equation (1) the (1-R) term represents the transmission "T" into the Ge substrate. In this case of front illumination we get:

$$T = \frac{(1-R_o)\ (1-R_1)\ (1-R_2)\ e^{-(\alpha_2 d_2 + \alpha_3 d_3)}}{1-R_o R_1 e^{-2\alpha_3 d_3} - R_1 R_2 e^{-2\alpha_2 d_2} - e^{-2(\alpha_2 d_2 + \alpha_3 d_3)} (R_o R_2 - 2R_o R_1 R_2)} \qquad (2)$$

where in (2):

$$R_o = \frac{(n_3-1)^2 + k_3^2}{(n_3+1)^2 + k_3^2}$$

$$R_1 = \frac{(n_2-n_3)^2 + (k_2-k_3)^2}{(n_2+n_3)^2 + (k_2+k_3)^2} \qquad (3)$$

$$R_2 = \frac{(n_1-n_2)^2 + k_1-k_2)^2}{(n_1+n_2)^2 + (k_1+k_2)^2}$$

The absorption coefficient α is related to the imaginary part of the complex refractive index (n-ik) by the expression

$$\alpha = \frac{4\pi k}{\lambda_o}$$

where λ_o is the free space wavelength of light.

Using the n and k values for the three semiconductor materials at say 1.06μm wavelength, the value of T comes out to be 0.6532, i.e. only about

65 percent of the incident photons are able to enter the Ge region. The reflection from the GaAs surface is 30.3 percent at such a wavelength.

2.1.2 Transmission Mode:

In this case, we can have an anti-reflection film on the Ge to minimize reflection losses. If n_o is the refractive index of the film, then the reflection coefficient is given by

$$R = \frac{R_0 + R_1 + 2\sqrt{R_0 R_1} \cos\left(\frac{4\pi n_o d_o}{\lambda_o} + \phi\right)}{1 + R_0 R_1 + 2\sqrt{R_0 R_1} \cos\left(\frac{4\pi n_o d_o}{\lambda_o} + \phi\right)} \qquad (4)$$

where in (4),

$$R_0 = \left(\frac{n_o - 1}{n_o + 1}\right)^2 \quad , \quad R_1 = \frac{(n_1 - n_o)^2 + k_1^2}{(n_1 + n_o)^2 + k^2} \quad \text{and} \quad \phi = \tan^{-1} \frac{2 n_o k_1}{n_1^2 + k_1^2 - n_0^2} \qquad (5)$$

Reflectivity minima is reached when $\left(\frac{4\pi n_o d_o}{\lambda_o} + \phi\right)$ equals π, 3π . . . giving the value of minimum reflectivity as

$$R_{min} = \frac{R_0 + R_1 - 2\sqrt{R_0 R_1}}{1 + R_0 R_1 - 2\sqrt{R_0 R_1}} = \left(\frac{\sqrt{R_1} - \sqrt{R_0}}{1 - \sqrt{R_1 R_0}}\right)^2 \qquad (6)$$

The value of "d_o" for this condition is given by

$$d_o = \frac{\lambda_o}{4\pi n_o} \times \left(\pi - \tan^{-1} \frac{2 n_o k_1}{n_1^2 + k_1^2 - n_o^2}\right) \qquad (7)$$

The optimum thickness of SiO ($n_o \simeq 1.9$) anti-reflection coating comes out to be 1380 Å at which the reflection loss for the wavelength is only 0.68 percent. For SiO_2 ($n_o = 1.45$) coating these values are 1815 Å and 11.49 percent loss.

2.2 Estimation of Collection Efficiency, F_d

2.2.1 Reflection Mode:

The transport of photo-excited electrons is described by the equation

$$\frac{d^2n}{dx^2} - \frac{n}{L_{n1}^2} = \frac{G(x)}{D_{n1}} \tag{8}$$

where L_{n1} and D_{n1} are the diffusion length and diffusion constant for electrons in the p-Ge (region 1). The photocarrier generation function G(x) is given by

$$G(x) = N.T.\ \alpha_1 e^{-\alpha_1 x} \tag{9}$$

where N is the incident photon flux, T is given by eq. (2) and α_1 is the absorption coefficient of p-Ge at the operating wavelength. The boundary conditions are n=0 at x=0 and $x=d_1$, giving the value of F_d in reflection mode (RM) as:

$$F_d\ (RM) = \frac{\alpha_1}{\alpha_1 + 1/L_{n1}} - \frac{2\alpha(e^{-d_1/L_{n1}} - e^{-\alpha_1 d_1})}{L_{n1}(\alpha_1^2 - 1/L_{n1}^2)(e^{d_1/L_{n1}} - e^{-d_1/L_{n1}})} \tag{10}$$

The second term in this expression becomes zero for large d_1/L_{n1} ratios. Fig. 4 shows this collection efficiency as a function of αL_n for different values of d/L_n. For operation at λ μ where the absorption coefficient in Ge, α_1, is more than 10^4 cm^{-1}, the collection efficiency in reflection mode will be close to unity since the photoelectrons are generated in the Ge very close to the ZnSe/Ge interface. However Fig. 4 will be useful for studying the operation of such photocathodes at longer wavelengths.

2.2.2 Transmission Mode:

In this case, the boundary conditions are n=0 at $x=d_1$ and

$$\frac{dn}{dx} = \frac{nS}{D_{n1}} \text{ at } x = 0$$

where S is the surface recombination velocity. This leads to

$$F_d\ (TM) = \left\{ \frac{\alpha_1^2 L_{n1}^2}{\alpha_1^2 L_{n1}^2 - 1} \left[\frac{D_{n1} + S/\alpha_1}{D_{n1} + S\ L_{n1}} e^{-d_1/L_{n1}} - e^{-\alpha_1 d_1} \right] + \frac{\alpha_1 L_{n1} \tanh\left(\frac{d_1}{L_{n1}} + \phi\right)}{\alpha_1^2 L_{n1}^2 - 1} \left[\frac{\alpha_1 L_{n1}(D_{n1} + \frac{S}{\alpha_1})}{D_{n1} + S\ L_{n1}} e^{-d_1/L_{n1}} - e^{-\alpha d_1} \right] \right\} \tag{11}$$

where ϕ is given by

$$\tanh \phi = \frac{SL_{n1}}{D_{n1}} \qquad (12)$$

This expression can be simplified for the extreme case of S equal to zero.

$$F_d(\text{TM for } S=0) = \frac{\alpha_1 L_{n1}}{\alpha_1^2 L_{n1}^2 - 1} \left[\alpha_1 L_{n1} \left(1+\tanh \frac{d_1}{L_{n1}}\right) e^{-d_1/L_{n1}} - e^{-\alpha_1 d_1} \left(\alpha_1 L_{n1} + \tanh \frac{d_1}{L_{n1}}\right) \right] \qquad (13)$$

Fig. 5 shows this collection efficiency as a function of αL_n for different values of d/L_n for the case of no surface recombination losses. The dashed curve for d/L_n ratio of 0.25 is for $S/\alpha D_n 1 = 0.02$, which at 1-1.4μm represents a surface recombination velocity of about 10^4cm sec^{-1}. Fig. 6 shows the effect of surface recombination losses for the case $d/L_n = 1$.

For operation at 1-1.4μm, where αL_n will be typically more than 150 for good quality Ge ($\mu_n \simeq 2400$ cm^2 v^{-1} sec^{-1}, $\tau_n \simeq 5 \times 10^{-6}$sec, $\alpha = 10^4 cm^{-1}$), we see that the effect of surface recombination velocity is very important. From the dashed curve in Fig. 5 we note that the expected collection efficiency of a thinned-down (e.g. a 15 mils Ge substrate thinned to about 2 mils in the active region) device will be less than 60 percent for the normal surface recombination velocity of about 10^4cm sec^{-1}. Figures 7 and 8 show this effect in greater detail. These figures show

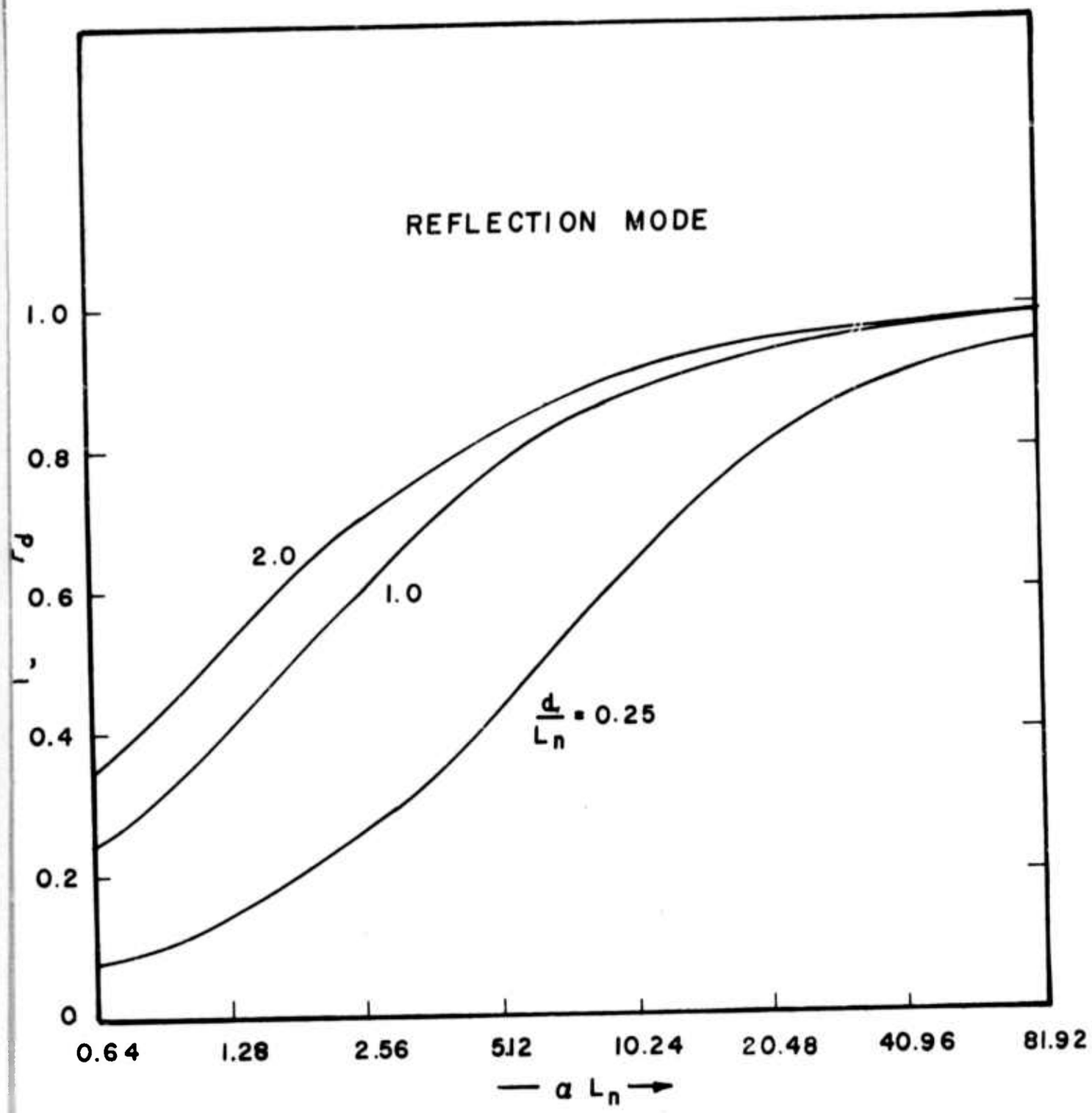


Fig. 4. F_d in reflection mode as a function of α for various thicknesses d.

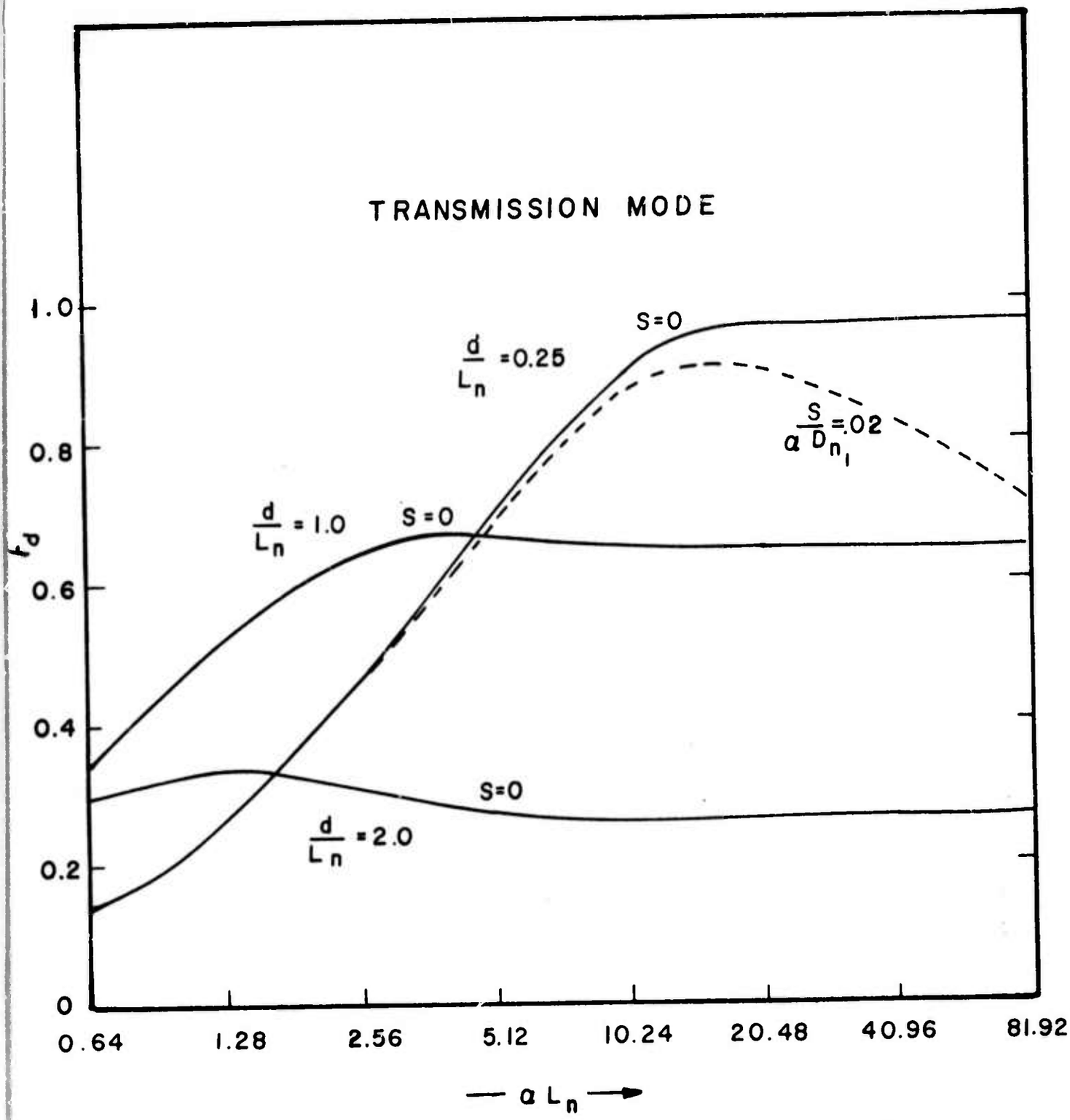


Fig. 5. F_d in transmission mode as a function of α for different thicknesses d, for the case of no surface recombination losses. The dashed curve shows the effect of surface recombination losses.

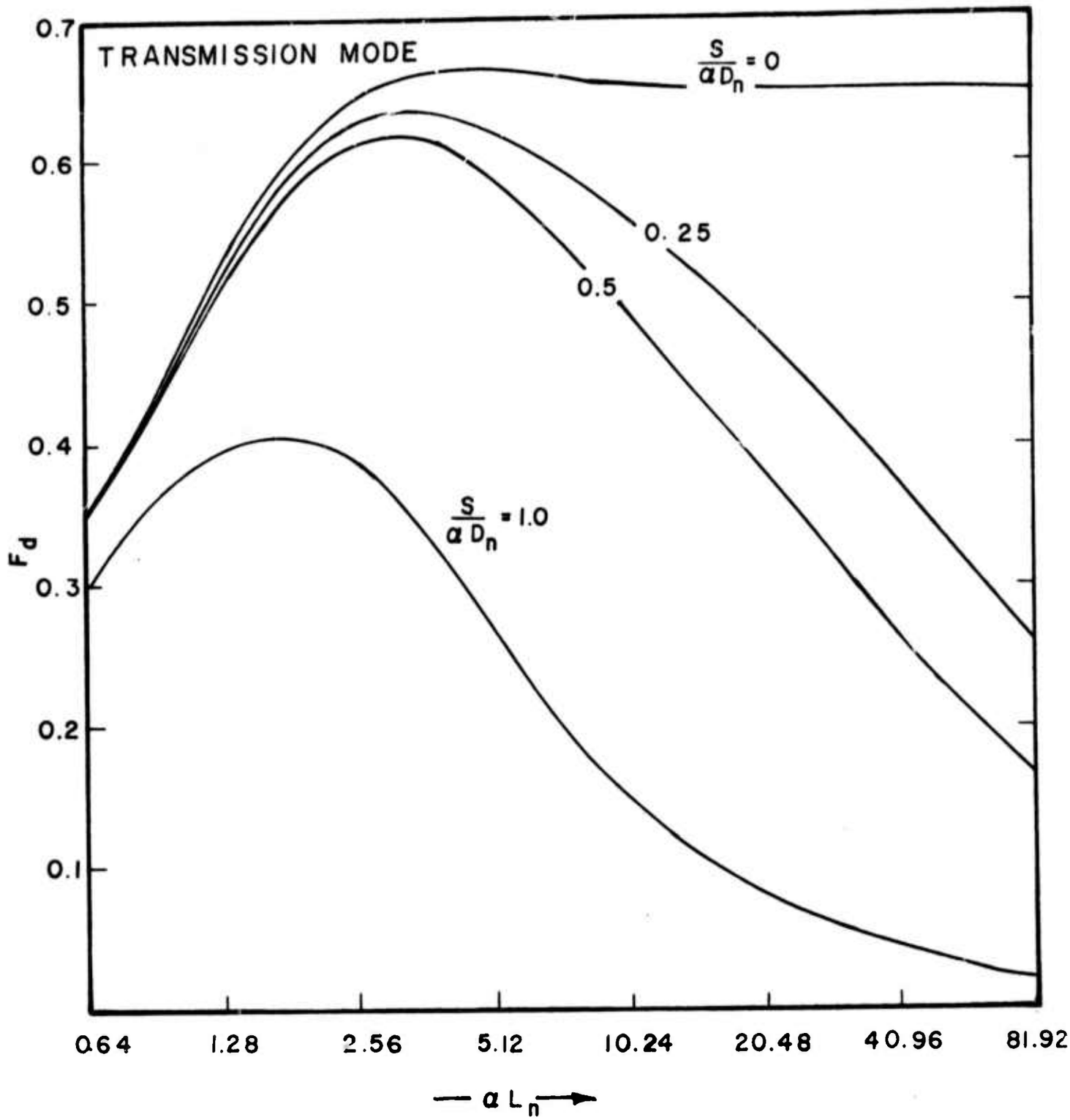


Fig. 6. F_d in transmission mode. Effect of change in surface recombination velocity.

the collection efficiency at different surface recombination velocities as a function of electron diffusion length for 1 and 2 mils active region thicknesses. For obtaining performance comparable to reflection mode, we need to have the collection efficiency F_d greater than the transmission T into Ge in reflection mode. From section 2.1.1 we note that if F_d in transmission mode can be made greater than 0.65 we can obtain higher overall efficiency than in the reflection mode. For 1.06μm operation, this means that for a surface recombination velocity S of 10^4cm sec^{-1}, the thickness of the active region has to be reduced to 1 mil or less. However, if by some surface treatment procedure we can bring S down to near 10^3 cm sec^{-1} in value, a more practical thickness of 2 mils can be tolerated for the active region of the Ge substrate.

2.3 Estimation of Transport Efficiencies, T_{ZnSe} and T_{GaAs}:

Under operating conditions, viz. Ge-ZnSe junction slightly reverse biased and ZnSe - GaAs junction slightly forward biased to get the flat conduction bands condition in the band diagram, it can be assumed that the electrons travel solely by diffusion processes in the ZnSe* and GaAs layers to reach the GaAs surface. This leads to the result:

$$T_{ZnSe} = \text{sech} \frac{d_2}{L_{n2}} \tag{14}$$

and

$$T_{GaAs} = \text{sech} \frac{d_3}{L_{n3}} \tag{15}$$

The following table shows the values of $\text{sech}(\frac{d}{L})$ and $\text{sech}^2(\frac{d}{L})$ as a function of d/L:

* In section 2.4 it is pointed out that the ZnSe may be fully depleted so the electron transport is field aided and T_{ZnSe} may approach unity.

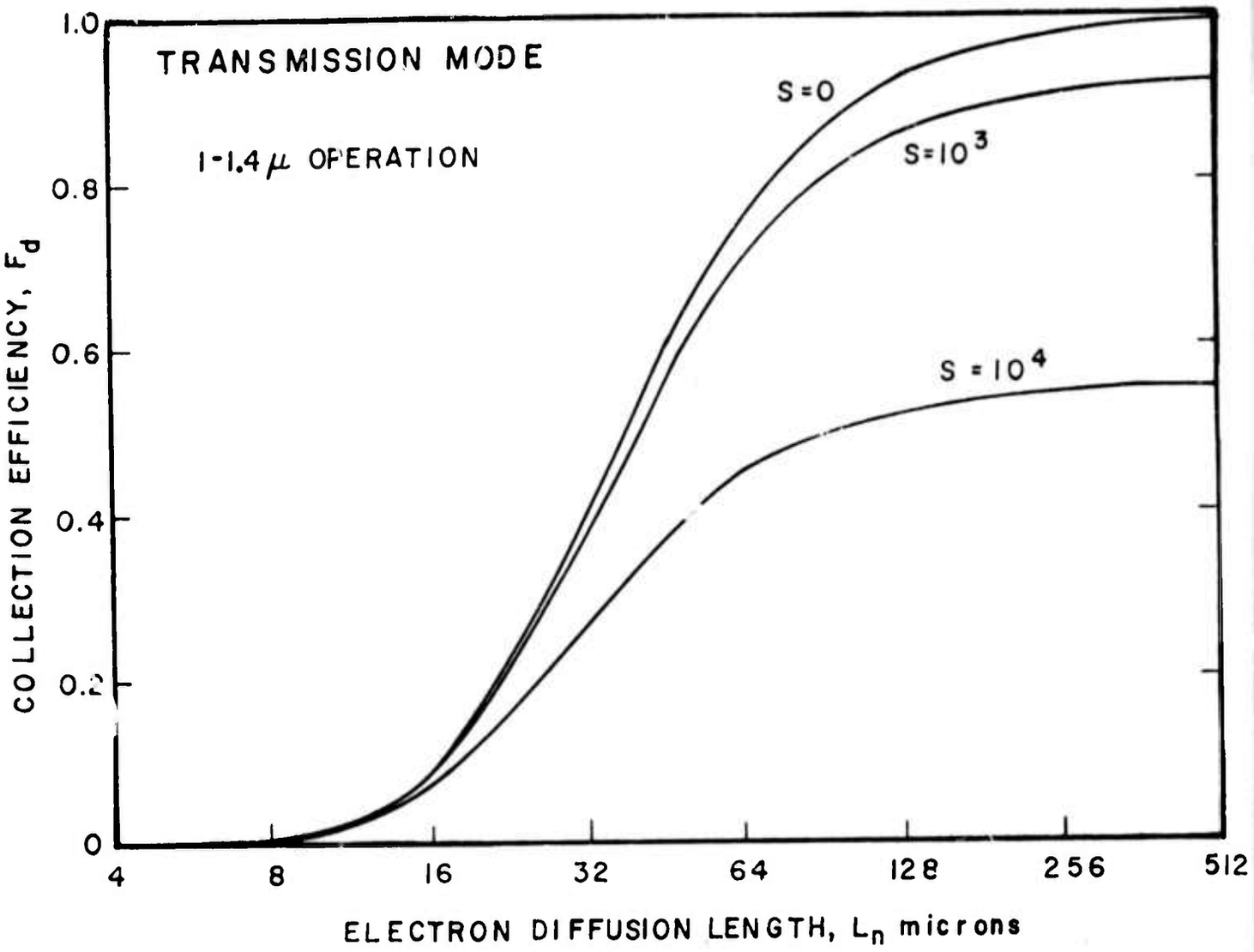


Fig. 7. Collection efficiency in transmission mode of the device with active Ge region thinned down to 7 mils for different surface recombination velocities. ($\alpha = 10^4$, $D_n = 60$).

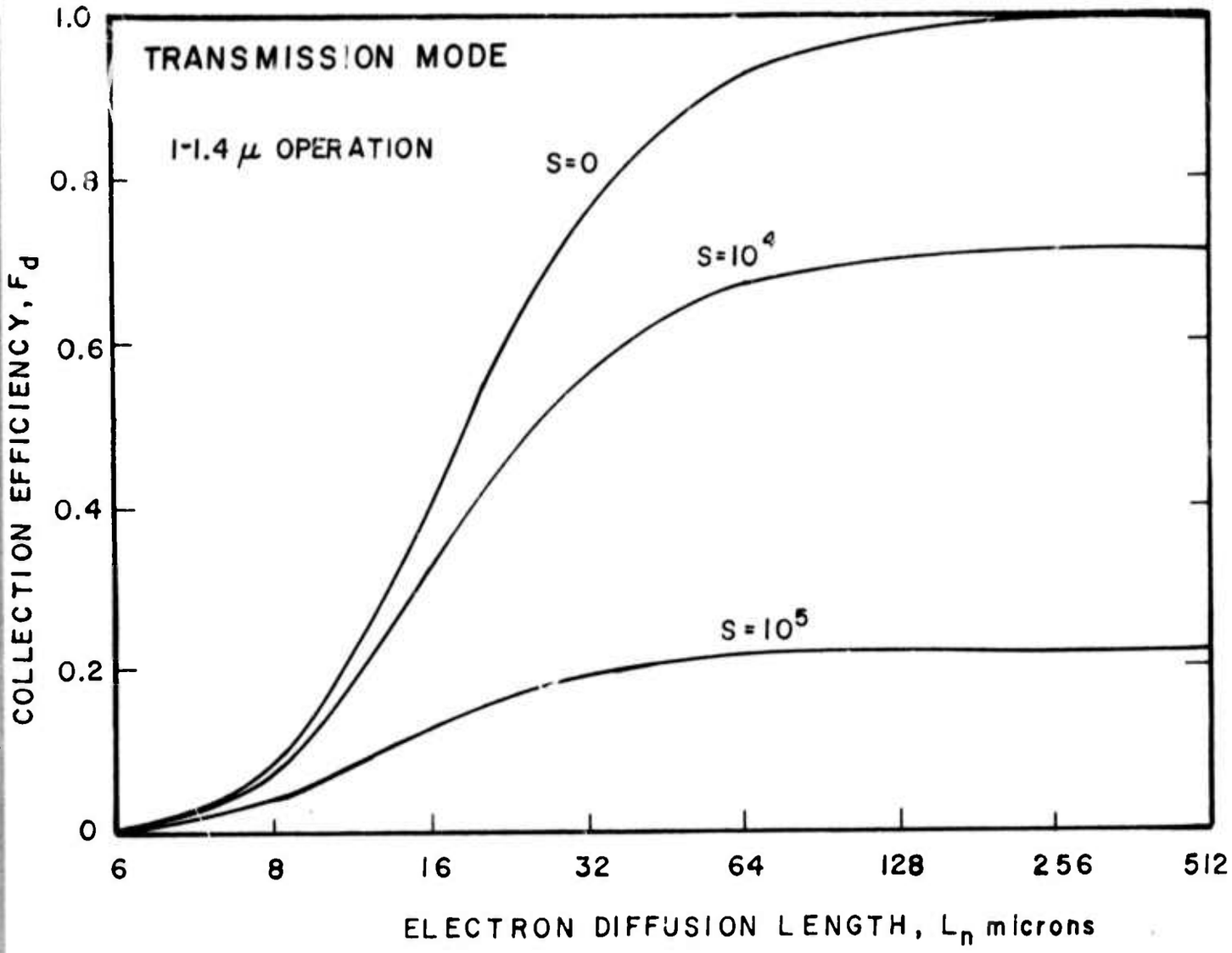


Fig. 8. Collection efficiency in transmission mode of the device with active Ge region thinned down to 1 mil for different surface recombination velocities. ($\alpha = 10^4$, $D_n = 60$).

Table 1 Transport factor as a function of thickness

$\frac{d}{L}$	sech $(\frac{d}{L})$	sech^2 $(\frac{d}{L})$
0.5	0.88	0.77
1.0	0.65	0.42
2.0	0.26	0.07
3.0	0.1	0.01
4.0	0.04	0.00

From Table 1 it can be seen that in order to have reasonable overall efficiency, the thicknesses of ZnSe and GaAs layers should be of the order of the electron diffusion length or less.

2.4 Estimation of Escape Probability

P is the escape probability and is principally determined by the low work function coating on the GaAs surface. It is also dependent on the crystal orientation of the surface as shown by James et al.[2] Analytical expression for P in terms of such material parameters is difficult to obtain. However, James and Moll[3] showed that the P value can be made to reach as high as 0.36 for electron emission from the Γ minima.

James et al[2] reported that the band bending is minimum for the (111B) face, followed by (100), (110) and (111A) faces in the order of increasing band-bending and thus decreasing escape probability. They also reported that during the usual heat cleaning cycle before cesiation, the GaAs surface develops (110) facets on the entire surface and therefore the escape probability figure for (110) face applies irrespective of actual orientation. This has some relevance to the seed planes that should be used in our growth system. Based on our past experience, in this lab, we decided to make growths on (100) Ge.

Further analysis of the proposed structure brings out the following

salient points.

(i) Since the ZnSe layer is the high resistivity layer in the proposed structure, the depletion regions of both the junctions on the two sides of ZnSe region will mainly be in the ZnSe layer. If we assume that the Fermi level in the ZnSe region is about 0.6 eV below its conduction band level (corresponding to ZnSe resistivity of about 4.3×10^7 Ω-cm) so that there is no Fermi level difference or built-in voltage at the Ge/ZnSe junction, we have about 0.83 eV as the value of the built-in voltage for the ZnSe/GaAs junction. A calculation of the depletion layer width under such conditions results in a value of about 0.23 cm. Clearly the ZnSe layer, which is to be only a few microns in thickness, will become completely depleted and the structure will behave as if we have an insulating layer sandwiched between two p-type semiconductors. An important feature of the ZnSe insulating layer is that its electron affinity value is quite close to that of Ge and also GaAs. This property assures the continuity of the conduction band edge in the band diagram as shown in Fig. 9(a) which is an improved version of Fig. 1 presented in the Introduction.

(ii) Because of the depletion effect mentioned above, there is no need to make any electrical contact to the ZnSe layer (which would have been a difficult task because of its high resistivity). Fig. 9b shows the bias arrangement needed. This proposed structure is now a much more attractive device because only two contacts are required.

(iii) After an external bias of about 0.8 V is applied, the band diagram looks like Fig. 9c, with no barrier to electron flow. In such a structure the dark emission current may be assumed to be governed by

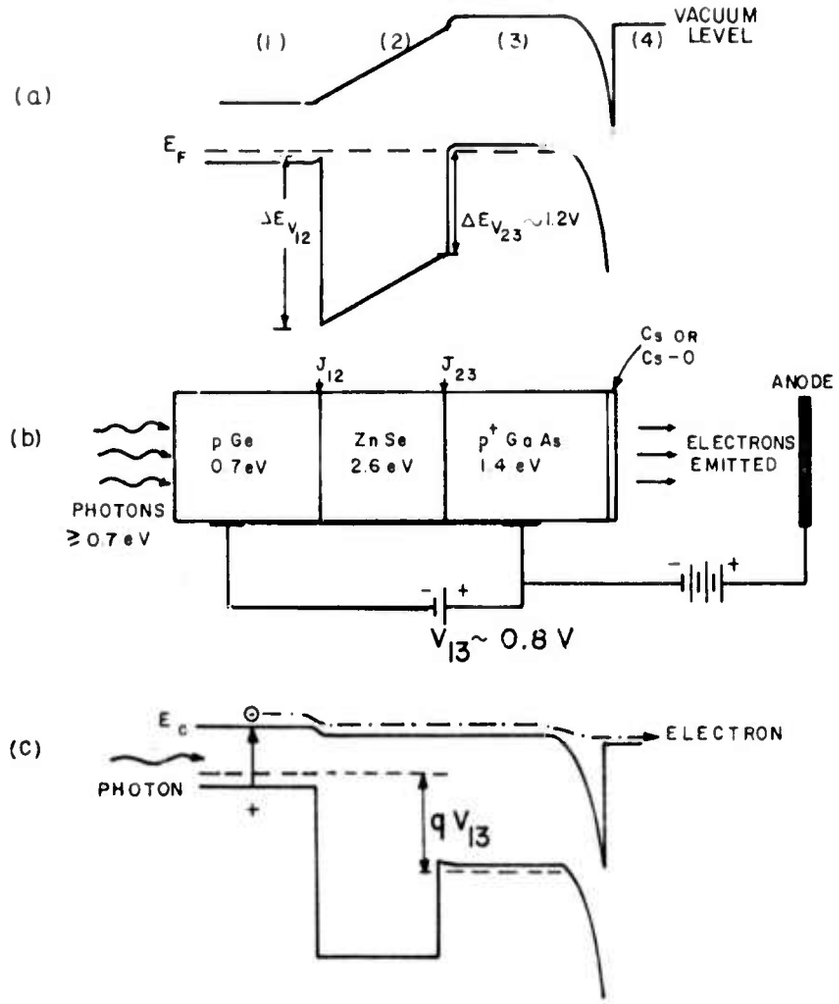


Fig. 9 pGe-νZnSe-p^+GaAs(Cs) electron-emitting photocathode: sensitivity to 0.7 eV (1.75μm) expected. (a) Energy diagram without bias voltages. (b) Bias circuit for operation of the structure. (c) Energy diagram with bias voltages applied.

the thermal generation of electrons in the p-Ge region.

The generation rate of electrons in p-Ge is $\frac{n_o}{\tau_n}$, where n_o is the equilibrium electron concentration and τ_n is the electrical lifetime. If we consider the p type Ge to be doped at $5 \times 10^{16} cm^{-3}$, then at 300^oK we have $n_o = 1.2 \times 10^{10}$ electrons cm^{-3}. To assess the generation rate we now have to assume a minority carrier lifetime: let us take τ_n as 10^{-5} sec, although this is a conservative value that might be larger in good quality Ge of this doping level. The generation rate (n_o/τ_n) is then 1.2×10^{15} electrons cm^{-3} sec^{-1}. The electron diffusion length corresponding to 10^{-5} sec is 300μm, however in the device proportions considered in the previous sections (2.2 & 2.3) the germanium layer thickness was taken as 1 mil (25μm). Hence we may assume that all the electrons generated in this 1 mil region enter the ZnSe as dark current. The current density is therefore $1.6 \times 10^{-19} \times 1.2 \times 10^{15} \times 25 \times 10^{-4}$ which is about 0.5μA cm^{-2}.

If we define the sensitivity of the detector as the light level in terms of photons cm^{-2} sec^{-1} which will generate the photoelectrons equal in number to the thermally generated electrons, for the wavelength range 1 - 1.55μm (for which the absorption coefficient range is 10^4 - 10^3 cm^{-1}), we obtain about 3×10^{12} photons cm^{-2} sec^{-1}. This corresponds to a power level of about 0.5μW cm^{-2}.

Since the expected maximum yield for the structure is about 9% the dark current will be 0.5×10^{-7} A/cm^2. This is five orders of magnitude higher than the dark current usually quoted for S-1 photocathodes but there are a few important points to keep in mind before comparing these figures. The first is that proposed structure is expected to have a quantum yield of about 9% up to a wavelength of the order of 1.5μm which is a wavelength region in

which most other photocathodes are non-operative. The second point is that if one operates the proposed photocathode at a lower temperature, say at $-50^{o}C$, the dark current should drop three orders of magnitude.

By using either dry-ice or a two-stage thermoelectric cooler, we can hope to get $200^{o}K$ as the operating temperature. At this temperature the n_i^2 value for Ge is 7 orders of magnitude lower than at room temperature. Therefore, the above mentioned sensitivity limit will be 3×10^5 photons cm^{-2} sec^{-1} at $200^{o}K$. However, it is expected that at $200^{o}K$, the sensitivity limit will depend on the background noise due to the surroundings.

In order to know the specification requirements for the possible use of the proposed photocathode structure as a night imaging device, we must consider the level of infrared illumination typically available from the night sky.

The proposed photocathode is expected to respond in the wavelength range 0.9μm to 1.6μm for operation in both the reflection and transmission mode. The 1.6μm limit is because of the intrinsic bandgap of the germanium in which the electron-hole pairs have to be created. The 0.9μm limit comes from (i) the bandgap of GaAs for the reflection mode or (ii) surface recombination losses because the carriers will be generated too close to the Ge surface for wavelengths less than 0.9μm in the transmission mode. From the published data on sky radiation we find that the night illumination due to airglow only (no moonlight) provides a cumulative zenith brightness of about 3×10^{10} photons cm^{-2} sec^{-1} $ster.^{-1}$ in the wavelength interval 0.9μm to 1.6μm. From the geometrical aspects of airglow illumination of targets, we find that an image-tube of 1 cm^2 photoemitter area and a field of view of about $\frac{\pi}{10}$ steradians pointed towards an expected target on the horizon, one would expect to receive $3 \times 10^{10} \times \frac{\pi}{10} \times \frac{1}{10}$ ($\simeq 10^9$) photons cm^{-2} sec^{-1} at the

site of a typical target. Therefore for the tube to be useful, the sensitivity needs to be at least 10^9 photons cm^{-2} sec^{-1} based on the typical minimum illumination available. The sensitivity limit estimated earlier for 200^oK operation is 3×10^5 photons cm^{-2} sec^{-1}.

From the above considerations it seems clear, at present, that the proposed device will require cooling. With a two stage thermoelectric cooler, resulting in 200^oK operating temperature, the device will be sensitive enough to the extent that it will be operating in the background noise limited situation. Under 200^oK conditions, the dark emission is expected to be about 5×10^{-15} amp. cm^{-2}.

3. Fabrication

Based on the design considerations mentioned in the previous section, the following features are suggested for the proposed Ge-ZnSe-GaAs structure (Fig. 10):

(a) Ge is to be the substrate material about 10-15 mils thick with the active (central) area of the device thinned down to less that 1 mil. thickness for transmission mode operation. This thickness is governed by two requirements--viz. (i) mechanical stability (ii) final image resolution. The thick outer ring will provide the electrical contact to the p-Ge.

(b) The ZnSe layer is to be about 1-3μm thick and high-resistivity n-type. These parameters are to be optimized later by electrical testing of the finished device. The epitaxial ZnSe layer should completely cover the Ge substrate. The electrical contact to this layer will be by a ring deposited along the periphery of the layer.

(c) The central active area of the ZnSe/Ge structure is to be covered

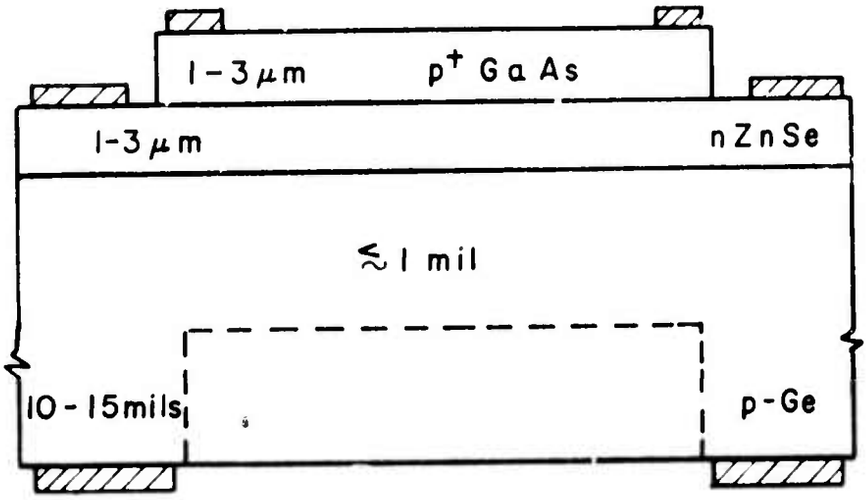


Fig. 10 Suggested cross-section of the Ge-ZnSe-GaAs device. (For the fully depleted ZnSe mode of operation as discussed in section 2.4 the contacts to the ZnSe are not needed. They are useful in the development stage for assessing the transport efficiencies of the individual junctions and regions).

with an epitaxial layer of GaAs, about 1-3μm thick and heavily Zn doped (p-type $\geq 5 \times 10^{18} cm^{-3}$). Again these parameters have to be optimized later by photoemission and electrical measurements on the finished structure after proper cesiation. This GaAs layer also has to have an electrical contact, preferably a ring deposited around the boundary of this layer.

The fabrication process has two major aspects. The first is the epitaxial growth of the layered structure and the second is the processing to fabricate the device with electrical contacts.

3.1 Epitaxial Growth of ZnSe and GaAs:

With the information and experience available at the beginning of this project, the close-spaced HCl transport system as shown in Fig. 11 appeared as the appropriate growth system to be used initially to epitaxially grow a layer of GaAs on the ZnSe layer previously grown on Ge.

The device application for optical image formation requires that the finished structure should have a flat-smooth surface and the epitaxially grown layers be uniform in thickness, free of pits and hillocks. For minimizing interface recombination losses, the heterojunction interfaces should be free of foreign impurities and have a minimum of dislocations and traps. This requires careful processing of the substrate, minimum exposure of the first grown layer of ZnSe to the atmosphere and slow cool down of the grown layers. In the initial phase of the project the following polishing procedures were adopted to prepare the Ge substrates.

After lapping both sides of the wafer flat and parallel using 3μm Al_2O_3 grit, it was etched twice for 10 seconds each in white etch (1 HF:5 HNO_3). Then the growth side of the wafer was polished on a rotating Pellon pad using a 1-2% NaOCl solution. After this step, the growth size samples

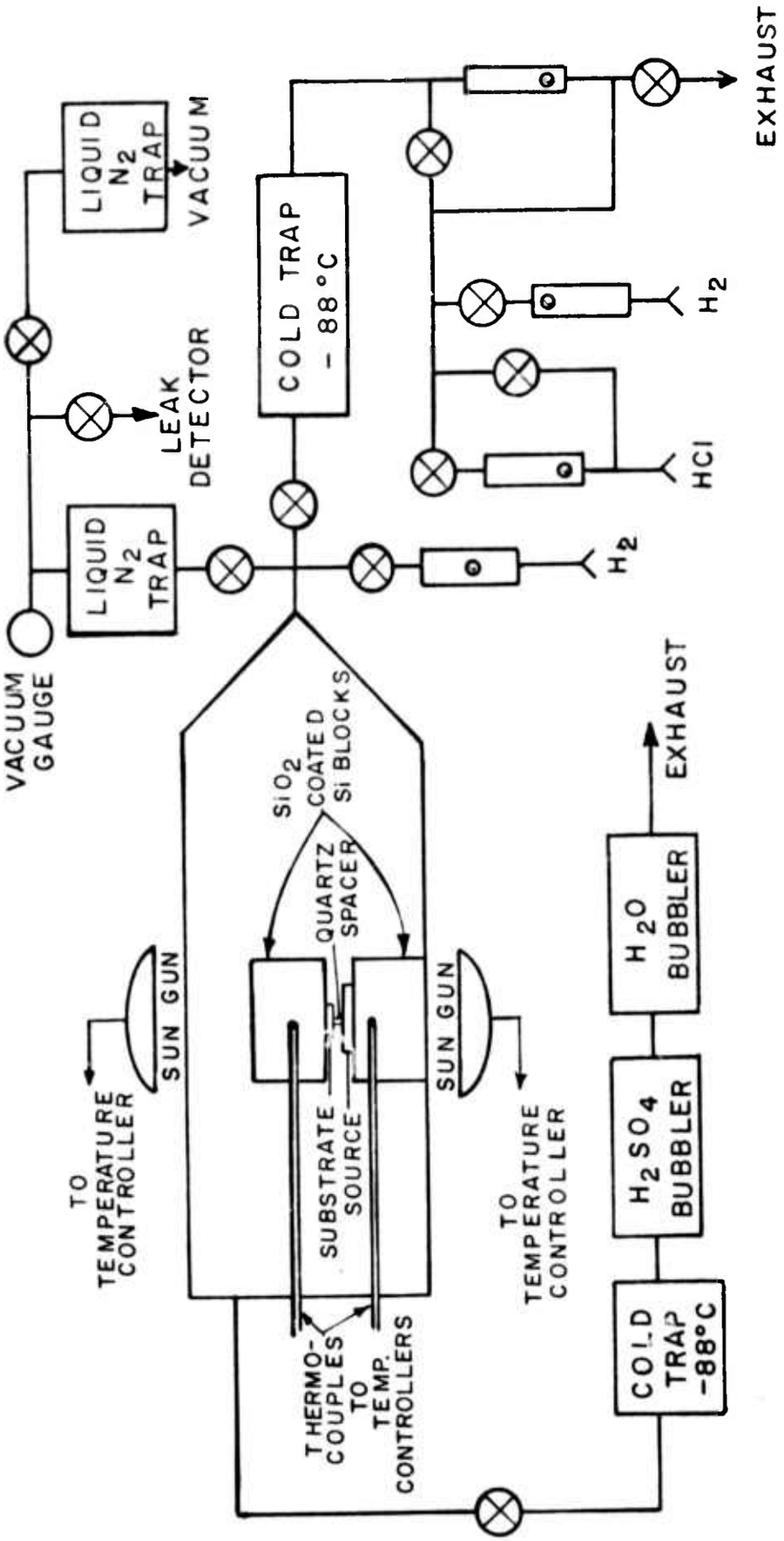


Fig. 11 Schematic diagram of the close-spaced epitaxial growth system.

were cut from the wafer and the back side was coated with a protective layer of SiO_2. The polished side was etched in HF to remove traces of SiO_2 deposited on this side and then treated in 1-2% NaOCl solution under ultrasonic agitation. Just before loading the sample in the growth system, the substrate was given a final polish etch. For (111) substrates, etching in a modified Superoxol etch (1 HF:4 H_2O_2:20 H_2SO_4) in a fast rotating beaker was found suitable while for (100) substrates, etching in 5 HNO_3:3 HF: 3 CH_3COOH in a still beaker was employed. The (111) substrates thus obtained had very smooth surfaces but the (100) substrates usually had several shallow pits, rectangular in shape.

Since the work of James et al[2] indicated best results for photoemission from the (111B) face of GaAs, some growth attempts were made on the (111) face of Ge. Although it is not clear how to ensure that the grown ZnSe layer will have the (111B) face on the top, theoretical considerations suggest that the (111B) face will be automatically favored because it is the faster growing surface in such a growth system. However the ZnSe growths on (111) Ge substrates formed a structure of triangular pyramids; the sides of the equilateral triangles varying from 5μm to about 20μm. Attempts to smooth out the growths by intentional misorientation of the substrate 5-8° off (111) did not succeed. The growths still showed inclined triangular pyramids.

The ZnSe growths obtained on (100) Ge substrates were much smoother, with very few features distinguishable under a metallurgical microscope (400x). The growth over the shallow pits in the substrate mentioned earlier smoothed itself out to result in relatively flat growth. Even though this growth feature helped in obtaining flat and smooth growths, Ge

substrate quality and arrangement of the close-spaced growth system needed improvement so that growths would be uniform in thickness resulting in better resolution of device. Fig. 12 shows the ZnSe growth morphology on Ge substrates and Fig. 13 shows an island of ZnSe isolated by etching.

A difficulty encountered with the close-spaced growth system as shown in Fig. 11 was mapping of the polycrystalline source crystal onto the seed during growth. If the source crystal is homogeneous and etches uniformly all over its surface, then we get a uniform growth. In the setup shown in Fig. 11 the quartz spacer sits on the source and substrate. This results in poor growth around the spacer because of change in growth dynamics near the spacer and the ZnSe layers grown in this setup were non-uniform. Since the design studies suggested that contact need not be made to the ZnSe layer, it became apparent that the fabrication procedure should be modified in a way to enable the growth of thinner ($\sim$ 1μm) and uniform layers of ZnSe. This required modification in the growth apparatus and also a thorough clean up of the gas metering system to give us reliable and smoother control of the flow rates. The Si blocks to hold the source and substrate crystals were modified to allow the growths to take place over the entire substrate surface. Fig. 14 shows the new arrangement. Now the substrate is held in place by gravity and is protected against sliding off-position by a proper size rectangular depression ($\sim$ 10 mils deep) in the lower Si block. The source crystal is held against the upper Si block at some preselected distance from the substrate by using quartz spacers as shown. Spacers of several thicknesses were prepared so that the effect of this distance on the growth features could be studied.

Various parameters affecting the growth quality and growth rate were

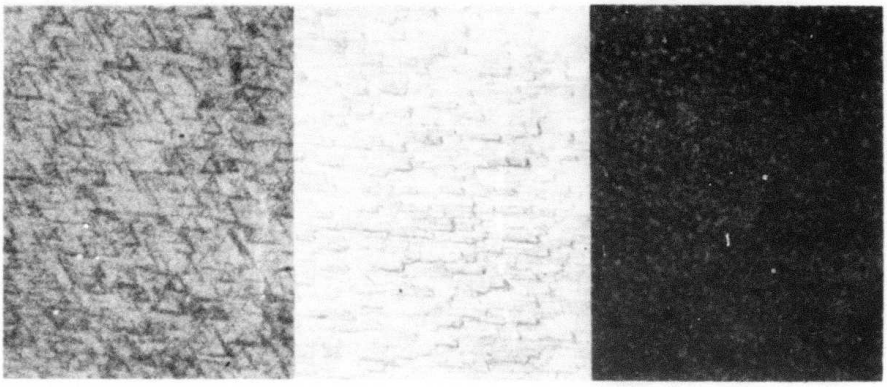


Fig. 12 ZnSe layer grown on Ge substrates

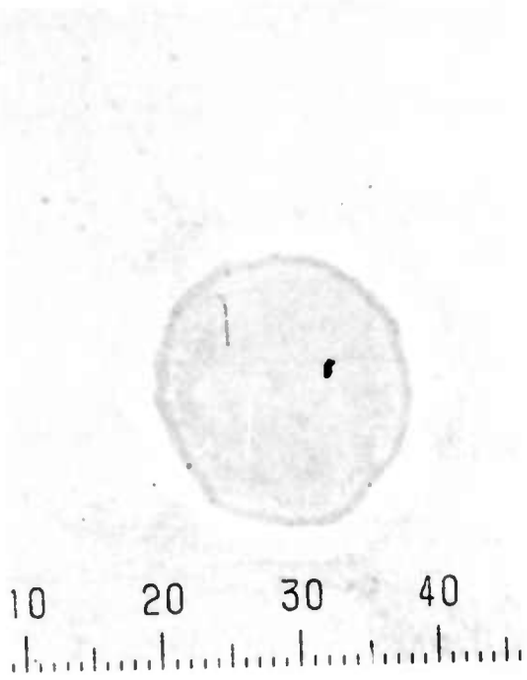


Fig. 13 2um ZnSe layer grown on (100) Ge

(10um per small division)

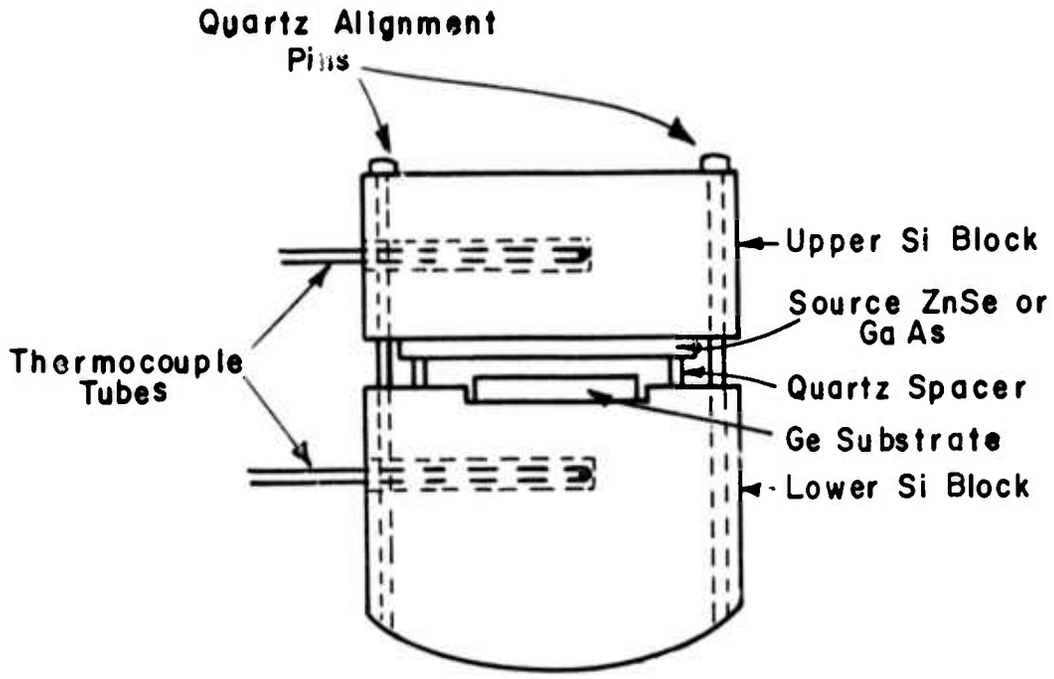


FIG. 14 New arrangement for holding samples during growth.

as follows:

(a) H_2 and HCl flowrates,

(b) Spacer thickness,

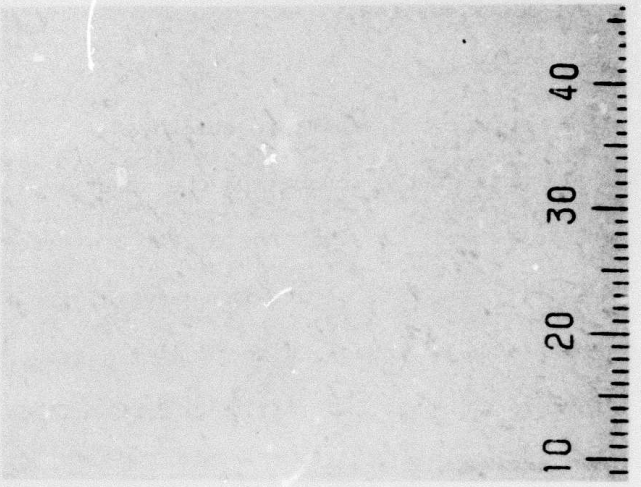
(c) Optimum source and substrate thickness,

(d) Temperatures of the source and the substrate.

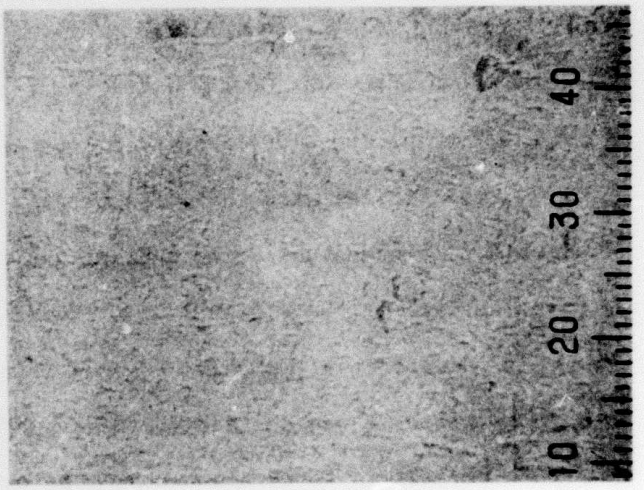
Growth runs were made to study the effect of these parameters on the growth quality and rate of growth. Several growth runs on (110) and (100) Ge substrates were made in the modified growth system. The new arrangement provided the expected fairly uniform thickness growth over the entire substrate surface.

The growth surfaces of ZnSe grown on (110) and (100) Ge substrates are shown in Fig. 15(a) and 15(b). The growth on the (100) plane is somewhat smoother in the area shown than that on the (110) plane and has fewer random features. In other areas the (100) growth is rougher and not as good as the best (100) growth obtained with the older blocks. This was probably a result of the growth parameters not being quite right for the new blocks. Imperfections on the surface of the polished Ge substrates, as referred to earlier, may serve as nucleation sites which produce irregularities in the grown ZnSe layer. Therefore it was decided to improve the polished surface and adjust the growth parameters to obtain smoother growths. Growths on the (100) and (110) planes are considerably smoother than those on the (111) or 8^{o} off the (111) plane. The latter show characteristic growth steps over the whole surface.

Fig. 16 shows a growth of ZnSe on (100) Ge in the modified growth system. The growth, $\simeq$ 6μm thick, is quite smooth and uniform over the entire Ge surface Fig. 16(a). In Fig. 16(b) there are some black spots

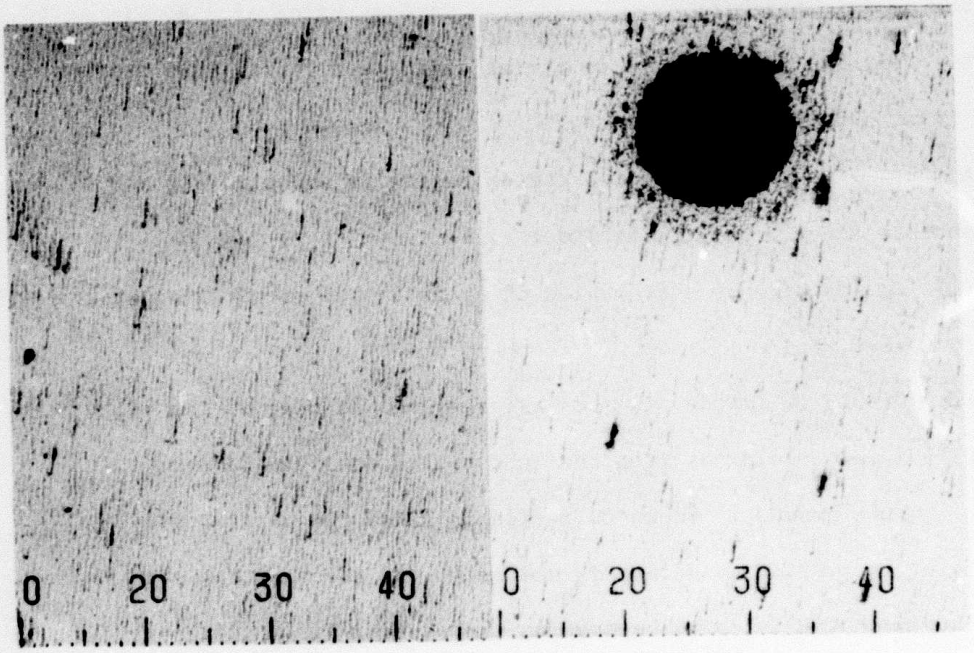


(a)



(b)

Fig. 15 Surface of ZnSe layers grown on (a) (110) Ge substrate at 565°C and (b) (100) Ge substrate at 542.5°C. A small division is 5μm.



(a) (b)

Fig. 16

ZnSe layer grown on 100 Ge at 582°C

a) Smooth surface area

b) Circular defect - inhibited growth

which we were able to reduce in number by careful seed preparation but not eliminate altogether.

Fig. 17 shows a scanning electron microscope photograph of the ZnSe layer (secondary emission mode) showing a magnified view of the circular black spots. As can be seen the smooth growth has considerable growth structure. As the defect is approached, the smoother ZnSe begins to break up into patchier growth and then into a region of very little growth. Near the center there is a ring of thicker growth that appears to surround a region of no growth.

A more magnified view of the center region is shown in Fig. 18. Explanations for the defects include:

(1) An impurity is left behind in areas in the preparation of the seed,

(2) Growth is impeded in some areas by HCl etching of the Ge,

(3) A particle drops from the ZnSe source onto the Ge seed.

Ge in the system is known to radically alter the growth rate[9] and a similar type of structure is seen near the edges of the seed where the Ge is most likely to be exposed to the surrounding environment due to an incomplete SiO_2 covering. In order to reduce the Ge which is available to react with the HCl, we tried different SiO_2 coating techniques. This is illustrated in Fig. 19. Growth runs with and without the backs of Ge seeds protected with SiO_2 as shown in Fig. 19, coupled with scanning microscope studies, have shown the growth morphology to be very dependent on the amount of Ge exposed to HCl. With careful SiO_2 coating and etching, the number of circular black defects was reduced to a minimum.

Effort was also made to further improve our close-spaced HCl epitaxy system. We tried to reduce possible trace oxygen contamination contributing

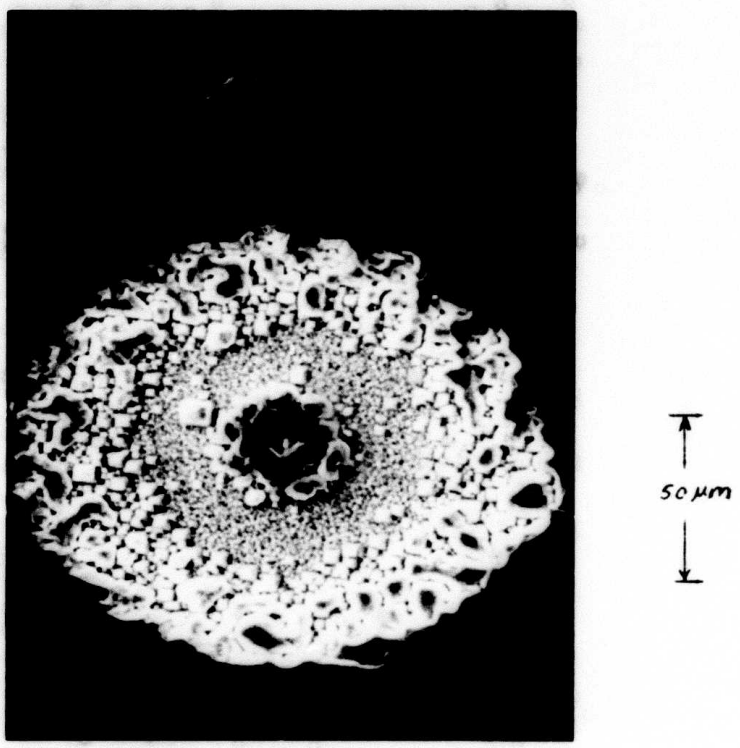


Fig. 17 SEM photograph of ZnSe layer on 100 Ge showing the circular area of inhibited growth and surrounding area of full growth.

Fig. 18 SEM picture of center of the circular defect.

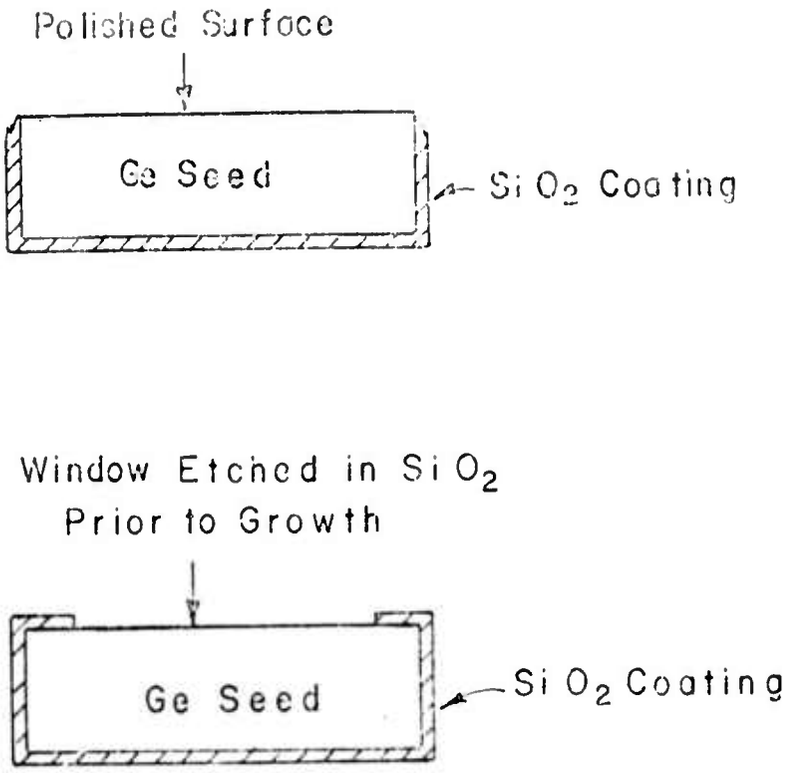


Fig. 19 Two Ge seed preparation techniques.

to irregularities in the growth. This included nitrogen bagging of all teflon connectors and valves, and heating of the main seal during closing. Electrical heaters were placed on all valve barrels having teflon stoppers. This helped minimize leakages along the valve barrels.

At one stage a leak check of the complete system showed that the palladium diffuser which supplied the hydrogen for the system had a leak in the palladium membrane. This probably was a contributing cause of many of our growth problems. A replacement palladium module was obtained and installed and frequent leak checks have been made since then to be sure it remained in good condition.

The final polishing etch step using NaOCl tends to leave a slight haze on the Ge surface. This was eliminated to some extent by using freshly made white etch (3HF: $1HNO_3$) instead of NaOCl in this step. The etching was followed by a rinse in high purity water ($\rho \geq 14$ MΩ) and surface was blown dry with high purity N_2 to achieve fast and uniform drying.

The cooling process after growth was changed by rearrangement of the control system on the heating lamps so that no significant temperature step would occur when switching from the growth conditions to a cooling rate of $2^{o}C$/min. for 2 hours. This minimizes growth strain due to thermal expansion coefficient mismatch.

Growth runs were done with various source-seed temperatures ($675^{o}C$-$600^{o}C$ is normal), source seed spacing (0.015" appears best) and HCl concentrations (0.02% - 0.04% is normal). Although in general ZnSe covered the (100) Ge seed for the normal growth conditions, there still was a tendency for a few spots of indifferent nucleation to appear on most seeds.

Table #2 shows the summary of early growth runs. Run #6 produced the best growth and device behavior that we have seen.

Performance of the growth system indicated that it needed improvement to give more reproducible growths. The following changes were made:

(a) Several modifications were made in the growth system to eliminate potential sources of contamination. A cold trap was inserted in the vent portion of the HCl-H_2 supply system to prevent back diffusion from an oil bubbler. This might have been a factor in causing some flow meters to stick and may have caused surface contamination on the seed. Static electricity was also found to cause some sticking of the flow meters floats. The rubbing of the sapphire float against the wall of the flow meter resulted in static charges on the inner wall of the flow meters which caused sticking. The problem was partially solved by discharging the float at intervals by allowing it to touch an earthed wire inserted in the base of the flow meter.

The HCl supply was replaced, a new regulator obtained, and the monel feed tube replaced with pyrex to eliminate corrosion contaminants from this source. The H_2 purifier was also repaired.

Other minor modifications were done in the growth system to reduce the system contamination. The exhaust end acid bubbler was replaced with an oil bubbler containing a low vapour pressure silicone diffusion pump oil (from Dow-Corning). During a thorough clean-up of the growth system a little vacuum pump oil contamination was found near the vacuum line connection to the growth system. This could have contributed contamination to the substrate and affected growth morphology. The vacuum pump has since been replaced

TABLE #2

SUMMARY OF DATA FOR PHOTOCATHODE GROWTH RUNS

PCS #	1	2	3	4	5	6	7	8	9	10	11	12
% HCℓ	.038	.022	.022	.038	.038	.038	.038	.022	.022	.022	.038	.038
Spacing (Mils)	>22	>22	>22	>22	~14 Uneven	15	15	15	9	9	15	15
Length of Run (Min.)	60	60	120	60	60	75	60	90	120	120	75	75
Temperature Source (°C)	675	673	675	675	675	673	675	650	650	650	675	675
Temperature Seed (°C)	561	576	550	582	596	582	580	600	600	600	591	593
ΔT (°C)	114	97	125	93	79	91	95	50	50	50	84	82
Growth Layer Thickness (μm)	3.9	<1	1.3	<.5	2.4	4-8	~3	4.1	0	-	2.9	3.1
Growth Rate (μm/hr.)	3.9	-	.67	-	2.4	-	~3	2.73	0	-	2.32	2.5
Seed Preparation	Polish NaOCℓ Superox Etch	Polish NaOCℓ HF NaOCℓ	Polish NaOCl HF NaOCl	Polish NaOCℓ HF NaOCℓ	Polish NaOCl Solv. NaOCl	Solv. HF NaOCℓ H_2O	Window HF Solv. NaOCℓ H_2O	Window HF NaOCl H_2O	Window H_2SO_4 Over-night H_2O	Window HF NaOCℓ H_2O	No Window HF NaOCℓ H_2O	Window HF NaOCℓ H_2O
Electrical Photo-Characteristics	-	-	-	-	Not Checked	Good, No Trapping	Trap-ping	Trap-ping	-	-	Some Trap-ping	
Remarks	Hillocks Bad Slow Cool	Thin Patchy	Patchy Cir. Defects	Thin Patchy	Some Patches Fairly Even	Even, Cir. Defects	Fewer Circ. Defects. Window Area Filled	"Hexagon Growth"	No Growth	Linde UHP H_2 Island Growth	Fairly Even Growth	Fairly Good Growth Over 80% of Ge Area

by a cryogenic sorption pump, in which no oil is used.

Another modification involved the lower Si-block that carried the Ge substrate in a rectangular notch. A new Si-block was prepared with a groove running across the top surface, Fig. 20, instead of a notch. Since the surface of the groove can be polished well, it removed the problem of uneven contact between the seed and the somewhat ridged surface of the notch. In the past this resulted in temperature gradients across the seed surface which were detrimental to the quality of the epitaxial growth.

(b) All flowmeters in the system were recalibrated. The actual gaseous flow rates were found to differ from the previously calculated rates by as much as a factor of 2. This error made the HCl concentration in the previous runs less than the expected percentages.

(c) Temperature corrections were determined for the temperature of the top surface of the lower Si-block by two different techniques. In one a GaSb crystal was placed at the top surface of the Si-block and its apparent melting point temperature was observed and compared with the established melting point. In the second technique a calibrated thermocouple (Fig. 21) was placed on the top surface of the Si-block and temperatures measured at the top of the lower Si-block. For a wide range of temperatures this correction was found to be between 1^{o} - $15^{o}C$. Therefore the original temperatures indicated on the system controllers for previous growth runs were adequately close to the true temperatures.

(d) Several growths were done with the improved system. These showed some improvement and in some growths a growth morphology similar to

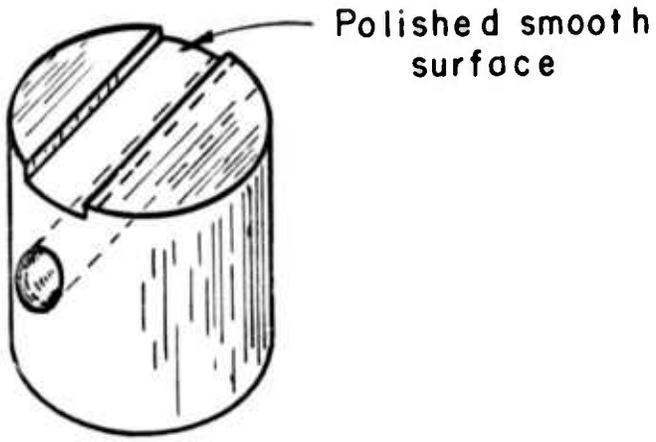


Fig. 20 Modified lower Si-block to ensure more uniform seed heating

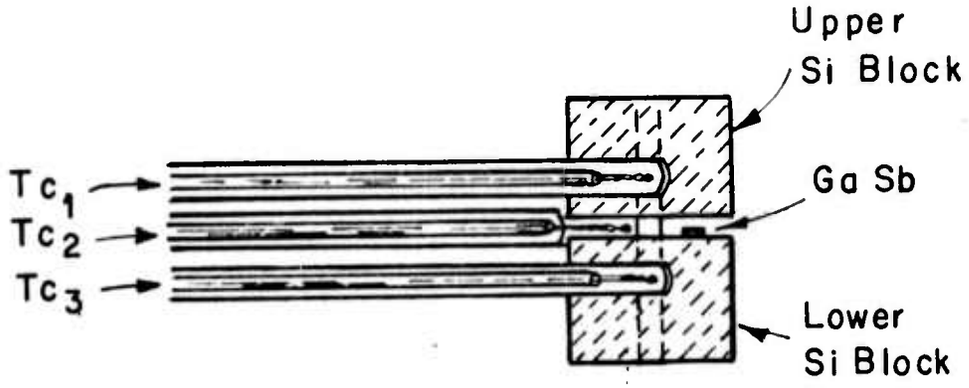


Fig. 21 Set up for temperature calibration measurements

GaSb melting point:

Tc_1	720°C
Tc_2	720°C
Tc_3	715°C
M.P.	(actual)
	703-712°C

Temperature correction:

Actual T is 8 to 17°C lower than block temp. at 700-750°C.

PCS-6 was obtained. PCS-6 was the growth that gave encouraging photo-response characteristics. However similar electrical characteristics have not been observed since. It appears that surface preparation of the Ge seeds is of critical importance.

(e) The effects of different surface preparation of the growth morphology was investigated by growing ZnSe simultaneously on two germanium substrates having different final etching techniques. The best growths obtained have been on germanium substrates which have had a final etch of NaOCl. The final etchants tried to date listed in the order of the quality of the growths obtained are NaOCl: White Etch: CP4:HF:No etch. An Auger spectrometer has recently become available and has been used to determine the effects of various surface treatments and preparation. The results are described in Appendix C.

If any of these etches were used to remove extensive material the resultant surface was deteriorated, hence it was not clear that all work damage is removed. Therefore various new schemes were tried to prepare Ge seeds free of scratches and etch pits. None gave the final perfection desired of the Ge seed. Various techniques tried include

i) HCl vapor phase etching of (100) Ge seeds in flowing $HCl-H_2$ atmospheres

ii) Hand lapping with colloidal silica

iii) Hand lapping with successive 3μm, 1μm and 0.3μm aluminum oxide grits followed by hand lapping with

.05μm grit slurried with 5% NaOCl solution. This is a chemical and mechanical polishing step. However we still found scratches on seeds or faint haze on the (100) surfaces.

A recent note by D.B. Holt comments on difficulties in obtaining repeatable epitaxial growth of ZnSe on (111) Ge.[10] Presumably his problems, like ours, were connected with or made worse by difficulties of achieving adequate substrate finish and system cleanliness.

(f) Recent growth runs showed uniformity of the grown layers and freedom from "stains." However the substrate often showed signs of slight etching of the seed under the ZnSe. When this was observed the ZnSe perfection was not good and the diode characteristics of the junction either showed undesired switching action or had rather high leakage currents.

(g) It was suspected that the quality of the solvents used in the substrate preparation might be a cause of irregular and non-reproducible surfaces. The use of redistilled acetone reduces the presence of haze often seen on prepared substrates. Therefore the purities of these solvents were checked using the gas chromatography. The results indicated that most the solvents in use were reasonably pure and should not have caused any problem in the growth of ZnSe on Ge.

In order to obtain better final seed finish, etching of germanium substrates in gaseous hydrogen chloride was tried. These experiments were similar to those done by Amick and Roth.[8]

However the results, summarized in Table 3, show that poor surface finishes were obtained. It was not obvious why the etching of (100) Ge was not as good as that on (111) Ge described in the Amick and Roth work.

Numerous ZnSe on Ge growth runs were made in the modified growth apparatus. Some of the growth runs resulted in good ZnSe layers covering more than 80% of the Ge seed, but none resulted in good device characteristics. Some of the devices made showed trapping phenomena and others showed bad junction characteristics. Table 4(a) and (b) show a summary of the growth runs made on (100) Ge seed material. There were some indications that HCl etching of the Ge seed occurred before the ZnSe initial coating and that this affected the crystal perfection and the electrical characteristics.

4. Measurement of the Electron Transport Properties in Ge/ZnSe/GaAs:

The requirements for satisfactory performance of the multi-layer structures involve many factors which needed to be evaluated. Such factors were:

a) High transfer efficiency of the electrons, photo-induced in the germanium, across the pGe-νZnSe interface.

b) Transfer of the electrons through the ZnSe to the GaAs interface without serious recombination loss (or trapping effects). If the ZnSe layer is 1μm thick this will require an electron diffusion length of several microns.

c) Efficient transfer of the electrons through the νZnSe-p^+GaAs interface without significant loss due to interface recombination or trapping.

d) Adequate electron lifetime in the p^+GaAs layer. The electron diffusion lengths observed by James et al for GaAs doped with 4×10^{19} Zn atoms cm^{-3} and 1×10^{19} Zn cm^{-3} were 1.0μm and 1.6μm respectively.

TABLE 3

Gaseous HCℓ Etching Experiments on (100) Germanium

	HCℓ-1	HCℓ-2	HCℓ-3	HCℓ-4
Seed and Preparation.	(100)Ge with SiO_2 coating on one side. Size - .36" x .24" Prepolished, methanol cleaned, and dried.	Terminated seed from HCℓ-1. Dusted off with a Q-tip prior to loading.	(100)Ge (G.D. 13705) Size .36" x .24" x 15 mil. SiO_2 coated, Lapped 1 μm, 3 μm, solvent cleaned, H_2O, dried.	(100)Ge, (G.D. 13705) Prepolished. SiO_2 coated. Lapped 3 μm, 1 μm, .3 μm, solvent cleaned. White etch. Solvent. N_2 dried.
% HCℓ	15% *	15% *	15% *	.5% *
Time	5 min. in situ.	10 min. in situ.	10 min. in situ.	5 min. in situ.
Temp	820°C.	820°C.	830°C.	805°C.
H_2 Pre-bake	10 minutes	15 minutes	10 minutes	5 minutes at 820°C.
Slow Cooling	no	no	no	-
Etched Thickness	18 μm	47 μm	29 μm	-
Appearance	Shiny. Some scratches, etch pits visible to naked eye 20 - 40 μm in size. EPD $100/cm^2$.	Scratches removed. Edges etched round. Shiny near center. Same density of etch pits. Dull and hazy near the edges.	Similar to HCℓ-2. Pronounced edge haze. Most of the scratches gone. Large etch pits present.	Similar to HCℓ-3 -

* uncorrected.

TABLE 4(a)

SUMMARY OF DATA FOR PHOTOCATHODE GROWTH RUNS

PCS #	13	14 A	14 B	15 A	15 B
% HCℓ	.038	.038	.038	.038	.038
Spacing (Mils)	15	15	15	15	15
Length of Run (Min.)	90	90	90	125	125
Temperature Source (°C)	675	675	675	675	675
Temperature Seed (°C)	590	590	590	576	576
ΔT (°C)	85	85	85	99	99
Grown Layer Thickness (μm)	-	-	-	4	4
Growth Rate (μm/hr.)	-	-	-	2	2
Seed Preparation	No SiO_2, solvent, white etch (3:1, 15 sec.) H_2O N_2 dried.	Solvent, Annealed @ 600°C 20 min., SiO_2 HF NaOCℓ, solvents, N_2 dried.	Solvents, Annealed @ 600°C 20 min., SiO_2. HF solvent, N_2 dried.	SiO_2 window HF H_2O White etch, solvents N_2 dried.	SiO_2 window, HF, H_2O NaOCℓ, solvents, N_2 dried.
Electrical Photo-characteristics	-	Trapping	Bad diode char.	Trapping	Trapping
Remarks	Island growth, Ge badly etched. Go back to SiO_2 coating (G.D. 13705)	Good growth and good coverage of the seed. (GD 143136).	Dull patchy growth good coverage. (GD13705)	Dull growth, good coverage. (GD143136)	Shiny in some areas good coverage. (GD 13705)

TABLE 4(b)

SUMMARY OF DATA FOR PHOTOCATHODE GROWTH RUNS

16 A	16 B	17	18	19	20	21
.038	.038	.012	.04	.04	.04	.04
15	15	15	16	13	7-17	11
80	80	180	75	120	75	90
675	675	675	768	768	678	676
575	575	600	667	682	591	589.5
100	100	75°C	101	86	87	86.5
17.2	8.4	-	-	very thin	nil	-
12.9	6.3	-	-	-	-	-
solvents, SiO_2 window, HF, CP-4 solvents, N_2 dried	solvents, SiO_2 window, HF, NaCOℓ H_2O, N_2 dried	solvents, SiO_2, HF white etch, H_2O N_2 dried	SiO_2, lapped 3μ, 1μ, .3μ, solvents, white etch, H_2O, N_2 dried	SiO_2, white etch, solvents, H_2O, N_2 dried	SiO_2 Lapped 3μ, 1μ,.3μ, .05μ grit + NaCOℓ (5%), H_2O, solvents, N_2 dried	Lapped 3μ, 1μ, .3μ, .05 + .5% NaCOℓ, SiO_2, white etch, solvent, N_2 dried
Trapping	No Trapping	-	Bad diode char.	-	-	Trapping
Good shiny growth, good coverage, GD143136	Good shiny growth good coverage, low breakdown voltage GD13705	Good coverage. Dull growth, baked at 560°C for 90 min in situ. GD13705	Good coverage, HCℓ gaseous etching, see HCℓ-4 etch expt GD13705	Patchy growth poor coverage GD13705	Practically no growth.	100% coverage by a glassy ZnSe layer.

With Cs treatment the 4 x $10^{19}cm^{-3}$ material gave the best results, but with CsO treatment, the lighter doped material was better. It appears therefore that we should aim for a doping of 1x $10^{19}cm^{-3}$, a diffusion length of 1.6μm or greater and a layer thickness of 1μm or less.

e) Good emission efficiency from the Cs-O treated GaAs layer is also required in our structure.

f) Good ohmic contacts are required to the p^+GaAs and the pGe layer. Because the doping levels are high in these layers, it is not considered likely that these contacts will present any great difficulty. Evaporated silver, with a short heat treatment at 400°C, could be used on the p^+GaAs and indium could be used on the pGe.

Consider each of these factors in more detail. It should be possible to learn something about the interface performance and electron diffusion length in ZnSe by studying the behavior of pGe-νZnSe diode structures with electrons created in the Ge by photon initiation (with energy in the range 0.7 eV - 2.6 eV). If the ZnSe layer thickness is varied (perhaps by step etching of a growth starting at say 4μm) some information might be achievable on the effective electron diffusion length in the ZnSe, as well as on the interface transmission loss. The difficulty with the experiment, however, is likely to be the high resistivity of the ZnSe creating field effects and the related uncertainty of the behavior of the contact to the νZnSe.

Similar studies with a p^+GaAs-νZnSe structure with electron flow from the GaAs to the ZnSe might also tell us something about recombination at this interface. However, as the electron flow is in the opposite direction to that in the actual structure, the results may not be directly relevant.

Transistor action has been observed in nZnSe/pGaAs/nGaAs structures by the principal investigators in earlier work. But this was for nZnSe/pGaAs/nGaAs junctions under high injection conditions and with dopings that were not quite the same as planned for the present device. However it is possible that some p^+GaAs/νZnSe injection studies would be worthwhile. A further reason for such studies would exist if thick p^+GaAs layers (say 5μm) were grown since then electron diffusion length studies in the GaAs can be made by angle lapping and an optical probe or by electron beam sweeping with a scanning electron microscope.

Since the GaAs will be heavily doped, it will not be possible to determine the doping level by Schottky barrier depletion capacitance measurements. Reflectivity versus wavelength measurements have been successfully applied to determine doping in p^+GaAs by Pearson.

With the above group of measurements completed, the next logical step would be a study of the three-layer structure pGe/νZnSe/p^+GaAs with applied injection through the Ge. For these studies, it would not be necessary to coat the GaAs with Cs or Cs-O. Initially a simple ohmic contact should be sufficient, and the next step may be a water Schottky barrier contact. Recently Esher and Williams[4],[5] have obtained internal quantum yield curves using a water electrolyte Schottky contact and have shown those curves to be almost identical in shape to vacuum photoemission activation yield curves near threshold for negative electron affinity semiconductors like GaAs.

Figure 22 shows schematically an arrangement for making a water Schottky barrier contact to the GaAs. The light is shone incident on the GaAs so the structure would be operating in the reflection mode. The light could instead be shone on the Ge and measurements made in the transmission mode.

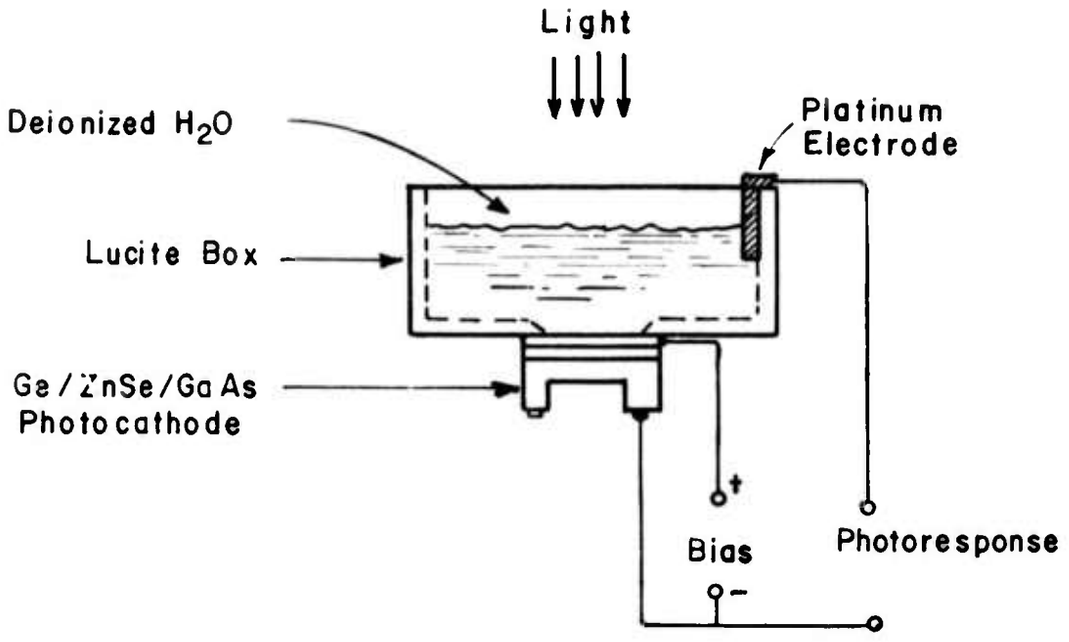


FIG. 22 H_2O Schottky Barrier Contact
(shown in reflection mode)

The first step in the direction to evaluate the device performance was to study the photoresponse of pGe/νZnSe junctions. Appendix (A) describes the details of fabrication for such a device.

Several pGe/νZnSe heterodiodes were provided with contacts (In and In + 2% Zn) and it was found that on reverse bias at 300°K most of them exhibited a certain switching action. Fig. 23 gives a plot of typical V-I characteristics of a pGe/νZnSe diode which shows the switching behavior. This switching action has been described [6],[7] as an electron trap filling action in the ZnSe near the interface. In some instances less than 1 volt of reverse bias could be applied without such switching action taking place. The reverse biased diodes were set up for monochromatic illumination through the ZnSe face. Fig. 24 shows a schematic diagram of the system for photoresponse measurements on the ZnSe/Ge junction. The spectral range was from 0.7 eV to 3.0 eV with many of the studies done between 1 and 1.45 eV photon energy. There was difficulty in deciding on the active collecting area in such an experiment since the effective collection area was affected by the high resistance of the ZnSe. The photo effect observed for electron transmission from the Ge to the ZnSe could represent yields of between 2.6% to 0.023% depending upon the area of collection chosen. To eliminate this uncertainty in value of the quantum yield figures we decided to obtain yield figures by illuminating from the Ge side.

Several pGe/νZnSe heterodiodes were made from growth runs done in the modified close-spaced HCl epitaxy system. Contacts were made to the νZnSe and the pGe with indium spheres and HCl as a flux in the alloy stage. Later we found In-Zn to provide an improved contact. I-V characteristics of diodes made from several runs showed switching action for many diodes but not all.

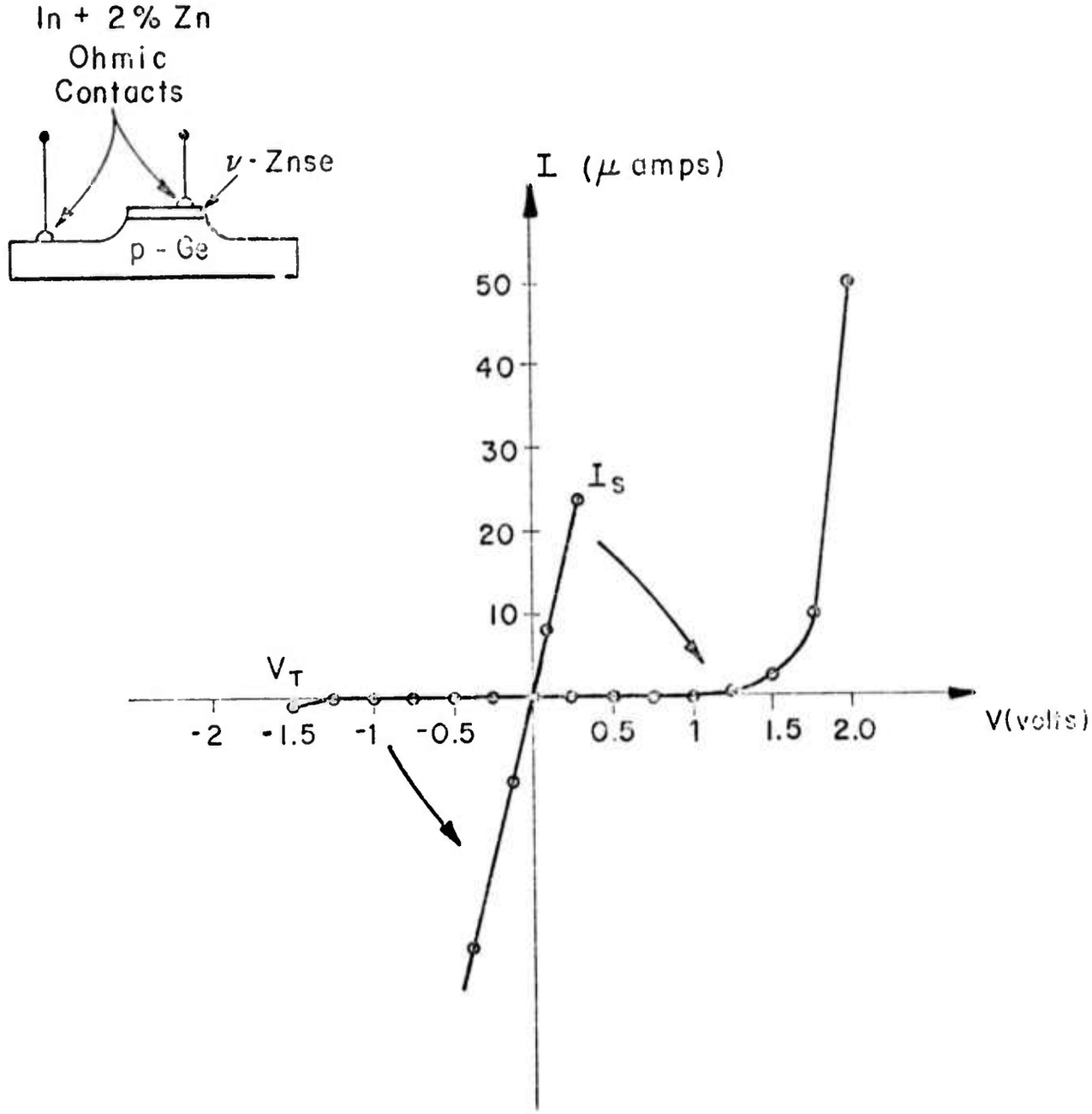


Fig. 23 Plot of typical V-I characteristics of ν-ZnSe/pGe diode, which shows switching behavior. (PES-5, S-4)

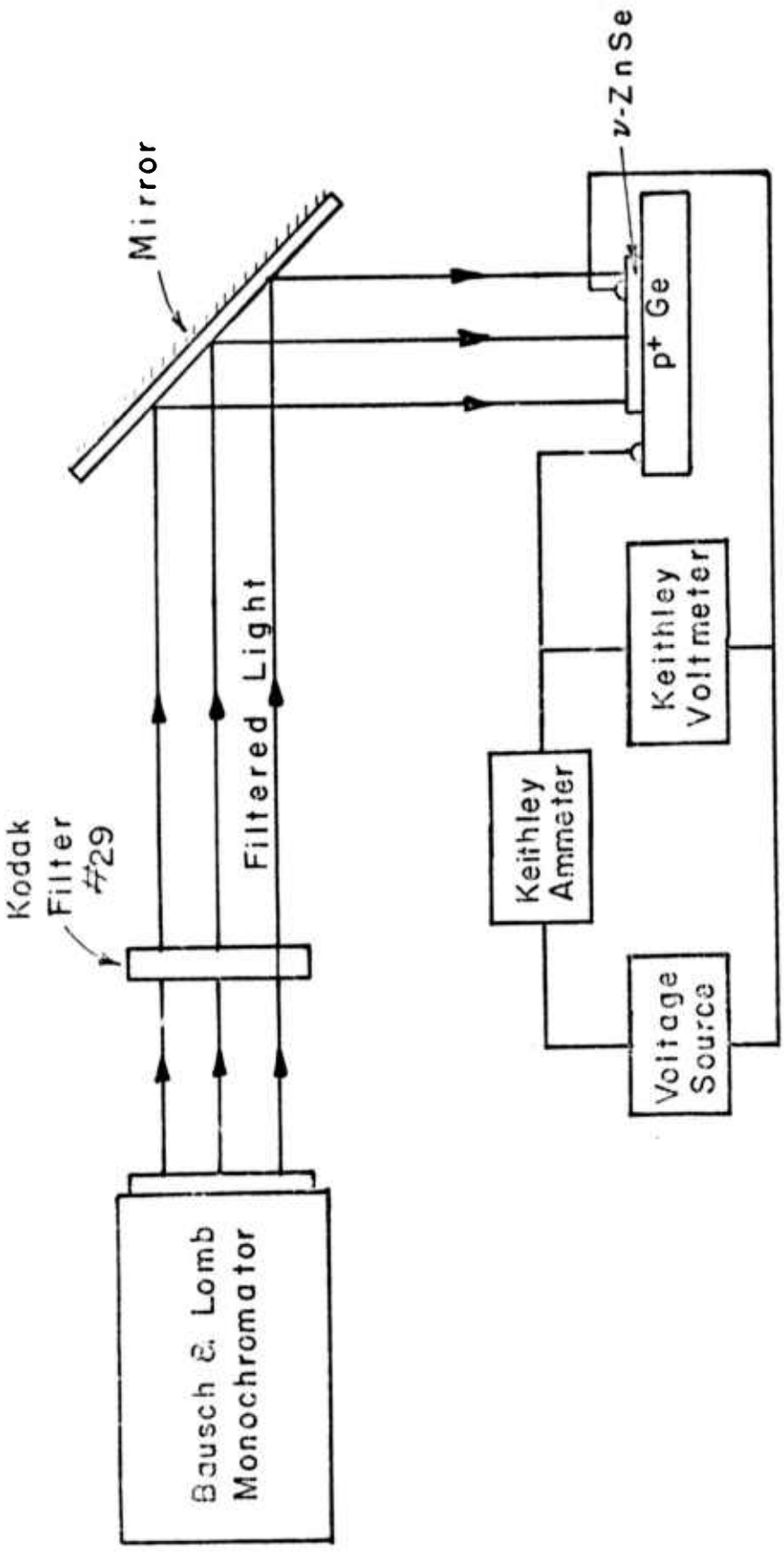


Fig. 24 Schematic diagram of system of photo-response measurements of the ZnSe/Ge junction.
(This shows illumination from the ZnSe side. In later studies the junction was illuminated from the Ge side.)

Those made from run PCS-6 showed no switching while most diodes from other runs showed switching behaviour.

The completed diodes were mounted on molybdenum discs with the ZnSe-In adjacent to the molybdenum, as in Fig. 25. In this arrangement the input radiation was incident on the Ge and generated electron-hole pairs quite close to the surface.

Hovel and Urgell[7] state that slower growth rates result in less trapping action, although it is unclear whether crystal imperfections in the ZnSe or Ge doping should be blamed for the switching action. (Growth run PCS-13 shows that growth is very significantly affected by the presence of Ge in the growth tube). Lowering the device temperature increased the reverse voltage that could be applied before switching occured. Lowering the temperature should also increase the quantum efficiency. Hence to study the above mentioned effects a cooling chamber was built using a two-stage thermoelectric cooler so that photoresponse measurements could be made at lower temperatures. Fig. 26 illustrates the cooling chamber. A summary of the photoresponse measurements made on two diodes from PCS-6 is shown in Table 5. Appendix (B) shows the calculation steps in arriving at the quantum yield figures given in Table 5. Fig. 27 gives the schematic diagram of the setup for the initial photoresponse measurements.

The significant results were the marked increase in quantum efficiency in the presence of room light falling on the ZnSe and the increase in efficiency as the temperature was reduced from 23^{o}C to -15^{o}C using the thermoelectric cooler. There can be several mechanism which separately or combined can account for this increase in efficiency. The two dominant effects could be either the room light filled the traps, or reduced ZnSe resistivity so that the effective junction area was reduced. There was

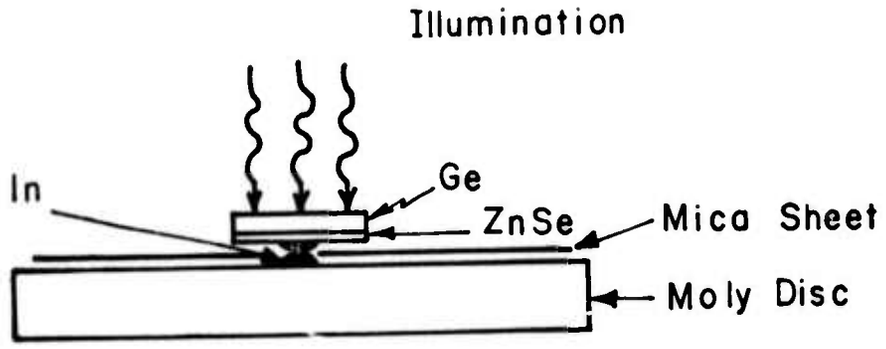


Fig. 25 Sketch showing a ν ZnSe/pGe heterodiode mounted on a molybdenum disc.

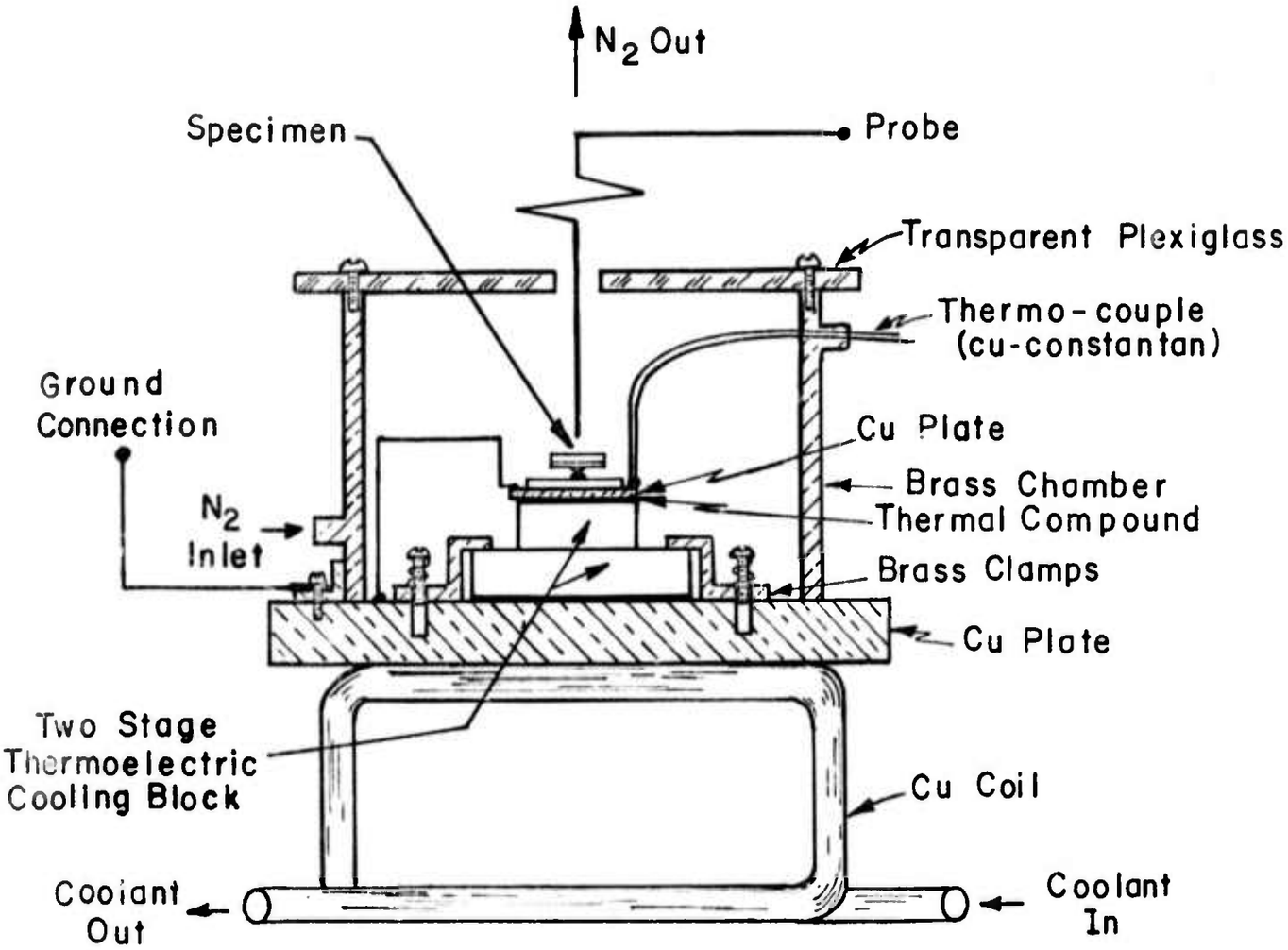


Fig.26 Schematic diagram of the cooling chamber.

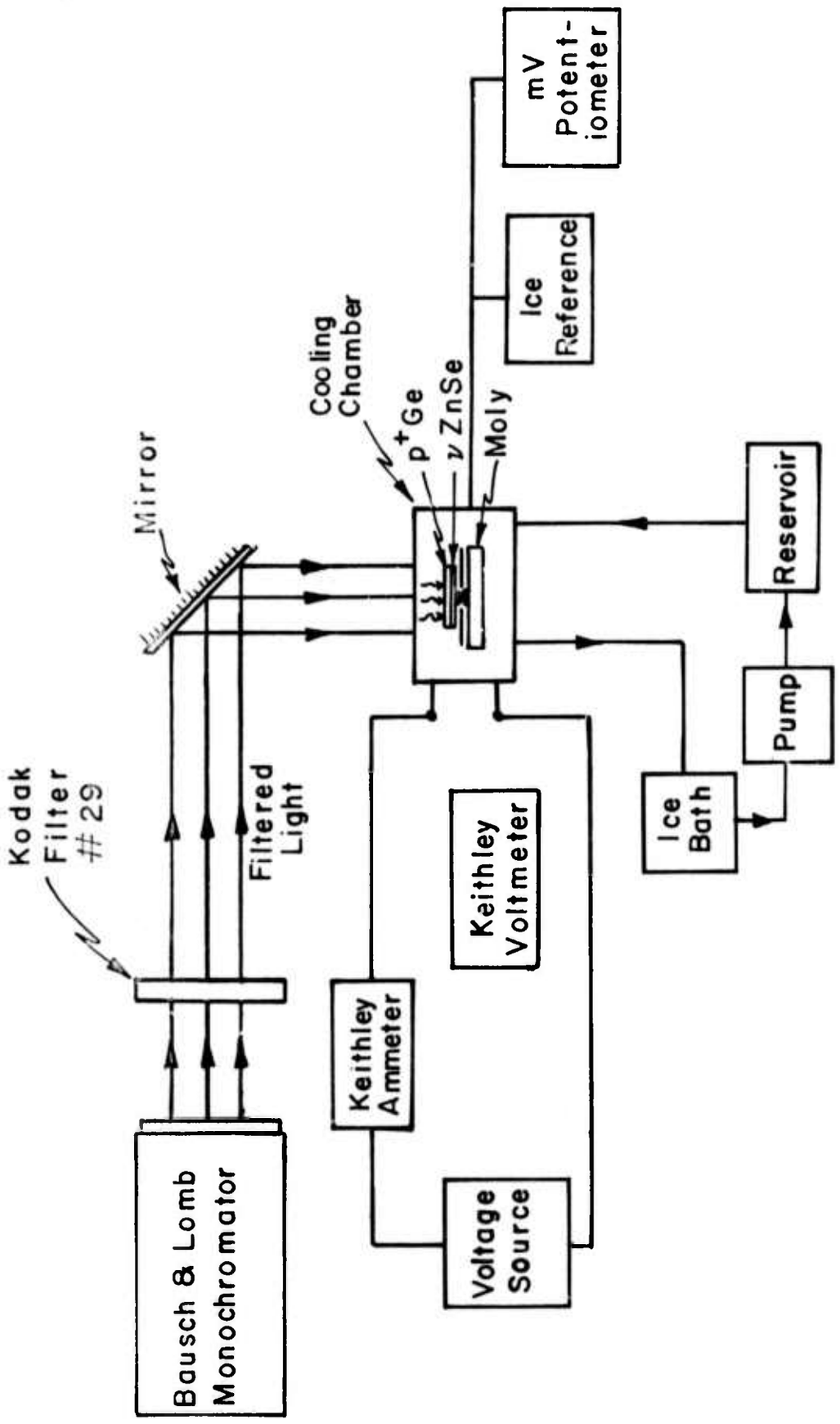


Fig.27 Schematic diagram of the system for photo-response measurement of a ν ZnSe/p Ge heterodiode at lower temperature.

TABLE 5 QUANTUM EFFICIENCY OF pGe/nZnSe DIODES*

(A) PCS-6, S-4

Temp.	Room Light	Dark Current	Photo + Dark Current	Quantum Efficiency
23°C	No	1.0×10^{-10}A	1.5×10^{-10}A	0.07%
23°C	Yes	6.7×10^{-10}A	6.0×10^{-9}A	7.7%
-10°C	No	1.0×10^{-10}A	1.5×10^{-10}A	0.07%
-10°C	Yes	4.5×10^{-10}A	1.2×10^{-8}A	17.6%

(B) PCS-6, S-8

Temp.	Room Light	Dark Current	Photo + Dark Current	Quantum Efficiency
23.5°C	No	0.9×10^{-10}A	1.4×10^{-10}A	0.067%
23.5°C	Yes	1.5×10^{-10}A	1.25×10^{-8}A	16.13%
-15°C	No	0.4×10^{-10}A	1.4×10^{-10}A	0.134%
-15°C	Yes	1.5×10^{-10}A	1.7×10^{-8}A	21.7%

* Source- 1μm radiation from a Bausch and Lomb monochromator which was passed through a #29 Kodak infrared filter to remove second order radiation.

some evidence for the trap filling mechanism, a) when the light was turned off there was a slow transient, b) the efficiency was increased at low temperatures and c) the maximum expected increase due to the area effect was 9 compared to an observed 250.

The improved quantum efficiency was quite encouraging and suggested that a detailed investigation was needed to determine the mechanism which was responsible for the increase.

It was decided to make photoresponse measurements in the presence of the bias light of various wavelengths and intensity. A cooling chamber employing a two-stage thermoelectric cooler was built to permit experiments at lower temperatures. Fig. 28 shows the schematic diagram of the system for photoresponse measurements of a νZnSe/p-Ge heterodiode in the presence of biasing light and at reduced temperatures.

A set of experiments was conducted at room temperature to determine the effect of bias light wavelength (or energy) on the gain while keeping the intensity of the source constant. Gain was defined as follows:

$$\text{Gain} = \frac{\text{Photocurrent due to infrared radiation in presence of biasing light}}{\text{Photocurrent due to infrared radiation in absence of biasing light}}$$

As the energy of the bias light was increased above 2eV significant improvement in the gain was noticed. For bias light of energy greater than 2eV the gain increased as the intensity of the bias lig was increased. Below a bias light of energy 2eV the increase in gain with intensity was very small. Fig. 29 and Fig. 30 show these results.

It was considered that since and ZnSe contact did not cover more than

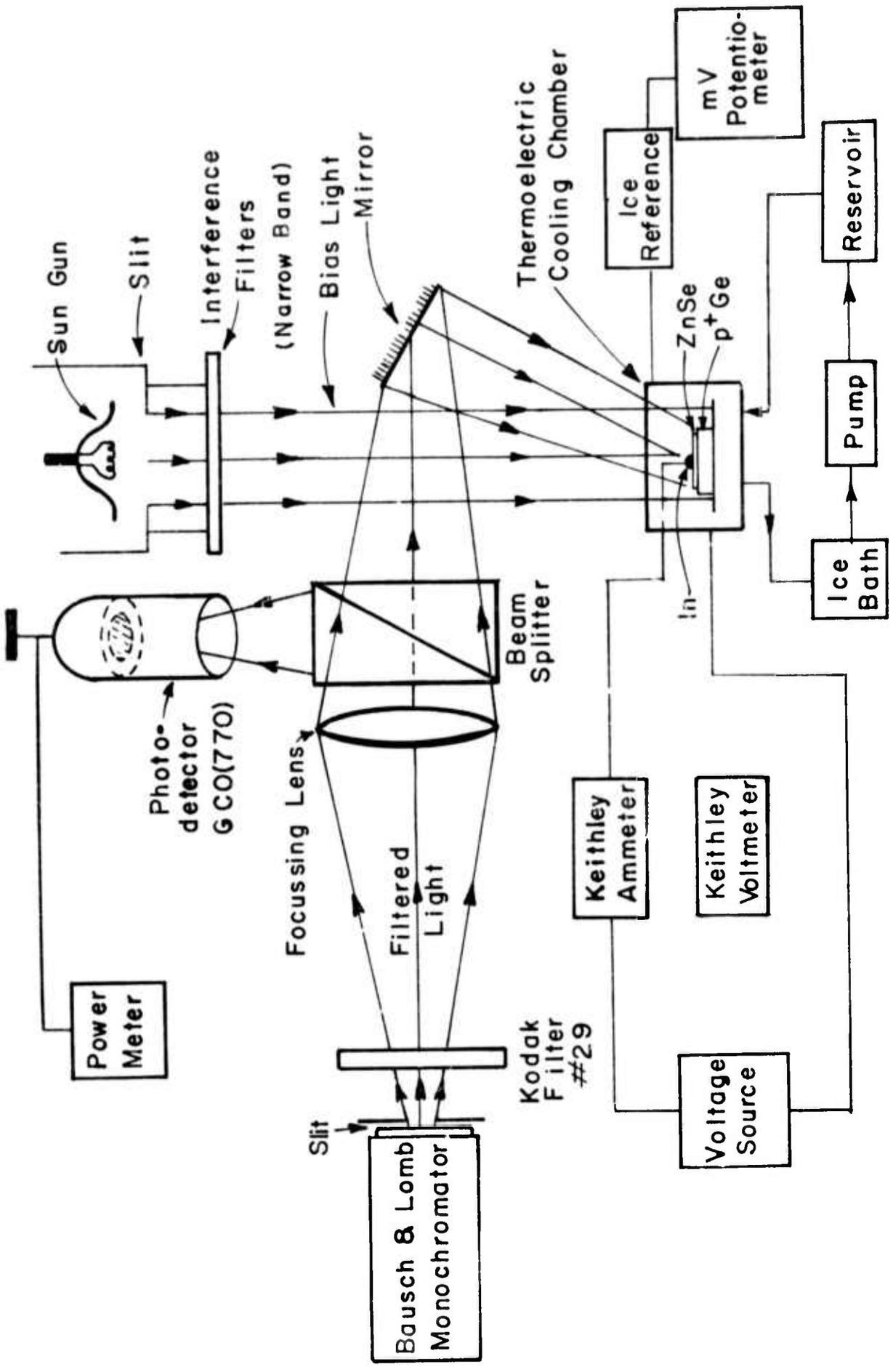
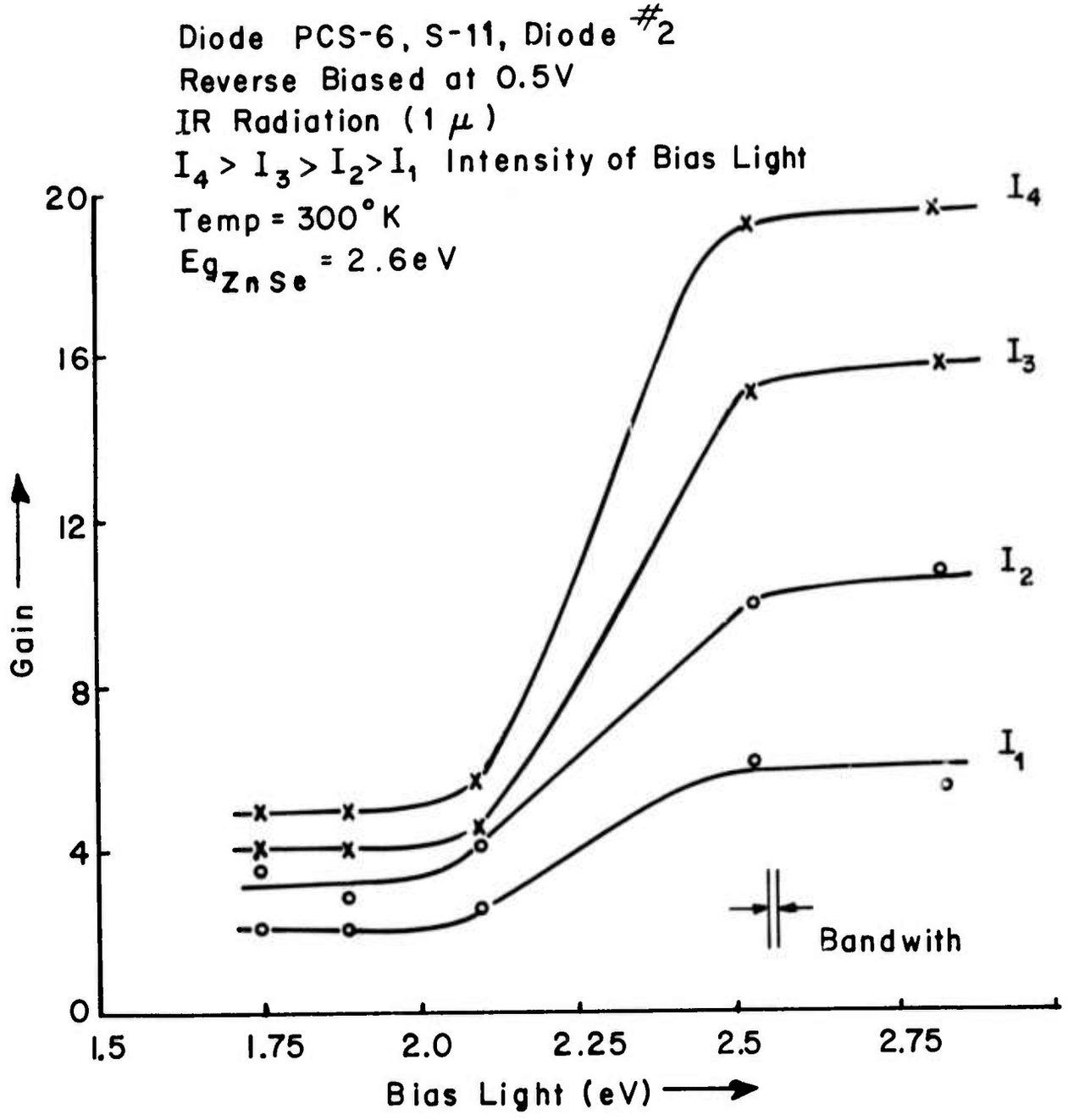
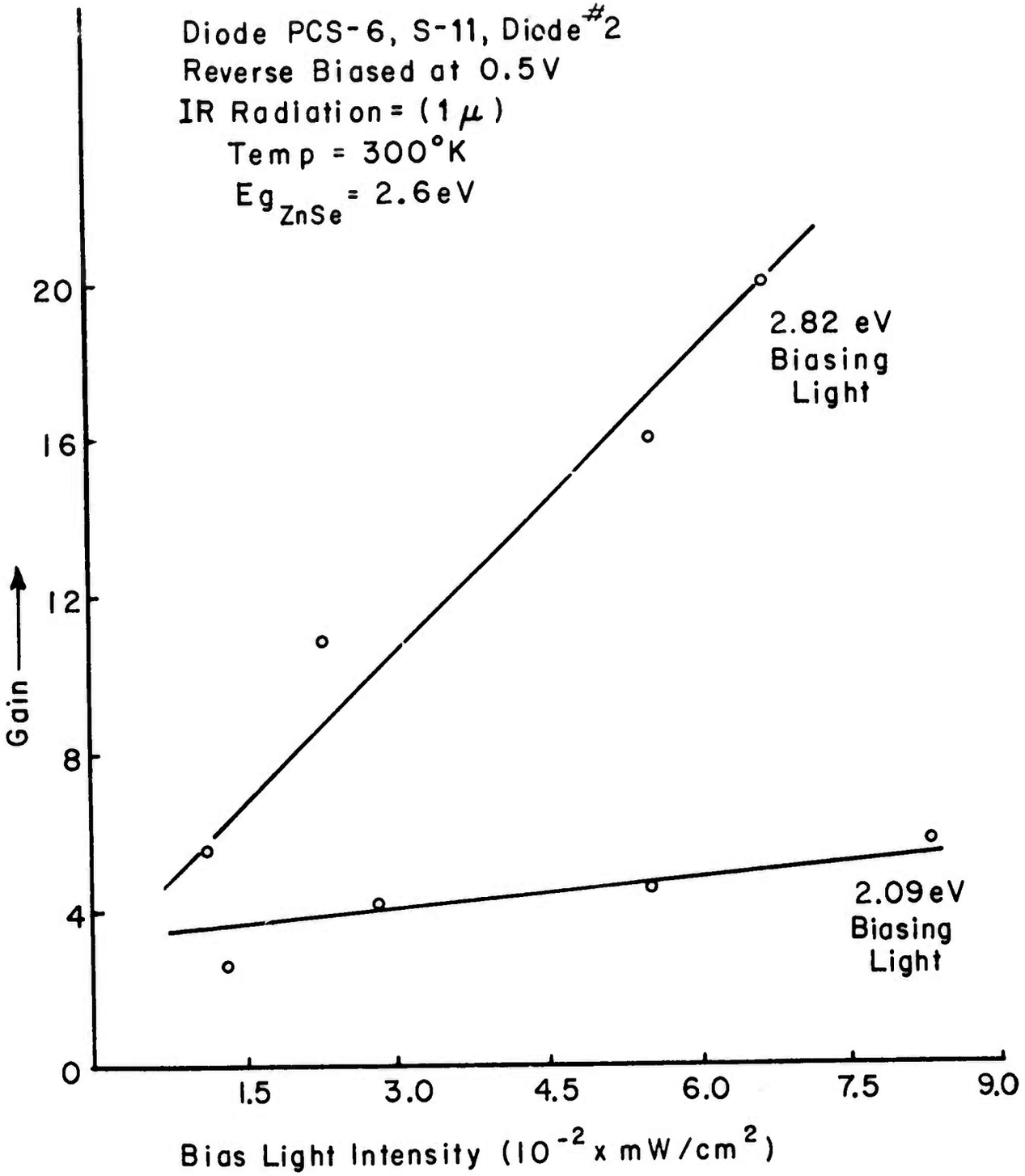


Fig. 28 Schematic diagram of the system for photo-response measurement of a vZnSe/p-Ge heterodiode in presence of biasing light, and at reduced temperature.



$$\text{Gain} = \frac{\text{Photocurrent Due To IR Radiation In Presence Of Biasing Light}}{\text{Photocurrent Due To IR Radiation In Absence Of Biasing Light}}$$

Fig. 29 Variation of gain with bias light wavelength and intensity



$$\text{Gain} = \frac{\text{Photocurrent Due To IR Radiation In Presence Of Biasing Light}}{\text{Photocurrent Due To IR Radiation In Absence Of Biasing Light}}$$

Fig. 30 Variation of gain with bias light intensity for two photon energies

a small part of the layer some of the effect of the bias light might involve a change of the ZnSe resistance and so change the area over which the photo-induced current was collected. To determine the extent of the area modulation effect upon the gain increases, a two-diode system experiment was conceived which is shown in Fig. 31. Photoresponse measurements on the diodes were taken separately and with both connected in parallel. The results plotted in Fig. 32 for various light intensities show that bias light of high intensity and high energy produced an area of modulation collection effect of 30%. Hence the area effect cannot be responsible for all the increase in gain observed (up to a factor of 20) with the bias light.

Further bias light experiments were done at reduced temperatures to fully characterize the effects and determine the extent of its usefulness in a photocathode device. The effect of the IR radiation intensity was investigated on the gain. The photocurrent increased linearly as a function of IR radiation intensity which was the expected result. Fig. 33 and Fig. 34 show plots of photocurrent vs. IR radiation intensity for different bias light intensities. The photocurrent plotted was in the presence of the biasing light. Photocurrent in the absence of the biasing light was a constant value. Fig. 35 and Fig. 36 show gain vs. bias light intensity for two different temperatures ($293^{o}K$ and $273^{o}K$). There was an increase in quantum efficiency as the temperature was lowered, but the improvement was not sufficient to be exciting, and typical quantum efficiencies were only a few percent.

Some transient effects of the bias light reported previously indicate trapping phenomena were involved in the transport of electrons across the Ge/ZnSe interface. It was decided therefore to attempt to characterize the device in terms of the active trap levels and their densities.

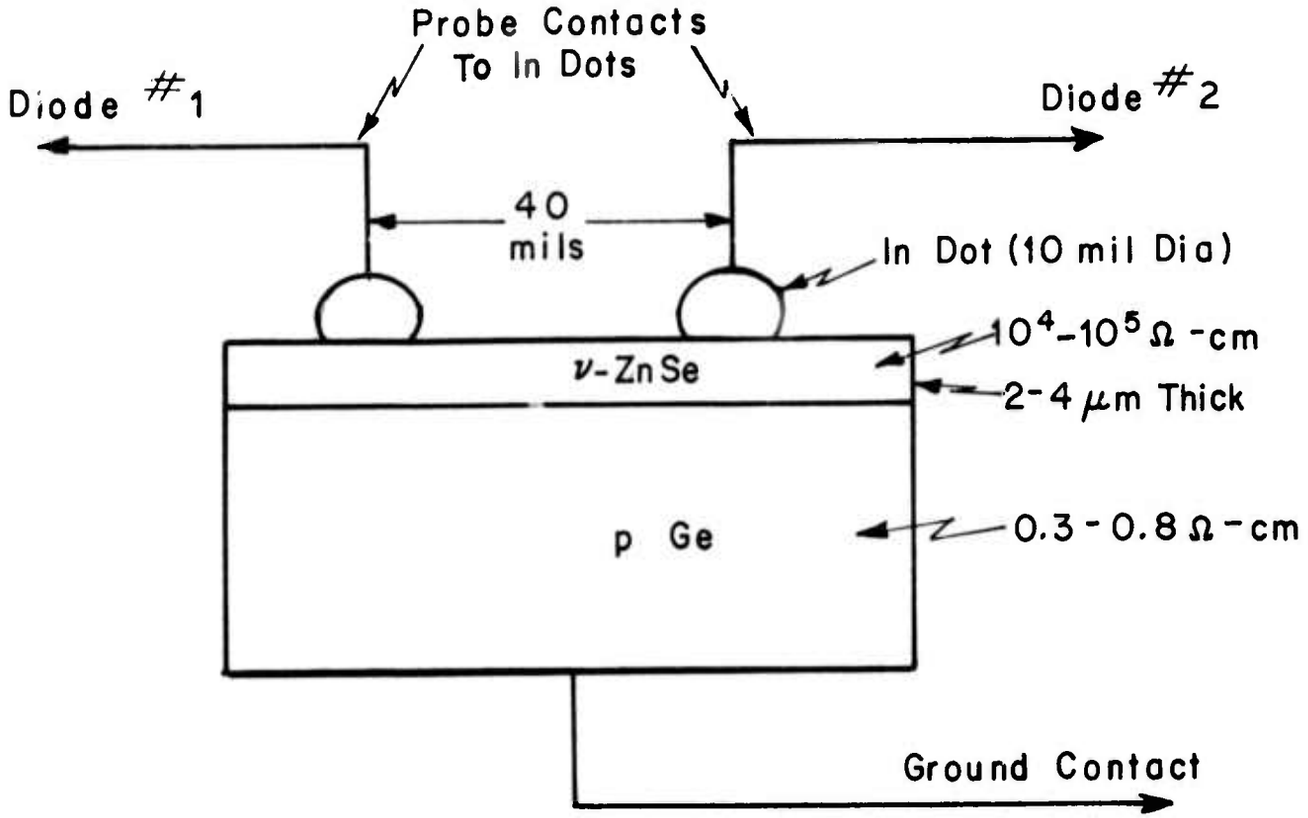


Fig. 31 Two diode system used to determine the area modulation effect in the presence of the biasing light of various wavelengths and intensities

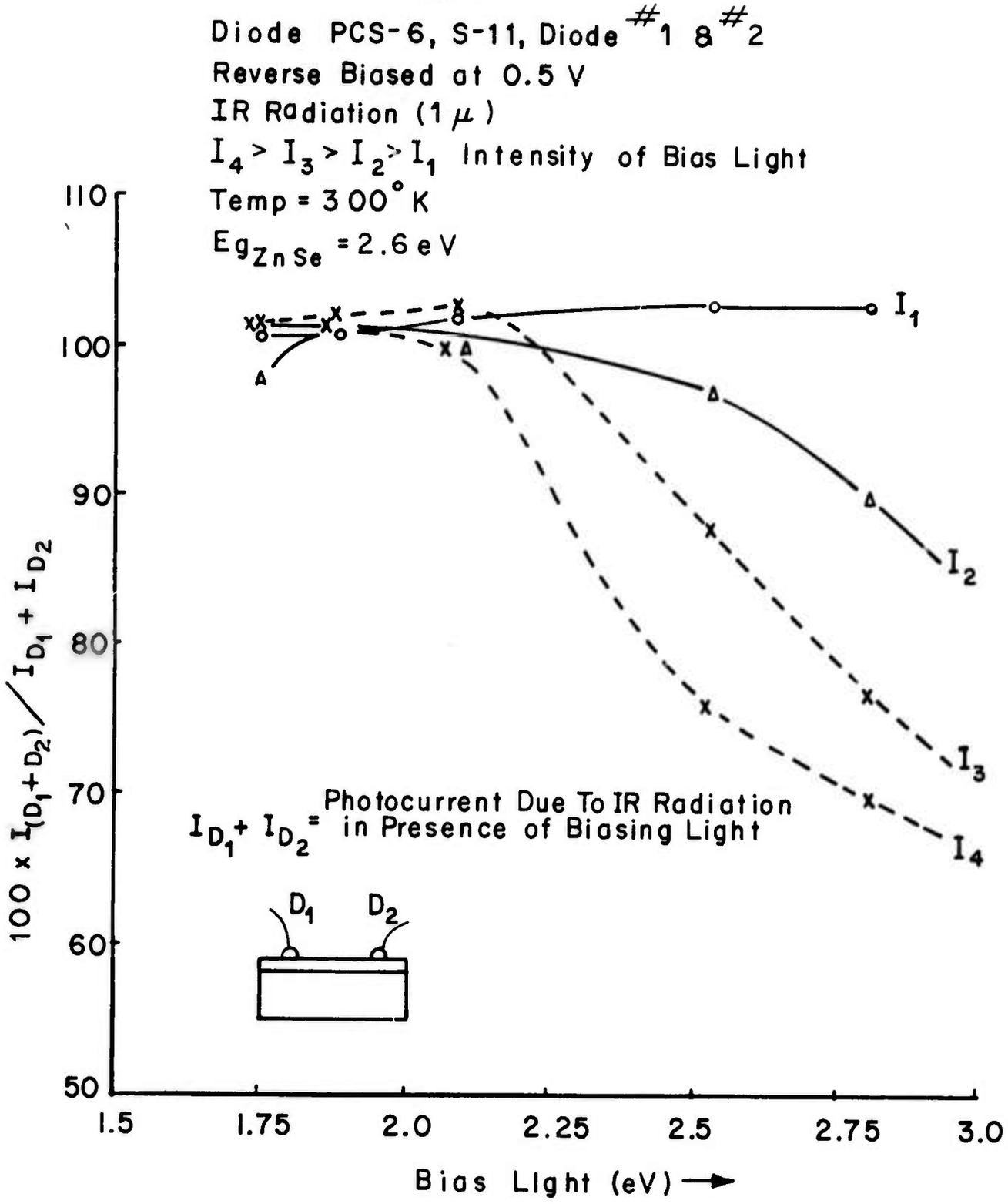


Fig. 32 Ratio of diode photocurrent when the diodes are connected in parallel to the sum of the individual diode photocurrents ($I_{(D_1 + D_2)} / I_{D_1} + I_{D_2}$) as a function of bias light energy for various bias light intensities

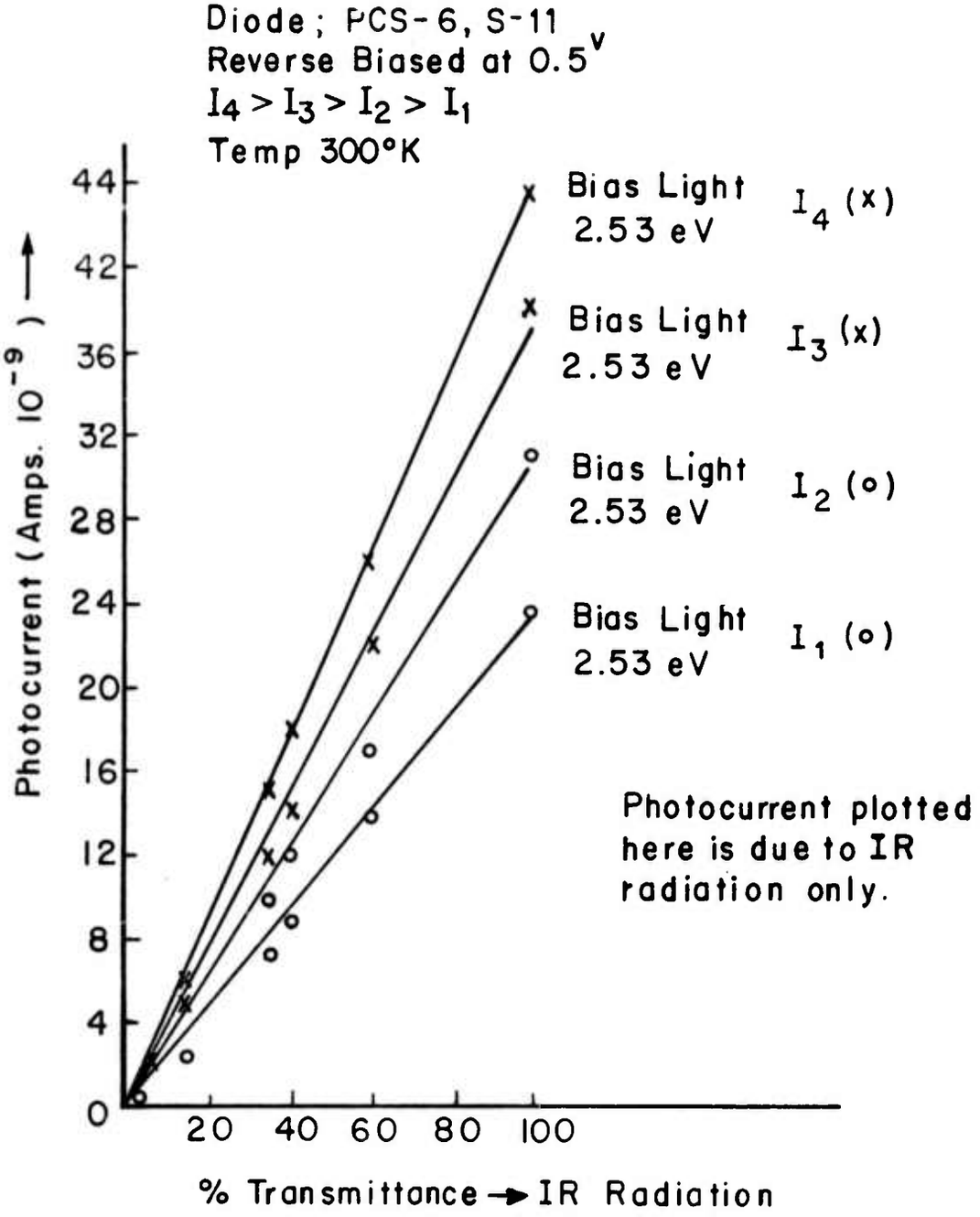


Fig. 33 Variation of photocurrent (or gain) with infrared radiation intensity for various bias light intensities, having a wavelength of 0.49 μm. PCS-6 S-11 is a Ge/ZnSe diode where the Ge is p type 0.3 ohm-cm and the ZnSe is a grown layer approximately 4 μm x 0.2 cm x 0.2 cm and the ZnSe side is provided with an indium contact of .025 cm diameter and the illumination is provided on this side.

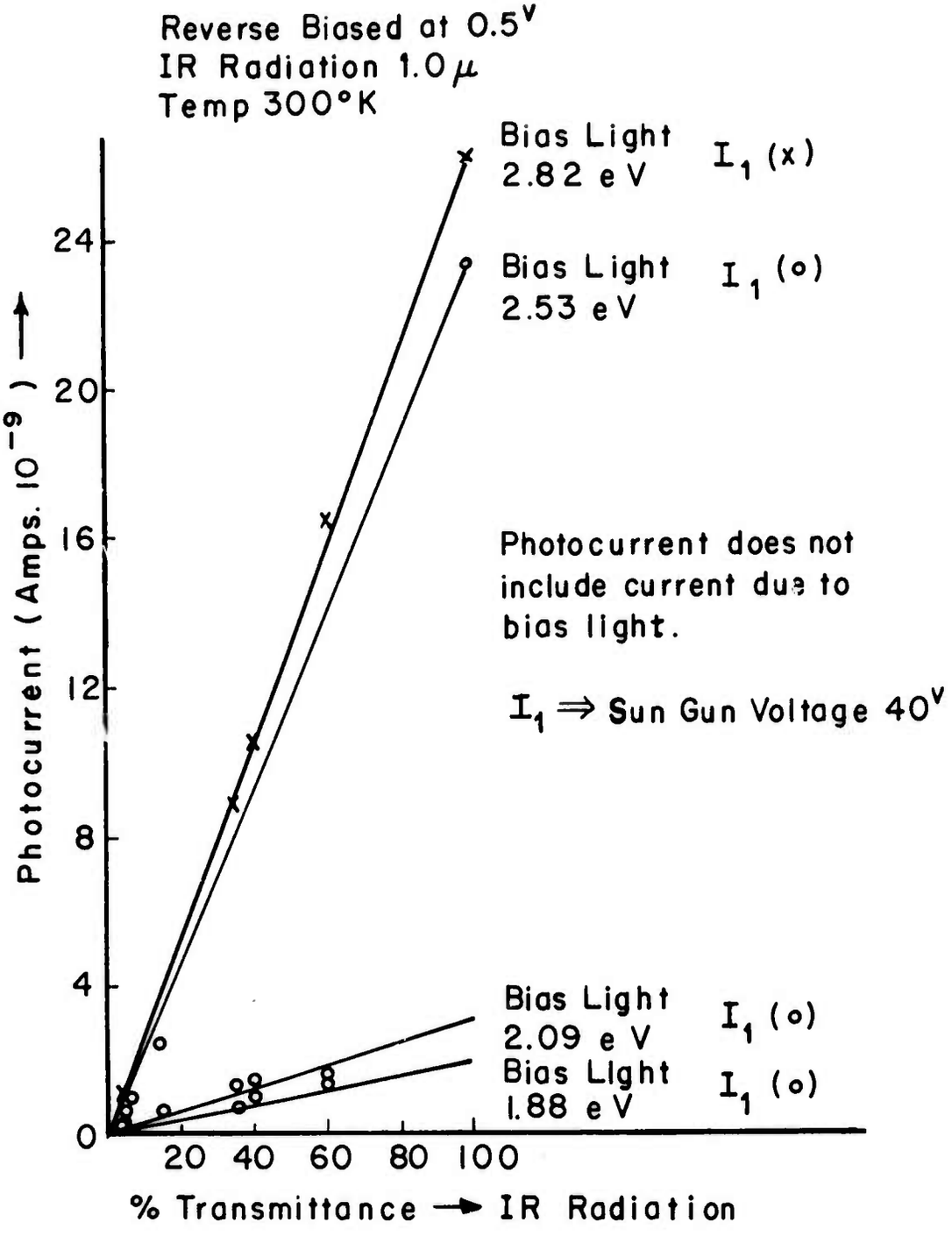


Fig. 34 Variation of photocurrent (or gain) with infrared radiation intensity for various bias light wavelengths keeping the intensity of the bias light constant.

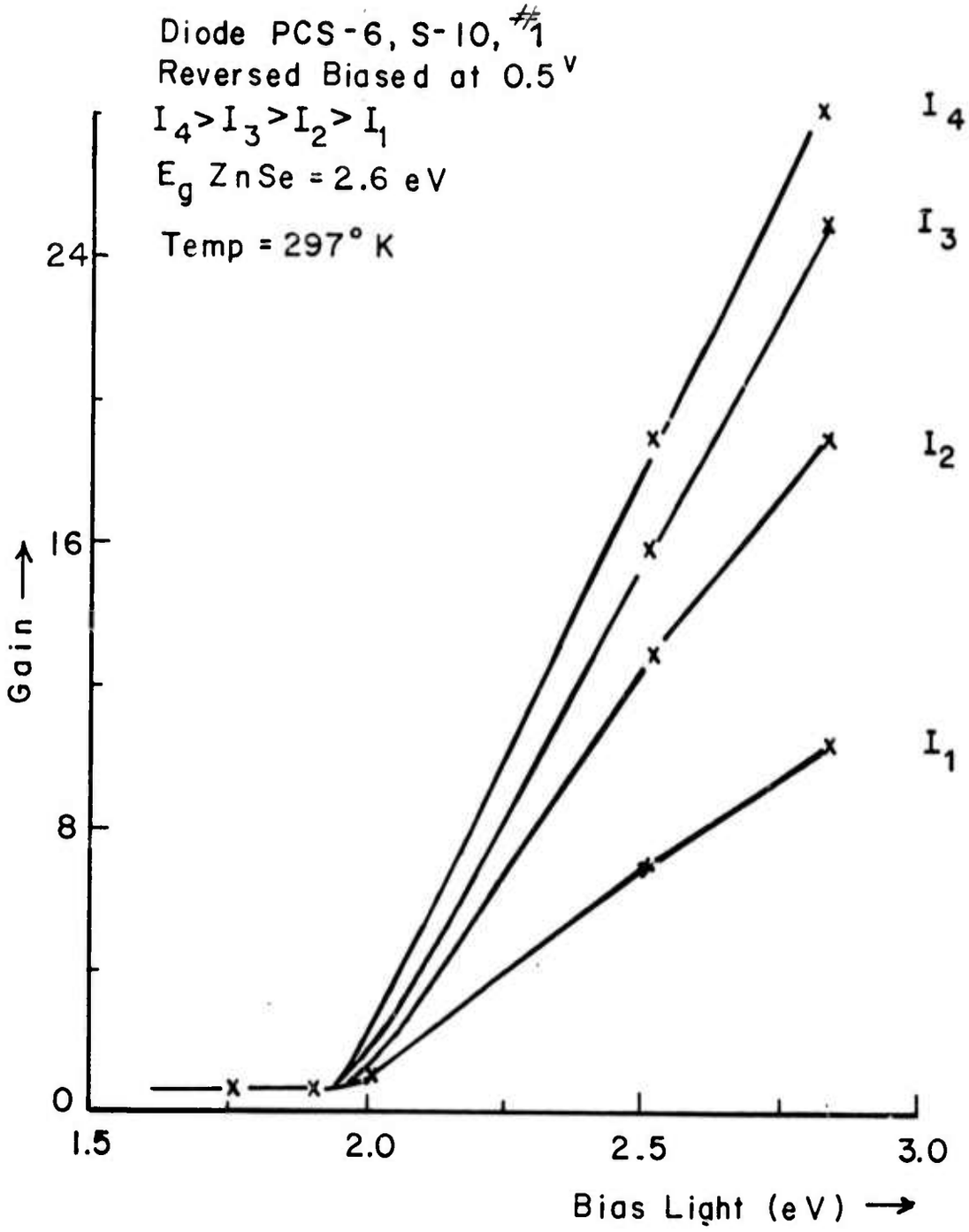


Fig.35 Variation of gain with bias light wavelength for various bias light intensities at room temperature.

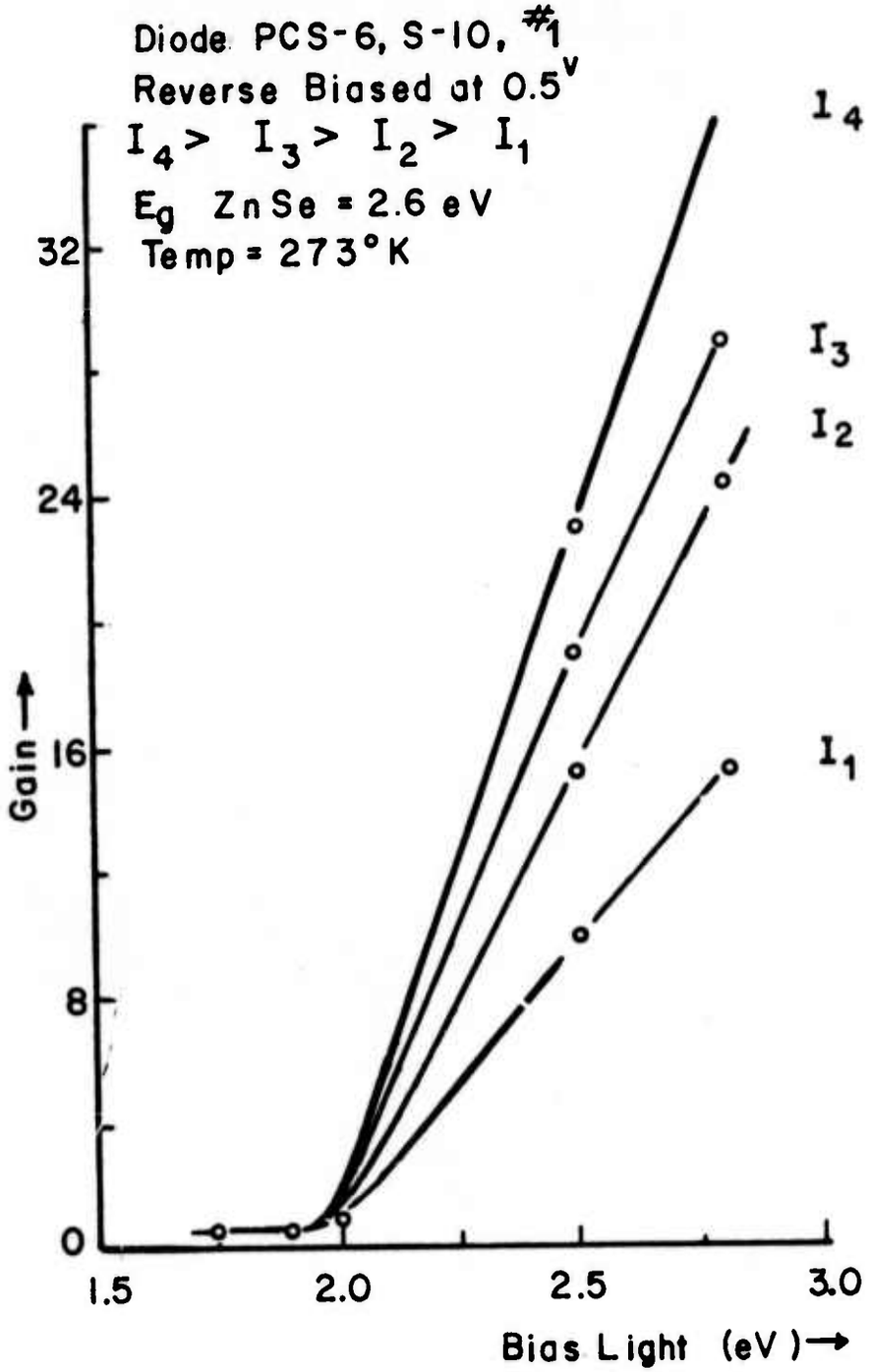


Fig. 36 Variation of gain with bias light wavelength for various bias light intensities below room temperature.

As one approach to this characterization, capacitance (at 1 MHz) versus voltage measurements were made with and without light at room temperature and below, see Fig. 37 and Fig. 38. The nature of the capacitance variation with voltage and with temperature was somewhat similar to effects seen in MOS type structures due to interface and bulk traps. It should be possible to model and extract information from such studies.

Some transient capacitance vs. time measurements and transient current vs. time measurements were also attempted to characterize the trap levels and their densities. But some instrumentation problems affected the results. If these could be solved, transient capacitance studies have the potential of providing further information about trap conditions.

To study the trap distribution at the interface of Ge and ZnSe the diodes from run PCS-6 have been studied at various temperatures. Fig. 39 shows the I-V characteristic of diode PCS-6, S-10, #1M. The log I vs. V curve is not a straight line, which therefore indicates that a normal exponential diode equation is not valid. When the data are plotted in a log I vs. log V scale, Fig. 40, some semblance of linearity occurs. In the low current region of the log I vs. log V plot at room temperature (below 10^{-7} Amp.) the plot has a slope of 4.5 indicating a high power law region. This is sometimes seen for space charge limited flow in the presence of a trap distribution. Above 10^{-7} Amp. the value of slope is 1.9 indicating a more usual space charge limited flow condition.

Study of such characteristics over a range of temperatures would be needed to establish more certainly the roles of space charge limited flow, tunneling and over-the-barrier injection in such diodes. However before this could be done we ran out of good PCS-6 material.

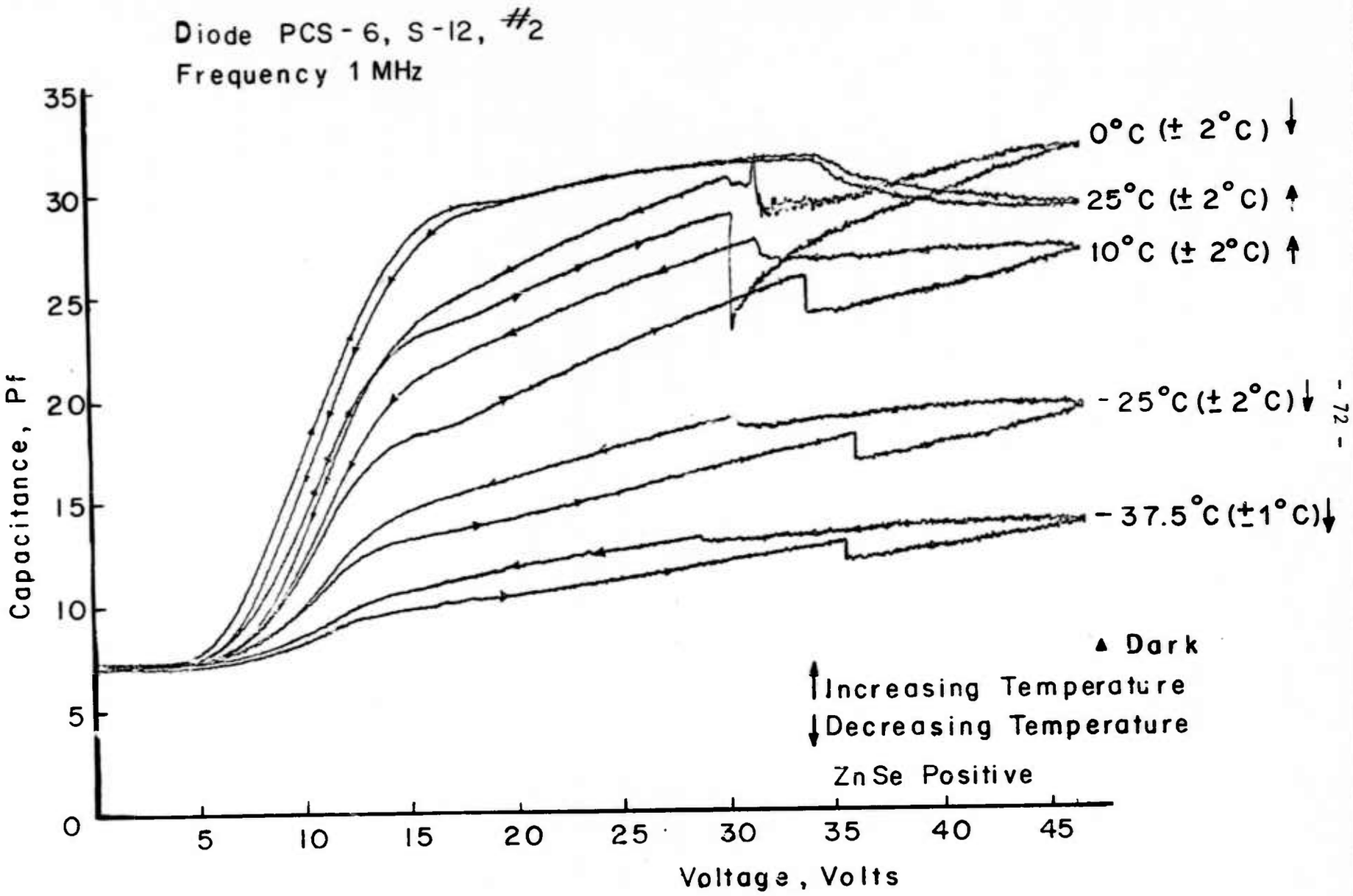


Fig. 37 C-V plots for vZnSe/P-Ge heterodiode at various temperatures in dark. Hysteresis is evident in all these plots.

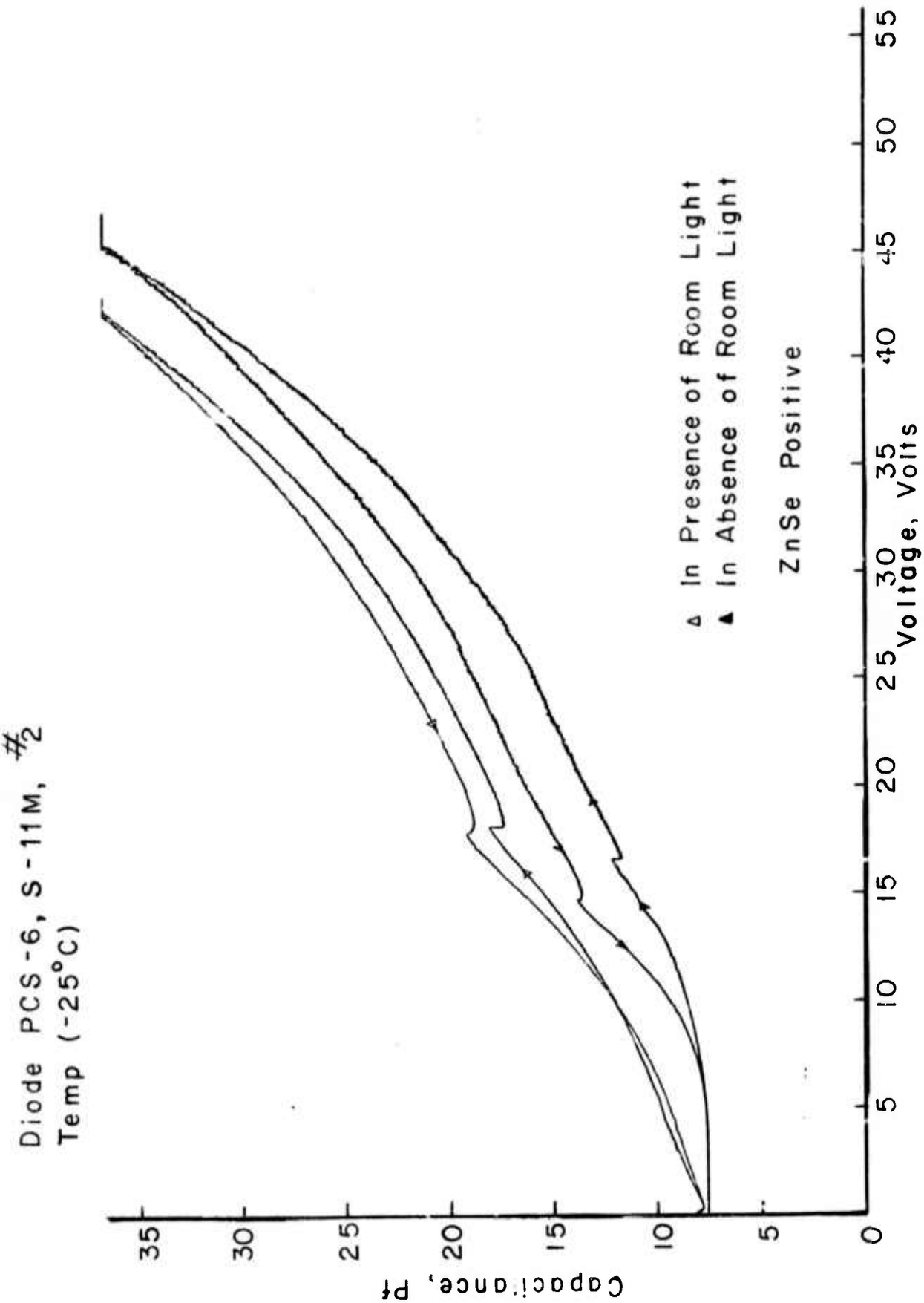


Fig. 38 C-V plots in the presence and absence of room light below room temperature.

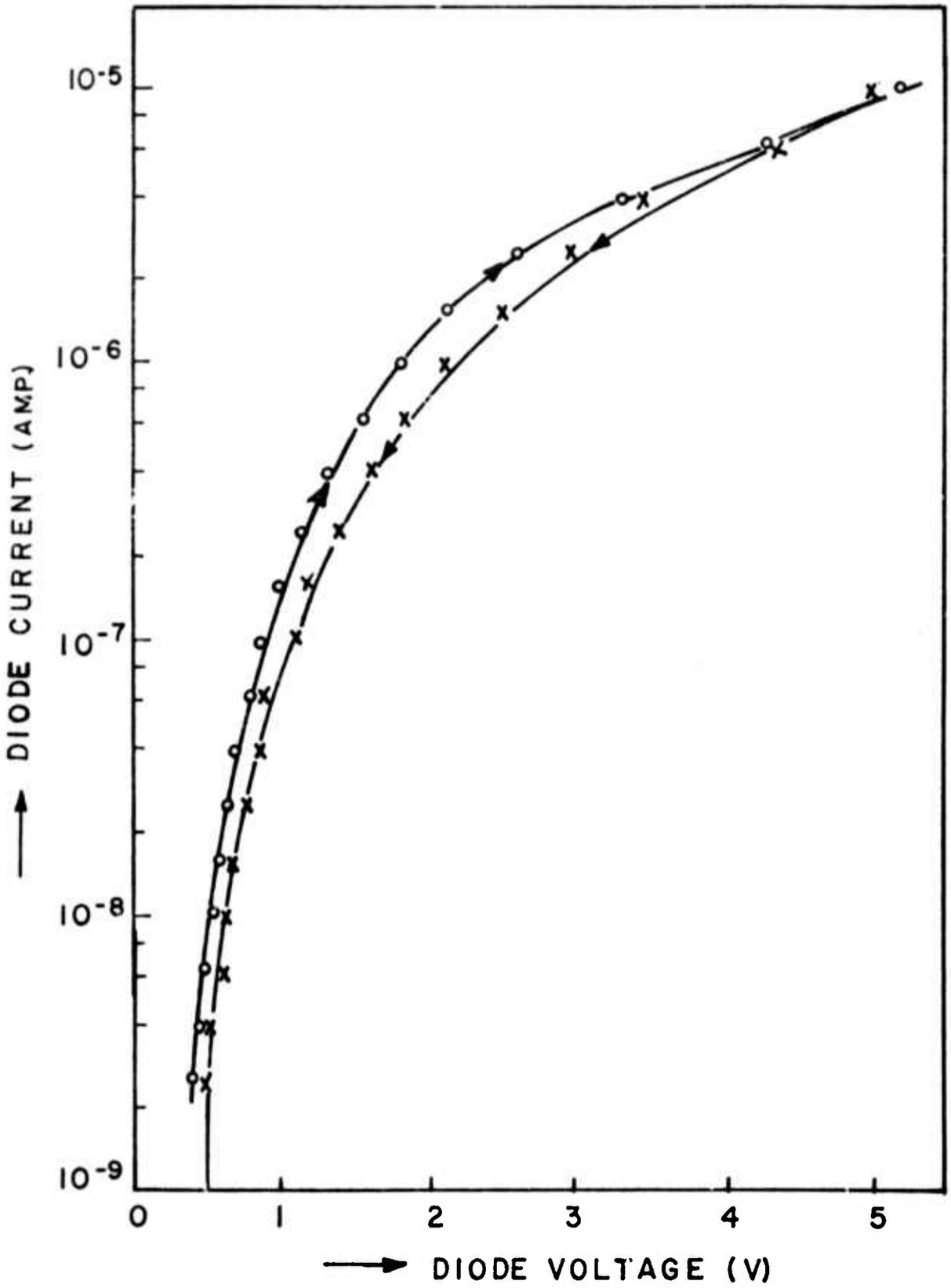


Fig. 39 Forward log I vs. V ZnSe/Ge Diode Characteristics. (PCS-6 S-1 M #1) at Room Temperature. o-While increasing current from '0' to max. X-While decreasing current max. to '0'.

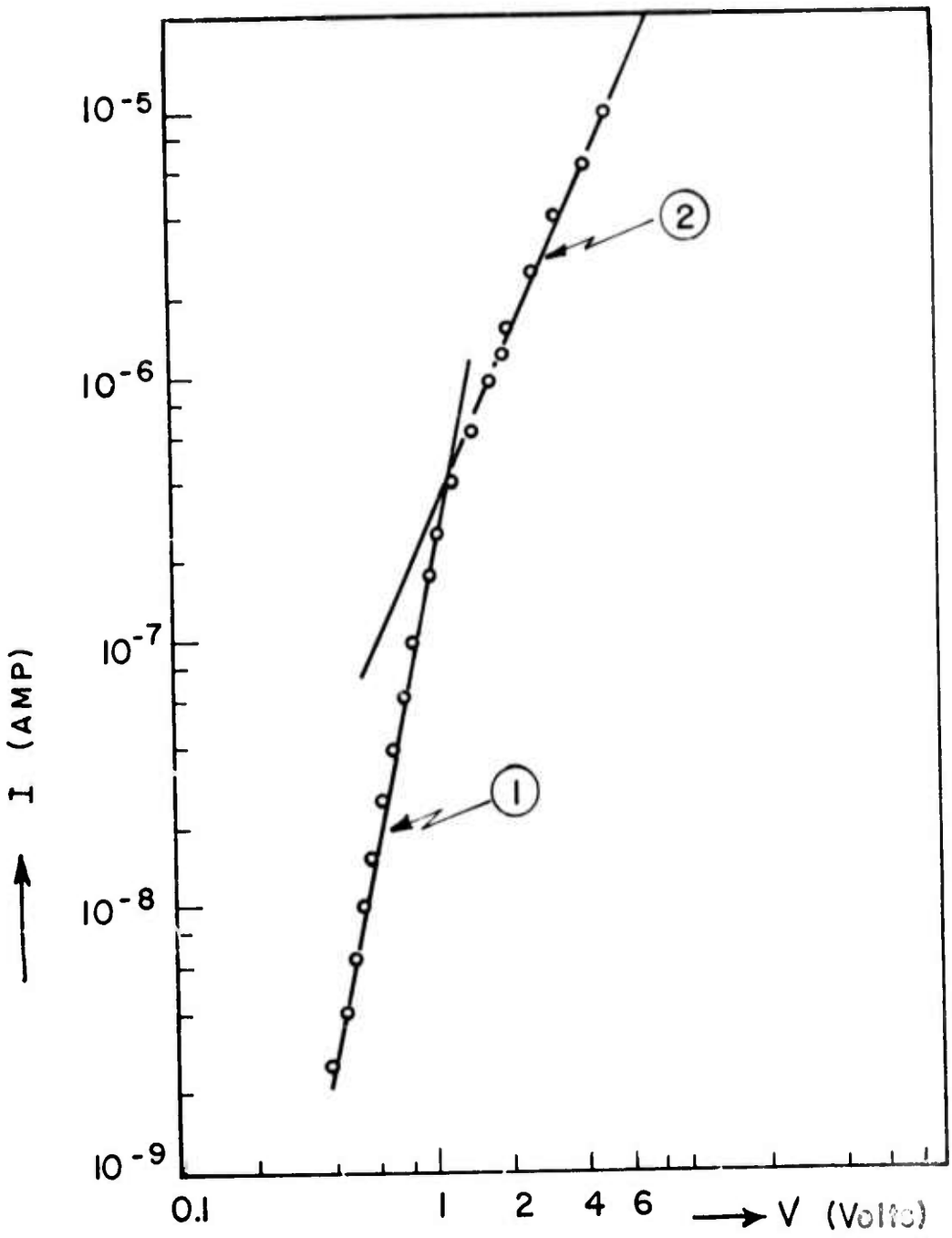


Fig. 40 Log I - Log V Characteristic Plot for ZnSe/Ge Diode PCS-6 S-1 M #1 at Room Temperature. Region (1) ($> 10^{-7}$ Amp) is of slope 4.5 and region (2) of slope 1.9.

5. Conclusions

The analysis of the proposed electron emitting structure pGe/νZnSe/p^+GaAs (Cs) suggests that the field-assisted photocathode concept is potentially capable of giving interesting emission efficiency for 1μm input infrared radiation of even longer wavelength radiation, approaching 1.7μm for the bandgap of Ge. However for a suitably low dark leakage current the device structure would have to operate at about 200°K by thermoelectric cooling or other means.

Practical realization of the structure has not been achieved within the time span of the contract. It has been found to be particularly difficult to achieve high grade interfaces by the growth of ZnSe on Ge substrates by the HCl close-spaced transport process explored. When good growth morphology was obtained it could not be repeated and the I-V characteristics of the pGe/νZnSe junctions made showed switching characteristics associated with traps. These trapping actions prevented electrons photo-induced in the Ge from crossing into the ZnSe with high transfer efficiency. There is no model available for this trapping although one might speculate that Ge is incorporated in the ZnSe layer. Extensive experimentation would have to be done to provide the solid evidence needed for model building. The one or two experiments that we had time to attempt in this respect either failed because the instrumentation was not adequate, or gave results that were too complex to interpret. (In parentheses we may note that several other experimenters have seen such switching actions but none has adequately explained them.)

HCl etching of the Ge during the early stages of growth appeared to be one factor that produced poor junction characteristics. This suggests that

in further studies attention should be given to possible evaporation or vapor deposition methods of achieving the desired structure. It is unlikely that another organization (University or Industry) will do much better with an HCl close-spaced epi-process than we did. Several ways that do not use HCl can be thought of for fabricating Ge/ZnSe junctions but in general they involve growing the Ge as a thin layer on ZnSe substrates rather than the otherway around. Although this is not very acceptable for the device structure under consideration, they might well be valuable for getting a better fundamental understanding of this interface.

Alternatively other sets of semiconductors should be examined, such as suggested by Kennedy[11], that do not involve the problems associated with II-VI compound semiconductor junctions.

6. Appendices

6.1 Appendix A: Fabrication of pGe/νZnSe Diodes

A stepwise procedure to fabricate pGe/νZnSe diodes is given here.

1. A sample is scribed using a diamond scriber. Most of the diodes fabricated were smaller than or equal to 100 x 50 mil. Since scribing is a form of cleaving, it minimized the leakage current along the edges.
2. The sample is thoroughly solvent cleaned to remove any debris left on the sample as a result of scribing. Fig. A-1 shows the sample.
3. Using bees wax or white wax (bees wax is found to be better) the sample is mounted on a lapping block with the ZnSe face down.
4. A metallurgical polishing wheel with 6μm diamond grit is used to remove the coating of SiO_2 and several mils of Ge. The starting

Ge seed thickness was of the order of 15 mils. Since the electron diffusion length in this Ge material was found to be of the order of 7-8 mils, it was desirable to remove 7-8 mils of Ge.

5. Final polishing is done again using a metallurgical polishing wheel employing 0.3μm and 0.05μm Al_2O_3 powder respectively. At this stage the Ge side is very shiny.

   In some instances step 4 used hand lapping with 3μm Alumina powder (with water) instead of 6μm diamond grit. Then step 5 was omitted and final polishing was done by etching with fresh white etch ($3HNO_3$: 1HF).

6. The sample is dismounted from the lapping block and boiled in acetone to remove the bees wax.
7. Using black wax the sample is mounted on a glass slide with the polished Ge facing down.
8. An island on the ZnSe is masked u ng black wax, as shown in Fig. A-2.
9. ZnSe from the unmasked regions is etched away using 5% Br_2 methanol.
10. The sample is thoroughly rinsed with methanol to remove any trace of the etchant.
11. The sample is washed with de-ionized water for 2-3 minutes.
12. A mesa is etched by etching the sample in ($3HNO_3$: 1 HF) white etch for 1 minute.
13. The etchant is gradually replaced with D.I. water.
14. The sample is dismounted from the glass-slide and boiled in trichloroethylene to remove black wax.
15. The sample is given a thorough solvent cleaning.
16. Using an alloy stage (with HCl gas as the flux in H_2) an In dot

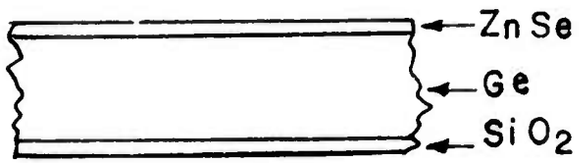


Fig. A-1 Diagram showing the starting sample of ZnSe on Ge

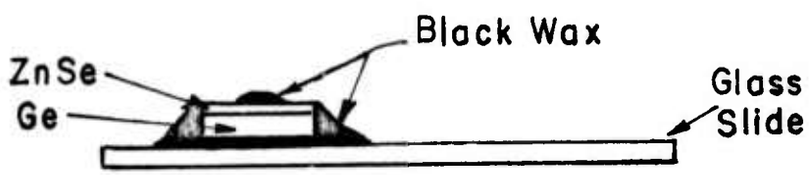


Fig. A-2 Schematic diagram showing the masking step

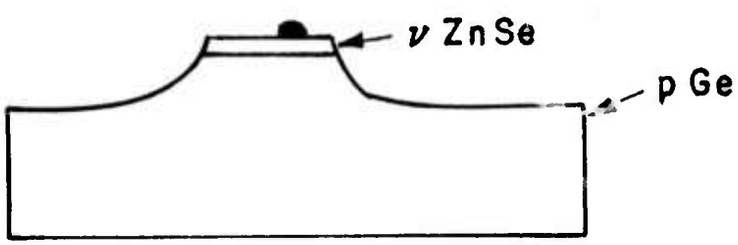


Fig. A-3 pGe/νZnSe mesa diode

is alloyed to the ZnSe layer at 250-300°C for 1 minute; as shown in Fig. A-3.

The diodes fabricated thus have shown good reverse characteristics with leakage currents of the order of nanoamps or sub-nanoamp. Such a diode should be kept in a dry box to prevent increase of the leakage current with humidity.

6.2 Appendix B: Calculation of Quantum Yield

Let P be the photons per cm^2 per sec striking the surface of the Ge on the far side from the junction. The absorption coefficient for the Ge is about $10^4 cm^{-1}$ for a photon energy of 1 eV and the reflection loss is about 40%. Therefore we can assume that the absorbed photon flux is 0.6 P and that this is all absorbed within a distance of a few microns from the Ge surface. Let $n_s cm^{-3}$ be the density of electrons induced as hole-electron pairs near this surface by the absorbed photon flux and assume that there is negligible surface recombination loss to simplify the problem. Then electrons diffuse into the bulk of the Ge recombining as they move down the diffusion gradient such that the density at a distance x from the surface is given by

$$n(x) = n_s \exp(-x/L_n)$$

where L_n is the diffusion length ($\sqrt{D_n \tau_n}$) for the electron.

The flux of electrons at the position x, i.e. the number of electrons crossing per cm^2 per sec. is given by

$$F_n(x) = -D_p \frac{dn}{dx} = \frac{D_p}{L_n} \left(n_s \exp(-x/L_n) \right) = F_n(s) \exp(-x/L_n)$$

If Q is the quantum efficiency (%) collection at the junction and I_p is the photocurrent measured and x_j is the junction depth, and A the junction area

(assumed to be the area of the indium contact on the ZnSe), then

$$\frac{I_p}{eA} = \frac{QF_n(x_j)}{100}$$

where e is the charge on an electron.

Hence

$$\frac{I_p}{eA} = \frac{Q\,F_n(s)\,\exp\,(-x_j/L_n)}{100}$$

and from $F_n(s) = 0.6P$

we have

$$Q = \frac{100\,I_p\,\exp\,(x_j/L_n)}{eA\;0.6\;P} \qquad \%$$

The photon flux P was determined from the output of a previously calibrated silicon duo-diode photo detector (type 1N2175, at 10 V reverse bias). The calibration was made with the use of an instrument for measuring the energy in a 1.06μm laser beam. The result of the calibration checked out in good agreement with the collector efficiency expected for a silicon junction photodetector. In a typical measurement (specimen PCS-6, S 8, x_j = 14.4×10^{-3} inches, $L_n = 7 \times 10^{-3}$ inches, area = 2.09×10^{-4} cm^2), the photon flux, P, was 2.99×10^{16} photons per cm^2 per sec. At -15°C and in the presence of room light, the photo-induced current was 1.7×10^{-8}A - 1.5×10^{-10}A. Hence from eq. (5) we have

$$Q = \frac{100 \times 1.689 \times 10^{-8}\ \exp\ (14.4/7)}{1.6 \times 10^{-19} \times 2.09 \times 10^{-4} \times 0.6 \times 2.99 \times 10^{16}} = 21.7\%$$

The area taken in this example was that of the indium contact to the ZnSe rather than the full area of the ZnSe since from previous studies it appeared that the ZnSe is high enough in resistance to restrict considerably any lateral collection. The extent to which the room light background illumination

tends to lift this restriction is illustrated in Fig. 32 and discussed in the associated text.

6.3 Appendix C: Auger Spectroscopy of Ge Surfaces

Auger electron spectroscopy has recently emerged as a sensitive method of surface analysis. J.M. Chen[12] and J.J. Grant et. al.[13] have used Auger spectroscopy successfully to study silicon surfaces. C.C. Chang[14] has used this method to study the contaminants on chemically etched silicon surfaces. Successful use of Auger spectroscopy in studying silicon surfaces motivated us to use this tool to investigate the contaminants on Ge surfaces. The need to obtain atomically clean Ge surfaces became apparent from our attempts to get reproducible and good epitaxial layers of ZnSe on Ge substrates. It was decided to use Auger spectroscopy to look at the effect of various cleaning, chemical etching and storing processes on the final cleanliness of the Ge seeds.

6.3.1 Effect of storing media

The storing medium just prior to loading the substrate into the growth system plays an extremely important role in determining the final substrate cleanliness. However meticulously the sample may have been prepared if it is not properly stored the substrate surface may become contaminated resulting in the growth of a poor layer on it. Table C-2 describes the effects of storing Ge substrate in various media and Table C-1 lists the sample preparation and experimental conditions for the Auger spectrographs in Figs. C-1 to C-4; and shows that all storing medium, commonly employed in the laboratory, result in carbon and oxygen contamination. Clean, dry air is perhaps the best choice because it results in minimum 'C' contamination. As shown later the 'O' can be removed by moderate

Table C-1 Sample preparation techniques and Auger analysis results for several Ge samples.

Figure	Sample #	Sample Preparation	Results
C-1	G-13-Ge-I	Stored in Auger spectrometer at 10^{-9} torr and sputter cleaned using argon ion bombardments; then stored in air for 2 hrs. and loaded back into the Auger spectrometer.	1. Trace 'A' shows the presence of 'O' and 'C' peaks. 2. Mild sputtering at 5mA for 3.5 min. removed all 'C' and 'O' contamination as shown by trace B.
C-2	G-14-Ge-II	Stored in Auger spectrometer at 10^{-9} torr and sputter cleaned using argon ion bombardment, then stored in D.I. water for 1/2 hr. and loaded back into the Auger spectrometer.	1. Trace 'A' shows the presence of 'O' and 'C' peaks. 2. Mild sputtering at 5mA for 3.5 min. removed all 'C' and 'O' contamination as shown by trace B.
C-3	G-26-Ge-II	Sample was sputter cleaned and stored in Auger spectrometer in 10^{-9} torr vacuum for several days.	1. Trace 'A' shows the return of 'C' and 'O' peaks due to storage in the Auger spectrometer. 2. Trace 'B' shows the effect of heating at 20 watts for 2 min. Note 'O' peak has nearly vanished while 'C' is unaffected. Circled 'D' peak has vanished after heating showing removal of hydrocarbons due to heating.
C-4	G-15-Ge-III	Diamond scribed from Ge slice prepolished by the manufacturer; solvent cleaned and stored in methanol (reagent grade) for 1 hr. before loading into the Auger spectrometer.	1. Trace 'A' shows the presence of 'C' and 'O' peaks. 2. Mild sputtering at 5mA for 3.5 min. removed all 'C' and 'O' contamination as shown by trace B.

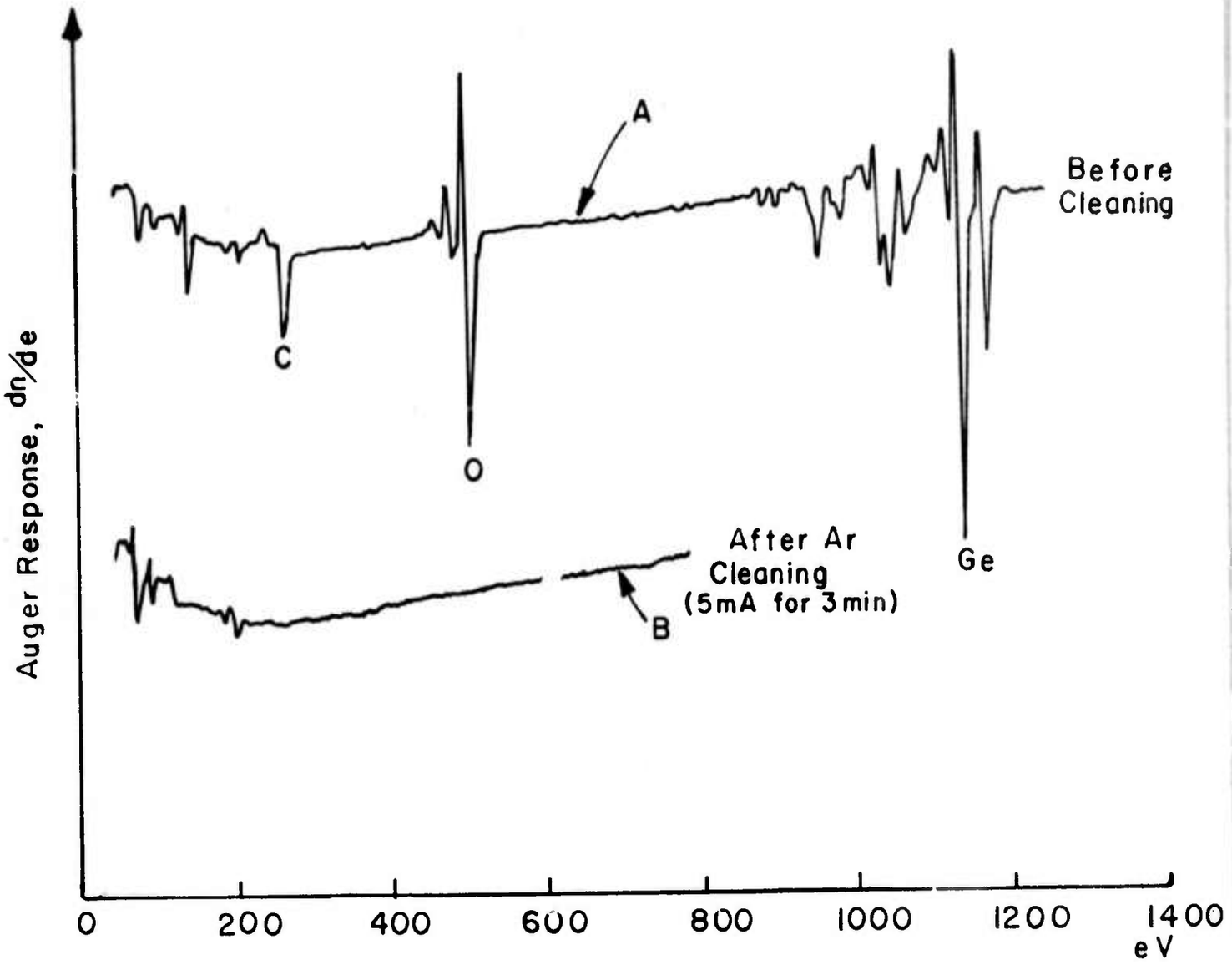


Fig. C-1 Auger spectra for specimen G13-GeI (air)

E_p = 3000V; I_p = 50μA; V_{mod} = 6; V_{mult} = 500; Sens. 0.5

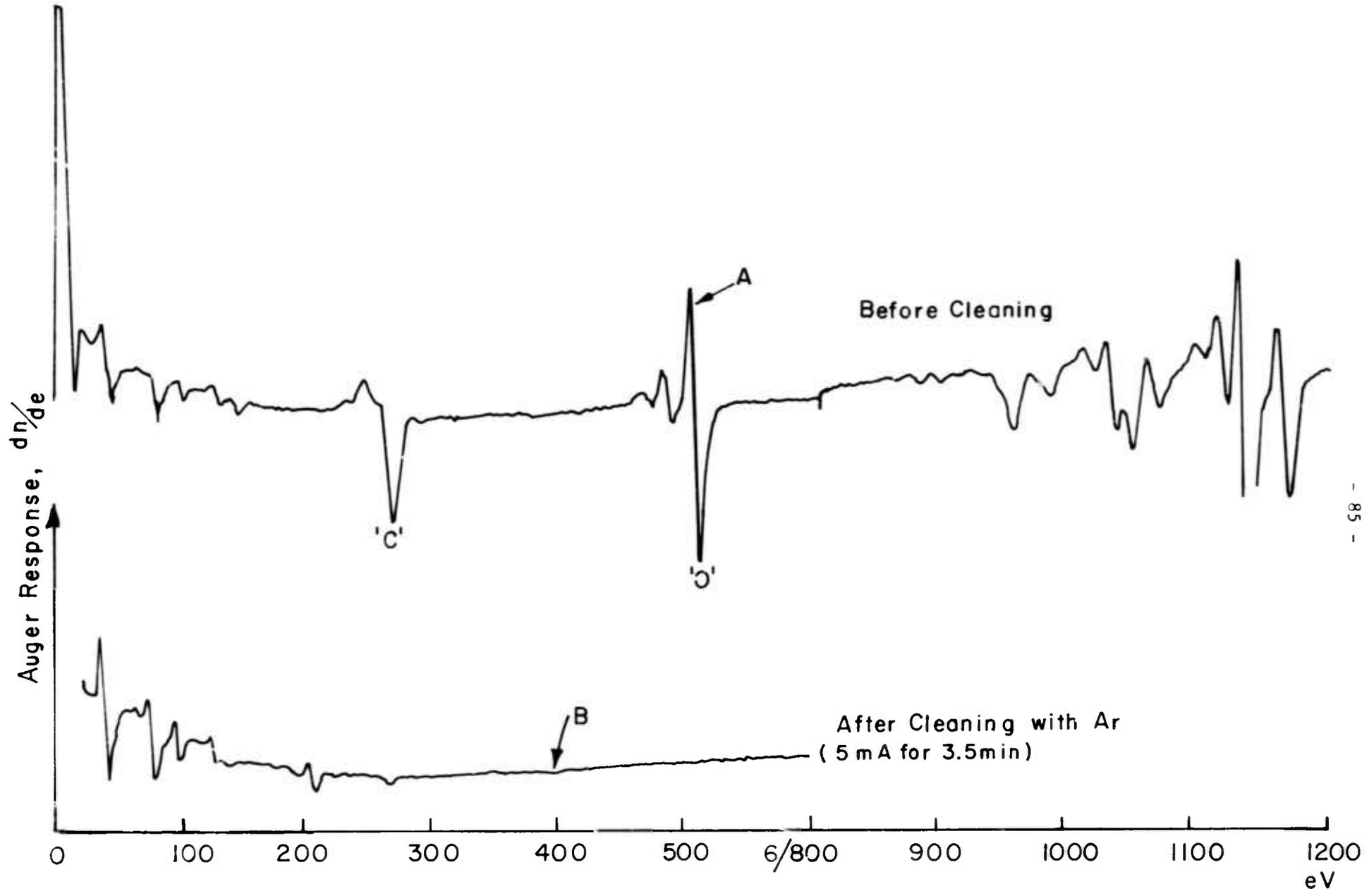


Fig. C-2 Auger spectra for specimen G14-GeII (water). E_p = 3000V; I_p = 50μA; V_{mod} = 6; V_{mult} = 500; sens 0.5

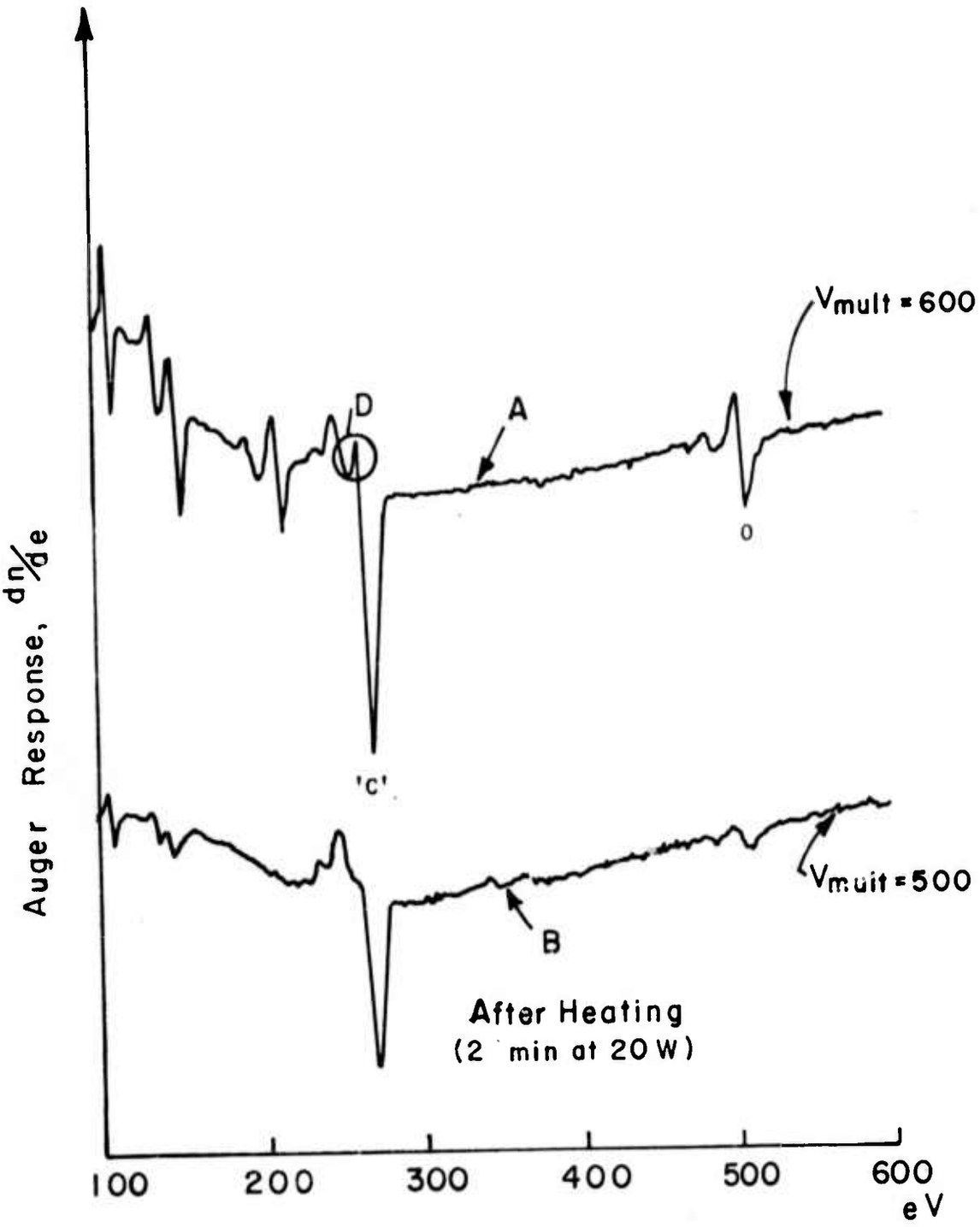


Fig. C-3 Auger spectra for specimen G-26-GeII

E_p = 3000V; I_p = 50μA; V_{mod} = 6; V_{mult} as labeled.

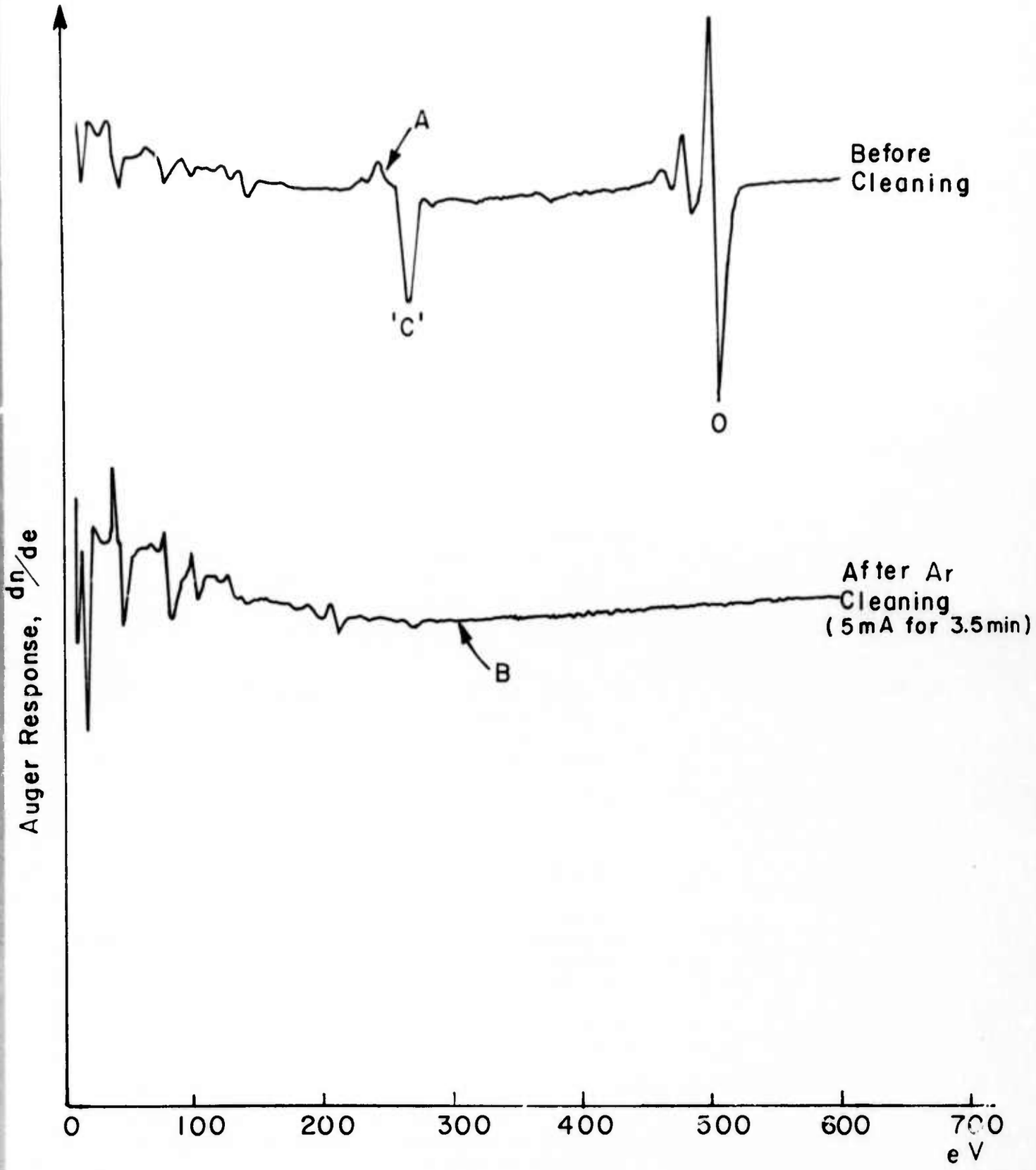


Fig. C-4 Auger spectra for specimen G- 15-GeIII

E_p =5000V; I_p = 50μA; V_{mod} = 6; V_{mult} = 500; Sens. 0.5

Table C-2 Auger analysis results for Ge samples stores in various media

Storing medium	Cleanliness Analysis*
AIR	Fig. C-1 shows that just storing in room air can result in 'C' and 'O' contamination of the surface. 'O' can be in the bound form as oxide or in an absorbed water-vapor form. Comparing Figs. C-1 to C-4 it is evident that 'C' contamination is minimum if Ge is stored in air. This 'C' could be further minimized by storing in "clean" dry air. The 'C' and 'O' found on the surface from storage in air are easily removed by a very mild sputtering.
WATER	Fig. C-2 shows the Auger analysis of a Ge surface stored in D.I. water. This results in moderate contamination 'C' and 'O'. By carefully looking at the 'C' peak it is evident that the hydrocarbon peak (see Fig. C-3,) is absent which indicates that the 'C' contamination is most probably in the element form. Heating experiments show that 'C' is not in gaseous bound form.
METHANOL	From Fig. C-4 it seems that methanol is the worst storing medium, it results in a fair amount of 'C' contamination while 'O' contamination is maximum. The hydrocarbon peak is absent here also.
ULTRA HIGH VACUUM OF AUGER SPECTRO-METER	Ge substrates, after sputter cleaning using argon ion bombardment and storage in the Auger spectrometer showed minimum 'O' and maximum 'C' contamination (as expected). Note the presence of the hydrocarbon peak which vanishes upon electron beam heating of the surface. The 'C' peak left is puzzling. It is not obvious where this 'C' is coming from. It could be coming either from bulk or decomposition of organic vapor by the electron beam.

*Fig. C-1 to C-4 all have same measurement conditions. Hence height of various peaks can be compared to get relative contaminations due to different storing medium.

heating. Some further study is underway to characterize the carbon contamination, its source and the ways to get rid of it.

6.3.2 Effect of final etching step

Evidence, collected in attempts to grow the best quality ZnSe epitaxial layers on Ge, indicates that extreme caution is required to prepare the surface of the Ge seed. The usual final processing step is chemical etching. The chemical etches chosen may well determine the contaminants found and their concentrations. Two commonly used etches for final surface treatment to Ge are:

1. Hypochlorite etch (3: ; H_2O: 5% NaOCl)
2. Modified superoxol ($4H_2O$; 1HF: $1H_2O_2$: $20H_2SO_4$) used while hot.

Fig. C-6 and C-5 are the Auger curves for the Ge surfaces treated with hypochlorite etch and superoxol (modified) respectively. There is not much difference between a surface treated with modified superoxol or hypochlorite etch.

6.3.3 Effect of heating and sputtering on the removal of contaminants (G-11 and G-26)

Some other experiments were done to study heating effects on these various samples. One such experimental analysis by the Auger spectrometer is presented in Fig. C-7. Sample G-11-GeII had 'C' and 'O' contamination as a result of the storing medium. Various heating cycles up to the melting point (80 watts, 1 min.) of Ge were tried. The 'O' contamination was completely eliminated while the 'C' contamination, except for the hydrocarbon peak disappearance, remained the same. Hence heating connot be used to remove 'C'. From the experiments done to study Ge surfaces its fairly clear that sputtering is the only way to get rid of 'C' contamination. The extent to which an etched Ge surface is contaminated by 'C', however, is not clear for the Auger spectrometer is itself a source

Table C-3 Auger analysis results for Ge samples with different final etching steps.

Figure	Sample #	Ge Sample Preparation	Results
C-5	G-36-Ge-VIII	Diamond scribed solvent cleaned, treated with freshly made superoxyl for 2 min., rinsed with D.I. water, dry N_2 dried, and immediately stored in the Auger spectrometer.	Little 'C' and 'O' contamination. Slight trace (insignificant) of 'S' visible. Light sputtering removes all these traces.
C-6	G-34-Ge-VII	Diamond scribed solvent cleaned, etched in hypochlorite etch for 2 min., rinsed with D.I.water, blown dry with dry, oil free N_2 and immediately stored in the Auger spectrometer.	Minimum 'O' contamination. Slight 'C' contamination. Slight 'S' trace visible. Light sputtering removes all these traces.

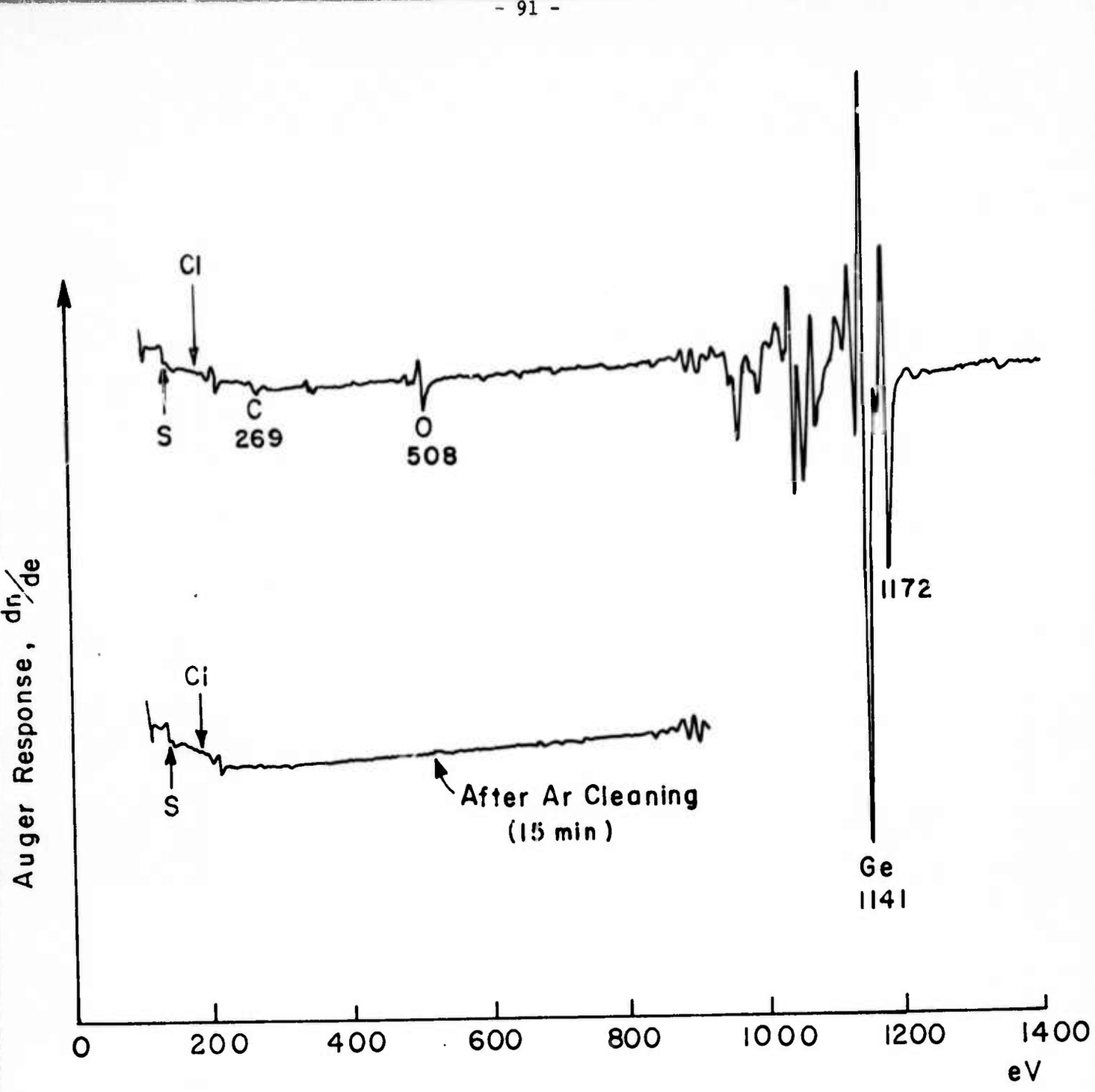


Fig. C-5 Auger spectra for specimen G-36-GeVIII

E_p = 5000V; I_p = 50μA; V_{mod} = 4; V_{mult} = 550; Sens. 0.5

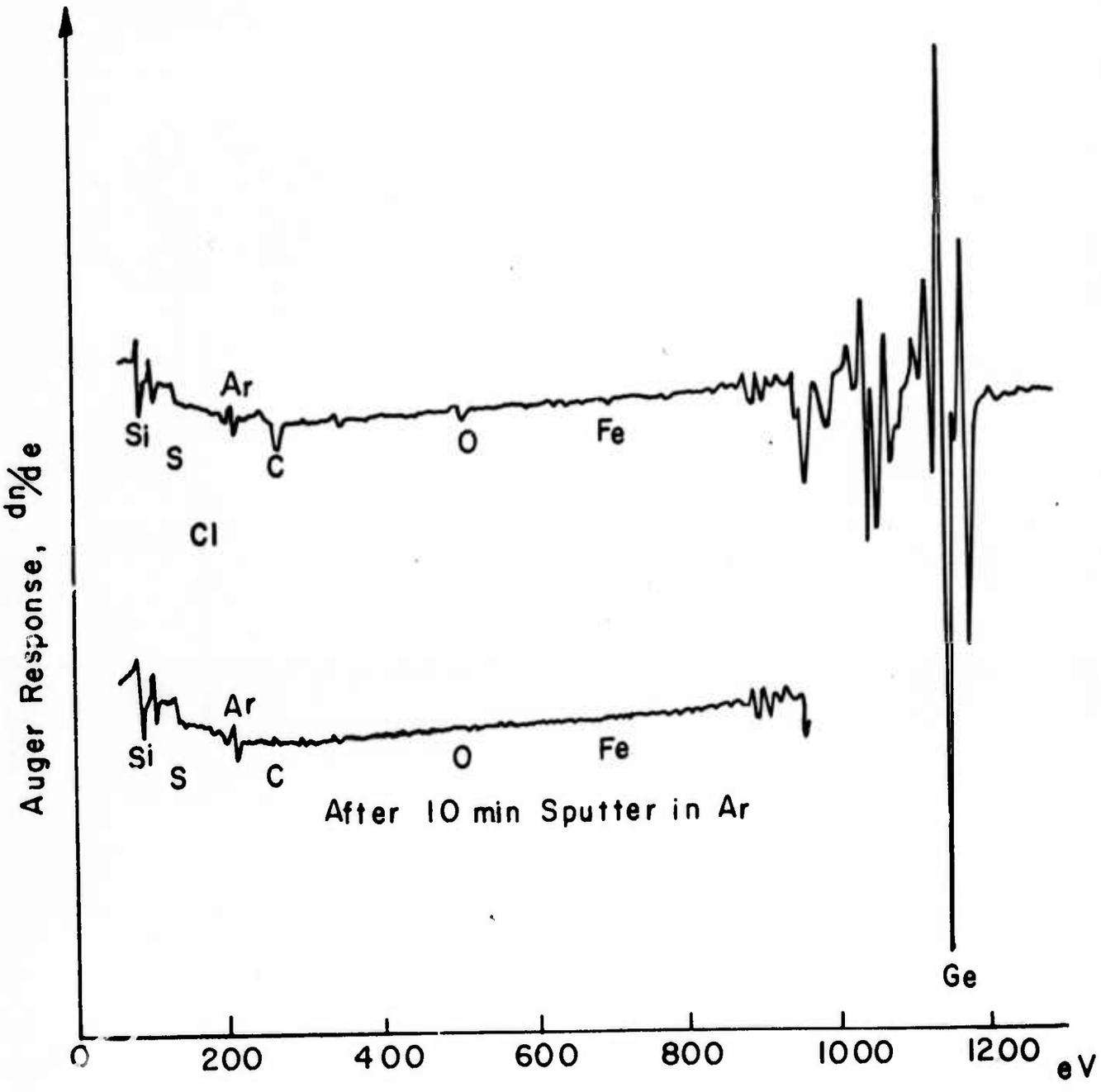


Fig. C-6 Auger spectra for specimen G-34-GeVII

E_p = 5000V; I_p = 50μA; V_{mod} = 4; V_{mult} = 550, Sens. 0.5

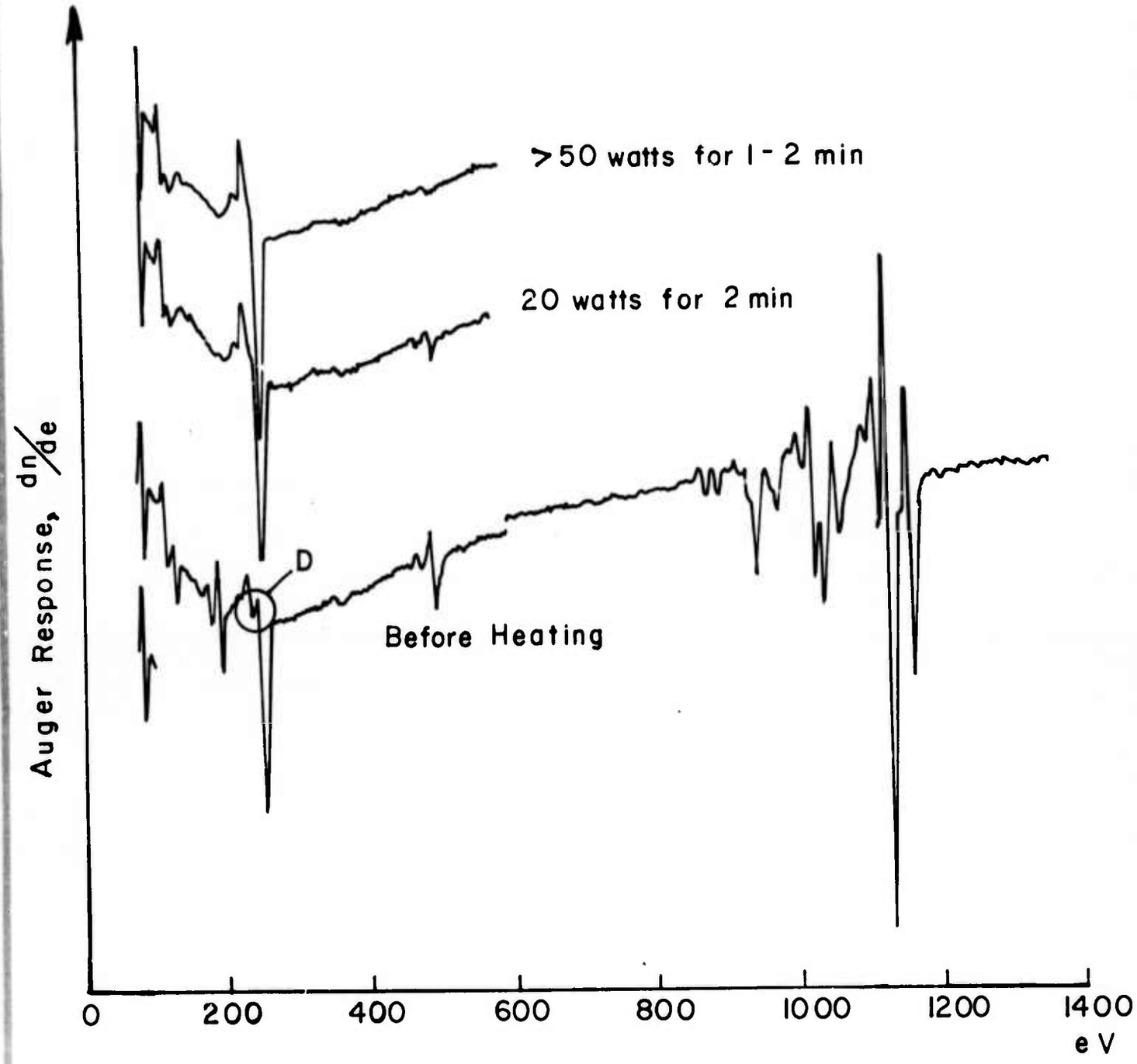


Fig. C-7 Auger spectra for specimen G-11-GeII

E_p = 3000V; I_p = 50; V_{mod} = 6 for <600eV, = 4 for >600eV; V_{mult} = 575, 540; Sens = 0.5

of 'C' contamination. Thus one cannot be sure how much of the 'C' observed is due to the sample preparation or the Auger spectrometer itself.

The question of 'C' contamination is further clouded by the Auger spectrometer analysis of a Ge surface coated with SiO_2 as shown in Fig. C-8. The SiO_2 was deposited using a Silane system. It is interesting that there is no 'C' contamination observed even though the SiO_2 surface was exposed to D.I. water, air and the Auger vacuum. Possibly the adhesion of the 'C' to SiO_2 is low.

6.4 Appendix D: Preparation of Ge seed and ZnSe source

6.4.1 Preparation of the Ge seed material

In order to obtain suitable epitaxy and low imperfection densities in epitaxial layers it is important that substrates be prepared with a flat, defect-free clean surface. This is usually accomplished by a combination of mechanical lapping and chemical polishing. A step by step procedure is outlined below for the preparation of a Ge substrate starting from a wafer sliced from an ingot.

1. The wafer is scribed into seed sizes using a diamond scriber. Since scribing is a form of cleaving, it minimizes edge effects by providing atomically clean and flat edges (assuming that cleavage plane is perpendicular to the seed surface, growth plane). This makes the (100) very attractive for cleaving. Fig. D-1 shows this scribing operation pictorially.
2. The scribed Ge seed, shown in Fig. D-1 (d) is rinsed with dionized water to remove all remaining debris sticking to the seed after scribing.
3. The seed is mounted on a lapping block as shown in Fig. D-2 (a)

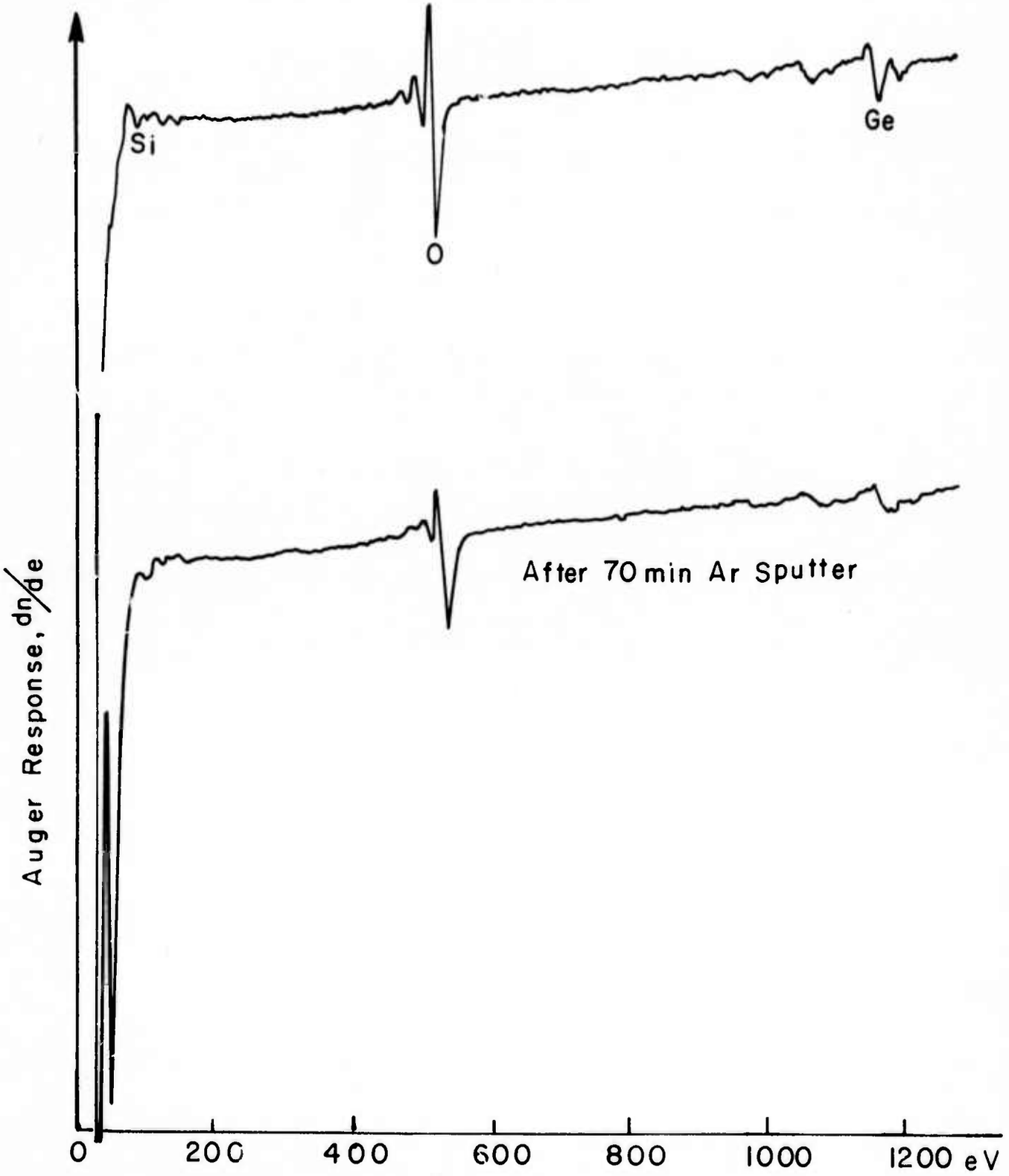
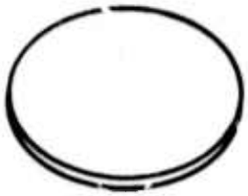
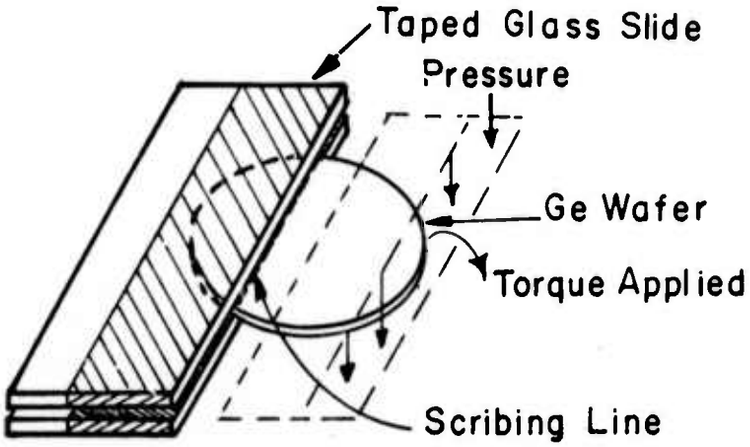


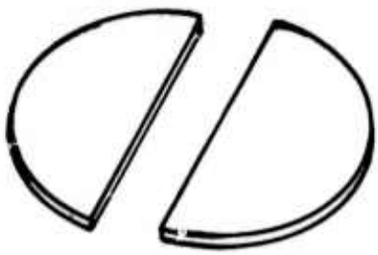
Fig. C-8 Auger spectra for specimen G-29-GeV (SiO_2 coated)
E_p = 2000V; I_p = 50μA; V_{mod} = 4; V_{mult} = 550; sens 0.5



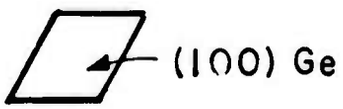
(a) Starting wafer.



(b) Wafer ready to be scribed.



(c) Wafer broken along the scribed line using a third taped glass slide and pressing it along the scribed line as shown in Fig. (b).

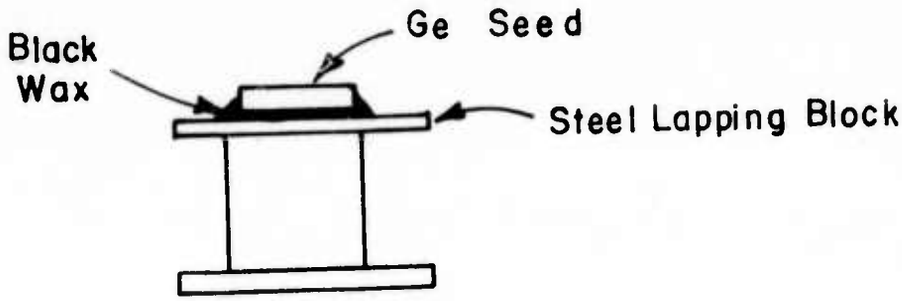


(d) Scribed Ge seed.

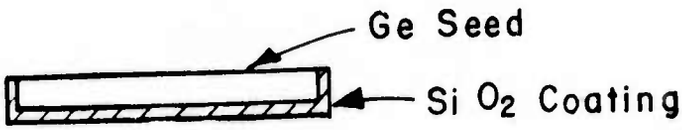
Fig. D-1 Ge substrate scribing.

and hand lapped on a glass plate using 3μm Al_2O_3 grit.
Several mils of material are removed (preferably 3-5 mils)
to remove any saw damage.

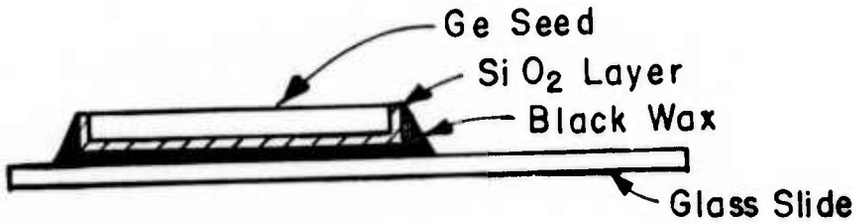
4. The seed is inverted and step '3' repeated.
5. The seed is similarly lapped with 1μm grit on both sides
to remove ≃ 20μm from each side.
Separate lapping plate must be used for lapping powders of different sizes. Seed and lapping accessories are thoroughly washed with D.I. water after each lapping step. This is to prevent lapping powder of one size mixing with another size.
6. The sample is demounted from the lapping block and thoroughly solvent cleaned.
7. Using a silane deposition system a SiO_2 layer (about 0.2μm thick) is grown-on one side and edges. Fig. D-2 (b) shows this clearly.
8. The seed is mounted, with SiO_2 coated side facing down on a glass slide using black wax. This is clearly shown in Fig. D-2 (b): precautions should be taken to ensure the protection of the SiO_2 coating on the sides of the seeds.
9. The top seed surface is etched in concentrated HF for 1 minute. This removes all stray SiO_2 particles from the top surface.
10. The sample is demounted and solvent cleaned.
11. The sample is mounted back on the lapping block and lapped with 0.3μm and 0.05μm Alumina grit successively.
While lapping with 0.3μm and 0.05μm grit, diluted Liquinox (5% water solvent) (soap) is added to it to ensure smooth lapping.
12. The sample is polished (side without SiO_2 coating) using a



(a) Seed mounted on a lapping block.



(b) SiO_2 coating on Ge seed.



(c) Seed mounted on a glass slide.

Fig. D-2 Further preparation of the Ge seed.

NaOCl water solution and the polishing procedure described by Reisman and Rohr.[15]

13. The sample is demounted and solvent cleaned.

14. (a) Final etching is given in 5% NaOCl solution for 2 minutes using ultrasonic agitation. Finally the sample is blown dry using a dry oil-free N_2 blast on the sample surface.

(b) Alternately final etching is given in white etch ($3HNO_3$: 1HF) for 1 minute and the sample rinsed in D. I. water. It is blown dry using a dry N_2 blast on the sample surface.

(c) Alternately the seed is given an etch in white etch for 30 sec. ($3HNO_3$: 1HF) and then final etching in buffered HF($20NH_4F$: 1HF) for 10 sec. The sample is then quickly rinsed with ultra pure water and blown dry in N_2.

Whenever a white etch treatment is given the sample is mounted on a glass slide using black wax. After etching the sample is demounted and solvent cleaned before being dried using dry N_2.

6.4.2 Preparation of ZnSe source

Polycrystalline ZnSe sources were used. The polycrystalline ZnSe source was lapped flat using reduced size grits down to 3μm. They were then degreased in trichloroethylene, acetone and methanol. The ZnSe is then etched in boiling concentrated HCl until the solution turns pink. The HCl is gradually replaced with ultrapure water. Finally the ZnSe is taken out of water and blown dry in dry N_2.

7. List of References

1. Milnes and Feucht, Appl. Phys. Lett., vol. 19, pp. 383-385 (1971).
2. James et al., J. Appl. Phys., vol. 12, pp. 4976-4980 (1971).
3. James and Moll, Phys. Rev., vol. 183, pp. 740-753 (1969).
4. Escher and Williams, J. Appl. Phys., vol. 44, pp. 525, 526 (1973).
5. Williams, R., J. Electrochem. Soc., vol. 114, p. 1173 (1967).
6. Hovel, H., J.,Appl. Phys. Lett., vol. 17, pp. 141-143 (1970).
7. Hovel, H. J., and Urgell, J.J., J Appl. Phys., vol. 42, pp. 5076-5083 (1971).
8. Amick, J.A., and Roth, E.A., RCA Review, pp. 473-487 (Dec. 1963).
9. Hovel, H.J., Ph.D. Thesis, Carnegie Mellon University (1968).
10. Holt, D.B., J. Appl. Phys., vol. 45, p. 966 (1974).
11. Kennedy, A.J., to be published, Solid State Electronics, 18,(1974).
12. Chen, J.M., Surface Science, 25, p. 305 (1971).
13. Grant, J.T., and Haas, T.W., Surface Science, 23, p. 347 (1970).
14. Chang, C.C., Surface Science, 23, p. 283 (1970).
15. Reisman, A. and Rohr, R., J. Electrochem. Soc., vol. 3, p. 315 (1964).

8. Presentations

Progress reports on the contract were presented at the following ARPA program review meetings.

October 3, 1972 - Arlington, Virginia

April 19, 1973 - Fort Belvoir, Virginia

November 27, 1973 - Arlington, Virginia

9. Personnel Engaged on the Project

Dr. D. L. Feucht, Principal Investigator, Professor of Electrical Engineering.

Dr. A. G. Milnes, Principal Investigator, Professor of Electrical Engineering.

Dr. R. Sahai, Project Engineer, February 1972 - January 1973.

P. K. Govil, Project Engineer, January 1973 - June 1974.

D. A. Niebauer, Technician.

10. Energy Conservation Measures

The University has instituted energy conservation measures that include lowering of lighting and temperatures in laboratories, offices and classrooms.

In the use of the experimental equipment for this contract, the engineer and technician involved have been taking all sensible energy conservation measures.