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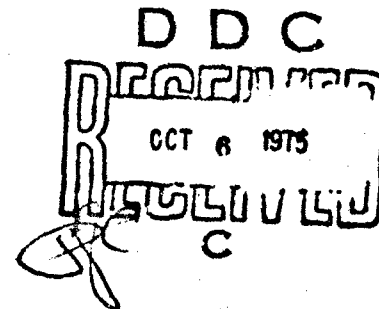
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**REVERSE CURRENT BLOCKING DIODES
FOR FLEXIBLE SOLAR ARRAY PROTECTION**

**HUGHES AIRCRAFT COMPANY
TECHNOLOGY DIVISION
EL SEGUNDO, CALIFORNIA**

APRIL 1975



**TECHNICAL REPORT AFAPL-TR-75-23
FINAL REPORT FOR PERIOD APRIL 1973 THROUGH APRIL 1975**

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**AIR FORCE AERO PROPULSION LABORATORY
Air Force Systems Command
Wright-Patterson Air Force Base, Ohio 45433**

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This report has been reviewed by the Information Office (ASD/OIP), and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nations.

This technical report has been reviewed and is approved for publication.

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Block 20 - ABSTRACT

The diode junction is diffused into a 1 x 2 cm, 8 mil thick, P-doped silicon blank. Nominal inverse voltage standoff characteristics of 140 volts at 1 mA leakage have been achieved with 20 ohm-cm base resistivity, 6 micrometer diffused junctions, and heavy silicon monoxide layers for surface passivation. Typical forward voltage drop at 0.3/3.0 amperes are of the order of 0.8/1.2 volts. Conventional diodes exhibit nominal inverse voltage standoff characteristics of 100 volts at 25 microamperes leakage, and typical forward voltage drop of 0.8/1.0 volt at 0.3/3.0 amperes.

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1. INTRODUCTION

This Blocking Solar Cell Final Report presents data on a program for development and testing of a diode for use on solar panels. The diode has the physical properties of a solar cell and the electrical properties of conventional diodes currently used for solar array reverse current isolation and protection. This combination of physical and electrical characteristics permits mounting of the diode on the panel surface in series with the solar cells, and is particularly useful for flexible arrays.

The program proceeded through development and test sequences as described below.

Initially, two manufacturers were awarded subcontracts to develop and deliver 40 evaluation diodes. The selected manufacturers were KSW Electronics, Inc. and the Heliotek Division of Textron. The development phase concluded with one of the manufacturers, Heliotek, delivering 42 diodes for evaluation tests. KSW was unable to deliver the required number of evaluation diodes. In addition to the diode development subcontract, it was necessary to procure second surface mirror covers to provide the diode assembly with appropriate thermal properties. Three vendors submitted sample covers, and after comparative testing, Optical Coating Laboratories Incorporated (OCLI) was selected as the cover vendor.

The Heliotek evaluation diodes, delivered with OCLI covers installed, successfully passed electrical, thermal, and radiation performance tests.

The evaluation phase was followed by a production phase in which Heliotek fabricated, tested, and delivered diodes using OCLI covers to a flight specification in accordance with a finalized production process.

The final phase of the program was a test phase during which the diode was subjected to qualification and environmental tests. Although formal qualification of the diodes is not considered accomplished, the testing has demonstrated that the design approach is sound, and with additional development as recommended in Section 7 of this report, qualification can be completed.

The pertinent characteristics of the production diode are:

Electrical (room temperature)

Forward Voltage Drop

at 0.3 ampere	0.8 volt maximum
at 3.0 amperes	1.2 volts maximum

Reverse Leakage Current

at 80 volts	0.1 mA maximum
at 120 volts	0.2 mA maximum
at 140 volts	1.0 mA maximum

Reverse Recovery Time

0.3 μ sec	nominal
---------------	---------

Mechanical

Size	1 by 2 cm
Thickness	0.015 inch (nominal) (including cover)
Weight	258 mg maximum

Contact Material

Titanium silver or aluminum

Tabs

Cells delivered with solder coated copper or aluminum tabs.

2. DIODE DEVELOPMENT PHASE

Two vendors, KSW Electronics, Inc. and the Heliotek Division of Textron, were selected for the diode development phase. The initial approach of both vendors was similar. It consisted of using epitaxial, N type silicon and diffusing a P layer using a planar process. Neither vendor was successful with this approach, being unable to achieve good diode reverse characteristics with reasonable yield. During development both vendors attempted to adapt their process to a bulk N starting material with a more highly doped region adjacent to the back contact to meet the required forward voltage characteristics. This approach was also unsuccessful, in not achieving satisfactory reverse voltage ratings. Heliotek then initiated experiments with a mesa process using the N bulk silicon, and found that they were able to get good yield, although at a voltage level (≈ 80 volts) below that required. The final major development step at Heliotek was to change the starting material to a P type similar to that used for standard solar cells, diffusing an N junction, etching a mesa which is then coated with silicon oxide for protection, and using a P+ back layer for achieving acceptable forward voltage performance. KSW continued development of planar diodes on various N substrates, but were never able to deliver evaluation devices within the program schedule.

During the period of diode development, three vendors, KSW, OCLI, and Heliotek submitted sample second surface mirrors which were tested at Hughes. OCLI was selected as the cover vendor on the basis of comparative tests, although the Heliotek covers were also satisfactory.

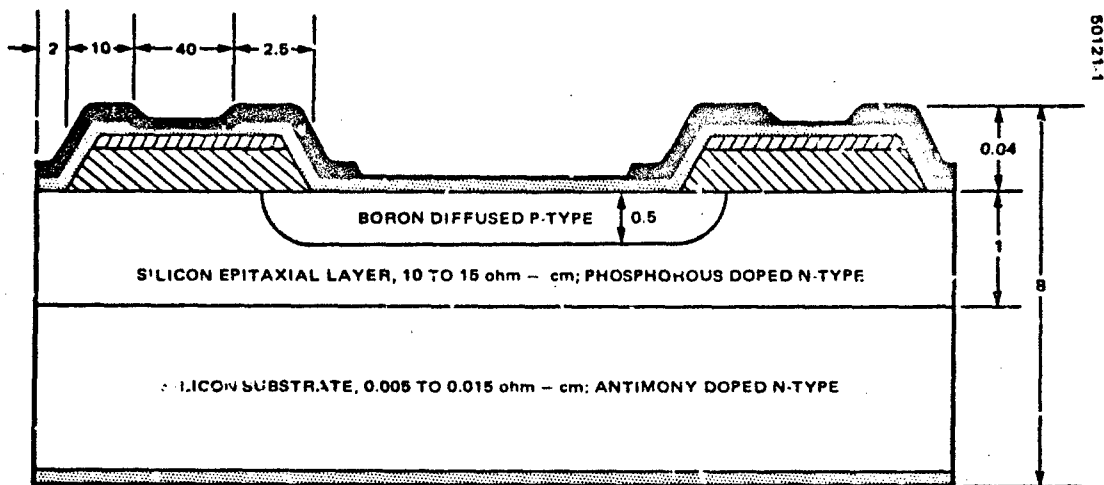
The development phase concluded with Heliotek delivering 42 diodes with OCLI covers installed, and with soldered or welded interconnects.

The remainder of this section describes the KSW, Heliotek, and cover developments.

KSW DEVELOPMENT PROGRAM

Method of Approach

The basic concept was to produce an epitaxial silicon planar design utilizing techniques which have been successful in producing small area



NOT TO SCALE

DIMENSIONS IN MILS

-  PROTECTIVE GLASS (OPTIONAL)
-  METALLIZATION
-  PHOSPHOROUS DOPED SiO_2
-  SiO_2

FIGURE 2-1. CROSS SECTION OF BLOCKING SOLAR CELL (KSW)

epitaxial planar diodes with breakdown voltages in excess of 350 volts, and with a forward current density considerably in excess of the diode requirement.

Initially, to ascertain facility capability to reproduce the small area diode, several slices of epitaxial material purchased from Transatron Electronic Corp. were processed using masks with small area (0.010 inch diameter) windows. The results indicated that the desired minimum breakdown voltage of 200 volts was readily obtainable and the forward current, proportional to the area, was more than adequate for the large area diode.

Next, mask sets applicable to the large area design of the blocking diode, as shown in Figure 2-1, were prepared by Photronic Labs, Inc. Emulsion copy plates were delivered to KSW, inspected, and found to conform to the design requirements.

Twenty-nine slices of epitaxial silicon were purchased from Transatron Electronic Corp. Slice diameter was 1-5/8 inches, with thicknesses from 0.009 to 0.010 inch.

A trial run of three slices was processed in the same manner as the small area diodes previously described. This was designated Process A shown in Table 2-1. The diodes (three per slice) were processed through titanium-silver metallization. Individual units were obtained by diamond scribing in the grid areas.

TABLE 2-1. PROCESS A

1. Standard slice clean for oxidation.
2. Oxidize at 1150°C for 30 minutes dry, 180 minutes wet, and 30 minutes dry in oxygen atmosphere.
3. Spin resist (KTFR), expose, and develop. Mask 1.
4. Etch thermal oxide from windows and grids.
5. Boron deposition at 950°C for 5 minutes warmup in oxygen, 7 minutes source on (B_2H_6) with oxygen and nitrogen, then 10 minutes soak in oxygen and nitrogen.
6. Boron drive = 1200°C for 90 minutes in 20 percent oxygen, 80 percent nitrogen atmosphere.
7. Phosphorous deposition: 1000°C for 5 minutes warmup in oxygen, 15 minutes PH_3 source on, 15 minutes soak in nitrogen and oxygen.
8. Phosphorous reoxidation at 1120°C for 60 minutes in dry oxygen.
9. Apply resist (KTFR), align, expose, and develop. Mask 2.
10. Etch boron and phosphorous oxides from windows.
11. Apply resist (KTFR), align, expose, and develop. Mask 3.
12. Clean for metallization.
13. Apply titanium-silver layer by high-vacuum vaporization to both sides of slices.
14. Remove metal masking resist (KTFR).
15. Scribe on grids and break.

Electrical results after processing were:

- 1) Best reverse voltage was 70 volts at 1 mA
- 2) All units met forward current requirements of >3 amperes at 1.0 volt.

In view of the failure to meet the reverse voltage requirement, the process was repeated to determine if any anomalies existed during the processing which could account for the observed soft breakdown characteristics. The results of the second trial were very similar; the forward current requirement was sufficient, but the best reverse characteristic was 100 volts at 1.0 mA.

The corrective actions undertaken are listed below in chronological order.

- 1) July 23, 1973 - Boron deposition time was increased from 22 minutes total time at 950 C to 30 minutes total time. Five Transitron epitaxial slices were processed.

Results: One diode of the fifteen completed units met the requirement of 200 volts at 1.0 mA. This unit cracked during forward testing.

- 2) August 10, 1973 - Boron deposition time was increased to 65 minutes to obtain a lower V/I ratio. A value of 8.0 was obtained as compared to $V/I = 21.0$ for the 30 minute boron deposition time.

Results: The boron oxide was very difficult to etch out of the windows (active areas). However, five of the nine diodes obtained 80 to 120 volts at 1.0 mA. All units were marginal for the forward requirement - 2 to 3 amperes at 1.0 volt.

- 3) September 12, 1973 - A run of six Transitron epitaxial silicon slices was made in which the phosphorous deposition and reoxidation steps were deleted. The hypothesis was that the boron oxide in the windows may not have been a complete mask for the diffusion of phosphorous atoms and would result in a degree of compensation sufficient to lower the sheet resistance of the boron diffused surface.

Results: Forward voltage values of 0.85 volt were obtained at 3 amperes. However, the inverse values were in the range of 30 to 70 volts at 1 mA.

- 4) September 20, 1973 - Three (3) slices of Transitron epitaxial silicon were processed, again omitting the phosphorous steps as in the previous run.

Results: Similar to the preceding run.

- 5) September 27, 1973 - Based on the supposition that the Transitron epitaxial material may have had imperfections in the epitaxial layer, bulk single crystal slices were obtained from Semimetals, Inc. to determine if improvements in the inverse characteristics could be obtained. Three slices were processed and contacted with titanium-silver (TiAg) on both contact surfaces. The inverse characteristic was not improved, the voltage obtained being 30 to 90 volts at 1 mA. The forward voltage drops were very high at 3 amperes. This was concluded to be the result of high back contact resistance.

Three slices of the Semimetals material were then subjected to phosphorous implanting on the cathode side to determine if the back surface concentration could be increased and thus result in a more nearly ohmic contact in conjunction with the TiAg metallization.

Results: Some improvement was obtained, but not sufficient to meet the 3 ampere specification.

- 6) October 11, 1973 - Epitaxial silicon slices with specifications equivalent to the Transitron epitaxial silicon specifications were purchased from Semimetals, Inc. Six (6) slices were processed in accordance with Process A showed in Table 2-1, which includes the phosphorous deposition and reoxidation steps.

Results: Results were comparable to those obtained with the Transitron epitaxial silicon; inverse voltages from 40 to 80 volts at 1 mA, and forward voltage drops in the vicinity of 0.85 volts at 3.0 amperes forward current.

- 7) October 25, 1973 - In the previous runs the boron drive was performed in the same diffusion tube in which the boron deposition took place. Due to continuing difficulties in the removal of the boron oxide thermally grown in the windows, a separate diffusion (drive) tube was installed and put into operation for this program. Three slices of the Semimetals epitaxial silicon were processed to the Process A program.

Results: Although the boron oxide removal was facilitated, no improvement in the reverse characteristic was noted.

- 8) November 6, 1973 - The previous program was repeated on six slices of Semimetals epitaxial silicon slices, except the phosphorous deposition and reoxidation steps were omitted.

Results: The inverse characteristics displayed from 60 to 90 volts at 1 mA. The forward voltage drops were very uniform; 0.85 volt at 3 amperes forward current.

HELIOTEK DEVELOPMENT PROGRAM

The flow chart showing the Heliotek process for their initial diode fabrication is shown in Figure 2-2. Heliotek selected a junction area considerably smaller than the total substrate area. Thermal analysis performed at Hughes (see Section 3 - Thermal Analysis) showed that the diode thermal performance was satisfactory with the proposed area. The smaller junction area was selected by Heliotek to improve response time and leakage characteristics while still achieving rated voltage drop at rated current.

Heliotek's first diodes were fabricated using both epitaxial and bulk N substrates by the process shown in Figure 2-2. Neither substrate successfully produced diodes with satisfactory reverse characteristics, the devices reaching 1 mA at voltages less than 30 volts.

Heliotek attributed this poor performance to charge neutrality balance in their oxide layer, and directed their efforts to achieving a satisfactory balance.

As a backup, several devices were processed at Ampex, because Ampex had an existing, diode process.

None of the devices processed at either Heliotek or Ampex showed noticeable improvement.

Because of these continuing difficulties, Heliotek thought that they might have better success with a mesa approach than with the planar approach that they had been pursuing.

Heliotek therefore ordered and received tooling for mesa device fabrication, and proceeded to fabricate devices with this tooling.

This process was similar in many respects to the basic approach that they had been pursuing consisting of:

- Basic silicon solar cell material (N type)
- Oxide coat and etch window
- Boron diffuse (P diffusion)
- Phosphorous diffuse (N+ back contact)
- Metallization

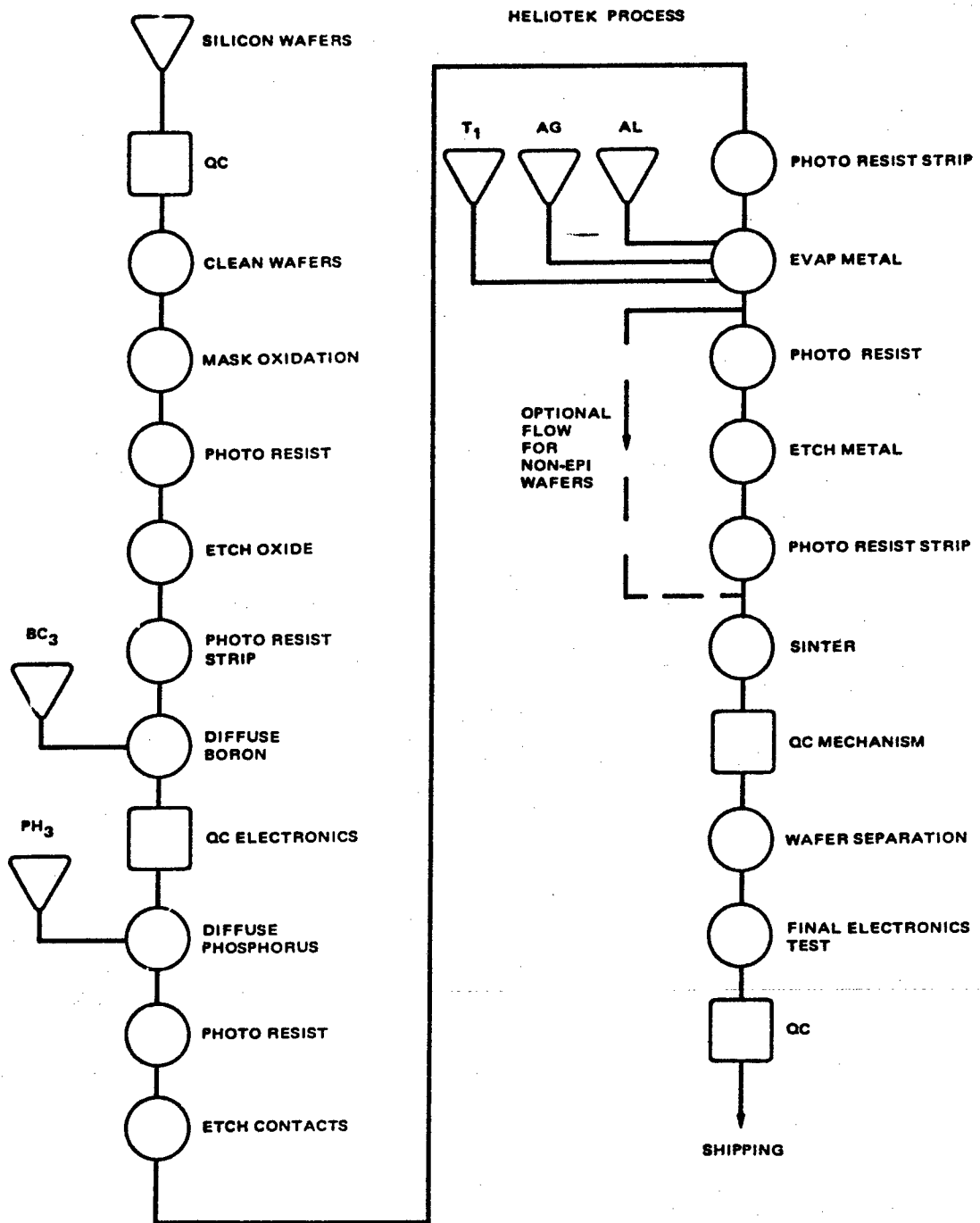
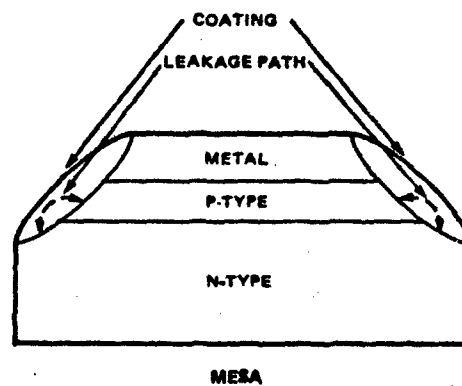
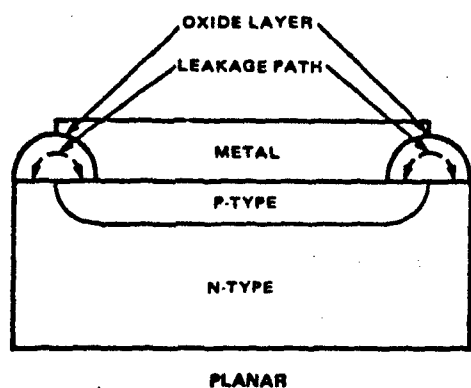


FIGURE 2-2. BLOCKING SOLAR CELL FLOW CHART – HELIOTEK PROCESS



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FIGURE 2-3. JUNCTION CROSS SECTION

In the recommended approach, after metallization, an additional etching operation is performed to form a mesa junction, as opposed to the planar junction previously supplied. As a final step, the mesa junction is coated to prevent humidity and impurities from contaminating the junction. Heliotek felt this approach offered a more timely solution to the leakage problem. In previous efforts they had been unable to successfully passivate the oxide layer over the junction periphery, which was causing high leakage effects. It was concluded that the most straightforward solution to reducing the leakage through the oxide layer was to remove this layer entirely, leaving the bare junction. The problem and proposed solution is shown in Figure 2-3.

To support the logic of switching to the mesa approach, Heliotek fabricated six sample devices in that construction using rough tooling. These devices were subjected to tests at Hughes to determine forward, reverse, and reverse recovery time characteristics as a function of temperature. A summary of the tests is presented below:

- 1) Forward Characteristics. All six devices exhibited satisfactory forward characteristics of ≤ 1.0 volt at 3.0 amperes.
- 2) Reverse Recovery Time. All six devices exhibited a satisfactory reverse recovery time of less than 3 μsec (actual readings were 0.5 μsec).
- 3) Reverse Leakage Current. A wide variation in reverse leakage current was recorded on the six devices. Initially, the leakage current was measured on all six devices with the data as shown in Table 2-2.

The diodes then had leads soldered to them, were taped to a terminal board, and placed in a temperature chamber. Forward and reverse characteristics at 100°, 25°, 0°, and -24°C were then taken. The leakage current data as a function of temperature were found to be inconsistent. Diode 4 was very consistent; with leakage current at 100 volts, it never rose above

TABLE 2-2. REVERSE LEAKAGE CURRENT

Diode											
1		2		3		4		5		6	
V		V	mA	V	mA	V	mA	V	mA	V	mA
20	100 μA	20	0.3	20	2.3	20	0.3	20	1.25	20	0.25
50	400 μA	50	0.9	65	5.0	50	1.0	50	3.5	50	0.55
80	1 mA	80	1.7	80	6.3	80	1.7	80	5.5	80	0.8
100	1.2 mA	100	1.9	100	7.5	100	2.1	100	7.0	100	0.95
118	2 mA	120	2.5	120	8.5	120	2.5	120	1.1	120	1.1

2.7 mA at all temperatures, and had leakage around 5 mA at 200 volts. Other diodes, diode 6 for example, which had an excellent leakage characteristic initially, would not support 50 volts during subsequent testing. The reason for this large variation in performance could not be fully explained, although it was postulated that the adhesive on the tape used to support the diodes on the terminal board could have softened during the 100°C test and contaminated the junction by flowing through the thin porous layer of silicon oxide which was being used to coat the junction. If this was what happened, it could be prevented in the future by using a heavier silicon oxide layer and, depending on the cover slide and cover slide adhesive, to provide additional protection for the junction.

Although inconclusive, the results of the tests were sufficiently encouraging to proceed with fabrication of larger lots of the mesa devices using production tooling to determine their performance and yield. In pursuing this work, Heliotek fabricated over 200 devices without being able to obtain consistent characteristics. The main problem still was inverse voltage, averaging about 10 to 15 mA leakage at 100 volts, not having normal diode characteristics, and appearing to act like a 10 kilohm resistor shunting the junction.

In evaluating this effect, Heliotek examined many potential causes, including the basic material itself, the oxide layer, the mesa etching sequence and time, and the contact metallization. All of these factors proved negative, although Heliotek felt that the problem might be due to small pin holes of intrinsic material shunting the junction. This hypothesis was based on the fact that Heliotek was able to produce devices with good reverse characteristics by diffusing the P layer only (boron), and also by diffusing in the P layer and the back N⁺ layer (phosphorous). However, in these latter devices, when metalized, the inverse voltage performance degenerated. In reviewing this data, Heliotek felt that the P junction diffusion was too shallow. If this were the case, during the N⁺ diffusion, the N⁺ material could find its way to the P region, perhaps through pin holes in the protective oxide layer, neutralizing small areas in the junction. Tests run by probing the P layer at one point might then show satisfactory inverse characteristics prior to metalization.

However, after metalization, the metal layer could contact the pin hole area, resulting in the shunting effect. There was evidence which followed this sequence, namely: good inverse characteristics prior to metalization and poor characteristics afterward. This could be caused by reasons other than the above, but attempts to isolate the effect to other causes proved unsuccessful.

If the poor inverse characteristic was due to insufficient junction depth, it could be verified by testing diodes with a deeper diffusion. If the P diffusion is of sufficient depth, it will not be neutralized by the N⁺ diffusion, even if the oxide layer has pin holes. An experiment to evaluate a deeper diffusion was performed.

A number of devices were subjected to a long, high temperature drive cycle (6 to 8 hours at 1150 C) which was to be followed by etching, metalization, mesa etch, and N+ back contact deposition. This experiment could not be completed because the hard glass surface formed during the deep drive cycle could not be removed in order to contact the junction. No further work was done on the N blank material after the conclusion of this experiment.

In view of the problems described above, Heliotek initiated an alternate design. This alternate design started with P material instead of the N material utilized for all prior devices by Heliotek.

The original selection of the N material was based on the availability of N type epitaxial material. This N material approach was retained, even when it was decided to try bulk material crucible grown. There was no other reason for preferring N bulk material in the design. Heliotek's decision to try the alternate path was based on availability of the P blank material used for most of their solar cells and good prior experience with it. The initial devices made with the P blank used 10 ohm-cm resistivity and a 1 micron N diffusion. The back surface was alloyed with aluminum to form a P+ back contact. Six of these devices were delivered to Hughes for testing. Tests were done at room temperature only. Results are as follows:

Device Number	V_F at 3 Amperes, V	Leakage	
		50 V	100 V
1	0.52	<0.1 mA	4 mA
2	1.24	<0.1 mA	3 mA
3	0.52	8 mA	18 mA
4	1.44	<0.1 mA	1.6 mA
5	1.28	<0.1 mA	16 mA
6	0.6	<0.1 mA	600 μ A

These results were considered encouraging, and a number of additional P blank experiments were performed as listed below:

	Number Made	Good	VR at 1 mA
1. First run - 10 ohm-cm, 1 micron diffusion	10	6	$\approx$ 70 V
2. 2nd run - 30 ohm-cm, 1.5 micron diffusion	24	$\approx$ 18	$\approx$ 90 V
3. 3rd run - 20 ohm-cm, 6 micron diffusion	12	7	$\approx$ 100 V

TABLE 2-3. REVERSE VOLTAGE DATA – DELIVERED CELLS

Aluminum Contact Cells		
Unit	Vr at 1 mA	Vr at 5 mA
1	120	136
2	118	134
3	120	135
4	112	120
5	119	134
6	120	136
7	128	136
8	122	136
9	112	120
10	118	136
11	110	120
12	124	132
13	125	132
14	120	132
15	110	130
16	128	138
17	120	130
18	120	128
19	122	130
20	110	120
21	128	132
22	12	132
23	112	130
24	110	120
25	112	128
26	112	130
27	115	132
28	116	124
29	120	130
30	122	130
31	120	130
32	100	116
33	110	120
Ti-Ag Contact Cells		
	Vr at 1 mA	Vr at 3 mA
1	140	160
2	115	125
3	120	130
4	115	120
5	120	125
6	115	120
7	110	120
8	85	110
9	Sample	

It is felt to be significant that three successive runs resulted in a good yield of devices with good diode characteristics. Although not shown in the chart, forward drops were all approximately 1 volt at 3 amperes. The one remaining development problem was improvement of the reverse voltage characteristic. The reverse voltage performance is a function of the base resistivity and the junction depth, although the back P+ diffusion may also be a factor. The selected resistivity of 20 to 30 ohm-cm and 6 micron junction depth should result in a reverse voltage rating in excess of 150 volts. One reason that the diodes did not demonstrate this higher voltage performance is that true 20 to 30 ohm-cm base material was not used. Although the material used for run 3 was initially measured at 20 ohm-cm, its resistivity was not stable when subjected to the diffusion drive temperature. It was felt that the 20 ohm-cm had been achieved by the compensation effect of entrapped oxygen rather than by basic doping level control. The heating process drove out the compensating impurities, resulting in 10 ohm-cm material.

Based on the above assumptions that true 20 ohm-cm material would result in satisfactory reverse voltage characteristics, Heliotek proceeded to process the 42 deliverable evaluation devices.

The devices were processed in accordance with Heliotek Manufacturing Control Document 021592, Appendix 1. Interconnects were soldered or welded to the diode, covers bonded and, after acceptance testing, the completed assemblies were delivered to Hughes. Electrical data on delivered devices and acceptance test samples are presented in Tables 2-3 and 2-4.

TABLE 2-4. FORWARD VOLTAGE ON
ACCEPTANCE TEST SAMPLES

Unit	VF at 25°C		VF at 100°C	
<u>Aluminum</u>	2 A	0.30 A	2 A	0.30 A
1	0.850	0.700	0.750	0.600
2	0.860	0.710	0.750	0.600
3	0.860	0.700	0.760	0.600
4	0.850	0.700	0.750	0.600
5	0.850	0.700	0.750	0.600
<u>Ti-Ag</u>				
6	0.850	0.710	0.750	0.600
7	0.840	0.710	0.740	0.600
8	0.840	0.700	0.740	0.600
9	0.850	0.700	0.750	0.600
10	0.840	0.700	0.740	0.600

COVER SLIDE DEVELOPMENT

A cover slide is required to provide the diode assembly with the appropriate thermal properties. A thermal analysis was performed (see Section 3) to determine the required solar absorptance and emittance characteristic. It was determined that the emittance property of 7940 quartz was satisfactory thermally, and that a good thermally reflective surface, such as aluminum, on the underside of the cover facing the sun would be required. Figure 2-4 shows the proposed cover slide. Sample cover slides were provided by KSW, OCLI, and Heliotek for screening tests. Although both overcoated (dielectric) and non-overcoated covers were supplied, an overcoat is essential to preserve the vapor deposited aluminum (VDA) characteristics; i. e., for protection from oxidation as well as increased mechanical durability. The following screening tests were performed on the sample cover slides.

- 1) Coupon Thermal Cycling. A total of 635 cycles from -300° to $+135^{\circ}$ F. The coupon consisted of a two-ply silica cloth laminated substrate material and solar cells bonded to the substrate with RTV 3144 adhesive, and blocking solar cell covers bonded to the cells with R-63489 (two specimens from each vendor with VDA overcoat).

Results are shown in Figure 2-5 (recognize the difficulty in photographing second surface mirrors). The KSW VDA delaminated during the test; OCLI and Heliotek passed.

- 2) Tape Peel per the following sequence (three samples each vendor, with and without VDA overcoat).

Tape Peel. If specimens pass, samples are immersed in boiling distilled water 4 to 6 minutes. After this, they are removed and the tape peel test is repeated.

The results are presented in Figure 2-6. The KSW specimens delaminated prior to boiling. Both OCLI and Heliotek passed post-boiling water tape peel. The discoloration of the two Heliotek samples without overcoat is due to oxidation discoloration; no delamination occurred.

- 3) LN₂ Thermal Shock (three samples each vendor, with and without VDA overcoat). The samples were dipped directly into LN₂ ten times.

Results are presented in Figure 2-7. The KSW sample with overcoat delaminated during the first dip. All other samples passed.

- 4) α and ϵ Measurements. Measurements were taken on two samples from each vendor (with VDA overcoat). Since quartz is the controlling ϵ factor, measurement of ϵ was made on one sample only.

Results of the measurements are presented in Figures 2-8 and 2-9, which showed spectral reflectance curves. Figure 2-8 shows averages of readings made on two samples from each of the three manufacturers, and the data was used to compute α_s . The data in Figure 2-9 was used to compute total normal emittance (ϵ_{TN}).

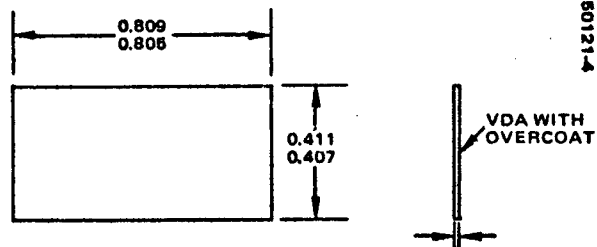
The following comments summarize the comparison test data of Table 2-5.

- 1) The values obtained for α_s are identical to within the accuracy of our equipment (± 0.015), but the Heliotek samples seemed to have a slightly lower α_s .
- 2) The value obtained for ϵ_{TN} is representative of a 7940 quartz surface of thickness greater than 3 mils.
- 3) The protective coating on the KSW samples was not uniform. It appeared to have been applied by brush.

Based on the screening test results, suggested vendor specifications, and Hughes standard VDA specifications, a blocking solar cell cover specification and revised drawing were produced. The two vendors who successfully passed the above tests; i. e., OCLI and Heliotek, were asked to quote for the total program cover buy. The development and production covers were bought at one time in order to realize a cost savings to the program. OCLI was selected as the cover vendor based on a lower cost proposal.

TABLE 2-5. COMPARISON TEST SUMMARY

Sample	Manufacturer	7940 Quartz Thickness, mils	Protective Coating	α_s^*	ϵ_{TN}^*
O-1	OCLI	8.5	Proprietary	0.11	0.81
O-2	OCLI	8.3	Proprietary	0.10	---
K-1	KSW	14.0	Silicone varnish	0.11	---
K-2	KSW	13.2	Silicone varnish	0.11	---
H-1	Heliotek	13.6	MgF ₂	0.10	---
H-2	Heliotek	14.7	MgF ₂	0.09	---



NOTES:
 SUBSTRATE MATERIAL TO BE
 CORNING GLASS WORKS NO. 7940
 FUSED SILICA, INDUSTRIAL GRADE
 SECOND SURFACE A1 MIRROR OCL I
 EDGES OF COVER TO BE PARALLEL
 WITHIN 0.002
 TOLERANCE ON ANGULARITY TO BE
 $\pm 0^\circ 15'$

FIGURE 2-4. PROPOSED COVER SLIDE

TEMPERATURE RANGE

-300 F to +175 F

NUMBER OF CYCLES

636

DESIGNATION	SUBCONTRACTOR	SAMPLE DESCRIPTION
K-3 & K-4	KSN	2.0 X 2.0 CM. WITH OVERCOAT
O-3 & O-4	O.C.L.I.	2.5 X 2.5 CM. WITH OVERCOAT
M-3 & M-4	HELIOTEX	1.9 X 6.0 CM. WITH OVERCOAT

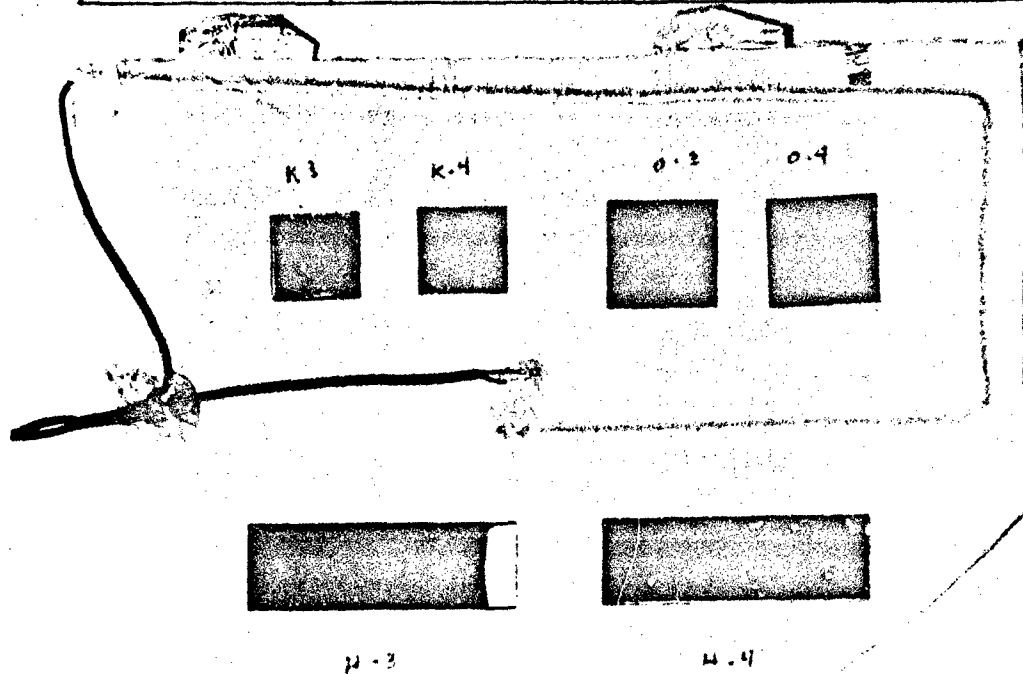


FIGURE 2-5. SUBSTRATE TEST COUPON THERMAL CYCLE ENVIRONMENTAL TEST RESULTS (PHOTO 4R31523)

SUBCONTRACTOR: KSW
NO. OF SAMPLES: 1
SAMPLE DESCRIPTION: 2.0 x 2.0 CM. WITH
OVERCOAT

SUBCONTRACTOR: KSW
NO. OF SAMPLES: 2
SAMPLE DESCRIPTION: 2.0 x 2.0 CM. WITHOUT
OVERCOAT

SUBCONTRACTOR: HELIOTEX
NO. OF SAMPLES: 1
SAMPLE DESCRIPTION: 1.9 x 5.8 CM. WITH
OVERCOAT

SUBCONTRACTOR: HELIOTEX
NO. OF SAMPLES: 2
SAMPLE DESCRIPTION: 1.9 x 5.8 CM. WITHOUT
OVERCOAT

SUBCONTRACTOR: C.C.L.I.
NO. OF SAMPLES: 3
SAMPLE DESCRIPTION: 2.5 x 2.5 CM. WITH
OVERCOAT

FIGURE 2-6. ADHESION TEST RESULTS
(PHOTO 4R31525)

IN. DIRECTION

SUBCONTRACTOR: KSW
 NO. OF DIPS: 1
 NO. OF SAMPLES: 1
 SAMPLE DESCRIPTION: 2.0 X 2.0 CM. WITH OVERCOAT



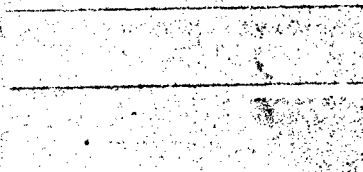
SUBCONTRACTOR: HELIOTEX
 NO. OF DIPS: 10
 NO. OF SAMPLES: 2
 SAMPLE DESCRIPTION: 1.9 X 2.8 CM. WITH OVERCOAT



SUBCONTRACTOR: KSW
 NO. OF DIPS: 10
 NO. OF SAMPLES: 2
 SAMPLE DESCRIPTION: 2.0 X 2.0 CM. WITHOUT
 OVERCOAT



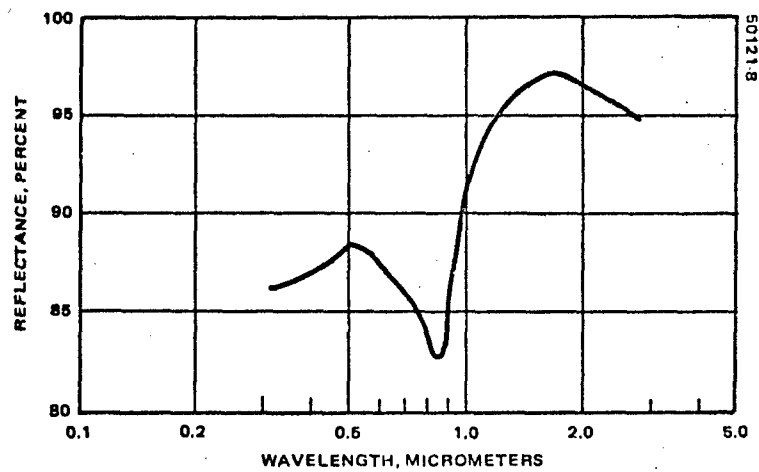
SUBCONTRACTOR: HELIOTEX
 NO. OF DIPS: 10
 NO. OF SAMPLES: 2
 SAMPLE DESCRIPTION: 1.9 X 2.8 CM. WITHOUT
 OVERCOAT



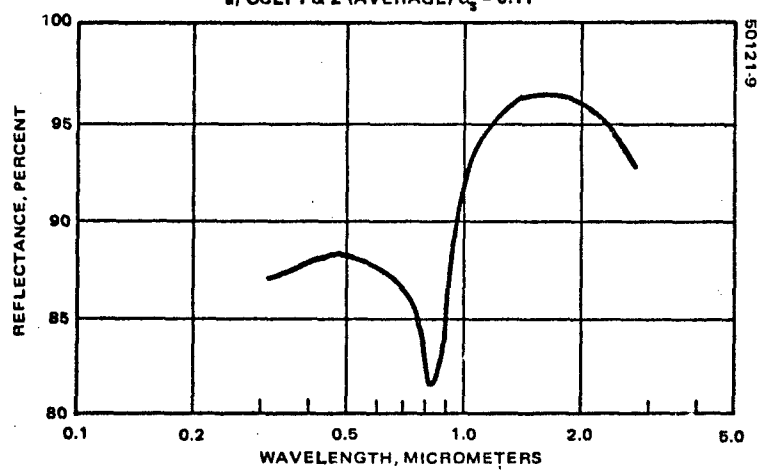
SUBCONTRACTOR: O.C.L.I.
 NO. OF DIPS: 10
 NO. OF SAMPLES: 3
 SAMPLE DESCRIPTION: 2.5 X 2.5 CM. WITH OVERCOAT



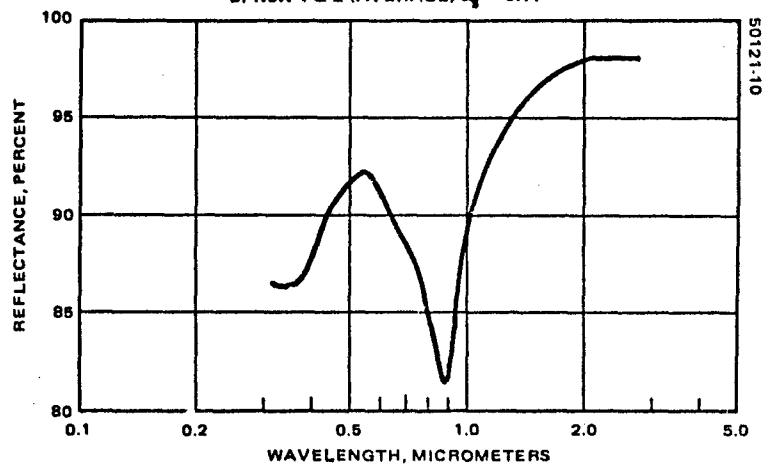
FIGURE 2-7. THERMAL SHOCK TEST RESULTS
 (PHOTO 4R31524)



a) OCLI 1 & 2 (AVERAGE) $\alpha_s = 0.11$



b) KSW 1 & 2 (AVERAGE) $\alpha_s = 0.11$



c) HELIOTEK 1 & 2 (AVERAGE) $\alpha_s = 0.09$

FIGURE 2-8. SPECTRAL REFLECTANCE (SOLAR REGION)

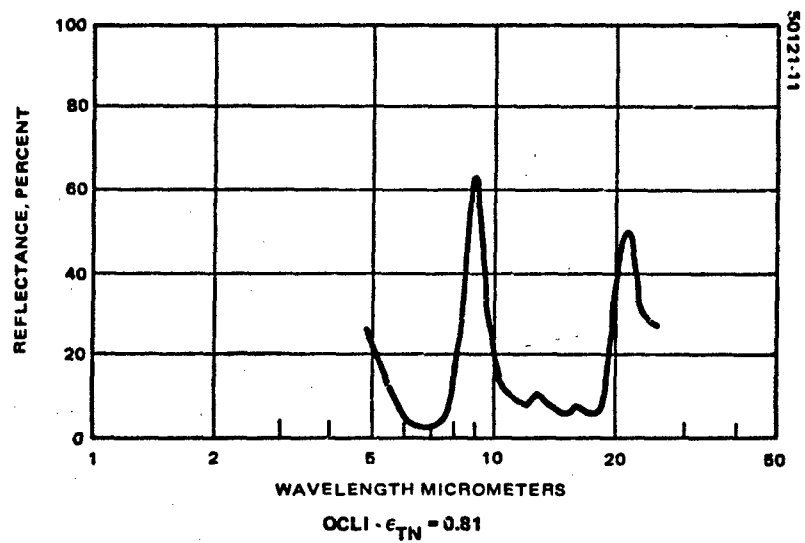


FIGURE 2-9. SPECTRAL REFLECTANCE (300°K BLACKBODY REGION)

3. DIODE EVALUATION TEST PROGRAM

The purpose of the evaluation test program was to run preliminary comparative tests on diodes from both vendors prior to selection of the vendor for the production quantity of 400 devices. Since diodes were only provided by one vendor, the comparative aspect of the evaluation test was not required. However, the testing was still important in order to provide an early assessment of diode performance and to uncover anomalies requiring investigation prior to continuing with fabrication of the final 400 devices. Tests were performed in the following areas.

- Electrical characteristics
- Thermal cycling
- Weldability and solderability
- Radiation

Data from the electrical, thermal cycling, and weldability/solderability evaluation tests were considered satisfactory. However, radiation evaluation test results raised several questions which required additional development prior to proceeding with fabrication of production diodes. The evaluation test program is described in the remainder of this section.

ELECTRICAL TESTS

Twenty cells were electrically tested, including V_F at 0.3 and 3.0 amperes at room temperature, V_F at 3.0 amperes at 195°F, V_R at room temperature, T_{rr} at room temperature, and V_R at room temperature following the 195°F test. In the latter test it was observed that lower voltage values were recorded after the 195°F exposure. The cause of this change was not investigated at this time. It was decided to incorporate a heavier silicon oxide coating in the next diodes to provide better protection from potential sources of junction contamination. The electrical data is presented in Tables 3-1 and 3-2.

TABLE 3-1. BLOCKING DIODE ELECTRICAL EVALUATION TEST DATA

Interconnect Type	Diode Serial Number	V _F (0.3 A I _F) Ambient	V _F (3.0 A I _F) Ambient	V _F (3.0 A I _F) +195°F	I _R (V _R = 150) Ambient	V _R at 1 mA	T _{rr} , μsec
Mesh soldered ↓	1	0.680	0.850	0.720	64 mA	184	2.80
	2	0.670	0.820	0.726	—	124	2.60
	4	0.680	0.820	0.726	—	130	2.60
Mesh soldered	5	0.680	0.800	0.713	—	130	2.60
Foil welded ↓	28	0.670			—	128	1.40
	1	0.670			—	136	1.60
	11	0.670	0.798	0.711	—	122	2.20
	27	0.670	0.822	0.755	—	120	1.80
	20	0.680	0.793	0.725	—	120	2.80
	6	0.670			—	125	0.80
	7	0.670			—	132	1.40
	4	0.680	0.797	0.714	—	125	2.60
	31	0.670			—	130	1.20
	23	0.690			—	125	1.80
	15	0.680			—	125	1.80
	22	0.670			50 mA	170	1.20
	16	0.670			1 mA	—	1.40
	24	0.670	0.816	0.720	—	130	2.80
	8	0.670			—	130	1.00
	5	0.680	0.790	0.722	—	130	2.00
Foil welded							

THERMAL ANALYSIS

Thermal analysis was performed to confirm the adequacy of the 1 by 2 cm size and the planned front and back shielding to operate within reliable temperature limits. This analysis takes into account cell thickness (8 mils), diode area limitations (i. e., how much of the 1 by 2 cm blank must be utilized for the diode junction), and adhesive area and thickness limitations. Results of this analysis indicated that the 1 by 2 cm, 8 mil thick design is acceptable, and that the junction area can be very small without experiencing unacceptable temperature rise.

Figures 3-1 and 3-2 present parametrically the interrelationship of internal power dissipation, required surface area for radiant heat rejection, and temperature for the panel mounted diodes. Figures 3-1a and 3-2a are for synchronous orbit conditions, while Figures 3-1b and 3-2b present similar data for the subsolar point passage in a 200 n. mi. circular orbit. Subsolar point passage at 200 n. mi. represents the hottest environmental

TABLE 3-2. POST HIGH TEMPERATURE (+195°F)
ELECTRICAL EVALUATION TESTS

Interconnect Type	Diode Serial Number	V_F (0.3 A _I)	V_R at 1 mA	Decrease in V_R after 195°F Test
Mesh soldered	1	0.680	133	51
	2	0.680	119	5
	4	0.680	120	11
Mesh soldered	5	0.680	120	10
Foil welded	28	0.670	117	11
	1	0.670	124	12
	11	0.670	110	12
	27	0.670	108	12
	20	0.680	112	8
	6	0.670	125	0
	7	0.670	122	10
	4	0.680	118	7
	31	0.670	124	6
	23	0.690	112	13
	15	0.680	118	7
	22	0.670	136	34
	16	0.670	132	18
	24	0.670	118	12
	8	0.670	122	8
Foil welded	5	0.680	119	11

conditions the diodes will experience. The assumed environmental parameters are noted on each figure.

To generate the figures, a set of thermal radiative properties for the diodes and substrate had to be assumed. A second surface mirror made of aluminized quartz and bonded to the sun facing side of the diode, similar to a cover slide, was assumed for the front thermal finish. This treatment minimizes the solar loads (the prime environment heat source) on the diode. The silica or glass cloth that is to be used as the array substrate was assumed to back the diode. The solar absorptance (α) and the IR emittance (ϵ) used in the analysis for both the front and back sides are shown on each figure. Other assumptions implicit in the analysis include: 1) a diode-to-substrate contact area greater than 80 percent of the diode surface area, 2) a negligible temperature gradient through the glass substrate, 3) radiant energy rejection from both the front and back sides of the diode (i. e., two times the diode surface area), and 4) no lateral fin away from the diode edges to assist in rejecting the dissipated energy. This last assumption

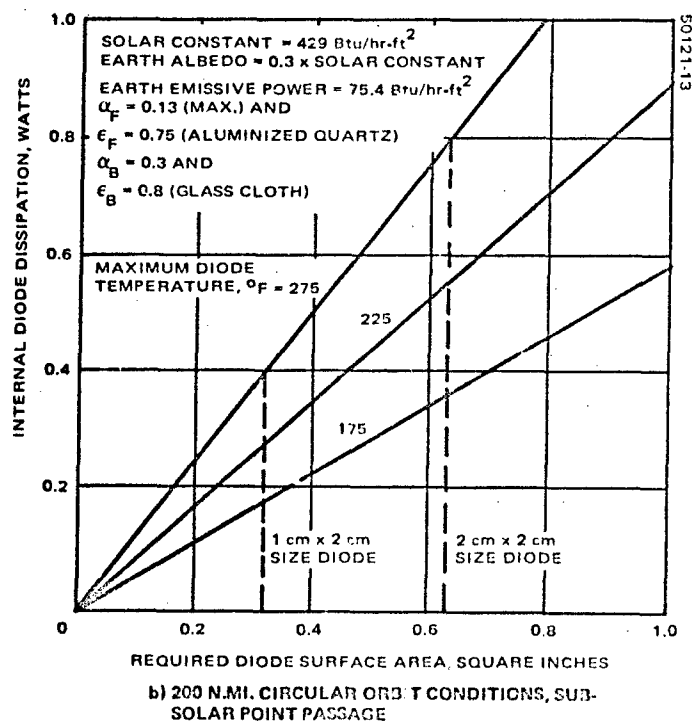
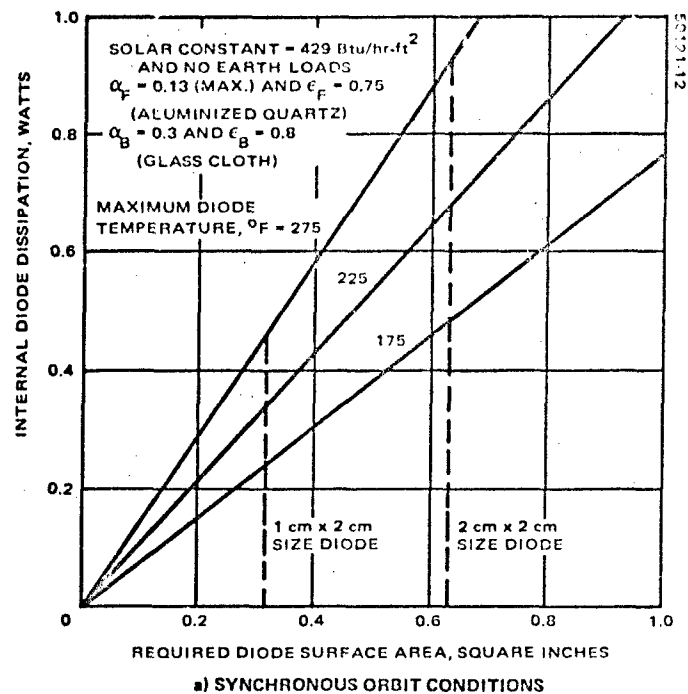


FIGURE 3-1. PANEL DIODE SURFACE AREA REQUIRED TO REJECT INTERNAL DIODE POWER DISSIPATION AT VARIOUS MAXIMUM DIODE TEMPERATURES

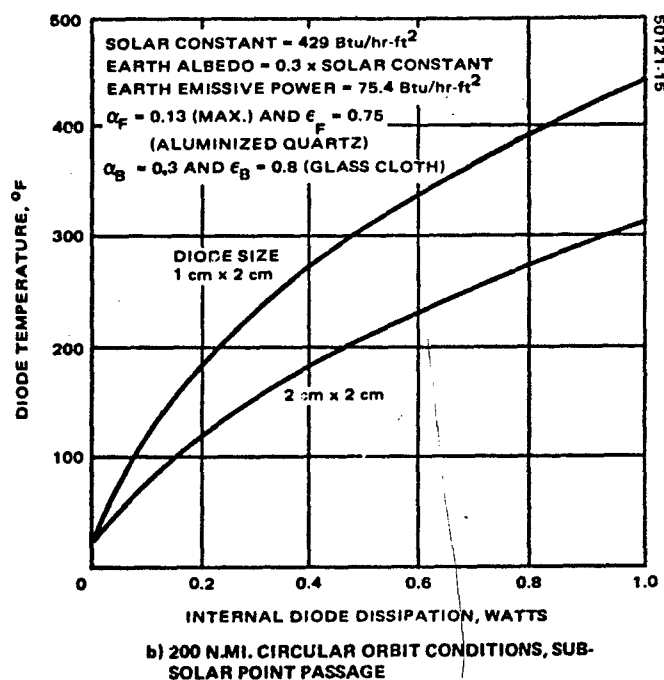
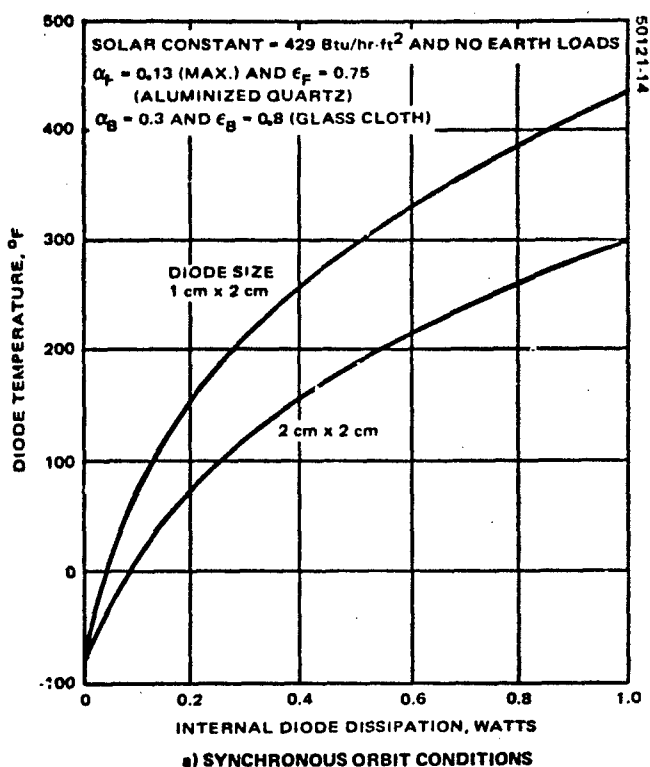


FIGURE 3-2. PANEL DIODE TEMPERATURE VERSUS INTERNAL DIODE POWER DISSIPATION FOR VARIOUS SIZE DIODES

50121-16

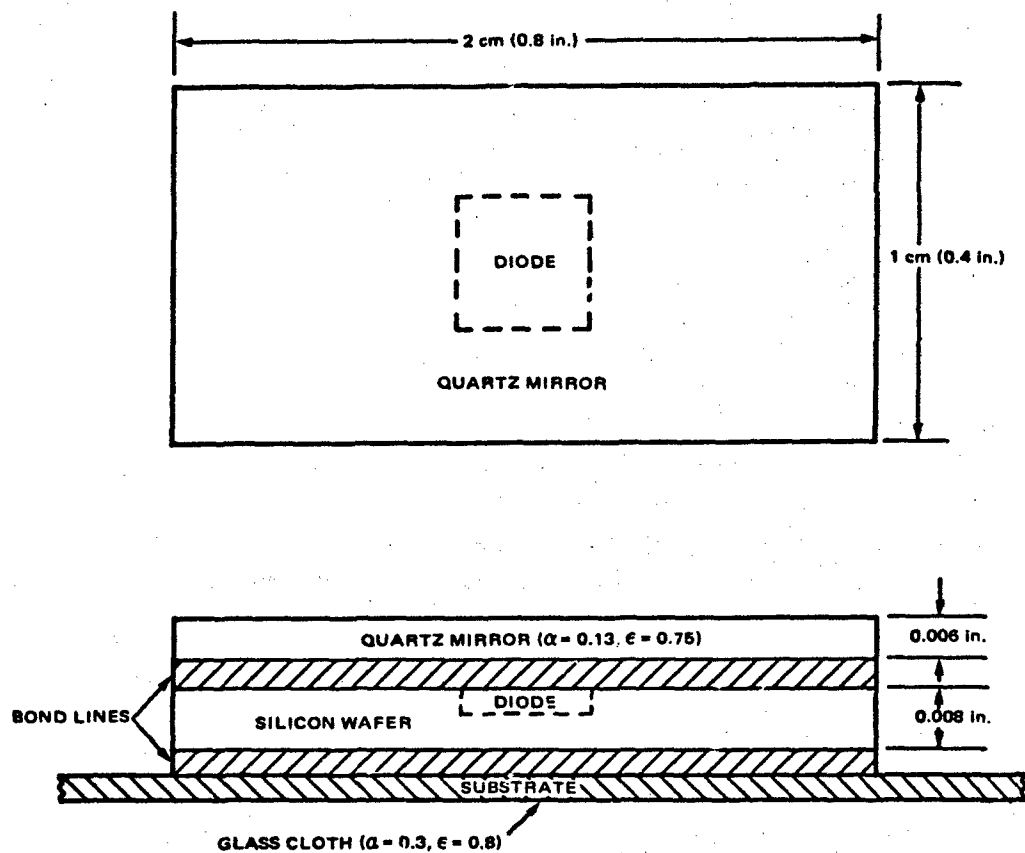


FIGURE 3-3. BLOCKING SOLAR CELL CONFIGURATION

adds some conservatism to the analysis, since it is apparent that some amount of lateral fin will exist due to bus interconnects and the substrate.

The thermal analysis presented in Figures 3-1 and 3-2 determined the bulk average temperature of a panel mounted diode as a function of power dissipation, radiating area, and orbital conditions (synchronous and low earth). The bulk model approach provides mean temperature levels of the cell, but gives no indication of temperature variations in the body. Further study was required to determine the temperature distribution in the cell assembly as a function of diode size, silicon wafer thickness, and bond line thickness. Dimensions and configuration of the baseline cell assembly are illustrated in Figure 3-3. A probable range of diode sizes was established to be from 0.1 by 0.1 to 0.6 by 0.2 inch; maximum bond line thickness was estimated to be 0.01 inch.

The effects of diode size and wafer thickness on wafer ΔT were determined with the following assumptions:

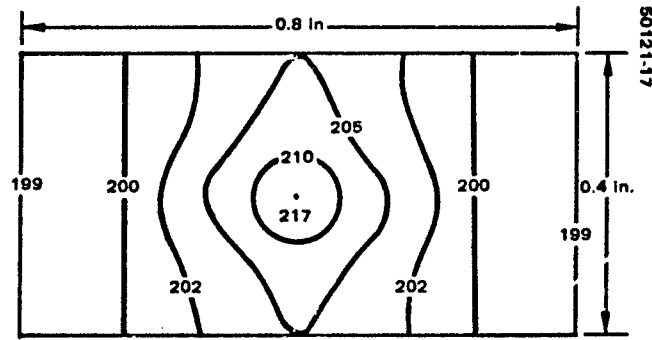
- 1) An infinite thermal conductance across the silicon/quartz and silicon/substrate interfaces
- 2) No environmental heat loads (earth, IR, albedo, direct solar)
- 3) The diode is square

The first two assumptions provide maximum T's (center to edge). A secondary effect of assumption (2) is a lower than actual bulk temperature. Figures 3-1 and 3-2 show bulk temperatures of 250° F (synchronous) and 275° F (low earth) at 0.4 watt dissipation, whereas the model assuming no environmental heat loads predicts 202° F at 0.4 watt dissipation (orbit independent). Assumption (3) was employed to eliminate the number of variables (length/width) associated with a rectangular configuration.

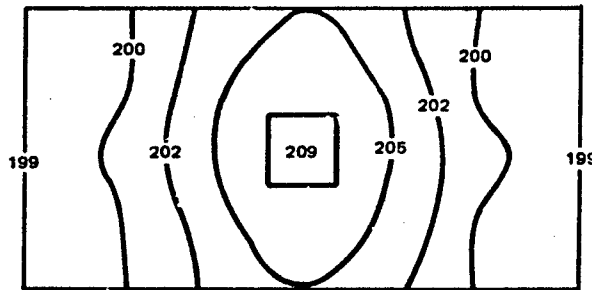
Figure 3-4 presents the temperature distribution in the silicon wafer with a 0.4 watt dissipation. The figure shows distributions associated with a point source and with a 0.1 inch square diode. The point source analysis provides an upper bound on the center-to-edge temperature difference which is seen to be 18° F. This ΔT is reduced to 10° F with a heat source distributed within a 0.1 inch square. As mentioned previously, the assumptions employed in this analysis predict a bulk temperature of 202° F. The two sets of isotherms indicate the relationship of bulk temperature to temperature distribution for the system under consideration.

To the first order, the center-to-edge ΔT is directly proportional to the dissipation rate and inversely proportional to the wafer thickness. Thus, for the point source configuration:

$$\text{Center to edge } \Delta T = 18^{\circ}\text{F} \left[\frac{Q}{0.4} \right] \left[\frac{0.008}{t} \right]$$



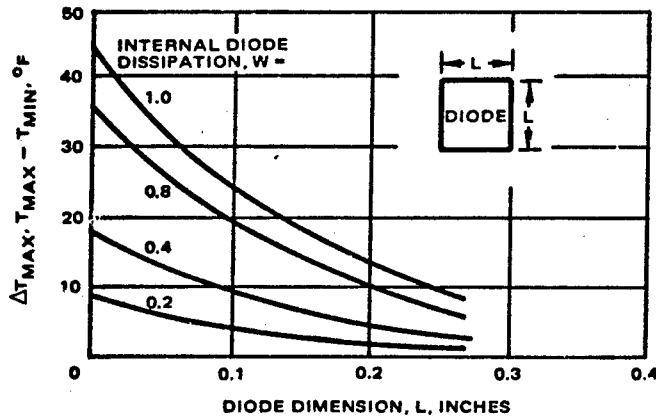
DIODE - POINT SOURCE



NUMBERS - TEMPERATURE, °F

DIODE 0.1 x 0.1 in.

FIGURE 3-4. SILICON TEMPERATURE DISTRIBUTION, 0.4 WATT



Q, W	BULK TEMPERATURE (SYNC), °F
0.2	180
0.4	250
0.6	320
0.8	380
1.0	420

FIGURE 3-5. MAXIMUM SILICON ΔT VERSUS DIODE SIZE

Figure 3-5 was constructed from this relationship and the diode size effects of Figure 3-4.

The Table in Figure 3-5 summarizes bulk temperatures as a function of diode dissipation. Comparison of the graph and table data show the wafer ΔT s are relatively small compared to the bulk temperature.

Another area of investigation involved the determination of the effect of bond line thickness on the diode temperature level. In view of the relatively small ΔT s shown in Figures 3-4 and 3-5, a bulk conduction model was employed to establish the effect of bond line thickness on diode temperature. The model was based upon the assumptions:

- 1) Equal bond line thickness between the silicon/quartz and silicon/substrate
- 2) The substrate and quartz are at the same temperature
- 3) The bonding material exhibits a thermal conductivity of 0.1 BTU/hr-ft-°F, which is a typical value for silicones and epoxies.

For a 1.0 watt dissipation rate, the following results were obtained:

<u>Glue Thickness, in.</u>	<u>ΔT (Diode-Substrate = Diode-Quartz), °F</u>
0.001	0.9
0.005	3.6
0.010	7.0
0.020	14.0

These results are linear with respect to heat dissipation and glue thickness. The ΔT 's are seen to be small, thus indicating the validity of assumption (2).

It is concluded from these results that the bulk cell temperatures presented in Figures 3-1 and 3-2 are indicative of the diode temperature.

For an 0.1 by 0.1 inch diode, an 0.020 inch bond line, and 0.4 watt dissipation, the bulk temperature of the wafer will be 5° F above the cell bulk temperature (Figures 3-1 and 3-2), and the diode temperature will be 7° F above the wafer bulk temperature.

THERMAL TESTS

Vacuum Tests

The object of this test was to determine the operational temperature characteristics of the diodes mounted on various substrates and to compare the results to the thermal analysis. Two diodes of each type were tested.

The first phase of the experiment consisted of measuring the forward voltage of each diode at 0.2, 0.4, and 0.6 ampere, and at a series of temperatures from 100° to 280°F (in increments of 20°F). The diode temperatures were set by placing the devices in an oven at the specified temperature and pulsing the current through the devices for approximately 1 ms. The pulse repetition rate was set such that the duty cycle remained less than 1 percent to minimize heating.

To measure the forward voltage of these pulses, an oscilloscope was used in a differential mode comparing the peak voltage of the current pulse to a reference voltage set with a DVM. This technique allowed easy measurement to within ± 2 mV. Thermal equilibrium within the chamber was assumed when the temperature within the chamber, as measured with a mercury bulb thermometer, remained within 2°C for 10 minutes or more. A series of temperature versus voltage calibration curves was then plotted from this data.

The second phase of this experiment was conducted in a vacuum chamber. Inside the chamber was an LN₂ cold wall shroud maintained at -320° F and a 500 watt infrared tungsten lamp to radiatively cool and heat the devices. The mechanical configuration of the components inside the vacuum chamber is straightforward. The Phase 2 test procedure consisted of measuring the forward voltage of the diodes at 0.2, 0.4, and 0.6 ampere, first with no illumination, next with a 70 percent relative maximum voltage to the tungsten lamp, and finally with 85 percent relative maximum voltage to the tungsten lamp. The 70 percent point corresponds to approximately 400 watts radiated by the lamp, and 85 percent corresponds to approximately 500 watts radiated by the lamp.

Assuming a cylindrical radiation pattern, the incident energy at 12.7 cm from the lamp should be approximately 400 mW/cm². A 1 by 2 cm diode would then intercept approximately 800 mW. The substrate, being about 4 by 4 cm, would intercept 6.4 watts. Using an average absorptivity over the test coupon of 0.1, the coupon would adsorb a power of 640 mW. The incident infrared energy for this experiment is considerably higher than expected in space; however, the approximations used to determine this value would yield higher than actual values, and the coupon did not contain working solar cells. The presence of working solar cells could considerably alter the local substrate temperature.

Previous experiments and predictions have been based on absorption and radiation from an area the size of the diode only. That is, heat conduction along the length or width of the substrate is not considered. In so doing, the values predicted should be worst case conditions (assuming α and ϵ values used were actual measured values).

A comparison between theoretical and measured values can be drawn by determining the rise in temperature per watt of dissipation and comparing this value with the measured values. The 1 by 2 cm diodes have a single side area of 0.807 by 0.409 inch = 0.330 square inch. Figure 3-1 shows that for a 0.33 square inch diode, and a temperature rise of 100° F, an internal power of 0.22 watt can be dissipated. This is a 100° F/0.22 watt - 455° F/watt thermal impedance. Measured values obtained from the plotted data are tabulated on Table 3-3.

It is noted that the measured thermal impedance data are consistently lower than the predicted, and that the thermal impedance under illumination is lower than without illumination. This reduction in impedance results from the T^4 dependence of radiation on temperature.

In conclusion, the measured thermal impedance values demonstrate that the theoretical values are conservative worst case values. This is probably due to thermal conduction along the substrate material, giving an effectively larger radiating surface.

Thermal Cycling Test

A thermal cycle test consisting of 100 thermal cycles between -185° and +100° C were run on test coupons. These coupons consisted of three silver-titanium contact diodes and three aluminum contact diodes. All of the diodes were bonded to a silica cloth substrate using RTV 3144. The diodes were then cycled at the temperature shown above, each cycle consisting of 0.5 minute at the high temperature and 2 minutes at the low temperature. No cracks or failures were directly attributed to the cycling. There were two problems. A small crack was observed in one of the soldered diodes; however, the crack was thought to have been present initially. The crack did not grow during cycling. Furthermore, electrically, the cracked diode performed normally. A second diode, which had a high (≈ 200 volts) rating prior to bonding, had a low (≈ 30 volts) rating after bonding. This loss in voltage rating was of concern, but the cause was not determined.

TABLE 3-3. THERMAL IMPEDANCE (°F/Watt)

S/N	Volt Illumination, percent (500 W Lamp)		
	0	70	85
3	430	290	280
4	405	370	310
12	445	350	300
13	430	300	315

4. RADIATION

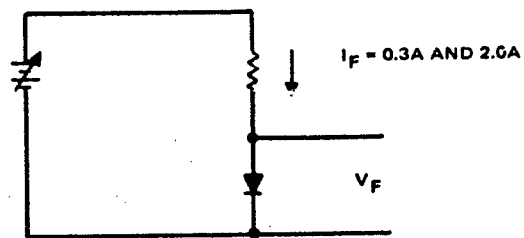
Radiation effects testing in the Reverse Current Blocking Diode program involved exposing the blocking diodes to radiation in four specific phases, as follows:

- 1) Total ionizing dose exposure
- 2) Prompt dose exposure
- 3) Simulated fission spectrum electron exposure
- 4) Underground test

Total dose tests were conducted with the Hughes Aircraft cobalt-60 gamma source. Prompt dose tests were conducted using the Hughes linear accelerator (LINAC) and the TREF Pulserad 1590 flash X-ray (FXR) machine. Simulated fission spectrum electron testing utilized the Hughes LINAC. Results of the testing are presented herein.

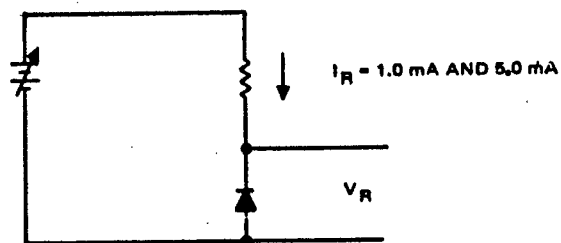
Total ionizing dose tests evaluated the effects of low dose rate gamma radiation on diode parameters. The exposure in this test simulated the gradual absorption of energy due to natural space radiation encountered by space satellite systems. The test was conducted by exposing the diodes to gamma radiation in controlled increments. Diode operating characteristics were measured before, between, and after exposures to the gamma radiation. Changes in diode operating parameters indicated the existence of radiation sensitivity.

Prompt dose testing involved exposure of the diodes to high dose rate radiation pulses. During exposure to the radiation pulses the diodes were monitored to record photocurrent levels and storage time. Diode operating parameters were measured before and after exposure to detect the occurrence of permanent damage. This test simulated nuclear weapon generated gamma pulses. Dose rates of varying levels were delivered by two radiation effects machines. Lower dose rate Bremsstrahlung (gamma) radiation was obtained from the Hughes LINAC and higher dose rate Bremsstrahlung was obtained from the TREF Pulserad 1590 FXR machine. To fill in the midrange dose rate gap, the Hughes LINAC was operated in the direct electron mode.

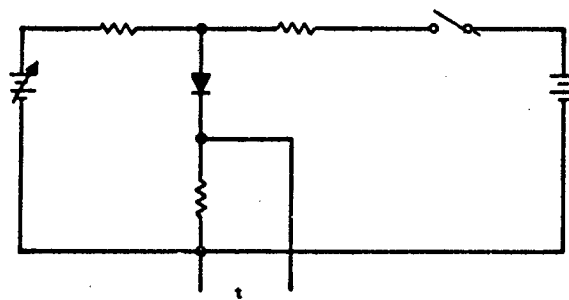


50121-19

FORWARD VOLTAGE DROP, V_F



REVERSE VOLTAGE DROP, V_R



REVERSE RECOVERY TIME t_{rr}

FIGURE 4-1. REVERSE CURRENT BLOCKING DIODE
PARAMETER MEASUREMENT CIRCUITS

Nuclear weapon generated fission spectrum electrons were simulated by direct electron operation of the Hughes LINAC. Exposure in this test was carried out at low dose rates which required multiple pulsing of the LINAC to build up the required electron fluence. Diode parameters were measured prior to and following exposure.

TOTAL IONIZING DOSE TEST

Description of Test

Nine blocking diodes were exposed in the total dose tests. These diodes had a resistivity of 10 ohm-cm, and were part of the initial shipment of evaluation diodes. Five of the diodes tested were fabricated with aluminum tabs welded to the diode. The remaining four diodes had silver-titanium tabs soldered to the diodes. All diodes were complete with cover glass. The general procedure of this test involved measuring specific operating parameters prior to and following each exposure to the cobalt-60 gamma radiation.

The parameters selected for measurement were:

- 1) Forward voltage drop (V_F) at forward currents of 0.3 and 2.0 amperes
- 2) Reverse voltage drop (V_R) at reverse currents of 1.0 and 5.0 mA
- 3) Reverse current recovery time (t_{rr})

Test circuits utilized in parameter measurements are presented in Figure 4-1.

Test Results

Results of total ionizing dose testing are presented in Figures 4-2 and 4-3, and are discussed below:

- 1) V_F - Minor changes were observed in this parameter, as shown in Figure 4-2a
- 2) V_R - All diodes tested exhibited a tendency for V_R to improve (increase) as total dose was increased for accumulated dose levels up to 10^7 rads (Si), as shown in Figure 4-2b. Further exposure to cobalt-60 gamma seemed to cause V_R to start decreasing, as shown in Figure 4-2b.
- 3) t_{rr} - Exposure to total ionizing dose tended to cause the diode to become faster, as shown by the decrease in t_{rr} in Figure 4-3. The change in t_{rr} was greater for welded tab diodes than for diodes with soldered tabs. The reason for

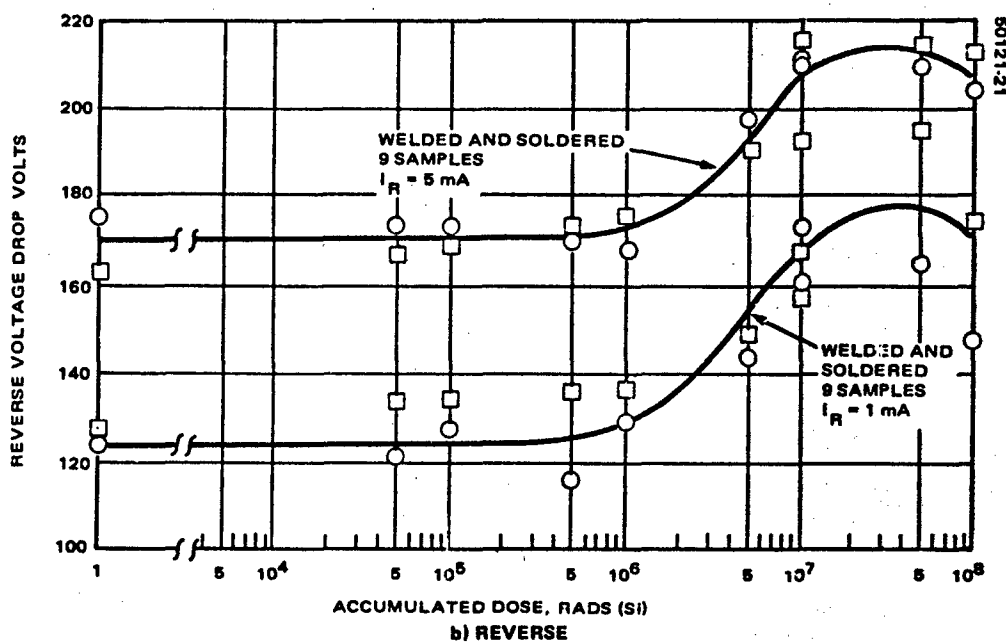
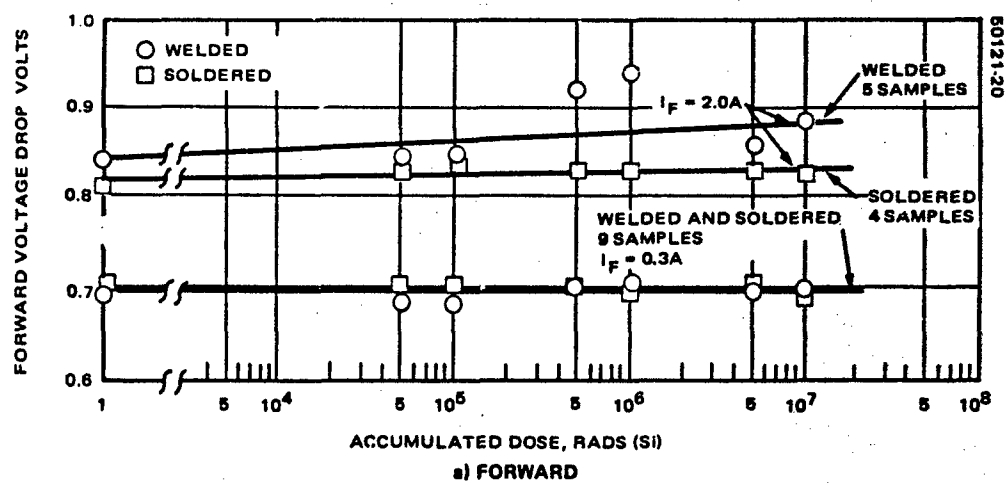


FIGURE 4-2. VOLTAGE DROP VERSUS COBALT 60 DOSE

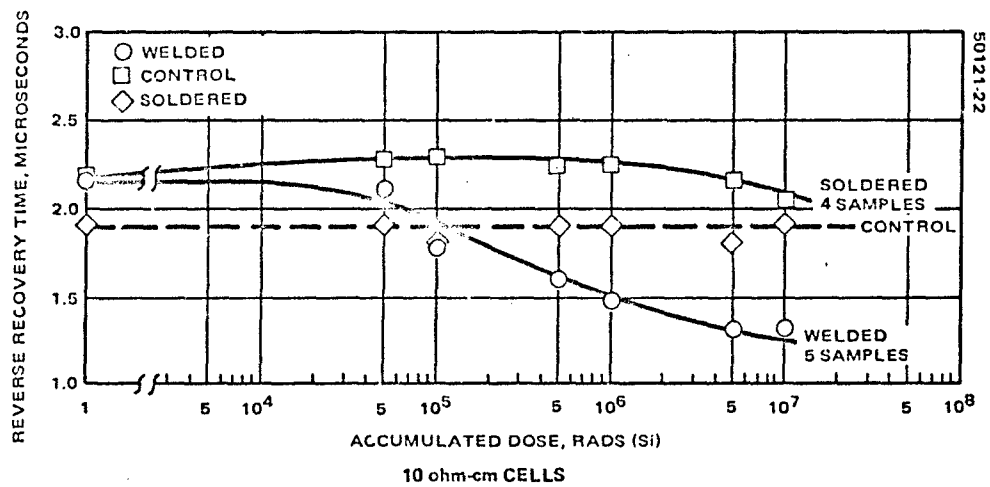


FIGURE 4-3. REVERSE RECOVERY TIME VERSUS COBALT 60 DOSE

this difference in parameter variation is not understood, but since the change represented parameter improvement, this phenomena was not studied further.

PROMPT IONIZING DOSE TEST (LINAC)

Description of Test

Five diodes with welded aluminum tabs were exposed to LINAC generated Bremsstrahlung radiation pulses with 100 ns pulsewidth and 10^7 to 6×10^7 rads (Si)/second dose rate. These diodes were 10 ohm-cm cells, part of the original evaluation units, and had not been subjected to any radiation prior to exposure in this phase of the radiation effects test program. The diodes were placed in a circuit in which reverse bias was applied. The test circuit is presented in Figure 4-4. When irradiated in a reverse biased condition, the diode conducts pulses of photocurrent generated by the radiation pulse. The amplitude of the photocurrent pulse will be directly proportional to the dose rate of the radiation pulse up to the point where the bulk resistance of the diode or circuit impedance causes saturation of the circuit. A current sampling resistor was utilized to enable recording the photocurrent pulse. The value of the sampling resistor was kept low to preclude saturation due to circuit impedance. The general test procedure involved measuring the three previously identified performance parameters prior to exposure to the radiation pulse, recording the photocurrent pulse when the diode was irradiated, and measuring the parameters again following the exposure.

Test Results

LINAC test results are presented in Table 4-1 and Figure 4-5 and discussed below:

- 1) V_F and t_{rr} - No significant change was observed in these parameters.
- 2) V_R - The effects of LINAC Bremsstrahlung on V_R are tabulated in Table 4-1. The data indicates a slight increase in V_R , definitely no degradation in the parameter.
- 3) Photocurrent pulse amplitude demonstrated the linear relationship known to exist between photocurrent and radiation pulse dose rate.

PROMPT IONIZING DOSE TEST (FXR)

Description of Test

To extend the prompt dose testing to higher dose rate levels it was necessary to utilize a higher fluence machine. The Pulserad 1590 FXR

TABLE 4-1. LINAC AND FXR BREMSSTRAHLUNG EFFECTS ON
BLOCKING DIODE^a

Date	Burst	Dose Rate/Dose			V _R , V		I _p , μ A	ts, μ sec
		$\dot{\gamma}$ ^b	γ ^c	$\Sigma \gamma$ ^d	I _R = 1 mA	I _R = 5 mA		
January 16, 17, 18, 1974	Initial Reading	—	—	—	132	151	—	—
	LINAC Three bursts	10^7 to 6×10^7	—	8.8×10^3	144	170	Figure 4-5	0
January 24, 25, 1974	FXR	—	—	—	—	—	—	—
	1	2.2×10^{10}	1.4×10^3	7.2×10^3	125	159	—	—
	2	2.8×10^{10}	1.7×10^3	8.9×10^3	85	117	29	3.3
	3	6.5×10^{10}	4.2×10^3	1.3×10^4	72	94	77	3.4
	4	4.1×10^{11}	26.8×10^3	4.0×10^4	63	79	95	5.5
February 1974	5	4.7×10^{11}	30.8×10^3	7.1×10^4	61	77	100	5.9
	Post-5	—	—	—	—	—	—	—
	7	—	—	—	69	73	—	—

^a 10 ohm — cm cells

^b $\dot{\gamma}$, Rads (Si)/sec. — Dose rate

^c γ , Rads (Si) — Dose this shot

^d $\Sigma \gamma$, Rads (Si) — Accumulated dose

machine located at TREF was used in the Bremsstrahlung mode of operation to generate 65 ns radiation pulses with dose rates ranging from 2×10^{10} to 5×10^{11} rads/sec. The five diodes irradiated in the LINAC test were subjected to the FXR radiation environment. The diode circuit configuration was identical to that presented in Figure 4-4. Forward voltage, reverse voltage, and reverse recovery time were the parameters measured to determine radiation induced degradation. The performance parameters were measured prior to and following exposure to the FXR pulse. Photocurrent responses were also recorded during the exposure.

Test Results

As this test progressed it became apparent that although the measured photocurrent was greater than for the LINAC tests, the increase did not display the linear relationship which is known to exist between photocurrent magnitude and radiation pulse dose rate. This nonlinearity in photocurrent is due to current limiting by the diode bulk resistance. The existence of current limiting due to diode bulk resistance is further demonstrated by the presence of photocurrent stage time for the FXR test. The results are presented in Table 4-1 and Figure 4-5. Forward voltage and reverse recovery time did not vary because of exposure to the FXR pulses; however, reverse voltage showed definite degradation due to the FXR pulses. Table 4-1 shows how the value of V_R decreased with increased dose rate.

Initially it was suspected that the observed degradation of V_R might be caused by destructive heating due to high current density. This theory, however, was essentially disproved by a lab test which revealed no degradation of V_R, even after the diode had been subjected to ten consecutive

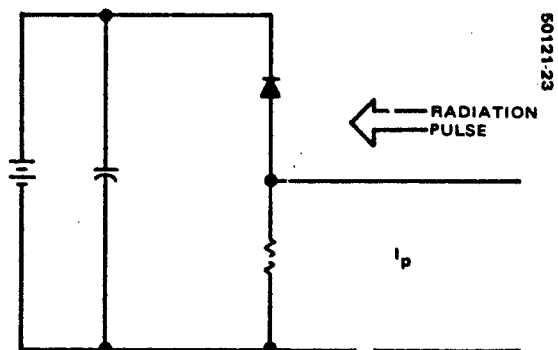


FIGURE 4-4. BLOCKING DIODE PHOTOCURRENT MEASUREMENT CIRCUIT

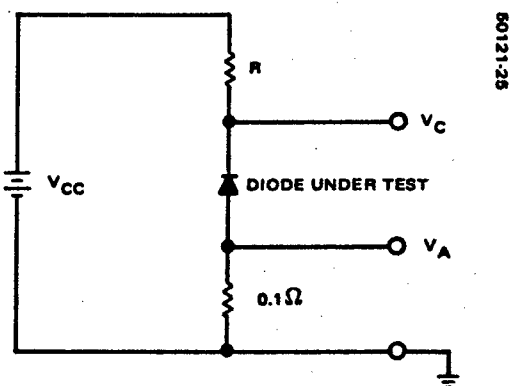


FIGURE 4-6. DIODE CIRCUIT CONFIGURATION FOR LINAC DIRECT ELECTRON EXPOSURE TEST

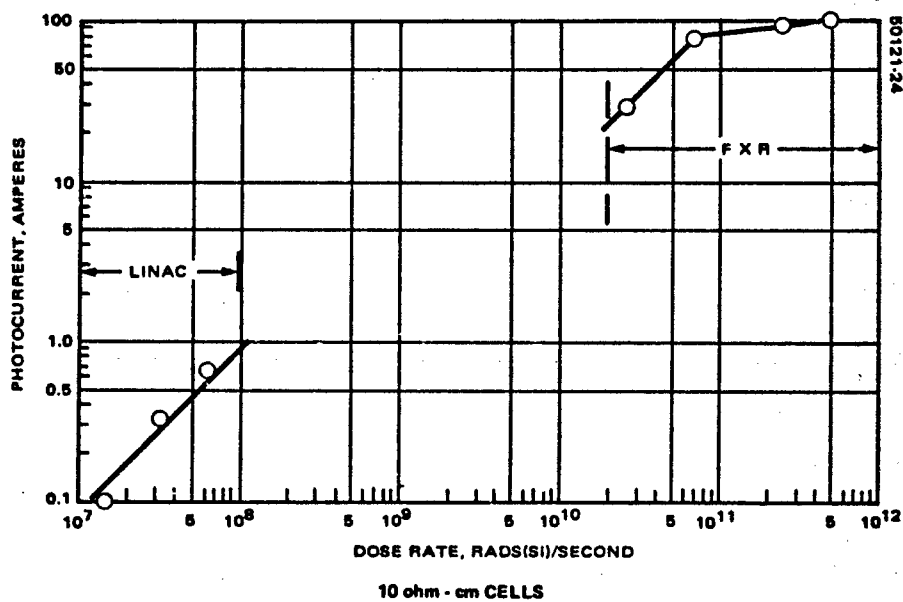


FIGURE 4-5. DIODE PHOTOCURRENT VERSUS BREMSSTRAHLUNG DOSE RATE

200 ampere pulses. Further tests performed by Heliotek and reported in program monthly reports have indicated that the mechanism of the observed degradation is not due to destructively high current density.

PROMPT IONIZING DOSE TEST (LINAC-ELECTRON)

Description of Test

Review of the FXR test results indicated that V_R degradation became significant for radiation pulse dose rates as low as 2×10^{10} rads/sec. When the LINAC is operated in the direct electron mode, dose rates of 2×10^{10} can be achieved. Therefore, an extensive test program was undertaken to determine what V_R degradation was dependent upon and to evaluate new lots of diodes. Objectives of each test are presented below:

- 1) Irradiate 10 ohm-cm diodes from evaluation units to determine dependency of V_R degradation.
- 2) Irradiate bare 10 ohm-cm diodes without tabs and glass cover slide to determine if damage dependency is related to the tabs or cover slide.
- 3) Irradiate 20 ohm-cm diodes to evaluate effect of increased resistivity and junction capacitance.
- 4) Irradiate 15 ohm-cm diodes.
- 5) Irradiate 3 ohm-cm diodes.

The diode circuit configuration in all cases was that shown in Figure 4-6. The values of V_{CC} and R were chosen to limit the photocurrent magnitude to desired levels, and instrumentation points were monitored to determine voltage across the diode and to determine the amplitude and time history of the photocurrent transient.

Test 1 Results

Initial tests using the LINAC revealed the same damage that was observed in the FXR test. Responses observed during this test are shown in Figure 4-7. The scope traces correspond to the test points of Figure 4-6. The top trace (V_C) is out of the field of view prior to the radiation exposure, then, because of photocurrent flow, the value of V_C changes to bring the trace into the field of view. Figure 4-7 shows response for a constant LINAC direct electron pulse. The relationship between photocurrent and storage time is readily visible. A relatively consistent indicator of the onset of V_R degradation was provided by the manner in which the bottom trace recovered; when the trace recovered with a single negative swing (pulses 1 and 2), there was usually no V_R degradation. Oscillating recovery such as shown in pulses 3 and 4 usually accompanied degradation of the value of V_R .

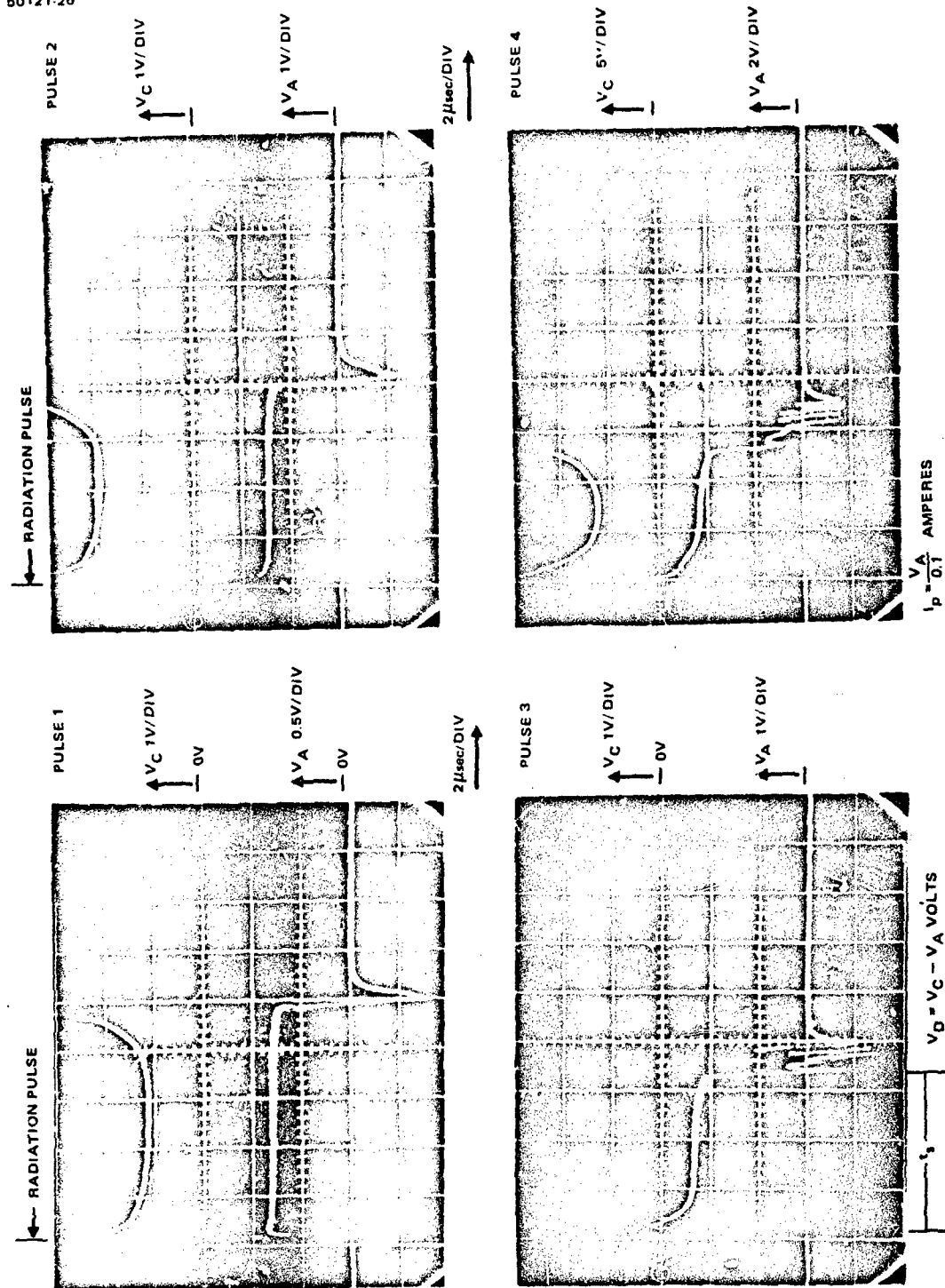


FIGURE 4.7. TYPICAL DIODE RESPONSE TO LINAC DIRECT ELECTRON PULSES

More detailed testing was set up to gain better definition of the dependence of V_R degradation upon the photocurrent transient. Three 10 ohm-cm diodes from the evaluation units and one standard axial lead diode were irradiated in this test. The radiation pulse conditions in this test were 10^{10} rads/sec dose rate, 1 μ sec pulsewidth, and 10^4 rads dose. The following information was recorded from the test:

- 1) Photocurrent (I_P)
- 2) Photocurrent storage time (t_g)
- 3) Voltage across diode (V_D)

These data were used to calculate the effective junction energy dissipation to determine a coarse estimate of the stress placed upon the diode junction. Results of this test are tabulated in Table 4-2 and plotted in Figure 4-8a. The test demonstrated that V_R degradation becomes significant when junction energy dissipation exceeds 100 μ J.

Test 2 Results

The second test was set up to determine whether the V_R degradation was caused by the attachment method for the tabs and glass cover slide. A group of bare diodes were obtained for these tests. These bare diodes had no connecting tabs and no glass cover slides. Exposure of these diodes to the LINAC direct electron beam was performed in the same manner as it was for the complete diodes. Initial exposures of the bare diodes revealed that the V_R degradation was not related to tab or cover slide attachment. The test was continued to determine the effect of dose rate upon V_R degradation. Results of this continued testing are presented in Figure 4-8a. The curves in Figure 4-8b show how the damage increases when the radiation pulse dose rate exceeds 10^{10} rads/sec.

Test 3 Results

Although the diode damage dependence had been identified in the first two tests, the actual mechanism of the damage remained undefined. Test 3 was to determine what effect diode junction capacitance had upon V_R degradation. This test was conducted on 15 ohm-cm diodes on which precise pre-radiation junction capacitance measurements were made at Heliotek. After exposing and damaging the diodes they were returned to Heliotek for post-radiation junction capacitance measurements.

Prior to conducting this test a set of circuit conditions representing the HASPS application were determined and presented in program monthly report No. 13. The conditions consisted of $V_{CC} = 25$ volts and $R = 0.5$ ohm, which results in a maximum photocurrent of approximately 45 amperes. Tests conducted after this point used these conditions.

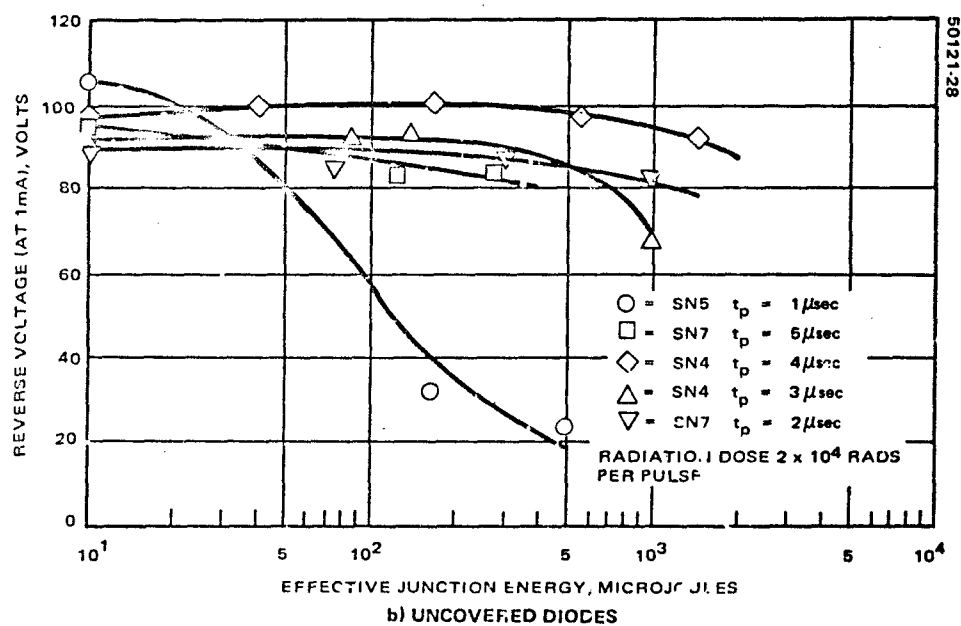
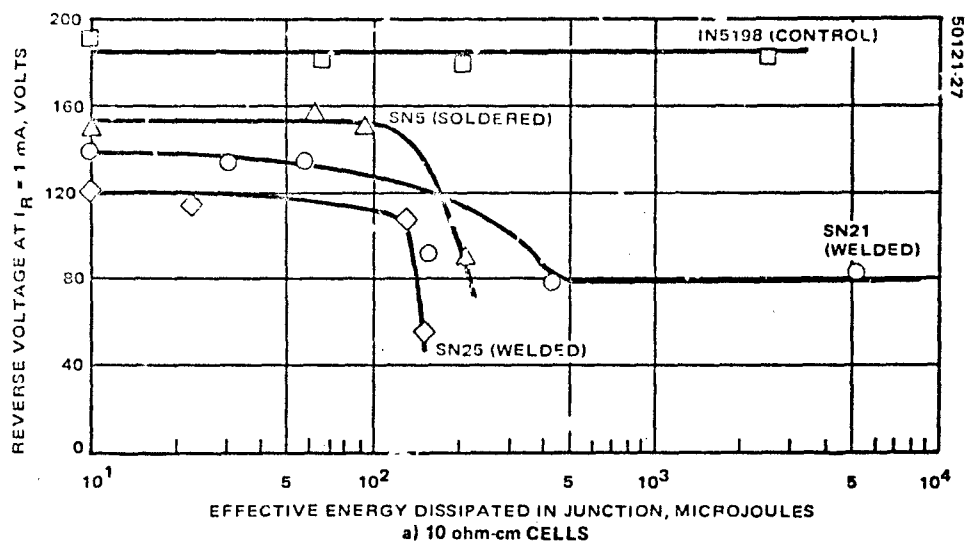


FIGURE 4-8. REVERSE VOLTAGE VERSUS EFFECTIVE ENERGY DISSIPATION IN JUNCTION

TABLE 4-2. LINAC DIRECT ELECTRON EFFECTS UPON
DIODE REVERSE VOLTAGE DROP^a

(Test date: 2-28-74)

Device No.	V_R (V) $I_R = 1$ mA	I_P , A	t_s μ sec	V_D V	E^b μ J
21 (welded)	138			Preburst	
	135	8.0	9.8	0.4	31.4
	134	14.5	8.0	0.5	58.0
	91	13.5	6.6	1.8	160.0
	79	23.0	5.1	3.7	434.0
	81	180.0	3.8	17.0	5,168
25 (welded)	123			Preburst	
	117	8.0	9.7	0.3	23.3
	108	14.0	7.8	1.2	131.0
	56	26.0	6.6	0.9	154.4
IN5198 (control)	187			Preburst	
	182	24.0	2.5	1.1	66.0
	180	44.0	2.0	2.4	211.2
	183	145.0	1.2	14.5	2,523
5 (soldered)	151			Preburst	
	153	8.5	10.0	0.05	4.3
	156	15.0	8.4	0.5	63.0
	150	24.0	6.8	0.6	97.9
	88	46.0	5.2	0.9	215.2

^a 10 ohm-cm cells
Radiation pulse remained constant
 1×10^4 rads; 1×10^{10} rads/sec; 1μ sec
^b $E = I_P V_D t_s$

Results of this test revealed that these diodes were significantly harder than the diodes tested in tests 1 and 2. Table 4-3 presents results of the test. General results of the Heliotek capacity measurements were inconclusive, as presented in program monthly report No. 15.

Test 4 Results

The next set of diodes tested were 20 ohm-cm devices. These diodes, although they started with excellent V_R values prior to irradiation, responded erratically to exposure. Test results are presented in Table 4-4. The erratic behavior of these diodes is readily demonstrated by device 406 which did not degrade after five 45 ampere photocurrent pulses, and device 408 which failed completely after one 45 ampere pulse. This test indicated that the higher resistivity diodes were as sensitive as others to the damage mechanism.

TABLE 4-3. LINAC DIRECT ELECTRON EFFECTS ON
DIODE REVERSE VOLTAGE^a

Test Data	Serial Number	Bias		LINAC Pulse Duration μ sec	Reverse Voltage		Comment
		Voltage	Current		0.2 mA, V	1.0 mA, V	
15 Mar	1	—	—	—	220	240	Initial reading
	1	25.0	11.5	5	165	217	
	1	25.0	25.0	5	164	211	
	1	25.0	46.0	5	139	179	
5 Apr	1	—	—	—	145	196	Initial reading Unbiased Unbiased
	1	—	—	1	144	196	
	1	—	—	1	143	202	
	1	25.0	45.0	1	145	204	
	1	25.0	45.0	1	148	202	
15 Mar	2	—	—	—	160	175	Initial reading Unbiased Unbiased Unbiased
	2	—	—	5	144	168	
	2	—	—	5	141	165	
	2	—	—	5	140	163	
	2	25.0	11.5	5	141	162	
	2	25.0	25.0	5	141	163	
	2	25.0	45.0	5	106	157	
	2	25.0	45.0	5	131	161	
	2	25.0	45.0	5	95	157	
5 Apr	2	—	—	—	103	175	Initial reading
	2	25.0	45.0	1	106	166	
	2	25.0	45.0	1	103	158	
	2	25.0	45.0	1	101	147	
	2	25.0	45.0	1	90	144	
5 Apr	11	—	—	1	154	166	Initial reading Unbiased Unbiased Unbiased Unbiased
	11	—	—	1	149	159	
	11	—	—	1	146	160	
	11	25.0	45.0	1	145	159	
	11	25.0	45.0	1	146	160	
	11	—	—	5	144	157	
	11	—	—	5	144	157	
	11	25.0	45.0	5	144	159	
	11	25.0	45.0	5	145	160	
	11	37.5	62.0	5	144	159	
	11	37.5	62.0	5	146	160	
	11	50.0	90.0	5	100	138	
5 Apr	14	—	—	—	183	199	Initial reading Unbiased Unbiased
	14	—	—	1	193	175	
	14	—	—	1	195	177	
	14	25.0	45.0	1	199	180	
	14	25.0	45.0	1	197	180	

^a15 ohm-cm cells with heavy silicon oxide layer over junction.

Test 5 Results

The last set of diodes exposed at the LINAC were 3 ohm-cm devices. These diodes started with low values of V_R and exhibited little sensitivity to irradiation. These results are presented in Table 4-5. For the condition

TABLE 4-4. LINAC DIRECT ELECTRON EFFECTS ON
20 CHM-CM DIODES
(Test date 6 May 74)

Device No.	Bias		V _R , V		Comments
	Voltage, V	Current, A	0.2 mA	1.0 mA	
401	-	-	246	255	Initial reading
	-	-	245	256	Unbiased
	-	-	242	256	Unbiased
	25	>100	77	105	
402	-	-	242	248	Initial reading
	-	-	242	253	Unbiased
	-	-	235	250	Unbiased
	25	45	100	187	
404	25	45	47	104	
	-	-	218	257	Initial reading
	-	-	216	257	Unbiased
	25	46	213	254	
	25	46	217	254	
	37.5	70	214	254	
405	50	90	205	242	
	25	120	91	137	
	-	-	157	206	Initial reading
406	25	~45	69	120	Five pulses
	-	-	242	248	Initial reading
407	25	~45	239	248	Five pulses
	-	-	221	247	Initial reading
	-	-	118	224	Unbiased
	-	-	116	227	Unbiased
	25	45	101	214	
	25	45	100	203	
408	37.5	65	96	136	
	25	45	123	250	Initial reading. Diode shorted on recovery from photo-current pulse.

representing the HASPS application, these diodes showed negligible damage. However, the V_R level was lower than considered acceptable for use.

FISSION SPECTRUM ELECTRON TEST

Description of Test

The fission spectrum electron test was conducted using the LINAC in the direct electron mode of operation. The diodes were exposed to the direct electrons at levels low enough to keep the absorbed energy to dose rates lower than the minimum dose rates previously observed to cause diode

TABLE 4-5. LINAC DIRECT ELECTRON EFFECTS ON DIODES
(Test date 6 May 74)

Device No.	Bias		V _R V		Comments
	Voltage, V	Current, A	0.2 mA	1.0 mA	
301	—	—	43	69	Initial reading Five pulses
	25	45	45	67	
305	—	—	87	88	Initial reading Unbiased Unbiased
	—	—	87	88	
	—	—	87	88	
	25	45	87	88	
	25	45	87	88	
	37.5	64	67	87	
	37.5	64	75	87	
	50	95	78	87	
	50	95	56	83	
	25	120	40	47	
306	—	—	85	97	Initial reading Unbiased Unbiased
	—	—	84	88	
	—	—	84	88	
	25	45	82	86	
	25	45	83	87	
	37.5	65	82	87	
307	50	80	53	68	Initial reading Unbiased
	—	—	87	88	
	25	45	86	88	
	25	45	84	88	
	37.5	65	84	88	
	50	90	78	87	
	25	120	83	87	

damage. The diodes were exposed while in the unbiased condition. The required fission spectrum electron fluence of 10^{14} electrons/cm² was equated to 1.51×10^{13} 10 MeV electrons/cm² through the use of the Monte Carlo electron transport program BETA II.

Test Results

To attain the required effective 3×10^{15} e/cm² (fission spectrum) at a low dose rate from the LINAC (10 MeV electrons), it was decided to expose the diodes to approximately 28,000 1-μsec wide electron pulses. Final results of V_R measurements after exposure to the required electron fluence showed no degradation.

IR SCANNER TEST

Description of Test

A test was set up to determine if localized junction damage was the cause of the observed V_R degradation. Such damage would be detectable as a localized region of high heat dissipation at the damage when current is forced through a damaged diode under test. An infrared sensitive camera was used to scan the surface of the diode, especially in the vicinity of the p/n junction, to detect any hot spots that may have been present.

Test Results

The test results were inconclusive in that no definite hot spots were observed within the diodes. However, the test did reveal that the edges of the diodes perpendicular to the diode junction consistently ran hotter than the rest of the diode. Problems due to insufficiently accurate control of the scanner as it searched the diode surface prevented achieving the test objective.

UNDERGROUND TEST

The blocking diodes were attached in pairs to 2.5 by 2.5 cm mounts, one with welded interconnects and one with soldered interconnects. Tables 4-6 and 4-7 show the test sample exposure levels and the sample matrix. The total test is reported in UGT No. 3 Test Report, Jan 1975, prepared for AF Aero Propulsion Laboratory, Wright-Patterson AFB. The diodes were coded as shown below.

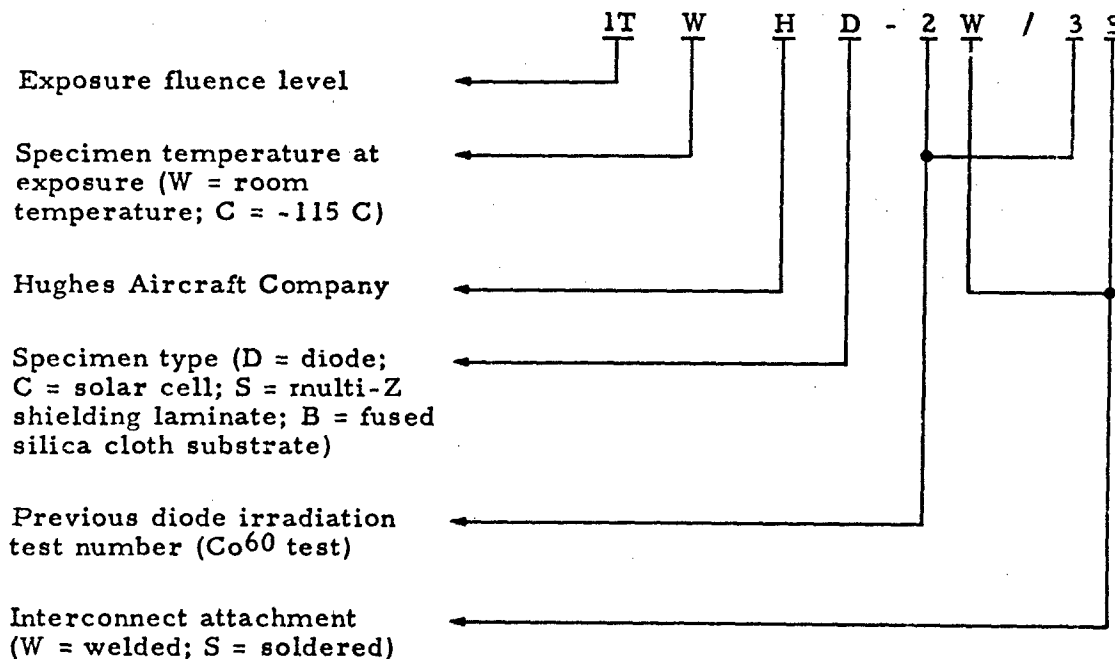


TABLE 4-6. TEST SAMPLE EXPOSURE LEVELS

Item	Exposed		Controls	
	Room Temperature	-115°C	Laboratory	Tunnel
Blocking diodes	3	1	-	-
Solar cells	3	1	-	1
6 mil	3	2	1	-
12 mil	4	-	1	1
Multi-Z shield				
Array substrate	3	-	1	1
With aluminum	2	-	1	1
Without aluminum				

TABLE 4-7. HUGHES SAMPLE MATRIX

Item	Exposure Level												Controls	
	1T			2T			4T			8T				
	Cold	Warm		Cold	Warm		Cold	Warm		Cold	Warm		Laboratory	Tunnel
Blocking diode	-	1TW HD-2W/3S		-	2TW HD-3W/6S		4TC HD-12W/8S	4TW HD-10W/7S		-	-		-	-
Solar cell (high efficiency)	-	1TW HC-3/6		2TC HC-5/6	2TW HC-1/6		-	4TW HC-2/6		-	-		-	T HC-4/6
Multi-Z shield	-	1TW HC-7/12		2TC HC-11/12	2TW HC-8/12		4TC HC-10/12	4TW HC-12/12		-	-		L HC-13/12	T HS-6
Fused silica cloth substrate	-	1TW HS-2		-	2TW HS-3		-	4TW HS-4		-	8TW HS-5		L HS-1	T HS-6
	-	-		-	-		-	4TW HB-1/AI HB-2/AI		-	8TW HB-3/AI		L HB-5/AI	T HB-4/AI
	-	-		-	-		-	4TW HB-6		-	8TW HB-7		L HB-9	T HB-8

All samples incorporated in this test were previously irradiated at the Hughes LINAC or TREF 1590 FXR in a study of junction power dissipation capabilities.

Test Results

As anticipated, the soldered blocking diodes were destroyed through thermomechanical effects. The aluminum, welded technology diodes appeared to have suffered no damage, remaining intact throughout the test.

5. PRODUCTION DIODE

DESCRIPTION

The blocking solar cells were fabricated to the following drawing and specification list (see Appendices B and C).

258665	Blocking Solar Cell, Covered
X3354450	Cover Slide, Blocking Solar Cell
X3286385-1	Blocking Solar Cell
258162	Strip, Interconnection
PS 30964-028	Product Spec., Blocking Solar Cell, Covered
XPS 31456-001	Product Spec., Solar Cell, Aluminum Contact
PS 30660-080	Product Spec., Solar Cell, Bar Contact, Titanium-Silver Contact
PS 30964-025	Product Spec., Cover Slide
258666	Blocking Solar Cell, Covered
X3354450	Cover Slide, Blocking Solar Cell
X3286385-2	Blocking Solar Cell
3205755-1	Strip, Positive End, Solar Cell
PS 30964-028	Product Spec., Blocking Solar Cell, Covered

PERFORMANCE

Production cells were tested for voltage drop, reverse current, and reverse voltage in accordance with TS 30964-026 "System Specification, Qualification and Environmental Test" (Appendix B). These functional tests were conducted on the cells as they were received, and also following burn-in or other tests.

Diode Voltage Drop Test

Purpose

This test was designed to measure the voltage in the forward direction across the device under specified conditions.

Procedure

Using a Tektronix 575 curve tracer, the current sweep was adjusted to obtain forward currents of 0.3 and 3.0 amperes. The forward voltage was read at these specified values of the current. The temperature was held at $25^{\circ} \pm 2^{\circ} \text{C}$. Maximum acceptable voltage readings were:

0.8 volt at 0.3 ampere

1.2 volt at 3.0 amperes

Results

The voltage readings are recorded in Tables 5-1 and 5-2. Table 5-1 gives voltage drop readings and reverse current and voltage readings for all the cells before and after 48 hour burn-in. Cells are listed by lot number, serial number, and type (welded or soldered). Table 5-2 gives this same data for the cells which completed the 168 hour burn-in.

Reverse Current and Reverse Voltage Test

Purpose

This test was designed to measure the voltage and current in the reverse direction through the diode.

Procedure

Using a Tektronix 575 curve tracer, the voltage sweep was adjusted to obtain reverse voltages of 80, 120, and 140 volts. The reverse current was read at these voltages and recorded. Maximum acceptable currents were:

0.1 mA at 80 volts

0.2 mA at 120 volts

1.0 mA at 140 volts

TABLE 5-1. VOLTAGE DROP AND REVERSE CURRENT AND VOLTAGE READING
(48 Hour Burn-in)

Diode Type	Lot No.	Serial No.	V _f at 0.3 A		V _f at 3 A		I _R at 80 V		I _R at 120 V		I _R at 140 V	
			Pre	Post	Pre	Post	Pre	Post	Pre	Post	Pre	Post
Soldered	653	2	0.64	0.65	0.85	0.86	0.01	0.015	0.015	0.015	0.015	0.015
		3	0.67	0.67	1.02	1.02	0.01	0.01	0.01	0.01	0.01	0.01
		4	0.65	0.65	0.88	0.88	0.025	0.03	0.1	0.22	0.1	0.15
		5	0.69	0.69	0.96	0.96	0.001	0.01	0.01	0.01	0.01	0.02
		7	0.64	0.64	0.9	0.84	0.13	0.16	0.16	0.2	0.18	0.32
		8	0.65	0.66	0.88	0.88	0.005	0.01	0.05	0.08	0.07	0.14
		9	0.65	0.64	0.87	0.89	0.02	0.04	0.025	0.04	0.025	0.05
		10	0.66	0.66	0.92	0.92	0.01	0.01	0.01	0.01	0.015	0.015
		11	0.67	0.66	0.92	0.9	0.005	0.1	0.05	0.4	0.6	0.5
		13	0.66	0.66	0.9	0.89	0.005	0.005	0.01	0.005	0.01	0.005
		14	0.66	0.65	0.89	0.89	0.005	0.005	0.005	0.005	0.005	0.005
		15	0.64	0.64	0.89	0.88	0.001	0.001	0.001	0.005	0.005	0.01
		16	0.65	0.65	0.88	0.88	0.01	0.01	0.01	0.01	0.01	0.01
		17	0.65	0.65	0.88	0.88	0.025	0.05	0.03	0.06	0.03	0.06
		18	0.73	0.73	0.97	0.98	0.02	0.02	0.02	0.02	0.02	0.02
		19	0.65	0.65	0.92	0.94	0.01	0.01	0.1	0.03	0.3	0.15
		20	0.67	0.67	0.96	0.97	0.03	0.03	0.2	0.18	0.4	0.5
		24	0.65	0.65	0.87	0.86	0.02	0.025	0.02	0.025	0.02	0.025
		25	0.68	0.67	0.99	0.98	0.1	0.4	0.4	0.8	0.7	1.0 at 132 V
		26	0.65	0.61	0.91	0.88	0.01	0.025	0.18	0.2	0.9 at 136 V	0.9 at 136 V
		37	0.66	0.66	0.98	0.92	0.005	0.005	0.1	0.05	0.6	0.25
		41	0.66	0.66	0.86	0.86	0.005	0.005	0.005	0.005	0.005	0.005
		46	0.66	0.66	0.94	0.94	0.025	0.07	0.2	0.4	0.4	0.6
		47	0.68	0.69	0.89	0.9	0.02	0.01	0.03	0.03	0.05	0.05
		51	0.65	0.64	0.91	0.9	0.14	0.07	0.2	0.16	0.24	0.3
		52	0.64	0.67	0.86	0.94	0.01	0.02	0.02	0.09	0.1	0.12
		53	0.66	0.66	0.96	0.97	0.01	0.015	0.01	0.015	0.01	0.015
		55	0.7	0.7	0.92	0.92	0.001	0.01	0.02	0.01	0.2	0.38
		56	0.65	0.65	0.87	0.88	0.02	0.015	0.04	0.03	0.1	0.18
		57	0.68	0.68	0.88	0.88	0.01	0.01	0.01	0.05	0.01	0.07
		59	0.71	0.69	1.0	0.98	0.05	0.01	0.18	0.08	0.4	0.2
		61	0.65	0.65	0.92	0.92	0.01	0.01	0.02	0.03	0.08	0.08
		62	0.66	0.66	0.91	0.91	0.03	0.04	0.03	0.04	0.03	0.04
		64	0.68	0.68	0.92	0.91	0.03	0.03	0.04	0.03	0.04	0.03
Soldered	653	42	0.63	0.65	0.86	0.94	0.04	0.03	0.1	0.14	0.1	0.18

Table 5-1 (continued)

Diode Type	Lot No.	Serial No.	V_f at 0.3 A		V_f at 3 A		I_R at 80 V		I_R at 120 V		I_R at 140 V	
			Pre	Post	Pre	Post	Pre	Post	Pre	Post	Pre	Post
Soldered	655	1	0.66	0.67	0.96	0.95	0.01	0.01	0.01	0.01	0.07	0.07
		2	0.69	0.68	0.9	0.88	0.01	0.01	0.01	0.01	0.01	0.01
		5	0.67	0.67	1.02	1.02	0.02	0.01	0.03	0.03	0.04	0.04
		6	0.7	0.7	1.0	1.0	0.01	0.02	0.025	0.05	0.02	0.08
		7	0.79	0.79	1.14	1.14	0.01	0.001	0.01	0.001	0.03	0.04
		10	0.64	0.65	0.92	0.92	0.01	0.01	0.1	0.04	0.7	0.7
		12	0.69	0.7	1.08	1.08	0.05	0.03	0.18	0.3	0.3	0.5
		13	0.66	0.66	0.87	0.86	0.01	0.01	0.01	0.01	0.01	0.01
		15	0.68	0.68	1.08	1.08	0.01	0.01	0.015	0.01	0.015	0.01
		16	0.7	0.7	1.1	1.08	0.03	0.03	0.03	0.03	0.03	0.03
		17	0.74	0.73	0.95	0.94	0.01	0.01	0.01	0.01	0.015	0.01
		18	0.71	0.71	0.9	0.9	0.01	0.01	0.015	0.01	0.04	0.1
		19	0.73	0.74	0.94	0.95	0.01	0.01	0.01	0.01	0.05	0.015
		20	0.64	0.64	0.86	0.84	0.01	0.01	0.02	0.01	0.03	0.03
		21	0.72	0.73	1.16	1.16	0.01	0.01	0.01	0.01	0.01	0.01
		22	0.71	0.72	0.92	0.91	0.01	0.01	0.01	0.01	0.01	0.01
Soldered Welded	655	23	0.66	0.67	0.97	0.96	0.01	0.01	0.01	0.01	0.01	0.01
	650	14	0.72	0.7	1.04	0.91	0.015	0.025	0.04	0.05	0.05	0.07
		15	0.76	0.75	1.14	1.06	0.01	0.005	0.03	0.01	0.05	0.03
		16	0.7	0.68	0.94	0.91	0.01	0.015	0.02	0.03	0.03	0.03
	650	18	0.68	0.67	0.94	0.96	0.015	0.01	0.06	0.03	0.11	0.08
	648	1	0.69	0.7	0.95	0.94	0.04	0.04	0.06	0.07	0.1	0.11
		2	0.72	0.7	1.02	0.97	0.06	0.3	0.13	0.3	0.18	0.35
		3	0.68	0.69	0.94	0.94	0.01	0.01	0.01	0.01	0.01	0.015
		4	0.73	0.71	1.0	0.96	0.02	0.03	0.025	0.045	0.03	0.06
	648	5	0.73	0.72	1.04	1.02	0.01	0.01	0.02	0.02	0.02	0.025
	646	1	0.66	0.65	0.95	0.88	0.03	0.05	0.06	0.09	0.07	0.14
		3	0.72	0.71	1.04	0.97	0.015	0.01	0.025	0.015	0.025	0.02
		4	0.63	0.64	0.85	0.9	0.06	0.055	0.1	0.1	0.2	0.2
		6	0.62	0.65	0.84	0.88	0.07	0.06	0.08	0.07	0.11	0.09
		7	0.67	0.65	0.96	0.86	0.015	0.005	0.025	0.01	0.05	0.025
		8	0.66	0.66	1.04	0.97	0.07	0.06	0.18	0.12	0.5	0.2
		9	0.67	0.65	1.04	0.93	0.4	0.58	0.45	0.65	0.5	0.7
		10	0.67	0.63	1.16	0.93	0.03	0.03	0.035	0.04	0.04	0.05
		11	0.69	0.64	1.16	0.9	0.16	0.21	0.18	0.24	0.22	0.27
		12	0.66	0.64	1.2	0.93	0.05	0.06	0.065	0.08	0.075	0.09
		13	0.68	0.64	1.18	0.91	0.01	0.025	0.03	0.03	0.03	0.035
Welded	646	14	0.66	0.64	1.18	0.93	0.06	0.06	0.08	0.12	0.14	0.18

Table 5-1 (continued)

Diode Type	Lot No.	Serial No.	V _f at 0.3 A		V _f at 3 A		I _R at 80 V		I _R at 120 V		I _R at 140 V	
			Pre	Post	Pre	Post	Pre	Post	Pre	Post	Pre	Post
Welded	646	15	0.67	0.65	1.04	0.87	0.01	0.015	0.03	0.025	0.15	0.05
		16	0.63	0.64	0.93	0.97	0.03	0.04	0.035	0.045	0.035	0.05
		17	0.64	0.635	0.9	0.9	0.3	0.24	0.5	0.42	0.65	0.5
		18	0.63	0.64	0.86	0.87	0.015	0.04	0.03	0.06	0.04	0.08
		19	0.77	0.76	1.06	1.04	0.02	0.03	0.03	0.045	0.04	0.065
		20	0.64	0.64	0.88	0.88	0.01	0.02	0.015	0.025	0.02	0.035
		21	0.64	0.64	0.86	0.89	0.1	0.15	0.12	0.18	0.18	0.22
		22	0.64	0.66	0.92	0.93	0.01	0.01	0.02	0.015	0.02	0.02
		23	0.65	0.65	0.88	0.97	0.045	0.045	0.06	0.13	0.08	0.105
		24	0.65	0.65	0.95	0.96	0.03	0.03	0.04	0.05	0.05	0.06
		25	0.64	0.63	0.85	0.85	0.005	0.015	0.01	0.06	0.015	0.065
		26	0.64	0.64	0.84	0.89	0.09	0.11	0.12	0.16	0.14	0.18
		27	0.66	0.66	0.86	0.88	0.04	0.12	0.05	0.13	0.08	0.14
		28	0.69	0.69	0.89	0.91	0.015	0.02	0.04	0.03	0.06	0.05
	660	6	0.63	0.69	0.99	1.04	0.04	0.04	0.05	0.06	0.06	0.075
		10	0.68	0.68	1.02	1.0	0.09	0.07	0.1	0.12	0.1	0.18
		11	0.66	0.68	0.98	1.06	0.11	0.15	0.14	0.2	0.16	0.28
		12	0.67	0.68	0.97	1.06	0.04	0.07	0.05	0.08	0.06	0.1
		13	0.67	0.67	1.02	0.96	0.01	0.025	0.025	0.06	0.05	0.15
		14	0.68	0.68	1.02	0.97	0.005	0.02	0.02	0.06	0.03	0.11
		15	0.66	0.67	1.0	1.0	0.01	0.015	0.02	0.03	0.04	0.07
		17	0.67	0.66	1.04	0.96	0.02	0.02	0.04	0.05	0.04	0.1
		18	0.67	0.68	1.04	1.04	0.06	0.05	0.1	0.1	0.2	0.2
		19	0.69	0.70	1.02	1.16	0.025	0.03	0.04	0.05	0.05	0.07
		20	0.70	0.71	1.1	1.08	0.25	0.16	0.25	0.18	0.25	0.2
		21	0.68	0.69	1.04	0.97	0.02	0.025	0.05	0.12	0.08	0.24
		23	0.66	0.67	1.02	0.98	0.03	0.03	0.04	0.06	0.07	0.08
		25	0.68	0.68	1.08	1.02	0.01	0.05	0.02	0.1	0.03	0.18
		26	0.69	0.68	1.2	0.99	0.04	0.04	0.07	0.08	0.1	0.11
		32	0.68	0.68	1.1	1.08	0.02	0.02	0.04	0.05	0.2	0.1
		33	0.66	0.66	0.96	0.98	0.01	0.015	0.02	0.03	0.04	0.04
		34	0.67	0.68	0.97	1.12	0.005	0.01	0.01	0.01	0.01	0.015
		36	0.68	0.67	1.08	1.04	0.02	0.03	0.03	0.07	0.045	0.12
		37	0.70	0.71	1.14	1.12	0.09	0.07	0.14	0.18	0.18	0.18
		39	0.68	0.68	1.06	0.96	0.015	0.02	0.03	0.04	0.04	0.06
		40	0.69	0.67	1.08	0.99	0.015	0.04	0.02	0.05	0.03	0.06
		42	0.67	0.70	0.98	1.24	0.06	0.1	0.12	0.16	0.14	0.2
		43	0.67	0.68	1.04	1.04	0.005	0.01	0.02	0.02	0.04	0.04
Welded	660	44	0.68	0.69	1.06	1.06	0.045	0.06	0.1	0.14	0.2	0.18

Table 5-1 (continued)

Diode Type	Lot No.	Serial No.	V _f at 0.3 A		V _f at 3 A		I _R at 80 V		I _R at 120 V		I _R at 140 V	
			Pre	Post	Pre	Post	Pre	Post	Pre	Post	Pre	Post
Welded	660	45	0.66	0.66	0.99	0.97	0.1	0.15	0.2	0.5	0.4	0.8
		46	0.66	0.67	1.02	1.0	0.03	0.05	0.09	0.1	0.12	0.12
		47	0.66	0.67	1.0	0.94	0.025	0.04	0.07	0.1	0.12	0.5
		49	0.67	0.67	1.0	0.99	0.03	0.07	0.06	0.14	0.08	0.18
		50	0.67	0.68	1.02	1.04	0.04	0.12	0.08	0.16	0.12	0.24
	660	51	0.66	0.67	0.99	0.99	0.015	0.015	0.02	0.025	0.025	0.03
		668 1	0.77	0.77	1.18	1.2	0.02	0.03	0.03	0.04	0.04	0.05
		3	0.77	0.76	1.18	1.06	0.05	0.05	0.06	0.08	0.12	0.22
	668	4	0.76	0.76	1.12	1.2	0.02	0.04	0.035	0.1	0.055	0.8
		7	0.77	0.76	1.24	1.18	0.03	0.03	0.05	0.08	0.03	0.13
		668 8	0.77	0.77	1.1	1.04	0.015	0.02	0.06	0.1	0.12	0.22
	661	1	0.68	0.68	1.08	1.04	0.005	0.01	0.01	0.01	0.01	0.015
		2	0.66	0.66	0.96	1.0	0.04	0.06	0.1	0.12	0.13	0.16
		4	0.66	0.66	0.92	0.89	0.005	0.01	0.01	0.01	0.01	0.01
	661	6	0.60	0.79	1.18	1.08	0.075	0.05	0.2	0.2	0.3	0.25
		10	0.67	0.68	0.97	1.04	0.04	0.04	0.06	0.06	0.11	0.08
	670	1	0.66	0.66	0.97	0.95	0.03	0.04	0.06	0.06	0.075	0.06
		2	0.72	0.72	1.04	1.04	0.025	0.02	0.05	0.05	0.08	0.07
		4	0.71	0.71	1.18	1.18	0.025	0.02	0.06	0.05	0.08	0.07
	670	5	0.66	0.66	1.0	0.98	0.05	0.03	0.08	0.05	0.09	0.06
		7	0.65	0.65	0.92	0.94	0.025	0.035	0.03	0.045	0.035	0.06
	672	1	0.66	0.66	1.0	1.0	0.03	0.02	0.1	0.06	0.2	0.12
		3	0.68	0.67	1.14	1.02	0.015	0.015	0.04	0.03	0.1	0.05
		4	0.68	0.70	1.02	1.12	0.15	0.04	0.23	0.06	0.3	0.1
	672	5	0.69	0.67	1.2	1.06	0.07	0.015	0.19	0.03	0.25	0.07
		6	0.71	0.72	1.08	1.08	0.025	0.02	0.03	0.03	0.04	0.04
	669	1	0.66	0.66	1.0	1.0	0.08	0.17	0.11	0.2	0.14	0.23
		2	0.67	0.68	0.95	1.1	0.04	0.045	0.09	0.12	0.25	0.2
		3	0.66	0.66	1.0	0.98	0.025	0.025	0.03	0.025	0.035	0.04
		4	0.69	0.69	1.06	1.1	0.035	0.025	0.045	0.03	0.05	0.03
		5	0.65	0.65	0.96	1.0	0.06	0.02	0.11	0.12	0.17	0.2
		6	0.66	0.66	1.02	0.90	0.035	0.025	0.075	0.05	0.11	0.14
		9	0.66	0.66	0.94	0.92	0.015	0.03	0.02	0.04	0.025	0.08
		10	0.66	0.66	1.06	0.96	0.03	0.04	0.06	0.1	0.1	0.15
		11	0.67	0.67	0.97	0.95	0.05	0.025	0.055	0.03	0.06	0.03
Welded	669	13	0.67	0.68	1.02	1.04	0.05	0.04	0.06	0.045	0.07	0.05

Table 5-1 (continued)

Diode Type	Lot No.	Serial No.	V_f at 0.3 A		V_f at 3 A		I_R at 80 V		I_R at 120 V		I_R at 140 V	
			Pre	Post	Pre	Post	Pre	Post	Pre	Post	Pre	Post
Welded	671	3	0.71	0.67	1.24	1.12	0.015	0.01	0.025	0.02	0.03	0.03
		5	0.72	0.71	1.28	1.16	0.01	0.01	0.02	0.02	0.03	0.025
		6	0.66	0.66	1.02	1.02	0.02	0.005	0.04	0.01	0.05	0.01
		7	0.65	0.65	1.0	0.90	0.01	0.02	0.015	0.04	0.02	0.06
		8	0.65	0.64	0.95	0.93	0.01	0.005	0.01	0.01	0.015	0.01
		10	0.68	0.68	1.26	1.16	0.03	0.01	0.05	0.02	0.08	0.05
		11	0.66	0.65	1.04	0.94	0.005	0.005	0.01	0.005	0.015	0.005
		12	0.68	0.71	1.18	1.2	0.005	0.005	0.005	0.01	0.01	0.015
		13	0.66	0.66	1.02	0.91	0.02	0.015	0.03	0.02	0.04	0.01
		14	0.74	0.74	1.04	0.97	0.005	0.005	0.015	0.015	0.02	0.025
	667	5	0.74	0.74	1.2	1.12	0.04	0.08	0.03	0.17	0.11	0.2
		7	0.78	0.77	1.14	1.14	0.01	0.005	0.1	0.1	0.3	0.4
		9	0.72	0.75	1.08	1.16	0.075	0.02	0.1	0.03	0.12	0.03
		10	0.72	0.74	1.02	1.06	0.01	0.01	0.015	0.02	0.02	0.04
		11	0.72	0.72	1.1	1.04	0.02	0.02	0.05	0.04	0.07	0.05
		12	0.77	0.77	1.1	1.1	0.03	0.03	0.04	0.06	0.05	0.75
		13	0.79	0.80	1.12	1.16	0.045	0.03	0.065	0.05	0.075	0.07
		14	0.76	0.75	1.14	1.1	0.03	0.025	0.07	0.09	0.18	0.3
		15	0.76	0.78	1.04	1.1	0.07	0.05	0.11	0.1	0.13	0.12
		16	0.74	0.74	1.04	1.02	0.005	0.01	0.025	0.02	0.03	0.06
	639	1	0.68	0.66	0.97	0.92	0.015	0.02	0.09	0.08	0.25	0.2
		2	0.67	0.66	1.04	0.98	0.03	0.025	0.18	0.08	0.65	0.4
		3	0.68	0.64	1.08	0.85	0.01	0.015	0.06	0.07	0.2	0.14
		5	0.67	0.65	1.0	0.96	0.03	0.03	0.04	0.04	0.04	0.055
		8	0.68	0.64	1.02	0.86	0.02	0.02	0.03	0.02	0.03	0.02
		9	0.67	0.62	0.98	0.9	0.01	0.015	0.04	0.015	0.3	0.02
		10	0.69	0.68	1.06	1.03	0.01	0.015	0.03	0.025	0.1	0.1
		11	0.67	0.65	0.95	0.94	0.04	0.04	0.03	0.16	0.4	0.9
		13	0.63	0.67	0.91	0.97	0.01	0.01	0.06	0.02	0.2	0.025
		14	0.63	0.68	1.02	1.06	0.01	0.005	0.01	0.005	0.04	0.01
		15	0.66	0.64	0.99	0.85	0.005	0.005	0.005	0.01	0.01	0.01
		16	0.66	0.7	0.99	1.16	0.005	0.005	0.02	0.02	0.04	0.1
		18	0.71	0.7	1.08	1.12	0.03	0.02	0.08	0.3	0.4	0.3
		19	0.66	0.66	0.92	0.96	0.03	0.07	0.12	0.25	0.2	0.4
Welded	639	20	0.68	0.66	0.94	0.98	0.03	0.02	0.07	0.4	0.5	0.8

Table 5-1 (continued)

Diode Type	Lot No.	Serial No.	V _f at 0.3 A		V _f at 3 A		I _R at 80 V		I _R at 120 V		I _R at 140 V	
			Pre	Post	Pre	Post	Pre	Post	Pre	Post	Pre	Post
Welded	643	1	0.68	0.66	1.04	1.1	0.02	0.015	0.03	0.03	0.04	0.05
		2	0.7	0.66	1.16	1.04	0.015	0.02	0.04	0.12	0.1	0.4
		3	0.7	0.68	1.16	1.18	0.07	0.075	0.13	0.2	0.3	0.6
		4	0.67	0.66	1.0	1.02	0.015	0.02	0.12	0.15	0.25	0.3
		5	0.66	0.66	0.92	0.92	0.015	0.02	0.19	0.4	1.0 at 136 V	1.0 at 136 V
		6	0.66	0.64	0.9	0.87	0.01	0.01	0.02	0.025	0.1	0.03
		7	0.65	0.64	0.93	0.88	0.01	0.02	0.04	0.04	0.2	0.2
		9	0.67	0.65	0.97	0.94	0.005	0.01	0.02	0.03	0.3	0.3
		10	0.65	0.66	0.9	1.0	0.02	0.03	0.1	0.15	0.4	0.5
		11	0.67	0.64	0.94	0.86	0.02	0.02	0.04	0.04	0.1	0.1
		14	0.66	0.64	0.96	0.92	0.01	0.02	0.02	0.04	0.02	0.1
		15	0.67	0.66	1.04	1.04	0.015	0.015	0.04	0.04	0.1	0.06
		16	0.65	0.65	0.94	0.94	0.03	0.045	0.17	0.5	0.9 at 136 V	1.0 at 136 V
		19	0.66	0.65	0.96	0.92	0.06	0.05	0.06	0.08	0.2	0.14
		20	0.66	0.65	0.95	0.92	0.015	0.015	0.1	0.04	0.4	0.15
		21	0.68	0.66	1.08	1.08	0.01	0.01	0.01	0.02	0.1	0.08
		23	0.65	0.65	0.92	0.88	0.005	0.015	0.01	0.025	0.015	0.03
		24	0.67	0.64	1.02	0.99	0.015	0.02	0.1	0.18	0.25	0.5
		25	0.68	0.68	1.12	1.04	0.022	0.02	0.2	0.3	1.0 at 136 V	1.0 at 132 V
	645	1	0.66	0.69	0.94	0.96	0.01	0.01	0.02	0.02	0.02	0.02
		2	0.68	0.68	0.89	0.96	0.01	0.025	0.13	0.03	0.9	0.25
		3	0.68	0.65	0.94	0.86	0.02	0.06	0.15	0.16	0.9	0.3
		4 ^a	0.68		1.0		0.045		0.6		1.0 at 124 V	
		5	0.74	0.73	1.1	1.0	0.01	0.01	0.3	0.02	0.9 at 136 V	0.06
		6	0.76	0.74	1.08	1.06	0.025	0.03	0.06	0.08	0.1	0.13
		8	0.74	0.7	1.2	1.02	0.02	0.01	0.03	0.02	0.05	0.055
		9	0.76	0.73	1.1	1.02	0.02	0.025	0.03	0.04	0.06	0.08
		10	0.73	0.71	1.04	0.98	0.005	0.01	0.02	0.025	0.1	0.03
		12	0.76	0.73	1.06	1.04	0.01	0.015	0.01	0.02	0.01	0.03
		14	0.73	0.73	1.08	1.1	0.01	0.02	0.03	0.04	0.15	0.1
		15	0.73	0.71	1.04	1.0	0.07	0.08	0.1	0.12	0.3	0.2
Welded	645	16	0.7	0.68	1.12	1.02	0.01	0.015	0.02	0.02	0.1	0.1
		17	0.68	0.64	0.96	0.91	0.01	0.03	0.02	0.04	0.01	0.06

^a Cover cracked so not burned in.

Table 5-1 (continued)

Diode Type	Lot No.	Serial No.	V_f at 0.3 A		V_f at 3 A		I_R at 80 V		I_R at 120 V		I_R at 140 V	
			Pre	Post	Pre	Post	Pre	Post	Pre	Post	Pre	Post
Welded	645	18	0.68	0.67	1.08	1.04	0.04	0.025	0.08	0.08	0.2	0.2
		19	0.69	0.68	0.94	0.94	0.13	0.2	0.36	0.3	0.65	0.6
		20	0.7	0.67	0.98	0.86	0.005	0.02	0.02	0.04	0.2	0.1
		21	0.73	0.69	1.0	0.96	0.05	0.05	0.08	0.08	0.1	0.13
		22	0.69	0.66	0.91	0.86	0.01	0.02	0.04	0.03	0.7	0.45
Welded	645	23	0.65	0.64	0.91	0.88	0.11	0.2	0.22	0.5	0.5	0.6
Soldered	657	1	0.64	0.64	0.86	0.88	0.005	0.02	0.01	0.12	0.01	0.3
		2	0.65	0.64	0.86	0.86	0.015	0.02	0.02	0.17	0.05	0.24
		3	0.64	0.65	0.82	0.83	0.02	0.02	0.02	0.02	0.06	0.08
		4	0.65	0.64	0.84	0.9	0.01	0.015	0.01	0.015	0.015	0.015
		5	0.64	0.64	0.84	0.84	0.02	0.02	0.11	0.11	0.15	0.15
		6	0.65	0.64	0.84	0.84	0.01	0.015	0.1	0.015	0.2	0.05
		7	0.64	0.64	0.84	0.86	0.02	0.03	0.07	0.08	0.11	0.2
		8	0.64	0.65	0.83	0.84	0.01	0.01	0.1	0.15	0.5	0.25
		9	0.64	0.65	0.86	0.9	0.025	0.03	0.03	0.03	0.03	0.03
		10	0.65	0.65	0.84	0.84	0.02	0.02	0.02	0.02	0.02	0.02
		11	0.64	0.65	0.84	0.84	0.005	0.01	0.005	0.01	0.01	0.01
		12	0.65	0.64	0.86	0.88	0.01	0.015	0.01	0.015	0.015	0.015
		13	0.64	0.66	0.86	0.88	0.005	0.01	0.005	0.01	0.005	0.01
		14	0.64	0.64	0.84	0.84	0.005	0.005	0.005	0.005	0.005	0.005
		15	0.64	0.64	0.82	0.83	0.005	0.01	0.01	0.1	0.01	0.12
		16 ^a	0.66		0.89		0.01		0.01		0.01	
		17	0.64	0.65	0.84	0.84	0.05	0.04	0.08	0.04	0.4	0.04
		18	0.63	0.64	0.85	0.86	0.01	0.01	0.01	0.01	0.05	0.06
		19	0.65	0.66	0.83	0.84	0.01	0.01	0.04	0.03	0.08	0.1
		20	0.64	0.65	0.81	0.82	0.02	0.02	0.1	0.02	0.22	0.18
		21	0.64	0.65	0.84	0.86	0.01	0.01	0.01	0.01	0.015	0.01
		22	0.66	0.65	0.94	0.94	0.01	0.01	0.025	0.01	0.15	0.03
		25	0.64	0.65	0.84	0.85	0.01	0.01	0.015	0.07	0.3	0.5
		26	0.64	0.66	0.86	0.87	0.01	0.005	0.01	0.005	0.01	0.005
		27	0.65	0.66	0.85	0.86	0.01	0.005	0.01	0.005	0.01	0.005
		28	0.64	0.64	0.84	0.85	0.01	0.01	0.03	0.1	0.06	0.15
		29	0.65	0.65	0.85	0.86	0.01	0.01	0.02	0.02	0.09	0.08
		30	0.64	0.65	0.88	0.88	0.01	0.005	0.01	0.05	0.02	0.12
		32	0.64	0.65	0.82	0.82	0.01	0.01	0.01	0.02	0.01	0.08
Soldered	657	33	0.64	0.64	0.86	0.87	0.01	0.01	0.015	0.2	0.22	0.3

^aCover cracked so not burned in.

Table 5-1 (continued)

Diode Type	Lot No.	Serial No.	V_f at 0.3 A		V_f at 3 A		I_R at 80 V		I_R at 120 V		I_R at 140 V	
			Pre	Post	Pre	Post	Pre	Post	Pre	Post	Pre	Post
Soldered ↓	657 ↓	34	0.64	0.65	0.87	0.88	0.01	0.01	0.01	0.01	0.01	0.01
		35	0.64	0.64	0.86	0.86	0.01	0.005	0.01	0.005	0.01	0.005
		37	0.64	0.65	0.86	0.86	0.015	0.01	0.02	0.01	0.02	0.01
		38	0.63	0.64	0.81	0.82	0.02	0.02	0.02	0.02	0.02	0.02
		39	0.65	0.65	0.84	0.85	0.02	0.015	0.02	0.015	0.02	0.015
		40	0.64	0.65	0.87	0.86	0.015	0.02	0.02	0.02	0.02	0.02
		41	0.65	0.65	0.9	0.9	0.01	0.01	0.01	0.01	0.01	0.01
		42	0.64	0.63	0.84	0.84	0.01	0.005	0.01	0.005	0.01	0.005
		43	0.66	0.65	0.83	0.84	0.015	0.02	0.015	0.02	0.02	0.02
		657 44	0.64	0.65	0.86	0.86	0.005	0.01	0.005	0.01	0.005	0.01
Soldered	567	45	0.64	0.64	0.84	0.85	0.01	0.01	0.01	0.01	0.01	0.01

Results

Results are recorded in Tables 5-1 and 5-2, along with the voltage drop results.

Reverse Recovery Time Test

Purpose

The purpose of this test is to measure the reverse recovery time by observing the reverse transient current through a specified load resistance on switching from a specified forward bias to a specified reverse bias.

Procedure

Adjust V_1 and R_1 for a forward diode current of 1.5 amperes.
Adjust R_2 and V_2 for a reverse current of 4 amperes with the diode shorted.
Read the reverse recovery time, t_{rr} , on the oscilloscope.

Summary

Forward current = 1.5 amperes

Temperature = $25^\circ \pm 2^\circ \text{C}$

t_{rr} $\leq 3 \mu\text{sec}$

Results

Test results are shown in Table 5-3.

TABLE 5-2. VOLTAGE DROP AND REVERSE CURRENT AND VOLTAGE READING
(168 Hour Burn-in)

Diode Type	Lot No.	Serial No.	V _f at 0.3 A		V _f at 3 A		I _R at 80 V		I _R at 120 V		I _R at 140 V		
			Pre	Post	Pre	Post	Pre	Post	Pre	Post	Pre	Post	
Soldered	653	3	0.67	0.65	1.02	0.88	0.01	0.01	0.01	0.01	0.01	0.7	
		10	0.66	0.64	0.92	0.88	0.01	0.015	0.01	0.015	0.015	0.015	
		14	0.65	0.65	0.89	0.9	0.005	0.002	0.005	0.002	0.005	0.002	
		15	0.64	0.66	0.88	0.90	0.001	0.002	0.005	0.004	0.01	0.01	
		17	0.65	0.66	0.88	0.88	0.05	0.03	0.06	0.03	0.06	0.035	
		18	0.73	0.73	0.98	0.96	0.02	0.02	0.02	0.03	0.02	0.03	
		24	0.65	0.66	0.86	0.88	0.025	0.03	0.025	0.03	0.025	0.03	
		42	0.65	0.66	0.94	0.94	0.03	0.01	0.14	0.05	0.18	0.14	
		53	0.66	0.66	0.97	0.94	0.015	0.01	0.015	0.01	0.015	0.01	
		55	0.7	0.7	0.92	0.92	0.01	0.07	0.01	0.2	0.38	0.5	
	653	56	0.65	0.66	0.88	0.86	0.015	0.02	0.03	0.1	0.18	0.22	
		62	0.66	0.66	0.91	0.92	0.04	0.04	0.04	0.04	0.04	0.045	
		655	2	0.68	0.70	0.88	0.89	0.01	0.005	0.01	0.005	0.01	0.005
			7	0.79	0.78	1.14	1.1	0.001	0.005	0.001	0.005	0.04	0.06
			10	0.65	0.66	0.92	0.94	0.01	0.005	0.04	0.05	0.7	0.3
	13		0.66	0.66	0.86	0.86	0.01	0.01	0.01	0.01	0.01	0.04	
	15		0.68	0.68	1.08	1.06	0.01	0.005	0.01	0.005	0.01	0.005	
	655	18	0.71	0.64	0.9	0.86	0.01	0.015	0.01	0.015	0.1	0.015	
		19	0.74	0.74	0.95	0.95	0.01	0.01	0.01	0.01	0.015	0.015	
		657	1	0.64	0.66	0.88	0.87	0.02	0.07	0.12	0.2	0.3	0.5
			3	0.65	0.65	0.83	0.84	0.02	0.015	0.02	0.02	0.08	0.09
			4	0.64	0.65	0.9	0.86	0.015	0.01	0.015	0.01	0.015	0.01
	9		0.65	0.66	0.9	0.89	0.03	0.05	0.03	0.05	0.03	0.05	
	10		0.65	0.64	0.84	0.85	0.02	0.025	0.02	0.03	0.02	0.03	
	657	6	0.64	0.66	0.84	0.85	0.015	0.01	0.015	0.01	0.05	0.3	
		7	0.64	0.65	0.86	0.86	0.03	0.04	0.08	0.11	0.2	0.18	
		11	0.65	0.66	0.84	0.85	0.01	0.005	0.01	0.005	0.01	0.005	
		14	0.64	0.64	0.84	0.84	0.005	0.005	0.005	0.005	0.005	0.005	
		17	0.65	0.64	0.84	0.85	0.04	0.04	0.04	0.05	0.04	0.05	
		18	0.64	0.65	0.86	0.87	0.01	0.01	0.01	0.01	0.06	0.015	
		20	0.65	0.65	0.82	0.84	0.02	0.015	0.02	0.02	0.18	0.3	
		21	0.65	0.66	0.86	0.86	0.01	0.01	0.01	0.01	0.01	0.01	
		22	0.65	0.66	0.94	0.94	0.01	0.01	0.01	0.015	0.03	0.04	
		25	0.65	0.65	0.85	0.86	0.01	0.005	0.07	0.09	0.5	0.5	
	Soldered	657	26	0.66	0.66	0.87	0.87	0.005	0.005	0.005	0.005	0.005	0.005
			28	0.64	0.65	0.85	0.86	0.01	0.01	0.1	0.12	0.15	0.5

Table 5-2 (continued)

Diode Type	Lot No.	Serial No.	V _f at 0.3 A		V _f at 3 A		I _R at 80 V		I _R at 120 V		I _R at 140 V			
			Pre	Post	Pre	Post	Pre	Post	Pre	Post	Pre	Post		
Soldered	657	29	0.65	0.66	0.86	0.94	0.01	0.01	0.02	0.01	0.08	0.09		
		30	0.65	0.64	0.88	0.87	0.005	0.005	0.05	0.005	0.12	0.05		
		32	0.65	0.65	0.82	0.84	0.01	0.005	0.02	0.02	0.08	0.05		
		33	0.64	0.64	0.87	0.86	0.01	0.02	0.2	0.04	0.3	0.4		
		34	0.65	0.65	0.83	0.83	0.01	0.005	0.01	0.005	0.01	0.005		
		35	0.64	0.65	0.86	0.88	0.005	0.002	0.005	0.004	0.005	0.005		
		37	0.65	0.66	0.86	0.88	0.01	0.005	0.01	0.005	0.01	0.005		
		38	0.64	0.66	0.82	0.85	0.02	0.015	0.02	0.015	0.02	0.015		
		39	0.65	0.66	0.85	0.87	0.015	0.01	0.015	0.01	0.015	0.01		
		40	0.65	0.66	0.86	0.88	0.02	0.015	0.02	0.015	0.02	0.015		
		42	0.63	0.64	0.84	0.85	0.005	0.02	0.005	0.02	0.005	0.025		
		43	0.65	0.66	0.84	0.86	0.02	0.02	0.02	0.02	0.02	0.025		
Soldered Welded	639	44	0.65	0.64	0.86	0.84	0.01	0.005	0.01	0.005	0.01	0.005		
		45	0.64	0.65	0.85	0.84	0.01	0.01	0.01	0.01	0.01	0.01		
		3	0.64	0.66	0.85	0.94	0.015	0.005	0.07	0.025	0.14	0.07		
		5	0.65	0.68	0.96	0.98	0.03	0.015	0.04	0.04	0.055	0.7		
		8	0.64	0.67	0.86	0.94	0.02	0.02	0.02	0.04	0.02	0.18		
		9	0.62	0.69	0.9	1.04	0.015	0.005	0.015	0.025	0.02	0.2		
		10	0.68	0.70	1.03	1.06	0.015	0.01	0.025	0.03	0.1	0.04		
		14	0.68	0.68	1.06	1.02	0.005	0.01	0.005	0.01	0.01	0.25		
		15	0.64	0.65	0.85	0.92	0.005	0.005	0.01	0.005	0.01	0.005		
		639	16	0.7	0.66	1.16	0.97	0.005	0.01	0.02	0.2*	0.1	1.1 at 130 V	
		Welded	643	1	0.66	0.68	1.1	1.1	0.015	0.02	0.03	0.03	0.05	0.05
				2	0.66	0.69	1.04	1.1	0.02	0.03	0.12	0.14	0.4	0.32
4	0.66			0.66	1.02	1.0	0.02	0.015	0.15	0.09	0.3	0.26		
7	0.64			0.67	0.88	0.94	0.02	0.05	0.04	0.09	0.2	0.14		
9	0.65			0.66	0.94	1.02	0.01	0.005	0.03	0.1	0.3	0.7		
10	0.66			0.68	1.0	1.1	0.03	0.02	0.15	0.1	0.5	0.5		
11	0.64			0.65	0.86	0.92	0.02	0.02	0.04	0.06	0.1	0.11		
14	0.64			0.68	0.92	0.95	0.02	0.025	0.04	0.05	0.1	0.15		
15	0.66			0.66	1.04	1.04	0.015	0.04	0.04	0.2 ^a	0.06	1.4 at 124 V		
20	0.65			0.66	0.92	0.90	0.015	0.01	0.04	0.03	0.15	0.5		
643	21			0.66	0.68	1.08	1.04	0.01	0.01	0.02	0.03	0.08	0.11	

^a Cover cracked so not burned in.

Table 5-2 (continued)

Diode Type	Lot No.	Serial No.	V _f at 0.3 A		V _f at 3 A		I _R at 80 V		I _R at 120 V		I _R at 140 V		
			Pre	Post	Pre	Post	Pre	Post	Pre	Post	Pre	Post	
Welded	645	1	0.69	0.70	0.96	0.96	0.01	0.01	0.02	0.01	0.02	0.1	
		5	0.73	0.74	1.0	1.1	0.01	0.01	0.02	0.3	0.06	0.9	
		8	0.7	0.72	1.02	1.0	0.01	0.015	0.02	0.02	0.055	0.05	
		9	0.73	0.76	1.02	1.06	0.025	0.02	0.04	0.08	0.08	0.18	
		10	0.71	0.72	0.98	1.02	0.01	0.01	0.25	0.03	0.03	0.03	
		12	0.73	0.76	1.04	1.1	0.015	0.005	0.02	0.015	0.03	0.02	
		15	0.71	0.73	1.0	1.04	0.08	0.08	0.12	0.16	0.2	0.25	
		16	0.68	0.7	1.02	1.04	0.015	0.01	0.02	0.02	0.1	0.1	
		17	0.64	0.68	0.91	1.04	0.03	0.015	0.04	0.02	0.06	0.04	
		21	0.69	0.71	0.96	0.96	0.05	0.03	0.08	0.06	0.13	0.1	
	646	1	0.65	0.66	0.88	0.88	0.05	0.05	0.09	0.12	0.14	0.22	
		3	0.71	0.71	0.97	1.02	0.01	0.005	0.015	0.01	0.02	0.02	
		4	0.64	0.66	0.9	0.88	0.055	0.035	0.1	0.06	0.2	0.12	
		6	0.65	0.70	0.88	0.93	0.06	0.07	0.07	0.08	0.09	0.1	
		10	0.63	0.68	0.93	0.96	0.03	0.025	0.04	0.03	0.05	0.03	
		13	0.64	0.66	0.91	1.04	0.025	0.005	0.03	0.015	0.035	0.03	
		14	0.64	0.67	0.93	0.92	0.06	0.09	0.12	0.16	0.18	0.3	
		18	0.64	0.65	0.87	0.88	0.04	0.04	0.06	0.2	0.08	0.5	
		20	0.64	0.65	0.88	0.88	0.02	0.02	0.025	0.03	0.035	0.03	
		22	0.66	0.66	0.93	0.93	0.01	0.01	0.015	0.18	0.02	0.8	
		19	0.76	0.78	1.04	1.16	0.03	0.06	0.045	0.18	0.065	0.6	
		24	0.65	0.66	0.96	1.04	0.03	0.025	0.05	0.03	0.06	0.04	
	646	28	0.69	0.72	0.91	0.95	0.02	0.02	0.03	0.16	0.05	0.9	
		648	1	0.7	0.70	0.94	0.95	0.04	0.04	0.07	0.09	0.11	0.12
			3	0.69	0.68	0.94	0.9	0.01	0.01	0.01	0.1	0.015	0.24
	648	4	0.71	0.72	0.96	1.0	0.3	0.2	0.045	0.04	0.06	0.2	
		5	0.72	0.74	1.02	1.08	0.01	0.005	0.02	0.01	0.025	0.015	
	650	14	0.7	0.71	0.91	0.95	0.025	0.02	0.05	0.18	0.07	0.7	
		15	0.75	0.77	1.06	1.06	0.005	0.005	0.01	0.005	0.03	0.01	
		16	0.68	0.68	0.91	0.9	0.015	0.02	0.03	0.03	0.03	0.5	
Welded	650	18	0.67	0.68	0.96	0.9	0.01	0.005	0.03	0.03	0.08	0.07	

TABLE 5-3. REVERSE RECOVERY TIME PER PARA 4.3

Lot No.	Serial No.	t_{rr} , μ sec	Lot No.	Serial No.	t_{rr} , μ sec
653	7	1.8	667	4	2.0
	13	1.6		5	2.0
	20	1.2		7	3.2
	24	1.6		9	1.2
657	25	1.4		10	1.6
	28	1.4		12	1.6
	30	1.2		13	1.4
	45	1.6		14	1.2
655	5	1.2		15	2.2
	7	1.1		16	2.2
	10	1.0	600	6	1.2
668	4	1.4		18	1.2
	8	1.8		23	1.2
660	36	1.2		37	1.0
	2	2.8		40	1.2
670	7	1.6	672	4	1.6
			661	1	1.8
				4	2.0

PRODUCTION DIODE PROBLEMS

The only major manufacturing problem experienced during diode fabrication was with welding. Welds of consistent strength could not be accomplished. A comparison of the pull strength of welded and soldered assemblies is shown in Table 5-4. The inconsistency of the welded samples is very apparent. In addition to the inconsistency in pull strength, it was also found that considerable difficulty was encountered in welding to the P+ back surface. The P+ process used resulted in a very rough surface. Attempting to weld to this surface resulted in problems varying from the tool sticking to the weld to no contact at all between the tab and diode. The vendor also experienced mechanical damage to the diodes during welding. These welding problems caused the production yield to drop to an unacceptably low level, and Heliotek suggested that an additional development phase was required to produce a satisfactory welded diode within the cost objective for the program. After some consideration, a decision was made to reduce the deliverable quantity of cells and to recommend additional welding development in a later phase of this program.

TABLE 5-4. PULL TEST INTERCONNECT (MECHANICAL)

Serial No.	P-Contact Pull Test, gm							N-Bar Pull Test, gm						
	Tab							Tab						
	1	2	3	4	5	6	7	1	2	3	4	5	6	7
<u>Welded</u>														
4	0	0	80	110	60	50	0	0	90	0	0	160	120	0
7	70	80	180	120	120	90	80	50	110	160	110	140	150	0
21	80	140	210	120	170	120	70	110	130	85	a	170	170	110
24	90	60	80	120	100	50	10	30	200	110	120	140	110	80
28	0	30	70	110	50	40	65	20	0	a	30	150	150	110
<u>Soldered</u>														
1	920	215	250	200	340	640		610	610	610	200	190	250	
2	600	220	235	280	190	675		510	510	190	130	240	670	
3	500	285	300	225	210	840		530	530	310	230	170	600	

a Diode cracked at weld

6. QUALIFICATION AND ENVIRONMENTAL TESTS

The qualification testing of the cells was performed at both the cell vendor and at Hughes Aircraft Company, while the environmental testing of the cell coupons was performed at Hughes Aircraft Company. All testing was governed by TS 30964-026 "System Specification, Qualification and Environmental Test, Reverse Current Blocking Diodes For Flexible Solar Array Protection." Tests performed are listed below:

Qualification

Type Approval

Temperature and Humidity

Thermal Shock

High Temperature Vacuum

Vibration

Endurance

Environmental

Mechanical Pull

Roll Up

Temperature Cycling Test

TYPE APPROVAL TESTS

Temperature and Humidity Test

Purpose

This test was performed for the purpose of evaluating the performance of the diode after long term exposure to a combined high temperature, high humidity environment.

Procedure

The test specimens were placed in a sealed test chamber and the temperature and humidity raised to $45^{\circ} \pm 5^{\circ}\text{C}$ and 95 ± 5 percent relative humidity. The test specimens were exposed to this environment for 96 hours. At the end of this period, visual examination and the functional tests were conducted.

Thermal Shock

Purpose of Test

This test was performed to evaluate the ability of the diode to withstand a rapid temperature change between high and low temperature operating limits.

Procedure

The diodes were subjected to five temperature cycles at a minimum thermal rate of 30°C per minute between the extremes of $90^{\circ} \pm 10^{\circ}\text{C}$ and $-196^{\circ} \pm 10^{\circ}\text{C}$. The diodes remained at the extremes for 1 hour. Visual examination and the functional tests were then conducted.

High Temperature/Vacuum Test

Purpose of Test

This test was performed to evaluate the combined environments of high temperature and vacuum on the diode performance.

Procedure

The diodes were placed in a test chamber reduced in pressure to a vacuum of at least 10^{-5} Torr. The temperature was raised to $140^{\circ} \pm 10^{\circ}\text{C}$. The diodes remained in the chamber for 168 hours. At the end of this period, the diodes were allowed to return to room ambient temperature and pressure. The diodes with silver-titanium contacts were then removed, and the test was repeated for the diodes with aluminum contacts, except that the temperature was raised to 200°C and the test conditions maintained for 1 hour prior to the 168 hour test. At the end of this period, the diodes returned to room ambient temperature and pressure. All diodes were visually inspected and electrically tested.

The Type Approval Test data and results are shown in Table 6-1.

TABLE 6-1. TYPE APPROVAL TEST DATA AND RESULTS **hellotek**

NO. 021802

DATE 6/6/74

TYPE APPROVAL TEST

PAGE 7

ELECTRICAL TEST DETAIL SHEET

Lot # See Below

TAT Para. 4.5

Test TEMP-HUMIDITY

P/N 258665

Tested by 

Checked by ER

Date of Test 10/10/74
10/16/74

PRE-TEST

POST-TEST

Cell No.	V_F ① 0.3A	V_F ① 3.0A	V_F ① 0.3A	V_F ① 3.0A
670-8	0.65	0.78	0.65	0.84
667-8	0.77	1.0	0.77	0.97
671-4	0.70	0.78	0.64	0.76
668-5	0.82	1.1	0.82	1.0
667-1	0.81	1.1	0.81	1.0
667-2	0.85	1.1	0.85	1.0
667-18	0.88	1.1	0.81	0.96
661-13	0.87	1.2	0.83	1.0
660-41	0.65	0.79	0.65	0.79
660-31	0.65	0.91*	0.65	0.78

*Probable instrumentation/reading error

V_F = Forward Voltage

Table 6-1 (continued)

hplclak

NO. 021802

DATE 6/6/74

TYPE APPROVAL TEST

PAGE 8

ELECTRICAL TEST DETAIL SHEET

Lot # See Below

Tested by



TAT Para. 4.5

P/N 258665

Checked by

ER

Test TEMP-HUMIDITY

10/10/74

Date of Test 10/16/74

PRE-TEST

POST-TEST

Cell No.	I_R (mA)	I_R (mA)	I_R (mA)	I_R (mA)
	@ 120 V_R	@ 140 V_R	@ 120 V_R	@ 140 V_R
670-8	0.13	0.25	0.3	0.4
667-8	.09	.3	.12	.22
671-4	.09	.05	.2	.25
668-5	.1	.5	.3	0
667-1	.15	.2	.3	.32
667-2	< .1	< .1	.1	.1
667-18	.1	.15	.15	.2
661-13	.1	.2	.12	.2
660-41	< .1	< .1	.02	.05
660-31	.1	.5	.25	.7

 I_R = Reverse Current

Table 6-1 (continued)

hellotekNO. 021802DATE 6/6/74

TYPE APPROVAL TEST

PAGE 7

ELECTRICAL TEST DETAIL SHEET

Lot # See BelowTAT Para. 4.6Test THERMAL SHOCK

P/N 258665

Tested by Checked by E RDate of Test 10/16/74
11/1/74

Cell No.	V_F	V_F	V_F	V_F
	@ 0.3A	@ 3.0A	@ 0.3A	@ 3.0A
670-8	0.65	0.84	0.86*	0.83
667-8	0.77	0.97	0.78	0.99
671-4	0.64	0.76	0.64	0.77
668-5	0.82	1.0	0.82	0.99
667-1	0.81	1.0	0.81	0.99
667-2	0.85	1.0	0.84	0.99
667-18	0.81	0.96	0.81	0.98
661-13	0.83	1.0	0.83	0.98
660-41	0.65	0.79	0.64	0.74
660-31	0.65	0.78	0.65	0.78

*Probable recording error (see Hi Temp-Vac data)

 V_F = Forward Voltage

Table 6-1 (continued)

heliotekNO. 021802DATE 6/6/74

TYPE APPROVAL TEST

PAGE 8

ELECTRICAL TEST DETAIL SHEET

Lot # See BelowTAT Para. 4.6

P/N 258665

Tested by Checked by EJPTest THERMAL SHOCKDate of Test: 10/16/74
11/1/74

PRE-TEST

POST-TEST

Cell No.	I_R (mA)	I_R (mA)	I_R (mA)	I_R (mA)
	@ 120 V_R	@ 140 V_R	@ 120 V_R	@ 140 V_R
670-8	.3	.4	.2	.25
667-8	.12	.22	.15	.15
671-4	.2	.25	.1	.1
668-5	.3	0	.4	.9
667-1	.3	.32	.15	.2
667-2	.1	.1	*	*
667-18	.15	.2	.2	.3
661-13	.12	.2	.2	.3
660-41	.02	.05	.1	.2
660-31	.25	.7	.15	.7

*No reading obtained (unit shorted)

 I_R = Reverse Current

Table 6-1 (continued)

hellek

NO. 021802

DATE 6/6/74

TYPE APPROVAL TEST

PAGE 7

ELECTRICAL TEST DETAIL SHEET

Lot # See Below

Tested by 

TAT Para. 4.7

P/N 258665

Checked by ER

Test HI TEMP. VAC.

Date of Test 11/1/74
11/21/74

PRE-TEST

POST-TEST

Cell No.	V_F @ 0.3A	V_F @ 3.0A	V_F @ 0.3A	V_F @ 3.0A
670-8	0.86*	0.83	0.65	0.75
667-8	0.78	0.99	0.78	0.98
671-4	0.64	0.77	0.64	0.77
668-5	0.82	0.99	0.83	1.0
667-1	0.81	0.99	0.59*	1.0
667-2	0.84	0.99	0.84	1.0
667-18	0.81	0.98	0.81	0.98
661-13	0.83	0.98	0.84	1.1
660-41	0.64	0.74	0.65	0.79
660-31	0.65	0.78	0.65	0.79

*Probable recording error (see Thermal Shock data)

V_F = Forward Voltage

Table 6-1 (continued)

hellotek

NO. 021802

DATE 6/6/74

TYPE APPROVAL TEST

PAGE 8

ELECTRICAL TEST DETAIL SHEET

Lot # See Below

Tested by

TAT Para. 4.7

P/N 258665

Checked by *ER*

Test HI-TEMP. VAC.

Date of Test 11/1/74
11/21/74

PRE-TEST

POST-TEST

Cell No.	I_R (mA)	I_R (mA)	I_R (mA)	I_R (mA)
	① 120 V_R	② 140 V_R	③ 120 V_R	④ 140 V_R
670-8	.2	.25	.1	.4
667-8	.15	.15	.4	> 1
671-4	.1	.1	< .1	.4
668-5	.4	.9	.3	.1
667-1	.15	.2	< .1	.2
667-2	*	*	*	*
667-18	.2	.3	< .2	< .1
661-13	.2	.3	< .1	.2
660-41	.1	.2	< .1	.3
660-31	.15	.7	< .2	> 1

*No reading obtained (unit shorted)

 I_R = Reverse Current

Table 6-1 (continued)

hellotek

NO. 021802

DATE 6/6/74

TYPE APPROVAL TEST

PAGE 7

ELECTRICAL TEST DETAIL SHEET

Lot # 673

Tested by 

TAT Para. 4.5

P/N 258666

Checked by 

Test TEMP-HUMIDITY

Date of Test 10/10/74
10/16/74

PRE-TEST

POST-TEST

Cell No.	V_F @ 0.3A	V_F @ 3.0A	V_F @ 0.3A	V_F @ 3.0A
3	.65	.77	.65	.73
4	.66	.82	.66	.81
6	.65	.78	.64	.77
7	.67	.84	.67	.84
8	.71	.96	.71	.96
9	.66	.81	.65	.80
10	.66	.83	.66	.82
11	.65	.80	.65	.77
12	.66	.80	.66	.80
14	.65	.79	.65	.79

 V_F = Forward Voltage

Table 6-1 (continued)

hellotek

NO. 021802

DATE 6/6/74

TYPE APPROVAL TEST

PAGE 8

ELECTRICAL TEST DETAIL SHEET

Lot # 673

Tested by (3)

TAT para. 4.5

P/N 258666

Checked by EP

Test TEMP-HUMIDITY

Date of Test 10/10/74
10/16/74

PRE-TEST

POST-TEST

Cell No.	I_R (mA) @ 120 V_R	I_R (mA) @ 140 V_R	I_R (mA) @ 120 V_R	I_R (mA) @ 140 V_R
3	< .1	< .1	< .1	.25
4	.2	.2	.2	.2
6	< .1	< .1	< .1	< .1
7	< .1	.1	< .1	.2
8	< .1	.3	.2	.5
9	.2	.4	.2	.5
10	< .1	< .1	< .1	< .1
11	< .1	< .1	< .1	< .1
12	< .1	.1	.2	.3
14	< .1	< .1	< .1	.2

I_R = Reverse Current

Table 6-1 (continued)

heliotek

NO. 021862

DATE 6/6/74

TYPE APPROVAL TEST

PAGE 7

ELECTRICAL TEST DETAIL SHEET

Lot # 673

Tested by

TAT Para. 4,6

P/N 258666

Checked by

Test THERMAL SHOCK

10/16/74
Date of Test 11/1/74

PRE-TEST

PCST-TEST

Cell No.	V_F @ 0.3A	V_F @ 3.0A	V_F @ 0.3A	V_F @ 3.0A
3	.65	.73	.65	.73
4	.66	.81	.66	.81
6	.64	.77	.64	.77
7	.67	.84	.65	.85
8	.71	.96	.70	.96
9	.65	.80	.65	.81
10	.66	.82	.66	.83
11	.65	.77	.65	.74
12	.66	.80	.66	.80
14	.65	.79	.65	.81

 V_F = Forward Voltage

Table 6-1 (continued)

hellotek

NO. 021802

DATE 6/6/74

TYPE APPROVAL TEST

PAGE 8

ELECTRICAL TEST DETAIL SHEET

Lot # 673

TAT Para. 4.6

Ttest THERMAL SHOCK

P/N 25866

Tested by

Checked by ER

Date of Test 10/16/74
11/1/74

PRE-TEST

POST-TEST

Cell No.	I_R (mA)	I_R (mA)	I_R (mA)	I_R (mA)
	@ 120 V_R	@ 140 V_R	@ 120 V_R	@ 140 V_R
3	<.1	.25	.1	.4
4	.2	.2	.2	.3
6	<.1	<.1	.1	.1
7	<.1	.2	.2	.2
8	.2	.5	.3	.6
9	.2	.5	.3	.7
10	<.1	<.1	.1	.3
11	<.1	<.1	.1	.1
12	.2	.3	.4	1.0
14	<.1	.2	.5	.7

 I_R = Reverse Current

Table 6-1 (continued)

hellotek

NO. 021892

DATE 6/6/74

TYPE APPROVAL TEST

PAGE 7

ELECTRICAL TEST DETAIL SHEET

Lot # 673

Tested by 

TAT Para. 4.7

P/N 258666

Checked by 

Test HI-TEMP. VAC.

Date of Test 11/1/74
11/21/74

PRE-TEST

POST-TEST

Cell No.	V_F	V_F	V_F	V_F
	<u>0.3A</u>	<u>3.0A</u>	<u>0.3A</u>	<u>3.0A</u>
3	.65	.73	.66	.78
4	.66	.81	.66	.82
6	.64	.77	.65	.78
7	.65	.85	.67	.85
8	.70	.96	.71	.96
9	.65	.81	.66	.81
10	.66	.83	.67	.83
11	.65	.74	.65	.81
12	.66	.80	.66	.81
14	.65	.81	.65	.80

V_F = Forward Voltage

Table 6-1 (continued)

hellotek

NO. 021802

DATE 6/6/74

TYPE APPROVAL TEST

PAGE 8

ELECTRICAL TEST DETAIL SHEET

Lot # 673

Tested by 

TAT Para. 4,7

Checked by FR

Test HI-TEMP. VAC.

11/1/74

Date of Test 11/21/74

PRE-TEST

POST-TEST

Cell No.	I_R (mA)	I_R (mA)	I_R (mA)	I_R (mA)
	@ 120 V_R	@ 140 V_R	@ 120 V_R	@ 140 V_R
3	.1	.4	.2	> .1
4	.2	.3	< .1	< .1
6	.1	.1	< .1	< .1
7	.2	.2	.2	< .1
8	.3	.6	.4	> .1
9	.3	.7	.4	< .1
10	.1	.3	< .1	.2
11	.1	.1	< .1	< .1
12	.4	1.0	> 1	> 1
14	.5	.7	.6	.8

I_R = Reverse Current

Summary and Conclusions

Twenty blocking solar cells (10 each, P/N 258776, Rev. D, and P/N 258666, Rev. C) were subjected to the following environmental tests in accordance with Heliotek Type Approval Test Procedure 021802, Rev. A.

- 1) Temperature and humidity
- 2) Thermal shock
- 3) High temperature-vacuum

No significant degradation was observed in forward voltage characteristics for the cells as a result of these tests.

No significant degradation was observed in reverse current characteristics for the cells as a result of these tests, with the following exceptions:

Three each of the P/N 258665 cells (S/N 667-8, 668-5, and 660-31) and the P/N 258666 cells (S/N 673-8, -9, and -14) showed minor changes in reverse current characteristics as a result of these tests.

Two cells (P/N 258665, S/N 667-2 and P/N 258666, S/N 673-12) both failed as a result of thermal shock testing.

VIBRATION TEST

Purpose

The vibration test was performed to determine the effect of two differently oriented vibrations on the component parts.

Procedure

The test was conducted using two HASP type substrates wound on a vibration test mandrel. The substrates are panels approximately 10 feet in length and 8 inches wide on which are bonded a number of solar cells in groups plus some dummy cells. The blocking diodes were interconnected to the live solar cell arrays and bonded to the substrate per XPS 31456-011. The complete arrangement and location of the diodes is shown in Figure 6-1.

The substrate was wound on the vibration test mandrel with a tension of 2.3 pounds. Figure 6-2 shows the direction of the wrap with respect to the load orientation.

The test mandrel with panels was vibrated for 3 minutes in two differently oriented directions. The vibration frequency was a nominal 50 cps with a nominal peak acceleration of 20 g. Following the vibration, electrical tests, as specified in paragraph 4.1 and 4.2 of the test specification were performed. The results are shown in Tables 6-2 and 6-3.

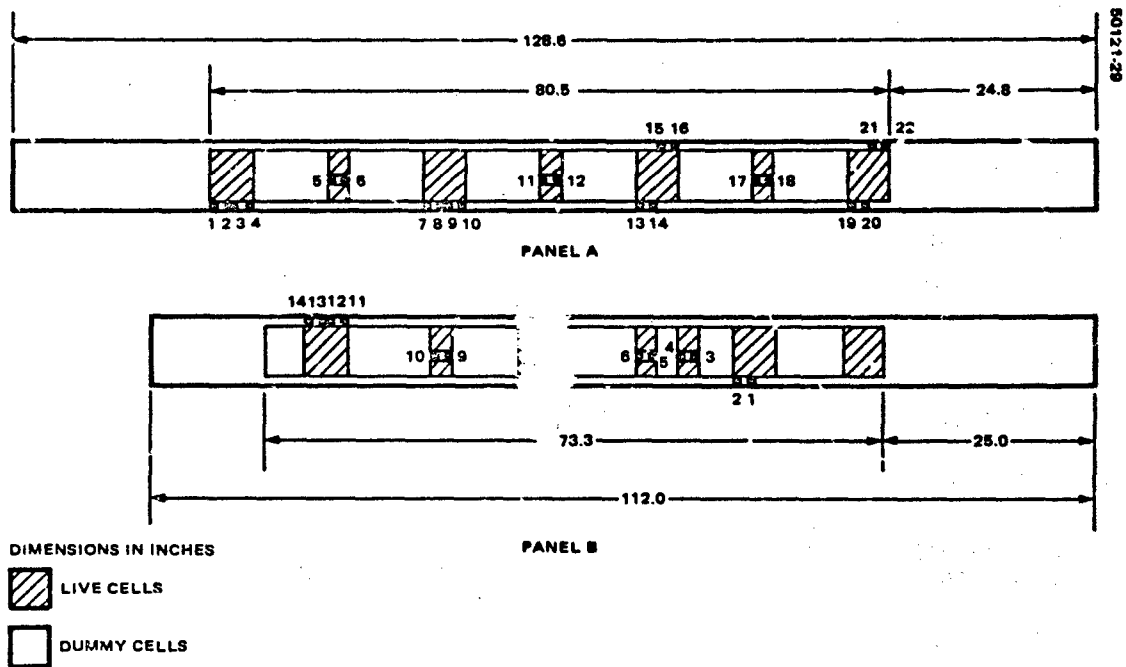


FIGURE 6-1. DIODE ARRANGEMENT AND LOCATION

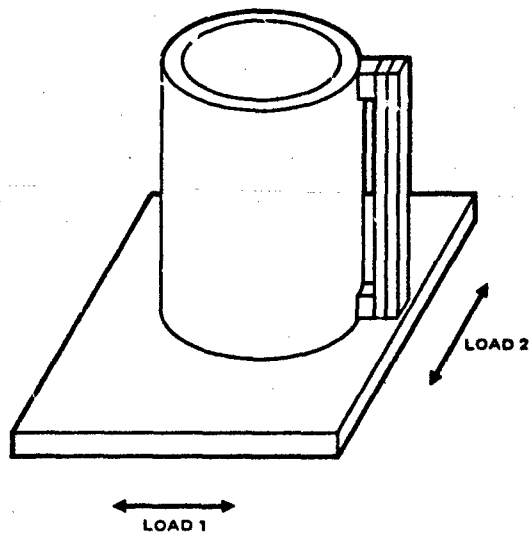


FIGURE 6-2. VIBRATION LOADS

TABLE 6-2. ELECTRICAL DATA PRE AND POST VIBRATION TEST, PANEL A

Diode Type	Lot No.	Serial No.	V _f at 0.3 A		V _f at 5 A		I _R at 80 V		I _R at 120 V		I _R at 140 V		Position on Panel Diagram (see Figure 6-1)
			Pre	Post	Pre	Post	Pre	Post	Pre	Post	Pre	Post	
Soldered	653	8	0.66	0.28	0.91	0.94	0.005	0.005	0.005	0.02	0.2	0.15	12
	655	1	0.67	0.69	1.02	1.04	0.005	0.005	0.005	0.005	0.2	0.18	11
		23	0.68	0.69	1.02	1.06	0.005	0.005	0.01	0.005	0.015	0.01	5
	657	8	0.65	0.66	0.9	0.93	0.005	0.02	0.5	0.5	1.0 at 130 V	1.0 at 130 V	18
Welded		27	0.66	0.66	0.91	0.92	0.005	0.005	0.01	0.005	0.02	0.005	6
		41	0.65	0.66	0.94	0.96	0.005	0.02	0.01	0.025	0.01	0.025	17
	639	18	0.73	0.74	1.2	1.24	0.05	0.06	0.3	0.3	0.7	0.8	4
		19	0.67	0.67	0.95	0.97	0.04	0.05	0.12	0.14	0.3	0.15	21
	643	5	0.66	0.67	0.95	0.95	0.02	0.02	0.06	0.06	0.2	0.1	15
		16	0.68	0.68	1.0	1.04	0.03	0.03	0.6	0.6	0.9 at 132 V	0.9 at 132 V	16
	645	2	0.68	0.69	1.0	1.02	0.03	0.04	0.11	0.06	0.3	0.1	20
		19	0.68	0.69	0.99	1.06	0.45	0.45	0.9	0.85	1.0 at 128 V	1.0 at 128 V	22
	646	11	0.66	0.67	0.98	0.98	0.2	0.3	0.25	0.3	0.3	0.35	2
		17	0.66	0.66	0.98	0.98	0.25	0.25	0.4	0.4	0.5	0.5	7
		18	0.67	0.67	1.02	1.04	0.07	0.07	0.14	0.14	0.2	0.16	13
		21	0.65	0.66	0.96	0.98	0.4	0.5	0.5	0.6	0.6	0.7	1
		23	0.66	0.66	0.97	0.95	0.06	0.08	0.1	0.12	0.12	0.14	14
		26	0.65	0.66	0.94	0.96	0.12	0.12	0.15	0.16	0.18	0.2	19
	639	27	0.67	0.68	0.98	1.0	0.03	0.05	0.04	0.06	0.05	0.07	10
		1	0.66	0.67	0.94	0.96	0.015	0.02	0.07	0.07	0.17	0.17	9
		20	0.68	0.68	1.04	1.04	0.02	0.02	0.05	0.035	0.1	0.06	8
	645	23	0.66	0.66	0.94	0.99	0.12	0.25	0.4	0.5	0.6	0.6	3

TABLE 6-3. ELECTRICAL DATA PRE AND POST VIBRATION TEST PANEL B

Diode Type	Lot No.	Serial No.	V _f at 0.3 A		V _f at 3 A		I _R at 80 V		I _R at 120 V		I _R at 140 V		Position on Panel Diagram (see Figure 5-1)
			Pre	Post	Pre	Post	Pre	Post	Pre	Post	Pre	Post	
Soldered	653	9	0.77	0.78	1.08	1.12	0.01	0.05	0.025	0.02	0.06	0.03	12
		26	0.70	0.71	0.94	0.97	0.015	0.02	0.06	0.07	0.14	0.16	5
		47	0.72	0.72	1.24	1.26	0.08	0.08	0.3	0.3	0.8	0.8	7
	655	16	0.67	0.68	1.0	1.06	0.06	0.015	0.1	0.04	0.2	0.03	8
		657	0.72	0.73	1.08	1.08	0.005	0.005	0.01	0.015	0.02	0.02	11
Welded	639	13	0.71	0.72	1.14	1.18	0.05	0.04	0.06	0.045	0.06	0.05	6
		2	0.65	0.66	0.91	0.95	0.04	0.035	0.05	0.04	0.05	0.045	10
		11	0.74	0.75	1.04	1.1	0.005	0.04	0.2	0.18	0.7	0.5	1
	643	3	0.65	0.65	0.32	0.94	0.01	0.005	0.1	0.05	0.5	0.5	9
		25	0.72	0.74	1.04	1.04	0.005	0.005	0.03	0.005	0.2	0.01	2
	650	10	0.66	0.67	0.93	0.95	0.005	0.005	0.06	0.06	0.16	0.16	4
		11	0.65	0.66	0.94	0.96	0.02	0.015	0.2	0.1	0.9 at 136 V	0.9 at 136 V	3
		12	0.69	0.70	1.18	1.12	0.03	0.03	0.2	0.03	0.75	0.9 at 136 V	14
		13	0.68	0.68	1.08	1.04	0.04	0.04	0.18	0.16	0.5	0.6	13

Visual inspection revealed two small cracks on diode 14 on Panel B after vibration, and a small crack plus a corner chip on diode 4 on Panel A. Diode 4 sustained a small chip in the corner after the first roll-up before vibration. After vibration the crack had propagated, causing a broken corner, and a second small crack had formed.

Conclusion

The small cracks on diode 14 of Panel B did not affect the electrical performance in any way. They appear to be in the cover slide only. The chip and cracks on diode 4 of Panel A likewise did not change the electrical performance. The small crack resulting from the roll-up acted as a notch, and apparently triggered the chipping. Since this test was a severe one (qualification level) amounting to a 50 percent overtest, the minor cracks in the cover slides are not surprising.

ENDURANCE TEST

Purpose of Test

This test was performed to determine the effects of a 1000 hour burn-in on the electrical characteristics of the diodes when subjected to the specified conditions.

Procedure

The blocking cells were subjected to a 1000 hour burn-in test where a maximum current of 3 amperes was passed through each device while the device temperature was maintained at 95°C. Changes in the electrical characteristics as a function of time were monitored and evaluated.

Results

The results are shown in Table 6-4.

These results show that all diodes functioned satisfactorily after running for 1000 hours at high temperature (95°C) and high forward current (3 amperes). There were, however, changes in performance resulting from this exposure which should eventually be evaluated. Presently, however, this evaluation is considered beyond the scope of the current contract.

MECHANICAL PULL TEST

Purpose of Test

This test was performed to verify that a flight configured interconnect and cell combination has sufficient mechanical pull strength.

TABLE 6-4. ENDURANCE TEST SUMMARY

Serial No.	Reverse Characteristics					Forward Characteristics				
	V_R at 0.2 mA					V_F at 0.3 A				
	Pre	Post	Percent	Pre	Post	Pre	Post	Percent	Pre	Post
<u>Welded</u>										
2	122	130	6.6	136	142	0.67	0.66	-1.5	0.79	0.81
6	116	130	12.1	130	144	0.67	0.66	-1.5	0.78	0.82
8	104	108	3.8	124	124	0.67	0.66	-1.5	0.78	0.82
15	128	132	3.1	140	146	0.67	0.66	-1.5	0.9	0.82
17	128	120	-6.3	142	140	0.68	0.67	-1.5	0.78	0.82
28	114	113	3.5	124	134	0.68	0.67	-1.5	0.83	0.82
29	84	70	-16.7	128	120	0.67	0.66	-1.5	0.95	0.81
<u>Soldered</u>										
101	110	160	45.5	142	190	0.68	0.67	-1.5	0.77	0.80
104	116	164	41.4	130	180	0.68	0.67	-1.5	0.78	0.80
105	108	142	31.5	120	157	0.68	0.66	-2.9	0.76	0.81
107	122	144	18.0	132	170	0.68	0.67	-1.5	0.76	0.81
108	108	138	17.8	122	144	0.68	0.66	-2.9	0.77	0.80
109	120	172	43.3	128	196	0.68	0.67	-1.5	0.78	0.80
111	116	136	17.2	132	146	0.68	0.67	-1.5	0.73	0.82
112	172	>200	-	200	>200	0.68	0.67	-1.5	0.78	0.81

Procedure

The interconnect material was attached to the cell by weld or solder. After the connection was made, the interconnect material was slit into 100 mil wide sections. Each sector was tested on a Unitek Micropul Model 6-092-03 pull tester. The cell was clamped to the tester frame and the interconnect sector was clamped to the pull tester arm. The pull force in grams was recorded when the sector failed. These data are shown in Table 6-5.

The data showed that the welded cells were unsatisfactory, and led to the welding evaluation and corrective action as described in the previous section.

Subsequently, a pull test was conducted on three more cells using the same procedure. These results are shown in Table 6-6.

ROLL-UP TEST

Purpose of Test

This test was designed to verify that the diode, as connected in a typical array configuration, will be capable of withstanding a large number of roll-up operations.

Procedure

The vibration test machine and one panel were used to perform this test. The panel with the diodes bonded on was loaded in the series cell direction and rolled with the cells facing away from the roller. A load of 0.77 pound was applied to the panel, and the panel was rolled-up, or cycled, 500 times. The cells were electrically tested per 4.1 and 4.2 both before and after the roll-ups. The results are shown in Table 6-7. The visual inspection revealed no damage to the diodes as a result of the roll-ups.

TEMPERATURE CYCLING TESTS

Purpose of Test

This test was designed to verify the integrity of the interconnected diode under simulated temperature cycling.

Procedure

A temperature cycling test consisting of 1000 temperature cycles was conducted on two of the flexible panel segments. The test was run with

TABLE 6-5. PULL TEST INTERCONNECT (MECHANICAL)

Serial No.	P-Contact Pull Test, gm							N-Bar Pull Test, gm						
	Tab							Tab						
	1	2	3	4	5	6	7	1	2	3	4	5	6	7
<u>Welded</u>														
4	0	0	50	110	60	50	0	0	90	0	0	160	120	0
7	70	80	180	120	120	90	80	50	110	160	110	140	150	0
21	80	140	210	120	170	120	70	110	130	95	-- ^a	170	170	110
24	90	60	80	120	100	50	10	30	200	110	120	140	110	80
28	0	30	70	110	50	40	65	20	0	-- ^a	30	150	150	110
<u>Soldered</u>														
1	920	215	250	200	340	840		610	610	610	200	190	250	
2	600	220	235	280	190	675		510	510	190	130	240	670	
3	500	285	300	225	210	840		530	530	310	230	170	600	

^a Diode cracked at weld

TABLE 6-6. SUMMARY INTERCONNECT
(MECHANICAL) PULL TEST

Serial No.	P-Contact Pull Test, gm							N-Bar Pull Test, gm						
	Tab							Tab						
	1	2	3	4	5	6	7	1	2	3	4	5	6	7
Welded														
660/20	250	170	160	190	165	220	a	140	180	205	190	215	190	
660/45	160	180	250	210	150	230		190	160	160	195	175	180	
669/1	170	170	180	240	200	165	b	Off in cutting						100

^a Filter cracked at 220

^b Filter cracked at 24

TABLE 6-7. ROLL UP TEST DATA

Diode Type	Lot No.	Serial No.	V _f at 0.3 A		V _f at 3 A		I _R at 80 V		I _R at 120 V		I _R at 140 V	
			Pre	Post	Pre	Post	Pre	Post	Pre	Post	Pre	Post
Soldered	657	41	0.66	0.68	0.96	1.04	0.02	0.01	0.025	0.01	0.025	0.01
		8	0.66	0.66	0.93	0.93	0.02	0.005	0.5	0.5	1.0 at 130 V	1.1 at 130 V
Welded	646	26	0.66	0.70	0.96	1.04	0.12	0.12	0.16	0.16	0.2	0.2
		2	0.69	0.69	1.02	1.06	0.04	0.03	0.06	0.14	0.1	0.3
	645	19	0.69	0.70	1.06	1.08	0.45	0.4	0.85	0.8	1.0 at 128 V	1.1 at 130 V
		19	0.67	0.68	0.97	1.12	0.05	0.025	0.14	0.14	0.15	0.3

the Hughes Automatic Temperature Cycling Tester. The test consisted of thermal cycling the two flexible panel segments between $-196^{\circ} \pm 10^{\circ} \text{C}$ to $+90^{\circ} \pm 10^{\circ} \text{C}$. After every 200 cycles, the blocking diodes were subjected to a visual inspection and functional tests per paragraphs 4.1 and 4.2 of TS30964-026.

The electrical data are shown in Table 6-8.

TABLE 6-8. ELECTRICAL DATA FROM THERMAL CYCLE TEST
TEMPERATURE CYCLING TEST PER PARAGRAPH 6.4

Number of Cycles	Diode Type	Serial No.	V_f at 0.3 A	V_f at 3 A	I_R at 80 V	I_R at 120 V	I_R at 140 V
0	Welded	1	0.78	1.12	0.045	0.1	0.1
		2	0.80	1.18	0.005	0.02	0.025
	Soldered	3	0.64	0.82	0.02	0.03	0.03
		4	0.70	0.88	0.05	0.18	0.5
210	Welded	1	0.78	1.16	0.005	0.01	0.75
		2	0.82	1.36	0.01	0.01	0.09
	Soldered	3	0.66	0.84	0.02	0.5	0.6 at 124 V
		4	0.72	0.98	0.06	0.2	0.5
574	Welded	1	0.73	1.04	0.01	0.02	0.03
		2	0.79	1.12	0.004	0.004	0.004
	Soldered	3	0.64	0.85	0.02	0.03	0.03
		4	0.70	0.88	0.05	0.18	0.40
800	Welded	1	0.78	1.28	0.025	0.075	0.6
		2	0.81	1.3	0.005	0.01	0.01
	Soldered	3	0.65	0.86	0.015	0.015	0.015
		4	0.70	0.88	0.04	0.19	0.5
1000	Welded	1	0.74	1.1	0.05	0.1	0.2
		2	0.81	1.18	0.01	0.015	0.015
	Soldered	3	0.65	0.86	0.07	0.3	0.5
		4	0.70	0.91	0.05	0.15	0.9

7. CONCLUSIONS AND RECOMMENDATIONS

The work on this program has succeeded in developing a process for fabricating flat pack panel mounted diodes suitable for use on flexible solar panels. The diode junction is diffused into a 1 by 2 cm, 8 mil thick, P doped silicon blank. Although having a slightly higher base resistivity, the blank is identical to that which is used for conventional solar cells. The nominal electrical diode characteristics of forward and reverse voltage and reverse recovery time are suitable for panels such as HASPS and other 28 volt nominal systems. Approximately 350 production lot and evaluation diodes with both soldered and welded interconnects, complete with second surface mirror covers for thermal control, were fabricated and subjected to a comprehensive series of tests to determine their performance. These tests included electrical, environmental, radiation, and endurance. With minor exceptions, the diodes performed within specification limits after all environmental exposures. Two problems which require further development and test were discovered during the program. The first, which arose during manufacturing, was related to the process of welding the interconnect tabs to the diode contacts. The diode vendor was unable to perform this welding operation with acceptable repeatability or pull strength. It should be emphasized that this welding problem is not unique to these diodes, since welding of aluminum interconnects is a new technology which is still in the development phase.

The second problem was determined during the test sequences. The diode, although operating within specification limits after test exposure, showed larger changes in reverse leakage characteristics as a result of test sequences than is considered acceptable in conventional diodes. This may be a characteristic of this type of device or may be eliminated by additional development work. The particular environments for which diode leakage characteristic changes were observed were prompt ionizing radiation, endurance, and thermal cycling. Because of the welding difficulty and reverse voltage sensitivity, the diode was not completely qualified for flight use as had been initially intended. For full qualification status, an additional development and test program is required as recommended below.

MANUFACTURING

- 1) Increase the diode blank thickness to provide greater strength and easier handling.

- 2) Resolve the welding problem by investigating other welding methods; in particular, seam welding. Investigate processes for making the P+ surface more uniform, thereby providing a more compatible surface for welding.
- 3) Investigate a junction coating process less porous than the silicon oxide which is currently used to protect the mesa junction.
- 4) Investigate role of base resistivity in diode stability. More sophisticated techniques can be utilized to determine final base resistivity

TEST AND ANALYSIS

- 1) Radiation. Perform additional radiation testing and analysis to fully identify and understand the actual mechanism by which prompt ionizing radiation affects diode performance.
- 2) Reverse Voltage Stability. Determine the cause of changes in reverse characteristics produced by various test exposures. Confirm that stable characteristics can be obtained by process improvements such as improved junction coating.
- 3) Repeat the formal qualification tests on 20 diodes of each type.

APPENDIX A. MANUFACTURING CONTROL DOCUMENT

Hughes Aircraft Company
P.O. 04-706462-LT1

heliotek

A Division of  Inc.

PAGE 1

MANUFACTURING
CONTROL
DOCUMENT

NO 021592

DATE 12/26/73

HBD
HUGHES BLOCKING DIODE

APPROVED BY

A. J. Peters
A. Peters
Project Manager

APPROVED BY

H. Chamberlain
H. Chamberlain, Mgr.
Quality Assurance

REV.	DATE	BY	REVISION DESCRIPTION	APPROVED

101

PRECEDING PAGE BLANK



SPEC. NO. 021592

MANUFACTURING
CONTROL DOCUMENT

DATE 12/26/73

PAGE 2

1.0 SCOPE

This Manufacturing Control Document identifies the processes, procedures and inspection documents used for the manufacture of the blocking diode per the requirements of HAC Specification XDS30964-022.

2.0 DOCUMENTS

2.1 Heliotek Process Specifications

Table I lists Heliotek processes used on this program.

2.2 Heliotek Inspection Documents

Table II lists Heliotek inspection documents to be used on this program.

2.3 Product/Process Flow Charts.

Pages 5 and 6 of this document present the flow charts with referenced specifications.

3.0 QUALITY ASSURANCE PROVISIONS

3.1 Processing

Quality Assurance inspection shall be as detailed in the procedures.

3.2 Testing

Testing shall be as required by the development engineer and per the Acceptance Test Procedure.

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CONTROL DOCUMENTPAGE 3

TABLE I. PROCESS PROCEDURES

<u>Number</u>	<u>Revision</u>	<u>Title</u>
911-001	A	Crystal Growing
911-002	N/C	Mechanical Processing
911-003	B	Diffusion
911-006	N/C	Application of Antireflection Coating
911-008	A	Tape Pull Test
911-011	N/C	Electrical Testing
911-016	N/C	Back Etching (PROPRIETARY)
911-020	N/C	Removal of Antireflection Coating from Contact Area
911-030	N/C	Aluminum P ⁺ Evaporation
911-036	N/C	Mesa Mask
911-037	N/C	Mesa Etch
911-029	N/C	Clean for P ⁺ Deposition

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TABLE II INSPECTION DOCUMENTS

<u>Number</u>	<u>Revision</u>	<u>Title</u>
021326	N/C	Acceptance Test Procedure, HS-350, Solar Cells, Job No. 4140
021328	N/C	Resistivity Measurement and Sectioning Inspection
021329	N/C	Slab Inspection
021330	N/C	Silicon Slice Inspection
021331	N/C	Diffusion Furnace Temperature Surveillance
021332	N/C	Sheet Resistance Surveillance
021333	N/C	Tape Control Procedure
021334	N/C	Contacting Inspection
021335	N/C	Mechanical Inspection, Unfiltered Solar Cells
021336	N/C	Electrical Testing
021337	N/C	Mechanical Inspection, Filtered Solar Cells
021390	N/C	Acceptance Test Procedure

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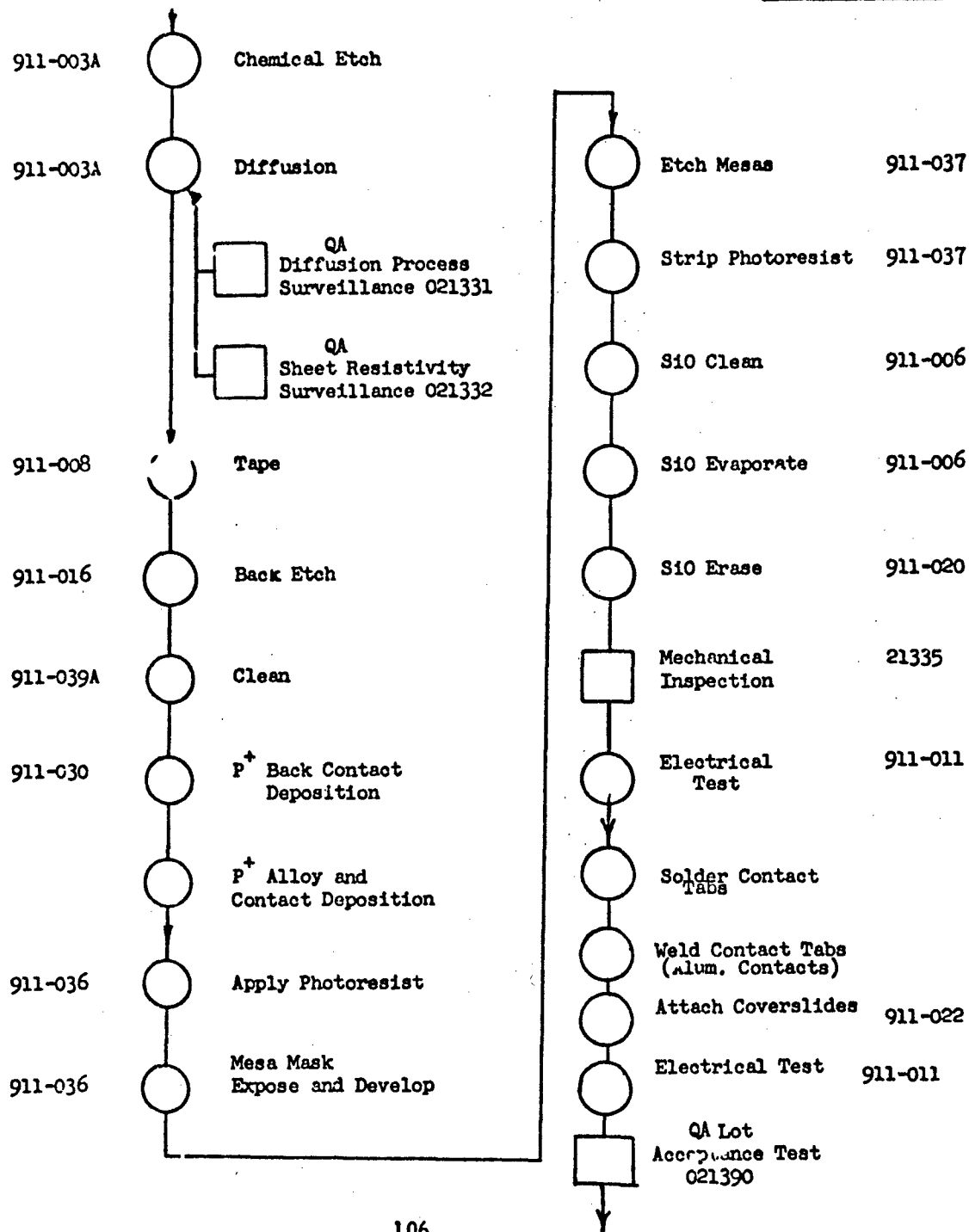


Diffusion and Final Processing

SPEC. NO. 021592

DATE 12/26/73

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APPENDIX B. DIODE SPECIFICATIONS

HUGHESHUGHES AIRCRAFT COMPANY
CULVER CITY CALIFORNIA**TITLE**PRODUCT SPECIFICATION
BLOCKING SOLAR CELL,
COVERED

PS 30964-028

NUMBER

CODE IDENT NO. 83377

Total Pgs 13

A
REV LTRRELEASED PRINT
RESPONSIBLE ENGINEERING ACTIVITY

REA ORG CODE 41-15-20

A
REV7-17-74
REL DATENR
REL BY

INITIAL APPROVALS	DATE	REV LTR	DATE	APPROVAL		
PREPARED		H	9-17-74	NR	SEE DCN	177390
CHECKED <i>[Signature]</i>	1/25/74					
APPROVED <i>[Signature]</i>	1/25/74					

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PRODUCT SPECIFICATION,
BLOCKING SOLAR CELL,
COVERED

HUGHES AIRCRAFT CO.
CULVER CITY, CALIF.
CODE IDENT NO. 82577

1

SH NO.

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REV LTR

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1.0 SCOPE

This specification covers the requirements for a blocking solar cell of a type used on spacecraft solar panel assemblies.

1.1 Design Requirements - The blocking solar cell shall be designed to meet all requirements specified herein, in accordance with the following relative priority list:

- a) Reliability
- b) Electrical performance characteristics including nuclear and natural radiation resistance.
- c) Structural characteristics such as strength and weldability/solderability.
- d) Thermal characteristics
- e) Weight

1.2 Conflicting Requirements - Conflicting requirements arising between this specification and any other specification or drawing listed herein shall be referred in writing to Hughes Aircraft Company (HAC) for interpretation and clarification.

1.2.1 Requests for Deviation - Requests for deviation from this specification or applicable drawings, specifications, publications, materials and processes specified herein, shall be considered design changes or design deviations and shall not be allowed except by written authorization from HAC.

1.3 Materials, Parts and Processes - When a material, part or process is not specified herein, the Seller's selection shall assure the highest uniform quality and condition of the product suitable for the intended use, and such selection shall be submitted for the review and concurrence of HAC, with the exception of such materials, parts and processes involving information proprietary to the Seller, in which case the Seller shall provide suitable documents showing specification compliance.

1.4 Changes - Any change in materials, parts, processes, manufacturing area, following acceptance tests, shall require the prior approval of HAC. HAC may require that additional testing be performed prior to granting approval of any vendor-negotiated change request.

2.0 APPLICABLE DOCUMENTS

The following documents of the date and/or revision shown are a part of this specification to the extent noted in subsequent paragraphs:

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Hughes Aircraft Company Drawings

XPS 31456-001	Procurement Specification, Solar Cell Aluminum Contact
PS 30660-080	Procurement Specification, Solar Cell, Bar Contact, Titanium-Silver Contact
258665	Source Control Drawing Blocking Solar Cell, Covered Aluminum Contact
258666	Source Control Drawing Blocking Solar Cell, Covered Silver Titanium Contact
X3354450	Coverslide, Blocking Solar Cell
258162	Strip Interconnect Aluminum
3205755	Strip Interconnect Copper

Other Sources

NASA-63-106	Radiation Damage Resistance for Silicon Solar Cells, 31 October 1962
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3.0 REQUIREMENTS

3.1 Design Description - The blocking solar cell shall have the physical properties of a solar cell and either aluminum contacts or silver-titanium contacts. The individual cells shall be capable of being electrically interconnected by means of an ultrasonic welding assembly process or by soldering in series-parallel groups.

3.1.1 Configuration - The dimensions and overall configuration of the cell shall conform to the Hughes Control Drawings.

3.1.2 Cell Defects - The maximum perimetric chip allowed shall be 0.025 inch deep by 0.150 inch long and the maximum corner chip shall be 0.60 inch on the hypotenuse. Surface nicks shall not exceed 0.050 inch x 0.050 inch. Cracks shall not be allowed.

3.1.3 Materials - All materials used in the blocking solar cell shall be in accordance with:

- a) XPS 31456-001 for the aluminum contact cells
- b) PS 30660-080 for the titanium silver contact cells

3.1.4 Cell Cover - The cells herein shall be procured with a cover installed (HAC Furnished Cover X3354450). The cover adhesive will be Dow type 93-500.

3.1.5 Cell Junctional Area - The blocking solar cell junction area shall be located at the upper cell surface to which the top bar contact(s) are applied. The junction shall not extend over or wrap around any edges of the cell.

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3.1.6 Negative and Positive Contacts - The cell contact(s) shall be free of adhesives or foreign material which could interfere with weldability or solderability. Contact surfaces shall be free of protrusions greater than 25 microns. The contacts shall conform to the requirements of Para. 3.1.7.

3.1.7 Contact Material - The contact material shall be as specified in Paragraph 3.1.3 and bonded to the silicon in such a manner as to insure that the strength of the bond exceeds the strength of the silicon when subjected to the tests set forth in Paragraph 3.1.8. The aluminum contacts shall be capable of having aluminum interconnectors attached using an ultrasonic welding process.

3.1.8 Contact Tests

a) Peel Test - As part of the in-process testing, the following test shall be performed by the Seller and a Certificate of Compliance shall be issued certifying, for HAC acceptance purposes, that the test has been performed as described herein. The peel test will be done to 100% of the cells on both sides as an in-process test and not as a portion of lot acceptance testing.

After contact deposition, each cell shall be tested by applying Scotch Brand No. 810 tape or approved equivalent to the cell contacts.

The tape shall be pressed to transparency, and then pulled away from the contact with a uniform continuous pull at an angle between 45° and 90° to the cell surfaces. Each cell shall then be examined for conformance to the contact coverage requirements. Any cell not meeting the above requirements shall be rejected.

Tape used in the peel test shall be traceable to the manufacturer's production lot. Procedures for storage requirements, shelf life indication and pull test shall be approved by HAC.

b) Welded Tab Pull Test (Aluminum contact only) - As part of the in-process testing, the following sample test shall be performed by the vendor and a Certificate of Compliance shall be issued certifying, for HAC acceptance purposes, that the test has been performed as described herein. The pull test will be done as an in-process test and not as a portion of lot acceptance test.

A single sample from each contact evaporation batch shall be destructively tested by attaching the pull tabs, as shown in Figure 1, and measuring peak force during a non-limited pull. Testing shall be performed at 100 ± 50 gram per second load rate using a Unitek Model 6-092-01 motor driven tester with peak reading Chatillon gage (Unitek Model 7-014-02, or HAC approved equivalent). Results shall be dispositioned as follows:

Pull value greater than 250 grams, all modes	PASS
Tab with aluminum pulled from cell leaving either submetal or the bare silicon cell surface exposed	FAILURE
Tab pulled out of test fixture, tab broken, or tab cell contact separated	REPEAT ON SAME CELL
Cell broke near or away from joint	REPEAT ON SAME OR NEW CELL

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Welded joint separated, removing aluminum from contact, and pulled out some silicon now adhering to tab

REPEAT ON
SAME CELL

Tab pulled off, leaving some aluminum on contact and pulled out some silicon now adhering to tab

PASS

Tab pulled complete divot of silicon out of cell. Tab pulled off leaving aluminum from tab on cell with no cell contact material or silicon adhering to tab

PASS

More than one tab pull failure shall constitute plating batch failure. Test cells shall not be deliverable.

3.1.9 Cleanliness - The cells shall be free of foreign material or contamination which could interfere with welding or soldering on contact areas, or which could interfere with adhesive curing or bonding to front and rear surfaces of the cells. The cells shall be suitable for interconnection welding, cover bonding, and cell-to-substrate bonding, without any additional cleaning.

3.1.10 Mechanical Durability - The cell shall be designed to provide mechanical durability by attention to silicon blank edges and surface condition, and by minimization of residual internal stresses.

3.1.11 Weight - The weight of the blocking solar cell shall be less than 115 milligrams.

3.1.12 Configuration Requirements - The device shall be compatible with either flexible roll-up array or rigid panel array concepts.

3.1.13 Cell Interconnects - The cells herein shall be procured with the interconnects installed according to HAC Drawings 258665 and 258666.

The interconnects to be furnished by HAC shall comply with HAC Dwg. 258162 for welded interconnects and 3205755 for soldered interconnects.

The soldered or welded interconnect, shall be installed in such a manner as to insure that the strength of the assembly as specified in 3.1.14.

3.1.14 Cell Interconnect Tests - After the interconnect has been installed and prior to cover bonding 1 cell of each type shall be selected and subjected to destructive tests to verify the integrity of the welded or soldered junction to withstand a pull of 200 grams or greater.

3.2 Performance Requirements

3.2.1 Ratings at Beginning of Life

$V_f = 1.2 \text{ V (max) at 3 amps, } 25^\circ\text{C}$
 $= 0.8 \text{ V (max) at 0.3 amps, } 25^\circ\text{C}$

$I_r = 0.1 \text{ ma (max) at 80 V}$
 $= 0.2 \text{ ma (max) at 120 V}$
 $= 1.0 \text{ ma (max) at 140 V}$

$T_{rr} = 3 \mu\text{.sec}$

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3.3 Environmental Performance - The blocking solar cells shall meet all performance requirements of this specification prior to and after the environmental conditions specified herein. (Ref. Paragraph 4.6 for degradation as a result of testing.)

3.3.1 Storage - The solar cells shall be capable of meeting all performance requirements of Paragraph 3.2 after storage at a relative humidity of 50 percent maximum and at a temperature of $25^{\circ} \pm 20^{\circ}\text{C}$ for a period of 24 months.

3.3.2 Temperature - Humidity - The blocking solar cells shall meet all performance requirements of Paragraph 4.6 after being tested in accordance with Paragraph 4.6.2 for 4 days at $95 \pm 5\%$ relative humidity, 45°C .

3.3.3 Operational Life - The solar cells shall be designed for an operational life of 10 years in the space environment.

3.3.4 Thermal Shock Cycling -

- a) The type blocking solar cells shall be designed for the following thermal cycling environments:

<u>Temperature Range, $^{\circ}\text{C}$</u>	<u>Number of Cycles</u>
-185 to +60	650
- 85 to +85	3,000 (design goal 40,000)

- b) The type blocking solar cells shall meet all performance requirements of Paragraph 4.6 after being subjected to a rate of change of temperature of 30°C per minute over a temperature range of -196 to $+90^{\circ}\text{C}$ in accordance with Paragraph 4.6.3.

3.3.5 High Temperature - Vacuum - The blocking solar cells shall meet all performance requirements of Paragraph 4.6 after exposure to a temperature of 140°C and a vacuum of 1×10^{-5} Torr for a period of 168 hours, plus an exposure of 200°C for 1 hour (for aluminum contact cells only), when tested in accordance with paragraph 4.6.4.

3.4 Interchangeability - Solar cells bearing the same part number shall be physically and functionally interchangeable without selection or fit. The HAC part number for these cells shall be that shown on the Cell Drawing.

4.0 TESTS

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4.1 General

4.1.1 Test Apparatus - All meters, scales, thermometers, and similar measuring test equipment used in conducting tests specified herein shall be accurate within 1 percent of the full scale value. Full-scale deflection of meters should not be more than twice the maximum value of the quantity being measured. All test apparatus shall be calibrated at suitable intervals and records of such calibration shall be available for inspection by HAC. HAC may examine the Seller's test equipment and determine that the Seller has available and utilizes correctly, gauging, measuring and test equipment of the required accuracy and precision, and that the instruments are of the proper type and range to make measurements of the required accuracy. The calibration of gauges, standards, and instruments shall be checked in a mutually agreed upon primary standards laboratory if disputes concerning performance occur. The cost of such check is to be borne by Seller.

4.1.2 Test Records - Records shall be kept of all tests and of applicable manufacturing data and these records shall be made available for inspection by HAC. Prior to and following each test of Paragraph 4.5, a thorough visual examination of the test items shall be conducted. All physical markings, defects and other visual characteristics shall be noted and recorded as a portion of the test records.

4.1.3 Test Conditions - Unless otherwise specified herein, all tests shall be performed at the following nominal ambient conditions:

- a) Temperature $25^{\circ} \pm 2^{\circ}\text{C}$
- b) Relative Humidity no greater than 50 percent

4.2 Classification of Tests - Tests shall be classified as follows:

- a) Acceptance tests
- b) Type approval tests

4.3 Sampling Procedures - The sample procedures for acceptance test of Paragraph 4.5 shall meet the requirements of Military Specification MIL-STD-105D for an AQL of 2.5 percent defective excluding the 100% electrical performance tests of Paragraph 4.5.2.

4.4 Test Locations - Unless otherwise specified in the contract, or in the specifications, type approval and acceptance tests shall be performed by the Seller at the Seller's plant. If the use of outside test facilities are required, the use of these facilities shall be subject to approval by HAC. HAC shall have the right to witness, inspect, and review all type approval and acceptance tests.

4.5 Acceptance Tests - A lot shall nominally consist of from 100 to 4000 blocking solar cells, manufactured under essentially the same conditions and submitted for acceptance at substantially the same time. The sampling plan shall comply with Paragraph 4.3.

4.5.1 Examination of Product - The blocking solar cells shall be inspected to determine compliance with respect to materials, workmanship, dimensions, and weight as specified in Paragraphs 3.1.1, 3.1.2, 3.1.3, 3.1.9, and 3.1.11.

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4.5.2 Electrical Performance - It shall be the Seller's responsibility to perform adequate testing and to obtain and submit adequate data to demonstrate that the requirements of Paragraph 3.2 are met. In addition to the Seller's tests, HAC will conduct at its option 100 percent electrical performance tests of delivered blocking solar cells.

4.6 Type Approval Tests - Type Approval Tests, when required by the contract shall be conducted in the manner described below prior to initial cell deliveries. A sample of 20 blocking solar cells, unless otherwise noted, shall be selected at random from a production lot. When two or more test cells fail to meet the requirements of this specification, the extent and cause of failure shall be determined and corrective action initiated. After corrective action has been taken, type approval and acceptance tests shall be repeated as required based upon review of the failure analysis by HAC and the Seller. Cells subjected to type approval test shall not be used for flight hardware, but shall be deliverable to the Buyer at completion of TAT. The cells shall be subjected to type approval tests in the order listed below. Each test shall be performed on the entire cell sample unless otherwise noted. Degradation of each individual cell parameter shall not exceed 5 percent.

4.6.1 Initial Tests - All blocking solar cells selected for the type approval test program shall first be subjected to acceptance tests in accordance with Paragraph 4.5.

4.6.2 Temperature and Humidity - The test specimens shall be placed in a sealed test chamber and the temperature and humidity raised to $95\% \pm 5\%$ relative humidity and $45 \pm 5^\circ\text{C}$. The test specimens shall be exposed to this environment for 4 days. At the end of this period, electrical performance test in accordance with Paragraph 4.5.2 shall then be conducted and the requirements of Paragraph 3.2 shall be met.

4.6.3 Thermal Shock - The cells shall be subjected to five temperature cycles at a minimum thermal rate of 30° per minute between the extremes of $90^\circ \pm 10^\circ\text{C}$ and $-196 \pm 10^\circ\text{C}$. The solar cells shall remain at the extremes for a minimum of one hour. Electrical performance tests in accordance with Paragraph 4.5.2 shall then be conducted and the requirements of Paragraph 3.2 shall be met.

4.6.4 High-Temperature Vacuum - The solar cells shall be placed in a test chamber reduced in pressure to a vacuum of at least 10^{-5} Torr. The temperature shall be raised to $140^\circ\text{C} \pm 10^\circ\text{C}$. The solar cells shall remain in the chamber for a period of 168 hours. The cells shall similarly be exposed to a temperature of 200°C for 1 hour in vacuum (for aluminum contact cells only) At the end of this period, the cells shall be allowed to return to room ambient temperature and the electrical performance tests in accordance with Paragraph 4.5.2 shall be conducted and the requirements of Paragraph 3.2 shall be met.

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4.7 Retest - Any changes made unilaterally by the supplier in manufacturing techniques, processes, materials, quality control levels, manufacturing sites or type of manufacturing equipment shall be cause for complete retest per Paragraph 4.6 at no cost to HAC.

4.8 Hughes Aircraft Company Tests - If after receipt by Hughes, a number of solar cells prove defective, such as to indicate a vendor process control problem, the individual cells or the entire lot may be rejected.

5.0 PREPARATION FOR DELIVERY

5.1 Shipping Container - The Seller shall provide containers of the size required for the delivery lots. Containers shall employ sealed humidity barrier bags with a desiccant quantity capable of assuring relative humidity no greater than 30 percent. The Seller shall demonstrate the suitability of the humidity capability of the desiccated container during packaging of the initial delivery lots. An indicator of desiccant water absorption shall be provided. All materials used in the shipping container shall be non-flaking and non-shredding.

5.2 Identification - Each solar cell shipping box shall be legibly identified by the following:

- a) HAC Part Number (Specification and Drawing Number)
- b) Seller's Part Number
- c) Month and Year of Manufacture
- d) Lot Number
- e) HAC Purchase Order Number
- f) Cell Type (P/N or N/P)

6.0 INSPECTION

6.1 General - The materials, processes and assembly covered by this specification shall be subjected to extensive inspection and testing by both the Seller and HAC.

6.2 Inspection

6.2.1 Seller Inspection - Product quality assurance shall be provided by the Seller by a series of in-process inspections commencing with receipt of raw materials and parts, and continuing through the finished product. The selected inspection points shall have the approval of HAC. A record shall be maintained of all inspection and be subject to review by HAC.

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6.2.2 HAC Source Inspection - The Hughes Aircraft Company shall at its option provide inspection to adequately monitor the Seller's quality control effort including in-process inspection and in-process tests. The complete hardware may be source inspected by HAC to assure that the product conforms to all the requirements specified by the applicable drawings and specifications and may include witnessing of acceptance tests.

6.2.3 Rejected Assemblies - Rejected assemblies shall not be resubmitted for approval without furnishing full particulars concerning the rejection, the measure taken to overcome the defects, and the prevention of their future occurrence. Each rejected assembly shall be identified by a serialized rejection tag. This rejection tag shall not be removed until rework requirements have been complied with, and the tag shall be removed only by, or in the presence of, an authorized representative of HAC.

6.3 Uniformity of Product - The Seller shall submit for HAC approval sufficient documentation to describe the cell and process required. Changes shall be subject to the requirements of Paragraph 1.4. The documentation shall include:

a) Detailed Physical Description of Blocking Solar Cell

- Seller's drawing (if used)
- Starting material parameters, such as:
 - purity
 - dislocation density
 - dopant material, dopant level, and original chemical form
 - Hall coefficient
 - oxygen content
 - crystal orientation
 - silicon source
- junction depth
- contact composition and substrate temperature during deposition
- other data as required to describe the cell

b) Quality Assurance Program, including a detailed flow chart: the flow chart shall show all processing steps and control/inspection points and procedures.

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DEVELOPMENT CHANGE NOTICE						HUGHES AIRCRAFT CO. CULVER CITY CODE IDENT 82577		DCN No 177390			
PRODUCT NAME/DESIGNATION <i>HS-229</i>				CONTROL ITEM AFFECTED (NUMBER NAME) <i>NONE</i>				DCN REV LTR	DATE <i>16 SEP 74</i>		
SHEET <i>1</i> OF <i>2</i>											
AFFECTED DRAWINGS/SPECIFICATIONS											
NUMBER	NEW	D.V. CHG	ADV CHG	NUMBER	NEW	D.V. CHG	ADV CHG	NUMBER	NEW	D.V. CHG	ADV CHG
<i>PS 30964-028</i>		<i>A</i>									
DESCRIPTION OF CHANGE											
<i>DELETE PARAGRAPH 3.3.6 AND 4.6.5</i> <i>Was: 3.3.6 Radiation - The solar cells with covers shall be designed to the following requirements:</i> <i>a) The solar cell design (with cover) shall be optimized for end-of-life performance under the following environmental conditions:</i> <i>RADIATION: 1) 10 year synchronous equatorial orbit or 5 year at 200 NM trapped electrons, trapped protons, and solar flare protons.</i> <i>2) artificial -- AFAPL Table I, 25 May 1970</i> <i>b) The Seller shall certify that the cells with covers applied are optimized for the above requirements.</i> <i>4.6.5 Radiation - The solar cells with covers applied may be subjected by the Buyer to radiation testing to verify the requirements of Paragraph 3.3.6.</i>											
REASON FOR CHANGE											
<i>EXTENSIVE IRRADIATION TESTING AT HAC FULLERTON INDICATES THAT BLOCKING SOLAR CELLS WITH A SHARP REVERSE CHARACTERISTIC UNDERGO MINIMAL DEGRADATION. THIS SHARP CHARACTERISTIC IS IMPOSED ON VENDOR THROUGH NEW PERFORMANCE REQUIREMENTS.</i>											
RELATED FACTORS											
FACTOR		YES	NO	FACTOR		YES	NO	FACTOR		YES	NO
PERFORM REQ/DESIGN OBJ			☒	COST			☒	CONTROL ITEM INTENS			☒
SYSTEM/OTHER CONTROL ITEM			☒	SCHEDULE			☒				
CHANGE CLASS	CHANGE EFF		DISPOSITION OF ITEMS				CUSTOMER APPROVAL REQUIRED		YES	NO	
<i>DI</i>	<i>5/N 1-UP</i>		<i>N/A</i>						☐	☐	
APPROVALS											
ORIGINATOR	DATE				DATE				DATE		
<i>H.F. [Signature]</i>	<i>7/10/74</i>										
RESPONSIBLE ENGINEER					AUTH FOR DISTRIBUTION						
<i>E. [Signature]</i>	<i>7/10/74</i>				<i>[Signature]</i>				<i>7/17/74</i>		
122											

DEVELOPMENT CHANGE NOTICE
CONTINUATION SHEET

HUGHES AIRCRAFT CO.
CULVER CITY
CODE IDENT 01877

DCN NO. 177390

DCN
REV
LTR

SH 2 OF 2

DATE
16 SEP 74

REVISE PARAGRAPH 3.2.1

Was:

3.2.1

Ratings at Beginning of Life

- I_f = 3 amperes at 100°C ambient
- V_f = 1.0 V (max) at 3 amps, 25°C
- V_f = 0.8 V (max) at 0.3 amps, 25°C
- V_R = 100 V at 1 ma maximum
- T_{rr} = 3 μ .sec

HUGHES HUGHES AIRCRAFT COMPANY CULVER CITY CALIFORNIA	TITLE PROCUREMENT SPECIFICATION SOLAR CELL, ALUMINUM CONTACT	XPS 31456-001 NUMBER	
		CODE IDENT NO. 82377	
		SH 1 OF 15	C REV LTR

RELEASED PRINT RESPONSIBLE ENGINEERING ACTIVITY		
HASPS		
REA ORG CODE 41-15-20		
C REV	12-20-73 REL DATE	NR REL BY

INITIAL APPROVALS	DATE	REV LTR	DATE	APPROVAL	
PREPARED D. MAEDING		B		TZ	REVISED & RETYPED
CHECKED		C	19 DEC 73	SEE DCN 13548	WD E. RN
APPROVED WC Dumbach	9/6/73				
TZ	9/6/73				
Gubeloff	9/11/73				

1.0 SCOPE

1.1 This specification covers the requirements for the design and construction of a photovoltaic solar cell of a type used on spacecraft solar panel assemblies.

1.2 Design Requirements - The solar cell shall be designed to meet all requirements specified herein. Test programs shall be successfully completed demonstrating the ability of the solar cell to meet all performance requirements in accordance with the following relative priority list:

- a) Reliability
- b) Air mass zero sunlight conversion efficiency, including nuclear and natural radiation resistance
- c) Structural characteristics such as strength and weldability
- d) Thermal Characteristics
- e) Weight

1.3 Conflicting Requirements - Conflicting requirements arising between this specification and any other specification or drawing listed herein shall be referred in writing to Hughes Aircraft Company (HAC) for interpretation and clarification.

1.3.1 Requests for Deviation - Requests for deviation from this specification, or applicable drawings, specifications, publications, materials and processes specified herein, shall be considered design changes or design deviations and shall not be allowed except by written authorization from HAC.

1.4 Materials, Parts and Processes - When a material, part or process is not specified herein, the Seller's selection shall assure the highest uniform quality and condition of the product suitable for the intended use, and such selection shall be submitted for the review and concurrence of HAC, with the exception of such materials, parts and processes involving information proprietary to the Seller, in which case the Seller shall provide suitable documents showing specification compliance.

1.5 Changes - Any change in materials, parts, process, manufacturing area, following TAT, shall require the prior approval of HAC. HAC may require that additional testing be performed prior to granting approval of any vendor-negotiated change request.

2.0 APPLICABLE DOCUMENTS

2.1 The following documents of the date and/or revision shown are a part of this specification to the extent noted in subsequent paragraphs:

PROCUREMENT SPECIFICATION, SOLAR CELL, ALUMINUM CONTACT	HUGHES AIRCRAFT CO. CODE IDENT NO. 82877	2 PAGE NO.	XPS 31456-001 NUMBER	C REV
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Military Specifications

MIL-STD-105D

Sampling Procedures and Tables for Inspection
by Attributes, 2 March 1964

Hughes Aircraft Company Drawings

XPS 31456-003 Procurement Specification, Solar Cell Cover

AFAPL-TR-72-44 Effects of Space and Nuclear Environments on
Lithium Doped Cells, July 1972

AFAPL Contract
F33614-70-C-1361 Procurement Specification, Solar Cells, Silicon,
Nuclear Detonation Resistant, July 1972.

HAC 255962 HAC Solar Cell, Aluminum Contacts

3.0

3.1

Design Description - The solar cell shall be a single crystal silicon type with shallow-diffused junction and aluminum contacts. The individual solar cells shall be capable of being electrically interconnected by means of an ultrasonic welding assembly process, in series-parallel groups. Cell types shall be defined as follows:

TYPE N/P: 10 Ω cm (7-14) --Part No. xxxxxx-2 (N/P)
TYPE P/N: Lithium Doped --Part No. xxxxxx-1 (P/N)

3.1.1

Configuration - The dimensions and overall configuration of the solar cell shall conform to the Hughes Source Control Drawing.

3.1.2

Cell Defects - The maximum perimetric chip allowed shall be 0.025 inch deep by 0.150 inch long and the maximum corner chip shall be 0.060 inch on the hypotenuse. Surface nicks shall not exceed 0.050 inch x 0.050 inch. Cracks shall not be allowed. The cell antireflection coating shall have no voids larger than 0.075 inch in diameter, and no more than five voids between 0.045 and 0.075 inch in diameter, and no more than 10 voids between 0.015 and 0.045 inch in diameter. Voids not detectable by the unaided eye shall be neglected.

3.1.3

Materials - All materials contained in the solar cell shall have an atomic number of 15 or less, with the exception that titanium may be used in the cell contacts to an effective titanium thickness not exceeding one micron; also, arsenic may be used as a dopant. The Seller shall certify that the cells meet this requirement.

3.1.4

Cell Cover - The cells herein shall be procured without coverglasses. However, the cells shall be suitable for use with a cover installed which conforms to HAC XPS 31456-003. (6 mil 7940 fused silica, 0.400 micron cutoff filter, no A/R coating). The cover adhesive will be one of the following Dow types: 182, 184, R-63-488, R-63-489, or 93-500.

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- 3.1.5 Cell Junction Area - The solar cell junction area shall be located at the upper cell surface to which the top bar contact and grids are applied. The junction shall not extend over or wrap around any other edges of the cell.
- 3.1.6 Solar Cell Absorptance and Emittance - Average emittance of the active area of the solar cell top surface with the coverglass applied, shall not be less than 0.83 from 25°C to 125°C. Average absorptance to solar radiation in the wavelength region 0.2 to 2.5 microns shall not exceed 0.82. The Seller shall certify that the solar cells meet this requirement.
- 3.1.7 Negative and Positive Contacts - The cell contacts shall be free of adhesives or foreign material which could interfere with weldability. Contact surfaces shall be free of protrusions greater than 25 microns. The contacts shall conform to the requirements of Paragraph 3.1.8.
- 3.1.8 Contact Material - The cells shall have 99.9% pure aluminum contacts, bonded to the silicon in such a manner as to insure that the strength of the bond exceeds the strength of the silicon when subjected to the peel tests set forth in Paragraph 3.1.9. The contacts shall be capable of having aluminum interconnectors attached using an ultrasonic welding process.
- 3.1.9 a) Peel Test - As part of the in-process testing, the following test shall be performed by the Seller and a Certificate of Compliance shall be issued certifying, for HAC acceptance purposes, that the test has been performed as described herein. The peel test will be done to 100% of the cells on both sides as an in-process test and not as a portion of lot acceptance testing.

After contact deposition, each solar cell shall be tested by applying Scotch Brand No. 810 Tape or approved equivalent to the cell N-contact, grids and P-contact surfaces. The tape shall be pressed to transparency, and then pulled away from the contact with a uniform continuous pull at an angle between 45° and 90° to the cell surfaces. On the bar contact and grids the pull shall begin at the grid tips and progress toward the bar. Each cell shall then be examined for conformance to the contact coverage requirements. Any cell not meeting the above requirements shall be rejected.

Tape used in the peel test shall be traceable to the manufacturer's production lot. Procedures for storage requirements, shelf life indication and pull test shall be approved by HAC.

b) Welded Tab Pull Test - As part of the in-process testing, the following sample test shall be performed by the vendor and a Certificate of Compliance shall be issued certifying, for HAC acceptance purposes, that the test has been performed as described herein. The pull test will be done as an in-process test and not as a portion of lot acceptance test.

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A 1% minimum sample from each contact evaporation batch shall be destructively tested by attaching the pull tabs, as shown in Figure 1, and measuring peak force during a non-limited pull. Testing shall be performed at 100 ± 50 gram per second load rate using a Unitek Model 6-092-01 motor driven tester with peak reading Chatillon gage (Unitek Model 7-014-02, or HAC approved equivalent). Results shall be dispositioned as follows:

Pull value greater than 250 grams, all modes	Pass
Tab with aluminum pulled from cell leaving either submetal or the bare silicon cell surface exposed	Failure
Tab pulled out of test fixture, tab broke, or tab cell contact separated	Repeat on same cell
Cell broke near or away from joint	Repeat on same or new cell
Welded joint separated, removing aluminum from contact, and pulled out some silicon now adhering to tab.	Repeat on same cell
Tab pulled off, leaving some aluminum on contact and pulled out some silicon now adhering to tab	Pass
Tab pulled complete divot of silicon out of cell	Pass
Tab pulled off leaving aluminum from tab on cell with no cell contact material or silicon adhering to tab	Pass

More than one tab pull failure shall constitute plating batch failure. Test cells shall not be deliverable.

- 3.1.10 Cell Anti-Reflection Coating - An anti-reflection coating shall be applied to the solar cell active surface. Coating material shall be of the silicon monoxide type (or HAC-approved alternate). Coating characteristics shall be such as to optimize the solar cell absolute power output with HAC XPS 31456-003 cover applied, under 1AU air mass zero, normal incidence illumination, at 60°C.
- 3.1.11 Covering Loss - Power output of the bare solar cell at the condition specified in Paragraph 3.2 shall not degrade more than 4% upon installation of the HAC XPS 31456-003 cover. The Seller shall apply covers to 50 cells from the first lot and measure cover losses at the specified voltage to verify this requirement. A Certificate of Compliance shall be provided for all subsequent lots.
- 3.1.12 Cleanliness - The solar cells shall be free of foreign material or contamination which could interfere with welding on contact areas, or which could interfere with adhesive curing or bonding to front and rear surfaces of the solar cells. The solar cells shall be suitable for interconnection welding, cover bonding, and cell-to-substrate bonding, without any additional cleaning.

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3.1.13

Mechanical Durability - The solar cell shall be designed to provide mechanical durability by attention to silicon blank edges and surface condition, and by minimization of residual internal stresses.

3.2

Power Output - The power output of solar cells without covers, under air mass zero spectral conditions, 1 A.U. solar radiation intensity and at a cell test block temperature of 25°C, shall meet the following requirements,

Cell Type	Voltage Volts *	Lot Minimum* Average Current, Amperes	Minimum Current* Per Cell, Amperes
P/N	0.470	0.126	0.105
N/P	0.445	0.126	0.105

* or HAC-approved alternate current-voltage specification of equal power.

The Seller shall separate solar cells into two-milliamper categories according to their current output at the specified voltage, and identify the categories in all deliveries to HAC. The categories will be determined at the above test conditions in the following manner.

- 1) Category 1 will consist of those solar cells whose current output is equal to or greater than 105 milliamperes and less than or equal to 107 milliamperes.
- 2) Category 2 will consist of those solar cells whose current output is greater than 107 milliamperes and less than or equal to 109 milliamperes.
- 3) Category 3 and up will consist of cells in consecutive two-milliamper categories above 109 milliamperes.

3.2.1

Illumination Sources - The source of radiation used to illuminate the cell for purposes of confirming cell power, Paragraph 3.2., shall be sunlight at the earth's surface at Table Mountain, California, or at other HAC-approved test sites with the following minimum sunlight conditions:

- 1) Illumination intensity shall be greater than 96 mw/cm^2 equivalent space solar radiation measured from the calibrated space cell; i.e., M shall be ≤ 1.26 .
- 2) No visually detectable precipitation.
- 3) No fluctuating cloud cover.
- 4) No testing shall be performed before 9:00 a.m. or after 3:00 p.m., Standard time.

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The calibrated space cell to be used shall be HAC standard cell A1A/B. The calibrated output of this cell shall be (at 1AU, 25°C, air mass zero spectral illumination) as follows:

A1A: 71.20 mv

A1B: 67.74 mv

A collimating tube equipped with baffles may be used, in which case it shall be used for both the space cell measurements and cells under test. The tube shall have a minimum length-to-diameter ratio of 10.

The power output under these conditions shall be corrected to air mass zero by multiplying by M, where M equals the ratio of the standard cell's calibrated space output divided by its output under test.

3.2.2 Temperature Variation - The Seller provide test data (I-V curves) on 50 sample cells from the first lot to determine the voltage-current characteristics of the cells at -50°C, 0°C, 50°C and 100°C. The tests shall be run with a constant illumination source as specified in Paragraph 3.2.1 or HAC-approved alternate. A Certificate of Compliance shall be provided for all subsequent lots. The requirement of this paragraph shall be met by the tests of Paragraph 4.6.3.

3.3 Environmental Performance - The solar cells shall meet all performance requirements of this specification including power output as defined in 3.2, prior to the environmental conditions specified herein. (Ref. Paragraph 4.6 for degradation as a result of testing.)

3.3.1 Storage - The solar cells shall be capable of meeting all performance requirements of Paragraph 3.2 after storage at a relative humidity of 50 percent maximum and at a temperature of 25° ±20°C for a period of 24 months.

3.3.2 Temperature - Humidity - The type N/P solar cells shall meet all performance requirements of Paragraph 4.6 after being tested in accordance with Paragraph 4.6.4 for 30 days at 90 ± 5 % relative humidity, 45°C. This shall be a design goal for type F/N cells.

3.3.3 Operational Life - The solar cells shall be designed for an operational life of seven years in the space environment.

3.3.4 Thermal Shock Cycling

a) The type N/P and type P/N solar cells shall be designed for the following thermal cycling environments:

<u>Temperature Range, °C</u>	<u>Number of Cycles</u>
-185 to +60	650
- 85 to +85	3,000 (design goal: 40,000)

b) The type N/P solar cells shall meet all performance requirements of Paragraph 4.0 after being subjected to a rate of change of temperature

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of 30°C per minute over a temperature range of -196 to +140°C in accordance with Paragraph 4.6.5. This shall be a design goal for type P/N cells.

- 3.3.5 High Temperature - Vacuum - The type N/P solar cells shall meet all performance requirements of Paragraph 4.6 after exposure to a temperature of 140°C and a vacuum of 1×10^{-5} Torr for a period of 168 hours, plus an exposure of 200°C for 1 hour, when tested in accordance with Paragraph 4.6.6. This shall be a design goal for type P/N cells.
- 3.3.6 Ultraviolet Illumination - The type N/P and type P/N solar cells shall meet all performance requirements of Paragraph 4.6 after being subjected to high intensity ultraviolet radiation with the HAC XPS 31456-003 cover installed, for an illumination period not less than 200 hours in accordance with Paragraph 4.6.7.
- 3.3.7 Radiation - The solar cells with covers shall be designed to the following requirement:
- a) The solar cell design (with cover) shall be optimized for highest end-of-life absolute output under the following environmental conditions:
 - Radiation: 1) 7 year synchronous equatorial orbit trapped electrons, trapped protons, and solar flare protons.
 - 2) artificial -- AFAPL Table I, 25 May 1970
 - Temperature: 1) 7 year soak temperature prior to artificial exposure; +85°C max.
 - 2) steady state temperature for annealing purposes following artificial exposure; +60°C
 - b) The Seller shall certify that the cells with covers applied are optimized for the above requirements.
- 3.4 Interchangeability - Solar cells bearing the same part number shall be physically and functionally interchangeable without selection or fit. The HAC part number for these cells shall be that shown on the Cell Drawing.

4.0 TESTS

4.1 General

- 4.1.1 Test Apparatus - All meters, scales, thermometers, and similar measuring test equipment used in conducting tests specified herein shall be accurate within 1 percent of the full scale value. Full-scale deflection of meters should not be more than twice the maximum value of the quantity being measured. All test apparatus shall be calibrated at suitable intervals and records of such calibration shall be available for inspection by HAC. HAC may examine the Seller's test equipment and determine that the Seller has available and utilizes correctly, gauging, measuring and test equipment of the required accuracy and precision, and that the instruments are of the proper type and range to make measurements of the

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required accuracy. The calibration of gauges, standards, and instruments shall be checked in a mutually agreed upon primary standards laboratory if disputes concerning performance occur. The cost of such check is to be borne by Seller.

- 4.1.2 Test Records - Records shall be kept of all tests and of applicable manufacturing data and these records shall be made available for inspection by HAC. Prior to and following each test of Paragraph 4.5, a thorough visual examination of the test solar cells shall be conducted. All physical markings, defects and other visual characteristics shall be noted and recorded as a portion of the test records.
- 4.1.3 Test Conditions - Unless otherwise specified herein, all tests shall be performed at the following nominal ambient conditions:
- a) Temperature $25^{\circ} \pm 5^{\circ}\text{C}$
 - b) Relative Humidity no greater than 50 percent
- 4.2 Classification of Tests - Tests shall be classified as follows:
- a) Acceptance tests
 - b) Type Approval test
- 4.3 Sampling Procedures - The sampling procedures for acceptance test of Paragraph 4.5 shall meet the requirements of Military Specification MIL-STD-105D for an AQL of 2.5 percent defective excluding the 100% electrical performance tests of Paragraph 4.5.2.
- 4.4 Test Locations - Unless otherwise specified in the contract, or in the specifications, type approval and acceptance tests shall be performed by the Seller at the Seller's plant. If the use of outside test facilities are required, the use of these facilities shall be subject to approval by HAC. HAC shall have the right to witness, inspect, and review all type approval and acceptance tests.
- 4.5 Acceptance Tests - A lot shall nominally consist of from 100 to 4000 solar cells, manufactured under essentially the same conditions and submitted for acceptance at substantially the same time. The sampling plan shall comply with Paragraph 4.3.
- 4.5.1 Examination of Product - The solar cells shall be inspected to determine compliance with respect to materials, workmanship, dimensions, and weight as specified in Paragraph 3.1.1, 3.1.2, 3.1.7, and 3.1.12.
- 4.5.2 Electrical Performance - It shall be the Seller's responsibility to perform adequate testing and to obtain and submit adequate data to demonstrate that the power output requirements of Paragraph 3.2 are met. In addition to the Seller's tests, HAC will conduct at its option 100 percent electrical performance tests of delivered solar cells. Solar cell power output shall be determined at a cell block temperature of

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25 ± 2°C.

- 4.5.2.1 To comply with Paragraph 3.2 and 3.2.1 a sample of 100 solar cells from the first lot shall be selected in a random manner proportional to the distribution of the lot, and their electrical performance (I-V curve) determined in sunlight as specified in Paragraph 3.2.1. Such measurements shall be performed on two separate days to obtain an average air mass zero short-circuit-current for each cell. The average of the short circuit currents of these secondary standards shall be used to set and maintain solar simulation light source intensity level and thereby establish acceptance criteria for the solar cells at Seller's and Buyer's facility. The light source used by the Seller for the above testing for a lot shall have HAC approval.
- 4.5.2.2 A sample of 100 secondary standard solar cells shall be used for no longer than 180 days from the time of initial sunlight test, at which time a replacement sample of 100 cells shall be selected from a current production lot to be employed per Paragraph 4.5.2.1.
- 4.5.2.3 To confirm that the sample of Paragraph 4.5.2.1 remains representative of cells from subsequent lots, a sample of 10 % but not to exceed 50 cells from each lot shall be selected in a random manner proportional to the distribution of the lot and electrical performance (I-V curve) determined under the acceptance test solar simulator light source, with a Corning CS-2-60 filter placed in the light source beam. Electrical performance (I-V curve) of the same cell sample shall also be determined under the solar simulator light source without the filter and a ratio (R) determined between the average of short-circuit-current of the cell sample measured under the two light source conditions. The ratio (R) for each lot shall not deviate from the ratio (R) for the lot from which the 100 cell sample was selected by more than two percent. Greater deviation shall require selection of a replacement 100 cell sample from the current lot per Paragraph 4.5.2.2.
- 4.6 Type Approval Tests - Type approval tests, when required by the contract shall be conducted in the manner described below and prior to initial cell deliveries. A sample of 100 solar cells, unless otherwise noted, shall be selected at random from a production lot. When two or more test cells fail to meet the requirements of this specification, the extent and cause of failure shall be determined and corrective action initiated. After corrective action has been taken, type approval and acceptance tests shall be repeated as required based upon review of the failure analysis by HAC and the Seller. Cells subjected to type approval test shall not be used for flight hardware, but shall be deliverable to the Buyer at completion at TAT. The solar cells shall be subjected to type approval tests in the order listed below. Each test shall be performed on the entire 100-cell sample unless otherwise noted. Degradation of individual cell output shall not exceed 5 percent, and degradation of the sample average power output shall not exceed 2 percent, at completion of the TAT Program. The preceding applies to type N/P cells. Type P/N cells shall be subjected to type approval tests for engineering information only.

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- 4.6.1 Initial Tests - All solar cells selected for the type approval test program shall first be subjected to acceptance tests in accordance with Paragraph 4.5 including sub-paragraph 4.5.2 and meet all the requirements of Section 3.0 including sample output and cell minimum power output.
- 4.6.2 Covering Loss - The Seller shall apply HAC XPS31456-003 covers to 50 cells randomly selected from the first lot to verify compliance to the covering loss requirement of Paragraph 3.1.12. A Certificate of Compliance shall be provided for all subsequent lots.
- 4.6.3 Temperature Variation - The Seller shall provide test data (I-V curve) on 50 sample cells from the first lot to determine the voltage-current characteristics of the cells at -50°C , 0°C , $+50^{\circ}\text{C}$ and 100°C . The test shall be run with a constant illumination source as specified in Paragraph 3.2.1 or HAC-approved alternate. A Certificate of Compliance shall be provided for all subsequent lots.
- 4.6.4 Temperature and Humidity - The test specimens shall be placed in a sealed test chamber and the temperature and humidity raised to $95\% \pm 5\%$ relative humidity and $45 \pm 5^{\circ}\text{C}$. The test specimens shall be exposed to this environment for 30 days. At the end of this period, electrical performance test in accordance with Paragraph 4.5.2. shall be conducted and the requirements of Paragraph 3.2 shall be met using a laboratory light source calibrated per Paragraph 4.5.2.
- 4.6.5 Thermal Shock - The solar cells shall be subjected to five temperature cycles at a minimum thermal rate of 30° per minute between the extremes of $140 \pm 10^{\circ}\text{C}$ and $-196 \pm 10^{\circ}\text{C}$. The solar cells shall remain at the extremes for a minimum of one hour. Electrical performance tests in accordance with Paragraph 4.5.2 shall then be conducted and the requirements of Paragraph 3.2 shall be met using a laboratory light source calibrated per Paragraph 4.5.2.
- 4.6.6 High-Temperature Vacuum - The solar cells shall be placed in a test chamber reduced in pressure to a vacuum of at least 10^{-5} Torr. The temperature shall be raised to $140 \pm 10^{\circ}\text{C}$. The solar cells shall remain in the chamber for a period of 168 hours. The cells shall similarly be exposed to a temperature of 200°C for 1 hour in vacuum. At the end of this period, the cells shall be allowed to return to room ambient temperature and the electrical performance tests in accordance with Paragraph 4.5.2 shall be conducted and the requirements of Paragraph 3.2 shall be met.
- 4.6.7 Ultra-Violet Illumination Test - Fifteen of the 100 type approval solar cells shall be subjected to high intensity ultra-violet radiation from a Model No. 700-J Ultra-Violet lamp unit manufactured by Shannon Luminous Materials Company, Hollywood, California, or the equivalent. The cells, with cover applied, shall be positioned normal to the irradiation with the active cell areas facing the illuminating source. The cells shall be positioned about the centerline of the lamp unit at a distance of approximately $3\frac{1}{4}$ inches from the open end of the lamp housing. Forced air cooling shall be employed to maintain the cells at a temperature in the range 40° to 50°C . Duration of the test shall be 200 hours. Upon completion, the cells shall be tested for electrical performance in accordance with Paragraph 4.5.2, and the requirements of Paragraphs 3.2 shall be met using a laboratory light source calibrated per Paragraph 4.5.2. In lieu of performing the ultraviolet radiation

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test the Seller may provide sufficient evidence and certification that similar solar cells employing the same materials of construction have satisfactorily completed the test.

4.6.8 Radiation - The solar cells with covers applied may be subjected by the Buyer to radiation testing to verify the requirements of Paragraph 3.3.7.

4.7 Retest - Any changes made unilaterally by the supplier in manufacturing techniques, processes, materials, quality control levels, manufacturing sites or type of manufacturing equipment shall be cause for complete retest per Paragraph 4.6 at no cost to HAC.

4.8 Hughes Aircraft Company Tests - If after receipt by Hughes, a number of solar cells prove defective, such as to indicate a vendor process control problem, the individual cells or the entire lot may be rejected.

5.0 PREPARATION FOR DELIVERY

5.1 Shipping Container - The Seller shall provide containers of the size required for the delivery lots. Containers shall employ sealed humidity barrier bags with a desiccant quantity capable of assuring relative humidity no greater than 30 percent. The Seller shall demonstrate the suitability of the humidity capability of the desiccated container during packaging of the initial delivery lots. An indicator of desiccant water absorption shall be provided. All materials used in the shipping container shall be non-flaking and non-shredding.

5.2 Identification - Each solar cell shipping box shall be legibly identified by the following:

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- a) HAC Part Number (Specification and Drawing Number)
- b) Seller's Part Number
- c) Month and year of manufacture
- d) Lot number
- e) Category (refer to Paragraph 3.2)
- f) HAC Purchase Order Number
- g) Cell type (P/N or N/P)

6.0

- 6.1 General - The materials, processes and assembly covered by this specification shall be subjected to extensive inspection and testing by both the Seller and HAC.

6.2 Inspection

- 6.2.1 Seller Inspection - Product quality assurance shall be provided by the Seller by a series of in-process inspections commencing with receipt of raw materials and parts, and continuing through the finished product. The selected inspection points shall have the approval of HAC. A record shall be maintained of all inspection and be subject to review by HAC.

- 6.2.2 HAC Source Inspection - The Hughes Aircraft Company shall at its option provide inspection to adequately monitor the Seller's quality control effort including in-process inspection and in-process tests. The complete hardware may be source inspected by HAC to assure that the product conforms to all the requirements specified by the applicable drawings and specifications and may include witnessing of acceptance tests.

- 6.2.3 Rejected Assemblies - Rejected assemblies shall not be resubmitted for approval without furnishing full particulars concerning the rejection, the measure taken to overcome the defects, and the prevention of their future occurrence. Each rejected assembly shall be identified by a serialized rejection tag. This rejection tag shall not be removed until rework requirements have been complied with, and the tag shall be removed only by, or in the presence of, an authorized representative of HAC.

- 6.3 Uniformity of Product - The Seller shall submit for HAC approval sufficient documentation to describe the cell and process required. Changes shall be subject to the requirements of Paragraph 1.5. The documentation shall include:

a) Detailed Physical Description of Solar Cell

- Seller's drawing (if used)
- Starting material parameters, such as:
 - purity
 - dislocation density
 - dopant material, dopant level, and original chemical form
 - Hall coefficient
 - oxygen content
 - crystal orientation

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- silicon source
 - junction depth
 - lithium concentration at junction, and concentration profile (for type P/N cell)
 - contact composition and substrate temperature during deposition
 - other data as required to describe the cell
- b) Quality Assurance Program, including a detailed flow chart: The flow chart shall show all processing steps and control/inspection points and procedures, including methods of lithium concentration monitoring and control.

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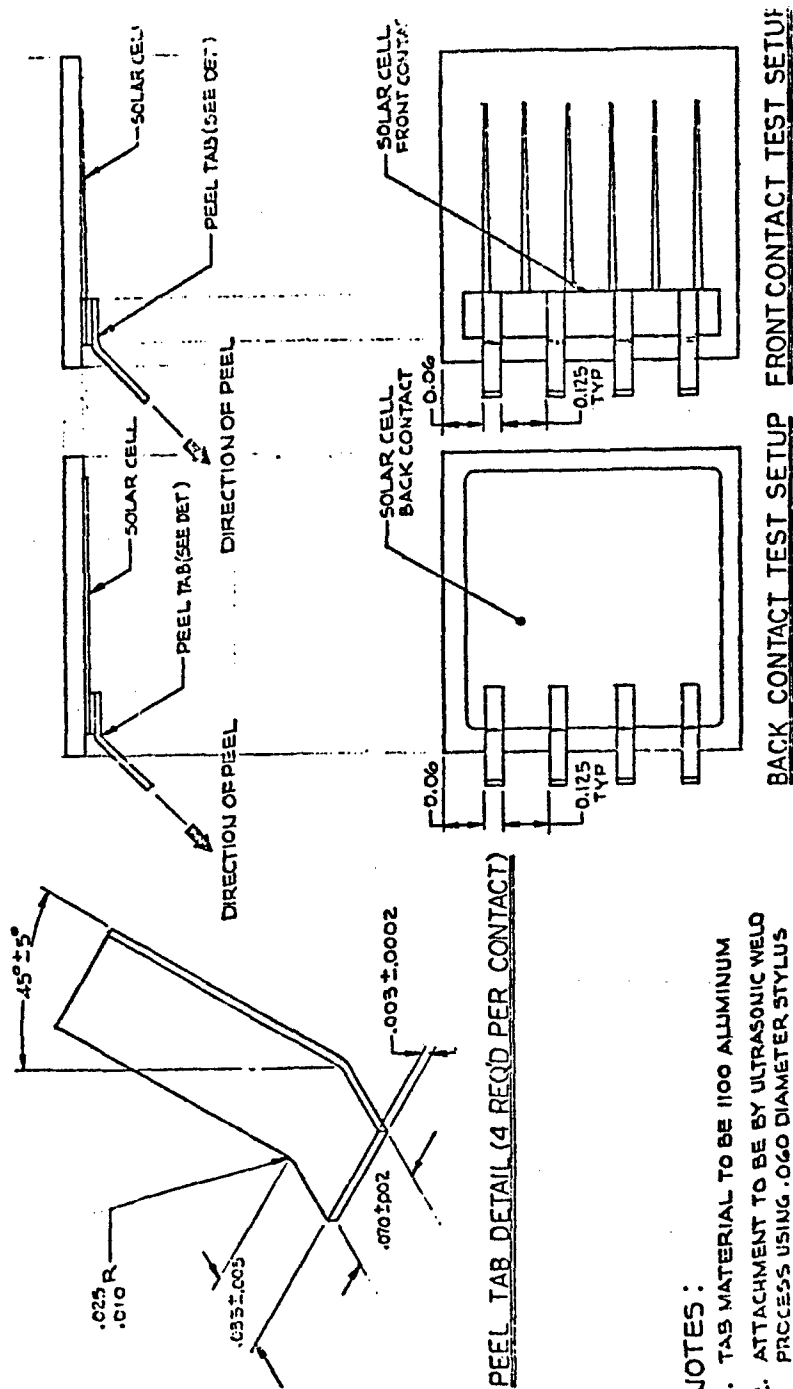


FIGURE 1 PULL TEST ARRANGEMENT

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INITIAL APPROVALS			
	DATE		DATE
T. Eakins	10 OCT 68	D REV. by ECA 192870	3 July 71
W. Dawson	14 OCT 68		
E. Levy	15 OCT 68		

1.0 SCOPE

1.1 This specification covers the requirements for the design and construction of a photovoltaic solar cell to be used on spacecraft solar panel assemblies.

1.2 Design Requirements - The solar cell shall be designed to meet all requirements specified herein. Test programs shall be successfully completed demonstrating the ability of the solar cell to meet all performance requirements of this specification. The solar cell shall be designed for optimum operation in accordance with the following relative priority list:

- a) Reliability
- b) Air mass zero sunlight conversion efficiency
- c) Spectral characteristics
- d) Thermal characteristics
- e) Weight

1.3 Conflicting Requirements - Conflicting requirements arising between this specification and any other specification or drawing listed herein shall be referred in writing to Hughes Aircraft Company (HAC) for interpretation and clarification.

1.3.1 Requests for Deviation - Requests for deviation from this specification, applicable drawings, specifications, publications, materials and processes specified herein, shall be considered design changes or design deviations and shall not be allowed except by written authorization from HAC.

1.4 Materials, Parts and Processes - When a material, part or process is not specified herein, the Seller's selection shall assure the highest uniform quality and condition of the product suitable for the intended use, and such selection shall be submitted for the review and concurrence of HAC, with the exception of such materials, parts and processes involving information proprietary to the Seller, in which case the Seller shall provide suitable documents showing specification compliance.

1.5 Changes - Any change in materials, parts, process or manufacturing area shall require the prior approval of HAC. HAC may require that additional testing be performed prior to granting approval of any vendor-negotiated change request.

2.0 APPLICABLE DOCUMENTS

2.1 The following documents of the date and/or revision shown are a part of this specification to the extent noted in subsequent paragraphs:

Military Specifications

MIL-STD-105D Sampling Procedures and Tables for inspection
by Attributes, 2 March 1964

Hughes Aircraft Company Drawings

PS 30660-083 Procurement Specification, Solar Cell Cover

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3.0 REQUIREMENTS

3.1 Design Description - The solar cell shall be nominally 10 (7-14 ohm-cm. bulk resistivity) 0.1-cm shallow diffused silicon N-on-P junction type with coverglass applied. The individual solar cells with coverglass installed shall be capable of being electrically interconnected by means of a soldering assembly process, in series-parallel groups.

3.1.1 Configuration - The dimensions and overall configuration of the solar cell shall conform to the Hughes Source Control Drawing. The solar cell cover shall conform to HAC Procurement Specification PS 30660-083.

3.1.2 Cell Defects - The maximum perimetric chip allowed shall be 0.025 inch deep by 0.150 inch long and the maximum corner chip shall be 0.060 inch on the hypotenuse. Surface nicks shall not exceed 0.050 inch x 0.050 inch. Cracks shall not be allowed. Silicon monoxide shall have no voids larger than 0.075 inch in diameter, and no more than five voids between 0.045 and 0.075 inch in diameter, and no more than 10 voids between 0.015 and 0.045 inch. Voids not detectable by the unaided eye shall be neglected.

3.1.2.1 Cell Cover Defects - Chips shall not extend more than 0.015 from the edge, with maximum legs on corner chips of 0.025 inch. The cell covers shall contain no bubbles larger than that specified for its overall thickness. The following criteria shall be used in determining the allowable bubbles in the cell covers:

- a) For cover thicknesses greater than .025", the maximum diameters of included bubbles shall be .015".
- b) For cover thicknesses between .015" and .025", the maximum diameters of included bubbles shall be .010".
- c) For cover thicknesses between .006" and .015", the maximum diameters of included bubbles shall be .005".
- d) For cover thicknesses less than .006", closed bubbles of .005" maximum diameter and open bubbles no greater than .003" shall be acceptable.
- e) Included bubbles of less than .005" diameter shall be discounted in covers of all thicknesses. The allowable number of bubbles of the maximum size specified shall not exceed three for an equivalent 2 x 2 area.

Cracks shall not be allowed. These conditions shall not conflict with Paragraph 3.1.2.3.

3.1.2.2 Cell Cover Adhesive Defects - There shall be no evidence of delamination or discoloration in the adhesive. 10X magnificant shall be used for determining delamination. Adhesive voids along the cover edges shall not exceed 0.015 inch in depth. Adhesive bubbles other than at the cover edges shall not exceed 0.015 inch in diameter and there shall be no more than five such bubbles per cell, discounting bubbles less than 0.005 inch in diameter.

3.1.2.3 Bare Cell Exposure - No portion of the active area of the solar cell shall be exposed with respect to the coverslide, or with respect to the "n" contact solder film, except for the solder coverage allowance defined in Para. 3.1.7.

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3.1.3 Solar Cell Absorptance and Emissance - Average emissance of the active area of the solar cell top surface with the coverglass applied, shall not be less than 0.83 from 25° C to 125° C. Average absorptance to solar radiation in the wavelength region 0.2 to 2.5 microns shall not exceed 0.82. The Seller shall certify that the solar cells meet this requirement.

3.1.3.1 Ultraviolet Cutoff Filter - The ultraviolet cutoff filter on the cell cover shall have the following characteristics.

<u>Wavelength</u> <u>(Microns)</u>	<u>Transmittance</u> <u>(percent)</u>
From 0.300 to 0.370 0.400 $\pm$ 0.015	Less than 1 average 50

The Seller will certify that the filter on the solar cell cover meets this requirement.

3.1.4 Negative Contact - The exposed negative (top) contact of the cell shall be free of adhesive or foreign material which could interfere with solderability. The contact shall conform to the requirements of Paras. 3.1.6 and 3.1.7.

3.1.5 Positive Contact - The positive contact surface of the cell shall be flat within 0.003 inch and free of all contaminating material.

3.1.6 Plating Coverage - Plating coverage of the titanium-silver "N" contact shall be a minimum of 99 percent of the "N" contact area shown on the solar cell drawing. Plating coverage of the titanium-silver "P" contact shall be minimum of 95 percent of the "P" area shown on the cell drawing.

3.1.7 Contact Material - The cells shall have titanium-silver type plated contacts, or HAC approved alternate, bonded to the silicon in such a manner as to insure that the strength of the bond exceeds the strength of the silicon when subjected to the peel test set forth in Paragraph 3.1.8. The negative contact shall be 99 percent covered with a solder film. The negative grids under neath the coverglass shall be 90 percent covered with a solder film. The positive contact shall have a minimum of 90 percent solder coverage of the solder area shown on the solar cell drawing.

3.1.8 Peel Test - As part of the in-process testing, the following test shall be performed by the Seller and a certificate of Compliance shall be issued certifying for HAC acceptance purposes that the test has been performed as described herein. The peel test will be done as an in-process test and not as a portion of lot acceptance testing.

After contact deposition, each solar cell shall be tested by applying Scotch Brand No. 810 Tape or approved equivalent to the cell N-contact, grids, and P contact surfaces. The tape is pressed to transparency, and then pulled away from the contact with a uniform continuous pull. On the N contact (and grids) the pull shall begin at one end of the contact bar and progress toward the other end. Each cell is then examined for conformance to the contact coverage requirements (Paragraph 3.1.6 of the specification.) Any cell not meeting the above requirements is rejected.

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Tape used in the peel test shall be traceable to the manufacturer's production lot. Procedures for storage requirements, shelf life indication and pull test shall be approved by HAC.

3.1.9 Weight - Total assembled solar cell weight including the coverglass shall not exceed that specified on the cell drawing.

3.2 Power Output - The power output of solar cells with HAC PS 30660-083 coverglass applied under air mass zero spectral conditions, and solar radiation intensity of 139.6 mw/cm^2 shall meet the following requirements:

Test Conditions

<u>Temperature, °C</u>	<u>Voltage, Volts</u>	<u>Power, Milliwatts*</u>
25 ± 2	0.445 ± 0.002	55.85 minimum average per lot 51.18 minimum per cell

*The electrical performance of the solar cell shall be measured with an illumination source as specified in Paragraph 3.2.1. The Seller shall submit adequate data with each lot showing specification compliance.

The Seller shall separate solar cells into two milliampere (2 MA) categories according to their current output at 0.445 volts and identify the categories in all deliveries to HAC. The categories will be determined at the above test conditions in the following manner:

- 1) Category 1 will consist of those solar cells whose current output is equal to or greater than 115 milliamperes and less than or equal to 117 milliamperes.
- 2) Category 2 will consist of those solar cells whose current output is greater than 117 milliamperes and less than or equal to 119 milliamperes.
- 3) Categories 3 and up will consist of cells in consecutive two-milliampere categories above 119 milliamperes.

The Seller shall submit test data to the Buyer to certify that this requirement has been satisfactorily completed.

3.2.1 Illumination Sources - The source of radiation used to illuminate the cell for purposes of confirming cell power, Para. 3.2, shall be sunlight at the Earth's surface at Table Mountain, California, or at other HAC-approved test sites with the following minimum sunlight conditions:

- 1) Illumination intensity shall be greater than 96 mw/cm^2 equivalent space solar radiation measured from the calibrated space cell; i.e., M shall be 1.26. M is defined as the ratio of the space cell's short circuit current in space to the cell's short circuit current under test conditions.
- 2) No visually detectable precipitation.
- 3) No fluctuating cloud cover.
- 4) No testing shall be performed before 9:00 a.m. or after 3:00 p.m., Standard time.

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The calibrated space cell to be used shall be a HAC Primary Standard Cell or a HAC-approved secondary standard cell calibrated to 139.6 mw/cm², air mass zero illumination, and a temperature of 25°C.

A collimating tube equipped with baffles may be used, in which case it shall be used for both the space cell measurements and cells under test. The tube shall have a minimum length-to-diameter ratio of 10. The power output under these conditions shall be corrected to air mass zero by multiplying by M.

3.2.2 Intensity Variation - The Seller shall provide test data (I-V curves) on 50 sample cells from the first lot to establish the voltage-current characteristic of the cells at 100, 115, 130, and 150 milliwatts per square centimeter illumination intensities. The cells shall be maintained at 25°C throughout the test. The illumination source shall be calibrated using the cells and data obtained from the tests of Paragraph 4.5.2. Light intensity shall be preset to achieve a proportionate increase in the test cells short circuit current. A certificate of Compliance shall be provided for all subsequent lots. The requirement of this paragraph shall be met by the tests of Paragraph 4.6.2.

3.2.3 Temperature Variation - The Seller shall provide test data (I-V curves) on 50 sample cells from the first lot to determine the voltage-current characteristics of the cells at -50°C, 0°C, 50°C and 100°C. The tests shall be run with a constant illumination source as specified in Paragraph 3.2.1 or HAC-Approved alternate. A Certificate of Compliance shall be provided for all subsequent lots. The requirement of this paragraph shall be met by the tests of Paragraph 4.6.3.

3.3 Environmental Performance - The solar cells shall meet all performance requirements of this specification including power output as defined in 3.2, prior to the environmental conditions specified herein. (Ref. Para. 4.6 for degradation as a result of testing.)

3.3.1 Storage - The covered solar cells shall be capable of meeting the storage requirements specified below.

a) The solar cells shall be capable of meeting all performance requirements of Para. 3.2 after storage at a relative humidity of 50 percent maximum and at a temperature of $21^{\circ} \pm 15^{\circ}$ C for a period of 24 months.

b) The solar cells shall be capable of meeting all performance requirements of Para. 3.2 after storage at a relative humidity of 95 percent maximum and at a temperature of $24^{\circ} \pm 20^{\circ}$ C for a period of one month.

3.3.2 Temperature - Humidity - The solar cells shall meet all performance requirements of Para. 4.6 after being tested in accordance with paragraph 4.6.4.

3.3.3 Operational Life - The solar cells shall be designed for a minimum operational life of seven years in the space environment.

3.3.4 Thermal Shock - The solar cells shall meet all performance requirements of Para. 4.6 after being subjected to a rate of change of temperature of 30° C per minute through a temperature range between 140°C and -196°C in accordance with paragraph 4.6.5.

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3.3.5 High Temperature - Vacuum - The solar cells shall meet all performance requirements of Para. 4.6 after exposure to a temperature of 140° C and a vacuum of 1×10^{-5} Torr for a period of 168 hours when tested in accordance with Paragraph 4.6.6.

3.3.6 Ultra-Violet Radiation - The solar cells shall meet all performance requirements of Para. 4.6 after being subjected to high intensity ultra-violet radiation for an illumination period not less than 200 hours in accordance with Paragraph 4.6.7.

3.4 Interchangeability - Solar cells bearing the same part number shall be physically and functionally interchangeable without selection or fit. The HAC part number for these solar cells shall be that shown on the Source Control Drawing.

4.0 TESTS

4.1 General

4.1.1 Test Apparatus - All meters, scales, thermometers, and similar measuring test equipment used in conducting tests specified herein shall be accurate within 1 percent of the full-scale value. Full-scale deflection of meters should not be more than twice maximum value of the quantity being measured. All test apparatus shall be calibrated at suitable intervals and records of such calibration shall be available for inspection by HAC. HAC may examine the Seller's test equipment and determine that the Seller has available and utilizes correctly, gauging, measuring and test equipment of the required accuracy and precision, and that the instruments are of the proper type and range to make measurements of the required accuracy. The calibration of gauges, standards, and instruments shall be checked in a mutually agreed upon primary standards laboratory if disputes concerning performance occur, the cost of such check is to be borne by Seller.

4.1.2 Test Records - Records shall be kept of all tests and of applicable manufacturing data and these records shall be made available for inspection by HAC. Prior to and following each test of Paragraph 4.6, a thorough visual examination of the test solar cell shall be conducted. All physical markings, defects, and other visual characteristics shall be noted and recorded as a portion of the test records.

4.1.3 Test Conditions - Unless otherwise specified herein, all tests shall be performed at the following nominal ambient conditions:

- a) Temperature $25^{\circ} \pm 5^{\circ} \text{C}$
- b) Relative humidity no greater than 50 percent

4.2 Classification of Tests - Tests shall be classified as follows:

- a) Acceptance Tests
- b) Type Approval Tests

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4.3 Sampling Procedures - The sampling procedures for acceptance tests of Paragraph 4.5 shall meet the requirements of Military Specification MIL-STD-105D for an AQL of 2.5 percent defective, excluding the bare cell exposure requirements of Para. 3.1.2.3 and the electrical performance test of Paragraph 4.5.2.

4.4 Test Location - Unless otherwise specified in the contract, type approval and acceptance tests shall be performed by the Seller at the Seller's plant. If the use of outside test facilities are required, the use of these facilities shall be subject to approval by HAC. HAC shall have the right to witness, inspect, and review all type approval and acceptance tests.

4.5 Acceptance Tests - A lot shall nominally consist of from 1000 to 8000 solar cells, manufactured under essentially the same conditions and submitted for acceptance at substantially the same time. The sampling plan shall comply with Paragraph 4.3. Lot sizes shall be defined in the Statement of Work.

4.5.1 Examination of Product - The solar cells shall be inspected to determine compliance with respect to materials, workmanship, dimensions, and weight as specified in Paragraphs 3.1.1, 3.1.2, 3.1.2.1, 3.1.2.2, 3.1.4, 3.1.5, 3.1.6 and 3.1.9. In order to insure compliance with Para. 3.1.2.3 and 3.1.7, 100% inspection will be carried out by the vendor.

4.5.2 Electrical Performance - It shall be the Seller's responsibility to perform adequate testing and to obtain and submit adequate data to demonstrate that the power output requirements of Paragraph 3.2 are met. In addition to the Seller's tests, HAC will conduct at its option 100 percent electrical performance tests of delivered solar cells. Solar cell output shall be determined at a temperature of $25 \pm 2^{\circ}\text{C}$.

4.5.2.1 To comply with Paragraph 3.2 and 3.2.1 a sample of 100 solar cells from the first lot shall be selected in a random manner proportional to the distribution of the lot, and their electrical performance (I-V curve) determined in sunlight as specified in Paragraph 3.2.1. Such measurements shall be performed on two separate days to obtain an average air mass zero short-circuit-current for each cell. The average of the short circuit currents of these secondary standards shall be used to set and maintain solar simulation light source intensity level and thereby establish acceptance criteria for the solar cells at Seller's and Buyer's facility. The light source used by the Seller for the above testing for a lot shall have HAC approval.

4.5.2.2 A sample of 100 secondary standard solar cells shall be used for no longer than 180 days from the time of initial sunlight test, at which time a replacement sample of 100 cells shall be selected from a current production lot to be employed per Paragraph 4.5.2.1.

4.5.2.3 To confirm that the sample of Paragraph 4.5.2.1 remains representative of cells from subsequent lots, a sample of 50 cells from each lot shall be selected in a random manner proportional to the distribution of the lot and electrical performance (I-V curve) determined under 2800°K color temperature tungsten illumination. Electrical performance (I-V curve) of the 50 cell sample shall also be determined under the solar simulator light source of Paragraph 4.5.2.1 which has been set using the 100 secondary standard solar cells, and a ratio (R) determined between the average of short-circuit-current of the 50 cell sample measured under the two light sources. The ratio (R) for each lot shall not

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deviate from the ratio (R) for the lot from which the 100 cell sample was selected by more than two percent. Greater deviation shall require selection of a replacement 100 cell sample from the current lot per Paragraph 4.5.2.2.

4.6 Type Approval Tests - Type approval tests, when required by the Statement of Work, shall be conducted in the manner described below and prior to initial cell deliveries. A sample of 100 solar cells with coverglass shall be selected at random from a production lot. When two or more test cells fail to meet the requirements of this specification, the extent and cause of failure shall be determined and corrective action initiated. After corrective action has been taken, type approval and acceptance tests shall be repeated as required based upon review of the failure analysis by HAC and the Seller. Cells subjected to type approval tests shall not be used for flight hardware but shall be deliverable to the Buyer at completion of TAT. The solar cells shall be subjected to type approval tests in the order listed below. Each test shall be performed on the entire 100-cell sample unless otherwise noted. Degradation of the sample average power output shall not exceed 2 percent at completion of TAT program.

4.6.1 Initial Tests - All solar cells selected for the type approval test program shall first be subjected to acceptance tests in accordance with Paragraph 4.5 including sub-paragraph 4.5.2 and meet all the requirements of Section 3.0 including sample average power output and cell minimum power output.

4.6.2 Intensity Variation - The Seller shall provide test data on 50 sample cells from the first lot to establish the voltage-current characteristic of the cells at 100, 115, 130, and 150 milliwatts per square centimeter illumination intensities. The cells shall be maintained at 25° C throughout the test. The illumination source shall be calibrated using the cells and data obtained from the tests of Paragraph 4.5.2. Light intensity shall be preset to achieve a proportionate increase in the test cells short circuit current. A Certificate of Compliance shall be provided for all subsequent lots.

4.6.3 Temperature Variations - The Seller shall provide test data (I-V curves) on 50 sample cells from the first lot to determine the voltage-current characteristics of the cells at -50° C, 0° C, 50° C and 100° C. The tests shall be run with a constant illumination source as specified in Paragraph 3.2.1 or HAC-approved alternate. A Certificate of Compliance shall be provided for all subsequent lots.

4.6.4 Temperature and Humidity - The test specimens shall be placed in a sealed test chamber and the temperature and humidity raised during a 2-hour period to 52° C and 95 percent relative humidity, respectively. At the end of a 6-hour soak period, the heat source for the chamber will be turned off. During the following 16-hour period, the temperature shall drop at a uniform rate to 37° C or less. Three such 24-hour cycles shall be performed consecutively. At the end of this period, electrical performance tests in accordance with Paragraph 4.5.2 shall be conducted and the requirements of Paragraph 3.2 shall be met using a laboratory light source calibrated per Paragraph 4.5.2.

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4.6.5 Thermal Shock - The solar cells shall be subjected to five temperature cycles at a minimum thermal rate of 30°C per minute between the extremes of $140 \pm 10^{\circ}\text{C}$ or above and $-126 \pm 10^{\circ}\text{C}$ or below. The solar cells shall remain at the extremes for a minimum of one hour. Electrical performance tests in accordance with Paragraph 4.5.2 shall then be conducted and the requirements of Paragraph 3.2 shall be met using a laboratory light source calibrated per Paragraph 4.5.2.

4.6.6 High Temperature-Vacuum - The solar cells shall be placed in a test chamber and the chamber reduced in pressure to a vacuum of at least 10^{-5} Torr. The temperature shall be raised to $140^{\circ} \pm 10^{\circ}\text{C}$. The solar cells shall remain in the chamber for a period of 168 hours. At the end of this period, the cells shall be allowed to return to room ambient temperature and the electrical performance tests in accordance with Paragraph 4.5.2 shall be conducted and the requirements of Paragraph 3.2 shall be met using a laboratory light source calibrated per Paragraph 4.5.2.

4.6.7 Ultra-Violet Radiation Test - Fifteen of the 100 type approval solar cells shall be subjected to high intensity ultra-violet radiation from a Model No. 700-J Ultra Violet lamp unit manufactured by Shannon Luminous Materials Company, Hollywood, California, or the equivalent. The cells shall be positioned normal to the irradiation with the active cell areas facing the illuminating source. The cells shall be positioned about the centerline of the lamp unit at a distance of approximately $3\frac{1}{2}$ inches from the open end of the lamp housing. Forced air cooling shall be employed to maintain the cells at a temperature in the range 40° to 50°C . Duration of the test shall be 200 hours. Upon completion, the cells shall be tested for electrical performance in accordance with Paragraph 4.5.2 and the requirements of Paragraph 3.2 shall be met using a laboratory light source calibrated per Paragraph 4.5.2. In lieu of performing the ultraviolet radiation test the Seller may provide sufficient evidence and certification that similar solar cells employing the same materials of construction have satisfactorily completed the test.

4.6.8 Paragraph 3.1.2 and 3.2 shall apply after each test in paragraphs 4.6.4, 4.6.5, 4.6.6 and 4.6.7.

4.7 Retest - Any changes made unilaterally by the supplier in manufacturing techniques, processes, materials, quality control levels, manufacturing sites or type of manufacturing equipment shall be cause for complete retest per Paragraph 4.6 at no cost to HAC.

4.8 Hughes Aircraft Company Tests - If after receipt by Hughes, a number of solar cells prove defective, such as to indicate a vendor process control problem, the individual cells or the entire lot may be rejected.

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5.0 PREPARATION FOR DELIVERY

5.1 Shipping Container - The Seller shall provide containers of the size required for the delivery lots with a desiccant quantity capable of assuring container ambient relative humidities of no greater than 30 percent in compliance with the requirements of Paragraph 3.3.1A. Solar cells may be packaged in an area with an ambient relative humidity no greater than 50 percent provided that the desiccant capability will reduce the relative humidity inside the container to a level no greater than 30 percent within a time period not to exceed 48 hours. The Seller shall demonstrate the suitability of the relative humidity capability of the desiccated container during packaging of the initial delivery lots. Desiccant may be replaced by Seller periodically, if necessary. An indicator of desiccant water absorption shall be provided. All materials used in the shipping container shall be non-flaking and non-shredding. Cells will be packed in cell trays within the shipping container. Trays will be supplied by H. A. C. The tape used in bundling the trays together shall leave no residue.

5.2 Identification - Each solar cell shipping box shall be legibly identified by the following:

- a) HAC Part Number (Specification and Drawing Number)
- b) Seller's Part Number
- c) Month and year of manufacture
- d) Lot number
- e) Category (refer to Paragraph 3.2)
- f) HAC Purchase Order Number

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6.0 QUALITY ASSURANCE PROVISIONS

6.1 General - The materials, processes and assembly covered by this specification shall be subject to extensive inspection and testing by both the Seller and HAC.

6.2 Inspection

6.2.1 Seller Inspection - Product quality assurance shall be provided by the Seller by a series of in-process inspections commencing with receipt of raw materials, and parts and continuing through the finished product. The selected inspection points shall have the approval of HAC. A record shall be maintained of all inspection and be subject to review by HAC.

6.2.2 HAC Source Inspection - The Hughes Aircraft Company shall at its option provide inspection to adequately monitor the Seller's quality control effort including in-process inspection and in-process tests. The complete hardware may be source inspected by HAC to assure that the product conforms to all the requirements specified on the applicable drawings and specifications and may include witnessing of acceptance tests.

6.2.3 Rejected Assemblies - Rejected assemblies shall not be resubmitted for approval without furnishing full particulars concerning the rejection, the measure taken to overcome the defects, and the prevention of their future occurrence. Each rejected assembly shall be identified by a serialized rejection tag. This rejection tag shall not be removed until rework requirements have been complied with, and the tag shall be removed only by, or in the presence of, an authorized representative of HAC.

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1.0 SCOPE

This specification provides the requirements for the design and construction of covers for blocking solar cells to be used on spacecraft solar panel assemblies. The blocking solar cell covers shall be capable of being bonded to blocking solar cells with a suitable adhesive.

This specification applies to second surface Al mirrors to be manufactured for use as thermal control devices on space vehicles. Since this device may be used in hardened applications, all chemical elements must be of low Z material.

1.1 Design Requirements

The blocking solar cell cover shall be designed to meet all requirements specified herein. Test programs shall be successfully completed demonstrating the ability of the blocking solar cell cover to meet all performance requirements of this specification. The blocking solar cell cover shall be designed for optimum operation in accordance with the following relative priority list:

- 1) Reliability
- 2) Thermal Characteristics, i.e., low α and high ϵ
- 3) Radiation hardness
- 4) Weight

1.2 Materials, Parts and Processes

When a material, part or process is not specified herein, the Seller's selection shall assure the highest uniform quality and condition of the product suitable for the intended use, and such selection shall be submitted for the review and concurrence of HAC, with the exception of such materials, parts and processes involving information proprietary to the Seller, in which case the Seller shall provide suitable documents showing specification compliance.

Any change in materials, parts, process or manufacturing area shall require the prior approval of HAC. HAC may require that additional testing be performed, at no cost to HAC, prior to granting approval of any vendor-negotiated change request.

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2.0 APPLICABLE DOCUMENTS

The following documents form a part of this specification to the extent referenced herein:

MIL-O-13830A	Military Specification "Optical Components for Fire Control Instruments; General Specification Governing the Manufacture, Assembly, and Inspection of"
MIL-C-675A	Military Specification "Coating of Glass Optical Elements"
MIL-M-13508B	Military Specification "Mirrors, Glass, Front Surfaces Aluminized, for Optical Elements"

Hughes Aircraft Company Drawings

X 33 54450 (latest revision)	HAC Control Drawing of Blocking Solar Cell Cover
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3.0 REQUIREMENTS

3.1 Design Description

The blocking solar cell cover shall be fabricated from Corning Glass Works No. 7940 synthetic fused silica, industrial grade.

- 3.1.1 Configuration. The dimensions and overall configuration of the cover shall be as shown on the applicable HAC Source Control Drawing. The Seller shall submit any detailed drawing(s) on the cover for HAC approval.
- 3.1.2 Material. The mirrors shall consist of an aluminum coating, vapor deposited on one surface of fused silica. This coating shall be overcoated to protect it from degradation.
- 3.1.3 Surface Quality. Surface quality shall be 80-50 per MIL-O-13830A.

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- 3.1.4 Geometrical Tolerances. Mirror substrates shall be fabricated to the following tolerances:

Dimensional Tolerance

- | | |
|------------------------------|-------------------------------------|
| 1) Length | ± 0.002 inch |
| 2) Width | ± 0.002 inch |
| 3) Thickness | ± 0.002 inch |
| 4) Perpendicularity of sides | $90^\circ \pm 15'$ |
| 5) Edge Chips | 0.010 inch max projection into face |
| 6) Parallelism of sides | ± 0.002 inch |

- 3.1.5 Corner Chips. Corner chips shall not exceed 0.020 inch on either leg or extend more than 0.015 inch into the face of the cover.

- 3.1.6 Bubbles. Closed bubbles of 0.005 inch maximum diameter and open bubbles no greater than .003 inch shall be acceptable.

Included bubbles of less than .005 inch diameter shall be discounted. The allowable number of bubbles of the maximum size specified shall not exceed two for an equivalent 1 x 1 cm area.

Cracks will not be allowed.

- 3.1.7 Appearance. The coated surface, when observed through the substrate (face) by the unaided eye, shall give the appearance of uniform coverage. The uncoated surface shall be free of all metal deposition and other contamination. The overcoated surface (back) shall have a distinct color when viewed under white light.

- 3.1.8 Optical Properties (Face).

Absorptance (a_s) of incident radiation having distribution corresponding to the Johnson Solar Distribution shall not exceed 0.13 when integrated between 0.28μ and 2.5μ .

The total specular reflectance from the face ($\bar{R}$) shall be used to calculate a_s using the following formula:

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$$\alpha_s = \frac{\int_{0.28\mu}^{2.50\mu} (1-R\lambda) S\lambda \cdot d\lambda}{\int_{0.28\mu}^{2.50\mu} S\lambda \cdot d\lambda}$$

Where the $R\lambda$ is the measured reflectance at the wavelength λ , $S\lambda$ is the value of the Johnson Solar constant at wavelength λ , and $d\lambda$ is the wavelength interval over which the integration is made.

3.1.9 **Weight.** Average cover weight per lot shall not exceed that specified on the Hughes Source Control Drawing.

3.2 **Environmental Performance**

The covers shall meet all requirements of this specification after being exposed to the following tests

3.2.1 **Coating Adherence.** The coating shall not separate or show evidence of separation from the substrate after being immersed in boiling distilled water for 5 minutes and then tested using cellulose tape conforming to LT-90-C (Ref: MIL-M-13508, Para. 4.4.6).

3.2.2 **Humidity Resistance.** The coated parts shall show no evidence of degradation when tested in a thermostatically controlled humidity chamber having a relative humidity of between 95 and 100 per cent and a temperature of $120^\circ \pm 4^\circ\text{F}$ for a period of 24 hours. (Ref. MIL-C-675, Para. 4.4.6).

3.2.3 **Coating Hardness.** The coating shall show no evidence of degradation when rubbed a minimum of 50 strokes in straight lines or circular motions with a pad of clean dry cheesecloth conforming to CCC-C-271, approximately 3/8 inch diameter and 1/2 inch thick, bearing with a force of 1 pound minimum on the coated surface (Ref: MIL-M-13508, Para. 4.4.5).

3.2.4 **Temperature Cycle.** The coating shall withstand being cooled to the temperature of liquid nitrogen, be retained at this temperature for 1 hour, and subsequently heated to $175^\circ \pm 10^\circ\text{C}$, and retained at this elevated temperature for a period of 1 hour.

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3.2.5 High Temperature Vacuum. The coating shall withstand exposure to a temperature of $140^{\circ} \pm 10^{\circ} \text{C}$ and a pressure of $1 \times 10^{-5} \text{mm Hg}$ or less for a period of 168 hours.

3.3 Storage. The blocking solar cell cover shall be capable of meeting the storage requirements when stored in the unopened package as delivered by the supplier as follows:

- 1) Storage at a relative humidity of 50 percent maximum and a storage temperature of $21 \pm 15^{\circ} \text{C}$ for a period of 24 months.
- 2) Storage at a relative humidity of 95 percent and at a storage temperature of $24 \pm 20^{\circ} \text{C}$ for a period of one month.

3.4 Operational Life

The blocking solar cell cover shall be designed for a minimum operational life of 7 years in the space environment.

3.5 Interchangeability

Blocking solar cell covers bearing the same part number shall be physically and functionally interchangeable without selection or fit. The HAC part number for these blocking solar cell covers shall be that shown on the Source Control Drawing.

3.6 Cleanliness

The covers as received from the Seller, with no other cleaning by the Buyer, shall be free of all wax or other contamination which may interfere with adhesive bonding of the cover to the solar cell, or which may degrade optical properties when exposed to the space environment.

4.0 TESTS

4.1 General

4.1.1 Test Apparatus. All meters, scales, thermometers, and similar measuring test equipment used in conducting tests specified herein shall be accurate within one percent of the full-scale value. Full-scale deflection of meters should not be more than twice the maximum value of the quantity being measured. All test apparatus

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shall be calibrated at suitable intervals and records of such calibration shall be available for inspection by HAC. HAC may examine the Seller's test equipment and determine that the Seller has available and utilizes correctly, gauging, measuring and test equipment of the required accuracy and precision, and that the instruments are of the proper type and range to make measurements of the required accuracy. The calibration of gauges, standards, and instruments shall be checked in a mutually agreed upon primary standards laboratory; if disputes concerning performance occur, cost of checks shall be borne by Seller.

4.1.2 Test Records. Records shall be kept of all tests and of applicable manufacturing data and these records shall be made available for inspection by HAC. Prior to and following each test of Paragraph 4.4, a thorough visual examination of the test cover shall be conducted. All unusual physical markings, defects, and other visual characteristics shall be noted and recorded as a portion of the test records.

4.1.3 Test Conditions. Unless otherwise specified herein, all tests shall be performed at the following nominal ambient conditions:

- 1) Temperature $25^{\circ} \pm 5^{\circ}\text{C}$
- 2) Relative Humidity No greater than 50 percent

4.2 Sampling Procedures

Five parts per manufacturing lot will be sampled. Manufacturing lot is equivalent to coating lot or coating batch.

4.3 Test Location. Unless otherwise specified in the contract, acceptance tests shall be performed by the Seller at the Seller's plant. If the use of outside test facilities are required, the use of these facilities, shall be subject to approval by HAC. HAC shall have the right to witness, inspect, and review all acceptance tests.

4.4 Acceptance Tests. A shipping lot shall nominally consist of 500 to 10,000 covers, except special lot sizes, manufactured under essentially the same conditions and submitted for acceptance at substantially the same time. Acceptance tests shall be performed on each manufacturing lot.

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4.4.1 Individual Acceptance Tests

4.4.1.1 Dimensional Tolerances. All mirrors shall be inspected for conformance to the dimensional tolerances specified in Paragraphs 3.1.1, 3.1.4, 3.1.5 and 3.1.6. Any instrumentation used for inspection shall be capable of measuring the accuracy stated.

4.4.1.2 Surface Quality. All mirrors shall be visually inspected per MIL-O-13830A for conformance to the surface quality specified in Paragraph 3.1.3.

4.4.1.3 Appearance. All mirrors shall be inspected visually for conformance to Paragraph 3.1.7. Inspection will be conducted using white light reflected from each surface and without magnification.

4.4.2 Lot Acceptance Tests. For lot acceptance test purposes, each coating batch shall be considered to be a lot. Unless otherwise indicated by the appropriate test paragraph, separate groups of parts may be selected for each test.

4.4.2.1 Optical Properties (Face). The optical properties from the face of the mirror shall be measured at an angle of 8° from the normal and shall meet the following:

<u>Wavelength in Microns</u>	<u>Minimum Reflectance (percent)</u>
0.38	87 percent
0.475	88 percent
1.0	90 percent

Spectral measurements will be made on a minimum of three samples of appropriate size. A Cary 14 Spectrophotometer shall be used to conduct these measurements. Mirrors which do not meet the above reflectance values may be re-evaluated using the formula of Paragraph 3.1.8. The mirrors will be considered acceptable providing they meet the solar absorption requirements of Paragraph 3.1.8.

4.4.2.2 Coating Adherence. Five samples from each coating batch shall be immersed in boiling distilled water for a period of between 4 and 6 minutes. After this time period, the parts shall be removed from the water and the adhesive surface of a length of 3M Type 600 Cellulose Tape shall be applied to the coated surface of the mirror. The tape shall be applied so that it extends over the test part edges. The applied tape shall be set by rubbing the back. Holding the mirror so it will not break, the tape is removed from the mirror surface by quickly pulling at an oblique angle to the mirror surface.

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The metallic coating shall show no signs of delamination or separation with the substrate.

For the lot to be accepted, all samples tested must meet the requirements specified in Paragraph 3.2.1. If a failure occurs, an additional four samples from the same batch will be tested; any failure in the second lot shall be cause for rejection of the entire batch. Slight imperfections, such as pinholes, are not to constitute cause for rejection.

4.4.2.3 Humidity Resistance. Five mirrors per coating lot shall be selected at random and submitted to the humidity test specified in Paragraph 3.2.2. Failure of any part to meet the requirements of Paragraph 3.2.2 shall constitute failure of this test.

4.4.2.4 Coating Hardness. Five mirrors previously tested per Paragraph 4.4.2.3 shall be tested per Paragraph 3.2.3. Failure of more than one part to meet the requirements of Paragraph 3.2.3 shall constitute failure of this test.

4.4.2.5 Certification of Thermal Cycling. Certification of compliance to the requirements of Paragraph 3.2.4 shall be supplied with each shipping lot. Certification may be used in lieu of test.

Five parts per shipping lot shall be submitted to the following tests:

The temperature cycling test shall consist of three complete cycles, per Paragraph 3.2.4. The rate of temperature change shall be not less than 2°C per minute. During the test, no condensation shall be allowed to form on the mirror. Mirrors shall comply with the requirements of Paragraph 3.2.1 after completion of this test.

4.5 Confirmation of Optical Properties

Following all tests in Paragraph 4.4, the sample shall conform to Paragraph 3.1.8. HAC, at its option, will conduct tests on delivered covers. Any covers determined during HAC tests to be defective in such a manner as to indicate "out-of-control" process shall be cause for rejection of the entire lot.

4.6 Retest

Any change made unilaterally by the Seller in manufacturing techniques, processes, materials, quality control levels, manufacturing sites or type of manufacturing equipment shall be cause for complete retest for affected lots per Paragraph 4.4 at no cost to HAC.

4.7 Test Samples

Acceptance test samples shall not be shipped to fulfill contract quantities. The samples shall be identified and retained for a period of three months.

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5.0 PREPARATION FOR DELIVERY

5.1 Packaging

Each mirror shall be individually wrapped in paper that will not scratch, leave a residue, corrode the metal surface, or interfere with cell bonding. These shall be placed in containers that will prevent damage during shipment. Containers shall contain mirrors from only one lot.

5.2 Marking

1) Each individual container shall be permanently and legibly marked with the lot number, followed by the total number (in parenthesis) of individual mirrors in the container.

2) With each lot, the following information shall be supplied:

Customer part number
Mirror lot number
Number of individual mirrors per lot
Total number of containers in lot
Date of manufacture
Substrate material
Certificate of compliance

5.3 Shipping Container

The Seller shall provide containers of the size required for the delivered lots with a desiccant capable of assuring container ambient relative humidities of no greater than 50 percent. Desiccant may be replaced by Seller periodically, if necessary. An indicator of desiccant water absorption shall be provided. All materials used in the shipping container shall be non-flaking and non-shredding.

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6.0 INSPECTION

6.1 General

The materials, processes, and assembly covered by this specification shall be subjected to extensive inspection and testing by both the Seller and HAC.

6.2 Inspection

6.2.1 Seller Inspection. Product quality assurance shall be provided by the Seller by a series of in-process inspections commencing with receipt of raw materials and parts, and continuing through the finished product. The selected inspection points shall have the approval of HAC. A record shall be maintained of all inspection and be subject to review by HAC.

6.2.2 HAC Source Inspection. The Hughes Aircraft Company shall at its option provide inspection to adequately monitor the Seller's quality control effort including in-process inspection and in-process tests. The complete hardware may be source inspected by HAC to assure that the product conforms to all the requirements specified by the applicable drawings and specifications and may include witnessing of acceptance tests.

6.2.3 Rejected Assemblies. Rejected assemblies shall not be resubmitted for approval without furnishing full particulars concerning the rejection, the measure taken to overcome the defects, and the prevention of their future occurrence. Each rejected assembly shall be identified by a serialized rejection tag. This rejection tag shall not be removed until rework requirements have been complied with, and the tag shall be removed only by, or in the presence of, an authorized representative of HAC.

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DEVELOPMENT CHANGE NOTICE		HUGHES PROPERTY OF HUGHES AIRCRAFT COMPANY CODE IDENT 82577		DCN 245251	REV LTR
		SHEET 1 OF 1			
PROGRAM	SYS/EQUIP NAME OR DESCRIPTION		CONTROL ITEM NAME AND NUMBER		
HS-229	Blocking Solar Cell		Coveralide		
ENGINEERING DRAWINGS AND SPECIFICATIONS					
NUMBER	NEW	D.V. CHG	DE-LETE	ADV CHG	
XPS 30964-025		X			

DESCRIPTION OF CHANGE

1) Para 3.2.2

IS: - - - having a relative humidity of between 95 and 100 per-cent and a temperature of $120^{\circ} \pm 4^{\circ} F$ for a period of 24 hours. (Ref. MIL-C-675, Para. 4.4.6).

WAS: - - - having a relative humidity of between 95 and 100 per-cent and a temperature of $120^{\circ} \pm 4^{\circ} F$ for a period of 72 hours. (Ref. MIL-C-675, Para. 4.4.6).

2) Para 4.4.2.5

IS: Certification of Thermal Cycling. Certification of compliance to the requirements of Paragraph 3.2.4 shall be supplied with each shipping lot. Certification may be used in lieu of test.

WAS: Certification of Thermal Cycling. Certification of compliance to the requirements of Paragraph 3.2.4 shall be supplied with each shipping lot.

REASON FOR CHANGE

Update specification requirements

CLASS D-I CRITERIA									
AFFECTS FUNCTIONAL OR ALLOCATED CONFIGURATION IDENTIFICATION	YES	NO	MAKES A CONTROL ITEM NON-INTERCHANGEABLE	YES	NO	AFFECTS A CONTROL ITEM OR SYSTEM INTERFACE	YES	NO	
		X			X				X
CAUSES A CHANGE TO TWO OR MORE CONTROL ITEMS WITH DIFFERENT REAS		X	CAUSES SIGNIFICANT CHANGE IN COST		X				
AFFECTS THE SYSTEM OR ANOTHER PRODUCT MODEL		X	DELAYS DELIVERY OF A CONTROL ITEM		X				
CHANGE CLASS	☐ D-I ☒ D-II		CHANGE EFFECTIVITY	DISPOSITION OF ITEMS		CUSTOMER APPROVAL REQUIRED		YES	NO
			Ser. No. 1 and Up	N/A				☐	☒
APPROVALS									
PREPARED BY	ORG CODE	DATE		ORG CODE	DATE	PROGRAM MANAGER	ORG CODE	DATE	
<i>F. H. H. H.</i>	41-15-20	9/24/73	<i>E. L. H. H.</i>	41-15-20	9/24/73				
CHECKED BY						AUTH FOR RELEASE			
<i>R. W. G. H.</i>	41-15-20	11/15/73							
RESPONSIBLE ENGINEER						RELEASED BY			
<i>R. W. G. H.</i>	41-15-20	9/24/73				<i>H. H. H. H.</i>	41-15-20	9/24/73	

HUGHES HUGHES AIRCRAFT COMPANY SPACE AND COMMUNICATIONS GROUP	T. E. SYSTEM SPECIFICATION, QUALIFICATION AND ENVIRONMENTAL TEST, REVERSE CURRENT BLOCKING DIODES FOR FLEXIBLE SOLAR ARRAY PROTECTION	NUMBER TS 30964-026	REV —			
		CODE IDENT NO. 82577	TOTAL PAGES 10			
RELEASED PRINT RESPONSIBLE ENGINEERING ACTIVITY REA ORG CODE 41-15-30 <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 20%; text-align: center;">— REV</td> <td style="width: 40%; text-align: center;">8-6-74 REL DATE</td> <td style="width: 40%; text-align: center;">N.F. REL BY</td> </tr> </table>				— REV	8-6-74 REL DATE	N.F. REL BY
— REV	8-6-74 REL DATE	N.F. REL BY				
INITIAL APPROVALS						
<i>E. Levy Jr</i>	DATE	8/9/73	DATE			
<i>H. F. Changue Jr</i>	DATE	8/6/74	DATE			

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1.0 SCOPE

This qualification and environmental test specification establishes the performance parameters, test setups, test procedures, data requirements and data analysis for evaluating the performance of the reverse current blocking diode for flexible solar array protection.

2.0 APPLICABLE DOCUMENTS

None.

3.0 OVERALL TEST APPROACH

The overall test approach for the reverse current blocking diode consists of evaluation and radiation tests on preproduction samples, acceptance tests of production cells at the cell vendor, qualification tests of cells at both the cell vendor and at Hughes Aircraft Company, and environmental tests of cell coupons at Hughes Aircraft Company. All tests are listed below:

1) Evaluation Tests

Workmanship
Electrical Characteristics
Temperature Extremes
Weldability/Solderability

2) Radiation Tests

3) Acceptance Tests

Visual and Mechanical
Weight
Forward Voltage Drop
Forward Current
Reverse Voltage

4) Qualification Tests

Type Approval Tests
Temperature and Humidity
Thermal Shock
High Temperature Vacuum
Vibration
Endurance

5) Environmental Tests

Mechanical Pull Test
Roll Up Test
Vacuum Chamber Test
Temperature Cycling Test

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This specification defines Items 4 and 5 of the tests listed above, namely the Qualification and Environmental Tests.

4.0 FUNCTIONAL TESTS

4.1 Diode Voltage Drop

Purpose. - This test is designed to measure the voltage in the forward direction, across the device under the specified conditions.

Test Setup. - This test shall be run using a Tektronix 575 or equivalent curve tracer.

Procedure. - The current sweep is adjusted to obtain the specified values of forward current of 0.3 and 3.0 amperes. The forward voltage is read when the forward current equals the specified values.

Summary

- a) Test Current at 0.3 and 3.0 amperes.
- b) Voltage Readings at $25^{\circ} \pm 2^{\circ}\text{C}$:
 - 0.8V maximum at 0.3 amperes.
 - 1.2V maximum at 3.0 amperes.

4.2 Reverse Current and Reverse Voltage

Purpose. - This test is designed to measure the voltage and current, in the reverse direction, through the device.

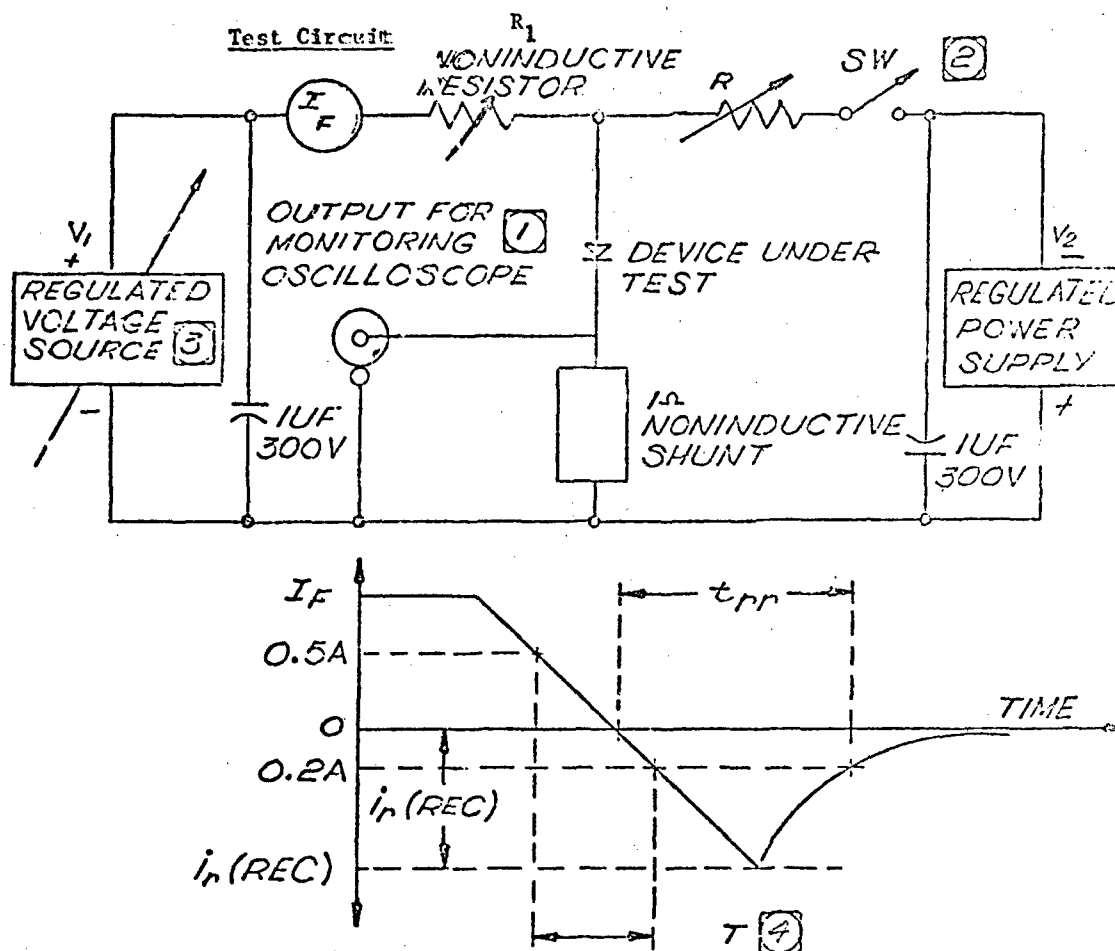
Test Setup. - This test shall be run using a Tektronix 575 or equivalent curve tracer.

Procedure. - The voltage sweep is adjusted to obtain the specified value of reverse voltage across the device. The reverse current is then read from the current axis.

Summary

- a) Test Voltages: 50, 100, 200V.
- b) Test Currents at $25^{\circ} \pm 2^{\circ}\text{C}$:
 - 0.1 milliamperes maximum at 80 volts
 - 0.2 milliamperes maximum at 120 volts
 - 1.0 milliamperes maximum at 140 volts

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NOTES:

- 1 Monitoring oscilloscope requirements: $t_r \leq 14 \mu\text{sec}$, $R_{in} \leq 9 \text{ megohm}$, $C_{in} \leq 12 \text{ pf}$, $L_{in} \text{ (series)} \leq 0.5 \mu\text{h}$.
- 2 Switch (SW) characteristics: Mercury-wetted make before-break relay switch at rate. The relay should conduct for approximately 640 μsec and be open for approximately 7.7 msec. (C.P. Clare HCP 1004 or equivalent).
- 3 Voltage source characteristics: Output impedance $\leq 0.5 \text{ ohm}$ from 0 to 2 kHz.

System Specification
Qualification and
Environmental Test

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4.3 Reverse Recovery Time

Purpose. - The purpose of this test is to measure the reverse recovery time by observing the reverse transient current through a specified load resistance on switching from a specified forward bias to a specified reverse bias.

Procedure. - Adjust V1 and R1 for a forward diode current of 1.5 amperes. Adjust R2 & V2 for a reverse current of 4 amps with the diode shorted. Read the reverse recovery time t_{rr} on the oscilloscope.

Summary

Forward Current = 1.5A
Temperature = $25^{\circ} \pm 2^{\circ}\text{C}$
 $t_{rr} \leq 3 \mu\text{sec}$

5.0 DIODE QUALIFICATION TESTING

Diode qualification tests will be performed partly by the cell vendor and partly by Hughes. Qualification tests as listed below:

Vendor Tests (20 cells total, 10 aluminum contact, 10 silver-titanium contact)

- 1) Temperature and Humidity
- 2) Thermal Shock
- 3) High Temperature Vacuum

Hughes Tests

- 1) Vibration
- 2) Endurance Test

Each of the planned qualification tests is described below.

5.1 Vendor Tests

5.1.1 Temperature and Humidity

Purpose. - This test is performed for the purpose of evaluating the performance of the diode after long term exposure to a combined high temperature, high humidity environment.

Procedure. - The test specimens shall be placed in a sealed test chamber and the temperature and humidity raised $45^{\circ} \pm 5^{\circ}\text{C}$ and $95\% \pm 5\%$ relative humidity. The test specimens shall be exposed to this environment for 96 hours. At the end of this period, visual examination and the functional tests shall be conducted.

5.1.2 Thermal Shock

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Purpose of Test. - This test is performed to evaluate the ability of the diode to withstand a rapid temperature change between high and low temperature operating limits.

Procedure. - The cells shall be subjected to five temperature cycles at a minimum thermal rate of 30° per minute between the extremes of $90^{\circ} \pm 10^{\circ}\text{C}$ and $-196^{\circ} \pm 10^{\circ}\text{C}$. The solar cells shall remain at the extremes for one hour. Visual examination and the functional tests shall then be conducted.

5.1.3 High Temperature/Vacuum

Purpose of Test. - This test is performed to evaluate the combined environments of high temperature and vacuum on the diode performance.

Procedure. - The solar cells shall be placed in a test chamber reduced in pressure to a vacuum of at least 10^{-5} Torr. The temperature shall be raised to $140^{\circ} \pm 10^{\circ}\text{C}$. The solar cells shall remain in the chamber for a period of 168 hours. At the end of this period, the cells shall be allowed to return to room ambient temperature and pressure. The cells with silver-titanium contacts shall then be removed. Repeat the test for the cells with aluminum contacts, except that the temperature shall be raised to 200°C and the test conditions maintained for one hour. At the end of this period, the cells shall be allowed to return to room ambient temperature and pressure. All cells shall be visually inspected and electrically tested.

5.2 Hughes Tests - Vibration tests on blocking diodes shall be performed at Hughes and shall be accomplished with the blocking diodes interconnected to 3 x 4 solar cell arrays. The blocking diodes and solar cell arrays shall be bonded to a HASP type substrate per XPS 31456-011. The substrate shall be wound on the vibration test mandrel with a tension of $2.3\text{ lb} \pm 0.1\text{ lb}$. The blocking diode bonding, coverslide and cushioning shall be representative of a flight configured blocking diode assembly.

5.2.1 Vibration Test

Purpose - The vibration test is performed for the purpose of determining the effect of each of two differently oriented vibrations on component parts.

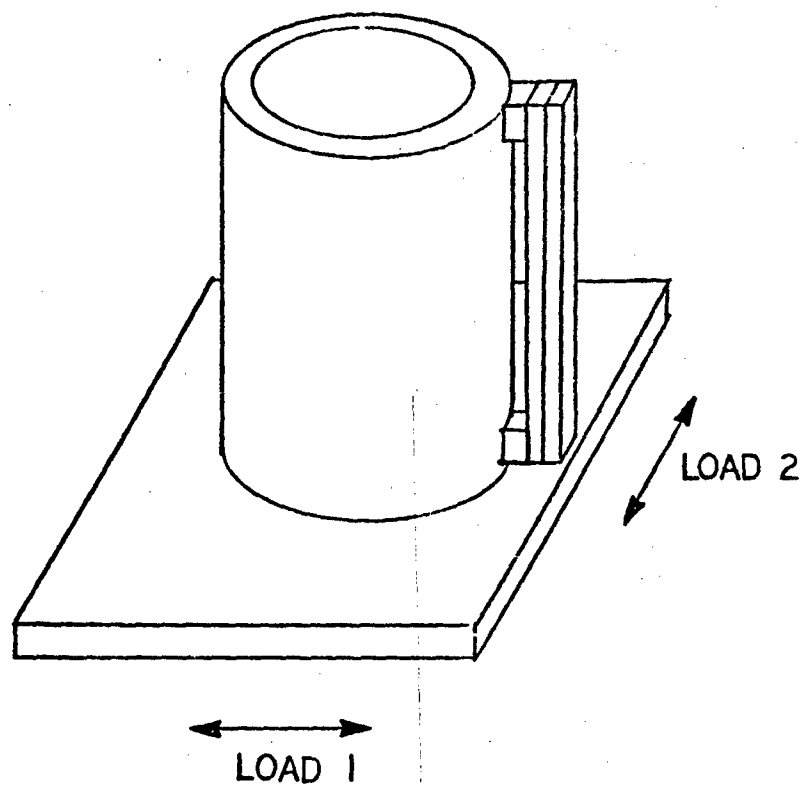
Procedure -

Orientation - The first oriented vibration shall be applied as shown in Figure 1 (LOAD 1) for a period of 3 minutes $\pm$ 15 seconds. The second oriented vibration shall be applied as shown in Figure 1 (LOAD 2) for a period of 3 minutes $\pm$ 15 seconds.

Amplitude - The vibration test shall be performed with a nominal peak acceleration of 20 g's.

Frequency - The vibration frequency shall be a nominal 50 HZ. A careful visual inspection shall be performed after the completion of both phases of the vibration test. All discrepancies shall be recorded. Electrical tests shall then be performed as specified in Paragraph 4.1 and 4.2.

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VIBRATION LOADS

FIGURE 1

System Specification,
Qualification and Environmental Tests

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5.2.2 Endurance Test

Purpose of Test - This test will determine the effects of a 1000 hour burn-in on the electrical characteristics of the diodes when subjected to the specified conditions.

Procedure. - The blocking cells will be subjected to a 1000 hour burn-in test where a maximum current of 3 amperes will be passed through each device while the device temperature is maintained at 95°C. Changes in the electrical characteristics as a function of time will be monitored and evaluated.

6.0 ENVIRONMENTAL TEST PROGRAM

This phase of the developmental test program will determine the compatibility of the diode as part of a solar array. Hughes will fabricate eight (8) flexible panel segments (four with integral aluminum contacted cells and four with silver-titanium contacted cells) for environmental testing. Each segment will consist of three cells in parallel by four cells in series with two redundant parallel blocking diodes in series with the solar cells. Included in this phase, which will be limited to approximately two (2) months, are the following environmental tests: mechanical pull strength test; roll-up tests on a simulated storage drum; thermal-vacuum testing, and temperature cycling tests in a non-vacuum. All tests will be conducted at HAC.

6.1 Mechanical Pull Test (5 Cells, Each Type)

Purpose of Test. - This test is designed to verify that a flight configured interconnect and cell combination has sufficient mechanical pull strength.

Test Apparatus. - This test will be performed using a Unitek Micropul Model 6-092-03 pull tester.

Procedure. - Solder or weld the interconnect material to the cell. After the connection has been made, slit the interconnect material into 100 mil wide sectors. Pull each of these sectors separately by clamping the cell to the pull tester frame and clamping the pull tester arm to the interconnect. Pull each sector until the interconnect breaks or the solder or weld joint gives. Record the pull at which the failure occurs.

6.2 Roll Up Test (One Sector, Each Type)

Purpose of Test. - This test is designed to verify that the diode, as connected in a typical array configuration will be capable of withstanding a large number of roll up operations.

System Specification	HUGHES AIRCRAFT CO.	9	—	TS 30965-026
Qualification and Environmental Test	CULVER CITY, CALIF.	SH NO.	REV LTR	NUMBER
	CODE IDENT NO. E2577			

Procedure. - Test samples shall be cycled 500 times. The test sample shall be loaded at 0.77 lbs. The samples shall be loaded in the series cell direction and rolled with the cells facing away from the roller. After completion of the test, the diodes shall be subjected to a visual examination and functional tests per Paragraph 4.1 and 4.2.

6.3 Vacuum Chamber Tests (One Aluminum Array Segment, One Silver-Titanium Array Segment)

Purpose of Test. - This test is designed to verify the thermal characteristics of the diodes when operating in a typical panel application with planned front and back shielding.

Test Circuit. - Same as shown for the forward voltage test.

Test Apparatus. - Thermal vacuum chamber and heaters.

Procedure. - Calibrate diode voltage versus temperature at 0.3, 0.4, 0.5, 0.6, and 0.7 amps by placing the diode in a controlled temperature chamber and recording the diode voltage from 100°F to 300°F in 20°F increments.

Then place the array segment in a vacuum chamber with LN₂ cold walls and heaters to simulate solar input. The chamber pressure shall be less than 10⁻⁵ Torr. Measure stabilized diode voltages with 0.3, 0.4, 0.5, 0.6, and 0.7 amps current. Calculate the diode operating temperature at each current.

Summary

Calibration Currents - 0.3, 0.4, 0.5, 0.6, and 0.7 amps.

Calibration Temperatures - 100° to 300°F.

Vacuum Chamber Pressure - 10⁻⁵ Torr.

Currents for Vacuum Measurements - 0.3, 0.4, 0.5, 0.6, and 0.7

6.4 Temperature Cycling Test (One Aluminum Diode Array Segment, One Silver-Titanium Diode Array Segment)

Purpose of Test. - This test is designed to verify the integrity of the interconnected diode under simulated temperature cycling.

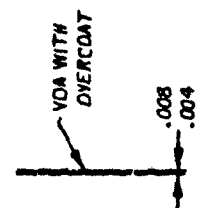
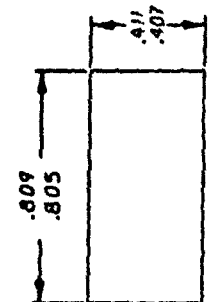
Test Apparatus. - This test will be run with the Hughes Automatic Temperature Cycling Tester.

Procedure. - A temperature cycling test consisting of 1000 temperature cycles will be conducted on two of the flexible panel segments. The test will consist of thermal cycling the two flexible panel segments between -196° ± 10°C to +90° ± 10°C. After every 200 cycles, the blocking diodes shall be subjected to a visual inspection and functional tests per Paragraphs 4.1 and 4.2.

System Specification Qualification and Environmental Test	HUGHES AIRCRAFT CO. CULVER CITY, CALIF. CODE IDENT NO. 82577	10 SH NO.	— REV LTR	TS 30964-026 NUMBER
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APPENDIX C. DIODE DRAWINGS

QTY	AUTHORITY	CONC'L	REVISIONS	DATE	APPROVED
			A REDRAWN WITH CHANGZ	11/1/73	11/1/73
			B SEE DCN 176677	11/1/73	11/1/73



- NOTES UNLESS OTHERWISE SPECIFIED
1. ITEMS PURCHASED TO THIS DRAWING SHALL COMPLY WITH HAC SPEC XPS 30964-025.
 2. SUBSTRATE MATERIAL TO BE CORNING GLASS WORKS NO T190 FUSED SILICA INDUSTRIAL GRADE.
 3. SECOND SURFACE AI MIRROR OC11 PROCESS NUMBER 8210008
 4. EDGES OF COVER TO BE PARALLEL WITHIN .002
 5. TOLERANCE ON ANGULARITY TO BE $\pm 0^\circ 15'$

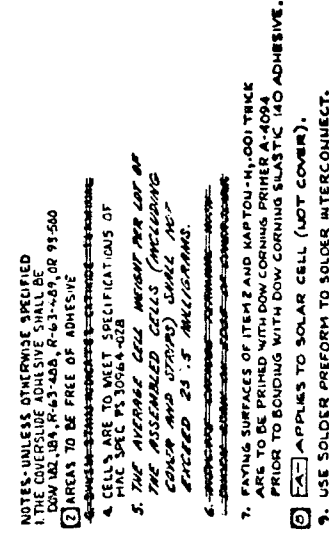
RELEASED PRINT
N5 229
11/1/73
11/1/73

QTY	CODE	PART NO. OR IDENTIFYING NO.	NAME	DATE
			MUGHES	11/1/73
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND FRACTIONS 1/16 1/8 3/16 1/2 3/4 1 1 1/2 2 3 4 5 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40 42 44 46 48 50 52 54 56 58 60 62 64 66 68 70 72 74 76 78 80 82 84 86 88 90 92 94 96 98 100 1/32 1/64 1/128 1/256 1/512 1/1024 1/2048 1/4096 1/8192 1/16384 1/32768 1/65536 1/131072 1/262144 1/524288 1/1048576 1/2097152 1/4194304 1/8388608 1/16777216 1/33554432 1/67108864 1/134217728 1/268435456 1/536870912 1/1073741824 1/2147483648 1/4294967296 1/8589934592 1/17179869184 1/34359738368 1/68719476736 1/137438953472 1/274877906944 1/549755813888 1/1099511627776 1/2199023255552 1/4398046511104 1/8796093022208 1/17592186044416 1/35184372088832 1/70368744177664 1/140737488355328 1/281474976710656 1/562949953421312 1/1125899906842624 1/2251799813685248 1/4503599627370496 1/9007199254740992 1/18014398509481984 1/36028797018963968 1/72057594037927936 1/144115188075855872 1/288230376151711744 1/576460752303423488 1/1152921504606846976 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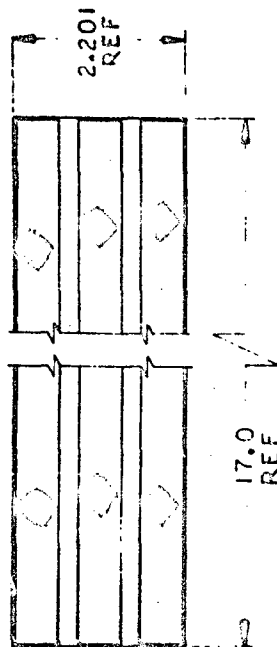
06-51-10 800 800 100
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Lester Thompson Program
1967-1970-8

MELTONIA DIV. OF TEXTRON ELEC. MFG. 5711 WASH. CIR. #1542 NEWTON, MASS. 01945	09732 TSD
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2. USE SOLDER PREFORM TO SOLDER INTERCONNECT.
 3. -A- APPLIES TO SOLAR CELL (NOT COVER).

AUTHORIZED BY ECA1761903



NOTES-UNLESS OTHERWISE SPECIFIED

1. SOLDER ELECTROPLATE .00001 TO .00007 THICK, SOLDER COMPOSITION SHALL BE 60 ± 10 PERCENT TIN AND THE REMAINDER LEAD.
2. IDENTITY PER HP 0-5, TYPE II

MAKE FROM 250000

BLANK, STRIP, SOLAR CELL

5205700