ELECTRONIC SENSOR PACKAGE AND DATA TRANSMISSION SYSTEM FOR PROJECT 'TELEPLANE'

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ELECTRONIC SENSOR PACKAGE AND DATA TRANSMISSION SYSTEM FOR PROJECT "TELEPLANE"

Information Transmission Branch
System Avionics Division

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August 1975

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A functional and detailed description of an electronic data system to be utilized in a Remotely-Piloted-Vehicle (RPV) test environment.

It includes descriptions of a basic electronic sensor package; a digital data transmission system and its signal structure; and an associated receiving/decoding scheme.

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FOREWORD

This report has been prepared by Project Engineer Kenneth E. Ayers to describe an Air Force Avionics Laboratory effort, accomplished in direct co-operation with Flight Dynamics Laboratory's Project Teleplane.

The effort was initiated in the course of evaluating an inexpensive Remotely-Piloted-Vehicle (RPV) System, when Project Teleplane discovered a need to have certain parameters of flight data presented to the ground, via radio link.

The Technical Support Group for the Information Transmission Branch was given the task of designing a package to sense the required parameters and transmit the information from the RPV to a fixed receiving station.

It is the purpose of this report to provide both a functional and detailed description of the circuitry used to accomplish this end.

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I. BACKGROUND

In the search for a reliable, expendable (and therefore inexpensive) weapon system, the Remotely-Piloted-Vehicle (RPV) appears as a natural choice. With the operator located safely on the ground, controlling the mission via radio link, all human factors such as life support systems and egress systems, may be removed as constraints upon the overall system. The result is a considerable reduction in size and cost, as well as the virtual elimination of risk to the "pilot."

However, to effectively operate such a vehicle, it is imperative that specific parameters, pertaining to powered flight, be made available to the "pilot." Examples of such parameters are heading, airspeed, and altitude, not to mention the visual information necessary for locating geographical references and targets. These requirements naturally imply that the vehicle have some form of communications link with its operator.

The problem of providing visual data has been solved by mounting a television camera in the nose and directing its "field of vision" by a radio link identical to the one used to control the vehicle.

The purpose of this report is to describe the system used to relay the additional data that is needed for effectively executing a mission.

II. REQUIREMENTS

The initial requirements were for a system that would transmit, on a single narrowband radio channel, the following parameters:

PARAMETER	RANGE
Altitude	0-2000 ft
Airspeed	0-200 knots
Engine RPM	0-10,000 RPM
Heading	0-359°

Power Consumption and Space requirements were not explicitly defined, but were to be consistent with general requirements for airborne equipment, i.e., low power and smallest practical size.

The data transmission was to occupy a Single RF Channel with a 3-KHz bandwidth, and for the purposes of psychological evaluation by the Aerospace Medical Laboratories, data was to be displayed in both an analog and a digital format.

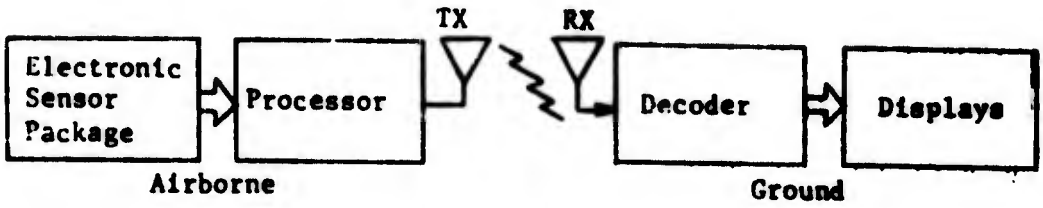

Figure 1. System Block Diagram

The system can be divided into the four basic functional blocks shown in Figure 1: the Sensor Package, a sensor processor and transmitter, a receiver and decoder, and the display package.

All of the parameters are converted, by the Sensor Package, into 0-10V analog signals and fed into the signal processor. Here the signals are multiplexed and converted into a digital format for transmission.

In the ground based portion of the system, the received digital signal is applied to the decoder where the data is recovered, de-multiplexed, and converted back to an analog output, which is fed into the display unit.

III. THE ELECTRONIC SENSOR PACKAGE (Circuit Description)

The Sensor Package consists of four sensors, on three printed circuit cards, two of which are identical.

One card contains the circuitry for an electronic barometric altimeter and an ambient temperature sensor. The other two cards are electronic tachometers ——— one being used directly as an engine RPM sensor and the other, used in conjunction with a propeller-driven generator, senses airspeed.

Each sensor is scaled such that its output is an analog signal varying from 0 to +10V over the range of the parameter being measured.

IV. THE ALTIMETER

The Electronic Barometric Altimeter has two integrated circuits performing four distinct functions as shown in Figure 2.

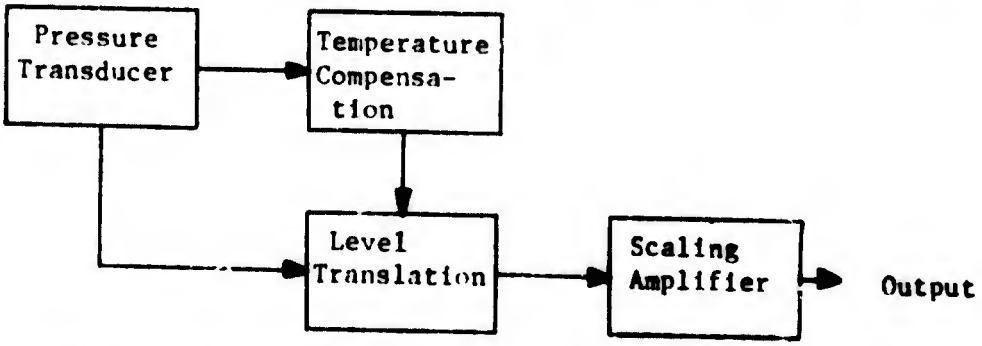

Figure 2. Functions of the Electronic Barometric Altimeter

The heart of the altimeter is the pressure transducer, a hybrid absolute pressure sensor with internal temperature sensing elements.

Figure 3 gives the schematic diagram of the altimeter circuitry. It can be seen that the pressure transducer has two outputs. The pressure output is taken from pin 1 and applied to the first amplifier of the level translation circuitry. Here it is summed with the temperature compensated reference voltage from ZD1. This translates the 2.5V to 12.5V pressure voltage to a 0 to -10V, with this output being applied to a second summing amplifier.

Two additional voltages are summed in this amplifier. The first is a temperature correction voltage, derived from the temperature compensation circuit. The other voltage is derived from the zero reference adjustment and is used to offset the altimeter to ground zero for the local area.

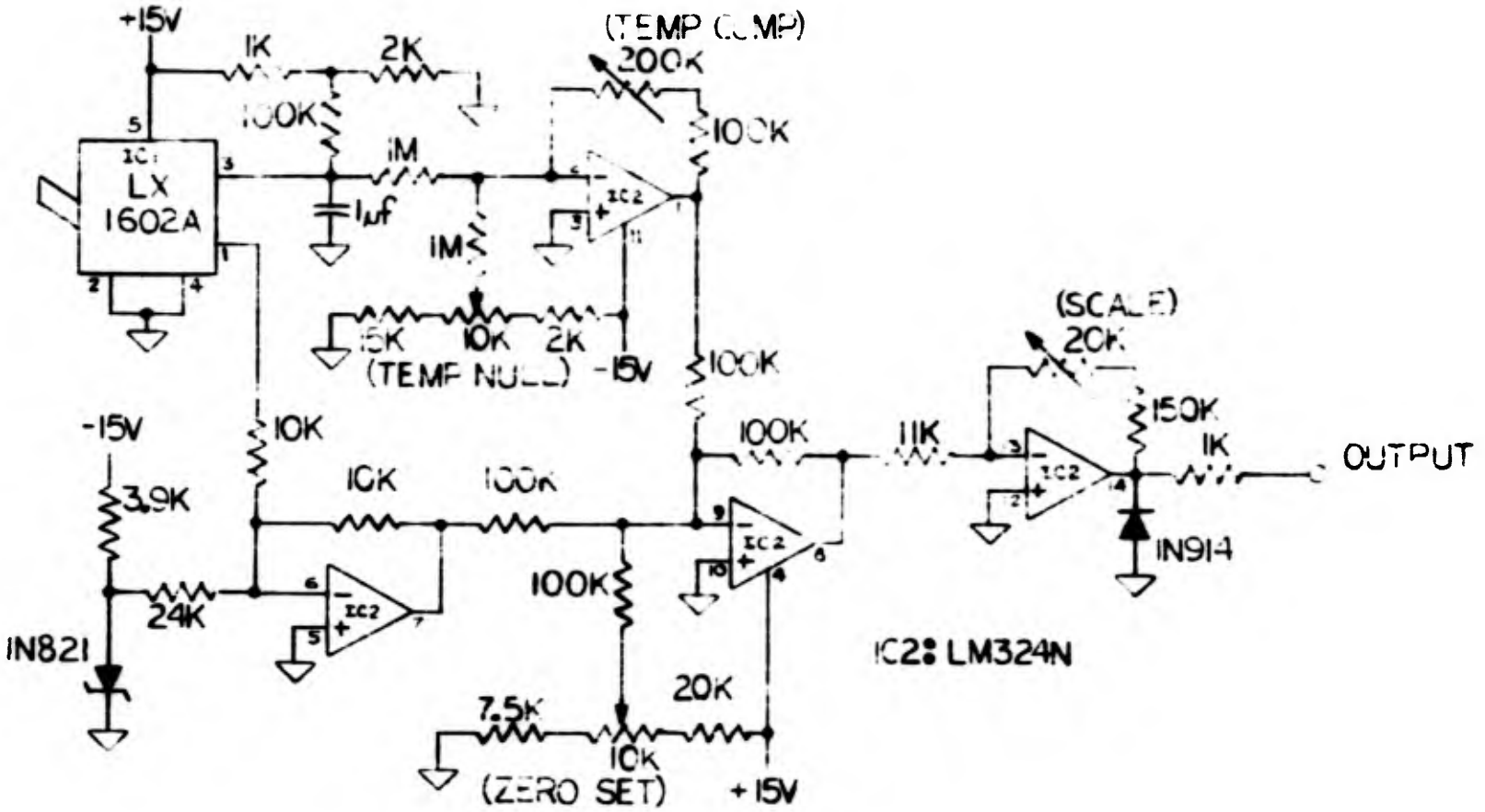

Figure 3. Altimeter Schematic Diagram

The corrected, offset, altitude voltage is applied to the scaling amplifier, with its gain controlled by the Scale Factor adjustment pot. With this adjustment, the output is set so that a 2000 ft change from ground level produces a 10V change in the output voltage.

A temperature correction voltage is obtained from temperature sensing elements within the pressure transducer and is made available at pin 3. This voltage is applied to the temperature compensation amplifier where it is summed with a nulling voltage that eliminates the temperature sensor bias voltage from the output. The gain of this stage is controlled by the Temperature Compensation Linearity Adjustment, being set for optimum correction over the desired temperature range.

V. TEMPERATURE SENSOR

Even though ambient temperature was not among the original system requirements, circuit implementation is so straightforward that it was decided to include this parameter. Boasting the simplicity of a single dual-op amp package and a few external components, the temperature sensing circuitry was quite easily included on the same circuit board as the altimeter (Figure 4).

The sensor itself relies on the temperature dependence of a semiconductor junction. Thus, we have, as a sensing element, a diode-connected transistor whose junction current is a function of the ambient temperature and is linear over a wide temperature range.

The output voltage is developed across the sensor load resistance, and applied to the Scaling amplifier. The Scaling Factor adjustment controls the sensitivity of the circuit and thus sets the full scale temperature range. The sensor voltage, at the input to the Scaling amplifier, is summed with a negative voltage. This voltage can be adjusted to equal the sensors output voltage at 0°C, thereby zeroing the circuit's output.

Following the scaling amplifier is a standard unity gain inverting amplifier that provides a positive voltage output with respect to ground.

VI, ENGINE RPM AND AIRSPEED

Despite functional differences and actual sensor configuration, the engine RPM and airspeed data are converted by identical circuits. Basic operation is that of a duty-cycle detector, in which the period of the incoming signal is compared to an internally generated reference time period. Figure 5 gives the schematic diagram of the RPM Sensor Circuit.

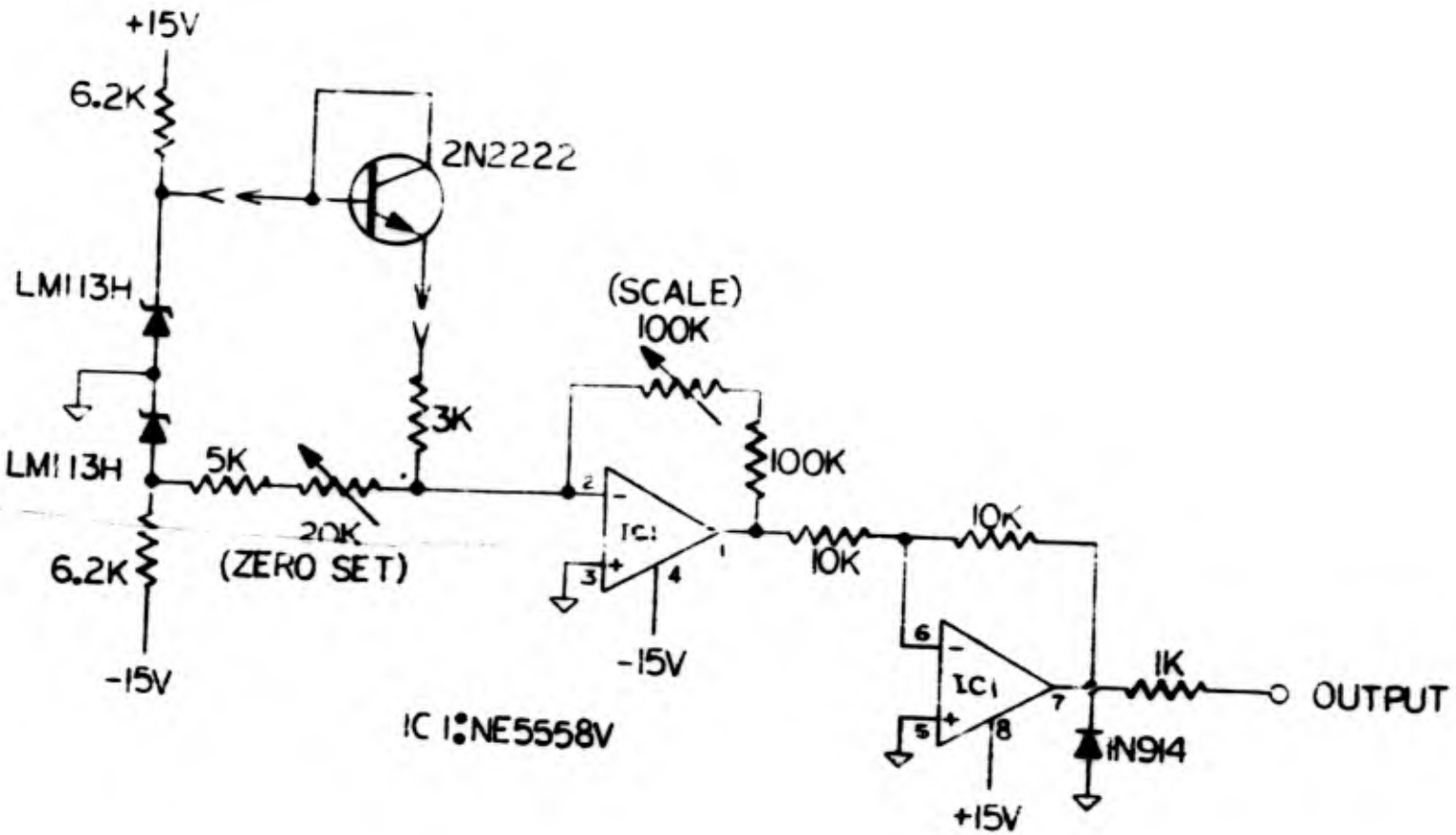

Figure 4. Temperature Sensor Schematic Diagram

The input signal is applied to a unity gain buffer amplifier, and, from the buffer stage, coupled to a shaping amplifier. Operating with open loop gain, the shaping amplifier would normally be driven into saturation on both positive and negative signal swings. However, diode D_1 restricts negative output excursions to about -0.7V, while zener diode ZD_1 limits the positive swing to +4V - producing a squared, TTL compatible signal.

As the output from the shaping amplifier makes a low-to-high transition, it triggers a one-shot multivibrator, IC_2, producing a positive going output pulse, with the pulse width being controlled by the range adjustment. This pulse is the internal reference time period.

Transistors Q_2 and Q_3 are connected as a differential amplifier with a constant current source, Q_1. The biasing on the differential amplifier is such that Q_2 is normally conducting and Q_3 is normally cutoff.

The base of Q_4 sees a series of positive pulses of fixed pulse width, with the time between them equal to the period of the input signal. Q_4 acts as a switch in the bias network of Q_3, and during the positive reference pulses, Q_4 switches on, allowing Q_3 to conduct. The current through Q_3 is regulated by the constant current source, Q_1, and is used to charge capacitor Cx.

Thus, capacitor Cx charges only during the reference time and the total average charge will be a function of the ratio between the reference time and the period of the input signal, the duty cycle. As the input frequency increases, the reference time, which is fixed, becomes a greater percentage of the total period and the capacitor receives a greater average charge. The charge on the capacitor is buffered by the output amplifier to minimize the effects of loading on the capacitor.

As mentioned previously, the actual sensor configurations for engine RPM and airspeed are different. In the case of the engine RPM Sensor, a photo transistor is mounted directly behind the aircraft's propeller. As each blade of the propeller passes in front of the sensor, the transistor is cut off, producing a pulse that goes from +15V to 0V. This is the signal that is coupled to the input of the engine RPM circuit.

The airspeed sensor is a small AC motor mounted on a boom and a propeller is attached to the motor shaft. In this case, the motor is used as a generator and, as the airspeed increases, the propeller rotates at a higher RPM. The output of the sensor is a sinusoidal voltage, approximately 175V peak-to-peak, with the frequency being a function of airspeed (Figure 6). This signal is coupled into a limiter circuit that clips the

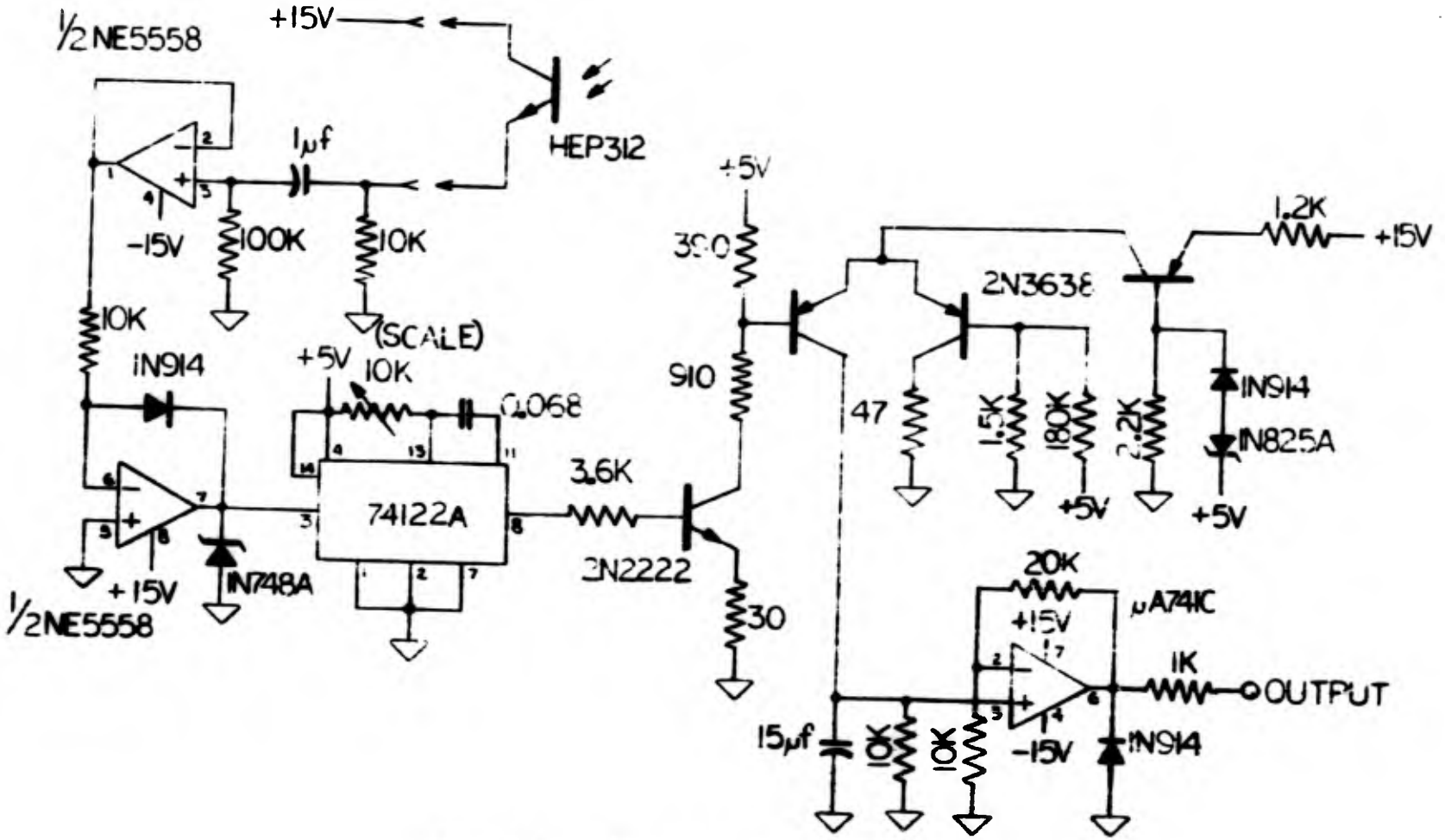

Figure 5. RPM Sensor Schematic Diagram

waveform at +5V and -0.7V, and into a transistor amplifier. The output is a square wave, limited to 5V in amplitude, with a frequency that varies with airspeed. Limiting is performed as close to the sensor as practical, so as not to transmit the full 175V p-p signal which would create excessive noise in other parts of the system.

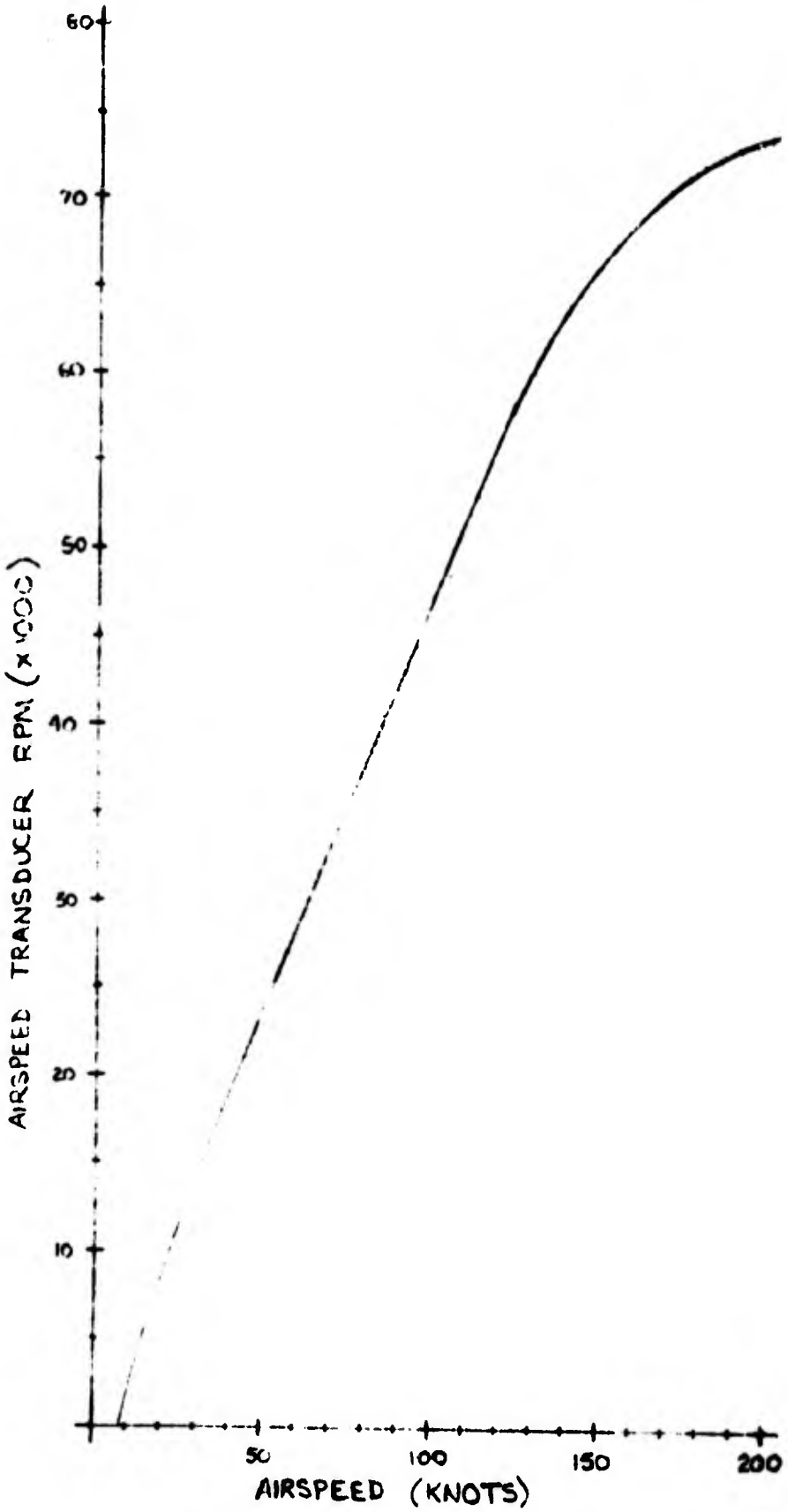

Figure 6. Airspeed Sensor Output Curve

VII. DATA DOWNLINK (Signal Structure)

With the desired parameters having been converted to analog signals by the Sensor Package, some method was needed that would transmit the information from the aircraft to the ground-based operator. The transmission should be relatively immune to interference from external noise and must update the data at a rate consistent with the operator's ability to react to changes. Thus, a system of sequentially sampling each channel and then digitally encoding the multiplexed signal for transmission seemed a reasonable approach.

However, in an effort to reduce the complexity of the system, certain problems were encountered, specifically in the area of synchronizing the ground station with the airborne unit. Since digital data transmission implies the use of clocking signals, some method of supplying a clock was necessary. Without resorting to complex phase-locking techniques, or to a separate clock transmitter, it was agreed that the data should provide its own clock. Thus, the obvious method of transmitting a pulse for a "one" and no pulse for a "zero," was out of the question, due, primarily, to the possibility of a string of "zeroes." Another synchronization problem was that of determining which channel of information was being transmitted at any given time. Both of these prime synchronization problems are solved by the Systems Signal Structure (Figure 7).

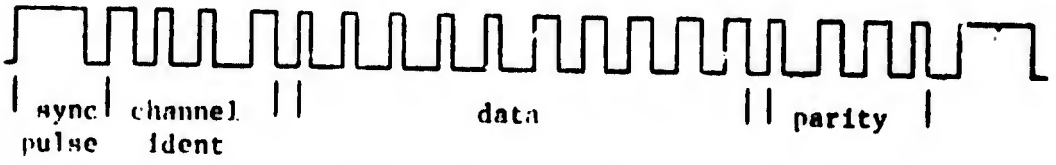

Figure 7. Systems Signal Structure Schematic

The data stream for each channel is preceded by a long sync pulse. The next four pulses identify the channel being transmitted (a total of sixteen possible channels), followed by ten pulses that convey the data for that specific channel. The last four pulses are parity bits and provide a means of checking for errors in the transmission.

Notice that the signal structure is composed of three different pulse widths. The longest is the sync pulse, and it has a duration of 1200 usec. In the data stream itself (i.e., channel ident, data and parity) the two pulse widths signify binary "ones" and "zeroes," with a "zero" being 200 usec and a "one" 400 usec. Thus, the three pulse widths have a 1:2:3 ratio that makes them easily distinguishable from each other.

With this signal structure, both channel and system synchronization have been provided and, since each bit is a sep-

arate pulse, all clocking signals have been provided.

VIII. DATA DOWNLINK (Functional Circuit Description)

Once the basic signal structure had been decided upon, it was necessary to devise a method of generating it. This is the purpose of the downlink package, which is comprised of four functional blocks (Figure 8).

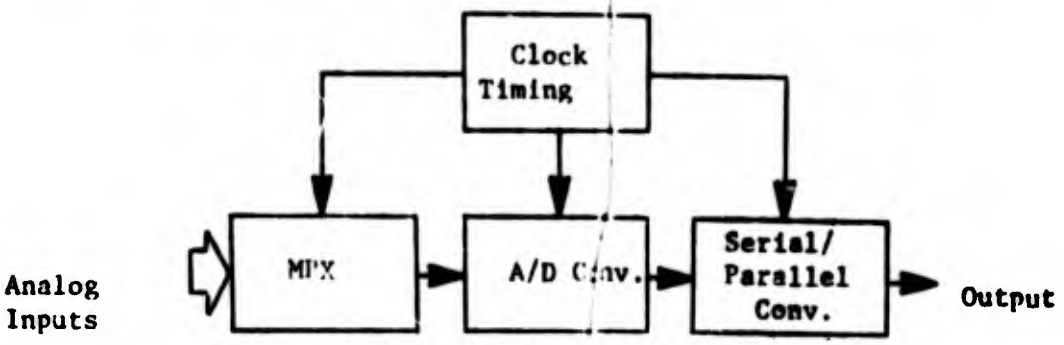

Figure 8. Data Downlink Schematic

Analog voltages from the sensor packages are applied to the multiplexer. This unit sequentially samples each input and applies the multiplexed signal to an A/D converter where it is transformed into a binary number. From the A/D converter the data is applied to a register and stored. At the proper time, this data is combined with channel identification and parity bits, and serially extracted from the register, being applied directly to the transmitter.

DATA DOWNLINK (Detailed Circuit Description)

A good starting point, in describing the Data Downlink circuit's operation, is the clock and timing generator, since it is this functional block that commands and controls the other three blocks (Figure 9).

All timing is derived from a standard oscillator utilizing two inverters from IC1, and a 1 MHz frequency determining crystal. Two buffered outputs are taken from the oscillator, with one being used in the A/D converter circuitry. The other is applied to the input of a counter chain (IC2-IC4) that merely divides the 1 MHz Standard by a factor of 400, producing a 2.5 KHz main clock (MCLK).

Referring to Figure 10, the basic timing signals, it can be seen that the signal format it divided into forty timing intervals (0-39) and, in order to keep track of these forty intervals, IC6 and IC7 are connected to form a modulo 40 counter. Of the forty timing intervals, the first four (0-3) are of specific interest, because during these four intervals,

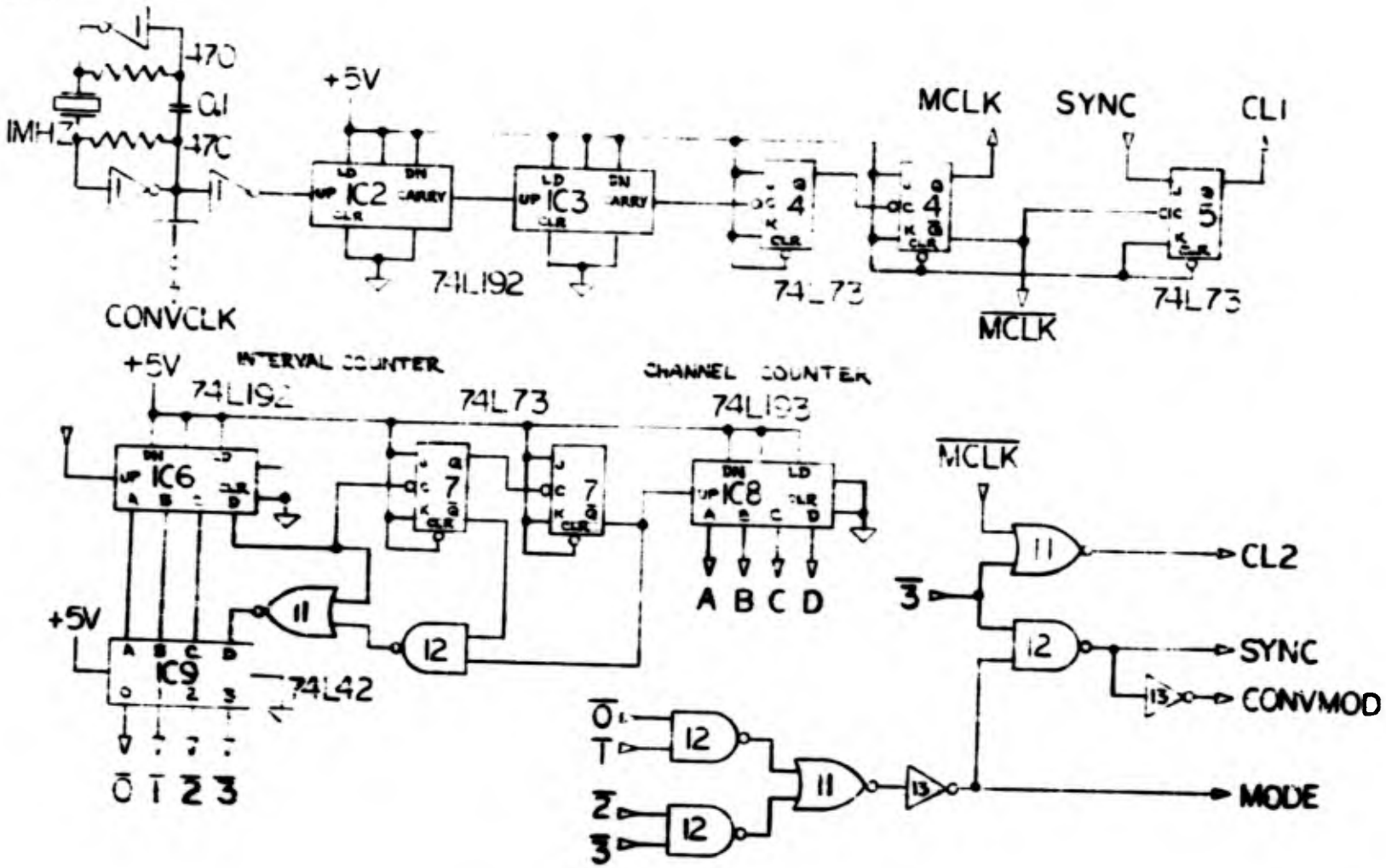

Figure 9. Clock Generator and System Timing

all signal processing is performed and the data is loaded in the output register. IC9, a BCD to decimal decoder, decodes the counters outputs. However, if IC9 were operated just to decode the first four bits, the intervals 0-3 would be decoded four times during each data stream. To prevent this a separate decoder consisting of IC11C and IC12D determines when the interval counter has counted above ten and produces a logical "one" at the MSB input of IC9.

The decoding structure of IC9 is such that any BCD number greater than nine will not be decoded. Thus, once the interval counter has passed ten, the smallest BCD number seen by IC9 will be an eight, and all lower order numbers will not be decoded. This allows the decoding of intervals 0-3 to occur once and only once during each forty counts, with the decoded outputs going from a high to low state during the interval.

Four decoded outputs ($\overline{0}$-$\overline{3}$) are taken from IC9 and applied to two NAND gates IC12A and B, with the outputs of these gates driving the inputs of NOR gate IC11A. The logic proceeds as follows: Only during the intervals 0-3 will one of the inputs to the two NAND gates be low, resulting in a high output. Since, during these intervals, one input to IC11A will always be high, its output stays low for the entire four intervals. This signal is inverted and designated MODE, which will be used to enable loading data into the output registers.

Another timing signal is produced by gating the $\overline{3}$ interval with MCLK, in NOR gate IC11B, producing a positive going pulse during the first half of the fourth timing interval. This pulse, designated CL2, will be used in conjunction with the MODE signal to load the output register.

The sync gate (labled SYNC) is generated by gating the MODE pulse off during the fourth interval with the $\overline{3}$ signal. This produces a low going pulse with a duration of three timing intervals that will ultimately be used to generate the system's sync pulses. Inverting the SYNC gate generates a signal, designated CONVMOD, that will control the operation of the A/D converter.

A final timing signal (CL1) is also used to control data flow in the output register; it is the clock that will shift the data out of the register. The CL1 signal is essentially one half the frequency of the MCLK, except that it is inhibited during the 1-3 time intervals. This clock is derived by flip-flop IC5.

A last sub-function within the clock and timing generator is the address counter, IC8. This is a four-bit binary counter that advances one count each time the interval counter overflows. It sets the operation of the multiplexer and supplies

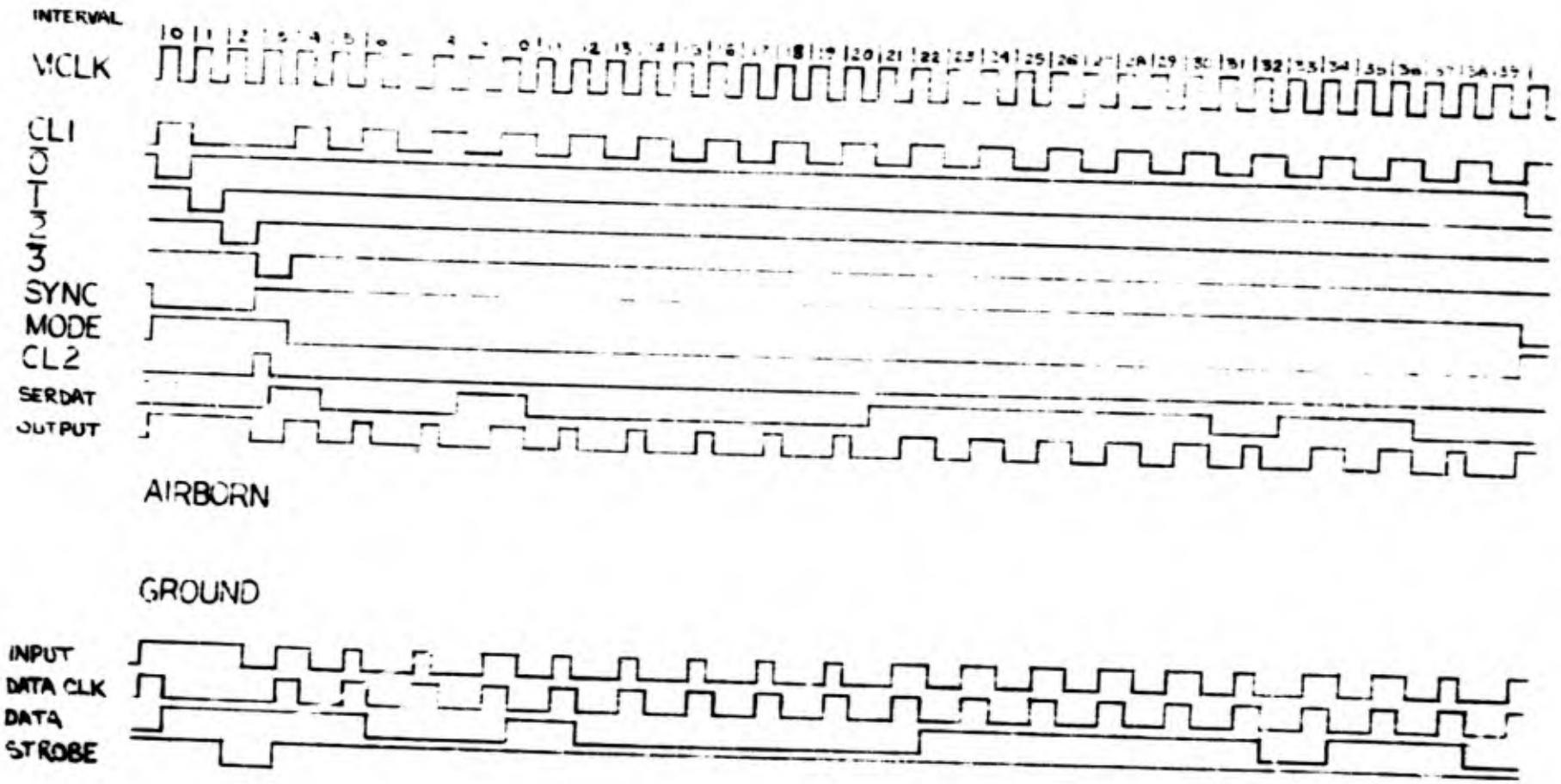

Figure 10. System Timing Diagram

the channel ident code to the output register.

IX. DATA DOWNLINK (Multiplexer)

Operation of the multiplexer circuit (Figure 11) is controlled directly by IC18, a one-of-sixteen decoder, which receives a four-bit binary input number from the channel address counter. This number corresponds to the number of the channel whose data is being processed and transmitted. IC18 decodes this binary number and causes the appropriate output to go low for the duration of the channel's data stream, while all other outputs remain in a high state.

Each output from IC18 is inverted by a bare collector inverter, with the collector tied to +15V through a 2K ohm pull-up resistor and used to drive one of sixteen CMOS FET Switch control inputs. A common output buss, designated MPX, connects the outputs of all sixteen FET Switches, while their inputs are the various analog sensor voltages. When the control input goes high, the FET Switch presents a low impedance, and its input is connected to the output buss. Thus, one at a time, all sixteen inputs are connected to the output bus, or multiplexed.

X. DATA DOWNLINK (A/D Converter)

The circuit that provides the digital representation of the sensor voltages is the analog-to-digital (A/D) converter, and in this case it is termed a tracking A/D Converter. Interestingly enough, the heart of this circuit is a digital-to-analog (D/A) converter that is used as part of a feedback loop.

Shown in Figure 12 is a simplified functional version of the D/A Converter used in the feedback loop.

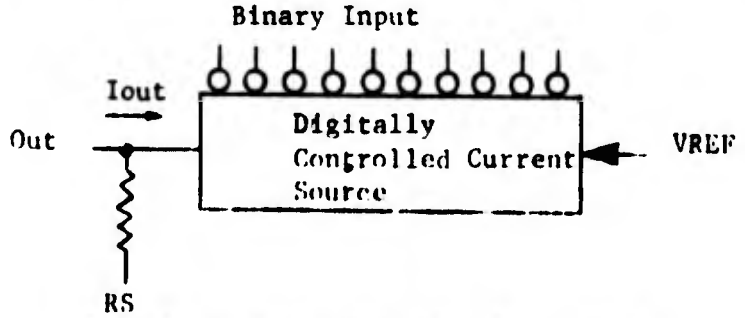

Figure 12. D/A Converter, Simplified

The circuit is merely a digitally controlled current source, where the output current is proportional to the 10-bit binary input number. A summing resistor (RS) is included within the circuit, enabling it to be used with an op-amp in a current to voltage converter. It is important to note, that this D/A converter uses complementary logic, i.e., an all zero input produces maximum output current. Relationships between Rs and

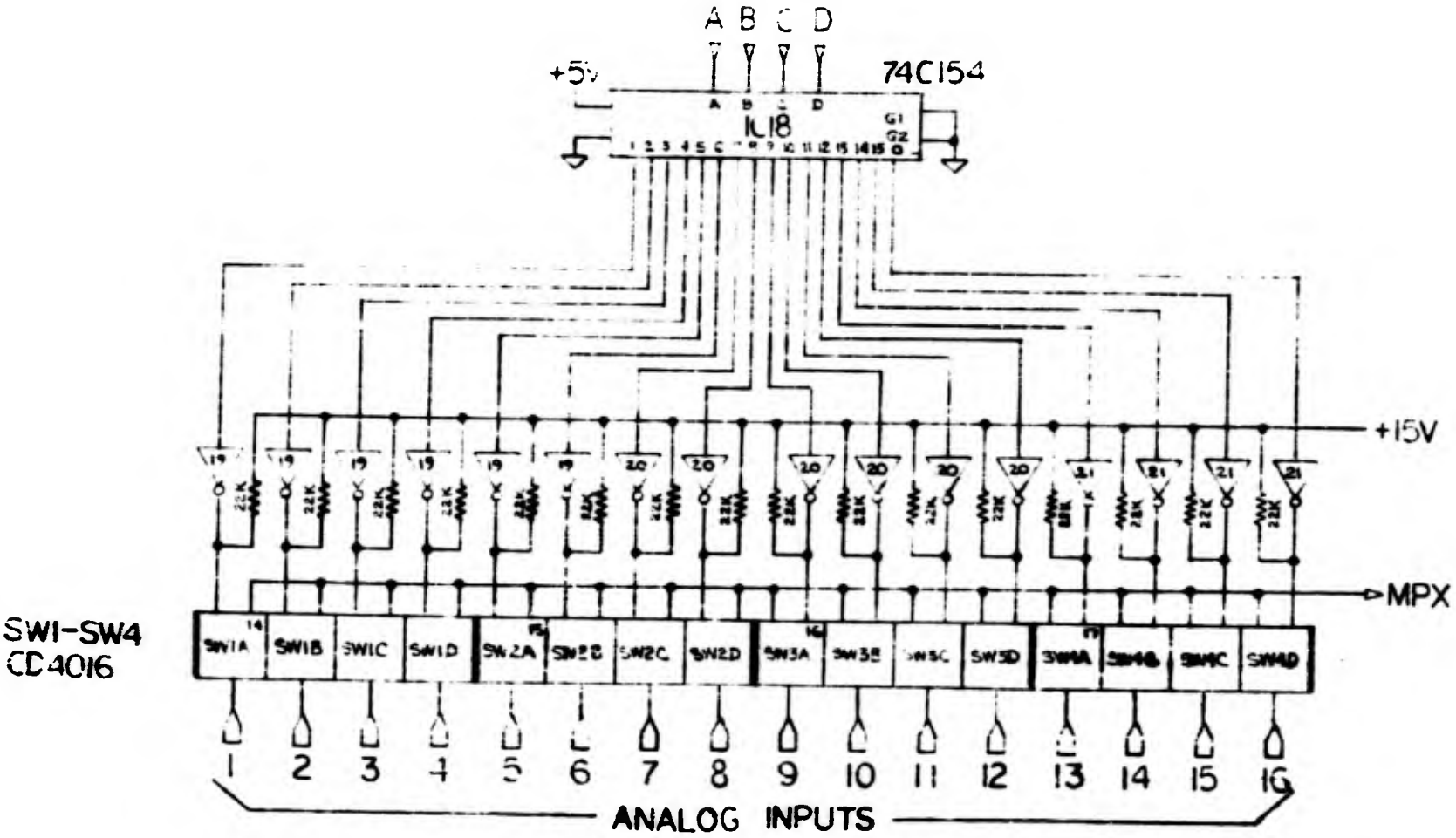

Figure 11. Multiplexer Schematic Diagram

Iout are given as in Equation 1.

$$I_{out}\ (max) \times R_s = 10V \qquad (1)$$

In the tracking A/D Converter, this relationship is utilized to produce a nulling circuit and, when the null has been achieved, the circuit is said to be locked.

Figure 13 gives the schematic diagram for the tracking A/D Converter used in this System. The multiplexed analog voltage (MPX) is buffered by a voltage follower, IC22, and applied to the summing resistor of the D/A converter. Here the input voltage is compared to the output current of the D/A Converter, with the output being applied to a voltage comparator (IC24). A D-type flip-flop, IC25, latches to the comparators output and drives a clock gating circuit (IC26) for a 10 Bit up/down counter. The outputs from the counter are applied to the binary inputs of the D/A converter, establishing the feedback loop.

Clocking for the up/down counter (CONVCLK) is derived directly from the 1 MHz Standard, and is controlled by two gating signals, the converter mode (CONVMOD) and the D-type latch. The CONVMOD Signal enables the clock (and thus the entire converter circuit) for the duration of the Sync pulse, while the latch outputs merely route the clock to either the count up or count down inputs of the counter.

For the sake of convenience, in making an intuitive analysis of the operation of the tracking A/D Converter, let us assume that the D/A Converter's output current is zero (binary inputs all "one's") and the input voltage (MPX) changes from 0 to +5V. This creates a positive error voltage at the output of the D/A Converter. The comparator senses this error voltage at its inverting input and switches to a low state. On the next rising edge of the CONVCLK, IC25 will latch with its $\overline{Q}$ output going high, routing the clock to the count down input of the 10-bit counter. As the counter counts down, the D/A Converter output current increases, resulting in an increased voltage drop across Rs, which reduces the output error voltage.

Now, since the full scale voltage is ten volts, and the number of counter states is 2^{10} or 1024, the smallest change in output, produced by changing the least significant bit (LSB), is equivalent to 10/1024 V, or approximately 10mV. Thus, if the input voltage is, for example, 4.995V, there is no counter state that will be exactly equivalent to the input voltage. Therefore, when the counter has counted down halfway, the D/A converter output error voltage will still be slightly positive. However, one more count will be too great, producing a negative error voltage, causing the comparator to switch to a high state. On the next clock signal, IC25 will latch to this new state, commanding the counter to reverse and count up. So the counter

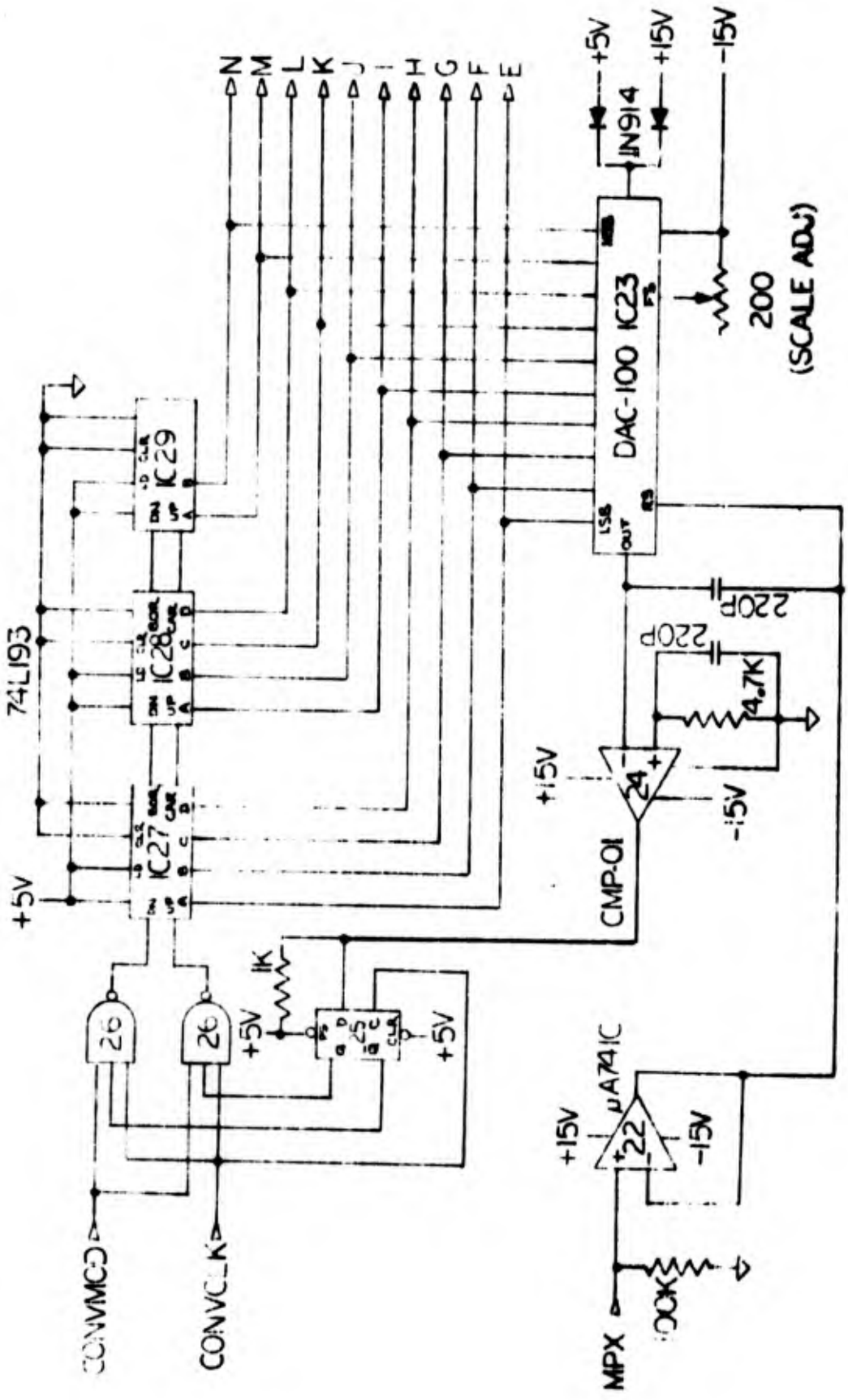

Figure 12. D/A Converter, Simplified

counts up one bit, which produces a positive error voltage that causes the comparator to switch a gain and command the counter to down count once again.

At this point the loop is locked and the converter is "dithering" about the actual value, producing a 1/2 bit error in the output. The digital output will continue to "track" the input voltage until the CONVMOD signal disables the clock, thereby placing the A/D converter in a HOLD mode, in which its binary output is held steady.

The slew rate of the converter is limited, primarily, by the clock rate. Therefore, any signal that changes more than approximately 10mV per usec will cause an unlocked condition and the output may or may not be valid. A full-scale (10V) change will take a maximum of 1024 counts for lock, or 1.024 msec. Since the conversion process occurs during the sync pulse, which is 1.20 msec in duration, the A/D converter will have a minimum of 176 clock intervals in which to track the input voltage before the output is "frozen."

Parallel outputs E through N are a binary representation of the input voltage and comprise the data portion of the system's output signal.

XI. DATA DOWNLINK (Output Register)

The primary function of the output register (Figure 14) is to store all eighteen bits of parallel data and convert them to a serial bit stream at the proper time. The actual register is composed of five four-bit shift registers, with parallel load capability. Parallel loading of data occurs on the high-to-low transition of the CL2 signal when the MODE signal is in a high state. When the MODE input is low, the CL1 signal controls the operation, shifting the contents of the register one bit to the right on each CL1 falling edge.

A look at the basic timing signals (Figure 10) will illustrate how these relationships are used to effect a parallel to serial conversion of the data.

During the sync time (intervals 0, 1, and 2) the A/D conversion takes place and the data is not necessarily stable. At the beginning of interval 3, the A/D converter is placed in a HOLD mode, and the parallel inputs are "frozen." At this time, the final parity bits are determined. These parity bits (P_1, P_2, P_3, and P_4) provide a means of checking for errors in transmission, since they are derived by MOD 2 adding certain bits of the data and the channel ident, according to the relationships in (2). Halfway through interval 3, a falling edge

$$P_1 = A \oplus L;\ P_2 = C \oplus L;\ P_3 = E \oplus J;\ P_4 = G \oplus I \qquad (2)$$

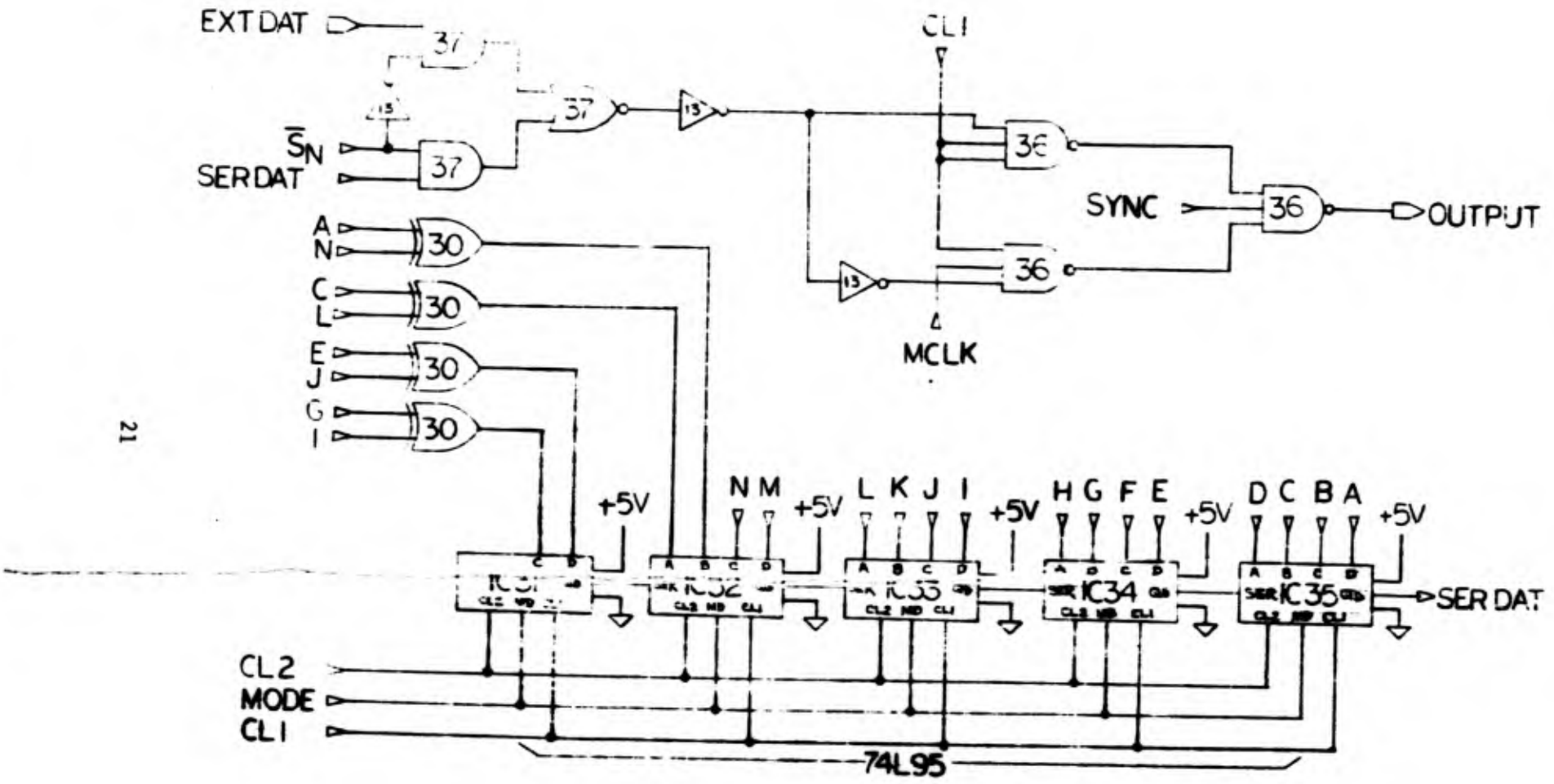

Figure 14. Output Register Schematic Diagram

occurs on the CL2 signal, loading all eighteen bits of information into the registers, and the output code generation begins.

As it is clocked by the CL1 signal, the contents of the register appears, one bit at a time, at QD of IC35, which is connected to AND - OR - INVERT gate, IC37. This gating structure is merely a data switch, allowing external digital data to be encoded and transmitted. However, for normal operation, the serial data (SERDAT) will be routed through to the output coding logic (IC36).

Recall that, in defining the signal structure, a binary "one" was to be represented by a long pulse, while a "zero" was to be a short one. Now looking at the basic timing signals, it can be seen that the durations of the positive portions of MCLK and CL1 (after the Sync pulse) have the proper 1:2 ratio.

In performing the task of output coding, IC36 acts as a selector gate, selecting the positive portion of either CL1 or MCLK, depending upon whether SERDAT is a "one" or a "zero." If the data is a "one", the upper gate is enabled, allowing CL1 to develop the output signal. With SERDAT at "zero", inverter IC13D enables the lower gate and selects MCLK to generate the output pulse. Immediately after a data pulse is generated, on the CL1 falling edge, a new bit of data is shifted to the output of the register and awaits the proper timing signals.

XII. DATA DOWNLINK (Summary)

A brief summary of operation will aid in tying together the individual functional blocks; but first, a review of the System Concept is in order.

The system is a 16-channel, time-multiplexed, pulse-modulated, data downlink. Sixteen channels of information are transmitted sequentially with the basic signal structure providing all synchronization and data information.

A synchronizing pulse precedes the data stream for each channel, followed by four pulses identifying the channel being sampled. The actual data is contained in the next ten pulses, with a parity tail (derived from the MOD 2 addition of specific data and ident bits) occupying the last four pulses.

Binary data is conveyed by pulse width modulation; a wide pulse represents a "one", and a narrow pulse represents a "zero."

The time required for the transmission of one channel is 16 milliseconds, yielding an update period of 256 milliseconds, or approximately four updates per second.

A 1 MHz crystal controlled oscillator provides the frequency standard for the System. A divide-by-400 counter generates the main clock and a mod 40 counter determines the framing for data pulses, with 40 timing intervals per channel.

At the beginning of a channel's data stream, the channel address counter is incremented by one count, and, during the first three timing intervals, the sync pulse is generated.

The channel address is decoded and used to select the proper switch in the multiplexer, which connects that channel's input voltage to a tracking A/D converter.

At the end of the sync pulse, the A/D conversion has been completed and the converter data is frozen. Half a timing interval after the sync period, the four bits of channel ident, ten bits of data from the A/D converter, and four bits of parity information are parallel loaded into a buffer register. This register is unloaded serially, and each new bit is used to generate an output pulse, with the data state determining the width of the pulse.

XIII. GROUND STATION (Functional Block Diagram)

In the airborne DATA DOWNLINK package, information from the basic sensors, in the form of analog voltages was converted to a 10-bit binary code. This information was placed in a serial data stream along with synchronization and channel identification and applied to a transmitter as amplitude modulation. The ground station has the task of detecting the synchronization signals, discriminating between the transmitted "one's" and "zero's," and separating the channel ident. In addition, a provision has been made, using the parity word to provide a visual indication of the error rate in transmission.

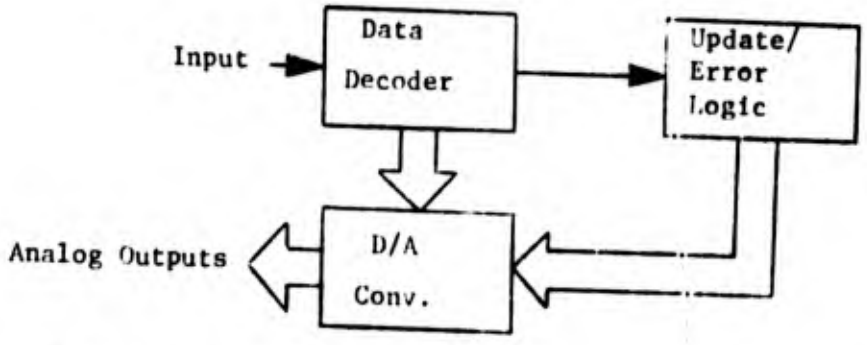

Figure 15. Ground Station Functional Block Diagram

Functionally, the ground station is composed of just three blocks. Note, specifically, the lack of clock and timing circuits, which is due to the nature of the signal structure. The first functional block decodes the serial data stream and per-

forms a serial to parallel transformation. The ten bits representing the actual data are applied to the D/A converter, while the channel ident and parity bits are processed by the update/error logic block. It is here that the determination is made based on parity checks whether or not to accept each data stream as valid information.

XIV. GROUND STATION (Receiver Interface and Data Decoder)

The output of the receiver is not of the proper amplitude or wave shape to reliably drive the TTL inputs of the data decoder. For this reason, a circuit consisting of IC29 and IC30 provides the proper interface between the receiver and the logic (Figure 16).

IC29 is a voltage comparator with its inverting input biased to approximately one volt. Thus, whenever the output of the receiver, which is inverted, falls below one volt, the comparator switches from a high to a low state. The comparator's output drives an inverter chain that is used primarily for shaping the signal, driving it to provide fast edges necessary for TTL.

The interface output drives two decoding circuits, each comprising one half of a dual (retriggerable) one-shot multivibrator. The lower one-shot utilizes the retrigger capability to detect the sync interval, and a look at the timing diagram (Figure 10) will show how this is done.

On each rising edge of the input signal, the one-shot is triggered. If another rising edge occurs before the time constant ends, the multivibrator will be retriggered for an entire time constant. Notice, on the timing diagram, that, excluding the sync intervals, the rising edges occur every 800 usec. However, the time between the sync pulse rising edge and the first data bit is 1600 usec. The time constant for IC1B is set at 1000 usec and the one-shot is retriggered by every data pulse, never allowing the time constant to expire. But, during the sync interval, the time between rising edges is 600 usec longer than the one-shot time constant, and IC1B will shut off for this time. The negative-going pulse produced at this time indicates that the input has just seen a sync pulse, and, this output is labeled $\overline{\text{STROBE}}$.

A second one-shot, IC1A, is used to decode the data, and it is also a rising-edge-triggered multivibrator. Ideally, the input pulses should be 400 usec wide if the data is a "one," and 200 usec wide for a zero. For this reason, the time constant for IC1A is set at 300 usec.

Every time the input "sees" a rising edge, IC1A produces a 300 usec output pulse. This pulse is gated with the incoming

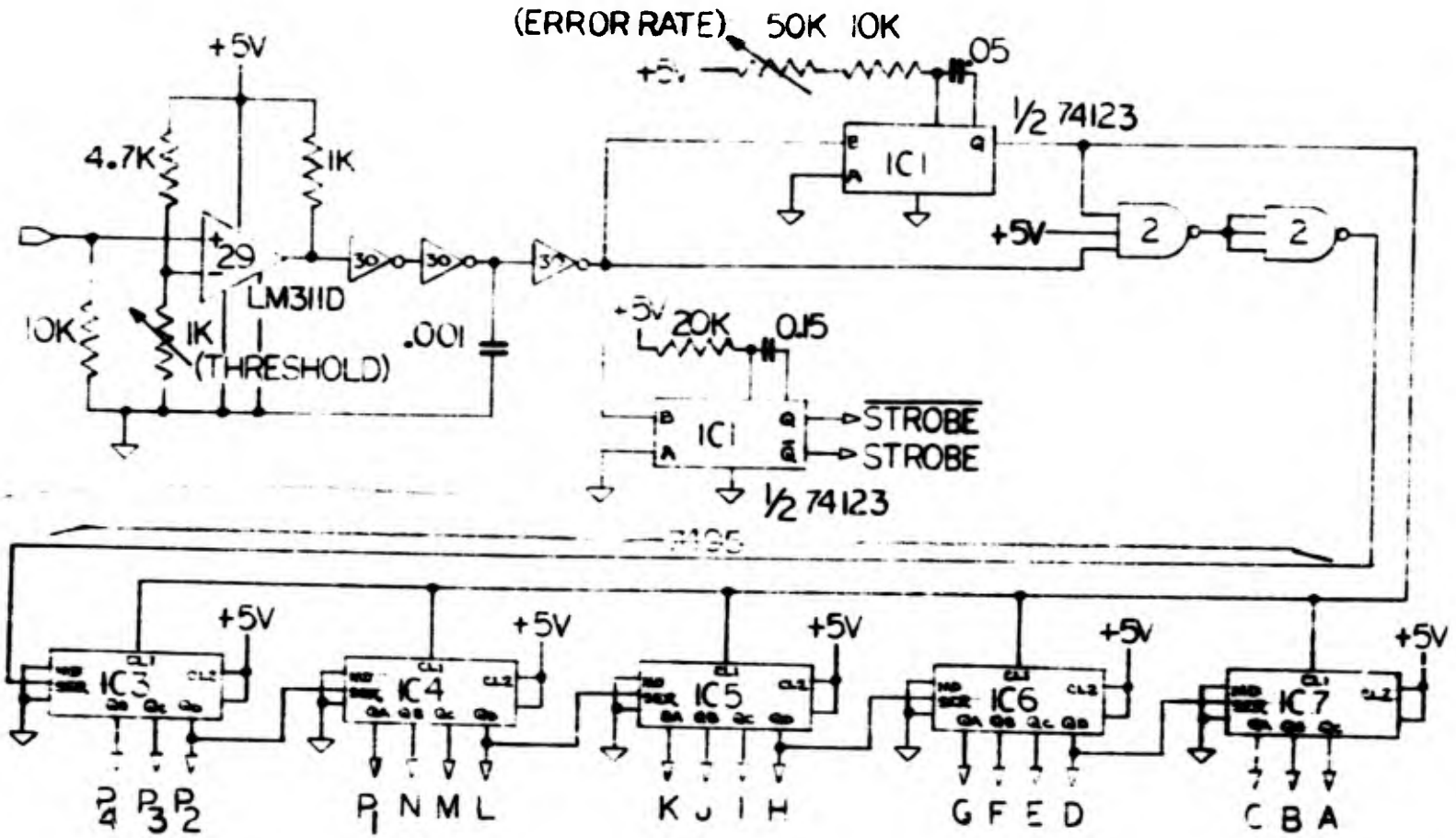

FIGURE 16. DATA DECODER SCHEMATIC DIAGRAM

data stream in IC2, and the output is applied to the serial input of a 20-stage shift register. The 300 usec one-shot pulses are applied to the register's clock input, causing the serial data to be entered on the falling edge of the pulse. If the triggering pulse is 400 usec wide, representing a binary "one," the serial data input will still be at a high state on the falling edge of the clock, thus entering a "one" into the register. A 200 usec wide, "zero" pulse will have disappeared 100 usec before the clock and a "zero" will be entered. Notice that the sync pulse immediately following each data stream will cause an extra "one" to be entered into the register, compensated for by extracting the parallel data from register outputs 2-19.

It was found that the bandwidth limiting imposed by the transmitter/receiver link, tended to "stretch" the data pulses considerably. This is due, primarily to the rounding of the rising and falling edges of the pulses. For this reason, the time constant of IC1A has been made variable and is properly adjusted for a minimum error rate.

XV. GROUND STATION (Update/Error Logic)

The update/error logic (Figure 17) is charged with the task of determining the validity of the data in the register. This is done by examining the information bits and generating four internal parity bits P_1', P_2', P_3', and P_4', by the same formula used to generate the original parity word. Thus:

$$P_1' = A \oplus N;\ P_2' = C \oplus L;\ P_3' = E \oplus J;\ P_4' = G \oplus I \qquad (3)$$

The four generated parity bits in (3) are compared with the parity bits in the register. If there have been no errors introduced in transmission (by noise pulses, for example), the parity bits should agree and the outputs from IC10A and IC10B will be high. This indicates that the data that has been decoded is valid. Then, when the sync interval is detected the STROBE input to IC2C sees a 600 usec positive pulse, forcing the output low which enables IC11.

IC11 is a one-of-sixteen decoder that receives four inputs from the data register ———— the four bits of channel identification ———— and causes the decoded output to go low. Each output is inverted by a bare collector inverter and used to control the D/A conversion for that particular channel.

If, for some reason, there has been an error incurred in transmitting the data, a parity check will fail at one or more bits and the output of IC2C will remain high, even during the STROBE pulse. This output is inverted by IC10C and applied to one input of IC10D. The other input receives a STROBE

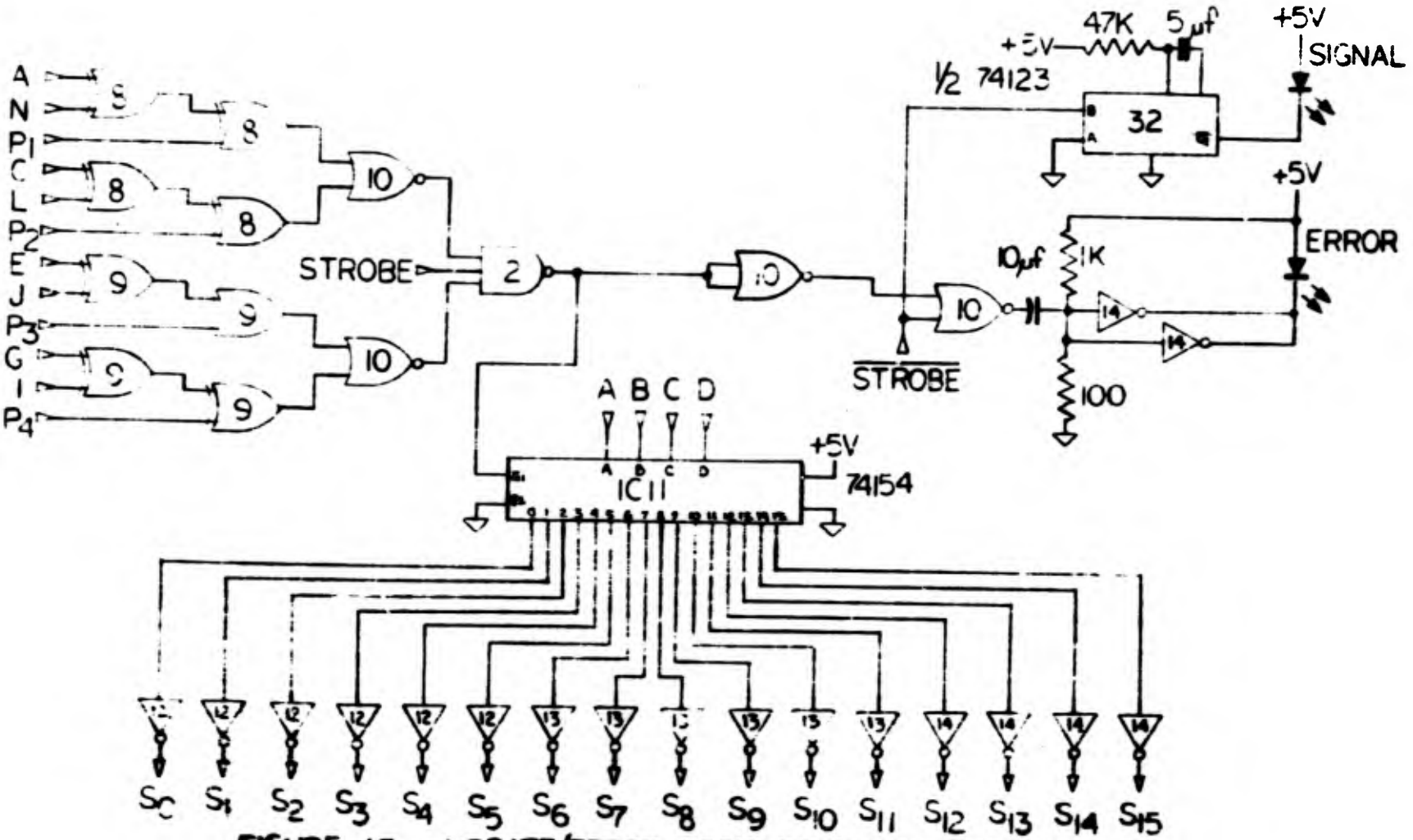

FIGURE 17. UPDATE/ERROR LOGIC SCHEMATIC DIAGRAM.

pulse (negative going for 600 usec) and the output will be a positive going pulse. This positive going pulse causes inverters IC14E & F to turn on, allowing the error indicator Light Emitting Diode (LED) to conduct. A 10 uF capacitor holds the LED on for a period considerably longer than the 600 usec error pulse, making the light more visible. The result is that the LED will blink on every time a parity check fails. Notice that, if no error were present, the output of IC10C would go high for the duration of the STROBE pulse, forcing IC10D to remain low, and the LED would not conduct.

XVI. GROUND STATION (D/A Converter)

The D/A converter IC15 (Figure 18) is fed the 10 bits of data from the register and converts them into a proportional current output. Since the actual D/A converter used on the ground is the same as the one used in the airborne tracking A/D converter circuit, the data bits are already in the proper complementary form.

The output current is transformed to an analog voltage by op-amp IC16B and buffered by a voltage follower, IC16A. Nulling capability is provided in the voltage follower circuitry to compensate for cummulative offset errors in the system.

This analog voltage should, at the time of the STROBE signal, be the same as that seen by the airborne A/D converter for a given channel. The voltage is applied to the common inputs of sixteen sample-and-hold circuits.

Each sample-and-hold circuit is composed of one FET Switch, a capacitor storage element, and a high impedance buffer amplifier.

During the 600 usec STROBE pulse, the channel ident is decoded ———— assuming a valid parity check ———— and the decoding circuit turns on the proper FET Switch. This provides a low impedance charging path for the storage capacitor in that sample-and-hold circuit. The capacitor charges to the new voltage and then, after the STROBE, slowly discharges through the high impedance of the buffer amplifier.

If the transmission is error free, each sample-and-hold will receive a new charge four times per second. However, should an error occur during any channel, the error logic will prevent that sample-and-hold from accepting an incorrect voltage and it will hold the previous value until the next valid update, discharging by approximately one percent per second.

In addition to recovering analog data, the ground station must respond to the downlink's ability to transmit one channel of digital data. This capability is provided by IC31, a ten-bit latch. The decoded output for the channel which was selected

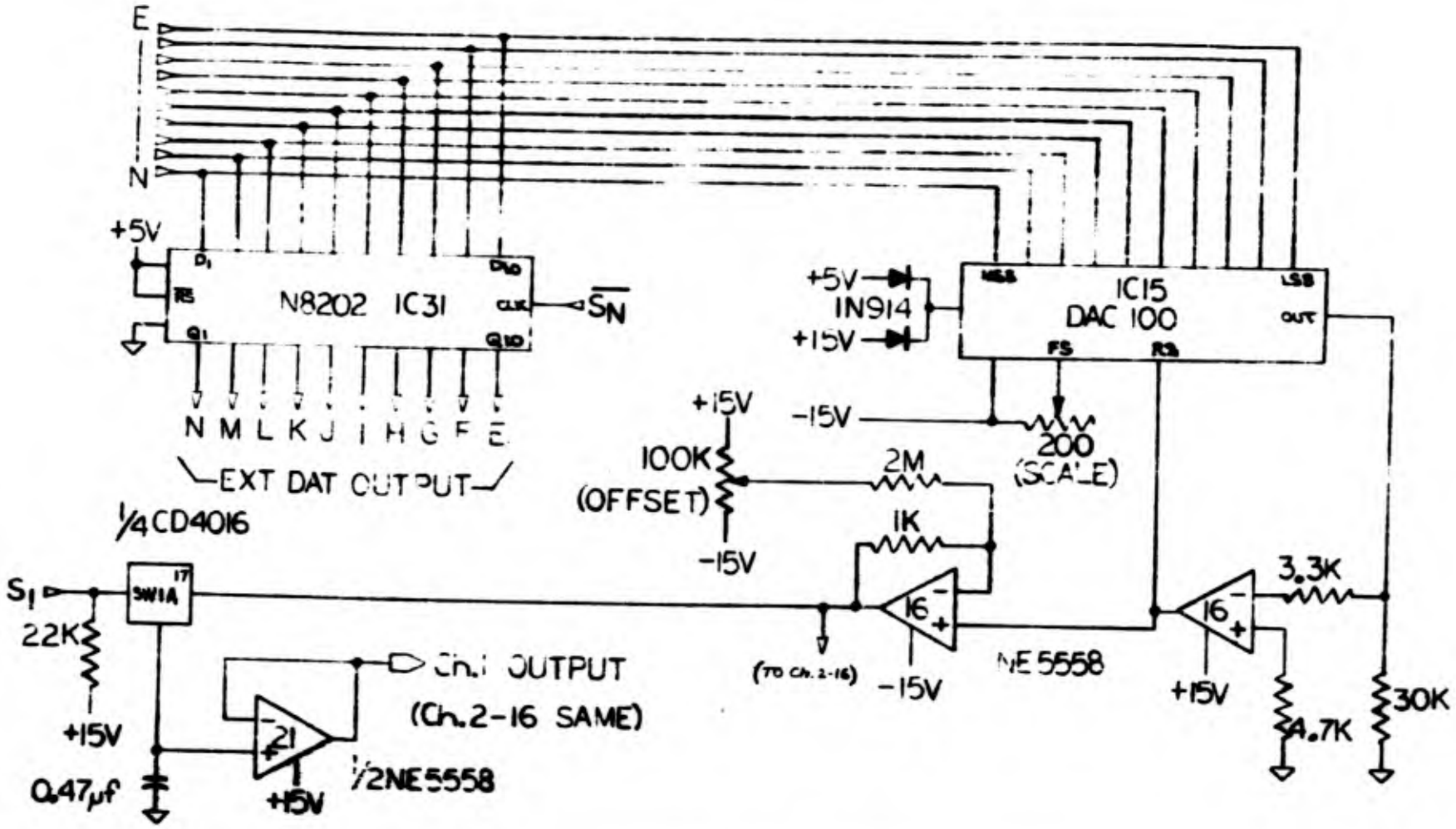

FIGURE 8. D/A CONVERTER SCHEMATIC DIAGRAM

to receive digital data directly is connected to clock input of the latch. The ten bits of data are connected to the D inputs, and, when the proper channel ident code is decoded (assuming that the parity check is good) the ten bits of data will appear at the outputs of the latch and remain there until there is a change in that channel's data.

XVII. GROUND STATION (Summary)

The output of the receiver is shaped by the interface circuit, and applied to the DATA DECODER. Here, utilizing the retrigger capability of a one-shot multivibrator, each sync interval is detected, producing a STROBE pulse. Another one-shot pulse is used to discriminate between the long "one" data pulses and the shorter "zero" pulses.

As it is decoded, data is serially entered into a register and extracted in parallel. The 10 bits of data are applied to the D/A converter, where they are converted to an analog voltage.

Channel ident and parity bits are applied to the update/error logic. If a parity check passes, the strobe pulse will enable the address decoder and allow the converted analog voltage to be applied to that channel's sample-and-hold circuit.

Should the parity check fail ———— signifying a transmission error ———— the error logic will cause an LED error indicator to flash and prevent the sample-and-hold circuit from being updated to a possibly incorrect voltage.

Sixteen buffered outputs are available to drive a combination of analog and digital panel meters, depending upon the requirements of the mission.