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Gainesville, Florida

Investigation and Study of Computational Techniques for the Design and Fabrication of Integrated Electronic Circuits

Final Report
September, 1975

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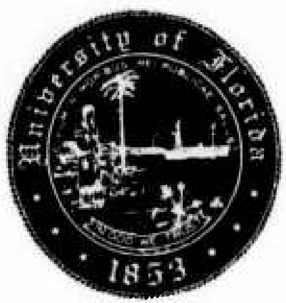

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ARPA - Univ. of Florida Program for

Computer Aided Engineering of
Integrated Semiconductor Circuits

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Investigation and Study of Computational Techniques for the Design and Fabrication of Integrated Electronic Circuits

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PREFACE

Under ARPA Grant MDA903-74-G5, the University of Florida, Gainesville, Florida, has undertaken a program of study on the topic of Computer Engineering of Integrated Circuits. The purpose of this program was to identify problem areas associated with the design and development of integrated semiconductor circuits; problem areas that result in excessive cost and inadequate availability of the particular type electronic structures required by the DoD. An additional purpose of this study is to recommend a program of research and development directed toward alleviating the identified problem areas.

This project was undertaken with full recognition of the complexity of the task at hand. It was also expected that a diversity of opinions would be encountered concerning the real source of existing DoD IC procurement problems. This expectation was realized; therefore, many conclusions presented here represent the most prevalent opinions drawn from numerous scientists and engineers actively working in the field of semi-conductor integrated circuits. Among these individuals are representatives from many industrial organizations engaged in IC design, development, and manufacturing. In addition, among these individuals are representatives from various branches of the DoD, and from several academic institutions engaged in research of particular value to the goals of this program.

As with any effort of this type, I am indebted and owe thanks to many people who have contributed their time and effort to this project. In particular, special thanks are due to all members of the program Steering Committee who undertook hours of extra work in their desire to assure the success of this study program.

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SUMMARY

This study program has identified an important difference between the IC business for industrial applications and for DoD system applications: namely, the relative number of IC structures, of a given design, that are manufactured at a given time. For economic reasons the commercial IC market is based upon large volume manufacturing--where a new IC product can be manufactured in large volume, and over an extensive period of time. DoD system contractors seldom (if ever) have a need for the quantity of IC structures that semiconductor manufacturers consider economically practical. For this reason, DoD system contractors are subject to many IC procurement problems for which there is no immediate solution.

It is suggested that this emphasis upon large volume manufacturing is a natural consequence of the state-of-the-art. IC design and development is an exceedingly costly undertaking, and the financial investment required to produce a new IC structure is easily regained only in a large volume market. Therefore, the IC procurement problems experienced by DoD system contractors frequently result from their small volume requirements. If a procurement order can be satisfied by an existing commercial structure (or by minor modifications of such a structure), the order will be completed in a relatively

short period of time, and at a reasonable cost. If, instead, a procurement order involves the design and development of an entirely new IC structure, the total cost becomes excessive.

Semiconductor manufacturers recognize the crucial nature of economical IC design methods in this highly competitive industry. As a consequence, most (if not all) manufacturers utilize computer techniques to solve design problems that would otherwise require many man years of effort. Furthermore, the value and effectiveness of these computer techniques are evidenced by a continued development effort that is directed toward improving existing computational capabilities; this effort also indicates recognition of the necessity to reduce future IC design and development costs. Nevertheless, it is generally acknowledged that fundamental constraints exist upon our ability to expand these computer design techniques. These constraints arise from an inadequate understanding of physical mechanisms associated with IC design and operation.

Computer techniques for IC design are based on the use of mathematical models to approximate the structure under consideration. Some of these models are derived from first principles and, as a consequence, they are highly accurate. In contrast with these accurate mathematical models, many others are heuristic in nature; these heuristic models are used to approximate mechanisms for which there is only incomplete understanding.

The inadequacy of these heuristic models, in conjunction with important difficulties associated with process measurement and evaluation, contribute extensively to the excessive IC design and development costs. Therefore, recommendations resulting from this study program are directed toward alleviating existing shortcomings in our present computer techniques for engineering semiconductor integrated circuits.

Modeling of semiconductor device operation falls into two broad categories: first, mathematical models that approximate physical mechanisms associated with device operation and, second, network representations of these devices for circuit analysis purposes. It is recommended that mathematical models be developed whereby the IC design engineer can accurately calculate the electrical properties of a semiconductor device from proposed physical and geometrical data. In addition, it is recommended that methods be established whereby these physical models for semiconductor device operation can yield the necessary parametric data for an accurate network representation of the proposed structure. This device modeling program is recommended to include both bipolar and MOSFET type of semiconductor structures.

An important implication drawn from this device modeling effort is the need to accurately model physical processes used for IC fabrication. For example, there is need for mathematical models that can predict the impurity atom distribution

arising from diffusion into silicon. Similar needs exist for predicting the impurity atom distribution arising from ion implant techniques, and the subsequent thermal diffusion from an implanted profile. It is recommended that a program of research be initiated that will yield the basic information needed to develop mathematical models for these (and other) IC fabrication processes. In addition, it is recommended that such mathematical models be implemented in computer programs that are applicable for IC design and engineering purposes.

It is also suggested that software system development for IC design have neglected some important aspects of this problem. For example, problems of computational stability exist in software systems for IC analysis, and there is little (or no) effort directed toward the solution of these problems. Furthermore, these software systems have not been developed with a view toward a rigorous application of device and process models. As a consequence, it is proposed that techniques of design optimization be applied in the design of IC structures at a process level; thereby, we can develop a capability to desensitize their electrical characteristics to fabrication process variations.

All recommendations presented here are a consequence of extensive investigation into problem areas associated with IC design and development. Three well-defined programs of effort are recommended:

1. The development of models for semiconductor device operation.
2. The development of models for IC processing techniques.
3. The development of a software system for IC design that can adequately utilize these new modeling capabilities.

Each of the above programs involve fundamental research, the development of mathematical models to approximate specific aspects of IC operation, and an experimental verification of these mathematical models. In addition, it is proposed that each of these models be implemented into computer software systems that are applicable to IC design and development.

Investigation and Study of Computational Techniques for the Design and Fabrication of Integrated Electronic Circuits

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CHAPTER I

Introduction

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CHAPTER I

INTRODUCTION

§1.0 General

Many Department of Defense (DoD) system contractors use integrated electronic circuits (IC's). These semiconductor structures are utilized in a large number of different applications: communication systems, radar, control circuits for ground-based equipment, etc. This new technology provides a means whereby the packing density of electronic circuits can be a thousand-fold greater than densities previously obtained using discrete component circuitry. This large packing density offers important advantages in many DoD systems.

A large number of different IC structures are available in the commercial marketplace (and at an exceedingly low cost). However, these structures seldom satisfy DoD requirements. The integrated circuits required by DoD usually introduce special problems of design and manufacturing, and these problems are well known throughout the electronic industry. In past years industrial organizations have enthusiastically offered their facilities for the design and development of electronic equipment specifically intended for DoD systems. Today this situation has changed. The semiconductor industry is often unresponsive to procurement requests for special IC

structures, and when this industry is responsive the cost is excessive.

In some situations this procurement problem has been alleviated by establishing DoD in-house IC design facilities. Also, numerous DoD system contractors have established independent in-house IC facilities. In many cases these in-house facilities offer a means for obtaining IC structures that cannot be easily (or economically) procured from commercial semiconductor organizations. From a long term viewpoint, however, it is not clear that these in-house IC facilities represent an adequate solution for this procurement problem.

Prior to initiating this study project numerous representatives of the semiconductor industry were consulted in order to obtain opinions concerning the source of this procurement problem. Little was gained from these consultations--each person offered a different opinion. Despite this divergence of opinions there was one suggestion offered by many industrial organizations: low cost IC structures could become readily available to DoD system contractors if they based their IC requirements upon commercially available structures. It was also warned that if these IC requirements are not based upon commercially available structures, an excessive procurement cost must be expected. The only solution offered for procuring nonstandard IC structures is to establish government supported design and fabrication facilities throughout the semiconductor industry. It was also stated that industry would not introduce these special structures into their existing commercial manufacturing facilities.

For this reason the present study project was undertaken with the purpose of understanding the fundamental sources of this difficulty. After gaining this understanding, a second goal for this project was to propose a solution that would be consistent with present industrial practices and, in addition, would minimize the IC procurement problem.

This study project was initiated with some insight into possible sources of this difficulty. It was recognized that despite the availability of numerous computer software systems for IC design, the total engineering costs for a new IC structure are excessively large. It was also recognized that DoD system contractors place procurement orders for IC structures that involve only a small quantity of devices of a given type; a substantially smaller quantity than is economically feasible for a large segment of the semiconductor industry. It was assumed that these two problems (costly engineering and small volume requirements) represent important sources of the present procurement difficulties.

A well-structured (and accurate) computer software system for IC design was initially believed to offer the potential for a substantial engineering cost reduction. In addition, it was believed that any rigorous evaluation of existing computer methods for IC design (and an alleviation of their shortcomings) would introduce a wide scope of fundamental questions that could not be answered by any individual engineer or scientist presently working in the field. Detailed information concerning the technical problems associated with the computer engineering of IC semiconductor structures requires input from

numerous specialists that are actively engaged in the solution of these problems on a day-to-day basis. Complications also arise because only a very few highly knowledgeable people in the semiconductor field would even be familiar with these underlying IC design problems, or be in contact with scientific specialists to whom specific questions could be directed.

For this reason, a steering committee was formed for this study program. This steering committee was composed of engineers and scientists who are recognized authorities in various technical aspects of the semiconductor industry: a list of steering committee members is given on page 6 of this report. To further enhance our ability to gain insight into this overall IC engineering and procurement problem, many steering committee members were requested to organize and chair workshops on their individual areas of specialty. The topics considered at these workshops were decided upon during an initial steering committee meeting at the University of Florida. It was also decided that for each workshop approximately six guests would be invited to offer opinions on yet unsolved problems that are known to prevent the development of a rigorous, cost saving, computer software system for IC design and engineering. In addition, these workshops offered the steering committee members an opportunity to question each specialist on IC design and engineering problems that are presently encountered throughout the semiconductor industry.

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Computer Aided Engineering of
Integrated Semiconductor Circuits

Steering Committee

Chairman: Prof. D.P. Kennedy, Univ. of Florida

Vice Chairman: Prof. F.A. Lindholm, Univ. of Florida

Administration: Prof. W.F. Kaiser, Univ. of Florida

Committee Members

Dr. W.M. Bullis, National Bureau of Standards, Washington, D.C.

Dr. M.J. Callahan, Motorola Corp., Phoenix, Ariz.

Prof. S.W. Director, Univ. of Florida, Gainesville, Fla.

Dr. W.J. Kitchen, National Security Agency, Ft. Meade, Md.

Prof. J. Meindl, Stanford Univ., Stanford, Calif.

Dr. H.G. Rudenberg, A.D. Little Corp., Cambridge, Mass.

Dr. C. Thornton, U.S. Army, Ft. Monmouth, N.J.

Prof. R. Van Overstraeten, Katholieke Universiteit, Leuven, Belgium

The topics selected for these workshops are as follows:

Topic	Chairman
Process Prediction and Modeling	C. Thornton (ECOM)
Semiconductor Device Analysis	D.P. Kennedy (U. of F.)
Test Sites for Manufacturing Process Evaluation	M. Bullis (NBS)
IC Analysis and Design	S. W. Director (U. of F.)
Microprocessors	G. Rudenburg (A.D. Little)

A detailed list of workshop guests is given in an Appendix to this report.

The following sections of this chapter provide an overview of some conclusions drawn from these workshops. In addition, brief outlines are presented on research and development that are recommended as a means to alleviate some of the existing IC procurement problems.

§1.1 Industrial IC Design and Manufacturing

An overview of industrial IC design and manufacturing problems places in proper perspective some important difficulties encountered throughout the semiconductor industry. In addition, such an overview provides insight into problem areas that contribute to the existing IC procurement difficulties experienced by both the DoD and the DoD system contractors. An important aspect of this overview is an identification of those problem areas that industry can be expected to eliminate, and those problem areas that will be eliminated in the near future only by possible government funding.

Industrial IC design and engineering techniques are, from practicality, influenced by economic necessity. Design and manufacturing problems receive extensive attention if they place significant limitations on the margin of profit realized from a given IC product. Problems having little impact on this margin of profit receive little attention. Sound business practices seek a maximum return. If technical problems result in costly IC design techniques, these costly techniques will be retained until there are sufficient financial reasons for modifying the situation.

To date, the semiconductor industry has a large investment in the development of software systems for IC design and engineering. These computational tools provide a means to solve IC design problems that would otherwise require an unreasonably large engineering staff. Clearly, this software system development involved a large financial investment, and this investment was directed toward the solution of problems that have a substantial influence on the margin of profit. Today, these systems are used by nearly every IC manufacturer in the semiconductor industry, despite the fact that there remain many important problems associated with the application of these software systems.

Numerous examples of these problem areas can be found in the application of modern software systems for IC design. For example, computer programs for the analysis of integrated circuits, and computer programs for establishing the layout and wiring of an integrated circuit, both suffer from unique prob-

lems associated with their application. Further, it is generally recognized that solutions to these problems would substantially reduce IC design costs. Despite this situation, these problems (and their solution) represent a low priority effort throughout the semiconductor industry. The economic impact resulting from these application difficulties remains small in a large-volume manufacturing situation.

Many aspects of IC manufacturing have a substantially greater economic impact upon the semiconductor industry than the initial design and engineering costs. A particularly costly situation is the volume of defective products encountered during IC manufacturing. Typically, 50% (or less) of all production starts yield satisfactory product at the output of a manufacturing line. If, indeed, a semiconductor manufacturer is forced to throw away 100,000 potential IC structures per month, in one year the loss of revenue from manufacturing scrap can exceed the initial design and engineering costs.

The semiconductor industry has become resigned to the fact that a poor manufacturing yield is inherent in the IC business, and that little can be done to modify the situation. Thus, a substantial financial investment is directed toward "cutting-short" this manufacturing loss--identifying faulty IC structures during the initial phases of a manufacturing process. Most semiconductor companies consider the continued processing of scrap a significant part of their manufacturing costs, and feel that the most expensive scrap are those bad IC structures reaching final test.

Another potentially dangerous problem in IC manufacturing is the stability of yield from a given production line. Few (if any) IC manufacturers believe their fabrication processes are under adequate control. Most manufacturers have experienced periods when the yield of good devices from a production line decreases to a disastrous level, and for no obvious reason. Thereafter, it may take several days (or weeks) to identify the source of difficulty and return the yield to an economically sound level. For this reason, the development of process monitoring techniques represents a high priority effort throughout the semiconductor industry.

For obvious reasons a substantial part of this process monitoring effort has been directed toward process stabilization, rather than toward the measurement of basic process parameters. It is often stated that the semiconductor industry must develop on-line measurement techniques that quickly identify inadvertent changes in any given process step. It would be informative if these monitoring techniques yield quantitative processes information, yet this type of information is less important than an ability to identify when changes have taken place.

These IC manufacturing problems, alone, provide some insight into the IC procurement problems experienced by the DoD and their system contractors. The inadequacy of process monitoring techniques produces an unstable situation that most manufacturers fear; therefore there is great reluctance to upset an IC production line that is producing a marketable product. For this reason, it has been stated by numerous IC

manufacturers that under no condition would they modify the process procedures used in a going production line to accommodate a small quantity order for special IC structures.

An important, and often unrecognized, aspect of the IC manufacturing problem is associated with production line start-up for a new product. Many well-established semiconductor organizations have undergone serious financial difficulties during this critical period. In fact, some new semiconductor component manufacturers are driven into bankruptcy before their new product manufacturing lines have become operational.

From a practical point of view, introducing a new IC product into manufacturing represents a large financial gamble. The techniques used for production line debugging are highly empirical, and the problems to be solved are often a consequence of many interrelated process variables. Further complications result from the large in-process fabrication time for IC structures; in general, experiments designed to improve the yield of good IC structures from a production line frequently require several weeks for adequate evaluation.

It is emphasized that present IC design techniques provide no satisfactory method whereby an engineer can evaluate, *a priori*, the consequences of manufacturing process variables upon the electrical properties of a new IC structure. Thus, an important aspect of manufacturing start-up sometimes involves redesign of the IC structure to accommodate these process variables; this redesign procedure is necessarily empirical in nature. A need for computational methods to aid in the solu-

tion of this problem has been stated by many IC manufacturers, and some study is underway toward this end.

The foregoing overview of industrial IC design and manufacturing problems provides some insight into the procurement difficulties experienced by the DoD and their system contractors. The large design and development costs for a new IC structure have serious consequences upon the ultimate cost for small quantity procurement orders. The semiconductor industry has little need to reduce this cost through research and development; adequate large volume business is available to operate their manufacturing lines at near full capacity. Present costs associated with IC design and development are not necessarily excessive for the large volume markets to which the semiconductor industry is presently directing its attention.

The problems associated with manufacturing yield are most important to the semiconductor industry. These yield problems are of minor direct importance to the small quantity user of IC semiconductor structures. For example, if a DoD system contractor requires 100 IC structures of a particular type, the cost differential is small if these structures are fabricated to either a 10% yield or a 75% yield of satisfactory components. This situation is particularly true in view of the cost for design and development of such a component.

There are indirect problems associated with these manufacturing difficulties that do, indeed, affect the small quantity user of IC structures. These problems produce a reluctance on the part of the IC manufacturers to

modify (in any way) the processes used in an operating production line. For this reason, fabrication of small quantity orders of IC's is often limited to off-line production facilities, which again increases the cost and limits the availability of such structures.

§1.2 Multiple Source IC Procurement

In §1.1 (Industrial IC Design and Manufacturing) many problems of IC design and manufacturing were outlined, with reference to the manner in which these problems impact the small quantity user of IC structures. In a similar manner we discuss here some difficulties these problems produce in establishing a second-source (or multiple-source) for IC structures. One must conclude from this discussion that a true "second source" for a given IC cannot often be established without a significant degradation of the electrical characteristics during initial design and development. This need for degrading the electrical characteristics is recognized by many IC design engineers, and it is often stated to be a serious (and important) problem.

A properly designed and documented discrete component electronic structure can, in general, be successfully produced by any qualified electronic manufacturer. Today, complex discrete component electronic circuits can be designed by one manufacturer and produced in large volume by another. Few problems arise in the transfer of information necessary to duplicate a given discrete component circuit by any knowledgeable electronic organization. To date, a similar situation has not

been achieved in the design and fabrication of semiconductor integrated circuits. In the absence of special design considerations, integrated circuits designed by one industrial organization can be adequately reproduced only by that organization. In fact, serious problems frequently arise within a given company when manufacturing for a particular IC is transferred from one production line to another.

The reasons for this situation are manyfold. One important source of difficulty is the small, inadvertent, process variabilities encountered in any IC manufacturing facility. Each step in the fabrication process (diffusions, oxidations, metallizations, etc.) is subject to small degrees of variability, and the magnitude of these variabilities differ from one production line to the next. Experience shows that two different production lines in a given company can exhibit substantially different process variabilities; an even greater difference can be expected between the production facilities of two different semiconductor manufacturers.

An additional source of difficulty arises from inadequate process monitoring techniques that are used throughout the semiconductor industry. Seldom will these monitoring techniques provide adequate characterization of an IC fabrication process. Most monitoring techniques are designed to show changes in a given process rather than quantitatively establish the important process parameters. Resulting from this situation is a self-consistent set of process monitoring tools within any one given semiconductor manufacturer; in general, all production lines can be expected to utilize the same monitoring methods. In

contrast with this situation, it is unlikely that two different semiconductor manufacturers will use an identical set of process-monitoring techniques. For this reason, transfer of an IC manufacturing process from one industrial organization to another can represent an exceedingly costly task. It has been found that the ultimate cost of such a transfer can sometimes be approximately equal to the cost of two independent design and development projects for the same IC structure.

Presently, this type of problem is successfully solved only through a significant loss of electrical performance. The IC designer first samples the electrical characteristics of devices (and other components) presently being fabricated by numerous IC manufacturers; this sampling is accomplished using special test structures. Thereafter, the new IC is designed while assuming a worst-case situation--the design is based upon the worst electrical characteristics selected from the entire set of experimental measurements. Experience shows this design technique yields an IC that can be procured on a multiple source basis. Unfortunately, a significant loss is realized in the resulting electrical characteristics.

§1.3 Overview of Proposed Research and Development

From the foregoing sections of this chapter it is evident that the present difficulties of IC procurement are a consequence of many interrelated problems. Some of these problems are self-evident and require little elaboration. Other problems are not frequently viewed as a source of difficulty within the semi-

conductor industry; IC design engineers have learned techniques whereby they can by-pass these problems, making a rigorous solution unnecessary. The purpose of this section is to provide an overview of problems that influence the procurement of small quantities of IC structures of an unique design. In addition, presented here is an outline for research and development that will alleviate the most important of these procurement problems.

There is substantial verification that computer software systems for IC design offer a significant cost reduction. The semiconductor industry has made a large financial investment in such software systems; thereby, heretofore difficult problems of IC design and engineering are solved at a cost that is economically practical within the framework of industrial requirements. An important difficulty arises because industry has little immediate need to further improve these software systems and, hence, to further reduce IC design costs. The semiconductor industry is directing its energy (and financial resources) toward yet unsolved problems that have greater impact on their margin of profit.

For this reason, it is suggested that this software development effort be continued under the sponsorship of ARPA. Implicit in this effort is an identification of problem areas in IC design that are costly and, thereafter, undertaking research directed toward the solution of such problems. In addition, solutions resulting from research must be implemented into software systems that are cost effective for the semiconductor industry.

The type of research necessary for this recommended program becomes evident by viewing those areas of industrial IC design where computational techniques are linked to engineering empiricism. One well-known link arises in the characterization of semiconductor devices for circuit design purposes. It is suggested these equivalent circuit approximations for semiconductor devices represent a technical boundary between two contrasting aspects of IC design:

1. Highly sophisticated computational techniques that apply classical methods of network analysis to the solution of complicated circuit design problems,

2. Heuristic methods of analysis where transistor engineers introduce extensive empiricism to solve problems for which there is only a limited amount of basic understanding.

There is ample evidence to show that research must be directed toward the solution of this particular problem.

Present industrial engineering practices effectively "by-pass" this problem. Highly heuristic engineering techniques are used to develop laboratory prototypes of new semiconductor devices. Thereafter, having fabricated a number of such devices, they are subjected to an extensive experimental characterization procedure: their electrical properties are measured throughout a wide range of operating conditions. Similar heuristic methods are next used to develop equivalent circuits to approximate the measured electrical properties of these devices. These equivalent circuits are used for computational investigations of the IC structures in which the devices are to be used. There are many obvious short-

comings of this overall technique but, in general, it has proven successful in an industrial environment. One important shortcoming is the necessity to fabricate and measure the semiconductor devices prior to circuit analysis.

It is proposed that research be directed toward the solution of problems that will eliminate this particular empirical aspect of IC design and development. A substantial cost reduction would be realized if a capability exists whereby the electrical properties of semiconductor devices could be mathematically predicted (from basic process parameters) prior to laboratory experimentation. Assuming this capability, the IC engineer could calculate the electrical performance of an IC and thereby establish necessary process modifications prior to fabricating such structures. This capability would eliminate the costly experimental empiricism presently used to optimize IC characteristics and maximize fabrication yield.

The availability of such computational techniques would offer important advantages to the DoD and their system contractors. Specifically, the design of an IC could be based upon measured process parameter information from each individual vendor. Suitable design modifications could be introduced into a required IC structure to assure that each vendor can satisfy the necessary electrical specifications using his particular fabrication processes. It would no longer be necessary to design on a "worst-case" basis to assure multiple sources for a given IC structure.

This proposal immediately introduces questions concerning the availability of such processing data from IC manufacturers. Traditionally, the semiconductor industry considers this type of information a company secret. Despite such problems, one IC manufacturer (Motorola) has given assurances that process information could be made available on a need-to-know basis. In addition, it has been stated that if unique IC structures could be fabricated on existing large-volume manufacturing facilities, it would represent a relatively simple (and inexpensive) solution to the problem. Under no conditions would these manufacturers modify the processes used in their production lines, although to utilize an existing fabrication facility represents only a bookkeeping problem that is easily solved.

Thus, the proposed research and development effort resulting from this study is directed toward the solution of the numerous problems of IC design that are presently solved by empirical techniques. Having gained this basic knowledge, it is proposed that computer software systems be developed that utilize this knowledge in the form of mathematical models suitable for engineering purposes. The most important of these problems is found in the area of semiconductor device physics and the fabrication processes for these devices. It is also proposed that the availability of these computational tools will make evident some important shortcomings in our existing computer techniques for IC design. These shortcomings must also be eliminated.

§1.4 Subdivision of Proposed Research and Development

The research and development proposed for this ARPA program falls into three well-defined categories:

A. Software Systems for IC Design

B. Semiconductor Device Research and Modeling

C. Process Prediction and Modeling

In each of these categories mathematical models are available to describe mechanisms for which there is presently adequate understanding. In contrast with these areas of adequate understanding, many problems must be solved for which present understanding does not agree with experimental observation; such problems are solved by empirical techniques. It is unrealistic to believe that this empiricism can be entirely eliminated from this IC design procedure. A more realistic goal is to undertake research directed toward those aspects of the IC design problem that are presently solved by empiricism and, at the same time, have a significant influence upon the ultimate cost of design and engineering.

A. Software Systems for IC Design

The software system aspects of this proposal have been influenced by two important factors: first, the successful industrial effort in this area and, second, the extensive financial support (both industrial and government) being directed on this topic. This proposed ARPA project has been designed to place emphasis upon the solution of problems presently not being undertaken by either government or industry.

It is often stated by IC design engineers that important difficulties arise in IC fabrication from inadvertent variations in the manufacturing process. Furthermore, a need has been recognized for computational techniques whereby one can calculate the consequences of these process variabilities upon the electrical properties of an IC. Attempts have been made to implement this capability into an existing IC circuit analysis program (ASTAP). These attempts, to date, have been unsuccessful. For this reason, it is suggested that research be undertaken that is directed toward the development of mathematical techniques whereby one can calculate the consequences of fabrication process variabilities upon the electrical properties of an IC.

Practical limitations of modern electronic computers place serious restrictions upon the size (or complexity) of electrical circuits that can be evaluated by computational techniques. For this reason, computer analysis of electrical circuits is accomplished on a basic cell format. These cells are experimentally interconnected to form a complete IC structure. This interconnection is accomplished with only limited knowledge of potential difficulties in the overall IC structure that can arise from electrical parameter variabilities (due to fabrication process variabilities) in each basic cell. As a consequence, it is not infrequent that one combination of cells is easily manufactured while another combination yields no satisfactory IC structures.

The semiconductor industry is presently developing methods whereby the electrical properties of each cell are representable as basic elements, and the consequences of their interconnection can be studied on a computer. This computational technique is called 'macro-modeling'. There is little indication that these macro-modeling development projects are directed toward the evaluation of difficulties that may arise from electrical parameter variabilities from each cell.

For this reason, it is recommended that the foregoing research on process variability analysis be undertaken on two levels:

1. on an elemental circuit level
2. on a complete IC level (using macro-modeling).

This computational capability will offer a means whereby IC design engineers can evaluate the adequacy of a new structure from a parameter variability point of view.

Assuming the successful development of the foregoing computational techniques, a new method must be developed whereby the multitude of process variables associated with IC fabrication can be adjusted in a systematic fashion to gain the desired results. This technique will provide a means to establish the combination of process parameters that essentially desensitize an IC structure to small process parameter variations.

It is emphasized that the foregoing multi-variable optimization technique would be applicable to many different aspects of IC design, other than at a circuit level. Heuristic methods are traditionally used in the design of transistors, resistors, etc., and there is need for a systematic design technique to accommodate the inadvertent process variabilities encountered during fabrication.

A final topic of research arises from problems of convergence and stability in IC circuit design programs. This problem is associated with the equivalent circuit representations of transistors that is used in these circuit design programs. A given equivalent circuit representation yields excellent (fast) convergence during circuit analysis of one type logic configuration, and poor (slow) convergence for another type logic configuration. Further, it is not uncommon to encounter instabilities during circuit design which implies a need to restructure the equivalent circuit.

The origin of this stability problem is not adequately understood, and there is substantial confusion concerning its elimination. For example, a given equivalent circuit representation will work satisfactory in one type of circuit analysis program, and it will produce instabilities in another circuit design program.

It is proposed that research be directed toward understanding, and eliminating this particular problem. Many

persons have suggested the problem could stem from algorithms presently used for analysis of integrated circuits, but there is little factual information on this subject.

In summary, the recommended research in areas of software systems are directed toward the evaluation of process variabilities upon the electrical properties of an IC. In addition, this research is directed toward designing IC's that are tolerant to those process variables. This research includes the development of computational methods for the following tasks:

A. Fabrication process analysis on an elemental circuit level.

B. Fabrication process analysis on a chip level (using macro-modeling).

C. Multi-variable optimization of IC structures.

D. Stability problems in circuit analysis programs.

B. Semiconductor Device Research and Modeling

During IC design, semi-heuristic network approximations (equivalent circuits) are used to represent the transistors in computer programs used to calculate the electrical properties of IC structures. The parametric information required for these equivalent circuit approximations is presently obtained by laboratory measurements upon typical transistors. This parametric information is often in the form of median values and the statistical spread for each parameter

(if available). It is frequently found that network approximations developed in this fashion do not adequately characterize the devices under consideration; when such inadequacies are encountered, heuristic modifications are introduced to satisfy a given requirement.

Fundamental problems arise when these equivalent circuits are used to calculate the consequences of manufacturing process variabilities upon the electrical properties of an IC (as in the IBM ASTAP program). Processes variabilities are introduced into circuit analysis through measured parametric data of the relevant semiconductor components. Thereby, it is implied that no correlation exists between the parametric variabilities in an IC and, as a consequence, unrealistic (and overly pessimistic) results are obtained. In short, this technique produces a "worst-case" solution that is inadequate for engineering purposes.

It is proposed that research be directed toward the development of rigorous mathematical models of semiconductor operation. The purpose of these models is to provide a computational link between the process parameters used for IC manufacturing and the electrical properties of the resulting semiconductor devices. Thereby, a means will be available for the IC circuit designer to establish parametric data needed for the equivalent circuit approximation for each semiconductor device. In addition, these models will provide a means whereby an engineer can establish the correlation between the electrical parameter variabilities that are encountered in any IC structure.

An initial research effort should be directed toward the most frequently used semiconductor devices: the MOSFET and the bipolar transistor. The purpose of this research is to obtain a quantitative understanding of numerous physical mechanisms contributing to the electrical properties of these semiconductor devices. After having gained this understanding, mathematical models that approximate these mechanisms must be implemented into computer software systems for the evaluation of practical semiconductor devices.

An intended goal for this effort is to provide IC engineers with a computational capability whereby basic fabrication process parameters can be introduced into a computer program, and from this input data the electrical parameters can be established for the resulting semiconductor devices. Having this capability, it will be unnecessary to undertake extensive empirical laboratory studies as a means to obtain a required semiconductor device.

In conjunction with the development of mathematical models for transistor operation, it is recommended that models also be developed for semiconductor structures to be used in fabrication process evaluation. Presently, the National Bureau of Standards has an experimental program underway that is aimed toward developing new semiconductor structures (test-patterns) for process evaluation. This recommendation would represent a joint effort with NBS on the evaluation of these structures;

such a cooperative effort would be advantageous to the overall goals of the DoD.

C. Process Prediction and Modeling

Important IC design problems result from an inability to quantitatively predict the impurity atom profiles in semiconductor material that result from some widely used fabrication processing techniques. For example, during the past 20 years the semiconductor industry has been using thermal diffusion for transistor fabrication, yet today we cannot adequately predict the impurity profiles resulting from a diffusion process. As a consequence, semiconductor device design is accomplished by empirical methods; the required electrical characteristics of a transistor are obtained by empirical process variations.

The purpose of this proposed research is to develop methods whereby the consequences of conventional semiconductor fabrication processes can be predicted, and thereby eliminate the need for empiricism. Substantial judgement is necessary in the selection of these research topics. This effort must be directed toward those processing techniques used extensively throughout the semiconductor industry, techniques also expected to be used in the foreseeable future. In addition, research must also be directed toward those processing techniques now under development. These techniques are expected to eventually be in widespread use throughout the semiconductor industry.

For this reason, it is recommended that research be directed toward a solution of the thermal diffusion problem. One goal for this research is to develop a mathematical model for impurity atom diffusion into silicon. This model should contain the numerous physical mechanisms known to influence impurity atom diffusion, thereby providing the degree of agreement between theory and experiment that is needed for semiconductor device design.

It is also proposed that research be directed toward a solution of the auto-doping problem encountered during epitaxial growth of silicon on silicon. Again, an important goal for this research is to develop detailed knowledge about impurity atom doping of the epitaxial layer, from a buried layer. Thereafter, the knowledge gained during this research is to be directed toward the development of a mathematical model for the buried layer impurity atom distribution, after epitaxial growth.

In conjunction with research on diffusion and epitaxial growth, it is also recommended that research be directed toward problems of ion implantation. This fabrication technique introduces technical problems for which there is little understanding. The purpose of this research is to gain a basis understanding to the degree required for semiconductor device design. After having gained this understanding, an important aspect of the research is to develop mathematical models for ion implantation that accurately predict those semiconductor parameters important to device analysis.

Oxide growth on silicon represents an important process in MOSFET fabrication, yet little understanding is available on this subject. The oxide growth rate is influenced by many factors. For this reason, processes necessary to attain a given oxide thickness have been determined empirically. Further, the electrostatic charges encountered in an oxide layer have a significant influence upon the resulting MOSFET; thus, empirical methods have been developed to reduce these charges. It is proposed that research be undertaken on the overall topic of oxide growth on silicon as a means to eliminate an important source of empiricism in the semiconductor industry.

CHAPTER II

Proposed Program Organization

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CHAPTER II

Proposed Program Organization

§2.0 Introduction

It is recognized that this program of effort is of sufficient magnitude to require several years for its completion; at this time it is estimated the entire program will involve 5 to 7 years of research and development. It is also recognized that the technical scope of this proposed project is too large to be undertaken by any individual university, or other semiconductor organization. For this reason, the plan for this program is to utilize, on a subcontract basis, the technical expertise of other organizations that have world recognition in the field of semiconductors.

It is proposed that the University of Florida form a program office for this proposed project--see Fig. 1. The program office will have the responsibility for project organization and evaluation, setting goals and benchmarks for the individual projects, financial planning, etc.; all decisions made by this office will be subject to review and approval by an executive committee. Further, this executive committee will have for technical guidance an advisory committee composed of scientists selected from both project associates and other knowledgeable persons in this field.

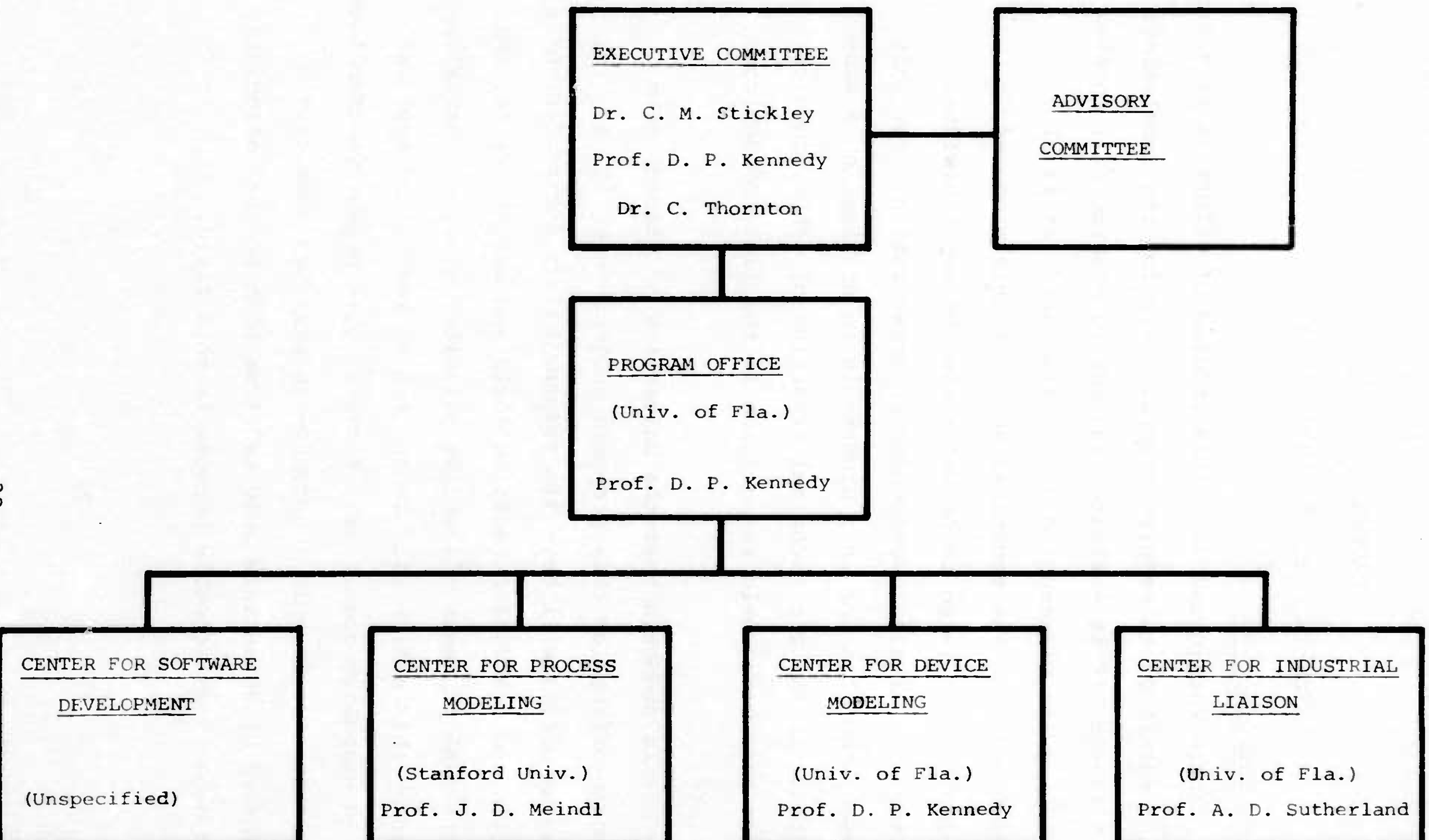

Fig. 1 Proposed Program Organization

In addition, it is proposed that the University of Florida, on a subcontract basis, form four centers to undertake responsibilities associated with many different aspects of this program:

Title	Location
Center for Device Modeling	University of Florida
Center for Industrial Liaison	University of Florida
Center for Process Modeling	Stanford Univ., Stanford, CA.
Center for Software Development	Unspecified

Each center will have a specified mission under this program, and the authority to issue subcontracts, hire consultants, etc. Further, these centers will have the responsibility to organize their individual programs, consistent with the overall project plans of this effort.

§2.1 Center for Device Modeling (Univ. of Fla.)

The Center for Device Modeling has the responsibility to develop mathematical models that adequately represent semiconductor device operation. This modeling task should be accomplished using two different approaches, and both of these approaches are of equal importance. First, from specified geometrical and physical properties for the semiconductor devices used in an IC, mathematical models are required whereby we can accurately predict the resulting low-frequency and high-frequency electrical characteristics.

Second, from these physical models of device operation, equivalent circuit approximations must be developed that are suitable for circuit analysis purposes.

In conjunction with this research, it will also be the responsibility of this Center to quantitatively evaluate the engineering capabilities of our present theory of semiconductor device operation. Clearly, this quantitative evaluation will be obtained only through a detailed comparison between the predicted electrical characteristics of semiconductor devices and their experimentally measured characteristics. This experimental evaluation will consist of both controlled laboratory experiments and a cooperative experimental program with large volume semiconductor manufacturers.

An important goal of this project is to establish computational methods whereby the electrical properties of semiconductor devices can be accurately established, without requiring the use of an unreasonable amount of computer time. In addition, such computational techniques must offer an ability to calculate the influence upon these electrical parameters of process parameter variabilities encountered during IC manufacturing. These aspects of device modeling will be the responsibility of this Center for Device Modeling.

There have been several different proposed methods for computing the consequences of manufacturing process variabilities upon the electrical characteristics of semiconductor devices. Some of these proposed methods appear satisfactory for the analysis of devices, yet unsatisfactory from a circuit analysis point of view. Similarly, methods that appear most satisfactory for circuit analysis have not been adequately studied from a device analysis point of view. Thus, techniques to be used for this aspect of the proposed IC design procedure remain undefined.

It will be a responsibility of the Center for Device Modeling to establish the method to be used for this aspect of the proposed IC design technique--which we call Manufacturing Process Simulation. A study of the associated problems will be established in cooperation with the Center for Software Systems; the purpose of this study is to develop a computational method that is practical from both a circuit analysis point of view and from a device analysis point of view. From this study should evolve a prescribed program of research to be undertaken by both Centers that will lead to an ability to computationally simulate IC manufacturing.

In conjunction with modeling the physical mechanisms associated with semiconductor device operation, this Device Modeling Center is also responsible for modeling test sites

for process analysis of IC manufacturing facilities. The experimental aspects of this program will be done under the ARPA/NBS program, and the Device Modeling Center will provide computational back-up for this ARPA/NBS effort. An important aspect of this computational work is to investigate relative sensitivities of various process parameters upon the measured electrical characteristics of specific test site structures. Thereby, it is intended to select those test site structures most suitable for the previously mentioned analysis of IC manufacturing facilities.

Another important responsibility of this Center is an extension of the forementioned analysis of semiconductor device operation: the development of equivalent circuit representations of semiconductor devices that are applicable to the computer analysis of IC structures. These equivalent circuits must adequately characterize both the low frequency and high frequency electrical properties of semiconductor devices and, at the same time, these equivalent circuits must be sufficiently simple to be practical.

All of the forementioned areas of responsibility will involve the development of computer programs. The computational techniques, and other aspects of those programs important to user application, must be taken into consideration and suitably documented for user application.

§2.2 Center for Industrial Liaison

It has been often stated that industrial involvement is an important ingredient in a program of this type. This involvement can take many forms: direct financial assistance, technical assistance in the solution of identified tasks, application and evaluation of the computational techniques developed under this program, etc. The responsibility of this Center is to actively encourage and solicit this needed industrial involvement.

One technique suggested to encourage the participation (and help) of the semiconductor industry is by the organization of periodic workshops on topics investigated under this program. During such workshops, members of this research team could present technical results that are directly applicable to industry, and offer the necessary technical information for industrial implementation.

It has also been suggested that researchers involved in this project should be encouraged to present the results of their efforts at appropriate scientific meetings, in technical journals, etc. Further, publication of this research should take place at the earliest practical time.

Experience has shown that many industrial organizations are receptive to visitation and discussions with persons involved in this project. Initial efforts in this direction have produced offers of assistance and cooperation in the

solution of a large class of technical problems. It is believed that a concentrated effort in this direction will generate substantial industrial participation, and insure that the results of this research program become accepted (and used) throughout the semiconductor industry. It is the responsibility of this Center for Industrial Liaison to actively solicit industrial assistance in the solution of problems associated with the aims and goals of this project. Included in this responsibility is the formation of a suitable technique for information flow between this research program and the semiconductor industry.

§2.3 Center for Process Modeling

During past months an important deficiency in our present knowledge was continuously reinforced by this study program: an inability to predict *a priori* the consequences of most IC fabrication processes. It was generally agreed that this difficulty has been overcome by industry in a practical, yet inefficient, way--by laboratory empiricism. A major responsibility of the Center for Process Modeling is the elimination of this situation. Specifically, it is the responsibility of this Center to develop mathematical models for each IC fabrication process that is required for the design of an IC structure.

Clearly, this area of investigation is very broad in scope, and it includes many different IC fabrication processess: ion implantation, thermal diffusion, oxide growth, etc. As a consequence, it is important that detailed value judgments be made concerning each and every processing investigation to be undertaken under this program. These value judgments must be based upon a need, with relation to the overall aims and goals of this project. Specifically, it will be necessary to establish that each investigation is being directed toward the solution of a problem that must be solved before we can inexpensively design IC structures on a computer.

An important goal for each individual investigation is the development of mathematical models that adequately predict the consequences of a particular fabrication process. In many situations this mathematical model will take two different forms: first, a complex (and rigorous) model that provides the required accuracy and, second, a simplified (approximate) model that needs little computation time, yet offers sufficient accuracy for small variations from a given median. It is the responsibility of this Center to develop both types of mathematical model.

Ion implantation has become an important technique for IC fabrication. For this reason, a mathematical model for ion implantation must be developed that is suitable for IC

design and development. This mathematical model must adequately describe the ion distribution in silicon after implantation--both directly into silicon and through an intervening oxide layer. Furthermore, this mathematical model must provide all additional information required (distribution of lattice damage, etc.) to calculate the subsequent diffusion of these ions throughout the semiconductor material.

An important application of ion implantation is found in the fabrication of IC structures using MOSFET devices: ion implantation is often used to tailor the threshold voltage of previously fabricated MOSFET's. It is hoped that future research into fabrication processes will eliminate the need for such a tailoring procedure. Nevertheless, as a contingency measure it is believed that a model should be developed for ion implantation into a thin surface layer of silicon, through an intervening SiO_2 layer. This model should yield adequate information concerning the distribution of implanted ions and, in addition, it should yield adequate information concerning the states introduced into both the SiO_2 layer and the silicon during implantation.

During the past 20 years impurity atom diffusion into silicon has been used extensively for device fabrication. Despite this world-wide experience with diffusion as a device processing technique we cannot, today, adequately predict

the resulting impurity atom distribution; such information is necessary before one can accurately predict the electrical characteristics of devices fabricated by diffusion. Furthermore, many of the mathematical models used to characterize impurity atom diffusion in silicon are exceedingly heuristic in nature, and provide poor agreement with experiment. For this reason, it will be the responsibility of this Center to develop a mathematical model for impurity atom diffusion into silicon that is adequate for the aims and goals of this project.

Another aspect of this process modeling problem is the development of an adequate mathematical model for autodoping of epitaxially grown silicon during growth upon a silicon substrate. The important information to be gained from this effort is a model for the initial epitaxial layer doping produced by autodoping, prior to diffusion. From this particular model, it is intended to obtain an accurate mathematical description of the initial conditions from which buried layers of impurities diffuse into the epitaxially grown material during all stages of IC fabrication.

In addition to these forementioned tasks, it will be the responsibility of this Center to undertake research leading to an understanding, and characterization, of both thermally grown SiO_2 and vapor deposited dielectrics. The

purpose of this effort is to generate computer models of these insulators to be used in analyzing device characteristics, with sufficient accuracy to permit an adequate prediction of these characteristics prior to device fabrication.

§2.4 Center for Software Development

It will be the responsibility of this Center for Software Development to organize and plan a program of research and development that is directed toward the solution of important software problems encountered in the design and engineering of IC structures. Further, it will be the responsibility of this Center to have full knowledge of those areas of research where government and/or industrial research is being directed in this field. With this knowledge, the program of research undertaken by this Center will be aimed toward the solution of software problems that are not being adequately addressed by the semiconductor industry.

The principal effort of this Center will be directed toward the design and development of a computer program for the electrical analysis of an IC. This computer program will offer a computational capability not presently available throughout the semiconductor industry. Specifically, this computer program will offer a capability to calculate the electrical properties of an IC from basic process parameters,

using the mathematical models developed at other Centers under this program of effort. This circuit analysis program will also provide a capability to calculate the consequences of statistical process changes arising during IC manufacturing and, in addition, modify the basic design to desensitize a proposed IC to these process changes.

The research undertaken by this Center for Software Development will be directed toward the solution of circuit analysis problems associated with this project:

A. Stability and convergence of computational methods used for circuit analysis.

B. Process variability analysis at a circuit and at a chip level.

C. Utilization of design optimization techniques (or other methods) for the desensitization of an IC to process changes.

These particular problems have been identified by the semiconductor industry as representing important sources of difficulty (and cost) in the design of an IC.

An additional area of responsibility for this Center concerns the equivalent circuit representation of transistors, as used in circuit design programs throughout the semiconductor industry. A cooperative program of equivalent circuit development is to be undertaken by this Center, in

conjunction with the Center for Device Modeling. This program of development is to be directed toward well known problems of stability and convergence associated with the electrical analysis of integrated circuits.

CHAPTER III

Proposed Program of Research

Semiconductor Devices

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CHAPTER III

Proposed Program of Research

Semiconductor Devices

§3.0 Introduction

Resulting from the workshop discussions on semiconductor devices (Appendix II), a program of research and development is proposed. This program was planned at the University of Florida under the direction of Prof. D. P. Kennedy, principal investigator for the present study program. This proposal covers a research effort directed toward solutions of those particular problems viewed by specialists in the field as contributing to the high cost of IC design.

The end goal for this proposed effort is the development of mathematical models for device operation that can be used for IC engineering. Included in this effort is an implementation of these models into computer programs to serve as engineering tools for the DoD and their system contractors. It is our intent that these computer programs offer a capability to accurately predict the electrical properties of a semiconductor device from basic fabrication processing parameters.

Suggested here is a necessity to develop two entirely different levels of device models, from the point of view of physical and mathematical rigor. A first level of complexity represents the most rigorous type of mathematical model that can now be developed for the analysis of semiconductor devices;

for calculations of both steady-state and transient operation. A second level of complexity represents simple, but no less accurate, mathematical models for device operation. This second type of mathematical model has the particular advantage of an increased computation speed, which is of great importance for the solution of a large class of engineering problems.

Rigorous mathematical models of transistor operation offer a capability to study, and understand, the complex mechanisms involved in bipolar transistor operation -- a problem emphasized by many specialists in the field. It is fully recognized that rigorous calculations of this type are of only limited value to the device designer. Experience shows that rigorous calculations of semiconductor device operation involve an excessive amount of computer time and, therefore, are economically impractical for IC design and development. Nevertheless, the understanding gained from such calculations will provide the foundation for developing simple computational methods for device engineering.

Many (but not all) importantbipolar transistor electrical parameters can now be accurately calculated using very simple mathematical models. Proposed here is a program of development to implement these concepts into a computer software system. These models have particular value to the device designer and, in addition, particular value in the design and development of

integrated electronic circuits. The computer time required for this type calculation is very small and, therefore, these models offer a capability to establish the parametric distributions arising from inadvertent fabrication process variations encountered in any IC manufacturing facility. Thereby, a means is available to implement the first step toward solving a problem voiced by a wide segment of the semiconductor industry: to desensitize an IC against these process variabilities.

Another need for this IC design procedure is satisfied through a proposed cooperative program of research between the University of Florida and the National Bureau of Standards. This effort is directed toward the development of test-sites that can be used to monitor important IC fabrication process parameters. It is proposed that mathematical models be developed for the test-sites under investigation at the NBS Laboratories. Using these mathematical studies we intend to identify individual process parameters that influence the measured test-site characteristics. This mathematical effort, in conjunction with the NBS experimental effort, is directed toward the development of techniques whereby an IC manufacturer can quantitatively evaluate each and every process parameter influencing IC performance.

It is emphasized that this proposed program of research is not intended to represent an abstract study of IC design theory. Throughout all phases of this effort detailed experimental verification will represent an important ingredient. Through laboratory investigations at the Univ. of Fla., in conjunction with industrial cooperation, each theoretical study will be evaluated for its agreement with experiment, and its applicability to IC design.

§3.1 Technical Program -- Bipolar Transistors

It is generally agreed that there is a need for mathematical models whereby the electrical properties of a bipolar transistor can be accurately calculated from process information. Presently, this capability does not exist, and the end goal for this proposed effort is to develop such a capability. This implies a necessity to undertake research in areas associated with the task: physics of bipolar transistor operation and mathematical techniques to be used. Proposed here is a program of effort directed toward this particular goal.

§3.1.1 Bipolar Transistor Analysis

Computational methods are now available whereby the electrical characteristics of semiconductor devices can be calculated on a computer. It is generally recognized that these methods are suitable for rigorous one-dimensional steady-state calculations of transistor operation. It is also recognized

that these methods are unsatisfactory for either one-dimensional transient calculations or two-dimensional steady-state calculations. In short, these computational methods often require an unreasonable amount of computer time. In fact, most people knowledgable in the field believe that two-dimensional transient solutions for bipolar transistor operation represent an unreasonable computational task.

A study of this problem has been undertaken by applied mathematicians at the Univ. of Florida. It has been concluded from this study that mathematical techniques presently used throughout the semiconductor industry might not be appropriate for the task at hand. Specifically, it is concluded that finite-difference methods used for the solution of differential equations could represent the source of two important problems: first, the excessive computer time required for transistor calculations and, second, computational instabilities that are frequently encountered by workers in this field. For this reason, in conjunction with the development of computer programs using conventional methods of analysis, we propose a study of other mathematical methods that could alleviate some of the existing computational problems.

One particular topic of mathematical investigation is the use of integral methods, as opposed to the existing finite difference methods. Although the resulting integrals are known to be intractable, from an analytical point of view, these

integrals can be evaluated numerically. Further, it is known that integral solutions of boundary value problems are inherently more stable than differential solutions. For this reason, it is believed integral methods of analysis will require substantially less computer time than presently needed for bipolar transistor studies.

In conjunction with these mathematical investigations, it is proposed that computer programs be developed for rigorous one-dimensional studies of bipolar transistors on a steady-state and transient basis. The purpose of this proposed effort is two-fold: first, to provide computational tools that are necessary for further studies of bipolar transistor operation and, second, to establish the groundwork for a similar effort toward the two-dimensional transient analysis of this problem.

It is recognized that several computer programs of this type have been under development throughout the country. For this reason, our aim is to build upon this effort, rather than duplicate this effort. The Univ. of Florida has received assurance that some of these computer programs will be made available for this project. The big problem is documentation; seldom do workers adequately document their efforts. From these workers we usually receive a deck of computer cards (or a computer tape), a program listing, and a two or three page set of operating instructions. Our task is to set up flow

charts of the main program and all subroutines, and to establish the precise method of computation used in each step of the analysis.

It is proposed that in this manner we obtain computer programs for the one-dimensional steady-state and transient analysis of bipolar transistors. These computer programs will be studied, documented, and a users manual written that offers adequate information for its use by other workers in this field. Thereafter, these computer programs will be given to the entire semiconductor industry, as a service offered under this program.

A similar situation exists for the two-dimensional steady-state analysis of bipolar transistors, except a computer program for this particular calculation is now available at the Univ. of Florida. In fact, we now have two versions of this computer program: one for the IBM/370 computer and another for the CDC/6600 computer. It is proposed that this computer program be adequately documented in a users manual and, thereby, be made available to all workers in this field.

It is emphasized that this two-dimensional computer program suffers from the same problems outlined in previous discussions: it is exceedingly time consuming under some modes of operation and, in addition, it exhibits many well known types of instabilities. As a consequence, further effort on this computer program is being proposed only because of its advanced state of development; it can be made available to the semicon-

ductor industry in a relatively short period of time, and with only a small amount of additional effort. It is believed that within the time frame for this proposed project, new and faster methods will be developed for the solution of this bipolar transistor problem.

Another proposed effort in this area is the development of a computer program for the two-dimensional transient analysis of bipolar transistors. Clearly, the development of this type of computer program represents a formidable task. Finite-difference methods of analysis (used in almost all modern mathematical investigations of transistor operation) are too slow for this inherently difficult problem. Furthermore, the application of finite-difference methods to this problem would require an unreasonable amount of computer memory. For this reason, the forementioned studies directed toward applying new methods of analysis to device problems must be undertaken before initiating this part of the effort.

This is not intended to imply that finite-difference methods of analysis cannot be applied to this problem. One worker in Germany has reported the results of two-dimensional transient calculations, using this method of analysis. This worker has openly admitted the use of extensive computer time in order to obtain his solutions.

A discussion on this particular calculation was undertaken in our workshop on Device Analysis (see Appendix II). The recognized difficulties associated with this particular calculation, in conjunction with the secrecy with which this worker has treated his computational methods, has produced elements of doubt in the minds of some specialists. In fact, one specialist suggested that a true transient analysis had not been conducted but, instead, it was a psuedo-transient type of calculation.

There are new indications that this German worker will provide suitable information on his computational methods. It is proposed we follow this path, in conjunction with studies of new mathematical methods for solving the two-dimensional transient problem. It is believed that this background will provide adequate information to establish a course of action directed toward a solution for this computational problem.

§3.1.2 Manufacturing Process Simulation

For many years semiconductor device manufacturing involved as much "art" as science. There are several reasons for this situation. One important reason arises from the extreme sensitivity exhibited by the electrical characteristics of a bipolar transistor to small variations in its fabrication process. Furthermore, a non-linear relation exists between these electrical characteristics and the fabrication process parameters; thereby we obtain an additional degree of complication. In

general, substantial experience is required to recognize the complex interrelation between the electrical characteristics exhibited by a given transistor structure and its fabrication process parameters; unfortunately, it is seldom this experience "carries-over" from one fabrication process to the other.

Despite an extensive effort directed toward a solution for this problem, it has never been completely solved. Significant advances have been made in our device fabrication technology, yet these improvements are used to make better (and faster) semiconductor devices, and not to solve this problem of fabrication reproducibility.

For the foregoing reasons, manufacturing simulation on a computer of semiconductor device fabrication processes represents an important ingredient for the economical design of IC structures. This opinion has been voiced by persons involved in many aspects of IC design, development, and manufacturing (for example, see Appendices I, II, III, IV). Furthermore, this simulation ability offers a first step toward desensitizing IC structures to manufacturing process variations; an important aspect of this IC design problem (see Appendix IV).

Using experimental process parameter data, a psuedo-random number generator is adjusted to provide process parameters (and their probability distributions) in substantial agreement with experiment. Thereby, we obtain sets of calculated process

parameters, and each individual parameter exhibits the degree of variability (from one set to the next) that is encountered during device manufacturing. Furthermore, coupling can be introduced between selected process parameter variations to simulate correlations that may exist during device fabrication; for example, when two regions of an IC are fabricated using a single diffusion process.

From each set of process parameters generated in this fashion, an impurity atom distribution can be calculated that represents one of a family of distributions that will appear in manufactured semiconductor devices. Because the probability distributions of these calculated process parameters are in basic agreement with experiment, the resulting impurity atom distributions calculated from these parameters will exhibit a frequency of occurrence similar to that encountered in manufactured products.

Each impurity atom profile calculated in this fashion can be used in mathematical models for the semiconductor device under consideration. Thereby, using each profile we can calculate 15 to 20 individual electrical parameters for the resulting device. By repeating this sequence of calculations for one to five thousand different impurity profiles, we can approximate the electrical parameter distributions obtained from the semiconductor devices manufactured on a given production line.

Several years of experience have been gained using this computational technique for the evaluation of bipolar transistor manufacturing processes. This experience shows that the agreement between theory and experiment is satisfactory for engineering purposes. Furthermore, this experience also shows the value of simplistic mathematical models for this particular application, as compared to the models used for initial device design.

The usefulness of these simplistic models (containing many, relatively crude, approximations) arises from the fact that each individual profile calculation (and the associated electrical parameter calculations) represent only a small perturbation from the median impurity atom distribution. For all practical purposes, this calculation is a type of perturbation analysis, rather than an analysis of structures of widely different physical and electrical properties.

The fundamental necessity of using simplified models becomes obvious when we consider the number of individual calculations associated with a given process simulation. Assuming a statistical sample consisting of five thousand different impurity atom profiles, we could calculate an aggregate of one hundred thousand individual electrical parameters for the resulting semiconductor devices. Clearly, unless simple (and easily calculated) mathematical models are used, the total computer time would be prohibitive.

Many years of experience are available in the simulation of bipolar manufacturing procedures. An important conclusion drawn from this experience is that electrical parameter distributions observed in bipolar transistor manufacturing are mostly a consequence of variations in the vertical profile of the structure (perpendicular to the semiconductor surface). For this reason, no reason has yet been found to use device models that are more complex than one-dimensional approximations; this greatly simplifies the obvious problems of computation speed. It is emphasized, this statement is based upon past experience. It is possible that further development of this computational technique will show the necessity of introducing more complex mechanisms into these models for a bipolar transistor.

For the foregoing reasons, it is proposed that a project is undertaken at the Univ. of Florida to simulate the fabrication of bipolar transistors on a computer. This project will involve the development of simplistic mathematical models that can be evaluated at high speeds on a computer, in the manner previously outlined. Resulting from this simulation are the parametric variabilities for the equivalent circuits used during IC analysis; these parametric data will contain all correlations needed for IC analysis and process desensitization (see Chapter V).

§3.1.3 Basic Research

An ability now exists to calculate many electrical characteristics of a bipolar transistor. Most (but not all) of the D.C. properties of this structure can be calculated, assuming a detailed knowledge of the impurity atom profile; the accuracy of such calculations are adequate for most engineering purposes (1% to 10%). Despite this situation there are many electrical characteristics that cannot be calculated, with any reasonable degree of accuracy. The reasons for this situation remain unknown, although it is often suggested that the inadequacies of our present theories arise from a lack of understanding about physical mechanisms associated with bipolar transistor operation.

Some important electrical characteristics of bipolar transistors for which we have limited (or no) understanding are as follows:

1. current gain
2. frequency (or transient) response
3. very low current operation
4. very high current operation
5. temperature dependence of the electrical characteristics

It is believed that problems associated with current gain and frequency (or transient) response may arise from a common source.

There has been substantial conjecture about the source of this difficulty. For many years it was believed that some of these electrical characteristics were strongly influenced by two-dimensional mechanisms of transistor operation, and our theory is essentially one-dimensional in nature. It is now becoming evident that a more serious problem exists. Namely, it is now generally acknowledged that mechanisms exist within a transistor that are not described by existing mathematical models. For this reason, basic research must now be directed toward bipolar transistor operation as a means to gain understanding about these mechanisms.

A. Current Gain and Frequency Response

Traditional concepts concerning physical mechanisms associated with current gain and frequency response have tended to lead us astray. Specifically, existing theory of transistor current gain yields results that are in poor agreement with experiment: the calculated gain is substantially greater than the measured gain. To alleviate this situation we have assumed a very small minority carrier lifetime in our mathematical models (about 10 ns) and, thereby, brought theory and experiment into reasonable agreement. There is little (or no) experimental evidence to prove the lifetime is, in fact, this short. We have assumed a lifetime that provides reasonable agreement with experiment, and explained it away as a consequence of device fabrication processing.

There is now substantial evidence to show that the emitter injection efficiency limits the current gain of a bipolar transistor. The reasons for this situation remain unknown, although there are many unproven theories capable of explaining the phenomenon. Two of these theories claim the high emitter region doping represents an important source of difficulty. One high doping theory proposes a band-gap change, with an increase of doping, and thereby obtains substantial agreement between experiment and theory (see Appendix II). Another high doping theory proposes that the density of recombination centers in silicon increases faster than the increase of doping. Thereby, a spatially dependent minority carrier lifetime exists within the emitter region; a mechanism not considered in existing models of transistor operation.

It is proposed that the Univ. of Florida undertake a program of research directed toward answering these questions. Initially, this research will be directed toward the problem of emitter injection efficiency and its influence on current gain. Included in this research are basic studies of high doping in semiconductor material, and its influence upon the band-gap of silicon. Despite the stated agreement between experiment and theory (Appendix II) there is increasing evidence to show that the doping range used in bipolar transistor fabrication produces little (or no) band-gap change. Nevertheless, there is experimental evidence implying that the emitter region

electric field arising from an impurity atom gradient is substantially smaller than its theoretically predicted value; if so, this situation could produce a reduced minority carrier injection efficiency.

This particular problem is of great importance to the semiconductor industry. There is experimental evidence to show an inadequate injection efficiency is presently being compensated by a base width reduction. An important consequence of this situation is a substantial yield reduction during bipolar transistor fabrication, due to pipes.

It is also proposed the Univ. of Florida undertake a program of research directed toward an understanding of the other forementioned problems of bipolar transistor operation. The overall goal of this effort is to gain the required understanding to introduce into mathematical models the associated physical mechanisms. Thereby, these models will provide better agreement between experiment and theory than is presently obtainable.

§3.1.4 I^2L Studies

It is becoming increasingly evident that I^2L type logic structures will be important in the future design and development of integrated circuits. Further, it is becoming increasingly evident that current gain of the vertical transistor is an important property of this structure. Thereby, our models for I^2L operation contain the same inadequacies as our models

for bipolar transistor operation: an incomplete characterization of the mechanisms associated with current gain.

It is proposed the Univ. of Florida undertake the development of one-dimensional and two-dimensional mathematical models for the I^2L type semiconductor structure. Initially these mathematical models would be based upon steady-state type operation as a means to fully establish electric current flow paths within this structure. From research on the current gain problem, at a later time these models will be updated to include detailed mechanisms associated with vertical transistor current gain.

Initially, no consideration will be given to the development of a two-dimensional transient solution for this problem. At a later time, after bipolar transistor transient analysis problems have been solved, the development of a computer program for the two-dimensional transient analysis of an I^2L structure should represent a straightforward task.

§3.2 Technical Program-MOS Transistors

It can be shown that traditional theory for MOSFET operation contains a multitude of simplifications and approximations that are clearly inapplicable in many situations. Experience has shown (see Appendix II). that this theory yields poor agreement with experiment for the weak inversion mode of operation. Further, this theory yields poor agreement with experiment for MOSFET structures containing a channel length less than about 7μm.

A careful review has been made of all proposed modifications of traditional MOSFET theory as a means to attain better agreement between experiment and theory. This review shows that most proposed modifications are extensions of traditional theory, without taking into consideration inherent inconsistencies contained within this theory. Furthermore, many of these proposed modifications are heuristic in nature, with a sufficient number of adjustable constants to assure agreement between experiment and theory.

As a means to alter this pattern of research, this proposed program is directed toward an elimination of heuristic methods in the analysis of MOSFET operation. A computer program is now available for the rigorous two-dimensional steady-state analysis of this semiconductor device. The mathematical equations solved by this computer program represent general mechanisms associated with hole-electron transport in semiconductor material; these equations are derived from solid-state physics, and they are not unique to the device under consideration. Further, the electrical properties predicted by this computer program agree with experiment, particularly in regions of device operation where traditional theory fails: short channel structures and weak inversion operation.

It is proposed that the Univ. of Florida undertake, under this program, a study of the physical mechanisms involved in

MOSFET operation that could not be studied on an experimental basis. Thereby, in a computational sense, we can "see" inside the MOS transistor and accurately evaluate the dominant mechanisms influencing its electrical characteristics.

It is believed this technique of analysis will yield a simple one-dimensional solution for MOSFET operation that is adequate for the design and engineering of a wide class of MOSFET structures.

§3.2.1 MOS Transistor Analysis

The steady-state two-dimensional computer analysis of a MOSFET represents a substantially easier problem than a similar analysis of a bipolar transistor (see §3.1.1). For this reason, under the direction of Prof. D. P. Kennedy such a program was developed for IBM in about 1971. Since that time, under his direction, an improved version of this computer program has been developed at the Univ. of Florida. As a consequence, this program would be available for MOSFET studies at the initiation of this project.

Several requests have been received from the semiconductor industry for copies of this computer program. To date, these requests remain unsatisfied, due to inadequate documentation of this two-dimensional computer program. It is proposed that we fully document in a users manual all information needed for the use of this computer program and, in addition, all information

required for its improvement and modification by other workers in this field. Thereafter, it is proposed that this computer program be offered to the semiconductor industry as an output from this ARPA program.

Despite the availability of this steady-state two-dimensional computer program for MOSFET analysis, the development of a transient counterpart is not recommended at the initiation of this project. Instead, it is recommended that the mathematical studies outlined in §3.1.1 get well underway before this aspect of the MOSFET problem be undertaken.

§3.2.2 Manufacturing Process Simulation

It has been emphasized by numerous representatives from the semiconductor industry (see Appendix IV) that simulation of the IC manufacturing process, on a computer, represents an important problem to be solved under this program of effort. This capability, in conjunction with the development of design optimization techniques, could offer a means whereby an IC can be designed for a minimum sensitivity to manufacturing process changes. This particular direction of research and development is viewed as a solution (or partial solution) to the multiple source problem encountered by most DoD system contractors.

As in the simulation of bipolar transistor manufacturing (§3.1.2), MOSFET manufacturing will require the development of simplistic mathematical models that can be quantitatively

evaluated on a computer at high speed. Thereby, we rule out the forementioned two-dimensional analysis methods. Nevertheless, this simplistic mathematical model must, of necessity, yield results that are in substantial agreement with experiment.

The development of such a mathematical model is now underway, and it is recommended that this effort is continued under this proposed ARPA program. Unlike the traditional theory of MOSFET operation, this effort is directed toward a one-dimensional analytical method that implicitly contains the two-dimensional mechanisms known to be associated with MOSFET operation. Thereby, we obtain a simplistic one-dimensional theory that will offer adequate agreement with experiment for MOSFET structures of any arbitrary channel length, and for any degree of channel inversion.

§3.2.3 Basic Research - MOSFET

There are numerous unanswered questions associated with the operation of MOSFET structures. A question of particular importance is the reduced mobility of inversion layer carriers (see W. Latton, Appendix II). The weak inversion mode of operation yields an inversion layer carrier mobility that is approximately one-half its measured value in bulk semiconductor material. Another reduction of about one-half is realized in the strong inversion mode of operation. Traditionally, this mobility reduction is attributed to scattering at the oxide-semiconductor inter-

face, although it is not entirely clear that this interpretation is correct.

It has been suggested by C. T. Sah (see Appendix II) that oxide-semiconductor interface roughness extends into the semiconductor material to a depth of about one lattice constant (5Å). It is indeed difficult to understand how surface roughness could significantly influence the mobility of inversion layer carriers.

A similar argument could be developed concerning coulomb scattering of mobile carriers by interface charges. Carriers within this inversion layer provide an extensive degree of coulomb shielding and, thereby, minimize the mechanism of coulomb scattering. It is again difficult to understand how this traditional concept of inversion layer carrier scattering can have a significant influence upon inversion layer mobility.

Furthermore, it is now recognized that traditional electrostatic mechanisms, alone, are not applicable to a mathematical calculation of the inversion layer carrier distribution. It has been experimentally and theoretically established that the energy of these carriers is quantized in a direction perpendicular to the oxide-semiconductor interface. Hence, quantum mechanical mechanisms cannot be neglected in such a calculation. An initial quantum mechanical study of this problem shows that the inversion layer carrier distribution can differ, significantly, from classical theory, yet there is an inadequate understanding of this overall problem.

This particular aspect of MOSFET operation is presently under investigation at the Univ. of Florida. A quantum mechanical analysis is being made of this inversion layer carrier distribution, with an aim toward understanding the carrier mobility problem. An end goal for this project is to develop a mathematical model for inversion layer carrier mobility, and its dependence upon the applied gate voltage. It is proposed that this research become a part of the ARPA program, because it is directed toward the solution of problems that significantly influence the design and development of this semiconductor device.

Another problem of particular concern are hot-carrier mechanisms encountered in the inversion layer of a MOSFET. It is indeed evident that increased demands upon IC operating speeds will produce a trend toward short channel MOSFET structures. It has been experimentally verified that hot-carrier mechanisms are encountered in a short-channel MOSFET, and that these mechanisms can produce serious modifications of the resulting electrical characteristics. It is proposed that a study of this problem should be an integral part of the basic research program on MOSFET operation.

The importance of this problem was emphasized by Prof. C. T. Sah (see Appendix II). Solid-state theory suggests two distinctly different relaxation times in semiconductor material. The momentum relaxation time in silicon is approximately 10^{-12} sec.

and, therefore, should produce little (or no) difficulty. Initial calculations imply an energy relaxation time of about 10^{-9} to 10^{-10} sec. It is suggested that this energy relaxation time could produce a fundamental limitation upon the maximum operating speed of a short-channel MOSFET. For this reason, the topic should be thoroughly investigated.

A topic of great concern to the semiconductor industry has arisen since our workshop on semiconductor device analysis. Namely, it has been experimentally observed that short-channel MOSFET structures exhibit problems of instability when operating in electric current saturation. This instability appears as a time dependent change in the volt-ampere characteristics. Further, this instability produces a change of threshold voltage when the source and drain islands of a device are interchanged. Thus far there is only limited understanding of this problem, and much confusion concerning its origin.

A qualitative explanation is based upon the mechanism of carrier multiplication in the drain junction space-charge layer. It has been suggested that secondary carriers from this multiplication process gain sufficient energy from the substrate electric field to enter the gate insulating oxide, in the vicinity of the drain junction. Thereby, this region of the oxide acquires an electrostatic charge that is capable of modifying the electrical characteristics of this device.

The importance of this problem becomes evident, in view of short-channel MOSFET trends throughout the semiconductor industry. For this reason, it is suggested that research should be initiated at the Univ. of Florida on this topic. The goal for this proposed project is to understand the fundamental source of difficulty and, thereby, develop engineering techniques for its minimization.

§3.3 Technical Program -- Test Sites

A large segment of the semiconductor industry uses test-sites for process monitoring. These test-sites take two distinctly different forms:

1. small test patterns located on each slice of semiconductor material processed for IC fabrication
2. slices of semiconductor material used for test purposes only, and processed through selected steps in IC fabrication.

In general, the first type of test method provides detailed information concerning the variations occurring in IC manufacturing, whereas the second type offers only gross information about individual processing steps.

Although the use of small test patterns on each slice provides substantial detailed information, this method of process evaluation offers many shortcomings. An important difficulty

arises from the delay time associated with an evaluation of this type test site is usually undertaken after completion (or near completion) of all IC processing procedures. As a consequence, if difficulties are detected it is likely that these difficulties have been underway for a substantial period of time and, in some serious situations, the production line is loaded with defective IC structures at various stages of completion.

Contrasting with this forementioned situation, processing test wafers along with IC fabrication provides the needed "early-warning" about production difficulties, although this method lacks the required accuracy. Seldom can test wafer structures be designed to monitor a given fabrication process with the sensitivity required for production control.

As a consequence, the semiconductor industry tends to use both process monitoring techniques. Frequently, the test site technique involves an array of large active devices, of the type used in the IC being fabricated; the increased size permitting probing and direct parameter measurement. Thereby, a detailed evaluation is obtained concerning the devices in an IC when, in fact, the characteristics of these devices cannot be measured. In addition to duplicating the active devices in an IC (except for physical size) these test sites sometimes include test patterns designed to monitor specific aspects of a fabrication process; aspects that could not be monitored through active device measurements.

Frequently the test wafer technique of process monitoring is limited to indirect measurement techniques: sheet resistance, epitaxial layer thickness, oxide thickness, etc. Although this monitoring technique provides important in-line processing information, the correlation of this type measurement to the process (or to the electrical properties of an IC) is sometimes a difficult task. It can be shown that test wafer measurements are often influenced by a multiplicity of different process variables, and one must make a judicious guess to locate the source of manufacturing problems indicated by such measurements.

Despite these difficulties, the semiconductor industry has been successful in their application of these process monitoring techniques. Furthermore, there is extensive experience in this area concerning what can (and what cannot) be accomplished using test sites. For example, it is fully recognized that test site measurements must be inherently simple; such measurements must be appropriate for automatic test equipment. Complex measurements like the transient response of a transistor cannot be used for process monitoring.

This industry's wide experience introduces other implications with regard to our proposed program of research on test-sites. Namely, the semiconductor industry has become familiar with a particular group of test patterns used on these test sites, and they will be reluctant to change without substantial justification. Further, a test site change involves modifications of

existing automatic test equipment, data storage and retrieval techniques, etc.; this could represent a costly and time consuming effort to many semiconductor manufacturers.

It is proposed that an important "first-step" for research in this area is to offer the semiconductor industry information they do not presently have about their existing test-site patterns. Specifically, through a mathematical analysis of existing test patterns it is proposed that fundamental understanding can be gained concerning the relative sensitivity of these patterns to individual IC processing parameters. Thereby, this program of effort will provide the semiconductor industry with important information that can be immediately applied to IC manufacturing. Furthermore, through this effort we can determine those particular fabrication processes that can (and cannot) be directly monitored today, and the need for future test pattern design and development.

Past experience shows that Monte Carlo methods of analysis are of particular value in the analysis of IC fabrication process test patterns. A mathematical model for these test patterns can often be developed in terms of fundamental process parameters associated with the IC fabrication. Thereafter, a psuedo-random number generator is used to vary each process parameter simultaneously, yet independently, similar to that experienced in any manufacturing facility. Thereby, a quantitative evaluation can

be made concerning the influence of each process variable upon the electrical measurements of each test pattern.

This area of investigation is an obvious overlap with the program of research now underway at the National Bureau of Standards. For this reason, it is proposed that test-site research represent a cooperative effort between the Univ. of Fla. and NBS. Because mathematical modeling represents an important part of the overall Univ. of Fla. effort, it is proposed that this effort be extended to include a mathematical "back-up" for NBS. Thereby, the Univ. of Florida will develop computational techniques and undertake mathematical studies to assist NBS in their test pattern research program.

§3.4 Proposed Technical Program -- Equivalent Circuits

The objective of equivalent-circuit modeling is to find a set of device-model equations suitable for the computer simulation of circuit behavior. Because of their intended use in computer-aided circuit analysis, the device-model equations are represented in the form of an interconnection of circuit elements--usually non-linear resistors, capacitors, and controlled sources.

Ideally, such a network representation of device behavior would have the following properties:

(a) It would represent both dc and transient response.

(b) It would represent the response to large-signals, thus accounting for the non-linearities inherent in the device.

(c) It would converge rapidly in all commonly used computer circuit analysis programs for any circuit of interest.

(d) It would be composed of circuit elements whose parameters are accessible to the circuit designer and are explicitly related to the parameters describing the device materials and structures.

(e) It would represent the device with the accuracy required by the circuit being analyzed. (This implies the need for a method of determining which aspects of the device characteristics affect significantly the performance of a given circuit.)

These five properties also constitute the goals of equivalent-circuit modeling.

In large part, the major deficiencies of the present-day models have the same origin as that discussed earlier in connection with the device-physics studies: the models fail to be based on an accurate and detailed understanding of the physical mechanisms governing device operation. Rather, they are based on a set of idealizing approximations augmented by the inclusion of enough adjustable parameters and circuit elements to enable agreement with experimental observations.

Because of the unavailability now of accurate and detailed modeling consistent with the internal physical mechanisms of device operation, curve-fitting models of this sort see wide employment in industry and have been developed to a high degree of sophistication. For a given design, one can always use such models to fit theoretical prediction with experiment if there are less observables of interest (propagation delay, logic swing, etc.) than there are independent variables (junction depths, surface concentrations, threshold voltages, parameters of the mask geometries, etc.).

The problem further is compounded by the large number of variables present. In part, these result from the inescapable variability deriving from the processing: variability of junction depth, of surface impurity concentration, of substrate concentration, of gate width and length, etc. The variability resulting from temperature causes additional problems. Customers are increasingly imposing reliability requirements on the manufacturer; and some of these requirements define the acceptable performance of a circuit over a given temperature range. Without an understanding of the physics of device operation imbedded in the equivalent-circuit models, one cannot achieve the maximum complexity yielded by the present technology. One must back away and do a very cautious over-design.

Such backing away becomes all the more prevalent as the technology becomes able to provide devices for which the idealizing approximations of the existing equivalent-circuit models fail severely. A current example is short-channel MOS devices. The inability to model short-channel effects accurately and consistently with the internal device physics greatly frustrates the ability to design effectively with such devices.

To a major extent, the deficiencies in the present-day equivalent circuit models for the MOS and bipolar transistors originate in the approximations they contain. Because the models largely have been derived in a heuristic and intuitive manner, the approximations imbedded in them remain obscure. Two general kinds of approximations can be identified, however, that appear to bear strongly on the inadequacies of the models:

A. REDUCTION-OF-DIMENSION APPROXIMATION:

By this approximation, one translates two- and three-dimensional boundary-value problems into coupled one-dimensional problems, thus achieving much simplification in the analysis of the device physics. Many examples exist of this piecewise one-dimensional method of analysis: the resolution of a device into intrinsic and extrinsic parts; Shockley's gradual case for field-effect transistors; characterization of the base resistance of bipolar transistors by regarding the

bipolar transistor as comprising many one-dimensional transistors connected in tandem, etc. The reduction-of-dimension approximation may introduce serious shortcomings, for example, in the modeling of short-channel MOS transistors and of bipolar devices in the inver-active and saturated operation for I^2L circuits.

B. QUASI-STATIC APPROXIMATION: By this approximation, to describe the response to time-varying excitation, one extrapolates functional dependencies for charge and current that are valid only in the dc steady state. In this way one represents the currents that flow to change the numbers of carriers accumulated in various parts of the device. This widely-used approximation is basic to the set of charge-control and Ebers-Moll models for the bipolar transistor, and to its counterpart for the MOS transistor.

Various aspects of the circuits and devices of the modern silicon technology -- smallness of device dimensions, inverse and saturated operation of transistors, speed of response, etc. -- tend to invalidate these two kinds of approximation. As we shall discuss, one part of the recommended program will concentrate on delineating the limits of validity of these approximations and on extending this validity where needed.

RECOMMENDED PROGRAM

The overall objective of the recommended program is to seek network representations for semiconductor devices that approximate the ideals [(a) through (e)] listed earlier. This list suggests the following general approach:

(a) Close ties with the semiconductor industry -- both to keep abreast of engineering needs as the technology advances and to secure industrial assessment and utilization of the network representations as they are developed.

(b) Computer experiments to help guide the development of the models, both from the standpoint of device physics and that of circuit analysis. The models should be consistent with the internal physics governing device behavior. Yet they also should enable rapid convergence in circuit-analysis programs.

(c) Laboratory experiments to assess the degree to which the device-model equations represent reality and to help suggest approximations useful for refining the accuracy of the models.

CHAPTER IV

Proposed Program of Research

Fabrication Processes

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CHAPTER IV

Proposed Program of Research
Fabrication Processes

§4.0 Introduction

Resulting from the workshop discussions (Appendix I), a program of research and development is proposed. This research program was planned through initial discussions between Prof. D.P. Kennedy (Univ. of Fla.) and Prof. J. Meindl (Stanford University), and at a later time, between Prof. Meindl and numerous experts in the field. Following are essential portions of the final research proposal submitted to the Principal Investigator of this study program by Stanford University.

§4.1 Thermal Oxidation and Chemical Vapor Deposition

The purpose of this proposed investigation is to characterize the processes used to produce thermal silicon dioxide films and associated dielectrics, along with relevant electrical and physical properties so that complex integrated circuits with predictable characteristics may be fabricated at reasonably low cost.

§4.1.1 General

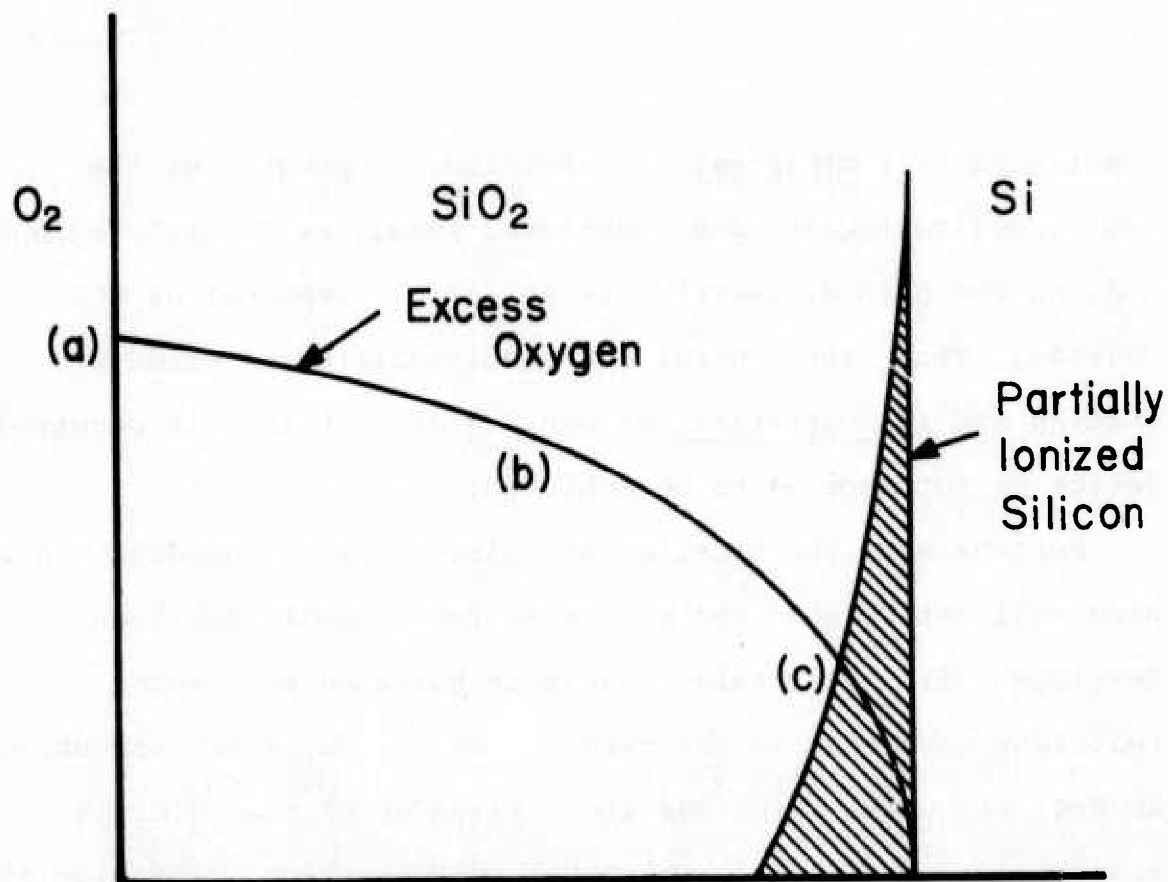
Thermal oxidation of silicon (SiO_2) is one of the key processes in integrated circuit fabrication. The oxide acts as a mask against dopant diffusion, allowing the preparation of

complex circuit patterns. In addition, it passivates the active device regions and junctions, insulates "field" regions, and, as the gate dielectric, is an actual component of MOS devices. Thus, the control and predictability of oxide processing and its electrical properties are critical if required device performance is to be achieved.

Fortunately, the kinetics of silicon thermal oxidation have been well established and a general relationship has been developed (1). This relationship is based on successive reactions occurring in the oxide being formed, which are shown in Fig. 2. These reactions are: transfer of the oxidizing species (O_2 or H_2O) into the outer oxide surface, diffusion of the species through the oxide, and reaction of the oxidizing species with silicon at the SiO_2-Si interface to form SiO_2. The general relationship is:

$$x_o + A\,x_o = B(t+\tau)$$

where x_o is the oxide thickness, t is the oxidation time, and A, B and τ are constants. These constants are a function of oxidation temperature, ambient, oxide properties, and silicon surface characteristics. Using this relationship, it would be possible to predict what oxide thickness would result from any series of oxidation steps and other high temperature heat treatments during IC fabrication. Cr, it would be possible to choose those process conditions which would result in a final desired oxide thickness.



$$x_o^2 + Ax_o = B(t+\tau)$$

where: $A = 2D(1/k + 1/h)$

$B = 2DC^*/N_1$

τ = Constant

For "large times,"

$$x_o \simeq Bt$$

For "small times,"

$$x_o \simeq B/A\,(t+\tau)$$

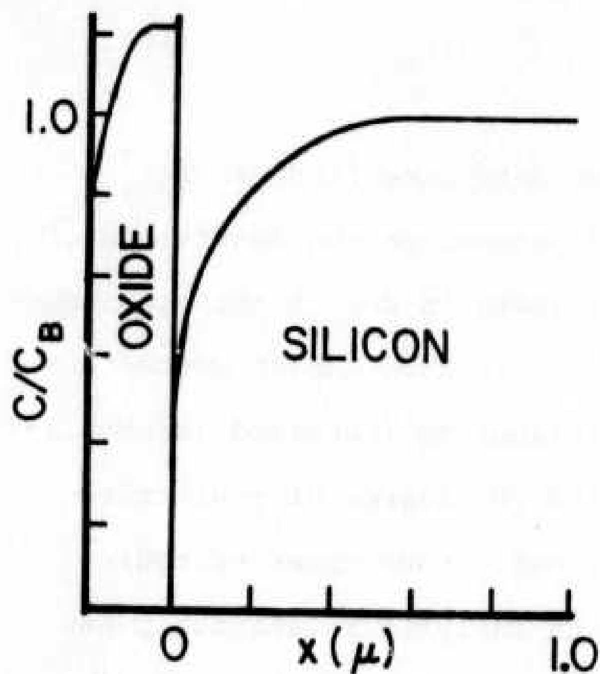
Fig. 2. Schematic illustration of proposed mechanism, plus the general relationship, for the thermal oxidation of silicon (3). The three stages of oxidation are indicated by (a), (b), and (c). In the general relationship, A, B, and τ are constants and x_o is the oxide thickness after time t.

Two important variables which determine final device electrical characteristics are dependent on the conditions of thermal oxidation. The first of these is dopant impurity concentration at the silicon surface. Surface dopant concentration (C_s) may be decreased (depletion) or increased (accumulation) depending on the dopant, and the degree of redistribution depends on oxidation conditions. Four cases of redistribution are shown in Fig. 3 . An analytic relationship has been developed (2) which allows a prediction to be made for final surface concentration after a single oxidation step. The prediction of surface concentration after a number of oxidation and diffusion treatments is much more complicated, but a solution to this problem would be highly desirable.

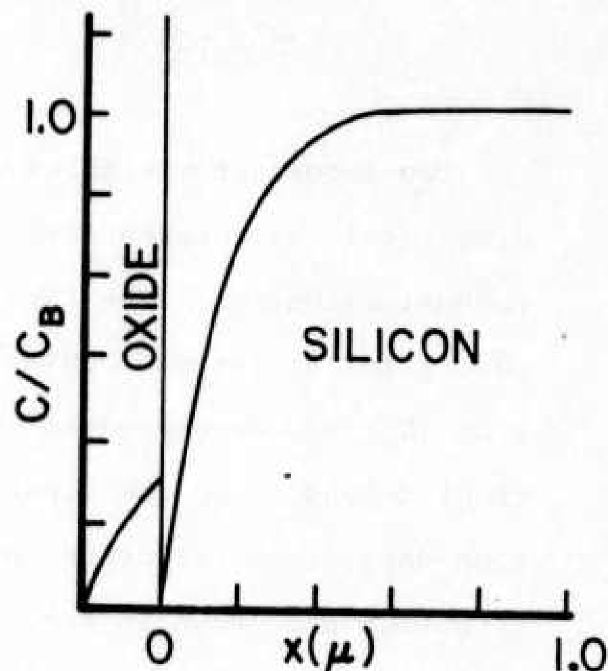
The second variable associated with thermal oxides directly affecting final device characteristics involves electrical charges in the oxide structure. It has been established that there are four types of charges associated with the thermally oxidized silicon system, and that these are the result of the oxidation process and subsequent processing conditions. These four types of charges are represented in Fig. 4 .

A number of integrated circuit device parameters, both bipolar and MOS, can be affected by the presence of one or more of these charges, or by changes in charge density during operating life. Some of these parameters are: junction leakage,

OXIDE TAKES UP IMPURITY (m<1)

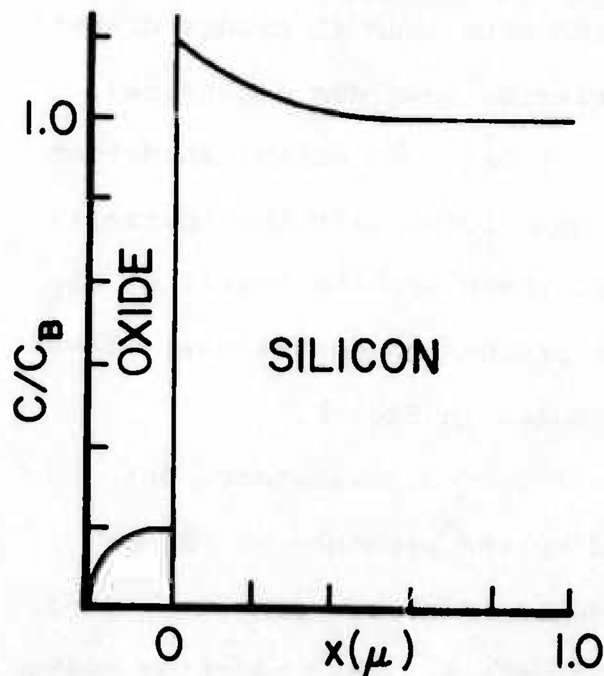


(a) Diffusion in oxide *slow* (boron)

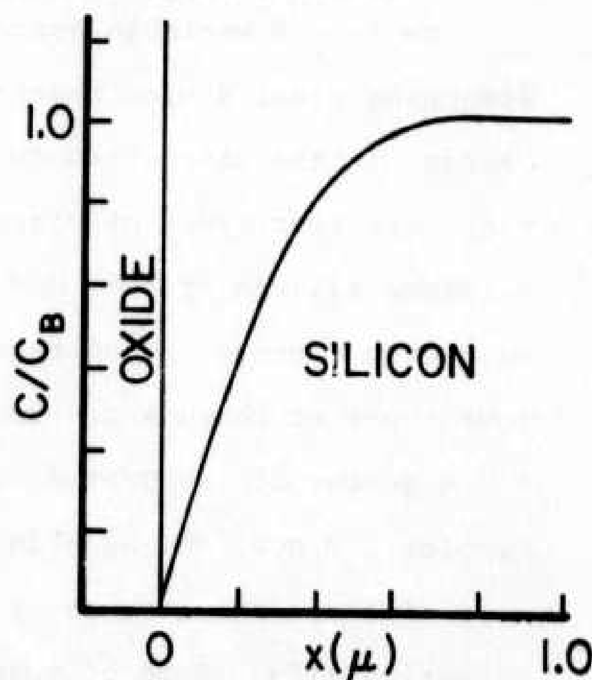


(b) Diffusion in oxide *fast* (boron with H_2 ombient)

OXIDE REJECTS IMPURITY (m>1)



(c) Diffusion in oxide *slow* (phosphorus)



(d) Diffusion in oxide *fast* (gollium)

Fig. 3 Four different cases of impurity redistribution in silicon due to thermal oxidation.

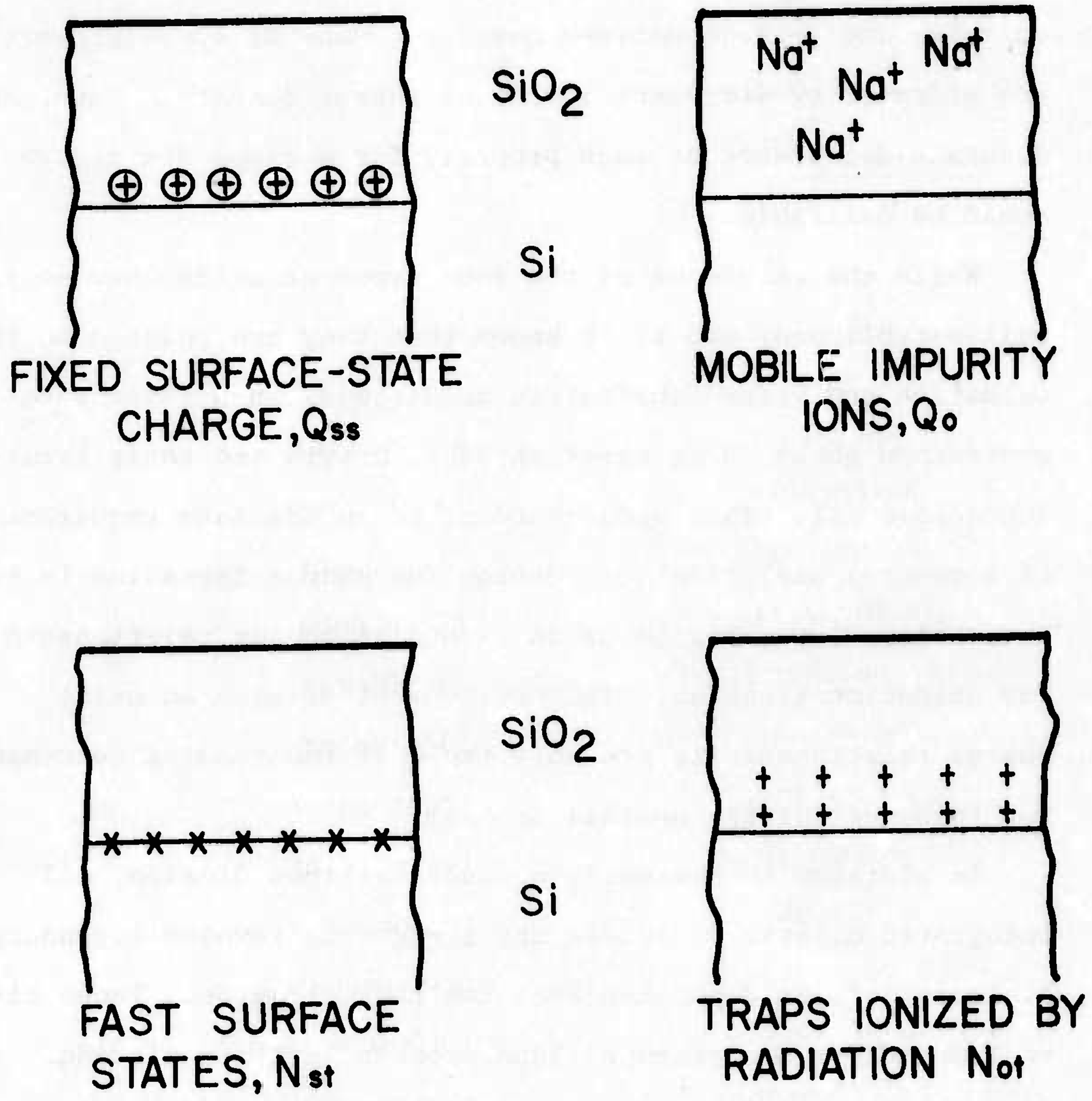


Fig. 4 . The four types of charges associated with the thermally oxidized silicon structure.

junction breakdown, noise, low current beta, MOS threshold voltage, and leakage between devices. Many of these properties are affected by different levels of charge density. Thus, an accurate dependence of each property for a given device type would be desirable.

While the existence of the four types of oxide charges is well established, and it is known that they are related to the oxidation and wafer fabrication conditions, much remains to be understood about their exact physical origin and their interdependence (3). This understanding is an absolute requirement if a general analytical expression for charge formation is to be developed, similar to or an extension to the relationship for oxidation kinetics. The development of such an oxide charge relationship is probably the most important requirement for this part of the overall program.

In addition to thermally produced silicon dioxide, all integrated circuit processes and structures involve secondary dielectric films deposited over the thermal oxide. These films included vapor deposited silicon dioxide, silicon nitride, phosphosilicate glass and others. They are used for impurity gettering, increasing voltage breakdown, masking against dopant diffusion or oxidation, and for many other requirements. The inclusion of these deposited dielectric films in IC structures can lead to additional device electrical instabilities.

Four types of instabilities are shown in Fig. 5. It is anticipated that analytical expressions used to predict the degree of these instabilities in combination dielectric films will be required later in this program, if complete modeling of IC fabrication is to be achieved.

An often neglected aspect of integrated circuit passivation and predictions thereof is that of reliability. Many engineers assume that once a charge is reproducibly controlled and its density is minimized, no additional difficulties will arise. This is not true. We are aware of a number of mechanisms whereby the various charges may be affected by subsequent device operation or testing, thus leading to device failure.[14] Thus, we will be including in the analytical relationships developed during this program the factors concerned with possible reliability implications.

One final note should be made of a recent development which is changing what has been for several years a reproducible aspect of thermal oxidation and thermal oxides. This is the incorporation of a chlorine species in the oxide for improved oxide characteristics. More will be said later about this subject, but it should be noted that both the general relationship for thermal oxidation kinetics, as well as oxide structure and charge formation, may be significantly altered. Thus,

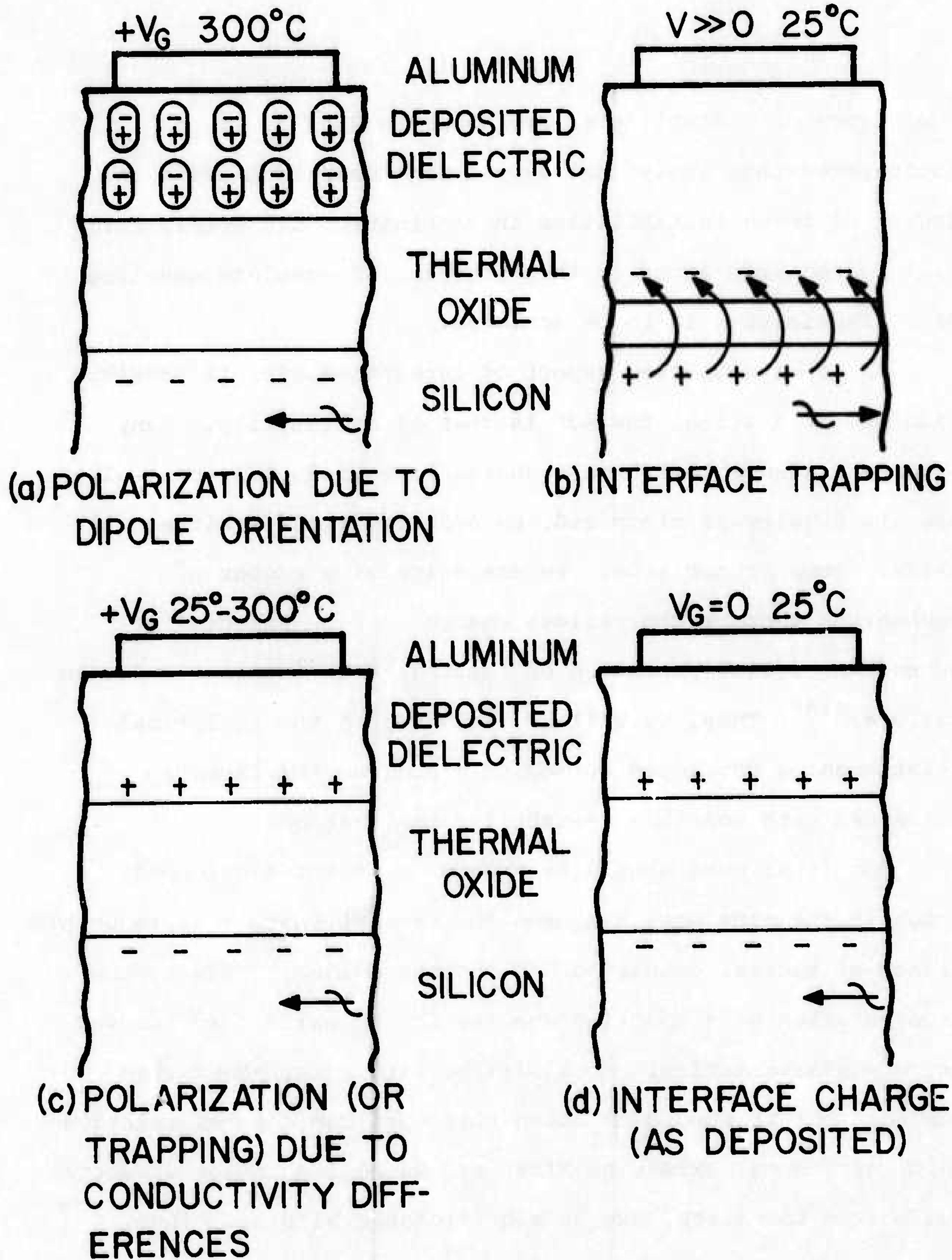


Fig. 5. Four different types of instabilities or charges associated with MIOS structures.

this special case of oxide gettering using chlorine ions must be considered in the development of a modeling program for integrated circuit fabrication.

Following is an outline of proposed projects which will allow us to achieve the overall objectives. These include both general topics over a five-year period as well as detailed projects to be accomplished the first year. We strongly believe that these types of programs will not be done by industry or other organizations - especially in the light of recent trends observed in industrial organizations.

§4.1.2 General Discussion of Projects for Three to Five Year Proposal.

The purpose of this section is to describe, in somewhat general terms, the projects that will be undertaken during the course of a three to five year program. The section following this one will deal specifically with the projects to be undertaken in the first year and will state in detail the goals of these projects.

It should be clear from the background information already covered in this proposal that oxidation kinetics and oxide charges are extremely important, in terms of the over-all project goal of reducing the cost of custom LSI to the DoD. This is true because knowledge at the present time is incomplete in both these areas; because oxides in their charges have important and demonstrable short and long term effects on both bipolar and MOS devices; and because the present state of knowledge about oxides in many cases requires expensive experimental procedures to optimize the fabrication

of a new device or integrated circuit. Better understanding and the ability to analytically predict oxide charge densities in particular would, it is believed, greatly reduce the time and cost of fabricating custom LSI for the DoD.

Toward this end, there are at least eight areas which merit investigation under this proposal.

1. Analytical prediction of oxide thickness, including effects such as doping in underlying diffused regions.

2. Analytical prediction and physical understanding of thermal oxide charge densities as a function of device processing.

3. Analytical prediction and physical understanding of charges associated with double layer dielectrics such as are commonly used in integrated circuits today.

4. Analytical prediction and physical understanding of oxide charges and oxide damage which result from ion implantation.

5. Analytical prediction and physical understanding of the effects of phosphorus and chlorine gettering on oxide charges.

6. Analytical prediction and physical understanding of the effects of oxide charges on long term device reliability.

7. Analytical prediction of the effects of thermal oxidation on the surface concentration of underlying diffused regions.

8. Analytical prediction and more complete physical understanding of the effects of oxide charges on the parameters of underlying devices.

§4.1.3 Specific First Year Projects and Goals

There are four specific areas which seem appropriate for investigation in the first year of this proposal.

A. The development of a computer program to accurately predict oxide thickness resulting from an arbitrary sequence of wet or dry oxidation steps, or from annealing treatments.

B. The development of an analytical expression for Q_{SS} - one of the most important oxide charges - as a function of processing.

C. An experimental and theoretical study of the effects of chlorine gettering on the kinetics of thermal oxidation and the various oxide charges.

D. The start of a comprehensive study involving experimental and theoretical work, whose goal would be to classify and understand all of the significant effects that oxide charges and CVD insulator charges have on underlying devices.

The following discussion of each of these areas will classify the goals of each specific project.

Computer Prediction of Oxide Thickness

In the Dec. 1965 Journal of Applied Physics, Deal and Grove published the following equation which predicts oxide thickness as a function of growth parameters:

$$x_o^2 + Ax_o = B(t+\tau) .$$

Solving this equation for the oxide thickness x_o, we obtain

$$x_o = \frac{A}{2}\left[1 + \frac{t+\tau}{A^2/4B}\right]^{1/2} - 1 .$$

The parameters A and B are given analytically and experimentally in the paper and are related to processing parameters; that is gas concentrations, diffusion coefficients and rate constants. Tau(τ) corresponds to a shift in the time axis, and reflects the fact that for dry O_2 oxides, an initial 230Å layer grows extremely rapidly. Tau (τ) can also be used as the initial oxide thickness when several sequential oxidations are used to arrive at a final oxide thickness. For example, at 1000°C and with a dry O_2 ambient, $A = 0.165\mu$, $B = 0.0117\mu^2/hr$ and $\tau = 0.37hr$.

This equation allows one to predict, for lightly or moderately doped substrates, the oxide thickness which results from a single oxidation step or from several sequential oxidation steps. It does not explicitly account for the enhanced oxide growth rate which is commonly observed over heavily phosphorus doped regions at temperatures below 1000°C.

One of the goals of this program is to allow computer prediction of device parameters which could result from a proposed processing schedule. One of the basic outputs of such a program would certainly be oxide thickness. We propose in the first year of this program to implement the oxide thickness equation on a computer, and further to include in it the effects of enhanced oxide growth over N^+ regions at low temperatures. These effects are important, for example, over the emitter region of bipolar devices. It is expected that considerable experimental work will be required to do this, to obtain more complete data on the constants A, B and

τ, and to include the effects of N^+ regions. The latter can be done by making some of these constants function of doping density.

Analytic Expression for Q_{ss}

Q_{ss}, or the fixed charge density at the interface of a silicon wafer and a thermally grown oxide, is clearly one of the most important parameters of an oxide. This is particularly true with respect to the effects of the oxide on underlying devices. No relationship equivalent to the oxide thickness expression just described currently exists for Q_{ss}. We propose in the first year of this project to attempt to devise such an expression. Conceivably, it could be an extension of the thermal oxidation relationship. We also propose to attempt in succeeding years to generate similar expressions for the other important oxide charges. A three to five year program could, therefore, hope to result in computer prediction of many of the important oxide properties - thickness and charge densities - which result from the various processing steps used to fabricate an integrated circuit.

A large body of experimental measurements of Q_{ss} exists in the literature. A good example of this is a paper by Deal et al. in the March 1967 Journal of the Electrochemical Society. Results such as these have shown that Q_{ss} is physically related to the silicon oxide structure in the Si-SiO_2 region, and that its density is a function of many processing parameters. Some of the more important are silicon crystal orientation, oxidation gas ambient, temperature and pull rate, and other high temperature annealing treatments.

We propose to take this experimental evidence, add to it where necessary, and then generate an analytical expression for the interface charge density resulting from a single oxidation step. Once this is done, an attempt will be made to generalize the expression to include the effects of several sequential oxidation and annealing steps. However, research has shown that in many cases, the final high temperature step in any given process is the most important in determining the magnitude of Q_{ss}.

Characterization of Chlorine Oxides

The addition of a chlorine species to thermal silicon dioxides for improved semiconductor passivation properties has been a significant development in the past couple of years. The chlorine is added to the oxidation ambient by bubbling oxygen through trichloroethylene, or by mixing gaseous hydrogen chloride with the oxygen or water vapor gas stream. It has been found that a few percent chlorine in the oxide will getter or complex mobile impurity ions, leading to improved threshold voltage stability and increased dielectric strength in MOS devices. Numerous other claims have been made, but are yet to be substantiated.

Enough improvements have been verified from the gettering standpoint that the effect of chlorine on thermal oxidation kinetics, and on subsequent charge properties, should be established. It is thus proposed that a project be carried out in which the effect of various concentrations of HCl in the oxidizing ambient (O_2 and H_2O) and oxidation temperature on

oxidation kinetics are determined. The constants in the general relationship would then be adjusted according to the effect due to chlorine. It is also anticipated that some analysis of the thermal oxide containing the chlorine species will be required, in order to establish the mechanism of chlorine incorporation.

The second part of this project will involve the determination of the effect of chlorine in the oxide on charge formation mechanisms. These results would then be used to modify the general relationship to be obtained for charge formation during integrated circuit fabrication.

Important tasks and milestones are listed below.

i. Determine effect of HCl conc. (2-15%) and oxidation time (0.25-16 hrs) on oxidation kinetics* and oxide chlorine content/distribution.

ii. Determine effect of HCl conc. (2-15%) on gettering/ion masking/breakdown properties of 1000Å oxide.

iii. Determine effect of oxidation temperature (800°-1200°C) on oxidation kinetics and chlorine content/distribution. Oxidation time and HCl conc. to be established.

iv. Determine effect of oxidation temperature on gettering/ion masking/breakdown properties of 1000Å oxide. HCl conc. to be established.

v. Determine effect of HCl concentration on Q_{ss}, N_{st} and (N_{ot}). Oxidation temperatures and oxide thickness to be established.

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*It is planned to investigate primarily dry O_2 oxidation.

Oxide Charge Effects on Device Performance

A large number of device effects have been ascribed to various oxide charges over the last decade. Some of these are reasonably well understood; others are not. Very few, if any of them, however, have been characterized to the point where analytical expression can be used to predict numerically the effects that a given oxide charge density will have on a particular device structure.

Some of these device effects are listed below.

a) Surface inversion characteristics for MOS type devices under both strong and weak inversion.

b) Stability of MOS and bipolar devices.

c) Junction breakdown and leakage characteristics in bipolar and MOS devices.

d) Bipolar transistor current gain over a wide range of collector currents.

e) Noise characteristics of bipolar and MOS devices.

f) Surface mobility of carriers in MOS and bipolar devices.

g) Channeling effects and surface inversion in bipolar devices.

h) Medium frequency transfer efficiency in charge coupled devices.

One of the principal outputs of this program should be a comprehensive description of these and other device effects. It should be emphasized that a quantitative, not only qualitative description of these effects is desired.

We propose to begin work on this task in the first year of the program. The first step is a complete compiling of previous work in this area. Such a compilation (involving a literature search among other things), has not been done and should serve to bring a wide collection of work into a comprehensive picture. Starting from this point, specific projects will then begin to fill the gaps in this overall picture of device effects.

One promising project in this area for the first year is to take specific examples of several types of circuits (i.e., static and dynamic MOS; linear and digital bipolar), and begin to look at device effects which are caused by oxide charge effects which can significantly affect device or circuit operation.

This project is not expected to be completed in the first year. Part of the information needed to quantify device effects will come from other parts of this insulator study. The importance of being able to predict device effects cannot be overemphasized, however, and therefore this part of the proposal must be started in the first year.

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§4.2 Ion Implantation

In a period of less than ten years, ion implantation has made its way from the physics research laboratory to the semiconductor production floor. This rapid development has been spurred by the fact that ion implantation provides a degree of process control that is difficult (or impossible) to achieve with conventional thermal processing of semiconductors. For example, the process has been proven to provide (1) a more flexible choice of doping sequence (e.g., base after emitter if desired; or tailoring of a junction C-V characteristic after preparation of the basic junction); (2) the possibility of highly accurate low dose implants (for high value resistors, threshold voltage control, and JFET channels); (3) the possibility of through-mask implants (for threshold control and buried channel CCDs); and (4) device uniformity from wafer to wafer and across a given wafer, which is difficult to obtain by thermal processing.

Because of its advantages in doping profile control and uniformity, ion implantation would appear to be especially suitable for obtaining (at relatively low cost) the wide variety of doping profiles that will be required in the fabrication of custom integrated circuits. Using this process, a minimum of experimentation will be required to achieve nearly any impurity profile required by a circuit designer; and, in principle at least, the process control is sufficient to permit computer-aided circuit design to proceed with a minimum of constraints imposed by process variables. At the same time,

however, it is premature to assume that a completely theoretical approach leading from models of ion implantation processing at one end, to finished circuits at the other, is possible. There are several reasons for this situation, of which some of the most important are as follows:

(1) The theory of the process has not yet been far enough developed to answer all of the questions that a circuit designer might ask (for example, ion range and damage distributions cannot be satisfactorily calculated for multiple layer targets, such as an Si_3N_4-SiO_2-Si sandwich);

(2) Complicated diffusion phenomena occur during the annealing of implanted layers, with the result that actual impurity profiles may bear no simple relation to the original implanted profile;

(3) The effects of indirect implantation of ions produced in the mask by an energetic primary ion passing through the mask are unknown, both with regard to their effect on the mask, and in their effect on the underlying semiconductor.

Answers to most of the important outstanding questions can surely be obtained, and will form the data base from which computer-aided design can reasonably proceed. These answers will require improvements in the theory of the implantation process, and careful experimentation will be required to verify the theoretical development. Once verified, the newly developed theory can provide the necessary framework for computer-aided IC design.

In what follows, we propose to do research on three main topics that we believe are central to the general problem of

applying ion implantation to the fabrication of custom integrated circuits, and at the same time be in research areas where we have already developed special competence and can therefore proceed with greatest efficiency. These three areas are:

(1) An extension of basic range and damage theory to permit accurate computation of impurity and damage profiles in Si, with and without SiO_2 and Si_3N_4 masks (work to be supported in a substantial part by IBM);

(2) a study of the effect of implantation damage on shallow diffusions, and

(3) a study of high dose through-mask implants, including both how the mask itself is affected, and to what extent secondary ions implanted from the mask into the semiconductor produce constraints on subsequent processing steps.

We will elaborate briefly on these projects.

§4.2.1 <u>Extensions of Range and Damage Theory</u>

The most complete computations of range and damage distributions presently available for ions of interest in Si technology are those recently completed by Mylroie at Stanford [1]. These computations show that higher order moments must be used in the construction of implanted impurity profiles, if one insists on an accurate agreement between theory and experiment. In particular, the use of a Gaussian distribution for the implanted ions can predict junction depths that are in error by as much as 100% in cases of practical importance. The addition of the third central moment reduces this error to

essentially zero, IF the concentration region of interest lies no more than 2 orders of magnitude below the peak of the impurity profile. However, if one wishes to obtain a fit between theory and experiment that is capable of accurately predicting impurity profiles over 5 orders of magnitude, then calculation of the fourth central moment is also required. Such predictions are not merely matters of academic interest, since the performance of fine geometry devices (e.g., microwave transistors) is very sensitive to exact junction placement and total base doping charge.

The theory recently developed by Mylroie and Gibbons [1] can be readily extended to permit such a computation. In addition, it is also possible to extend the theory to permit the computation of reasonably accurate range and damage distributions for ions that have been implanted through SiO_2 and/or Si_3N_4 masks of any thickness. No significant work has been done in this direction at the present time.

Substantial interest in performing such calculations has been expressed by IBM, including the provision of free computer time and programming skill. We therefore propose to allocate three days per month to the organization and direction of a joint venture between Stanford and IBM, with the purpose of computing the quantities that are necessary to construct highly accurate impurity profiles in Si, both with and without SiO_2 and Si_3N_4 masks. The ARPA contribution will consist of the salary of a co-principal investigator (J. F. Gibbons) for the portion of his time spent on this project, plus travel expenses

for four trips to the East Coast. Trips by IBM personnel to the West Coast, salaries of associated IBM employees, and computer time will be provided to the project free of charge by IBM. The results will be published in the general (non-proprietary) literature.

§4.2.2 Effects of Implantation Damage on Impurity Profiles in Annealed Si

A major unsolved problem in the field of ion implantation is concerned with the general question of how the annealing of implantation damage in a crystal affects the diffusion of the implanted species [2]. Briefly, the problem here is that implanted impurity ions create damage in the semiconductor lattice as they come to rest. Annealing of this damage produces a rich source of vacancies and Si interstitial ions, both of which may produce more diffusion (by orders of magnitude) of the implanted impurities during the annealing cycle than one would estimate from a simple calculation, based on the impurity diffusion coefficient at the annealing temperature.

It is clearly essential to characterize this diffusive redistribution accurately before device design can proceed on other than an empirical basis. The necessary characterization can be obtained most expediently by simply performing implantations under a reasonably general set of conditions, and by measuring the impurity profiles that result after various annealing cycles. These impurity profiles would then constitute a data base from which IC designs could proceed.

In the longer term, it is to be expected that research work on the problem of diffusive redistribution would lead to models of the process from which computations of actual impurity profiles could be made. These process models would then replace the experimentally-obtained profiles as the basis for computer-aided IC design. Work done at Stanford on proton-enhanced diffusion [3] provides a starting point for the development of such process models, though present theory requires important modification to include the saturation effects that occur when vacancies and interstitials are produced in the quantities typical of implantation-produced damage.

We propose to allocate 10 percent of the time of one of the co-principal investigators (JFG) to this problem. He will be assisted in this research by two Ph.D. candidates.

§4.2.3 Defects Arising as a Result of Through-Mask Implants

In the formation of bipolar transistor emitters, it is customary to implant as much as 10^{16} As/cm^3 in an impurity pre-deposition step, and then follow this with a thermal diffusion drive-in. This process is highly successful as long as the depth of the diffused junction is great enough; but for shallow junctions, the process does not produce good junction characteristics.

It has been generally assumed that the reason for this is that the damage produced by the As implantation does not fully anneal, and that junctions lying too close to this damage are affected by it. This general explanation is probably true,

though the damage that is actually responsible for poor junction characteristics may actually come from the mask, rather than as a direct result of the As implant. For example, at the edges of an oxide cut defining an emitter window, the oxide will be bevelled, so that in some areas As can just barely penetrate the mask. In these regions, there will be many 0^+ ions produced as recoils during the As implant. These recoiling 0 atoms can be implanted into the silicon in a sort of indirect ion implantation process. Evidence for this has recently been published by Sigmon et al. [4]. However, evidence has been published by Reddi et al. [5] which may contradict Sigmon's findings.

If oxygen knock-ons are implanted to any significant distance at the edges of the emitter window, junction characteristics would indeed be very poor, unless the dopant were diffused beyond the range of the 0 implants. It would be essential to verify the existence of this process, and to determine as precisely as possible the minimum additional diffusion necessary to produce good junctions. This would need to be done for several different masks (at least SiO_2, Si_3N_4 and photoresist), each of which would present special problems and possibilities of its own. For example, implantation through Si_3N_4 would produce nitrogen knock-ons, and hence (possibly) n-type doping of the underlying silicon. This could be either beneficial or detrimental, depending on the structure being fabricated. However that may be, a careful analysis and characterization of the effects

of the mask on junction characteristics and ultimate device geometry would be of great interest and application.

We propose to initiate studies of these problems in two directions. On the experimental side, we wish to obtain information on the extent of diffusion which is necessary to produce good junction characteristics, following a high-dose, through-mask implant. Related theoretical work will be done to calculate the range distribution of knock-on ions that are implanted into the semiconductor, and the damage distribution produced by them. This information should be useful for making theoretical calculations of the minimum diffusion that is required to produce satisfactory junction characteristics in the presence of unwanted doping by the knock-on ions.

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§4.3 Epitaxy

The use for high performance, conventional, and I^2L bipolar technologies in new defense systems is clear. Both improved packing density and enhanced performance capabilities will allow increased numbers of functions to be integrated onto single IC chips. The resulting reduction in IC package count is a dominant contributor to increased system reliability and reduced system size.

Thin epitaxial silicon layers are an essential component of high-performance bipolar integrated circuits. Several trends in process technology illustrate this point clearly. First, the trend toward smaller minimum surface geometries requires a similar scaling in vertical geometries. This effort to reduce device geometries, and hence capacitance, is the key to increased speed, as well as higher packing density. Second, new isolation technologies are often limited in penetration capabilities; two examples of this limitation are the Isoplanar and V-groove technologies. In addition, to minimize area consumption due to isolation dimensions, it is advantageous to use thin epitaxy. Finally, the Integrated Injection Logic (I^2L) technology uses epitaxial properties to determine performance of active devices. Thin layers are needed to assure the desired minority carrier transport efficiencies. However, a major technological problem occurs with thin epitaxial layers, due to dopant control during epitaxial growth.

The problem of dopant control in epitaxial layers occurs both in conventional bipolar and I^2L technologies. For conventional bipolar processes, layers are grown over diffused buried collectors. The auto-doping and out-diffusion problems during epitaxial growth are critical in thin layers. For standard bipolar devices, the buried layer profile affects breakdown voltage, parasitic capacitance and saturation collector resistance. For lateral pnp and I^2L devices, the buried layer or epitaxial profile is a key factor controlling emitter efficiency and current gain. New I^2L structures also use alternately doped epitaxial layers to improve efficiency and packing density [1].

Industrial solutions to dopant control in epitaxial layers are empirical rather than analytical. Production lines establish empirical controls for desired parameters. However, they lack the analytical capabilities necessary for designing a new process to desired specifications. Epitaxial process development is most often a "shot-gun" approach. The severity of the epitaxial technology transfer problem is increased as newer and more dense technologies are evolved. Yet, these advanced technologies are needed to solve the IC design problems for new generations of defense systems. Modeling of dopant control in epitaxial layers is needed. Only through such modeling will it be possible to prototype and transfer custom IC designs using new technologies.

Problem Definition

Two aspects of dopant control in thin epitaxial layers can be identified as being crucial for evolving analytical models. First, kinetics of dopant inclusion in the epitaxial layer must be modeled. Initially, uniformly doped layers, and later on nonuniformly doped multilayer structures must be studied, and in the end continuous growth or arbitrarily doped layers must be studied. Second, epitaxial growth over buried layers must be studied. Problems of outdiffusion and autodoping, initially one dimensional and later on two dimensional, must be modeled. The effect of substrate dopant, crystal properties, etc. must be studied. Both problems require understanding and evaluation of epitaxial reactor dynamics. During this program, methods for profile determinations and other measurements must be established. Finally, algorithms and computer models must be evolved to insure rapid transfer and efficient utilization of the epitaxial layer modeling results.

Research Approach

The whole area will be divided into three subgroups, (I) profile determination techniques, (II) kinetics of dopant inclusion, and (III) effects of existing layer dopants. A large portion of the work in these areas will be interrelated.

§4.3.1 Profile Determination Techniques

Several profile determination techniques will be investigated. Nondestructive techniques are advantageous for both speed and simplicity. Capacitance voltage techniques will be studied. A test pattern and computer programs are available from the National Bureau of Standards which use a diffused p-n junction

diode, with gated guard-rings [2]. The utility of these structures, and methods for isolating side-wall capacitance contributions will be considered. Independent determination of junction depth and lateral diffusion will increase the accuracy of this technique. Junction depth can be independently determined by groove-and-stain. Lateral diffusion parameters can be determined using scaled channel-length MOS devices, as well as the gated-diode structures. A second C-V technique to be studied is the use of deep-depletion MOS structures for profile determination. This technique is of value both for thin epitaxial layers and ion-implanted layers [3,4]. These non-destructive profile determination methods will be evaluated, and computer-aided techniques for their utilization will be developed.

Destructive profile determination techniques will be studied. These methods vary in difficulty and accuracy. The function of these methods in this work will be to bench-mark the non-destructive methods, and to choose the most reliable techniques for use in subsequent epitaxial layer studies. Two attractive techniques to be evaluated for in-house use are spreading resistance and anodic sectioning. Potential use of neutron activation analysis will be considered. The neutron technique offers good sensitivity for phosphorus layers. This technique will be a valuable calibration tool. Apart from profiling, neutron activation analysis will also be used for comparison of electrically active vs. total dopant inclusion. However, the remote location of such analysis facilities and the delays in obtaining results are major hindrances in the use

of this method. Other potentially useful methods to be considered are ion microprobe and surface analysis (Auger and ESCA), and infrared reflectivity techniques. However, reports to date indicate inadequate sensitivity of these methods for this work.

Apart from profiling, other evaluation techniques will be required in the work to determine the crystal quality. This will include X-ray topography for dislocation density, backscattering, selective etches, etc.

§ 4.3.2 Kinetics of Dopant Inclusion

Under this part of the project, various aspects of dopant inclusion will be studied. First, a study of growth of uniformly doped thin layers will be done. Along with the conventional dopants (B, As and P) special emphasis will be placed on antimony. This will consist of the study of segregation coefficient, gas flow sensitivity, and temperature sensitivity. Limits of high-doping will be investigated to determine departure from linearity, dopant inclusion vs. electrically active dopant, solid solubility limit, and effect on epi quality.

Kinetics of the doped layer formation will be studied exhaustively. The role of surface diffusion of silicon on growth, the mechanism of dopant incorporation at gas/solid interface, and the role of dopant in changing the growth will be investigated. This will yield highly useful information for subsequent work.

The limits and control of the dopant-concentration changes in multilayer epitaxial structures will be studied in

the next phase of the project. Such structures are esential for high performance devices. However, little consideration has been given to changes in epitaxial doping during a continuous deposition. Previous studies have considered the chemical reactions occurring during the epitaxial deposition, in an attempt to find the source of the atoms which lead to autodoping. In this phase of the project, a different approach will be taken. The entire epitaxial deposition process will be treated as a system and the dynamics of this system will be described. Development of computer-aided design tools is crucial in this phase of the project, owing to the multivariable nature of the problem. However, analytical approximations will be developed for limiting cases. Relationships will be developed to be as nearly system independent as possible. Methods for system-model parameter extraction will be evaluated.

In the initial work, the various processes, such as the dynamics of gas flow in the reactor plumbing and in the deposition chamber, the growth kinetics of the epitaxial layer, and the diffusion occurring during the deposition, will be treated together. The system will be characterized and modeled by a transfer function relating the dopant input gas flow to the impurity profile in the wafer, after the epitaxial deposition. If the system can be characterized in such a manner, the calculation of the optimum dopant flow as a function of time will allow fabrication of a nearly optimized series of epitaxial layers, or a graded layer. System time response related to

residual dopant atoms will be of special interest in a transition from a heavily doped to a lightly doped layer. The nature of this response will indicate the optimal sequence of operations for the fabrication of multilayer or graded epitaxial films.

After characterization of the entire system, the several components entering into the total system will be modeled separately. These components of the overall system include the plumbing of the reactor, the gas flow within the epitaxial deposition chamber, the diffusion of the depositing species to the wafer surface and their reaction there, and subsequent diffusion within the solid wafer during the remainder of the epitaxial depositon process. Resolution of the overall system characteristics into the various components should allow an understanding of the critical processes occurring in the epitaxial deposition cycle, so that the majority of the further effort can be focused on the limiting processes.

Polycrystalline silicon has become very important with the advent of silicon gate technology. However, very little work has been done to understand the dopant inclusion in polysilicon during the growth, and its effect on the film properties. A detailed study will be done to generate a complete model.

§4.3.3 Effects of Existing Layer Dopants (e.g., Buried Layer)

The objective here will be to study the effect of the dopants in the substrate on the growth and properties of the epitaxial layer. Initially, the work will be directed to large area buried layers. The primary objective will be to grow a

uniformly doped thin epitaxial layer over a highly doped buried layer. Arsenic doped n+-wells in p-type substrates will be used. Both implanted and diffused arsenic layers will be used. Good lattice match, low sheet resistance and low diffusion coefficient make arsenic buried-layers attractive for IC structures. However, anomalous diffusion and effects of high vapor pressure for As must now be included in computer models for epitaxial growth over these buried layers. Later on Sb will also be investigated as an alternative to As. Thin n-type layers (~ 1μ to 5μ thick) will be grown epitaxially. The doping profile will be studied as a function of buried layer and epitaxial deposition parameters. In this work, primary emphasis will be on understanding the buried layer diffusion dynamics and autodoping, from front and backside, during epitaxy in a controlled environment. Computer models for these processes will be developed. In addition, techniques for impurity profile determination discussed earlier will be evaluated.

Dependent upon the substrate and buried layer parameters, the quality of the epi-layer can change. A detailed study of film induction and defects in epitaxial layers dependent upon the substrate and buried layer parameters will be done. Dependence of the quality of epi layer on the type of element used for buried layer, surface concentration, and surface depletion prior to film growth will be investigated. The effect of the method of introduction of the buried layer dopant (i.e., implanted or diffused from gas or diffused from doped oxide) on the quality of epi will be investigated.

The effect of substrate crystal properties on the film growth will be investigated in the latter stage of the program. Crystal orientation effect on pattern shift will be studied. The effect of the defects in crystal structure on film quality will be studied.

Finally, two dimensional buried layer outdiffusion and autodoping effects and geometry limitations will be studied. As the size of the buried layer is made smaller, the two dimensional effects become more important.

During the present study, conventional processing techniques and equipment are to be used. New epitaxial layer technologies will not be considered. It is essential that the research approach be system independent so that techniques and computer tools can easily be transferred. Computer models and measurement techniques are required in both phases of this work. These models and techniques are indispensable tools for the transfer of epitaxial-layer deposition technologies. The evolution of high performance technologies makes the prototype-to-production transfer problems central to the viability of new defense systems.

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CHAPTER V

Proposed Program of Research

Software Systems

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CHAPTER V

Proposed Program of Research
Software Systems

§5.0 Introduction

For many years industry and government have been supporting research and development of software systems for IC design. Today, the yearly industry-wide expenditure for software development in this area is believed to far exceed the overall total cost of this proposed ARPA program. For this reason, it appears the present ARPA program could contribute little to this effort, except in problem areas not presently being addressed. Therein lies the basis for this proposed program of research on software systems. During the Workshop on IC Analysis and Design it became evident that despite an extensive research and development effort in this area, important problems remain to be solved; problems that contribute to the high cost of IC design and development.

The problem areas considered here have been suggested to arise from a communications gap between scientists engaged in various areas of IC design, development, and manufacturing. As a consequence, software systems for the electrical analysis of IC structures were not designed with a view toward aiding in the solution of many important problems in other areas of the semiconductor business. Furthermore, it has been suggested

that these problems are being ignored by scientists engaged in the electrical analysis of integrated circuits, and that this situation will continue without a concentrated effort to solve these problems.

For example, there are numerous problems of computational convergence and stability associated with the analysis of IC structures. Circuit designers attribute these problems to the lumped network approximation for transistors (equivalent circuits) used for circuit design. It has been stated that a given transistor equivalent circuit could converge adequately for the analysis of one type circuit configuration, yet for another circuit configuration it could produce an unstable situation. Further, it has been stated that a given transistor equivalent circuit, in combination with a given integrated circuit configuration, will sometimes exhibit computational stability using one circuit analysis program, and exhibit instability using another circuit analysis program.

Attaining stability and rapid convergence in any particular design situation is presently accomplished on a heuristic basis. Through experience, circuit designers learn methods to restructure their transistor equivalent circuits, as a means to attain fast computational speeds. Therefore, "rules-of-thumb" have been developed for the equivalent circuit configurations yielding stability and adequate computational convergence,

yet little understanding is available concerning the basic source of this difficulty.

To date, an industry-wide search has not revealed even one research effort directed toward the solution of this problem. Circuit designers are familiar with the problem, yet they accept it as a necessary evil, and with resignation that empericism is the only available solution. This particular problem has been identified as a particular source of difficulty toward realizing the overall goals of this program.

Another important problem area is associated with the inadvertant process variations arising in each and every step of IC fabrication. Techniques have been developed whereby we can establish the consequence of these process variations upon many electrical properties of transistors. Presently, there is no similar technique available whereby we can calculate the consequence of these process variations upon the electrical performance of an IC. Furthermore, there is only a small nationwide effort toward the solution of this problem.

Instead, scientists developing these circuit analysis methods are directing their attention toward the field of design optimization (see Appendix IV). Briefly, design optimization is a technique presently believed to offer a possibility for completely automating the design of an IC. Ultimately, it is believed a set of design specifications can be introduced

into a computer program, in conjunction with a set of weighting functions, and a mathematical solution will be automatically obtained for the particular problem at hand. This technique for design has been successfully applied to circuits less complex than an IC structure, and an extension of this method to IC design is now underway.

It is emphasized that available examples of design optimization have been directed toward the solution of problems offering only a minimum of interest to many semiconductor manufacturers. Namely, these examples use design optimization as a means to improve the electrical characteristics of an IC: increased switching speeds, etc.

Representatives from both the semiconductor industry and from the DoD system suppliers have stated a need that appears more important than improving the electrical performance of an IC. It is believed an ability to calculate the influence of fabrication processes variabilities upon an IC represents an important cost-saving advance in the state-of-the-art. Further, it was stated that design optimization techniques should be used as a means to desensitize an IC to these process variabilities. Thereby, an IC structure could be designed for improved manufacturability, rather than an improved electrical performance.

Thus, we have the basis for this proposed program of research on software systems. It is proposed that an important goal for this program is the development of a computer system for the electrical design of an IC. The purpose of this development effort is to establish the forementioned IC design capabilities that are not presently available to the semiconductor industry. Included in this effort is the basic research needed to overcome obvious problems associated with attaining the goals of this program.

§5.1 Software for Electrical Design of Integrated Circuits

It is proposed that a software system be developed for the electrical design of an IC. Initially this electrical design would be accomplished at a cell level and, at a later time, at a chip level, using macro-modeling techniques. A principal purpose for this developmental effort is to establish computational tools for IC design that can fully utilize the results gained from other research and development efforts proposed for this ARPA program. Further, this circuit design program will overcome shortcomings in our present IC design techniques that have been identified as important sources of difficulty (and cost) in our present engineering procedures.

It is proposed that this computer program for circuit design offer a capability for calculating the steady-state and transient properties of an IC from fundamental fabrication

process parameters. Further, it is proposed that this program provide a capability to calculate the consequences of process parameter variations upon these electrical properties of an IC. These computational capabilities must be implemented in such a fashion that the use of this computer program is economically practical for IC design and development: it should not use an excessive amount of computer time.

Clearly, data management becomes an important aspect of this type analysis. For this reason, included in this computer program are methods for systematically introducing processing data from test-pattern measurements. Further, output data from calculated results must be presented in a form that is convenient and useful for IC design and development.

It is also proposed that this circuit design program provide a means whereby an IC design can be modified to improve its manufacturability. Specifically, through modifications of a proposed IC structure it can be made less sensitive to process variations established by test pattern measurements. It is suggested that design optimization techniques could provide this desensitizing capability, yet all options should remain open at the initiation of this project.

§5.2 Stability and Convergence

In the electrical analysis of an IC, serious problems of convergence and stability arise for which there is only limited basic understanding. Some circuit configurations produce a very slow convergence rate when analyzed using iterative computational procedures. Other circuit configurations produce a divergent situation, and yield calculated results that are of no practical value. It has been stated that this type problem is a characteristic of the computer program being used for IC analysis; a circuit that is stable in one circuit design program can be unstable in another.

Using experimental methods, circuit designers find that a modification of the equivalent circuits used to approximate a transistor has significant influence upon this type situation. During the analysis of a given circuit, computational stability is greatly influenced by the equivalent circuits used for the transistors; some equivalent circuits yield stable results whereas others are unstable. For this reason, an empirical adjustment (and modification) of these equivalent circuits has become "fair game" for the circuit designer. With little concern about the physics of transistor operation, circuit designers modify the transistor equivalent circuits to satisfy two basic requirements: first, the circuit analysis program converges using a minimum of computer time and, second, the equivalent circuit adequately approximates terminal properties of the associated transistor.

This approach to the equivalent circuit problem is in direct contradiction to the efforts of those workers developing transistor equivalent circuits founded upon device physics. If for reasons of stability (or convergence) the circuit designer will not use these equivalent circuits, the effort is wasted. Therein we have a fundamental difficulty that must be overcome.

The development of equivalent circuits based upon transistor physics represents an important part of this overall ARPA program of effort. Equivalent circuits of this type are needed to calculate the consequences of fabrication process variations upon the electrical properties of an IC. Nevertheless, another constraint must be placed upon their design and development: these equivalent circuits must operate in a satisfactory manner when used in available circuit design programs.

At this time there is little understanding about this equivalent circuit problem, from a circuit analysis point of view. For this reason, it is proposed that a program of research be directed toward an understanding of this problem. A goal for this research is to formulate a set of equivalent circuit constraints that will yield a minimum of computation time in the analysis of IC structures. Thereafter, a cooperative effort should be established between this program and the equivalent circuit effort previously outlined in §3.4 of this report. Through this cooperative effort, transistor equivalent

circuits should be developed that are based upon the physics of device operation and, also, assure efficient operation of available circuit analysis programs.

§5.3 Manufacturing Process Simulation

In the design and development of integrated electronic circuits, problems arising from fabrication process variabilities represent an important source of difficulty. Presently, these structures are designed to yield satisfactory operating characteristics assuming median values for the electrical parameters for each transistor, resistor, etc. After completing a design in this fashion, it is frequently found that an IC cannot be manufactured without design modifications. An electrical design based upon median parametric values offers no assurance that an IC will yield satisfactory characteristics when subjected to the large parametric variations encountered in any semiconductor manufacturing facility.

The semiconductor industry frequently applies empirical methods to alleviate this situation. Despite a poor yield of satisfactory IC chips, manufacturing is continued and the resulting IC structures evaluated on a daily basis. Thereby, insight is gained concerning the problem areas, and the IC design is modified to maximize the yield of satisfactory chips. Clearly, this technique represents an empirical desensitation of the design to inadvertent manufacturing process variations; a problem that could be solved using computational methods of analysis.

One leading IC manufacturer (IBM) has recognized this particular problem as one of great importance. For this reason, a substantial financial investment has been directed toward a modification of their circuit analysis program. This modification was intended to offer a manufacturing process simulation capability to the IC designer. Presently IBM rents this computer program (ASTAP) for semiconductor IC design, but there are few satisfied customers. Techniques used by IBM for manufacturing process simulation have been found impractical; they yield inadequate results, and they are too costly to apply.

These techniques represent a "carry-over" of manufacturing process simulation methods first developed by D. P. Kennedy for semiconductor device design, and discussed in (§3.1.2) of this report. In ASTAP, a psuedo-random number is used to independently, and simultaneously, modify parametric data used to approximate semiconductor components within the IC structure. Thereby, it is suggested that the consequence of process variations are simulated, using this computer program.

Representatives from the semiconductor industry have voiced strong opposing views about this method of process simulation. It has been stated that calculations using ASTAP do not agree with experiment. This inaccuracy is attributed to a lack of correlation between the many parameter variations encountered in an IC; in practice, there is substantial correlation between these parameter variations. As a consequence,

the ASTAP technique is viewed as a worst-case design yielding results that are excessively pessimistic. In fact, one industrial representative stated the results of his evaluation of ASTAP: it predicted a negligible yield for an existing high yield product.

Another industrial representative voiced a strong negative opinion about the cost of running the ASTAP program. It was stated that the overall computer costs associated with IC design could not be justified and, hence, ASTAP is not used.

Despite the problems associated with manufacturing process simulation of an IC, it represents a capability that must be developed for the inexpensive design of custom structures. Further evidence of this need was outlined by a NSA representative concerning the problem of multiple source IC procurement (see Appendix IV). It was stated that NSA samples a large cross-section of IC manufacturing facilities and, thereafter, intentionally undertakes a worst-case design. Although this technique solves their multiple source problems, a significant loss is realized in performance of resulting IC structures.

It is proposed that this program of research undertake the development of a manufacturing process simulation capability at both a circuit level and at a chip level. This program should not duplicate the IBM efforts in this area but, instead, recognize past mistakes and learn from this experience. Resulting

from this effort will be a practical simulation method and, in addition, a basic computational tool needed for future advances using the methods of design optimization (§5.4).

First, it is suggested that by introducing into this program parameter variabilities at a fabrication process level (as outlined in §3.1.2 and §3.2.2) accurate correlations will be realized between these variabilities. Implied here is a need to distinguish between process variations appearing across a slice of silicon from those seen on a slice to slice basis. Past experience shows this to be a negligible problem of computer bookkeeping. Thereby, circuit calculations will be based upon sets of parametric data that contain the correlation needed for an accurate simulation of a manufacturing process.

An important problem remains yet unsolved in the manufacturing process simulation of an IC. Namely, present circuit analysis techniques are too slow for the Monte Carlo methods now used in such a calculation. For this reason, two paths of research are proposed. First, the development of computational techniques for circuit analysis that offer a substantial increase in speed. Second, the development of statistical methods that do not require the vast number of calculations (hence, the computer speed) necessary for a Monte Carlo analysis. Both of these methods have been considered by workers in this field and both offer a possible solution.

After having developed this capability and proven its applicability to IC design, it is proposed this technique be extended to the chip level of circuit analysis. Using macro-modeling methods that are now under development, it is suggested that process simulation at a chip level could be realized for future design of IC structures.

§5.4 Design Optimization

Design Optimization represents a new field of IC design that is directed toward a systemization of a very complicated procedure. Presently, IC design is accomplished on a computer using essentially heuristic methods that involve a substantial amount of "trade-off" between the electrical characteristics attainable from a particular IC circuit. There is no well defined (or organized) method to undertake this task, and in any given design situation more often than not success is related to the skill and experience of the design engineer. Therein we have a fundamental problem, and design optimization is often proposed as a solution for this problem.

It is emphasized that the name 'design optimization' is misleading if taken in its literal sense. Workers have emphasized that this analytical technique cannot assure an optimum solution for any given design problem (see Appendix IV). In most situations the resulting solution is suggested to be local, rather than global; therefore, the results of a given calculation (or optimized design) is frequently dependent upon the

starting point. Nevertheless, this technique has proven valuable for the automatic computer design of electrical networks, and it offers a similar potential for the design of integrated electronic circuits.

This is not intended to imply that the techniques of design optimization could be immediately implemented into a computer program for IC design. There is much to be learned before reaching this stage of development. Presently, the technique involves a set of operating constraints upon a given IC design, in conjunction with a set of weighting functions; these functions offer in a quantitative fashion the ability to "tradeoff" between various design parameters, in a manner similar to present IC design methods. Through illustrative examples, it has been shown that the ultimate gains of this design method (over a heuristic hand design) is exceedingly dependent upon these parameter weighting functions.

As a consequence, an application of design optimization techniques presently requires the same level of skill as existing methods of IC design. Despite this present situation, totally automated design methods have been developed in other areas of electrical engineering, and there is evidence that a similar capability can be developed for semiconductor IC design. This possibility has particular appeal when applied to problems associated with the manufacturability of integrated circuits.

It has been stated by industrial representatives (see Appendix IV) that design optimization techniques could produce a substantial cost reduction in the design and development of new IC structures. This cost reduction would be realized if these techniques are used for IC desensitization to changes of manufacturing process parameters. Thereby, we would obtain new IC structures that have been designed to exhibit an increased degree of manufacturability; they would have an increased tolerance to process parameter changes.

For this reason, it is proposed that research in this area be undertaken with a goal toward designing into new IC structures an increased degree of manufacturability. Fundamentally, this task represents a merging of Manufacturing Process Simulation techniques (§5.3) with those of design automation.

CHAPTER VI

Program Plan and Timetables

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CHAPTER VI

Project Breakdown and Timetable

§6.0 Introduction

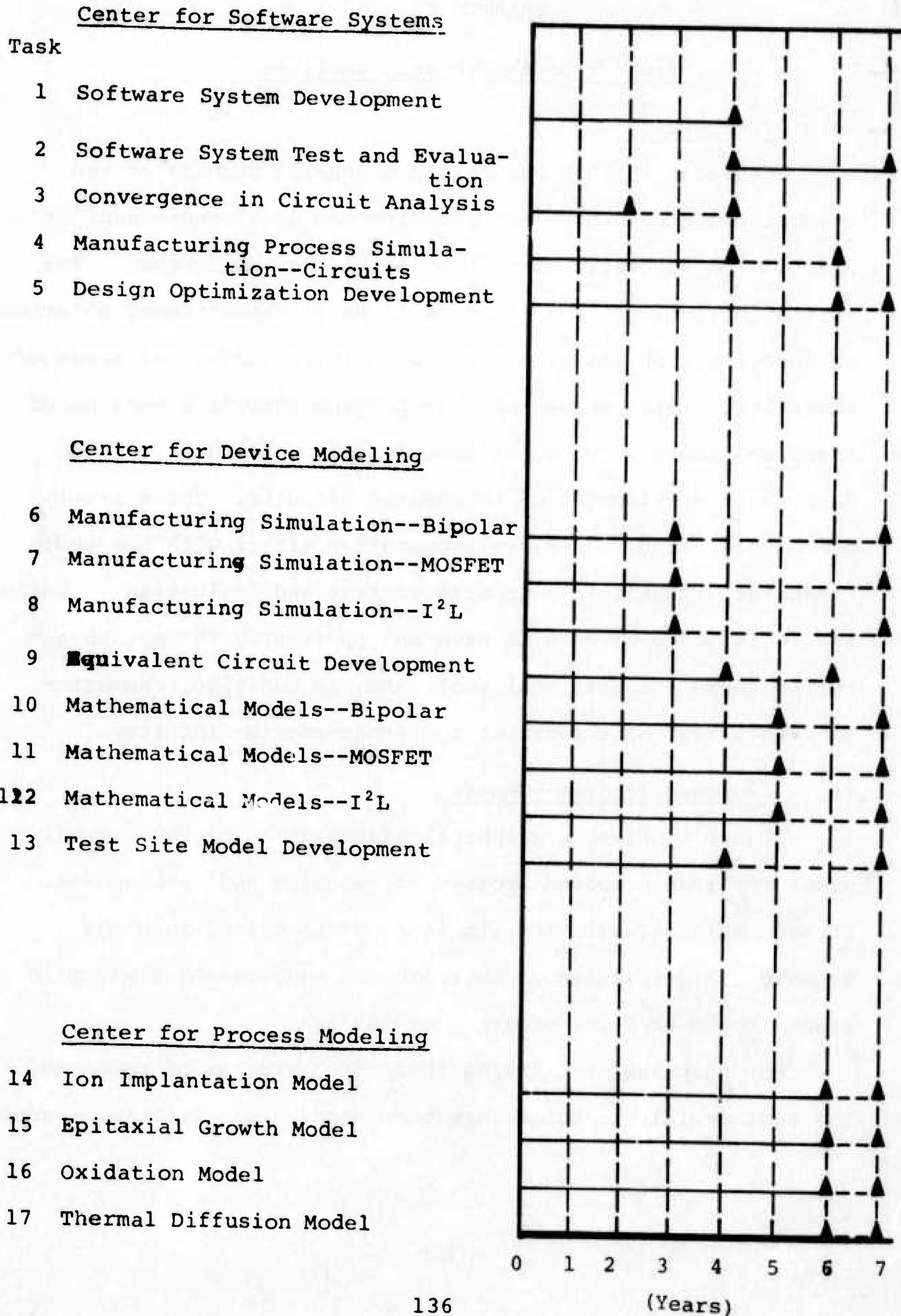
Presented in this chapter is a general summary of the overall proposed program of research and development and, in addition, a suggested timetable for its accomplishment. The initial efforts of each center will be directed toward solutions of specific problems associated with their individual areas of specialty. Later phases of this program involve a merging of these solutions into computational tools applicable to the design and development of integrated circuits. These later phases also involve a close cooperative effort with the semiconductor industry in a program of test and evaluation. Thereby, it is believed we will have an opportunity to improve and refine these computational tools and, in addition, encourage their utilization throughout the semiconductor industry.

§6.1 Proposed Program--General

Figure 6 offers a graphical illustration of the overall plans for this proposed program of research and development. Through this illustration, insight can be gained into the technical organization of this project and, in addition, milestones to be used for progress evaluation.

For purposes of unifying this large program of research, the test vehicle technique has been used. Specifically, a goal

Fig. 6 Program Timetable



has been set to construct a software system that is applicable for the design, development, and manufacturing of semiconductor integrated circuits. The availability of this software system will offer a method whereby we can accurately evaluate the technological advances made under this program. Further, through cooperative efforts with the semiconductor industry this software system can be applied to practical problems of IC design, as a complementary tool to their existing computational capabilities.

This proposed software system for IC design will offer a capability not presently available to the semiconductor industry. Namely, it will offer a means whereby the electrical performance of an IC can be predicted from basic process parameters. Included in this analysis is a computation of the electrical performance modificatons arising from a specified set of process parameter variations. Thereby, we can simulate on a computer the results to be expected when a new IC design is subjected to the process parameter variabilities associated with a given manufacturing facility. An additional capability of this proposed software system is to systematically modify and adjust the IC design as a means of desensitizing it against these fabrication process parameter variabilities; thereby replacing empirical methods presently used throughout the semiconductor industry.

The Center for Software Development will have the responsibility for those aspects of the program relating to this software development effort. In addition, this Center will undertake research and development relating to the circuit analysis aspects of this overall problem.

In Figure 6, tasks (1) and (2) represent the development and testing of this proposed software system. The first year of this activity represents a planning period [Task (1)] during which various aspects of related research efforts are incorporated into a common software system plan. During this first year's effort important decisions must be made concerning the overall approach to this problem: methods of undertaking Manufacturing Process Simulation at a circuit level; data base management from test sites, from process models, from device models, and from equivalent circuits; etc. Clearly, many problems will remain unanswered after this period of time. Nevertheless, decisions can be made concerning those aspects of the task now well understood, and plans can be made that are sufficiently flexible to accommodate future developments toward the end goal of this effort.

In task 1, it is proposed that four years be devoted to the design and development of this software system. Clearly, it would be unwise to undertake such a task without partial experimental verification of its contents. Therefore, this soft-

ware system effort will involve the development of computer programs to accomplish various computational tasks associated with IC design, and an experimental verification of each individual problem solution. Thereby, upon completion of this effort the entire software system will have been experimentally evaluated on a piecewise basis.

Task 2 represents test and evaluation of this software system as a whole. During this period extensive cooperation will be solicited from the semiconductor industry to obtain experimental verification of IC designs and, in addition, to identify shortcomings of the software system. Further, during this period extensive modification and refinement of this software system is expected through supporting activities that will be simultaneously underway; these activities are listed as additional task in this overall ARPA program.

Tasks 3, 4, and 5 (Fig. 6) represent individual research projects that are recommended to be undertaken and directed by the Center for Software Development. Task 3 involves a research effort aimed toward understanding problems of convergence and stability that exist in presently available computer programs for IC circuit analysis. Included in this research effort is a cooperative program of equivalent circuit development between this Center for Software Development and the Center for Device Modeling.

Tasks 4 and 5 represent programs of research and development that are closely related in nature. Task 4 involves a study of computational techniques whereby a manufacturing process simulation capability can be implemented into this software system for integrated circuit design. Task 5 is directed toward the application of design optimization techniques for the desensitization of an IC to process variabilities encountered during fabrication.

The Center for Device Modeling will be responsible for many tasks that are directly related to this software development effort, and for other tasks that represent technical "back-up" for this effort. Specifically, Task 6-9 (Fig. 6) have goals for the development of mathematical models used in this software system. Implementation of these models will be accomplished under Task 1.

Tasks 6-8 represent the development of simplistic models for manufacturing process simulation that offer a high computation speed. Many of these models are now available and, therefore, this development effort can be initiated at the start of this program. Other, no less important, models require development; in some situations this effort must await results from the mathematical model development tasks [Tasks 10-12]. An important part of this effort [Tasks 6-8] will involve a cooperative program with Task 9 (Equivalent Circuit Development)

where the calculated electrical parameters from these simplistic models are incorporated into equivalent circuits for the electrical analysis of IC structures.

Task 9 in Fig. 6 is the development of equivalent circuits for semiconductor devices that are applicable in the electrical analysis of integrated circuits. These equivalent circuits will represent a principal input to the circuit analysis program of parametric variabilities arising from the fabrication process. For this reason, these equivalent circuits must be founded upon the basic mechanisms of operation within semiconductor devices. They must also be of a form that is easily modified from calculations using simplistic device models (Tasks 6-8), and they must provide rapid convergence in the associated computer program for circuit analysis.

Included in this device analysis effort is the development of rigorous one and two dimensional mathematical models for transistor operation (Tasks 10-12). The purpose of these mathematical models is two-fold. First, these mathematical models will be used to investigate physical mechanisms associated with the steady-state and transient operation of transistors. Second, these mathematical models will be implemented into computer programs to be used by the semiconductor industry; there have been many requests for computer programs of this type.

Simplistic mathematical models to be used for manufacturing process simulation [Tasks 6-8] are developed through a detailed knowledge of physical mechanisms of device operation. Presently, some of these physical mechanisms are not understood and, as a consequence, there is no simplistic model available. An important aspect of the mathematical model development effort of this program [Tasks 10-12] is to gain this needed understanding and, thereby, support the program of manufacturing process simulation.

Task 13 represents a cooperative program of research and development between the Center for Device Modeling and the National Bureau of Standards. This cooperative effort is on the topic of test sites for IC process evaluation, and it will involve the mathematical modeling of specific test pattern structures. A principal direction for this modeling effort is to identify, using Monte Carlo methods of analysis, those test patterns that offer a large sensitivity to one particular process parameter. An adequate diversity of such test patterns would offer a means to monitor and evaluate every individual process parameter used for IC manufacturing.

The last four tasks listed in Fig. 6 [Tasks 14-17] represent an area of responsibility for the Center for Process Modeling at Stanford Univ. This particular aspect of the proposed program provides a needed link between IC fabrication process and mathematical models that predict the consequence of these processes upon the electrical properties of transistors.

Task 14 is a study of ion implantation, and the results of ion implantation into silicon. This research is aimed toward a prediction of the impurity profile resulting from ion implantation and, in addition, the damage profile arising from such a fabrication procedure. This study is directed toward implantations directly into silicon and through an oxide mask.

Tasks 15 and 16 in Fig. 6 represent a study of IC fabrication processes used today, yet areas where substantial experimental empiricism is used. Epitaxial growth, and auto-doping arising from a buried layer, represent areas where there is little theoretical understanding. Similar remarks are applicable to the oxidation techniques used in IC fabrication. These tasks are directed toward the development of mathematical models whereby the consequences of these processes can be predicted with an accuracy adequate for device analysis.

Task 17 is the continuation of an effort previously supported by the National Science Foundation. This task is directed toward the development of a rigorous mathematical model for the physical mechanisms associated with impurity atom diffusion into silicon, and other semiconductur materials. This effort, in conjunction with similar tasks undertaken at this Center for Process Modeling, provide an excellent opportunity to rigorously solve this long standing problem.

§6.2 Proposed Program Plan--Center for Device Modeling

Figure 7 graphically illustrates a proposed program plan for the Center for Device Modeling. Although this plan is subdivided into tasks relating to specific semiconductor devices, this subdivision is for convenience only. A substantial overlap exists between the work associated with these individual tasks. The MOSFET efforts [Tasks 1-8] are directed toward the development of mathematical models (steady-state and transient) for this semiconductor device. Similarly, Tasks 9-21 represent a multiplicity of efforts toward the mathematical modeling of bipolar transistor operation.

There are some topics of semiconductor operation for which our present understanding is inadequate. Tasks 22-27 in Fig. 7 (Device Research) outlines individual research projects directed toward those topics presently known to be required for this device modeling project. This is not intended to imply that this listing represents the only basic device studies proposed under this proposed program. There are other basic studies that are clearly needed for MOSFET model development, Tasks 4-6; further details are given later in this proposed program plan.

The last area of study and model development is directed toward the equivalent circuit representation of transistors (Tasks 28-30)--for both MOS and bipolar devices.

Fig. 7 Center for Device Modeling Task Timetable

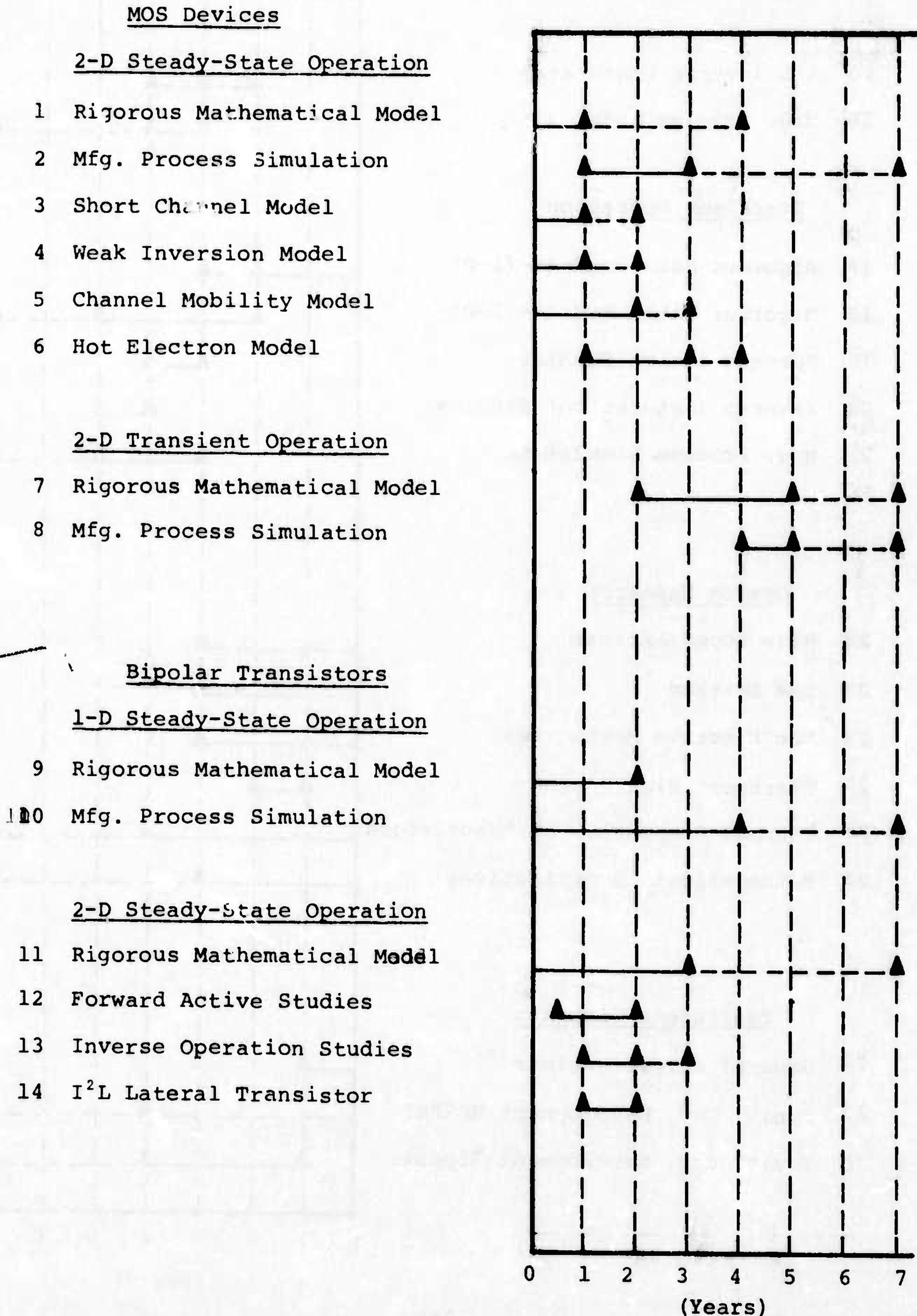


Fig. 7 Continued

Bipolar Transistors (Cont.)

15 I^2L Inverse Transistor

16 Mfg. Process Model I^2L

Transient Operation

17 Rigorous Math. Model--(1-D)

18 Rigorous Math. Model--(2-D)

19 Forward Active Studies

20 Inverse (saturation) Studies

21 Mfg. Process Simulation

Device Research

22 High Doped Emitter

23 L-H Emitter

24 Hot Electron Mechanisms

25 Transport High Doping

26 Thermal Properties of Transistors

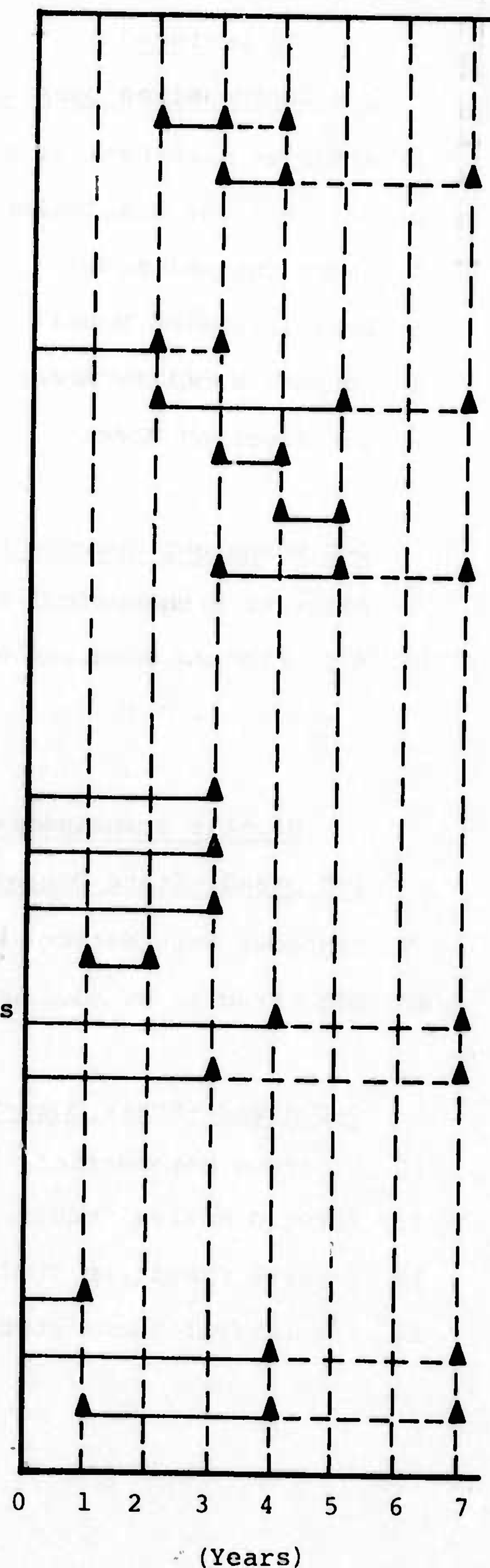
27 Mathematical Investigations

Equivalent Circuits

28 General Investigations

29 Equiv. Ckt. Development-MOSFET

30 Equiv. Ckt. Development-Bipolar



This proposed MOSFET modeling effort is directed toward the development of rigorous two-dimensional mathematical models for both the steady-state (Task 1) and the transient (Task 7) properties of this semiconductor device. A rigorous one-dimensional mathematical model for MOSFET operation is not obtainable because the physical mechanisms associated with this device are essentially two-dimensional. For this reason, all rigorous mathematical modeling tasks for MOSFET operation are based upon two-spatial dimensions.

It is recommended that Task 1 (Fig. 7) be undertaken immediately. A rigorous two-dimensional mathematical model for steady-state MOSFET operation is now available. The first year of this effort represents a "clean-up" of this computer program, and its detailed documentation. The follow-on effort on this topic represents a period of updating and improvement of this mathematical model, particularly from results derived from Tasks 5-6. It is now expected that this mathematical model, a computer program for quantitative calculations using this model, and a completely documented users manual will be available the first year of this program. This computer program will be offered to the semiconductor industry to assist them in the solution of MOSFET problems.

Immediately following this rigorous two-dimensional MOSFET modeling effort, a simplistic mathematical model for this structure will be developed for manufacturing process simulation (Task 2). A substantial part of this model is now available, although it is presently inapplicable for short channel devices, or for devices operating in the weak inversion mode of operation. This difficulty has been investigated. There is substantial reason to believe these short-channel and weak inversion problems can be overcome in the first year of this program (Tasks 3-4) and, thereafter, this process simulation model will be available for engineering use.

Tasks 5 and 6 represent fundamental investigation into MOSFET operation for which there is presently inadequate understanding. Furthermore, the physical mechanisms to which these research efforts are directed are inadequately described by any mathematical model of MOSFET operation, regardless of the degree of mathematical rigor. Task 5 (channel mobility model) is directed toward the problem of carrier mobility changes in an inversion layer, due to changes of gate voltage. An initial investigation on this topic has revealed some fundamental inaccuracies associated with existing mathematical models of MOSFET operation. After completing this task, a follow-on program is recommended whereby the understanding gained from this reserach is used to update the rigorous two-dimensional model (Task 1).

The study of hot electron mechanisms in the inversion layer of a MOSFET (Task 6) has both short-term and long-term implications relating to the use of this semiconductor device. Namely, it has been suggested that hot-electron mechanisms, in association with relaxation processes in the semiconductor crystal, could place fundamental limitations upon the maximum operating frequency (or switching speed) of a MOSFET. This research is directed toward an understanding of this problem, and its mathematical modeling.

A transient analysis of MOSFET operation has not, to date, been accomplished. There are reasons to believe that such an analysis could be accomplished using traditional methods of numerical analysis, although it is known this solution would require an excessive amount of computer time. Therefore, the initiation of this effort is delayed for about two years; thereby, the proposed mathematical investigation (Task 26) will have an opportunity to study this problem from a mathematical point of view. If better (and faster) mathematical methods can be applied to such a solution, it would be wasteful to start using traditional methods that are known to introduce many computational difficulties.

Clearly, manufacturing process simulation for MOSFET transient properties (Task 8) is a follow-on application of the findings from Task 7 (Rigorous Transient Model of a MOSFET).

The purpose of this process analysis effort is to describe in a simplistic model (one that can be calculated at high speed) physical mechanisms associated with the transient properties of this semiconductor device.

The proposed program for bipolar transistor modeling is subdivided in a manner similar to that for MOSFET modeling. There is one important exception to this similarity; the development of a rigorous one-dimensional model is proposed for the steady-state operation of bipolar transistors. The reason for this proposal is two-fold. First, a steady-state mathematical model is of prime importance to the device designers. Second, this type of model is now available, although such a model is not readily accessible to the semiconductor industry.

For this reason, Task 9 in Fig. 7 is directed toward acquiring one of these computer programs and adequately documenting it in a users guide. Thereafter, this mathematical model, a computer program based upon this model, and a detailed users guide will be made available to the semiconductor industry.

Thus far, all Mfg. process simulation for bipolar transistor operation has been accomplished on a one dimensional basis. Task 10 represents the development of this capability, based upon techniques that are now known and understood. Included in this task is the development of mathematical models for bipolar transistor operation, and their incorporation into a computer program for manufacturing process simulation. This proposed computer program

will also contain methods for data management and data print-out in a form applicable for bipolar transistor design.

The two-dimensional modeling of steady-state bipolar transistor operation introduces numerous problems of computer speed and capacity. Nevertheless, a computer program of this type is now available at the Univ. of Florida. For this reason, the initial part of Task 11 (Rigorous Steady-State 2-D Model) represents the documentation of this computer program and its dissemination to the semiconductor industry. At a later time, it is fully expected that a modified computer program will be developed under this Task; this modified program will be based upon mathematical techniques that yield a higher computation speed.

Despite the inherent difficulties associated with this two-dimensional computer program, Tasks 12-16 represent individual programs of investigation based upon its use. Tasks 12 and 13 are directed toward two-dimensional studies of transistor operation that heretofore have not been adequately investigated. The forward active studies of transistor operation (Task 12) is directed toward a detailed understanding of minority carrier injection mechanisms at the periphery of an emitter junction, as a function of emitter biasing voltage. Previous two-dimensional calculations have shown some unreported high current mechanisms in this region of a transistor that could significantly influence

its electrical characteristics. Task 13 (Inverse Operation Studies) is directed toward the development of a simplistic model for the bipolar transistor when operating in saturation; this simplistic model must be based upon the two-dimensional mechanisms revealed by rigorous calculations of this problem.

Tasks 14-15 represent a rigorous two-dimensional steady-state mathematical modeling of an I^2L type structure. This can be accomplished using a modified form of the forementioned computer program (Task 11). After developing this mathematical model, investigations will be directed toward lateral transistor operation (Task 14) and inverse operation of the vertical transistor in an I^2L configuration (Task 15). Thereafter, from insight gained from these investigations a simplistic mathematical model will be developed for I^2L operation (Task 16) that is suitable for manufacturing process simulation.

At this time two different mathematical models are available at the University of Florida for a one-dimensional transient analysis of bipolar transistors. It is recommended that one of these computer programs be documented in a users manual and made available to the semiconductor industry. This approach offers two advantages. First, it will make this computer program available to semiconductor organizations that would otherwise not have this computational capability. Second, this traditional type of finite-difference calculation would offer a basis for

comparison when testing new computational and mathematical methods (Task 27).

It is recommended that the development of a rigorous two-dimensional mathematical model for the transient operation of bipolar transistors be delayed until after studies on this topic have been completed. During the intervening time requests will be made to the Univ. of Aachen (Germany) for copies of their computer program offering this capability. Thereafter, this computer program will be subjected to a detailed evaluation. It is also recommended that proposed mathematical investigations at the Univ. of Florida (Task 27) be undertaken for a sufficient period to yield conclusions concerning the most hopeful path to follow toward a solution for this problem.

Tasks 19-21 in Fig. 7 represent effort based upon the utilization of this two-dimensional transient solution for bipolar transistor operation.

There are numerous problems associated with transistor operation for which we have only limited understanding. For example, the current gain of a bipolar transistor cannot be calculated with any reasonable degree of accuracy. The source of this difficulty is not known, and Tasks 22 and 23 are directed toward possible solutions for this problem. Task 22 is an investigation of the many proposed theories concerning the consequences of high doping in the emitter region of a

bipolar transistor; these theories suggest that the current gain is primarily a consequence of a poor emitter injection efficiency. Task 23 represents a study of the low-high emitter junction; this structure has been reported to yield a very large emitter injection efficiency.

Tasks 24 and 25 represent areas of research directed toward a solution for problems of transistor modeling for which there is only limited understanding. The hot electron problem is evidenced in device operation by a terminal velocity of mobile carriers in regions of large electric field. In the analysis of semiconductor devices, there is substantial confusion about the correct mathematical representation of this phenomenon, particularly in regions where both drift and diffusion are important. This research is directed toward a solution of this problem, and the mathematical representation of hot electron mechanisms in models for transistor operation.

Task 26 represents an important aspect of semiconductor device modeling, and a problem that has received inadequate attention: changes in the electrical characteristics of a transistor, due to changes of temperature. Under this program, it is suggested that research should be directed toward this problem as a means to accurately model the temperature characteristics of semiconductor devices.

An important research effort under this proposed program is essentially mathematical in nature [Task 27]. This research is directed toward the solution of problems recognized throughout the entire semiconductor industry: mathematical and computational difficulties associated with the analysis of semiconductor devices. Presently, a rigorous solution of many important problems of semiconductor device operation require an unreasonable amount of computer memory. Mathematicians skilled in applied mathematical analysis have suggested that this problem arises from the analytical techniques being used: namely, finite difference solutions for differential equations.

It is proposed that research be directed toward the solution of this problem of device analysis. Specifically, it is recommended that a research team be formed of mathematicians, numerical analysts, and device physicists. Through the joint efforts of these specialists it is proposed we seek methods of analysis that are more suitable for the problem at hand. Specifically, the goal for this proposed research effort is to develop mathematical methods that will, in time, provide a means to solve two-dimensional transient problems associated with transistor operation.

Tasks 28-30 in Figure 7 represent an effort of research and development that is directed toward the equivalent circuits used to describe transistor operation. There are three principal

tasks associated with this research. First, the development of fundamental principles upon which equivalent circuit networks are to be developed, Task 28. The second and third tasks represent the extension of these fundamental principles to the MOS transistor (Task 29) and to bipolar transistors (Task 30). Implied in this program of research is an incorporation of fundamental physics of device operation in the resulting equivalent circuits and, in addition, satisfying problems of stability and convergence associated with the electrical analysis of integrated circuits.

§6.3 Proposed Program Plan -- Center for Process Modeling

The Center for Process Modeling will undertake research and development in four areas that are of particular importance to this proposed program:

1. Ion Implant Studies,
2. Oxide Model Development,
3. Epitaxial Growth Modeling,
4. Theory of Thermal Diffusion.

The specific tasks associated with these research efforts, and a specific timetable, are shown in Fig. 8 of this report.

The first area of research (Ion Implantation) consists of six individual tasks, all directed toward a solution of problems that are of particular importance to this overall ARPA program. In general, several of these tasks are directed toward modeling

TASK

Ion Implant Studies

1) Profile Calculations

2) Profiles at Mask Edges

3) Mask Damage Theory

4) Trapping in Semicond.

5) Rad. Enhanced Diff.

6) Process Model Dev.

Oxide Model Dev.

7) Growth Model

8) Model for Q_{ss}

9) Ion Gettering

10) Device Modifications

11) Fast Surface States

12) Radiation Damage

13) Oxide-Nitride Interface

14) Impurity Pile-Up

15) Device Modifications

Epitaxial Growth

16) Profile Measurements

17) Kinetics of Dopant Inc.

a) Doped Layer Form.

b) Non-Uniform Doping

c) Poli-Growth

d) Layer Kinetics

18) Buried Layer Auto.

19) Geo. Considerations

Thermal Diffusion

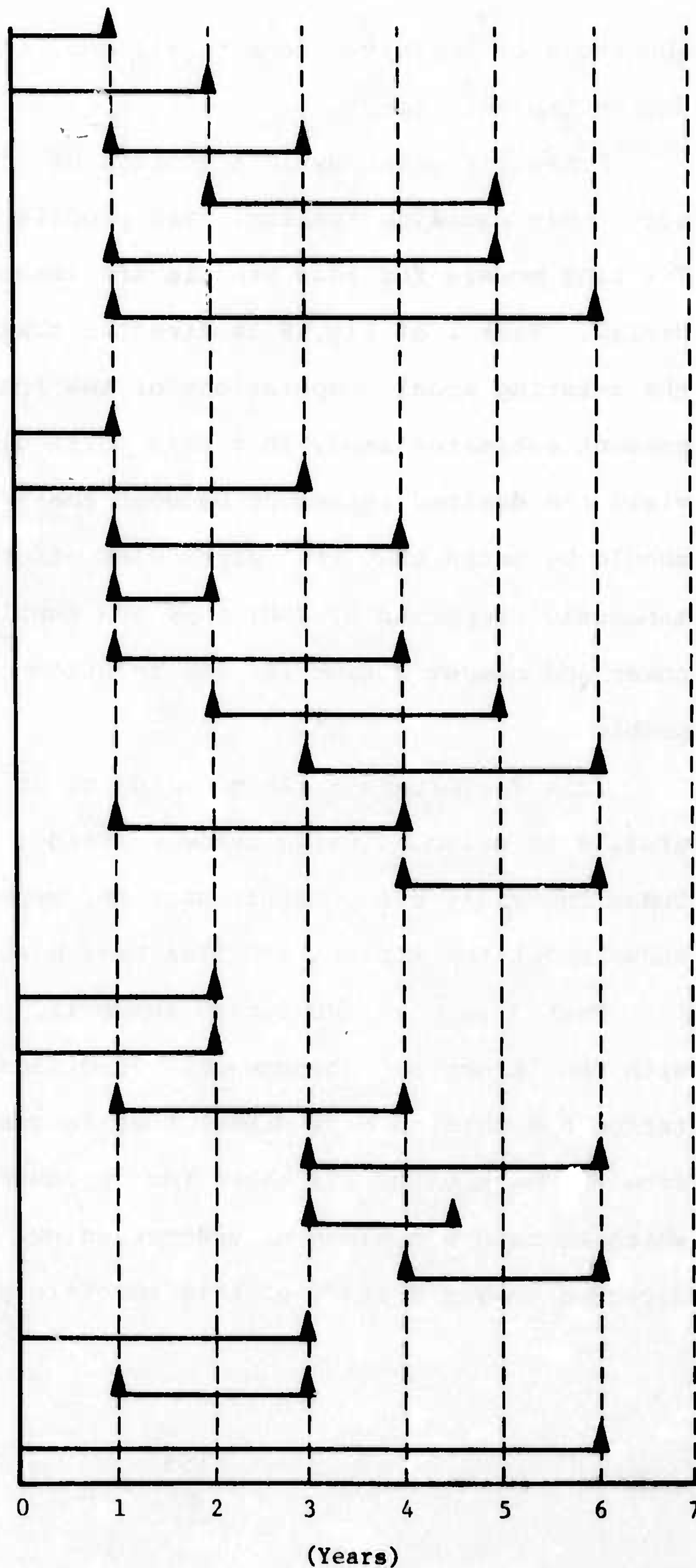


Figure 8. Center for Process Modeling -- program plan.

the range of implanted ions in silicon, and the damage produced during implantation.

Presently underway is a program of effort directed toward accurately modeling the implanted profile of boron in silicon. Existing models for this profile are inadequate for device design. Task 1 of Fig. 8 is directed toward introducing into the existing model computations of the fourth central moment; present estimates imply that this particular extension will yield the desired agreement between theory and experiment. It should be noted that this particular effort is being simultaneously supported by IBM; they are supplying substantial manpower and computer time for the solution of this particular problem.

Task 2 represents the modeling of an ion implanted impurity profile in silicon, using oxide, nitride, and photoresist masks. These materials are commonly used for masking, yet little is known about the implant profiles near mask edges.

Task 3 is directed toward answering problems associated with the "knock-on" phenomenon. Specifically, during implantation one obtains mask damage that forces ions into silicon, from the mask material; these ions produce lattice damage, for which we have a minimum of understanding. This task is directed toward a study of this specific problem.

Task 4 is directed toward a study and characterization of implantation produced trapping centers. Here we will investigate the electrical properties of traps that are produced by unwanted "knock-on" impurities, and residual damage in the silicon produced by ion implantation.

Task 5 is directed toward a study of radiation enhanced diffusion phenomenon. During implantation, impurity atoms are introduced into silicon with an accompanying vacancy distribution. Thereafter, diffusion from this implanted distribution will not follow laws governing traditional diffusion processes. Using the diffusion model developed under Task 20 of Fig. 8, it is intended to establish a means whereby the resulting diffusion profile is mathematically predictable.

Task 6 represents the incorporation into a single comprehensive model the results gained from all previous research tasks undertaken in this investigation of ion implantation. This comprehensive model will include the final impurity and trapping profiles for annealed multiple implants--through layers and other surface situations.

Tasks 7 through 15 are directed toward research and model development for the oxides, and other insulators, used in IC fabrication. This particular area of research is of importance to this project because it represents a topic for which there is little understanding and, therefore, our ability to model is presently inadequate.

Task 7 represents the development of a computer model for the growth of oxide on silicon. Oxide growth is dependent upon many factors: crystal orientation, residual doping, etc. Here, it is our goal to develop a mathematical model whereby the thickness of oxide growth can be predicted on a computer. There presently exists a model for this growth process, although this model has not been adequately tested and evaluated for device design purposes.

Task 8 is a development of models that adequately establish the density of excess ionized silicon at an SiO_2-silicon interface (Q_{SS}). The solution of this problem is of particular importance for the design and development of MOSFET structures. Therefore, this effort will be started at the initiation of this proposed ARPA program.

Task 9 is directed toward the development of a mathematical model for chlorine ion gattering processes which are almost universally used throughout the semiconductor industry. Today, gattering is not well understood. It is recognized that chlorine ions in SiO_2 influence the growth rate, surface states, etc.; this effort will offer a further improvement of the oxide growth model previously discussed under Task 7.

Task 10 represents a cooperative effort between the Center for Device Modeling and the Center for Process Modeling. This effort is directed toward an implementation of the oxide model into a two-dimensional mathematical model for a MOSFET and,

thereafter, an investigation of the consequences of these oxide mechanisms upon the electrical characteristics of this semiconductor device. The aim of this effort is to obtain an overall model whereby adequate agreement is obtained between experiment and theory.

Task 11 is the development of a mathematical model for fast surface states in the insulator of a MOSFET. A solution for this problem is of particular interest in any *a priori* design of MOSFET structures, although there is presently no suitable mathematical model for fast surface states. It is presently believed that such a mathematical model can be developed with a specific, and concentrated, effort toward this goal.

Task 12 represents a cooperative program between these oxidation studies and the forementioned ion implant investigations. The goal for this effort is to gain a quantitative understanding of oxide damage during ion implantation. Such a model could be used extensively for evaluating the consequences of threshold tailoring, as presently done throughout the semiconductor industry.

Task 13 is a study of the interface charges that are produced during the fabrication and operation of double-dielectric MOS structures. This problem is well known in industrial organizations that are studying, designing, and manufacturing MNOS type of semiconductor devices. There is extensive know-

ledge in this area, and it is believed that further knowledge will be forthcoming during the next few years.

Task 14 represents a study and mathematical modeling of impurity profiles arising from a simultaneous diffusion and oxidation. Basically, a close look must be given to the segregation coefficients of impurities in SiO_2. From this information, the mathematical model for (Task 20) will be used to calculate the agreement we obtain between experiment and theory. A goal for this effort is to develop an ability to accurately predict the impurity profile obtained during this type of fabrication process.

As before, Task 15 represents a detailed evaluation of the consequences arising from this overall study of oxides. The numerous oxide models will be introduced into two-dimensional mathematical models for semiconductor device operation, and calculations of the resulting electrical characteristics will be compared with experiment.

The next project area covered by this center represents the study of epitaxial growth of silicon on silicon. An important aspect of this effort is to model the impurity distribution in an epitaxial layer with the accuracy needed for the analysis of semiconductor devices. Tasks 16 through 19 represent investigations directed toward that particular goal.

It is well recognized that our present ability to measure impurity profiles in silicon are inadequate for a detailed study of the problem. For this reason, an initial effort will be directed toward the development of a suitable measurement capability. This particular task will be undertaken in coordination with work presently underway at NBS on the solution of such measurement problems.

The second topic of investigation is called kinetics of dopant inclusion (Task 17) in an epitaxially grown layer. The first phase of this effort will be directed toward a study of the parameters associated with the gas to solid phase transition arising during epitaxial growth; for example, the segregation coefficients involving the transfer of silicon and impurities from the gas to solid phase during layer growth. This task will represent part of the effort directed toward the development of a mathematical model for epitaxial growth.

Sub tasks under this general heading of the kinetics of dopant inclusion (Task 17) are listed as Task 17a through Task 17d. The first of these subtasks (Task 17a) is a study of the kinetics associated with doped layer formation. This study is directed toward developing a basic understanding of the physical mechanisms taking place in an epitaxial reactor. Subtask 17b is directed toward the modeling of epitaxial material growth with a prescribed impurity atom distribution;

this ability is of particular interest in the fabrication of I^2L structures. An additional subtask is the growth of polycrystalline layers of silicon, and the inclusion of dopants in such materials; this problem is of particular importance for the fabrication of silicon gate MOSFET structures. The last subtask (Task 17d) represents an investigation of the kinetics associated with the epitaxial growth of polycrystalline silicon material, and the development of a mathematical model that is based upon these physical mechanisms.

Task 18 in Fig. 8 is directed toward studies of the consequences of substrate doping upon the doping profile and lattice perfection of an epitaxial layer. This particular task is intended to answer many problems that arise in the fabrication of bipolar transistors, and are expected to also arise in the fabrication of I^2L structures. The end goal for this task is the development of a mathematical model that will predict the doping profile in an epitaxial layer, due to an underlying buried layer in the substrate material.

The last task under the topic of epitaxial growth (Task 19) represents a study of the consequences of substrate geometry upon the epitaxial layer. It is suspected that differences between the isolated buried layers used for bipolar transistor fabrication and the blanket substrate diffusions used for I^2L will produce significant differences in the resulting epitaxial layer doping profile. Again, this task will also be directed

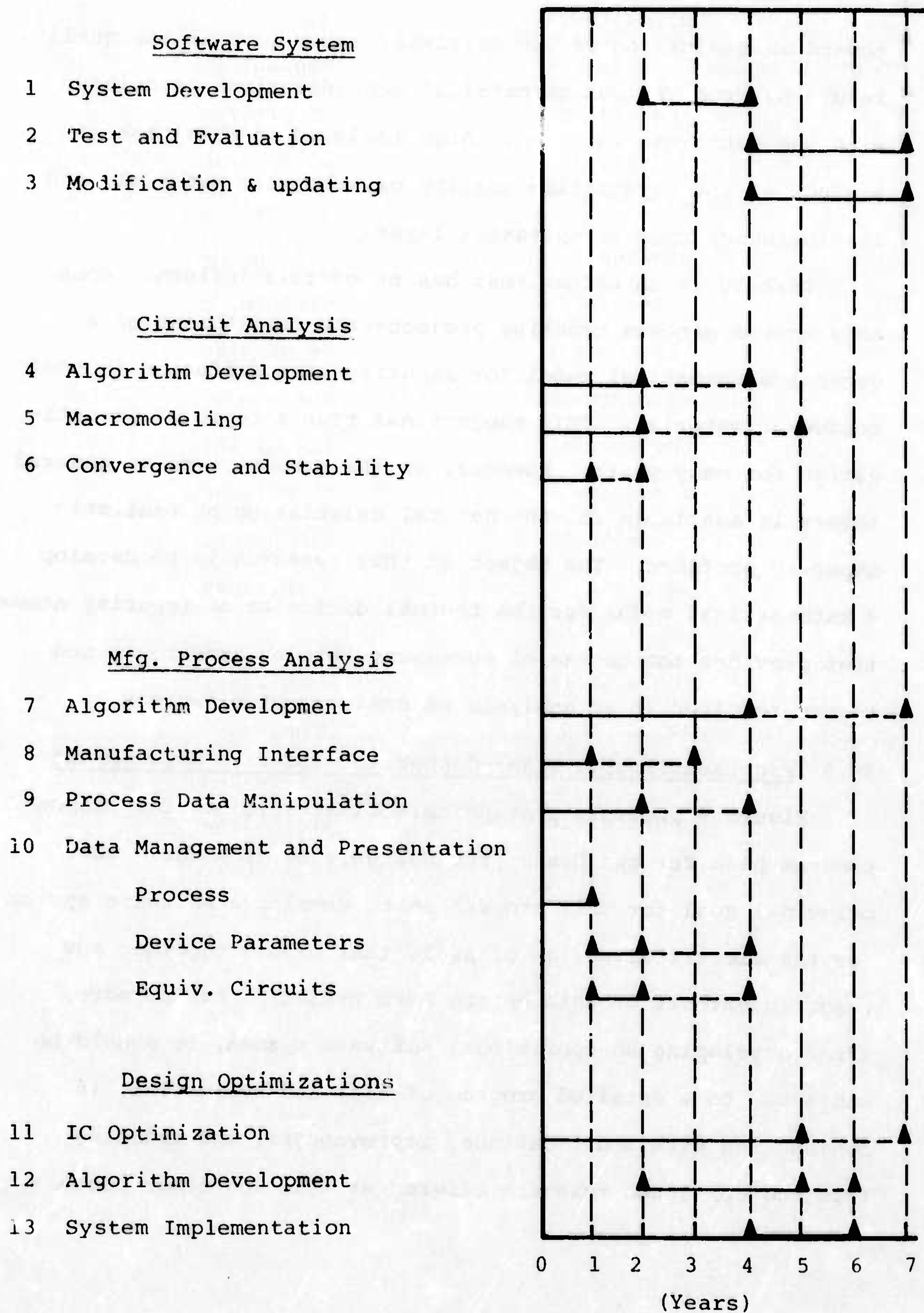
toward an evaluation of the epitaxial layer crystalline quality resulting from various geometrical considerations associated with the substrate material. Also included in this task is a study of the crystalline quality of substrate material, and its influence upon an epitaxial layer.

Task 20 is an effort that has an overall influence upon this entire process modeling project--the development of a general mathematical model for impurity atom diffusion in semiconductor material. This subject has been a topic of investigation for many years. However, at the present time no general theory is available for the general calculation of realistic impurity profiles. The object of this research is to develop a mathematical model for the thermal diffusion of impurity atoms that provides the degree of agreement between experiment and theory required in an analysis of semiconductor devices.

§6.4 Proposed Program Plan--Center for Software Development

Figure 9 presents a graphical illustration of the proposed program plan for the Center for Software Development. The principal goal for this program is to develop a software system for the electrical design of an IC that brings together the research efforts of this entire ARPA project. Furthermore, after developing an operational software system, it should be subjected to a detailed program of test and evaluation, in conjunction with modifications, improvements, and updating from the continued research efforts at this and other Centers.

Fig. 9 Center for Software Development Program Plan



Included in this program plan are research and development efforts that are essentially of a circuit analysis nature or, instead, are intimately related to the systems aspect of this problem. A substantial portion of this research effort is directed toward the solution of problems that remain unsolved in the area of circuit design and analysis.

Tasks 1-3 in Fig. 9 represent a development program that implements the overall results of this ARPA program into a software system. Task 1 is the initial implementation into one computer program that is operational for IC analysis and design. It is fully recognized that at this stage of the program there will remain many unanswered questions; therefore, this computer program will be incomplete from many points of view. For this reason, Tasks 2-3 represent a period of test and evaluation, in addition to the modification and updating of this analysis system. Testing and evaluation will be accomplished through a cooperative effort with the semiconductor industry, with DoD system vendors, and with DoD organizations that have in-house IC facilities.

Throughout this period of testing and evaluation, it is expected that some of the more difficult problems of this program will have been solved. Therefore, simultaneously a Task of system modification and updating (Task 3) will introduce improvements and refinements into this software system.

Further, included in this system development effort is the complete documentation of the software system, and assistance to the semiconductor industry for its adoption -- in part or in its complete form.

The circuit analysis aspects of this program plan [Tasks 4-6] addresses problems that can now be foreseen in the development of a circuit analysis and design system. For example, at this time it appears necessary to develop new algorithms for the electrical analysis of an IC [Task 4]; algorithms that offer a substantial increase of computing speed. This necessity arises from the proposed development of a capability for Manufacturing Processes analysis, in conjunction with the desensitization of an IC design to fabrication process variables.

Manufacturing Process Analysis at a chip level represents, today, a task that is beyond the state-of-the-art. Nevertheless, macromodeling of an IC cell, and of logic functions, could offer this capability within the lifespan of this ARPA program. For this reason, macromodeling is included as a topic of research [Task 5] in this program plan.

Problems of computational convergence and stability are encountered in many IC analysis programs used throughout the semiconductor industry. The source of this difficulty is unknown, and Task 6 (Fig. 9) is directed toward gaining an understanding of this problem. Through this understanding, is

intended that this Task will provide guidelines for equivalent circuit development that would assist in an alleviation of these problems. Furthermore, under this task a cooperative program will be established with the Center for Device Modeling. on the common problem of equivalent circuit representation of transistors for circuit design.

Manufacturing Process Analysis techniques have never been systematically implemented into a single computer program designed for that purpose. Past experience has been gained through the utilization of individual computer programs where problems of the manufacturing interface, process data manipulation, data management, etc. have been accomplished manually, and with great difficulty. For this reason, Tasks 7-10 represent the development of plans for the solution of these problems, and the implementation of these plans into practical software systems for inclusion into the IC design system of this program.

Task 7 represents the development of algorithms whereby processing data can be utilized in the design of an IC for manufacturing process simulation. Included in this task is the application of simplistic (high speed) mathematical models for transistor operation within the IC design system. Furthermore, this task will direct attent toward problems of utilizing these models in the process of IC design. In general, it

is proposed that this task provide a link between all research and development efforts working on related problems of manufacturing process simulation, and the software system development effort.

Any computational system of this type involves many problems of interface with the outside world. This situation is particularly true when required to interface with an IC manufacturing line. For example, problems of data acquisition from test site measurements have, in past years, produced weeks of delay before undertaking an analytical study of manufacturing process analysis. Task 8 in Fig. 9 is designated to formulate a detailed plan to solve these problems and, in addition, assist in the implementation of this plan into the IC design system.

Test site measurement data often requires extensive manipulation before it is applicable for manufacturing process analysis. In past years this manipulation procedure was done manually, with the aid of a computer. Typically, six to twelve weeks of effort was required to manipulate data; this same manipulation could be accomplished in a few seconds if done automatically on a computer. Task 9 represents an effort directed to automate these procedures and thereby greatly enhance the utility of this proposed IC design system.

This IC design system will generate and use hundreds of thousands of parameters, both measured and calculated. For this reason, there is a great problem of data management, and the presentation of data to the system user. Task 10 represents an effort directed toward a solution for this problem. It is important that the proposed solution for data presentation not involve expensive and complicated equipment. If so, the semiconductor industry would be reluctant to adopt this design system for their engineering facilities. It is the intention of this program to offer the semiconductor industry a circuit analysis and design package that is easy to use and inexpensive to implement. In addition, adequate information will be supplied with design package to enable its customization to satisfy individual needs.

It is not immediately evident how extensive design automation can be implemented in this design system for the automatic desensitization of an IC structure. Eventually IC desensitization might be accomplished on a totally automatic basis, but this ideal situation should not be expected from the near-in efforts of this program. Nevertheless, there is adequate evidence to show that manual desensitization procedures (using design optimization techniques) could be introduced at an early stage of design system development.

Tasks 11-13 represent efforts directed toward a solution of this design problem. Task 11 represents an on-going program of research on the overall topic of design optimization, and its application to the design and engineering of IC structures. It is now believed that the early stages of this research effort will yield some basic algorithms for IC desensitization in the early stages of this program. Thereafter, there will be a continuous updating and refinement of these algorithms (Task 12), and their eventual implementation into the overall IC design system.

APPENDIX I*

Workshop on Process Prediction and Modeling

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* Note: The contents of the Appendices are derived directly from conversations monitored (via audio tape) at the five major workshops indicated in the index. In an attempt to maintain the general tone and flavor of these conversations, information is presented in these appendices in approximately the same manner as taken from these tapes.

Appendix I

Workshop on Process Prediction and Modeling

A1.0 Introduction

A summary is presented of opinions, comments, and technical information gained from the workshop on Process Prediction and Modeling. This workshop was held at the U.S. Army Electronics Command, Ft. Monmouth, N.J. on July 23-24, 1974. Present at this meeting were the Steering Committee members listed on page 6 and, in addition, the invited guests listed below.

Dr. Bruce Deal	Fairchild Semiconductor, Palo Alto, California
Mr. Robert Donovan	Research Triangle Institute, Research Triangle Park, N.C.
Dr. Paul Gary	Bell Telephone Laboratories, Allentown, Pennsylvania
Dr. James Gasparus	ECOM, Ft. Monmouth, N.J.
Dr. William Johnson	IBM, Hopewell Junction, N.Y.
Dr. George Schnable	RCA Labs., Princeton, N.J.

A specific goal for this workshop was the evaluation of our present capability to quantitatively describe the consequences of IC fabrication processes. Further, where an inadequate capability existed, it was hoped that thiw workshop

could offer suggestions as to where the present theory was either incomplete or incorrect.

The specific process areas of interest are as follows:

(a) Oxidation processes used in IC fabrication

(b) Ion implantation of impurities into silicon

(c) Thermal diffusion into silicon

(d) Epitaxial growth of silicon on silicon

The scientists and engineers engaged in this workshop offered a wide scope of different opinions, yet these opinions could be broadly grouped into two categories: first, those of the large-volume manufacturer and second, those of the small-volume (custom design) LSI producer. The large-volume manufacturer saw little value in parametric control of fabrication processes, and considered the statistical defects arising in any IC manufacturing line to be of far greater importance. The custom IC designer considered these statistical defects to be of minor concern in the fabrication of a small-volume of IC structures; to the custom designer parametric problems were of greater importance

It was clearly stated that the difference between these two points of view arise from the volume of IC structures under consideration. Statistical defects due to pipes, photolithography, mask defects, etc., are of great importance in large

volume manufacturing. Such defects produce 60% to 80% of all production losses and thereby result in a continuing loss of revenue. On a long term basis, defect problems produce a far greater financial loss to the large-volume manufacturer than do the parametric problems under discussion at this workshop.

Contrasting with the views of large-volume manufacturers are the views of those interested in small-volume custom design. The custom designer places less importance upon statistical defects because they produce fewer problems in the initial fabrication of a new IC structure. In small-volume IC manufacturing, statistical defects produce a financial loss that is small, relative to the cost of design and development. The custom IC design never reaches a manufacturing volume level where statistical defects represent a serious problem.

Additional differences exist between large-volume and small-volume (custom design) IC manufacturers. In large-volume manufacturing it is relatively unimportant to have full understanding of the fabrication processes. Instead of relying upon fundamental understanding, the large-volume manufacturer will attain a desired result by trial-and-error engineering techniques. In small-volume manufacturing of custom IC structures, trial-and-error is not an economically sound engineering technique; basic understanding must be used to gain the desired result in a minimum period of time.

These two contrasting points of view provide substantial insight into future directions of industrial IC development.

Future industrial expenditures will be directed toward limiting financial losses during large-volume IC manufacturing, and basic understanding is unnecessary to accomplish this goal. It is therefore concluded that there are areas of IC fabrication processing where industrial organizations will solve the relevant problems, with no government intervention. There are other clearly defined areas of IC processing where government sponsored research appears necessary. These areas primarily involve the development of basic understanding.

A1.1 Comments on an IC Design Procedure

Discussions at this workshop revealed that IBM and Bell Labs. have developed similar views on needed IC design procedures. Specifically, they believe that IC design should be based upon the process variabilities encountered in a given IC manufacturing facility, and that the design should include an optimization of parametric yield to a particular manufacturing environment. This view is derived from the knowledge that process variabilities differ in each and every manufacturing line, and there is no reason to expect that a given design can be fabricated in any arbitrarily selected fabrication facility. Further, it is known that each design exhibits a different sensitivity to the numerous process variabilities encountered during fabrication. For this reason, a new IC structure cannot be assumed to be manufacturable on a given production line, even if this line is presently producing IC structures in a satisfactory manner.

It is suggested that an absence of this design procedure produces frequently experienced manufacturing "start-up" difficulties. Large volume IC manufacturers recognize that substantial empiricism is required during initial manufacturing start-up for a new product, even when using a well established manufacturing line. This is often called a "learning" period instead of a "redesign" period. During manufacturing start-up, the design of an IC is usually subjected to the empirical changes necessary to accomodate fabrication process variabilities; the structure is experimentally redesigned to maximize the yield of satisfactory devices. Experience at both IBM and Bell Labs. shows that this aspect of IC design can be accomplished on a computer prior to committing a new product to manufacturing.

This procedure utilizes measured processing data from a given production line. Mathematical models for physical and electrical properties of the resulting semiconductor devices are used, and Monte Carlo methods of analysis are applied to calculate parametric distributions arising from these process variabilities. Thereby, even at the device level one can computationally establish the expected yield of satisfactory transistors from a given production line. Further, at this point it is a relatively simple matter to alter the design of a given transistor in order to obtain a minimum expected fabrication loss due to devices with "out-of-spec." electrical characteristics.

It was emphasized by the Bell Labs. representative (Dr. P. Gary) that this design technique should be applied at each stage of IC design. A similar opinion has been voiced by the

principal investigator for this study program. Resulting from such a computational technique would be a detailed understanding of the consequences of process variabilities upon the electrical properties of an IC. Thereby, the design of an IC could be adjusted to accommodate these process variabilities; an application of this design technique would greatly simplify the problem of manufacturing "start-up".

There are numerous important problems that must be solved before the foregoing design technique becomes a reality. In particular, methods must be developed whereby fundamental fabrication process parameters can be measured during IC manufacturing. This particular problem will be addressed under the topic of device modeling. Additional problems exist with respect to calculating the consequences of process variabilities upon the electrical properties of an IC. Research directed toward the solution of this computational problem is suggested for the software effort of this proposed program.

Al.2 Thermal Oxidation

A discussion on oxidation was presented by Dr. Bruce Deal (Fairchild); he presented a general outline of the state-of-the-art, covered some significant problem areas, and probed the future for potential solutions of today's problems. It was made clear that while good process control is available for oxidation processes used in IC fabrication, this control is based upon empiricism and not on basic understanding. The consequences of this situation are the difficulties arising from introducing new oxidation processes into device fabrication;

each new process modification introduced produces a new round of empiricism. It was also emphasized that this empiricism is both expensive and time consuming. For this reason, changes and modifications of an oxide process involves substantial time before adequate control is attained for assurance of satisfactory semiconductor products.

It was also stated during this discussion that process control for oxidation requires substantial skill, and that maintaining process control is a difficult task. Semiconductor manufacturers frequently lose control of their oxidation process and, as a consequence, experience a production "bust." An important consequence of this situation on the part of IC manufacturers is substantial uncertainty over their ability to maintain control of a large volume manufacturing line.

The most common of these oxidation processes is the thermal reaction of O_2 or H_2O with silicon. In this process O_2 or H_2O diffuses through the SiO_2 layer, and reacts with Si. It is believed that partially oxidized Si exists at this Si-SiO_2 interface, and produces an interface charge known as Q_{ss}. In addition, other charges of lesser known origin exist in the oxide: fast interface states and positive charges deep in the oxide. It is also known that contaminants such as sodium, potassium, and lithium produce charges in the oxide. Clearly, this multiplicity of charges in the thermal-grown oxide offers many difficulties to process control.

Extensive research is presently directed toward a solution for these problems, but this research is not believed to be adequate on a long range basis. Government funding has been directed toward empirical process development. Studies are also under way in a large number of industrial organizations; again, these efforts are directed toward empirical processing techniques. Little (if any) of this research is directed toward basic understanding. It was agreed by all attendees that basic understanding is necessary before a real solution will be gained for the control of oxidation processes in IC fabrication.

To summarize the present state of this problem we quote a comment made at this discussion session:

> "We have fundamental laws for diffusion, but no fundamental laws for Q_{ss} prediction."

For this reason, it was suggested that a solution to this problem would probably arise from a combined effort between universit and industry. The industrial contribution represents valuable experimental data in conjunction with extensive experience. The university contribution would be directed toward a quantitative and qualitative theory for thermal oxidation.

A1.3 Ion Implantation

A discussion on ion implantation was presented by Dr. William Johnson (IBM); he offered a general outline of the field, discussed some significant problem areas, and probed some possibilities for solutions to today's problems. From Dr. Johnson's presentation it became immediately clear that great differences of opinion exist concerning the degree of predictability presently found in the ion implantation technique of doping semiconductor material. The ion implantation scientist believes the process is entirely predictable, whereas the device physicist disagrees. The reasons for this difference of opinion lie in the ultimate need for the predicted profile. The development of ion implantation techniques seldom involves questions of predictability at locations where the impurity atom density is two to three orders of magnitude below the peak density. In contrast, the device physicist is most concerned with this region of the implanted profile. Thus, from the device physicist's point of view, the predictability of an implanted profile is inadequate for device analysis.

In general, one can state that the implanted profile looks Gaussian, yet there are some important regions of deviation from this classical type of distribution. The deviation is usually encountered in the tail of the distribution where, in practical situations, a p-n junction would be formed. As a consequence, substantial error can arise in respect to the predicted location of an implanted junction.

Similarly, a lack of predictability in the tail of this distribution has important implications in the base region impurity distribution of bipolar transistors that contain ion implanted emitter junctions; this particular problem is most significant when implanting phosphorus ions for the emitter.

It was suggested that some of the present body of theory for ion implantation may not be adequate for our needs. Prof. Gibbons (Stanford) has done extensive research in this area, and finds a detailed calculation involves substantial computer time. Presently, there is need for further calculation on this problem and these calculations will be relatively expensive. Nonetheless, the calculations represent a one-shot situation; once completed, tables can be set up in a manual.

In addition, little information is available about the lateral profile from ion implantation. This profile could be of great importance in the design and fabrication of short-channel MOS structures. It was emphasized that the lateral profile may differ from the one presently under study. Calculations for the lateral profile should be undertaken in the near future, but at present the necessary skilled manpower is unavailable.

Despite the lack of predictability for an ion implanted impurity atom profile, the total ion dose (the integrated impurity atom density) is highly predictable. In fact, this quantity is far more predictable than is the quantity of

impurity atoms introduced by traditional chemical-vapor deposition techniques. For this reason, substantial agreement exists that in the foreseeable future ion-implantation might replace the pre-deposition technique presently used in a two-step diffusion process. Thereby, a greater degree of control will be gained over thermal diffusion.

One important problem arises in the utilization of this technique for device fabrication. Ion implantation introduces substantial lattice damage and, as a consequence, traditional thermal diffusion theory is no longer applicable. After having introduced impurity ions into silicon by ion implantation, there is no known analytical method whereby we can calculate the resulting profile after thermal diffusion. Therefore, there is presently substantial empiricism involved in any utilization of ion implantation for the pre-deposit step in thermal diffusion.

A further consequence of this lattice damage is encountered in the fabrication of ion implanted bipolar transistors--particularly ion implanted emitter junctions. In most situations lattice damage produces an exceedingly small emitter region minority carrier lifetime and, hence, an unreasonably low transistor current gain. Ion implanted emitter junctions produce a satisfactory current gain only after thermal diffusion, which moves these ions away from the region of damaged material.

It was frankly stated that ion implanted bipolar structures are unsatisfactory, except in a few rare cases. The

yield of good devices is low, and the need for excessive thermal diffusion produces unsatisfactory emitter junctions. For high frequency bipolar transistor fabrication, it was stated that traditional thermal diffusion techniques provide a significantly better emitter junction, resulting in higher gain and a steeper impurity atom gradient.

There was general agreement that ion implanted bipolar transistors represent a fabrication technique of the future, and that ion implanted MOS structures can now be made in a satisfactory fashion. Nevertheless, there are many problems associated with today's applications of ion implantation. These problems are presently being overcome by using empirical techniques rather than by gaining basic understanding.

A typical application of ion implantation requires that ions be implanted either through an oxide or in the near vicinity of an oxide. When ion implantation is accomplished through an oxide, a large quantity of oxygen is "knocked-off" and forced into the silicon. Typically, the oxygen content in silicon is estimated to be about 10% of the total implanted dose. The consequences of this mechanism are presently unknown. Basic studies will be necessary on this particular topic.

It was suggested that many areas of the ion implantation problem involve oxides used for semiconductor processing. It was also suggested that substantial advantage would be realized if the proposed research on oxides could be accomplished in coordination with the ion implantation research program.

Ion implantation appears to be less than a panacea for the semiconductor industry. For double-diffused MOS structures, ion implantation has proven to be of some value. Both TI and TRW are heavily engaged in the development of new applications for ion implantation, and they are encountering many difficult problems. Further, these companies (along with others) have developed techniques to overcome their particular problems, with little attempt to further advance our understanding of the subject. It is evident that fundamental research is needed in this particular area of the device fabrication technology.

Al.4 Thermal Diffusion

The subject of thermal diffusion prediction is familiar to most people in the semiconductor field. For this reason, no single individual was considered the workshop expert on this subject. Instead, a discussion on this topic was conducted on an open-forum basis, and the following represents a general summary of this discussion.

It is important to recognize that the technical literature contains a multitude of theoretical studies of this diffusion problem. Further, few of these studies have failed to show excellent agreement between theory and experiment, yet today we do not have a theory that actually works. The reasons for this situation were clearly stated by

R. Van Overstraetn: "There are too many unknown para meters." As a consequence, by adjusting these unknown parameters, excellent agreement is obtained between theory and experiment, regardless of the experiment used for evaluation. This situation has produced many theories that appear satisfactory, but which in reality are inadequate for process prediction.

In general, impurity atom diffusion in silicon is an exceedingly complicated process. Traditional theory of thermal diffusion is applicable to this problem, yet important modifications to this theory arise from the associated electrostatic charges. During diffusion, the impurity atoms are ionized, thus, they are undergoing random thermal motion in a sea of mobile holes and electrons. As a consequence impurity atom diffusion in a semiconductor is an ambipolar problem, and its solution will be obtained only by a relatively extensive computer calculation.

There are numerous views on the importance of the electric field that is produced by these mobile charges. Many of these views are based upon intuition rather than basic understanding. One attendee believed that the electric field would be most important in regions of the structure where the impurity atom density is small. In contrast with this view, at diffusion temperatures the intrinsic carrier density in silicon is approximately 10^{19} electrons/cm^3; for this reason, from a theoretical point of view little electric field could arise in regions where the impurity atom density

is less than about 10^{19} atoms/cm^3. Clearly, a detailed (and definitive) investigation should be conducted on this topic.

It was also stated that the electric field calculated from a quasi charge neutral approximation should be adequate for calculations of ambipolar diffusion. This may be true if we are only interested in situations where the impurity profile is attributed to quasi charge neutrality alone. Thermal diffusion from an ion implanted pre-deposition profile may involve large deviations from charge neutrality, and thereby result in an electric field that is far in excess of its quasi charge neutral magnitude. Again, we have a situation where detailed studies are required to attain a full understanding of the associated mechanisms.

In addition to traditional mechanisms of ambipolar diffusion, this theory must include the consequences of both Frenkel and Shottky defects in the semiconductor lattice. Lattice damage, ion-ion pairing, interaction between both donor and acceptor impurity ions, etc. must be included in the final solution of any problem involving impurity atom diffusion in silicon.

In addition to the mathematical theory of impurity atom diffusion, important questions arise about the boundary conditions of a diffusing species at the silicon surface. It is known that a SiO_2 layer forms at the silicon surface, and that this oxide contains a large impurity atom density; i.e., for boron diffusion, the oxide contains Boron trioxide. In addition, it has been found that boron forms a type of skin

at the semiconductor surface (believed to be SiB_4 or SiB_6), and that this skin is important when attempting to maintain solid solubility. Although these comments were made for boron, it is believed that similar mechanisms exist during phosphorus diffusion.

In conjunction with this discussion of impurity atom diffusion, particular emphasis was directed toward problems of measuring impurity atom profiles in silicon. It was suggested that solutions for this particular problem would be an important outcome of the NBS program.

A1.5 Epitaxial Growth of Silicon on Silicon

There was inadequate time available at this workshop to discuss in depth the problems of epitaxial growth. Nevertheless, from numerous comments by the workshop attendees it became evident that epitaxial growth of silicon on silicon is in the same state of development as other aspects of semiconductor IC processing. Namely, there is substantial industrial effort directed toward this problem, but little of the work is of a scientific nature. For example, industry is expending effort toward the development of epitaxial reactors in order to obtain a maximum of throughput but, unfortunately, most of this effort is empirical.

An important problem in epitaxial growth is the impurity atom profile resulting from a buried layer of impurities. Presently, there is no verified method for

predicting this profile. It is recognized that mechanisms other than thermal diffusion are associated with epitaxial growth; this is frequently called auto-doping.

At this time it is understood that Bell Labs. has a project under way on the topic of auto-doping. Although theoretical studies have yielded publications on this topic, we do not know where we stand on the problem. There is no indication that a workable theory is available for impurity profile prediction from a buried layer.

It was recommended by several attendees that an epitaxial equipment manufacturer should be contacted to undertake research on this topic. Further, it was specifically recommended that W. Benzing, Applied Materials Co., Santa Clara, Calif. was highly qualified in this area. Prof. J. Meindl (Stanford Univ.) volunteered to contact Dr. Benzing, and determine the possibility of a concrete proposal for research on the auto-doping problem.

Appendix II

WORKSHOP ON SEMICONDUCTOR DEVICE ANALYSIS

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Appendix II

Workshop on Semiconductor Device Analysis

A.2.0 Introduction

A summary is presented of opinions, comments, and technical information gained from the workshop on Semiconductor Device Analysis. This workshop was held at the University of Florida, Gainesville, Florida, on August 20-21, 1974.

Present at this meeting were the Steering Committee Members listed on page 5 and, in addition, the invited guests listed below:

Dr. G. Fossum	Sandia Corp., Albuquerque, N.M.
Dr. H. Gummel	Bell Labs., Murray Hill, N.J.
Dr. W. Lattin	Motorola Corp., Phoenix, Ariz.
Dr. A. Ruehli	IBM Corp., Yorktown Heights, N.Y.
Dr. C. Sah	Univ. of Ill., Dept. of E.E.
Dr. A. van der Ziel	Univ. of Minn., Dept. of E.E.

The purpose of this workshop was to evaluate our present capability to quantitatively describe the physical mechanisms of transistor operation that influence their terminal electrical characteristics. Where an inadequate capability exists, it was hoped this workshop could offer suggestions as to where present theory is either incomplete or incorrect. In addition, it was also within the scope of this workshop to discuss problems associated with the equivalent circuit representation of transistor structures for circuit design purposes.

The views of scientists and engineers engaged in this workshop were in general agreement on the crucial problem areas of bipolar transistor analysis. Principal differences of opinion arose concerning the basic cause of these problems. Some firmly believed they understood the source of some problem areas, although seldom were these problems believed solved. Others were doubtful about the accuracy of such views, yet had little to offer as possible alternate sources of the difficulty; in such cases it was suggested that inadequate knowledge was available on the subject.

It was often repeated by attendees that a need exists for further study of many problem areas. This opinion was unanimous on the transient (large signal and small signal) properties of transistors. Attendees recommended that techniques must be developed whereby a rigorous transient solution for transistor operation can be accomplished by computer. This computer program was not viewed as a design tool for transistors but, instead, a means to study and understand the associated mechanisms of transistor operation. Such understanding is not presently available.

A2.1 Bipolar Transistor Analysis

A discussion on our present knowledge (and modeling capabilities) for bipolar transistors was presented by D.P. Kennedy, Univ. of Florida. It was suggested that a large class of steady-state electrical characteristics for bipolar transistors can be calculated with an accuracy that is

adequate for engineering purposes. For this reason, it is believed that little additional research is required in this area--although it was stated that this belief is based upon inference, rather than exact knowledge.

The reason for the absence of exact information arises from our present inability to make accurate device measurements. Accurate impurity atom profile measurements cannot presently be made for bipolar transistors. Similarly, we cannot measure the base width of a bipolar transistor with the accuracy needed for detailed comparisons between theory and experiment. For this reason, the adequacy of our existing theory must be deduced on a statistical basis, using thousands of bipolar transistor measurements.

It should be emphasized that the foregoing remarks are limited to the forward-active mode of operation. Scant information is available on the saturation mode of bipolar transistor operation. We suspect that the saturation mode will offer few problems for our steady-state calculations, although this point requires further investigation.

In contrast with these steady-state computational capabilities, similar capabilities do not exist for the current gain and transient characteristics of bipolar transistors. Today, we cannot calculate the magnitude of current gain expected from a bipolar transistor. In our mathematical models we simply adjust the assumed minority carrier lifetime to obtain agreement between experiment and theory. Similarly, f_t

calculations based upon existing theoretical knowledge yields results that are a factor two or three greater than its experimentally measured value.

It was suggested that for both current gain and transient response (large signal and small signal), existing models may not contain the appropriate physical mechanisms.

It is generally agreed that the current gain of bipolar transistors is limited by the emitter injection efficiency. For this reason, substantial research has been directed toward understanding the consequences of high doping in the emitter region, and toward analysis of the influence of this high doping upon the emitter injection efficiency. Much of this work has been under the direction of R. Van Overstraeten (a Steering Committee member). He has proposed that wave function overlap between ionized impurities modifies the density of states within the emitter region. A predicted consequence of this mechanism is a modification of the emitter region "built-in" electric field and, hence, a reduction in emitter injection efficiency.

Similar problems are associated with the transient response of bipolar transistors. Most rigorous investigations of this topic have been done on a one-dimensional basis and, therefore, may be incomplete. This concept was reinforced by a recent paper on this topic by Prof. Engl (Aachen, W. Germany), who has undertaken a two-dimensional transient solution of bipolar transistor operation. Prof. Engl has shown substantial

proof that both one-dimensional and two-dimensional mechanisms contribute heavily to the transient switching properties of this semiconductor device. To date, the details of these mechanisms are not fully understood.

During this discussion, questions arose concerning the validity of Prof. Engl's mathematical methods. It was suggested that this method may not yield the true transient response. Nonetheless, it was generally agreed that further work is necessary in the area of transient analysis. To reduce the required computer time, this work should initially be undertaken by mathematicians and numerical analysts. Thereafter, the resulting computer programs should be used to study the physical mechanisms encountered during transistor switching.

An additional discussion on the high-doping effects in an emitter region was presented by R. Van Overstraeten. He stated that rigorous calculations have been undertaken to evaluate the consequences of high doping on a one-dimensional bases. These calculations show satisfactory agreement with experiment for the following electrical characteristics:

1. magnitude of the current gain (β)
2. the temperature dependence of β
3. prediction of f_t
4. capacity of emitter junction
5. current dependence of f_t
6. current dependence of β
7. difference between double-diffused and double implanted devices

After stating such far-reaching agreement between experiment and theory, Prof. Van Overstraeten cautioned that the theory was not mature, and required further research.

Next, Prof. Van Overstraeten outlined some important limitations of this theory that must be studied. He stated that his work is actually based upon several high doping studies for deep impurities in GaAs. These results were thereafter extrapolated to obtain the degree of band splitting expected for shallow impurities; this extrapolation, he said, may not be valid. In addition, an extrapolation is made from very high impurity atom densities to those normally used in semiconductor material. Again, the extrapolation may be invalid. In addition, he stated that, in his view, recombination was not a significant source of β reduction. This point was questioned by a workshop attendee and Prof. Van Overstraeten's view was restated - the lifetime is not overly important.

Thereafter, a discussion was presented by G. Fossum (Sandia), giving his views of the bipolar transistor problem. He emphasized the need to have mathematical models for the physical mechanisms involved in bipolar transistor operation. From these mathematical models, he suggested that adequate quantitative information could be obtained to formulate the parametric information needed for their equivalent circuit representation. Thereby, a system of models of this type would provide an ability to relate the device fabrication process to the resulting electrical characteristics of an IC.

Dr. Fossum also emphasized a need to have accurate material parameter data: mobilities, lifetime of minority carriers, etc. He also emphasized the necessity for studying the consequences of material processing upon these basic parameters.

Next Dr. Fossum discussed problems with the state of our understanding of the physics of bipolar transistor operation. He emphasized a need to further develop this understanding, particularly with regard to multi-dimensional mechanisms. To his knowledge, important problems such as high-current transistor operation have only been studied on a one-dimensional basis. He believes this approach is a serious mistake. In addition, he suggested that our low current studies are inadequate; the low-current mode of operation involves mechanisms such as space-charge layer recombination, surface recombination, etc.

After the informal presentations by Prof. D.P. Kennedy, Prof. R. Van Overstraeten, and Dr. G. Fossum, a general discussion took place between workshop attendees on the topic of bipolar transistors. This discussion offered a general summary of the state-of-the-art in bipolar transistor modeling, and of our present knowledge of some physical mechanisms involved in the operation of this semiconductor device.

It was generally agreed by all attendees that any modeling effort for bipolar transistor operation should be

accomplished at several levels of complexity. This situation is a direct consequence of economic considerations--the more complex the mathematical model, the more expensive it is to use on a computer. Nonetheless, despite excessive computer costs it was generally agreed that mathematical models of the most complex type must be developed: these are two-dimensional transient solutions for this semiconductor device.

It was suggested that for engineering purposes we might be restricted to one-dimensional and pseudo two-dimensional mathematical models. This restriction arises from the necessity of making a large number of computer runs during transistor design; the more complex models may prove too expensive for this purpose.

After this discussion of the basic transistor model problem, other discussions took place on the characterization of fundamental physical parameters of the semiconductor material. A parameter of particular interest is the minority carrier lifetime. Great emphasis was placed upon the research of Dr. C.T. Sah (an attendee at this workshop) concerning the defect centers produced by impurity ions, and the influence of these defects upon the minority carrier lifetime. There was general agreement that this subject is of great importance, although only limited information is available that is of direct value to our program.

An additional problem in this area is the influence of IC processing upon these basic semiconductor parameters. It

was agreed that for practical reasons we must neglect the consequences of processing. Furthermore, it was frankly stated that if there is an attempt in this research to predict the minority carrier lifetime in a semiconductor device, we are probably "off-base."

A presentation was next given by Prof. F.A. Lindholm (a Steering Committee Member) on the equivalent circuits used to represent transistors during circuit design. He admitted that the study of these equivalent circuit representations has been underway for many years (since about 1954), yet the associated problems have not been solved. Thereafter, he directed his presentation toward an exposition of the basic complexity of this problem, and the accepted methods (both good and bad) for its solution.

It was emphasized that the goal of equivalent circuit research is to attain an elementary network that describes all the important physical mechanisms of transistor operation. Clearly, this is a difficult problem, since an equation describing these transistor mechanisms involves three-dimensional boundary value problems. Further, we can generally state that these three-dimensional boundary value problems cannot be solved by analytical methods. Such a solution is necessary to obtain the parametric interdependence for an equivalent circuit.

For this reason, workers have tended toward simplifications that take many forms. An important simplification is

to reduce the dimensions of the problem at hand. That is, we assume no important mechanisms take place in a given dimension within a given transistor; thereby, we can reduce a complex three-dimensional boundary value problem to a two-dimensional boundary value problem.

Following the procedure of model simplification, we tend to introduce approximations upon approximations. Clearly, to assume that no important mechanisms take place in a given spatial direction is a simplifying approximation--it may, or may not, be in accord with the physical facts. Thereafter, having reduced a 3-D boundary problem to a 2-D boundary problem, we simplify the 2-D problem by breaking it up into coupled (and sometimes uncoupled) 1-D problems. For example, the 2-D model for a bipolar transistor is subdivided into an extrinsic and an intrinsic region, and these two regions are assumed to be almost independent of each other.

Thereby, we have simplified the model of a bipolar transistor to a form used today in semiconductor circuit design. Detailed study is directed toward a one-dimensional analysis of the intrinsic transistor region, and toward its representation in an equivalent circuit. Little attention has been given to extrinsic region. Typical of this approach are the following equivalent circuits for bipolar transistors:

Ebers-Moll Model (1954)
Beufoy-Sparks Model (1957)
Linvill Lumped Model (1958)
Modified Ebers Moll (1960-on)
Gummel-Poon Model (1970)
Fossum Expandable Model (1973)

Today, the modified Ebers-Moll model is most often used throughout the semiconductor industry.

Prof. Lindholm's next point of emphasis was that despite apparent differences between these various models, these differences are not real. In fact, it has been shown that these models are all the same in network configuration, and that they are all representable in the form of the Ebers-Moll model. The differences among these models arise in the device physics used to express the functional dependencies of the circuit elements.

Further, an inherent weakness is found in all of these models: their ability to approximate the transient response of a bipolar transistor. In all equivalent circuit development, a quasi-static approximation is made to characterize the transient response. In this quasi-static approximation we assume the transistor switches from one steady-state mode to another at an infinite rate. Clearly, this over-simplification could be totally inadequate in many practical situations.

From this outline, in conjunction with the previous discussion, it becomes evident that extensive research is needed in this area of equivalent circuit development. Clearly, the entire job cannot be completed until more understanding is available on the physical mechanisms associated with transistor operation. Nevertheless, much can be done with regard to

modeling the physical mechanisms we presently understand. For example, a careful evaluation is needed to determine the validity of our quasi steady-state approximation. It is not presently proven that the switching properties of a transistor can be derived from its steady-state properties.

A final point of emphasis was the necessity to develop these equivalent circuit models from the basic physical mechanisms of device operation. The bipolar transistor is an exceedingly complex structure, and there is substantial interrelation between its electrical parameters. If, indeed, the parametric yield of an IC manufacturing line is poor, there is little hope of quickly identifying the difficulty if the device equivalent circuits are not based upon basic physical mechanisms.

A general discussion took place concerning the validity and applicability of existing equivalent circuit representations for bipolar transistor operation. Many questions were directed toward Dr. Gummel, since he has wide experience in this field. He agreed that the quasi steady-state approach was based upon the correct electrostatic charges in a transistor, although questions must be asked about how fast these changes move in and out of each region of the device. In Dr. Gummel's opinion, the simple approximations we presently use are of questionable applicability in a frequency domain type of analysis, although they are less questionable in the

switching domain.

Further comment was directed toward the reduction of dimensions approximation. It is not always correct to reduce the assumed dimensions of a transistor, yet it is not always wrong. In each individual application it is necessary to evaluate the situation, and to establish whether or not it is reasonable to apply this approximation. The applicability is most often dependent upon the particular transistor under consideration. For example, as we reduce the size of a transistor, the mechanism of emitter crowding is essentially eliminated. In contrast with this situation, a reduction in size often changes the aspect ratio and, hence, makes sidewall effects more important.

Substantial attention was given to practical difficulties inherent in utilizing these more complex mathematical models in the computer analysis of IC structures. Most of these complex solutions cannot be used in the design of an IC because of their complexity--they cannot fit into the computer. The need for using simplified approximations is obvious, but the shortcomings of these approximations could represent a serious problem. Furthermore, in most real engineering situations one cannot adequately guess about the validity of one model simplification against another.

It was again suggested that this particular problem area represents an important application of the rigorous, although slow speed, mathematical models for transistor operation.

With these rigorous solutions we can remove the guess work, and can establish the general validity of our approximate models.

An important point was raised by Dr. Gummel concerning an approximation that is presently made and which could lead to trouble in the near future. In our present theory of device operation we consider the impurity atom distribution a continuum. As our devices have gotten smaller and smaller, the validity of this approximation comes more into question; at some point our impurity distribution can no longer be considered a profile. Instead, within the crystal we have big potential columns with little (or nothing) in between--where electrons wander freely.

In spite of this situation our theory works. Our continuous differential equations describe semiconductor characteristics fairly well. But if we continue in this direction--we continue to make devices smaller in all dimensions--we will have to be careful. Eventually, our scattering mean free path will become comparable to our base width. At this stage we could be in serious trouble.

This statement by Dr. Gummel reflects the opinion of numerous others in the field of device analysis. Studies of this problem are presently under way at the University of Florida, for both the bipolar transistor and the MOSFET. Further, it was stated that the results of initial studies of this topic would soon be submitted for publication.

Dr. Gummel raised another point concerning the temperature characteristics of bipolar transistors. For purposes of example, he stated that experimental measurements are made of current gain (β) vs. emitter current. In some of these measurements it is known that we are getting local heating. Despite this knowledge, none of our theoretical efforts are directed toward taking into consideration the consequences of temperature upon current gain. It was suggested that in such situations, the current gain should be measured on a pulse basis--but researchers have never performed the experiment in this fashion. In Dr. Gummel's opinion, precision modeling of the bipolar transistor will eventually require taking the consequence of temperature into account.

Thereafter, Dr. Gummel presented some general views of the modeling problem and its practical value to engineers. He believes that mathematical models for device operation represent an important diagnostic tool for IC fabrication. In this application, such a model provides a necessary link between the device characteristics and the fabrication process. In addition, these mathematical models provide crucial insight into device mechanisms, which are valuable for many other reasons; therefore, we must, for instance, learn to predict f_t accurately.

Nonetheless, for logic circuits another question must be raised. Namely, the device area decreases approximately as the square of its dimensions, whereas the routing decreases approximately linearly. This situation implies that the para-

sitic loading will remain large. With a decrease of device size, the wiring will determine f_t. For this reason we may not need to accurately predict f_t for structures of the future, due to this parasitic problem.

A2.2 MOSFET Analysis

A session on MOSFET Analysis was held during this workshop, and a kick-off discussion was presented by Prof. D.P. Kennedy. The principal emphasis of his presentation was directed toward outlining work under way at Univ. of Florida on the theory of MOSFET operation. Because this work is based upon the use of a 2-D computer solution of the problem, many technical details were discussed. It was recognized by all attendees that the work now under way at U. of F. is totally consistent with previously proposed applications of similar computer programs for bipolar transistors.

The mathematical basis for this forementioned computer program is the traditional steady-state ambipolar diffusion equations of Van Roosbroek. Although this particular program is new, a similar computer program was developed by Prof. Kennedy when he was associated with IBM. For this reason, extensive experience is available concerning the agreement between this two-dimensional theory and measurements taken on laboratory devices.

Many copies of a previously developed computer program have been used at IBM by engineers engaged in device develop-

ment. It is concluded that within our present knowledge of FET theory, satisfactory agreement is obtained with experiment. This theory extends from very short channel structures to very long channel structures. Furthermore, for all ranges of channel length, adequate agreement is obtained from very strong inversion to very weak inversion. In short, this agreement is sufficient to assume the two-dimensional model is correct, within a framework of the appropriate physical mechanisms. For this reason, all development of simple engineering models at U. of F. is based upon a standard, represented by the two-dimensional computer solutions of this problem.

In addition, use of this computer program provides a means for evaluating physical mechanisms associated with MOSFET operation. In short, it is no longer necessary to guess about the physical mechanisms of operation; this computer program is used to quickly gain required understanding.

From this point, a discussion was presented on some physical mechanisms of MOSFET operation that are not considered in our present theory of this structure. These physical mechanisms were drawn from rigorous two-dimensional calculations, and they contradict many accepted concepts. A consequence of this situation was an extensive technical discussion on the details of MOSFET operation, since many attendees have published papers on this topic. In short, these calculations show important areas of MOSFET operation where some attendees' publications are incomplete. Although this presentation produced a heated technical discussion, it also

had other advantages. It was clearly shown that there are important things to be learned, (and insights to be gained) by a multi-dimensional analysis of semiconductor devices.

Included in this discussion was an outline of the mechanisms not presently modeled in the two-dimensional computer program. For example, hot-electron mechanisms are not considered in a rigorous fashion. Furthermore, the variation of channel mobility with gate voltage is not modeled in this analysis, although such work is presently under way at the University of Florida. It was generally recognized by all attendees at this workshop that despite the absence of these second-order mechanisms, this particular computer program would be exceedingly valuable for device design and engineering.

A discussion was also presented on quantum mechanical mechanisms present in the inversion layer of an MOSFET. Furthermore, it was shown that these quantum mechanical mechanisms have been experimentally observed, and that they may be the next crucial step in the development of this two-dimensional computer program. A quantum mechanical solution for the inversion layer carrier distribution is being developed at the University of Florida. After completion of this work it is planned to introduce this solution into the fundamental equations used in our two-dimensional computer program.

The presentation by D.P. Kennedy concluded with a general discussion session on the topic of MOSFET modeling. An important point was raised by W. Lattin co cerning the

reproducibility of MOSFET structures from a fabrication point of view. He explained that many unknown factors are involved in this reproducibility problem, and that there is a significant need for a theoretical study of this topic. For example, he stated that both long-channel and short-channel MOSFET structures are sometimes placed upon the same slice. When this experiment is performed, the results are very confusing; there is sometimes little correlation between device characteristics and channel length.

D.P. Kennedy had direct knowledge of this reproducibility problem, yet little experience in its solution. Nevertheless, it was stated that IBM at Burlington has been studying the problem using computational techniques he previously developed for a similar problem in bipolar transistor fabrication. Specifically, a random number generator was used to simulate the process parameter variabilities occuring during device fabrication. Thereafter, conventional Monte Carlo methods of analysis were used in mathematical models of the MOSFET to show the relative importance of each process parameter upon particular electrical parameters. Thereby, they were able to establish the process parameters producing a particular type of reproducibility problem.

Another point raised during this discussion session was the need to extend our computational abilities to a three-dimensional model. Some attendees believed the two-dimensional model was adequate, while others believed a three-

dimensional model could be needed. This question was resolved by recognizing that the two-dimensional model will be adequate for most practical situations. Furthermore, our need for a three-dimensional model is based upon guesswork, and not upon proven fact. After the two-dimensional mathematical model is widely available, we can try it for these questionable situations. If, indeed, the two-dimensional model does not agree with experiment, we should evaluate the necessity of extending our analysis to three spatial dimensions.

The next discussion was presented by Prof. C.T. Sah on some topics he believed would be important to future development of the MOSFET. In his opinion, it appears that short-channel (and very short-channel) structures will be very important in the future. As a consequence, he emphasized the importance of hot-electron mechanisms in an inversion layer, and restricted his comments to hot electron mechanisms in a direction parallel to the oxide-semiconductor interface. Another point of emphasis was the fast surface-state charge and discharge time. Again, this is a mechanism that would be most significant to a short-channel structure, where the high frequency properties of the structure are of great importance.

There was one exception to this situation. Prof. Sah discussed a problem he believed to be important for weak

inversion--the patch effect believed to exist in the interface surface charge. He placed emphasis upon his belief that a patchwork of surface charge at the oxide and semiconductor interface would tend to turn the inversion layer into a similar patchwork--one that contains regions of large surface inversion charge. The conductivity of a weakly inverted channel would be like islands of high conductivity. He linked this situation to that encountered in an amorphous semiconductor and, therefore, he believes there is presently some theoretical understanding of the problem. Little was stated about how, and in what way, this problem would become important from the point of view of a device designer.

For the short-channel device, he proposed that hot electron mechanisms could produce a fundamental limitation in the frequency response. Prof. Sah suggested that a little-known phenomenon in semiconductor materials is the energy relaxation time, which can be longer than the well-known momentum relaxation time. For purposes of comparison, the momentum relaxation time is about 10^{-12} to 10^{-13} sec., whereas the energy relaxation time is about 10^{-9} to 10^{-10} sec. This energy relaxation time is of the same order as the switching times of typical short-channel devices; hence, it could be a source of difficulty.

The question was raised by Prof. Lindholm if this mechanism could now be influencing the maximum operating

frequency of short-channel MOSFET transistors. Prof. Sah had no answer to this question--although the possibility does, indeed, exist. We may (or may not) have encountered this mechanism in some of our very high-speed MOSFET structures, without recognizing it as a fundamental source of difficulty. Nevertheless, in his mind this problem is real, and it is only a matter of time before it will be encountered in MOS operation. Research on the topic should get under way as soon as possible.

Prof. Sah placed emphasis upon the need to incorporate a working model of interface surface-state trapping into all computer programs for MOSFET analysis. He believes this mechanism alone could produce a fundamental limitation upon the speed at which an MOSFET can be turned on. From his comments there is little indication that there is any quantitative information on this problem, as applied to the MOSFET. Nonetheless, his comments are based upon laboratory measurements undertaken at the University of Illinois.

A side issue was raised during his discussion concerned the interface scattering mechanism in an MOSFET: this scattering limits the mobility of carriers within an inversion layer. He stated that his measurements indicate that surface scattering results from a boundary region that is approximately 5 Å (or about one lattice constant) wide, in an inversion layer that is 30 to 50 Å wide at room temperature. A later discussion with Prof. Sah on this topic indicated that his

estimate of the inversion layer thickness was based upon the work of F. Stern (IBM).

A presentation was next given by Dr. W. Lattin from Motorola. His stated intent was to present the research he saw necessary from an industrial point of view. During his introductory remarks he clearly stated that there are some problems industry could solve on its own, and there was little need for universities to become involved. He also stated that there are other problems that industry will not solve, yet they do need a solution; in short, industry will find empirical ways around such problems, rather than solve them. Much of his emphasis was placed upon problems arising in MOSFET circuit design and those arising in the modeling of active devices. After his introductory statements, he elaborated upon each problem separately.

Dr. Lattin reinforced earlier statements concerning the importance of understanding physical mechanisms associated with the mobility of carriers in an inversion layer. He stated that this mechanism places important limitation upon IC circuit design. For example, at small values of gate voltage this mobility appears to be about one-half its value in bulk silicon. At large value of gate voltage the inversion layer mobility undergoes another reduction of about one-half, reducing the total mobility to about one-quarter its value

in bulk material. From Dr. Lattin's point of view, we must develop a physical understanding of this problem and, in addition, we must have accurate models for the reduction of channel mobility with gate voltage. Industry presently uses a heuristic mathematical representation for this phenomenon; this heuristic representation is fitted to each individual experimental situation.

A point raised in this presentation was the need for three-dimensional mathematical models for MOSFET operation. It is not presently known whether this particular need is unique at Motorola, or if this need is widespread in the semiconductor industry. Nevertheless, Dr. Lattin stated that a technique used to conserve real-estate in an IC design is to introduce odd shaped IC structures (when viewed on their horizontal plane). Thereby, structures that are normally representable in two spatial dimensions become well defined three-dimensional structures. Little (or no) study has been directed toward understanding the consequences of such a practice, yet experiment shows that each structure differs from its two-dimensional counterpart.

He emphasized the need for a detailed understanding of the weak inversion problem, and a method for modeling this mode of MOSFET operation. Motorola is presently designing MOSFET structures that operate with approximately 5.0 volts on the gate electrode; these devices exhibit a threshold of about 0.6 to 1.0 volt. As a consequence, during circuit

operation a small residual voltage on the gate electrode can produce a comparitively large source-drain electric current (in the order of 10's of μa). This particular problem introduces great difficulties in the design of CMOS and n-channel structures.

Dr. Lattin next discussed the need for a detailed model for mechanisms producing a substrate electric current during MOSFET operation. He explained that most IC manufacturers use a substrate bias in their circuit designs, and it is believed that power supplies used for this purpose are required to handle a negligible electric current. In fact, a careful look at the situation shows these power supplies must handle a substantial electric current, since the substrate of an MOSFET involves many complex physical mechanisms. Dr. Lattin attributed some of the observed substrate current to the mechanism of impact ionization within the drain junction space-charge layer. He claimed that no mathematical model was presently available whereby this impact ionization current could be quantitatively established.

Note: Recent discussions with Dr. Lattin on this subject further emphasized the importance of this situation. It is now recognized that impact ionization represents only a minor source of this substrate electric current. Measurements show a substantial transient current in the substrate power supply; this current is tentatively attributed to capacitance

mechanisms that come into play during turn-on and turn-off. The total substrate electric current is relatively small for an individual MOSFET. If, instead, one monitors the substrate electric current for an entire IC chip, the transient current can become very large. By extrapolating this situation to future IC structures (with the packing densities now predicted by the semiconductor industry), it appears reasonable to expect a future substrate bias supply transient current in the order of 0.5 Amps.

Having published papers on the topic, Dr. Lattin believes that a detailed knowledge should be gained about the consequences of impact ionization on MOSFET operation. He needs information on the path of all secondary electric current in a MOSFET, due to impact ionization mechanisms; this would enable him to calculate the resulting substrate voltage distribution. Recognizing that this problem is two-dimensional in nature, he was assured by Prof. Kennedy that in the future, when the present two-dimensional program is in good shape, he will have this capability. Calculations of impact ionization in a semiconductor device represent a relatively straightforward computation. Furthermore, the results of such calculations should be in good agreement with experiment.

Next, Dr. Lattin commented upon the available equivalent circuit representations for a MOSFET. He frankly stated that there is a great emphasis upon the development of these equiva-

lent circuits, yet there is too little emphasis upon their practical applicability. A problem of great concern is the convergence of these equivalent circuits in computer programs used for circuit design. A given equivalent circuit representation yields excellent (fast) convergence during circuit analysis of one type logic configuration, and very poor (slow) convergence for another type logic configuration. In fact, it is not uncommon to encounter instabilities during circuit design; this usually implies a need for serious modifications of the equivalent circuit.

A discussion previously presented by Prof. Sah was reinforced by Dr. Lattin; he offered his opinion concerning the charging and discharging of surface states at the semiconductor and oxide interface. Unlike the previous view of this topic, Dr. Lattin believes this problem is of current importance and that a model for this mechanism, if available, would be put into immediate use. He stated that our present lack of understanding has necessitated taking a heuristic approach: a capacitor is used in equivalent circuits to approximate this physical mechanism, based upon laboratory measurements. Each new device requires a new series of measurements.

Dr. Lattin also reinforced the accuracy of a conclusion from the workshop on Process Modeling and Prediction. He stated a need for detailed understanding concerning the impurity atom distribution arising from ion implantation through an oxide insulator. Presently Motor[illegible] used this technique

for threshold adjustment in an MOSFET, and from necessity this is accomplished by empirical experimentation. In addition, he suggested the possibility of an increase of surface-states during this radiation process, although this comment was based upon little (or no) factual data.

His next topic was directed toward a problem heretofore not mentioned by other scientists at this or previous workshops. He stated that an area of needed research is the electrostatic breakdown of oxides, and protection techniques whereby the damage from inadvertent electrostatic charges can be eliminated. He recognizes that this problem is relatively unglamorous, from the device physicists's point of view, nevertheless it is an ever-increasing problem in the semiconductor industry.

Dr. Lattin ended his discussion by restating his belief that the equivalent circuit problem is one of extreme importance. A detailed study is necessary to obtain equivalent circuits that adequately represent the MOSFET. This need for a rigorous model of physical mechanisms is contradictory to the need for model simplicity--and there is no immediate answer to the problem. An accurate network representation of these physical mechanisms is worthless if the equivalent circuit is too large, or it will not converge when used during circuit design.

A2.3 General Discussion Session

After completion of Dr. Lattin's presentation, a general

discussion was encouraged by all attendees at this workshop. The purpose of this discussion was to solicit comments, criticisms, and additions to the presentations given on the topic of MOSFET modeling. This discussion period did, indeed prove valuable. Areas of agreement and disagreement among the attendees became evident and a few new (and important) points were raised. It became evident that each attendee placed a different degree of importance on points raised during the previous presentations, and that their opinion were weighted by the problems each individual faces on a daily basis. For example, scientists involved in IC design and development placed greatest importance upon short-term problems that are of immediate concern, whereas university people took a long-range view of the situation.

It was generally agreed that an important source of today's difficulties arises from the fact that we do not know in quantitative terms the present state-of-the-art. There are numerous theories for device operation that are based upon simplifying approximations and assumptions, yet little information is available on the range of validity and applicability of this theoretical work. This situation has produced an extensive amount of empiricism in the field of device design, since the semiconductor industry has inadequate time and manpower to undertake the task of evaluation. It was also recognized that there are fundamental difficulties associated with undertaking such a program of evaluation.

Similar remarks were directed toward the available equivalent circuit representations for semiconductor devices. A need for simplifying these equivalent circuits is obvious from the circuit designer's point of view; these equivalent circuits can easily approach the complexity of any circuit to be analyzed. For this reason, guidelines are necessary to establish conditions under which one can use each level of equivalent circuit complexity. It was emphasized that an immediate contribution would be the establishment of such guidelines and the distribution of such information to the semiconductor industry.

This aspect of the problem was summarized as a stated need for publications that provide quantitative evaluations of the state-of-the-art on device modeling. This publication could be a book on the subject that is readily available to the public. Prof. Lindholm openly stated his interest in becoming involved in the writing of such a book, possibly contributing that part dealing with equivalent circuits for active devices. With this in mind, he voiced concern about the availability of necessary information from industry. In reply to his concern, it was stated that such information would not be readily available. Nonetheless, if such a publication was made available on topics presently in the open literature, it would represent a real service. After industry realizes the value of this type work, they will be less reluctant to offer their own knowledge of the subject--possibly for a

second edition.

A point of general agreement was the necessity to develop mathematical models for device operation that are rigorous from a physical and mathematical point of view. For the MOSFET this model should be multi-dimensional. A first goal toward its development should be for a steady-state solution and, later, for a transient solution. It was recognized that such a computational tool would probably not be useful for general device design. Instead, its availability would provide a means to develop and evaluate more elementary models that will be used by the working device engineer.

The need for this capability was reinforced by W. J. Kitchen (NSA), through his views of the present techniques for MOSFET IC design. In short, he believes there is no available way to evaluate the models now in use and, as a consequence, these models have evolved into patchwork upon patchwork. Each time the existing model is found not to agree with experiment, a new "band-aid" is added. From his observations, the semiconductor industry has been using this technique for the last 20 years. The only saving part of the situation is that these models now have enough adjustable constants so that they can be used to fit anything.

A closing comment on this topic by Prof. A. van der Ziel was a warning about making these models too complicated. In his experience, he finds that relatively simple models are

often adequate and that complex models sometimes lead to trouble. Namely, complex models frequently have more adjustable constants than observables and, as a consequence, the models can be made to fit any experimental observation. This problem was previously stated by W. I. Kitchen.

A2.4 Miscellaneous Comments by Workshop Attendees

A final "wrap-up" discussion was held on topics relevant to this workshop on devices and their equivalent circuits. Little new information was gained except on one point that was not covered in this workshop: the interaction and communication between device physicists, equivalent circuit designers, and circuit analysis engineers. It became evident that a serious problem exists in any interaction between these specialists. Each individual has opinions concerning problems associated with his particular field of specialization, and is frequently reluctant to compromise (or yield) in order to simplify problems arising in the other's area.

Particular emphasis was placed upon the need for extreme simplicity in equivalent circuit models used in existing computer programs for circuit design and analysis: SPICE, SEPTR, ASTAP, etc. Each of these computer programs has its own characteristics, with regard to acceptable equivalent circuit models for active devices. An equivalent circuit that adequately converges in one circuit analysis program may not converge in another. An additional complication arises because an equivalent circuit that works for the analysis of one logic

circuit configuration may not for another configuration--using the same circuit analysis program. Clearly, this problem must be addressed in the development of equivalent circuits for active semiconductor devices.

It was stated by Prof. Lindholm that a program of research should be initiated toward an understanding of this equivalent circuit tolerance problem. Furthermore, he voiced his interest in this problem as a topic for investigation. Attendee recommendations for this effort were directed toward the development of standards for the equivalent circuits to be used in circuit design programs, and for the design of equivalent circuits that will operate in any presently available computer program for IC design.

Dr. W. Lattin (Motorola) raised a point of concern that is recognized throughout the entire semiconductor industry--he calls it the data acquisition problem. Most IC manufacturers have developed extensive data acquisition capabilities. They are gathering large quantities of data, yet they do not know what to do with it. He voiced an opinion that research is needed on electrical measurements that can be made, using test sites, to obtain insight into fundamental device properties. Furthermore, he offered the facilities of Motorola for a program of study on this topic.

At that time Dr. Lattin was informed of a planned cooperative effort between NBS and University of Florida on that particular topic. The general plan of this effort is to under-

take both mathematical and experimental studies of testsites for IC process monitoring. Further details of this research will be available in the future, and Motorola's participation in this effort could represent a valuable contribution.

APPENDIX III

Workshop on Test-Sites

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Appendix III

Workshop on Test-Sites

A3.0 Introduction

On Sept. 6, 1974, a one-day workshop on IC manufacturing test-sites was held at the Camelback Inn, Scottsdale, Arizona by the National Bureau of Standards. This aspect of the IC problem represents an important part of both the NBS/ARPA program and the Univ. of Fla./ARPA program; therefore, all Steering Committee members attended this workshop. Thereby, without duplication of the NBS effort, workshop members gained insight into this problem and, in addition, insight into specific areas where additional research would be appropriate and valuable.

This workshop was organized as a formal scientific meeting and, therefore, only limited speaker-audience interaction was possible. Nevertheless, in the time available this type of meeting organization offered a greater number of speakers than at the previous Univ. of Fla. workshops. As a consequence, there was a greater diversification of topics discussed. These speakers were drawn from a large segment of the semiconductor industry. Oral papers were presented on topics ranging from the most scientific approach to this test-site problem to an entirely heuristic approach to their development.

In retrospect, a workshop on IC fabrication test-sites would be of only limited value if organized under rules first

set down for the Univ. of Fla. study program: selection of about six recognized experts in the field. This entire topic (manufacturing test-sites) is considered highly proprietary in the semiconductor industry. As a consequence, there are few acknowledged experts in this field. Furthermore, it was not known whether one semiconductor IC manufacturer had greater knowledge in this area than another semiconductor IC manufacturer. For this reason, greater insight was gained by inviting speakers from a wide segment of the semiconductor industry, and offering a platform for many to discuss those aspects of the problem they believed to be non-proprietary. Thereby, it became easy to "read-between-the-lines" and determine the level and quality of effort on this topic that is now underway.

After this one-day workshop all Steering Committee members attended a one-half day discussion session on this topic. In addition to the NBS representative on our Steering Committee (Dr. M. Bullis), Dr. M. Beuler (NBS) was present at this discussion session; he is actively involved in this problem at the NBS Labs. The purpose of this session was to evaluate and discuss particular aspects of the test-site problem and, in addition, establish the framework for a cooperative NBS/Univ. of Fla. program of research on this topic.

A3.1 Summary of Steering Committee Meeting

It was generally agreed by all attendees that the speakers at this workshop indicated a substantial level of effort was underway in this area by a wide segment of the semiconductor industry. Furthermore, the quality of each presentation indicated the importance industry is placing on obtaining solutions for this problem. Each speaker demonstrated a high level of knowledge about test-sites, and a level of technical excellence seldom encountered at such meetings. It was indeed obvious that the semiconductor industry places substantial reliance upon test-site evaluations for process control, but from the point of view of a large-volume IC manufacturer. Their principal interest in test-site evaluation is directed toward identifying inadvertent changes in a given manufacturing line, and little emphasis is placed upon linking these measurements to specific process parameters.

This is not intended to imply that industry is not interested in linking test-site measurements to specific parameters. In conversations with one Steering Committee member, it was pointed out that two (or more) speakers stated that they do not know how to solve the problem. Clearly, each test-site measurement is influenced to a greater or lesser degree by several process parameters. It was stated by these speakers that they do not know how to separate the "signal" from the "noise".

Because NBS has extensive experience working with the semiconductor industry, their views of this problem are of

particular interest. As stated by Dr. M. Bullis (NBS), the problem is exceedingly complex from both a technical point of view and a people point of view. A balance must be attained between what is technically reasonable and what is acceptable to the technical community. It is indeed obvious that a technically ideal test-site would be totally unacceptable if it was too complicated or, instead, it used too much wafer real estate. For this reason, test-site design and development must be accomplished in close cooperation with the intended users.

In addition, Dr. Bullis stated that the NBS program is not necessarily directed toward an interpretation of test-site structures now used by industry. These structures are directed toward evaluating device parameters (for example) that have direct influence upon IC operation; not the critical process parameters. It is evident that critical process parameters require measurements, but we must first have detailed knowledge about which parameters are critical and must be controlled. Dr. Bullis stated an NBS need for guidance in this area.

In response to this statement, Prof. Kennedy stated that there are two distinctly different technologies now in use for IC design: the bipolar technology and the MOS technology. In his opinion, critical process parameters for the bipolar technology are well defined; about 90% to 95% of them could be

listed today. In contrast, little information is available for the MOS fabrication technology, and further knowledge is required in this area.

Many test-sites for the bipolar technology have been designed by circuit and/or layout engineers. As a consequence, many test-sites are designed to yield important circuit parameters: current gain (β), resistor values, etc. Few of these test-sites are designed to yield fabrication process data. In short, many of these test-sites have been designed by the wrong people, and because these people traditionally control the mask design, it becomes difficult to alter the test-sites now being used.

Next, this round-table discussion was directed toward the degree of complexity one can utilize in test-site measurements. It was evident to all attendees that test-site measurements must be simple, and of a type that can be accomplished on high-speed (automatic) measurement equipment. High frequency measurements and/or switching transient measurements, for example, would be totally unacceptable to the semiconductor industry.

This need for simplification produces complications in the evaluation of fabrication processes. Although base-width is an important physical parameter for bipolar transistor operation, there is no simple method whereby this parameter can be

measured using test-sites. In fact, it was agreed there is no accurate laboratory method available whereby this parameter can be measured, whether or not a test-site is used.

Thus, we have an overall approach to this problem of process evaluation and control using test-sites. Many critical device parameters cannot be measured using test-sites: frequency response, switching speed, base width, etc. Rather than attempting to invent techniques whereby these complicated parameters can be measured, it is preferable to use simple test-sites for monitoring all important process parameters. From these data, we can maintain control over the complicated device parameters.

At this point in the discussion questions arose concerning the advisability of recommending new test-sites to the semiconductor industry; test-sites designed to monitor specific process parameters. It was mostly agreed by these attendees that new test-sites introduced problems of education that are sometimes difficult to overcome. Prof. Kennedy suggested that new test-sites should be introduced only when the need has been established. He recommended that we should first direct our attention toward test-sites presently used throughout the semiconductor industry, and we should thoroughly study these test-sites as a means to obtain required processing information. After completing this task we will be in a better position to evaluate the need for new test-sites.

This approach to the test-site problem was reinforced by Mr. Calahan (Motorola) through a discussion of difficulties arising from an introduction of new test-sites into IC manufacturing. He cited the necessary modifications of automatic measuring equipment, the necessity to restructure the data base within an organization, etc. His outline of these problems made it evident that the problem does not necessarily arise from the reluctance of engineers to accept change -- it can also become very costly for a semiconductor manufacturer.

For this reason, before the semiconductor industry will introduce new test-sites into IC manufacturing it must be proved that their use can provide valuable and important information. Toward this goal Dr. Bullis stated the present NBS approach to this problem. He suggested that a catalog be issued on the topic of test-sites. This catalog would contain documented information on each test-site; what it is, how it is used, what information it yields. In short, this catalog would provide necessary understanding for test-site monitoring of IC fabrication processes.

Prof. Kennedy raised a mild objection to this standard test-site monitoring technique. His experience in bipolar transistor manufacturing showed that no two bipolar transistor designs yield the same set of critical process parameters that require careful monitoring. Some transistor designs are

critically dependent upon changes of epitaxial layer thickness, whereas other designs are critically dependent upon the emitter region diffusion temperature. As a consequence, it is sometimes difficult to know what test-sites are required for process monitoring. The selection of suitable test-sites could be accomplished using a computer sensitivity analysis of a device, prior to mask fabrication. If, instead, the test-site was composed of a large version of the transistors to be manufactured (so that they could be probed for electrical characterization), test-site selection would become unnecessary.

It was indicated that this latter technique is presently used at Motorola, and with adequate success.

The topic of discussion next shifted to evaluation and interpretation of test-site measurement data. It was generally agreed that this problem will involve an extensive degree of mathematical modeling, which is a field well suited to present efforts at Univ. of Fla. For this reason, a close cooperative program should be initiated between the Univ. of Florida and NBS on the study of test-sites from both experimental and mathematical points of view.

Questions were raised by Prof. J. Meindl (Stanford) concerning the use of test-sites for procurement of custom IC structures. Dr. Bullis stated that this question was premature, since numerous other questions must be answered before this

question of test-site utilization can be addressed. Mr. Beuler (NBS) did provide some insight into this problem. He stated that a request was made to two semiconductor companies for the fabrication of test-sites from NBS masks. He stated that one company refused, and the other company agreed -- but on a conditional basis. It was stated that NBS would receive no information on the test-sites until a study had been undertaken by their engineers and, thereby, the test-site properties were fully understood. Furthermore, before test-site measurements were given to NBS, the company engineers must have completed an evaluation of these test-sites to know all information they were giving away about their manufacturing process.

In reply to this experience, Dr. Kitchen (NSA) stated some basic fears of semiconductor manufacturers in association with test-site evaluation. It was stated that some manufacturers are reluctant to reveal their process information through test-site evaluation for sound business reasons, and that these reasons are not connected to problems of company secrecy. Namely, semiconductor companies fear that outside knowledge of process parameter variabilities would result in a comparison between various manufacturers. If so, they fear being "beat on the head" by customers because their process control is not equal to the process control obtained by other companies.

This fear becomes amplified by a lack of confidence in the capability of test-site techniques to adequately characterize a

manufacturing process. If, indeed, conclusions are drawn about the inadequate capability of a company to control their manufacturing, it would represent a difficult situation if this conclusion was derived from bad measurements.

Dr. Kitchen stated that cooperative efforts with industry on the use of test-sites are actually a give and take situation. If by sending test-sites through their manufacturing line a company has something to gain, little resistance will be encountered. If there is little (or nothing) to gain, the manufacturer will probably not cooperate.

In relation to this problem, Prof. Kennedy viewed the company secrecy problem as temporary in nature. Specifically, semiconductor manufacturers are now starting to view as secret the equipment whereby they manufacture semiconductor devices, and not the process parameters attained. Questions relating to how a given manufacturer obtains parameter reproducibility, with the through-put needed for manufacturing, represent an important company secret. The actual process parameters used in the devices represents only a minor level of propriority information; in many cases all manufacturers achieve the same end results.

Questions also arose concerning the distinction between using test-sites for process monitoring and the use of in-line process monitoring techniques. After discussions on this topic it was concluded that the important difference between these

two process monitoring methods is their relative sensitivity. In-line process monitoring methods usually have inadequate sensitivity to be used for "fine-tuning" a manufacturing line. Nevertheless, these monitoring methods can be used to prevent gross changes in a process, and they can detect these changes before a large amount of product has been ruined. The test-site method for process monitoring offers a large degree of monitoring sensitivity and, therefore, it can be used for this fine-tuning process.

An important shortcoming of the test-site method is that process control information is obtained after the fact; bad test-site measurement data could mean the entire production line needs reworking. Clearly, the availability of adequately sensitive in-line process monitoring methods would represent a superior method for process control -- but we don't know how to accomplish this goal. For this reason, we must go along with the use of test-sites until new in-line monitoring techniques have been invented.

It was admitted by these attendees that the test-sites presently being used will, indeed, exhibit an adequate degree of process sensitivity, but we often do not understand the relation between test-site measurements and the relevent process parameters. Prof. Kennedy stated that in cases where this relation is understood, it is sometimes necessary to undertake a program of data reduction and manipulation before the desired

information is obtained. Therein we have an important task for this program: to obtain the needed understanding about test-site measurements and the associated problem of data manipulation.

A brief, but important, point was made in connection with the use of optical testing methods. It was pointed out that test-site measurement techniques yield measured parameters in a form that is easily stored on a computer tape. Optical testing methods seldom yield measurements in this form and, therefore, are not easily used in data reduction schemes that involve test-sites.

Further emphasis was placed upon the importance of test-sites as a starting point in any well organized IC design procedure. Assuming test-sites can be used to establish the basic processing parameters used for IC fabrication, it is not difficult to visualize an IC design procedure based upon this processing information. For this reason, it is evident the goal for a test-site research program is to identify and develop test-site structures capable of yielding this type of process parameter information.

Attendees recognized that a detailed understanding of these test-site structures could be obtained by mathematical modeling techniques, on a computer. For this reason, it appears a cooperative program of research between NBS and U. of F. would be advantageous. In this cooperative program the U. of F.

could offer assistance in the area of test-site analysis, and in a study of the sensitivity of test-site measurements to individual process parameters associated with IC fabrication.

APPENDIX IV

Workshop on Integrated Circuit Analysis and Design

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Appendix IV

Workshop on Integrated Circuit Analysis and Design

A4.0 Introduction

A summary is presented of opinions, comments, and technical information gained from a workshop on integrated circuit analysis and design. This workshop was held at the University of Florida, Gainesville, Florida on Nov. 7-8, 1974. Present at this meeting were The Steering Committee Members listed on page 5 and, in addition, the invited guests listed below:

Dr. R. Diephuis	Applicon, Inc.
Dr. C. Gwyn	Sandia Corp.
Dr. G. Hachtel	IBM
Mr. P. Loslabene	National Security Agency
Dr. G. Temes	UCLA
Mr. W. Wiemann	Motorola

The purpose of this workshop was to evaluate our present capability to design integrated circuits on a computer. Topics of particular interest included those areas of IC design that are inadequate and costly. It was hoped that workshop attendees could offer suggestions as to where these capabilities are inadequate, and to areas of research that would alleviate such problems.

Attendees at this workshop offered clear evidence of a problem previously raised at these workshop meetings: there is a pronounced lack of communication between scientists engaged in the circuit aspects of IC design and those engaged

in the solid-state device aspects of IC design. As a consequence, problems associated with linking together these two areas of specialty are not often addressed in an adequate fashion. This situation is further aggrevated by a need to produce working IC structures. Engineers engaged in circuit and chip design must produce workable IC structures, and in a minimum time. For this reason, where fundamental understanding is unavailable for the solution of their design problems, circuit and chip designers must solve their problems by empirical methods.

A4.1 Design of Custom (Low-Volume) IC Structures (National Security Agency)

A valuable and constructive discussion was presented by Mr. P. Loslabene on the topic of custom IC design for the National Security Agency. Mr. Loslabene has been involved with custom IC design for NSA since 1965 and, therefore, is intimately familiar with the topic. Furthermore, he has the responsibility to satisfy IC design requirements for NSA, despite problems arising from the state-of-the-art in circuit design, device design, and IC manufacturing. As a consequence, he has been involved in the development of techniques whereby NSA satisfies their IC needs, despite these problems.

Most IC structures used by NSA are for low speed logic applications-- in the order of 1.0 MHZ or less. Therefore,

many problems associated with high-speed structures are avoided. Nevertheless, many NSA IC design and procurement problems are typical of those encountered by most DoD system contractors. Typically NSA requires only 100 IC chips of a given design; sometimes this initial requirement will attain a total production level of 10,000 structures. On one occation the total production requirements for a given IC was 10^4 structures. Despite these moderate volume levels (when compared with commercial IC manufacturing) they are, in reality, small: for example, a total of 10^4 chips was required over a period of 10 years.

Another problem emphasized by Mr. Loslabene was the long development, testing, and production cycle for NSA systems using IC structures; he stated an expectation that this cycle time could run to 15 years. As a consequence, many problems arise when working with the rapidly changing semiconductor industry. For example, he suggested the level of activity in a given semiconductor technology could be approximated by a Gaussian type distribution, with 26 limits of about 5 years. As a consequence, it is sometimes difficult to put into service a system that contains a given semiconductor technology, before that technology is obsolete.

A difficulty frequently stated by other small volume IC users was restated by Mr. Loslabene: the need to develop multiple procurement sources.

He said that NSA usually attempts to have more than two sources for a given structure, and they would like to have eight or nine. This situation is often in opposition to well known practices throughout the semiconductor industry. For example, semiconductor device manufactures seldom (if ever) reveal their methods for IC fabrication. As a consequence, contracting for the design of a given IC through one semiconductor manufacturer could imply a similar expendature for each additional procurement source.

Particular emphasis was made of the necessity to introduce design modifications into an IC during the associated system design and development cycle. This situation is hindered by obvious economic difficulties and, in addition, a problem that is often neglected: there is an inadequate number of people skilled in the art of IC design.

After discussing the overall problem of custom IC design, development, and procurement at NSA, Mr. Loslabene outlined the techniques used to overcome these problems. He initiated this aspect of his presentation with a discussion of the estimated life cycle of a technology -- from inception to obsolesence. As previously stated, this estimate is about 15 years. Although the ideal system development cycle is seldom (if ever) achieved, this ideal would be as follows:

A. Start system design when technology is in its infancy,

B. Complete initial design, field test system, and undertake necessary redesign during technology build-up,

C. Enter system production at peak of technology.

A more typical situation was stated to be as follows:

A. Select a technology and initiate design; thereafter the technology disappears,

B. Select another technology and redesign; thereafter the company specializing in that particular technology fails,

C. Select a third technology, but it is too late.

Clearly, this is a pessimistic view of the situation, yet it does show a broad outline of problems arising in the design of IC structures.

A method used to alleviate such problems is through an identification of industrial trends. Extensive time is devoted in discussions with persons at different semiconductor companies. These discussions are directed toward estimating their technical directions: for example, major production trends over the next few years; areas of commercial effort and investment, etc. Such information is considered of

particular value because NSA cannot significantly influence industrial trends; instead, they must go along within them. Furthermore, it is considered dangerous to "second-guess" industry in such important matters.

In addition, an attempt is made to minimize IC processing difficulties that arise from a mismatch between NSA requirements and industrial capabilities. Studies are made of parametric data for semiconductor devices fabricated by a large number of IC manufacturers. Thereafter, this parametric data is correlated with existing NSA requirements, and appropriate IC vendors are selected. It was stated that many such manufacturers can provide documentation concerning this parametric data, although this source of information is often found inadequate. For this reason, each manufacturer is supplied with test site masks and contracted to fabricate necessary test sites for parametric data evaluation. Thereby NSA obtains detailed parametric information for the semiconductor devices to be incorporated into a new IC design.

Typical of many custom IC users, NSA requires multiple sources for their IC structures. As a consequence, a worse case situation is taken from the accumulated test chip parametric data. It was specifically stated that this design procedure produces a serious degradation of electrical properties for the resulting structure. An example cited was a CMOS IC

structure designed on a worst case bases from parametric data of nine vendors. This same IC structure yielded twice the performance when designed on a worst case basis from the parametric data of one given vendor.

Mr. Loslabene indicated that this worst case design technique was necessary, in view of the state-of-the art, yet it yields an inefficient system:

A. Systems use too much power.

B. Chips use too much area.

C. Systems use too many chips.

Furthermore, he stated that an important goal for any custom IC design procedure is to eliminate the necessity to do things in this way.

Included in this general outline of the NSA IC design procedures were many technical details about their software systems. In addition, a substantial discussion was presented on the merits of utilizing standard logic cells in the design of IC structures. Particular emphasis was placed upon the standard cell as a cost saving measure through a reduction of IC design time. Another point of emphasis was the problem of skill-mix in IC design: one man cannot be fully knowledgable in circuit design, device physics, and system architecture. Further, because the "black-art" of semiconductor IC design is found primarily at the cell level, the use of standard (and

well documented) logic cells eliminates a large class of problems that can be solved by only a limited number of people.

Mr. Loslabene concluded his presentation with a recommended list of IC design problems that he believed needed solving:

1. Data Base Management
2. Device Models
3. Optimization Methods
4. Test Sequence generation
5. Fault Modeling
6. Design Rule Checking

This particular list of problems can be classified into three groups, and only one of these groups is of particular interest to this program of study. The first group represents problems common to both NSA and the semiconductor industry, and is receiving substantial attention throughout the nations without government intervention. The second group represents problem areas that are receiving extensive government support and, therefore, this ARPA program should not become involved. The last group represents problem areas that are receiving negligible attention by either industry or government, and are important to the economical design of IC structures.

As stated in a previous workshop (Appendix II), the device model problem is of particular importance to the entire

field of IC design and development. For this reason, it is recommended as a topic of research for this ARPA program. A second topic recommended by Mr. Loslabene is in the field of design optimization. Because an in-depth discussion of design optimization was presented by other guests at this workshop, further comments are given at a later point in this workshop summary.

(Sandia Laboratories)

After Mr. Loslabene's presentation, a presentation was given by Dr. C. Gwyn of Sandia Laboratories on essentially the same topic. A great deal of similarity was found between custom IC design at Sandia and at NSA; therefore, these similarities will not be repeated. An important difference between these two organizations lies in their effort toward the analysis of semiconductor devices. NSA has no apparent effort toward the computer analysis of semiconductor devices, whereas a substantial effort is indicated by Sandia on this particular topic.

It was emphasized by Dr. Gwyn that Sandia's effort in CAD is relatively new and, as a consequence, their entire computer software system is under development. Many of their individual IC design software systems have been acquired from others working in this field:

Logic simulation from Auburn Univ.
Layout and Wiring from RCA.
Circuit Design from a multiplicity of Sources.

Having acquired these software systems, Sandia is directing substantial effort toward modifications, improvements, etc.; in short, customizing these software systems to their own particular needs.

At Sandia Labs., MOSFET IC design bears a strong similarity to that found at NSA. A standard cell approach is used, although they have developed their own catalog of logic cells. Furthermore, the information available concerning the electrical and physical properties of their standard cells is essentially the same as that available at NSA.

Contrasting with NSA efforts, Sandia Labs is directing substantial effort toward the development of an IC design capability based upon a bipolar technology. It was stated that they are not intending to use a standard cell approach for bipolar IC structures but, instead, they are using a standard process library for bipolar transistor fabrication. It is planned to select from this library proven bipolar transistor device characteristics and their associated fabrication processes. Thereafter, using conventional computer techniques, they plan to design IC structures from this set of standard devices and their processes.

Furthermore, requirements for device characteristics not in their standard process library will be satisfied using mathematical models for bipolar transistor operation. Computer programs will be available to model the physical mechanisms of bipolar transistor operation. Using these proposed computer programs, in conjunction with process data for a device similar to the one required, their intention is to calculate the necessary process modifications. Thereby, the new fabrication process (diffusion times, doping levels, etc.) will be used to initiate the design of a new bipolar IC structure.

Clearly, a computational capability of this type will necessitate the development of some sophisticated bipolar transistor analysis techniques. It was stated that Sandia has such an effort underway, yet the size of this effort was not clearly stated. Presently, they have both a steady-state and a transient capability for the one-dimensional analysis of bipolar-transistors. Further, they now have under development a computer program for the two-dimensional analysis of bipolar transistors.

It was stated by Dr. Gwyn that Sandia plans to undertake the development of a computer program for the two-dimensional transient solution of bipolar transistor operation. He clearly stated that the completion of such a computational capability was in the undefined future, yet it was said that

this effort is underway. Questions by Workshop attendees concerning how the known computational problems are to be solved produced no definite answers.

Dr. Gwyn emphasized that a large part of their bipolar transistor effort is directed toward a solution of the well known radiation hardening problem. Their intention has been to model the consequences of ionizing radiation upon the physical properties (and, hence, on the electrical properties) of bipolar transistors.

Their success toward solving this radiation problem is consistent with previous discussions of bipolar transistor modeling at the workshop on this subject (see Appendix II). It was stated that prior to irradiating transistors there is unsatisfactory agreement between experiment and theory. For this reason, adjustable constants within the model (lifetimes, mobilities, doping, etc.) are used to attain the necessary agreement.

After having made these adjustments, the physical changes produced by radiation are introduced into their mathematical models, and calculations made to establish the resulting electrical modifications. Using this procedure, theory and experiment are stated to be in excellent agreement.

A4.2 Industrial Design of IC Structures

A highly informative discussion was presented by Mr. W. Wiemann (Motorola) on the topic of IC design and development in an industrial environment. Mr. Wiemann's presentation was directed toward the history of IC design at Motorola. He outlined some of the problems they have encountered over past years and the attitudes toward this subject that presently exist at Motorola. This experience is of particular importance to the program under consideration because Motorola was one of the first companies to enter the field of custom IC design. Later, after gaining experience in this area, Motorola was forced to abandon the custom IC field, and direct their attention toward large volume IC design and manufacturing.

In the late 1960's Motorola initiated a program for the computer design of IC structures. Initially this work was directed toward the design of elementary structures containing only 5 or 6 transistors on a given chip. Later, Motorola directed their attention toward cell design, using techniques similar to those presently in operation at NSA and Sandia. Through the years Motorola gained substantial experience in this design technique, and they used this experience to enhance their IC manufacturing. An IC design center was installed in Boston with an aim toward assisting customers

with their design problems and, thereafter, undertaking the manufacturing of these new structures.

Since that time Motorola has closed their Boston IC design center, they have abandoned the concept of custom designing and manufacturing IC structures, and they have directed their attention toward the large volume market. At this time only in-house custom design and manufacturing requirements are satisfied by the semiconductor operation.

This experience of Motorola in the custom IC design business was outlined by Mr. Wiemann as a basic manufacturing problem. The Boston operation was extremely successful from an IC design point of view -- there was a large amount of business. Most of this business was directed to satisfy small quantity IC needs, and it produced few (if any) large volume manufacturing requirements. In a short period of time he stated that the factory "disowned" them, and Motorola would not undertake manufacturing of the structures they designed for customers.

He stated that manufacturing a large number of custom IC structures produces a sequence of production line problems: special handling, special testing, and special chip characterization. For example, when 20-30 different IC structures are coming through the production line (at the same time), each structure will involve a different test set-up. In fact, sometimes these custom IC structures require a reconfiguration of

the entire manufacturing line. As a consequence, Mr. Wiemann stated that the production facility for custom IC structures remains in a constant state of flux.

An additional experience of Motorola is particularly important, in view of the design methods presently being used at NSA and Motorola. It was stated that the Motorola custom design techniques were based upon a standard cell concept, with a cell library similar to that now used at NSA. Motorola found that cell library maintenance represented an overwhelming problem. A major problem arises from the inventiveness and ingenuity of engineers in this field. Each new IC design resulted in additions to the cell library; in short, each engineer would do his "thing" and design new cells which must be added to the library.

An additional cell library maintenance problem arises from the state of flux found in the semiconductor business. Namely, the technology in this field changes so fast that a cell set lasts for only about 6 months.

This library maintenance problem, in conjunction with other unstated problems, resulted in an abandonment of the standard cell approach by Motorola. Design without the standard cell approach was initiated when Motorola entered the calculator chip business. Since that time Motorola has found no necessity to re-adopt the standard cell technique, even for their existing microprocesser business.

Today, Motorola's approach to IC design places great emphasis upon computer analysis, yet their implementation of computer methods differs from that in other semiconductor organizations. For example, these computer techniques are viewed as "tools" and "aids" for the IC design engineer, and not as a step toward eliminating the design engineer. Motorola is not intending to adopt a design system whereby the engineer enters the system with a sequence of requirements and comes out of the system with a complete design. Instead, their circuit design program, their layout and wiring program, etc. are viewed as stand-alone design tools that are available for engineers.

Through the use of this loosely coupled system of computer programs, it is believed Motorola attains a maximum of flexability. Technology changes are easily accommodated through changes of individual computer design tools, rather than a redevelopment and reorganization of a complete design system. Recognizing vast differences between the Motorola and NSA/Sandia approach to this problem, Mr. Wiemann discussed various Motorola computer IC design tools, and their experience with these tools. A degree of stress was placed upon those aspects of computer design being addressed by NSA/Sandia that are being essentially ignored by Motorola; and he discussed the reason for this situation.

It was stated that computer design techniques discussed at this workshop often suffer from a lack of credibility among many engineers. For this reason, some older IC technologies at Motorola place a minimum of emphasis upon these computer design techniques. The design of bipolar transistor IC structures, for example, is often accomplished without relying extensively upon computer layout and wiring. Engineers frequently find they obtain only 80% to 90% of a layout from their computer solutions, and the remaining must be completed by hand. Further, in order to complete this final 10% or 20% of a layout it is frequently necessary to re-do about 50% of the layout done by computer.

Similarly, most MOS designs at Motorola rely heavily upon hand layout, although this layout process uses computer aids. Further, this MOS effort is directed toward attaining standard products that can be manufactured at high volume. They are directing their efforts toward a standard product microprocessor, a sequence of standard product interface chips, and a family of ROM's and RAM's for their microprocessor. This, again, emphasizes the views Motorola has developed from their past experience with custom LSI: they are now directing an effort toward standard product manufacturing, and at a large volume.

Mr. Wiemann also discussed other views of computer design for IC's that are in disagreement with the views of previous speakers. It was evident from his comments that his views were drawn from practical experience, rather than from theory. For example, in his mind the logic design for an IC structure is based upon experience of the design engineer. For this reason, the most important use for a logic similator is to verify a new design; hence all that is needed is zero-one simulation. He stated that a calculation of delay in a logic simulator is of little (or no) interest to the designer. After having verified the logic design for an IC, the design engineer goes into circuit design where he undertakes a critical path analysis for the structure under consideration.

Similar remarks were directed toward the topic of automatic test generation. He stated that nobody at Motorola cares about having this capability. Their testing is based upon the development of a suitable test pattern that includes important logic elements of the chip being fabricated. Using this technique, Motorola has encountered no problems -- even when manufacturing chips containing 10,000 transistors. A parting comment on this topic was directed toward their experience with IC manufacturing for the government. In general, they have no information about what a government

chip is suppose to do; therefore how else could it be tested after manufacturing.

Thereafter, Mr. Wiemann discussed the need for fabrication process modeling. Presently, Motorola has a Monte Carlo capability for the d.c. characteristics of a structure, but undertaking a similar calculation on a transient basis is altogether too expensive. Although IBM has stated a capability in this needed area (ASTAP), this claim is unfounded. Motorola concluded that a transient Monte Carlo analysis of a 100 transistor structure (using ASTAP) would take an unreasonable amount of CPU time (he claimed one week). For this reason, Motorola is presently working on this problem, but with little success.

It was stated that computer memory people have a particular interest in this area of Transient Monte Carlo analysis. At this time they undertake a worst-case design, and experience shows this technique is unsatisfactory. There is a need for Monte Carlo capabilities in calculations of switching speeds and memory access time.

Another area of need is in IC manufacturing. If, indeed, a Monte Carlo analysis could establish critical processes in IC manufacturing, this information would offer important advantages. In his mind, a solution for this problem must be found.

Mr. Wiemann's concluding comments were directed toward a need for improved models for MOS transistors. It was claimed that Motorola, as in other companies, find existing models for MOSFET operation inadequate and inaccurate. Motorola now has a limited effort toward the development of better models, but they need help.

A4.3 Design-Optimization

Prof. S. Director gave a short presentation on the advantages of using the optimization techniques he has developed for an initial phase of IC design. He presented one example of its application to a two-input nand gate selected from the NSA library. After a detailed discussion of this design technique, and the sequence of computer calculations necessary for optimization, he showed the following results: an area reduction of one-half, a satisfactory propagation delay time, and a satisfactory down level at the output. More important are the views and comments by workshop attendees on this topic.

It was quickly agreed that the word "optimization" is misleading. The computational technique called design-optimization does not necessarily yield the optimum solution for a given problem; the resulting solution could be local, not global. It is more appropriate to consider this method

a systemization of IC design, and its goal is to search out solutions for IC design problems in an organized fashion.

One attendee stated that this design technique was aimed toward eliminating the "gut feeling" necessary for IC design, and it would probably be of little value for the experienced engineer. Furthermore, after viewing the utilization of such a technique, he stated that the method appears too complex for the inexperienced engineer.

It was emphasized by Prof. Director that his proposed method offered a significant saving of computer time, over other possible methods; for example, using a Monte Carlo approach. Again this particular point was not immediately evident to workshop attendees. Sensitivity calculations are needed for each independent variable associated with the particular problem under consideration. Furthermore, heuristically selected weighting functions are used for design parameters, rather than the independent variables. As a consequence, the overall computer requirements might (or might not) be less than that required by traditional methods of design.

From this discussion it became evident that "design-optimization" is a new area of investigation, and that it is receiving a normal amount of resistance from the technical community. It should be recognized that computer design of

semiconductor structures received a similar critical review in the recent past. Therefore, at this time we cannot accurately evaluate the influence this analytical technique will have on our future methods of IC design.

Following Prof. Director's short presentation, two workshop guests offered verification of some views voiced by the attendees: Dr. G. Hachtel (IBM) and Dr. G. Temes (UCLA). Dr. Hachtel's presentation provided an important illustration of semiconductor IC design using these techniques. Contrasting with Dr. Hachtel's topic of presentation, Dr. Temes offered suggestions, recommendations, and his insight into this problem; his opinions were drawn from experience in the application of design optimization to electrical networks.

Dr. Hachtel's presentation was directed toward outlining many technical and mathematical details (and problems) associated with the design of specific IC circuits at IBM. This presentation made one point very clear: in its present state of development, design-optimization techniques are not appropriate for the novice engineer. The application of this design method requires extensive "gut" feeling, in conjunction with equal skill in the area of mathematical analysis.

It was specifically stated that a most difficult part of design optimization is clearly specifying the problem to be solved. In most practical situations we seldom design to

obtain (or minimize) one individual circuit characteristic (for example: power, chip area, input drive, delay time, etc.); instead, most situations involve a set of design requirements. Further, in any design problem there are trade-offs between these requirements; sometimes minimum power is more important than a minimum delay time. Thus, these levels of importance between design characteristics become a difficult part of problem specification, and this aspect requires extensive experience and skill. The levels of importance between design characteristics are introduced as weighting functions into the computer program he described for IC design.

Another point raised by workshop attendees, and answered by Dr. Hachtel, concerned the question of obtaining a true optimum. Dr. Hachtel stated that one obtains a local minimum for any given solution, and it is seldom (if ever) known if this minimum represents a true optimum. Implied during his discussion was that a true optimum is a questionable concept in any practical design problem; some solutions are better than other solutions, with no one solution a true optimum.

An important emphasis in this presentation was the consequences of modifying relative levels of importance placed upon the various design requirements. A small change

of weighting factors would yield an entirely different solution for a given problem, with some solutions better than others. Thereby, we have the need for engineering insight and skill. A skillfully selected set of weighting factors can yield various levels of quality in a given design. No given solution is either right or wrong, yet one solution can be significantly better than another.

One example presented involved the design of an ROM using MOS technology, weighting functions were altered as a basis of trade-off between various electrical characteristics. Starting from an initial man designed structure, his computer program was used to improve upon this design. This particular problem was undertaken as a "trial-run" to test the technique and, in addition, to gain experience. For this reason, the overall effort required three months, although a substantial part of this time was devoted to removing program "bugs".

Resulting from this effort was a ROM design that is substantially superior to the initial structure. Details of the design procedure used by Dr. Hachtel indicated his extensive knowledge (and skill) of the consequences arising from different trade-off combinations within the structure under consideration. This particular illustrative example showed what could be accomplished using this technique on a non-automatic basis.

After gaining the experience and insight necessary to accomplish this design task, Dr. Hachtel did not program this insight into an automatic ROM design procedure. In fact, the possibility of automatic design techniques was not clearly pointed out either by Dr. Hachtel or Prof. Director; their emphasis was upon the improved design each had obtained in particular applications of the technique. A broader view of design-optimization potentialities was given by Prof. Temes in his illustrations of past accomplishments in the design of electrical networks.

Professor Temes offered substantial insight into this design technique through a simple illustration. During his lectures on this subject at Stanford Univ. he gave a class assignment for the design of an elementary feedback circuit: there were 20 students in the class, and he got 19 different solutions. Further, he emphasized that each student had, individually, attained a correct solution. He attributed this situation to the starting point, (or initial guess) taken by each student. From this initial guess the design-optimization technique leads to a local minimum, and there is no global solution obtainable by the present method.

This apparently contradictory situation was used to illustrate the need to have extensive understanding about the problem to be solved. A cle distinction must be made

between parameters that are variables and parameters that are fixed by the technology. Further, the design engineer must have a clear understanding of the consequences of variable changes upon the circuit, and he must initiate the design from a set of conditions near the desired solution.

Professor Temes also gave some illustrations of automatic circuit design on a computer. These illustrative examples arise from experience gained through manual design-optimization and, thereafter, programming this experience into a design algorithm. One example was a voltage variable delay line for a video tape recorder which was a 200 element R-C network. After many man hours of effort, an automatic design procedure was developed, and the total design now can be accomplished for a few cents of computer time.

Professor Temes next discussed the application of design-optimization techniques to the design of semiconductor integrated circuits. It was stated that he considers this problem far more complicated than those encountered in his past experiences. For this reason, new algorithms are needed; algorithms that are substantially simpler (and faster) than those described by previous workshop speakers. At this time he views processing parameters as the true variables of an IC, and thus process parameter sensitivity as an important characteristic to be minimized in any IC design.

He emphasized a need in IC design to start the design-optimization procedure from a practical, and reasonable, set of initial conditions. Presently there is no obvious way to initiate this design procedure; he therefore suggested that a "shot-gun" approach might be considered -- Monte Carlo methods.

Prof. Temes suspects that a design-optimization procedure based upon parametric minimization will not yield a unique IC structure but, instead, a multiplicity of potentially satisfactory structures. If we include in this design procedure a requirement to minimize the process parameter sensitivity, he believes the number of satisfactory structures would reduce to a point where selection becomes a simple task.

A4.4 General Discussion

After completing the presentations by the invited guests, a round-table discussion was initiated on an important aspect of the question under consideration. Namely, what areas of research on this topic would ARPA funding produce a significant reduction of IC costs to the DoD and their system contractors?

Clearly, this type of approach produces many digressions and irrelevant discussions. Nevertheless, the workshop attendees did offer some further insight into the problem at hand.

Professor Director restated his convictions that design-optimization is an important topic of the future. Although this field is now in its initial stages of development, research funding should be directed toward its further development. A particularly important area of application is process desensitization. Existing Monte Carlo methods are too expensive and, therefore, a new approach must be discovered; possibly the approach suggested by T. Scott (IBM) at a recent meeting in New Hampshire. Because Dr. Director attended this meeting under ARPA sponsorship, he will report on the technique suggested by T. Scott.

Dr. Hachtel gave further emphasis to the comments of Prof. Director. More importantly, he placed particular emphasis upon a problem that has been clearly evident throughout this entire study program: The lack of communication between circuit designers, device designers, and engineers involved in the graphics aspect of IC design. He suggested that this lack of communication has resulted in fragmented efforts in these three areas and, therefore, has minimized the value of research. Further, he emphasized a need for better models for semiconductor device operation, and the gains from research support in this area.

Mr. Loslabene of NSA emphasized one aspect of the IC design problem that is exceedingly costly, yet could not be easily addressed by ARPA research support: Misc. administrative and documentation problems. For example, data base management, documentation, and other non-technical problems. He believes these problems are far more important than the technical problems discussed at this workshop.

Dr. C. Thornton (ECOM) placed emphasis upon many aspects of this program. He believes problems like placement and routing are being adequately covered by other government funding, and should not be considered under this program. In contrast with this well supported aspect of IC design, he considers process desensitization most important, and research should be directed toward this problem. In addition, Dr. Thornton placed great emphasis upon the need to bring the results of this research effort into the public domain.

Mr. Wiemann (Motorola) recommended that this research effort be directed toward the cell based concept of IC design. This technique for design is not particularly valuable when applied to large volume (standard product) type of situations, but it is valuable for custom IC. Further, he emphasized a need to develop process monitoring wafers for IC design purposes. His comments on design-optimization were directed toward one particular application: process desensitization.

He considers that area minimization, for example, is a trivial aspect of design-optimization, in contrast with desensitizing an IC design to manufacturing process variables. Only by satisfying this aspect of the design procedure can small quantity IC manufacturing be realized from large semiconductor manufacturing.

Appendix V

Workshop on Microprocessors

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Appendix V

Workshop on Microprocessors

A5.0 Introduction

On Oct. 7, 1974, a workshop on semiconductor microprocessors was held in Cambridge, Mass. Unlike other workshops held under this ARPA/U. of F. study program, this workshop on microprocessors was not aimed toward answering technical questions concerning the design, development, and manufacturing of custom IC structures. Instead, the purpose of this workshop was to inquire into questions raised at a Steering Committee Meeting concerning the applicability of microprocessors toward the solution of the custom IC problem. It was suggested that most situations in DoD systems design requiring custom IC electronic structures could be satisfied using commercially available microprocessors. As a consequence, the entire topic of custom IC, and the problems associated with the procurement of custom IC structures, might be irrelevant.

A large number of semiconductor device manufacturers have made specific long-range commitments in the field of microprocessors Some companies are offering for sale either first or second generation microprocessors, and at a relatively low cost. Many of these companies make claim to a solution of the custom IC problem because their microprocessors are a large-volume item of standard design and can be customized to

specific applications. Thereby, it is claimed that a lower total systems cost is realized by customizing the application of a standard product, rather than designing a custom product to satisfy a specific application.

Despite this claim by semiconductor manufacturers, the need for custom IC structures has not diminished to a significant degree. Many DoD system manufacturers retain their large and expensive in-house IC capability, and there is no clearly evident trend toward a total re-thinking of this custom IC problem. The microprocessor has, indeed, made some inroad into areas of IC application once satisfied by custom IC structures. Nevertheless, the shift from custom IC's to microprocessors is far short of the claims made concerning the applicability of microprocessors to the solution of this problem.

This workshop was planned as a means to gain insight into this particular question. Substantial controversy arose concerning its organization. It was suggested that representatives of numerous microprocessor manufacturers should be invited to discuss this problem with Steering Committee members. This suggested workshop organization appeared inappropriate: the problem is one of performance/cost trade-off between the custom IC and the microprocessor in specific applications. A detailed knowledge of this trade-off lies mainly with individual DoD system manufacturers, and not necessarily with microprocessor

manufacturers. There is such a vast number of different DoD areas of IC application (communication systems, weapon systems, radar systems, etc.) that it is hardly expected that a semiconductor manufacturer could have the necessary expertise.

For this reason, most invited guests at this workshop were selected for their knowledge of electronic design for DoD system contractors. Many of these guests have first-hand experience in solving these design problems, and understand the necessary trade-off between custom IC's and the use of microprocessors in DoD systems:

Dr. B. Dunbridge	TRW
Dr. R. Thun	Raytheon
Dr. O. Marble	Honeywell
Dr. C. Neugebauer	GE
Dr. P. Georgantas	Autonetics/Rockwell
Dr. P. Martin	A. D. Little
Lt. R. Ray	WPAFB-A.F. Avionics Lab
Dr. G. Fougere	A. D. Little
Dr. P. Strong	A. D. Little

After reviewing the presentations of these invited guests it became evident that problems associated with the microprocessor are not unlike the problems associated with custom IC's. Only a small part of the microprocessor market (about 8%) is directed toward government systems; thus, this particular

application has little influence upon the direction and trends of microprocessor design and development. As a consequence, the peripheral equipment necessary to use microprocessors in government systems requires substantial customization; frequently the custom IC requirements to implement a microprocessor are comparable to those for a complete custom IC design.

Communication systems represent one area where the microprocesser appears to have a minimum of applicability; they appear too slow to satisfy even the most elementary single-channel secure voice communication requirements. Clearly, future development of microprocessors will yield a substantial increase in speed, but it is doubtful that this situation will alter their applicability to communication systems. There is a continuous increase of sophistication, and a continuous need for an increased speed in the digital parts of these systems. As a consequence, communication systems represent a moving target, and it is questionable if the microprocessor can ever be used in this particular application.

It was stated that some of the slow speed needs in radar systems are well satisfied by microprocessors; for example, in phased array antennas, where the phase angle is set every mill-second. The most important digital aspects of radar systems are altogether too fast for microprocessors and, like communication systems, the speed requirements are undergoing a continuous increase; again, we have a moving target. These speed

limitations of the microprocessor is not viewed as a short term situation but, instead, a fundamental problem arising from their architecture. It was stated by one workshop guest that it is difficult to see how the microprocessor can ever compete with the speeds attained from the arithematic unit of a radar processor, and this level of speed is needed in today's systems.

A similar situation was stated to exist in weapon systems. Slow speed applications such as bookkeeping, navigation, etc. are well satisfied by the modern microprocessor. There is also a large class of weapon system electronics that require a substantially greater computation speed than obtainable from microprocessors.

Briefly, it appears the inherent flexibility of microprocessors has been attained with a substantial loss of computing speed. In many system applications, the speed requirements are often satisfied by custom arithematic units that are designed to attain minimum of computation time. At this time there is no obvious way the microprocessor can be designed to yield a computing speed comparable to that obtained from a custom IC and, at the same time, retain the inherent flexibility realized from an arithematic unit working in conjunction with a ROM.

A5.1 Microprocessors in Communication Systems

A detailed discussion was presented by Dr. B. Dunbridge (TRW) on the topic of microprocessors and their application in communication systems. For purpose of background information he stated that a large part of his effort is directed toward the development of IC structures for communication system applications. Some of these communication systems are intended for spacecraft applications, where reliability is of utmost importance. Other communication systems are intended for avionic applications, where there are continuing requirements for an increased complexity and system sophistication.

Both of these applications for communication systems (Avionic, and spacecraft) involve a continuous trend toward an increased data transmission rate and, hence, greater bandwidth. In general, these systems involve time division multiplexing of secure communication channels, and transmission systems involving pulse code modulation. As a consequence, when the required speed of these systems is taken into consideration, it becomes immediately obvious that microprocessors now available on the market are altogether too slow.

Furthermore, the rate of development and advancement in this field was stated to imply that microprocessors of the future would probably not "catch up" with their needs. These communication systems undergo a continuous increase in the

number of required channels, an increased bandwidth for these individual channels, and an increased need that all information transmitted be secure. As a consequence, communication system speed requirements were stated to be increasing faster than the increase of available microprocessor speeds.

It was stated that TRW was solving their problems through the design and development of custom IC structures; mostly bipolar. In general, the level of integration in these systems involves about 500 (or more) transistors on a chip--or about 100 gates. He stated that there are some penalties when using this approach, but these penalties are not unreasonable. One problem is an increased development time, although this aspect must be qualified in terms of the application. Structures that push the state of the art can represent a significant increase of time. In contrast, when they don't push the state of the art this overall development time is only about 2 months longer than when using "off the shelf" items.

Dr. Dunbridge made a clear distinction between the reliability aspects of IC structures for spacecraft applications and for avionic applications. Spacecraft applications require the ultimate of reliability, since they will be in use for many years. In contrast, avionic applications do not have the same need for reliability, yet the overall life-cycle cost is very important. The cost of replacement parts (and their avail-

ability), for example, become important factors when viewing the application of IC structures for avionic communication systems.

A question was directed to Dr. Dunbridge concerning the applicability of microprocessors for secure voice communication on a single channel basis. He stated that their speeds were adequate for this type application; in fact, the microprocessor would represent an "over kill" and, therein, we encounter another source of difficulty. Namely, an "over kill" design for this type communication system implies an excess power requirement. Power consumption is an important aspect of these simple voice communications systems and, therefore, the microprocessor is inappropriate. This statement was confirmed by the NSA representative who has extensive experience in the design of secure voice communication systems.

A5.2 Microprocessors in Weapon and Radar Systems

An informative discussion was presented by Dr. R. Thun (Raytheon) on the application of microprocessors in weapon and radar systems. He initiated his discussion by stating that microprocessors have many uses, although these uses are of a restrictive nature. Namely, the computing power of microprocessors is particularly small due to their slow speed. Nevertheless, there are many computing tasks where high speed is unnecessary, yet these tasks are being accomplished on a

high speed central computer. In such situations the microprocessor could significantly reduce overall computing costs by taking the load of a central computer and, thereby, increasing their efficiency.

He stated that there is presently a big (and useful) "splash" on the topic of microprocessors. It is the first time semiconductor people have put everything together into a complete system. Unfortunately, these microprocessor systems have been put together without deep thought about their design and implementation. As a consequence, the architecture of these minicomputers is not organized and the available software is limited.

From an architectural point of view, the microprocesser is substantially different than the arithematic unit in a radar processor. For this application we need a more powerful function generator and less peripheral equipment. For example, in a microprocessor data is taken from memory, and this produces a significant decrease of speed. In a radar processor there are internal registers to fetch and return data, thereby producing an increase of overall computing speed.

It was stated that the microprocessor does not contain special function generators, and this is a significant drawback. As a consequence, we are computing special functions with only a limited function capability; a particularly inef-

fective way to do things. Microprocessor design is based upon ROM control, which is exceedingly efficient from a device point of view, but it slows you down tremendously. The system must return to the ROM for each instruction step, in contrast with modern computers where there is about 20 logic steps between each clock cycle. It is estimated that on the average this produces a 1:10 disadvantage on the side of the microprocessor.

As a consequence, it has not been considered practical to replace the arithmatic units of even medium performance computers with modern microprocessors. This is not intended to imply that we could not run many microprocessors in parallel and thereby increase the overall computing speed. He stated that it is sometimes possible to run two or three microprocessors in parallel and thereby equal the performance of a single less sophisticated minicomputer.

Due to the increased sophitication of today's weapon systems, we are trying to compute more functions on a computer. As a consequence, the performance requirements of these weapon computers keeps going up. Like the communication system problem, we are shooting at a running target. Presently Raytheon is designing a minicomputer with an add time of about 0.5 μs, which is way beyond the capabilities of a modern microprocessor.

Despite this situation, there are many low-speed problems of weapon control where the microprocessor is applicable: bookkeeping, navigation, etc. Contrasting with these slow speed applications we have a large class of communication problems that require special minicomputers for satisfactory operation.

An extensive study has been undertaken on the utilization of microprocessors in missiles, such as the Sparrow and Hawk. This application is well suited to the technique because of limited speed requirements. Conclusions from this study show that the microprocessor would work in this application, and the task could be accomplished in the next 3-4 years. Nevertheless, in this application there is a tradeoff in device complexity and, therefore, a toss-up between the microprocessor and the minicomputer.

It was emphasized that this missile application for microprocessors may evaporate in the near future. There is a continuous program of modification and improvement in these weapon systems and, thereby, a continuous increase of system sophistication. As a consequence, we are chasing after a moving target; in the near future the computing requirements may exceed our microprocessor capabilities.

Some of the radar guided missiles present a different picture. Microprocessors could be used for the slow computational requirements in these weapon systems. For example,

when using phased array antennas, a microprocessor could set the phase angle, which is accomplished by changing antenna elements about every millisecond. For the high speed arithmatic needs of the radar system the microprocessor is entirely inapplicable.

A5.3 <u>Discussion Session on Microprocessors</u>

After the presentation of Dr. Thun, comments were requested of Mr. M. Callahan (a Steering Committee Member) because his organization (Motorola) is heavily committed toward the manufacturing and marketing of microprocessors. He had few disagreements with previous comments directed toward the low speed characteristics of microprocessors. He stated that the low frequency consumer market is 4-5 times that of the military market and, therefore, there is little insentive to address this problem. In short, microprocessor manufacturers are going after the largest part of the market--the low performance end.

Mr. Callahan stated his belief that military system performance requirements are generally higher than the requirements placed upon commercial products. For this reason, it is not surprising that the available microprocessors could not satisfy a large class of these military requirements. Further, he gave recognition to the fact that custom IC structures, like the minicomputer, produces a system having better performance characteristics and requiring lower input power. Neverthe-

less, this custom design technique is more costly, and this added cost cannot be tolerated in the commercial marketplace.

Next, he suggested the source of this cost was associated with the initial design and development of a computational system; these are non-recurring costs that are amortized over a production run. In his estimation, a standard product has the lowest non-recurring cost whereas the custom military product has the highest. There is a general trend to trade-off performance for developmental cost in the commercial market; this market would like a higher level of performance, but they won't pay a 2 or 3 times price increase for it. Further, since the military market for high performance is less than 10% of the total market, it is unwarranted from an economic point of view.

Thereafter, Dr. Rudenburg (A. D. Little) reinforced these opinions, and offered further insight into the problem of production volume. He stated that if a customer orders one million/year of a given IC design, he can get what he wants. To this Mr. Callahan stated that if you want 10 million units Motorola would design it for free, and if you want 500 units it is questionable if we would do it at all.

Dr. Rudenburg also discussed the problem of microprocessor design. He viewed the development of a microprocessor as a tremendous task, requiring a minimum of 2-3 years for its completion. Further, in order to accomplish this task the

design engineer requires all the computer aids the state of the art permits. Therein we have an important cost associated with microprocessor design: the computer design system. Such a system offers a clear reduction of engineering costs, yet there are hidden expenditures, such as system maintenance. If, indeed, we increase these costs by placing an improved performance specification upon the microprocessor, it is unknown what the resulting total cost would be.

Addressing the question of microprocessor development costs, Mr. Callahan stated that production runs for the INTEL 8080 or the Hughes 1600 is, in his opinion, in excess of 100 thousand systems. This is a necessity in view of the nonrecurring costs, which includes the development and maintenance of a design software system. Nevertheless, he stated that manufacturers of microprocessors cannot start all over again with each new product; they try to build upon knowledge gained about their ongoing software and microprocessor hardware. It was emphasized that the software development associated with each microprocessor development represents a significant part of the overall cost.

An important question is the trade-off needed in military systems in order to use microprocessors. Dr. Thun suggested that the performance specifications of microprocessors would limit their use to only about 10% to 15% of the existing

systems. Except as peripheral devices, the microprocessor could not be even considered for about 70% of all applications.

A5.4 Discussion Session on Custom IC

After dealing with commercial market limitations upon microprocessor performance characteristics, the discussion session was directed toward a solution for this problem. It was generally recognized that custom minicomputers are needed for a wide class of military applications, as a means to attain the required performance specifications. Further, it was recognized that such structures would represent only a small part of the semiconductor market and, therefore, would be difficult to obtain from large volume manufacturers.

A question was raised by Mr. Callahan about the development of standard IC structures that would hit a large part of the military market. A principal objection to this type of solution was who would (or could) set up the needed standards. Another objection was the problem of system improvement and updating, which would produce obsolescence of standard military IC's in a relatively short period of time. The only obvious (temporary) solution to this problem was stated by Dr. Thun: the captured semiconductor facilities within a system house.

Dr. Thun suggested that this method of acquiring needed military IC devices involved a cost factor of 2 or 3. Nevertheless, such a facility is amortized over an entire system and, therefore, it represents only a small total cost increase. Such a facility should not be considered a cost center within the system house, and it should not be expected to pay its own way.

Next, questions arose concerning the use of captured IC fabrication facilities within the semiconductor industry. Mr. Callahan (Motorola) has continuously suggested a need for this mode of operation, as a means to obtain custom military IC structures. Contrasting with this view, Prof. Kennedy has suggested that an industrial pilot facility could be used for small quantity IC manufacturing, thereby eliminating the need for a captured facility. In his view, a pilot line operation is geared to small quantity fabrication; it has a greater flexibility in its mode of operation; and every semiconductor company has a pilot line for manufacturing "back-up". In short, the military IC products would represent a profit source from a facility that is now operated on an overhead basis.

Mr. Callahan's arguments against this view are exceedingly convincing. First, he stated that the pilot line at Motorola has been adjusted in size to accommodate the next 1-3 year market outlook. Any expansion of this facility to accommodate

military IC orders would be an added expense; an extra overhead cost that must be paid for by the military. In fact, Mr. Callahan contends that if he thought we had settled on a "forever" technology base, Motorola would not have a pilot line.

Mr. Callahan also stated an important problem of motivation, and its influence upon the success of an organization. In his experience, if a person spends 20% of his time on military projects and 80% of his time on commercial projects a serious problem will arise. This person will direct his attention toward the largest (commercial) effort, and the military problems will suffer. In his opinion, there cannot exist within a given semiconductor facility such mixed requirements. The entire facility (both engineers and managers) must be oriented toward the small volume military IC requirements, and totally divorced from commercial aspects of the business.

Again a question was raised concerning the use of major building blocks for military applications. Dr. Rudenburg suggested that 1 or 2 years ago the Air Force did a study on this topic, and the TRW 16 bit fast multiplier may have resulted from study recommendations. Beyond this particular effort, the attendees were unfamiliar with any positive attempt to organize the military IC needs into standard building blocks.

Mr. Callahan suggested that if such a standardization could be accomplished it would offer many advantages. Specifically, "if you could come up with 10 or 20 that would satisfy 90% of the military needs, that would be different that doing 2000 of a custom type." The advantages of this method are particularly true if it represented only 2% of the semiconductor market. If things were done in this way the military would get a "good shot" at getting IC's fabricated by industry.

One attendee raised questions concerning the need for a standard product, in contrast with the use of standard processes. Thereby, a library could be developed for standard processes that have been proved,* and processes selected that offer a multiplicity of industrial sources. In short, use standard processes and create design tools that take advantage of this standardization.

Mr. Callahan claims this technique of custom IC design is impractical. Even small process changes are important, and unproven. He stated that there are several different design approaches:

1. use a standard process to organize standard circuits into a custom array;

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*Note: This approach to the custom IC design problem has been proposed by Dr. C. Gwyn, Sandia Labs (See Appendix IV).

2. custom design circuits, and use a standard process for their fabrication; and
3. custom design circuits that use a non-standard process.

This last technique introduces questions of reliability, no matter how small the change may be.

This reliability question introduces some serious problems. For example, he suggested we consider the question of a change in oxide thickness to modify the threshold voltage of a MOSFFT. Such a change could be trivial, yet it produces a serious reliability exposure. The 10,000 Å metallization used for fabrication may not cover an increased oxide step, although 4 devices out of 1000 may be satisfactory. These satisfactory IC's may pass tests, yet they represent a serious reliability exposure.

It was also stated by Mr. Callahan that design ground rules could be established to eliminate problems of this type, but we don't have them today. Most design systems do not take into account the fine points of IC design that are known to be important throughout the entire semiconductor industry. As a consequence, if you want to use my process (as is) that is acceptable; if not, I have no way of knowing what the consequences will be.

Dr. Thun raised questions concerning a problem he has encountered in his procurement of IC's from the semiconductor industry. He stated that system specifications are initially based upon the characteristics obtainable from a given process. If in a year or two he needs more devices of the same type, the process has changed and these structures are no longer attainable. The buyer doesn't care how the manufacturer meets the circuit requirements, but he does know that he cannot take the responsibility to undertake a circuit redesign at this late date. All that is required on the part of the manufacturer is to change his processes to its original form and, thereby, meet the specs of the new order.

Mr. Callahan confirmed that this represents a real problem. If you design an IC based upon a given process, there is little (or no) assurance that this process will remain stable. IC manufacturers are continually changing the process as a means to improve the yield of their commercial products. As a consequence, if a customer uses only a limited range of the original distribution there is no way to determine if these structures will be available at a later time.

One workshop attendee commented that this is not a hypothetical situation but, in fact, is real. He has encountered this type of situation on several occasions over the past few years.

At this point Dr. Rudenburg suggested that the problem of pulling out old process instructions and trying to follow them is not unlike a completely new manufacturing start-up cycle. As a consequence, the high production houses do not dare to undertake such a task -- even if the changes are only minor modifications of their current process. He suggested that in most cases this change would involve a modification of the time associated with a given operation, and not the temperature. Nevertheless, any change represents a major difficulty. It was stated that in today's state-of-the-art, a retrace problem of this type is no different than doing a new design: trying to put into production something that requires a new set of fabrication instructions.

It was stated that this retrace problem requires a level of discipline not frequently encountered in IC manufacturing. As a consequence, many computer aids are required. The nearest to this required discipline was found at Collens over past years; all the required data were in storage. This computer system would distribute process steps and past experimental data, and remove all others -- it worked reasonably well.

Thereby, having extensive data on process measurements the task could be accomplished: test pattern readings, etc. Dr. Rudenburg stated that if this task was accomplished with people, and we depended essentially upon their memory, there

is always a long learning curve. If, instead, the task is done using computer aids there are examples where this learning curve is very short.

Despite this discussion, Mr. Callahan stated that if someone says they want to change our (Motorola) production line, we won't even talk to them. We have enough trouble keeping it the way it is! If a custom design is manufacturable on an existing line, this is satisfactory.

In his view there are two ways to design a custom IC:

1. rigorously characterize the process and design circuits about it; or
2. redesign the process to meet the circuit needs.

Mr. Callahan stated that in his view the first path is the easier to follow.

At this point questions arose about the availability of such information from Motorola. In answer to these questions, Mr. Callahan stated that all you need to know are the parameters necessary to characterize and design your circuits. He stated that there are certain things that we (Motorola) will openly give the customer: junction depths, sheet resistance measurements, etc. Contrasting with this type information, I am not going to tell you how I clean my wafers, or my oxidation procedures, etc.: these are the witchcraft aspects of our process, and they are proprietary -- we won't

tell anybody. Our circuit designers do not need this type of information, and I don't think our customers need it in order to design their circuits.

Next, questions were raised about the Motorola attitude toward production line changes if, indeed, there was available a capability to immediately return the line to its original state -- without a yield change. Mr. Callahan stated that he was not sure. Probably if the production line was operating at 80% capacity, such changes would be done; if the line was running at 110% capacity -- in no way would the changes be introduced.

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Under ARPA Grant MDA903-74-G5, the University of Florida, Gainesville, Florida, has undertaken a program of study on the topic of Computer Engineering of Integrated Circuits. The purpose of this program was to identify problem areas associated with the design and development of integrated semiconductor circuits; problem areas that result in excessive cost and inadequate availability of the particular type electronic structures required by the DoD. An additional purpose of this study is to recommend a program of research and development directed toward alleviating the identified problem areas.

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This project was undertaken with full recognition of the complexity of the task at hand. It was also expected that a diversity of opinions would be encountered concerning the real source of existing DoD IC procurement problems. This expectation was realized; therefore, many conclusions presented here represent the most prevalent opinions drawn from numerous scientists and engineers actively working in the field of semi-conductor integrated circuits. Among these individuals are representatives from many industrial organizations engaged in IC design, development, and manufacturing. In addition, among these individuals are representatives from various branches of the DoD, and from several academic institutions engaged in research of particular value to the goals of this program.

As with any effort of this type, I am indebted and owe thanks to many people who have contributed their time and effort to this project. In particular, special thanks are due to all members of the program Steering Committee who undertook hours of extra work in their desire to assure the success of this study program.