RADC-TR-75-278
Final Technical Report
February 1976

RELIABILITY EVALUATION OF PROGRAMMABLE READ-ONLY MEMORIES (PROMs)

Hughes Aircraft Company

Rome Air Development Center
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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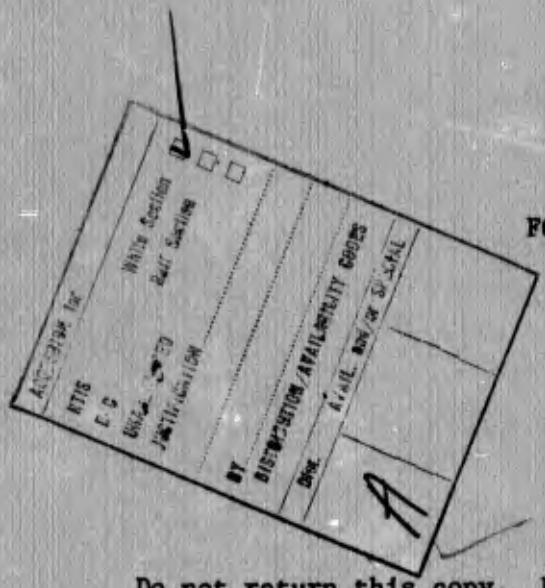

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REPORT DOCUMENTATION PAGE

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1. REPORT NUMBER: RADC-TR-75-278	2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE *(and Subtitle)*: RELIABILITY EVALUATION OF PROGRAMMABLE READ-ONLY MEMORIES (PROMs).	5. TYPE OF REPORT & PERIOD COVERED: Final Technical Report. 4 Mar 74 – 3 Mar 75
	6. PERFORMING ORG. REPORT NUMBER: N/A
7. AUTHOR(s): T. M. Donnelly, W. W. Powell, C. M. Dewitt, III, D. R. Jerand, M. Penberg, K. L. Wong	8. CONTRACT OR GRANT NUMBER(s): F30602-74-C-0156
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Hughes Aircraft Company, Data Systems Division, Culver City CA 90230	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 62702F, 55190457
11. CONTROLLING OFFICE NAME AND ADDRESS: Rome Air Development Center (RBRM), Griffiss AFB NY 13441	12. REPORT DATE: February 1976
	13. NUMBER OF PAGES: 268
14. MONITORING AGENCY NAME & ADDRESS *(if different from Controlling Office)*: Same; AF-5519; 551904	15. SECURITY CLASS. *(of this report)*: UNCLASSIFIED
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT *(of this Report)*

Approved for public release; distribution unlimited. 288 p.

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

Same

18. SUPPLEMENTARY NOTES

RADC Project Engineer:
James J. Dobson (RBRM)

Available in DDC.

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

Reliability	Life Test	Nichrome Fuse
Memory	Failure Rate Model	Titanium-Tungsten Fuse
PROM	Memory Programming	Avalanche-Induced-Migration
Screening Test		

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

(See Reverse)

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This final report presents the results of a study performed by the Data Systems Division of Hughes Aircraft Company under Rome Air Development Center Contract No. F30602-74-C-0156. The primary objectives of this study were to: (1) assess unique factors affecting the reliability of 1024-bit open collector programmable read-only memories (PROMs) from three technologies, i.e., nichrome fusible links, titanium-tungsten fusible links and avalanche induced migration (AIM) or "blown diode" technology; (2) recommend programming, testing and screening guidelines for the subject PROMs; and (3) develop a failure prediction technique for the subject PROMs.

Before the start of this study, public information regarding PROMs was almost non-existent; available information tended to vary considerably as to conclusions regarding the reliability of various PROM technologies. To develop a comprehensive understanding, therefore, during the study it was necessary to perform a circuit review of each device type, programming experiments and microscopic analyses. Also an extensive effort to collect data from various PROM users and vendors was made.

Experiments conducted on the nichrome fuse PROMs resulted in a correlation between fuse gap appearances and times-to-program. Fuses that exhibited long fingers or strands in the open gap region were predominantly seen in one manufacturer's devices using programming times in the 10 to 150 μs range. These fingers get progressively shorter, and the gaps get progressively narrower in the fuses that experienced longer blow time conditions. Fuses with long blow times have a higher probability of reconduction. Based on user data and experiments performed, the programming schedule of two programming pulses of 100 μs rise time and 10 ms in length appeared to be a good compromise for optimum programming yield and reliability for nichrome fuse PROMs. In this procedure a single programming pulse is applied to all the fuses to be programmed, and a second pulse is then applied to those fuses which would not program on the first attempt. During the second pulse time, current losses due to parasitic leakage paths are minimized. The probability of reconducting fuses occurring during operational usage is reduced by the short pulse time.

Data from tests of specially fabricated nichrome fuses and theoretical studies on reconducting fuses led to the conclusion that temperature and voltage across the fuse gap would accelerate reconduction. High temperature operational burn-in appears desirable; however, not all potential reconducting fuse failures were culled out in a 168-hour dynamic burn-in test conducted. One failure was found to occur after 600 hours of operation at 125^{o}C ambient.

One user reported that moisture penetrating through cracks in the passivation caused electro-corrosion of nichrome fuses. Subsequently, he used the "freeze-out" test, described in Mil-M, 38510/201, to cull out essentially all the bad parts in the lot. This led to the conclusion that the "freeze-out" test should remain in the specifications until the products could be proven otherwise.

Severe limitations on programming experiments were encountered on two of the technologies studied. Because of internal programming control circuits on the Ti:W fuse PROMs, variations in external programming pulse waveforms such as amplitude to control the currents flowing through the fuses were not attainable. For the AIM technology, existing microanalysis techniques were found to be limited for analysis of structural changes in the diode junction. Therefore, information provided in this study regarding these two technologies was developed primarily through literature search and user and vendor contacts. Currently, 1024-bit PROMs using Ti:W fuses are available in plastic packages; mil-temperature range devices in hermetic packages will be available in late 1975. Reported cases of reappearing bits experienced on Ti:W fuses were associated with internal programming anomalies on the chip which resulted in several fuse failures occurring in one device. SEM analysis of the Ti:W fuse revealed a strong reaction between the passivation and fusing zone during programming leaving non-etchable debris near the gap. Data gathered during the study on the AIM technology revealed that no definitive description of the mechanism responsible for shorting a diode during programming could be identified. This was further supported by the vendor, who indicated that no internal research on his behalf had identified the true mechanism except that aluminum at the emitter window is an important ingredient.

Programming yield data collected on more than 50,000 1024-bit PROM devices, indicated a general programming yield of 90 percent. This yield can be higher or lower depending on the source of programming, programming equipment, programming criteria, etc.

Data gathered for developing contributory factors to a failure rate model indicate that with optimum programming and screening, the PROM failure rates are in the same order as comparable ROMs. The failure mechanisms unique to nichrome memory elements could contribute from a few percent to 20 percent of the total failure rate for 1K and 2K PROMs. Failure rate models utilizing the Mil-Hdbk-217B ROM model as the starting point and including additional contributory factors associated with unique PROM features were developed.

PREFACE

This final report is the culmination of a 12 month Study on Reliability Evaluation of Programmable Read-Only Memories (PROMs) commencing 4 March 1974 and terminating 3 March 1975. It is submitted in accordance with the provisions of Exhibit A Line Item A002 for Contract No. F30602-74-C-0156.

The contents of the report represents the fulfillment of the above contract by the Data Systems Division of Hughes Aircraft Company and does not necessarily represent the recommendation, conclusions or approval of the United States Air Force.

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Special acknowlegement is made to the following persons for their contribution to this study.

J.R. Devaney and A.M. Sheble, Hi-Rel Laboratories, for their extensive microanalysis effort.

Dr. R.S. Mo, Xerox, for making available a wealth of information on his pioneering work on PROMs and specially fabricated fuses as well as failure rates.

R.D. Mobley, Collins Radio Group, for making available PROM failure data and SEM photographs.

B.W. Murry, Honeywell Information Systems, for contributing SEM photographs.

R.S. Foote, Information Storage System, for contributing optical photographs and failure rate information.

P.G. Franklin, Monolithic Memories, Inc., for making available information on PROMs and specially fabricated fuse investigation.

Thanks also goes to all of the PROM users and vendors contacted. This group, whose names are presented in the Appendix, contributed valuable information as well as technical consultation.

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EVALUATION

The prime objective of this study was to establish effective reliability procedures for testing, qualifying, and screening microcircuit programmable read-only memories (PROMs). This study evaluated programming fusing methods and materials to assess their reliability. A failure rate prediction technique was developed for PROMs and an effort was made to establish future limitations and trade-offs as a function of technologies, complexities and screening.

The major conclusions of the study are that programming methods should be carefully controlled and that the use of the "freeze-out" test as described in MIL-M-38510/201 should be continued. Fuses that require long programming times show smaller fuse gaps, and are more susceptible to reconduction or "regrowth." Fuses that take shorter times to blow have wider gaps and do not show reconduction failures.

The study concluded that the rise time of the programming pulse should be kept relatively long, from 50 to 100 microseconds. The pulse width itself should be kept relatively short, 10 milliseconds maximum. One programming pulse should be applied to each link that is to be programmed, cycling through the addresses. The PROM can then be checked, and fuses that fail to program on the first pulse can be hit with one more pulse. If it fails to program on the second pulse, the part should be rejected.

The findings of the study will be used in the preparation of MIL-M-38510 detail specifications for PROMs. The tests and programming methods will be added to MIL-STD-883 and the failure rates will be incorporated into MIL-HDBK-217B.

James J. Dobson

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Solid State Applications Section
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1.0 INTRODUCTION

Purpose of Study

This final report presents the results of a study performed by the Data Systems Division of Hughes Aircraft Company under Rome Air Development Center Contract No. F30602-74-C-0156. The primary objectives of this study were to:

- Assess unique factors affecting the reliability of bipolar Programmable Read-Only Memories (PROMs) of three different memory element technologies
- Recommend programming, testing and screening guidelines for the subject PROMs
- Develop a failure rate prediction technique for the subject PROMs.

A PROM, by design, requires the application of an electrical programming pulse to change the resistance of its memory elements permanently to the desired levels representing either a "0" or "1" state. Programming can be done by the supplier, the distributor or the user. If a user does it, he may assume the responsibility of determining the integrity of the device through proper programming, verification and testing after programming, and additional screening, such as burn-in, to cull out infant mortality failures. Whereas, for ordinary integrated circuits the supplier would assume the total responsibility for providing a reliable part.

Before the start of this study, evidence showed that programming and memory element technologies were interdependent functions that directly affect the achievement of reliability. This evidence was first reported on devices employing nichrome thin film fusible links, since this was the first of the current PROM technologies. Two failure modes for these devices were identified. One is known as reappearing bits or more universally known as "growback" and the second known as self-programming in which an unprogrammed fuse becomes open due to electrochemical corrosion. These failure modes were reported by many users and manufacturers, who gave conflicting opinions and conclusions as to their causes and cures. The conflicting opinions were in part due to the limited capabilities of existing failure analysis and microscopy equipment to analyze the tiny 1/2 μm

gap width of a programmed fuse and the fact that many users and manufacturers did not publish data concerning their findings. The rate of programming energy applied to the fuse appeared to be strongly related to the "growback" probability.

This experience with early PROMs cast doubt on their reliability, not only on those of the Nichrome Fuse Link technology but on all the technologies that followed. Most of the experiments, which had been conducted to develop concepts relating to programming techniques, had been performed on fusible links deposited on test chips in order to be able to apply experimental energy waveforms to the fuses. Although these tests provided some answers concerning programming and reappearing bits, other questions remained unanswered regarding conditions introduced by the programming and read circuitries used on actual PROM devices.

This PROM Reliability Evaluation was conducted to gain sufficient confidence in the reliability of PROMs to permit their use in critical military applications and to assure the achievement of high reliability in the devices by optimum programming techniques and screening tests.

Scope of the PROM Reliability Evaluation Study

This study was conducted utilizing as vehicles 1024 bit bipolar PROM devices from three technological types: Nichrome Fusible Links, Titanium-Tungsten Fusible Links, and Avalanche Induced Migration (AIM) or "Blown Diode" Technique. Nichrome PROMs from two suppliers and the others from one supplier each were utilized. Three specific areas were investigated:

1. Programming and Electrical Test
2. Programmed and unprogrammed fuse reliability
3. Reliability Math Modeling

Within these three areas, the following specific tasks were accomplished.

1. Programming and Electrical Test

    a. The unique electrical test problems associated with PROMs were determined. (Investigation of general electrical characteristics, such as switching and DC parameters was outside the scope of this study.)

b. Methods of programming elements and their eventual reliability were evaluated for each device.

c. Concepts for optimizing programming yield and reliability were developed.

d. Variations in programming pulses such as fusing currents, pulse waveforms and their effect on fusing were studied.

2. Programmed and Unprogrammed Fuse Reliability

a. Failure mechanisms associated with each memory element technology under study were identified.

b. The effects of programmed and unprogrammed memory elements on the reliability of the device were studied. Problems such as electro-chemical and reconduction fuse failures were included in the study.

c. Material and geometry characteristics of fusible links and AIM technology were determined.

d. Screening concepts for PROM reliability enhancement, including an evaluation of the "Freeze-out" test, were developed.

3. Reliability Prediction Math Model

a. Historical, field, and test reliability data were collected for use in estimating values of parameters selected in development of a reliability prediction math model.

b. Various failure mechanisms were evaluated for their effect on the ultimate failure rate of PROMs.

c. A failure rate math model, compatible in format with Mil-Hdbk-217B models, was formulated.

Historical Background of PROM Technologies Studied

The first field Programmable Read Only Memory (PROM) was introduced in early 1970. Today there are four different bipolar PROM technologies, at least 11 manufacturers, and more than 40 device types ranging from 256- to 4096-bit memory capacities. Some users are presently working with manufacturers on the design of 8K and 16K PROM devices. Basic variations in technologies relate to methods used to store a non-volatile memory bit. Memory elements may consist of either nichrome fusible links, titanium-tungsten fusible links, polysilicon fusible links, or a reverse-biased emitter-base diode utilizing what is known as the Avalanche Induced Migration (AIM) technology. The three technologies studied are further discussed below.

Nichrome (NiCr) Fusible Links – The use of nichrome as thin film resistor elements was first adopted in 1960 in microcircuit fabrication. These resistor elements have been the subject of many studies concerning nichrome properties and their reliability. The deposition of nichrome thin films in devices was not new; however, the application of nichrome as a programmable fusible link was new when first introduced in April 1970. With a growing demand for PROM devices, several semiconductor manufacturers entered the market, many of whom also used a nichrome fuse as a memory element. These elements may vary in configuration, thickness or composition. Basic to each design is the application of a programming current pulse of sufficient energy to produce a non-conductive gap region in the fuse while preventing damage to the surrounding oxides and substrate silicon. Failure to accomplish an optimum fusing condition results in decreased reliability. Failure can be caused by insufficient current supplied to the fuse which in turn is affected by material variations and by circuitry limitations. The contributing factors include:

1. Variations in β across the Si wafer and inadequate breakdown voltage levels in the programming circuitry
2. Poor fuse delineation provided by the photoresist process
3. Variation in thickness of the nichrome fuses
4. Variation in nichrome composition
5. Effects of minor contaminants, especially alkaline contaminants in the etchants
6. Distance of the nichrome fuse from the fusing circuitry.

Of the manufacturers studied, two use Nichrome fusible links. Each manufacturer has implemented changes to his 1024-bit PROMs. One manufacturer made major changes during September 1972 and the other in June 1973. Both changes were aimed at improving programmability and reliability. Some of the changes were

1. Use of a new process to provide tighter control of the cross-sectional area of the fusible link.
2. Implementation of a new screen utilizing a bias to test fusible links contained in each device (not accessible to users)

3. Verification of programmed patterns utilizing a reduction in power supply voltage (approximately 4 volts)
4. Utilization of double masking to reduce pinholes.

A complete account of each manufacturer's design and process changes as well as internal screening procedures is difficult to obtain because of the proprietary nature of the information.

Titanium-Tungsten (Ti:W) Fusible Links – First introduced in late 1973, PROMs utilizing Ti:W links have also undergone many design and process changes to increase the current density delivered during fusing. Essentially all the factors that affect NiCr fusible links also affect Ti:W links. In 1975, a special electrical screening test was implemented for 256, 512 and 1024-bit PROMs to cull out devices that would self-program by internal leakage current. Process controls on the cross-sectional area have also been revised to maintain the narrow, 0.07 mil, fuse neck width. As of April 1975, PROMs utilizing Ti:W fuses have not been available in a Mil temperature range device; however, they are expected to be offered in late 1975.

Avalanched-Induced Migration (AIM) – Using an earlier approach of programming diode matrices, the AIM device was introduced in September 1971. The AIM technology utilizes one of two back-to-back diodes in a floating base transistor configuration to serve as the memory element. Programming is accomplished by shorting the emitter-base junction. The AIM technology has also experienced a learning curve incorporating the following changes:

1. January 1972 – the chip was reduced in size to improve speed and increase programming yield.
2. February 1973 – circuitry changes were made to improve chip enable speed and reduce programming path resistance and required voltage.
3. June 1974 – the number of after programming pulses which are applied after the emitter-base short has been sensed was reduced to prevent degradation of the base-collector junction.

2.0 PROM MEMORY ELEMENT STRUCTURES

The PROM memory element structures encompassed by this study are

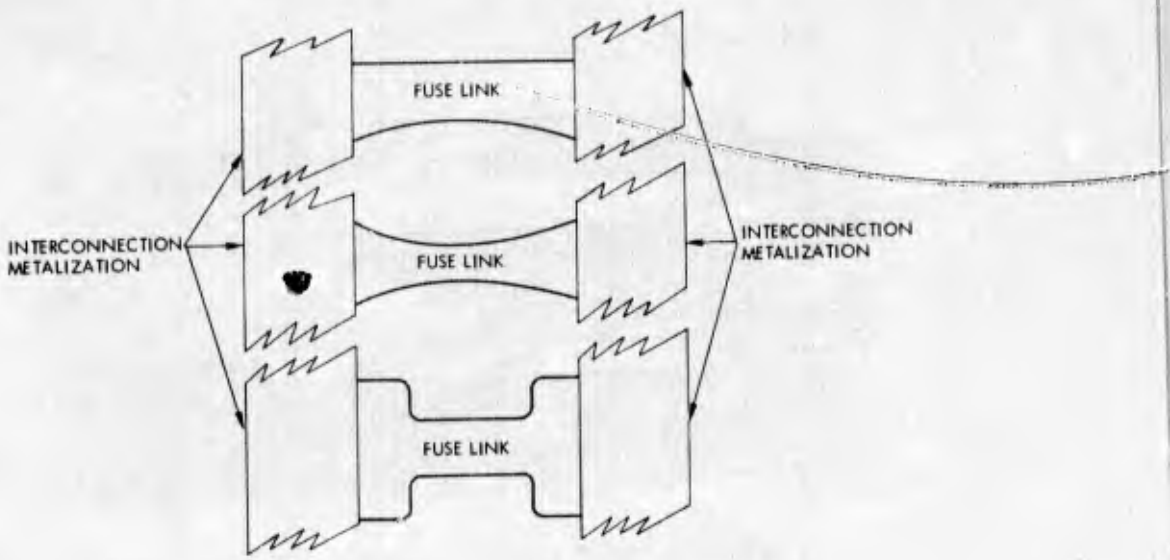
1. Fuse Link PROMs, employing either nichrome (NiCr) or titanium-tungsten (Ti:W) fuse materials
2. AIM (avalanch-induced migration) PROMs, conventionally referred to as "blown diode" fuses

A survey of available Fuse Link PROMs indicates that a variety of different shaped fuse links are used throughout the semiconductor industry. In part, these differences occur because of fuse material selection and/or composition. Programming reliability is also a factor. Fuse link material thickness, cross-section, length between opposed termination pads, resistance, etc., all may affect fuse link ease of fabrication, programmability and ultimate reliability. Material selection and associated fabrication processes do affect the occurrence and frequency of potential failure modes such as unprogrammed "opens" and "growback" links or unwanted "shorts." An understanding of fuse configurations, materials and processes is, therefore, quite necessary in generating an accurate picture of PROM device reliability. Top views and a sectional view of a fuse link along its length are shown in Figure 1; the vertical scale is exaggerated for clarity.

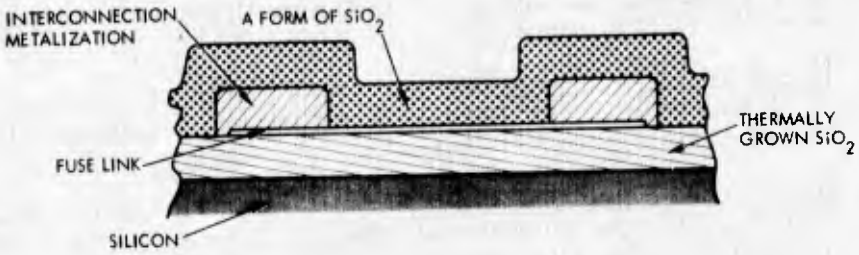
The AIM or "blown emitter-base" junction PROM is quite different in concept and configuration from that of the conventional fuse link type PROM. In effect, the programming pulse or pulse train is used to blow one diode of a "back-to-back" diode pair. The supplier of these devices indicates that the programming phenomenon is not a surface mechanism occurrence, but one that occurs a micron or more below the surface of the device, within the bulk silicon itself. Programming of these devices by high current pulses causes the emitter N/P junction to short permanently. A vertical sectional view of an AIM memory element with vertical scale exaggerated for clarity is shown in Figure 2.

Nichrome Fuse Technology

Nichrome (NiCr) was an obvious first choice as the fuse material for PROM devices because it has a wealth of literature behind it as a known



a. Top views of various fuse links.



b. Sectional view of fuse link.

Figure 1. Fuse links.

resistor material. Various evaporation techniques are well documented, including a variety of percentage combinations with predictable TCRs. NiCr adheres well to the SiO_2 surface of semiconductor devices. Standard etchants can be used. Experience on IC's, however, has shown that NiCr is susceptible to electro-corrosion mechanisms that occur when moisture reaches the surface of the NiCr through pinholes or cracks in the protective glass overcoat layer.

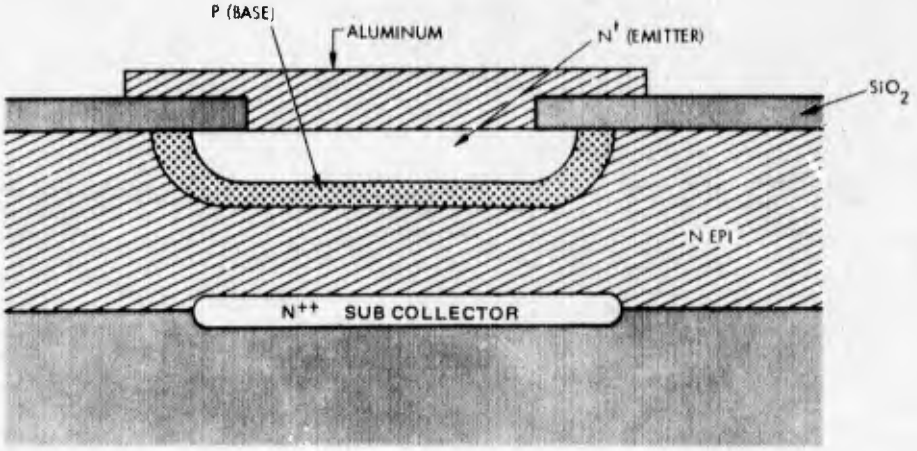


Figure 2. AIM memory element, sectional view.

The characteristics of this technology are detailed below:

1. Wafer Oxide Thickness. The thermally-grown Si wafer oxide coating is 6000-8000 Å thick.

2. Nichrome Fuse Dimensions. In the neck region the fuse is 0.15 to 0.20 mil wide. The fuse is 0.4 to 1.0 mil long and the NiCr fuse material is 150 to 250 Å thick.

3. Nichrome Deposition Method. No metal interface material is used beneath NiCr to improve adhesion. Thermal evaporation is used to deposit NiCr on PROM wafer, followed by annealment at elevated temperature. Actual annealment temperature and duration are considered proprietary information by suppliers, as this process is used to provide a homogeneous distribution of both nickel and chromium within the fuse material film, thereby reducing programming problems. Suppliers use crystal oscillator film thickness monitoring instrumentation for real-time monitoring of NiCr depositions.

4. Nichrome Film Composition. Spectrographic analysis is used to verify the composition of the nichrome films. One supplier using nichrome fuses states that the most stable fuses which provide the most repeatable programming results are those made of approximately 50 percent Ni and 50 percent Cr films. The exact composition is considered proprietary by the suppliers.

5. Fuse Termination Pads. Aluminum is used as the termination pad and conductor material contacting each end of the nichrome fuse link. Termination pad thickness is approximately 1 micron. The width of conductors making contact with fuse termination pad ends are approximately 0.4 to 0.5 mil. No undercoat film is used to improve adhesion of the aluminum conductor/termination pads. No information is available on the contact resistance between the aluminum termination pads and the nichrome fuse links.

6. Fuse Overglass. The overglass is composed of phosphorous-doped silox and is approximately 1 micron thick.

   The fuse overglass is inspected for pinholes following completion of the silox processing. PROM wafers are examined under a zoom microscope at magnifications of more than 100X. In general, no additional tests are used to ensure overglass film integrity, such as submersion in a metal etch solution of quality control test samples.

7. PROM Die Separation. Diamond, laser and single-wheel saws are used to separate wafers into PROM dies.

8. Fuse Programming Test Information. Fusing temperature in the fuse "neck" region has been calculated at approximately 1600°C, which is several hundred degrees above the melting point of this material. Fusing voltage is approximately 7 to 8 volts; fusing current densities have been estimated at $2 - 5 \times 10^7$ amp/cm^2. Every PROM device is tested at both the wafer and die level; each 1024-bit PROM has approximately 50 test fuses per chip which can be programmed to verify "good" chips. These test fuses permit both row and column checks.

9. Fuse Resistance Values. Resistance of the NiCr film centers around 100 ohms/square; actual fuse values are between 300 to 500 ohms including photoresist/photoetch processes variations. When programmed open, the fuse resistance should be in the meg-ohm region with workable minimum down to around 4000 ohms.

Titanium-Tungsten Fuse Technology

The titanium-tungsten (Ti:W) fuse technology is presently being pursued by one PROM supplier only. Initial user results are quite promising; however, the number of Ti:W-fused PROMs in use at this time is small compared to nichrome-fused devices; Ti:W devices are as yet unavailable in Mil-Std approved packages.

Ti:W has excellent etchability properties that permit accurate definition of very small fuse geometries. Ti:W films form protective oxides (TiO_2 and WO_3) when exposed to oxygen sources; formation of such oxides improve adhesion of Ti:W fuse material to SiO_2 surfaces. Ti:W fuse material should be highly resistant to electro-corrosion caused by moisture penetration of minute pinholes or cracks in the SiO_2 overglass, due to the high tungsten percentage of the fuse material. The 800-1000 Å thick Ti:W fuse structure provides fuses which have very uniform resistance values which are easier to attain than when a substantially thinner film of 200 Å is employed.

The extremely small geometry of the Ti:W fuse link could create problems in establishing a tight nominal resistance value for the fuse links, which in turn could affect programming techniques and results. Evidence exists that quartz overglass is necessary to prevent Ti:W fuse oxidation during package sealing operations. Exposure of the Ti:W fuse material to O_2 at elevated temperatures (approximately 425°C) will cause substantial changes in the fuse resistance value, which in turn affects fuse programming voltage and current requirements. Also Ti:W is brittle. Cracks have been shown to develop, which can open Ti:W fuses, after a PROM die is ultrasonically cleaned subsequent to glass removal, during sample preparation for SEM analysis.

The characteristics of this technology are detailed below:

1. Wafer Oxide Thickness. The thermally-grown silicon wafer oxide coating is 5000 to 6000 Å thick.
2. Ti:W Fuse Dimensions. The neck region is 0.06 to 0.09 mil wide. The fuse is 0.2 to 0.3 mil long and the Ti:W fuse material is 800 to 1000 Å thick.
3. Ti:W Deposition Method. Platinum silicide is used as an interface material beneath the Ti:W layer to improve adhesion; the thickness of this layer is approximately 400 Å. The Ti:W film is sputtered onto the PROM wafers, which are heated during the sputtering process to improve film adhesion. Exact annealing temperature was not disclosed.
4. Titanium-Tungsten Film Composition. The sputtered Ti:W fuse material is comprised of 10 percent Titanium and 90 percent Tungsten. A proprietary photoetch process, using hydrogen peroxide, is used to define the 0.06 to 0.09 mil fuse geometry. The extremely narrow fuse neck design was necessitated by the relatively low resistance of the Ti:W material combination, which would have required in excess of 100 milliamps to blow a fuse of Ti:W which had the same width as most nichrome-fused PROMs.
5. Fuse Termination Pads. Aluminum is used as the termination pad and conductor material connecting one end of the fuse to the address circuitry; the other end of the fuse is connected to the emitter contact of the fuse isolation transistor. Termination pad thickness is approximately 12,500 Å. The width of the conductors making contact with fuse termination pad ends is approximately 0.4 mil in the fuse area. To improve aluminum adhesion 800 to 1000 Å of Ti:W fuse material is deposited by sputtering beneath termination pad areas.

6. Ti:W Fuse Overglass Information. This supplier uses two different passivation approaches. PROMs which are packaged in plastic packages are protected with a quartz overglass, which is deposited by sputtering process. PROMs which are to be packaged in hermetically sealed packages are protected with a coating of SiO_2 deposited by the SILANE process. Quartz overglass thickness is estimated at 10,000 to 12,500 Å. The quartz overglass is inspected for pinholes by examination under a 40 X microscope. No other method of determining the presence of pinholes or cracks in the overglass is employed.

7. PROM Die Separation. Laser scribing and roller breakout are used to separate PROM dice from each other; this process is followed by a visual inspection to eliminate damaged devices.

8. Ti:W Fuse Programming Test Information. Fusing temperature in the fuse "neck" region has been calculated at approximately 3300°C; fusing current has been measured at 40-70 milliamps. Every Ti:W PROM device is tested at both the wafer and die level; each 1024 bit PROM has 65 test bits per chip, which can be programmed to verify "good" chips. These fuses are used for both row and column checks.

9. Ti:W Fuse Resistance Values. Resistance of the 800 to 1000 Å thick Ti:W fuse is nominally 50 ohms. When programmed open the fuse resistance should be in the meg-ohm region.

Avalanched-Induced Migration (AIM)(Blown Diode) Technology

The junctions of the back-to-back diode pair memory element are inherently sealed against environmental effects as it lies beneath the VAPOX, aluminum film, and N^+ diffusion layers. Current is forced through the element before and after programming to assure that the element has been properly programmed. Each bit is operated at a current level that is 1/400th of the programming current used to short the emitter-base junction. No special fuse material combinations or deposition controls are required to achieve a reliable bit programming technology; AIM technology employs standard semiconductor processes throughout.

The necessarily close proximity of emitter-base junctions to their associated collector-base junctions requires very close control of reverse current pulses used to short or program a bit. Improper programming can create conditions of "OVERBLOW" forming a conductive link between the collector-base junction, thereby shorting a row line to a column line.

The characteristics of this technology are detailed below:

1. Device Configuration

a.	Device density	0.8 mil centers
b.	Emitter depth	1.8 to 1.9 μm
c.	Base thickness	0.3 μm
d.	Submerged N-type channel width	0.8 mil (subcollector diffusion)
e.	Submerged N-type channel depth	6 microns (depth of epi-thickness)
f.	Size of collector electrodes	0.5 x 1.0 mil
g.	Width of conducting columns or conductors	0.3 mil
h.	Approximate area of base-emitter junction area	0.2 x 0.2 mil

2. Dual Layer Metallization. Aluminum metallization is deposited in two layers, each layer is 10,000 Å thick. This process reduces "opens" across oxide steps in addition to improving conductor and termination pad uniformity.

3. Overglass Information. The use of overglass protection is a recent addition to the AIM PROM process, primarily used on Mil Spec devices; commercial PROMs are not supplied with overglass protection as the supplier feels that his devices do not really need this additional layer of protection. Those devices supplied with overglass protection are subjected to a variation of the VAPOX process; the overglass consists of a sandwich structure consisting of VAPOX layer – phosphorus-doped glass layer – Vapox layer. This sandwich structure is approximately 10,000 Å thick. This overglass structure is annealed at 425°C for 4 minutes during the aluminum metallization alloying process. Each PROM wafer is subjected to a visual pinhole count to ensure the protection afforded by the VAPOX process. Sample quantities of PROM wafers are put through a metal etch solution to check the effectiveness of the overglass protective layer.

4. PROM Die Separation. Tempress scribe and break are used to separate PROM dies.

5. Memory Element Junction Resistance. Normal resistance of the junction is in the 1000 meg-ohms region. Program shorted junction resistance is less than 10 ohms.

3.0 PROM CIRCUIT DESCRIPTIONS

The circuit schematics were studied to gain an understanding of the programming circuits and the ways that programming failures might occur, such as "would not program," "extra bits," and "slow to program." Of special interest are the test circuits included on the chip in the form of extra rows and columns. These circuits might be used in non-destructive tests to screen out parts which cannot be reliably programmed.

Vendor A

Read Circuitry – The chip layout is shown in Figure 3, and a skeletal outline of the circuit schematic is shown in Figure 4. The memory is organized into 256 words of 4 bits. The fuse matrix is, therefore, divided into four blocks representing the 4 bits. Each block consists of 32 rows and eight columns.

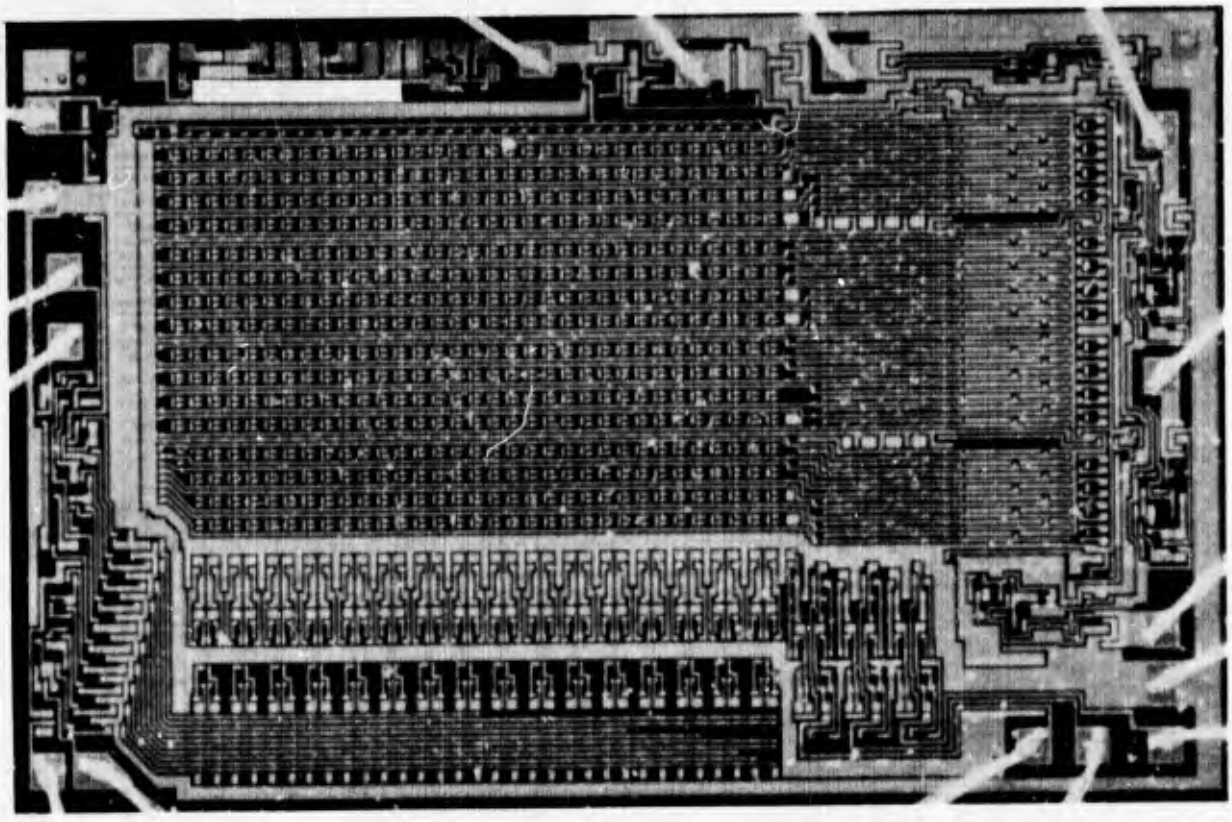


Figure 3. Vendor A 1024-bit PROM chip layout (74-27959).

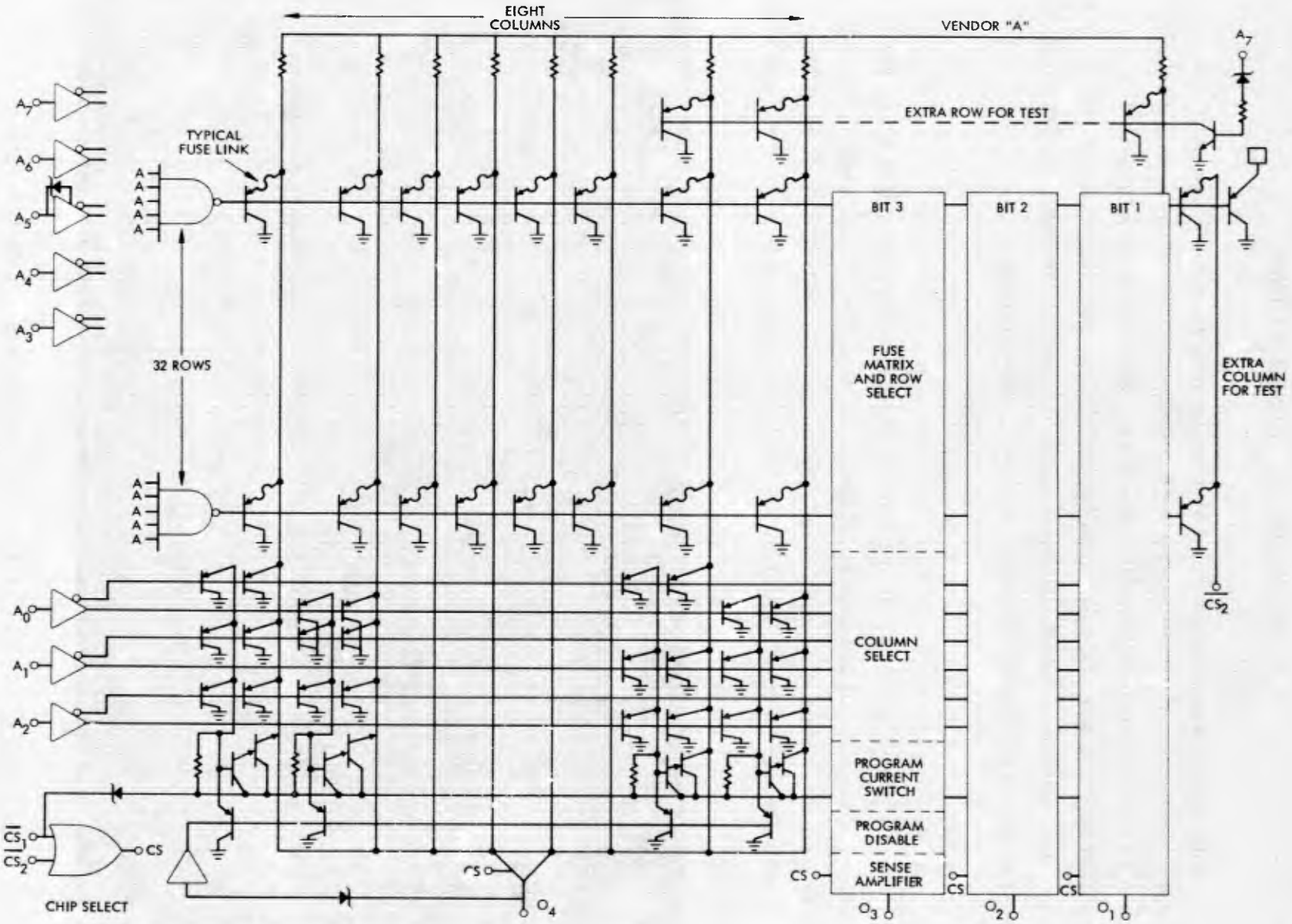


Figure 4. Vendor A 1024-bit PROM skeletal circuit schematic.

Addressing for reading out the memory is accomplished by selecting the required row and columns. The address inputs from the package pins are brought in through buffer drivers that generate both true and inverted terms.

Row select is accomplished by bringing the various combinations of these terms corresponding to A_3 through A_7 to 32 NAND circuits which are connected to row conductors which cross the matrix. The selected NAND circuit grounds its conductor, turning on a row of PNP select transistors which, in turn, grounds all the fuses in that row.

Column select is accomplished by a PNP transistor matrix driven by the A_0 through A_2 terms. The effect of this matrix is to ground all the columns in each bit except the selected one. Thus in each bit only one column can rise and drive the sense amplifier into which the eight columns are OR'd. This column will rise only if the selected fuse has been opened, breaking the ground connection provided by the row select. The stored information is then transmitted to the output pins provided the sense amplifiers have been activated by a chip select circuit by pulling both $\overline{CS}_1$ and $\overline{CS}_2$ low.

Programming Circuitry – Additional circuitry for programming the fuses is superimposed on that required for read out. Because of package pin limitations, the pins had to be shared for read and programming. The programming circuitry is invisible during normal operation because of the zener input diodes that operate at voltages higher than the normal TTL logic levels. Some of the circuitry is shared for both functions. Row select is accomplished by the same method described above. The correct column is selected by enabling the appropriate program current switch (see Figure 4). The inputs to these Darlington pairs are normally grounded by a program disable circuit that is controlled through zeners via the output pins. When the desired output pin is raised to 11 Volts, the program disable is removed for the eight switches associated with that bit. However, an additional column select transistor matrix associated with the read column select acts to ground the inputs to all the switches except that of the desired column. The read column select is also operative, grounding all the columns except the selected one.

The programming current is introduced through CS_1. When this pin is raised to 25 volts, current flows through the isolating zener diode to the collector bus of the program current switches, where it divides with the majority

of the current flowing through the base drive resistors of the 31 unselected current switches, and the remainder current flowing down the column conductor to the selected fuse and then to ground through the row select switch.

Test Circuitry – The programming of a PROM device may be considered the completion of its manufacturing process. This complicates the predelivery testing of unprogrammed parts. For this reason, test circuitry is included on the chip, which permits at least partial evaluation of the functioning of the address and sense circuits, access time, and fuse programmability.

In Vendor A's part an extra column and an extra partial row of fuses with their associated switches are provided. A row select switch is provided near the extra column which is connected to a probe pad used for wafer or die testing. A given fuse on the extra column can be selected using the conventional row select addressing. The extra column fuses are bussed to the $\overline{CS}_2$ pin so that their fusing characteristics can be measured independently of the column select and program current switches. After programming a pattern into this column, the functioning and possibly the speed of the row select circuits can be measured.

The extra row is selected by taking A_5 and A_7 pins to a high input voltage of 9 to 12 volts. The A_5 input buffer includes another isolation zener which, when operated at the high input voltage, takes both buffer output terms low. This deselects all the main storage rows. Taking A_7 high triggers another zenered circuit which selects the extra row. This row can now be read or programmed using the conventional column select circuitry to enable a functional test of the column select and sense circuits. The efficiency of the programming circuits can be evaluated by programming the extra row and observing the current waveforms and times required for programming.

A further measure of access time can be made by column switching between programmed and unprogrammed fuses in the extra row and measuring the transition delays at the outputs. A similar test can be made by pulsing the row deselect circuit associated with A_5 pin while cycling through the various address locations, this time treating A_7 as a normal address pin.

Read Circuitry – The chip layout is shown in Figure 5, and the circuit schematic is shown in Figure 6. This device is also partitioned into four 32 x 8 blocks. It differs from that of Vendor A in that a diode select matrix is used rather than a transistor matrix.

Row select is accomplished in a similar manner as Vendor A, except that a row of diode cathodes is grounded by the select transistor in this case. The desired column is selected by turning on one of eight series column select transistors in each bit block that connects the desired column to the sense amplifier buss. The column select transistors are controlled by diode gates operating on the A_0 to A_2 address terms.

If the selected fuse is unblown, the sense amplifier bus will be connected to ground and an output high results. The sense amplifiers are activated by an enable gate controlled by $\overline{CE_1}$ and $\overline{CE_2}$.

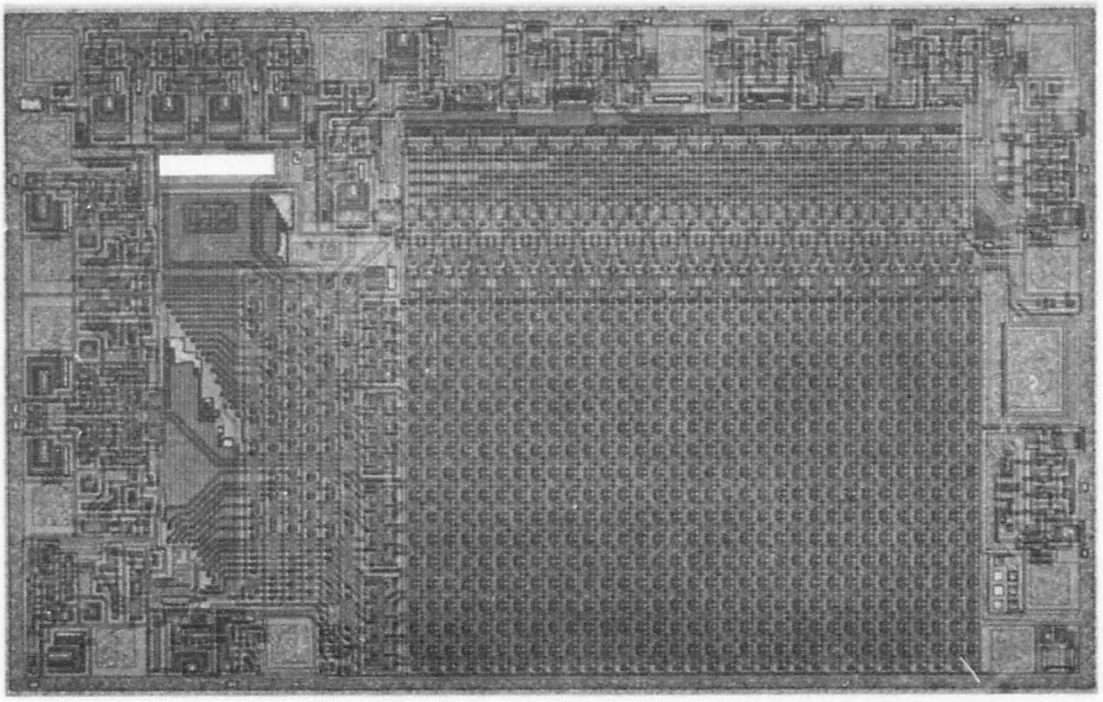


Figure 5. Vendor B 1024-bit PROM chip layout.

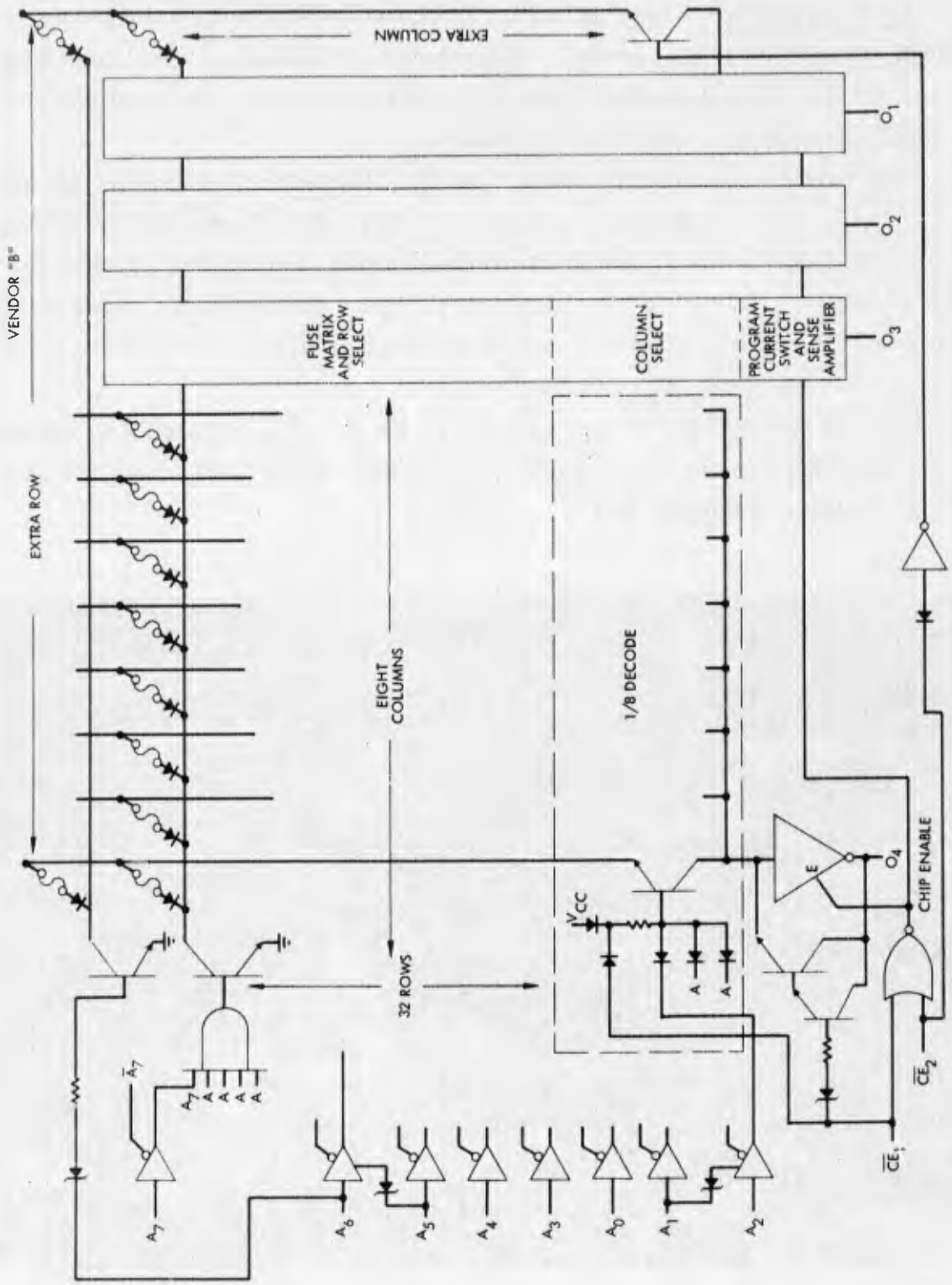


Figure 6. Vendor B 1024-bit PROM skeletal circuit schematic.

Programming Circuitry – This device also uses zeners to mask the programming circuits during normal operation. To program the device, the desired fuse is selected using the same row and column select circuits as in readout. $\overline{CE_1}$ is then taken to 28 to 34 volts, providing base drive through a zener diode to the Darlington current switches and connecting the output pins to their respective sense amplifier busses. At the same time the sense amplifiers are disabled to prevent damage by program current. A diode from $\overline{CE_1}$ to the column select diode gates provides additional base drive current to the column select transistors.

After the preliminaries, the desired bit can be programmed by taking the corresponding output pin O_x to 20 to 26 volts. The programming current flows through the Darlington and column select switch to the fuse and then to ground through the select diode and row select transistor.

Test Circuitry – This device also includes an extra row and an extra column of fuses for test. Extra row and column select switches are provided for their operation. They share the programming and sense circuits with the main fuse matrix and operate as an extension of that matrix but utilize a different method of selection. These fuses are not directly accessible through the package pins.

Extra row select is accomplished by first disabling the main row select switches and then enabling the extra row switch as follows. Taking the A_6 input to a logic high and the A_5 input to 11 volts activates a zener circuit to the A_6 buffer, causing both A_6 buffer outputs to go low. A no select condition results on all the AND gates driving the main row select switches. This condition causes all four output pins to go low so that a V_{OL} measurement can be made. Taking the A_6 input to 11 volts activates another zener circuit to turn on the extra row select switch to enable the extra row to be programmed and read out by the same method used for the main matrix.

The extra column is selected in a similar manner. Taking A_2 to a logic high and A_1 to 11 volts disables the main column select switches while taking $\overline{CE_2}$ to minus 1.0 volt turns on the extra column select switch. A number of fuses are omitted in the deposition of the test row and columns. The resulting pattern permits a check of the functioning of the address circuits and a partial check of access time before programming the test fuses.

Read Circuitry – The chip layout is shown in Figure 7, and the circuit schematic is shown in Figure 8. This device differs from the previous two in that the row select switch connects the selected fuse to V_{cc} rather than ground. This switch is a multiple emitter transistor with the fuses in the row connected to the emitters. The bases of the switches are driven by AND gates controlled by the A_3 through A_7 address buffers.

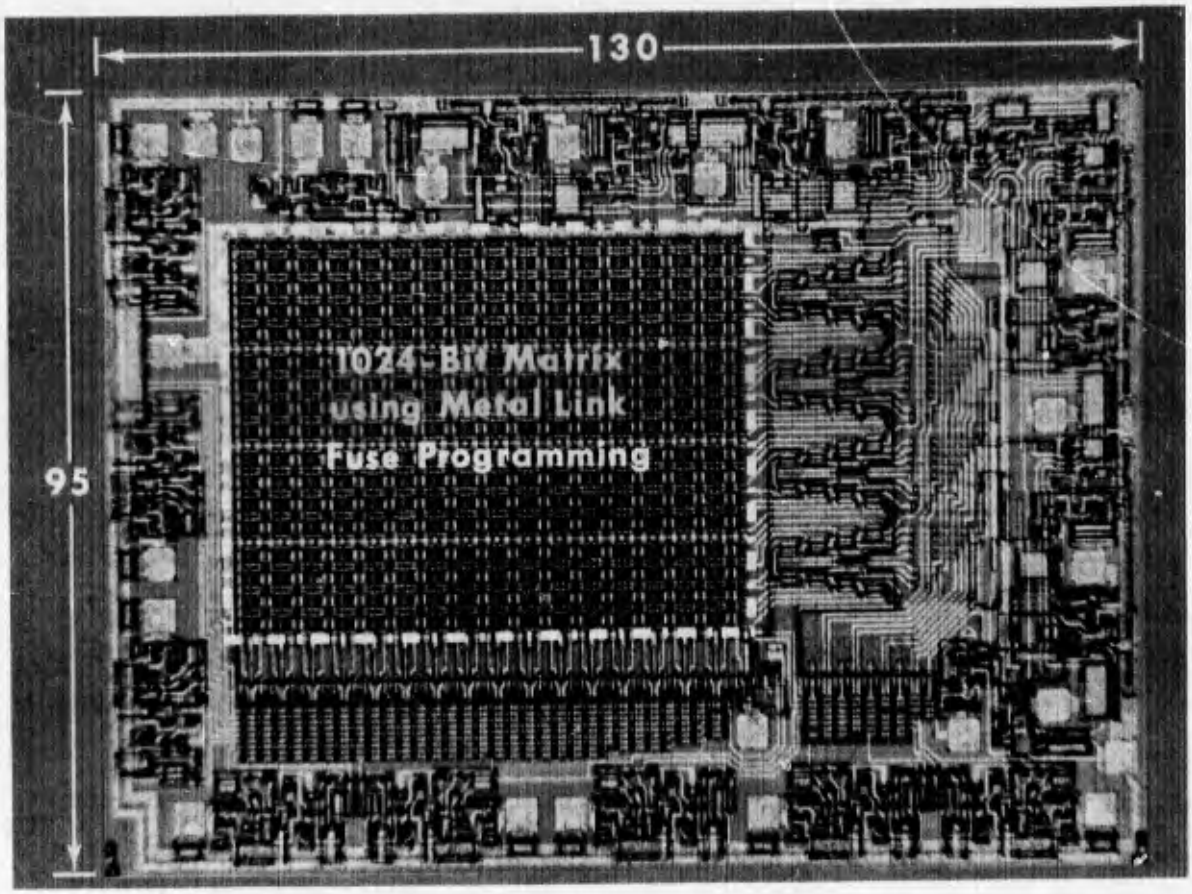


Figure 7. Vendor C 1024-bit PROM chip layout.

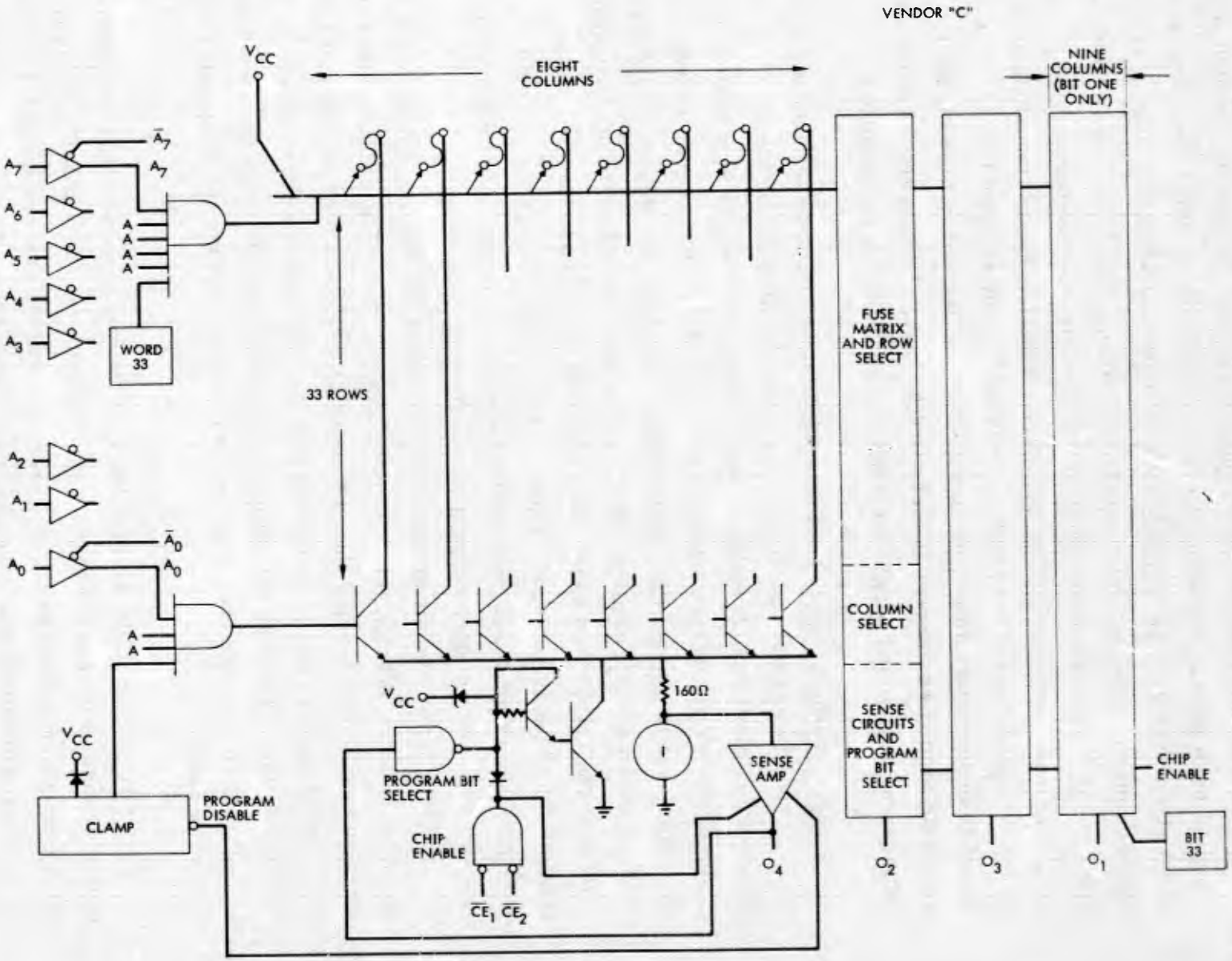


Figure 8. Vendor C 1024-bit PROM skeletal circuit schematic.

Column select is accomplished by a row of transistor switches controlled by AND gates operating on the outputs of address buffers A_0 through A_2. One input of each gate is bussed to a clamp circuit which holds that input at about 1.5 Volts above ground. This has the effect of limiting the column select base drive from the gate to a level below that required to bring the current detector I connected to the sense amplifier input out of saturation. This prevents toggling of the sense amplifier by column select base current alone in the cases where the collector is isolated from V_{cc} by an open fuse. If the fuse is intact (and the sense amplifier is activated by the chip enable circuit), the resulting amplified current is sufficient to bring the current detector I out of voltage saturation and toggle the sense output to the high condition.

Programming Circuitry – The programming current is supplied through the V_{cc} pin via normal select circuits and a Darlington switch which grounds the column select switch emitter buss. As a preliminary step both chip enable inputs must be temporarily taken high to set the outputs in high impedance state and to ground the inputs of the Darlingtons. Next the output pin O_x of the desired bit is grounded, which turns off a disable circuit (Program Bit select) to the Darlington associated with that bit. Next, the V_{cc} pin is clamped to about 10.5 Volts. Thus the necessary voltage drive required for programming is provided, and at the same time the zener is triggered to conduct and provide a supply current to the Darlington circuit.

Another zener circuit disables the clamp on the column select drive and operates another disable on the sense amplifiers. The latter raises both the inputs and outputs of all four sense amplifiers to a high impedance condition preventing the flow of programming current into the sense inputs of the unselected bits. Finally, the chip enable inputs are returned to ground and the last disable is removed from the Darlington allowing the programming current to flow.

Test Circuitry – This device also incorporates an extra row and extra column of fuses for test purposes. In common with the Vendor B design, the test fuses are an extension of the main fuse matrix and are accessible through the main programming and read circuits. Special gates are provided for addressing the extra row and column switches. However, in this case the test

circuits are not available after the chip is packaged. Instead internal pads are provided so that select signals to the test circuits may be introduced by probes. Other probe pads are provided at various critical points in the address and sense circuits for operational tests.

Vendor D

Read Circuitry – The chip layout is shown in Figure 9 and the circuit schematic is shown in Figure 10. The matrix is partitioned into 4-bit blocks of eight columns and 33 rows. The extra row is for testing. The programmable memory element in this device has the form of an NPN transistor with its base floating. The collectors of a row are bussed to a row select switch driven by a decoding AND gate. The input terms to the gates come from the

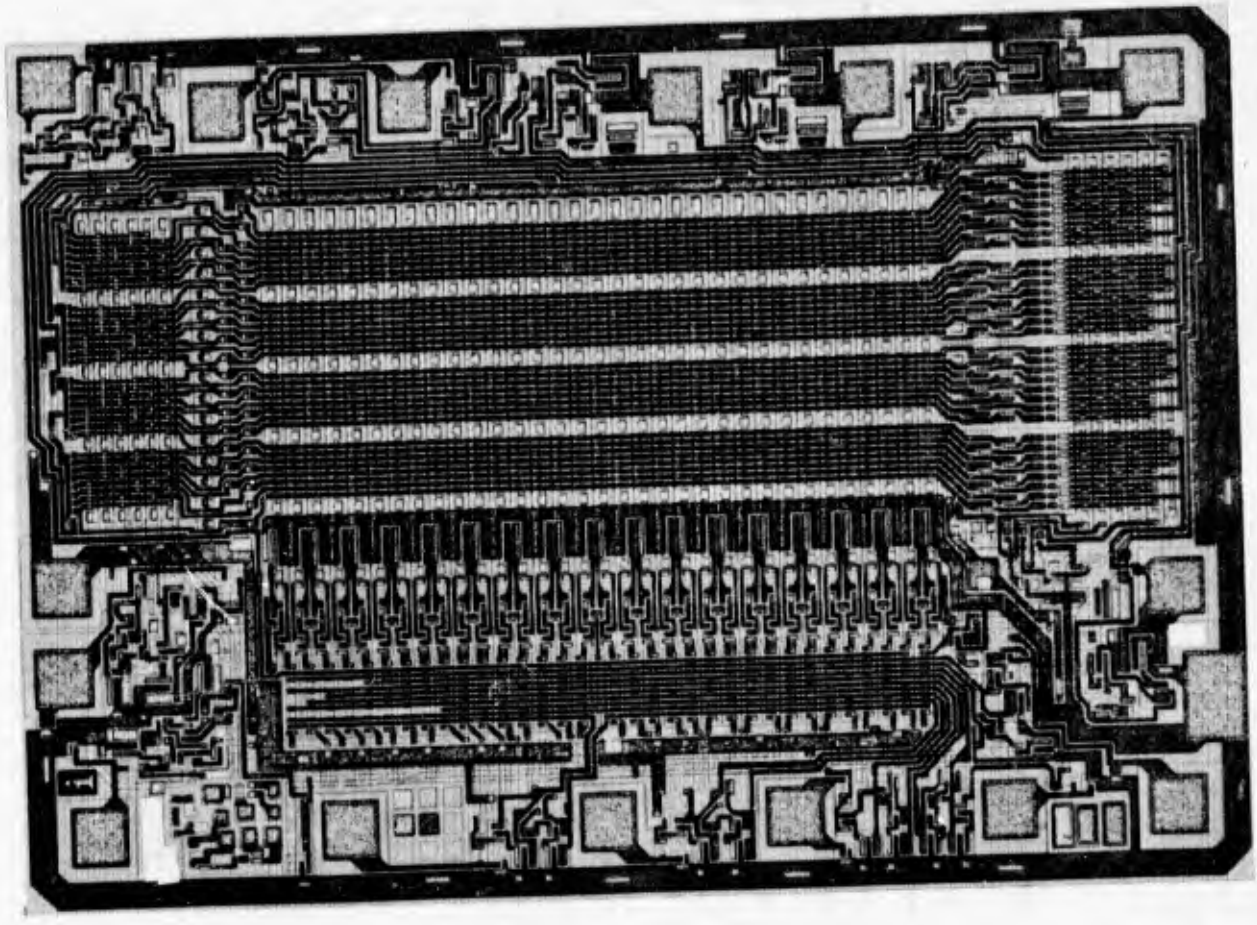


Figure 9. Vendor D 1024-bit PROM chip layout.

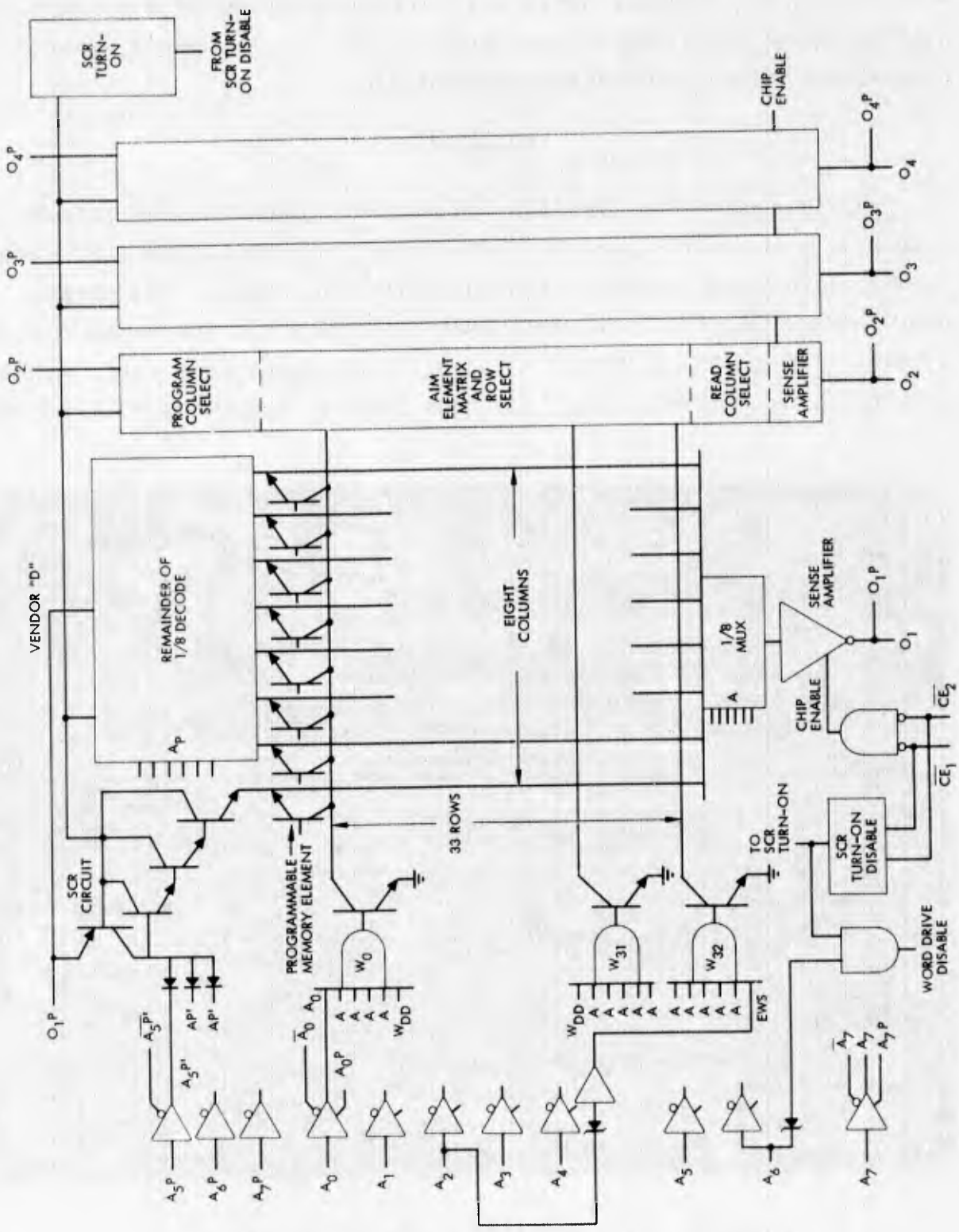


Figure 10. Vendor D 1024-bit PROM skeletal circuit schematic.

address input buffers A_0 through A_4 except for one extra disable (W_{DD}) term required for use in selecting the test row and programming after the devices are installed on boards.

Two column select circuits are provided. The one near the top of Figure 10 is used in programming. The lower one, used in reading, consists of multiplexing gates which connect the selected column to the sense amplifier buss. These gates are controlled by address buffers A_5 through A_7.

If the sense amplifiers are enabled by the chip enable circuit, their outputs will rise or fall depending on whether the base-emitter junction of the selected element has been shorted or not. The collector-base junction of the memory element must remain intact to serve as a matrix select diode.

Programming Circuitry – In programming, the appropriate row is selected by the same circuits used to readout. Column select is accomplished by the upper decode circuit. A diode gate controlled by the A_5 through A_7 buffers, enables the correct Darlington column switch. These switches connect the output pin to the column conductor busses. These circuits operate in a latching mode; once base current is provided to turn on the top most transistor, the resulting Darlington current will keep it turned on, thus acting like an SCR. The initializing current is provided by a zener circuit (SCR turn-on) that conducts when the output pin is raised above normal logic levels. This design prevents operation of the programming circuits during normal read operation and yet permits programming verification at levels of or slightly lower than TTL high. SCR turn-on is also controlled by a disable circuit which is utilized when the devices are installed on boards. On-board programming is discussed further below.

The programming procedure is as follows. First, the sense amplifier output is raised to a high impedance state using the chip enable circuit. Next, the desired address is selected turning on the correct row select switch and enabling of correct programming column switch. A 200 ma programming pulse of 7.5 μs duration is then introduced at the desired output pin O_x. The resulting voltage triggers the SCR turn-on circuits, latching the column switch and allowing avalanche current to flow into the selected base emitter junction to be programmed. At the end of the pulse, the current is reduced to 20 ma, and the resulting output pin voltage is measured. If it is below

7 volts, the junction is considered shorted. If not, the programming and interrogation pulses are repeated in sucession until shorting does occur. At this point, a terminal procedure is performed involving a second successful interrogation after 10 μs and four additional 200 ma x 7.5 μs programming pulses. The apparent purpose of this procedure is to provide additional safety margins for shorting the emitter-base junction, without damaging the collector-base junction.

If it is necessary to program these devices after mounting on a board where output pins are bussed together, a technique is required for selecting only the desired part for programming. One or both of the chip enable pins on the unselected parts are taken to a level of about 6.9 volts. This will operate an SCR turn-on disable circuit to prevent the initial latching of the programming column select gates on the unselected parts. At the same time this circuit also causes the word drive disable circuit to turn off the row select switches on these parts.

Test Circuitry – This device provides only an extra row of fuses for test. It is addressed by taking pins A_2 and A_6 to about 8.3 Volts while taking the remaining address pins to a logic high. A_6 operates a zener circuit to disable all the row select gates except the extra test row. A_2 operates another zener circuit to provide the select term for the extra row gate. Programming tests can be made on the row using the normal procedure. The extra row has a pattern placed in it during processing which can be used to check the operation of the address circuits by exercising the other address terms while holding A_2 at 8.3 Volts. Partial access time measurements can be made in the same way. Use can also be made of the word drive disable and SCR turn-on disable to check internal circuit operation and breakdown voltages.

4.0 PROGRAMMING

General

Since little published data existed regarding the effects of programming on the reliability of fusible links of actual PROM devices, a series of experiments had to be performed that utilized variations in the recommended vendor programming schedules. These experiments consisted of variations in the pulse waveforms such as rise times, widths, amplitudes, etc. After programming, SEM photographs were taken of the chemically etched fusible links both before and after a plasma etch process. A description of the sample preparation and SEM analysis techniques is given in the Appendix. Each programming experiment was correlated to the physical appearance of the fuse link after programming. The experiments were conducted only on devices from vendors A and B. Program voltage variations on the Vendor C parts were not possible because the programming circuit operates at a raised V_{CC} level, and any reduction in voltage levels result in random programming. However, the Vendor C devices were monitored during programming and the times-to-blow recorded (Table 1) to allow a correlation of programming time to fuse appearance. Figures 11 and 12 are SEM photos of Vendor C fuses after chemical etch, while Figure 13 shows the same fuses after plasma etching. Additionally, programming experiments were stopped on the Vendor D devices after difficulty in correlating programming pulse waveform variations to visual structure changes in specific emitter-base junction regions. To date none of the users contacted or the vendor were able to supply any optical or SEM pictures of sectional views of the shorted junction that delineate the shorting structure, aluminum pipe or otherwise. A new technique for junction analysis must be developed before such a structure can be studied.

A Spectrum Dynamics Model 550 Memory Programmer modified to permit pulse variations was used for the programming. A Tektronix Model 7623 Storage Oscilloscope and a Tektronix Model P6042 DC Current Probe were used to monitor the programming voltage and current waveforms to observe anomalies during programming which might give a clue to possible failure

TABLE 1. PROGRAMMING SCHEDULE – VENDOR C Ti-W FUSES (SAMPLE 1)

Figure Number Before* Plasma Etch	Figure Number After* Plasma Etch	Fuse	Pulse Amplitude, volts	Length, ms	Rise Time, μs	Time-to-Program, μs	Comment
11	None	T	-	-	-	-	Unprogrammed Fuse
12a	13a	B2190	10.5	10	0.5	<10	Short Program Time
12a	13a	B3190	10.5	10	0.5	130	Medium Program Time
12b	13b	B2188	10.5	10	0.5	<10	Short Program Time
12b	13b	B3188	10.5	10	0.5	100	Medium Program Time
12c	13c	B2249	10.5	10	0.5	<10	Short Program Time
12c	13c	B3249	10.5	10	0.5	530	Long Program Time
12d	13d	B260	10.5	10	0.5	<10	Short Program Time
12d	13d	B360	10.5	10	0.5	350	Long Program Time

*All of the fuses were first chemically etched

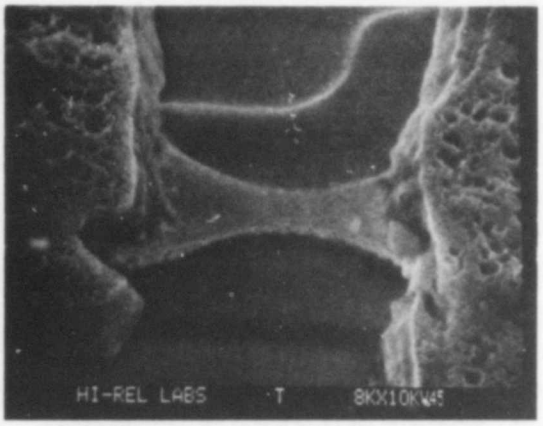
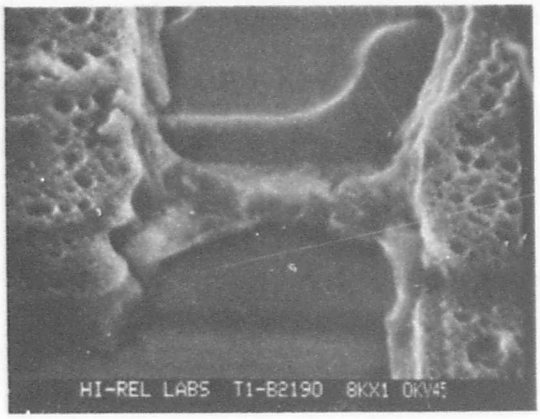


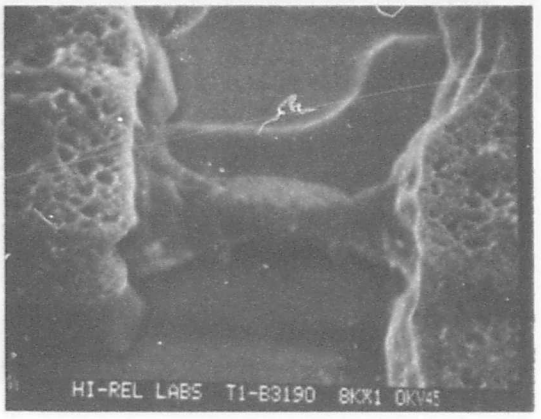
Figure 11. SEM photo of Vendor C fuse after chemical etch – unprogrammed fuse.

modes. All SEM analyzed fuses from programming experiments listed in Tables 2 through 4 for Vendors A and B are shown in Figures 14a-f, 16a-n, and 18a-n, respectively, for fuses that were chemically etched and Figures 15a-k, 17a-f, and 19a-n for selected fuses after plasma etching.

The fuses in the main storage array (1024 fuses) were used for the various experiments rather than the test fuses (less than 100 fuses) to obtain a larger fuse sample size. Since electric current reaching any of these fuses is difficult to measure accurately, the time required for fusing was used as a measure of the energy deposition rate. To simulate "fast and slow blow" fusing conditions, the pulse amplitude was either increased or decreased. The relationship between blow time and pulse amplitude is illustrated in Figure 20. The pulse amplitude is bounded between the minimum power required to program the memory element and the circuitry limitations such as junction breakdowns or current saturation levels. Other considerations are circuit stresses and chip heating. In most cases where the voltages were near the recommended programming voltage, the fuse opened when the voltage had been raised to near the maximum value and the fusing time was thus controlled by the rise time. For fast rise times, e.g., less than 1 μs, the fuse opening was delayed for several microseconds because of the thermal time constant of the fuse link. When the voltage was reduced, the fusing could occur at times extended to several seconds. Variations in the programming pulses revealed a direct correlation to the physical appearance of

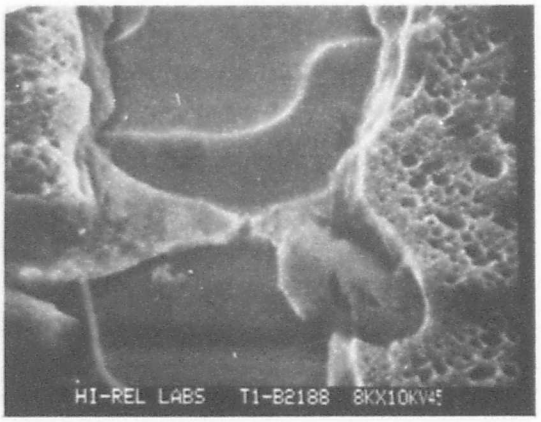


PULSE AMPLITUDE	10.5 VOLTS
LENGTH	10 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	$<$10 μs

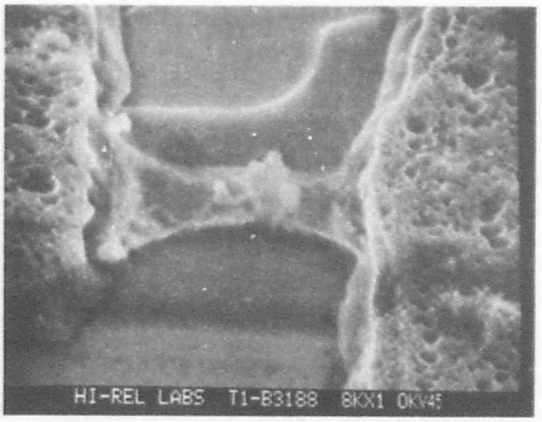


PULSE AMPLITUDE	10.5 VOLTS
LENGTH	10 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	130 μs

a.



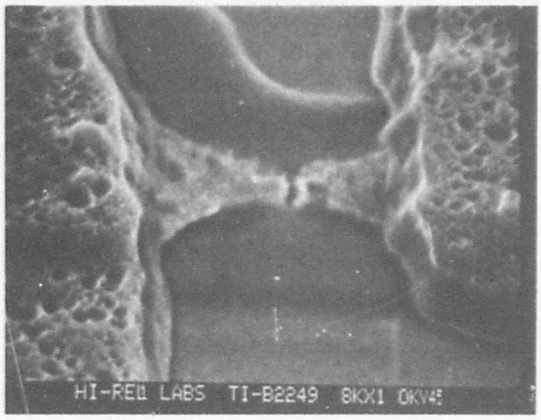
PULSE AMPLITUDE	10.5 VOLTS
LENGTH	10 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	$<$10 μs



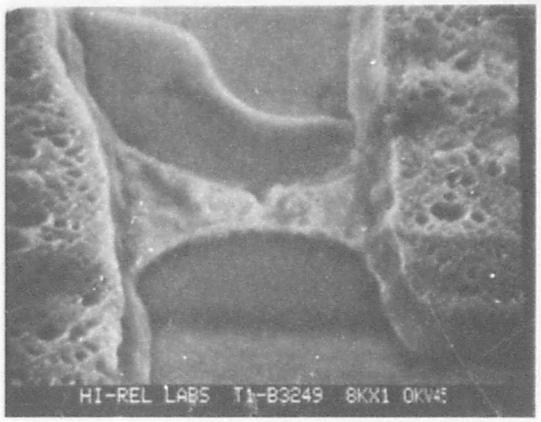
PULSE AMPLITUDE	10.5 VOLTS
LENGTH	10 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	100 μs

b.

Figure 12. SEM photos of Vendor C fuse before plasma etch (sheet 1).

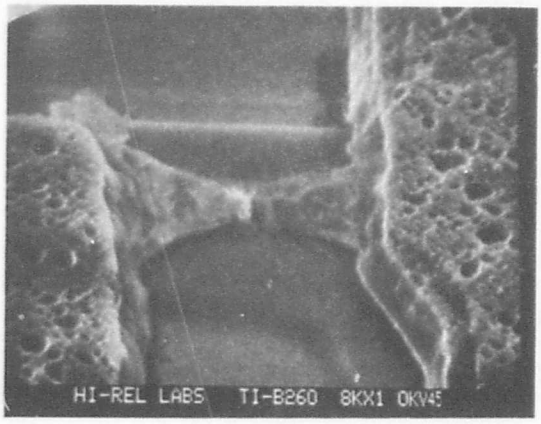


PULSE AMPLITUDE	10.5 VOLTS
LENGTH	10 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	<10 μs

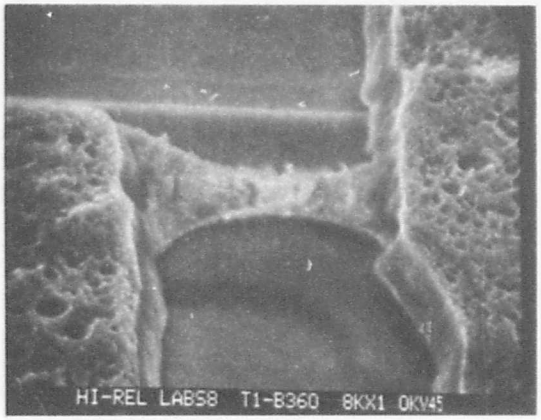


PULSE AMPLITUDE	10.5 VOLTS
LENGTH	10 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	530 μs

c.



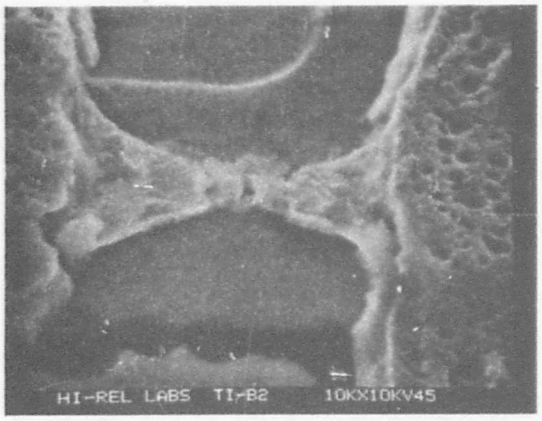
PULSE AMPLITUDE	10.5 VOLTS
LENGTH	10 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	<10 μs



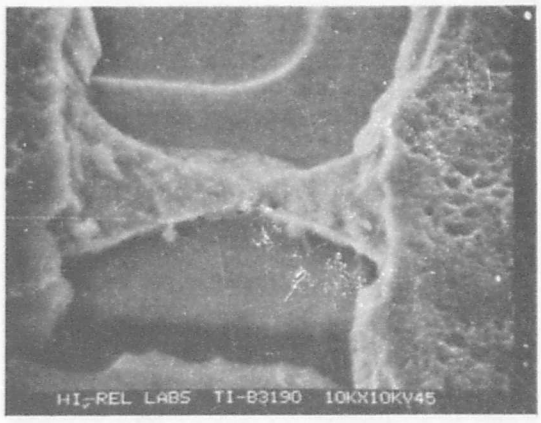
PULSE AMPLITUDE	10.5 VOLTS
LENGTH	10 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	350 μs

d.

Figure 12. SEM photos of Vendor C fuse before plasma etch (sheet 2).

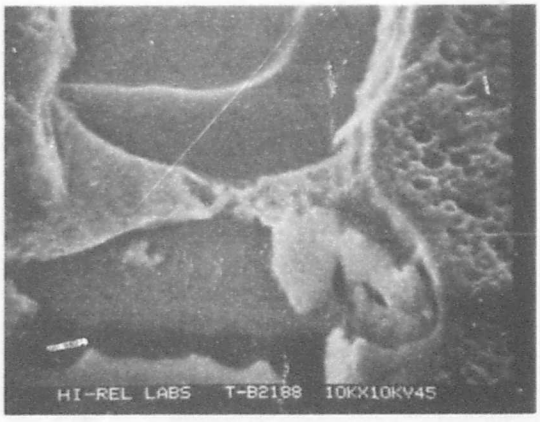


PULSE AMPLITUDE	10.5 VOLTS
LENGTH	10 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	<10 μs

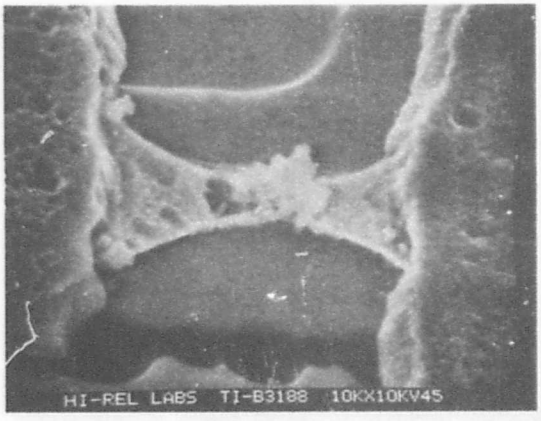


PULSE AMPLITUDE	
LENGTH	
RISE TIME	
TIME-TO-PROGRAM	

a.



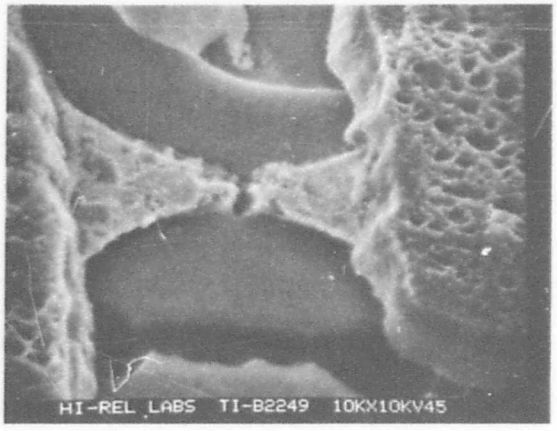
PULSE AMPLITUDE	10.5 VOLTS
LENGTH	10 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	<10 μs



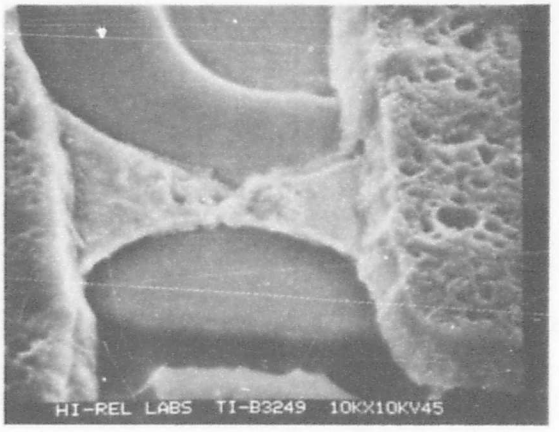
PULSE AMPLITUDE	
LENGTH	
RISE TIME	
TIME-TO-PROGRAM	

b.

Figure 13. SEM photos of Vendor C Ti:W fuse aft plasma etch (sample 1) (sheet 1).

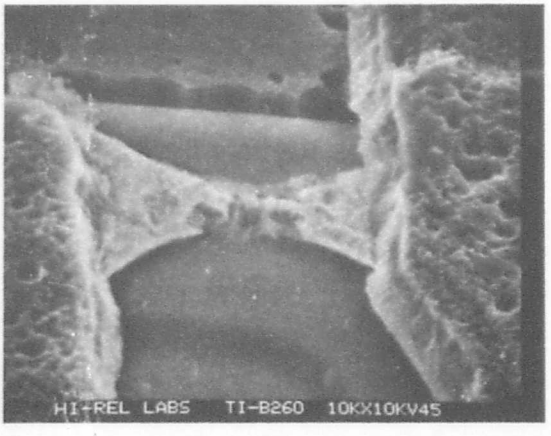


PULSE AMPLITUDE	10.5 VOLTS
LENGTH	10 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	<10 μs

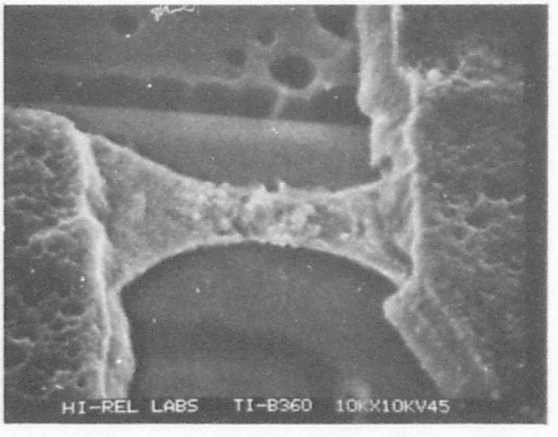


PULSE AMPLITUDE	10.5 VOLTS
LENGTH	10 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	530 μs

c.



PULSE AMPLITUDE	10.5 VOLTS
LENGTH	10 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	<10 μs



PULSE AMPLITUDE	10.5 VOLTS
LENGTH	10 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	350 μs

d.

Figure 13. SEM photos of Vendor C Ti:W fuse after plasma etch (sample 1) (sheet 2).

TABLE 2. PROGRAMMING EXPERIMENTS – VENDOR A NICHROME FUSES (SAMPLE 24, DEVICE SUBJECTED TO 168 HOURS DYNAMIC BURN-IN TESTING BEFORE SEM ANALYSIS)

Programming Experiment	Figure Number Before* Plasma Etch	Figure Number After* Plasma Etch	Fuse	Pulse Amplitude, volts	Length, ms	Rise Time, μs	Time-to-Program	Number of Pulses	Comment
Short Rise Time	14a	15a	B3244	25	12	0.5	3 μs	1	Voltage continued after programming
Short Rise Time	14a	15a	B325	25	12	0.5	3 μs	1	Voltage continued after programming
Program on Rise Time	14b	15b	B3248	25	12	130	128 μs	1	Voltage continued after programming
Program on Rise Time	14b	15b	B3240	25	12	130	128 μs	1	Voltage continued after programming
Program on Rise Time	14c	15c	B4241	25	192	130	128 μs	1	Long after pulse
Program on Rise Time	14c	15c	B4249	25	192	130	125 μs	1	Long after pulse
Program on Pulse Level	14d	15d	B4115	23	192	128	1.67 ms	1	Long after pulse
Program on Pulse Level	14d	15d	B4243	23	192	128	1.25 ms	1	Long after pulse
Program on Pulse Level	14e	15e	B4215	22	192	126	10.3 ms	1	Long after pulse
Program on Pulse Level	14e	15e	B4207	22	192	126	8.8 ms	1	Long after pulse
Short After Pulse	14f	15f	B4200	21	1.9	125	1.2 ms	1	Voltage stopped after programming
Short After Pulse	14f	15f, 15g	B4208	21	1.9	125	0.9 ms	1	Voltage stopped after programming
Program on Pulse Level	14g	15h	B486	21	12	125	7.5 ms	1	Voltage stopped shortly after programming

*All of the fuses were first chemically etched.

(Continued next page)

(Table 2, concluded)

Programming Experiment	Figure Number: Before* Plasma Etch	Figure Number: After* Plasma Etch	Fuse	Pulse Amplitude, volts	Length, ms	Rise Time, μs	Time-to-Program	Number of Pulses	Comment
Program on Pulse Level	14g	15h	B470	21	12	125	10.5 ms	1	Voltage stopped shortly after programming
Long Time to Program	14h	15i	B4221	20	192	123	135 ms	1	Extended programming time
Long Time to Program	14h	15i	B4253	20	192	125	100 ms	1	Extended programming time
Multiple Pulses	14i	15j	B492	20	12	125	180 ms	15	Long program time
Multiple Pulses	14i	15j	B484	20	12	125	204 ms	17	Long program time
Partial Programming	14j	15k	B4122	20.5	12	125	-	1	Pulse terminated prior to programming
Partial Programming	14j	15k	B4114	20.5	12	125	-	1	Pulse terminated prior to programming

*All of the fuses were first chemically etched.

TABLE 3. PROGRAMMING EXPERIMENTS – VENDOR A NICHROME FUSES (SAMPLE 25, DEVICE NOT SUBJECTED TO DYNAMIC BURN-IN)

Programming Experiment	Figure Number Before* Plasma Etch	Figure Number After* Plasma Etch	Fuse	Pulse Amplitude, volts	Length, ms	Rise Time, μs	Time-to-Program	Number of Pulses	Comment
Short Rise Time	16a	None	B3244	25.0	12	0.5	5 μs	1	Voltage continued after programming
Short Rise Time	16a	17a	B3252	25.0	12	0.5	5 μs	1	Voltage continued after programming
Program on Rise Time	16b	None	B3248	25.0	12	130	125 μs	1	Voltage continued after programming
Program on Rise Time	16b	None	B3240	25.0	12	130	125 μs	1	Voltage continued after programming
Program on Rise Time	16c	17b	B4249	25.0	129	130	130 μs	1	Long after pulse
Program on Rise Time	16c	None	B4241	25.0	192	130	125 μs	1	Long after pulse
Program on Pulse Level	16d	None	B4179	22.5	192	125	0.92 ms	1	Long after pulse
Program on Pulse Level	16d	None	B4187	22.5	192	125	1 ms	1	Long after pulse
Pulse Stopped After Programming	16e	None	B4192	21.5	1.9	122	1.9 ms	1	Time to program equals pulse length
Program on Pulse Level	16f	None	B4127	21.5	192	130	8.1 ms	1	Long after pulse
Program on Pulse Level	16f	None	B4103	21.5	192	130	11.2 ms	1	Long after pulse
Program on Pulse Level	16g	None	B495	21.5	192	122	11.2 ms	1	Long after pulse
Program on Pulse Level	16h	17b	B486	21.0	12	120	8.6 ms	1	Voltage stopped shortly after programming

*All of the fuses were first chemically etched.

(Continued next page)

(Table 3, concluded)

Programming Experiment	Figure Number Before* Plasma Etch	Figure Number After* Plasma Etch	Fuse	Pulse Amplitude, volts	Length, ms	Rise Time, μs	Time-to-Program	Number of Pulses	Comment
Long Time to Program	16i	None	B4237	20.5	192	122	100 ms	1	Extended programming time
Long Time to Program	16j	None	B4245	20.5	192	122	100 ms	1	Extended programming time
Long Time to Program	16j	None	B4229	20.5	192	122	144 ms	1	Extended programming time
Multiple Pulses	16k	None	B4228	20.5	12	122	108 ms	9	Long programming time
Partial Programming	16l	17c	B4186	20.8	12	120	-	Partial	Pulse terminated prior to partial programming
Partial Programming	16m	None	B4178	20.8	12	120	-	Partial	Pulse terminated prior to partial programming
Partial Programming	16m	17d	B4194	20.8	12	120	-	Partial	Pulse terminated prior to partial programming
Test Fuse Comparison	16n	17e	BT1	-	-	-	-	-	Programmed by vendor
Test Fuse Comparison	16n	17e, 17f	BT2	-	-	-	-	-	Programmed by vendor

*All of the fuses were first chemically etched.

TABLE 4. PROGRAMMING EXPERIMENTS – VENDOR B NICHROME FUSES (SAMPLE 11, DEVICE SUBJECTED TO 168 HOURS DYNAMIC BURN-IN TESTING BEFORE SEM ANALYSIS)

Programming Experiment	Figure Number		Fuse	Pulse Amplitude, volts	Length, ms	Rise Time, μs	Time-to-Program	Number of Pulses	Comment
	Before* Plasma Etch	After* Plasma Etch							
Short Rise Time	18a	19a	B133	26	10	2.5	3 μs	1	Voltage continued after programming
Short Rise Time	18a	19a	B149	26	10	2.5	3 μs	1	Voltage continued after programming
Program on Rise Time	18b	19b	B132	26	10	60	55 μs	1	Voltage continued after programming
Program on Rise Time	18b	19b	B148	26	10	60	55 μs	1	Voltage continued after programming
Program on Rise Time	18c	19c	B48	21	200	28	28 μs	1	Long after pulse
Program on Rise Time	18c	19c	B418	21	200	28	28 μs	1	Long after pulse
Program on Pulse Level	18d	19d	B429	21	200	28	30 μs	1	Long after pulse
Short Programming Pulse	18e	19e	B431	21	40	28	30 μs	1	Voltage stopped after programming
Short Programming Pulse	18e	19e	B421	21	40	28	35 μs	1	Voltage stopped after programming
Program on Pulse Level	18f	19f	B4112	12.5	200	15	360 μs	1	Short rise time – long after pulse
Program on Pulse Level	18f	19f	B4122	12.5	200	15	800 μs	1	Short rise time – long after pulse
Program on Pulse Level	18g	19g	B440	12.5	2	15	810 μs	1	Short rise time – medium after pulse
Program on Pulse Level	18g	19g	B4125	12.5	2	15	800 μs	1	Short rise time – medium after pulse

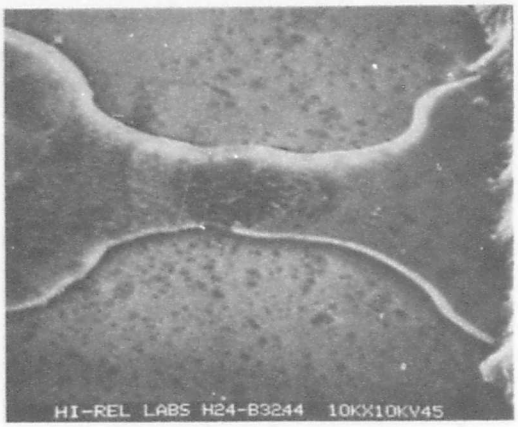
*All of the fuses were first chemically etched.

(Continued next page)

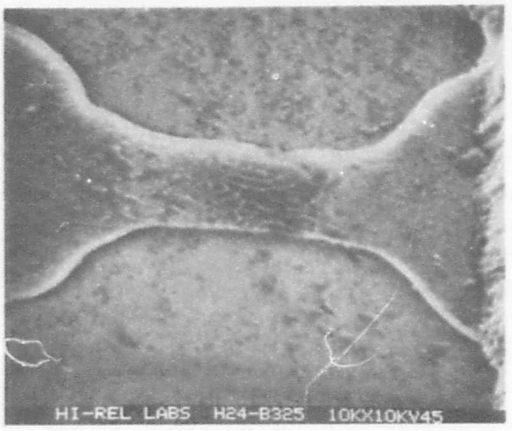
(Table 4, concluded)

Programming Experiment	Figure Number: Before* Plasma Etch	Figure Number: After* Plasma Etch	Fuse	Pulse Amplitude, volts	Length, ms	Rise Time, μs	Time-to-Program	Number of Pulses	Comment
Long Time to Program	18h	19h	B2185	12.3	200	14	144 ms	1	Short rise time – long after pulse
Long Time to Program	18h	19h	B2187	12.3	200	14	130 ms	1	Short rise time – long after pulse
Long Time to Program	18i	19i	B265	12.3	200	14	180 ms	1	Short rise time – long after pulse
Program on Pulse Level	18j	19j	B420	12	10	15	2.9 ms	1	Short rise time – long after pulse
Program on Pulse Level	18j	19j	B484	12	10	15	3.2 ms	1	Short rise time – long after pulse
Program on Pulse Level	18k	19k	B438	12	200	15	3.5 ms	1	Short rise time – long after pulse
Program on Pulse Level	18k	19k	B4102	12	200	15	3.4 ms	1	Short rise time – long after pulse
Program on Pulse Level	18l	19l	B4106	11.2	200	14	21 ms	1	Short rise time – long after pulse
Program on Pulse Level	18l	19l	B442	11.2	200	14	25 ms	1	Short rise time – long after pulse
Multiple Pulses	18m	19m	B2190	12	200	15	800 ms	4	Long time to program
Multiple Pulses	18m	19m	B2188	11	200	15	1300 ms	7	Long time to program
Multiple Pulses	18n	19n	B4124	10.8	10	13	170 ms	17	Long time to program
Multiple Pulses	18n	19n	B460	10.8	10	13	100 ms	10	Long time to program

*All of the fuses were first chemically etched.

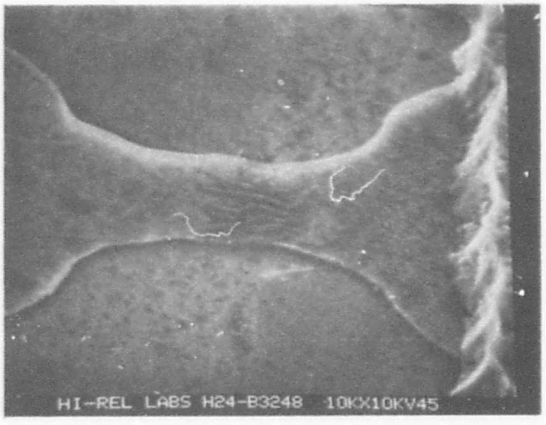


PULSE AMPLITUDE	25 VOLTS
LENGTH	12 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	3 μs

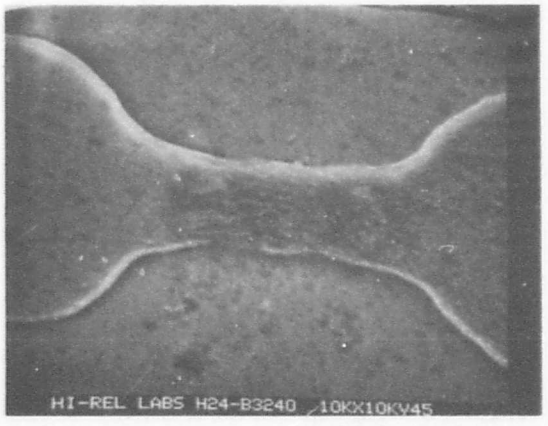


PULSE AMPLITUDE	25 VOLTS
LENGTH	12 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	3 μs

a.



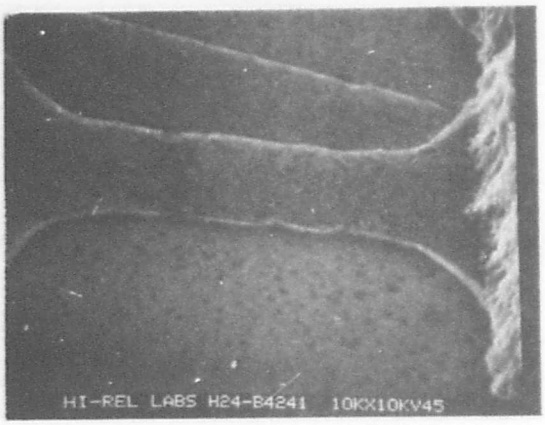
PULSE AMPLITUDE	25.0 VOLTS
LENGTH	12 ms
RISE TIME	130 μs
TIME-TO-PROGRAM	128 μs



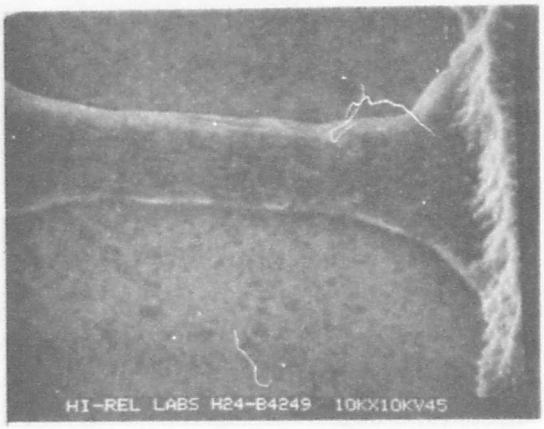
PULSE AMPLITUDE	25.0 VOLTS
LENGTH	12 ms
RISE TIME	130 μs
TIME-TO-PROGRAM	128 μs

b.

Figure 14. SEM photos of Vendor A fuse before plasma etch (sheet 1).

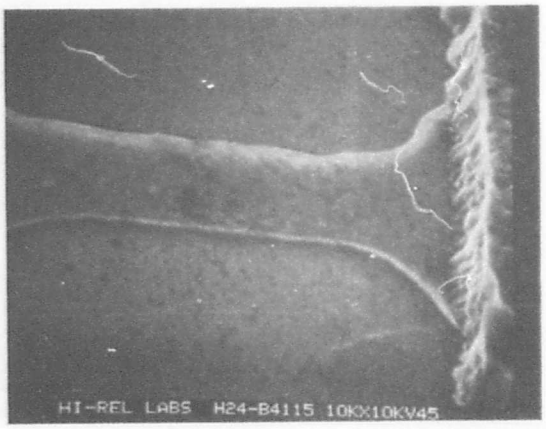


PULSE AMPLITUDE	25.0 VOLTS
LENGTH	192 ms
RISE TIME	130 μs
TIME-TO-PROGRAM	128 μs

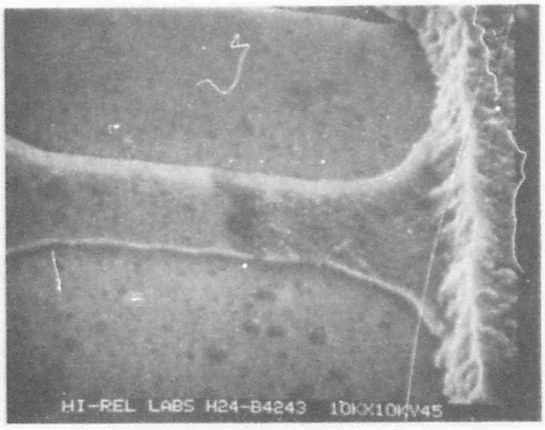


PULSE AMPLITUDE	25.0 VOLTS
LENGTH	192 ms
RISE TIME	130 μs
TIME-TO-PROGRAM	125 μs

c.



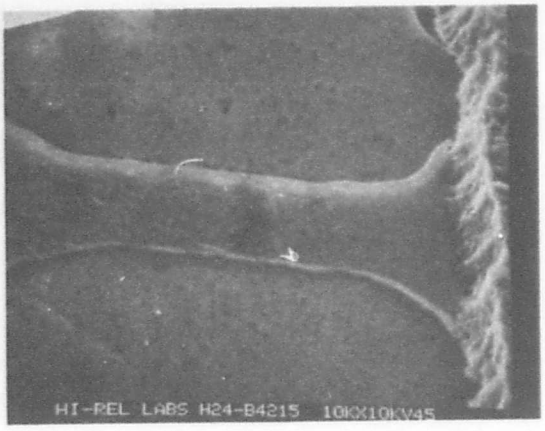
PULSE AMPLITUDE	23.0 VOLTS
LENGTH	192 ms
RISE TIME	128 μs
TIME-TO-PROGRAM	1.67 ms



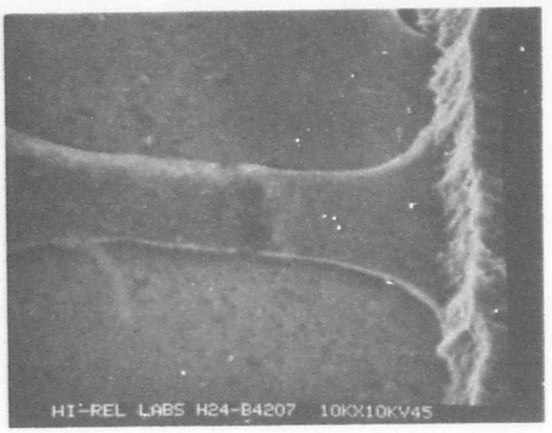
PULSE AMPLITUDE	23.0 VOLTS
LENGTH	192 ms
RISE TIME	128 μs
TIME-TO-PROGRAM	1.25 ms

d.

Figure 14. SEM photos of Vendor A fuse before plasma etch (sheet 2).

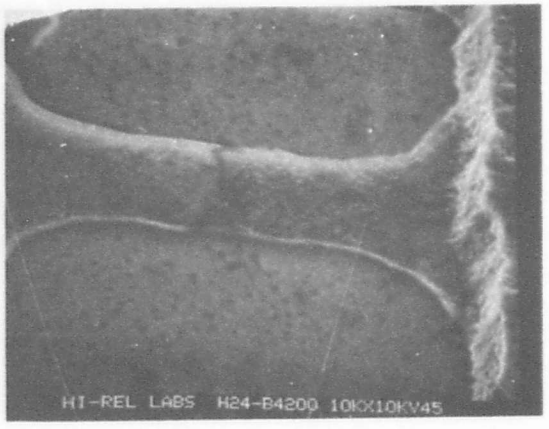


PULSE AMPLITUDE	22.0 VOLTS
LENGTH	192 ms
RISE TIME	126 μs
TIME-TO-PROGRAM	10.3 ms

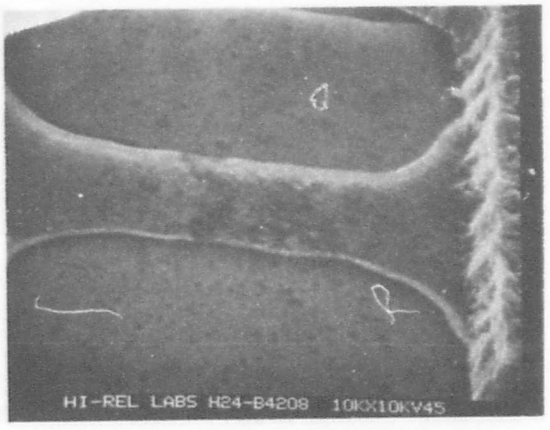


PULSE AMPLITUDE	22.0 VOLTS
LENGTH	192 ms
RISE TIME	126 μs
TIME-TO-PROGRAM	8.8 ms

e.



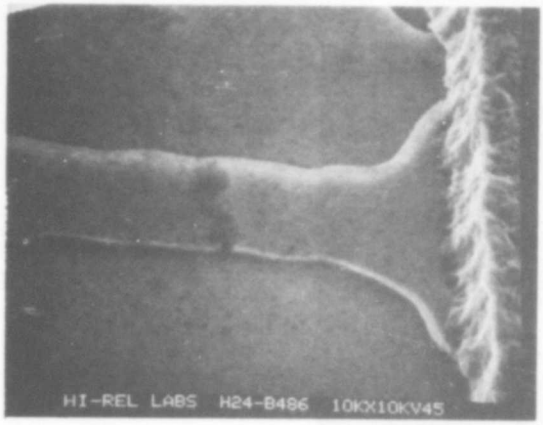
PULSE AMPLITUDE	21.0 VOLTS
LENGTH	1.9 ms
RISE TIME	125 μs
TIME-TO-PROGRAM	1.2 ms



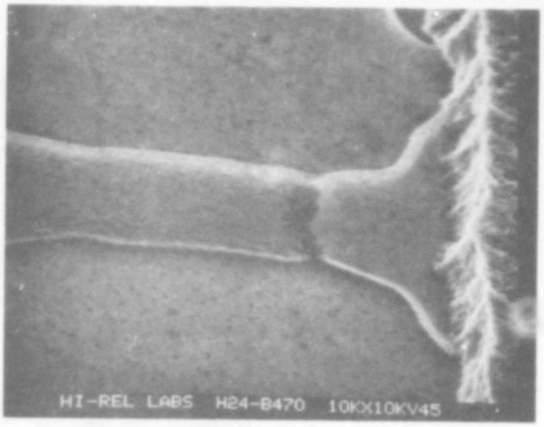
PULSE AMPLITUDE	21.0 VOLTS
LENGTH	1.9 ms
RISE TIME	125 μs
TIME-TO-PROGRAM	0.9 ms

f.

Figure 14. SEM photos of Vendor A fuse before plasma etch (sheet 3).

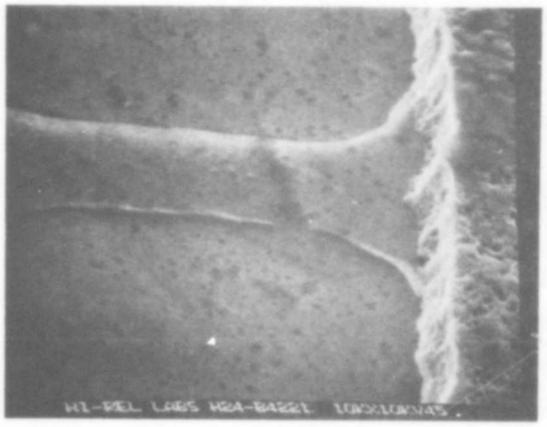


PULSE AMPLITUDE	21.0 VOLTS
LENGTH	12 ms
RISE TIME	125 μs
TIME-TO-PROGRAM	7.5 ms

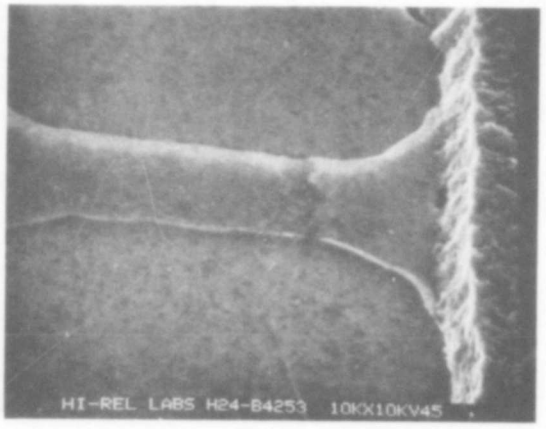


PULSE AMPLITUDE	21.0 VOLTS
LENGTH	12 ms
RISE TIME	125 μs
TIME-TO-PROGRAM	10.5 ms

g.



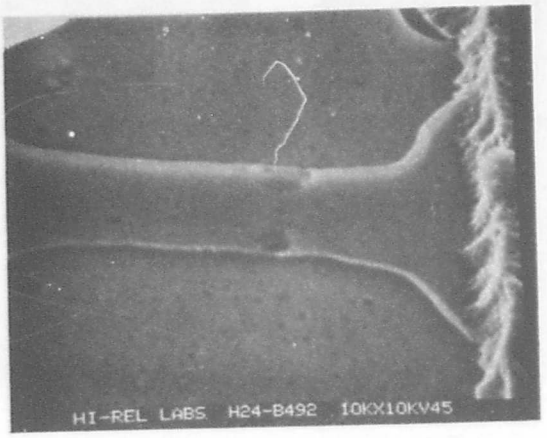
PULSE AMPLITUDE	20 VOLTS
LENGTH	192 ms
RISE TIME	123 μs
TIME-TO-PROGRAM	135 ms



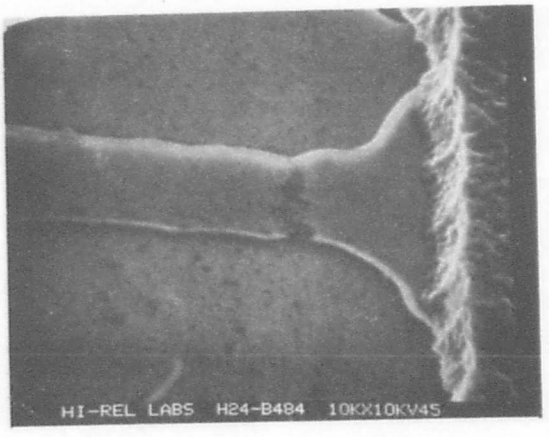
PULSE AMPLITUDE	20 VOLTS
LENGTH	192 ms
RISE TIME	125 μs
TIME-TO-PROGRAM	100 ms

h.

Figure 14. SEM photos of Vendor A fuse before plasma etch (sheet 4).



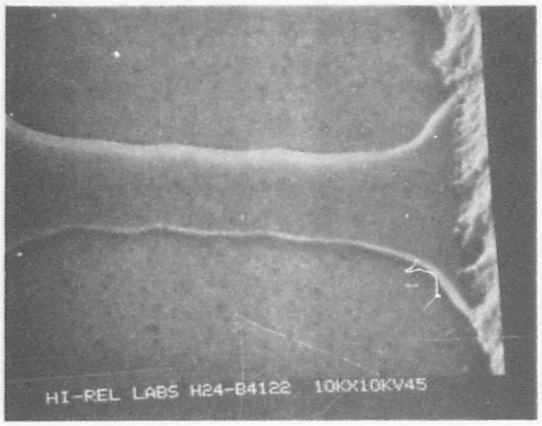
PULSE AMPLITUDE	20.0 VOLTS
LENGTH	12 ms
RISE TIME	125 μs
NUMBER OF PULSES TO PROGRAM	15 PULSES
TOTAL PROGRAMMING TIME	180 ms



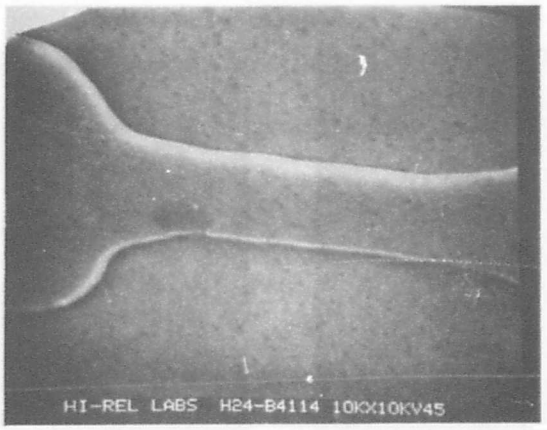
PULSE AMPLITUDE	20.0 VOLTS
LENGTH	12 ms
RISE TIME	125 μs
NUMBER OF PULSES TO PROGRAM	17 PULSES
TOTAL PROGRAMMING TIME	204 ms

i.

Figure 14. SEM photos of Vendor A fuse before plasma etch (sheet 5).



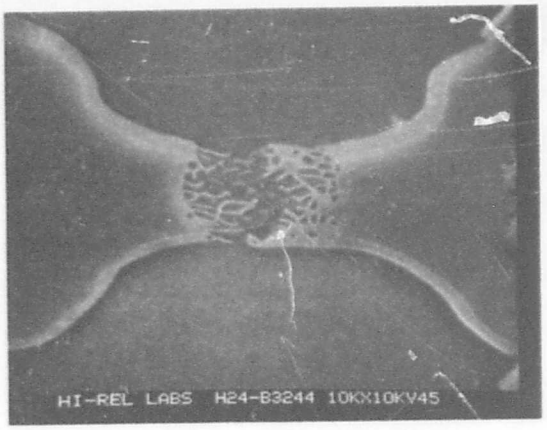
PULSE AMPLITUDE 20.5 VOLTS
LENGTH 12 ms
RISE TIME 125 μs
EXPERIENCED PARTIAL PROGRAMMING PULSE



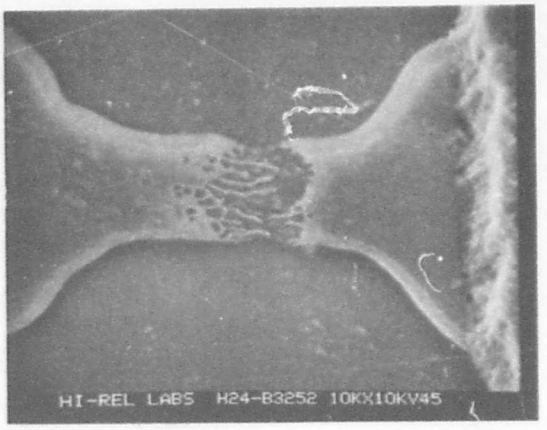
PULSE AMPLITUDE 20.5 VOLTS
LENGTH 12 ms
RISE TIME 125 μs
EXPERIENCED PARTIAL PROGRAMMING PULSE

j.

Figure 14. SEM photos of Vendor A fuse before plasma etch (sheet 6).

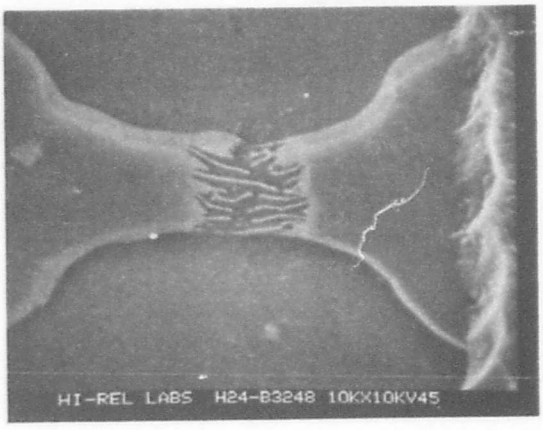


PULSE AMPLITUDE	25 VOLTS
LENGTH	12 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	3 μs

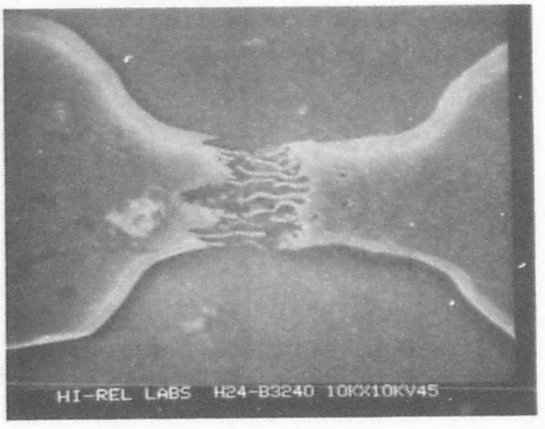


PULSE AMPLITUDE	25 VOLTS
LENGTH	12 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	3 μs

a.



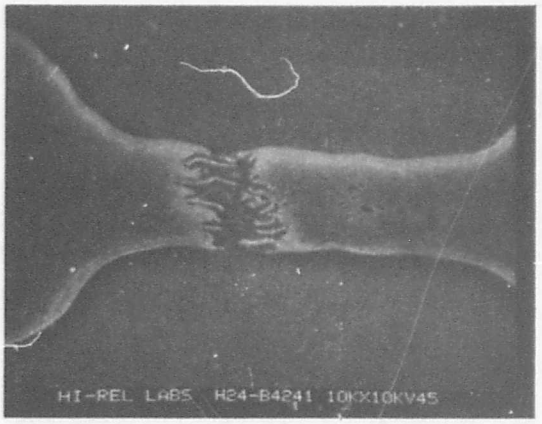
PULSE AMPLITUDE	25 VOLTS
LENGTH	12 ms
RISE TIME	130 μs
TIME-TO-PROGRAM	128 μs



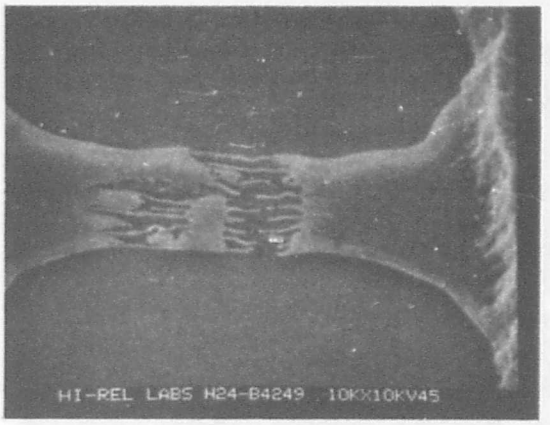
PULSE AMPLITUDE	25 VOLTS
LENGTH	12 ms
RISE TIME	130 μs
TIME-TO-PROGRAM	128 μs

b.

Figure 15. SEM photos of Vendor A nichrome fuse after plasma etch (sample 24) (sheet 1).

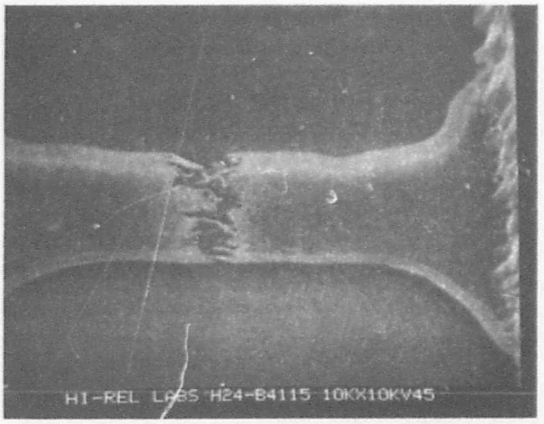


PULSE AMPLITUDE	25 VOLTS
LENGTH	192 ms
RISE TIME	130 μs
TIME-TO-PROGRAM	128 μs

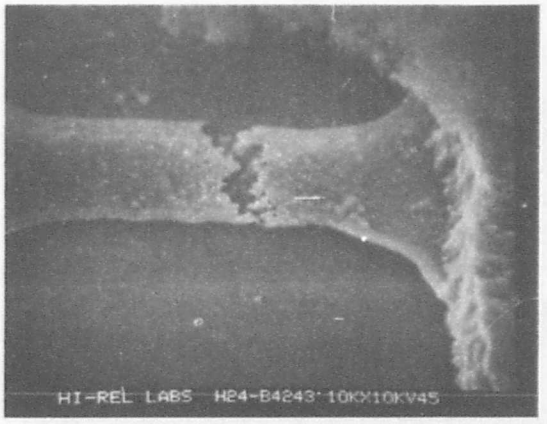


PULSE AMPLITUDE	25 VOLTS
LENGTH	125 ms
RISE TIME	130 μs
TIME-TO-PROGRAM	125 μs

c.



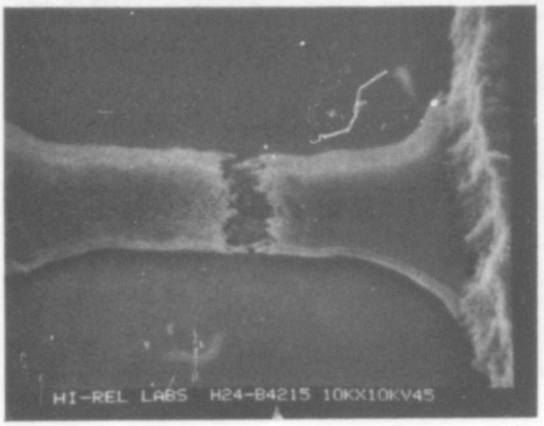
PULSE AMPLITUDE	23 VOLTS
LENGTH	192 ms
RISE TIME	128 μs
TIME-TO-PROGRAM	1.67 ms



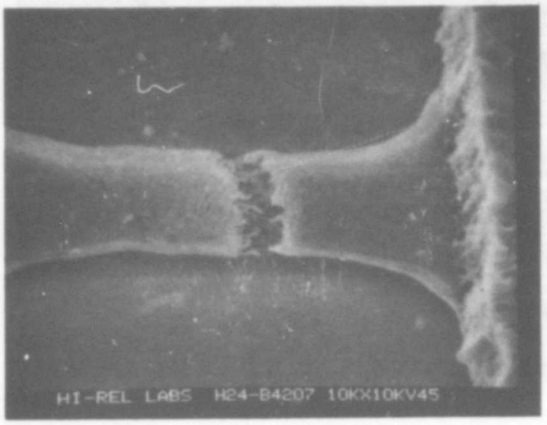
PULSE AMPLITUDE	23 VOLTS
LENGTH	192 ms
RISE TIME	128 μs
TIME-TO-PROGRAM	1.25 ms

d.

Figure 15. SEM photos of Vendor A nichrome fuse after plasma etch (sample 24) (sheet 2).

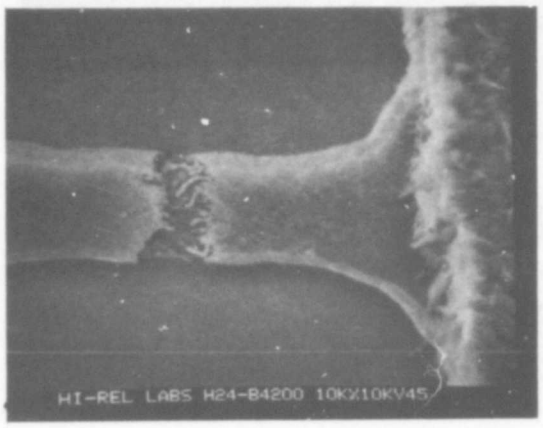


PULSE AMPLITUDE	22 VOLTS
LENGTH	192 ms
RISE TIME	126 μs
TIME-TO-PROGRAM	10.3 ms

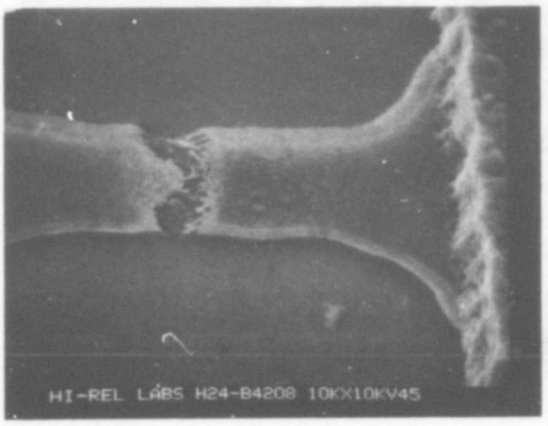


PULSE AMPLITUDE	22 VOLTS
LENGTH	192 ms
RISE TIME	126 μs
TIME-TO-PROGRAM	8.8 ms

e.



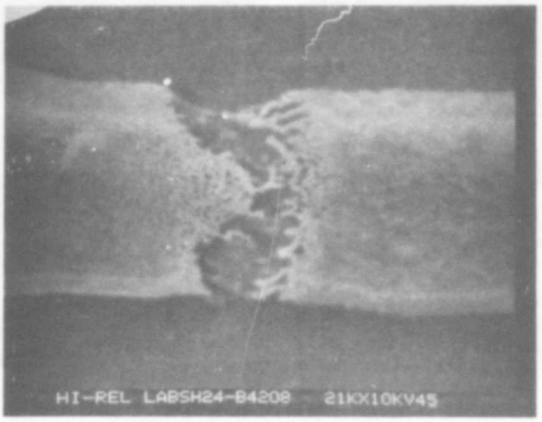
PULSE AMPLITUDE	21 VOLTS
LENGTH	1.9 ms
RISE TIME	125 μs
TIME-TO-PROGRAM	1.2 ms



PULSE AMPLITUDE	21 VOLTS
LENGTH	1.9 ms
RISE TIME	125 μs
TIME-TO-PROGRAM	0.9 ms

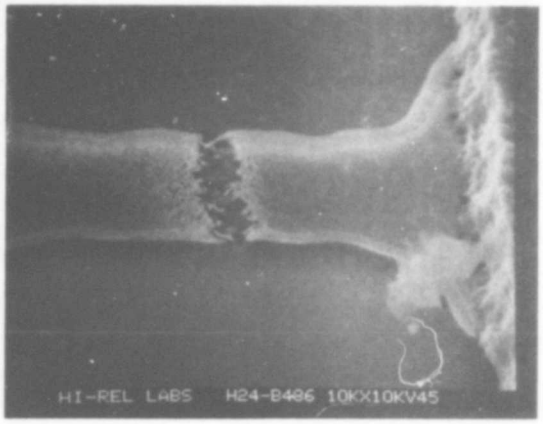
f.

Figure 15. SEM photos of Vendor A nichrome fuse after plasma etch (sample 24) (sheet 3).

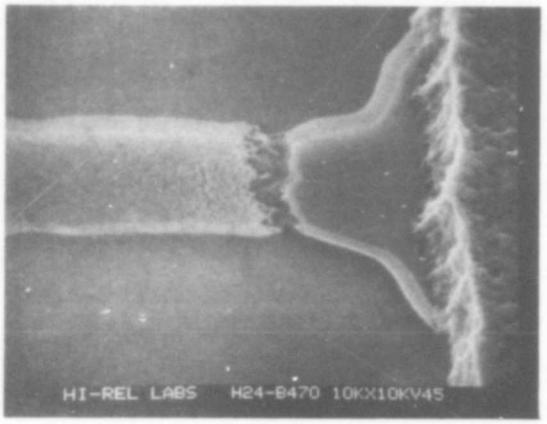


PULSE AMPLITUDE	21 VOLTS
LENGTH	1.9 ms
RISE TIME	125 μs
TIME-TO-PROGRAM (ADDITIONAL PHOTOGRAPH)	0.9 ms

g.



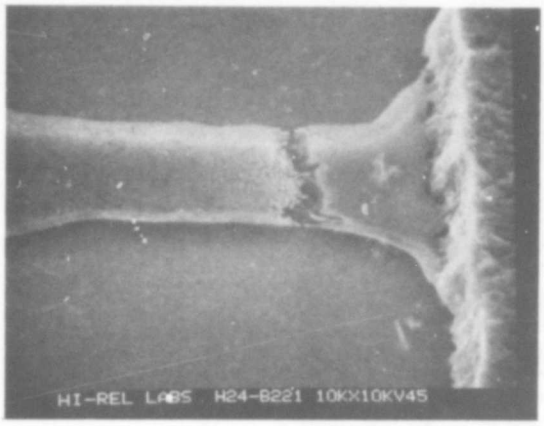
PULSE AMPLITUDE	21 VOLTS
LENGTH	12 ms
RISE TIME	125 μs
TIME-TO-PROGRAM	7.5 ms



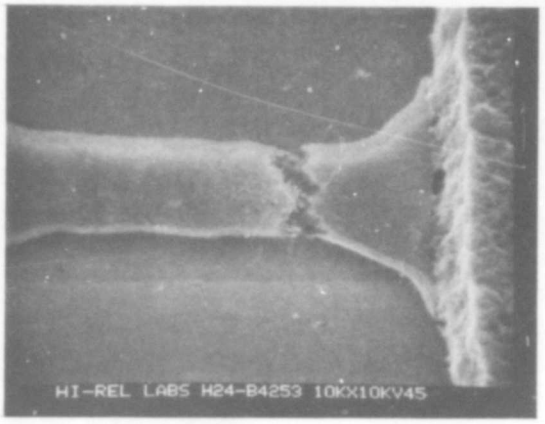
PULSE AMPLITUDE	21 VOLTS
LENGTH	12 ms
RISE TIME	125 μs
TIME-TO-PROGRAM	10.5 ms

h.

Figure 15. SEM photos of Vendor A nichrome fuse after plasma etch (sample 24) (sheet 4).

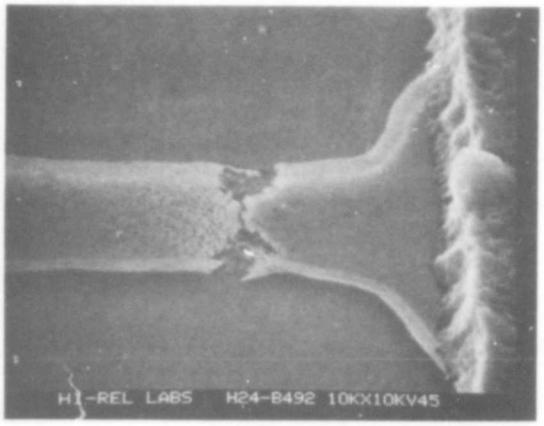


PULSE AMPLITUDE	20 VOLTS
LENGTH	192 ms
RISE TIME	123 μs
TIME-TO-PROGRAM	135 ms

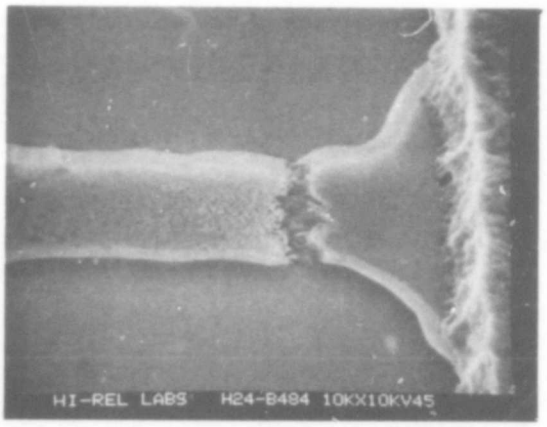


PULSE AMPLITUDE	20 VOLTS
LENGTH	192 ms
RISE TIME	125 μs
TIME-TO-PROGRAM	100 ms

i.



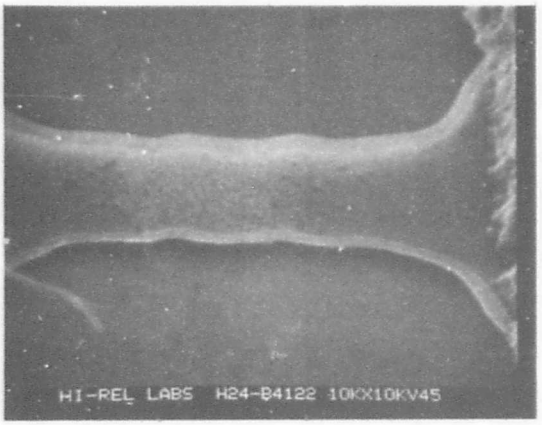
PULSE AMPLITUDE	20 VOLTS
LENGTH	12 ms
RISE TIME	125 μs
NUMBER OF PULSES TO PROGRAM	15 PULSES
TOTAL PROGRAMMING TIME	180 ms



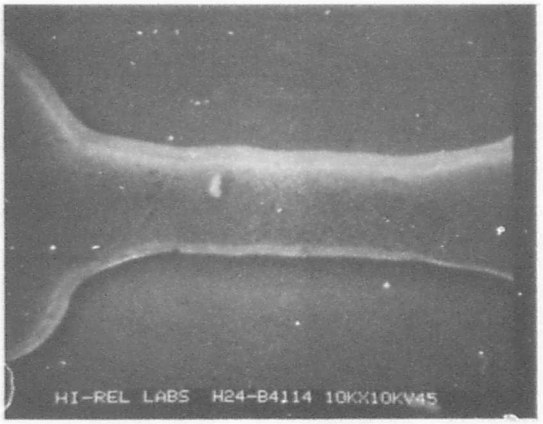
PULSE AMPLITUDE	20 VOLTS
LENGTH	12 ms
RISE TIME	125 μs
NUMBER OF PULSES TO PROGRAM	17 PULSES
TOTAL PROGRAMMING TIME	204 ms

j.

Figure 15. SEM photos of Vendor A nichrome fuse after plasma etch (sample 24) (sheet 5).



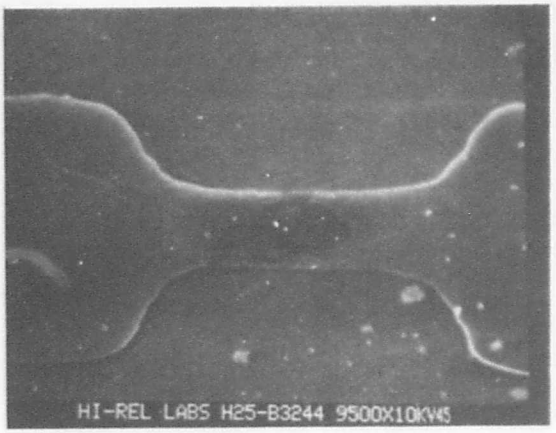
PULSE AMPLITUDE 20.5 VOLTS
LENGTH 12 ms
RISE TIME 125 μs
EXPERIENCED PARTIAL PROGRAMMING PULSE



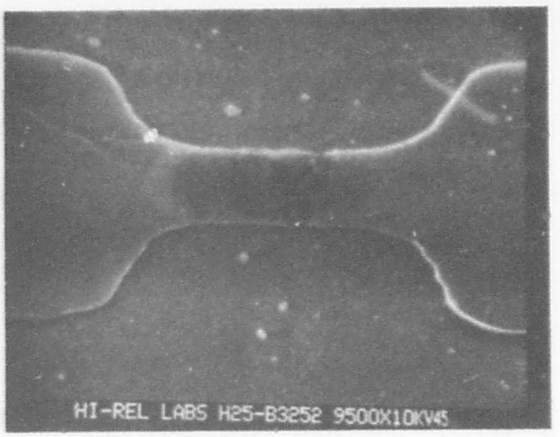
PULSE AMPLITUDE 20.5 VOLTS
LENGTH 12 ms
RISE TIME 125 μs
EXPERIENCED PARTIAL PROGRAMMING PULSE

k.

Figure 15. SEM photos of Vendor A nichrome fuse after plasma etch (sample 24) (sheet 6).

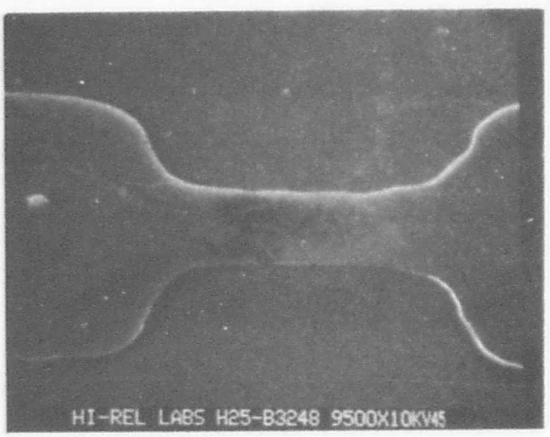


PULSE AMPLITUDE	25.0 VOLTS
LENGTH	12 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	5 μs

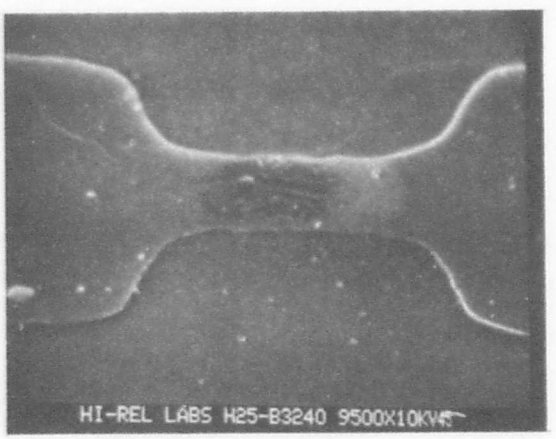


PULSE AMPLITUDE	25.0 VOLTS
LENGTH	12 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	5 μs

a.



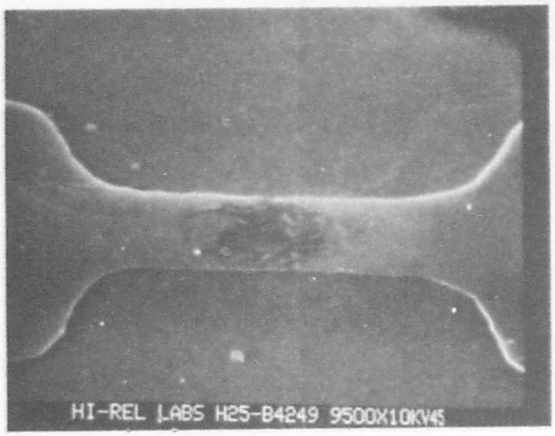
PULSE AMPLITUDE	25.0 VOLTS
LENGTH	12 ms
RISE TIME	130 μs
TIME-TO-PROGRAM	125 μs



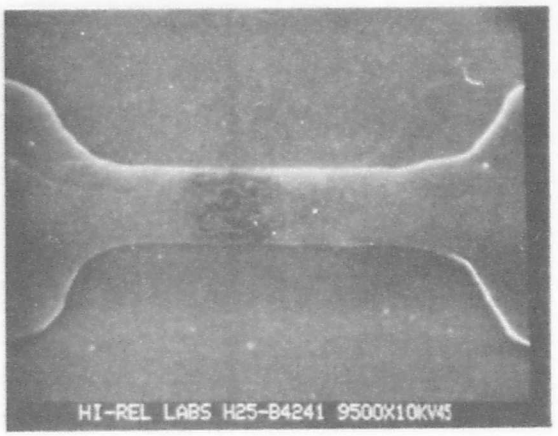
PULSE AMPLITUDE	25.0 VOLTS
LENGTH	12 ms
RISE TIME	130 μs
TIME-TO-PROGRAM	125 μs

b.

Figure 16. SEM photos of Vendor A nichrome fuse before plasma etch (sample 25) (sheet 1).

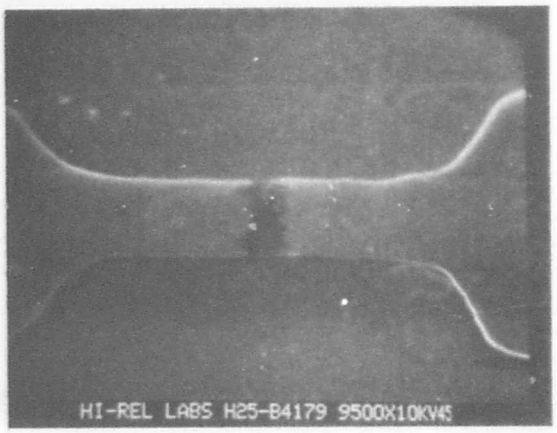


PULSE AMPLITUDE	25 VOLTS
LENGTH	192 ms
RISE TIME	130 μs
TIME-TO-PROGRAM	130 μs

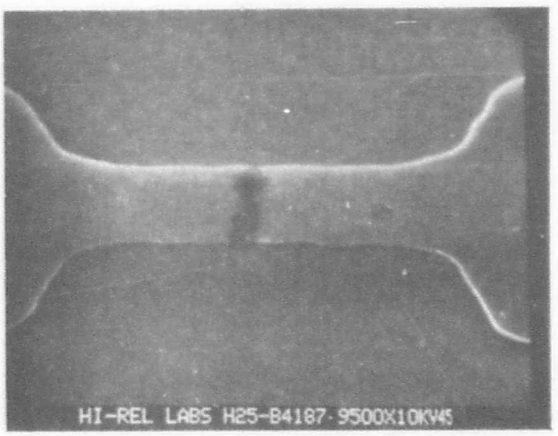


PULSE AMPLITUDE	25 VOLTS
LENGTH	192 ms
RISE TIME	130 μs
TIME-TO-PROGRAM	125 μs

c.



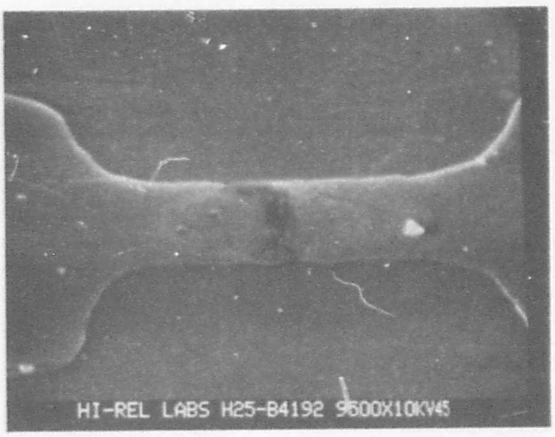
PULSE AMPLITUDE	22.5 VOLTS
LENGTH	192 ms
RISE TIME	125 μs
TIME-TO-PROGRAM	0.92 ms



PULSE AMPLITUDE	22.5 VOLTS
LENGTH	192 ms
RISE TIME	125 μs
TIME-TO-PROGRAM	1 ms

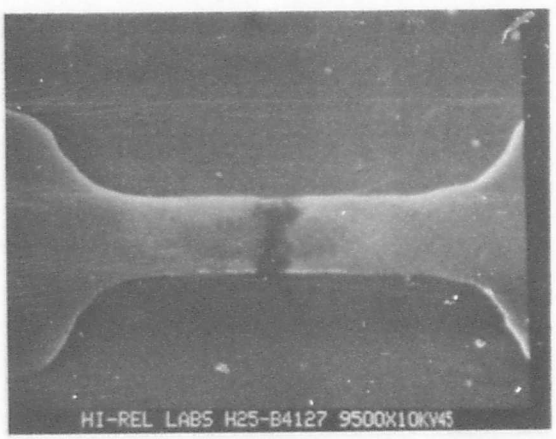
d.

Figure 16. SEM photos of Vendor A nichrome fuse before plasma etch (sample 25) (sheet 2).

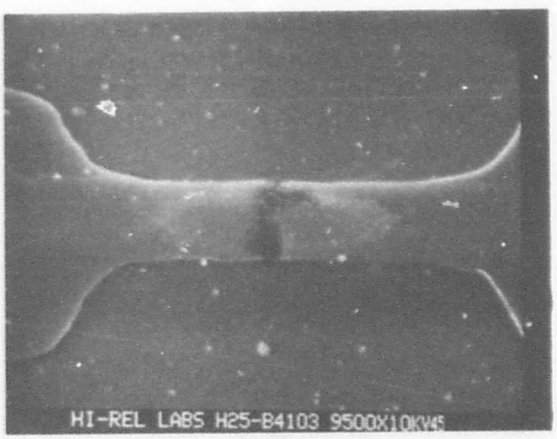


PULSE AMPLITUDE	21.5 VOLTS
LENGTH	1.9 ms
RISE TIME	122 μs
TIME-TO-PROGRAM	1.9 ms

e.



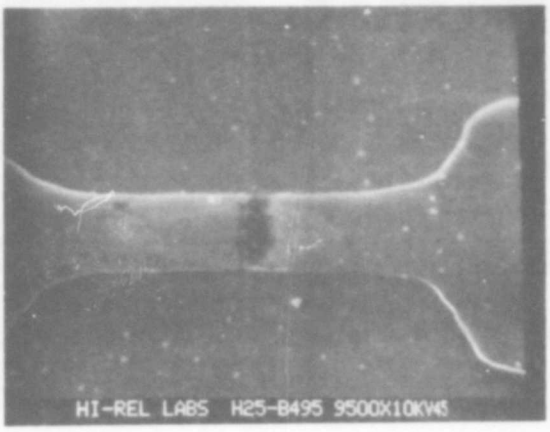
PULSE AMPLITUDE	21.5 VOLTS
LENGTH	192 ms
RISE TIME	130 μs
TIME-TO-PROGRAM	8.1 ms



PULSE AMPLITUDE	21.5 VOLTS
LENGTH	192 ms
RISE TIME	130 μs
TIME-TO-PROGRAM	11.2 ms

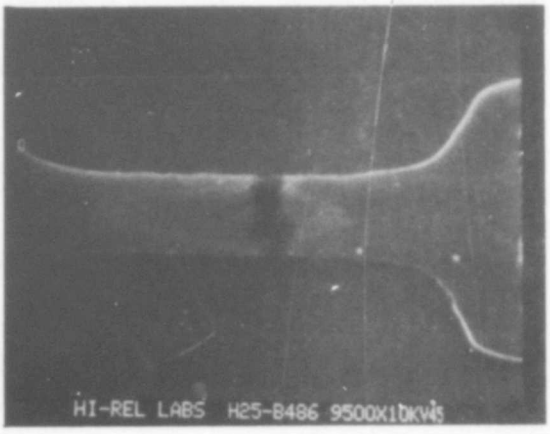
f.

Figure 16. SEM photos of Vendor A nichrome fuse before plasma etch (sample 25) (sheet 3).



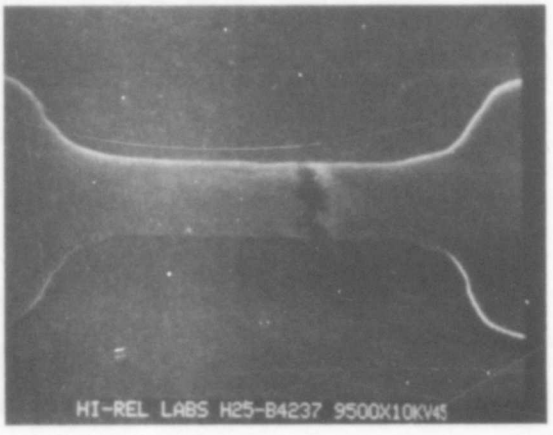
PULSE AMPLITUDE	21.5 VOLTS
LENGTH	192 μs
RISE TIME	122 μs
TIME-TO-PROGRAM	11.2 ms

g.



PULSE AMPLITUDE	21.0 VOLTS
LENGTH	12 ms
RISE TIME	120 μs
TIME-TO-PROGRAM	8.6 ms

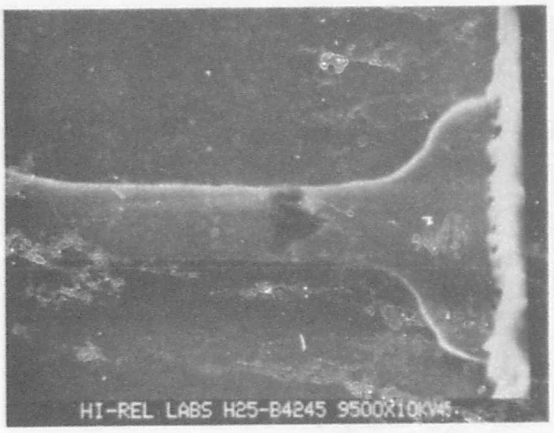
h.



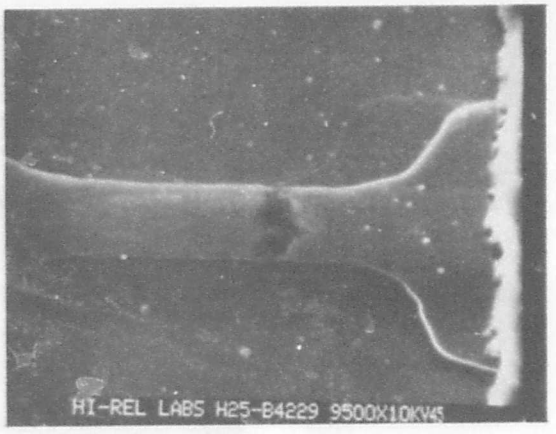
PULSE AMPLITUDE	20.5 VOLTS
LENGTH	192 ms
RISE TIME	122 μs
TIME-TO-PROGRAM	100 ms

i.

Figure 16. SEM photos of Vendor A nichrome fuse before plasma etch (sample 25) (sheet 4).

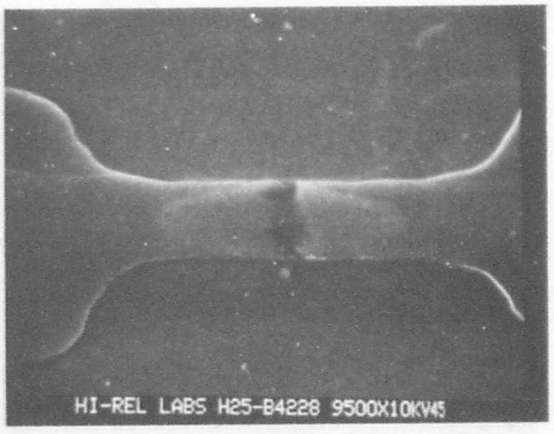


PULSE AMPLITUDE	20.5 VOLTS
LENGTH	192 ms
RISE TIME	122 μs
TIME-TO-PROGRAM	100 ms



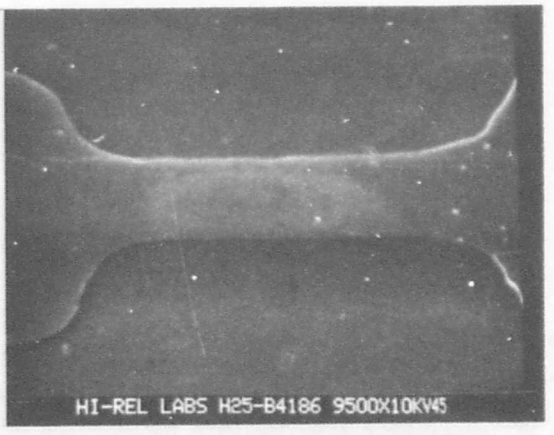
PULSE AMPLITUDE	20.5 VOLTS
LENGTH	192 ms
RISE TIME	122 μs
TIME-TO-PROGRAM	144 ms

j.



PULSE AMPLITUDE	20.5 VOLTS
LENGTH	12 ms
RISE TIME	122 μs
NUMBER OF PULSES TO PROGRAM	9 PULSES
TOTAL PROGRAMMING TIME	108 ms

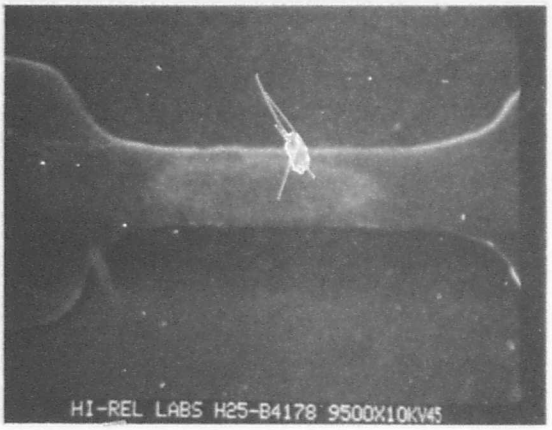
k.



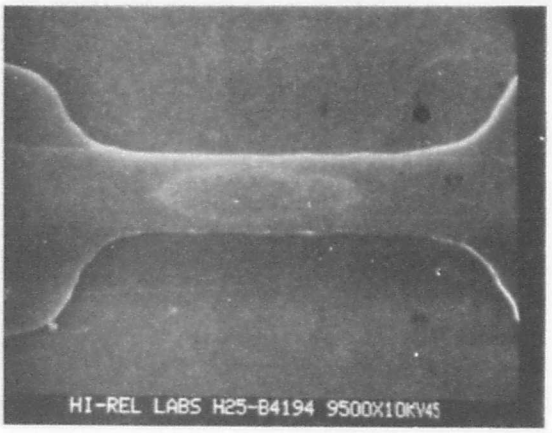
PULSE AMPLITUDE	20.8 VOLTS
LENGTH	12 ms
RISE TIME	120 μs
EXPERIENCE PARTIAL PROGRAMMING PULSE	

l.

Figure 16. SEM photos of Vendor A nichrome fuse before plasma etch (sample 25) (sheet 5).

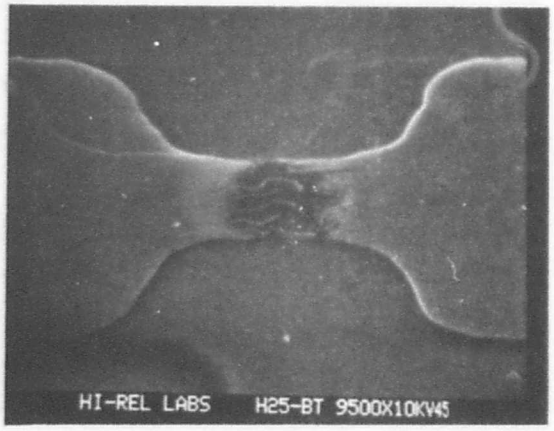


PULSE AMPLITUDE 20.8 VOLTS
LENGTH 12 ms
RISE TIME 120 μs
EXPERIENCE PARTIAL PROGRAMMING PULSE

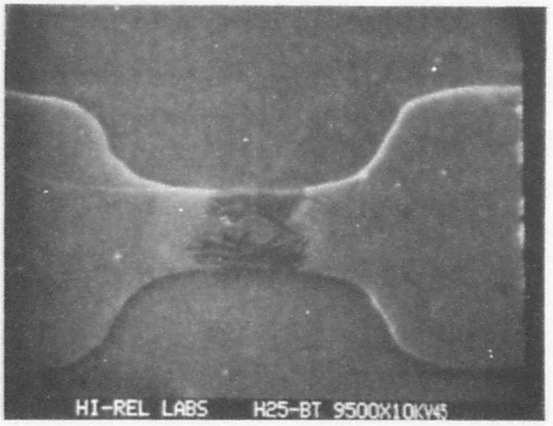


PULSE AMPLITUDE 20.8 VOLTS
LENGTH 12 ms
RISE TIME 120 μs
EXPERIENCE PARTIAL PROGRAMMING PULSE

m.



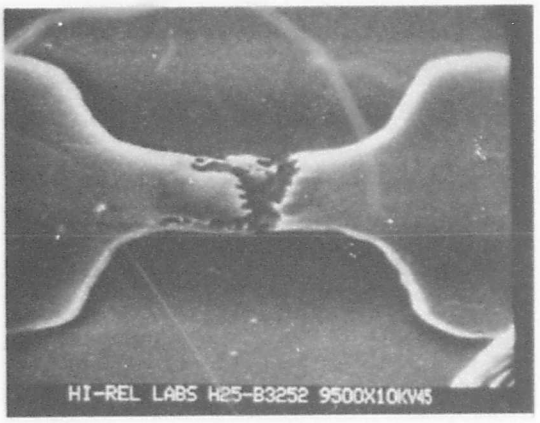
TEST FUSE PROGRAMMED BY MANUFACTURER BEFORE SHIPMENT



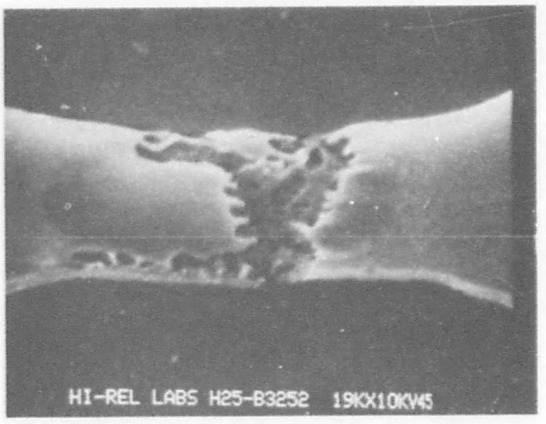
TEST FUSE PROGRAMMED BY MANUFACTURER BEFORE SHIPMENT

n.

Figure 16. SEM photos of Vendor A nichrome fuse before plasma etch (sample 25) (sheet 6).

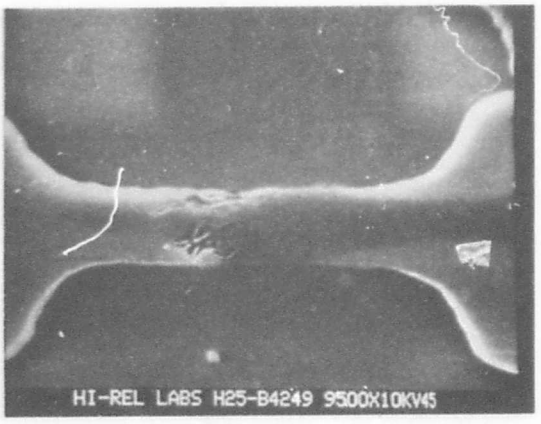


PULSE AMPLITUDE	25 VOLTS
LENGTH	12 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	5 μs

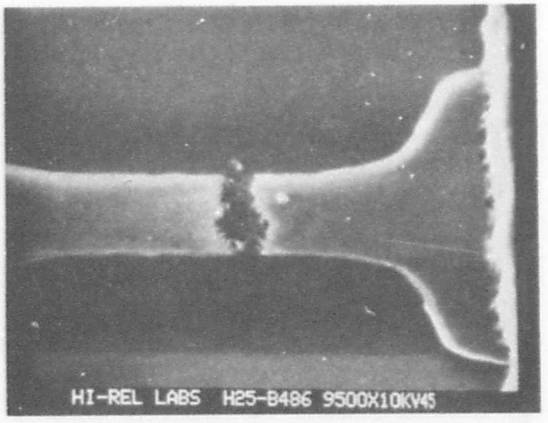


PULSE AMPLITUDE	25 VOLTS
LENGTH	12 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM (ADDITIONAL PHOTOGRAPH)	5 μs

a.



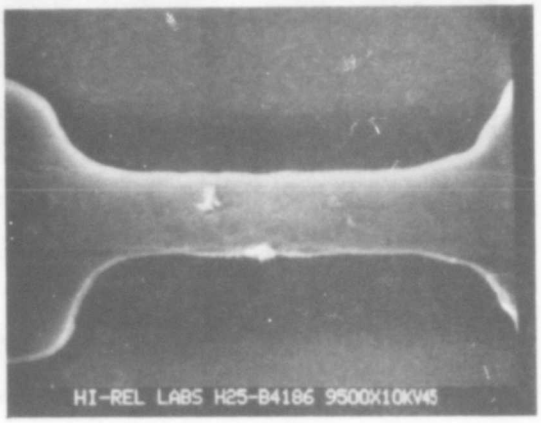
PULSE AMPLITUDE	25 VOLTS
LENGTH	192 ms
RISE TIME	130 μs
TIME-TO-PROGRAM	130 μs



PULSE AMPLITUDE	21 VOLTS
LENGTH	12 ms
RISE TIME	120 μs
TIME-TO-PROGRAM	8.6 ms

b.

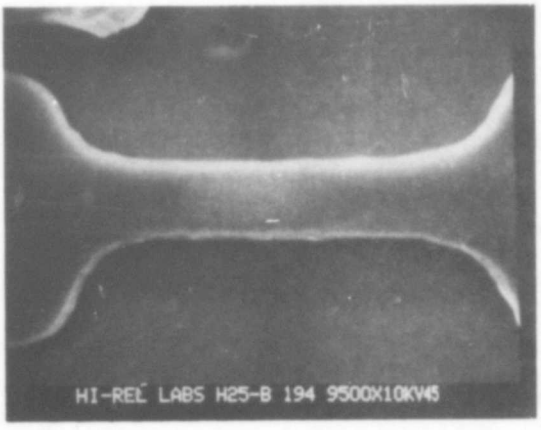
Figure 17. SEM photos of Vendor A nichrome fuse after plasma etch (sample 25) (sheet 1).



PULSE AMPLITUDE	20.8 VOLTS
LENGTH	12 ms
RISE TIME	120 μs

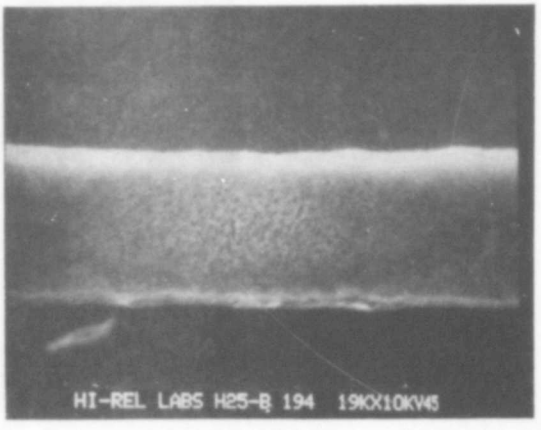
EXPERIENCED PARTIAL PROGRAMMING PULSE

c.



PULSE AMPLITUDE	20.8 VOLTS
LENGTH	12 ms
RISE TIME	120 μs

EXPERIENCED PARTIAL PROGRAMMING PULSE

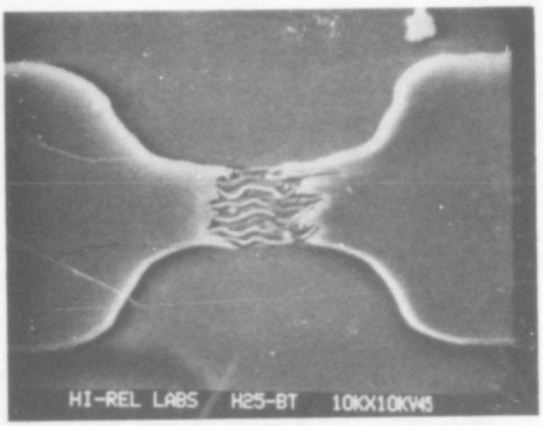


PULSE AMPLITUDE	20.8 VOLTS
LENGTH	12 ms
RISE TIME	120 μs

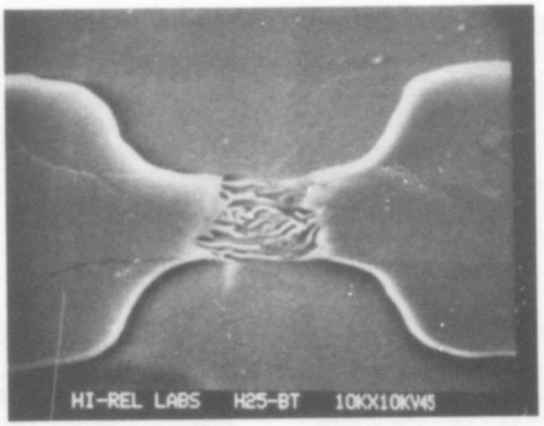
EXPERIENCED PARTIAL PROGRAMMING PULSE
(ADDITIONAL PHOTOGRAPH AFTER PLASMA ETCH)

d.

Figure 17. SEM photos of Vendor A nichrome fuse after plasma etch (sample 25) (sheet 2).



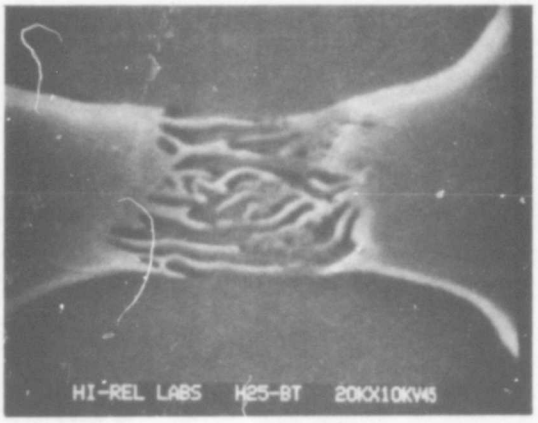
BT1
TEST FUSE PROGRAMMED BY MANUFACTURER
BEFORE SHIPMENT



BT2
TEST FUSE PROGRAMMED BY MANUFACTURER
BEFORE SHIPMENT

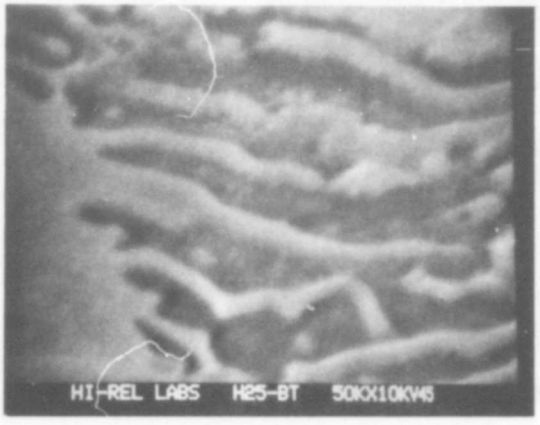
e.

Figure 17. SEM photos of Vendor A nichrome fuse after plasma etch (sample 25) (sheet 3).



BT2

TEST FUSE PROGRAMMED BY MANUFACTURER
(ADDITIONAL PHOTO)

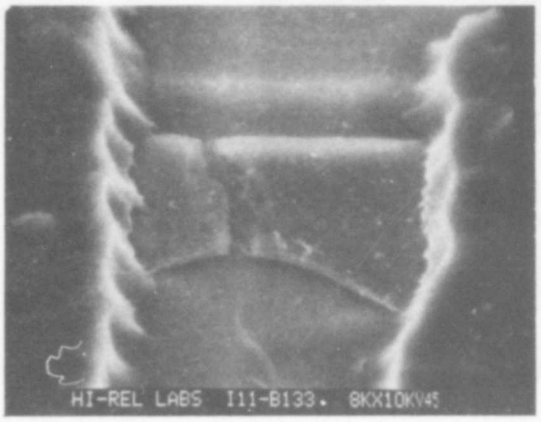


BT2

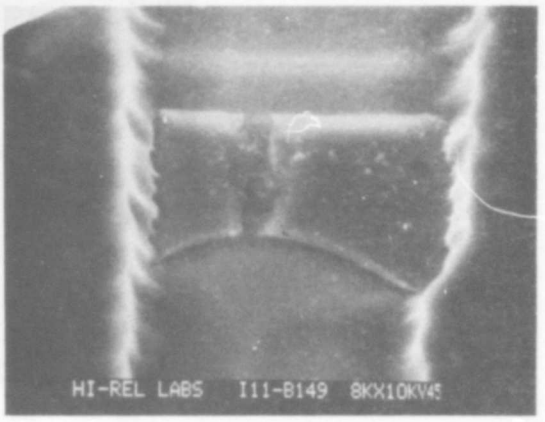
TEST FUSE PROGRAMMED BY MANUFACTURER
(ADDITIONAL PHOTO)

f.

Figure 17. SEM photos of Vendor A nichrome fuse after plasma etch (sample 25) (sheet 4).

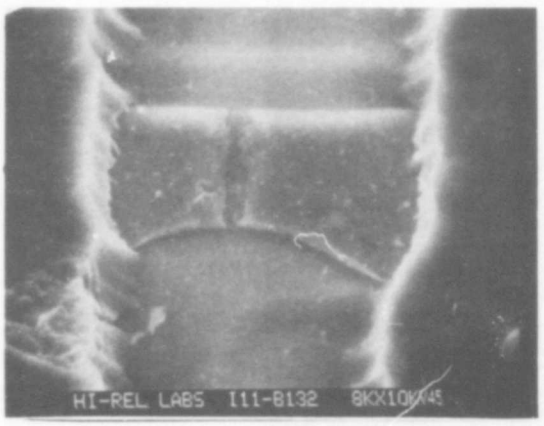


PULSE AMPLITUDE	26 VOLTS
LENGTH	10 ms
RISE TIME	2.5 μs
TIME-TO-PROGRAM	3 μs

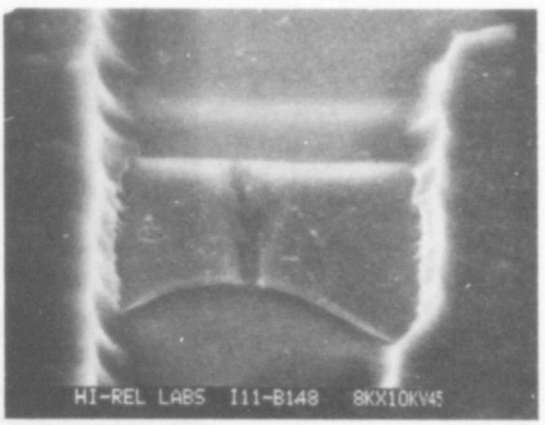


PULSE AMPLITUDE	26 VOLTS
LENGTH	10 ms
RISE TIME	2.5 μs
TIME-TO-PROGRAM	3 μs

a.



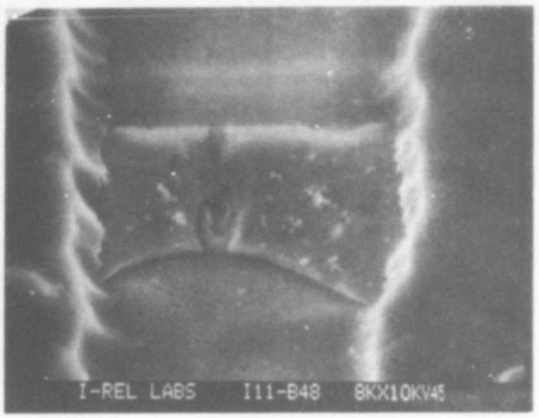
PULSE AMPLITUDE	26 VOLTS
LENGTH	10 ms
RISE TIME	60 μs
TIME-TO-PROGRAM	55 μs



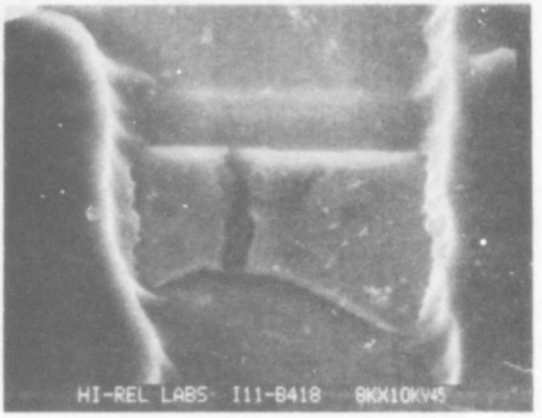
PULSE AMPLITUDE	26 VOLTS
LENGTH	10 ms
RISE TIME	60 μs
TIME-TO-PROGRAM	55 μs

b.

Figure 18. SEM photos of Vendor B nichrome fuse before plasma etch (sample 11) (sheet 1).

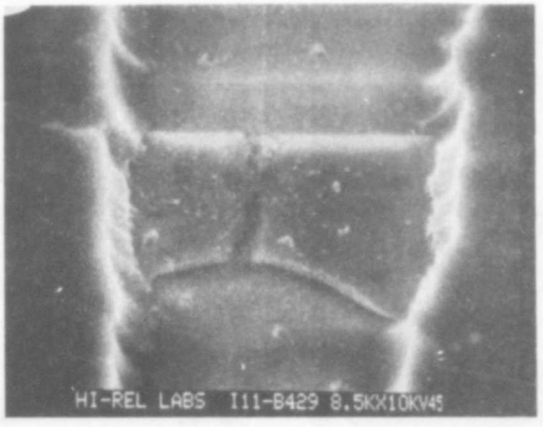


PULSE AMPLITUDE	21 VOLTS
LENGTH	200 ms
RISE TIME	28 μs
TIME-TO-PROGRAM	28 μs



PULSE AMPLITUDE	21 VOLTS
LENGTH	200 ms
RISE TIME	28 μs
TIME-TO-PROGRAM	28 μs

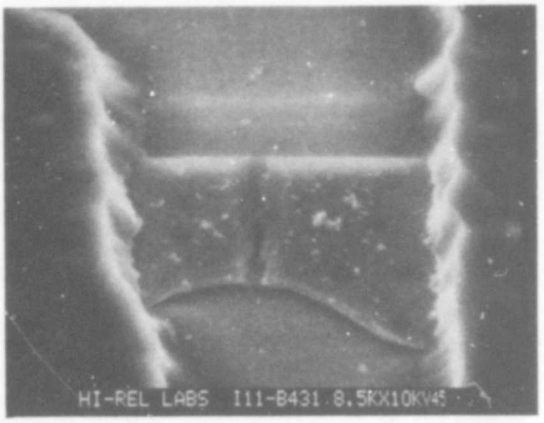
c.



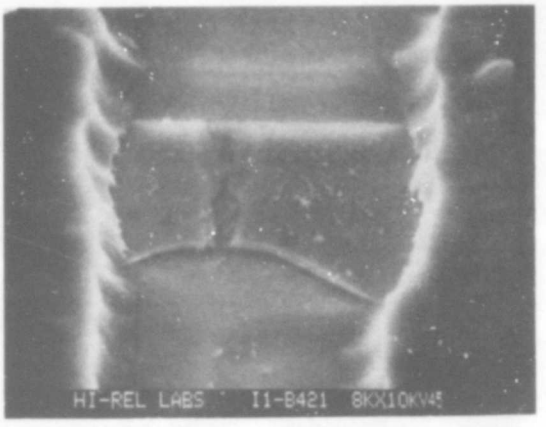
PULSE AMPLITUDE	21 VOLTS
LENGTH	200 ms
RISE TIME	28 μs
TIME-TO-PROGRAM	30 μs

d.

Figure 18. SEM photos of Vendor B nichrome fuse before plasma etch (sample 11) (sheet 2).

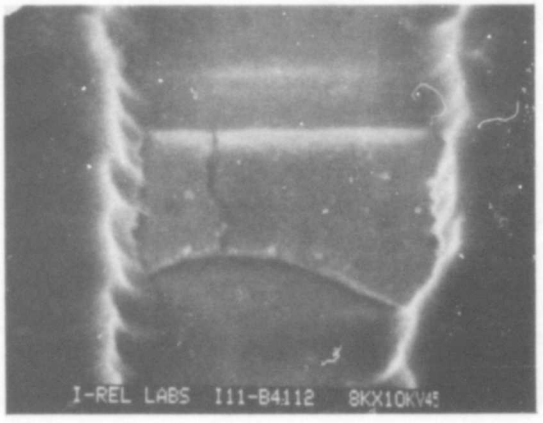


PULSE AMPLITUDE	21 VOLTS
LENGTH	40 μs
RISE TIME	28 μs
TIME-TO-PROGRAM	30 μs

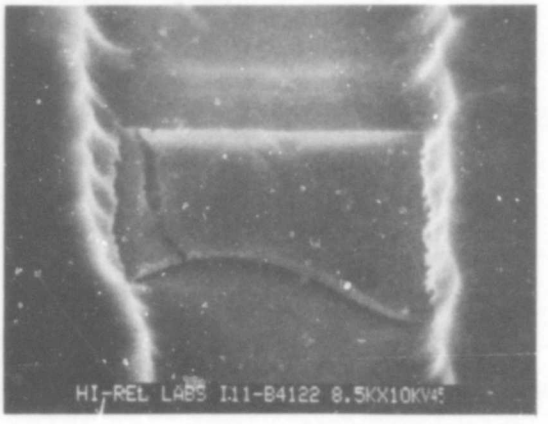


PULSE AMPLITUDE	21 VOLTS
LENGTH	40 μs
RISE TIME	28 μs
TIME-TO-PROGRAM	35 μs

e.



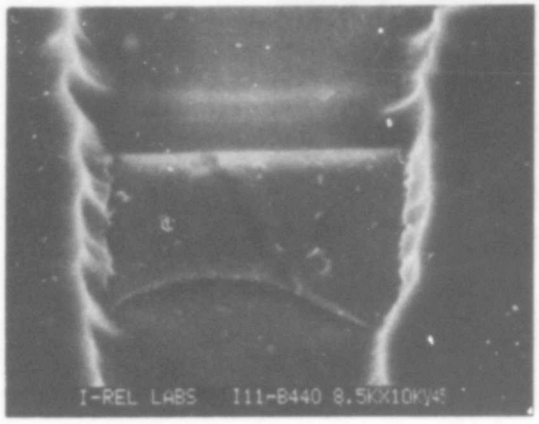
PULSE AMPLITUDE	12.5 VOLTS
LENGTH	200 ms
RISE TIME	15 μs
TIME-TO-PROGRAM	360 μs



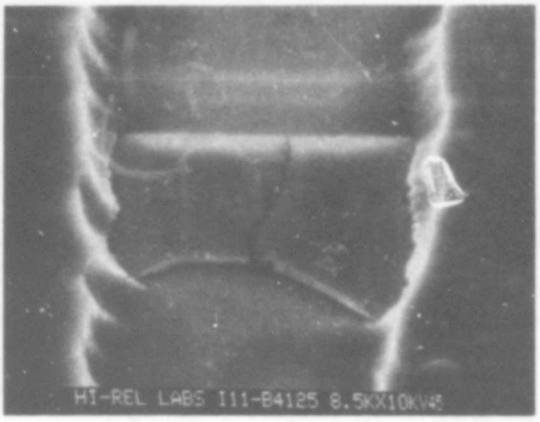
PULSE AMPLITUDE	12.5 VOLTS
LENGTH	200 ms
RISE TIME	15 μs
TIME-TO-PROGRAM	800 μs

f.

Figure 18. SEM photos of Vendor B nichrome fuse before plasma etch (sample 11) (sheet 3).

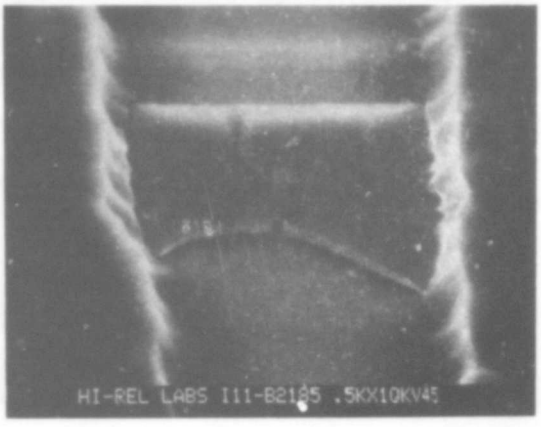


PULSE AMPLITUDE	12.5 VOLTS
LENGTH	2 ms
RISE TIME	15 μs
TIME-TO-PROGRAM	810 μs

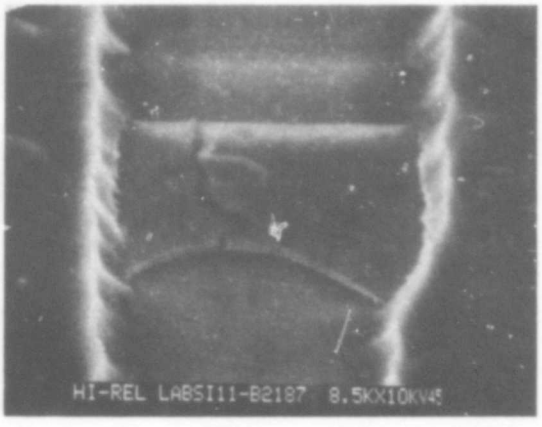


PULSE AMPLITUDE	12.5 VOLTS
LENGTH	2 ms
RISE TIME	15 μs
TIME-TO-PROGRAM	800 μs

g.



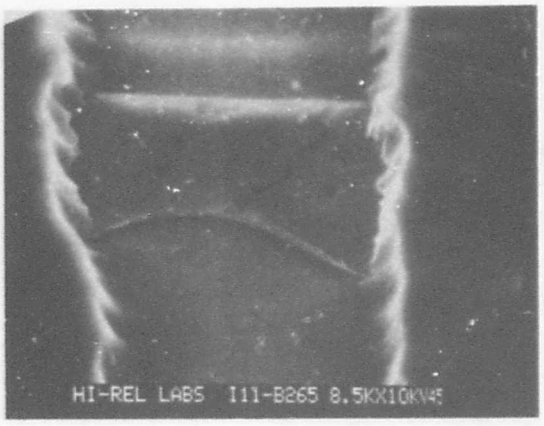
PULSE AMPLITUDE	12.3 VOLTS
LENGTH	200 ms
RISE TIME	14 μs
TIME-TO-PROGRAM	144 ms



PULSE AMPLITUDE	12.3 VOLTS
LENGTH	200 ms
RISE TIME	14 μs
TIME-TO-PROGRAM	130 ms

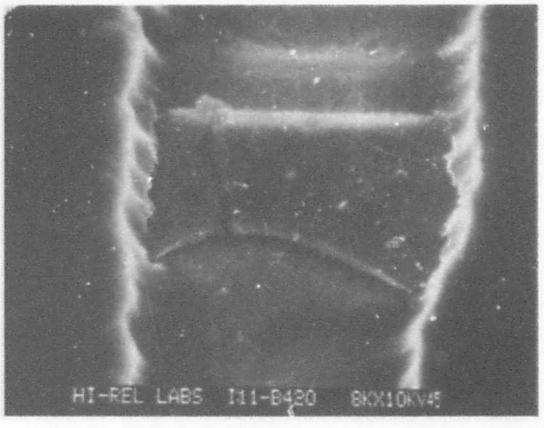
h.

Figure 18. SEM photos of Vendor B nichrome fuse before plasma etch (sample 11) (sheet 4).

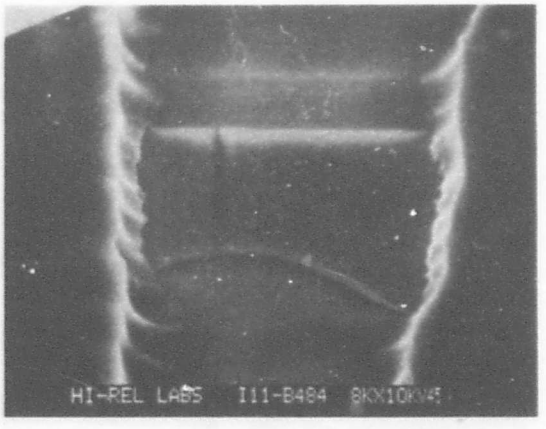


PULSE AMPLITUDE	12.3 VOLTS
LENGTH	200 ms
RISE TIME	14 μs
TIME-TO-PROGRAM	180 ms

i.



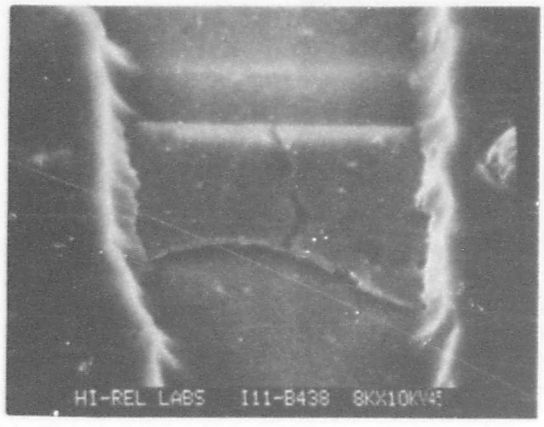
PULSE AMPLITUDE	12 VOLTS
LENGTH	10 ms
RISE TIME	15 μs
TIME-TO-PROGRAM	2.9 ms



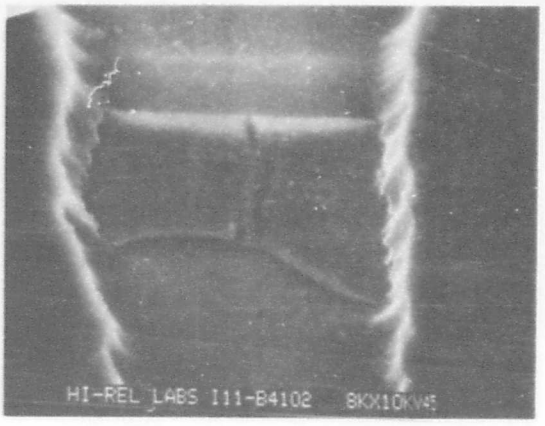
PULSE AMPLITUDE	12 VOLTS
LENGTH	10 ms
RISE TIME	15 μs
TIME-TO-PROGRAM	3.2 ms

j.

Figure 18. SEM photos of Vendor B nichrome fuse before plasma etch (sample 11) (sheet 5).

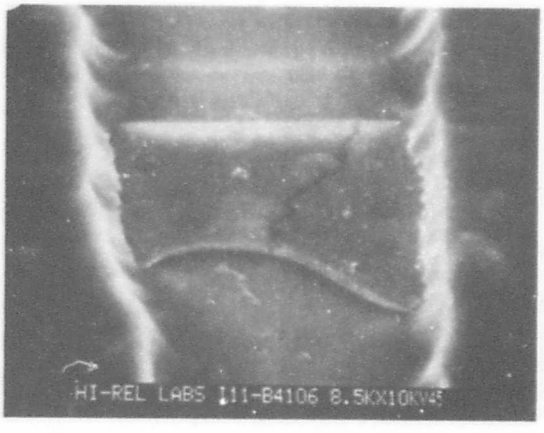


PULSE AMPLITUDE	12 VOLTS
LENGTH	200 ms
RISE TIME	15 μs
TIME-TO-PROGRAM	3.5 ms

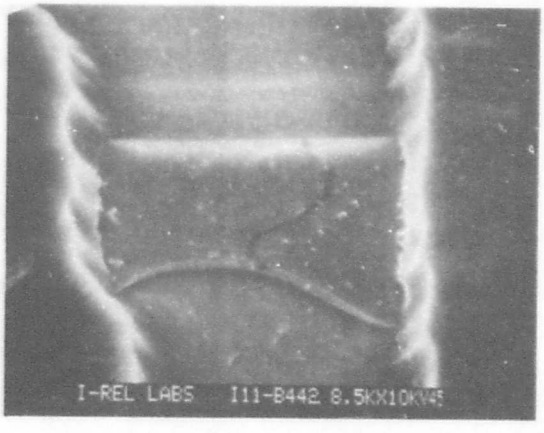


PULSE AMPLITUDE	12 VOLTS
LENGTH	200 ms
RISE TIME	15 μs
TIME-TO-PROGRAM	3.4 ms

k.



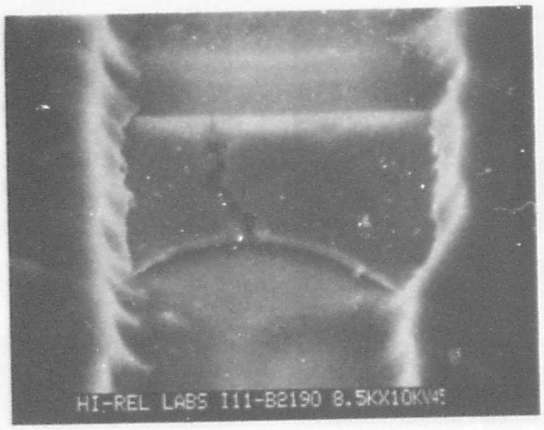
PULSE AMPLITUDE	11.2 VOLTS
LENGTH	200 ms
RISE TIME	14 μs
TIME-TO-PROGRAM	21 ms



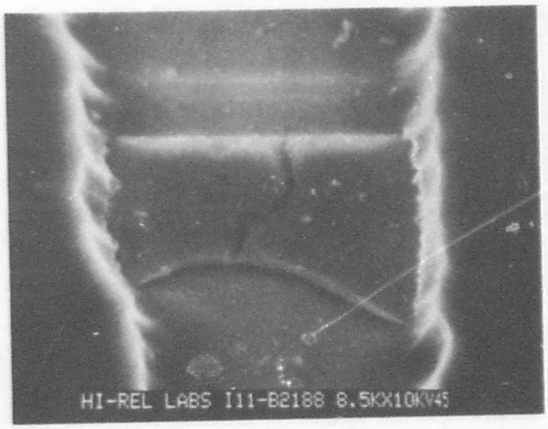
PULSE AMPLITUDE	11.2 VOLTS
LENGTH	200 ms
RISE TIME	14 μs
TIME-TO-PROGRAM	25 ms

l.

Figure 18. SEM photos of Vendor B nichrome fuse before plasma etch (sample 11) (sheet 6).



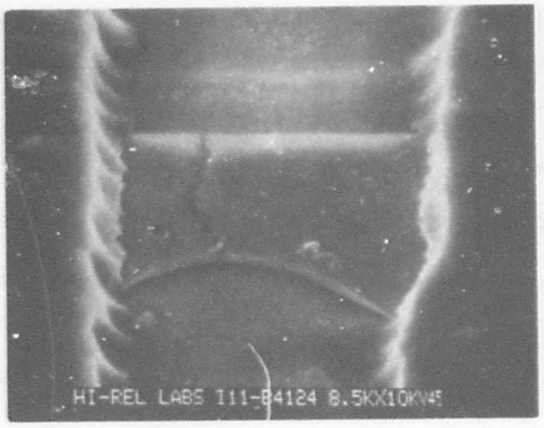
PULSE AMPLITUDE	12 VOLTS
LENGTH	200 ms
RISE TIME	15 μs
NUMBER OF PULSES TO PROGRAM	4 PULSES
TOTAL PROGRAMMING TIME	800 ms



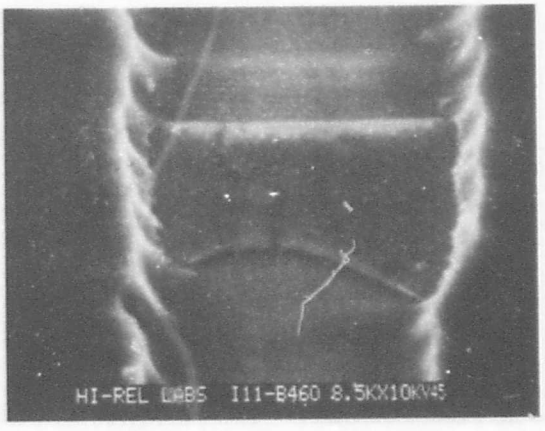
PULSE AMPLITUDE	11 VOLTS
LENGTH	200 ms
RISE TIME	15 μs
NUMBER OF PULSES TO PROGRAM	7 PULSES
TOTAL PROGRAMMING TIME	1300 ms

m.

Figure 18. SEM photos of Vendor B nichrome fuse before plasma etch (sample 11) (sheet 7).



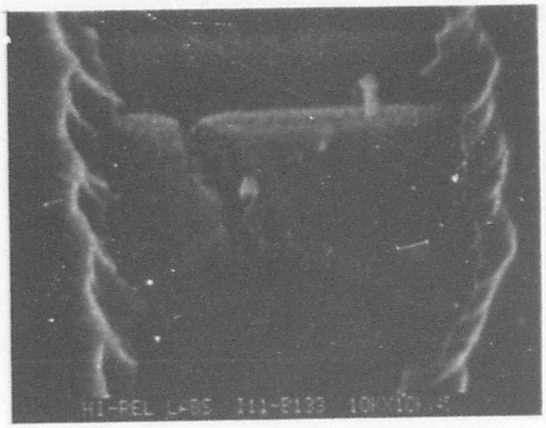
PULSE AMPLITUDE	10.8 VOLTS
LENGTH	10 ms
RISE TIME	13 μs
NUMBER OF PULSES TO PROGRAM	17 PULSES
TOTAL PROGRAMMING TIME	170 ms



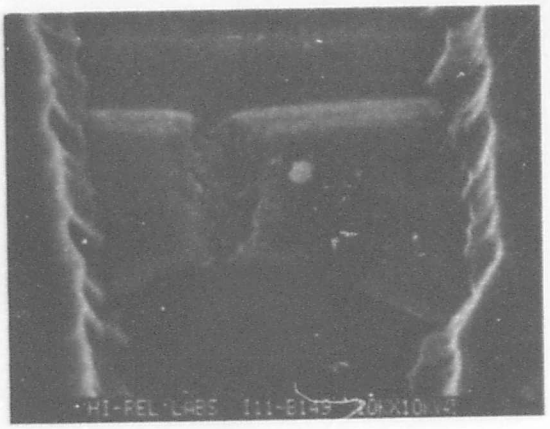
PULSE AMPLITUDE	10.8 VOLTS
LENGTH	10 ms
RISE TIME	13 μs
NUMBER OF PULSES TO PROGRAM	10 PULSES
TOTAL PROGRAMMING TIME	100 ms

n.

Figure 18. SEM photos of Vensor B nichrome fuse before plasma etch (sample 11) (sheet 8).

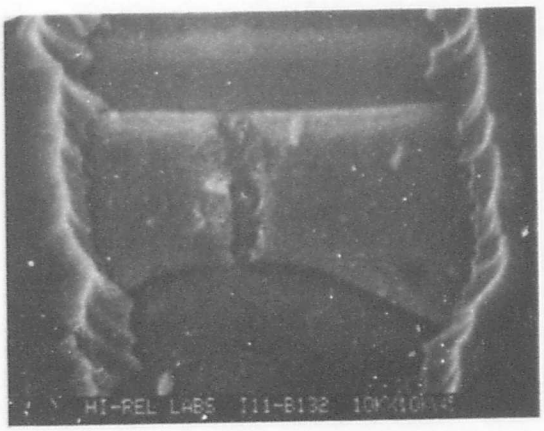


PULSE AMPLITUDE	26 VOLTS
LENGTH	10 ms
RISE TIME	2.5 μs
TIME-TO-PROGRAM	3 μs

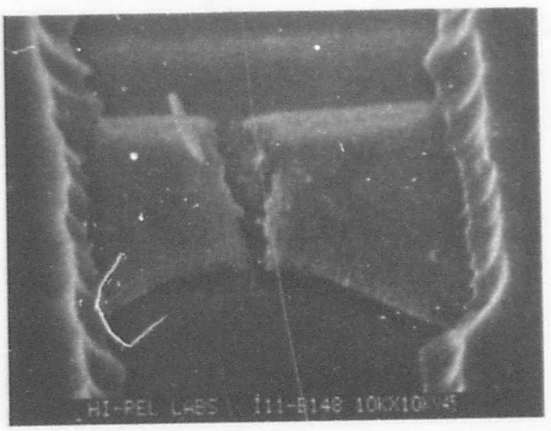


PULSE AMPLITUDE	26 VOLTS
LENGTH	10 ms
RISE TIME	2.5 μs
TIME-TO-PROGRAM	3 μs

a.



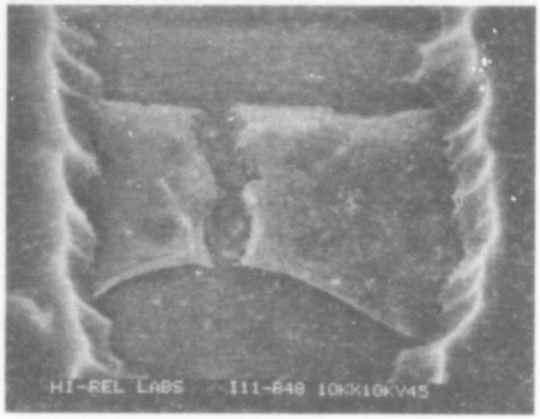
PULSE AMPLITUDE	26 VOLTS
LENGTH	10 ms
RISE TIME	60 μs
TIME-TO-PROGRAM	55 μs



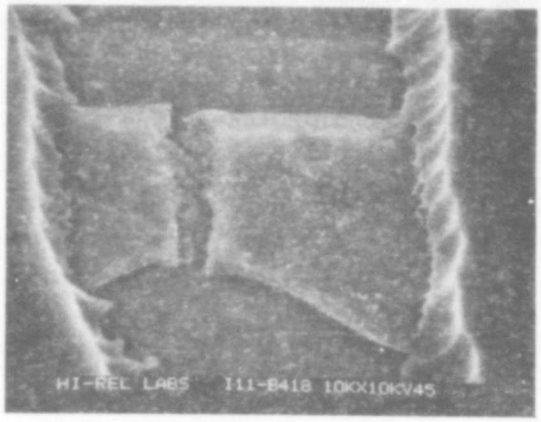
PULSE AMPLITUDE	26 VOLTS
LENGTH	10 ms
RISE TIME	60 μs
TIME-TO-PROGRAM	55 μs

b.

Figure 19. SEM photos of Vendor B nichrome fuse after plasma etch (sample 11) (sheet 1).

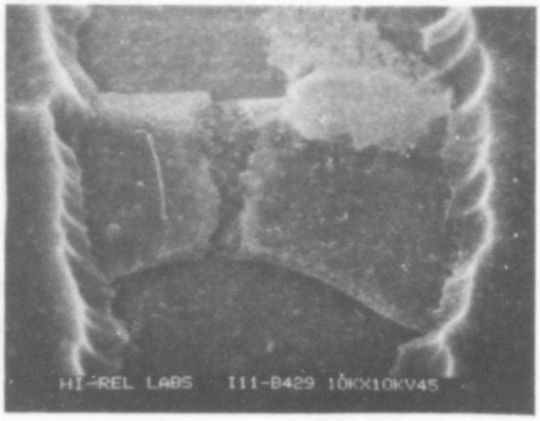


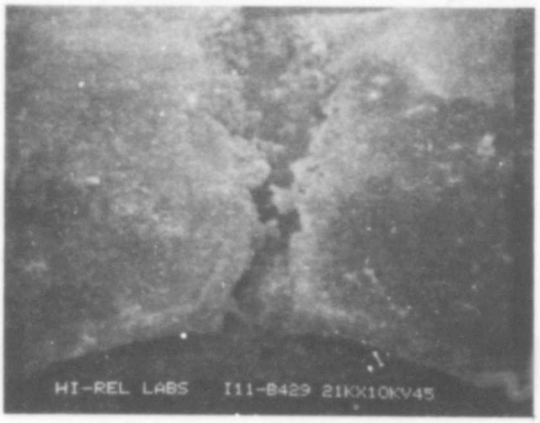
PULSE AMPLITUDE	21 VOLTS
LENGTH	200 ms
RISE TIME	28 μs
TIME-TO-PROGRAM	28 μs



PULSE AMPLITUDE	21 VOLTS
LENGTH	200 ms
RISE TIME	28 μs
TIME-TO-PROGRAM	28 μs

c.

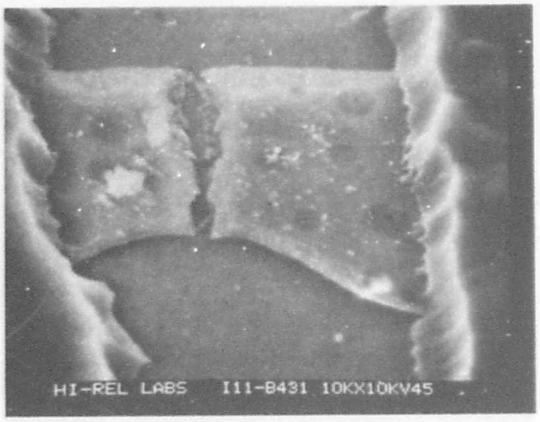




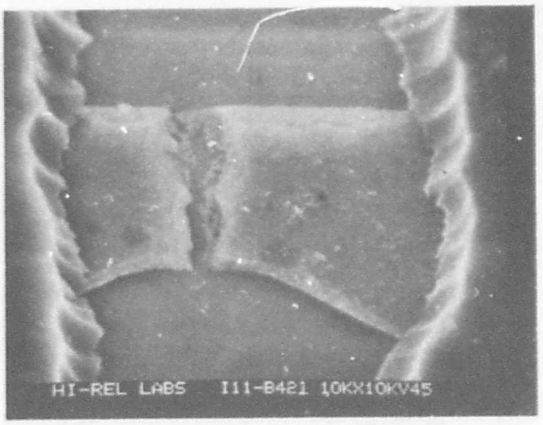
PULSE AMPLITUDE	21 VOLTS
LENGTH	200 ms
RISE TIME	28 μs
TIME-TO-PROGRAM	30 μs

d.

Figure 19. SEM photos of Vendor B nichrome fuse after plasma etch (sample 11) (sheet 2).

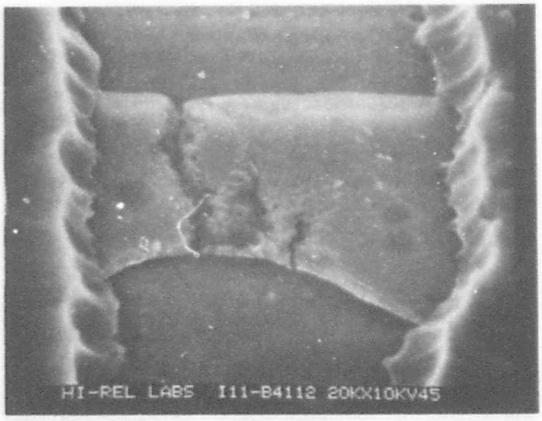


PULSE AMPLITUDE	21 VOLTS
LENGTH	40 μs
RISE TIME	28 μs
TIME-TO-PROGRAM	30 μs

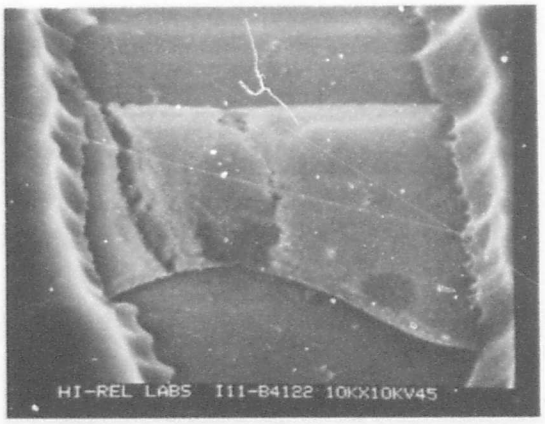


PULSE AMPLITUDE	21 VOLTS
LENGTH	40 μs
RISE TIME	28 μs
TIME-TO-PROGRAM	35 μs

e.



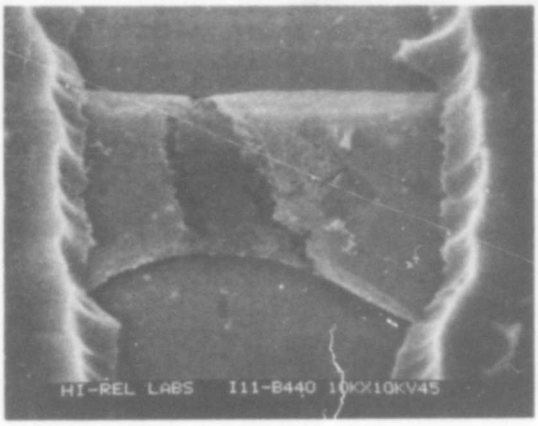
PULSE AMPLITUDE	12.5 VOLTS
LENGTH	200 ms
RISE TIME	15 μs
TIME-TO-PROGRAM	360 μs



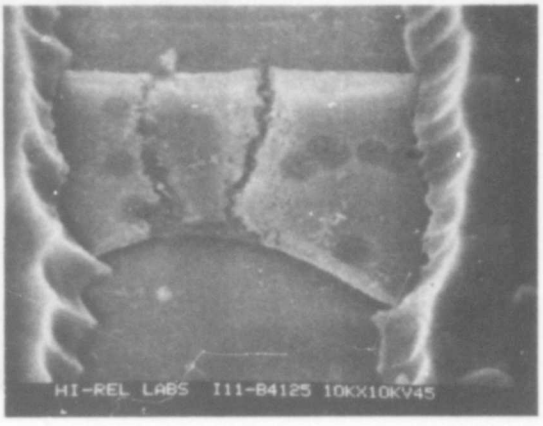
PULSE AMPLITUDE	12.5 VOLTS
LENGTH	200 ms
RISE TIME	15 μs
TIME-TO-PROGRAM	800 μs

f.

Figure 19. SEM photos of Vendor B nichrome fuse after plasma etch (sample 11) (sheet 3).

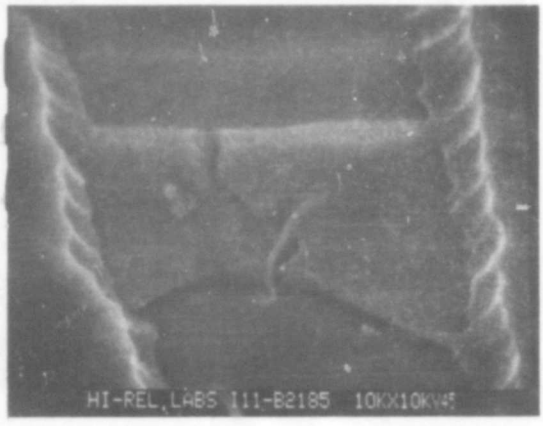


PULSE AMPLITUDE	12.5 VOLTS
LENGTH	2 ms
RISE TIME	15 μs
TIME-TO-PROGRAM	810 μs

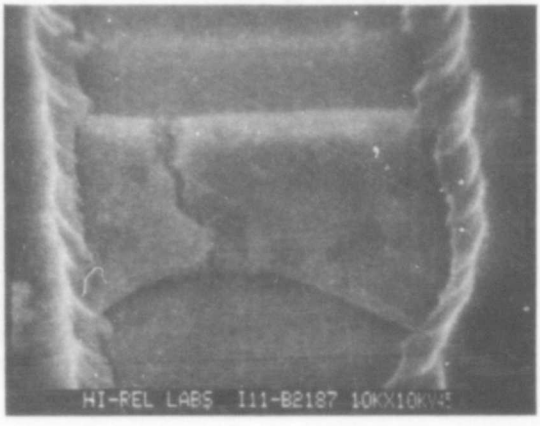


PULSE AMPLITUDE	12.5 VOLTS
LENGTH	2 ms
RISE TIME	15 μs
TIME-TO-PROGRAM	800 μs

g.



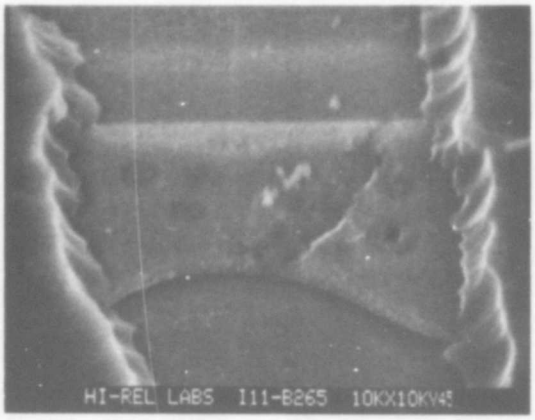
PULSE AMPLITUDE	12.3 VOLTS
LENGTH	200 ms
RISE TIME	14 μs
TIME-TO-PROGRAM	144 ms



PULSE AMPLITUDE	12.3 VOLTS
LENGTH	200 ms
RISE TIME	14 μs
TIME-TO-PROGRAM	130 ms

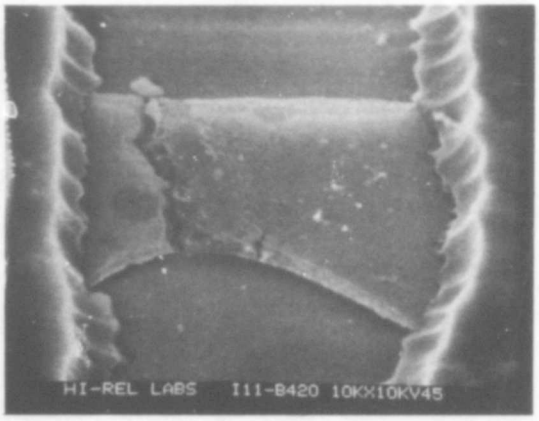
h.

Figure 19. SEM photos of Vendor B nichrome fuse after plasma etch (sample 11) (sheet 4).

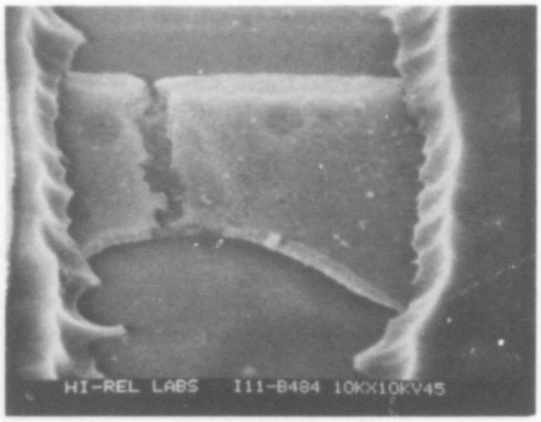


PULSE AMPLITUDE	12.3 VOLTS
LENGTH	200 ms
RISE TIME	14 μs
TIME-TO-PROGRAM	180 ms

i.



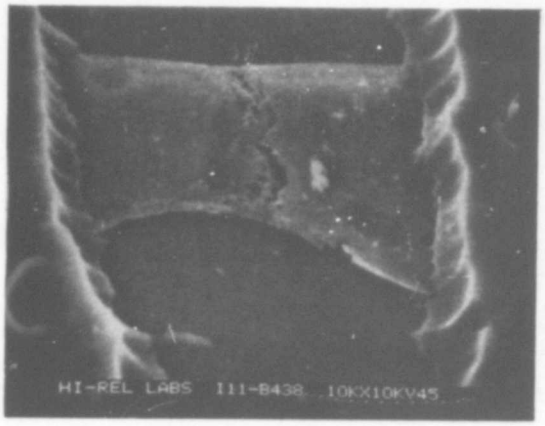
PULSE AMPLITUDE	12 VOLTS
LENGTH	10 ms
RISE TIME	15 μs
TIME-TO-PROGRAM	2.5 ms



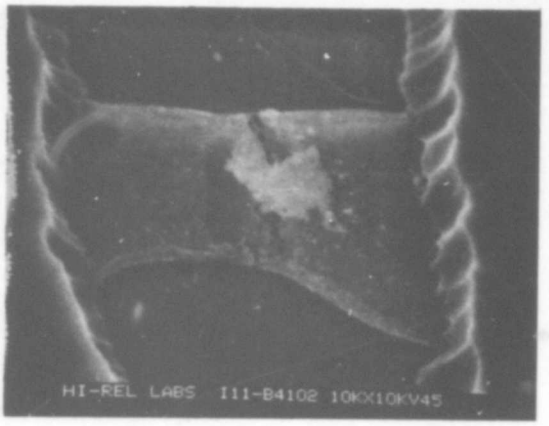
PULSE AMPLITUDE	12 VOLTS
LENGTH	10 ms
RISE TIME	15 μs
TIME-TO-PROGRAM	3.2 ms

j.

Figure 19. SEM photos of Vendor B nichrome fuse after plasma etch (sample 11) (sheet 5).

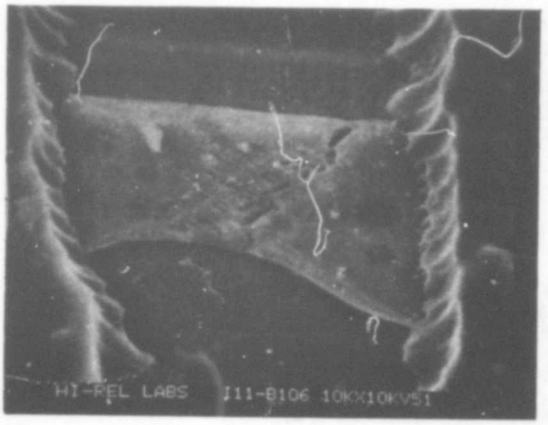


PULSE AMPLITUDE	12 VOLTS
LENGTH	200 ms
RISE TIME	15 μs
TIME-TO-PROGRAM	3.5 ms

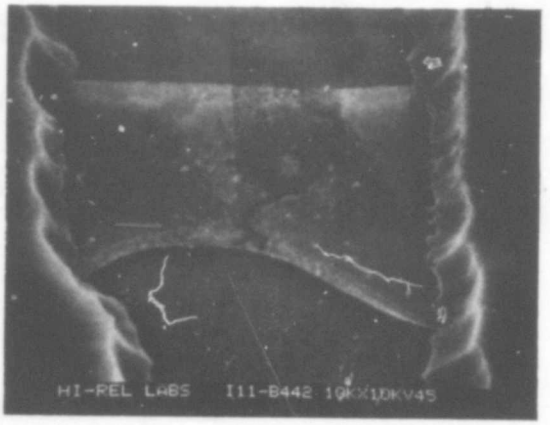


PULSE AMPLITUDE	12 VOLTS
LENGTH	200 ms
RISE TIME	15 μs
TIME-TO-PROGRAM	3.4 ms

k.



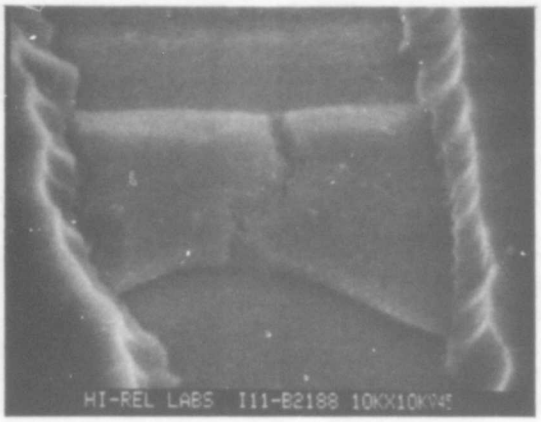
PULSE AMPLITUDE	11.2 VOLTS
LENGTH	200 ms
RISE TIME	14 μs
TIME-TO-PROGRAM	21 ms



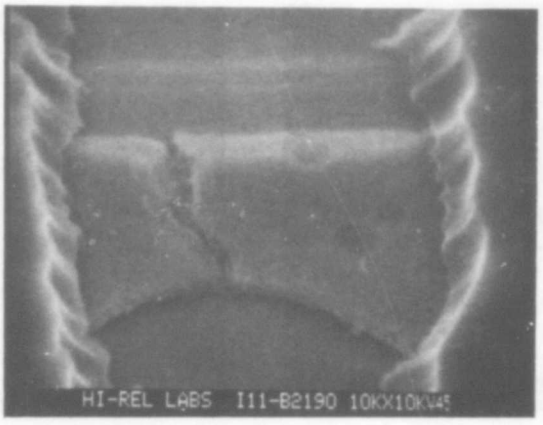
PULSE AMPLITUDE	11.2 VOLTS
LENGTH	200 ms
RISE TIME	14 μs
TIME-TO-PROGRAM	25 ms

l.

Figure 19. SEM photos of Vendor B nichrome fuse after plasma etch (sample 11) (sheet 6).



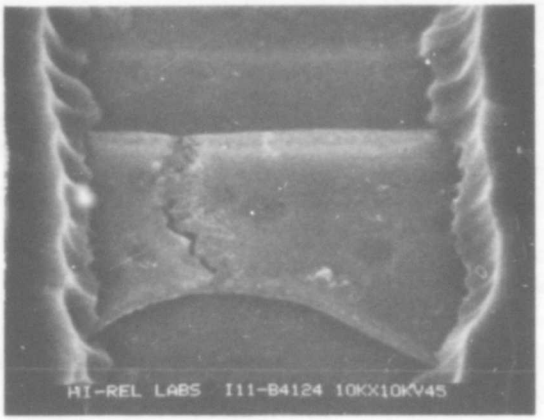
PULSE AMPLITUDE	12.0 VOLTS
LENGTH	200 ms
RISE TIME	15 μs
NUMBER OF PULSES TO PROGRAM	4 PULSES
TOTAL PROGRAMMING TIME	800 ms



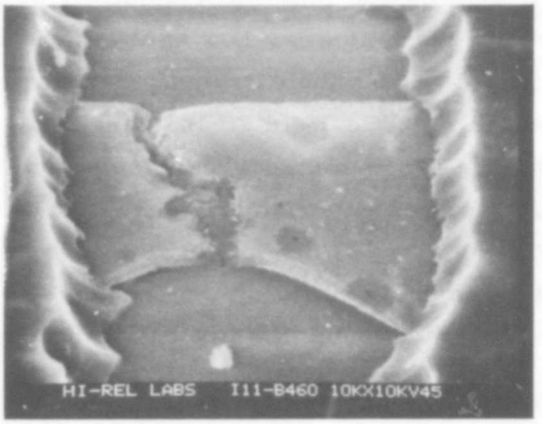
PULSE AMPLITUDE	11.0 VOLTS
LENGTH	200 ms
RISE TIME	15 μs
NUMBER OF PULSES TO PROGRAM	7 PULSES
TOTAL PROGRAMMING TIME	1370 ms

m.

Figure 19. SEM photos of Vendor B nichrome fuse after plasma etch (sample 11) (sheet 7).



PULSE AMPLITUDE	10.8 VOLTS
LENGTH	10 ms
RISE TIME	13 μs
NUMBER OF PULSES TO PROGRAM	17 PULSES
TOTAL PROGRAMMING TIME	170 ms



PULSE AMPLITUDE	10.8 VOLTS
LENGTH	10 ms
RISE TIME	13 μs
NUMBER OF PULSES TO PROGRAM	10 PULSES
TOTAL PROGRAMMING TIME	100 ms

n.

Figure 19. SEM photos of Vendor B nichrome fuse after plasma etch (sample 11) (sheet 8).

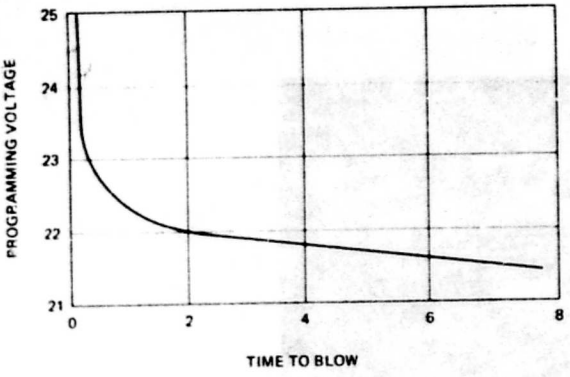


Figure 20. Relationship illustration of fusing time versus program pulse voltage (nichrome fuse element)

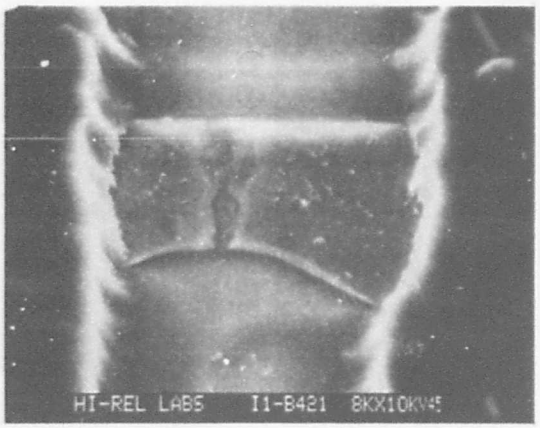
the fusing region. Fuses from the same vendor, programmed with the same pulse waveform, have similar physical appearances.

Some of the individual experiments performed and pertinent observations are discussed in the remainder of this section.

Individual Experiments

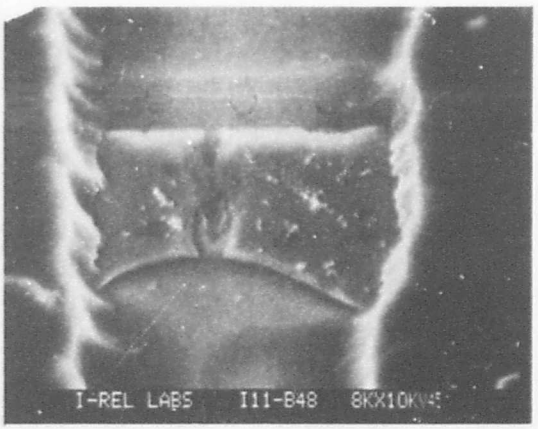
Extended Programming Pulse – It has been suggested that the remainder of the pulse voltage sustained across the fuse after the fuse has opened may modify the character of the fuse gap. During this time the programming voltage would be applied across the extremely narrow opened fuse gap and would create an intense electric-field stress condition. To evaluate this effect, some fuses were programmed with pulses terminated shortly after fusing and others with pulses extended for more than a hundred milliseconds. SEM analyses of Vendor A and B fuses revealed no physical difference as a result of sustained pulse voltage after fusing occurred. Similarities in Vendor B fuses programmed under the two conditions are shown in Figure 21.

Time-to-Program – A comparison was made of fuses programmed on a pulsewidth of microseconds to ones which programmed on a pulsewidth of over a hundred milliseconds. The variations in physical appearance of each vendor type as a result of the indicated programming time are shown in Figures 22a-e. In most cases where the striated pattern was observed in



PULSE AMPLITUDE	21 VOLTS
LENGTH	40 μs
RISE TIME	28 μs
TIME-TO-PROGRAM	35 μs

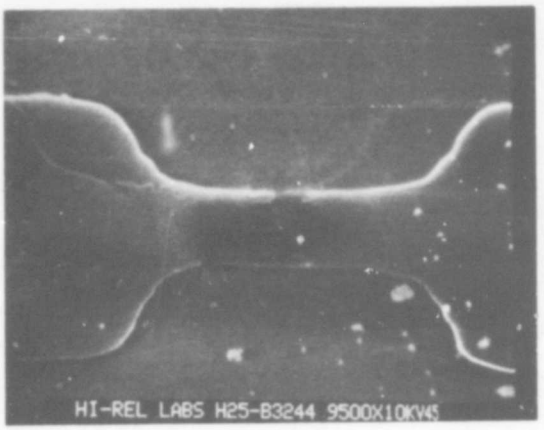
a.



PULSE AMPLITUDE	21 VOLTS
LENGTH	200 ms
RISE TIME	28μs
TIME-TO-PROGRAM	28μs

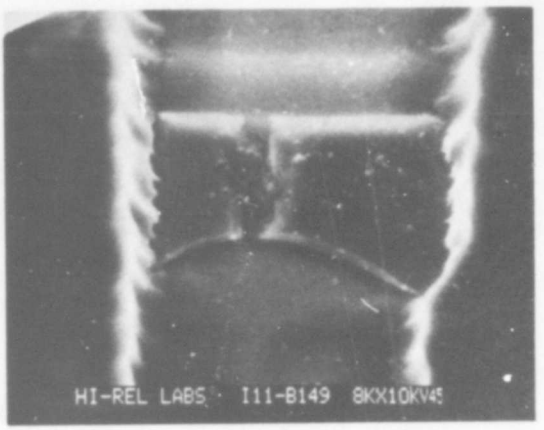
b.

Figure 21. Vendor B short and long afterpulse comparison before plasma etch.



VENDOR A

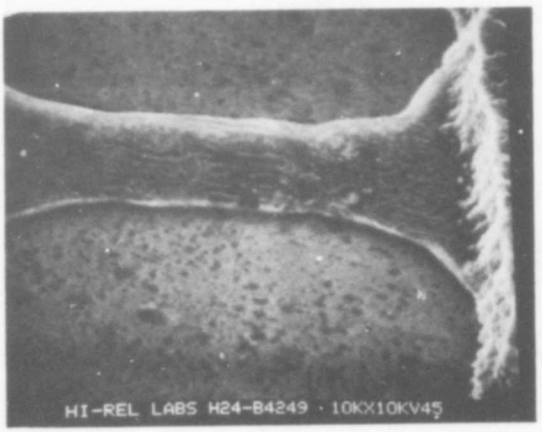
PULSE AMPLITUDE	25 VOLTS
LENGTH	12 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	5 μs



VENDOR B

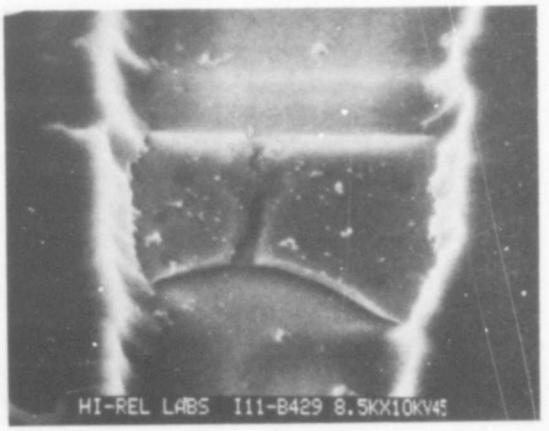
PULSE AMPLITUDe	26 VOLTS
LENGTH	10 ms
RISE TIME	2.5 μs
TIME-TO-PROGRAM	3 μs

a.



VENDOR A

PULSE AMPLITUDE	25 VOLTS
LENGTH	192 ms
RISE TIME	130 μs
TIME TO-PROGRAM	125 μs

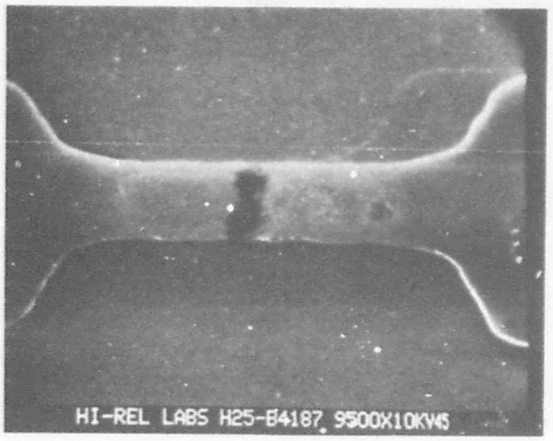


VENDOR B

PULSE AMPLITUDE	21 VOLTS
LENGTH	200 ms
RISE TIME	28 μs
TIME-TO-PROGRAM	30 μs

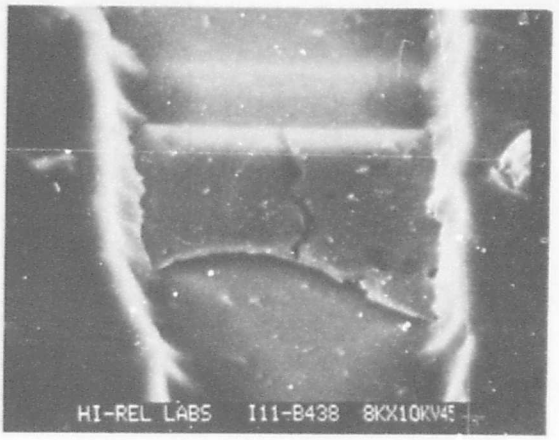
b.

Figure 22. Time-to-program comparison before plasma etch (sheet 1).



VENDOR A

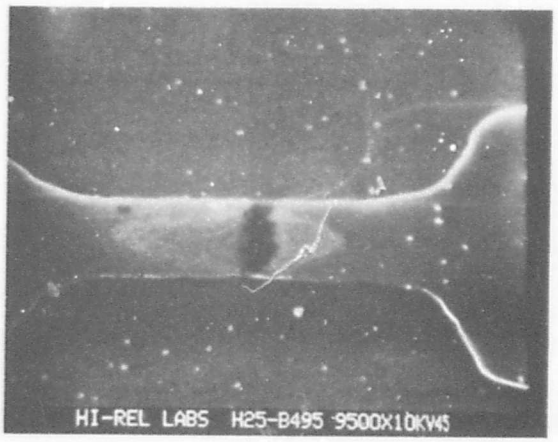
PULSE AMPLITUDE	22.5 VOLTS
LENGTH	192 ms
RISE TIME	125 μs
TIME-TO-PROGRAM	1 ms



VENDOR B

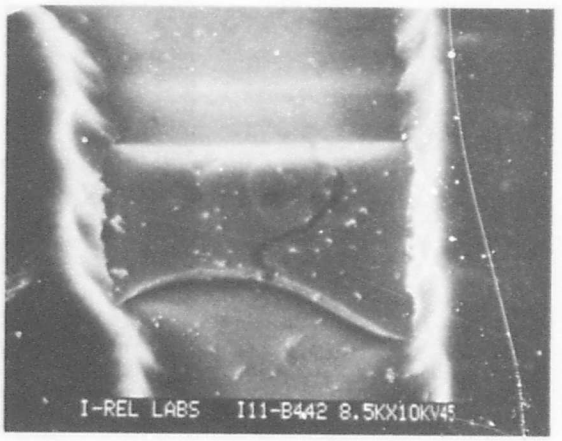
PULSE AMPLITUDE	12 VOLTS
LENGTH	200 ms
RISE TIME	15 μs
TIME-TO-PROGRAM	3.5 ms

c.



VENDOR A

PULSE AMPLITUDE	21.5 VOLTS
LENGTH	192 μs
RISE TIME	122 μs
TIME-TO-PROGRAM	11.2 ms

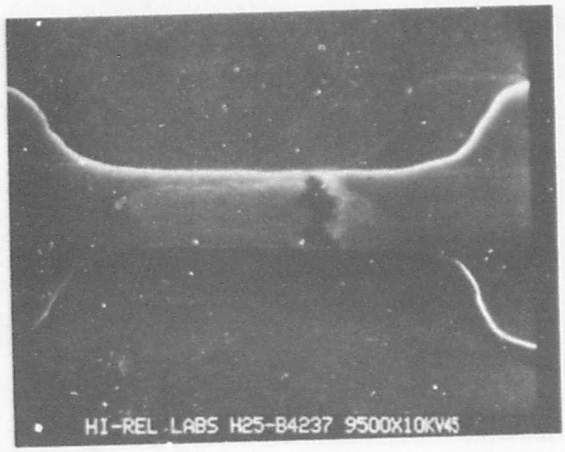


VENDOR B

PULSE AMPLITUDE	11.2 VOLTS
LENGTH	200 ms
RISE TIME	14 μs
TIME-TO-PROGRAM	25 ms

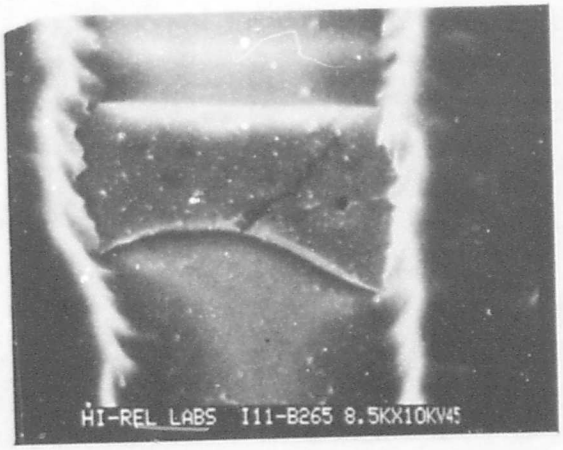
d.

Figure 22. Time-to-program comparison before plasma etch (sheet 2).



VENDOR A

PULSE AMPLITUDE	20.5 VOLTS
LENGTH	192 ms
RISE TIME	122 μs
TIME-TO-PROGRAM	100 ms



VENDOR B

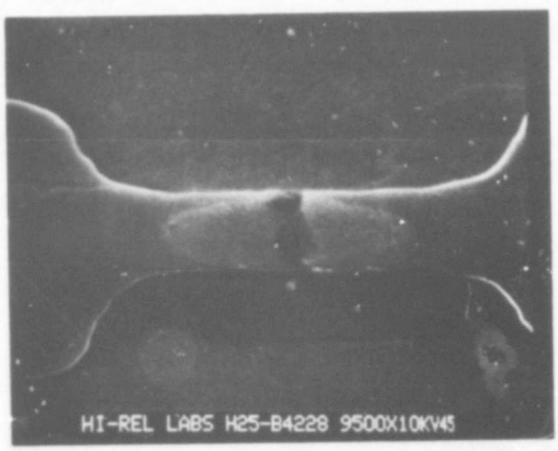
PULSE AMPLITUDE	12.3 VOLTS
LENGTH	200 ms
RISE TIME	14 μs
TIME-TO-PROGRAM	180 ms

e.

Figure 22. Time-to-program comparison before plasma etch (sheet 3).

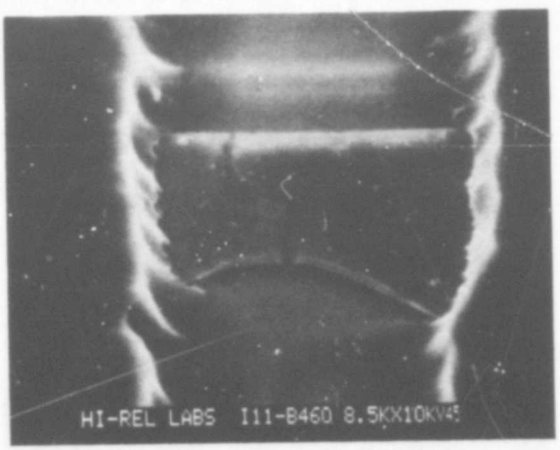
Vendor A, it could be associated with fuses programmed on faster programming times. Additionally, a larger area of the fuse material in both Vendor A and B was altered under faster programming. Also, apparent in the figures is the variation in physical appearance after programming between the two vendor types. These differences might be attributed to variations in the geometry, thickness and material composition of the nichrome metallization. A more detailed discussion on this subject is contained in Section 5.

Multiple Pulse – Several fuses were programmed using a series of pulses as opposed to fusing with a single pulse. Typical fuses which were observed by vendors A and B using multiple pulses are shown in Figure 23. When these fuses are compared with others that received a similar total energy programming time, little difference is seen between fuses opened by many short pulses and those opened with one long pulse, if the total energy time to programming is similar.



VENDOR A

PULSE AMPLITUDE	20.5 VOLTS
LENGTH	12 ms
RISE TIME	122 μs
NUMBER OF PULSES TO PROGRAM	9 PULSES
TOTAL PROGRAMMING TIME	108 ms



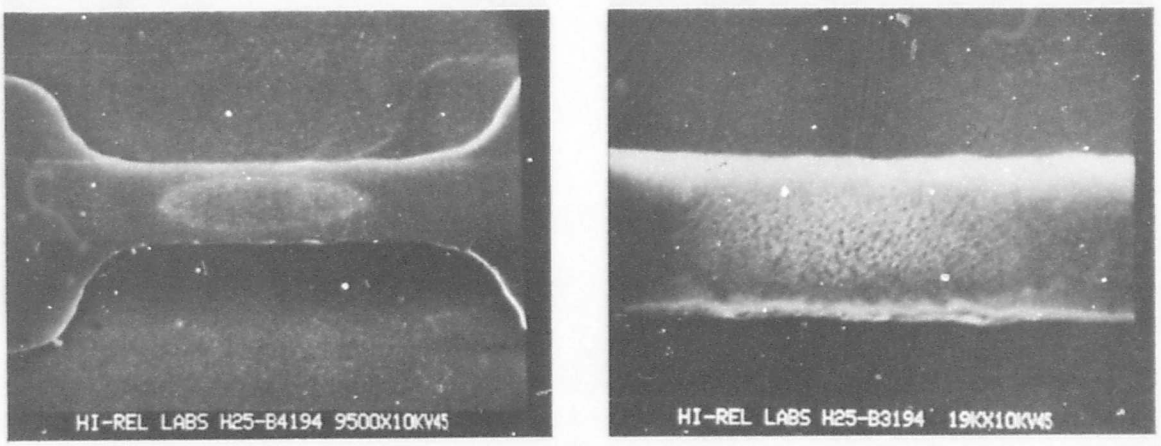
VENDOR B

PULSE AMPLITUDE	10.8 VOLTS
LENGTH	10 ms
RISE TIME	13 μs
NUMBER OF PULSES TO PROGRAM	10 PULSES
TOTAL PROGRAMMING TIME	100 ms

Figure 23. Multiple pulse programming before plasma etch.

Partial Fusing – In this experiment the programming pulse was cut off before actual fusing to observe the effect of partial programming on the fuse link. It was difficult to sense the current change to determine the start of fuse opening. A fixed pulse length was used instead of cutting off the pulse via current sensing. The physical appearance of the initial fusing reaction of a vendor A nichrome fuse before the opening of a fuse gap is shown in Figure 24. This elliptical reaction zone can be seen on fully programmed fuses. Resistance of the fuse shown in Figure 24 was measured to be 500 ohms after chemically etching away the passivation.

Effects of Process Variations – Several nichrome fuses on a device were programmed utilizing identical pulses to observe the repeatability of the physical appearance of each fuse. Although a similar physical gap appearance was seen on fuses in the same device, physical variations were observed in different devices from the same vendor. Fuses programmed with identical pulse waveforms had slight variations in physical gap appearance even though some fuses were in devices having lot date codes within 2 weeks of each other. This is not to say that no correlation was noted between programming



BEFORE PLASMA ETCH

AFTER PLASMA ETCH

VENDOR A

PULSE AMPLITUDE	20.8 VOLTS
LENGTH	12 ms
RISE TIME	122 μs

Figure 24. Partial programming.

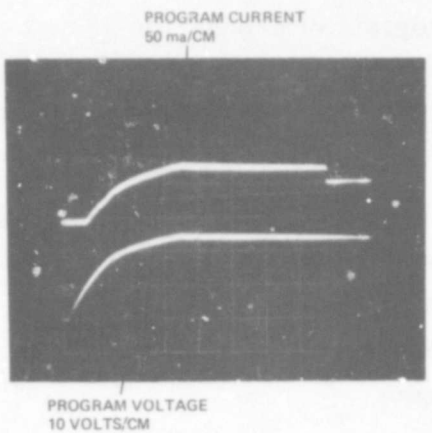
pulses and physical gap appearances, but rather that device to device variations in process controls cause additional variation in the physical characteristics of the fuse gap.

Test Fuse Programming Comparison – Sample devices used in the experiments were screened originally by the vendor who used test fuses on the chip. Two nichrome test fuses programmed by the vendor (Figures 16n, 17e, and 17f) appear very similar in appearance in fuses programmed by Hughes on the same device having a time-to-program of around 100 μs (Figures 15b and 15c).

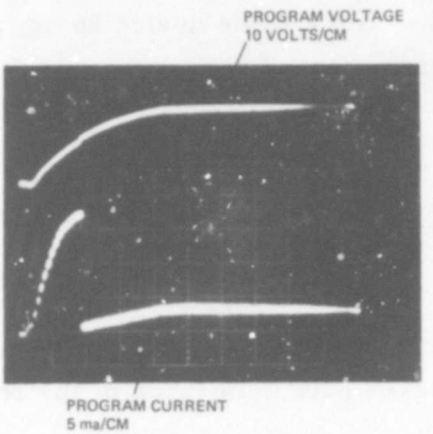
Pertinent Observations

Programming Time – Programming time was found to be relatively constant for fuses along a column; therefore, some experiments were arranged by columns on the chip. For a given programming voltage, the fusing time increased for columns furthest from the row select circuits because of the increased path impedance of the row diffusion runs.

Programming Current Waveforms – By observing the current waveform, the fusing event could be detected by a downward transition of the current as the fuse opened and its portion of the current ceased. Typical waveforms for Vendor A and B fuses are shown in Figure 25. The high residual current after fusing, in the Vendor A waveform, is caused by leakage down the program current switch base drive transistors. A fuse current of approximately 18 mA could be estimated from the height of the current transition from 70 to 52 mA. Fusing time decreases with higher currents. Anomalies were occasionally noted in the current waveform, particularly on difficult to program parts. An example is shown in Figure 26. The sharp upward transition might be attributed to a junction breakdown within the device. Such a breakdown could limit the voltage applied to the fuse, thus increasing the time required for programming or making it impossible to program. If the breakdown were of the V_{CER} variety, a reduction in fuse voltage after the breakdown would occur. In this case, a slowly rising program voltage would allow the fuse to reach a higher temperature before



a. Vendor A, Time: 50 μs/cm



b. Vendor B, Time: 20 μs/cm

Figure 25. Programming waveforms of nichrome PROM.

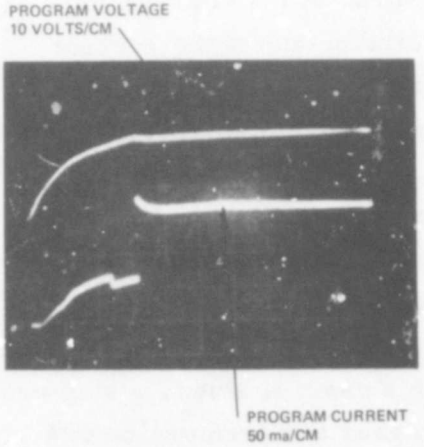


Figure 26. Programming current anomaly of nichrome PROM, Vendor A, Time: 50 μs/cm.

breakdown than would a rapidly rising pulse which reaches breakdown in less than the thermal time constant of the fuse-substrate system. This might explain the increased programming yield experienced with slower rise time program pulses. As an example, one difficult to program fuse was subjected to 60 fast rise pulses with no success. The current waveforms displayed the abnormal current transient. A subsequent single slow rise pulse of the same amplitude programmed the fuse.

Effect of Raising V_{cc} – Another type of anomaly was observed in which the slope of the current rise decreased at a certain level suggesting a transistor coming out of saturation. A part which refused to program and displayed this effect with a V_{cc} of 5 volts was successfully programmed after raising V_{cc} to 5.5 volts, thereby increasing the base drive.

Refusal to Program Devices – Cases of refusal to program, where the observed current waveform is normal in shape but low in amplitude, may be attributed to high programming path impedance.

Extra Bits – In another type of programming failure, extra bits were found to be programmed other than those intended. In many cases, the cause was an inoperative circuit or open bond wire for one of the address terms. As a result, two applied addresses differing by the power of two, corresponding to the faulty term, accessed the same memory elements. This was evidenced by a repetition of output data every 2^n addresses, n being the order of the faulty address. Other extra bit failures, more difficult to explain, may be caused by more subtle address circuit failure or to diversion of programming current to other addresses by junction breakdown in the current steering circuits.

Burn-In and "Grow Back" Experiments

In performing the fusing experiments described in the previous subsection, two devices from each of vendors A and B were prepared under as nearly identical fusing conditions as possible. One device from each vendor was subjected to an operational burn-in and monitored for any changes in stored data, and then subjected to SEM examination for comparison with the device that was

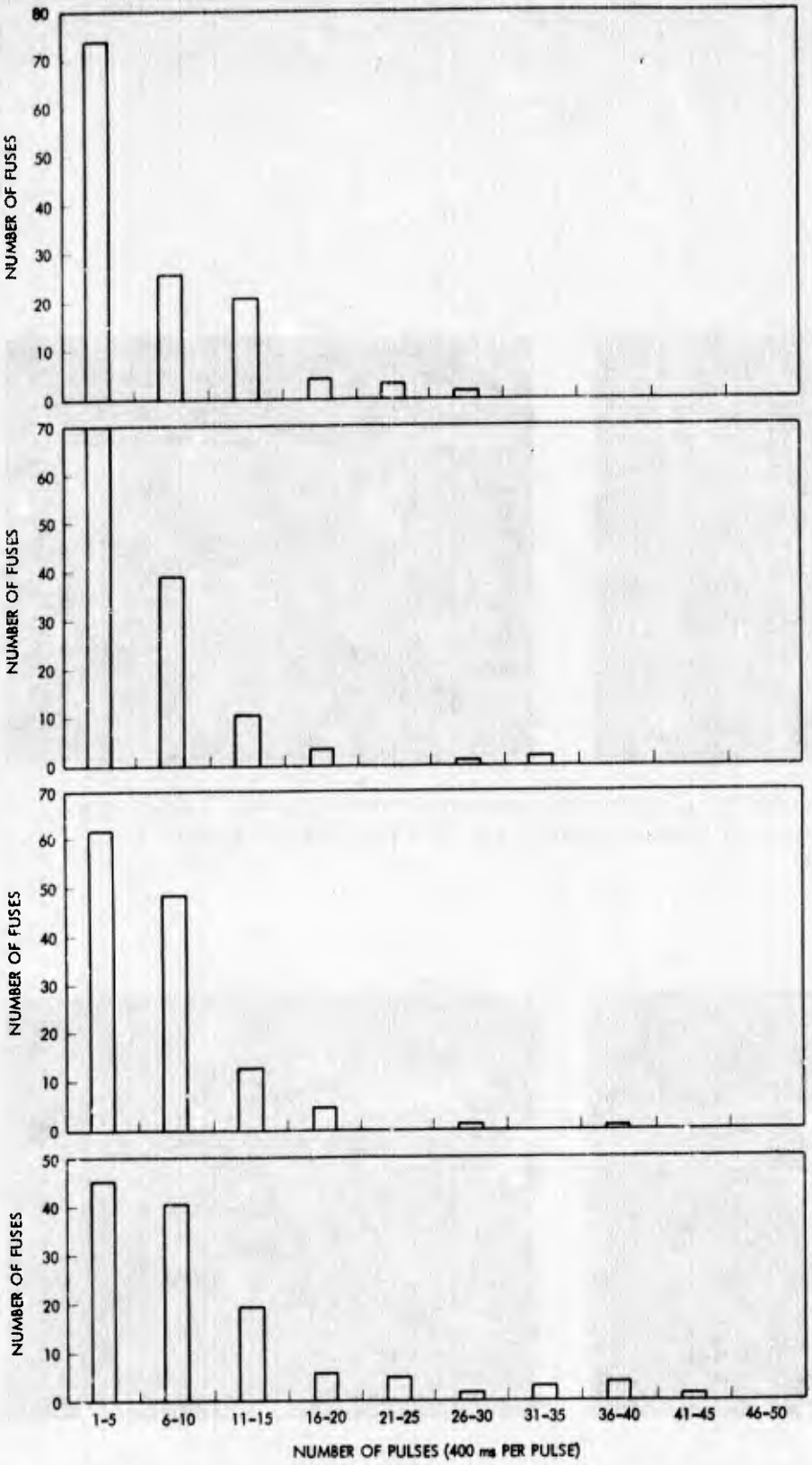
not burned-in. The objective was to detect susceptibility to reconduction due to any of the programming variations tried and also to observe changes such as whisker growth in the gap region caused by the burn-in.

The burn-in involved 410 hours of operation at 125°C ambient temperature, with the address inputs being cycled by an 8-bit counter at a 1 MHz rate. V_{cc} was set at 5.0 volts.

The data were checked periodically at room temperature with V_{cc} set alternately at 5.0 and 4.2 volts. No changes in the stored data were detected. It should be noted that the total sample size of burned-in fuses was 300, and the sample size for each experimental category was about a dozen so that only limited statistical inferences can be drawn from this result.

The samples then were subjected to SEM examination. Unfortunately, the Vendor B unburned-in sample was lost because it was not prepared correctly for SEM examination. For the Vendor A devices, the effect of burn-in of the fused gap can be evaluated by reviewing Figures 14 and 15 (burn-in) and Figures 16 and 17 (no burn-in) and by comparing fuses programmed under similar conditions. No obvious changes in physical appearance were found to be caused by burn-in.

A further experiment was conducted to correlate "slow to program" fuses to probability of reconduction. Here, 512 fuses on a Vendor A part were subjected to rectangular programming pulses of 400 ms at various reduced amplitudes such that one to 40 such pulses were required to open the fuses. The fuse population distribution relative to the number of pulses required for each bit – Columns are shown in Figure 27. After programming, the device was subjected to dynamic burn-in (125°C) conditions for a period of 840 hours. Two data changes due to fuse reconduction were observed, the first at 120 hours and the second at 648 hours. SEM photographs of these two fuses are shown in Figures 28 and 29. The first failure (H22B111) was originally programmed with six 400 ms pulses and the second (H22B4209) with 13 such pulses. Both fuses were programmed beyond the vendors' recommended programming schedule. However, the failure occurring beyond the conventional burn-in time of 168 hours leads to the conclusion that further studies of optimal burn-in criteria such as temperature,



NOTE: PROGRAMMING PULSE AMPLITUDES WERE VARIED TO OBTAIN VARIED NUMBER OF PULSES TO PROGRAM

Figure 27. Distribution of number of pulses to program for nichrome fuses.

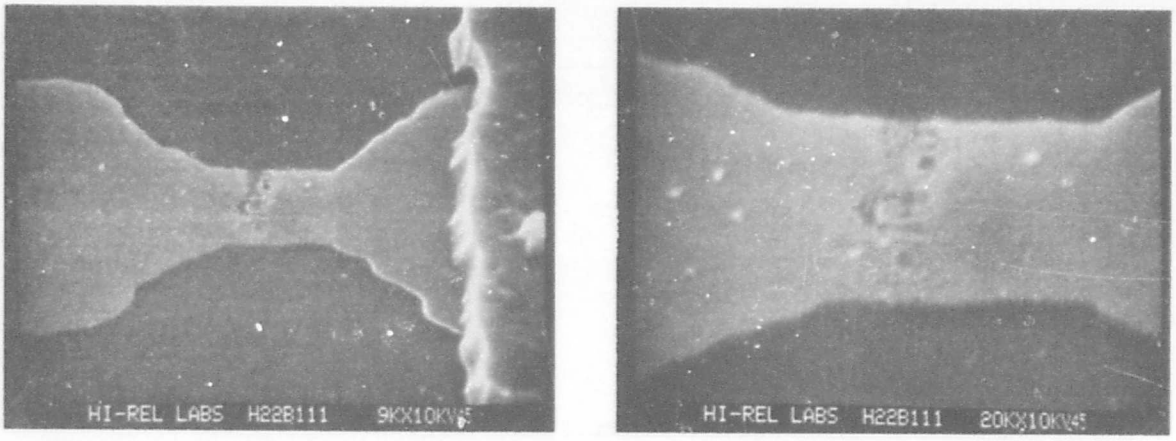


Figure 28. SEM photos of nichrome fuse reconducting after 120 hours of dynamic burn-in testing (chemical and plasma etched)

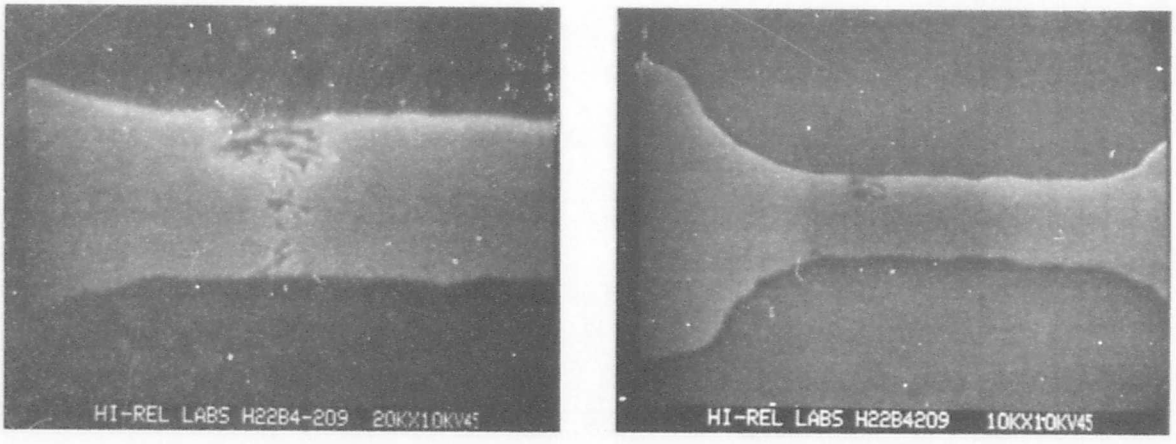


Figure 29. SEM photos of nichrome fuse reconducting after 648 hours of dynamic burn-in testing (chemical and plasma etched)

time duration, etc., are a necessity. Although this experiment was conducted on a part from one vendor, PROMs programmed under similar conditions would probably produce reconduction failures in other types of fusible link technologies. Future programming experiments should be conducted on a large sample of devices and technologies to develop a statistical population distribution of failures due to reconduction.

Programming Yield Experience

Reliable programming becomes an ever increasing problem as the size and complexity of PROMs continues to increase. The larger a PROM's capacity, the more chances exist for device defects and programming errors. PROMs consisting of 4096-bit capacities are now available from several vendors. With in-house programming, the user must become familiar with many complex programming procedures that vary, not only from one vendor to another but also from one PROM device type (512 bit) to another (1024 bit). In cases where quantities are high enough, the vendors may provide the programming, but usually programming is performed by the user or commercial services available through electronic component distributors. Utilizing the services of a distributor depends largely on the number of PROMs required, program simplicity, expense of programming equipment, and device reliability requirements. Distributors mainly program devices and are not involved in reliability screening requirements, both electrical and environmental. Therefore, distributors usually show a higher throughput in programming yield (sometimes 10 percent higher) than do most users concerned with screening out potential failure mechanisms during the programming cycle. For example, some fuses exhibited as slow to program may, after repeated pulses, eventually "blow." However, these fuses are considered unreliable and candidates for failures with reappearing bits once in operational use. Under conditions where cost objectives are primary and reliability objectives are secondary, distributor sources provide more appeal.

During this study, approximately 40 PROM users were contacted as sources for programming yield data. These sources utilized programming equipment ranging from small manually operated programming machines which addressed PROM memory addresses by adjusting thumbwheel switches and programming bits by depressing a pushbutton to fully automatic, universal programmers. Automated equipment has the capability of programming virtually any type of PROM and has options for accepting inputs from keyboard punched paper tape, mark sense cards or programmed PROMS. The programming equipment must be flexible enough to translate data inputs into the requirements for each PROM type, including information on programming one's or zero's plus the correct timing, voltages and currents. The programming equipment vendors solve this data problem with personality modules (program cards), one for each PROM type. These modules provide versatility, both in updating equipment to handle new PROMs and in amending programming procedures to meet vendors' changing requirements for old ones. With updating available, the life expectancy of universal programming equipment is probably greater than 5 years.

Most of the yield data, supplied by the many users contacted, contained a range of 88 to 93 percent experienced on 1024-bit PROMs. These data basically reflect a yield experienced after fallout of programming and access time failures and are based on a sample population of more than 50,000 1024-bit PROM devices (see Table 5). Yields could be expected to increase on some devices to as high as 98 percent at the end of 1975, as manufacturing processes, programming methods and manufacturing methods for enhancing reliability mature. A small population of yields achieved on distributor programmed devices is given in Table 5. Observations of distributor data indicate a wider range of yields is experienced between distributors than between users who program their own PROM devices.

Programming Recommendations

Suggestions directed at optimizing programming yields and reliability on fusible link devices are detailed below. If restrictions are placed on the programming pulse schedule (e. g., short pulsewidth and few number of

TABLE 5. PROGRAMMING YIELD DATA

User Data

		Part Population	Loss	Yield
1.	Vendor M (NiCr)	1,399	10.3	89.7
2.	Vendor N (Junction)	22,262	11.5	88.5
3.	Vendor O (Ti:W)	16,709	8.2	91.8
4.	Vendor P (NiCr)	12,133	12.0	88.0

Distributor Data

		Part Population	Loss	Yield
1.	Vendor N (Junction)	2,066	6.5	93.5
2.	Vendor P (NiCr)	3,007	1.1	98.9
3.	Vendor O (Ti:W)	50	8.0	92.0
4.	Vendor M (NiCr)	(No Information)		

Distributor Data

		Part Population	Loss	Yield
1.	Vendor P (NiCr)	1,202	9.2	91.8
2.	Vendor N (Junction)	763	10.3	89.7
3.	Vendor O (Ti:W)	(No Information)		
4.	Vendor M (NiCr)	(No Information)		

pulses) for minimizing "growback," the result will be a decreased programming yield as long as the circuit deficiencies previously discussed continue to occur. Decrease in programming yield impacts the cost to the user. The recommendations involve either a means of circumventing the circuit deficiencies, non-destructive screening techniques to cull out unreliable devices or diverting the difficult to program parts to less critical applications as these parts would tend to have "growbacks."

Control of chip temperature during programming is useful. Low temperatures will decrease the junction breakdown tendency; although higher temperatures may be more useful if low beta is the problem. Temperatures can be controlled by heat sinking or by reduced programming pulse duty cycle if low temperature is required.

A gradual increase in programming voltage would allow fusing of the link before the breakdown voltage is reached. This can be achieved either by the slow rise time approach recommended by Vendor A or by a succession of rectangular pulses of increasing amplitude. The latter method has the advantage of allowing the pulse train to be stopped when fusing is detected. Then "extra bit" failures would be reduced if they are breakdown induced. In either case, the rate of increase in programming voltage must be rapid enough to prevent "slow ramp" pulse conditions, which have been shown to produce reconduction fuse failures.

Changing the order in which the fuses are programmed may be useful. If appreciable leakage of programming current occurs through unprogrammed bits, it is profitable to program the most difficult bits at the end when many of the leakage paths have been opened by programming. The difficult bits are generally those furthest from the row select circuits where the row run impedance comes into play. The simplest technique is to program all of bit 4, then 3-2-1 in that order. A better method would be to program by columns moving away from the row select circuits. It should be remembered that the geographical position of the fuses may bear a strange relationship to the address order so that a position map on the chip is necessary. However, the difficult to program bits may be due to a weak address switch and so unpredictable in position. In this case, if more than one program pulse is permissible, it may help to make a single pulse pass over the entire matrix to catch as many fuses as possible before returning to the first address for the second pulse.

Another approach is to make non-destructive tests on the device to detect weak programming circuits. Weak devices could be delegated to non-critical applications. One method is to apply programming voltage while addressing open fuses on the test row and column, checking for abnormally

high currents which imply junction breakdowns are occurring. The test voltage must be higher than the specified program voltage to take into account the increased chip temperatures encountered in actual programming. Higher temperature may reduce the breakdown threshold. A second method is to apply a fast rise time programming pulse to each fuse in the test row and column while measuring the peak programming current before fusing. Several microseconds are available because of the thermal time constant of the fuse. Abnormally high currents imply junction breakdowns; abnormally low currents imply low beta or high path impedance problems.

All of these methods require further investigation and should be regarded as suggestions.

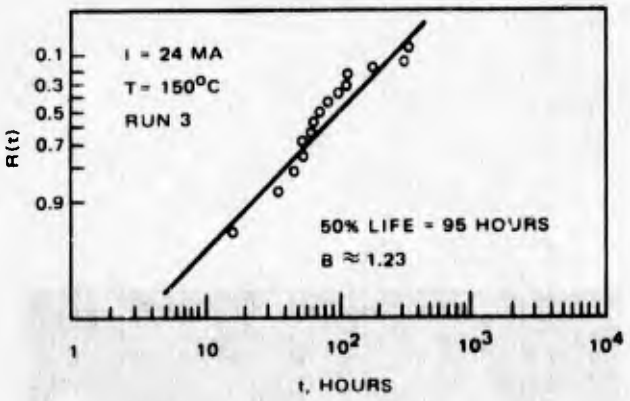
5. RELIABILITY PHYSICS OF MEMORY ELEMENTS

This section contains a detailed discussion of nichrome fusible links; the information is based on PROMs obtained from two suppliers. Included are programmed opening of nichrome fuse links, the basic characteristics of the programming mechanisms and how they are affected by variations in programming pulses (time-to-blow). Also included is a detailed discussion of fuse programming mechanisms in which sublimation, oxidation, melting, diffusion, and electromigration, are described. Opening of unprogrammed nichrome fuse links due to electrocorrosion is also covered in addition to fuse reconduction or grow-back. The discussion of the characteristics of titanium-tungsten PROMs includes the theory of programmed fuses, opening unprogrammed Ti:W fuses, and TI:W fuse reconduction or grow-back. The section concludes with a description of the characteristics of the avalanche-induced migration (AIM) blown diode PROM technology.

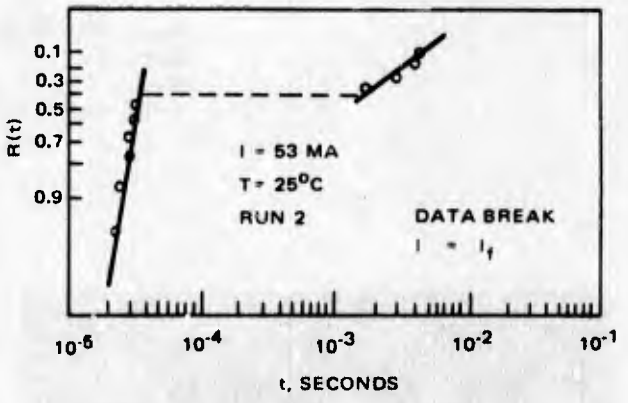
Nichrome Fusible Link PROMs

Programmed Opening of Nichrome Fusible Link PROMs – Variations in programming techniques, nichrome film composition and fuse geometry all affect opened fuse gap formation phenomena. The term "gap" as used here refers to the fusing reaction zone as observed under SEM analysis after chemical and plasma etching. The appearance of fuse gaps are quite dependent on the programming pulse that controls time-to-blow of the fuse link. An attempt to correlate the appearance of fuse gaps with times-to-blow leads to speculation that several different fuse opening mechanisms are involved with each type of gap formation and that certain mechanisms dominate a particular gap type. Dr. Roger Mo in his early PROM fuse investigation observed a definite break in the data on the cumulative distribution curve of time to fuse open, when the fusing current was near the

melting point. This break is shown in Figure 30*. This reinforces the postulate of the existance of many mechanisms for fuse opening. Dividing fuse link gaps into basic categories, i.e., short, intermediate and long time-to-blow gaps, serves to group those mechanisms that contribute to the formation of each gap type. The following subsections contain postulates of fuse opening mechanisms. However, agreement as to the mechanisms responsible for fuse link gap formation must await additional investigative data-gathering and supportive research, test and evaluation efforts. Gradual improvement in fuse materials, geometry, programming techniques and address and read circuitry will modify basic programming mechanisms.



a. For relatively low stresses, where fuse temperature does not reach melting point, failure times follow Weibull distribution

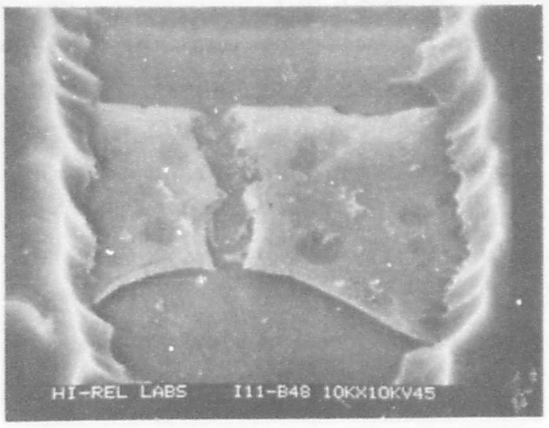


b. A high current stress, data break observed which indicates different failure mechanisms--energy calculations show fuses melt above this break point

Figure 30. Weibull plots

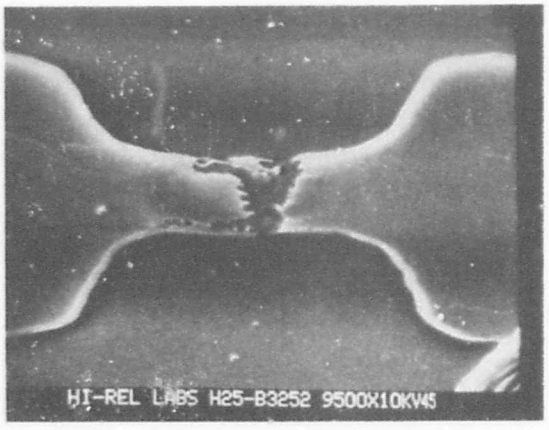
Short Time-to-Blow Fuse Link Gaps — A review of Figure 31 indicates that these fuse openings appear quite clean and relatively free of debris in the gap area after chemical and plasma etching. The time-to-blow period generally is in the low microsecond range up to about 100 μs; during this

*This figure is taken from R.S. Mo and D.M. Gilbert, "Reliability of NiCr Fusible Link Used in PROMs," Journal of the Electromechanical Society on Solid-State Science and Technology, July 1973.

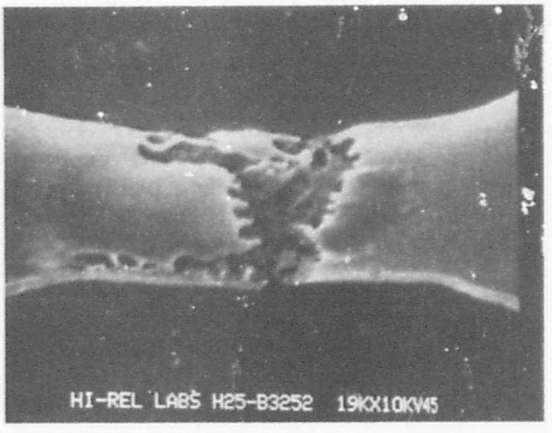


PULSE AMPLITUDE	21 VOLTS
LENGTH	200 ms
RISE TIME	28 μs
TIME-TO-PROGRAM	28 μs

a.



PULSE AMPLITUDE	25 VOLTS
LENGTH	12 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	5 μs



PULSE AMPLITUDE	25 VOLTS
LENGTH	12 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM (ADDITIONAL PHOTOGRAPH)	5 μs

b.

Figure 31. SEM photos of nichrome fuse with large gap (chemical and plasma etched)

time energy is pumped into the fuse neck region over an extremely short interval. Relative temperature as a function of the length of the fuse based on calculations by one PROM supplier is shown in Figure 32. The extremely rapid heating involved results in melting as well as rapid expulsion of the fuse neck material into the surrounding SiO_2 matrix; this rapid expulsion can be characterized as sublimation and diffusion of the nichrome in the neck region, in which the chrome molecules undergo rapid oxidation through combination with available oxygen in the SiO_2 matrix, while the nickel is diffused into the SiO_2 at a rapid rate due to its high energy content. The extremely rapid heating of the neck region, including transfer of energy from the chrome and nickel molecules to the glass matrix, results in the glass surrounding the neck region becoming plastic or molten. Completion of the short programming pulse or pulse train permits the glass to cool; during cooling it is forced into the evacuated gap region by the compressive stress of the overglass structure. The short time-to-blow fuse gap provides the most reliable

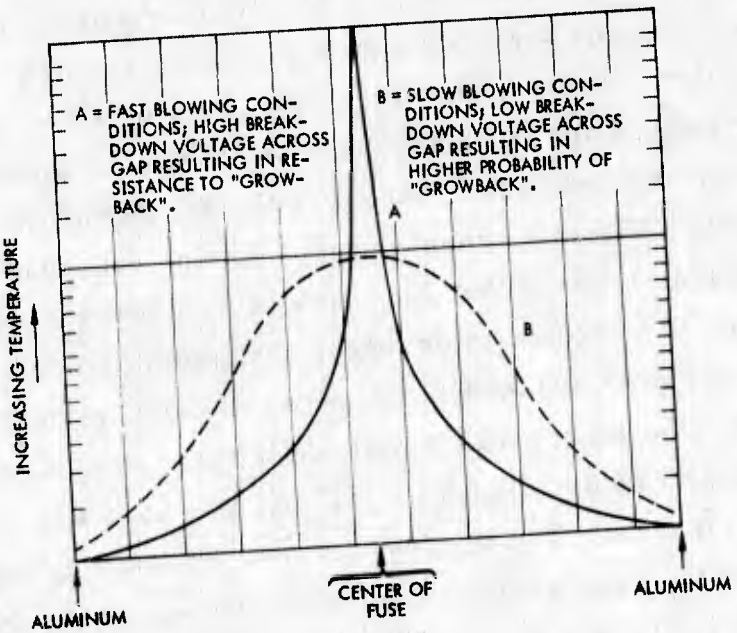
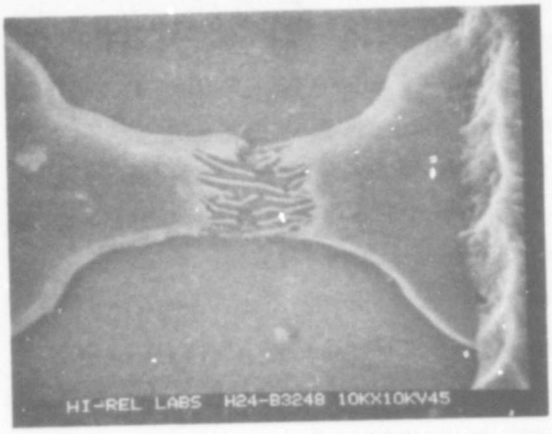


Figure 32. Calculated temperatures along length of particular nichrone fuse configuration

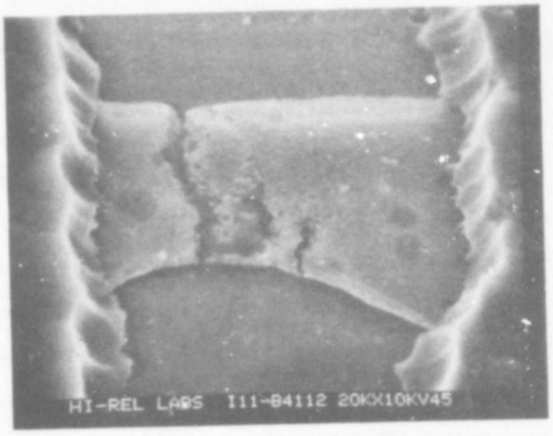
configuration for programmed fuse links; as little conducting debris or other metallization is left in the gap region to facilitate grow-back. For one of the fuse types, filaments or fingers may form but a void region suggesting a break tends to form near the center of the fuse. Rapid heating of the fuse neck region also results in relatively complete oxidation of the chrome material covering each fuse link end.

Intermediate Time-To-Blow Fuse Link Gaps – As can be seen from Figures 33 and 34, the physical appearance of these fuse gaps is quite different than those shown in Figure 31. Fuses in this category have been programmed over a time-to-blow interval of approximately 100 μs to 10 ms. For one fuse type, the fuse gaps shown after plasma etching are very wide and are noticeably different because of the many filaments or fingers that project from each fuse end, toward the center of the gap area (Figure 34). Rapid heating of the fuse neck area probably has caused complete oxidation of available chrome molecules and has left aggregates of nickel in the gap region. Electron and charged particle flow during the programming pulse aids in the formation of the molten nickel into larger filaments or fingers, which are aligned along the direction of flow. The filaments from each end of the gap probably interconnect with each other during the initial phase of the programming pulse; however, the extremely high resistance of each strand or bridge results in its rapid breakdown due to instantaneous heating of the filament structures while the current is flowing across the gap through the extremely small filament cross-sections linking both fuse ends. The matrix material separating the nickel filaments is probably a combination of SiO_2/Cr_2O_3. The chrome oxide mixes with the molten glass in the immediate area of the fuse neck and aids in the separation of filaments projecting from each gap end. Not all the nickel molecules will end up as filaments; some of this material will be expelled from the fuse gap area and forcibly diffuse into the glass matrix. The high resistance or insulating matrix between filaments may be considered as a form of cermet. Although the filament



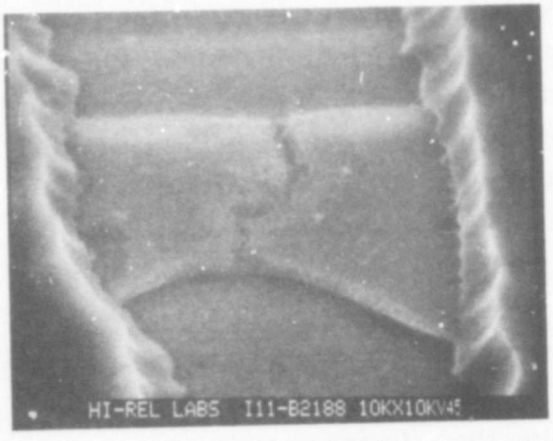
PULSE AMPLITUDE	25 VOLTS
LENGTH	12 ms
RISE TIME	130 μs
TIME-TO-PROGRAM	128 μs

Figure 33. SEM photo of nichrome fuse with filaments/fingers (chemical and plasma etched)



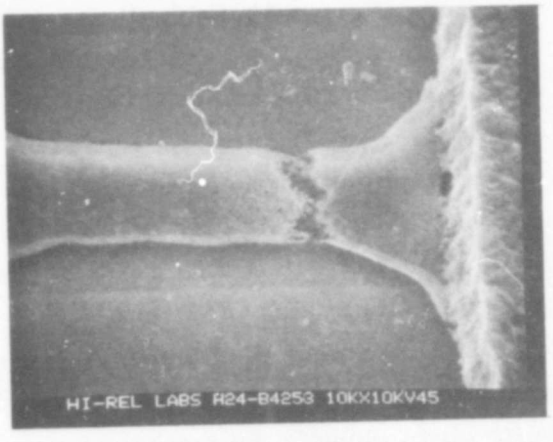
PULSE AMPLITUDE	12.5 VOLTS
LENGTH	200 ms
RISE TIME	15 μs
TIME-TO-PROGRAM	360 μs

Figure 34. SEM photo of nichrome fuse with multiple cracks and spongy formation (chemical and plasma etched)



PULSE AMPLITUDE	11.0 VOLTS
LENGTH	200 ms
RISE TIME	15 μs
NUMBER OF PULSES TO PROGRAM	7 PULSES
TOTAL PROGRAMMING TIME	1370 ms

a.



PULSE AMPLITUDE	20 VOLTS
LENGTH	192 ms
RISE TIME	125 μs
TIME-TO-PROGRAM	100 ms

b.

Figure 35. SEM photos of nichrome fuse with narrow gap (chemical and plasma etched)

structures appear to resemble metal whiskers or dendrites, they cannot be classified as either type of structure, as they are formed in an entirely different manner and show rounded ends rather than crystalline ends.

Not all nichrome-fused PROM types provide such clear-cut evidence of filament structure formation. The gaps of another fuse type show little, if any, filament structures, when programmed in the same manner (Figure 34). There are spongy formations at the ends of the gap. Some of these fuses showed double gap or multiple crack structures. The lack of a significant filament structure may be attributed to a predominance of nickel in the nichrome film which prevents separation and alignment of the molten nickel into filaments after oxidation of the chrome. It can be presumed that sufficient molten nickel in the gap area will create a stub or relatively uniform fuse end structure, rather than the filaments seen in the other fuse link gaps. Even with extremely accurate and calibrated thin film deposition monitors which can provide real-time indication of film thickness and resistivity during deposition, some changes in the composition of the nichrome can occur. These changes, which may be due to evaporation rate, vacuum system background (residual) gases, variations in substrate deposition temperature, etc., can affect the composition of the nichrome film. These differences in film composition will affect the formation of fuse gaps subjected to the same programming procedure, even though these devices are from the same supplier, but are not fabricated in the same PROM manufacturing run. Because each supplier tends to develop his own nichrome fuse composition, the problem of categorizing PROM fuse gaps based on time-to-blow programming is complicated further.

Calibration of filament or finger diameter from SEM photographs indicates that these structures are approximately 100 to 200 Å in diameter. It has been difficult to identify the materials comprising these fingers because the sample programmed fuse surface must be exposed to permit surface analysis methods to be used in quanitatively identifying the composition of the fingers. Initially, the sample fuse must undergo chemical and plasma etching, primarily to remove the 10,000 Å of overglass material that covers the surface of the

semiconductor device. In general, the plasma is comprised of ions which principally attack dielectric materials such as SiO_2 and chrome oxide. By means of SEM voltage contrast analysis the fingers have been shown to be conductive. If it can be assumed that sufficient free oxygen is present in the surrounding glass matrix to permit oxidation of the chromium during programming pulse occurrence, then the filaments or fingers seen in the gap must consist of relatively pure nickel.

The following approach may be used to examine the composition of the filaments seen in the fuse gap. With this approach, first the overglass must be removed and then examined with secondary ion mass spectrometry (SIMS). While the material in the blown gap is being gradually removed, SIMS is used to raster-scan over the fuse gap area containing the fuse gap filaments. As the spatial resolution of the SIMS is determined by the diameter of the incident ion beam, the 1 micron beam can be used to obtain information on an area containing the filaments. Since the sensitivity of the SIMS is very high, trace materials with concentrations as low as a few parts per billion can be detected. Many intermediate time-to-blow fuse gaps show a high concentration of filaments; these gaps can be eroded slowly or sputtered away and an analysis made of the filament material. In particular, a determination can be made as to the percentage of nickel and chromium that can be found in these filaments. As mentioned previously, most of the SiO_2 and chrome oxides should have been removed by the chemical and plasma etching processes used in preparation of the programmed fuse samples.

Long Time-To-Blow Fuse Link Gaps – As indicated in Figure 35, these fuses have gaps which are considerably narrower and more jagged in appearance than short time-to-blow fuse gaps, which they somewhat resemble. Fuse gaps which have been programmed over a time-to-blow interval of higher than about 10 ms have this jagged appearance. Additionally, gaps of one fuse type form angles up to 45 degrees to the fuse length axis. Most of these jagged gaps do not occur at or across the fuse neck but seem to be displaced from the neck region by some relatively significant distance. It is theorized that as energy is pumped into the neck region over a 10-100 ms

interval, the relatively slow heating results in oxidation of the chromium combined with electromigration of the nickel along grain boundries, which is evidenced by the irregular gap configurations. Nichrome grain boundaries form during film nucleation in the nichrome deposition process. In most instances, those grain boundaries facilitating electromigration of nickel during the long time-to-blow pulse would not necessarily occur or pass through the middle of a fuse neck region. This fact could account for most of the gap formation that occurs some distance from the middle of the neck area. In any event melting occurs at least during the last portion of gap formation. As oxidation and electromigration remove material from the forming gap area, the remaining strands or bridges connecting the fuse ends will provide extremely high resistance paths to the pulse current. These last connecting strands or bridging areas probably undergo melting of the remaining nickel, with almost immediate diffusion into the surrounding SiO_2 and chrome oxide matrix. Melting can be assumed as one of the long time-to-blow mechanisms, as ragged sections with substantial amounts of missing fuse material can be seen when examining this programmed fuse link type. It is quite likely that the last remaining conductive links occupied these areas. The resultant insulating matrix in the gap may be considered as a form of cermet.

Summary of Nichrome fuse gap characteristics – The nichrome fuse gap characteristics are summarized in Table 6.

Nichrome Fuse Link Programming Mechanisms – In the preceding subsections several key mechanisms associated with the programming of nichrome fuse links were mentioned including (1) sublimation, (2) oxidation, (3) melting, (4) diffusion, and (5) electromigration. Each of these mechanisms is further discussed in some detail in this subsection.

Sublimation – Sublimation may be considered as a process in which certain materials pass from the solid state directly into the gaseous or vapor state, without evidencing a liquid phase between the solid and vapor states. Refractory metals usually sublime when heated in a vacuum. Chromium

TABLE 6. NICHROME FUSE GAP CHARACTERISTICS

Type of Fuse link gaps	Reference Figure	Comments
Short time-to-blow	Figure 31	• Time-to-blow less than 100 μs • Relatively large, clean gap • Gap separation at fuse neck forms a relatively clean line; and for one fuse type formation of some filaments/fingers • Mechanisms include: sublimation, oxidation, diffusion, melting • Little debris seen in gap because SiO_2 deforms into vacancy as a result of compressive stress
Intermediate time-to-blow	Figures 33 and 34	• Time-to-blow between 100 μs and 10 ms • Very large gap with distinct filament/finger formation for one fuse type and relatively narrow gap, double gap or multiple cracks with spongy formation for the other fuse type • Mechanisms include: melting, oxidation, diffusion • Filaments occupy gap region with SiO_2/Cr_2O_3 cermet matrix, which separate fingers
Long time-to-blow	Figure 35	• Time-to-blow greater than 10 ms • Narrow ragged gap - probably along film grain boundaries • Most of the gaps of one fuse type are off center to the electrically positive end of the fuse • One fuse type has gaps form at an angle up to 45 degrees to fuse neck axis, rather than straight across • Mechanisms include: oxidation modified by rapid electromigration along grain boundaries, to form irregular gap configurations; and melting occurs during last portion of gap formation. • A form of cermet occupies the gap region

also demonstrates this phenomenon when it is evaporated in a vacuum from the pure state. The rapid expulsion of fuse link material from the neck region can be characterized as sublimation; the extremely rapid heating of the nichrome material in the fuse neck imparts enough energy to both the chromium and nickel molecules to cause a part or all of them to pass from the solid (film) state directly into a vaporized state, with instantaneous diffusion and penetration of the surrounding SiO_2 matrix material. The high instantaneous heating of the fuse neck area and its surrounding glass matrix probably causes immediate softening of the glass which further facilitates diffusion/penetration of the nickel and unoxidized chromium molecules into the matrix material.

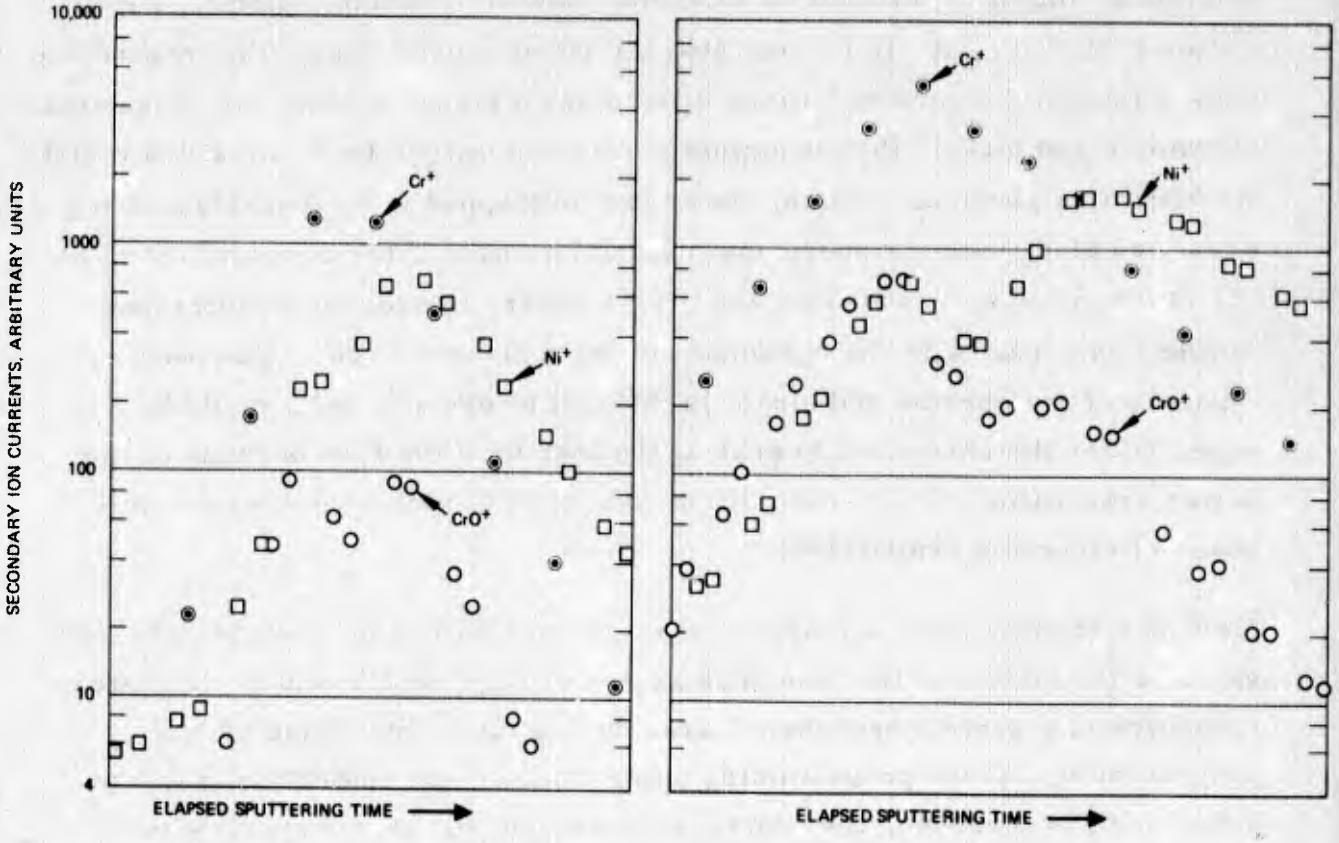
Oxidation – Dr. Roger Mo* has done considerable work in examining the composition of nichrome fuse links via SIMS. This technique bombards the sample material surface with a beam of ions, and a fraction of the molecules sputter off leaving the surface as ions; these ions are collected and mass analyzed. Some of the measurements on specially fabricated fuses are given in Figure 36.** During the measurement process, material was being sputter removed; hence, the measurements made with respect to a particular sputter time would be related to the material found at a particular depth. An unprogrammed fuse is shown in Figure 36a; it is shown that the chromium concentration peaks near the surface, while the nickel peaks near the bottom. It should be noted that the chrome oxide forms a double peak which can be interpreted as oxidation of the chromium at the top and bottom interfaces, between the fuse and its overglass, or between the fuse and the thermally-grown oxide upon which the nichrome was deposited. Note that the resolution of the SIMS is approximately 1 micron, while the fuse width is approximately 5 microns and the gap is about 1/2 micron; this complicates detailed analysis of the fuse surface and structure. The depth resolution of the SIMS is also affected by the shape of the sputtered crater. Hence, exact values and fuse

*R. S. Mo, private communication.
**ibid.

boundaries might be difficult to determine due to 'smearing effect'. From Figures 36b and c, it can be seen that the chrome oxide content increased and peaked toward the surface. Since silicon has a higher affinity for oxygen than chromium and nickel, the chromium cannot rob oxygen from the silica matrix. As noted in a previous section, water can be trapped in the overglass if it is deposited along with the overglass material as part of the conventional chemical vapor (Silox or Vapox) process. This water, in addition to entrapped oxygen, can react with the chromium to form chrome oxide. The peaking tendency of the chrome and nickel is difficult to explain, as it would be expected for the chromium to peak at the bottom of the fuse because of the faster evaporation of chromium when compared to nickel, during the initial phase of nichrome evaporation.

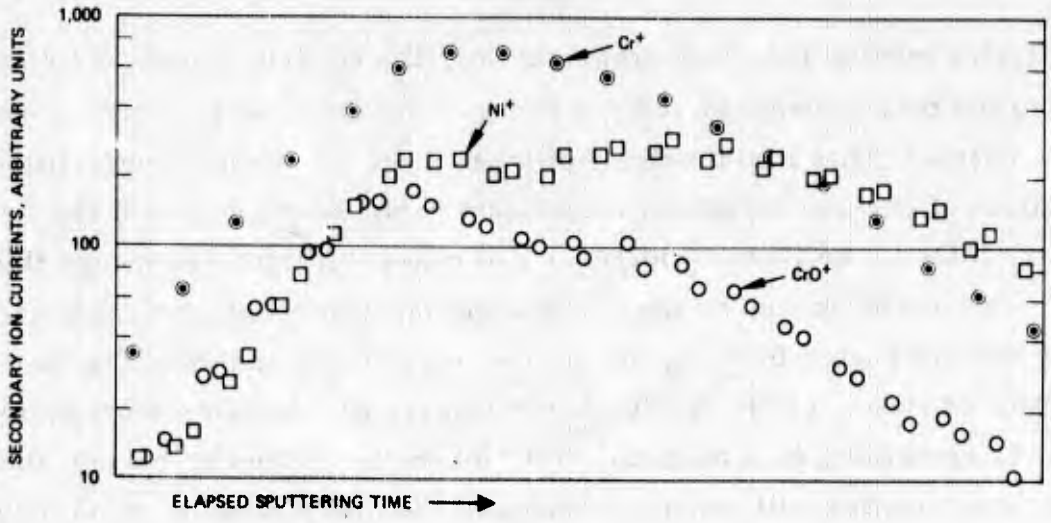
Melting – Melting plays a major role in intermediate time-to-blow fuse link gaps. Examination of the fuse neck region of Figures 37a and b, indicates formation of a central egg-shaped area during the initial phase of fuse programming. If the programming pulse train is terminated just short of actual melt occurrence, the central neck region will be brought to a temperature where the nichrome becomes plastic and is probably hot enough to permit oxidation of the chromium; this assumption is based on the appearance of the egg-shaped area, which resembles the flake-like thin crust-like oxide film.

During normal fuse link programming, the current causes the central area of the fuse to undergo rapid melting, which also affects the surrounding glass matrix. This rapid melting process at high temperature facilitates formation of chrome oxide and subsequent rapid intermixture of the Cr_2O_3 with the SiO_2. The flow of electrons and charged particles through this neck region is intense enough to shape the aggregates of nickel molecules remaining in the gap region into fingers or filaments which line up along the direction of flow. These neatly shaped fingers or filaments must be formed when the remaining fuse material is either in the melted or plastic state. More rapid heating will cause expulsion of the nickel and the remaining chromium at such a rate that it diffuses into the SiO_2 matrix; slower heating,



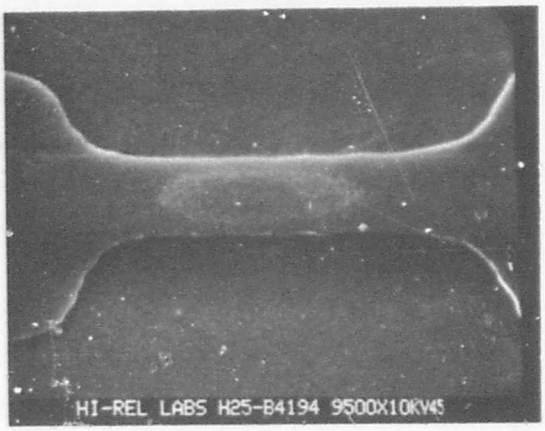
a. Unblown NiCr fuse links

b. Slow-blown NiCr fuse links



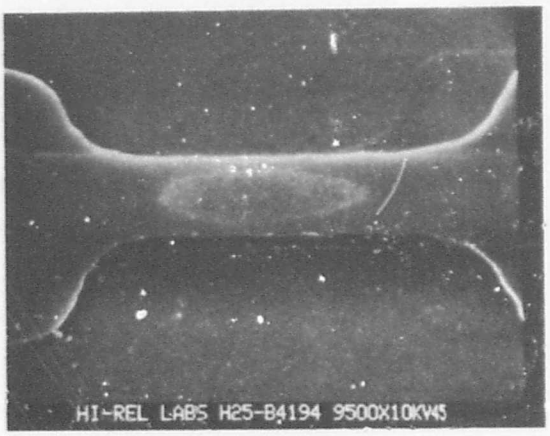
c. Fast-blown NiCr fuse links

Figure 36. Depth profiles



PULSE AMPLITUDE 20.8 VOLTS
LENGTH 12 ms
RISE TIME 120 μs
EXPERIENCE PARTIAL PROGRAMMING PULSE

a. Chemically etched



PULSE AMPLITUDE 20.8 VOLTS
LENGTH 12 ms
RISE TIME 120 μs
EXPERIENCED PARTIAL PROGRAMMING PULSE

b. Chemical and plasma etched

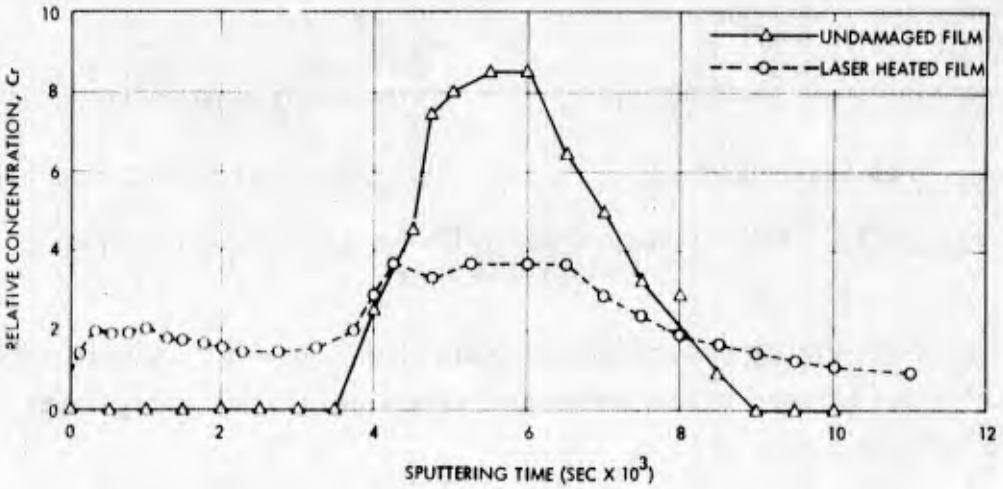
Figure 37. SEM photos of partially programmed (not opened) Nichrome fuse.

caused by lower energy programming pulses, will permit the fuse neck material to be removed by oxidation and electromigration along metal film grain boundaries.

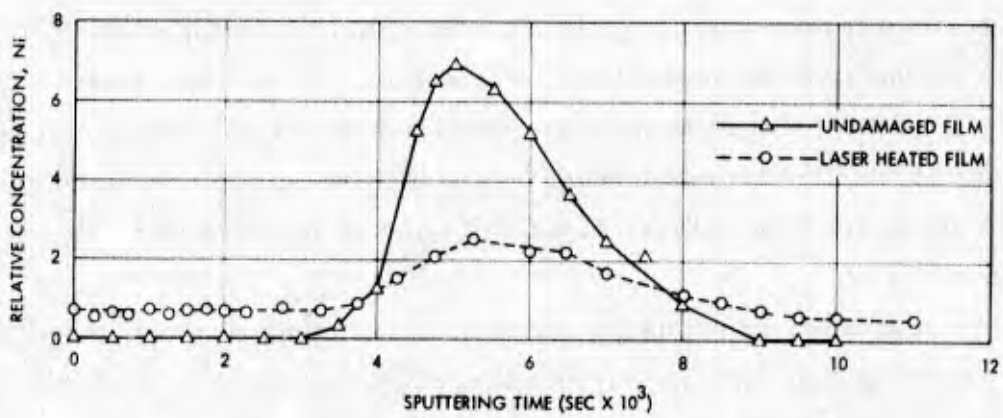
Diffusion – When two materials are brought into intimate contact and then raised to a high temperature, the rate of diffusion or molecular interchange at the interface increases. In general, the higher the temperature, the more rapid the exchange of molecules at the interface. In PROM devices, the nichrome fuse material is in intimate contact with the thermally-grown SiO_2 below and the vapor-deposited overglass structure on top. When the fuse is heated by programming pulses, rapid diffusion in the fuse neck region is expected to occur.

In an experiment conducted 2 years ago at Hughes to determine diffusion of nichrome material into the surrounding SiO_2, a nichrome resistor of approximately 150 Å was sandwiched between two SiO_2 films approximately 1000 thick. A YAG laser beam was used to cut the nichrome film with the beam

intensity controlled to a point where the SiO_2 films were not shattered or made to bubble. A sputtering auger analysis was performed on both the unheated nichrome and the heated nichrome regions. During the measurement process, material was being sputter removed; hence, the measurements made with respect to a particular sputter time would be related to the material found at a particular depth. The results of the auger measurements are given in Figure 38. The nickel and chromium are both shown to diffuse upward and downward into both SiO_2 films. An examination of the top surface of the SiO_2 film indicated the presence of nickel and chromium, as evidenced by the readings taken at sputter time zero.



a. Auger chromium peak versus sputtering time



b. Auger nickel peak versus sputtering time

Figure 38. Auger measurement results, $SiO_2 - NiCr - O_xSi$ sandwich.

Electromigration – Electromigration is the motion of flow of atoms which results from the passage of direct current in a conducting material. The transport in a conductor occurs from the interaction of charge carriers, such as electrons, with atoms rather than directly from the electric field force exerted on the ionic cores of the atoms. D'Heurle and Rosenberg* have made a rather extensive study on this subject. In essence, the conducting material is moved along in the same direction as the electron flow. The movement increase is relative to the increase of electric current density and temperature. At the neck of the nichrome fuse, the resistance is highest and the cross-section is smallest. Hence, it has the highest temperature and current density along the length of the fuse. The higher movement at the neck results in depletion of the neck area material. This depletion causes a further current density and temperature increase, which in turn results in faster depletion in this area. This condition accelerates until the conductor completely opens. The resultant break can consist of interconnecting voids extending from edge to edge along grain boundry paths. Glass passivated conductors show a reduced electromigration activity as compared to unpassivated conductors. This theory appears plausible for cases in which the currents through the fuses are insufficient to cause melting.

J. R. Black**estimated that the median time to failure (MTF) by electrical open of a metallization is given by

$$MTF = \frac{K_1 AT}{J^n D_o \exp(-Q/KT)}$$

where:

A = cross sectional area of the metal

J = current density

D_o = diffusion coefficient

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*F. M. D'Heurle and R. Rosenberg, IBM, "Electromigration in Thin Film," in Physics of Thin Films, edited by G. Hass, M. H. Francombe and R. W. Hoffman, 7, Academic Press, pp. 257-310, 1973.

**J. R. Black, "Physics of Electromigration," 12th Annual Proceedings, Reliability Physics Symposium, April 1974.

T = absolute temperature

Q = activation energy

K = Boltzmann constant

K_1 = proportional constant

The value of n varies between 1 to 3 under ideal conditions, depending on current density, trapped vacancies, glass sandwich structure, and temperature gradient caused by the current flow. For the case of the fuse link, one additional factor greatly affects the reaction rate which is reflected in the value of n. This factor is the thermal gradient across the length of the fuse resulting from the neck-down configuration of the fuse, heat conduction through the SiO_2, and heat conduction through the ends of the fuse to the aluminum pads. Thus, the center of the fuse becomes the hottest region. The temperature difference from the center of the fuse to the ends could be over 1000°C for short intervals. This large gradient could raise the value of n way above 3, which is the maximum measured under a normal steady-state condition of current flowing through well cooled metallization.

Opening of Unprogrammed Nichrome Fuse Links – Several years ago, the phenomenon of "disappearing resistors" was uncovered when thin film nichrome resistors were deposited onto silicon chips as part of the then new IC technology. The failure mechanism has been identified as electro-corrosion. This mechanism is caused primarily by water gaining access to the nichrome resistor traces through cracks and/or pinholes in the IC over-glass structure. Paulson, Lane and Bart* provided a comprehensive treatise on this subject.

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*W. M. Paulson, "Reliability of Thin Film Nichrome Resistors used on Radiation Hardened Integrated Circuits," Motorola, Final Technical Report, RADC-TR-73-105, April 1973, (AD911401).

C. H. Lane, "Nichrome Resistor Properties and Reliability," RADC Final In-House Report, RADC-TR-73-181, June 1973, (AD765534).

J. J. Bart, "Electron Beam Microanalysis of Electrochemical Attack on Thin Film Nickel-Chromium Resistors, "RADC Technical Report, RADC-TR-73-220, October 1973, (AD772677).

Electro-Corrosion Characterization – At the height of the "disappearing resistor" problem, failure rates of 50 percent at the component level were occurring for nichrome resistors during low temperature burn-in tests between 20 and -25°C. Burn-in at high temperature in the range from 125 to 175°C did NOT give rise to failures. Since failures occurred in the temperature range around the dew point of water, tests were designed to establish if water was a necessary causal factor. No change occurred in the resistors if they were soaked in deionized water for several days; however, if the resistors were electrically biased so that the normal rated current was flowing, the nichrome film underwent a rapid disintegration. Disintegration or void formation occurred at the most positive end of the resistor element as it emerged from the water. A similar result occurred with a biased logic chip when a drop of water was placed on its surface. The resistors on the logic gate were 0.5 mil wide and approximately 100 Å thick. For an open circuit nichrome resistor, the minimum size void can be as small as $2.4 \times 10^{-13} cm^3$ of material or 2.12×10^{-12} grams of nichrome. The required weight of water to react with this quantity of nichrome is 3.45×10^{-13} grams. The experiment at Hughes showed that a potential of approximately 1.4 volts was necessary for the reaction to take place. This potential is slightly in excess of the dissociation potential (1.22 V) for H_2O. Paulson's experience* indicated that 2.5 volts was required for reaction. Should the water contain ion-producing chemicals, electro-corrosion can occur at a very low potential. J. J. Bart**indicated that the variation in time to failure of nichrome resistors was not well correlated with the water contained in the packages that house the resistors but was correlated with the sodium contents measured at the defect sites in the passivation glass. Research papers from a variety of sources indicate that the electro-corrosion process entails some of the nickel forming nickel hydroxide, while chromium is oxidized to the chromic state which then forms chromic acid and water.

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*ibid., W. M. Paulson.

**op. cit., Bart, p.

Sources of Water for Electro-Corrosion – The source of water which facilitates the electro-corrosion process is either the package sealing glass (when such packages are used) or the package background atmosphere or inert gas employed during the sealing process. During the high temperature (485°C) devitrification cycle of solder sealing glass, water can be driven off from the surface of the screened-on material and water is evolved from the decomposition of the organic binders and forming additives used during the sealing process. Water vapor concentrations up to 35,000 ppm, with a dew point at approximately 22°C, have been found in package cavities.

Vapor deposition of the overglass also provides an additional source of water for electro-corrosion. The main reaction byproduct is a phosphorus-doped SiO_2 which can be described by

$$4PH_3 + SiH_4 + 6O_2 \rightarrow SiO_2 + 2P_2O_5 + 16H$$

Hydrogen, which is liberated, is in a highly active condition and will react with the abundant supply of oxygen to form water. Since water is formed in the immediate vicinity of the deposited glass, some may be included in the overglass layer.

Water may also be made available from other sources, depending on the structure of the device and its associated packaging materials. The water content of a number of thin film materials has been calculated and this information is provided in Table 7.

Contributions of Pinholes and Microcracks to [illegible] Corrosion – Variations in chip surface profiles, masking defects [illegible] surface of the device permit or facilitate the [illegible] of pinholes and microcracks in the overglass structure. In some [illegible], pinholes can be associated with the overglass film while microcracks can be associated with the nichrome-aluminum metallization interface. Microcracks in the overglass can be caused by shadowing of the aluminum during the evaporation process. Pinholes have been caused by residue matter found on the surface of the wafer. This matter is usually particulate material trapped within the initial nucleating film layer. In the case of residual matter on the surface of

TABLE 7. WATER AVAILABLE FROM DIELECTRICS
(FILM THICKNESS 1 μm)

	Monolayers
*PSG + SiO_2 Cap	100
PSG (6 percent P by weight)	81
SiO_2 (CVD)	62
Thermal Oxide 15D – 60W – 15D	58
Thermal Oxide 15D – 30W – 60D	42
Alumino Silicate Glass Corning 1723	42
Sputtered Quartz	21

*Phosphosilicate Glas (PSG)

the wafer, random relaxation phenomena occurs which gives rise to a pinhole when all the fabrication sequences have been completed. Both the pinholes and microcracks present sites of high surface energy for the preferential condensation of water from the vapor. Voids can be generated under circumstances in which a liquid H_2O film has been formed on the surface of the packaged and enclosed device and pinholes are present in the overglass; if the pinholes reach down to the chip surface, the H_2O film is allowed to come in contact with the nichrome resistor film. The subsequent test or use of the device in its operational mode provides the activating potential across the resistor or fuse, facilitating electro-corrosion of the nichrome material.

An additional source of pinholes in the overglass has been traced to the overglass deposition process; deposition temperatures are such that they will give rise to grain growth in the aluminum conductors and termination pads of the device. Grain growth or film reconstruction occurs, which results in the formation of aluminum hillocks or spikes; these structures can occur up to 5 microns high. The rough aluminum metallization and tall spikes are shown in Figure 39. These spikes can project through the

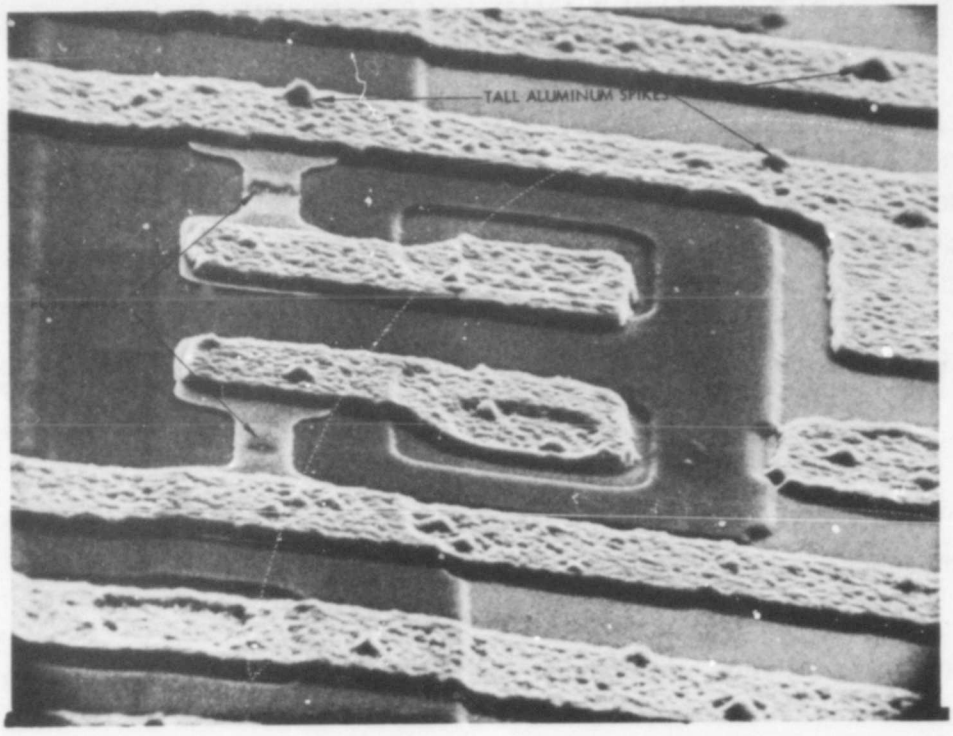


Figure 39.* Two partially blown fuse links and tall aluminum spikes

overglass which is approximately 1 micron thick. Should these spikes appear at the edge of the nichrome-aluminum interface, an easy path becomes available for water to move down through the overglass and come into contact with the nichrome film.

Premature decomposition of the reactant gases employed in depositing the overglass film can create pinholes which come into direct contact with the nichrome films. During premature decomposition of the Silox or Vapox gases, free SiO_2 is formed, which rests only on the substrate's surface; adhesion of the free SiO_2 is quite poor and during the etching of windows or steps, this material can be washed away. Masking defects are major contributors to pinholes. One supplier is now using double masking to minimize this problem. The prevention of pinholes and maintenance of overglass

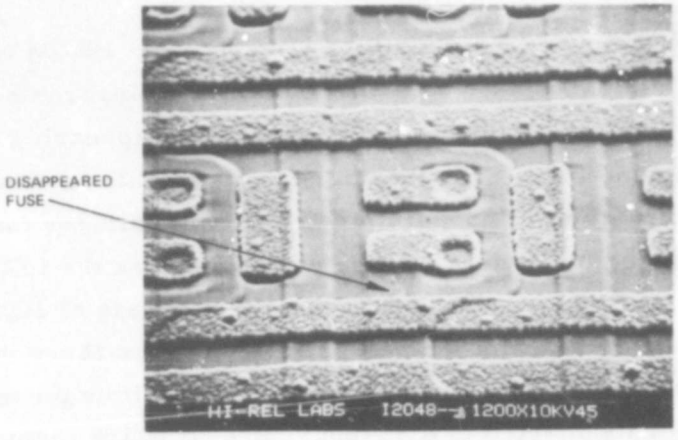
*Provided by P.H. Eisenberg

integrity is an absolute necessity for PROM devices because of the very high density of nichrome fusible links on each chip and the damaging effects on device reliability should water penetrate through the overglass film.

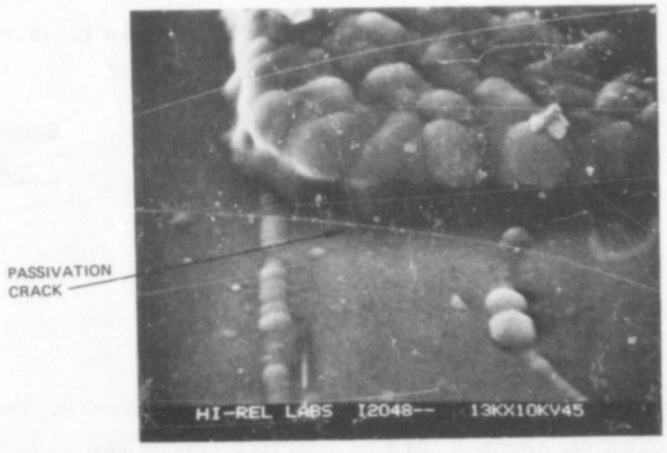
Unprogrammed Nichrome Fuse Failure Experience – PROM nichrome fuse links are usually smaller in length and width, but comparable in thickness to the IC nichrome resistors that experienced the "disappearing resistor" problem. Nichrome fuses are, therefore, susceptable to electro-corrosion as a failure mechanism. Unprogrammed fuse link failures totaling 19 or more were reported by a user in 1974, which includes the following information. Data were provided on a 2K PROM used at a rate of 1000 to 2000 per month. A standard programmer was used to program these devices. Following programming, the devices were employed in various pieces of equipment, which in turn were subjected to a 96-hour burn-in which included temperature-cycling (-15 to +55°C); power was applied to these devices and cyled on and off. The equipment was then subjected to electrical tests. Changes in PROM output bits were detected on some devices. Fault isolation data indicated that output bits and addresses had failed randomly, rather than being associated with specific locations. The following data illustrate two devices that experienced bit changes:

S/N	Address	Initial Output Pattern	Output Pattern Changed to
19	68	1110	1010
	201	0100	0000
	309	1101	0101
26	211	1111	1110

A series of tests (Thermal Cycling, dynamic burn-in, leak test, etc.) was then performed on sample lots to identify the cause of failure. Several failed devices were then delidded and subjected to SEM examination. A nichrome fuse, which failed due to electrochemical degradation, is shown in Figure 40 before the glass passivation was removed. The definite fracture in the passivation, existing near the nichrome-aluminum interface, can be seen in Figures 40b and c. This fracture resulted in exposure of the

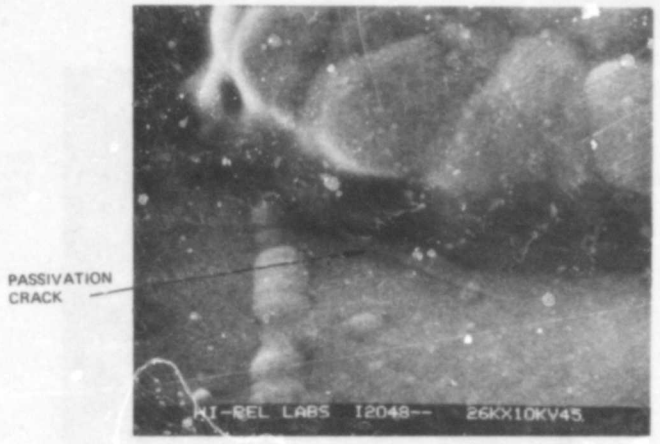


a. Entire area



b. Close-up of portion of disappeared nichrome fuse

Figure 40. SEM photos of PROM chip with disappeared nichrome fuse (passivation intact)
(Sheet 1)



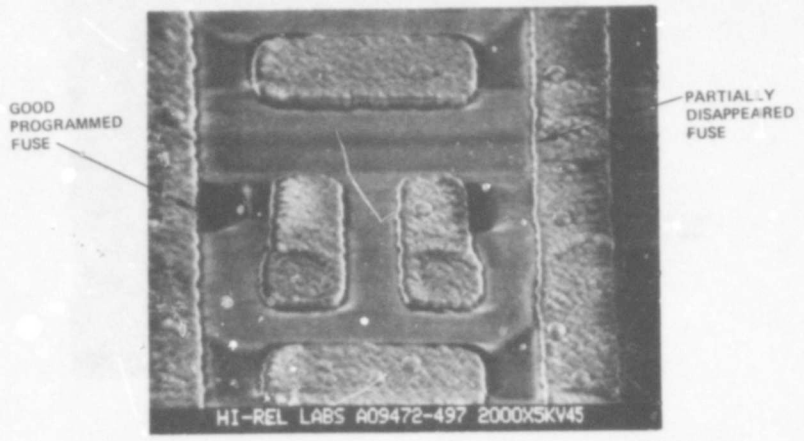
c. Close-up of passivation crack on top of nichrome fuse shown in b

Figure 40. SEM photos of PROM chip with disappeared nichrome fuse (passivation intact) (Sheet 2)

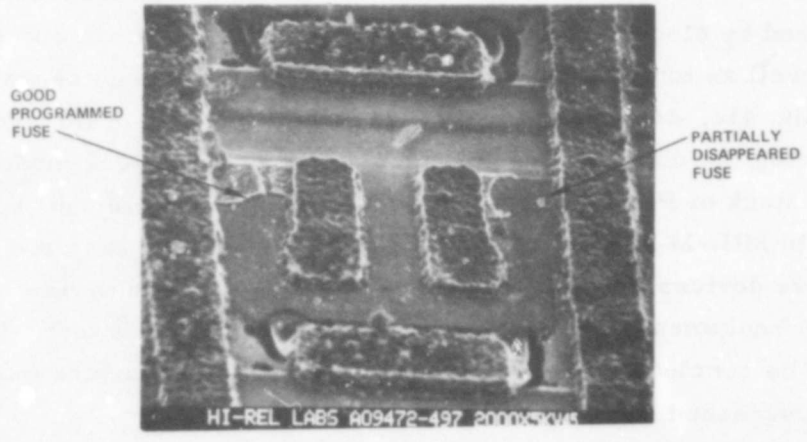
nichrome fuse to moisture. Figures 41 and 42 show additional failed fuse links, caused by electro-chemical degradation. Figures 41a and 42a show partial as well as total corrosion of fuses before the overglass was removed. Figures 41b, 41c, 42b and 42c show fuses after removal of the overglass.

Following the discovery of the electro-corrosion failure mode, the remaining stock of PROM devices were put through 'freeze-out' tests described in MIL-M-38510/201 specification. This test was used to cull out defective devices. No failures were reported on good devices subsequently installed in equipment, after having passed the 'freeze-out'test. It can, therefore, be concluded that devices susceptible to this failure mode can be effectively screened through use of the freeze-out test.

When the black Cerdip package (Type I) was used, a significantly higher number of failures occurred than with the white Cerdip package (Type II) from the same PROM vendor. After the vendor was notified of the failures, he deleted the Type I package from his MIL-temperature PROM line.

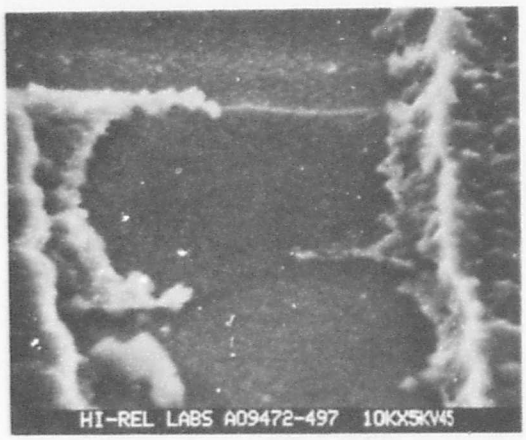


a. Passivation intact



b. Passivation removed

Figure 41. SEM photos of PROM with one good programmed and one partially disappeared nichrome fuse (Sheet 1)



c. Close-up of partially disappeared nichrome fuse shown in b

Figure 41. SEM photos of PROM with one good programmed and one partially disappeared nichrome fuse (Sheet 2)

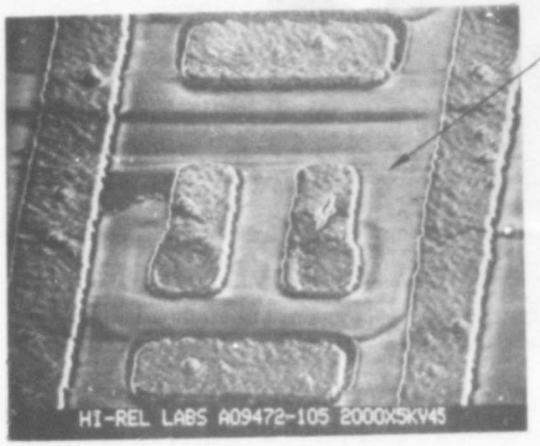
Realizing the importance of packaging techniques to the electro-corrosion problem Zatz,* performed experiments on Cerdip and Kyoto packages, with the following results:

	CERDIP	KYOTO
Sample Size	100	200
Total Failures	27	0
Average Dew Point	$+18^{\circ}C$	$-30^{\circ}C$

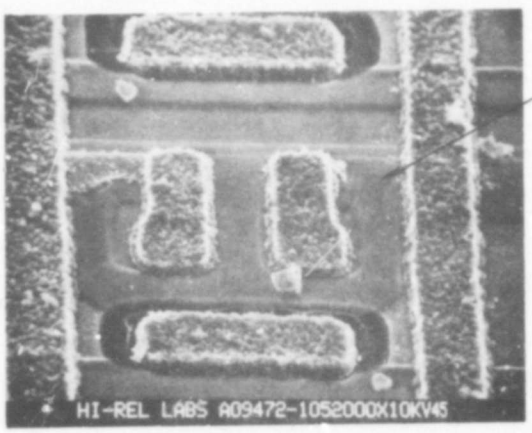
In this experiment, devices of Type 54L00 were put into Cerdip and Kyoto packages, which were then put into a chamber under $0^{\circ}C$ ambient, with bias voltage cycled at 1 minute intervals, for a total of 1000 hours. The failures were attributed to electrolytic corrosion of the nichrome resistors on the IC chips.

It appeared that the sealed-in water in a black Cerdip package was sufficient to cause failures. The Kyoto and the white ceramic dip package with the solder seal appeared to give satisfactory protection against this

*S. Zatz, F. A. Malzahn, H. Samelson and R.E. Sulouff, "Changes to Integrated Circuit Packages Reduce Contamination and Provide Major Reliability Improvement in Dielectric Isolated Devices," Proceedings of Government Microcircuit Application Conference, June 1974.

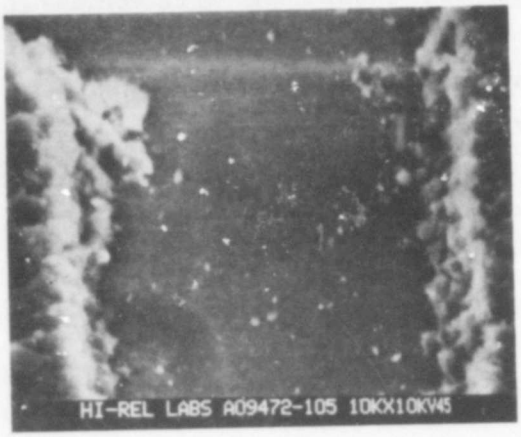


a. Passivation intact



b. Passivation removed

Figure 42. SEM photos of PROM chip with completely disappeared nichrome fuse (Sheet 1)



c. Close-up of completed disappeared fuse

Figure 42. SEM photos of PROM chip with completely disappeared nichrome fuse (sheet 2)

failure mechanism. The package seal must also be satisfactory; integrity of the seal can be verified by screening tests, such as thermal shock and vacuum leak.

A second user also reported a PROM failure due to electro-corrosion. Failure analysis revealed that a void in the passivation permitted the moisture to reach the fuse. This occurrence was isolated and was probably caused by random defects in masking or contaminant particle on the wafer during processing.

Long Term Current Effects on Unprogrammed Nichrome Fuse – Experiments conducted under this study have shown that with low programming pulse voltage amplitude, it could take as long as 15 to 20 seconds of pulse time to open a fuse. Thus speculation arises of the possibility that under normal usage of low current the unprogrammed fuse could open up after some years. Dr. Roger Mo* described empirical data obtained for estimating the 50 percent lifetime of specially fabricated nichrome fuses. The fuses used were

*R.S. Mo and D.M. Gilbert, "Reliability of NiCr Fusible Link Used in PROMs," Journal of the Electrochemical Society on Solid-State Science and Technology, July 1973

approximately 350 Å thick and 6 μm wide at the fuse neck. The composition of the nichrome was roughly 65 percent Ni and 35 percent cr. Fuses were opened utilizing various amount of current. Some fuses took as long as 100 days of current application before opening. Weibull plots were used to estimate 50 percent life times for the groups of fuses (Figure 30). It was found that the 50 percent life-times for low fuse currents follow the Arrhenius equation

$$L_f = A \, Exp \, (\phi / KT_f)$$

where:

- A = constant
- K = Boltzmans constant
- ϕ = Activation energy
- T_f = Calculated fuse temperature
- L_f = 50 percent lifetime

T_f was calculated from known fuse resistance, fuse current, fuse current required to bring fuse to melting point (1400°C), and chip temperature. The data covered the range of T_f from 1400°C to 300°C. It was found by extrapolation from the Arrhenius model that at T_f of 110°C that the 50 percent life time is in the order of 10^5 years, which corresponds to less than 1 percent failure after 10 years of continuous operation of a 1024 bit PROM. If the temperature T_f is 50°C, the 50 percent lifetime would be around 10^9 years. The life times of particular fuse types would vary depending on the fuse material composition, geometry and electrical stress imposed. It is felt that, within the design practices traditionally used, long term current effects should not cause concern in the reliability of PROMS.

Unprogrammed Nichrome Fuse Failure Prevention – From the preceding discussions it can be concluded that the primary failure mechanism for an unprogrammed nichrome fuse is electro-corrosion. The three interacting factors affecting the opening of unprogrammed nichrome fuse links by

electro-corrosion are the presence of: (1) water which has been able to find a path to the fuse link material, (2) alkaline contaminants in the water reaching the fuse material, and (3) an electrical potential across the fuse. The presence of electrical potential is unavoidable as the fuse is part of the circuit. It has been reported that under certain favorable conditions which include the presence of alkali ion contaminated H_2O, a nichrome resistor can open within microseconds, after an electrical potential is applied. Thus, even if a sampling technique was used to interrogate fuse links to minimize electrical potential application they could still open under conditions favorable to this type of failure mode. Alkali compounds, particularly sodium compounds, can be found inside hermetically-sealed packages, although processes are being improved toward minimizing this kind of contamination. Water appears to be the most controllable factor; one can either (1) minimize water content inside the package, or (2) prevent water inside the package from making contact with the fuse link material.

If the surface of the silicon chip is perfectly passivated, water inside the package will never reach the nichrome film. For integrated circuits, a double layer of passivation, consisting of evaporated SiO and vapor-deposited SiO_2, has been adopted during the past several years to prevent microcracks and pinholes. PROM suppliers generally employ only a single layer of passivation; SEM photographs of microcracks in the overglass have been used to identify the relationship between passivation defects and opening of unprogrammed fuse links. Improving PROM device reliability will require further efforts on the part of suppliers to improve PROM device passivation processes and package seal and use of low water content packages. Meanwhile, the "freeze-out" test remains the most effective method of screening out potential corrosion failures.

Reconduction of Opened Fuse Links

Marginally-Opened Fuse Links – Current programming yield losses of nichrome fuse link PROMs are approximately 5 to 10 percent. This percentage partially depends on how the bit is tested to determine its '0' or '1' state; many variables, such as V_{cc} and temperature, may not be at the specified values when tested. This could lead to acceptance of a bit whose apparent resistance is high enough to simulate values associated with that of a correctly programmed (opened) fuse link. When interrogated under operating conditions in its equipment, leakage across an 'opened' fuse would permit sufficient current to flow to permit it being considered as an unprogrammed bit under certain electrical and environmental conditions. These devices, therefore, exhibit bits that appear to have grown back, or reconducted. Actually, these fuses were conducting the same current immediately following their programming, rather than changing state as a result of their usage in equipment. It is, therefore, important that this type of failure mechanism be minimized. Suppliers have suggested subjecting the PROMs to temperature extremes and lower V_{cc}, while verifying the programmed bits; these tests can be used for weeding out marginal PROM devices.

Increased Conduction of Open Fuse Links – Many users have experienced fuse 'grow-back'. The term reconduction is more appropriate for describing this phenomenon, as it involves increased conduction of the fuse link. The electrical characteristics of open fuse gaps and their relationship to reconducting fuses are discussed in this section. The reconduction mechanism is explored in terms of its causal factors.

Unlikely Growth of Whiskers and Dendrites in the Fuse Gap – Many of the SEM photos of blown fuse links show conducting fingers extending from the fuse link ends into the open gap. This led to the speculation that these fingers might be similar to whisker or dendritic growths that were experienced with various metals. Unfortunately the fuse gap is beneath approximately 10,000 Å of overglass material. Visual observation of these fuse fingers or filaments was not possible without etching off the SiO_2. Thus if filament growths exist they cannot be observed visually, since preparing the

specimen includes chemical and/or plasma etching processes and would change the fuse environment completely. Whisker growths are usually connected with high current and high temperature conditions; dendritic growths are usually associated with contamination, moisture and high temperature. These conditions were not experienced by PROM devices that exhibited reconducting fuse links. The fingers in the open fuse gaps have round ends that are similar to the solidification of molten metal, rather than any kind of crystalline growth that would appear as sharp crystalline discontinuities. From these observations it was concluded that these fingers or filaments do not grow and that reconduction is caused by a combination of factors that are not normally associated with whiskers or dendritic growths.

Fuse Gap Electrical Characteristics — In an earlier section, it was concluded that the fuse gap consists mainly of dielectric material with scattered metal aggregates. Conduction through such material is believed similar to conduction through a thin film dielectric. Jonscher* offers the following theory on conduction through a thin film dielectric. In principle a dielectric film should show an ohmic region of voltage-current (V/I) characteristics at low electric fields. At higher field regions, the behavior depends to a large extent on temperature. An example of dielectric conduction, from Johscher,* is shown in Figure 43. The four regions are indicated by dotted lines. Region I is the ohmic region already mentioned. Region II gives a relationship of

$$I \approx e^{\left(\frac{1}{T}\right)\left(V^{1/2}\right)}$$

where T denotes temperature.

*A.K. Jonscher, "Electronic Conduction in Dielectric Films," in Thin Film Dielectrics, edited by F. Vrathny, published by the Electrochemical Society, 1969.

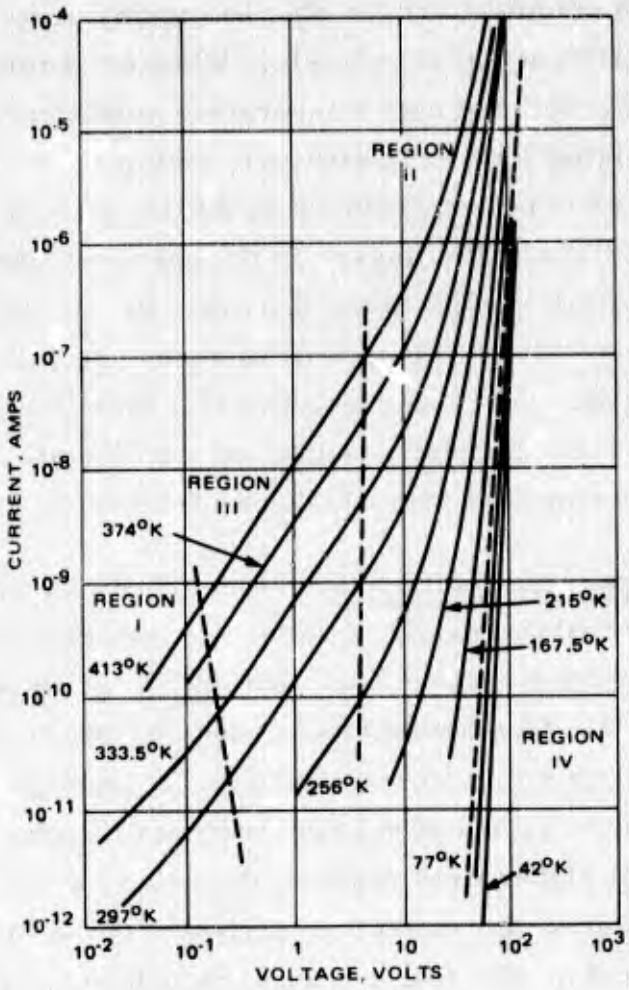


Figure 43. Current voltage characteristics of high conductivity silicon oxide (typical example).

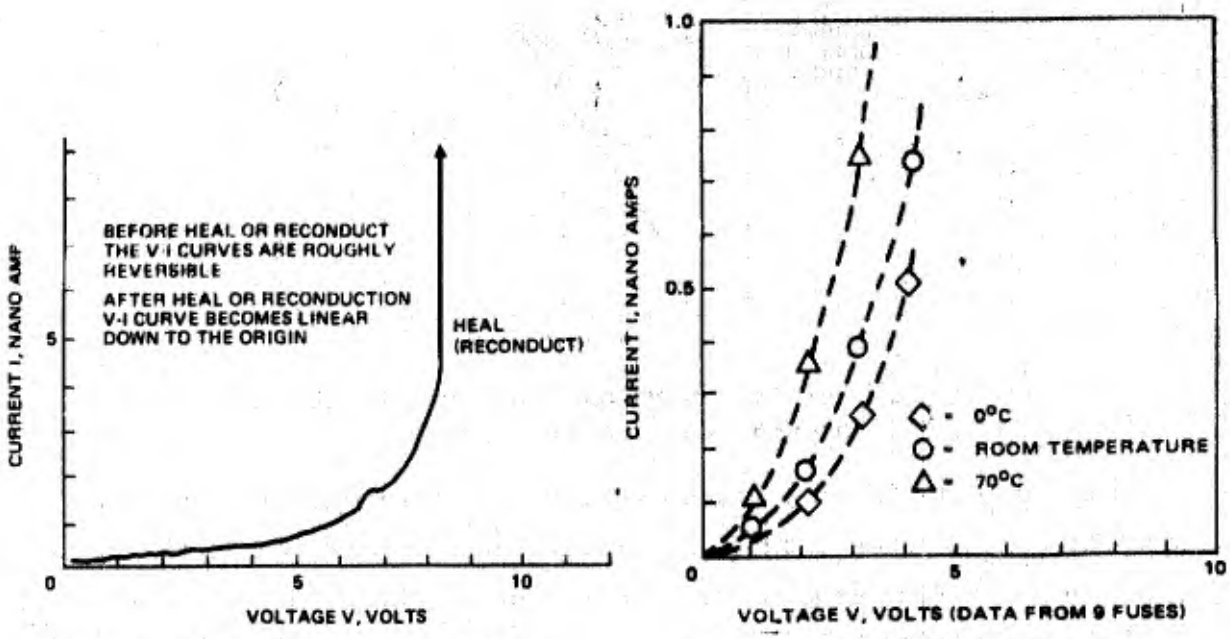
Region III is intermediate between regions I and II and gives a relationship of

$$I \approx V^n \qquad (\text{for } 1 < n < 2)$$

At region IV the relationship becomes

$$I \approx V^n \qquad (\text{for } 5 < n < 15)$$

V/I characteristics of program opened NiCr fuses reported by Mo* are shown in Figure 44. The fuses were specially fabricated for evaluation. These V/I characteristics resemble those shown in Figure 43.



a. Of opened nichrome fuse.

b. Versus temperature of nichrome fuses.

Figure 44. V/I characteristics.

Reconduction with Respect to Breakdown Potential and Time — Generally a dielectric film will break down if a sufficiently high potential is applied across the film. The theories involved include electrical breakdown under the names of intrinsic, avalanche, field emission and thermal breakdown. It is believed that the ultimate breakdown mechanism for the fuse gap is the thermal breakdown which can be initiated in many ways via electrical breakdown. It is theorized that thermal conditions during breakdown can cause the adjacent metal to melt and can cause a permanent connection across the dielectric. The thermal breakdown process in terms of the V/I characteristics is depicted in Figure 45.**

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*R.S. Mo, private communications.

**op. cit., Jonscher.

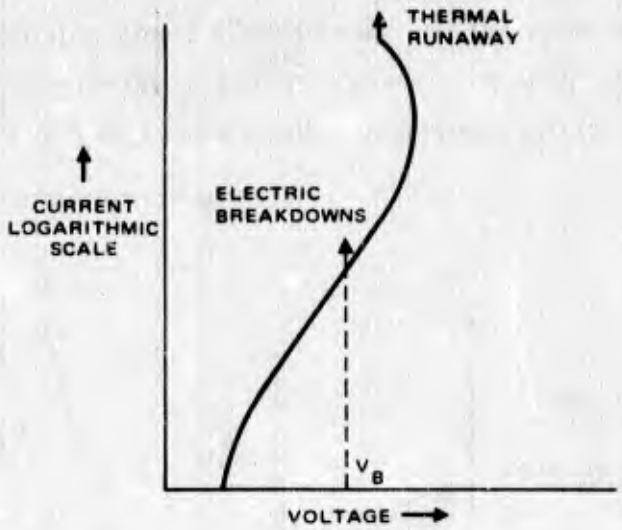

Figure 45. Identification of breakdown process with V/I characteristic.

Fuse gap breakdown voltages versus time-to-program of specially fabricated NiCr fuses is shown in Figure 46.* Voltage ramps of varous slopes were used to program the fuses to obtain the various times-to-program. Data on reconduction were also collected on fuses other than those tested for breakdown voltages. The probability of reconduction (fraction of total) of these fuses is also plotted in Figure 46. From this figure, a relationship between breakdown voltage and reconduction probability can be deduced; the lower the breakdown voltage, the higher is the probability of reconduction. This relationship follows the concept of thermal breakdown mechanism for fuse gap reconduction. The distribution of various early mortality failure modes of NiCr PROM devices with respect to operating time is shown in Figure 47.* It is seen that the reconduction phenomenon is time related, i.e., a fuse reconducts after a voltage is applied across the fuse for a length of time rather than instantaneously. A further look into the thermal breakdown mechanism is required. Klein** discusses the phenomenon of

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*P.G. Franklin, Monolithic Memories, Inc., "Programmable Read Only Memory Reliability Report II," April 1, 1974.

**N. Klein, "Electric Breakdown in Thin Dielectric Films," in Thin Film Dielectrics, edited by F. Vrathny, published by the Electrochemical Society, 1969.

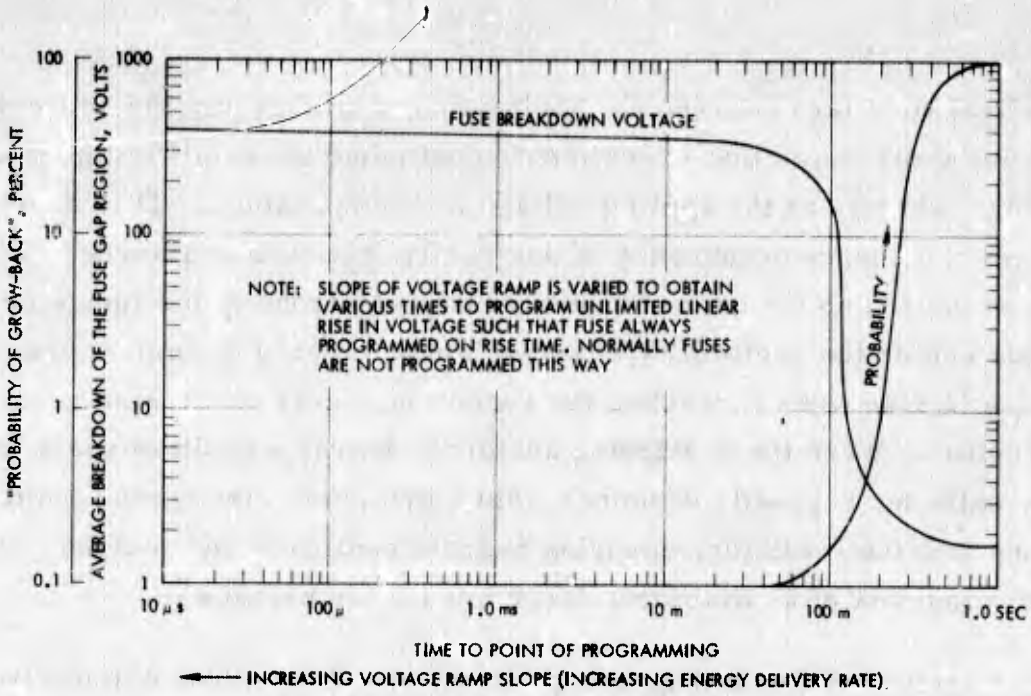


Figure 46. Time to program versus gap breakdown voltage and "grow-back" or reconduction probability of voltage ramp programmed nichrome fuses.

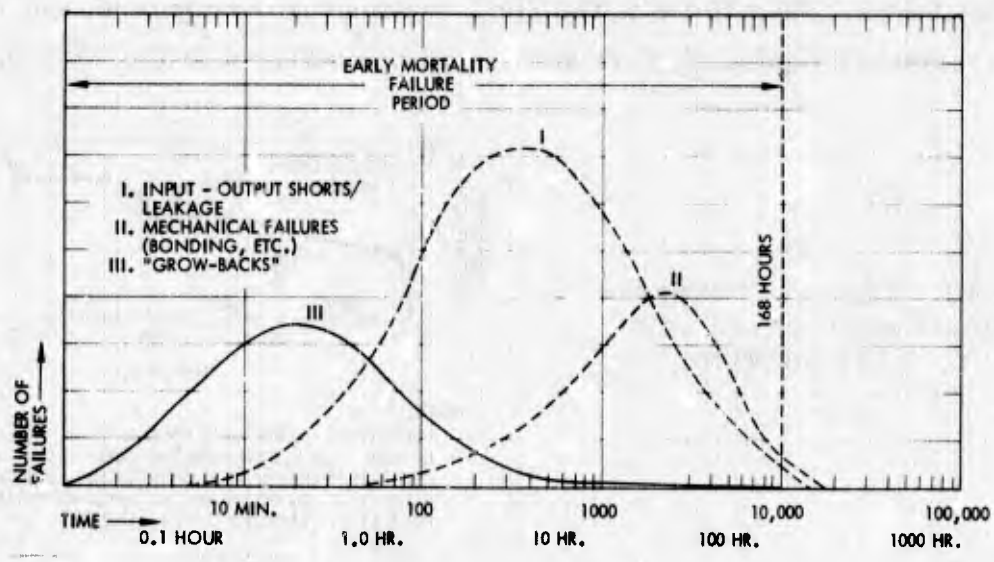
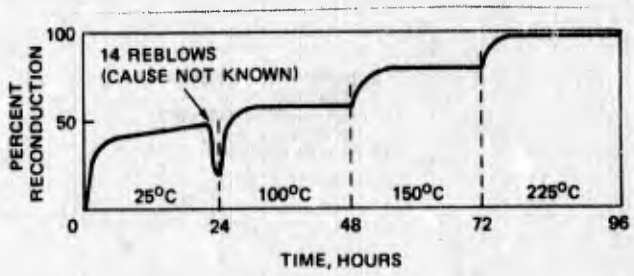


Figure 47. Distributions of failures according to failure mode versus operating time of certain nichrome PROMs.

statistical time lags between the application of voltage and the consequent breakdown and shows that experiments confirmed the relationship of lag time varying inversely as the applied voltage and temperature. This theory involves the chance occurrence of destructive electron avalanche. These chances depend on the rate of supply of free electrons in the insulator at the cathode and on the probability of an avalanche induced by impact ionization growing in size when it reaches the anode, in excess of the size required for destruction. When the developing avalanche leaves a positive space charge at the cathode, it greatly enhances field emission of electronics from the cathode into the insulator, ensuring current continuity and making possible the development of an avalanche large enough for breakdown.

Reconduction with Respect to Temperature and Time – The cumulative reconduction curve, Figure 48* was obtained from applying 4.5 V across specially fabricated fuses that were blown by a ramp voltage of 1 V/sec. The voltage was continuously applied through every change of temperature. At each temperature a new infant mortality region developed such that most of the changes occurred within 2 hours of the temperature step. The total number of reconductions increases with temperature. An anomaly developed just before 24 hours, when some of the reconducting fuses reopened, but they soon reconducted again. A slow voltage ramp was used to facilitate obtaining



NOTE:
FUSES WERE BLOWN WITH 1 V/SEC RAMP. 4.5V WAS APPLIED ACROSS EACH BLOWN FUSE THROUGH TEMPERATURE CHANGES.71 OUT OF 72 BLOWN FUSES RECONDUCTED. MOST RECONDUCTION OCCURRED WITHIN 2 HOURS OF TEMPERATURE STEPS. TEMPERATURE CHANGED EVERY 24 HOURS.

Figure 48. Time and temperature effects on reconduction of slow ramp blown nichrome fuses.

*From R.S. Mo, private communications.

fuses that would reconduct. Therefore, the information here should not be used for estimating reconduction probabilities on actual PROM devices.

As described in the section on programming experiments, an experiment was conducted with 512 fuses in an actual device opened with rectangular voltage pulses of various amplitudes to obtain different blow times. Some pertinent information on reconduction is summarized here. A distribution of blow times in terms of number of pulses for this group is given in Figure 49. These devices were then put on test under the condition of dynamic addressing and 125°C ambient temperature. At the end of 840 test hours, two reconductions had occurred, one at 120 hours and one at 648 hours with corresponding blow-times of 2.4 and 5.2 seconds, respectively. These

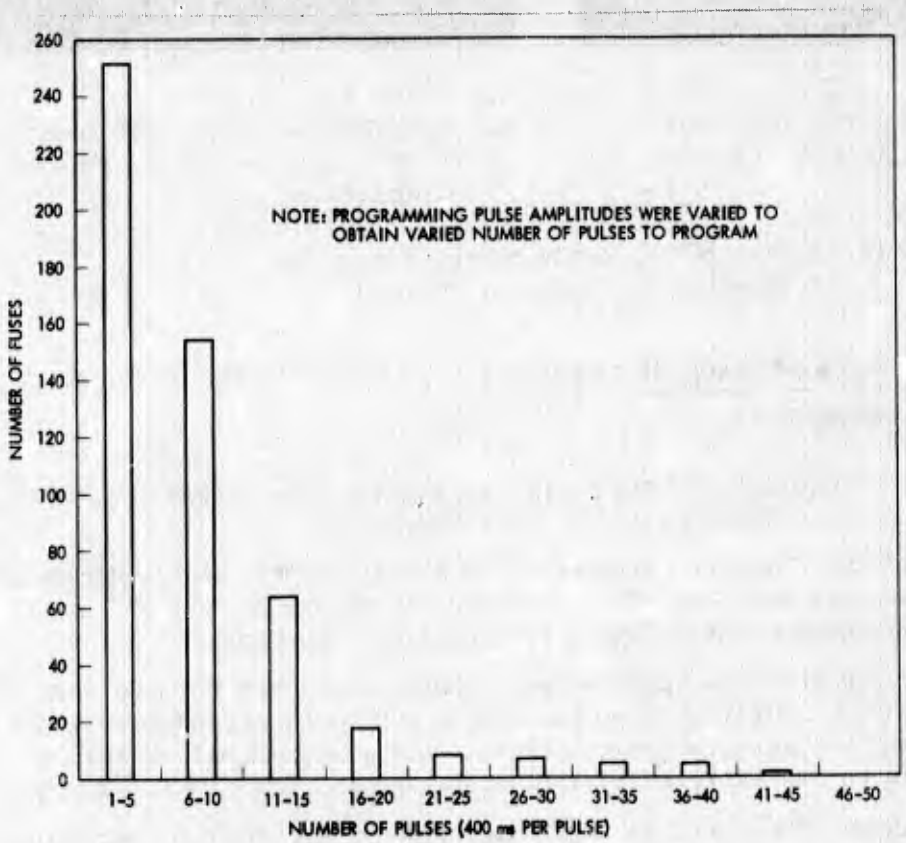
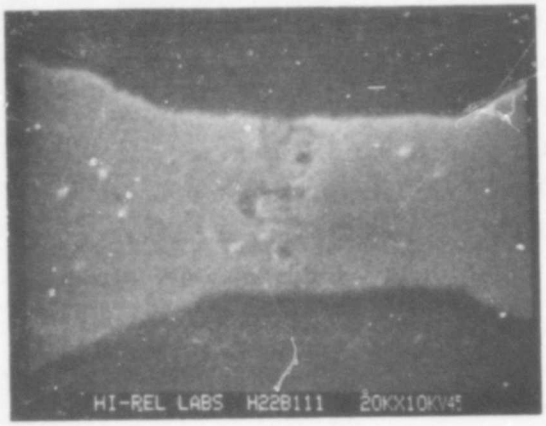
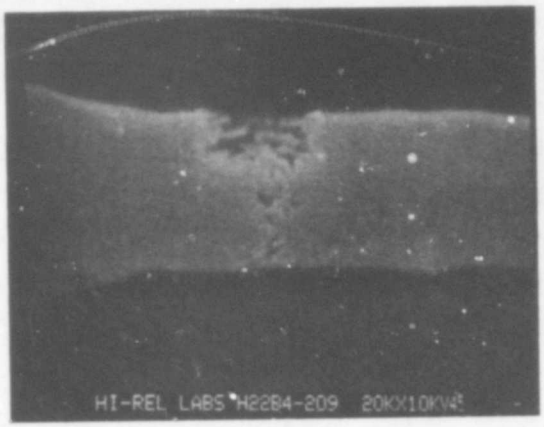


Figure 49. Distribution of number of pulses to program for nichrome fuses.

two fuses were examined by means of SEM. SEM pictures of these fuses after plasma etching are shown in Figure 50. The shape of the open gaps of these fuses is classified as being long time-to-blow fuse link gaps.



a. Reconducted after 120 hours of of operation at 125°C PROM ambient.



b. Reconducted after 648 hours of operation at 125°C PROM ambient.

Figure 50. SEM photos of nichrome fuse (chemical and plasma etched).

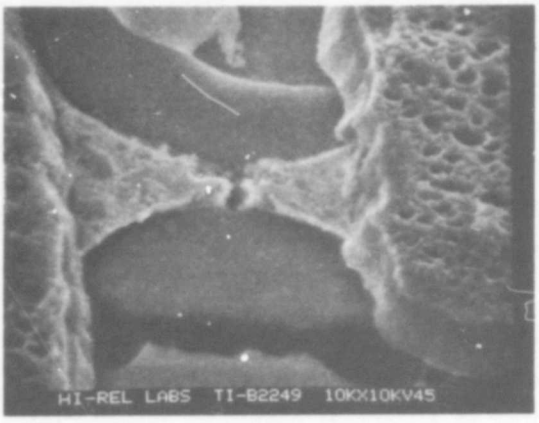
Summary of Fuse Reconduction Mechanisms – The above discussion on reconduction is summarized below:

1. Under low voltages, an open gap can show a conductance similar to the conductance through a thin film dielectric.
2. A gap will demonstrate breakdown if a sufficiently high voltage is applied across the gap. The mechanism can be described as an electrical breakdown followed by a thermal breakdown.
3. The time lag between application of voltage across the gap and breakdown is a statistical event with lag times varying inversely as the applied voltage and temperature. This statistical variation gives rise to the early mortality phenomenon of fuse reconduction.
4. Narrow gaps likely will have the thinnest dielectric film structure separating the fuse link ends. Hence, they are most prone to reconduction occurrence under favorable voltage and temperature conditions.
5. The final mechanism that forms the permanent bridge is the melting together of the fuse ends at the gap.

Theory of Programmed (Open) Titanium-Tungsten Fuse Links – Programming of Ti:W fuse links is significantly different than programming nichrome fuses. An evaluation of Figure 51 indicates a high degree of uniformity in the appearance of fuse gaps throughout a significant population of blown Ti:W fuse links. The PROM programming circuit contains a zener diode that prevents turn-on of the program transistor below 7 to 8 volts. Each programmed fuse, therefore, is subjected to about 40 to 70 milliamps of current, unless leakage paths exist that reduce the current level to some value which will prevent fuse programming in a normal manner. Should the programmer fail to deliver 7 volts, the resulting current level will not be sufficient to blow the fuse link.

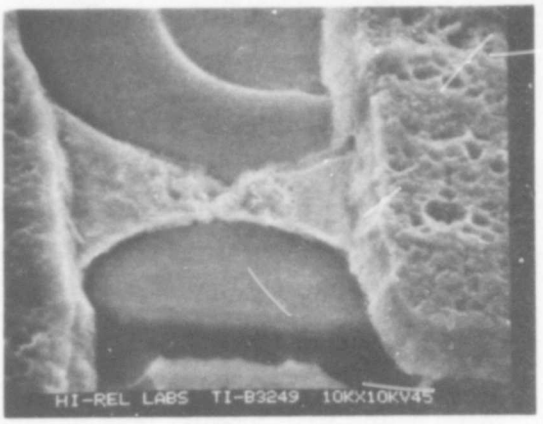
An examination of SEM photos of blown fuse links indicate an extremely small gap; the surface texture of each blown fuse link suggests that the outer molecular layers of the fuse have probably undergone substantial oxidation. Note the extreme reticulated and "flake-like" condition of the fuse surfaces, which might be caused by rapid oxidation of the titanium to its most stable oxide, TiO_2. The partial pressure of oxygen of some metal oxides as a function of temperature is shown in Figure 52.* Examining this family of lines indicates that titanium can rob oxygen from SiO_2 as the partial pressure of oxygen is quite high in the region surrounding the Ti:W fuse neck area during programming. The supplier of the Ti:W PROM indicates that the fuse neck temperature can rise to 3300°C while being programmed to the "open" state. The SiO_2 overglass and thermally-grown substrate oxide will tend to disassociate or vaporize at this temperature, releasing free oxygen which recombines with the highly active titanium-tungsten fuse material ends, forming a protective coating of TiO_2. It is doubtful that the fuse neck temperature will be elevated to a point where a large quantity of tungsten could oxidize; therefore, the fuse neck region will consist of a matrix of melted SiO_2, TiO_2, some TiO, trace amounts of WO_3, free tungsten and

*W. Espe, Materials of High Vacuum Technology, Pergamon Press, New York, 1969.



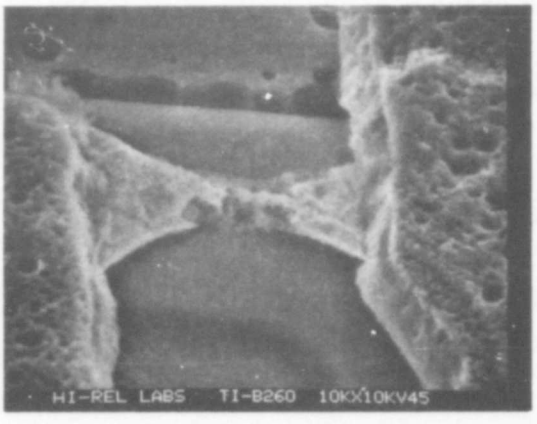
PULSE AMPLITUDE	10.5 VOLTS
LENGTH	10 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	<10 μs

a.



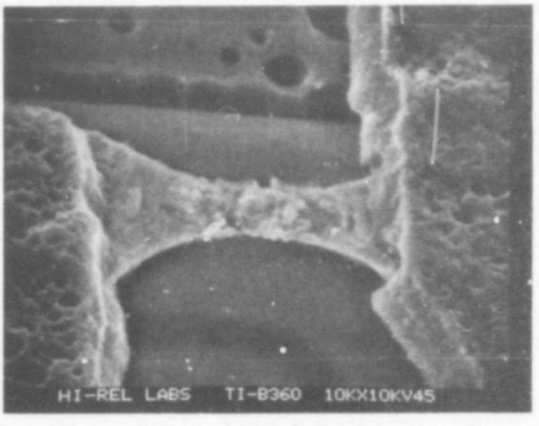
PULSE AMPLITUDE	10.5 VOLTS
LENGTH	10 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	530 μs

b.



PULSE AMPLITUDE	10.5 VOLTS
LENGTH	10 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	<10 μs

c.



PULSE AMPLITUDE	10.5 VOLTS
LENGTH	10 ms
RISE TIME	0.5 μs
TIME-TO-PROGRAM	>350 μs

d.

Figure 51. SEM photos of programmed Ti:W fuse (chemical and plasma etched)

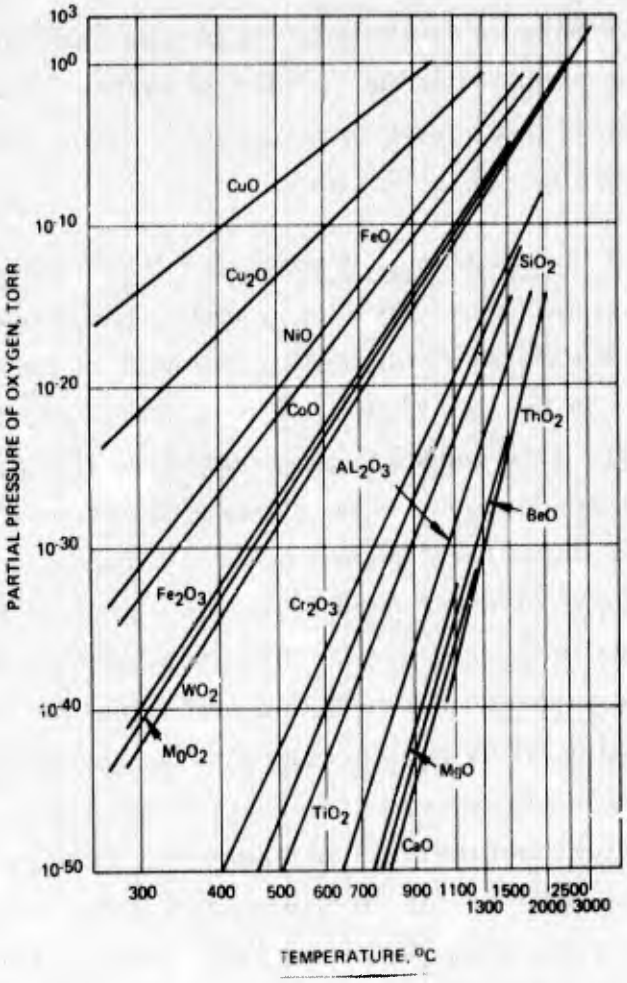


Figure 52. Partial pressure of oxygen of some metal oxides as function of temperature.

and possibly free silicon. The surface of the fuse material will consist primarily of TiO_2.

Ti:W Fuse Self Programming Possibility – Since the Ti:W fuses are thicker than nichromes and are rich in tungstens; therefore, the Ti:W fuses are less susceptible to electro-corrosion than the nichrome fuses. Although some self programming failures were reported; leakage paths appeared to be the cause. The vendor has implemented a test on his 256, 512, and 1024-bit PROMs to cull out such defectives. In essence this test runs through a simulated programming routine addressing every fuse, but without grounding the output. If the circuits are normal nothing will happen, but if high leakage exists some fuses would open and the part would be rejected.

Presently Ti:W PROMs are available in plastic packages only. The electrocorrosion problem might be quite different for different package types. In any event additional investigation will be required before more definitive conclusions can be drawn.

Ti:W Fuse Reconduction or "Growback" Possibility – The opportunity for fuse relinkage or 'grow-back' is probably small because of the high melting point of the Ti:W metallization, as well as the TiO_2 material covering the fuse ends in the gap region. The presence of an SiO_2/TiO_2 matrix, which is left in the fuse gap after programming, will also reduce the opportunity for fuse reconduction. It is possible to encounter momentary fuse reconduction and experience in instantaneous change in bit state because of the formation of one or more field emission-enhanced avalanche points between fuse ends in the gap area. It is possible that an extremely thin dielectric film separates fuse ends in a number of places within the gap area; these thin insulating films can undergo avalanche breakdown when the particular fuse link is interrogated during the normal equipment operation. The theory for electrical and thermal breakdown of Ti:W gap insulation is believed to be the same as for nichrome, which has been discussed in detail under the sections covering Nichrome Fuse Links. The permanent dielectric breakdown, resulting from field emission-enhanced avalanche, can be summarized as the occurrence of melting, evaporation, or disassociation of the molecular structure of the dielectric matrix material. The difference between nichrome and Ti:W fuse links might be their reaction to electron avalanche, field emission phenomena and thermal breakdown. Thermal breakdown in the nichrome fuse gap can cause melting of fuse end filaments, resulting in reconduction; this breakdown can be caused by the relatively low melting point of the nichrome material (1350°C), when compared to Ti:W, which has a much higher melting point (3300°C). Resistance to thermal breakdown and subsequent thermal run-away of Ti:W fuse ends is aided by the presence of TiO_2, which acts like an insulator covering fuse ends; this material also has a high melting point (1850°C). Ti:W fuses which have been programmed "open" might experience momentary reconduction; bit interrogation pulses could cause avalanche-inducing current to flow. Any

instantaneous short created by thermal breakdown can supply enough heat to the bridging metal molecules or conducting channel ends to permit re-oxidation without melting the ends together immediately following the interrogation pulse.

The Ti:W PROM vendor has stated there has been no evidence of "grow-back" to date, either by the PROM manufacturer or by device users. One of the users contacted indicates that they had experienced bit reversal on programmed devices. However, the cause might be in the device circuitry rather than the fuses because multiple fuse failures have occurred on the same device rather than one fuse failure per device. Intermittent reconduction, if it exists, can be verified by programming every fuse link of a 1024-bit PROM, with subsequent periodic interrogation of every bit. If a fuse link provides an indicated change-of-state, which is self-corrected during the following interrogation cycle, momentary breakdown of fuse material oxides may have occurred, followed by immediate re-oxidation. Verification of this potential intermittent failure mode for Ti:W PROMS may be suggested for a future PROM reliability program.

Avalanche-Induced Migration (AIM) Memory Elements

AIM (blown diode) PROMs are considerably different than their more conventional competitors, the fusible-link PROMs. Topics covered in this discussion include:

1. The AIM technology as covered in the AIM Patent No. 3,742,592, "Electrically Alterable Integrated Circuit Read Only Memory Unit and Process of Manufacturing."
2. Programming Pulse Requirements; the Relationship Between Junction Physical Characteristics and Programming Pulses; the AIM Diode Shorting Mechanism; Correlation of AIM Programming Techniques to the AIM Transistor Shorting Mechanism; and the Results of Diode Shorting Mechanism Investigations, including those of the device supplier, Hughes and RADC.

AIM Technology – The method of fabricating an AIM device is to use a pair of back-to-back diodes connected between each cross-over of row and column in a matrix. One of these diodes can be electrically shorted by the application of sufficient power in reverse voltage direction. These

back-to-back diodes are actually the emitter-base and collector-base junctions of a transistor, with a floating base. The total depth of the base region in the transistor is approximately 2 microns, with the distance between the emitter-base junction and the collector-base junction being of the order of 0.3 - 0.5 micron. The desired programmed short can be produced by a power or main pulse having a current of 150 to 200 milliamperes. The current required is a function of the size and geometry of the transistors used in the AIM device. If the applied current is reduced, it will be required to flow for a longer period to produce the same result. This longer pulse can be provided by using either a larger number of pulses or by the extension of the pulsewidth; the former approach is more preferable. A voltage in excess of 7 volts must be applied to the transistor, which is sufficient to cause reverse conduction through the emitter-base junction when the programming pulse is applied. One possible problem resulting from this programming method is that over-voltage of the emitter-base junction to short it out can also cause the failure of the adjacent collector-base junction; this can occur during improper programming, as the base thickness separating the two junction interfaces is approximately only 0.3 - 0.5 micron thick. The vendor recommends a programming procedure that is designed to enable shorting of the emitter-base junction only, without damaging the collector-base junction. A key factor in programming emitter-base junctions is the application of limited reverse current pulses through the emitter-base junction, while monitoring its resistance between pulses, thereby degrading the junction gradually; thus the desired junction shorting should be achieved without damage to the collector-base junction. As the base-emitter junction is progressively shorted or degraded, the resistance of the junction to the passage of low current monitoring pulses is measured. When the reverse biased junction resistance is reduced to a predetermined value, programming is terminated after the application of four additional power pulses to assure a safety margin in the short. The pulsed current value used for programming the reverse-biased junction is approximately 100X the rated value for the transistor.

AIM Diode Shorting Mechanisms – The vendor of AIM PROMs states that the exact mechanism involved in the electrical shorting of the base-emitter junction has yet to be conclusively identified. The vendor's patent

(Patent No. 3,742,592) states: "It may be postulated that metal atoms from an ohmic contact of the emitter actually migrate through the emitter-base junction."

During the early stages of AIM shorting mechanism investigations, it was presumed that second breakdown could be the primary shorting mechanism. Second breakdown, as described by J.S. Smith,* has its origin in the development of a localized region of high temperature within a conducting junction and can be caused primarily by non-uniform current conduction. Hot spots are formed at the junction interface, resulting in localized thermal runaway. Finally, the temperature in this localized area exceeds the melting point of the silicon, destroying the crystal lattice structure in this region; permanent shorting of the junction results.

Recently, the AIM device vendor has provided indirect evidence that second breakdown is probably not involved in shorting of AIM emitter-base junctions. Experimental quantities of PROMs were fabricated with a titanium:tungsten barrier layer between the aluminum metallization and the silicon junction contact areas. Current pulses thus cannot cause aluminum shorting spikes or channels to form because of the Ti:W barrier layer. The emitter-base junction was shorted, however, by the application of 50 to 100 percent more current than the normal programming pulse. When shorting did occur, both the emitter-base and the collector-base junctions were destroyed, suggesting that the crystal lattice structure of the base region of the transistor melted. It can, therefore be assumed that this catastrophic shorting was the result of a completely different mechanism than is normally responsible for single junction shorting. It is theorized that the alleged aluminum shorting spikes or channels normally produced by programming pulses could not be formed because of the Ti:W barrier layer, thereby necessitating the application of additional current to achieve junction shorting by second breakdown or a similar mechanism that causes melting of the base junction region.

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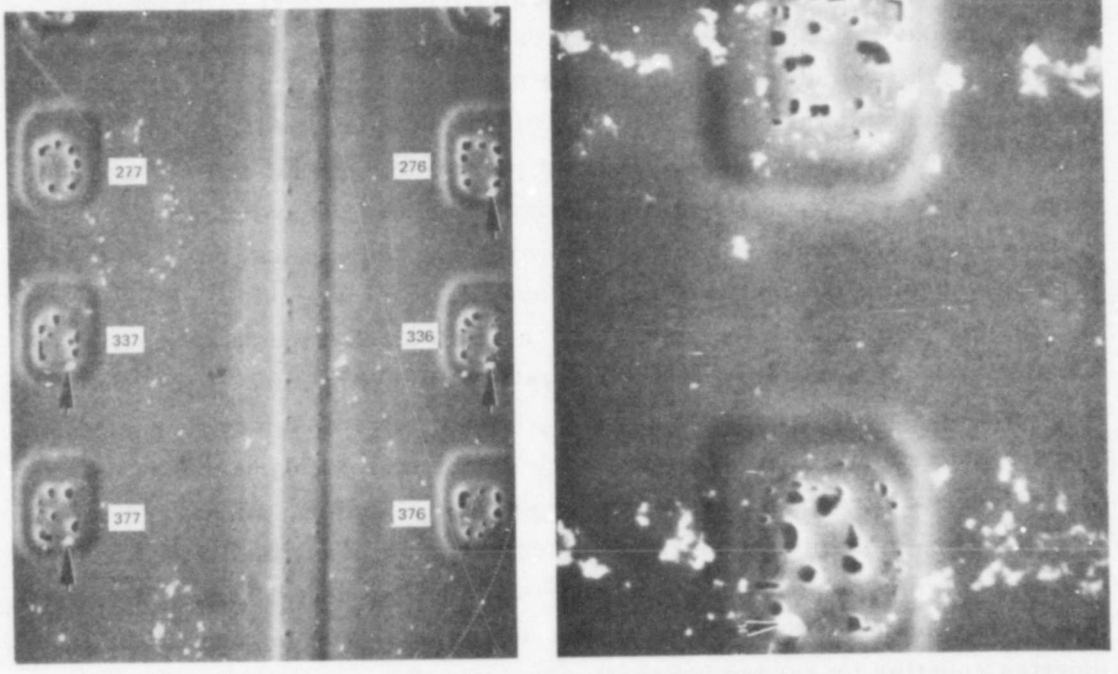
*J.S. Smith, RADC, "High Current Transient Induced Junction Shorts," Proceedings of the Ninth Annual Reliability Physics Symposium, March 1971.

There are continuing efforts to determine the exact shorting mechanism involved during programming; these efforts are being made by both the vendors and users of AIM PROM devices. Though the shorted region can be identified by its electrical characteristics, it has been difficult to identify the shorted junction area visually, even under very high magnification, due to its extremely small size. SEM photos* of the top views of programmed junctions with aluminum metallization removed (Figures 53a and b) consistently indicate a dimpled region that can be seen as a light spot on the periphery of the emitter contact area. This "dimpled" region appears on programmed transistors only, suggesting that this spot may be the location of the aluminum-rich shorting channel. The dimpled region is indicated by an



a. b.

Figure 53. SEM photos of top view of emitter contact after aluminum removal of AIM memory element.

*Figure 53 provided by Mr. B.W. Murry of Honeywell Information Systems.

arrow in Figure 53. The other black spots seen around the periphery of the emitter area could be shallow alloy pits formed during annealment of the aluminum to the silicon wafer's surface. An optical microphotograph* of a programmed junction is shown in Figure 54. Again a white spot is displayed.

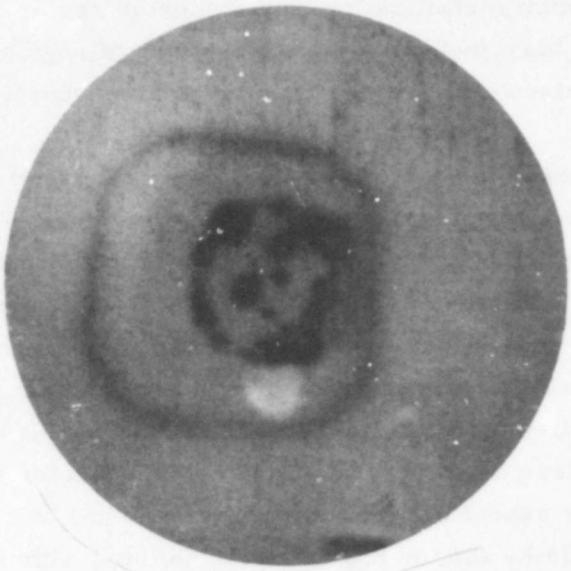


Figure 54. Optical photo of top view of emitter contact (after aluminum removal of AIM memory element).

Additional Information Relating to Formation of Aluminum-Rich Shorting Channels – As AIM shorted junction areas are likely to be formed well below the surface of the device (typically 1.5 microns), a substantial amount of chemical and plasma etching is required before the shorted area can be examined by micro-analysis tools. J.S. Smith** observed in transistors

*Figure 54 provided by Mr. R.S. Foote of Information Storage Systems.

**J.S. Smith, RADC, "Analysis of Electrical Overstress Failures," Proceedings of the Eleventh Annual Reliability Physics Symposium, April 1973.

with overvoltage failures that "Removal of the contact metallization, oxide, and silicon etching can delineate the short, but unless the short is massive, it is nearly impossible to tell which of the many imperfections the etch brings out is the shorted region." It is quite possible that AIM programming pulses that are longer than 100 μs in duration may permit the visible appearance of aluminum metallization in the shorted region. Smith states that it is possible to have metallization in the shorted region of a failed transistor for shorter pulsewidths but the diameter of the shorted region is generally larger.

J.F. Knudsen* in his work on examining induced transistor failures employed electrical probe tests, precise metallographic cross-sectioning and X-ray microprobe methods to determine potential shorting mechanisms. Results revealed highly conductive aluminum-rich channels within the monolithic silicon; these channels were nominally 10 microns wide by 6 microns deep and extended continuously from the base contact to the collector contact. The AIM supplier indicated that indeed such bridging was observed on their early PROM designs where the emitter and collector contacts were side by side. Another aspect of this problem that should be considered is that for longer pulsewidths and/or higher power pulses, aluminum may be found as a result of the silicon melting first with relatively rapid aluminum migration into the melted region. Although the actual shorting mechanism may be difficult to observe or identify, available theories seem to re-enforce rather than detract from each other; this pertains to the theory of formation of aluminum-rich channels as well as the possibility of crystal lattice melting due to some mechanism similar to second breakdown, with almost immediate migration of aluminum into the melt areas. Once shorted, the AIM base-emitter junction will probably retain its programmed condition, as there is no documented evidence to date that these devices have experienced bit reversal. The reported failures appeared to be related to the circuitry in general.

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*J.F. Knudsen, Lockheed, "Metal Bridging Under Planar Oxide," Proceedings of the 1970 Annual Symposium on Reliability, February 1970.

AIM Memory Element Failure Mechanisms – Based on the foregoing discussions it appears that once a diode is shorted, it is not likely that it would open. Reliability data have not revealed any open "shorted" diode failures. The probability of an unprogrammed diode shorting would be similar to the shorting of a diode in an IC. Since the isolation diode is right behind the diode being programmed, the programming heat might affect the isolation diode. Too much heat would weaken the isolation diode and increase its chance of failing. However, presently no failure data exist to substantiate this possibility.

6.0 SCREENING

Applicable screening tests for nichrome PROM devices, Ti:W PROM devices, and AIM PROM devices are discussed in this section. Coverage of current screening tests required in the various classes by MIL-STD-883 and MIL-M-38510 specification as well as screening tests required for the memory elements are detailed.

Special Screening Tests for Nichrome PROM Devices

The predecessor of the "freeze-out" test as specified in MIL-M-38510/201 was developed to counteract the nichrome resistor problem that occurred when thin film nichrome were initiated on silicon chips. The failure mechanism, as described in detail in Sections on opening of unprogrammed nichrome fuse links, occurs at low temperatures (between -25 and +20°C) with bias applied to the device. The problem arises when water present inside the package moves onto the nichrome elements through cracks and pinholes in the passivation glass. When normal electrical bias is applied, the nichrome film disintegrates rapidly due to electro-corrosion. The bias potential required to initiate and maintain the reaction varies with the relative purity of the water.

The "freeze-out" test as specified in MIL-M-38510/201 is conducted at temperatures aimed at precipitating any water present in faulty packages by taking the parts through the dew point and applying normal bias at the same time as shown in Figure 55. The reaction, once initiated can occur in a very short time (as little as 5 μs) under the right contaminated water conditions.

Unprogrammed nichrome fuse failure experience and the recent PROM failures due to electro-corrosion have been discussed previously. This continuing failure mode leads to the recommendation that the "freeze-out" test be utilized as a useful and significant screen for the nichrome fuse devices.

A critical factor in preventing unprogrammed nichrome fuse failure is to stop water from reaching the nichrome fuse links. If the passivation layer is truly perfect, water inside the package will never reach the nichrome

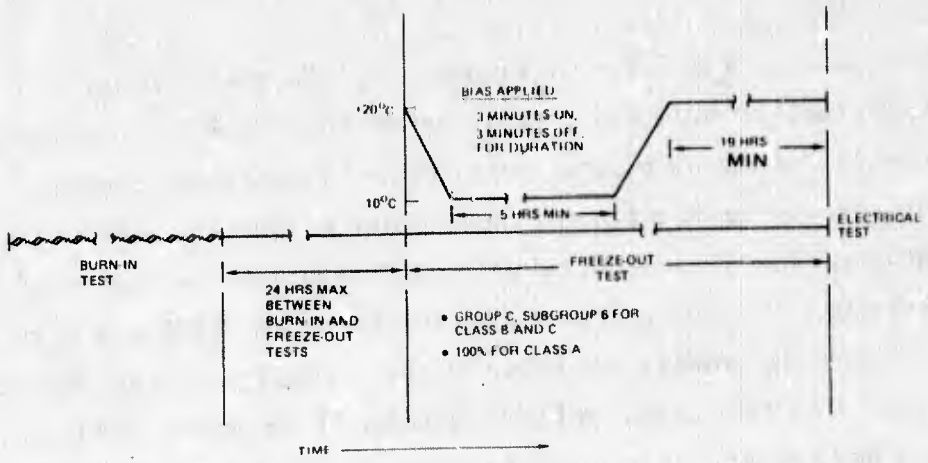

Figure 55. Freeze-out test diagram*

fuses. Double layered passivation, consisting of evaporated SiO and vapor-deposited SiO_2 has been used recently by some IC manufacturers to prevent microcracks and pinholes. Evidence available for this study indicates that PROM suppliers employ only a single layer of passivation. It appears that until the passivation layer is improved by the PROM manufacturers, the "water drop" test as described in MIL-M-38510/201 should be used to detect the presence of pinholes and microcracks in the oxide for Class A devices. Since the integrity of the passivation layer is closely associated with the individual wafer lots, the sampling of the "water drop" test must be accomplished with "wafer" lots identified.

User Q conducted a "freeze-out" test on an extremely small sample (see Appendix A) in which two of the parts were purposely sealed with 40 percent relative humidity atmosphere; no failures occurred. A "water-drop" test was then conducted on these same two parts, and one device failed open after 30 seconds because of cracks in the passivation layer. However, the Al and NiCr were degraded on both parts. It is recommended that tests be performed with sufficient sample sizes to arrive at more definitive conclusions.

It is possible that a cermet is formed when the fuse "blows." Cr/SiO is fairly common type of cermet. When a marginal open occurs that is prone to reconduct (grow back), the gap is in the order of 1/2 a micron across, with

*From Para. 4.3.e of MIL-M-38510/201, 21 August 1972

possibly as low as 4 to 6 K ohm resistance. A small portion of the area might allow the Cr/SiO cermet to be sufficiently metal rich (25 percent SiO, 75 percent Cr) to act as typical cermets in an annealing process. The change in resistance of a typical cermet due to temperature is shown in the family of curves in Figure 56 taken from Bergmann and Sandvik.*

Generally, cermets are annealed to obtain low TCR and trim resistance values. Annealing lowers the value of sheet resistivity and thus total resistance. For this case, only marginally blown fuses in which the gap is extremely narrow are of immediate interest. For a typical cermet, the influence of heat treatment on resistance change is small and rather unpredictable at low temperatures of less than 200°C. At closely controlled temperatures 400° and above, predictable resistivity reductions are obtained. For this case, if the resistance value of a programmed fuse is marginal, (e. g., in the range of 6 or 7 K ohm), the annealing process at 400°C non-operating might reduce the value of the resistance by 45 percent in a 20-minute time period if there is a particular mix of Cr/SiO cermet (75/25) in the gap. Then a change of state to a resistance level that is considered conducting would occur. If this theory is correct, it provides a viable screen to eliminate marginally programmed devices. More important, this annealing process results in stabilizing the cermet of the remaining good devices so that they will not vary in resistance at normal operating temperatures. At Naval Ammunitions Depot, Crane** experiments were conducted above 374°C, which is the Au-Si eutectic temperature of the die attach solder. Damage to all parts resulted. The practical limit for annealing might be 370°C or less depending on the construction of the part. This area still needs further investigation. Some questions to be answered are: Is there really a cermet of some kind in the gap and what is its chemical makeup.

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*S. Bergmann and F. Sandvik, "High Precision Cermet Resistors," Mikroelectronik 5, International Congress on Microelectronics, Munich 1972, published by R. Oldenbourg Verlag, Munich, 1973, pp. 187-198. (Norwegian Institute of Technology, Trondhiem University, Norway)

**Morris L. Robertson, "Evaluation of PROM Devices," Report No. 7024-WJW:dlb, 8200-(158), December 19, 1974, NAD Crane, Indiana.

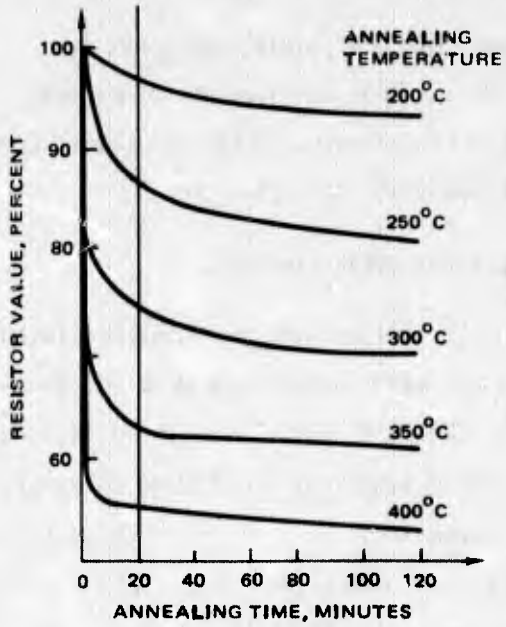


Figure 56. Resistance as function of time (when heated at different temperatures) for a typical cermet.

A determination of anneal time and temperature that would be most useful in stabilizing the cermet resistance must be established. More questions than answers are available at this time.

An additional test is a possibility following burn-in. Some PROM manufacturers have recommended a lower V_{cc} while subjecting the devices to temperature extremes and monitoring the programmed bits. This was not verified by experiment during the study but is recommended for future investigations.

Special Screening Tests for Titanium-Tungsten (Ti:W) Fuse Link Devices

Operating problems related to unscheduled programming (i. e., self programming) during use have been reported for some Ti:W devices. The vendor has initiated a special electrical test to screen out devices with the potential for this inadvertent programming due to leakage currents on 256, 512 and 1024 bit PROMs. A complete programming routine is run on each device but with the output pin ungrounded, thus without actually programming the fuses. If any bit is programmed during this test, that particular device is rejected. This test should be conducted by the vendor on all delivered devices until it is demonstrated that this type of PROM does not have this

failure mode. From available data utilized in this study, no need for additional special screening tests above those of nichrome devices was readily discernible beyond the preceding discussions. The necessity for "freeze-out" and "water-drop" tests has not been determined.

Special Screening Tests for AIM Devices

As a result of user failure data in which temperature sensitive failures occurred, a temperature extreme electrical parameter check after programming is proposed for AIM devices of Class B and Class A of MIL-M-38510. It is proposed that the final electrical tests be modified to dwell at high and low maximum rated operating temperatures for a period of 1 hour and then check the programmed fuses at these temperatures. This is the only additional screen proposed for this type of PROM.

Special Screening Tests for PROMs in General

A number of failed PROMs of other than AIM technology showed multiple bit changes. These were believed to be caused by effects of circuit parameter variations on marginal memory elements. The same test as described for AIM devices would aid in weeding out such incipient failures.

Standard Screening Tests

MIL-STD-883 Method 5004.1 is generally applicable for all PROM devices with some important provisions as to when the tests are conducted with relationship to the programming of the devices. Of course, the Precap visual inspection must be performed before capping--thus before programming. This examination still is the most important to ensure a high degree of reliability and is one of the most effective screens. Fall-out rates of up to 20 percent of IC lots, depending on the workmanship schedule set up by the manufacturer, have been detected; and up to two orders of magnitude of improvement in failure rates have been achieved by precap visual inspection. Thermal cycling, burn-in and final electrical parameter check screens together with the added temperature extreme parametric check to cull out marginal devices, should be conducted after programming the devices.

The screening tests of MIL-STD-883 are based on failure experience data on SSI/MSI devices similar to those in Table 8. More detail is given in Table 9.

The failure categories in Table 8 are translated into broad problem areas in Table 9 column (4). These areas are broken down into the time in the fabrication cycle at which the basic mechanism is tripped (column 7), the failure modes the device exhibits (column 5), and failure mechanisms (column 6). The method of detection (column 1) has been subcolumned into the MIL-STD-883 screening tests plus the "freeze-out", high temperature stress, and "water-drop" tests. The tests that protect the memory element and the remainder circuits are indicated in columns 2 and 3.

Surface flaws represent the largest contributor to IC failure rates in general. PROM devices are included in that population as well. The precap visual screen remains as the most powerful in ridding the population of this type of defect. Included in the general category of surface flaws are slice preparation, passivation, masking, etching and wire bonding (at chip). Stabilization bake, temperature cycling, interim electrical parameter check, burn-in, reverse bias burn-in, mechanical shock, centrifuge, and vibration all contribute to discovery and removal of surface flaw related problems by rejecting affected ICs. In addition, special PROM screens added are "freeze-out" and "water-drop" to detect and remove defective memory portions of

TABLE 8. BIPOLAR FAILURE BREAKDOWN FROM INDUSTRY-WIDE SURVEY - 1970

Failure Category	Percent Contribution
Surface Flaws	34.5
Metallization	22.9
Bonding and Leads	28.8
Design	5.5
Other	5.8
Die	2.5
	100.0

PROM devices, e.g., cracks and pinholes in passivation, mask problems, irregularities in the photo resist patterns, improper removal of oxide (over etch), spotting and contamination.

Metallization and bonding leads are the next largest contributions to IC failure rates. Again the precap visual screen assumes a very important role eliminating such failure mechanism contributors as:

1. Scratched or smeared metallization due to handling
2. Corrosion due to chemical residues
3. Improper bond alignment
4. Excessive loops, sags, or lead length.

Stabilization bake, temperature cycling, mechanical shock, centrifuge, interim electrical parameter checks, burn-in, radiographic, and vibration tests all contribute to screening out defects caused by metallization, bonding and lead categories by removing (rejecting) afflicted ICs.

Other problems such as hermetic seal, loose conducting particles in the package, dislocation and stacking faults, and overbonding/underbonding are screened utilizing hermetic seal test, mechanical shock, vibration, interim electrical parameter check, and vibration for those ICs with the described problems. PROMs with nichrome fuses are protected from nonhermetic packages utilizing "freeze-out" test.

Summary of Screening Recommendations

The following recommendations for special screens were made in the nichrome fuse types:

1. Use "freeze-out" test per MIL-M-38510/201
2. Use "water-drop" test per MIL-M-38510/201 on a wafer lot basis.

Two possible areas of additional investigation for nichrome devices:

1. Modified test after burn-in at temperature extremes (high and low) with lowered V_{cc} while monitoring the programmed bits.
2. Further study related to the possible existence of cermet together with experiments on "annealing" screening tests.

1																
Pre-Cap Visual	Stabilization Bake	Thermal Shock	Temp. Cycling	Mech. Shock	Centrifuge	Hermetic Seal	Interim Electrical Parameter Check	Burn-in	Interim Electrical Parameter Check	Reverse Bias Burn-in	Final Electrical Test	Radiographic	Qualification or Quality Conformance	Vibration	External Visual	"Freeze out"
X			X				X									
X	X		X							X						
X	X		X					X					X			X
X	X		X					X					X			
X							X									
X							X									
X							X									
X							X									X
X							X									
X	X		X					X								X
X	X		X				X	X		X						X
X	X		X	X	X									X		
X			X					X		X						
X	X		X					X								X
X	X		X					X								
	X		X					X								
	X		X				X	X	X							
			X				X	X								
X				X							X			X		
X				X	X									X		
X				X	X			X						X		

TABLE 9. MIL-STD-883 SCREENING TESTS AND PROM FAILURE MODE MATRIX

					2	3	4	5	6	7
Vibration	External Visual	"Freeze-out"	Hi Temp. Stress	"Water Drop"	Memory Element Screen	Non-Memory Element Portion Screen	Problem Category	Failure Mode	Failure Mechanism	Point at Which Reliability-Influencing Variable Is Introduced
						Ni:Cr,AlM, Ti:W	Surface Flaws	Open, possible shorts in subsequent metalization	Cracks, chips, scratches (general handling damage)	Slice Preparation
					AlM	Ni:Cr,AlM, Ti:W	Surface Flaws	Degradation of Junction characteristics	Contamination	Slice Preparation
		X		X	AlM	Ni:Cr, Ti:W	Surface Flaws	Electrical breakdown in oxide layer between metalization and substrate; shorts caused by faulty oxide diffussion mask	Cracks and Pinholes	Passivation
				X	Ni:Cr	Ni:Cr,AlM, Ti:W	Surface Flaws	Low breakdown and increased leakage in the oxide layer	Nonuniform thickness	Passivation
						Ni:Cr,AlM,	Surface Flaws	Opens and/or shorts	Scratches, nicks blemishes in the photo mask	Masking
					AlM		Surface Flaws	Opens and/or shorts	Misalignment	Masking
				X	Ni:Cr	AlM,Ti:W	Surface Flaws	Performance degradation caused by parameter drift; opens or shorts	Irregularities in Photo-resist patterns (line widths, spaces, pin holes)	Masking
		X		X		Ni:Cr,AlM Ti:W	Surface Flaws	Opens and/or shorts or intermittents	Improper removal of oxide	Etching
						Ni:Cr,AlM Ti:W	Surface Flaws	Shorts and/or opens in metalization	Undercutting	Etching
		X		X	Ni:Cr	AlM,Ti:W	Surface Flaws	Potential shorts	Spotting (etch splash)	Etching
		X		X	Ni:Cr	AlM,Ti:W	Surface Flaws	Low Breakdown, Increased Leakage	Contamination (Photo-resist, chemical residue)	Etching
X						Ni:Cr,AlM, Ti:W	Surface Flaws	Open	Cracked or chipped die	Wire—Bonding
						Ni:Cr,AlM Ti:W	Metal-ization	Opens, near open, shorts near shorts	Scratched or smeared metalization (handling	Handling
		X		X		AlM,Ti:W	Metal-ization	Opens in Metalization	Corrosion (Chemical residue)	Metalization Process
						Ni:Cr,AlM Tl:W	Metal-ization	High contact resistance or opens	Misalignment and contaminated contact areas	Metalization Process
						Ni:Cr,AlM Ti:W	Metal-ization	Open metalization due to poor adhesion	Oxide contamination: material incompatibility	Metalization Process
						Ni:Cr,AlM Ti:W	Metal-ization	Open metalization, poor adhesion, or shorts	Improper alloying temperature or time	Metalization Process
						Ni:Cr,AlM Ti:W	Metal-ization	Opens and/or high resistance intra connections	Thin metalization due to insufficient deposition or oxide steps	Thin metalization
X						Ni:Cr,AlM Ti:W	Bonding & Leads	Performance degradation caused by overheating	Voids between header & die	Die Bonding
X						Ni:Cr,AlM Ti:W	Bonding & Leads	Cracked or lifted die	Poor die-to-header bond	Die Bonding
X						Ni:Cr,AlM Ti:W	Bonding & Leads	Opens or shorted bonds	Insufficient bonding-pad areas or spacings	Wire bonding design

(Continued next page)

1																
Pre-Cap Visual	Stabilization Bake	Thermal Shock	Temp. Cycling	Mech. Shock	Centrifuge	Hermetic Seal	Interim Electrical Parameter Check	Burn-in	Interim Electrical Parameter Check	Reverse Bias Burn-in	Final Electrical Test	Radiographic	Qualification or Quality Conformance	Vibration	External Visual	"Free out
X				X	X		X							X		
X							X									
X				X	X							X		X		
X				X	X									X		
X				X	X							X		X		
	X		X		X											
	X		X	X	X									X		
	X		X	X	X									X		
				X				X				X		X		
				X												
X		X	X	X										X		
							X	X	X		X					
							X				X					
							X	X	X		X					
																X
				X	X							X		X		
							X									X
											X					
													X			

(Table 9, continued)

					2	3	4	5	6	7
oration	External Visual	"Freeze-out"	Hi Temp. Stress	"Water Drop"	Memory Element Screen	Non-Memory Element Portion Screen	Problem Category	Failure Mode	Failure Mechanism	Point at Which Reliability-Influencing Variable Is Introduced
X						Ni:Cr,AlM Ti:W	Bonding & Leads	Opens, shorts, or intermittent operation	Improper bonding procedure or control	Wire bonding process
						Ni:Cr,AlM Ti:W	Bonding & Leads	Opens and/or shorts	Improper bond alignment	Wire bonding process
X						Ni:Cr,AlM Ti:W	Bonding & Leads	Shorts to case, substrate, or other leads	Excessive loops, sags, or lead length	Wire bonding process
X						Ni:Cr,AlM Ti:W	Bonding & Leads	Broken leads causing opens or shorts	Nicks, cuts, and abrasions on leads	Wire bonding process
X						Ni:Cr,AlM Ti:W	Bonding & Leads	Shorts or intermittent shorts	Unremoved pigtails	Wire bonding process
						Ti:Cr,AlM Ti:W	Bonding & Leads	Lifted or cracked die	Material mismatch	Die Bonding
X						Ni:Cr,AlM Ti:W	Bonding & Leads	Lifted lead bond	Material incompatibility or contaminated bonding pad	Wire bonding process
X						Ni:Cr,AlM Ti:W	Bonding & Leads	Open Bonds	Plague formation	Wire bonding design
X						Ni:Cr,AlM Ti:W	Bonding & Leads	Performance degradation caused by overheating	Voids between header and die	Die Bonding
						Ni:Cr,AlM Ti:W	Bonding & Leads	Wire weakened & Breaks or intermittent lifted bond; open	Overbonding and underbonding	Wire bonding
X						Ni:Cr,AlM Ti:W	Die	Opens and Potential opens	Improper die separation resulting in cracked or chipped die	Die separation
						Ni:Cr,AlM Ti:W	Die	Degradation of junction characteristics	Dislocations and stacking faults	Crystal slice preparation
						Ni:Cr,AlM Ti:W	Die	Unpredictable component value	Nonuniform resistivities	Crystal slice preparation
						Ni:Cr,AlM Ti:W	Die	Improper electrical performance and/or shorts, opens, etc.	Irregular surface	Crystal slice preparation
		X			Ni:Cr		Disappearing Bit	Open fuse (programmed unintentionally)	Chemical reaction with water in package, contaminants in package	Etching, Passivation, final seal processing
			X		Ni:Cr, Ti:W		Reappearing Bit	Shorted fuse (unprogrammed)	"Grownback" Phenomena	Programming
				X	Ni:Cr		Self Programming	Open Fuse (programmed unintentionally)	Chemical reaction with contaminants in package and added water	Programming
X						Ni:Cr,AlM Ti:W	Other	Intermittent shorts	Loose conducting particles in package	Final seal processing
		X		X		AlM,Ti:W	Other	Performance degradation shorts or opens caused by chemical corrosion or moisture	Poor hermetic seal	Seal
						Ni:Cr,AlM Ti:W	Other	Completely inoperative	Improper marking	Final seal processing
						Ni:Cr,AlM Ti:W	Other	Intermittent shorts	Electrolytic growth of metal or metallic compounds across glass seals between leads or between leads and metal cases	Final seal processing

(Continued next page)

2

1																
Pre-Cap Visual	Stabilization Bake	Thermal Shock	Temp. Cycling	Mech. Shock	Centrifuge	Hermetic Seal	Interim Electrical Parameter Check	Burn-in	Interim Electrical Parameter Check	Reverse Bias Burn-in	Final Electrical Test	Radiographic	Qualification or Quality Conformance	Vibration	External Visual	"Freeze out"
	X		X				X	X	X							
	X		X					X		X						
	X		X			X	X						X			X
															X	

(Table 9, concluded)

					2	3	4	5	6	7
Vibration	External Visual	"Freeze-out"	Hi Temp. Stress	"Water Drop"	Memory Element Screen	Non-Memory Element Portion Screen	Problem Category	Failure Mode	Failure Mechanism	Point at Which Reliability-Influencing Variable Is Introduced
						Ni:Cr,AlM Ti:W	Other	Performance degradation resulting from unstable and faulty passive and active components	Improper control of doping profiles	Diffusion
						Ni;Cr,AlM Ti:W	Other	Performance degradation caused by inversion and channeling	Incorrect atmosphere sealed in packaged	Final seal processing
		X			Ni:Cr	AlM,Ti:W	Other	Shorts and/or opens in the metalization caused by a leak	Cracks, voids in Kovar-to-glass seals	Final seal processing
	X					AlM,Ti:W	Other	Open Circuit	Broken or bent external leads	Final seal processing

2

A special programming screen test was recommended for Ti:W fuse types. No other additional screening tests were recommended for Ti:W fuse types over the normal current MIL-STD-883 IC screening tests. The necessity for "freeze out" and "water drop" tests has not been determined.

A high and low temperature modified final electrical test was proposed for all PROMs after programming, in particular to AIM devices to check for marginally programmed elements.

7.0 PROM FAILURE RATE PREDICTION TECHNIQUE

Introduction

A failure rate prediction technique for PROMs has been developed; its basic foundation is the existing Mil-Hdbk-217B microelectronic failure rate model for ROM devices. The proposed PROM model is composed of two versions:

1. A comprehensive version consisting of factors that requires knowledge of the device's memory element technology and pertinent programming characteristics.
2. A simplex version consisting of a factor that requires a minimal knowledge of the device.

The comprehensive version of the PROM failure rate model is of the following form:

$$\lambda_{PROM} = \lambda_{ROM} + \Delta\lambda_{PROM} \tag{1}$$

where:

λ_{PROM} = overall PROM failure rate

λ_{ROM} = failure rate contribution for the corresponding ROM device

$\Delta\lambda_{PROM}$ = failure rate contribution for the failure mechanisms that are unique to PROM memory elements.

The simplex version of the PROM failure rate model is of the following form:

$$\lambda_{PROM} = K\lambda_{ROM} \tag{2}$$

where:

λ_{PROM} = overall PROM failure rate

λ_{ROM} = failure rate contribution for the corresponding ROM device

K = a scaler multiplier to take into account the failure rate contributions of the failure mechanisms which are unique to PROM memory elements

This section contains a description of both versions of the model, rationale for memory element failure contributions, and quantification of model parameters.

Mil-Hdbk-217B Models

The failure rate model for monolithic microelectronic devices presented in Section 2.1 of Mil-Hdbk-217B is of the basic form:

$$\lambda_p = \lambda_T + \lambda_M$$

where:

λ_p = the overall device failure rate for monolithic devices, e.g., λ_{ROM}

λ_T = the failure rate component due to time degradation causes that represents degradation mechanisms which are accelerated by temperature and electrical bias; composed largely of phenomena which follow the Arrhenius type rate acceleration

λ_M = the failure rate component due to mechanical (application environment) causes, and represents failure mechanisms resulting from mechanical stress directly or indirectly (such as stresses set up by thermal expansion)

The terms λ_T and λ_M are of the form:

$$\lambda_T = \pi_Q \pi_L C_1 \pi_T$$

$$\lambda_M = \pi_Q \pi_L C_2 \pi_E$$

where:

π_Q = quality factor (Table 2.1.5-1 of Mil-Hdbk-217B)

π_L = learning factor (Table 2.1.5-2 of Mil-Hdbk-217B)

π_T = temperature acceleration factor (Table 2.1.5-4 of Mil-Hdbk-217B)

C_1, C_2 = device complexity factors (Table 2.1.5-8 of Mil-Hdbk-217B for memories)

The model can be written in the following form:

$$\lambda_p = \pi_Q \pi_L (C_1 \pi_T + C_2 \pi_E) \tag{3}$$

The parameters π_Q, π_L and π_E are functions of the device screening, manufacturer's learning and operating environmental conditions, respectively. The parameter π_T, the temperature acceleration factor, is a function of the device junction temperature as well as the device technology (i.e., MOS or bipolar) as shown by the following relationship:

$$\pi_T = Ae^{-\frac{E_a}{K}\left(\frac{1}{T_J} - \frac{1}{298}\right)}$$

where:

A = constant

E_a = activation energy

K = Boltzmann's constant (0.86171×10^{-4} eV/°K)

T_J = device junction temperature (degrees Kelvin)

The value of the activation energy, E_a, is determined by the device technology. If the device is fabricated utilizing bipolar technology, then $E_a = 0.4131$ eV. E_a is assumed to be independent of temperature, a condition that is generally true if the temperature range is not too large.

The temperature acceleration factor π_T is a factor only of the first term λ_T, and the environmental multiplier π_E is a factor only of the second term λ_M. The implication of the model is that application environment affects only mechanical causes, and not time degradation causes, whereas device operating temperature affects only time degradation causes and not mechanical.

As mentioned previously, the microelectronic failure rate model is applicable to all monolithic ICs. The complexity factors, C_1 and C_2, are the only parameters within the model that vary with increasing device complexity. The quantification of these factors is summarized in Table 10.

TABLE 10. MIL-HDBK-217B COMPLEXITY FACTORS

Device Type*	Complexity Factors** ($F/10^6$ Hours)	
	C_1	C_2
Digital (SSI/MSI)	$1.29(10^{-3})(N_G)^{0.677}$	$3.89(10^{-3})(N_G)^{0.359}$
Digital (LSI)	$0.0187e^{(0.00471)N_G}$	$0.013e^{(0.00423)N_G}$
Memory (ROMS)	$0.00114(B)^{0.603}$	$0.00032(B)^{0.646}$

*Only monolithic bipolar digital devices are listed.

**The following definitions are given:

N_G = number of gates

B = number of bits

e = natural logarithm base, 2.718

Physics of Failure Modeling

As mentioned previously, the failure rate prediction technique that has been developed for PROMs utilizes the existing Mil-Hdbk-217B ROM failure rate math model as a basic foundation. This approach was selected since PROM devices are, in essence, ROM devices with additional circuitry to incorporate provisions for programming. That is, PROMs possess the failure mechanisms of ROMs, in addition to those failure mechanisms that are unique to their memory elements.

Basically, the circuitry that has been added to the ROM structure to facilitate programming is composed of:

1. Programming circuitry that is utilized in the programming of selected bits within the memory matrix.
2. Test fuses that indicate the programmability of the PROM chip.
3. Memory matrix elements, e.g., fuses, which are blown or remain unblown, depending on the programming requirements.

An analysis was performed on the three items listed above as to their relative impact on PROM reliability. The results of the analysis indicate that only the third item significantly affects PROM reliability. Some of the failure mechanisms related to PROM memory elements are felt to be sufficiently significant for incorporation into the model.

Under this study, three PROM types were considered:

1. Nichrome fuse link
2. Titanium-tungsten fuse link
3. AIM memory element.

The failure mechanisms of each memory element type shown above and justification for their incorporation into or exclusion from the model are discussed below.

Nichrome Fuse Link – As mentioned in the section on Reliability Physics of Memory Elements, the two most significant failure modes for nichrome fuse links are

1. The opening of unprogrammed nichrome fuse links
2. The reconduction of programmed nichrome fuse links.

The opening of unprogrammed nichrome fuse links, commonly referred to as the disappearing resistor problem, appears to the sense circuit as a high resistance. This change in resistance, from approximately 350Ω in the unprogrammed state to as high as 1 MΩ, is generally the result of electro-corrosion activity on the nichrome fuse link. Because the nichrome alloy has a low resistance to corrosion, this failure mechanism is felt to be significant, and therefore has been incorporated into the model.

The occurrence of this phenomenon can be reduced, however, by subjecting the PROM device to a "freeze-out" test. A discussion of the effects of this test on reliability has been covered in an earlier section.

The reconduction of programmed nichrome fuse links, commonly referred to as "grow-back," appears to the sense circuit as a low resistance. This change of resistance is a result of changes in conductivity in the fuse gap region. Because this failure mechanism can still be quite prevalent, it is felt to be significant and, therefore, has been incorporated into the model.

The occurrence of this phenomenon can be reduced, however, by subjecting the PROM device to a dynamic, maximum rated temperature burn-in. The effects of this test on reliability have been discussed in a previous section.

Titanium-Tungsten – Similar to nichrome, the two possible failure mechanisms for titanium-tungsten fuse links are

1. The opening of unprogrammed titanium tungsten fuse links
2. The reconduction of programmed titanium tungsten fuse links.

The opening of unprogrammed titanium tungsten fuse links is similar to the phenomena described for nichrome. Relative to this phenomenon, however, the titanium tungsten fuse links differ from the nichrome fuse link in two respects. First, the titanium tungsten fuse link is approximately two to three times thicker. The titanium tungsten fuse link is generally 800 to 1000 Å thick, while the nichrome fuse link is 150 to 250 Å thick. Second, the

titanium tungsten alloy, by the very nature of its composition, has a higher resistance to corrosion. For these two reasons, it is felt that the titanium tungsten fuse link is less susceptible to electrocorrosive activity but still subject to oxidation. However, the probability for such failures to occur has not been quantified.

The reconduction of programmed titanium tungsten fuse links is similar to the phenomenon described for nichrome. The conductive properties of the fuse gap region changes, allowing additional current to flow. Because of the high melting point of Ti:W, permanent reconducting even after an electrical breakdown of the open gap appears unlikely. Failure data collected thus far have not shown titanium tungsten to be susceptible to this failure mechanism. However, quantitative data are still lacking.

AIM Memory Elements – As mentioned in the sections for Reliability Physics of Memory Elements, the failure possibilities for AIM memory elements are

1. The shorting of unprogrammed AIM diode elements
2. The opening of programmed AIM diode elements
3. The shorting of the isolation diode (after programming stresses).

It should be noted that the failure mechanisms characteristic of AIM technology are not unique to PROMs. The breakdown of active element junctions are present in typical monolithic devices. This characteristic is certainly different from the two memory elements described previously. Since the AIM memory elements are additional to the basic ROM structure, and provide additional failure potential, their failure mechanisms have been incorporated into the model.

The Proposed PROM Failure Rate Models

The prediction technique which has been developed for PROMs is composed of two versions:

1. A comprehensive version of the form:

$$\lambda_{PROM} = \lambda_{ROM} + \Delta\lambda_{PROM}$$

2. A simplex version of the form:

$$\lambda_{PROM} = K\lambda_{ROM}$$

These expressions utilize the existing Mil-Hdbk-217B ROM failure rate model, which is represented by the term λ_{ROM}, as a basic foundation. The term λ_{PROM} and K are defined and quantified here for the comprehensive and simplex versions respectively.

Comprehensive Version of PROM Math Model – The comprehensive version of the PROM failure rate model incorporates provisions to account for the failure mechanisms unique to PROM memory elements. The subsection on Physics of Failure Modeling described the inherent failure mechanisms for memory elements of different types. Those failure mechanisms that were significant enough for inclusion into the model are summarized in Table 11.

TABLE 11. FAILURE MECHANISMS FOR THREE MEMORY ELEMENT TYPES

PROM Memory Element Type	Failure Mode of Memory Element			
	(1) Disappearing Fuse Link	(2) Reappearing Fuse Link	(3) Shorted Diode	(4) Opened Diode
Nichrome	Yes	Yes		
Titanium Tungsten	⊛	⊛		
AIM			Yes	Yes**

**Including either the memory diode or the isolation diode failure after stressed by programming.

The failure modes of the nichrome fuse link, (1) disappearing fuse link and (2) reappearing fuse link, are represented by columns (1) and (2),

respectively. Titanium tungsten's susceptibility to such failure modes has not been determined because of insufficient data as denoted by the ⊠ in the table. The failure modes of the AIM type memory element, (1) the shorting of unprogrammed memory elements and (2) the opening of programmed memory elements, are represented by columns (3) and (4), respectively.

The failure rate contributions for the four failure mode categories characterized in Table 11 are denoted below:

λ_{DFL} = failure rate contribution for the disappearing fuse link phenomenon

λ_{RFL} = failure rate contribution for the reappearing (or reconducting) fuse link phenomenon

λ_{SD} = failure rate contribution for the shorting of unprogrammed AIM memory diodes

λ_{OD} = failure rate contribution for the opening of programmed AIM memory diodes or isolation diode failures after programming

Since the four terms listed above represent the failure rate contribution for the failure modes that are unique to PROM memory elements, the following expression is obtained:

$$\Delta\lambda_{PROM} = \lambda_{DFL} + \lambda_{RFL} + \lambda_{SD} + \lambda_{OD} \tag{4}$$

Utilizing Equations (3) and (4), Equation (1) may be written in the following form:

$$\lambda_{PROM} = \pi_Q \pi_L (C_1 \pi_{T1} + C_2 \pi_E) + \lambda_{DFL} + \lambda_{RFL} + \lambda_{SD} + \lambda_{OD} \tag{5}$$

The expressions which comprise the term $\Delta\lambda_{PROM}$ are now considered individually by defining and quantifying the factors contained therein.

The Disappearing Fuse Link Term λ_{DFL} – The term λ_{DFL} has been incorporated into the model to account for the phenomenon of a resistor fuse link opening.

The following items influence unprogrammed fuse link reliability:

1. Device quality level
2. Manufacturer's production experience
3. Device temperature
4. Application environment.

The items listed above have been considered in the development of λ_{DFL}:

$$\lambda_{DFL} = C_3 \pi_Q \pi_L \pi_{T3} \pi_E \pi_{FM1} \tag{6}$$

where:

C_3 = complexity factor for the disappearing fuse link phenomenon

π_Q = quality factor

π_L = manufacturer's learning factor

π_{T3} = temperature acceleration factor for unprogrammed fuse links

π_E = application environment factor

π_{FM1} = the failure mechanism factor

The expression for λ_{DFL}, a multiplicative model, is based on the convention adopted by the RADC Notebook and Mil-Hdbk-217B for resistor failure rates. Each parameter within λ_{DFL} is considered individually here; information concerning its function and quantification are also given.

C_3 – Complexity Factor

The complexity factor, C_3, is a linear function that relates the number of unprogrammed fuse links to the normalized failure rate contribution for the disappearing resistor phenomena. The value of C_3 is obtained from the following equation:

$$C_3 = (\lambda_{FL})_{UNP} \cdot (N_{FL})_{UNP} \tag{7}$$

where:

C_3 = normalized failure rate contribution for the unprogrammed fuse link memory matrix

$(\lambda_{FL})_{UNP}$ = normalized failure rate for an unprogrammed fuse link

$(N_{FL})_{UNP}$ = number of unprogrammed fuse links in memory matrix

The value for the normalized failure rate of an unprogrammed fuse link, $(\lambda_{FL})_{UNP}$ was calculated utilizing the failure data collected from PROM users. The development of the formula that was utilized to calculate the value of $(\lambda_{FL})_{UNP}$ in addition to its application to the PROM failure data is given below.

Substituting the general form of the complexity factor, C_3, Equation (7), into the expression for λ_{DFL} yields:

$$\lambda_{DFL} = [(\lambda_{FL})_{UNP} \cdot (N_{FL})_{UNP}](\pi_Q \pi_L \pi_{T3} \pi_E \pi_{FM1}) \quad (8)$$

The term $(N_{FL})_{UNP}$, the number of unprogrammed fuse links in the memory matrix is simply:

$$(N_{FL})_{UNP} = (P_{FL})_{UNP} \cdot N_{FL}$$

where:

$(N_{FL})_{UNP}$ = the number of unprogrammed fuse links in the memory matrix

$(P_{FL})_{UNP}$ = the percentage of unprogrammed fuse links in the memory matrix

N_{FL} = the number of fuse links (or bits) in the memory matrix

To quantify $(\lambda_{FL})_{UNP}$ from test data the following mathematical manipulation is required.

Substituting the above expression into Equation (8) and solving for $(\lambda_{FL})_{UNP}$ gives

$$(\lambda_{FL})_{UNP} = \frac{\lambda_{DFL}}{[(P_{FL})_{UNP} \cdot N_{FL}](\pi_Q \pi_L \pi_{T3} \pi_E \pi_{FM1})} \tag{9}$$

Noting that the term λ_{DFL}, the failure rate contribution for the disappearing fuse link phenomenon, is equivalent to the number of device failures, f, divided by the number of device hours, t, or,

$$\lambda_{DFL} = f/t$$

then Equation (9) may be rewritten as

$$(\lambda_{FL})_{UNP} = \frac{f/t}{[(P_{FL})_{UNP} \cdot N_{FL}](\pi_Q \pi_L \pi_{T3} \pi_E \pi_{FM1})} \tag{10}$$

For multiple data sources the generalized form for $(\lambda_{FL})_{UNP}$ is

$$(\lambda_{FL})_{UNP} = \frac{\sum_{i=1}^{n} f_i}{\sum_{i=1}^{n} \left(t_i \left[(P_{FL})_{UNP_i} \cdot N_{FL_i} \right] \cdot \left(\pi_{Q_i} \pi_{L_i} \pi_{T3_i} \pi_{E_i} \pi_{FM1_i} \right) \right)} \tag{11}$$

where:

$(\lambda_{FL})_{UNP}$ = normalized failure rate for an unprogrammed fuse

f_i = number of failures for the i^{th} data source

t_i = number of device hours for the i^{th} data source

$(P_{FL})_{UNP_i}$ = the percentage of unprogrammed fuse links in the memory matrix for the i^{th} data source

N_{FL_i} = the number of fuse links (or bits) in the memory matrix for the i^{th} data source

$\pi Q_i \pi L_i \pi T3_i \pi E_i \pi FM1_i$ = normalizing factor for the i^{th} data source

The PROM failure data collected thus far, pertaining to the opening of unprogrammed fuse links, are presented in Table 12 and categorized (according to columns) as follows:

1. The source of data
2. The number of fuse links in the memory matrix, N_{FL}
3. The percentage of the memory matrix that is unprogrammed, $(P_{FL})_{UNP}$
4. The number of devices
5. The number of device hours, t
6. The number of failed devices as a result of an opened fuse link, f
7. The quality class of the device, π_Q
8. The manufacturer's production experience, π_L
9. The device ambient temperature, π_{T3}
10. The device application environment, π_E
11. The failure mechanism factor 1, π_{FM1}
12. The normalizing factor $\pi_Q \pi_L \pi_{T3} \pi_E \pi_{FM1}$
13. The quantity of normalized unprogrammed bit hours, $t \times [(P_{FL})_{UNP} \cdot N_{FL}] \times \pi_Q \pi_L \pi_{T3} \pi_E \pi_{FM1}$

The normalizing factor $\pi_Q \pi_L \pi_{T3} \pi_E \pi_{FM1}$ contained in column 12 is calculated by taking the product of the factors π_Q, π_L, π_{T3}, π_E and π_{FM1}, whose values are found in columns (7), (8), (9), (10) and (11), respectively. The values for the five π factors were extracted from tables shown later in the text and were used to normalize the failure data to the following conditions:

1. Quality level: Mil-M-38510, Class A (Jan)
2. Manufacturer's learning level: Mature

TABLE 12. PROM FAILURE DATA PERTAINING TO THE DISAPPEARANCE OF AN UNPROGRAMMED NICHROME FUSE LINK

(1) User Source of Data	(2) Device Size (Bits)	(3) Percent of Memory Element Unprog'd	(4) Number of Devices	(5) Number of Device Hours	(6) Number of Memory Element Failures	Math Model Parameters										(12) Normalizing Factor	(13) Normalized Unprogrammed Bit Hours (10^{12})
						(7) Quality		(8) Manufacturer's Learning		(9) Ambient Temperature		(10) Application Environment		(11) Failure Mechanism			
	N_{FL}	$(P_{FL})_{UNP}$		t	f	Class	π_Q	Status	π_L	(°C)	π_{T3}	Symbol	π_E	Type	π_{FMI}	$\pi_Q \pi_L \pi_{T3} \pi_E \pi_{FMI}$	$t \times [(P_{FL})_{UNP} \cdot N_{FL}] \times \pi_Q \pi_L \pi_{T3} \pi_E \pi_{FMI}$
1	1024	50	29,000	76,000,000	0	D	150	Mature	1	25	1.00	G_B	0.2	DFL	1	30.0	1,167,360
2	512	50	600	5,256,000	0	B	2	Mature	1	25	1.00	G_F	1.0	DFL	1	2.0	0.002,691
3	512	50	3,816	418,500	0	B-1	5	Mature	1	25	1.00	G_F	1.0	DFL	1	5.0	0.000,536
4	512	50	540	180,000	0	B-1	5	Mature	1	50	1.27	A_I	4.0	DFL	1	25.4	0.001,170
5	2048	50	384	2,521,344	0	D	150	Mature	1	38	1.13	G_F	1.0	DFL	1	169.5	0.437,625
				Total	0												Total 1,609,382

3. Temperature: $T_A = 25^{\circ}C$
4. Environment: Ground fixed
5. Failure Mechanism Factor 1: Nichrome fuse links

When the data contained in Table 12 are applied to Equation (11) the maximum likelihood and unbiased estimate of $(\lambda_{FL})_{UNP}$ is given by:

$$(\lambda_{FL})_{UNP} = \frac{\sum_{i=1}^{n} f_i}{\sum_{i=1}^{n} \left(t_i \left[(P_{FL})_{UNP_i} \times N_{FL_i} \right] \cdot \left(\pi Q_i \pi L_i \pi T3_i \pi E_i \pi FM1_i \right) \right)}$$

$$= \frac{0}{1.609,382 \times 10^{12}} = 0$$

This estimate is usually considered to be the unbiased value derived by the maximum likelihood method. This estimate does not reflect the common sense judgment that a non-zero failure rate really does exist, but the test time, by chance, has been too short to exhibit a failure event. For a point estimate of $(\lambda_{FL})_{UNP}$, the assumption of one third a failure, i.e.,

$$\sum_{i=1}^{n} f_i = 0.3 ,$$

might be utilized. This estimate is based on Bayesian statistics and other estimates.*

*E. L. Welker and M. Lipow, "Estimating the Exponential Failure Rate from Data with No Failure Events," Proceedings of the 1974 Annual Reliability and Maintainability Symposium," pp. 420-427.

Therefore,

$$(\lambda_{FL})_{UNP} = \frac{0.3}{1.609,382 \times 10^{12}}$$

$$(\lambda_{FL})_{UNP} = 0.186 \text{ failures}/10^{12} \text{ hours}$$

The two-sided lower and upper confidence limits (based on the χ^2 distribution) for r failures in the gamma prior using the Poisson failure model is

$$\frac{\chi^2\left(\frac{\alpha}{2} ; 2r\right)}{2T} \leq (\lambda_{FL})_{UNP} \leq \frac{\chi^2\left(\frac{\alpha}{2} ; 2r + 2\right)}{2T}$$

where:

r = number of failures, $\sum_{i=1}^{n} f_i$

T = test time, $\sum_{i=1}^{n} \left(t_i \left[(P_{FL})_{UNP_i} \times N_{FL} \right] \times \left(\pi Q_i \pi L_i \pi T3_i \pi E_i \pi FM1_i \right) \right)$

For a 50 percent two sided confidence limits with 0 failures, the lower limit is 0 and the upper limit is

$$\frac{1}{2} \chi^2\left(\frac{\alpha}{2} ; 2r + 2\right) = 1.386$$

Therefore,

$$\frac{0}{1.609,382 \times 10^{12}} \leq (\lambda_{FL})_{UNP} \leq \frac{1.386}{1.609,382 \times 10^{12}}$$

$$0 \leq (\lambda_{FL})_{UNP} \leq 0.861 \text{ (failures}/10^{12} \text{ hours)} \qquad (12)$$

π_Q – Quality Factor

The quality factor, π_Q, considers the device quality class and reflects its relative impact on unprogrammed fuse link reliability. See Table 13.

TABLE 13. QUALITY FACTOR, π_Q

Quality Level or Screen Class	Description	π_Q
A	Mil-M-38510, Class A (JAN)	1
B	Mil-M-38510, Class B (JAN)	2
B-1	Mil-Std-883, Method 5004, Class B	5
B-2	Vendor Equivalent of Mil-Std-883, Method 5004, Class B	10
C	Mil-M-38510, Class C (JAN)	16
D	Commercial (or non-mil standard) part, with no screening beyond the manufacturer's regular quality assurance practices. The indicated π_Q value represents an average for all grades of commercial parts	150

Water is one major component required for initiating the phenomenon that results in the opening of an unprogrammed fuse links. The presence of water within a package is usually the result of one of the following:

1. Water locked within the SiO_2 layer during fabrication
2. Humidity locked within the package during the sealing process
3. Loss of integrity of the package seal

It should be noted that before items 2 and 3 can contribute to the failure of an unprogrammed fuse link, cracks or pinholes must be present in the passivation. Water exterior to the chip requires a transport mechanism through the passivation to attack the resistor fuse links.

As recommended in the previous section on screening, tests such as the "freeze out" and "water drop" should be used per Mil-M-38510/201 procedures. Table 13, which was extracted from Table 2.1.5-1 of Mil-Hdbk-217B,

reflects the relative impact of the device screening class on unprogrammed fuse link reliability.

π_L – Learning Factor

The learning factor, π_L, considers the PROM manufacturer's design and process status and relates their relative effects on unprogrammed fuse link reliability.

When a semiconductor manufacture is in the early production phase of a PROM device or if there has been a modification in an existing design or process, additional reliability risks are incurred. Possible abnormalities in the deposition of the fuse link material on the SiO_2 substrate are the cause. A certain amount of time is required of the semiconductor manufacturer to optimize his design and/or process of resistor fuse links. Since the above relationship significantly affects the overall PROM device reliability, the manufacturer's learning factor, π_L has been incorporated into the term λ_{DFL}. The quantification of π_L is based on a similar factor delineated in Table 2.1.5.2 of Mil-Hdbk-217B, since it is felt that their relative impact on reliability is equivalent. The values for π_L are presented in Table 14.

TABLE 14. π_L, LEARNING FACTOR

1. The learning factor π_L is 10 under any of the following conditions:

   a. New device in initial production

   b. Where major changes in design or process have occurred

   c. Where there has been an extended interruption in production or a change in line personnel (radical expansion)

2. The factor of 10 can be expected to apply until conditions and controls have stabilized. This period can extend for as much as 6 months of continuous production.

   π_L is equal to 1.0 under all production conditions not stated in a, b, and c, above.

π_{T3} – Temperature Acceleration Factor

The temperature acceleration factor is an exponential function that considers the device operating ambient temperature and reflects its relative impact on unprogrammed fuse link reliability. The value of π_{T3} obtained from

$$\pi_{T3} = 0.0585e^{\left(\frac{T + 273}{105}\right)} \tag{13}$$

where:

π_{T3} = temperature acceleration factor for unprogrammed resistor fuse links

T = device ambient temperature (degrees C)

The value of π_{T3} can also be determined from Figure 57. The derivation of this expression is as follows.

Since the failure mechanism characteristic of unprogrammed fuse links is generally the result of chemical activity, it is accelerated by higher

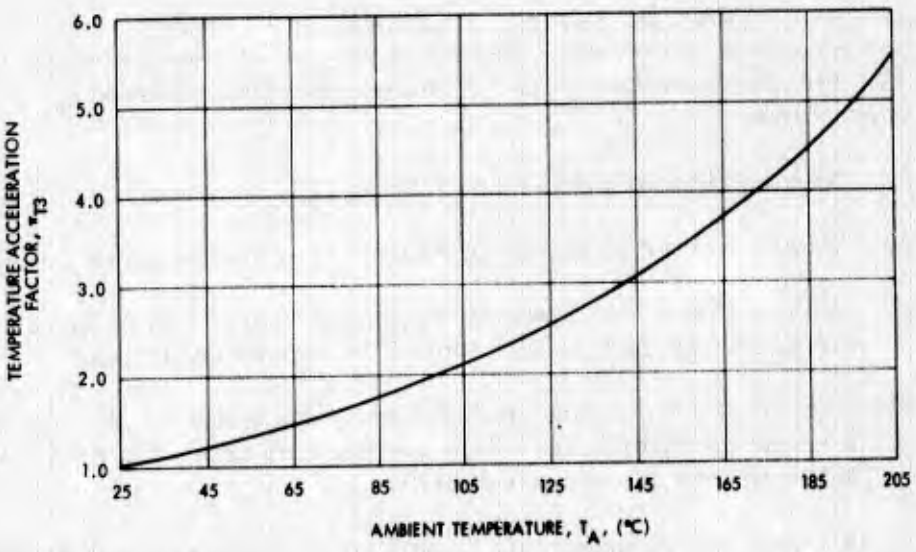


Figure 57. π_{T3} versus ambient temperature.

temperatures. Insufficient data are available, however, to quantify the relative reliability effect of unprogrammed fuse links with increasing temperature. Therefore, an approximation must be developed.

It is believed that the temperature acceleration factor that is derived by utilizing the base failure rate, λ_b, for metal film resistors (type Mil-R-10509), approximates the relationship described above. The base failure rate for metal film resistors (taken from section 2.5 of Mil-Hdbk-217B) is as follows:

$$\lambda_b = (1 \times 10^{-4}) e^{3.5\left(\frac{T + 273}{398}\right)} S^{\left(\frac{T + 273}{273}\right)}$$

where:

λ_b = base failure rate ($F/10^6$ hours)

T = ambient temperature (^oC)

S = electrical stress

An approximation to the temperature acceleration factor for unprogrammed fuse links, π_{T3}, is obtained when the following operation is performed:

$$\pi_{T3} = \frac{\lambda_b(\text{T degrees at 20 percent stress})}{\lambda_b(\text{25 degrees at 20 percent stress})}$$

$$\pi_{T3} = 0.0585 e^{\left(\frac{T + 273}{105}\right)}$$

π_E – Application Environment Factor

The application environment factor considers the device operating environment and reflects its relative impact on the unprogrammed fuse link reliability.

As mentioned previously, the presence of water within the PROM package poses as a potential threat to the reliability of unprogrammed fuse links. The presence of water, in many ways, is determined by the environment in which the device is operating.

For example, if a PROM device is subjected to a sub-freezing environment, condensation of water within the silicon substrate of the chip might occur, resulting in the potential electro-corrosion of resistor fuse links.

Also, consider the situation in which a PROM device is subjected to severe environments possibly resulting in the degradation of the package. One result could be the introduction of water into the package and the possible attack of the resistor fuse links through cracks or pinholes in the passivation.

It is believed that the π_E values presented in Table 2.1.5-3 of Mil-Hdbk-217B give reasonable approximation to the relative severity of the corresponding application environment with respect to the unprogrammed fuse link reliability. This table is reproduced here as Table 15.

TABLE 15. APPLICATION ENVIRONMENT FACTOR π_E

Application Environment	Symbol	π_E
Ground, Benign	G_B	0.2
Space Flight	S_F	0.2
Ground, Fixed	G_F	1.0
Airborne, Inhabited	A_I	4.0
Naval, Sheltered	N_S	4.0
Ground, Mobile	G_M	4.0
Airborne, Uninhabited	A_U	6.0
Naval, Unsheltered	N_U	5.0
Satellite or Missile Launch	M_L	10.0

Failure Mechanism Factor, π_{FM1}

In Table 11 it was indicated that not all PROM technologies are applicable to the disappearing fuse phenomenon. To account for this, the failure mechanism factor 1, π_{FM1}, has been incorporated into the model to allow the term λ_{DFL} to equal zero when applicable. The value of π_{FM1} is obtained from Table 16.

TABLE 16. FAILURE MECHANISM FACTOR 1, π_{FM1}

Memory Element Technology	π_{FM1}
Nichrome	1
Titanium Tungsten	*
AIM	0

The values contained within Table 16 indicate the applicability of each memory element type that has been studied thus far to the disappearing fuse phenomenon. The values for π_{FM1} are defined below:

π_{FM1} = 1: The failure data obtained to date indicate that this memory element type is susceptible to the disappearing fuse link phenomenon

π_{FM1} = 0: The failure data obtained to date indicate that this memory element type is not susceptible to the disappearing fuse link phenomena (or that this phenomenon is not applicable)

π_{FM1} = *: The failure data obtained to date are inconclusive with regard to this memory element's susceptibility to the disappearing fuse link phenomenon

The Reappearing Fuse Link Term, λ_{RFL} – The term, λ_{RFL}, has been incorporated into the model to account for the phenomenon of a programmed fuse link changing back to the unprogrammed state.

It has been determined that the following items influence programmed resistor fuse link reliability:

1. Temperature
2. Programming time
3. Programmer's learning
4. Quality screening level
5. Voltage applied across an open fuse.

The factors listed above have been considered in the definition of λ_{RFL}:

$$\lambda_{RFL} = C_4 \pi_Q \pi_L \pi_{T4} \pi_{PL} \pi_{PT} \pi_{FM2} \qquad (14)$$

where:

C_4 = complexity factor for the reappearing fuse link phenomenon

π_Q = quality factor

π_L = manufacturer's learning factor

π_{T4} = temperature acceleration factor for programmed fuse links

π_{PL} = programmer's learning factor

π_{PT} = programming time factor

π_{FM2} = failure mechanism factor

The form of λ_{RFL}, a multiplicative model, is based on the convention adopted by the RADC Notebook and Mil-Hdbk-217B for resistor failure rates. Each parameter within λ_{RFL} is considered individually here. Information concerning its function, quantification and rationale behind its quantification is also given.

C_4 – Complexity Factor

The complexity factor C_4, is a linear function that relates the number of programmed fuse links to the normalized failure rate contribution for the reappearing resistor phenomenon.

The value for C_4 is obtained from

$$C_4 = \left(\lambda_{FL}\right)_P \cdot \left(N_{FL}\right)_P, \tag{15}$$

where:

C_4 = normalized failure rate contribution for the programmed fuse link memory matrix

$\left(\lambda_{FL}\right)_P$ = normalized failure rate for a programmed fuse link

$\left(N_{FL}\right)_P$ = number of programmed fuse links in memory matrix

The value for the normalized failure rate of a programmed fuse link, $\left(\lambda_{FL}\right)_P$ was calculated utilizing the formula denoted by Equation (16) and the failure data collected from PROM users. The development of Equation (16) is not shown here since it is very similar to that for $\left(\lambda_{FL}\right)_{UNP}$ which was described earlier.

$$\left(\lambda_{FL}\right)_P = \frac{\sum_{i=1}^{n} f_i}{\sum_{i=1}^{n}\left(t_i\left[\left(P_{FL}\right)_{P_i} \cdot N_{FL_i}\right]\left(\pi Q_i \pi L_i \pi T4_i \pi PL_i \pi PT_i \pi FM2_i\right)\right)} \qquad (16)$$

where:

$\left(\lambda_{FL}\right)_P$ = normalized failure rate for a programmed fuse link

f_i = number of failures for the i^{th} data source

t_i = number of device hours for the i^{th} data source

$\left(P_{FL}\right)_{P_i}$ = the percentage of programmed fuse links in the memory matrix for the i^{th} data source

N_{FL_i} = the number of fuse links (or bits) in the memory matrix for the i^{th} data source

$\pi Q_i \pi L_i \pi T4_i \pi PL_i \pi PT_i \pi FM2_i$ = normalizing factor for the i^{th} data source

The PROM failure data collected thus far, pertaining to the reconduction of programmed fuse links are presented in Table 17 and categorized (according to columns) as follows:

1. The source of data
2. The number of fuse links in the memory matrix, N_{FL}
3. The percentage of the memory matrix that is programmed, $\left(P_{FL}\right)_P$
4. The number of devices

5. The number of device hours, t
6. The number of failed devices as a result of reconnected fuse links, f
7. The quality class of the device, π_Q
8. The manufacturer's production experience, π_L
9. The device ambient temperature, π_{T4}
10. The programmer's learning factor, π_{PL}
11. The programming time factor, π_{PT}
12. The failure mechanism factor 2, π_{FM2}
13. The normalizing factor, $\pi_Q \pi_L \pi_{T4} \pi_{PL} \pi_{PT} \pi_{FM2}$
14. The quantity of normalized programmed bit hours,
$$t \times \left[\left(P_{FL}\right)_P \times N_{FL}\right] \times \pi_Q \pi_L \pi_{T4} \pi_{PL} \pi_{PT} \pi_{FM2}$$

The normalizing factor $\pi_Q \pi_L \pi_{T4} \pi_{PL} \pi_{PT} \pi_{FM2}$ contained within column 13 is calculated by taking the product of the factors $\pi_Q \pi_L \pi_{T4} \pi_{PL} \pi_{PT}$ and π_{FM2}, whose values are found within columns (7), (8), (9), (10), (11) and (12), respectively. The values for the six π-factors were extracted from tables shown later in the text and were used to normalize the failure data to the following conditions:

1. Quality level: Mil-M-38510, Class A (JAN)
2. Manufacturer's learning level: Mature
3. Temperature: $T_A = 25^{\circ}C$
4. Programmers learning level: Mature
5. Programming time: 10 ms
6. Failure mechanism Factor 2: nichrome fuse links

When the data contained within Table 17 are applied to Equation (16) the maximum likelihood and unbiased estimate of $\left(\lambda_{FL}\right)_P$ is given by

$$\left(\lambda_{FL}\right)_P = \frac{\sum_{i=1}^{n} f_i}{\sum_{i=1}^{n}\left(t_i\left[\left(P_{FL}\right)_{P_i} \cdot N_{FL_i}\right]\left(\pi_{Q_i}\pi_{L_i}\pi_{T4_i}\pi_{PL_i}\pi_{PT_i}\pi_{FM2_i}\right)\right)}$$

(1) User Source of Data	(2) Device Size (Bits)	(3) Percent of Memory Element Programmed	(4) Number of Devices	(5) Number of Device Hours	(6) Number of Memory Element Failures	Math Model Parame							
						(7) Quality		(8) Manufacturer's Learning		(9) Ambient Temperature		(10) Programmer Learnin	
	N_{FL}	$(P_{FL})_P$		t	f	Class	π_Q	Status	π_L	(°C)	π_{T4}	Status	π
1	1024	50	29,000	76,000,000	26	D	150	Mature	1	25	1.00	Mature	
2	512	50	600	5,256,000	0	B	2	Mature	1	25	1.00	Mature	
3	1024	50		4,945,152	13	B-2	10	Mature	1	25	1.00	Mature	
4	512	50	3,816	418,500	0	B-1	5	Mature	1	25	1.00	Early	1
5	512	50	540	180,000	0	B-1	5	Mature	1	50	1.23	Early	1
6	2048	50	384	2,521,344	0	D	150	Mature	1	38	1.09	Mature	
				Total	39								

*This assumes that:

1. 1 ms average time to program corresponds to programming with a 20 ms pulse.
2. 5 ms average time to program corresponds to programming with a 200 ms pulse.

TABLE 17. PROM FAILURE DATA PERTAINING TO THE REAPPEARANCE OF A PROGRAMMED NICHROME FUSE LINK

Model Parameters							(13)	(14)
	(10) Programmer's Learning		(11) Programming Time		(12) Failure Mechanism		Normalizing Factor	Normalized Unprogrammed Bit Hours (10^{12})
π_{T4}	Status	π_{PL}	Time*	π_{PT}	Type	π_{FM2}	$\pi_Q\pi_L\pi_{T4}\pi_{PL}\pi_{PT}\pi_{FM2}$	$t \times \left[\left(P_{FL}\right)_P \cdot N_{FL}\right] \times \pi_Q\pi_L\pi_{T4}\pi_{PL}\pi_{PT}\pi_{FM2}$
1.00	Mature	1	1 ms	0.65	RFL	1	97.50	3.793,920
1.00	Mature	1	5 ms	0.81	RFL	1	1.62	0.002,180
1.00	Mature	1	5 ms	0.81	RFL	1	8.10	0.020,509
1.00	Early	10	5 ms	0.81	RFL	1	40.50	0.004,339
1.23	Early	10	5 ms	0.81	RFL	1	49.82	0.002,296
1.09	Mature	1	5 ms	0.81	RFL	1	132.44	0.341,941
								Total 4.165,185

$$\left(\lambda_{FL}\right)_P = \frac{36}{4.165,185 \times 10^{12}}$$

$$\left(\lambda_{FL}\right)_P = 9.362 \text{ (failures/}10^{12}\text{ hours)}$$

The two-sided lower and upper confidence limits (based on the χ^2 distribution) for r failures in the gamma prior using the Poisson failure model is

$$\frac{\chi^2\left(1 - \frac{\alpha}{2};\ 2r\right)}{2T} \leq \left(\lambda_{FL}\right)_P \leq \frac{\chi^2\left(\frac{\alpha}{2};\ 2r + 2\right)}{2T}$$

where:

$$r = \text{number of failures, } \sum_{i=1}^{n} t_i$$

$$T = \text{test time, } \sum_{i=1}^{n}\left(t_i\left[\left(P_{FL}\right)_{P_i} \times N_{FL_i}\right] \times \left({}^{\pi}Q_i\,{}^{\pi}L_i\,{}^{\pi}T4_i\,{}^{\pi}PL_i\,{}^{\pi}PT_i\,{}^{\pi}FM2_i\right)\right)$$

For a 50 percent lower and upper confidence limit with 39 failures:

$$\frac{1}{2}\chi^2\left(1 - \frac{\alpha}{2};\ 2r\right) = 34.6$$

$$\frac{1}{2}\chi^2\left(\frac{\alpha}{2};\ 2r + 2\right) = 44.1$$

Therefore:

$$\frac{34.6}{4.165,185 \times 10^{12}} \leq \left(\lambda_{FL}\right)_P \leq \frac{44.1}{4.165,185 \times 10^{12}}$$

$$8.31 \leq \left(\lambda_{FL}\right)_P \leq 10.6 \text{ (failures/}10^{12}\text{ hours)} \qquad (17)$$

π_Q – Quality Factor

The quality factor, π_Q, considers the device quality class and reflects its relative impact on programmed fuse link reliability. The value of π_Q, is obtained from Table 13.

The PROM failure data collected thus far indicate that the best technique to screen out potential growback failures is a high temperature dynamic burn-in. Analysis of available data pertaining to growbacks, in addition to the burn-in requirements delineated in Mil-Std-883 and Mil-M-38510, led to the belief that Table 13 also reflects the relative impact of the device screening class on programmed fuse link reliability.

π_L – Learning Factor

The learning factor, π_L, considers the PROM manufacturer's design and process status and relates their relative effects on programmed fuse link reliability. The value for π_L is obtained from Table 14.

The learning factor π_L, has been incorporated into the term λ_{RFL} for the same reason it was incorporated into λ_{DFL}. That is, possible abnormalities in the deposition of the fuse link material on the SiO_2 substrate resulting from an early production phase or modifications in an existing design or process could lead to potential programmed fuse link failures. The quantification of π_L for λ_{RFL} is equivalent to that given in λ_{DFL} since their relative impact upon reliability is equivalent.

π_{T4} – Temperature Acceleration Factor

The temperature acceleration factor π_{T4}, is an exponential function which considers the device operating ambient temperature and reflects its relative impact on programmed fuse link reliability.

The value of π_{T4} is obtained from

$$\pi_{T4} = 0.825^{e\left(\frac{T+273}{358}\right)^9}$$

where:

π_{T4} = temperature acceleration factor for programmed resistor fuse links

T = device ambient temperature (degrees C)

The value of π_{T4} can also be determined from Figure 58. The following gives the derivation of this expression.

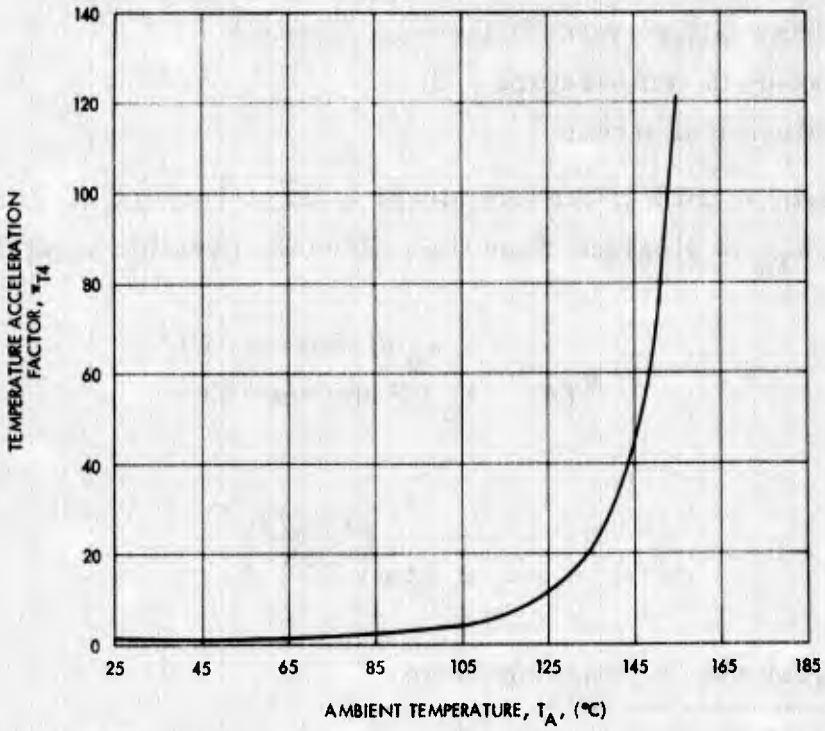


Figure 58. π_{T4} versus ambient temperature.

User and vendor data obtained to date have indicated that the phenomenon of growback is accelerated by higher temperatures. Since no quantitative information is available to construct a temperature acceleration equation for programmed fuse links, an approximation must be developed.

It is believed that the temperature acceleration factor that is derived by utilizing the base failure rate, λ_b for solid tantalum capacitors (type MIL-C-39003) approximates the relationship described above. This association was chosen since it is felt that the temperature accelerated dielectric breakdown that occurs within the blown region of programmed fuse links is

similar to that for solid tantalum capacitors. The base failure rate for solid tantalum capacitors (taken from Section 2.6 of Mil-Hdbk-217B) is

$$\lambda_b = 3 \times 10^{-3}\left[\left(\frac{S}{0.4}\right)^3 + 1\right] e^{\left(\frac{T+273}{358}\right)^9} \qquad (18)$$

where

λ_b = base failure rate (failures/10^6 hours)
T = ambient temperature (^oC)
S = electrical stress

An approximation to the temperature acceleration factor for programmed fuse links, π_{T4} is obtained when the following operation is performed:

$$\pi_{T4} = \frac{\lambda_b \text{ (T degrees C)}}{\lambda_b \text{ (25 degrees C)}}$$

$$= 0.82\, e^{\left(\frac{T+273}{358}\right)^9}$$

π_{PL} – Programmer's Learning Factor

The programmer's learning factor, π_{PL}, considers the programming technique and equipment utilized by the programmer and reflects their relative impact on programmed resistor fuse link reliability.

The value for π_{PL} is obtained from Table 18.

A significant amount of failure data collected to date indicate that many PROM failures are induced by misprogramming. The fault lies either with the programming technique or with the calibration of programming equipment. Because this factor significantly affects PROM reliability, it was decided to incorporate this factor into the model. The quantification of π_{PL} is based on a similar factor delineated in Mil-Hdbk-217B (π_L, Table 2.1.5-2) since it is felt that its relative impact on programmed fuse link reliability is equivalent.

TABLE 18. PROGRAMMER'S LEARNING FACTOR, π_{PL}

The programmer's learning factor, π_{PL}, is 10 under any of the following conditions:

1. Radical change in the programming technique.
2. Radical change in programming equipment.

The factor of 10 can be expected to apply until conditions and controls have stabilized. This period can extend for as much as 6 months. π_{PL} is equal to 1.0 under all conditions not stated in (1) and (2) above.

π_{PT} – Programming Time Factor

To ascertain the effects of time to program, or time to blow the fuse, to the chance of failure, or probability of reconduction, data from three sources were examined.

Source 1* has published a curve relating probability of "growback" or reconduction to time to blow (Figure 59). This curve was derived from data on specially fabricated nichrome fuses which were blown with voltage ramps of various slopes. As the interest in the time to blow is in the range of 10 to 100 ms the curve from Figure 59 was extrapolated down to the 10 ms point as shown in Figure 60.

Source 2** provided the data shown in Table 19. A curve developed from the confidence intervals constructed from Table 19 data is shown in Figure 61.

Source 3 contains data obtained from experiments performed under this study. See Figure 62. Details of the data are contained in the subsection on Reconduction with respect to Temperature and Time in the Section on Reliability Physics of Memory Elements.

*P. G. Franklin, "Programmable Read Only Memory Reliability Report II," Monolithic Memories, Inc., April 1974.

**Dr. R. S. Mo, private communications.

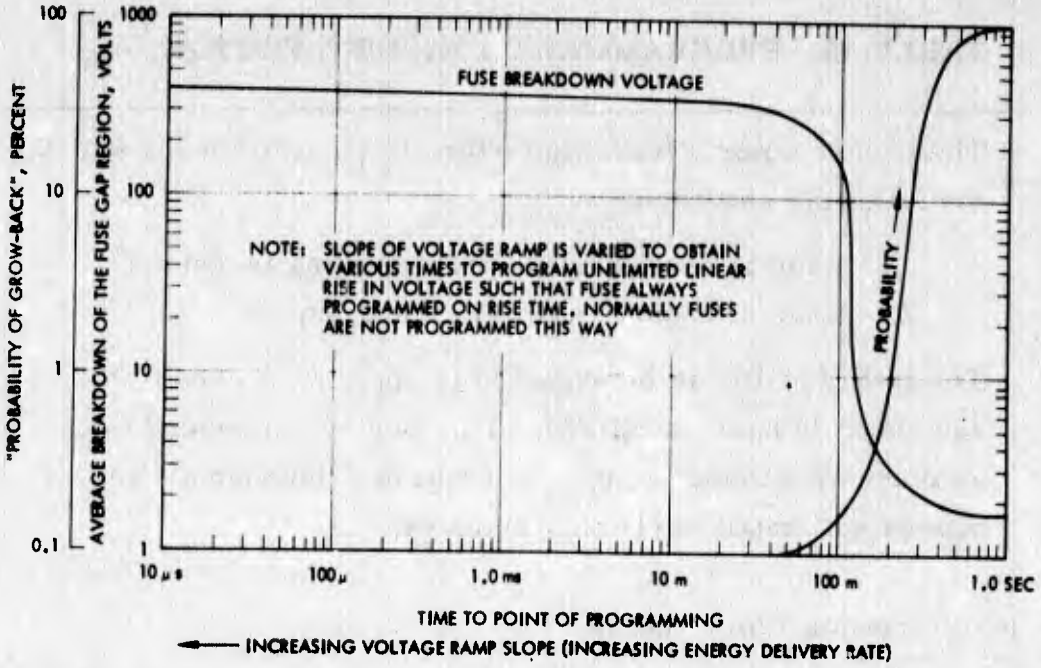


Figure 59. Time to program versus gap breakdown voltage and grow-back or reconduction probability of voltage ramp programmed nichrome fuses.

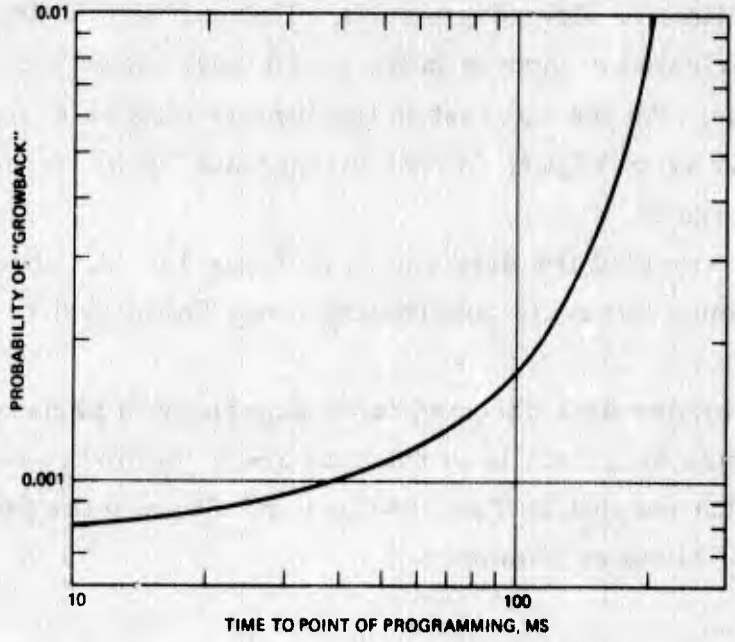


Figure 60. Probability of reconduction or grow-back versus time to point of programming of nichrome fuses programmed with voltage ramp (extrapolated from Figure 59)

TABLE 19. DATA ON RECONDUCTION OF SPECIALLY FABRICATED NICHROME

Fuses which were blown with Rectangular Voltage Pulses

[Fuse Ambient Temperature = 150°C
Voltage Across Fuse = 4.5 V
Test Time = 350 Hours
All reconductions occurred within 200 Hours]

Time to Blow, ms	Number of Fuses Used	Number of Fuses Reconducted	Percent Reconducted
10-750	205	8	3.9
1-10	91	2	2.2
0.01-1.0	55	0	0
0.01	162	0	0

The large differences among the three data sources on probability of reconduction with respect to a particular time to blow can be seen in Figures 60 through 62. There are many conceivable reasons for the differences:

1. The nichrome fuses have different geometry and composition.
2. The applied programming pulses are different.
3. The criteria for reconduction are different.
4. The voltages across the fuses during test are different.
5. The temperatures under test are different.
6. The test times are different.

Although the absolute probabilities are different for the various data, it might be possible to glean certain relations with respect to time to blow. One clear fact is that the probability of reconduction increases with time to blow. For the time to blow range of interest Table 20 has been constructed from values obtained from curves from Figures 60 and 61. A time to blow of 10 ms has been arbitrarily selected as the normalization point for calculation of relative probability of reconduction.

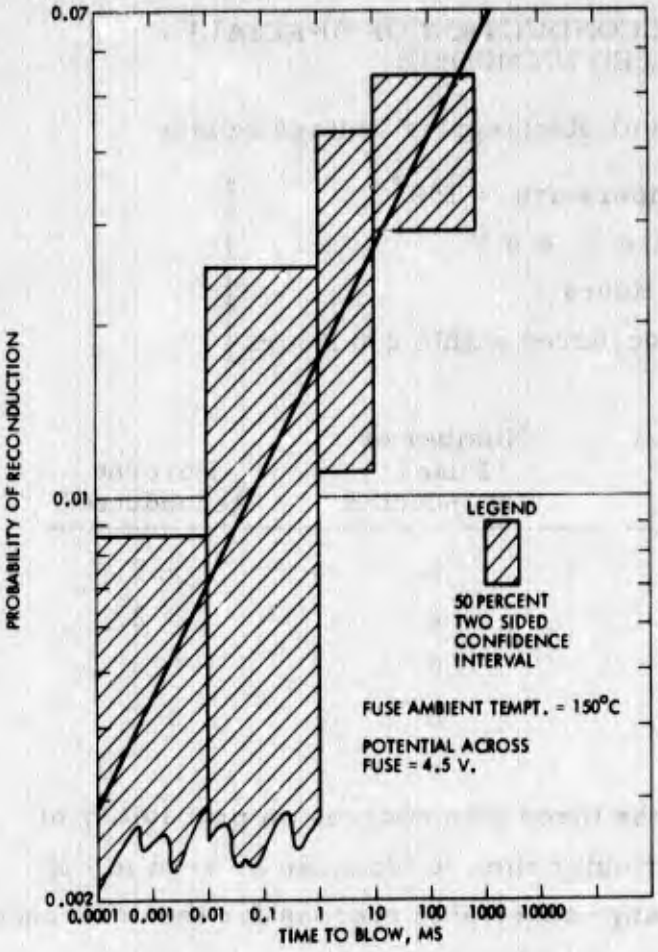


Figure 61. Probability of reconduction versus time to blow of specially fabricated nichrome fuses (derived from information obtained from Dr. R. S. Mo).

Based on the selected relative values of probability of reconduction from Table 20, a 15 percent increase can be expected in probability of reconduction changing from a 10 ms time to blow to 20 ms. It should be noted that the use of 20 ms pulse to program does not mean that all the fuses would have a time to blow of 20 ms. Data indicated that for one of the vendors most of the times to blow for nichrome fuses would be around 1 ms when programmed with the vendor recommended pulse voltage amplitude.

Failure Mechanism Factor, π_{FM2}

Table 11 indicated that not all PROM technologies are applicable to the reappearing fuse link phenomena. To account for this, the failure mechanism factor 2, π_{FM2}, has been incorporated into the model to allow the term λ_{RFL} to equal zero when applicable.

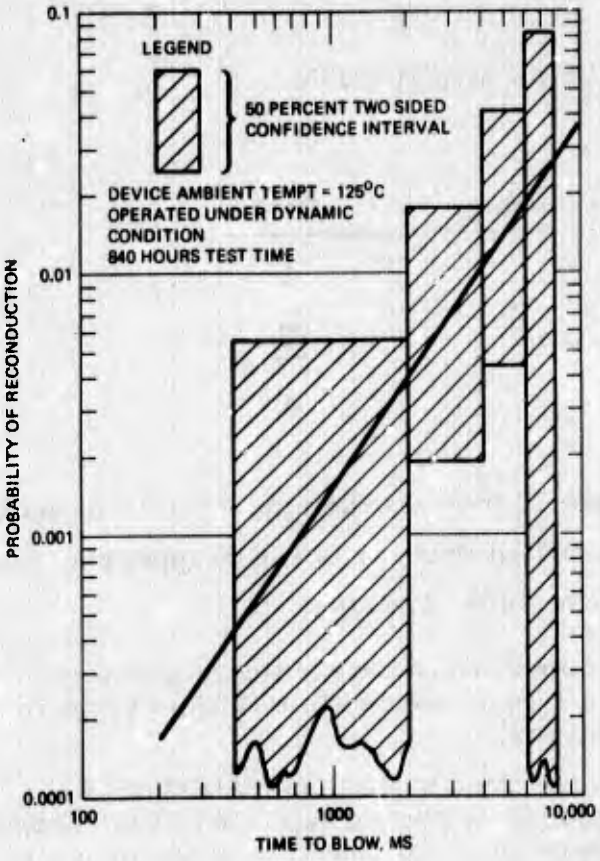


Figure 62. Probability of reconduction versus time to blow of nichrome fuses in 1K PROMs.

TABLE 20. RELATIVE EFFECTS OF TIME TO BLOW ON PROBABILITY OF RECONDUCTION

Time to Blow, ms	Probability of Reconduction				
	Figure 60		Figure 61		Selected Relative Values π_{PT}
	Absolute	Relative	Absolute	Relative	
1	—	—	0.017	0.63	0.65
10	0.0008	1	0.027	1	1
20	0.0009	1.13	0.031	1.15	1.15
40	0.0010	1.25	0.033	1.22	1.25
100	0.0017	2.13	0.042	1.56	2.0
200	0.0100	12.5	0.054	2.0	Undetermined

The value of π_{FM2} is obtained from Table 21.

TABLE 21. FAILURE MECHANISM FACTOR 2, π_{FM2}

Memory Element Technology	FM2
Nichrome	1
Titanium-Tungsten	⊡
AIM	0

The values contained within Table 21 indicate the applicability of each memory element type that has been studied thus far to the reappearing fuse phenomenon. The values for π_{FM2} are defined below:

$\pi_{FM2} = 1$: The failure data obtained to date indicate that this memory element type is susceptible to the reappearing fuse link phenomenon.

$\pi_{FM2} = 0$: The failure data obtained to date indicate that this memory element type is not susceptible to the reappearing fuse link phenomenon (or that this phenomenon is not applicable).

$\pi_{FM2} = ⊡$: The failure data obtained to date is inconclusive with regard to this memory element's susceptibility to the reappearing fuse link phenomenon.

The Shorted Diode Term, λ_{SD} – The term λ_{SD} has been incorporated into the model to account for the failure mechanism related to the shorting of an unprogrammed AIM memory element.

It has been determined that the following items influence unprogrammed AIM memory element reliability.

1. Device quality level
2. Manufacturer's production experience
3. Device temperature.

The items listed above have been considered in the development of λ_{SD}:

$$\lambda_{SD} = C_5 \pi_Q \pi_L \pi_{T1} \pi_{FM3} \quad (19)$$

where:

C_5 = complexity factor for failure mechanism related to the shorting of unprogrammed AIM memory diodes

π_Q = quality factor

π_L = manufacturer's learning factor

π_{T1} = temperature acceleration factor for bipolar devices

π_{FM3} = failure mechanism

Each parameter within λ_{SD} will now be considered individually, while giving information concerning its function and quantification.

C_5 – Complexity Factor

The complexity factor C_5, is a linear function which relates the number of unprogrammed AIM memory elements to the normalized failure rate contribution for the shorting of an unprogrammed AIM memory element. The value of C_5 is obtained from the following equation:

$$C_5 = (\lambda_{AIM})_{UNP} \cdot (N_{AIM})_{UNP} \tag{20}$$

where:

C_5 = normalized failure rate contribution for the unprogrammed AIM memory matrix

$(\lambda_{AIM})_{UNP}$ = normalized failure rate for an unprogrammed AIM memory element

$(N_{AIM})_{UNP}$ = number of unprogrammed AIM memory elements in the memory matrix

To quantify $(\lambda_{AIM})_{UNP}$ from test data the following mathematical manipulation is required. The value for the normalized failure rate of an unprogrammed AIM memory element, $(\lambda_{AIM})_{UNP}$ was calculated utilizing the formula denoted by Equation (21) and the failure data collected from PROM users. The development of Equation (21) is not shown here since it is very similar to that for $(\lambda_{FL})_{UNP}$ which was described earlier.

$$(\lambda_{AIM})_{UNP} = \frac{\sum_{i=1}^{n} f_i}{\sum_{i=1}^{n} \left(t_i \left[(P_{AIM})_{UNP_i} \cdot N_{AIM_i} \right] \left(\pi Q_i \pi L_i \pi T1_i \pi FM3_i \right) \right)} \quad (21)$$

where:

$(\lambda_{AIM})_{UNP}$ = normalized failure rate for an unprogrammed fuse link

f_i = number of failures for the i^{th} data source

t_i = number of device hours for the i^{th} data source

$(P_{AIM})_{UNP_i}$ = the percentage of unprogrammed AIM memory elements in the memory matrix for the j^{th} data source. [Note that $(N_{AIM})_{UNP} = (P_{AIM})_{UNP} \cdot N_{AIM}$]

N_{AIM_i} = the number of AIM memory elements in the memory matrix for the i^{th} data source

$\pi Q_i \pi L_i \pi T1_i \pi FM3_i$ = normalizing factor for the i^{th} data source

The PROM failure data collected thus far, pertaining to the shorting of unprogrammed AIM memory elements are presented in Table 22 and categorized (according to columns) as follows:

1. The source of data
2. The number of AIM memory elements in the memory matrix, N_{AIM}
3. The percentage of the memory matrix that is unprogrammed, $(P_{AIM})_{UNP}$
4. The number of devices
5. The number of device hours, t
6. The number of failed devices as a result of shorted AIM memory elements, f
7. The quality class of the device, π_Q
8. The manufacturer's production experience, π_L
9. The device junction temperature, π_{T1}
10. The failure mechanism factor 3, π_{FM3}
11. The normalizing factor, $\pi_Q \pi_L \pi_{T1} \pi_{FM3}$
12. The quantity of normalized unprogrammed bit hours, $t \times \left[(P_{AIM})_{UNP} \cdot N_{AIM} \right] \times \pi Q \pi L \pi T1 \pi FM3$

TABLE 22. PROM FAILURE DATA PERTAINING TO THE SHORTING OF AN UNPROGRAMMED AIM MEMORY ELEMENT

(1) User Source of Data	(2) Device Size (Bits) N_{AIM}	(3) Percent of Memory Element Unprogrammed $(P_{AIM})_{UNP}$	(4) Number of Devices	(5) Number of Device Hours t	(6) Number of Memory Element Failures f	Math Model Parameters (7) Quality: Class	(7) Quality: π_Q	(8) Manufacturer's Learning: Status	(8) Manufacturer's Learning: π_L	(9) Junction Temperature: (°C)	(9) Junction Temperature: π_{T1}	(10) Failure Mechanism: Type	(10) Failure Mechanism: τ_{FM3}	(11) Normalizing Factor $\pi_Q \pi_L \pi_{T1} \tau_{FM3}$	(16) Normalized Unprogrammed Bit Hours (10^{12}) $t \times [(P_{AIM})_{UNP} \cdot N_{AIM}] \times \pi_Q \pi_L \pi_{T1} \tau_{FM3}$
1	256	50	112	78,288	0	D	150	Mature	1	62	0.59	SD	1	88.50	0.000,887
2	256	50	145	142,000	0	C	16	Mature	1	62	0.59	SD	1	9.44	0.000,172
3	1024	50	100,000	1,314,000,000	0	D	150	Mature	1	51	0.36	SD	1	54.00	36.329,472
4	2048	80	364	91,728	0	D	150	Mature	1	70	0.83	SD	1	124.50	0.018,711
				Total	0										Total 36.349,242

The normalizing factor $\pi_Q \pi_L \pi_{TI} \pi_{FM3}$ contained within column 11 is calculated by taking the product of the factors $\pi_Q \pi_L \pi_{T1}$ and π_{FM3}, whose values are found within columns (7), (8), (9), and (10), respectively. The values for the four π-factors were extracted from tables shown later in the text and were used to normalize the failure data to the following conditions:

1. Quality level: Mil-M-38510, Class A (JAN)
2. Manufacturer's learning level: Mature
3. Junction temperature: $T_j = 75^{\circ}C$
4. Failure mechanism factor 3: AIM memory elements

When the data contained within Table 22 are applied to Equation (21) the value of $(\lambda_{AIM})_{UNP}$ (assuming one-third of a failure, e.g.,

$$\sum_{i=1}^{n} f_i = 0.3$$

as described in the subsection for $(\lambda_{FL})_{UNP}$ for the zero failure case) is given by the following:

$$(\lambda_{AIM})_{UNP} = \frac{\sum_{i=1}^{n} f_i}{\sum_{i=1}^{n} \left(t_i \left[(P_{AIM})_{UNP_i} \cdot N_{AIM_i} \right] \left(\pi_{Q_i} \pi_{L_i} \pi_{TI_i} \pi_{FM3_i} \right) \right)}$$

$$(\lambda_{AIM})_{UNP} = \frac{0.3}{36.349,242 \times 10^{12}}$$

$$(\lambda_{AIM})_{UNP} = 0.0083 \text{ (failures/}10^{12} \text{ hours)}$$

The two-sided lower and upper confidence limits (based on the χ^2 distribution) for r failures in the gamma prior using the Poisson failure model is

$$\frac{\chi^2\left(1 - \frac{\alpha}{2};\ 2r\right)}{2T} \leq (\lambda_{AIM})_{UNP} \leq \frac{\chi^2\left(\frac{\alpha}{2};\ 2r + 2\right)}{2T}$$

where:

$$r = \text{number of failures, } \sum_{i=1}^{n} f_i$$

$$T = \text{test time, } \sum_{i=1}^{n} \left(t_i \left[(P_{AIM})_{UNP_i} \times N_{AIM_i} \right] \times \left(\pi_{Q_i} \pi_{L_i} \pi_{T1_i} \pi_{FM3_i} \right) \right)$$

For a 50 percent two sided confidence limits with 0 failures, the lower limit is 0 and the upper limit is

$$\frac{1}{2} \chi^2\left(\frac{\alpha}{2};\ 2r + 2\right) = 1.386$$

Therefore,

$$\frac{0}{36.349,242 \times 10^{12}} \leq (\lambda_{AIM})_{UNP} \leq \frac{1.386}{36.349,242 \times 10^{12}} \tag{22}$$

$$0 \leq (\lambda_{AIM})_{UNP} \leq 0.0381 \text{ (failures/}10^{12}\text{ hours)}$$

π_Q – Quality Factor

The quality factor, π_Q, considers the device quality class and reflects the relative impact on unprogrammed AIM memory element reliability. The value of π_Q is obtained from Table 13.

The failure mechanism characteristic of an unprogrammed AIM memory element is identical to that experienced by a standard bipolar microelectronic device, since both are of the same construction and technology. In addition, the quality screens that are utilized for the standard bipolar microelectronic device have the same relative impact on reliability as that for the unprogrammed AIM memory element. Therefore, the quantification of the quality factor relative to the unprogrammed AIM memory element is based on that for microelectronic devices delineated in Table 2. 1. 5-1 of Mil-Hdbk-217B.

π_L – Learning Factor

The learning factor, π_L, considers the PROM manufacturer's design and process status and relates their relative effects on unprogrammed AIM memory element reliability. The value of π_L is obtained from Table 14.

When a semiconductor manufacturer is in the early production phase of a standard bipolar microelectronic device or if there has been a modification in an existing design or process, a learning period is experienced whereby modifications or adjustments are incorporated into the design or process to eliminate the apparent incongruities. Since unprogrammed AIM memory elements are of the same construction and technology as standard bipolar microelectronic devices, a similar time period is required to isolate and correct potential problem area. Therefore, the quantification of the learning factor relative to the unprogrammed AIM memory element is based on the learning factor for microelectronic devices delineated in Table 2. 1. 5-2 of Mil-Hdbk-217B.

π_{T1} – Temperature Acceleration Factor

The temperature acceleration factor is an exponential function that considers the device junction temperature and reflects its relative impact on unprogrammed AIM memory element reliability. The value of π_{T1} is obtained from the following Arrhenius expression:

$$\pi_{T1} = 0.1\, e^{-4794\left(\frac{1}{T_j + 273} - \frac{1}{298}\right)} \qquad (23)$$

where:

π_{T1} = temperature acceleration factor for unprogrammed AIM memory elements

T_j = device junction temperature (degrees C)

The value of π_{T1} can also be obtained from Figure 63.

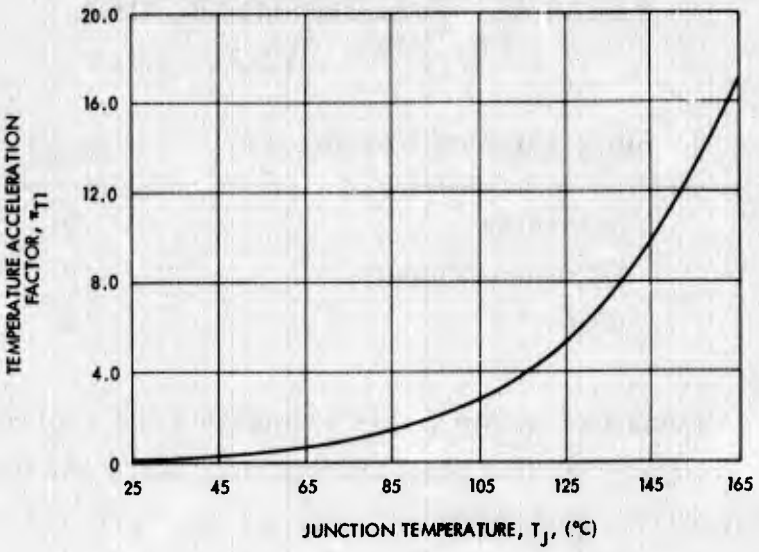


Figure 63. π_{T1} versus junction temperature.

The failure mechanisms characteristic of standard bipolar microelectronic devices are accelerated by elevated temperatures as defined by the Arrhenius equation above. Elevated temperature activate reactions within the chip that result in the degradation and possible failure of the device. Since an unprogrammed AIM memory element is constructed utilizing standard bipolar technology, the corresponding failure mechanism is accelerated by temperature identically to that described above. Therefore, the quantification of the temperature acceleration factor relative to the unprogrammed AIM memory element is based on that for standard bipolar microelectronic devices delineated in Table 2. 1. 5-4 of Mil-Hdbk-217B, which is denoted by Equation (23).

π_{FM3} – Failure Mechanism Factor

In Table 11 it was indicated that not all PROM technologies are applicable to the phenomenon resulting in the shorting of unprogrammed AIM memory elements. To account for this, the failure mechanism factor 3, π_{FM3}, has been incorporated into the model to allow the term λ_{SD} to equal zero when applicable. The value of π_{FM3} is obtained from Table 23.

TABLE 23. FAILURE MECHANISM FACTOR 3, π_{FM3}

Memory Element Technology	π_{FM3}
Nichrome	0
Titanium-Tungsten	0
AIM	1

The values contained within Table 23 indicate the applicability of each memory element type that has been studied thus far to the phenomenon resulting in the shorting of an unprogrammed AIM memory element. The value for π_{FM3} are defined below:

$\pi_{FM3} = 1$: The failure data obtained to date indicate that this memory element type is susceptible to the phenomenon resulting in the shorting of an unprogrammed AIM memory element.

$\pi_{FM3} = 0$: The phenomenon resulting in the shorting of an unprogrammed AIM memory element is not applicable to this memory element type.

The Opened Diode Term, λ_{OD}

The term λ_{OD} has been incorporated into the model to account for the failure mechanism related to the opening or changing to a higher resistance state of a programmed AIM memory element. This includes the possibilities of emitter contact window opening and changes in the aluminum pipe through the junction (if the pipe is indeed the shorting mechanism).

It has been determined that the following items influence programmed AIM memory element reliability.

1. Device quality level
2. Manufacturer's production experience
3. Device temperature
4. Programmer's learning factor.

The items listed above have been considered in the development of λ_{OD}:

$$\lambda_{OD} = C_6 \pi_Q \pi_L \pi_{T1} \pi_{PL} \pi_{FM4} \tag{24}$$

where:

C_6 = complexity factor for failure mechanism related to the opening of programmed AIM memory elements

π_Q = quality factor

π_L = manufacturer's learning factor

π_{T1} = temperature acceleration factor for bipolar devices

π_{PL} = programmer's learning factor

π_{FM4} = failure mechanism factor

Each parameter within λ_{OD} will now be considered individually, while giving information concerning its function and quantification.

C_6 - Complexity Factor

The complexity factor C_6, is a linear function which relates the number of programmed AIM memory elements to the normalized failure rate contribution for the opening of a programmed AIM memory element. The value of C_6 is obtained from the following equation:

$$C_6 = (\lambda_{AIM})_P \cdot (N_{AIM})_P \tag{25}$$

where:

C_6 = normalized failure rate contribution for the programmed AIM memory matrix

$(\lambda_{AIM})_P$ = normalized failure rate for a programmed AIM memory element

$(N_{AIM})_P$ = number of programmed AIM memory elements in the memory matrix

To quantify (λ_{AIM}) from test data the following mathematical manipulation is required. The value for the nomalized failure rate of a programmed AIM memory element, (λ_{AIM}) was calculated utilizing the formula denoted by Equation (26) and the failure data collected from PROM users. The development of Equation (26) is not shown here since it is very similar to that for $(\lambda_{PL})_{UNP}$ which was described earlier.

$$(\lambda_{AIM})_P = \frac{\sum_{i=1}^{n} f_i}{\sum_{i=1}^{n} \left(t_i \left[(P_{AIM})_{P_i} \cdot N_{AIM_i} \right] \left(\pi Q_i \pi L_i \pi T1_i \pi PL_i \pi FM4_i \right) \right)} \tag{26}$$

where:

$(\lambda_{AIM})_P$ = normalized failure rate for a programmed AIM memory element

f_i = number of failures for the i^{th} data source

t_i = number of device hours for the i^{th} data source

$(P_{AIM})_{P_i}$ = the percentage of programmed AIM memory elements in the memory matrix for the i^{th} data source and $(N_{AIM})_P = (P_{AIM})_P N_{AIM}$,

N_{AIM_i} = the number of AIM memory elements in the memory matrix for the i^{th} data source

$\pi_{Q_i}\pi_{L_i}\pi_{T1_i}\pi_{PL_i}\pi_{FM4_i}$ = normalizing factor for the i^{th} data source

The PROM failure data collected thus far, pertaining to the opening of programmed memory elements are presented in Table 24 and categorized (according to columns) as follows:

1. The source of data
2. The number of AIM memory elements in the memory matrix, N_{AIM}
3. The percentage of the memory matrix that is programmed, $(P_{AIM})_P$
4. The number of devices
5. The number of device hours, t
6. The number of failed devices as a result of opened AIM memory fuse elements, f
7. The quality class of the device, π_Q
8. The manufacturer's production experience, π_L
9. The device junction temperature, π_{T1}
10. The programmer's learning factor, π_{PL}
11. The failure mechanism factor, π_{FM4}
12. The normalizing factor, $\pi_Q\pi_L\pi_{T1}\pi_{PL}\pi_{FM4}$
13. The quantity of normalized programmed bit hours, $t \times [(P_{AIM})_P \times N_{AIM}] \times \pi_Q\pi_L\pi_{T1}\pi_{PL}\pi_{FM4}$

TABLE 24. PROM FAILURE DATA PERTAINING TO THE OPENING OF A PROGRAMMED AIM MEMORY ELEMENT

(1) User Source of Data	(2) Device Size (Bits)	(3) Percent of Memory Element Programmed	(4) Number of Devices	(5) Number of Device Hours	(6) Number of Memory Element Failures	Math Model Parameters										(12) Normalizing Factor	(13) Normalized Programmed Bit Hours (10^{12})
						(7) Quality		(8) Manufacturer's Learning		(9) Junction Temperature		(10) Programmer's Learning		(11) Failure Mechanism			
	N_{AIM}	$(P_{AIM})_P$				Class	π_Q	Status	π_L	(°C)	π_{TI}	Status	π_{PL}	Type	π_{FM4}	$\pi_Q \pi_L \pi_{TI} \pi_{PL} \pi_{FM4}$	$t \times \left[(P_{AIM})_P \cdot N_{AIM}\right] \times \pi_Q \pi_L \pi_{TI} \pi_{PL} \pi_{FM4}$
1	256	50	112	78,288	0	D	150	Mature	1	62	.59	Mature	1	OD	1	88.50	0.000,887
2	256	50	145	142,000	0	C	16	Mature	1	62	.59	Mature	1	OD	1	9.44	0.000,172
3	1024	50	100,000	1,314,000,000	0	D	150	Mature	1	51	.36	Mature	1	OD	1	54.00	36.329,472
4	2048	20	364	91,728	1	D	150	Mature	1	70	.83	Mature	1	OD	1	124.50	0.004,678
				Total	1												Total 36.335,209

The nomalizing factor $\pi_Q \pi_L \pi_{T1} \pi_{PL} \pi_{FM4}$ contained within column 13 is calculated by taking the product of the factors $\pi_Q \pi_L \pi_{T1} \pi_{PL}$ and $\pi_{FM4'}$ whose values are found within columns (7), (8), (9), (10), and (11), respectively. The values for the five π-factors were extracted from tables shown later in the text and were used to normalize the failure data to the following conditions:

1. Quality level: Mil-M-38510, Class A (JAN)
2. Manufacturer's learning level: Mature
3. Junction temperature: $T_j = 75^{\circ}C$
4. Programmer's learning level: Mature
5. Failure mechanism factor 4: AIM memory elements

When the data contained within Table 24 are applied to Equation (26) the maximum likelihood and unbiased estimate of $(\lambda_{AIM})_P$ is given by

$$(\lambda_{AIM})_P = \frac{\sum_{i=1}^{n} f_i}{\sum_{i=1}^{n} \left(t_i \left[(P_{AIM})_{P_i} \times N_{AIM_i} \right] \left(\pi_{Q_i} \pi_{L_i} \pi_{T1_i} \pi_{PL_i} \pi_{FM4_i} \right) \right)}$$

$$(\lambda_{AIM})_P = \frac{1}{36.\ 335,209 \times 10^{12}}$$

$$(\lambda_{AIM})_P = 0.0275 \text{ (failures/}10^{12} \text{ hours)}$$

The two-sided lower and upper confidence limits (based on the χ^2 distribution) for r failures in the Gamma prior using the Poisson failure model is

$$\frac{\chi^2 \left(1 - \frac{\alpha}{2};\ 2r\right)}{2T} \leq (\lambda_{AIM})_P \leq \frac{\chi^2 \left(\frac{\alpha}{2};\ 2r + 2\right)}{2T}$$

where:

r = number of failures, $\sum_{i=1}^{n} f_i$

T = test time, $\sum_{i=1}^{n} \left(t_i \left[(P_{AIM})_{P_i} \times N_{AIM_i} \right] \times \left(\pi_{Q_i} \pi_{L_i} \pi_{T_i} \pi_{PL_i} \pi_{FM4_i} \right) \right)$

For a 50 percent lower and upper confidence limit with 1 failure,

$$\frac{1}{2} \chi^2 \left(1 - \frac{\alpha}{2} ; 2r \right) = 0.288$$

$$\frac{1}{2} \chi^2 \left(\frac{\alpha}{2} ; 2r + 2 \right) = 2.693$$

Therefore,

$$\frac{0.288}{36.335,209 \times 10^{12}} \leq (\lambda_{AIM})_P \leq \frac{2.693}{36.335,209 \times 10^{12}} \qquad (27)$$

$$0.0079 \leq (\lambda_{AIM})_P \leq 0.0741 \text{ (failures/}10^{12}\text{ hours)}$$

π_Q - Quality Factor

The quality factor, π_Q, considers the device quality class and reflects the relative impact on programmed AIM memory element reliability. The value of π_Q is obtained from Table 13. The rationale for the quantification of π_Q is similar to that given earlier in the section describing λ_{SD}.

π_L - Learning Factor

The learning factor, π_L, considers the PROM manufacturer's design and process status and relates their relative effects upon unprogrammed AIM memory element reliability. The value of π_L is obtained from Table 14.

The rationale for the quantification of π_L is similar to that given earlier in the section describing λ_{SD}.

π_{T1} - Temperature Acceleration Factor

The temperature acceleration factor is an exponential function which considers the device junction temperature and reflects its relative impact upon programmed AIM memory element reliability. The value of π_{T1} is obtained from the Arrhenius equation denoted by Equation (23). The rationale for the quantification of π_{T1} is the same as that given earlier in the section describing λ_{SD}.

π_{PL} - Programming Learning Factor

The programming learning factor, π_{PL}, considers the programming technique and equipment utilized by the programmer and reflects their relative impact upon programmed AIM memory element reliability. The value for π_{PL} is obtained from Table 18.

The programming of AIM memory elements requires a series of pulses designed to breakdown the emitter-base junction and thereby turning the bipolar device into a diode. After each programming pulse, a sense pulse is applied to determine if the junction is shorted. After the shorting of this junction has been detected, four more programming pulses are applied to program the short. This was a change from the 10 pulses originally specified. Feedback from industry, however, indicates that there is some confusion with regard to the number after pulses required. This disparity, in addition to other problems encountered which are related to the programming of AIM memory elements, has been considered in the development of λ_{OD} by incorporating the factor π_{PL}. Because of the lack of sufficient data, however, the programming learning factor π_{PL} for AIM memory elements has been quantified identically to that for resistor fuse links which was shown in the section describing λ_{RFL}.

π_{FM4} - Failure Mechanism Factor

In Table 11, it was indicated that not all PROM technologies are applicable to the phenomenon result in the opening of programmed AIM memory elements. To account for this, the failure mechanism factor 4, π_{FM4}, has been incorporated into the model in order to allow the term λ_{OD} to equal zero when not applicable. The value of λ_{FM4} is obtained from Table 25.

The values contained within Table 25 indicate the applicability of each memory element type that has been studied thus far to the phenomenon resulting in the opening of a programmed AIM memory element. The values for π_{FM4} are defined below:

$\pi_{FM4} = 1$: The failure data obtained to date implicate that this memory element type is susceptible to the phenomenon resulting in the opening of a programmed AIM memory element.

$\pi_{FM4} = 0$: The phenomenon resulting in the opening of a programmed AIM memory element is not applicable to this memory element type.

TABLE 25. FAILURE MECHANISM FACTOR 4, π_{FM4}

Memory Element Technology	π_{FM4}
Nichrome	0
Titanium-Tungsten	0
AIM	1

Summary of Comprehensive Version of PROM Model – The comprehensive version of the PROM model, originally shown as Equation (5), is restated below:

$$\lambda_{PROM} = \pi_Q \pi_L (C_1 \pi_{T1} + C_2 \pi_E) + \lambda_{DFL} + \lambda_{RFL} + \lambda_{SD} + \lambda_{OD}$$

The relationships for λ_{DFL}, λ_{RFL}, λ_{SD} and λ_{OD} defined by equations (6), (14), (19) and (24), respectively are as follows:

$$\lambda_{DFL} = C_3 \pi_Q \pi_L \pi_{T3} \pi_E \pi_{FM1}$$

$$\lambda_{RFL} = C_4 \pi_Q \pi_L \pi_{T4} \pi_{PL} \pi_{PT} \pi_{FM2}$$

$$\lambda_{SD} = C_5 \pi_Q \pi_L \pi_{T1} \pi_{FM3}$$

$$\lambda_{OD} = C_6 \pi_Q \pi_L \pi_{T1} \pi_{PL} \pi_{FM4}$$

When the expressions above are substituted into Equation (8), the following is obtained:

$$\lambda_{PROM} = \pi_Q \pi_L (C_1 \pi_{T1} + C_2 \pi_E) + C_3 \pi_Q \pi_L \pi_{T3} \pi_E \pi_{FM1} + C_4 \pi_Q \pi_L \pi_{T4} \pi_{PL} \pi_{PT} \pi_{FM2} + C_5 \pi_Q \pi_L \pi_{T1} \pi_{FM3} + C_6 \pi_Q \pi_L \pi_{T1} \pi_{PL} \pi_{FM4}$$

When simplified, the above expression yields the comprehensive version of the PROM failure rate model:

$$\lambda_{PROM} = \pi_Q \pi_L \left[(C_1 \pi_{T1} + C_2 \pi_E) + C_3 \pi_{T3} \pi_E \pi_{FM1} + C_4 \pi_{T4} \pi_{PL} \pi_{PT} \pi_{FM2} + C_5 \pi_{T1} \pi_{FM3} + C_6 \pi_{T1} \pi_{PL} \pi_{FM4} \right] \quad (28)$$

where:

λ_{PROM} = PROM failure rate (failures/10^6 hours)

C_1 = Complexity factor for ROMs (Table 2.1.5-8 of Mil-Hdbk-217B)

C_2 = Complexity factor for ROMS (Table 2.1.5-8 of Mil-Hdbk-217B)

C_3 = Complexity factor for the disappearing fuse link phenomenon (Equation 7)

C_4 = Complexity factor for the reappearing fuse link phenomenon (Equation 15)

C_5 = Complexity factor for failure mechanism related to the shorting of unprogrammed AIM memory elements (Equation 20)

C_6 = Complexity factor for failure mechanism related to the opening of programmed AIM memory elements (Equation 25)

π_Q = Quality factor (Table 2.1.5-1 of Mil-Hdbk-217B)

π_L = Learning factor (Table 2.1.5-2 of Mil-Hdbk-217B)

π_{T1} = Temperature acceleration factor for bipolar devices (Table 2.1.5-4 of Mil-Hdbk-217B)

π_{T3} = Temperature acceleration factor for unprogrammed fuse links (Figure 57)

π_{T4} = Temperature acceleration factor for programmed fuse links (Figure 58)

π_E = Application environment factor (Table 2.1.5-3 of Mil-Hdbk-217B)

π_{PL} = Programming learning factor (Table 18)

π_{PT} = Programming time factor (Table 20)

π_{FM1} = Failure mechanism -1 factor (Table 16)

π_{FM2} = Failure mechanism -2 factor (Table 21)

π_{FM3} = Failure mechanism -3 factor (Table 23)

π_{FM4} = Failure mechanism -4 factor (Table 25)

Simplex PROM Failure Rate Model

The simplex PROM failure rate model, originally defined by Equation (2), consists of the Mil-Hdbk-217B ROM failure rate model multiplied by the factor, K; that is

$$\lambda_{PROM} = K \lambda_{ROM} \tag{29}$$

The factor K is a constant multiplier which takes into account the parameters that influence the comprehensive version of the PROM failure rate model. The value for K will be determined by calculating K factors from the following expressions:

$$K = \frac{\lambda_{PROM}}{\lambda_{ROM}}$$

$$K(\text{for NiCr}) = \frac{\pi_Q \pi_L (C_1 \pi_{T1} + C_2 \pi_E + C_3 \pi_{T3} \pi_E \pi_{FM1} + C_4 \pi_{T4} \pi_{PL} \pi_{PT} \pi_{FM2})}{\pi_Q \pi_L (C_1 \pi_{T1} + C_2 \pi_E)}$$

$$K(\text{for AIM}) = \frac{\pi_Q \pi_L (C_1 \pi_{T1} + C_2 \pi_E + C_5 \pi_{T1} \pi_{FM3} + C_6 \pi_{T1} \pi_{PL} \pi_{FM4})}{\pi_Q \pi_L (C_1 \pi_{T1} + C_2 \pi_E)}$$

The parameters are as defined in other subsections. The specific conditions selected for K factor calculations are:

1. Junction temperature, $T_J = 72^{\circ}C$
2. Airborne uninhabited environment
3. 50 percent of bits programmed
4. 100 ms programming pulse duration (approximately 5 ms average time to program)

K factors for Ti-W technology will not be calculated as data is not sufficient for drawing significant conclusion.

The K factors calculations for NiCr technology calculated with two sided 50 percent confidence limit failure rates from Equation 12 and 17 and the assumption of perfect programming are shown in Table 26.

It is realized that programming perfection will be a key factor in achieving high reliability. The K factors shown in Table 26 should be considered long term mature figures. For calendar year 1975 the programmers learning factor π_{PL} values are estimated to be as shown in Table 27.

Utilizing the π_{PL} values from Table 27 to operate on the corresponding limits, i.e., lower limits with lower limit failure rates, the K factors for calendar year 1975 are calculated and shown in Table 28.

TABLE 26. K FACTORS CALCULATION FOR NiCr PROMS (WITH PERFECT PROGRAMMING)

Complexity No. of Bits	λ_{ROM}* (f./10^6 hr.)	λ_{PROM}* (f./10^6 hr.)		K	
		Lower Limit	Upper Limit	Lower Limit	Upper Limit
1024	0.2346	0.2387	0.2431	1.02	1.04
2048	0.3630	0.3712	0.3799	1.02	1.05
4096	0.5730	0.5894	0.6069	1.03	1.06

* With $\pi_Q \pi_L = 1$

TABLE 27. π_{PL} RANGES FOR CALENDAR YEAR 1975 FOR NiCr PROMS

Complexity No. of Bits	π_{PL}	
	Lower Limit	Upper Limit
1024	1	2
2048	2	4
4096	3	7

TABLE 28. K FACTORS FOR NiCr PROMS FOR CALENDAR YEAR 1975

Complexity No. of Bits	K	
	Lower Limit	Upper Limit
1024	1.02	1.08
2048	1.04	1.20
4096	1.09	1.42

Similar calculations were performed for the K factors for the AIM technology and found that the changes from λ_{ROM} to λ_{PROM} were less than 1 percent. It is therefore concluded that the K factors are approximately 1. As can be noted from Tables 22 and 24 the AIM data is dominated by one data source. Definitive conclusions should not be drawn at this time.

Table 29 gives a summary of the K factors.

TABLE 29. SUMMARY OF K VALUES

Complexity No. of Bits		K Value		
		Technology		
		NiCr	Ti:W	AIM
1024	Year 1975	1.02 - 1.08	Undetermined	Approx = 1
	Long Term	1.02 - 1.04		
2048	Year 1975	1.04 - 1.20		
	Long Term	1.02 - 1.05		
4096	Year 1975	1.09 - 1.42		
	Long Term	1.03 - 1.06		

8.0 CONCLUSIONS AND RECOMMENDATIONS

This section contains a summary of all the findings; recommendations are given with respect to programming, screening and tests for reliability assurance.

Programming

Based on the programming experiments conducted, user and vendor data and theoretical analyses the following conclusions and comments related to programming can be drawn with respect to the various technologies.

Nichrome Technology

1. Fuses requiring long programming times-to-blow exhibit smaller fuse gaps, and are more susceptible to reconduction failures. Fuses with short times-to-blow have wider gaps and have not been known to experience reconduction failures. Time-to-blow varies inversely as the magnitude of the programming current pulse.
2. Defects in the programming circuitry such as junction breakdown or insufficient current gain contribute to difficulty in programming. Fast programming rise times tend to cause breakdown. A properly selected slow rise time programming pulse would increase the probability of fusing prior to the point of junction breakdown.
3. As the physical distance between the row of fuses and the row select circuits increases, the difficulty of programming these fuses increases due to row conductor run impedance.
4. Leakages associated with unprogrammed fuses could reduce the current flowing into the fuse being programmed. Difficult to program fuses may become easier to program after additional fuses on the chip have been programmed.
5. Physical changes in the fuse material in the gap as a result of programming are a function of fuse geometries, materials and circuitry variables which differ from manufacturer to manufacturer and lot to lot.
6. Electrocorrosion is one of the predominant failure mechanisms associated with nichrome fusible links. Improved manufacturing process controls and packaging have reduced the occurrence of electrocorrosion. However, continuation of the "freeze out" and "water drop" tests as described in Mil-M-38510/201 is recommended.

7. Reconduction failure can occur beyond the 240 hour Class A and 160 hour Class B burn-in test of Mil-Std-883A conditions presently required in Mil-M-38510/202. Further testing to determine optimum burn-in criteria still needs to be developed; however, dynamic cycling of memory elements is a necessity for culling out reconduction failures.

8. Present programming yields on 1024 bit PROMs reported by most users are approximately 90 percent. This yield will drop with the use of shorter programming pulses designed to enhance reliability. Because of process and material variations, it is expected that both reliability and yield would vary from lot to lot even though the same programming procedure were used. Since the sample sizes for the experiments conducted are extremely small, a definitive optimum programming scheme cannot be generated. However, based on present knowledge the following might be used as a starting point for optimizing the programming procedure for reliability and yield:

   Use two pulses of approximately 10 ms long with 50 μs to 100 μs rise time for programming nichrome technology PROMs. First, program a single pulse through each of the fuses to be programmed and then repeat the same process and program a single pulse through each of the fuses that would not program the first time. The voltage magnitude of the programming pulse should be made as high as possible without causing junction breakdowns and damage to the circuits.

   Using this procedure it is expected that the programming yield would be equal to or better than what the industry is experiencing and the contribution of failure rates by the fuses due to reconduction would be no more than 20 percent of comparable ROM failure rate for 1K and 2K PROMs. Additional work should be done on programming to verify the benefits obtainable from this recommended procedure.

Titanium-Tungsten (Ti:W) Technology

1. For Ti:W technology, a programming procedure similar to that recommended for the nichrome technology might have merit. However, at this point in time there is insufficient failure information for correlating programming effects to failures. Much more work needs to be done before a more definite conclusion can be drawn.

2. One user reported experiencing bit reappearing failures. These failures were experienced on one part per hundred devices used. Several bits failed on one device indicating that this is probably a problem in the programming control circuitry which failed to provide sufficient current for proper fuse opening in conjunction

with insufficient additional testing which did not reject these devices. Increased screening controls on the test fuses before shipment would reduce the probability of this event occurring.

3. Programming experiments were limited during this study due to the unique programming control circuitry within the device itself which makes varying of programming current impossible.

4. Ti:W fuses which were programmed and subjected to SEM analysis revealed that a strong reaction had occurred between the glass overlay and the fuse leaving hard to etch debris in the fusing reaction zone. Prolonged etching to remove the glass and debris sometimes can result in removal of the fuse material, giving a false indication of excessively wide gap regions.

5. Ti:W 1024 bit devices were also reported by a user to experience a 90 percent yield during programming.

AIM Technology

1. Correlation of programming waveform experiments to changes in the diode structure were limited by available microscopy equipment that was capable of analyzing localized structure changes at the junction. Programming experiments were therefore limited to electrical performance criteria with emphasis placed on optimum stress conditions to cull out possible failure mechanisms.

2. No exact mechanism responsible for shorting the emitter-base diode junction could be identified either by users or the vendor during this study although aluminum at the emitter window appears to be an important ingredient.

3. Some devices were found to have marginally programmed junctions which changed states at high temperatures. Therefore, high and low temperature testing of these devices after programming are recommended.

4. AIM 1024 bit devices were also reported by most users to experience a 90 percent yield during programming.

5. The number of after pulses applied after the desired memory junction resistance has been reached must be optimally controlled so as to preclude any possibility of degrading the collector-base junction which serves as an isolation diode.

Screening

1. A PROM is basically an MSI. The three technologies studied have bipolar T^2L circuits as their building blocks. Hence, the general screening procedures for bipolar MSI's are also applicable to these PROMs.

2. For the AIM devices, the memory elements are standard diodes. Therefore, no new screening technique are required for these devices. However, the sequence of screening test performance should be changed such that high and low temperature tests are done after programming. Then marginally programmed parts and parts with weakened isolation diodes will be screened out.

3. For nichrome technology PROMs, a high temperature storage test after programming for annealing the fuse gaps might be desirable. However, at present no measured data exist to substantiate this belief. The "freeze-out" test called out in Mil-M-38510/201 should be used since it is an effective screen for the electro-corrosion failure mode of the nichrome fuses. The "water drop" test from Mil-M-38510/201 for high reliability devices, if performed, should be done on a wafer lot basis. It is expected that the defects on the overglass would be wafer lot oriented, rather than production lot oriented.

4. For Ti:W technology PROMs little failure information is available for correlation with screening tests. The vendor has initiated a special electrical test to screen out devices with potential self inadvertent programming due to leakage currents. This special test should be continued until the product is proven otherwise.

5. The high and low temperature electrical test should also be done on fuse link type PROMs after programming as presently marginal fusing condition still exists.

6. A large scale screening and life test experiment needs to be performed to obtain sufficient information for definitive conclusions.

Burn-in

Industrial information indicated that fuse reconduction failures appear early in life and therefore dynamic burn-in test is an effective means for culling out defective parts due to reconduction. This was not supported in a limited burn-in test conducted during this study which did not show any failures. However, a 125°C ambient 800 hour operating test did result in reconduction failures at 140 hours and 648 hours. If an early mortality region exists, it probably extends to many hundreds of hours. In other words, the decreasing failure rate versus operating time characteristics might be rather gradual. This is not surprising as it is recognized now that monolithic devices have a decreasing failure rate characteristic extending

through many thousand hours. Even with a gradually decreasing failure rate curve benefits obtainable from burn-in tests are still significant. In order to maximize the effect, dynamic burn-in testing should be performed after programming, so that the defects on both the circuits and the programmed fuses may be culled out. Long operating tests under accelerated environmental conditions using a large device sample to determine the exact benefits of burn-in is recommended.

Reliability

1. In the early years of PROM application, burn-in played a very important role in maintaining sufficient reliability in PROMs even for commercial operations. Recent information indicates that the failure rates are sufficiently low so that burn-in testing is no longer economical for commercial applications. The bulk of the failure rate information collected in this study was on nichrome technology which was the most widely used PROM technology. The overall failure rates for 1K PROMs in commercial applications ranged from 5 failures/10^6 hour for the first months of operation, 1.5 failures/10^6 hours for the first 6 months of operation to 0.5 failure/10^6 hours for long term steady state conditions. A failure rate for roughly level "C" 1/2 K NiCr PROMs under airborne condition was reported at 4.5 failures/10^6 hours, with a projected steady state failure rate of 2.5 failures/10^6 hours.
2. Analyses done on opened nichrome fuses indicate that a very narrow gap could exist under electric current deprived conditions to the fuse. This kind of gap would tend to reconduct probably due to electrical and thermal breakdown in conjunction with melting of the nichrome at the gap ends. By means of the "freeze-out" test it is believed that electro-corrosion of nichrome fuses and possibly other types of fusible links can be kept to an insignificant amount. By means of optimum programming and burn-in plus high and low temperature electrical tests after programming, the failure rates contributed by both the ciruitry and the fuse links can be kept to a level comparable to contemporary MSI parts. The comprehensive and simplified failure rate models developed reflect these concepts. It was estimated for year 1975 the 1K to 2K NiCr PROM fuses could contribute 2 to 20 percent of the total device failure rate depending on methods of programming, screening, etc.; for long term condition their contribution could be in the 2 to 5 percent region.
3. Since data on Ti:W PROMs was only available from a limited amount of commercial users, little field data and screening information was obtained. Preliminary comments from these users did indicate a favorable opinion of titanium-tungsten as a memory element. Analysis conducted during this study and user data supplied was limited to 1024 bit open collector Ti:W PROMs in plastic encapsulated devices. It is anticipated that mil temperature range devices in hermetic packages will be available in late

1975. At that time it is recommended that freeze-out and water-drop tests be conducted to evaluate their effectiveness. No failures due to electrocorrosion were identified or obtained during this study.

4. For AIM PROMs the failure data indicated that the contribution of memory elements to the total failure rate was negligible. The information was dominated by one data source. A definitive conclusion cannot be drawn at this time.

5. The quantity of PROMs being used is increasing very rapidly. A great deal of field reliability data should become available soon. Contacts with all users should be maintained to update the failure rate information. This information coupled with additional programming, screening, burn-in and life test data can be used to validate the failure rate models developed.

9.0 RECOMMENDATIONS FOR FUTURE STUDY

Much significant information on three types of PROM technologies has been developed in this study. However, many of the interesting facts brought out more questions than answers. In depth studies will be required in many areas before the questions can be answered. The following are recommendations on future studies for answering some of the questions.

1. Circuit, Topography, Programming and Test Study

   The key programming variation lies in the amount of current reaching the memory element. This current is affected by the programming circuitry, circuit path impedance which is related to the chip topography and programming methods including factors of pulse rise time, pulse duration, multiple pulses, etc. Detailed analyses should be conducted to quantify the variations in programming energy flow due to the various causes. A necessary consideration will be the effect of the temperatures encountered in programming on the performance of the circuits and the necessary guard-banding required in room temperature testing.

2. Fusing Element Failure Mechanism Study

   The present study revealed that the physical appearance of a programmed fuse is related to the programming schedule used; and the appearance is related to probability of failure. In addition to the physical appearance an insight into the exact failure mechanism is needed. Analytical techniques such as ion backscattering, secondary ion mass spectrometry, Auger electron spectroscopy, photoelectron spectroscopy and electron spectroscopy for chemical analysis should be utilized to identify the composition and chemical state of the fused regions of the memory elements. Once the failure mechanisms are defined the ability of existing tests to uncover, aggravate or accelerate the failure mechanisms should be determined in order to provide additional tests and criteria that will cull out unreliable parts.

3. Analysis of Circuit Breakdown During Programming

   Anomalous step rise transients have been observed in the programming current waveforms of fusible link PROMs which are believed to be due to junction breakdowns in the decoders or enable circuitry. These are often observed in difficult to program devices and may interfere with the programming of the device by diverting current away from the selected memory element. The offending junction must be identified. If possible, probe measurements of the internal test transistors should be made in order to correlate the characteristics to the breakdown phenomena. Means for avoiding breakdown problems such as special programming procedures,

screening tests and control of chip temperature during tests should be investigated.

4. Study of Adequacy of Fuse Passivation

Electrocorrosion of fusible links due to moisture penetrating through cracks and pinholes in the passivation is one of the major failure modes on nichrome fuses and possibly other fuses. The adequacy of the fuse passivation for moisture protection needs to be investigated. Pinhole detection methods such as electrolysis bubble detection, electrochemical etching and specimen current mode of SEM might be used to inspect the state of the passivation film. If possible field evaluation of the manufacturer's methods should be made. This should include the identification of the materials and processes used for passivation and evaluation of the procedures for maintaining contamination free deposition and packaging.

5. Burn-in and Life Tests

The limited data from the present study does not reveal a clearly discernible optimal burn-in duration for culling of potential failure. A planned experiment should be performed with more devices which should be life tested after being subjected to varying lengths of burn-in at various temperatures. This effort should be aimed at correlating the burn-in effects with the failure mechanisms.

6. Inclusion of More PROM Technologies and Types

The study conducted was limited to the evaluation of 1024 bit PROMs from three technologies. More PROM technologies and higher bit capacity devices are now becoming available. It is recommended that with respect to the efforts recommended more PROM technologies, such as the polysilicon fuse technology, should be included in the study and more complex devices such as 2048 bit and 4096 bit PROMs should be used as evaluation vehicles.

APPENDIX A
PROM USER AND SUPPLIER EXPERIENCE DATA

The following experience data are segmented into three technology categories:

1. Nichrome Fusible Links
2. Titanium-Tungsten Fusible Links
3. Avalanched-Induced Migration (shorted-diode).

The data on each technology represent information gathered from several users and in one case from a PROM manufacturer. Since PROM production lots and calendar times are different for the user, it is expected that conflicting data and conclusions might exist. Publication of this information should not be interpreted as an endorsement or rejection of any particular manufacturer or technology but rather as a basis for understanding the evolution of various PROM technologies. Data contributed by various users and manufacturers to a State-of-the-Art survey of PROM Failure Modes meeting, held at the 1974 (Oct. 23-24) Reliability Analysis Center (RAC) Workshop, Rome, New York, have also been included in each technology segment.

Nichrome Fusible Link Technology

RAC meeting - contribution of users and manufacturers

1. Device programmability - programming yield
   a. Misprogrammed fuses result from internal breakdowns or leakage paths providing access to multiple fuse locations.
   b. Fuses that will not program reflect an internal circuit leakage or breakdown condition shunting the necessary programming current away from the selected fuse.
   c. Slow programming fuses reflect some conditions as fuses that will not program and result from poor process control of fuse physical dimensions.

2. Reappearing bits - fuse "grow-back"

a. Normal Fuse Parameters

(1) Unprogrammed resistance 10^2 ohm

(2) Programmed resistance greater than 10^6 ohm

b. "Grow-Back" Fuses Parameters

(1) Resistance range 10^3 ohm

(2) Exhibit excessive leakage currents

c. Conditions for "Grow-Back"

(1) Only under inducement of a voltage potential across gap region within a few volts of the breakdown voltage of the gap.

(2) Phenomenon is considered to be an early mortality fallout, failure within first 168 hours at ambient temperature.

(3) A fuse will not grow back without first exhibiting a leakage current.

d. "Grow-Back" Dependencies

(1) Programming time

(a) Direct acceleration between "grow-back" and programming time.

(b) For $t < 1$ ms oxidation reaction is more complete because of melting of fuse.

(2) Time and Temperature - suggests higher growback percentage at higher temperature.

(3) Bias Voltage Across Fuse - bias voltage accelerates and increases probability of growback.

(4) Early Mortality Fallout - The devices failing during the early operational hours (168 hours), accounting for approximately 1 percent of the product, may be grouped into three categories:

(a) 80 to 95 percent - exhibit input/output shorts often caused by stressing a defective component during programming.

(b) 5 to 15 percent - mechanical failures, assembly, workmanship defects.

(c) 1 to 5 percent - "grow-back" fuses resistance values change caused by dendritic relinking.

(5) Remedies for "Growback"

(a) Decrease programming time and increase pulse magnitude.

(b) Reduce bias voltage across open fuse.

(c) Increase the margin between the programming current and sensing current.

(d) Perfect process controls and increase fuse uniformity.

3. Self programming bits.

a. Bits initially unprogrammed become programmed during operation.

b. Causes

(1) Passivation voids above fuse allow moisture to corrode and open fuse. Freeze Test can be used for culling.

(2) Fuses are electrically stressed during operation, causes opening of fuse.

User U. Data

Device programmability. Noncompatibility of unprogrammed PROMs - indeed PROMs may be pin compatible, but in many cases devices not only have different parameter limits but the unprogrammed (virgin) devices of one type contain Logic 0 in all locations, while the devices of another type contain Logic 1. This required two different test problems for incoming electrical inspection of devices.

1. Noncompatibility of Programmers. Another problem was programming itself; i.e., two different programmers were required. Subsequently, it was learned that as the PROMs are redesigned by the manufacturers, the programmers also must be modified. In some cases, the original programmer destroyed a newer version of a device, while a modified programmer would not program the older version of a device (or vice versa).

2. Device Programmability. During the original negotiations, the manufacturers indicated that almost all devices are programmable; only "once in a while a device would not program". However, a 5 to 10 percent rate of devices which did not program was quite common in many production lots as shown in Table A-1. Cooling of the devices during programming generally (and sometimes drastically) improves their programmability. In one particular instance, between 30 to 40 percent of devices would not program without cooling; when CO_2 cooling was applied, more than 90 percent of the unprogrammable devices would program.

TABLE A-1. PROM PROGRAMMABILITY

Manufacturer	Type	Programmability Range per Lot, percent
DD	1024	60-90
	1024	90-95*
	2048	85-95
EE	1024	Programmed by Supplier
	2048	88

3. Susceptibility of PROMs to oscillations. An additional problem, susceptibility of devices to oscillations, occurred at room temperature but was much more severe during the temperature testing. Thus a careful circuits layout and other oscillation suppressing techniques should be used, and all apparent failures should be investigated.

4. Programmer Sensitivity. Another programming problem was the sensitivity of a commercially available programmer to noise on the 115 volt power line. When the programmer and a blower (used for cooling of devices) were plugged into the same power line, the transients produced by the blower would cause a programmer to malfunction; in some cases, this resulted in the programming of wrong bits.

5. Unprogrammed Test Fusible Links - Switching Characteristics. Generally, the switching characteristics (i.e., access time) cannot be tested on PROMs before programming. Various correlation

*Yield was increased due to redesign of device.

techniques are used to guarantee these characteristics. However, such techniques are not infallible and errors may occur as illustrated by the following example. In addition to the 1024 fusible links required for device operation, Manufacturer DD had additional links in the PROM. These links enabled additional electrical testing of the device. After the special testing was completed, the extra fusible links were blown open, thus testing the device for programmability. Because of an error in the manufacturing flow, some PROMs were not subjected to a complete test fuse blowing. Unprogrammed devices with the unblown test links passed normal testing but failed access time after programming. The manufacturer notified the user of this problem and sent their representative with equipment to correct the error. This example indicates the importance of performing a complete test on PROMs after programming.

6. Leakage Current Failures at Temperature Extremes. Two evaluation devices from Manufacturer EE failed during the initial measurements at high temperature (T_C +125°C). The output leakage current of both units considerably exceeded the maximum specification limit of 100 micro-amperes. However, both devices remained operational after conclusion of testing. Failures of this nature can be expected on any microcircuits which depend on guard-banding of room temperature testing (and are not tested 100 percent at temperature extremes by the manufacturer). The obvious solution for this type of failure is a 100 percent electrical testing at temperature extremes. However, this is rather costly and time consuming, and therefore should only be used in critical applications.

Reappearing Bits on 1024-bit PROM from Manufacturer DD. The malfunction of some devices manifested itself in some bits which appeared to be programmed initially but would revert to the unprogrammed state either after a few hours of operation or when the device was exposed to high/low temperature. Manufacturer DD admitted an apparent recover (1 to 2 percent) of a small number of devices caused by an incomplete opening of the nichrome fusible links. Approximately 2 months before User U contacted

the manufacturer, a new process was instituted in manufacturing that eliminated this problem. Also, for devices of the prior manufacturing vintage, an equally effective electrical screen (verification of programmed pattern at approximately 4 volts) was developed. Generally this type of failure was felt to be caused by regrowth of the blown fusible links; in actuality, the failure occurred because of incomplete programming.

Because of the design of the device, the current through the link is inversely proportional to the temperature of the device. Thus, if the device is at a high temperature or the programming pulse is applied slowly, the current density required to open the link will never be reached and the device will not be programmed correctly. Sometimes the current density is sufficient to change the link resistance to produce a logic 1 at the input to the buffer gate but not high enough to open the link completely. The device will appear as properly programmed initially but may recover to the unprogrammed state if the resistance of the link decreases sufficiently, by annealing to such an extent as to cause a logic 0 at the input to the output buffer.

The new process developed by Manufacturer DD was a tighter control of the cross-sectional area of the fusible link. This control ensured that the current density necessary to open the link was always reached with a correct programming pulse. The screen for devices of the old vintage consisted of an application of a bias to the test fusible links contained in each device. The manufacturer's test results on the old process devices indicated that the annealing prone devices failed very early in life, and the screening time duration of 8 hours was sufficient. In addition, verification of programmed pattern should be performed at a reduced power supply voltage (approximately 4.0 volts). The corrective actions undertaken by the manufacturer appeared to be 100 percent effective in elimination of this problem.

Self Programming Bits. Fusible link and programming problems occurred with 2048-bit PROM from manufacturer DD. Only one of these failures was related to a fusible link and was a result of a void in passivation over the fuse caused by photolithographic defect. Penetration of moisture through the void caused a corrosion of nichrome film and self-programming of the corresponding bit.

Silver Dot Contamination. Manufacturer DD made a double connection between the external ground pin (No. 8) and the silicon die. Both connections were made with 1 mil aluminum wires. One wire connected the ground pad on top of the die with the pin. The second connection was made to the bottom of the die. To facilitate bonding, a silver dot was placed on the metalized internal surface of the package (electrically connected to the bottom of the die) to which the aluminum wire was bonded. This silver dot in some lots of the packages had been contaminated by chlorine, which caused aluminum corrosion (it should be noted that when the ground wire was open, the device appeared to be misprogrammed rather than unprogrammed). For the future, Manufacturer DD redesigned the construction of the device replacing the silver dot with a silicon chip.

To determine the risk involved with the use of the silver devices, the manufacturer performed intermittent operation life tests. No failures occurred on the original 108 devices (three groups of 36 units each) subjected to testing. These devices operated over 500 hours. Three devices failed as a result of wire corrosion on two additional groups of devices (210 units and 167 units) subjected to a similar test. These groups of devices also operated for 500 hours; two failures occurred during the initial 48 hours of operation. The third failure occurred between 48 and 72 hours of operation. Based on results of this testing, an effective screen is to subject all silver dot devices to an intermittent operation (power cycling) burn-in at an ambient temperature of $-10^{\circ}C$. The low ambient temperature is necessary to stimulate corrosion produced by the residual trace amounts of moisture in the package in the presence of chlorine, which acts as a catalyst.

The best way to detect ground whisker (pin 8) corrosion failures (opens or high resistance) is to pass a relatively high (approximately 10 milliamperes) current through the isolation diode associated with the substrate. A positive voltage (current limited) is applied to the ground pin 8 and a negative voltage to an input pin. If the voltage drop exceeds 0.9 volt, the bond contact resistance is excessive (or the device is abnormal for some other reason) and the device should be rejected.

User W Data - (Commercial 1024 PROMs)

Device Programmability - incoming inspection dc testing (90 ns access)

1. Vendor G Date Code 7402-7432
   a. 34,076 parts tested/Rej. 1587/4.66 percent
2. Programming and AC Test
   a. Vendor G Date Code 7428-7432
   b. 12,133 parts tested/Prog. Rej. 1457/AC Rej. 474/12.0 percent Prog. Rej./3.91 percent AC Rej./15.91 percent Total
3. Manual Programming
   a. Vendor G - 950 parts/17.6 percent Prog. Rej.

Reappearing Bits

1. Burn-in statistics (experiments)
2. Design of Experiment. The three objectives in this burn-in are given below:
   a. Knowing "healing" is an infant problem, burn-in is in effect an accelerated life test, which will provide the statistics on "heals" (as well as healed samples for analysis).
   b. By using different temperature-time burn-in screens, the level of required burn-in can be determined.
   c. By using a low temperature cycle, the electrochemical attack problem, as studied by RADC can be checked. To achieve these objectives, the PROMs are divided into three approximately equal groups: group one is not burned-in and is used as a control group; group two is subjected to a 70°C oven temperature, 8-hours burn-in screen (V_{cc} at 5.0 V); and group three is subjected to a 90°C-0°C-90°C, 22-hour screen (V_{cc} = 5 V). This third screen is severe and includes the low temperature cycle for moisture condensation-chemical attack problem.

      The decision to do burn-in was made on 24 October 1972 and the task was to start on November 20th. The burn-in was to be done on the "new process" Vendor G PROMs only (date

code 7242 or later). As of 23 February 1973, a total of 698 parts were screened. (User W changed the screen 2 temperature from 70°C to 90°C on 3 January 1973 after the burn-in results up to that time were considered.)

3. Burn-In Test Data. The test data are summarized below:

a. Programming rejects:

(1) Average = 7.4 percent for date codes 7242, 45, and 46.

(2) For 7242, reject rate = 8.4 percent (30 devices tested).

(3) For 7245 and 46, reject rate = 6.9 percent.

Note: The programmer used multiple (four) 10 ms pulses. Lots with higher reject rates implied slower average blowing times.

b. Failures due to screening:

(1) Control group (verified after 24 hours): 0 failures.

(2) Screen 2 (low level, 8 hours): 0 failures.

(3) Screen 3 (90°C-0°C, 22 hours): 4 failures.
(or 1.7 percent)

Of the four failures, three were caused by other than healing (human error in programming: one device; damaged circuits: two devices. The latter cases probably were due to human error also). One failure was due to healing as verified by reblowing, etc. (device AB31).

c. Field failure returns: As of 26 February 1973, the following field returns were obtained:

(1) Screened parts:

(a) AC21, was subjected to 70°C 8-hour screen. One fuse healed.

(b) AJ31: problem was circuit speed, not fuse.

(2) Unscreened parts:

(a) No new process PROMs healed in the prototype systems.

(b) Ten of the "old process" PROMs returned from Systems were believed to be healers.

It should be noted here that the two "new process" PROM heals, both belong to 7242 date code: the early Vendor G "new process" devices.

4. Conclusions. The following observations were made:

   a. If it is assumed the 90°C burn-in is effective, and, therefore, the single failure due to healing (AB31) represents the only potential healer, it is concluded that 0.3 percent of the new process PROMs heal. (Obviously a single heal does not exactly inspire confidence in the conclusion).

   b. If all the healers of the 698 new process parts have been detected (2: AB31 and AC21), it is concluded that 0.3 percent of the PROMs heal.

   c. At least for the "new process" PROMs, a 70°C 8-hour screen is not sufficient to weed out potential healers. A more severe screen is needed. (The 90°C screen is seemingly effective).

   d. For the "old process", another user has seen as much as 3-5 percent PROMs heal, User W roughly 1-2 percent devices heal. The "new process" showed ~0.3 percent heals. Clearly the "new process" is significantly better. (According to the manufacturer the "new process" involves no fabrication process changes. The fuse mask has been altered, quality control has been tightened to ensure more uniform, faster programming).

   e. Both heals come from lot 7242, after Vendor G has just introduced the new process. It is possible that the percent healers for the later lots are even lower. However, this is a mere conjecture.

Self-programming Bits. Because no failures have occurred due to electrochemical attack, User W believes that this problem no longer exists with Vendor G PROMs.

Update of Information From User W

1. Field Experience Data. As of March 1975, user W has utilized 29,000 (1024 bit) PROM devices from Vendor G, with total device

hours estimated at 76×10^6. These commercial devices were operated in an ambient laboratory environment ($20^{\circ}C$). Ninety failures were experienced, with one-third undergoing failure analysis. The analysis reflected a contribution to the failure rate in the following proportions.

a. Failures associated with regular IC processing = 0.22 percent of all parts.

b. Failures associated uniquely to reconduction of nichrome fusible links = 0.09 percent of all parts.

A reconduction loss of 0.09 percent is considered very low since it was experienced on commercial devices (no burn-in), and numbers of this magnitude are very sensitive to PROM circuit design and vendor process controls. This corresponds to a failure rate of 0.4 failure/10^6 hours for reconduction.

2. Contamination Problem - A bad lot of 1K PROMs was experienced in late 1973. The problem was identified as:

a. A significant portion of that date code had serious copper contamination on the fuse link.

b. Copper contamination was verified by the manufacturer and was traced to a photo-resist operation. The manufacturer cured the problem. However, they did not purge the stock completely and some devices were shipped.

c. Parts of the same bad lot also showed silicon wafer (die) cracks.

d. Failure percentage for this lot is much higher: 0.6 percent failed due to reconduction (versus 0.09 percent); 0.6 percent failed due to IC failure mechanisms (versus 0.22 percent).

e. Parts in the field numbered 4000, which were of the bad lot date codes and experienced a failure rate of 1.7 failures/10^6 hours for reconduction.

User X Data (883 Level B Equivalent PROMs)

Device Programmability (Vendor H). The 1974 programming data are given in Table A-2. The 2K PROMs programmed by the vendor are listed in Table A-3.

TABLE A-2. 1974 PROGRAMMING DATA

Virgin 1K PROMs		Programmed by Vendor 1K PROMs	
Total received	1399	Total received	2728
rejected	283	rejected	325
Will not accept program	10.3 percent	Electrical at -55°C	3.6 percent
Electrical at 25°C	1.4 percent	Vol 5 V at -55°C	1.6 percent
Electrical at -55°C	2.1 percent	Vol 4.5 V at -55°C	1.6 percent
Vol 5 V at -55°C	1.0 percent	Hard to program (update)	0.1 percent
Vol 4.5 V at -55°C	3.3 percent	Program Errors	5.1 percent
Program Errors	2.6 percent	Lost in test	0.3 percent
	20.7 percent		12.3 percent

TABLE A-3. 2K PROMs PROGRAMMED BY VENDOR

Total Received	774	
Rejected	99	
Electrical at -55°C		0.12 percent
Vol 5 V at -55°C		0.90 percent
Vol 4.5 V at -55°C		11.3 percent
Lost in Test		0.36 percent
		12.68 percent

Reappearing Bits (512 PROMs). "Heals" per se have not been seen, although some "leakage at output" has been noted. The percent of devices failed at screening was about 10 percent. The percent due to healing is not known. In October 1972 parts were programmed and burned-in by Vendor G. Fuses healing on Vendor G 1024 PROMs, of date codes 72-39 through 72-42 have been noted.

Self Programming. No failures occurred because of the electrochemical attack of fuses.

Other. Before 73-40 date codes on 2048 PROMs from one vendor, several failures were experienced because of silver-dot contamination from residuals of chlorine chemicals.

User T Data - (Commercial PROMs)

Device Programmability. No data supplied.

Reappearing bits

1. Experience on old Vendor G process only
2. During 1971, about 500 parts of Vendor G 512 bit PROMs were used and no problems occurred.
3. To date 40-50,000 Vendor G 1024-bit PROMs have been used. Serious problems resulted in programming rejects and healing.
4. Healing appears to be an infant problem and occurs within 2-6 hours at 70°C with V_{cc}.
5. High temperature storage at 150°C and 200°C without V_{cc} did not bring out heals.
6. Burn-in after programming is "effective". "Less than 1 percent PROMs after passing burn-in screen still heal in the systems. The burn-in catches as much as 4-5 percent, depending on lots. The burn-in screen used is 55°C for 8 hours with V_{cc}.
7. Now burning-in all PROMs.
8. The "healing" problem exists for other NiCr PROM vendors also.

9. Healing has not been studied in terms of mechanisms, etc., and as functions of blowing time, bias voltage, temperature, etc. Trouble was not expected because of favorable experience with the 512-bit PROMs. The problem was discovered when in pilot production. Burn-in after programming had to be instituted and fortunately, it was found to be adequate as an interim solution.

Self Programming Bits

1. No unblown fuse reliability problems have occurred.

User Q Data (Commercial Mil Level 512 Bit PROM)

Device Programmability. No data.

Reappearing Bits. No data from use.

Self-Programming Bits. No data from use.

Special Tests

1. Freeze-out Test. The freeze-out test was performed in accordance with 4.3.e of the proposed MIL-M-38510/201 specification. It stipulates preconditioning at +125°C, electrical connections per test condition C of method 1015 of MIL-STD-883 cycled on and off at 3 minute intervals, 5 hours minimum at -10°C, and functional electrical tests after allowing the parts to slowly return to room temperature while still under cycled bias. Three groups of devices were tested per the summary in Table A-4.

2. Water Drop Test. The water drop test was performed in accordance with 4.4.3.g of the proposed specification. It consisted of placing a drop of high resistivity deionized water on the die while it was electrically functioning. The parts in Group I and Group II during the freeze-out tests were all subjected to the water-drop test. The devices in Group I and II were tested per the summary in Table A-5.

TABLE A-4. FREEZE OUT TEST RESULTS

Group Number	Package Type	Number of Devices	Length of Test, hours	Number of Failures	Additional Tests
I	Metal and ceramic flatpak dielectric isolation	6	24	0	All devices were opened at end and temperature cycled in 15 percent humidity resealed
I	Repeat	Same Parts	24	0	
II	Ceramic package junction isolation	2	1000	0	All devices were opened at end and temperature cycled in 40 percent humidity resealed
II	Repeat	Same Parts	52	0	
III	High Reliability	45	8	0	
	Commercial	35	8	0	
	Commercial	20	8	0	

TABLE A-5. WATER DROP TEST RESULTS

Group Number	Package Type	Number of Devices	Effects of Test
I	Metals and ceramic flat package dielectric isolation	6	1. No electrical failures 2. Aluminum interconnections wires opened on several devices. 3. Cracks in glass passivation layer of two devices - partial etching of aluminum metallization beneath the cracks
II	Ceramic package junction isolation	2	1. One device failed open after 30 seconds (open metallization on die) 2. Cracks in glass passivation layer 3. Aluminum metallization and NiCr affected

Conclusions. The conclusions reached are summarized below:

1. The devices under test were capable of passing the freeze out test as stipulated in "the proposed military specification."
2. The presence of large amounts of moisture does not in itself result in freeze out failures (15 to 40 percent).
3. Because one part which had a cracked glass overlay on the die passed 52 hours of freeze-out testing with 40 percent relative humidity in the package (later failing the water-drop test), it is concluded that the freeze-out test is not an effective screen for cracked glassivation even if the package has excessive moisture. The water drop test is capable of detecting cracks in the glass overlay. The aluminum metallization is apparently at least as susceptible as the NiCr links to failure during this test. If this test is applied to PROMS with NiCr links, it should also be applied to all integrated circuits that use aluminum die metallization. However, the glass overlay is not primarily intended to be a moisture barrier but a protection against small particulate contamination. Cracks in the glassivation are not sufficient cause to reject a lot. For these reasons, the water drop test is not considered a suitable criterion for PROM lot acceptance.

User V Data (Mil 512 Bit PROM)

Device Programmability. Devices programmed by the manufacturer were found to be incorrectly programmed during system checkout. All devices in stock were found to be misprogrammed. The problem was traced to a malfunctioning switch on the vendor's programmer. The exact number of faulty programmed devices is unknown.

Reappearing Bits/Self-Programming Bits. No reappearing bits or unblown fuse reliability programs occurred in 1.3×10^6 part hours of operation.

Screening Employed. The devices are 100 percent screened per Table A-6. There are 168 hours of assembly conditioning cycled from $+115^{\circ}C$ to $-40^{\circ}C$. The temperature/time parameters are given in Table A-7.

TABLE A-6. ASSEMBLY CONDITIONING PROFILE PARAMETERS

T_U (°C)	D_{T_U} (Minutes)	T_L (°C)	D_{T_L} (Minutes)
+115	0	-40	0

T = Temperature
D = Dwell Time
U = Upper
L = Lower

TABLE A-7. MONOLITHIC MICROCIRCUITS – 100 PERCENT SCREENING

	Test/Inspection	Description of Test/Inspection	Duration	Temperature
1.	Internal Visual Inspection (Precap)	MIL-STD-883, Notice 2, dated 20 November 1969, Method 2010.1, Condition B	X	X
2.	High Temperature Storage	Non-operating Temperature Storage, MIL-STD-883, Method 1008, Condition C, Non-operational	24 hours	150 ± 5°C (ambient)
3.	Temperature Cycling	Non-operating Temperature Cycling, MIL-STD-883, Method 1010, Condition C	10 cycles	-65°C to +150°C (ambient)
4.	Constant Acceleration	MIL-STD-883, Method 2001, Condition E, Y1 Axis, 30K g	X	X
5.	Seal Leak Test (Fine)	MIL-STD-883, Method 1014, Condition A or B, reject leak exceeding 1 x 10^{-8} atm/cc/second	X	X
6.	Seal Leak Test (Gross)	MIL-STD-883, Method 1014, Condition C or D	X	X
7.	Pre Burn-in Electrical Parameters	Critical DC electrical parameters measured	X	X
8.	Burn-in Test	MIL-STD-883, Method 1015, high temperature reverse bias and/or maximum power, depending on device type	168 hours	125°C minimum (ambient)
9.	Post Burn-in Electrical Parameters	Critical DC electrical parameters measured	X	X
10.	External Visual	MIL-STD-883, Method 2009	X	X
11.	Final Electrical Measurements	DC characteristics and selected AC parameters	X	25°C (ambient)

X = Indicated Test/Inspection is to be performed as defined under "Description of Test/Inspection".

Unit aging is conducted for a minimum of 48 on-hours with temperature cycling from -40°C to +83°C.

The 1.3×10^6 hours operating time includes device burn-in, assembly conditioning, unit aging, system burn-in, and system operation of the equipment.

Manufacturers Data (Vendor B)

Device Programmability

1. Programming. Several phenomena associated with programming are misprogrammed fuses, those that will not program, and slow programming devices. Together these account for most of the programming yield loss.

Misprogramming is chiefly due to internal breakdowns or leakage paths and provide access to multiple fuse locations. This has been reduced in current Vendor B PROM designs by special in-process testing and lowering the required programming voltage at the output. In the past, misprogramming was partially due to the vendor's inability to perform a complete decoding check at the package level on an unprogrammed device. Although extra test "word" and "bit" lines were incorporated on the chip, they were only accessible through extra probe pads on the die itself and could not be bonded out in the packaged form for lack of sufficient pins. The current designs do not have this problem because an advanced multiplexing concept is used in two of the input pins enabling a check of decoding on the package level as well as at wafer sort. This feature also allows access to a pattern of test fuses that are blown on the package level to check out the programming characteristics of each device. One input pin also allows V_{OL} testing on the unprogrammed device by turning on all four outputs.

Fuses that will not program usually reflect an internal circuit leakage or breakdown condition shunting the necessary programming current away from the selected fuse. Devices which program very slowly usually exhibit a similar lack of programming current for much the same reasons but the condition is only marginal. The slowness is relative for each programmer and its pulse train.

The occurrence of these phenomena has been greatly decreased in the current revision by improving the design, reducing the die size, and implementing special in-process tests.

2. Verification. After successful programming, the device should be tested to see that it conforms to the entire device electrical specification. High programming voltages may have accelerated the failure of marginal components in the circuitry. Therefore, after final testing one might expect some small additional fallout, usually less than 1 percent.

Early mortality fallout, that fraction of the devices failing during the early hours of operation, may be grouped into three categories:

a. 80-95 percent of the population of defective devices will exhibit input/output shorts; sometimes due to stressing a defective component in the circuit during programming.
b. 5-15 percent mechanical failures: typically assembly oriented workmanship defects.
c. 1-5 percent "grow-back"; where improperly programmed fuses change resistance value due to dendritic relinking.

It is important to note that the combined early mortality failure modes only account for 1 percent of the product, a figure much less than many conventional integrated circuits.

Reappearing Bits (Grow-Back)

1. Characteristics of "Grow-Back". In the vendor's failure analysis laboratory devices which failed in this mode have been extensively examined. Normally blown fuses display resistance >2 megohms. Careful probing through silox passivation to the aluminum on either side of the grow-back fuse has shown that all the failing fuse resistance values fall between 900 and 2000 ohms. These values are much higher than the 350 ohm value for an unprogrammed fuse. The output load characteristic was found to reflect this "twilight" fuse resistance region by sometimes appearing "on" (logic low) at high V_{CC} and/or high temperature and "off" (logic high) at low V_{CC} at low temperature. Varying the load on the output also had an effect on this transition from one state to another. Thus it becomes evident that some sort of low temperature or low V_{CC} test is necessary to detect this type of

failure. If by chance, the device is operated near the transition, the failure mode might appear as an oscillating bit. The reason for these V_{OL} effects is simple; the sense circuitry threshold levels overlap the region of "Grow-Back" fuse resistivities.

2. Cause of the Phenomena. During Vendor B's investigation as why fuses failed in this particular mode, only one of the many variables was consistently linked with "grow-back" failures, i.e., programming difficulty. Parts that would program very slowly (4-5 minutes) and which heated up in the process would invariably have a high incidence of failure, up to 2-3 percent.

To study the phenomena further, a test chip was designed to which fuses processed identically to the actual device were bonded to outside package pins. This enabled programming conditions at the fuse to be varied and the probability of "grow-back" under different stress conditions to be monitored. The results are summarized below:

a. Fuses that "grow-back" do so only under the inducement of a voltage potential across the gap region of the fuse within a few volts of the breakdown voltage of that gap.

b. Temperature cycling or high temperature storage did not induce failure and, therefore, cannot be used to screen out potential failures.

c. Most failures occur within the first 100 hours at room ambient under a stress of a few volts.

d. The "grow-back" fuses are always around 1000-2000 ohms and are easily reblown at currents typically below 1.0 mA.

e. The higher the breakdown voltage of the gap, the lower the probability that "grow-back" can ever take place no matter what potential is applied across the gap. Above a 20 volt breakdown, the effect virtually disappears. Blown fuses that demonstrate subsequent low voltage breakdowns in the gap region, around 0.5 - 2.0 volts, invariably grow back, when a field is applied, sometimes in milliseconds.

f. Limiting the rate at which programming current is available would always cause fuses to exhibit very low breakdown voltages across the gap region.

g. On fuses that opened on a fast rise time pulse (10 ms) the fuse resistance approached infinity almost instantaneously, whereas slow rise-time pulses (20 ms) exhibited an unstable slow decay characteristic lasting some 6 ms. The latter was generally associated with fuses that had a high probability of "grow-back" under an applied field. SEM inspection of such fuses exhibit unremoved metal in the gap regions.

h. Fuses without silox, exposed to air, could never be blown slowly enough to give low breakdowns in the gap region or display the attendant "grow-back" phenomenon. This suggested that oxidation may be an important mechanism of programming.

i. Fuses without silox exposed to forming gas, nitrogen-hydrogen mixture, a reducing atmosphere, grew back much more easily than those with silox under similar programming conditions. This supports the contention that oxidation plays an important part in the blowing mechanism at high dE_p/dt, i.e., fast blowing conditions.

The implications of these observations were extrapolated using actual devices in an exhaustive product engineering analysis that led to the following observations:

a. The devices which failed in the "grow-back" mode exhibited either a current limiting condition within the PROM circuitry or were current limited by the programming equipment. In any case, a definite correlation with limited programming energy was observed.

b. The maximum voltage across a fuse during normal operation would be no more than 2.9 volts and would occur only at a V_{CC} of 5.5 volts and only when certain bits were addressed. Not every blown fuse would see this stress level unless all addresses were clocked using a counter or some other random pattern generator.

c. It followed that the best screening for surfacing potential "grow-back" failures was a dynamic burn-in at maximum rated V_{CC}

and at maximum rated operating temperature. The failures would be detected best by using a low V_{cc} = 4.2 V and a high I_{ol} (output load) of 12 mA while performing a functional check.

d. Devices should characteristically program on the rise time of the pulse if there is no current limiting factor. If the fuse does not program then, higher voltages should be tried to overcome the current limiting condition. Longer pulses would only serve to raise the programming energy by slowly raising the ambient temperature and this has been shown to have a similar effect as slow rise time of the voltage pulse; both contribute to low breakdowns in the gap region and invite "grow-back" failures.

e. The rise time of the programming pulse should not exceed 100 μs.

f. The device oriented mechanisms which limit current to the fuse were

(1) Low breakdown on reverse biased junctions which normally prevent programming current from flowing in unwanted paths.

(2) Failure of circuit designs to assure sufficient programming current under worse case conditions encountered in process variations.

(3) Low beta such that the multiplex transistor was no longer capable of supplying sufficient current.

(4) Random defects simulating above conditions.

3. Conclusions. It is evident, not only from these studies, but those of other independent researchers, that "grow-back" is a field induced mechanism in which metal dendrite formation occurs in the gap region of a blown fuse. The phenomena is limited to fuses blown such that the breakdown voltage of the gap region is a low 2 to 5 volts and does not appear in fuses with high breakdown voltages.

The study of "grow-back" phenomena has provided the following results:

a. The phenomena appears as an early mortality failure mechanism and does not impact long term life (MTBF) of the

device. Field experience of billions of device hours support this contention.

b. Potential early failures can be removed effectively by use of a dynamic burn-in at maximum temperature and V_{cc}, followed by a special functional test.

c. Using information gained from these studies, new revisions of all the PROM family have been made. The resulting devices have shown impressive preliminary performance results over their earlier predecessors with virtual elimination of the "grow-back" phenomena.

Further study of the kinetics of the "grow-back" mechanism is continuing by gathering data at accelerated conditions to determine activation energies. Programming studies are continuing along similar lines to characterize the mechanism of programming at both low and high values of dE_p/dt.

Present data suggest a model whereby fast blowing conditions, i.e., high dE_p/dt, cause the fuse to open by a rapid oxidation reaction with silox producing narrow fuse gaps with characteristically high breakdown voltages and high resistance "grow-back." Detailed physical and chemical analysis of the gap region to substantiate this model have been difficult because of the small gap widths involved, 1000 to 5000 Å, which are outside the realm of normal spectroscopic methods.

Titanium-Tungsten Fusible Link Technology

Today only one manufacturer employs Titanium-Tungsten fusible link PROMS. These PROMS have only been available since January 1974 in commercial plastic packages, thus historical data from major military users are very difficult to obtain. Only one industrial user could be found that used a significant quantity of these PROMs, but field data were quite limited. According to one distributor only a small quantity of devices had been shipped to industrial users in the Southern California area during 1974. The manufacturers have indicated that Mil-temperature ceramic package devices should be available in late 1975.

RAC Meeting - Contribution of Users and Manufacturers

1. Device Programmability
   a. No data
2. Reappearing Bits
   a. No evidence of grow-back phenomena
3. Self-Programmable Bits
   a. No evidence of electro-chemical corrosion
4. Other information
   a. Titanium-Tungsten Fuse
      (1) Ti = W fuse is thicker and has melting point twice as great as NiCr
      (2) A higher power level is required to open fuses at higher temperatures
      (3) High power and temperature result in an "explosive" fuse opening that might increase the possibility of metallization shorts.
      (4) The manufacturer is considering a change to silox to reduce splattering.

User Y Data - (1024 Bit Commercial PROMs Plastic Packages)

Device Programmability. The 1974 data are given in Table A-8. The loss during programming was approximately 10 percent.

TABLE A-8. DEVICE PROGRAMMABILITY DATA

	Week 29	Week 30	Week 31	Week 34	Week 35	Week 38	Week 40	Week 41	Week 42
TOTAL QUANTITY	7728	1484	1795	1795	979	295	725	1136	772
Percent Rejected at Programming	2.6	10.3	9.5	9.0	11.0	6.1	7.8	7.7	9.5
Percent Rejected Access Time	0.68	3.4	0.44	0.4	4.0	4.1	?	1.9	?
TOTAL PERCENT REJECTED	3.28	13.7	9.94	9.4	15.0	10.2	7.8	9.6	9.5

Reappearing Bits. Grow-back did not occur. The commercial devices were returned to the vendor for analysis. Devices reported as field failures, failed for other reasons than reappearing bits.

Self-Programming Bits. No field failures were caused by electrochemical corrosion.

Other. Predominant failures occur during programming were due to out-of-spec, access time measures, and failure to program.

AIM Programming Technology

RAC Meeting - Contribution of Users and Manufacturers

Device Programmability - Programming Yield. Misprogrammed fuses result from leakage or internal breakdowns providing access to multiple fuse locations.

Slow and non-programming fuses reflect insufficient programming current level. The characteristics of programming element are diffusion-dependent. The emitter-base avalanche breakdown is very repeatable. Programming conditions are fairly uniform.

Programmability data are given in Table A-9.

TABLE A-9. PROGRAMMABILITY DATA

User	Number Of Bits	Percent Programmable
A	256	85 - 95
B	256	98
A	256	90
B	1024	95
B	2048	90 - 92

The normally programmed memory cell contains a low-resistance ohmic contact in series with a diode (CB junction) between row and column address lines.

On collector-base junction breakdown:

a. Originally specs indicated application of 16 additional programming pulses after diode is started. Now reduced to four additional pulses.
b. Extra pulses assured EB junction breakdown (variations in EB junction breakdown voltages)
c. 16 additional pulses tended to over-program device and caused extended aluminum migration and CB junction short.
d. CB junction short produced effective shorts between unselected and selected word lines which increased sync current from word driver circuitry.

Reappearing Bits. There is no evidence of any reappearing bits. The emitter-base junction avalanche breakdown is apparently an irreversible phenomena.

Self-programming Bits. Bits initially unprogrammed become programmed during operation because

a. Emitter-base junction is electrically stressed
b. Memory cell sees a potential of only 5 volts during normal operation.
c. May be caused by extraneous current spike.
d. Junction characteristics may have been degraded by leakage during programming.

User Y Data

Device programmability. 1024 bits PROMs (1974 data codes) are given in Table A-10. Most failures during programming are due to extra bits programming.

Reappearing Bits. No failures were experienced due to reappearing bits.

TABLE A-10. DEVICE PROGRAMMABILITY DATA

	Week 29	Week 30	Week 31	Week 34	Week 35	Week 38	Week 40	Week 41	Week 42
TOTAL QUANTITY	1082	1251	2818	2218	1656	2456	3908	3183	3690
Percent Rejected at Programming	11.0	10.8	11.1	11.0	12.0	12.5	12.1	11.7	11.5
Percent Rejected at Access Time	0.55	0.24	0.35	0.3	0.5	0.12	0.12	0.38	?
TOTAL PERCENT REJECTED	11.55	11.04	11.45	11.3	12.5	12.62	12.22	12.08	11.5

Average -- Percent Rejected at Programming = 11.5 percent,
percent Rejected Access Time = 0.32 percent

Self-programming bits. Electrochemical corrosion is not a problem so far as the diode element is concerned but still can occur with aluminum metallization. No electrochemical corrosion failures were experienced.

User U Data

1. Device Programmability (256 Bit - 1972 Date Code)
   a. 256 bit 70 to 90 percent
   b. 256 bit 85 to 95 percent (increase due to redesign of programmer)
2. Reappearing bits
   a. No failures due to reappearing bits
3. Self-programming bits
   a. No failures due to electrochemical corrosion.
4. Other (1024 Bit PROMs)

Open Metallization. One evaluation device failed after 504 hours of life test operation (this device was programmed in a repeating binary code). Electrical testing indicated that the inoperative portion of the device was in the decoding network, and the device was returned to the manufacturer who used a Scanning Electron Microscope (SEM) to determine that the failure was caused by open metallization over an oxide step. The primary reason for the open metallization was a gross overetching during the metal etch operation. The manufacturer indicated that as a result of this failure the

wafer inspection procedure had been improved; it is now performed at 500X as well as 100X magnification. Also, SEM inspection of a sample of every wafer fabrication run after metal etch as a process monitor has been instituted. It appears that manufacturer's corrective action should be effective; however, no additional devices have been tested from this manufacturer.

User V Data (2048 Bit PROM)

1. Device programmability (1975 Date Codes)
   Programming Data Only
   a. Number Programmed 769
      Number Failed 41 (Loss 5.3%)
      Failures due to:

Extra bits program	(19)
Would not program	(14)
Overheat and will not program	(3)
Access Time	(5)
Total	(41)

2. No system operation data available.

APPENDIX B

CONTACTS FOR PROM USER INFORMATION

The individuals and organizations who have contributed information utilized in this study are listed in Table B-1.

TABLE B-1. CONTACTS FOR PROM USER INFORMATION

Name	Contact	Location
Transaction Data Systems	Bruce Walker	San Diego, California
Raytheon Company	Aaron Dermardersian	Sudbury, Massachusetts
Naval Ammunition Depot Crane	Dale Platteter	Crane, Indiana
Honeywell Info. Systems	Thomas Byrne	Phoenix, Arizona
Singer-Kearfott Division	George Ebel	Little Falls, New Jersey
Univac Defense Systems	George Anderson	St. Paul, Minnesota
Lockheed, Missile Division	Jack Craig	Sunnyvale, California
Hughes Aircraft	John Maguire	Fullerton, California
Litton Aeroproducts	Lou Privatera	Canoga Park, California
Information Storage Systems	Bob Foote	Santa Clara, California
DOD	Ed Fox	Washington, D.C.
Draper Labs	Don Powers, Kinzy Jones	Cambridge, Massachusetts
Westinghouse	Bud Focht	Baltimore, Maryland
IBM	Fran Austin	Owego, New York
General Electric	Gene Bushunow Paul Hartung	Utica, New York
Litton Ind.	Phil Eisenberg	Canoga Park, California
Sperry Rand	Tom Brennan	Phoenix, Arizona
Odetics	Dick Petit	Anaheim, California
Martin Marietta	Don Space	Denver, Colorado
Collins Radio	Wes Merryman Roger Mobley	Cedar Rapids, Iowa
Xerox Data Systems	Roger Mo	El Segundo, California
Motorola	Jim Black	Phoenix, Arizona
International Communication Sciences	Mike Roth	Woodland Hills, California
Digital Equipment Corp.	Pete Barratt	Maynard, Massachusetts
Hazeltine	Morris Rudis	Long Island, New York

APPENDIX C
SPECIAL EQUIPMENT UTILIZED IN THIS STUDY

The equipment utilized in the PROM Reliability Evaluation is described in this appendix.

Spectrum Dynamics Model 550 Memory Programmer/Verifier

The Spectrum Dynamics Model 550 Memory Programmer/Verifier (Figure C-1) is designed specifically for programming field programmable ROMs and for verifying all ROMs. The unique design and packaging concept gives great programming and verification flexibility. A tape reader, an output printer, and a multiple production programming station for individual-device or card-level programming augment the Model 550 to comprise the 500 Series programming system. Personality modules designed specifically for individual device types allow programming ROMs with different configurations and programming specifications. All pin-for-pin compatibility devices

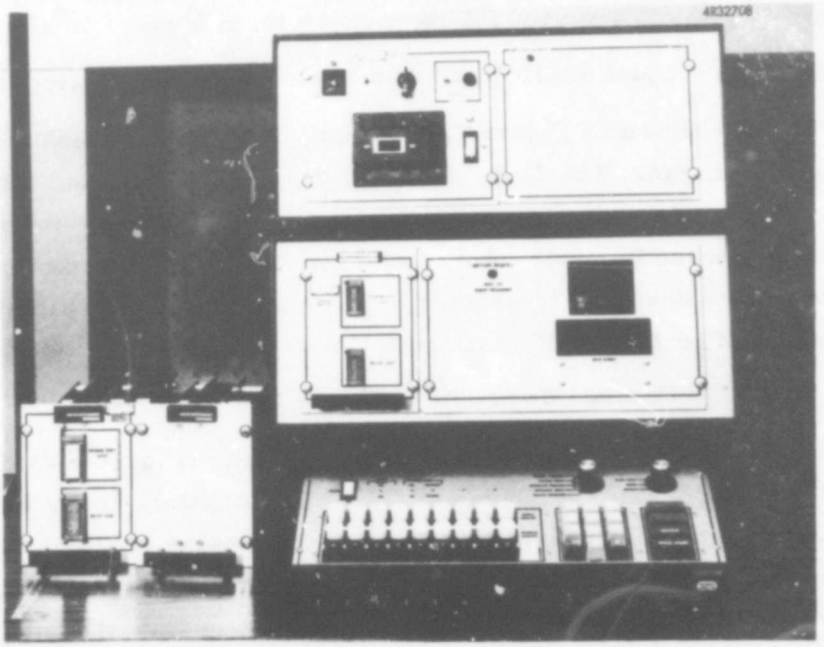


Figure C-1. Spectrum Dynamics Model 550 memory programmer and personality module adapter.

manufactured by various suppliers utilize similar programming techniques and the same personality module.

Clocked from a 10 MHz crystal-controlled clock, the Model 550 is a totally digital instrument. The clock, in conjunction with a frequency dividing circuit, provides accurate timing pulses to control all instrument logic functions to provide accurate program timing pulses, to guarantee precise duty cycles, and to supply test signals as required for each device to be programmed. The total digital approach enables the Model 550 to operate at maximum speed, cutting programming and testing time to an absolute minimum, as well as eliminating program errors.

Automatic programming capability extended by the tape reader, with scratch pad memory in the reader logic, allows storage of the next word while the Model 550 is programming and verifying previous sequence. The tape reader is equipped with logic that automatically checks the program format. It indicates an anomaly and stops input if the tape format is in error or the data selector gets out of sequence.

Various interchangeable personality modules readily adapt the memory programmer to each specific PROM manufacturer's specifications.

Cambridge Model S4-10 Steroscan Scanning Electron Microscope

The SEM shown in Figure C-2 is equipped with a lanthanum hexaboride (LaB_6) electron gun. The LaB_6 gun provides double the resultion of standard electron guns at the low accelerating voltages necessary for microelectronic device analysis and analysis of uncoated non-conducting specimens. The instruments are designed to provide high resolution topographical images from about 16X to 100,000X, with an ultimate resolution to 100Å.

Cameca Type MS 46 Electron Microprobe

The Cameca type MS 46 electron microprobe (Figure C-3) features four high resolution crystal spectrometers with five crystals under vacuum, the MS 46 was designed specifically to do analytical x-ray analysis and is not a compromised combination instrument. The spectrometers are all fully focusing, of the Johan or Johonnson type, and a time share computer station is available for quantitative reduction of data. Analysis can be performed in a variety of modes, including: line scanning, step scanning, X-ray and

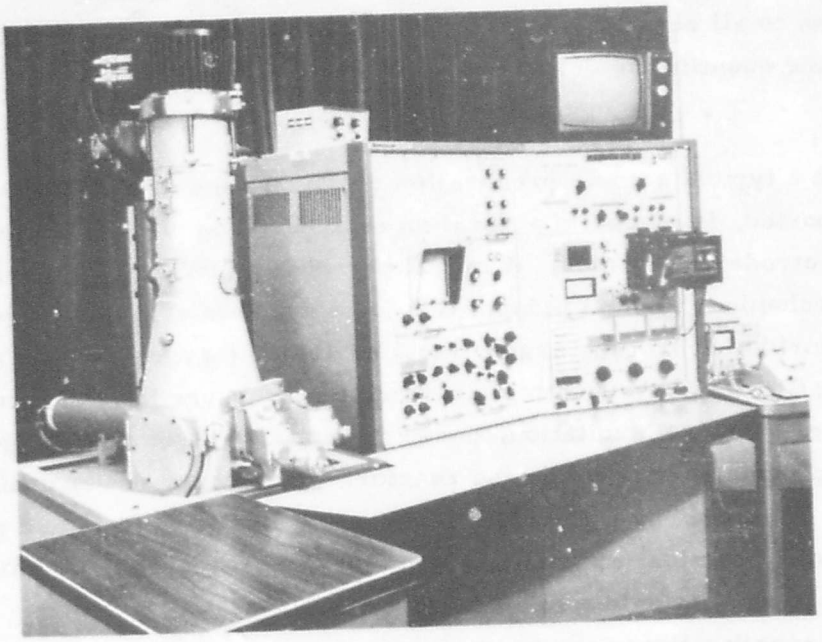


Figure C-2. Cambridge Model S4-10 steroscan. scanning electron microscope

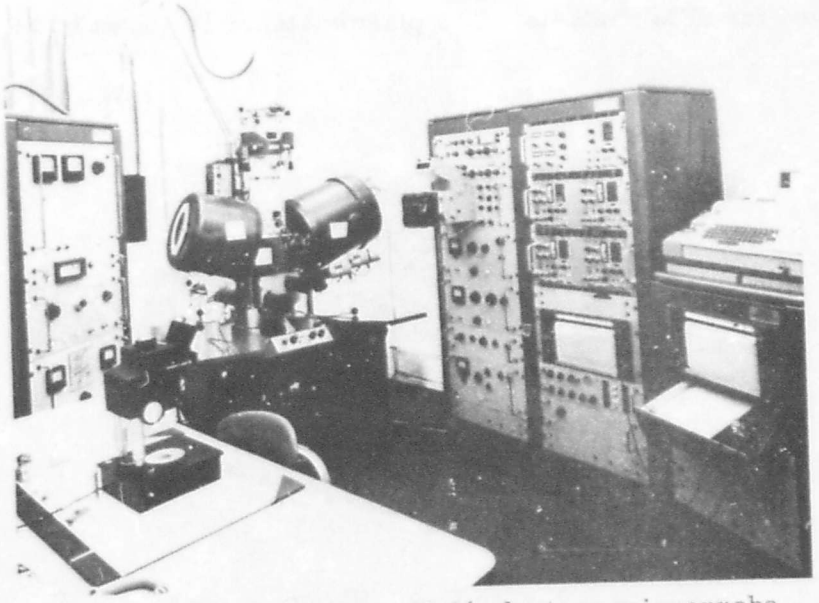


Figure C-3. Cameca type MS 46 electron microprobe.

absorbed electron imaging, and secondary electron imaging. The MS 46 is sensitive to all elements from boron through uranium and produces both qualitative and quantitative results.

Plasmod Plasma Etcher (Tegal Corporation)

In a typical sample preparation procedure the sample suitably mounted or supported, is placed in a reaction chamber around which a plasma excitation electrode is provided. A soft background vacuum of 0.01 torr is produced by a mechanical vacuum pump. Gas to be used for etching (oxygen, carbon tetrafluoride, hydrogen, argon, etc.) or ashing (oxygen) is then admitted at a controlled flow rate to attain an operating pressure in the range 0.5 to 1.0 torr. With RF excitation, power is increased from the RF generator until a plasma is initiated in the reactor. For proper power utilization, the system is "tuned" by a matching network. Only a few watts are required for the plasma chemical etching or ashing technique--perhaps 50 watts or less for most small sample reactors. Depending on the nature of the substrate, plasma reaction times can range from a few minutes to several hours. This is determined empirically by preliminary trials and is based on the desired extent or completion of etching or ashing. Once completed, the sample is removed for SEM analysis. The plasma etcher is shown in Figure C-4.

Figure C-4. Plasma etcher

APPENDIX D
SAMPLE PREPARATION AND SEM ANALYSIS STEPS

General

To obtain a correlation between applied programming pulses and the physical appearance of each opened fused link, a number of steps were required to prepare the fuse links for SEM analysis:

1. Removal of the passivation glass with chemical etch
2. Scanning Electron Microscope characterization of each fused link
3. Plasma etching of the fused link

The fusing reaction zone varies between 0.1 to 0.5 micron in width and is difficult to clearly delineate its physical appearance when normal optical microscopes are used. Therefore, the fuse structure must be viewed with an SEM. To obtain the highest spatial resolution in a standard mode-of-operation SEM, secondary electrons are used in image formation. Since the secondary electrons have low energies (less than 50 electron volts), their escape is limited to within 100 angstroms of the sample surface, and any subsurface detail will not be highly resolved in the secondary - electron mode. Therefore, the passivation must be removed for SEM analysis to reveal the subsurface metallizations for high-resolution inspection. Passivation removal can be accomplished by either wet-chemical methods or by plasma etching in a fluorine plasma. Since a reaction occurs between the fused link and the surrounding glass oxide, great care must be exercised to prevent damage to the physical properties of the fusing region during glass removal. A typical fusible link is a thin film between 150 and 300 Å in thickness sandwiched between a 10,000 - 15,000 Å thick low temperature glass overlay and an 8000 Å - 10,000 Å thick underlying silicon dioxide glass.

Passivation Removal

A wet chemical etch is performed with HF acide buffered one part HF to nine parts of 40 percent NH_4F solution. The etch is then stopped in methyl alcohol. Extreme care must be exercised in preventing damage to

the fuse link, in light of known drawbacks concerning wet chemical depassivation techniques. Periodic monitoring of the chip being etched, utilizing the SEM resulted in depassivation with no effect on the metallization.

SEM Examination

Once the glass overlay was removed, the fusing reaction zone is characterized. A Cambridge S4-10 SEM with a beam voltage of 10 kV is used. The SEM is a valuable tool in determining a correlation between programming pulses and resulting physical appearances of the fuse links.

Plasma Etch

To properly characterize the fusing reaction zone, a second step etching technique is employed using a fluoride plasma etch. In the plasma etching process, a reactant gas is excited into an active plasma by a radio-frequency field. The standard reaction for removal of silica (and similarly silicon) is

$$SiO_2(s) + CF_4(g) \rightarrow SiF_4(g) + CO_2(g)$$

The major advantages of plasma etching for removal of silicon and its compounds from bipolar devices are

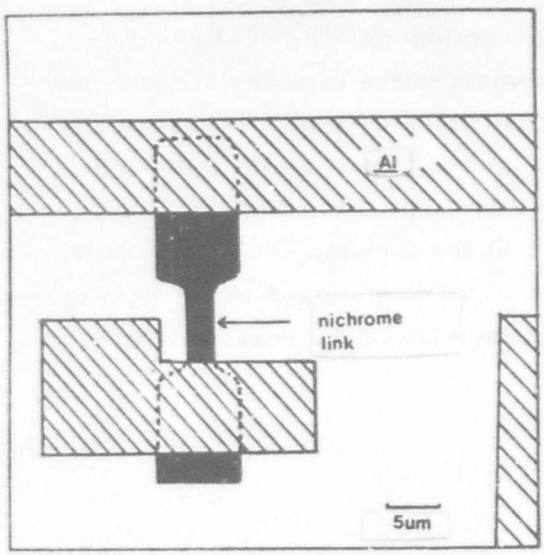
1. No attack of either aluminum or nichrome by the fluoride plasma
2. Reaction temperatures below $100^{\circ}C$.

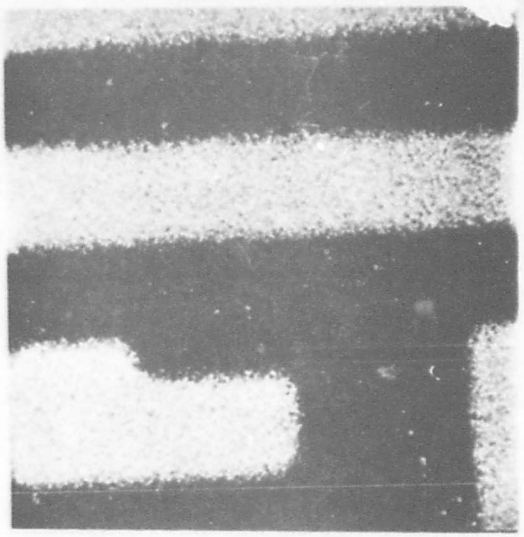
In this study, a PLASMOD Plasma Etcher manufactured by the TEGAL Corporation was used. Tetrafluoromethane (halocarbon 14) is bled into a 3-1/4 x 6-1/4 inch RF chamber at a partial pressure of approximately 0.5 torr. The RF field ionizes the gas into a highly reactive fluorine plasma, which readily attacks the silicon and silicon dioxide, but does not attack the nichrome fuse. However, as can be seen in figures on nichrome fuse links entitled "after plasma etch," a change in physical appearance of the fusing region was observed under SEM analysis. Based on this change, an electron microprobe analysis was conducted to:

1. Determine spatial distribution of nickel and chromium before and after plasma etch

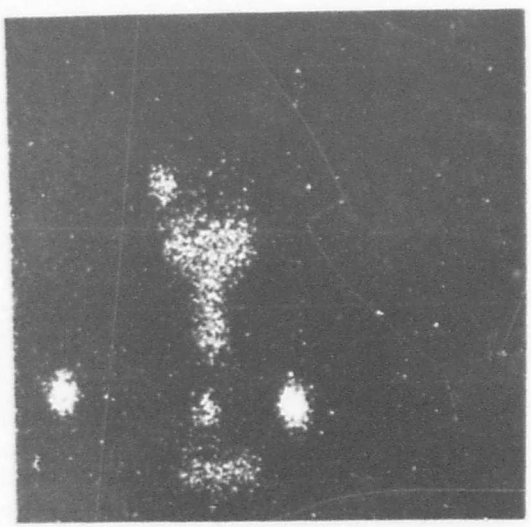
2. Perform an x-ray line scan on fused links for nickel and chromium after chemical etch and then on the same links after plasma etch.

The electron microprobe used in connection with the SEM resulted in quasi-analytical determination of the materials in the fuse gap of nichrome fusing technology. The electron microprobe detected random concentrations of nickel around the fused links and on the metallization which remained after the glass was removed. See Figures D-1 and D-2. Additionally, electron microprobe line scans revealed that the fluorine gas plasma had acted as a selective etch in removing chromium doped glass in the area of the fusion gap, thus, revealing the true shape and size of the reacted region. See Figures D-3 and D-4.



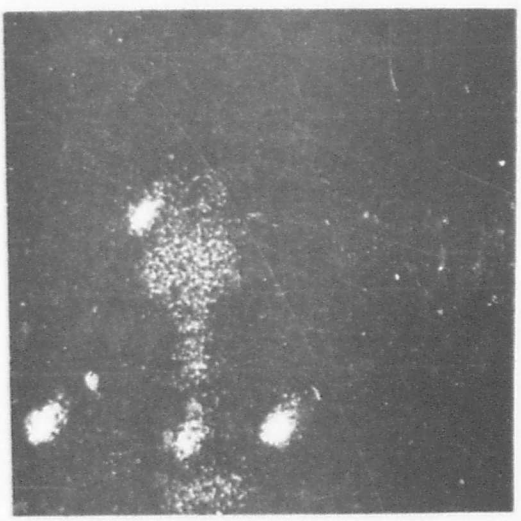


Al. Kα image



Ni. Kα image

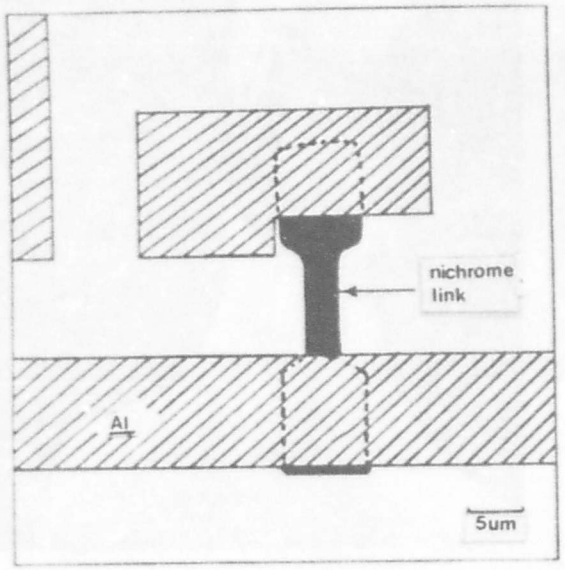
Glassivation Intact

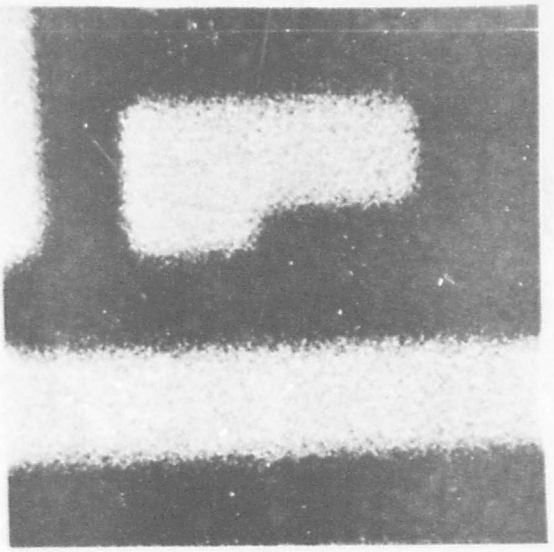


Ni. Kα image

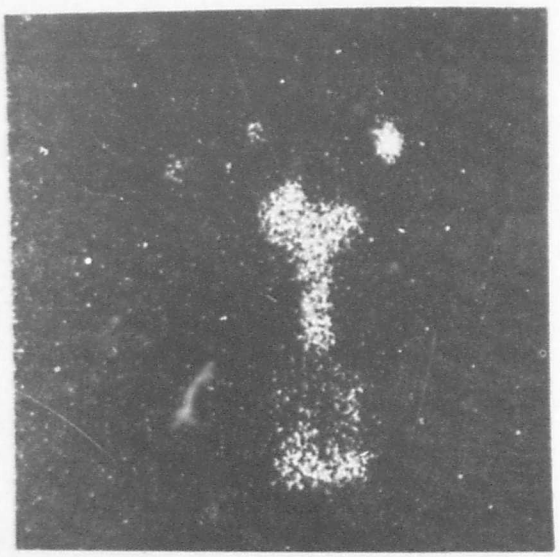
Glass Removed – Plasma Etched

Figure D-1. Electron microprobe, nickel concentration.

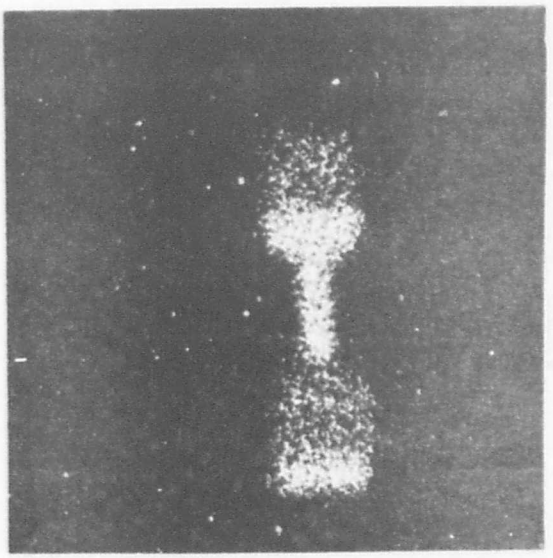




Al. Kα image

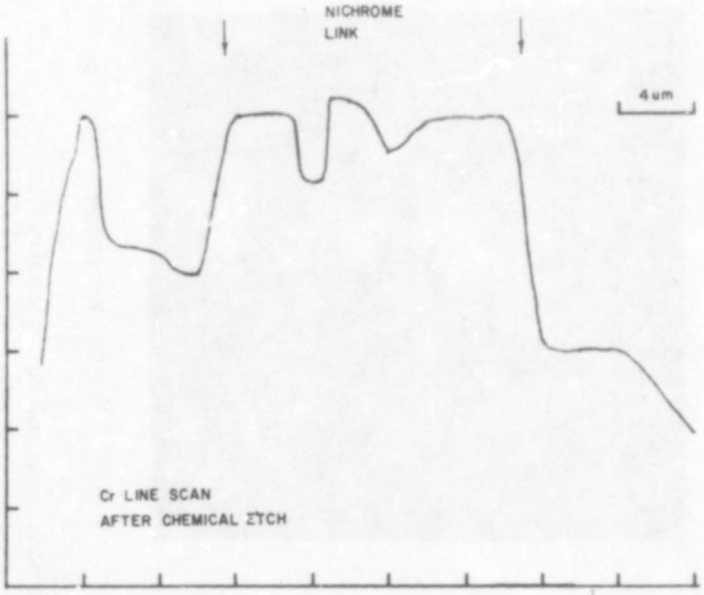


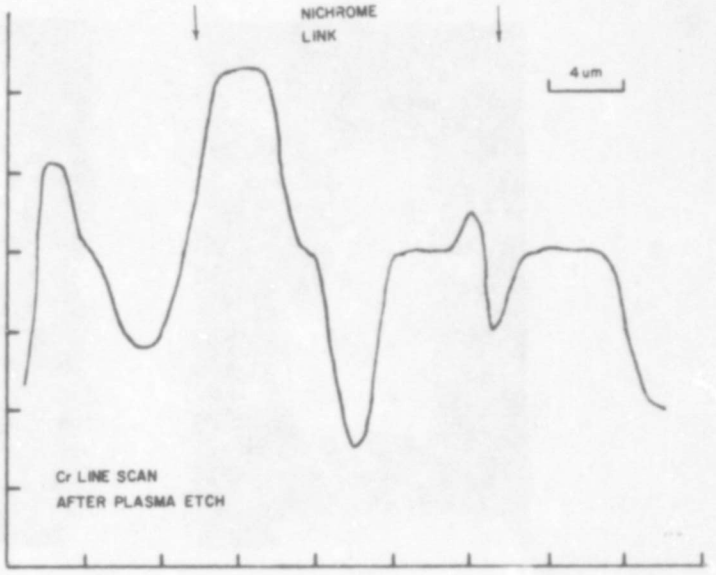
Ni. Kα image

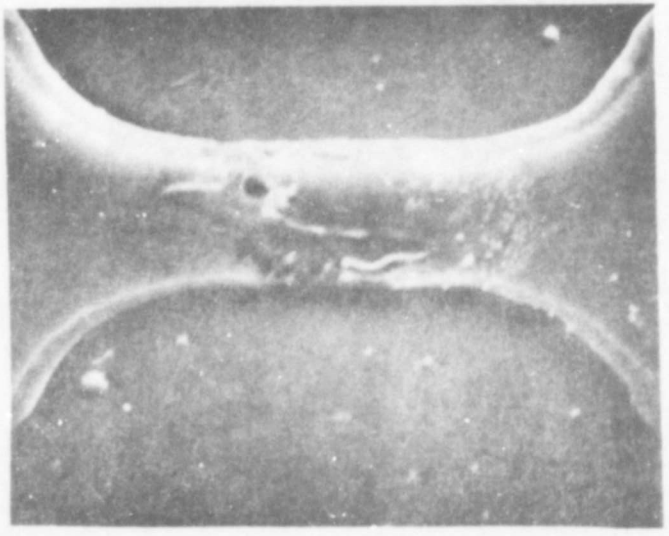


Cr. Kα image

Figure D-2. Electron microprobe, chromium concentration.







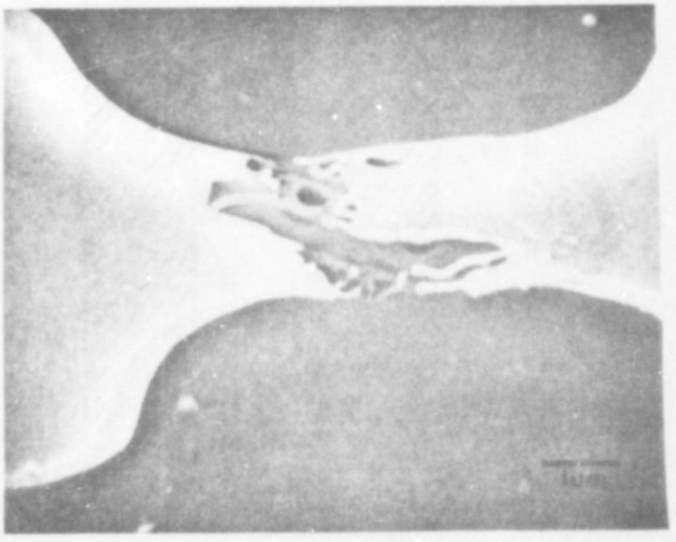


Figure D-3. Chromium line scan before and after plasma etch.

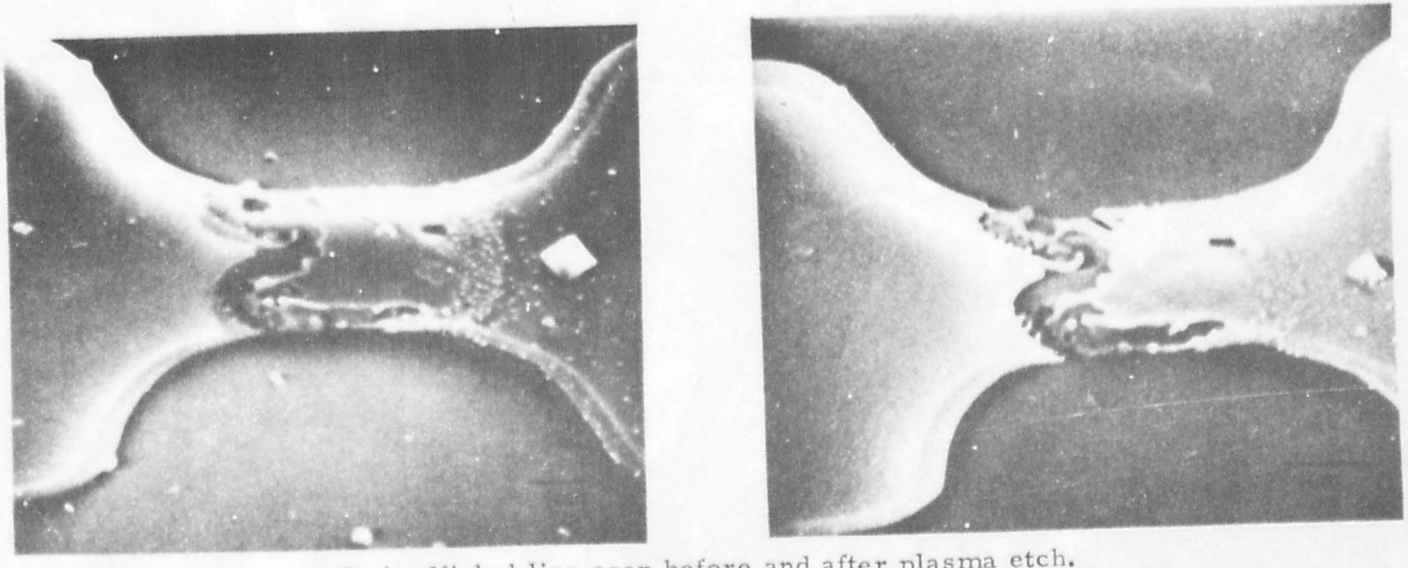


Figure D-4. Nickel line scan before and after plasma etch.

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RADC is the principal AFSC organization charged with planning and executing the USAF exploratory and advanced development programs for information sciences, intelligence, command, control and communications technology, products and services oriented to the needs of the USAF. Primary RADC mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, and electronic reliability, maintainability and compatibility. RADC has mission responsibility as assigned by AFSC for demonstration and acquisition of selected subsystems and systems in the intelligence, mapping, charting, command, control and communications areas.