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STUDY OF ELECTRONIC TRANSPORT AND BREAKDOWN
IN THIN INSULATING FILMS

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) Recent progress is reported on an ongoing program of studies of high-field electronic injection, transport, trapping, and dielectric breakdown in thin insulating films. The studies include corona-induced high-field injection and trapping, the combined use of corona and optical excitation, an investi- gation of the high-field generation of interface states, a study of high- field instabilities in the MOS system, and use of the scanning electron microscope to study lateral nonuniformities.			

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1. INTRODUCTION

We report here on recent progress in an ongoing program of research directed toward a basic understanding of the electronic properties of thin insulating films, including the mechanisms of charge injection, electronic transport, charge trapping, and dielectric breakdown. The objective of the program is to provide a rational basis for the choice of materials, processing methods and treatment of the insulating films in order to obtain the desired performance and reliability. We have reported previously on many of the results of these studies,¹⁻²³ and additional reports and papers are in preparation.

Our work in the past has concentrated on the properties of thermally grown silicon dioxide because of the importance of the Si-SiO₂ system in solid-state devices and circuits. The research techniques that we have developed are, however, immediately applicable to the study of other types of insulating films, and we are giving attention to aluminum oxide and other insulators of interest in night vision applications.

The organization of this report is as follows:

Section 2 describes recent results obtained on thermally grown SiO₂ by use of the corona-charging technique. As we have reported earlier, the corona technique provides a convenient and basically non-destructive method for studying high-field phenomena in thin insulating films.^{20,21} Here we report on two recently observed phenomena in the Si/SiO₂ system: (a) The buildup of a positive charge of trapped holes at fields above a threshold value of approximately 7.5 MV/cm, which we interpret in terms of impact ionization within the SiO₂. (b) The generation of electron traps in the oxide when the front surface is negatively charged to oxide fields greater than approximately 10 MV/cm. The negative charge in these traps alters the electric field distribution in the insulator under high-field conditions.

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Section 3 of this report describes the development of a new technique in which excitation by ultraviolet light is used to photoinject carriers into the insulator, and surface charging by corona ions is used to provide the electric field required for transport. The use of corona charging eliminates the need for a metallic field plate, and the use of UV light for photoinjecting carriers provides a degree of freedom not present in the original corona method. New results obtained by use of the combined UV-corona method are also presented.

Interface states are of great concern in MIS structures, and we have found previously that interface states are generated in the Si/SiO₂ system upon exposure to a sufficiently high field.²² If the high field is applied at liquid nitrogen temperature and then removed, the interface states do not appear until the sample is warmed. An exploration of this phenomenon, and of the information that can be derived from it, is given in Section 4 of this report.

The catastrophic breakdown of an insulator is preceded by an instability which develops on a time scale that under some circumstances is very fast and under other circumstances can be very slow. Some recent work on this instability is described in Section 5.

Lateral nonuniformities, such as ion aggregations and localized faults, can severely affect the performance of devices based on the MIS structure, and it is important to be able to identify and characterize any nonuniformities that may be present. In Section 6 of this report we describe the development of techniques for using the scanning electron microscope in the study of lateral nonuniformities, and we summarize some of the more important results that have been obtained on the Si-SiO₂ system by this means.

2. FURTHER CORONA-CHARGING STUDIES OF SILICON DIOXIDE

(H. S. Lee collaborating)

2.1. Introduction

We have previously reported on the development of corona-charging techniques for the study of high-field phenomena in thin insulating films, including the high-field injection of charge carriers and the transport and trapping of the carriers, and we have described results obtained by the use of these techniques on thermally grown silicon dioxide.^{5,10,20,21} The use of a corona discharge in a gas at atmospheric pressure to contact the unmetallized surface of an insulating film provides a powerful and convenient means for studying high-field processes, for the virtual absence of lateral surface conduction allows the use of very high field intensities - tantamount to breakdown - without destruction of the films.

Here we present the results of further corona studies of the Si-SiO₂ system, including (a) the observation and interpretation of positive charging in the oxide when the surface is charged positively to fields greater than about 7.5×10^6 V/cm, and (b) the determination of a threshold field for the generation of electron traps in the oxide when the surface is charged negatively.

2.2. Positive Oxide Charging Under Positive Corona Charging

We have previously shown that when the surface of a thin, thermally grown film of SiO₂ is charged to a sufficiently high positive potential, a current flows which is due to the Fowler-Nordheim tunneling of electrons from the conduction band of the silicon into the conduction band of the oxide with subsequent transport to the front surface.^{5,20,21} This mechanism has previously been proposed by Lenzlinger and Snow²⁴ and by Williams and Woods.²⁵ Since the charge injection is by tunneling, the observed currents are a very strong function of the electric field. In a good film of silicon dioxide thermally grown on a silicon substrate, the

electron tunneling current is of the order of 10^{-11} A/cm² at a field of 5.6×10^6 V/cm and of the order of 10^{-7} A/cm² at a field of 6.5×10^6 V/cm.^{3,4} Charge trapping in the oxide is negligible under these conditions.

More recently we have found that at oxide fields of $+7-8 \times 10^6$ V/cm (the + sign referring to the polarity of the surface), a positive charge builds up within the oxide. The presence of this charge increases the magnitude of the electric field at the Si-SiO₂ interface and thus acts to enhance the electron tunneling. Consequently, the charge buildup is important to both the current-voltage characteristics and the breakdown properties of the structure, and deserves close consideration.

Our experiments were performed on HCl-steam-grown oxides on 1-2 ohm-cm (100) silicon substrates. Both n-type and p-type substrates were used. A typical result is shown by the C-V curves of Fig. 21, which were obtained with a sample having a 2500 Å oxide grown on a p-type substrate. Curve 1 of that figure is the high-frequency (1 MHz) C-V characteristic of the sample in its original condition. In order to check for possible sodium contamination, the surface of the sample was charged positively to an oxide field of approximately 6×10^6 V/cm, placed in a vacuum chamber which was then pumped down to 10^{-6} torr, and was heated to 150°C for 15 min. This treatment should drive any sodium to the Si-SiO₂ interface, where its effect would show up as a negative shift of the C-V curve. To make sure that the drift field remained during the anneal, the surface potential was measured after the anneal, and showed an electric field remaining of approximately 5×10^6 V/cm. The result of the foregoing bias-temperature stress is shown by Curve 2 of Fig. 2.1. The effect is seen to be very small, indicating that ionic contamination was not an important factor in the final results.

The principal experiment was then performed. Positive corona in a helium atmosphere was used to produce an initial oxide field of approximately 7.5×10^6 V/cm. The corresponding current density was 0.87×10^{-6} A/cm², and the intensity of the corona was regulated to keep the current constant at this value. At intervals the corona charging was interrupted briefly and a C-V curve was taken to provide a measure of the

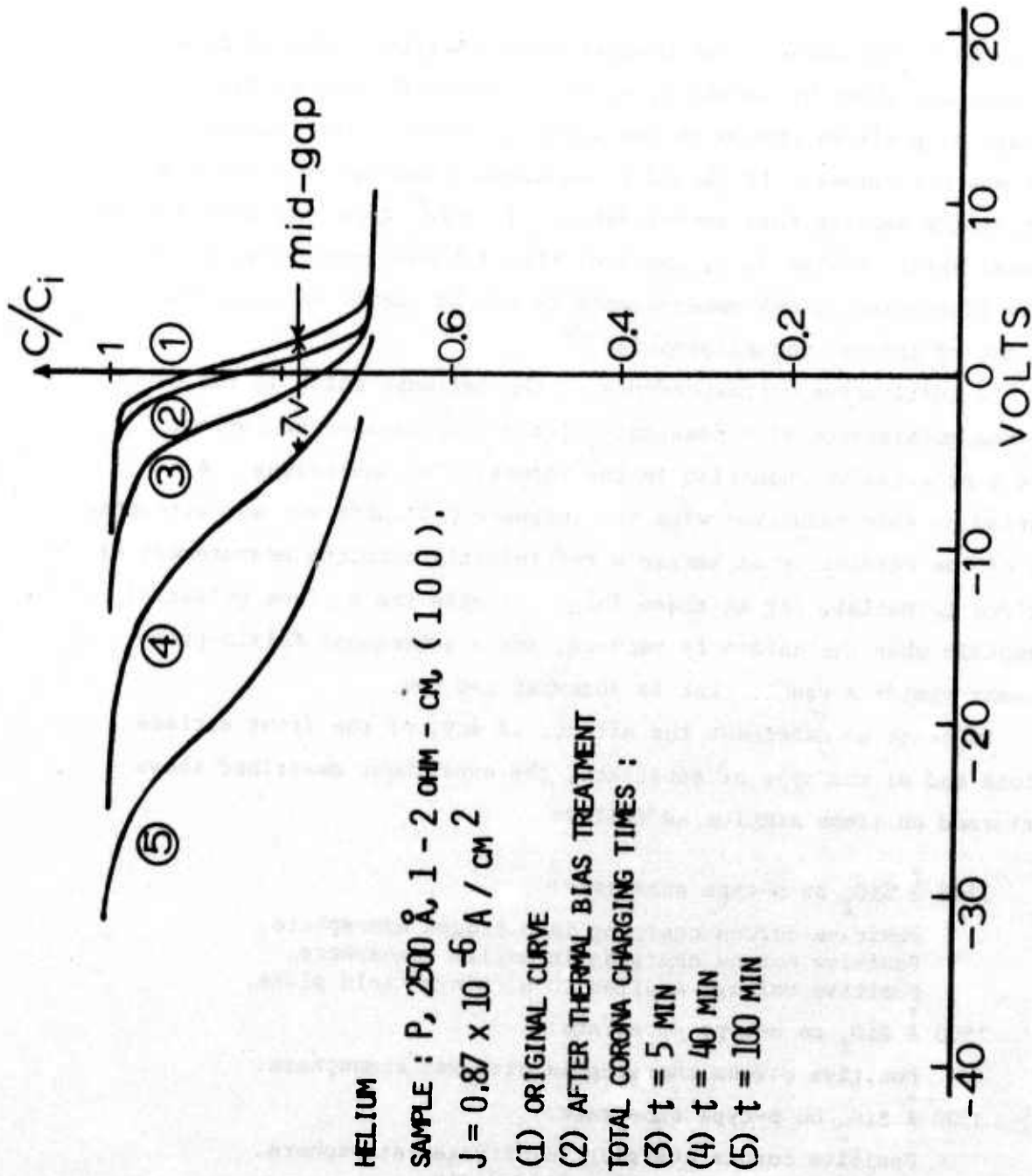


Fig. 2.1. Typical C-V curves, showing the result of large positive-corona currents.

charge stored in the oxide. The results after charging times of 5, 40, and 100 min. are shown by Curves 3, 4, and 5, respectively, of Fig. 2.1. The storage of positive charge in the oxide is shown by the leftward shift of the C-V curves. It should be emphasized that no such shift was found at fields smaller than approximately 7×10^6 V/cm. In addition to the lateral shift, Curves 3, 4, and 5 of Fig. 2.1 show some stretch-out which was identified by G-V measurements to be the result of interface states, not of lateral nonuniformities.²²

In qualitative correspondence to the leftward shift of the C-V curves, the maintenance of a constant value of corona-induced current required a progressive reduction in the intensity of the corona. A correlation of this reduction with the leftward C-V shift was not attempted because of the difficulty in making a sufficiently accurate measurement of the surface potential, for at these large currents the surface potential drops rapidly when the corona is removed, and a subsequent Kelvin-probe measurement yields a result that is somewhat too low.

In order to determine the effect, if any, of the front surface conditions and of the type of substrate, the experiment described above was performed on fresh samples as follows:

2500 Å SiO₂ on p-type substrate:

- Positive corona charging in nitrogen atmosphere.
- Positive corona charging in helium atmosphere.
- Positive voltage applied to aluminum field plate.

2500 Å SiO₂ on n-type substrate:

- Positive corona charging in nitrogen atmosphere.

3500 Å SiO₂ on p-type substrate:

- Positive corona charging in nitrogen atmosphere.
- Positive corona charging in dry air.

The results are plotted in Fig. 2.2 in terms of the effective density of trapped positive charges, N_t^* , that would be required to produce the observed

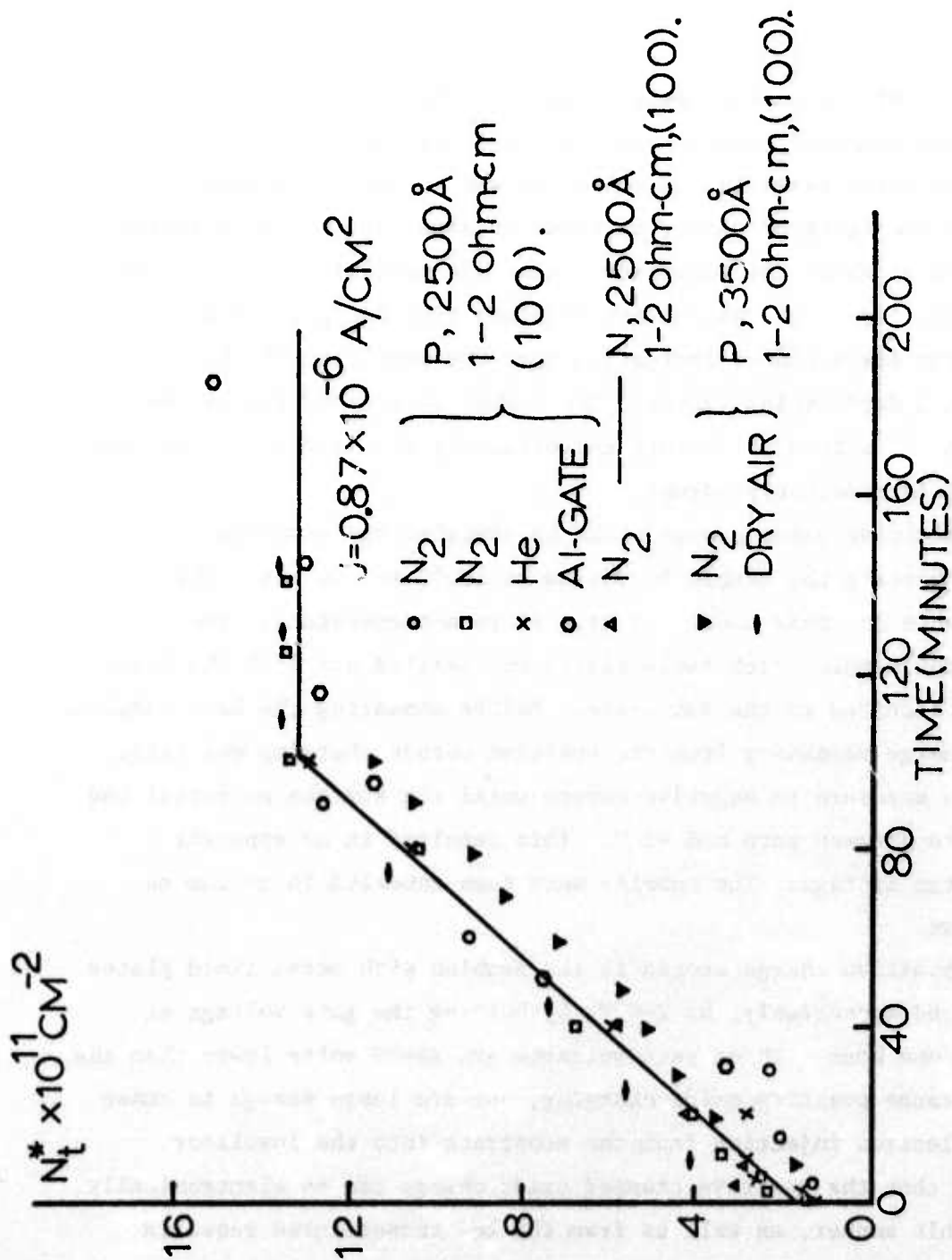


Fig. 2.2. Time evolution of the positive oxide charge caused by positive charging of the front surface to an initial field of $7.6 \times 10^6 \text{ V/cm}$.

C-V shift if all of the charges were trapped at the Si-SiO₂ interface. This density was computed from the voltage shift of the C-V curves at the point where the Fermi level in the substrate was at silicon midgap rather than at the flatband point, as there is some evidence that midgap is the position at which the interface states are neutral.²² It is seen that essentially identical results are obtained with all gases and also with an aluminum field plate, indicating that the condition of the front surface is not a determining factor. The number of trapped charges below the saturation value is seen to vary approximately linearly with time, and the saturation is remarkably abrupt.

The positive oxide charge could be annealed out essentially completely by heating the sample in vacuum at 100°C for 30 min. The charge was stable for this amount of time at room temperature. The annealing of the samples with field plates was carried out with the field plates short circuited to the substrate. Before annealing the bare samples, the surface charge remaining from the positive corona charging was first neutralized by exposure to negative corona until the surface potential had been reduced to between zero and -1 V. This resulted in no apparent change in charge storage. The samples were then annealed in vacuum as indicated above.

The positive charge stored in the samples with metal field plates could be reduced appreciably, by 2-6 V, by holding the gate voltage at 160-170 V for one hour. These gate voltages are 20-30 volts lower than the values which cause positive oxide charging, but are large enough to cause a continued electron injection from the substrate into the insulator. From the fact that the positive trapped oxide charge can be electronically bleached in this manner, as well as from the low temperatures required for thermal annealing, we conclude that the positive trapped charge was that of holes, not of positive ions.

The origin of the trapped holes is of great interest. The lack of front-surface dependence shown in Fig. 2.2 argues strongly against hole injection from this surface. A more likely source of the holes is

impact ionization within the bulk of the SiO_2 caused by a few of the transiting electrons which attain sufficiently large kinetic energies (> 9 eV) in the high electric field to create hole-electron pairs. Calculation shows that in the linear portion of Fig. 2.2, the ratio of trapped holes to total injected electrons is approximately 4×10^{-5} . The interpretation in terms of impact ionization is identical with the explanation given by Yang, Johnson, and Lampert¹⁷ for a slow instability, leading to breakdown, that has been observed in MIS structures under high field conditions, and is the mechanism proposed by DiStefano and Shatzkes²⁶ for dielectric breakdown. The corona-charging technique permits the study of this phenomenon under controlled, nondestructive conditions.

The lack of dependence on thickness and the abrupt saturation shown in Fig. 2.2 deserve further attention. When penetrating radiation is used to produce hole-electron pairs in the insulator of an MIS structure, the number of generated holes is equal to the number of generated electrons and is directly proportional to the thickness of the insulator. Our conditions here, however, are somewhat different, for the number of electrons in our experiment far exceeds the number of holes. A possible explanation is that the flux of holes arriving at the Si-SiO₂ interface under the conditions of our experiment is recombination-limited, so that the holes produced far from the interface are recombined and do not reach the hole traps at the interface.²³ The sharp saturation shown in Fig. 2.2 is extremely interesting, but we have no adequate model to offer for this at the present time.

2.3. High-Field Generation of Electron Traps in Silicon Dioxide

We have previously reported the observation that a positive stored charge appears in thermally grown silicon dioxide when the surface of the oxide is charged with negative corona ions to an oxide field greater than $(1.1 \pm 0.1) \times 10^7$ V/cm.^{20,21} The positive charge appears to be that of trapped holes, and it has been suggested²⁰ that the source of the holes is the silicon substrate.

More recently, we have reported on the discovery that negative corona charging to a sufficiently high field has the additional effect of generating substantial concentrations of electron traps within the oxide.^{19,21,23} The magnitude of the electric field required for generation of the electron traps is of considerable interest, and we give here the results of experiments designed to determine the threshold. The technique used for this determination was as follows: The surface of the sample was first charged with negative corona ions to produce a given electric field in the oxide. To determine whether electron traps had been generated by this process, electrons were tunnel-injected from the substrate into the oxide by charging the surface with positive ions. The objectives of the electron injection were (a) to neutralize any trapped holes, whose presence would tend to obscure the trapping of electrons, and (b) to fill any electron traps that might be present. The electric field in the oxide during the electron injection was kept below 7×10^6 V/cm to avoid positive charge buildup from this source (Sec. 1.2). A high-frequency (1 MHz) C-V curve was then taken to detect any charge storage in the oxide. The sequence of experiments was then repeated, starting with negative surface charging at a larger field than before.

Figure 2.3 shows the results obtained from a typical series of steps as described above. The sample had a p-type silicon substrate with (100) orientation and a resistivity of 10 ohm-cm. The oxide film was grown in dry oxygen to a thickness of 1750 Å. The corona charging of the sample was carried out in an atmosphere of dry air. Curve 1 of Fig. 2.3 is the original C-V characteristic of the sample. Curve 2 shows the relatively small effect produced by a 15-min injection of electrons from the substrate into the oxide, using positive corona charging at an insulator field of 6.6×10^6 V/cm in the manner described in the preceding paragraph. Curve 3, obtained after negative corona charging for 5 min at a field of -9.4×10^6 V/cm, is also relatively unchanged from the original.

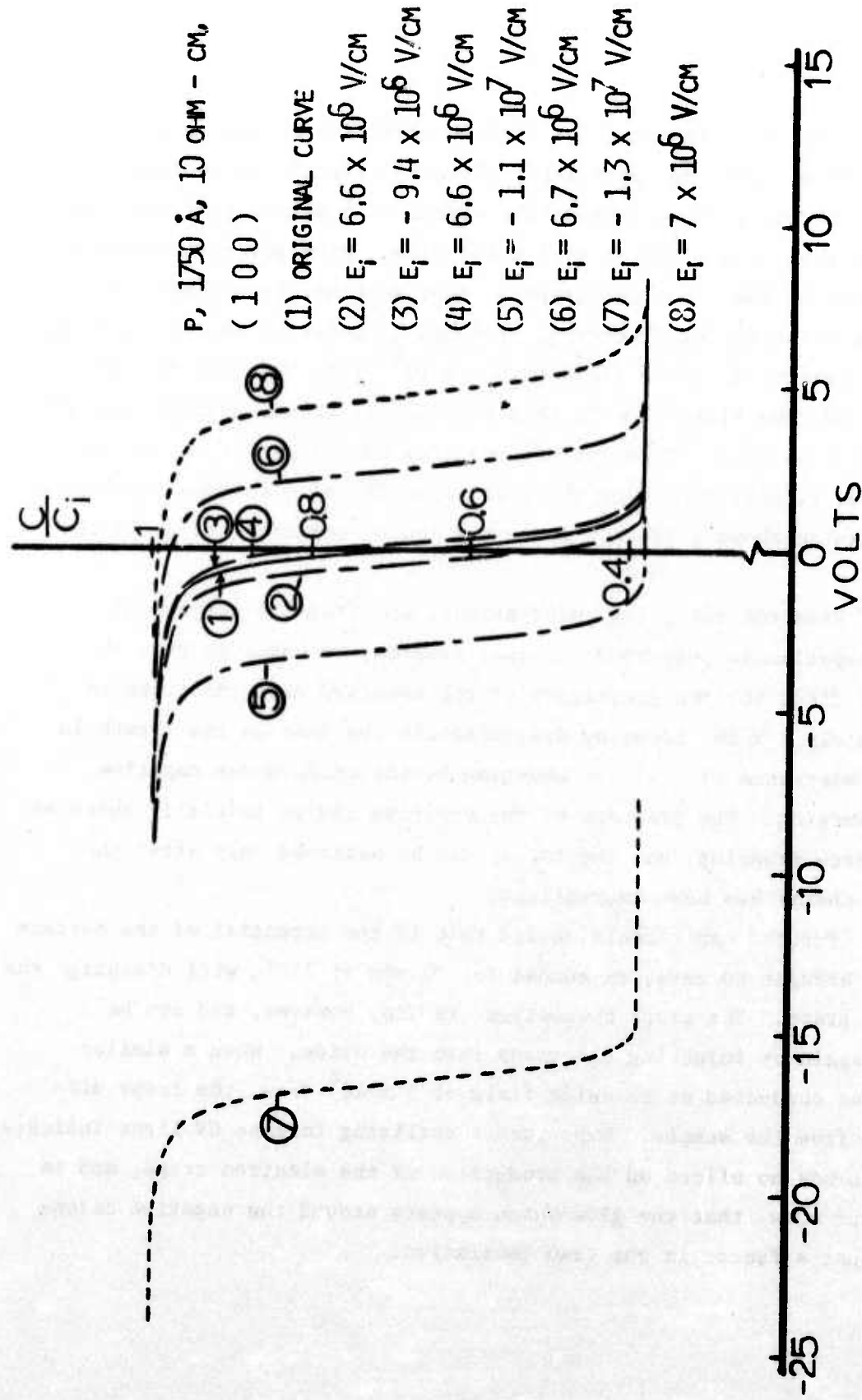


Fig. 2.3. Experimental results showing a threshold field of approximately $\sim 1 \times 10^7 \text{ V/cm}$ for production of the negative charging effect.

Curve 4, taken after exposure for 5 min to positive corona at a field of 6.6×10^6 V/cm, shows no appreciable charging effect. In contrast with the above, however, Curve 5 shows the effect of 5 min of charging with negative corona at a field of -1.1×10^7 V/cm. Here positive charging, as described in the first paragraph of this section, is evident. A subsequent injection of electrons, produced by positive corona charging of the surface to an oxide field of 6.6×10^6 V/cm, resulted in Curve 6, where, for the first time in this sequence of steps, negative charging of the oxide is seen. More intense charging with negative corona produced Curve 7, and, following this, an injection of electrons resulted in Curve 8, which shows a greater concentration of negative charge in the oxide.

From the foregoing observations, and from the results of similar experiments performed on other samples, we conclude that the threshold field for the generation of the observed electron traps is approximately 1×10^7 V/cm, or approximately the same as the threshold for the observance of positive charging in the oxide under negative corona charging. The presence of the positive charge initially obscures the electron trapping, and the latter can be observed only after the positive charge has been neutralized.

Further experiments showed that if the potential of the surface is first brought to zero, an anneal for 30 min at 150°C will discharge the electron traps. The traps themselves remain, however, and can be charged again by injecting electrons into the oxide. When a similar anneal was conducted at an oxide field of 5×10^6 V/cm, the traps disappeared from the sample. Experiments utilizing intense UV light indicate that this has no effect on the production of the electron traps, and in particular show that the glow which appears around the negative corona tip was not a factor in the trap generation.

3. COMBINED CORONA AND PHOTOEMISSION TECHNIQUES (H. H. Chao collaborating)

3.1. Background Discussion

Internal photoemission has been shown to be a useful tool for the study of interface properties,²⁷⁻³⁵ trapping phenomena,^{27,28} and ion migration in thin-film insulators.³⁰⁻³² In the usual experiments, metal-insulator-semiconductor (MIS) and metal-insulator-metal (MIM) capacitors with semi-transparent metal gates are used. When UV light is incident on the sample, the photocurrent is due, in general, to the emission of both electrons and holes from the negatively and positively biased electrodes respectively. Optical interference can be used as a tool to ascertain the contributions of electron and hole emission to the photocurrent.³⁶ If both hole and electron photocurrents are significant, the interpretation of the results of internal photoemission experiments is very difficult. Fortunately, in most cases, the contribution of one carrier can be neglected. Hole currents are negligible in both silicon dioxide³⁶ and aluminum oxide^{37,38} insulators, and electron photocurrents are negligible in silicon nitride.³⁵ However, this makes the internal photoemission technique unsuitable for studying the properties of holes in silicon dioxide and aluminum oxide and the properties of electrons in silicon nitride.

In order to overcome this difficulty, ions instead of a metal gate can be used to provide the necessary electric field in the insulator. The purpose here is to make the injection of carriers from the front surface negligible compared with the injection of carriers from the substrate.

A gas discharge at atmospheric pressure may be used to provide the ions.^{20,21,23} If the unmetallized surface of the insulator is charged with positive ions from a corona discharge and the corona is thereupon shut off, the positive charge retained on the surface can exist in either of two forms:

- (1) Positive ions sticking to the surface through image-force attraction.
- (2) Excess holes in surface states at the front surface.

When the surface potential is kept relatively low, tunneling currents can

be neglected and the surface potential will remain constant in the dark. When light with a photon energy smaller than the band gap of the insulator is incident on the sample, the surface potential can decrease through either of two processes:

- (I) Electrons may be emitted into the insulator from the substrate and drift to the front surface where they neutralize the surface charge.
- (II) The photons may excite electrons from the valence band of the insulator to the surface states at the front surface, leaving holes in the valence band which may thereupon drift toward the substrate.

Optical interference techniques can be used to determine which of the foregoing charge neutralization processes, (I) or (II), is the dominant one.

3.2. Analysis of the Optical Interference Technique

If charge-carrier trapping and recombination in the insulator can be neglected, the change in surface potential, ΔV_s , can be written as

$$|\Delta V_s|/C_i = |Q_i| + |Q_s| \quad (3.1)$$

where C_i is the insulator capacitance, Q_i is the charge injected at the substrate-insulator interface (Process I of the preceding section), and Q_s is the injection of charge at the surface (Process II of the preceding section). The magnitudes of Q_i and Q_s are respectively given by

$$|Q_i| = q A_i(h\nu) T(h\nu) F \quad (3.2)$$

$$|Q_s| = q A_s(h\nu) R(h\nu) F \quad (3.3)$$

where q is the magnitude of the electronic charge, F is the fluence of the incident monochromatic light, $A(h\nu)$ is the quantum yield for a photon with energy $h\nu$, $T(h\nu)$ is the transmittance of the light into the substrate, and $R(h\nu)$ is defined as

$$R(h\nu) = \left| 1 + \frac{E_o^-}{E_o^+} \right|^2$$

where E_0^+ and E_0^- are the amplitudes of the incident and reflected waves, respectively. For the internal photoemission of electrons from a metal or semiconductor into an insulator,

$$A_1(h\nu) = B(h\nu - \phi_b)^p$$

where B is a constant, ϕ_b is the barrier height, and p is a constant which depends on the substrate.^{27-35,39,40}

The functional form of $A_s(h\nu)$ is not known. However, it is reasonable to assume that it is a monotonically increasing function of $h\nu$. R and T are oscillatory functions of $h\nu$ as shown in Fig. 3.1. The maxima (minima) points of R and T occur for nearly the same photon energy, but the amplitudes of oscillation of R and T are quite different. Hence R/T and T/R will oscillate with quite large amplitudes as shown in Fig. 3.2. The location of the maxima (minima) points of T/R and R/T depend on the refractive indices of the substrate and insulator and the thickness of the insulator. By choosing a proper insulator thickness, we can have several maxima (minima) located in the range of the photon energy which we are interested. The maxima of R/T and T/R are much larger than unity; the minima of R/T and T/R are much smaller than unity.

The effect of R/T on the $|\Delta V_s|/qC_1TF$ and $|\Delta V_s|/qC_1RF$ vs. $h\nu$ plots can be seen more clearly if we rewrite Eq. (3.1) as

$$\frac{|\Delta V_s|}{qC_1TF} = A_1(h\nu) \left[1 + \frac{R}{T} \frac{A_s(h\nu)}{A_1(h\nu)} \right] \quad (3.4)$$

or alternatively as

$$\frac{|\Delta V_s|}{qC_1RF} = A_s(h\nu) \left[\frac{T}{R} \frac{A_1(h\nu)}{A_s(h\nu)} + 1 \right] \quad (3.5)$$

In the following, we will discuss how to use the oscillating property of R/T and T/R to find the contribution of each process to the photocurrent from the $|\Delta V_s|/q_1C_1TF$ vs. $h\nu$ plot and/or the $|\Delta V_s|/qC_1RF$ vs. $h\nu$ plot.

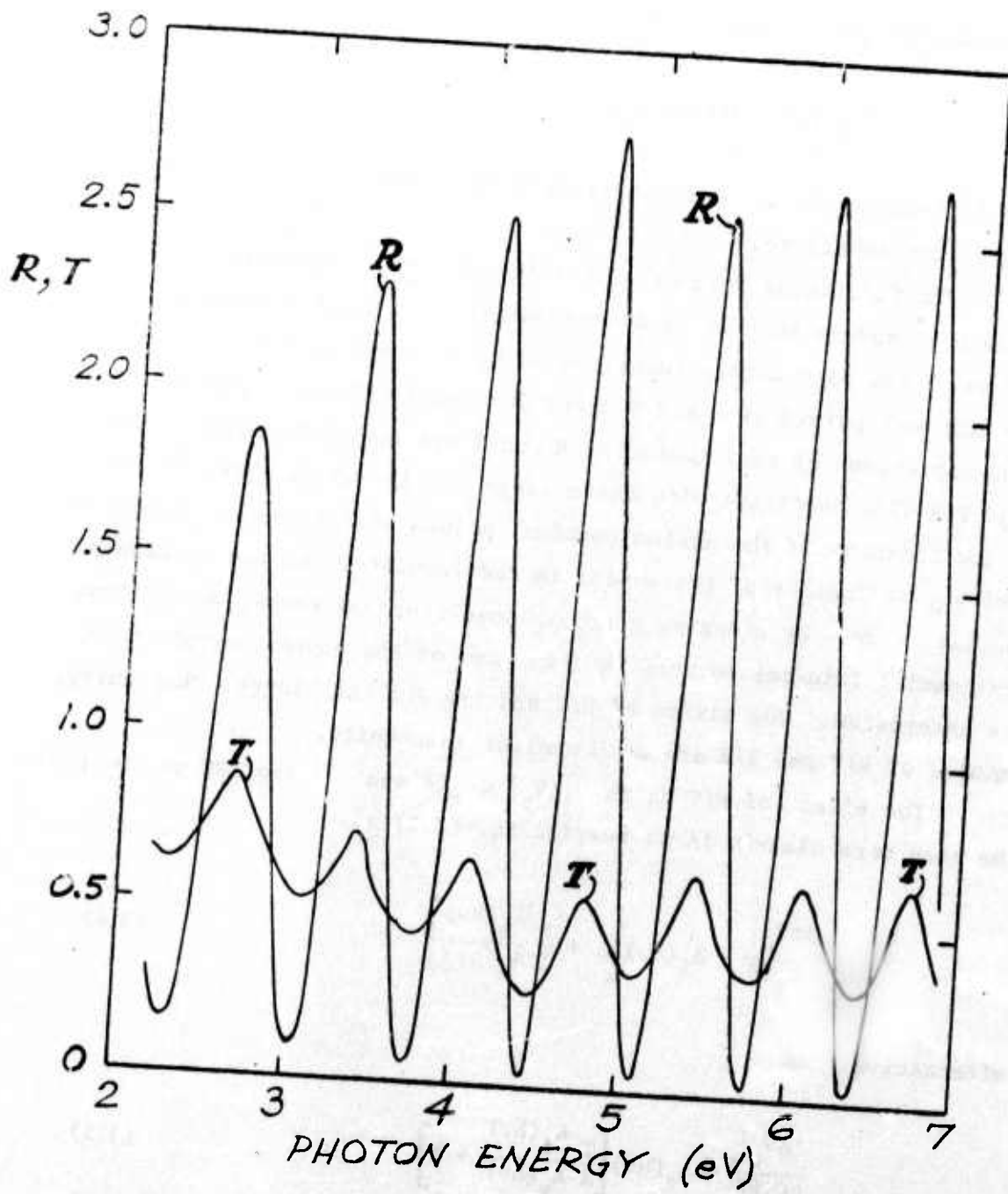


Fig. 3.1. Computer plot of transmittance, T , and of $R = \left| 1 + \frac{E_o}{E_o} \right|^2$ for an SiO_2 -Si structure with oxide thickness of 5526 Å.

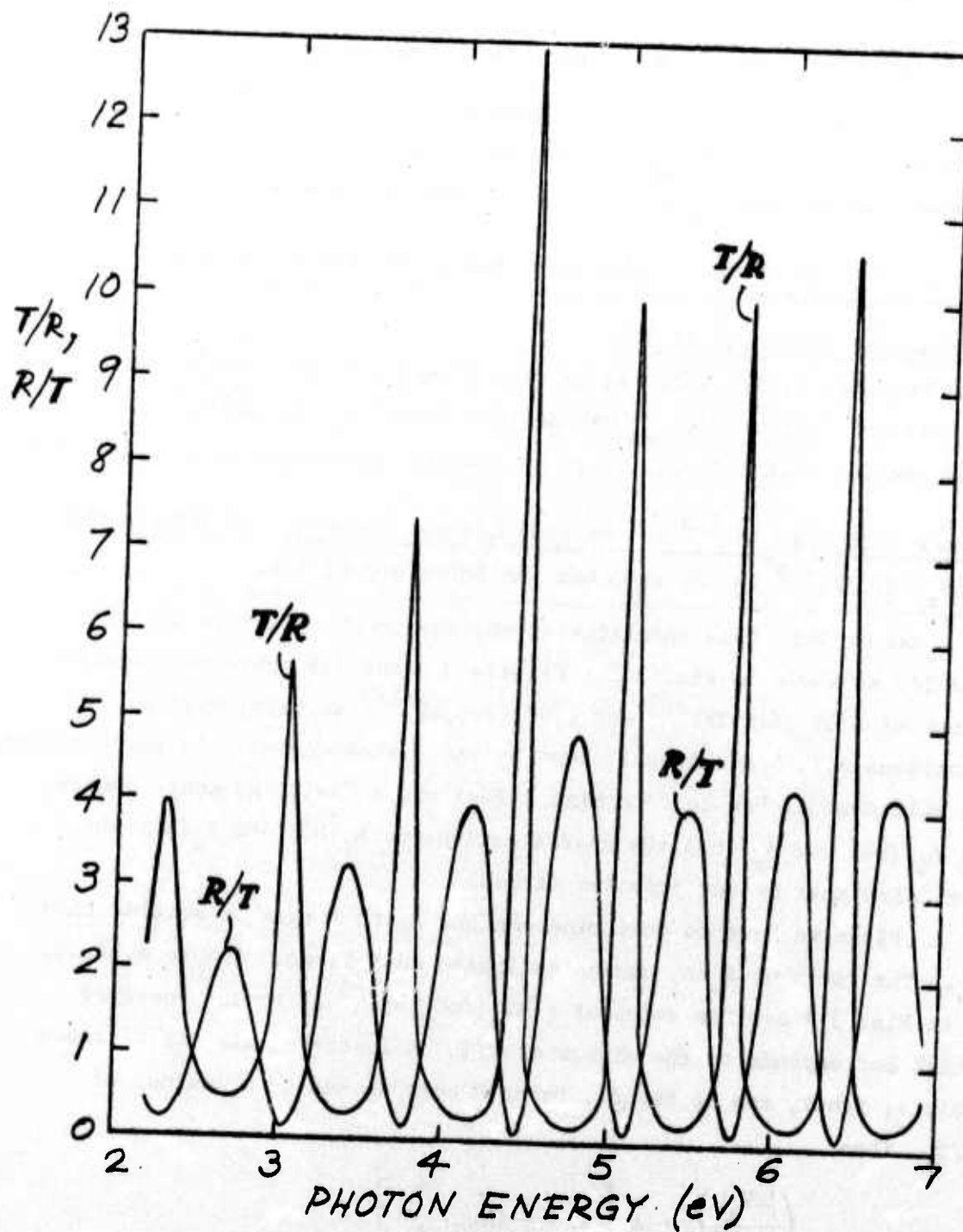


Fig. 3.2. Computer plot of T/R and R/T for SiO_2 -Si structure with oxide thickness of 5526 Å.

We will discuss three different situations separately.

- (A) If the $(|\Delta V_s|/qC_1 TF)^{1/p}$ vs. $h\nu$ plot is a straight line.

From Eq. (3.4), this can be true if and only if $\frac{R}{T} \frac{A_s(h\nu)}{A_i(h\nu)} \ll 1$ for all $h\nu$. Since $(R/T)_{\max}$ can be quite large, $A_s(h\nu)$ should be much smaller than $A_i(h\nu)$; i.e., the hole photocurrent is negligible.

- (B) If the $|\Delta V_s|/qC_1 RF$ vs. $h\nu$ plot is a simple monotonic function of $h\nu$ without any structure of T/R .

From Eq. (3.5), this can be true if and only if $\frac{T}{R} \frac{A_i(h\nu)}{A_s(h\nu)} \ll 1$ for all $h\nu$. Since $(T/R)_{\max}$ can be very large, $A_i(h\nu)$ should be much smaller than $A_s(h\nu)$; i.e., the electron photocurrent is negligible.

- (C) If the $(|\Delta V_s|/qC_1 TF)^{1/p}$ vs. $h\nu$ plot has the structure of R/T and the $(|\Delta V_s|/qC_1 RF)^{1/p}$ vs. $h\nu$ plot has the structure of T/R .

Assume that this insulator-on-semiconductor structure has R/T and T/R as shown in Fig. 3.2. Figures 3.3 and 3.4 show the computer plots of $(|\Delta V_s|/qC_1 TF)^{1/3}$ and $(|\Delta V_s|/qC_1 RF)^{1/3}$ as determined for the functions $A_i(h\nu)$ and $A_s(h\nu)$ shown by the dashed curves. In the following we will discuss how to determine $A_i(h\nu)$ and $A_s(h\nu)$. We shall denote by $A_i'(h\nu)$ and $A_s'(h\nu)$ the approximations to $A_i(h\nu)$ and $A_s(h\nu)$ which are calculated by our proposed method.

First we have to determine whether A_i is larger or smaller than A_s . The ratio of A_s/A_i can be estimated as follows. Points A, B, C, D in Fig. 3.3 are the values of $(|\Delta V_s|/qC_1 TF)^{1/3}$ at photon energies which corresponds to the minima of R/T . A least-squares fit of these points, $f(h\nu)$, can be found. Point G corresponds to a maximum of R/T . Then

$$\left(\frac{|\Delta V_s|}{qC_1 TF} \right)_G = A_i \left[1 + \frac{R}{T}(h\nu_G) \frac{A_s}{A_i} \right]$$

$$f(h\nu_G) \approx A_i \left[1 + \left(\frac{\frac{R}{T}(h\nu_B) + \frac{R}{T}(h\nu_C)}{2} \right) \frac{A_s}{A_i} \right]$$

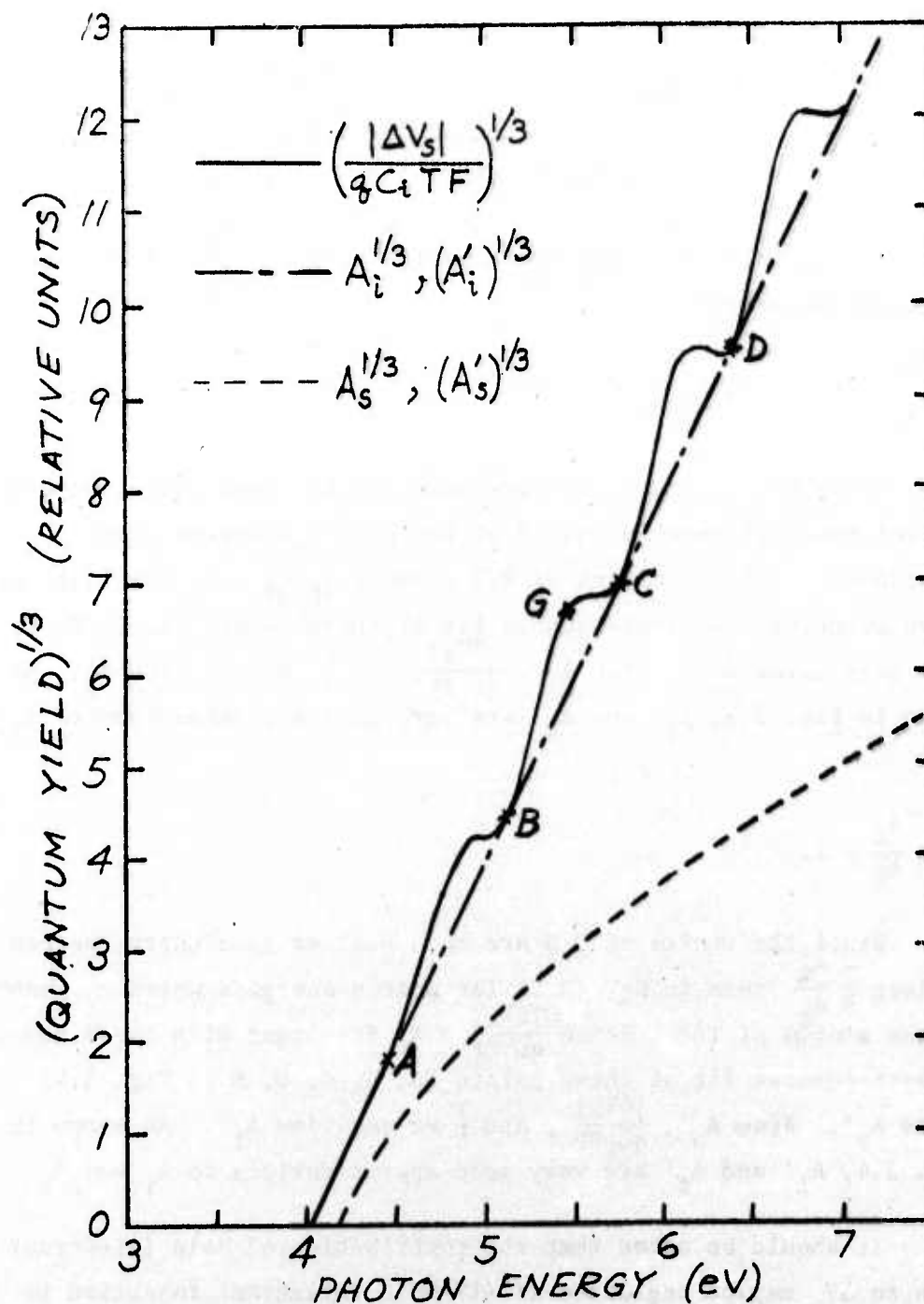


Fig. 3.3. Computer plot of $(\frac{|\Delta V_s|}{qC_i TF})^{1/3}$ vs. $h\nu$ for an insulator-on-semiconductor structure with R/T as shown in Fig. 3.2 and A_i, A_s as shown here. A_i' and A_s' are calculated from this $(\frac{|\Delta V_s|}{qC_i TF})^{1/3}$ vs. $h\nu$ curve by our proposed method.

Hence

$$\frac{A_s}{A_1} \approx \frac{\left(\frac{|\Delta V_s|}{qC_1 TF}\right)_G - f(h\nu_G)}{\frac{R}{T}(h\nu_G) - \frac{1}{2}\left[\frac{R}{T}(h\nu_G) + \frac{R}{T}(h\nu_C)\right]} \approx \frac{\left(\frac{|\Delta V_s|}{qC_1 TF}\right)_G - f(h\nu_G)}{\frac{R}{T}(h\nu_G)}$$

In the following, the cases with $\frac{A_s}{A_1} < 1$ and $\frac{A_s}{A_1} > 1$ will be discussed separately.

$$(i) \frac{A_s}{A_1} < 1.$$

Since the minima of R/T are much smaller than unity, we can neglect the $\frac{R}{T} \frac{A_s}{A_1}$ term in Eq. (3.4) for photon energies which correspond to the minima of R/T . Hence $\frac{|\Delta V_s|}{qC_1 TF} = A_1$ for light with these energies. A least-squares fit of these points (A, B, C, D, in Fig. 3.3) gives A_1' . From A_1' , $\frac{|\Delta V_s|}{qC_1 TF}$, and $\frac{R}{T}$ we can find A_s' . As shown in Fig. 3.3, A_1' and A_s' are very good approximations to A_1 and A_s .

$$(ii) \frac{A_s}{A_1} > 1.$$

Since the minima of T/R are much smaller than unity, we can neglect the $\frac{T}{R} \frac{A_1}{A_s}$ term in Eq. (3.5) for photon energies which correspond to the minima of T/R . Hence $\frac{|\Delta V_s|}{qC_1 RF} = A_s$ for light with these energies. A least-squares fit of these points (A, B, C, D, E in Fig. 3.4) gives A_s' . From A_s' , $\frac{|\Delta V_s|}{qC_1 RF}$, and $\frac{T}{R}$ we can find A_1' . As shown in Fig. 3.4, A_1' and A_s' are very good approximations to A_1 and A_s .

It should be noted that the contribution of hole (electron) injection to ΔV_s may be neglected if (1) hole (electron) injection is small compared with electron (hole) injection or (2) holes (electrons) recombine in a short distance.

When trapping in the insulator is important, the interpretation of the experiments will be very difficult if both electron and hole injection are significant. If electron injection from the substrate is

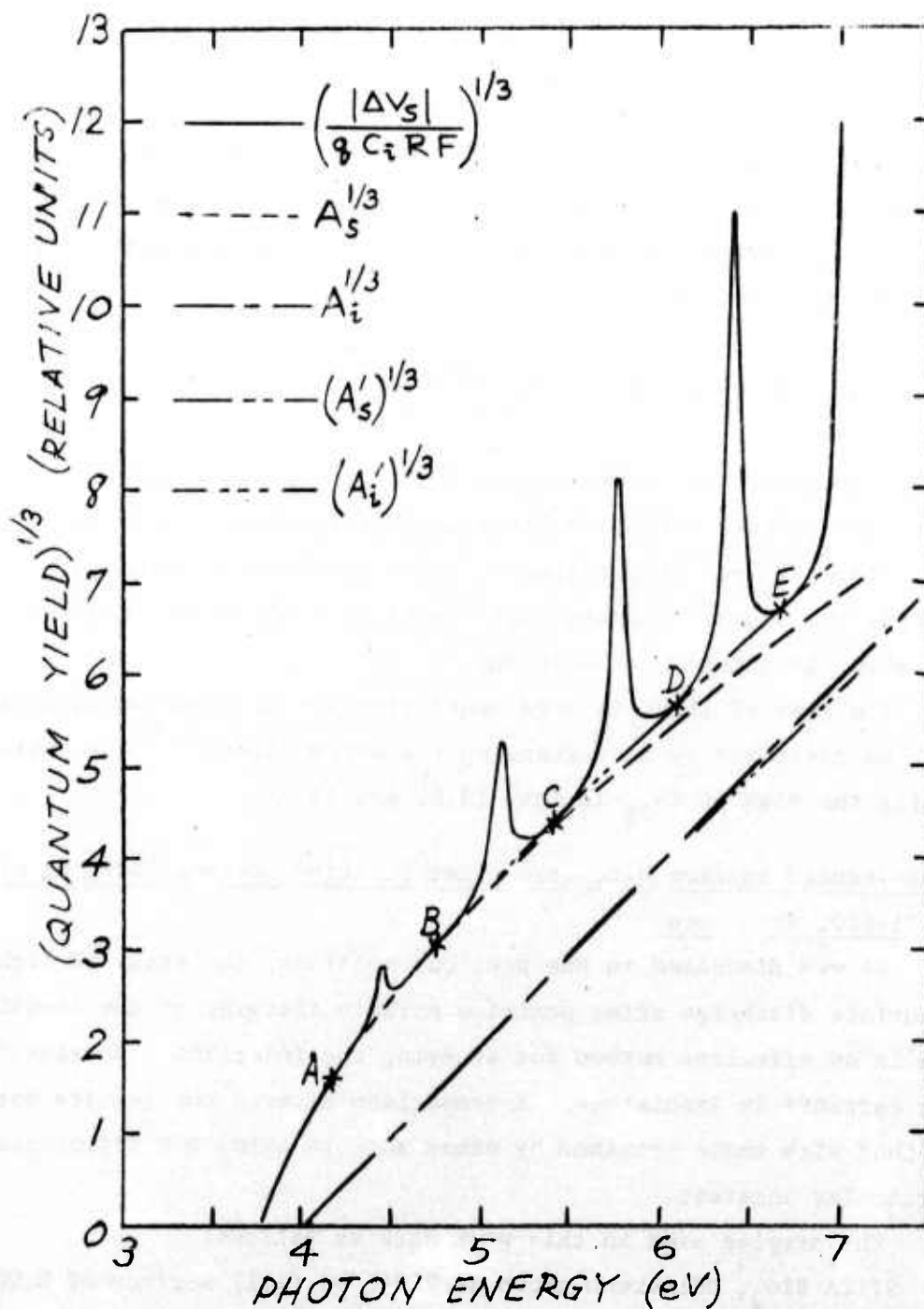


Fig. 3.4. $[\frac{|\Delta V_s|}{q C_i R F}]^{1/3}$ vs. $h\nu$ plot for an insulator-on-semiconductor structure with T/R as shown in Fig. 3.2 and A_i , A_s as shown here. A_i' and A_s' are calculated from this $[\frac{|\Delta V_s|}{q C_i R F}]^{1/3}$ vs. $h\nu$ curve by our proposed method.

dominant, the charge injected through the interface can be calculated from

$$Q_i = C_i (\Delta V_s - \Delta V_{FB}) \quad (3.6)$$

where C_i is the insulator capacitance, ΔV_s is the change of the surface potential, and ΔV_{FB} is the change of the flat-band voltage of the C-V curves. If hole injection from the front surface is dominant, the injected charge can be calculated from

$$Q_s = C_i (-\Delta V_s + \Delta V_{FB} \frac{x_t}{x_o - x_t}) \quad (3.7)$$

where x_o is the insulator thickness and x_t is the distance between the centroid of the trapped holes and the substrate-insulator interface.

Since ΔV_s and ΔV_{FB} rather than the current are measured, this method avoids the signal-to-noise ratio problem. This is particularly desirable when the quantum yield is small.

The case of light-induced neutralization of negative surface charge can be described by interchanging the words "electron" and "hole" and changing the sign of ΔV_{FB} in Eqs. (3.6) and (3.7).

3.3. Light-Induced Surface Discharge After Positive Surface Charging of the Si-SiO₂ Structure

As was discussed in the previous sections, the study of light-induced surface discharge after positive surface charging of the Si-SiO₂ structure is an effective method for studying the injection and transport of charge carriers in insulators. A comparison between the results obtained by our method with those obtained by other workers using MIS structures will be of particular interest.

The samples used in this work were as follows:

- (a) DN1: 5712A SiO₂, HCl-steam grown at 900°C on (111) surface of 0.001 Ω-cm n-type silicon.
- (b) N2 : 2500A SiO₂, HCl-steam grown at 900°C on (100) surface of 1 Ω-cm n-type silicon.
- (c) DP1: 5526A SiO₂, HCl-steam grown at 900°C on (111) surface of 0.001 Ω-cm p-type silicon.

Positive corona in dry air or N_2 was used to charge the surface to the desired potential. The maximum potentials used in this study correspond to oxide fields of 1.6×10^6 V/cm. After the corona was shut off, the chamber was pumped down to 10^{-3} torr. If the sample was kept in the dark, no change in surface potential was found after 24 hrs. The output of a Bausch and Lomb monochromator was used to discharge the surface potential to $V_s = V_{s(\text{initial})} - 2$ volts. After that, the chamber was filled with dry air or N_2 again and positive corona was used to charge the sample to its initial potential. The same process was repeated over a range of photon energies.

No flat-band voltage shift for the N_2 sample was found; hence there was no charge trapping in this sample. If we discharged the DN1 and DP1 sample repeatedly with light of the same photon energy, the discharge rate did not change. Hence there was no charge trapping in these samples.

Figure 3.5 shows the $|\Delta V_s|/qC_1 TF$ vs. photon-energy plot for the DP1 sample. Since the structure of R/T does not appear in the curves, the results suggest that the hole emission from the front surface may be neglected. Hence the quantum yield for electron emission from Si into SiO_2 for this sample is

$$\text{Quantum Yield} = \frac{|\Delta V_s|}{qC_1 TF} \quad (3.8)$$

The intercepts on the $h\nu$ axis correspond to the Si- SiO_2 barrier energy measured from the Si valence band for the particular value of oxide field. The change of barrier height with respect to field is consistent with Schottky lowering of the barrier if a dielectric constant equal to the optical value of 2.1 is used. The zero-field barrier energy is 4.3 eV. Those results agree with those obtained on MOS structures by other workers.²⁷⁻³⁵

The experimental results obtained on an N_2 sample showed the same characteristics.

There is additional evidence which shows that electron injection from Si into SiO_2 is the dominant process:

(1) The surface discharge is gas independent. If the injection of holes from the front surface were to contribute to the photocurrent, it would be expected that the characteristics of the surface discharge would depend on the species of ions on the front surface. However, the results shown in Fig. 3.6 do not show an ion dependence for the two gases used.

(2) Injection of electrons into the SiO_2 can take place from both the valence and conduction bands of the silicon. Evidence for this is shown in Fig. 3.7. For all three samples, extrapolation of $(\text{Quantum Yield})^{1/3}$ to zero shows an effective barrier height of 3.95 eV, which corresponds to the Schottky-lowered barrier from the silicon valence band to the oxide conduction band. The n-degenerate sample, DN1, shows a tail of injection at lower photon energies which, when plotted as in the inset of Fig. 3.7, indicates a barrier of approximately 2.9 eV. The difference between the two barriers corresponds to the band gap of silicon.

3.4. Summary

We propose here a new technique for studying charge-carrier injection and transport in thin insulating films. The technique uses internal photoinjection to provide the charge carriers and utilizes ions extracted from a corona discharge to charge the surface of the insulator and thus create the electric field required for transport. This method retains the principal advantage of the corona-charging technique, namely that high fields can be impressed on the insulator without danger of destructive breakdown. Also, the corona technique eliminates the need for a metal field plate and avoids the possible photoinjection that can take place from such a metallic overlay. The use of optical excitation to provide the carriers eliminates the dependence on high-field emission that was inherent in the original corona technique and thus introduces an additional degree of freedom into the experimentation. The origin and sign of the carriers can be analyzed by optical interference techniques.

We have verified the practicability of the method in preliminary experiments on the Si-SiO₂ system. With positive corona charging of the

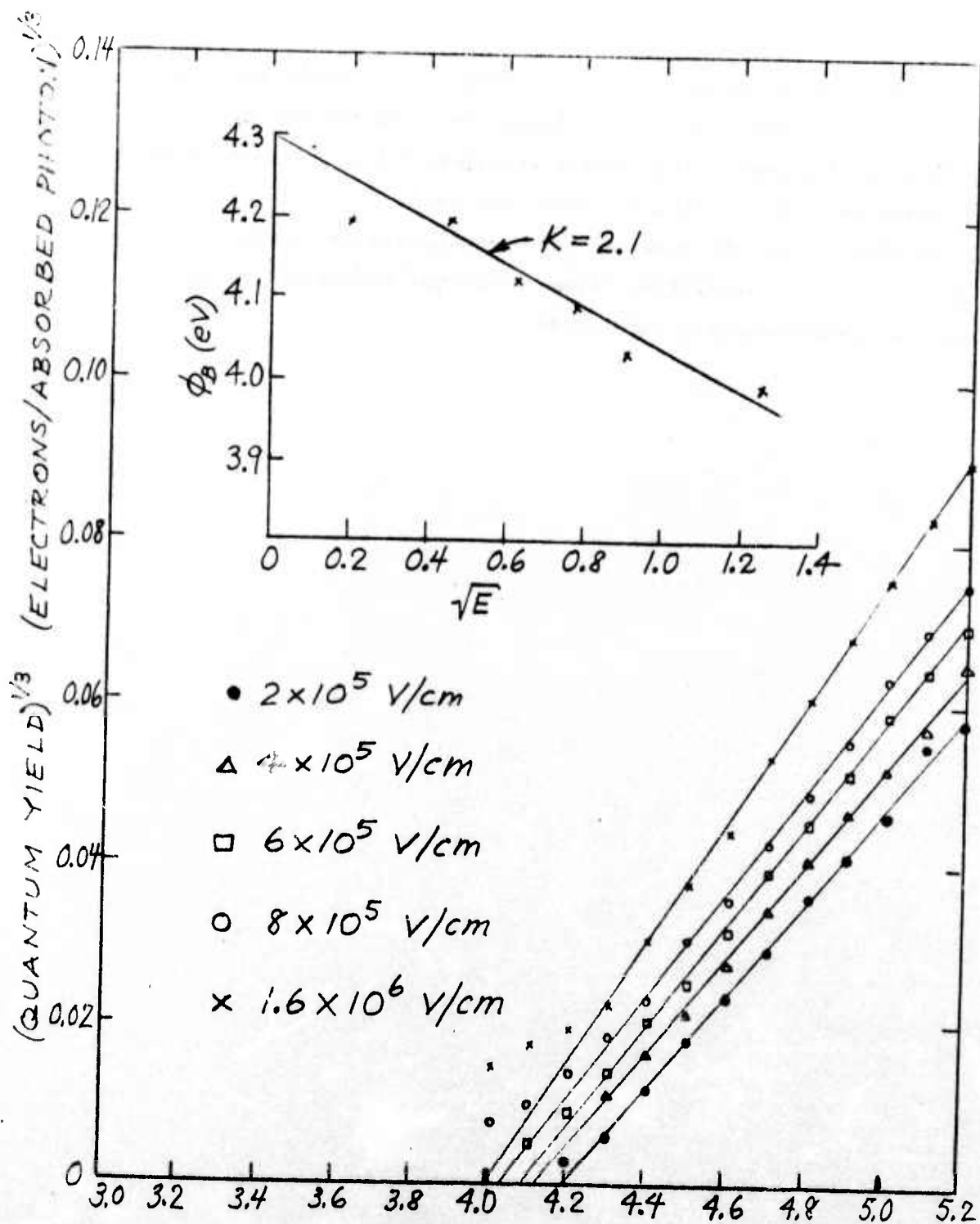


Fig. 3.5. $(\text{Si-SiO}_2 \text{ quantum yield})^{1/3}$ vs. photon energy for various fields. The Si-SiO_2 barrier energy ϕ_B (intercept on photon energy axis) 2 is plotted vs. square root of oxide field in insert. (DP1 sample.)

surface we observe electron photoinjection from the substrate into the oxide. The electron injection is principally from the valence band of the silicon at sufficiently large photon energies, but we can also observe electron injection from the silicon conduction band.

We plan to use the combined corona-photoemission technique in further studies of thin insulating films and of the properties of their interfaces with semiconducting substrates.

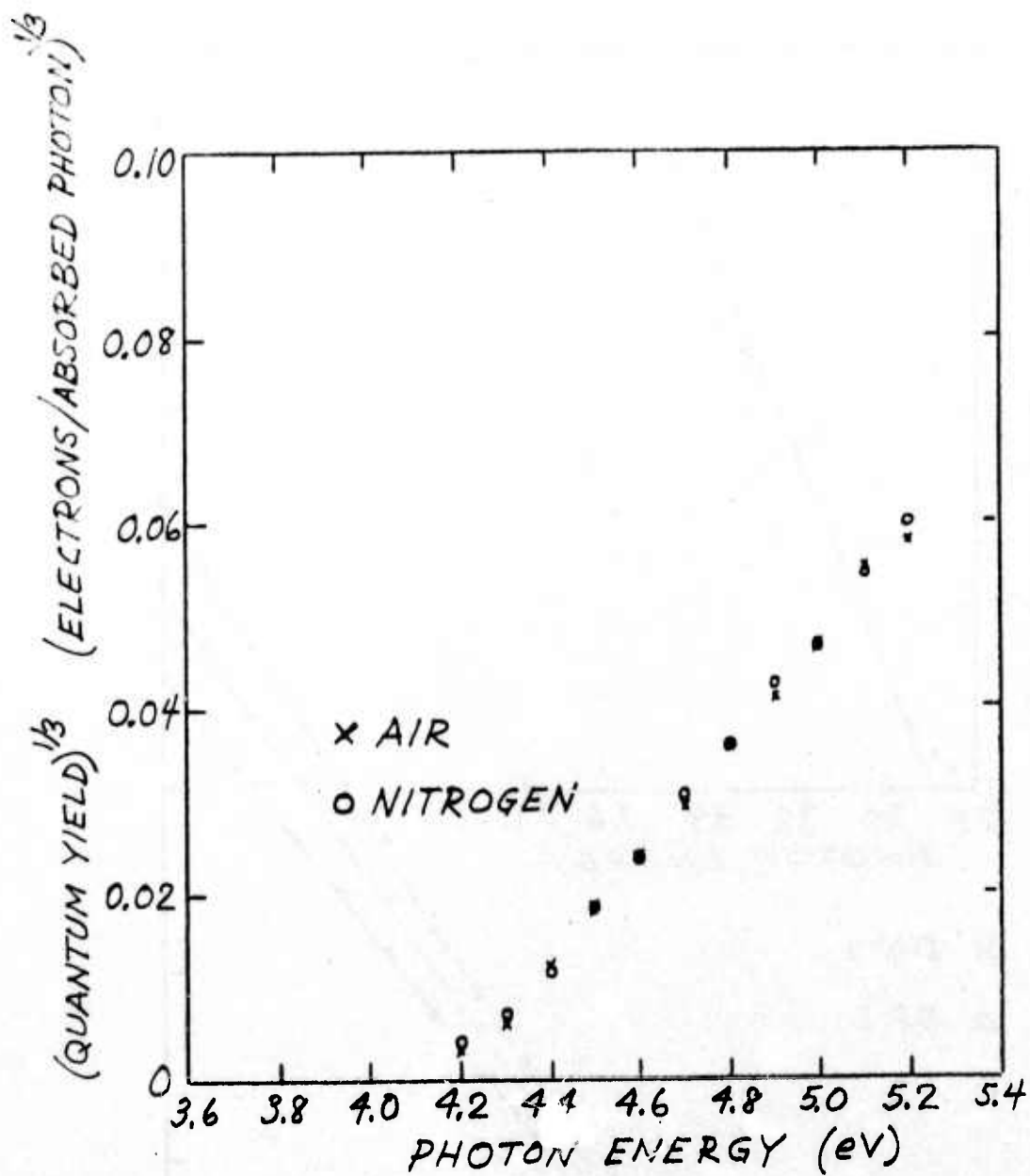


Fig. 3.6. (Quantum yield)^{1/3} vs. photon energy for an applied field of 0.2×10^6 V/cm. (DPI sample.)

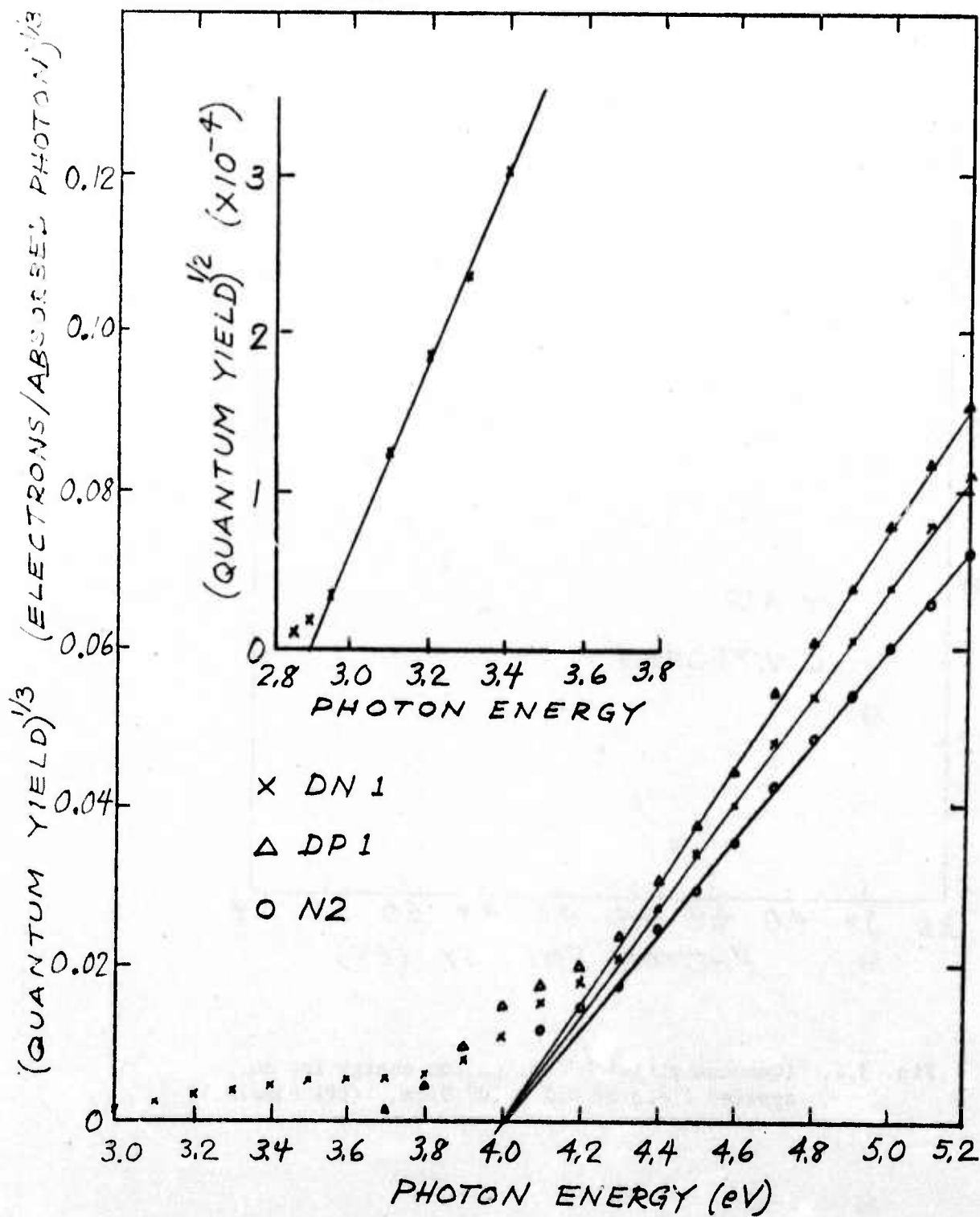


Fig. 3.7. $(\text{Quantum yield})^{1/3}$ vs. photon energy at $E = 1.6 \times 10^6$ V/cm for DN1, DP1, and N2 samples. Insert shows $(\text{Quantum yield})^{1/2}$ vs. photon energy for the low-energy part of the curve.

4. STUDY OF THE INTERFACE STATES GENERATED BY HIGH FIELDS IN THE Si-SiO₂ SYSTEM

(J. J. Clement and C. Jenq collaborating)

4.1. Introduction

Yang⁹ found that an MOS capacitor biased to a high field ($\sim 7.5 \times 10^6$ V/cm) with the field plate positive at low temperature ($\sim 100^\circ\text{K}$) for several minutes showed a parallel C-V shift in the negative-voltage direction. He attributed this shift to holes which were generated by impact ionization and then captured by hole traps in the SiO₂.

Chang²² studied this problem further and concluded that the parallelism of the C-V shift provided evidence that no interface states had been generated in the course of the high-field treatment at low temperature. After the sample was warmed, however, the room-temperature C-V curve showed a stretch-out. Chang was able to apply his diagnostic methods²² to show that the stretch-out was not caused by lateral nonuniformities in charge storage, as had been at first conjectured, but was due instead to interface states that had made their appearance during the warm-up process. He also found that if he assumed no redistribution of the trapped charges in the SiO₂ during the warm-up process, the charge-neutral level of the interface states lay close to the midgap.

In the remainder of this section we report on results that we have recently obtained in a further investigation of this problem.

4.2. Experimental Procedures

The samples were n-type, (100) silicon with 1-2 $\Omega\text{-cm}$ resistivity, having an HCl-steam grown oxide with a thickness of about 2500Å. The Al gate was about 1000Å in thickness, which permitted the breakdown of the oxide to be self-quenched by local evaporation of the Al gate.^{6,9,17}

The procedures of the experiment were:

- (1) The room temperature C-V curves of the sample was taken. The sample was then cooled to 91°K, and the C-V curve was again taken.
- (2) The sample was then biased gradually to the voltage that caused current multiplication to take place. This bias was held for a sufficient time to cause positive charging of the sample, typically 15 min.

- (3) The bias was removed and a C-V curve was taken.
- (4) The sample was warmed up to room temperature. During the warm-up process, a hole sweep-out bias, either positive or negative, was applied to the gate.

The room temperature C-V curves, both high-frequency and quasi-static, were taken in the dark. Of the C-V curves taken at lowered temperature, one set was taken in the dark with the gate voltage sweeping from accumulation into deep depletion at a rate of -1 V/sec. The others, which will be called "light-assisted" C-V curves, were taken by first bringing the sample into deep depletion, after which the sample was illuminated with ordinary light until the capacitance meter showed a steady maximum reading. The light was then cut off, after which the capacitance dropped to a lower value. The gate voltage was then ramped up at a rate of 1 V/sec.

4.3. Results

(A) Neutral Level of the Interface States

Figure 4.1 shows the room-temperature and the 91°K C-V curves of a sample which was subjected to steps (1) to (4) of the procedures described in the preceding section. Curve 1 is the room-temperature C-V characteristic, and Curve 2 is the 91°K C-V characteristic, both taken prior to high-field treatment. Curve 3 is the 91°K C-V curve taken immediately after the sample had been biased with the field plate positive at 188V for 15 min. Curve 4 is the room temperature C-V characteristic after the sample had been warmed up (in about 90 min) with the gate biased at -12.5V. Curve 3 shows a parallel shift of about -2.5V from Curve 2. Curve 4 is stretched out as compared to Curve 1, indicating the presence of interface states.

The capacitance at the point where the Fermi level is at silicon midgap is calculated to be $0.68 C_{ox}$. The voltage shift at this capacitance between Curves 1 and 4 is -2.55 V, which is reasonably close to the shift of -2.5 V at 91°K. Observations such as this led Chang²² to conclude that the neutral level of the interface states lies close to the silicon midgap. This conclusion, however, should be scrutinized carefully in the light of recent evidence, described in Part C of this section, which indicates that interface

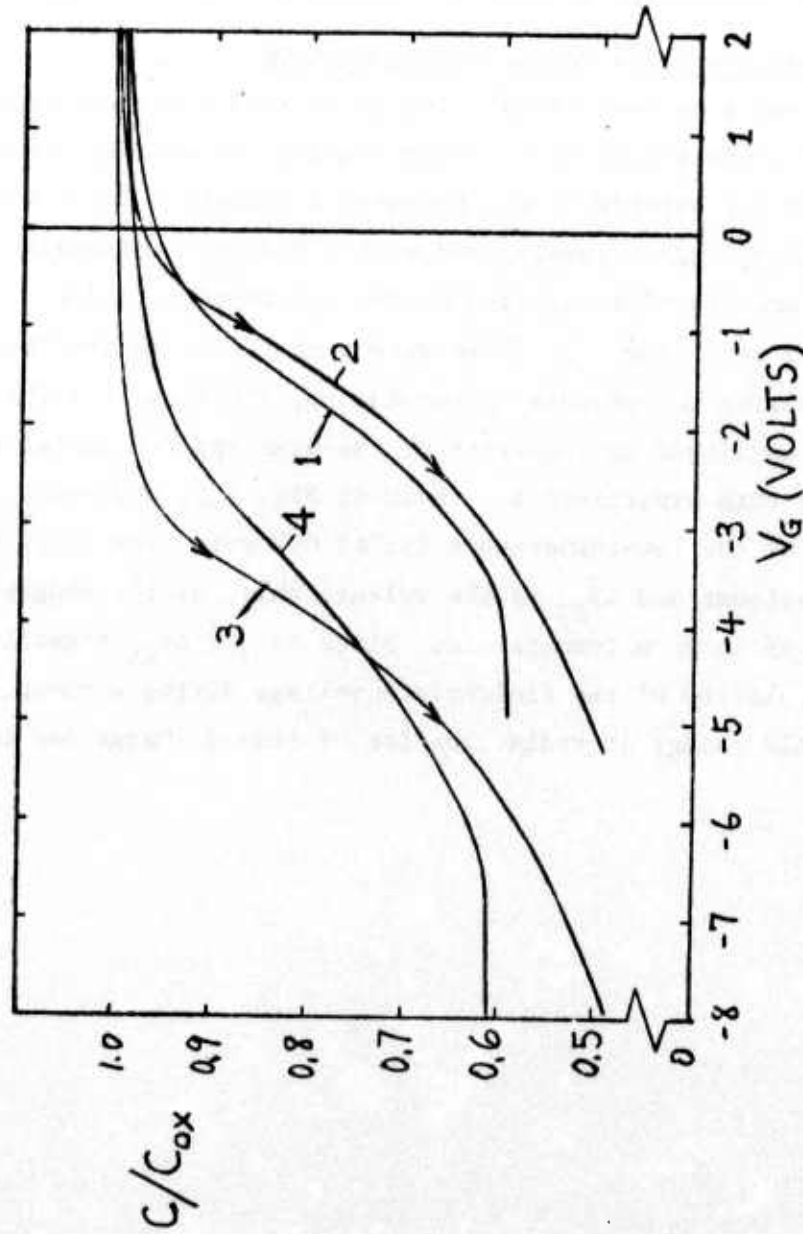


Fig. 4.1. C-V curves for the MOS structure.
Curve 1: Original characteristic.
Curve 2: At 91°K, before high-field treatment.
Curve 3: At 91°K, after application of 188V for 15 min, showing negative charge storage.
Curve 4: At room temperature, showing negative charge storage and interface states.

states of the acceptor type continue to be generated within the sample for many hours after warming up, and that the neutral level of these states cannot be at silicon midgap. We regard the voltage shift of the midgap capacitance to be the best available measure of the stored charge but it appears that the C-V curve should be taken as soon as possible after warm-up to minimize the distorting effects of continued interface-state generation.

(B) Stability of the Space Charge During Warm-Up

In order to test Chang's inference that there was negligible change or redistribution of space charge during the warm-up process,²² the above-described experiment was repeated a number of times with different amounts of high-voltage stressing and with different field-plate voltages, both positive and negative, applied during the warm-up period. A fresh sample was used each time. If there were a change or redistribution of space charge during the process of warming up, the final C-V shift should depend on the magnitude and polarity of the bias applied during warm-up. The results of this experiment are shown in Fig. 4.2, where ΔV_{LT} is the voltage shift of the low-temperature (91°K) C-V curve resulting from the high-field treatment and ΔV_{RT} is the voltage shift of the midgap capacitance after warming up to room temperature. Since $\Delta V_{RT} \approx \Delta V_{LT}$ regardless of the magnitude or polarity of the field-plate voltage during warm-up, we conclude that very little change or redistribution of stored charge has taken place.

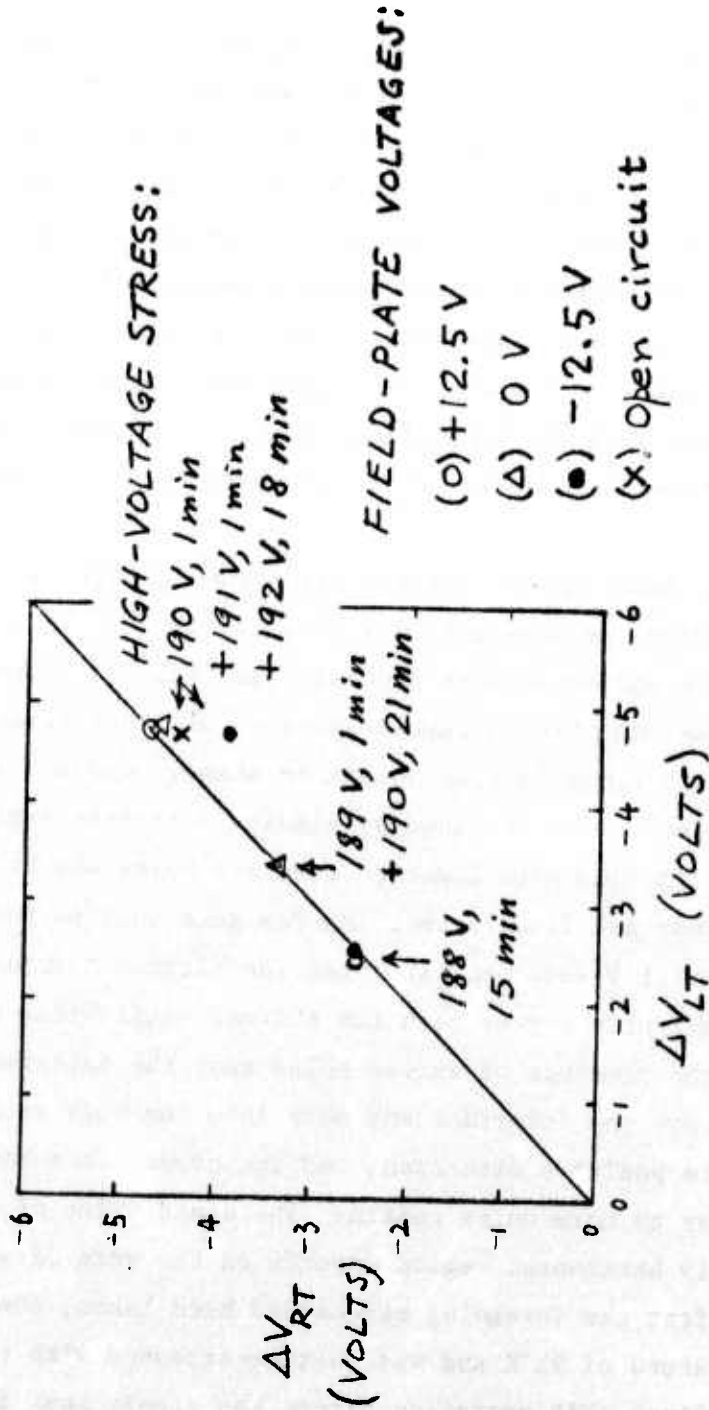


Fig. 4.2. Relation between the voltage shift of the low-temperature (91°K) C-V curve after high-field treatment, ΔV_{LT} , and the voltage shift of the midgap capacitance at room temperature, ΔV_{RT} , for different amounts of high-voltage stress and different field-plate voltages applied during the warm-up period.

(C) Continued Generation of Interface States After Warmup

As we have already observed, the application of a sufficiently large positive voltage to the field plate of an MOS structure results in both the storage of positive charge in the oxide and the generation of interface states; however, if the high field is applied at liquid nitrogen temperature, the positive charge appears immediately but the interface states do not make their appearance until the sample has been warmed up to approximately room temperature. Additional experiments, now to be described, show that the production of interface states, once it is initiated by the high field, continues to proceed for many hours at room temperature.

The experimental results are shown in Figs. 4.3 - 4.9. Curve 1 of Fig. 4.3 is the original C-V characteristic. This curve is almost ideal in shape and shows very few interface states. Curve 2 was obtained at 91°K by sweeping from accumulation into deep depletion at the rate of -1 V/sec. This curve is also normal in shape. Curve 3 is the 91°K "light-assisted" curve obtained by biasing into deep depletion, then temporarily flooding with light to generate holes and bring the sample into inversion, and finally sweeping the gate voltage toward accumulation at the rate of 1 V/sec. At first the capacitance remains almost constant at a value slightly higher than the thermal-equilibrium inversion value because of the presence of excess holes near the interface. These holes gradually leave the interface and move into the bulk as the gate voltage sweeps in the positive direction, and the capacitance begins its normal increase when no more holes remain. The exact value of capacitance in this approximately horizontal region depends on the rate of voltage sweep.

After the foregoing curves had been taken, the sample was held at a temperature of 91°K and was voltage-stressed with the field plate positive. Since this operation places the sample near its breakdown point, the stressing was done with great care. A voltage of 189 V was applied for 1 min, and when this was observed to result in only a moderate

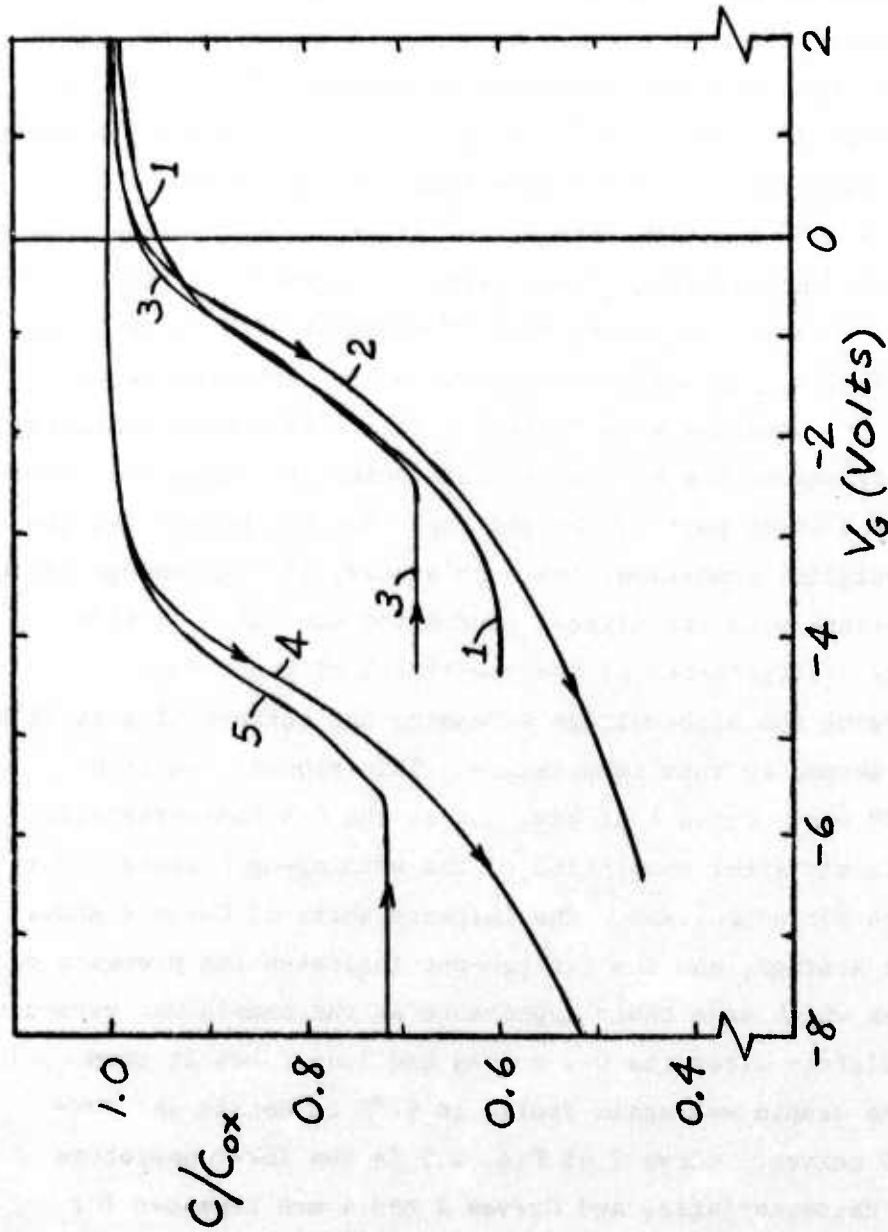


Fig. 4.3. C-V characteristics, 2500 Å SiO₂.
 (1) Original, at room temperature.
 (2) Original, deep depletion curve at 91°K.
 (3) Original, "light assisted" at 91°K.
 (4) Deep depletion curve at 91°K after stressing at 189 V for 1 min followed by 190 V for 21 min.
 (5) "Light assisted" curve at 91°K after stressing.

value of current, the voltage was increased to 190 V and was held for 21 min. Immediately after this, Curve 4 of Fig. 4.3 was taken. The negative shift of this curve as compared with Curve 2 indicates that the high-field treatment has resulted in the storage of positive charge in the oxide. Calculation shows that for this thickness of silicon dioxide, a one-volt shift corresponds to 8.4×10^{10} charges/cm² at the Si-SiO₂ interface. The observed voltage shift of 3.4 V thus indicates the presence of approximately 3×10^{11} positive charges/cm² after the high-field treatment. The corresponding light-assisted characteristic, Curve 5 of Fig. 4.3, shows the same effect. Curve 4 is almost exactly parallel with Curve 2, as can be seen in Fig. 4.9 (p. 44), where Curve 4 has been translated rightward until it coincides with Curve 2. This coincidence indicates that the high-field treatment has not, up to this point, produced any interface states in the upper part of the gap that were not present in the sample in its original condition, for such states, if high enough in the gap, can communicate with the silicon conduction band even at 91°K and should cause a stretch-out of the upper part of the curve.

Following the high-voltage stressing and curve-taking at 91°K, the sample was warmed to room temperature. This process required approximately 90 min. Curve 6 of Fig. 4.4 is the C-V characteristic obtained immediately after completion of the warming-up process. Curve 1 is repeated here for comparison. The leftward shift of Curve 6 shows positive charge storage, and the stretch-out indicates the presence of interface states which made their appearance as the sample was warmed up.

Immediately after the C-V curves had been taken at room temperature, the sample was again cooled to 91°K to obtain the low-temperature C-V curves. Curve 7 of Fig. 4.5 is the low-temperature deep-depletion characteristic, and Curves 2 and 4 are repeated for comparison. The presence of negative charge frozen into acceptor-like interface states is shown by the rightward shift of Curve 7 as compared with Curve 4. Curve 7 is not quite parallel with Curves 2 and 4, as is

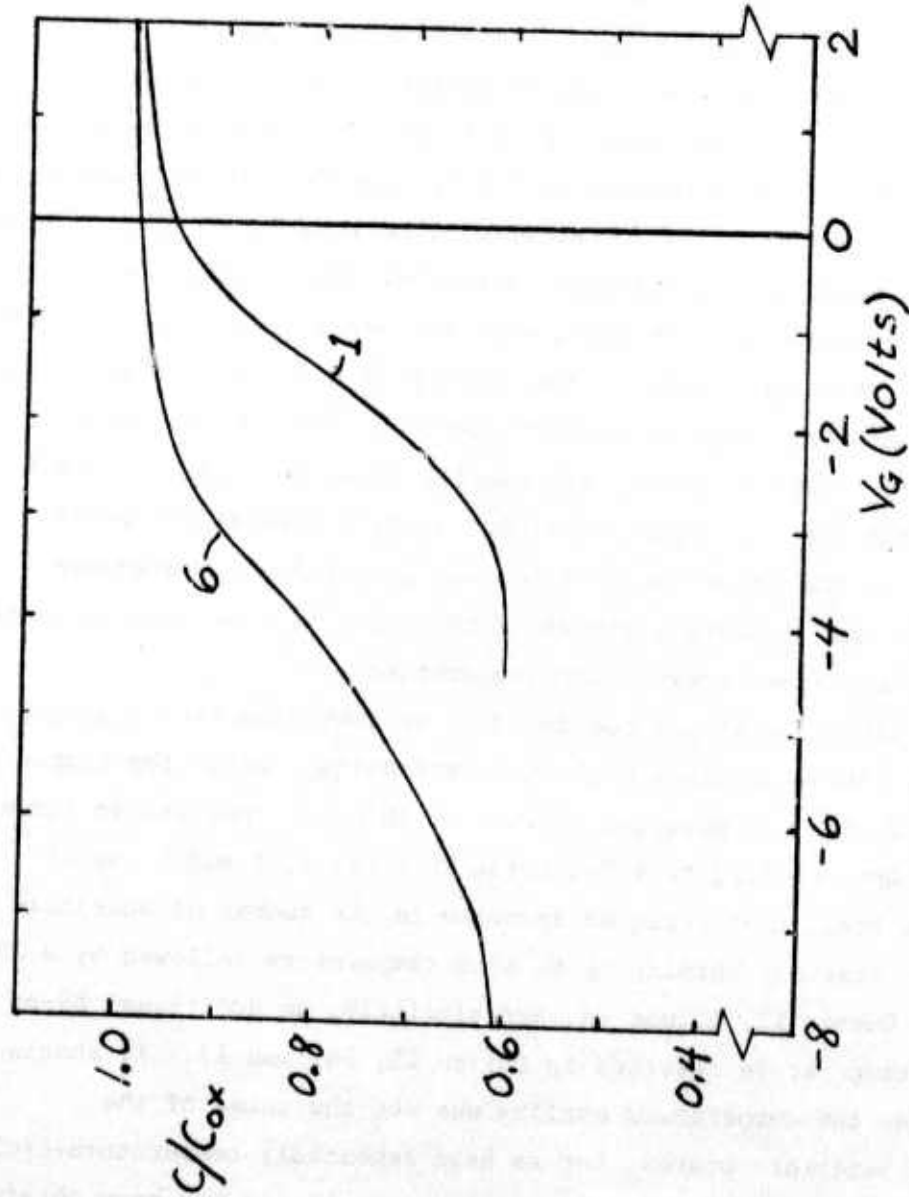


Fig. 4.4. Comparison between room-temperature C-V curves:
(1) Before stressing. (6) After stressing at
91°K and warmup requiring 90 min.

shown in Fig. 4.9 (p. 44). The discrepancy between the upper parts of the curves is caused by interface states which are present in Curve 7 and not present in Curve 4 and which are high enough in the gap to emit their electrons into the silicon conduction band even at 91°K. Electrons in deeper states are frozen-in and merely provide a fixed negative charge which partially compensates the positive charge stored in the oxide. Curve 8 of Fig. 4.5 is a light-assisted C-V characteristic in which temporary flooding of the interface with holes resulted in the neutralization of the negative charge in the acceptor-like interface states. As the gate voltage is swept in the positive direction, the electron concentration at the interface begins to rise, with the result that electrons are captured by the interface states. The buildup of negative charge at the interface produces the ledge observed in Curve 8, above which Curve 8 follows Curve 7. Taken together, the results shown in Figs. 4.3 - 4.5 indicate (a) that the high-field treatment at 91°K resulted in positive charge storage in the oxide but no immediate generation of interface states, and (b) that interface states of the acceptor type were generated as the sample was warmed toward room temperature.

The interface states continued to be generated over a long period of time without further high-field stressing. After the sample had warmed up to room temperature, a wait of 10 hours resulted in Curve 9 of Fig. 4.6. Upon cooling to 91°K, Curve 10 (Fig. 4.7) and Curve 11 (Fig. 4.8) resulted, indicating an increase in the number of acceptor-type interface states. Warming up to room temperature followed by a 20-hr wait produced Curves 12, 13, and 14, and similarly, an additional 69-hr wait at room temperature resulted in Curves 15, 16, and 17. It should be emphasized that the temperature cycling was not the cause of the generation of interface states, for we have repeatedly temperature-cycled unstressed samples between these two temperature limits and have obtained only characteristics like Curves 1, 2, and 3 of Fig. 4.3.

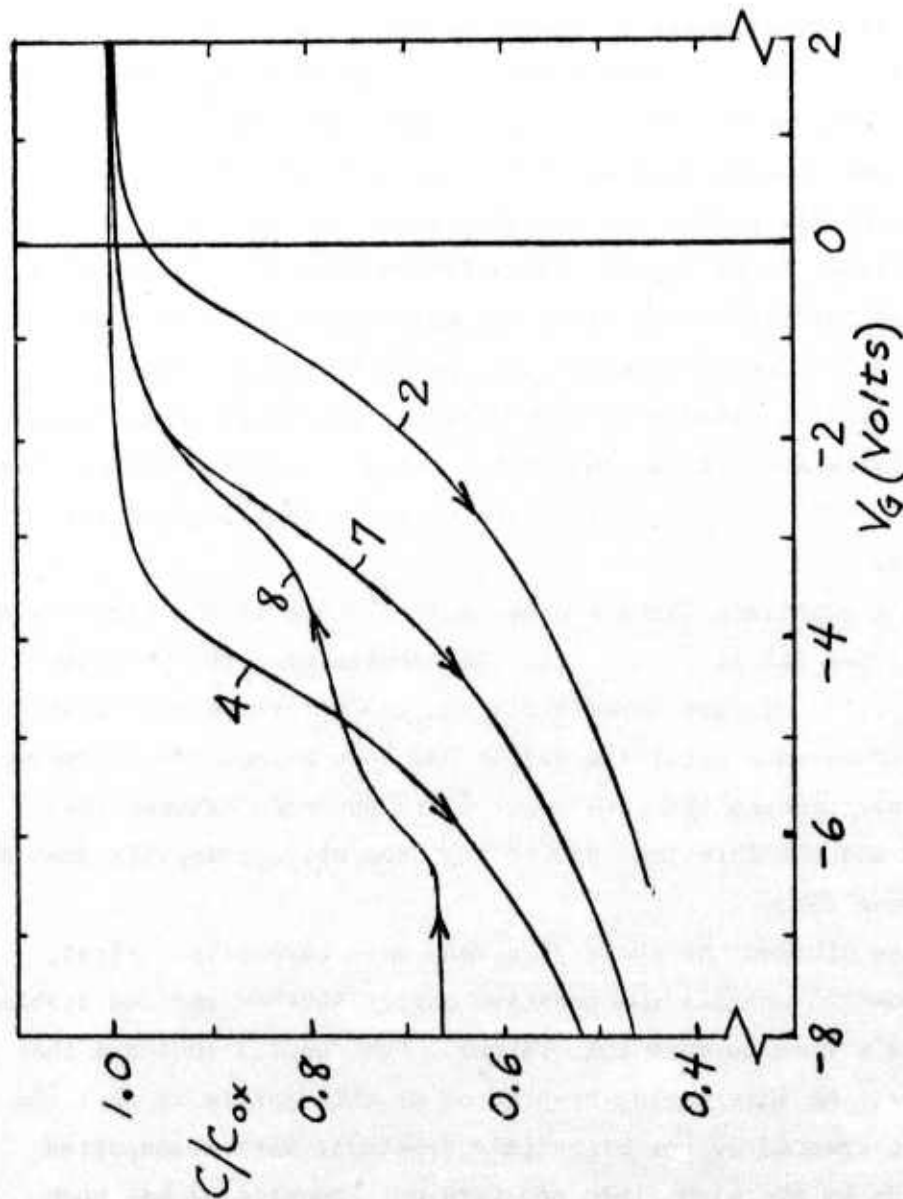


Fig. 4.5. Comparison between C-V curves at 91°K:
 (2) Original, deep depletion. (4) Deep depletion, immediately after stressing.
 (7) Deep depletion, after warmup and cooling down, (8) "Light-assisted," corresponding to Curve 7.

4.4. Conclusions

We find, in confirmation of Yang's observations,⁹ that high-field stressing ($\sim 7.5 \times 10^6$ V/cm) of an MOS structure with field plate positive results in the buildup of positive charge in the oxide. The positive charge is apparently that of trapped holes near the Si-SiO₂ interface. It is known that the current which flows through the oxide under these conditions consists of electrons which are injected into the oxide by Fowler-Nordheim tunneling from the silicon substrate, and the source of the holes is believed to be impact ionization in the oxide caused by a small fraction of the transiting electrons which gain sufficient energy in the high field to produce hole-electron pairs by lattice ionization (Sec. 2.2). It is also known that high-field stressing at room temperature produces interface states, and it has often been assumed that there is a one-to-one correspondence between the positive charging and the interface states.

We have confirmed Chang's observation²² that if the high-field stressing is carried out at liquid nitrogen temperature, the positive charging of the oxide appears immediately but the interface states do not make their appearance until the sample has been warmed toward room temperature. This removes the one-to-one correspondence between the positive charge and the interface states but does not necessarily deny a connection between them.

We have studied the above phenomena more carefully. First, there is the question whether the positive charge storage remains stable as the sample is warmed to room temperature. Our results indicate that it is indeed stable. An interesting by-product of this result is that the holes which were created by the high-field treatment were transported through the oxide by the high field and were not immobile as has been found with smaller fields at liquid-nitrogen temperature.⁴²⁻⁴⁴ Secondly, we find that interface states of the acceptor type continue to be generated at room temperature for many hours after the high-field treatment.

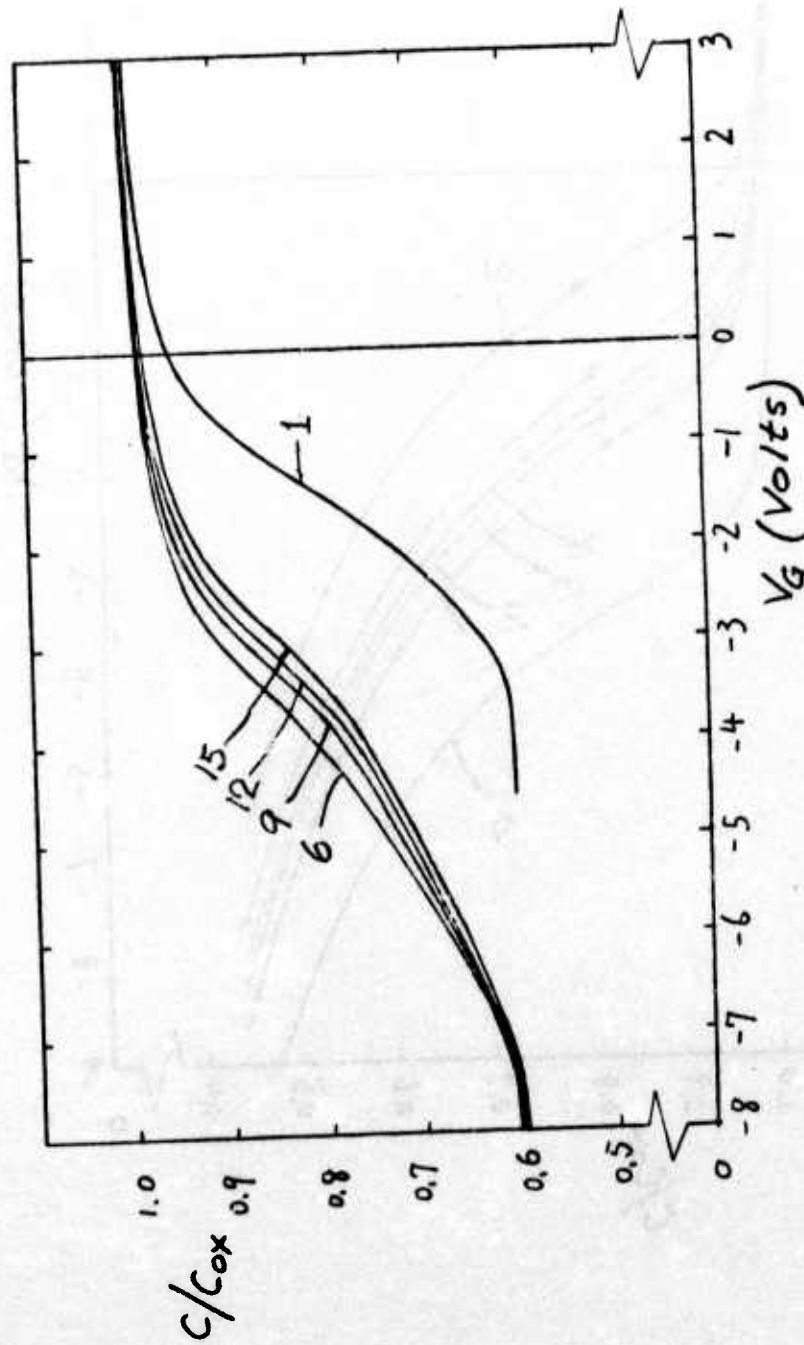


Fig. 4.6. Complete set of room-temperature C-V curves: (1) Original. (6) After stressing at 91°K and warmup. (9) After cooling, warmup, and wait of 10 hrs. (12) After cooling, warmup, and wait of 20 hrs. (15) After cooling, warmup, and wait of 69 hrs.

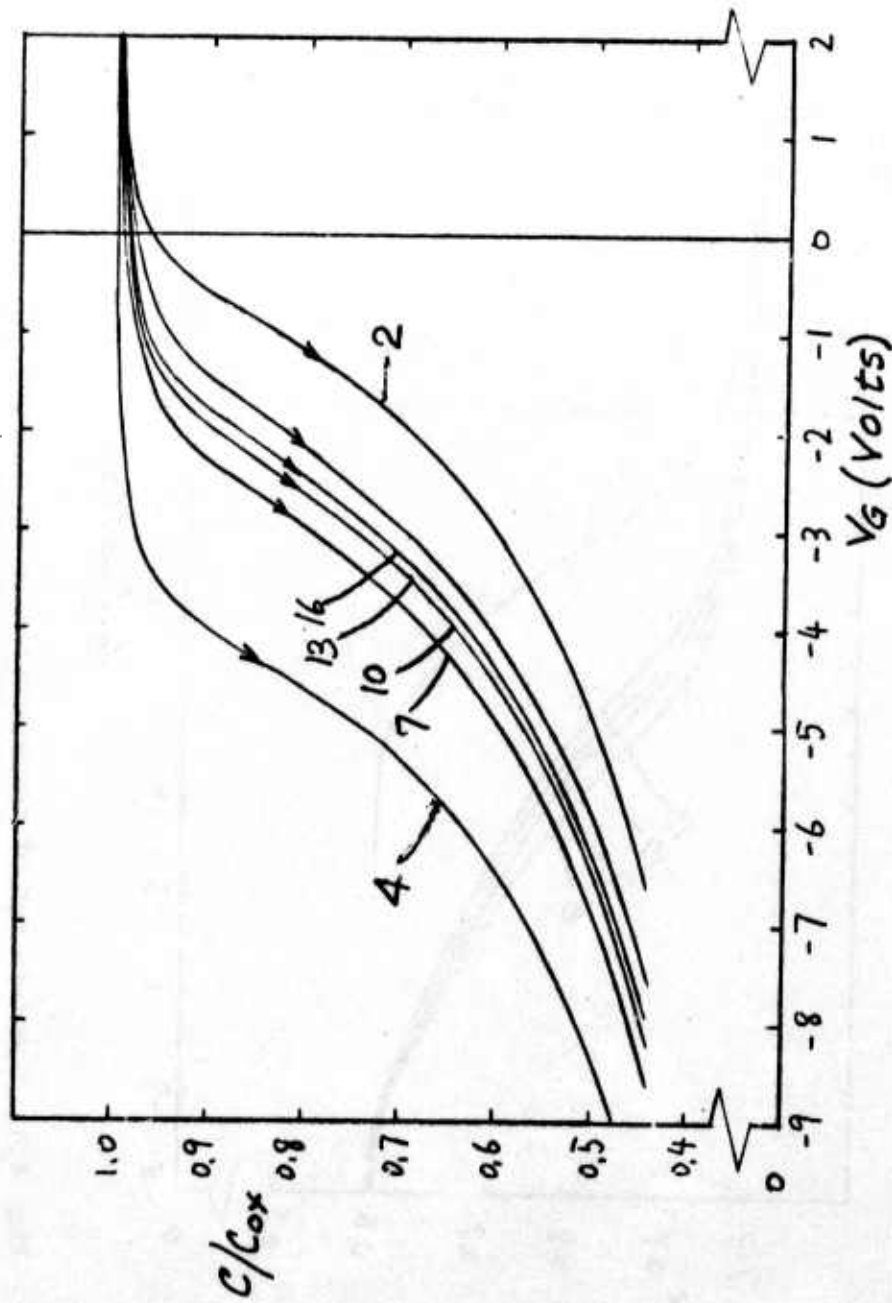


Fig. 4.7. Complete set of deep-depletion C-V curves at 91°K:
 (2) Original. (4) Immediately after stressing.
 (7) After warmup and cooling. (10,13,16) Taken after
 Curves 9-15 of Fig. 4.6.

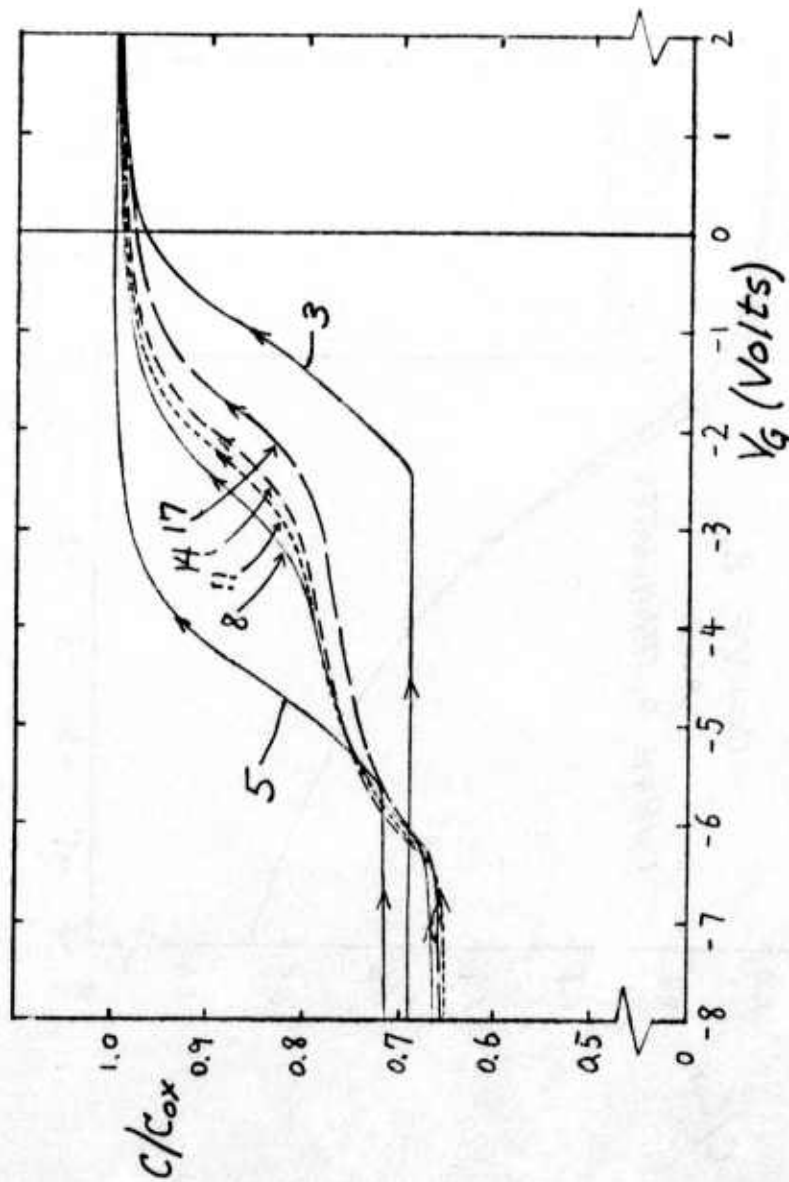


Fig. 4.8. Complete set of "light-assisted" C-V curves at 91°K. (3) Original. (5,8,11,14,17) Corresponding to Curves (4,7,10,13,16) of Fig. 4.7.

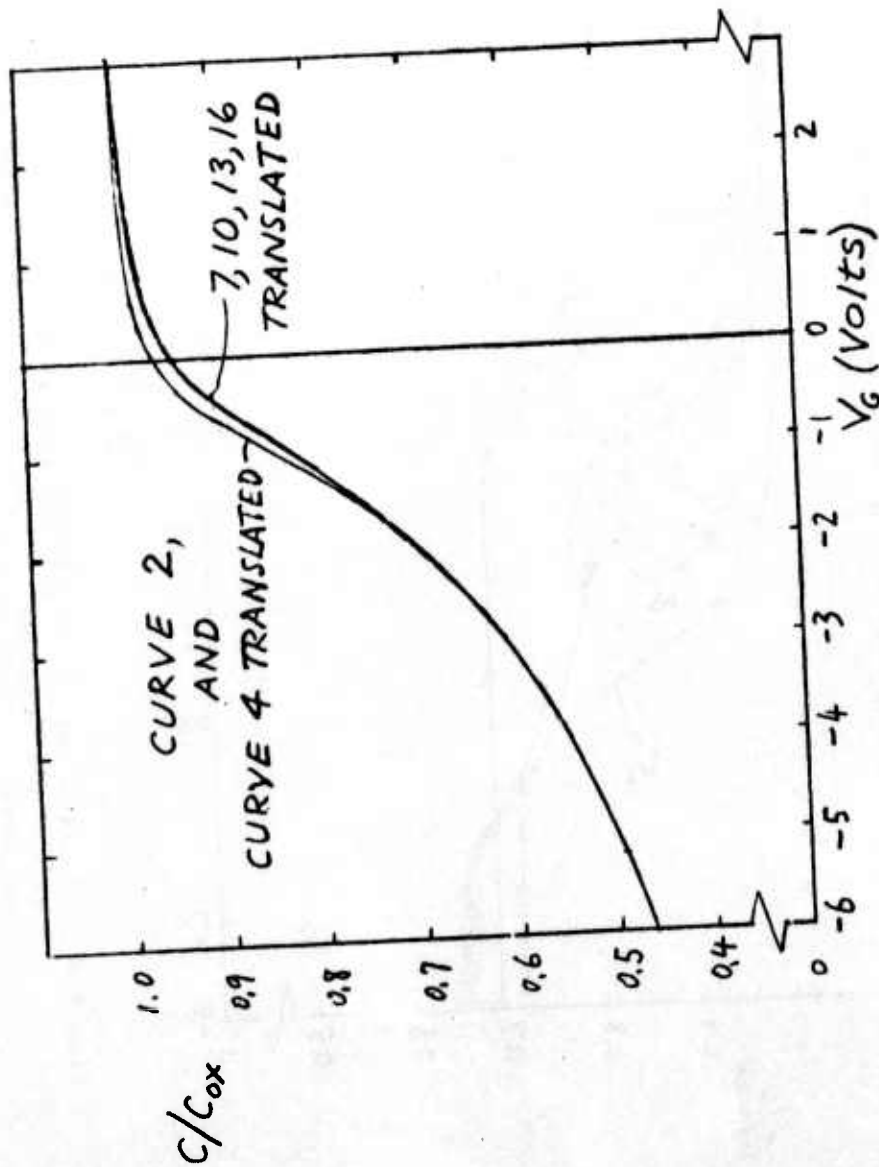


Fig. 4.9. Deep depletion curves after voltage stressing, translated to coincide with Curve 2 of the original sample in the depletion region. Curves Curve 4: Immediately after stressing. Curves 7, 10, 13, 16: After stressing, warming, and cooling.

5. HIGH-FIELD INSTABILITY IN THE MOS SYSTEM

(O. Bar-Gadda collaborating)

It has been reported by Osburn and Weitzman⁴¹ and by Yang^{9,17} that a slow instability appears on the application of a large (~ 8 MV/cm) field across a metal-SiO₂-Si capacitor. The instability occurs for both polarities of applied bias and appears to be independent of the electrode material. It occurs at comparable rates at both room temperature and liquid nitrogen temperature, and actually seems to be enhanced at low temperature. Previous observations of the instability have been rather sketchy, and it was our objective to study the phenomenon, and the mechanisms responsible for it, more carefully.

The current instability may be observed in two ways: by measuring the current-time (I-t) characteristic for different applied fields, or by comparing the current-voltage (I-V) characteristics (a) taken quickly and (b) in the steady state, if such a steady state exists. We have performed both types of experiments. The initial work in our laboratories was done by D. Y. Yang,^{9,17} and we have continued these studies.

Figure 5.1 is a Fowler-Nordheim plot for an Al-SiO₂-Si structure having a 2500-Å wet oxide and a 1000-Å Al field plate. The initial curve was measured over a period of several hours after first biasing the sample at a field of ~ 6 MV/cm for about 15 hours. The final curve was taken approximately a day later. The field is first held constant at a given value for about an hour and then incremented. When the incrementing process is completed, the field is decremented in steps, and the steady-state current is compared to the value obtained at the same applied field during the incrementing process to assure reproducibility. The curves are in good agreement with those measured by Yang and others. From the slope of the line we determine the effective mass for electron injection from the Si to be $m^* = 0.4 m_0$, in good agreement with previous determinations. We should mention, however, that this technique is not a very precise way of determining m^* or even the I-V curve. This is apparent from

Fig. 5.1, where it is seen that the magnitude of the current is very dependent on the previous history of the sample, i.e., how long the capacitor has been under high field stress. The reason for this is that the creation of interface states under high-field stressing reduces the current. Thus, under high field stress the current never reaches a true steady state, since the interface states are being continually formed. Nevertheless, for a short period of time the current relaxes to a value which would remain constant if no additional interface states were being created. To this extent one can measure an approximate steady state I-V curve for a fixed interface state distribution. The fact that the two curves shown give about the same slope (effective mass) which agrees with literature values indicates that the above assumptions are probably valid. If this is true, then it may explain the order-of-magnitude discrepancies in current measured by different people.

It can also be seen from Fig. 5.1 that at higher fields, the I-V curve seems to deviate upward from the Fowler-Nordheim straight line. This occurs for fields high enough to produce the current instability, in this case $E \sim 7.4$ MV/cm. This is easier to see in the I-t curves of Fig. 5.2. These curves were obtained by incrementing from 192 V to 195 V. For 192 V and 193 V there is an initial transient increase followed by a decay to steady state. For 194 V the maximum value of the transient is the steady state current. Above 194 V there is no steady state current, and the current builds up until destructive breakdown occurs.

An attempt was made to measure the I-V curve on a p-type sample also biased in accumulation to approximately 7.5 MV/cm. Here, no steady state current was observed. Instead, the current continually decreased. The C-V curve was measured initially and at the end of the experiment, some four days later. The result is shown on Fig. 5.3. The final curve shows distortion due to creation of interface states, and possibly a storage of positive charge in the oxide. A subsequent C-V curve taken four hours later shows that the voltage shift had been reduced slightly

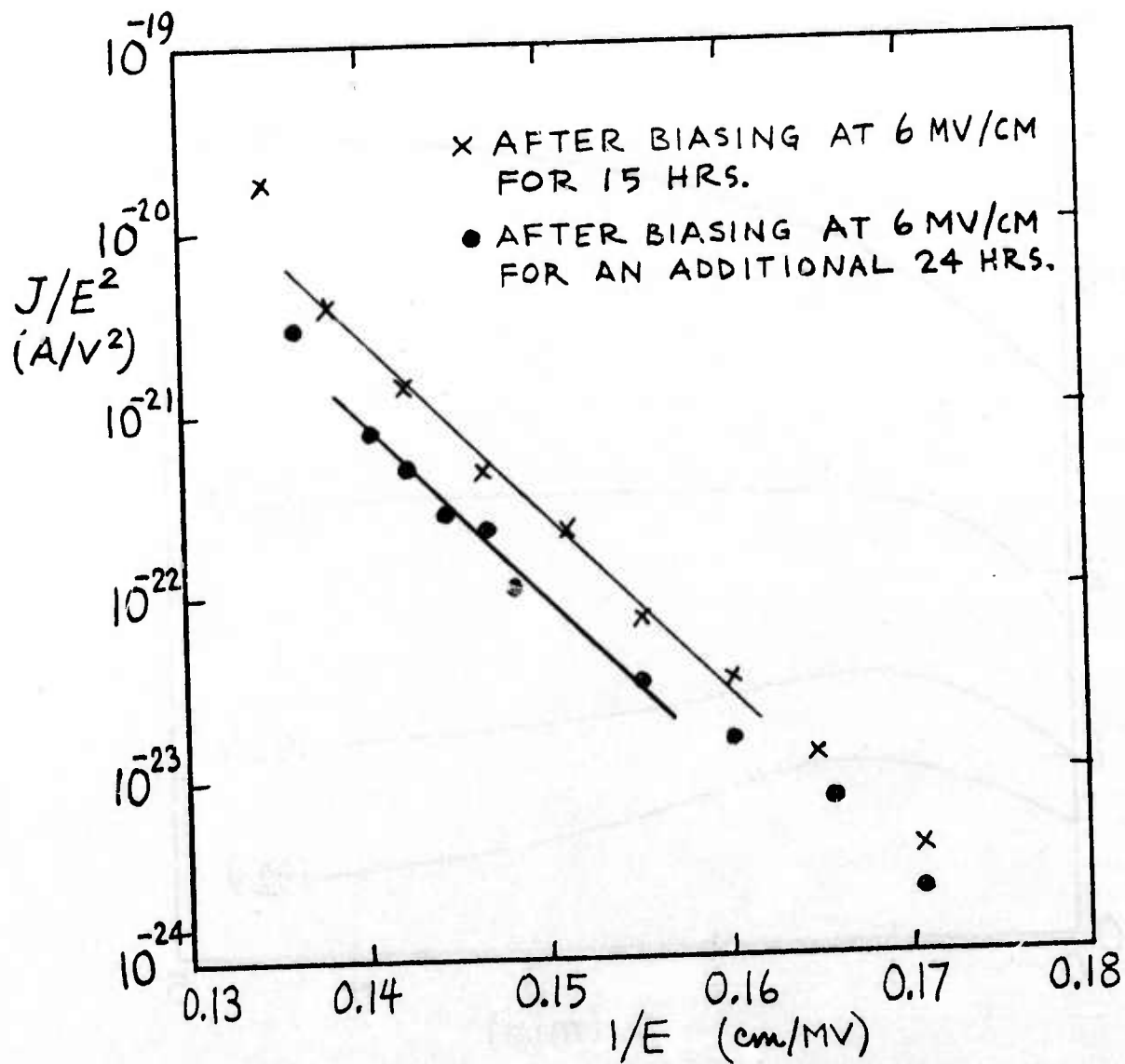


Fig. 5.1. "Steady-state" I-V characteristics.

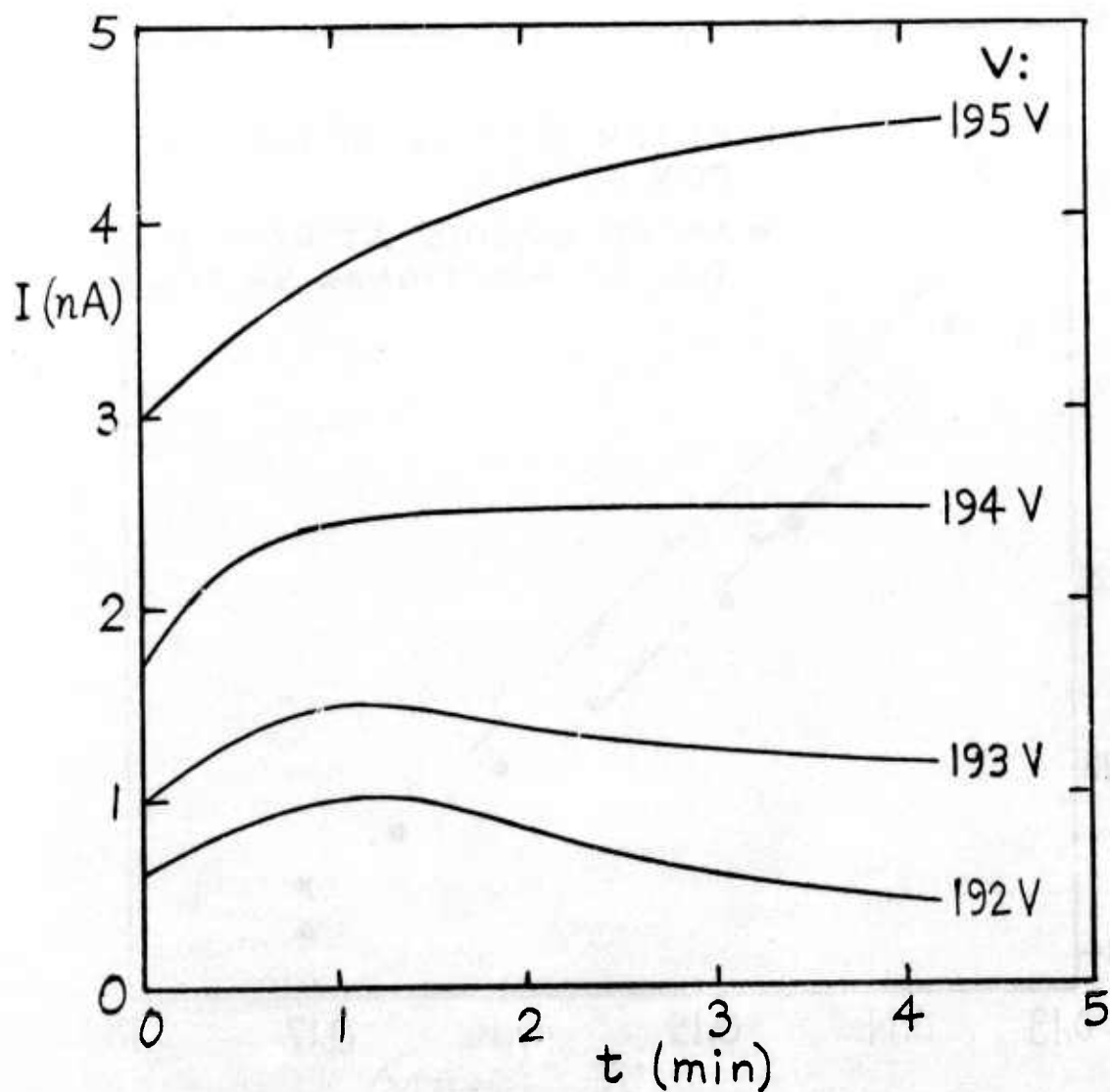


Fig. 5.2. High-field I-t characteristics. Oxide thickness = 2500 Å. Area of field plate = $1.3 \times 10^{-2} \text{ cm}^2$.

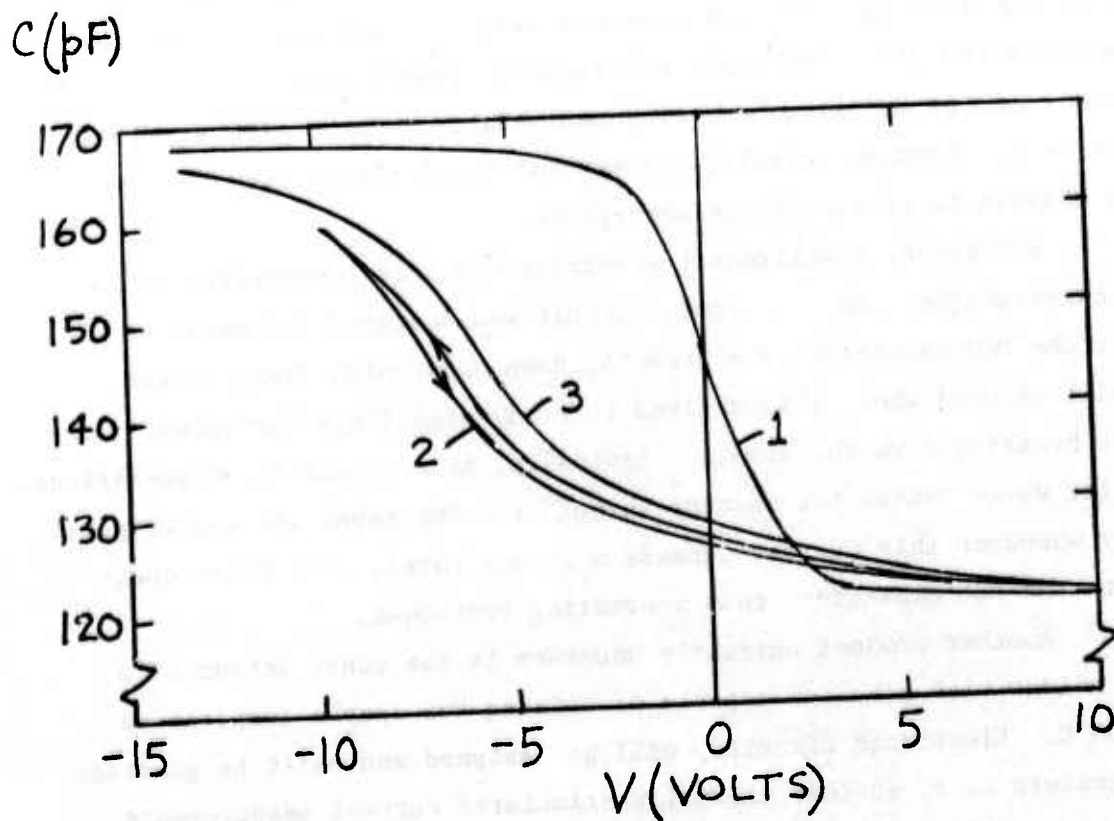


Fig. 5.3. Effect of negative bias stressing.
(1) Initial C-V curve.
(2) After 4 days at 7.5 MV/cm, field plate negative.
(3) Relaxation after 4 additional hours during
which sample was open circuited.
Field plate area = $1.3 \times 10^{-2} \text{ cm}^2$.

in magnitude. This effect has been observed by others and is generally referred to as the negative bias instability. Further investigation is planned.

The above results were obtained at room temperature in air. The sample was mounted on a gold-plated brass block and held down by a rough vacuum pressure. Dry nitrogen was used to continually flush the sample clean and dry. The probe was tungsten plated steel, and the probe pressure could be adjusted by a micromanipulator. The entire stage was mounted on an aluminum chassis, and several steel blocks were enclosed in the chassis to provide shock absorption.

Additional experimental apparatus has been constructed or is under construction. An electronic circuit was designed and built to protect the MOS capacitor from breaking down under high field stress. This will be used when it is desired to study high-field characteristics without breaking down the sample. Basically, it consists of an operational amplifier which senses the current through the MOS capacitor and triggers a relay whenever this current exceeds a preset level. The relay open-circuits the MOS capacitor, thus preventing breakdown.

Another project currently underway is the construction of a sample holder with a heater capable of raising the sample temperature to $\sim 400^{\circ}\text{C}$. Electronic circuitry will be designed and built to generate a temperature ramp, so that thermally-stimulated current measurements may be made. This will be used to investigate the nature of the hole traps in SiO_2 . We also wish to go to low temperatures (between liquid N_2 and room temperature) continuously and discretely so as to be able to investigate the high field current instability in this region of temperature.

6. SCANNING-ELECTRON-MICROSCOPE STUDIES OF LATERAL NONUNIFORMITIES

(P. Roitman and D. Guterman collaborating)

The existence of lateral nonuniformities in the metal-insulator-semiconductor (MIS) structure is of great concern. We have developed methods for utilizing the scanning electron microscope to image the internal structures of MIS devices. The beam of the electron microscope is used to induce a current within the sample, and an image is formed by the variations in this current as the electron beam is scanned in a raster over the surface of the sample.^{13,14,18} We have used the electron-beam induced current (EBIC) technique chiefly with conventional MOS structures utilizing a silicon dioxide insulator; however, implanted oxides and capacitors incorporating Al_2O_3 dielectric films have also been examined. Two types of structures, namely stacking faults and ion aggregates, have been extensively studied in MOS capacitors, and models have been developed to explain the observed images.

Stacking-fault (SF) structure is seen under low magnification as a scattering of small dots, visible in the EBIC mode and not present in secondary-emission mode. Under high magnification the dots are resolved into lines approximately $2-5 \mu$ long $\times 0.5 \mu$ wide. Figure 6.1a shows an example of this structure. The sample consisted of p-type Si, $1\Omega\text{-cm}$ boron doped, with a $3500 \text{ \AA}$ oxide HCl -steam grown on the (100) surface at 900°C . After oxide growth the sample was annealed in He at 1050°C for 15 minutes and in H_2 at 500°C for 15 minutes. A significant feature is that the lines are oriented in either the $[110]$ or $[\bar{1}10]$ directions. This orientation is characteristic of stacking faults on the (100) face of the diamond lattice.

In order to further determine the nature of the contrast observed at these structures, line scans were performed. In the line-scan mode, information is displayed on the CRT using deflection modulation rather than intensity modulation. A measure of contrast is obtained from the peak-to-peak height of the structure current measured at the substrate.

The contrast dependence of the structures was measured as a function of beam energy, beam current, gate bias and scan speed.

In general, a scan across the fault produces a structure current that is approximately a differential gaussian. The structures are not visible for beam energies below that required to completely penetrate the gate and the oxide. Above that value the contrast rises very rapidly with beam voltage for a few keV and then saturates.

The gate-bias dependence is shown in Fig. 6.2 for both p-substrate and n-substrate capacitors. The structures were visible only for positive (> 0 V.) bias in the p-sample and negative (< -15 V.) bias in the n-sample. This seems to imply that depletion is required for visibility in the former, while strong inversion is required for the latter. However, local oxide charging created during the line scan can dominate the state of the substrate. In the case of the p-sample with the gate biased slightly positive, holes became trapped at the Si/SiO₂ interface, tending to further deplete the substrate. In the n-sample with negative gate bias, holes became trapped at the gate/SiO₂ interface. These have little effect on the substrate other than tending to accumulate it slightly, requiring additional negative bias to maintain inversion. Further, when the bias is suddenly switched, time is required for the contrast to build up or decay, implying that oxide charging/discharging is important. It therefore appears that oxide charging does affect contrast, and that the structure is only revealed fully when the substrate is in inversion.

Contrast was found to increase linearly with beam current up to beam currents of ~ 100 pA, beyond which it tended to saturate. Image distortion also occurred at high beam currents due to spreading of the incident beam.

The dependence of the structure on scan speed is shown in Fig. 6.3. For low speeds the peak-to-peak current scales with the scan speed. Therefore, the time integral of the current is constant, i.e., the net flow of charge through the sample is independent of scan speed. At

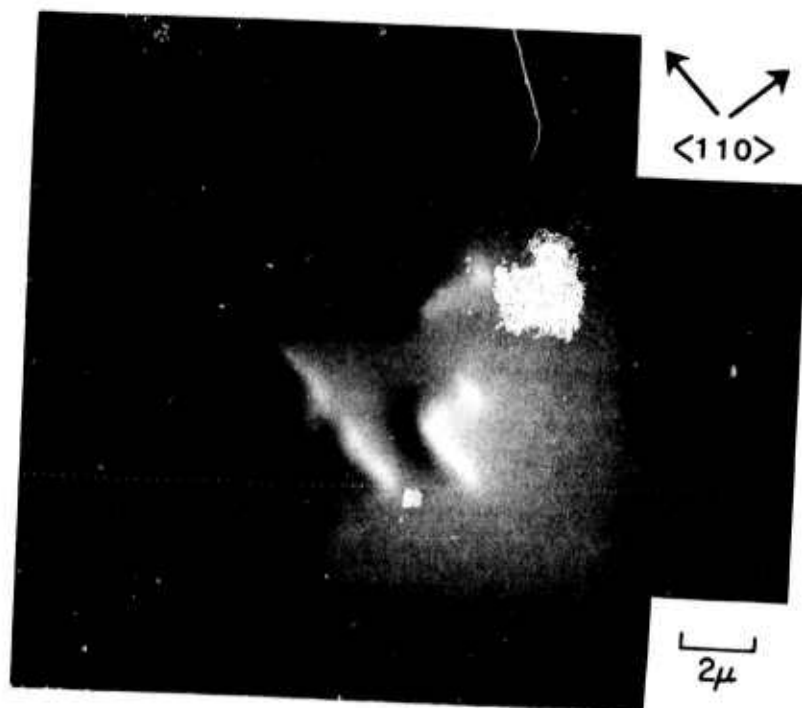


Fig.61a. Electron beam induced images of oriented "SF" structure in sample ST5. Imaging conditions: 35.9KeV, $V_g = 15V$, Mx 5000.

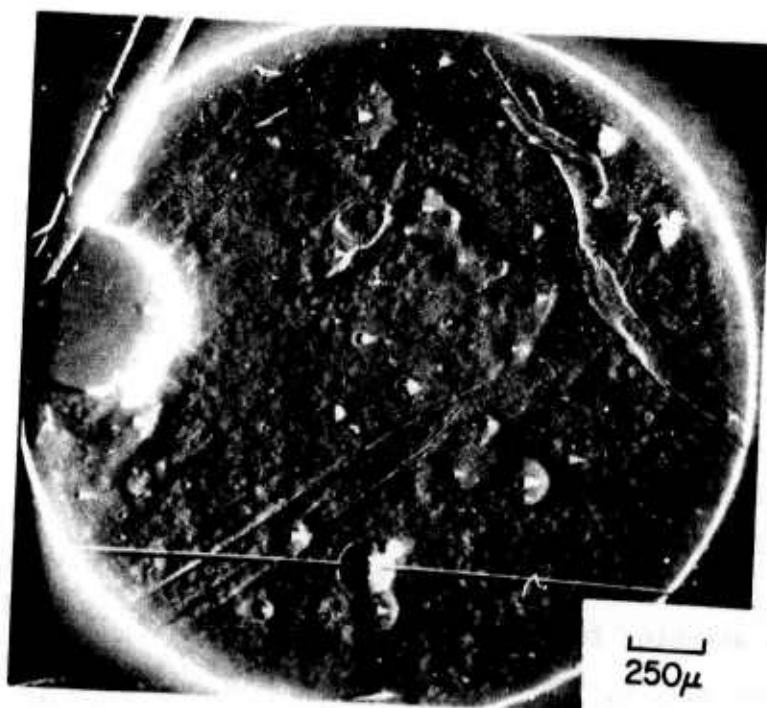


Fig.61b. Beam induced current image of sample ST19, taken after ion drift to the substrate, and bias thermal stressing for 10 hrs. at 300°C, $V_g = +20V$. Image reveals a large, highly contrasted IA structure with a bisecting line showing where line scans had been performed.

higher scan speeds ($\sim 10^{-2}$ cm/sec) the structure becomes distorted, indicating that the beam speed exceeds the time required for the beam-induced carriers to respond. Finally, opposite current polarities are observed in the two samples. In the case of the p-sample there is an initial flow of electrons out of the substrate to ground, and the flow reverses as the beam leaves the structure. For the n-sample the opposite occurs.

A model has been developed for the stacking-fault contrast mechanism. The current detected is a displacement current resulting from modulation of the depletion-layer capacitance. The modulation is caused by hole-electron pairs produced in the silicon by the incident beam.

A one-dimensional analysis has been made of the surface voltage and depletion-layer capacitance and charge in an MOS structure with constant applied voltage under electron illumination. The model assumes a gaussian incident beam of very penetrating electrons moving across the plane of the interface. The resulting displacement current is given by¹⁸

$$I(t) = \frac{C_o v I_o}{2\pi\beta\sigma^4} \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} \frac{g\tau}{d} (x - vt) e^{-[(x-vt)^2 + y^2]/2\sigma^2} dx dy \quad (6.1)$$

where C_o is the oxide capacitance, v is the beam velocity (in the x-direction), β is kT/q , I_o is the current in the incident beam, σ is the width of the incident beam, g is the pair generation per incident electron per unit length, τ is the lifetime of excess carriers in the substrate, and d is a rather complicated function of the substrate carrier concentrations which, however, tends to a constant in both accumulation and inversion. Note that if g , τ and d are independent of position, the integral is zero.

If the stacking fault is represented as a step in $g\tau/d$ of width W and height $g_1\tau_1/d_1$ over a background of $g_o\tau_o/d_o$, integration of Eq. (7.1) provides the result¹⁸

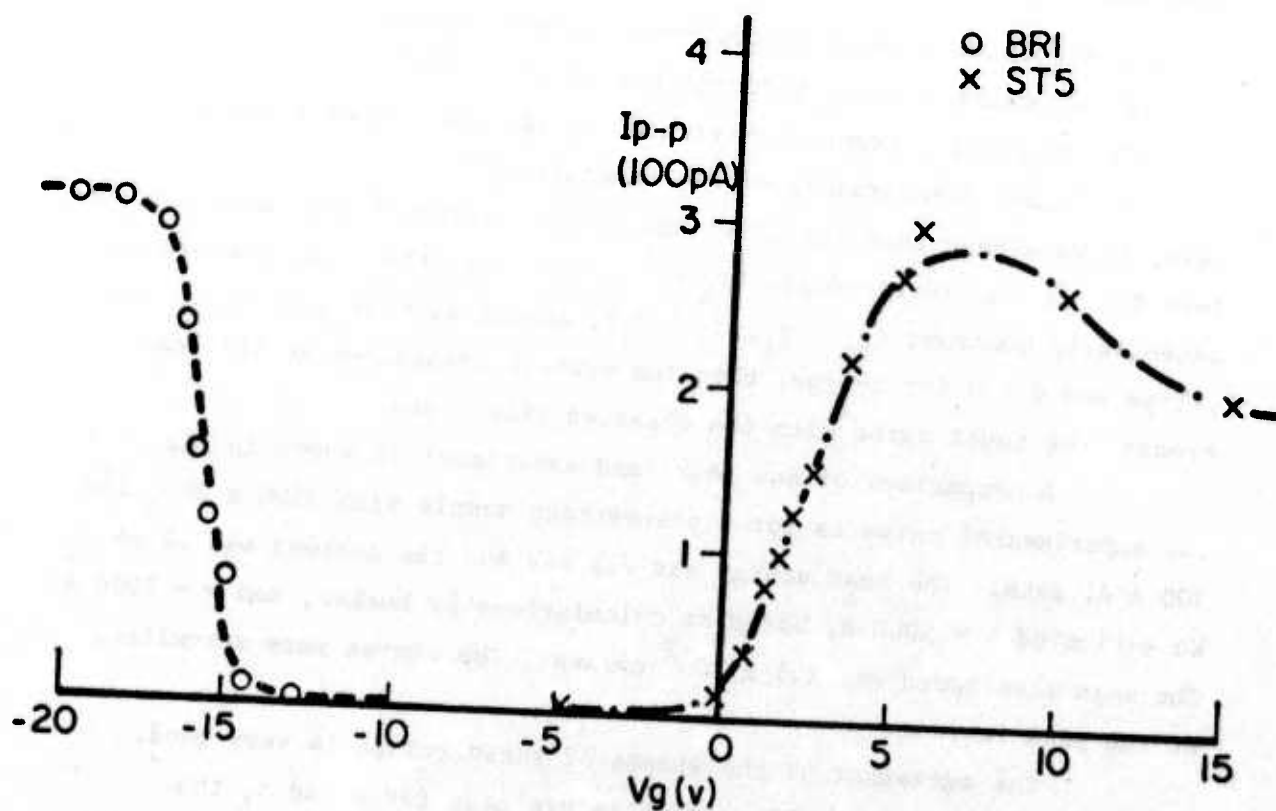


Fig. 6.2. Peak-to-peak current, providing a measure of image contrast, when the electron beam is scanned across a stacking fault, plotted as a function of gate bias applied to the MOS structure. Beam current = 100 pA. Sample BRI: 1 Ω -cm (100) n-Si with 1200 $\text{\AA}$ dry-grown SiO_2 . Sample ST5: 1 Ω -cm (100) p-Si with 3500 $\text{\AA}$ HCl-steam SiO_2 .

$$I(t) = \frac{C_o v I_o}{\sqrt{\pi \beta \sigma / 2}} \left(\frac{g_o \tau_o}{d_o} - \frac{g_1 \tau_1}{d_1} \right) e^{-w^2/2\sigma^2} e^{-(vt)^2/2\sigma^2} \sinh wvt/\sigma^2 \quad (6.2)$$

This expression includes the essential qualitative features experimentally observed in the induced currents:

- (1) structure current proportional to beam current,
- (2) structure current proportional to scan speed,
- (3) structure current much greater in inversion than accumulation [since $d(\text{inversion}) \ll d(\text{accumulation})$].

Also, if we assume that the lifetimes in the region of the fault are much less than in the surroundings ($\tau_1 \ll \tau_o$) and that the other factors are essentially constant ($g_o \sim g_1$, $d_o \sim d_1$), and if we note that $d > 0$ for p-type and $d < 0$ for n-type, then the current polarities as the beam crosses the fault agree with the observed line scans.

A comparison of Eq. (6.2) and experiment is shown in Fig. 6.4. The experimental curve is for a p-substrate sample with 3500 Å SiO_2 and 300 Å Al gate. The beam energy was 7.5 keV and the current was 10 pA. We estimated $\sigma = 5000$ Å, based on calculations by Nosker, and $w = 5000$ Å. The beam scan speed was 2.5×10^{-2} cm/sec. The curves were normalized at the peak current.

The agreement of the shapes of these curves is very good. Unfortunately, if reasonable estimates are made for g and τ , the amplitudes do not agree well, for the calculated current is much smaller than the observed current. The model includes two critical assumptions. One is low-level injection; that is, the density of pairs generated by the beam is assumed to be much less than the background doping density. Arithmetically, this turns out to be false. However, the theory for high-level injection has also been done, and it does not exhibit the qualitative agreement discussed above. Second, the model for the MOS structure is one dimensional, it assumes a steady state situation, and

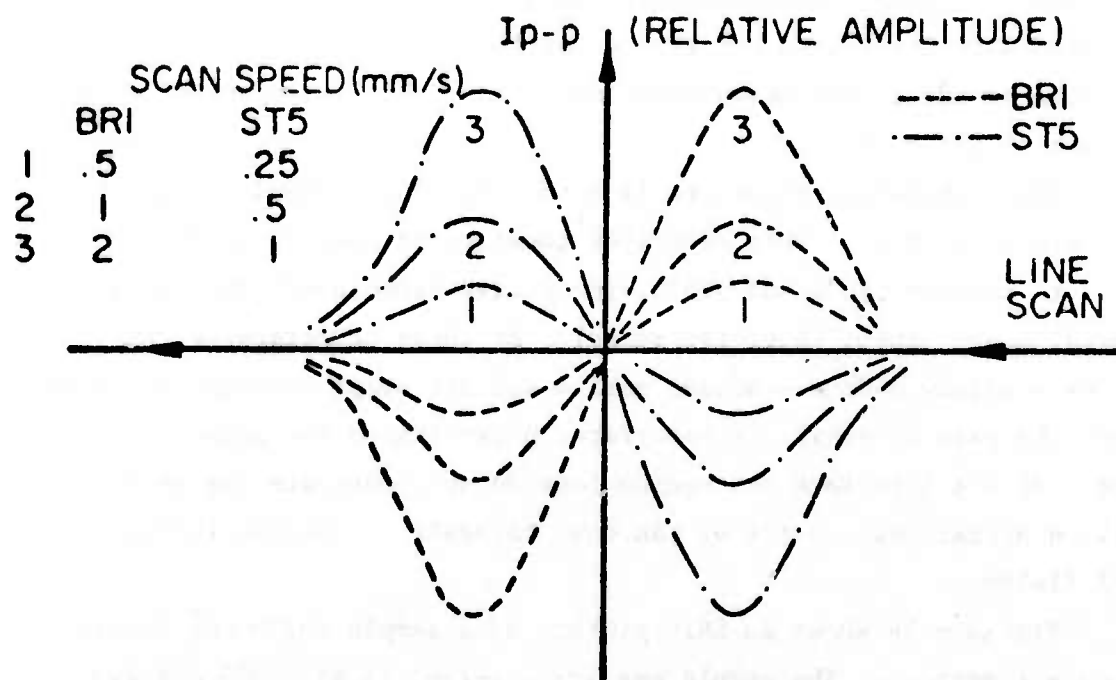


Fig. 6.3. Dependence of stacking-fault image contrast on scan speed.

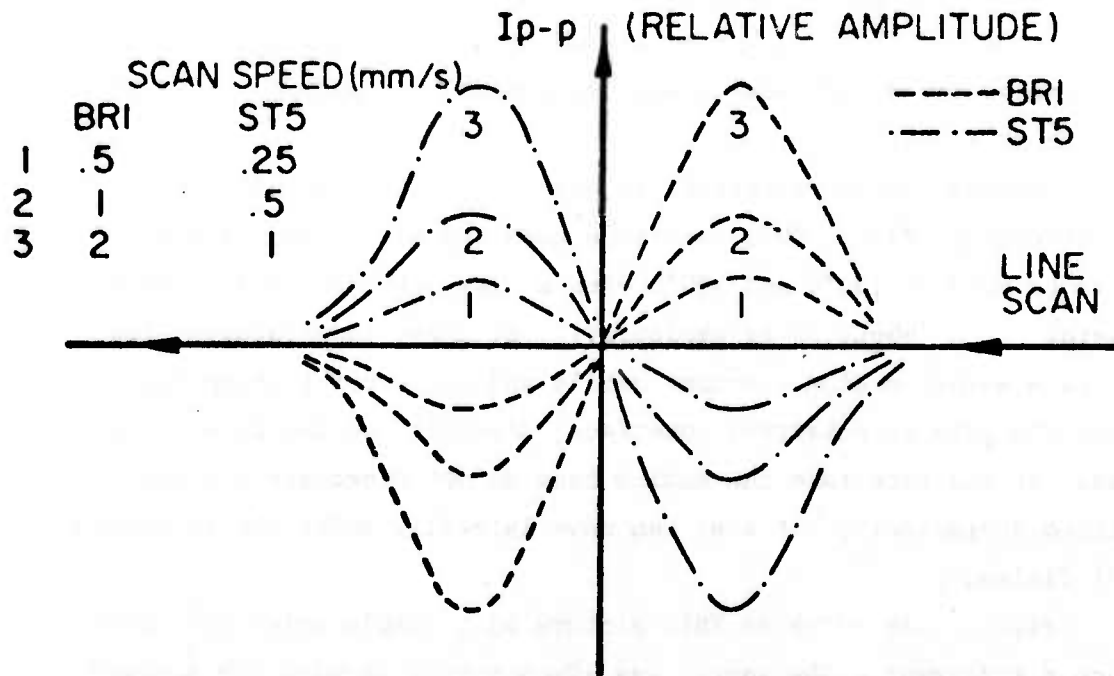


Fig. 6.3. Dependence of stacking-fault image contrast on scan speed.

ignores oxide charging. Unfortunately, relaxing these assumptions is considerably more difficult, but we are working on the problem. We are also working on the direct measurement of some of the parameters of this model, such as lifetime.

Ion-aggregation structure is seen only after extended bias-thermal stressing (BTS). This technique consists of heating an MOS capacitor to between 150°C and 300°C with a bias between +50 and -50 V, for several hours (about 10 hr typically). At these temperatures, ionic impurities - mainly sodium - become mobile and are swept through the oxide to either the gate or substrate interface, depending on the polarity of the bias. At the interface the sodium ions do not penetrate the metal or the silicon appreciably, but they can move laterally under the influence of local fields.

Figure 6.1b shows an EBIC picture of a sample which has undergone such a treatment. The sample was 1Ω-cm n-type Si with 300 Å steam grown oxide and 150 Å Au gate. The picture was taken at 5 kV and 1 nA. The average ion concentration was $4 \times 10^{13}/\text{cm}^2$. Two types of structure are immediately apparent. The first is an enhancement of the topological structure, which in this case may be due either to residual polishing damage or to residual oxide remaining from an oxide growth-stop-regrowth cycle. Since the structure was only faintly visible before ion drift, the enhanced contrast is probably due to sodium aggregation at the edges. The second type of structure consists of large cone-like features such as the one at bottom center of Fig. 6.1b. These appear to be due to sodium ions aggregating around a defect either in the metal film or in the substrate. These structures became visible at a beam energy just sufficient to penetrate the oxide, and the contrast increased with beam energy until the range of the electrons extended into the substrate, when it saturated. No dependence on scan speed was noted.

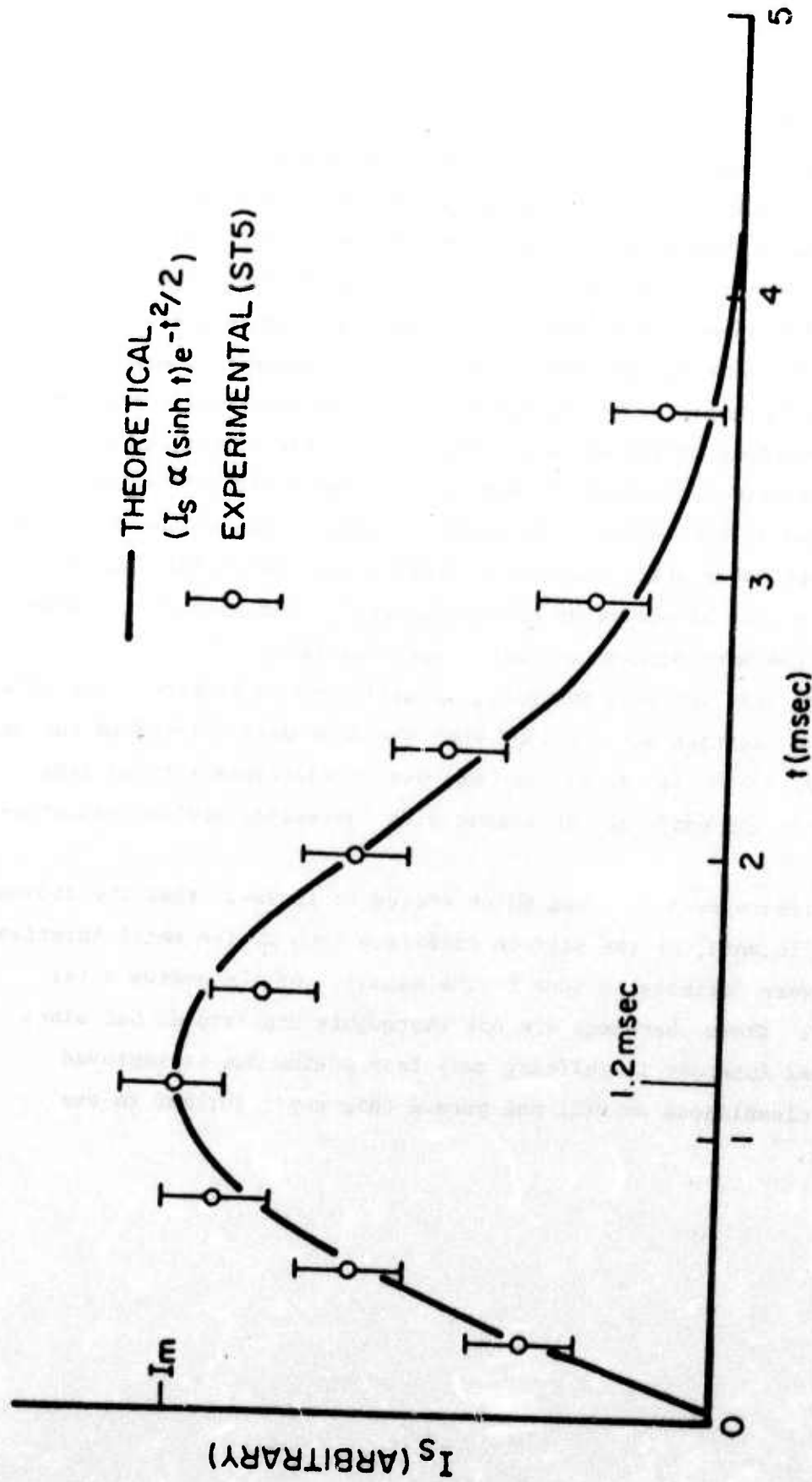


Fig. 6.4. Current/time dependence of SF structure observed in ST5. Theoretical curve obtained assuming beam and structure widths of 5000Å and scan speed of .25 mm/sec.

Line scans were also performed on these structures over a range of gate biases. Both the background and structure currents were ohmic, and the direction of the currents was consistent with the model of beam-induced conductivity. According to this model the collected current is due to pairs generated in the oxide which separate in the oxide field and move to the gate or substrate. In silicon dioxide we assume the current from the holes to be negligible. The electrons drift and are collected according to the shubweg model of Mott and Gurney, in which the electrons move a constant distance in a given field before being deeply trapped or recombined. The sheet of sodium ions at the interface forms a dipole layer which lowers the field across the oxide. This affects the number of electrons being collected. The more concentrated the sodium, the more pronounced this effect becomes.

For very low beam energies, insufficient to penetrate the gate, a reversal of contrast was observed when the ions were drifted to the gate. In this case, the collected current was due to electrons emitted from the metal into the oxide and increased with increasing sodium concentration.

Effects were observed which seemed to indicate that the sodium ions act differently at the silicon interface than at the metal interface. Also there were definite changes in the behavior of the sodium after irradiation. These phenomena are not thoroughly understood, but since technological interest is shifting away from sodium due to improved processing cleanliness we will not pursue this topic further in our future work.

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