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Hybrid Microelectronics Process and Quality Control Guide

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HONEYWELL INC.
St. Petersburg, Florida 33733

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Hybrid Microelectronics Process and Quality Control Guide.

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APPENDIX I TO PROCESSING STANDARDS FOR HYBRID MICROCIRCUITS
RESEARCH AND DEVELOPMENT TECHNICAL REPORT

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NOTICE TO USERS

This book has been written for the following purposes:

1. To identify critical processes and establish process controls and quality control data, which, if properly implemented may serve to replace some of the screens which are routinely performed after the hybrid assembly process.

2. To aid military procurement agencies to evaluate prospective hybrid vendors.

3. To aid hybrid vendors to evaluate their own processes.

4. To aid new vendors in establishing proper process controls and quality criteria.

5. To serve as a general information and reference source.

It should be noted that this book is a guide and not a specification. The information contained in it is recommended only, even though such words as 'mandatory' are used. In no case is it intended that the data listed be used as requirements to be imposed on a prospective vendor. However, since this guide is to be used by the military to evaluate prospective hybrid suppliers, it is important that it reflect the best information available. There may be processes which are "standard" at certain manufacturer's facilities which have not been mentioned, although an attempt at completeness has been made. Also, the information on the listed processes and materials may need to be improved and updated. For these reasons a tear-out comments sheet has been included which solicits user's inputs to ECOM and ensures a method whereby these comments can be evaluated and incorporated through periodic revisions.

GUIDE-REVISION REQUEST

To provide a means by which the Hybrid Microelectronics Process and Quality Control Guide can be continually updated and improved, it is desirable for users to recommend changes, additions, and deletions to ECOM. Each revision should be submitted on a separate sheet (or more). If an individual or an organization has several suggested revisions, it may be possible to meet with ECOM personnel to discuss them.

Guide-revision requests should be sent to:

Commander
U.S. Army Electronics Command
Attn: DRSEL-TL-IR (E.T. Hunter)
Ft. Monmouth, NJ 07703

Nature of Revision: Change Addition Deletion

Reference: Page No. ____________ Section No. _______ Paragraph _______

Comments:

1.1 Substrate Fabrication - Thick Film

Section: 1.1.1

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Substrate Fabrication	Gold (Fritted, Fritless & Mixed Bonded)	Thick Film Screen and Fire

Process Qualification Tests:
(1) Thickness - Optical Method, Stylus Method. (App. A., Test Nr. 1 or 2)
(2) Film Thickness - Four Point Probe. (App. A, Test Nr. 5)
(3) Bondability - (Appendix A, Test Nr. 3)
(4) Adhesion - Oiler Method (Appendix A, Test Nr. 4)

Process Controls:
(A) Mandatory (At start of each run): (1) squeegee speed, (2) squeegee pressure, (3) squeegee hardness, (4) squeegee material and dimensions, (5) breakaway distance.
(B) Additional Controls Required (Periodic monitoring): (1) room temperature, (2) humidity, (3) room cleanliness, e.g., dust, particles, etc.

Screens: (a) Mandatory: (1) Visual inspection

(b) Optional: (1) Conductivity Test
(2) All point continuity test

Critical Parameters:	Potential Problems:
(1) Thickness (2) Conductivity (Ω/□) (3) Firing Profile	(1) Material/Paste lot variations. (2) Contamination (3) Substrate problems (4) Bondability
Critical Previous Processes:	**Critical Subsequent Processes:**
- Lot qualification of pastes and substrates.	(1) High temperature operation. (2) Handling (3) Bonding (Die & Interconnect)
Critical Tools:	**Inspection Criteria:**
(1) Screen (2) Printer (3) Furnace (4) Alignment fixture. (5) Photolithographic equipment.	MIL-STD-883A Method 2017 ECOM Report #73-0326-F Sec. 5.7.

Notes/References:
(1) ECOM Report 73-0326-F and 75-1331-1 (2) Honeywell Survey (3) Honeywell Information (4) M. Fogiel, MODERN MICROELECTRONICS, (Research and Education Association, N.Y., 1972).

Section: 1.1.2

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Substrate Fabrication	Platinum - Gold	Thick Film Screen and Fire

Process Qualification Tests:
(1) Thickness - Optical Method, Stylus Method. (App. A. Test Nr. 1 or 2)
(2) Film Thickness - Four Point Probe. (Appendix A, Test Nr. 5)
(3) Solderability/Wettability - (Appendix A, Test Nr. 6)

Process Controls:
(A) Mandatory (At start of each run): (1) squeegee speed, (2) squeegee pressure, (3) squeegee hardness, (4) squeegee material and dimensions, (5) breakaway distance.
(B) Additional Controls Required (Periodic monitoring): (1) room temperature, (2) humidity, (3) room cleanliness, e.g., dust, particles, etc.

Screens: (a) Mandatory: (1) Visual inspection.

(b) Optional: (1) Conductivity test
(2) All point continuity test

Critical Parameters:	Potential Problems:
(1) Thickness (2) Conductivity (Ω/□) (3) Firing Profile	(1) Material/paste lot variations. (2) Contamination (3) Solderability (4) Substrate problems
Critical Previous Processes:	**Critical Subsequent Processes:**
- Lot qualification of pastes and substrates	(1) High temperature operation. (2) Handling (3) Soldering
Critical Tools:	**Inspection Criteria:**
(1) Screen (2) Printer (3) Furnace (4) Alignment fixture (5) Photolithographic equipment	MIL-STD-883A, Method 2017 ECOM Report, Sec. 5.7.

Notes/References:
(1) ECOM Report 73-0326-F and 75-1331-1. (2) Honeywell Survey (3) Honeywell Information (4) M. Fogiel, MODERN MICROELECTRONICS, (Research and Education Association, N.Y., 1972)

Section: 1.1.3

PROCESS: Substrate Fabrication	MATERIAL(S): Solder Pastes	METHOD/MACHINE: Thick Film Screen and Reflow

Process Qualification Tests:
(1) Thickness - Optical Method (Appendix A, Test Nr. 1)
(2) Solderability/Wettability (Appendix A, Test Nr. 6)

Process Controls:
(A) Mandatory (At start of each run): (1) squeegee speed, (2) squeegee pressure, (3) squeegee hardness, (4) squeegee material and dimensions, (5) breakaway distance.
(B) Additional Controls Required (Periodic monitoring): (1) room temperature, (2) humidity, (3) room cleanliness, e.g., dust, particles, etc.

Screens: (a) Mandatory: (1) Visual inspection after printing and reflow.

(b) Optional:

Critical Parameters:
(1) Thickness
(2) Control of atmosphere when drying hard solders.

Potential Problems:
(1) Material/paste lot variations.
(2) Contamination - flux.

Critical Previous Processes:
Lot qualification of pastes and previous printing

Critical Subsequent Processes:
(1) High temperature operation.
(2) Handling.

Critical Tools:
(1) Screen
(2) Printer
(3) Oven
(4) Alignment fixture
(5) Photolithographic equipment

Inspection Criteria:
MIL-STD-883A, Method 2017.

Notes/References:
(1) ECOM Report 73-0326-F and 75-1331-1. (2) Honeywell Survey (3) Honeywell Information (4) M. Fogiel, MODERN MICROELECTRONICS, (Research and Education Association, N. Y., 1972.

NOTE: More applicable to soft solders.

Section: 1.1.4

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Substrate Fabrication	Resistor Pastes	Thick Film Screen and Fire

Process Qualification Tests:
(1) Thickness - Optical Method/Stylus Method (App. A, Test Nr. 1 or 2)
(2) Resistance measurement - digital ohmmeter.

Process Controls:
(A) Mandatory (At start of each run): (1) squeegee speed, (2) squeegee pressure, (3) squeegee hardness, (4) squeegee material and dimensions, (5) breakaway distance.
(B) Additional Controls Required (Periodic monitoring): (1) room temperature, (2) humidity, (3) room cleanliness, e.g., dust, particles, etc.

Screens: (a) Mandatory: Visual inspection.

(b) Optional: Resistance measurement.

Critical Parameters:	Potential Problems:
(1) Thickness (2) Sheet resitivity (Ω/□) (3) Firing profile	(1) Material/paste lot variations. (2) Contamination (3) Substrate problems

Critical Previous Processes:	Critical Subsequent Processes:
Lot qualification of pastes and substrates.	(1) High temperature operation (2) Handling

Critical Tools:	Inspection Criteria:
(1) Screen (2) Printer (3) Furnace (4) Alignment fixture (5) Photolithographic equipment.	MIL-STD-883A, Method 2017. ECOM Report, Sec. 5.7.

Notes/References:
(1) ECOM Report 73-0326-F and 75-1331-1. (2) Honeywell Survey (3) Honeywell Information (4) M. Fogiel, MODERN MICROELECTRONICS, (Research and Education Association, N.Y., 1972).

Section: 1.1.5

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Substrate Fabrication	Dielectrics for Multilevel* Systems	Thick Film Screen and Fire

Process Qualification Tests:
(1) Dielectric Qualification Test (Appendix A, Test Nr. 12)

Process Controls:
(A) Mandatory (At start of each run): (1) squeegee speed, (2) squeegee pressure, (3) squeegee hardness, (4) squeegee material and dimensions, (5) breakaway distance.
(B) Additional Controls Required (Periodic monitoring): (1) room temperature, (2) humidity, (3) room cleanliness, e.g., dust, particles, etc.
(C) Visual inspection after printing, drying, firing.

Screens: (a) Mandatory: Visual check - each layer.

(b) Optional: All point continuity test

Critical Parameters:	Potential Problems:
(1) Thickness (2) Conductivity/resistivity. (3) Firing profile	(1) Material/paste lot variations (2) Contamination (3) Substrate problems (4) Pinholes - causing multilayer shorts.

Critical Previous Processes:	Critical Subsequent Processes:
Lot qualification of pastes and substances.	(1) High temperature operation (2) Handling (3) Bonding (4) Soldering

Critical Tools:	Inspection Criteria:
(1) Screen (2) Printer (3) Furnace (4) Alignment fixture (5) Photolithographic equipment	MIL-STD-883A, Method 2017 ECOM Report #73-0326-F, Sec. 5.7.

Notes/References:
(1) ECOM Report 73-0326-F and 75-1331-1. (2) Honeywell Survey (3) Honeywell Information (4) M. Fogiel, MODERN MICROELECTRONICS, (Research and Education Association, N.Y., 1972).

NOTE: *Commonly referred to as Multilayer.

1.2 Substrate Metallization - Thin Film

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Substrate Metallization	Nichrome-Nickel-Gold*	Thin Film Deposition and Subtractive Etch

Process Qualification Tests:
(1) Film Thickness - Four Point Probe or Stylus Method. (Appendix A, Test Nr. 5 or 2).
(2) Bondability Test (Appendix A, Test Nr. 3)

Process Controls:
(1) Monitor deposition time.
(2) Monitor resistance of Nichrome layer and Nickel layer.
(3) Quartz crystal monitor for Gold deposition.

Screens: (a) Mandatory:
(1) Visual inspection for cracks, voids, pinholes, discoloration.
(2) Four point probe each substrate for thickness.

(b) Optional:
(1) Adhesive tape test.

Critical Parameters:
(1) Film thickness.
(2) Sheet resistance (Ω/□)
(3) Film uniformity-system geometry.
(4) Deposition rate.
(5) Substrate temperature.

Potential Problems:
(1) Diffusion of Ni through Gold.
(2) Etching defects (a) Undercutting (b) Spotting (etch splash) (c) Contamination (photoresist, chemical residue.

Critical Previous Processes:
(1) Cleaning of substrates.
(2) Raw materials qualification; substrates, charge/target, sputtering gas.

Critical Subsequent Processes:
(1) High temperature application.
(2) Handling

Critical Tools:
(1) Deposition equipment
(2) Photolithographic equipment

Inspection Criteria:
MIL-STD-883A, Method 2017 Para. 3.1.3.2.

Notes/References:
(1) Honeywell Survey; (2) D.M. Mattox, Thin Solid Films, 18,173 (1973); (3) L.I. Maissel & R. Glang, Handbook of Thin Film Technology, McGraw-Hill Book Co., N.Y. 1970); (4) M. Fogiel, Modern Microelectronics (Research and Education Association, N.Y., 1972).

* Annealing recommended to relieve stress.

Section: 1.2.2

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Substrate Metallization	Chromium-Gold*	Thin Film Deposition and Subtractive Etch

Process Qualification Tests:
(1) Film Thickness - Four Point Probe or Stylus Method. (Appendix A, Test Nr. 5 or 2)
(2) Bondability Test (Appendix A, Test Nr. 3)

Process Controls:
(1) Monitor deposition time.
(2) Monitor resistance of Cr layer.
(3) Quartz crystal monitor for Gold.

Screens: (a) Mandatory: (1) Visual inspection for cracks, voids, pinholes, discoloration.
(2) Four point probe each substrate for thickness.

(b) Optional: (1) Adhesive tape test.

Critical Parameters:
(1) Film thickness
(2) Sheet resistance ($\Omega/\square$)
(3) Film uniformity-system geometry
(4) Deposition rate.
(5) Substrate temperature.

Potential Problems:
(1) Diffusion of Ni through Gold.
(2) Etching defects: (a) Undercutting (b) Spotting (etch splash) (c) Contamination (photoresist, chemical residue).

Critical Previous Processes:
(1) Cleaning of substrates.
(2) Raw materials qualification; substrates, charge/target, sputtering gas.

Critical Subsequent Processes:
(1) High temperature application.
(2) Handling.

Critical Tools:
(1) Deposition equipment
(2) Photolithographic equipment.

Inspection Criteria:
MIL-STD-883A, Method 2017
Para. 3.1.3.2

Notes/References:
(1) Honeywell Survey; (2) D.M. Mattox, Thin Solid Films, 18,173 (1973); (3) L.I. Maissel & R. Glang, Handbook of Thin Film Technology, (McGraw-Hill Book Co., N.Y. 1970); (4) M. Fogiel, Modern Microelectronics (Research and Education Association, N.Y.,1972).

* Recommended for conductor boards only.

Section: 1.2.3

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Substrate Metallization	Tantalum Nitride* Titanium-Palladium/Platinum-Gold	Thin Film Deposition and Subtractive Etch

Process Qualification Tests:

(1) Film Thickness - Four Point Probe or Stylus Method. (Appendix A, Test Nr. 5 or 2)
(2) Bondability Test (Appendix A, Test Nr. 3)

Process Controls:

(1) Monitor resistance of Tantalum Nitride.
(2) Monitor deposition time.
(3) Monitor flow of reactive gas.

Screens: (a) Mandatory: (1) Visual inspection for cracks, voids, pinholes, discoloration.
(2) Four point probe each substrate for thickness.

(b) Optional: (1) Adhesive tape test.

Critical Parameters:	Potential Problems:
(1) Thickness of film. (2) Sheet resistance Ω/□ (3) Reactive gas pressure (4) Deposition rate (5) Substrate temperature (6) Film uniformity-system geometry.	(1) Reactive sputtering requires rigid process controls. (2) Adsorbed gases in Titanium. (3) Etching defects.
Critical Previous Processes:	**Critical Subsequent Processes:**
(1) Cleaning of substrates/system (2) Raw materials qualification; substrates, targets, sputtering and reactive gases.	(1) High temperature application (2) Handling
Critical Tools:	**Inspection Criteria:**
(1) Deposition equipment (2) Photolithographic equipment	MIL-STD-883A, Method 2017 Para. 3.1.3.2.

Notes/References:

(1) Honeywell Survey; (2) D.M. Mattox, Thin Solid Films, 18,173 (1973); (3) L.I. Maissel & R. Glang, Handbook of Thin Film Technology, (McGraw-Hill Book Co. N.Y. 1970). (4) M. Fogiel, Modern Microelectronics (Research and Education Association, N.Y. 1972)

* Annealing recommended to relieve stress,

Section: 1.2.4

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Substrate Metallization	Gold*	Through-Mask Thin Film Deposition

Process Qualification Tests:
(1) Adhesive Tape Test (nondestructive).
(2) Film Thickness - Four Point Probe or Stylus Method. (Appendix A, Test Nr. 5 or 2)
(3) Bondability Test (Appendix A, Test Nr. 3)

Process Controls:
(1) Monitor deposition time.
(2) Quartz crystal monitor for thickness control.

Screens: (a) Mandatory: (1) Visual inspection for cracks, voids, pinholes, discoloration.
(2) Four point probe each substrate for thickness.
(b) Optional: (1) Adhesive tape test.

Critical Parameters:
(1) Thickness of film
(2) Surface smoothness.
(3) Deposition Rate.
(4) Substrate Temperature.
(5) Film Uniformity-System geometry.

Potential Problems:
(1) Masks are fragile.
(2) Resolution limited to 2-5 mils.
(3) Adhesion of Au to substrate.

Critical Previous Processes:
(1) Cleaning of substrates/system.
(2) Raw materials qualification; substrates, charge/target.
(3) Cleaning of masks.

Critical Subsequent Processes:
(1) Handling

Critical Tools:
(1) Deposition equipment.
(2) Mask fabrication equipment.

Inspection Criteria:
MIL-STD 883A
Method 2017
Para. 3.1.3.2.

Notes/References: (1) Honeywell Survey; (2) D. M. Mattox, Thin Solid Films, 18, 173 (1973); (3) L. I. Maissel & R. Glang, Handbook of Thin Film Technology, (McGraw-Hill Book Co., N.Y. 1970); (4) M. Fogiel, Modern Microelectronics (Research and Education Association, N.Y., 1972).

* Annealing recommended to relieve stress.

Section: 1.2.5

PROCESS: Substrate Metallization	MATERIAL(S): Other Metal Systems	METHOD/MACHINE: Thin Film Deposition and Subtractive Etch

Process Qualification Tests:

(1) Film Thickness - Four Point Strobe or Stylus Method. (Appendix A, Test Nr. 5 or 2)

(2) Bondability Test (Appendix A, Test Nr. 3)

Process Controls:

(1) Monitor deposition time.
(2) Monitor resistance of adhesion/resistor layer
(3) Monitor resistance of barrier layer
(4) Monitor thickness of conductor layer with quartz crystal.

Screens: (a) Mandatory: (1) Visual inspection for cracks, voids, pinholes, discoloration.
(2) Four point probe each substrate for thickness.

(b) Optional: (1) Adhesion test.

Critical Parameters:	Potential Problems:
(1) Film thickness (2) Sheet resistance Ω/□	(1) Diffusion of underlying layers through conductor layer (2) Etching defects: a) undercutting b) Spotting (etch splash) c) contamination
Critical Previous Processes: (1) Cleaning of substrates (2) Raw materials qualification: substrates, charge/target, sputtering gas.	**Critical Subsequent Processes:** (1) High temperature application (2) Handling
Critical Tools: (1) Deposition equipment (2) Photolithographic equipment	**Inspection Criteria:** MIL-STD-883A Method 2017 Para. 3.1.3.2

Notes/References: (1) Honeywell Survey; (2) D. M. Mattox, Thin Solid Films, 18, 173 (1973); (3) L. I. Maissel and Glang, Handbook of Thin Film Technology, (McGraw-Hill Book Co., N.Y. 1970); (4) M. Fogiel, Modern Microelectronics (Research & Education Association, N.Y., 1972)

1.3 Chip/Component Attach

Section: 1.3.1

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Chip Attach	Gold-Silicon w/o Preform	Eutectic

Process Qualification Tests:
(1) Chip Adherence Strength Test. (Appendix A, Test Nr. 7)
(2) Destructive Shear Test. (Appendix A, Test Nr. 8)
(3) Visual Inspection
(4) Infrared Thermal Test. (Appendix A, Test Nr. 9)

Process Controls:
(1) Visually inspect sample immediately after bonding.
(2) Shear test, nondestructive, five samples once per shift.
(3) Monitor stage temperature and dwell time.

Screens: (a) Mandatory:
(1) Visual inspection
(2) Centrifuge

(b) Optional:
(1) X-Ray
(2) Electrical Test (V_{SAT} transistors)
(3) Temperature cycle
(4) Nondestructive shear test

Critical Parameters:	Potential Problems:
(1) Stage Temperature (2) Dwell time (3) Collet pressure	(1) Temperature control (stage) (2) Voiding (3) Chip back metallization (must be alloyed) (4) Cleanliness of substrate surface.
Critical Previous Processes:	**Critical Subsequent Processes:**
(1) Surface cleaning (2) Metallization of substrate and chip	(1) Any involving high heat application. (2) Cleaning (solvent residue) (3) Rework (heat) (4) Sealing (heat)
Critical Tools:	**Inspection Criteria:**
(1) Collet (2) Temperature controller (3) Ambient gas	MIL-STD-883A, Method 2017 Para. 3.1.4

Notes/References:

Honeywell Survey

Section: 1.3.2

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Chip Attach	Gold-Silicon with Preform	Eutectic

Process Qualification Tests:

(1) Chip Adherence Strength Test. (Appendix A, Test Nr. 7)
(2) Destructive Shear Test. (Appendix A, Test Nr. 8)
(3) Visual Inspection.
(4) Infrared Thermal Test. (Appendix A, Test Nr. 9)

Process Controls:

(1) Visually inspect sample immediately after bonding.
(2) Shear test, nondestructive, five samples once per shift.
(3) Monitor stage temperature and dwell time.

Screens:

(a) Mandatory:
(1) Visual inspection
(2) Centrifuge

(b) Optional:
(1) X-Ray
(2) Electrical Test (V_{SAT} transistors)
(3) Temperature cycle
(4) Nondestructive shear test

Critical Parameters:

(1) Stage temperature
(2) Dwell time
(3) Collet pressure

Potential Problems:

(1) Temperature control (stage)
(2) Voiding
(3) Chip back metallization (must be alloyed)
(4) Cleanliness of substrate surface
(5) Preform composition

Critical Previous Processes:

(1) Surface Cleaning
(2) Metallization of substrate and chip.

Critical Subsequent Processes:

(1) Any involving high heat applications.
(2) Cleaning (solvent residue)
(3) Rework (heat)
(4) Sealing (heat)

Critical Tools:

(1) Collet
(2) Temperature controller
(3) Ambient gas

Inspection Criteria:

MIL-STD-883A, Method 2017
Para. 3.1.4

Notes/References:

(1) Solid State Technology, 18, 45 (1975)
(2) Honeywell Survey

Section: 1.3.3

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Chip Attach	Aluminum - Germanium	Eutectic/Manual

Process Qualification Tests:
(1) Chip Adherence Strength Test. (Appendix A, Test Nr. 7)
(2) Destructive Shear Test. (Appendix A, Test Nr. 8)
(3) Visual Inspection.
(4) Infrared Thermal Test. (Appendix A, Test Nr. 9)

Process Controls:
(1) Visually inspect sample immediately after bonding.
(2) Shear test, nondestructive, five samples once per shift.
(3) Monitor stage temperature and dwell time.

Screens: (a) Mandatory:
(1) Visual inspection
(2) Centrifuge

(b) Optional:
(1) X-Ray
(2) Electrical Test (V_{SAT} transistors)
(3) Temperature cycle
(4) Nondestructive shear test

Critical Parameters:
(1) Stage temperature
(2) Dwell time
(3) Collet pressure

Potential Problems:
(1) Temperature control (stage)
(2) Voiding
(3) Chip back metallization (must be alloyed)
(4) Cleanliness of substrate surface
(5) Preform composition

Critical Previous Processes:
(1) Surface cleaning
(2) Metallization of substrate and chip

Critical Subsequent Processes:
(1) Any involving high heat application
(2) Cleaning (solvent residue)
(3) Rework (heat)
(4) Sealing (heat)

Critical Tools:
(1) Collet
(2) Temperature controller
(3) Ambient gas

Inspection Criteria:
MIL-STD-883A, Method 2017
Para. 3.1.4

Notes/References:
(1) Honeywell Survey

Section: 1.3.4

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Chip Attach	Epoxy - Nonconductive	Manual

Process Qualification Tests:
(1) Chip Adherence Strength Test. (Appendix A, Test Nr. 7)
(2) Destructive Shear Test. (Appendix A, Test Nr. 8)
(3) Visual Inspection.

Process Controls:
(1) Visually inspect sample immediately after bonding.
(2) Shear test, nondestructive, five samples once per shift.
(3) Monitor amount of epoxy by visually inspecting samples for proper fillet.
(4) Monitor cure temperature and time.

Screens:
(a) Mandatory:
(1) Visual inspection
(2) Centrifuge

(b) Optional:
(1) Nondestructive shear test
(2) Temperature cycle

Critical Parameters:
(1) Epoxy quantity (thickness)
(2) Cure temperature
(3) Cure time

Potential Problems:
(1) Epoxy composition
(2) Epoxy run-out
(3) Epoxy aging (prior to application)
(4) Cleanliness
(5) Thermal degradation of epoxy

Critical Previous Processes:
(1) Cleanliness of substrate surface
(2) Gold metallization on chip back

Critical Subsequent Processes:
(1) Any application of high temperature
(2) Cleaning (solvent and residue)
(3) Rework (heat)
(4) Sealing (heat)

Critical Tools:

Inspection Criteria:
MIL-STD-883A, Method 2017
Para. 3.1.4

Notes/References:
(1) Honeywell Survey

Section: 1.3.5

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Chip Attach	Epoxy-Nonconductive	Machine Dispensed

Process Qualification Tests:
(1) Chip Adherence Strength Test. (Appendix A, Test Nr. 7)
(2) Destructive Shear Test. (Appendix A, Test Nr. 8)
(3) Visual Inspection.

Process Controls:
(1) Visually inspect sample immediately after bonding.
(2) Shear test, nondestructive, five samples once per shift.
(3) Monitor epoxy quantity dispensed.
(4) Monitor cure temperature and time.

Screens: (a) Mandatory: (1) Visual inspection
(2) Centrifuge

(b) Optional: (1) Nondestructive shear test
(2) Temperature cycle

Critical Parameters:	Potential Problems:
(1) Epoxy quantity (thickness) (2) Cure temperature (3) Cure time	(1) Epoxy composition (2) Epoxy run-out (3) Epoxy aging (prior to application) (4) Cleanliness (5) Thermal degradation of epoxy

Critical Previous Processes:	Critical Subsequent Processes:
(1) Cleanliness of substrate surface (2) Gold metallization on chip back	(1) Any application of high temperature (2) Cleaning (solvent and residue) (3) Rework (heat) (4) Sealing (heat)

Critical Tools:	Inspection Criteria:
(1) Epoxy dispenser	MIL-STD-883A, Method 2017 Para. 3.1.4

Notes/References:
Honeywell Survey

Section: 1.3.6

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Chip Attach	Epoxy - Nonconductive	Film Preform - Manual

Process Qualification Tests:

(1) Chip Adherence Strength Test. (Appendix A, Test Nr. 7)
(2) Destructive Shear Test. (Appendix A, Test Nr. 8)
(3) Visual Inspection.

Process Controls:

(1) Visually inspect sample immediately after bonding.
(2) Shear Test, nondestructive, five samples, once per shift
(3) Monitor cure temperature and time.

Screens:

(a) Mandatory:
(1) Visual inspection
(2) Centrifuge

(b) Optional:
(1) Nondestructive shear test
(2) Temperature cycle

Critical Parameters:

(1) Cure temperature
(2) Cure time

Potential Problems:

(1) Epoxy composition
(2) Epoxy run-out
(3) Epoxy aging (prior to application)
(4) Cleanliness
(5) Thermal degradation of epoxy

Critical Previous Processes:

(1) Cutting of preform to proper size
(2) Cleanliness of substrate surface

Critical Subsequent Processes:

(1) Any application of high temperature.
(2) Cleaning (solvent and residue)
(3) Rework (heat)
(4) Sealing (heat)

Critical Tools:

Inspection Criteria:

MIL-STD-883A, Method 2017
Para. 3.1.4

Notes/References:

Solid State Technology, 18, 45 (1975).
Honeywell Survey

Section: 1.3.7

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Chip Attach	Epoxy - Conductive	Manual

Process Qualification Tests:
(1) Chip Adherence Strength Test. (Appendix A, Test Nr. 7)
(2) Destructive Shear Test. (Appendix A, Test Nr. 8)
(3) Visual Inspection.
(4) Infrared Thermal Test. (Appendix A, Test Nr. 9)

Process Controls:
(1) Visually inspect sample immediately after bonding.
(2) Shear test, nondestructive, five samples, once per shift.
(3) Monitor amount of epoxy by visually inspecting samples for proper fillet.
(4) Monitor cure temperature and time.

Screens: (a) Mandatory: (1) Visual inspection
(2) Centrifuge

(b) Optional: (1) Nondestructive shear test
(2) Temperature cycle
(3) Electrical test (V_{SAT} transistors)

Critical Parameters:
(1) Epoxy quantity (thickness)
(2) Cure temperature
(3) Cure time

Potential Problems:
(1) Epoxy composition
(2) Epoxy run-out
(3) Epoxy aging (prior to application)
(4) Cleanliness
(5) Thermal degradation of epoxy

Critical Previous Processes:
(1) Cleanliness of substrate surface
(2) Gold metallization on chip back

Critical Subsequent Processes:
(1) Any application of high temperature
(2) Cleaning (solvent and residue)
(3) Rework (heat)
(4) Sealing (heat)

Critical Tools:

Inspection Criteria:
MIL-STD-883A, Method 2017
Para. 3.1.4

Notes/References:
Honeywell Survey

Section: 1.3.8

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Chip Attach	Epoxy - Conductive	Machine Dispensed

Process Qualification Tests:

(1) Chip Adherence Strength Test. (Appendix A, Test Nr. 7)
(2) Destructive Shear Test. (Appendix A, Test Nr. 8)
(3) Visual Inspection.
(4) Infrared Thermal Test. (Appendix A, Test Nr. 9)

Process Controls:

(1) Visually inspect sample immediately after bonding
(2) Shear test, nondestructive, five samples once per shift
(3) Monitor epoxy quantity dispensed
(4) Monitor cure temperature and time

Screens: (a) Mandatory:
(1) Visual inspection
(2) Centrifuge

(b) Optional:
(1) Nondestructive shear test
(2) Temperature cycle
(3) Electrical test (V_{SAT} transistors)

Critical Parameters:	Potential Problems:
(1) Epoxy quantity (thickness) (2) Cure temperature (3) Cure time	(1) Epoxy composition (2) Epoxy run-out (3) Epoxy aging (prior to application) (4) Cleanliness (5) Thermal degradation of epoxy
Critical Previous Processes:	**Critical Subsequent Processes:**
(1) Surface cleaning (2) Metallization of substrate and chip	(1) Any application of high temperature (2) Cleaning (solvent and residue) (3) Rework (heat) (4) Sealing (heat)
Critical Tools:	**Inspection Criteria:**
(1) Epoxy dispenser (2) Collet	MIL-STD-883A, Method 2017 Para. 3.1.4

Notes/References:

Honeywell Survey

Section: 1.3.9

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Chip Attach	Epoxy - Conductive - Screened	Manual

Process Qualification Tests:

(1) Chip Adherence Strength Test. (Appendix A, Test Nr. 7)
(2) Destructive Shear Test. (Appendix A, Test Nr. 8)
(3) Visual Inspection.
(4) Infrared Thermal Test. (Appendix A, Test Nr. 9)

Process Controls:

(1) Monitor emulsion thickness, screen mesh and screen distance from substrate while screening.
(2) Bond 25 samples (chips) per lot upon screening and perform destructive shear test.
(3) Visually inspect sample immediately after bonding.
(4) Shear test, nondestructive, five samples once per shift.
(5) Monitor cure temperature and time.

Screens: (a) Mandatory:

(1) Visual inspection
(2) Centrifuge

(b) Optional:

(1) Nondestructive shear test
(2) Temperature cycle
(3) Electrical Test (V_{SAT} transistors)

Critical Parameters:

(1) Epoxy quantity (thickness)
(2) Cure temperature
(3) Cure time

Potential Problems:

(1) Epoxy composition
(2) Epoxy run-out
(3) Epoxy aging (prior to application)
(4) Cleanliness
(5) Thermal degradation of epoxy

Critical Previous Processes:

(1) Epoxy screening
(2) Cleanliness of substrate surface
(3) Gold metallization on chip back

Critical Subsequent Processes:

(1) Any application of high temperature
(2) Cleaning (solvent and residue)
(3) Rework (heat)
(4) Sealing (heat)
(5) Wire bonding (stage heat)

Critical Tools:

(1) Screen printer
(2) Collet

Inspection Criteria:

MIL-STD-883A, Method 2017
Para. 3.1.4

Notes/References:

Honeywell Survey

Section: 1.3.10

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Solder Attach Capacitor Chip	All Sn-Pb-Ag Solders	Manual Tin and Reflow

Process Qualification Tests:

(1) Destructive Shear Test. (Appendix A, Test Nr. 8)
(2) Centrifuge
(3) Visual Inspection

Process Controls:

During capacitor tinning, visually inspect to be sure:
(1) Chip is shiny and bright.
(2) Chip is 100 percent tinned on both edges.
(3) No solder is on the body of the chip.
During capacitor mounting visually inspect to be sure:
(1) A good fillet is formed.
(2) A minimum of 75 percent of capacitor ends are solder covered.

Screens: (a) Mandatory:
(1) Visual Inspection
(2) Centrifuge

(b) Optional:
(1) Nondestructive Shear Test
(2) Temperature Cycle
(3) Electrical Test

Critical Parameters:	Potential Problems:
(1) Solder pot and hot plate temperature (2) Time needed for chip mounting (must be minimal)	(1) Solder leaching of conductor pads if left on hotplate too long (2) Improper tinning

Critical Previous Processes:	Critical Subsequent Processes:
(1) Solder screening onto conductor pads (2) Cleaning	(1) Any application of high temperature (2) Cleaning - Solvent Residue (3) Rework (heat) (4) Sealing (heat)

Critical Tools:	Inspection Criteria:
(1) Hotplate (2) Solder Pot	MIL-STD-883A

Notes/References:

Honeywell Survey

1.4 Wire Bonding/Electrical Connections

Section: 1.4.1

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Wire Bond	Aluminum to Gold	Ultrasonic

Process Qualification Tests:
(1) Bondability (Appendix A, Test No. 3).
(2) Visual Inspection.

Process Controls:
(1) Minimum of five bond loops pulled to destruction once per shift.
(2) Monitor energy, time, force.
(3) Visually inspect sample immediately after bonding.

Screens: (a) Mandatory: (1) Visual inspection.

(b) Optional: (1) Nondestruct pull test
(2) Centrifuge.
(3) Temperature cycle.
(4) Mechanical shock.

Critical Parameters:
(1) Pull strength.
(2) Bond resistance (after heat age)
(3) Wire quality/consistency
(4) Substrate/chip cleanliness

Potential Problems: (1) Nonsticking during bonding. (2) Increased resistance after heat age (Burn-In). Will occur if substrate temperature reaches 160°C or higher.
(3) Control of ultrasonic coupling.

Critical Previous Processes:
(1) Gold deposition or screen.
(2) Cleaning of all surfaces.
(3) Chip attach (flatness).

Critical Subsequent Processes:
(1) Burn-in or other high temperature processing.
(2) Handling.
(3) Cleaning.

Critical Tools:
(1) Bonding Machine.
(2) Bonding tool.
(3) Pull tester.
(4) Chuck or holding fixture.

Inspection Criteria:
MIL-STD-883A Method 2017, Para. 3.1.6.

Notes/References: (1) "Changes in strength and resistance after burn-in of aluminum wire bonds to thick and thin film gold." William R. Rodrigues de Miranda and R. G. Oswald - ISHM 1974. (2) "Changes in strength and resistance of aluminum to gold ultrasonic bonds after temperature, electrical and environmental stress." R. G. Oswald, W. R. Rodrigues de Miranda, C. W. White - ISHM 1975.

Section: 1.4.2

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Wire Bond	Aluminum to Aluminum	Ultrasonic

Process Qualification Tests:
(1) Bondability (Appendix A, Test No. 3).
(2) Visual Inspection.

Process Controls:
(1) Minimum of five bond loops pulled to destruction once per shift.
(2) Monitor energy, time, force.
(3) Visually inspect sample immediately after bonding.

Screens: (a) Mandatory: (1) Visual inspection.

(b) Optional: (1) Nondestruct pull test.
(2) Centrifuge.
(3) Temperature cycle.
(4) Mechanical chock.

Critical Parameters:
(1) Pull strength.
(2) Wire quality/consistency.
(3) Substrate/chip cleanliness.

Potential Problems:
(1) Nonsticking during bonding.
(2) Control of ultrasonic coupling.

Critical Previous Processes:
(1) Aluminum deposition.
(2) Cleaning of all surfaces.

Critical Subsequent Processes:
(1) Handling.
(2) Cleaning (corrosive or residue depositing agents).

Critical Tools:
(1) Bonding machine.
(2) Bonding tool.
(3) Pull tester.
(4) Chuck or holding fixture.

Inspection Criteria:
MIL-STD-883A Method 2017, Para. 3.1.6.

Notes/References:
(1) Honeywell survey.

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Wire Bond	Gold to Gold	Thermocompression Ball-Wedge

Process Qualification Tests:
(1) Bondability (Appendix A, Test No. 3).
(2) Visual Inspection.

Process Controls:
(1) Minimum of five bond loops pulled to destruction once per shift. Determine $\overline{X}$ and R (or S) and record.
(2) Monitor stage and capillary temperature, force and time if applicable.
(3) Visually inspect sample immediately after bonding.

Screens: (a) Mandatory: (1) Visual inspection.
(2) Centrifuge.

(b) Optional: (1) Nondestruct pull test.
(2) Temperature cycle.
(3) Mechanical shock.

Critical Parameters:
(1) Pull strength.
(2) Wire quality/consistency.
(3) Substrate/chip cleanliness.

Potential Problems:
(1) Bond lift during bonding.
(2) Capillary plugging.
(3) Lifting/breaking of single wedge bond.

Critical Previous Processes:
(1) Gold deposition/screening.
(2) Cleaning of all surfaces.

Critical Subsequent Processes:
(1) Handling.
(2) Cleaning (corrosive or residue depositing agents).

Critical Tools:
(1) Bonding machine.
(2) Capillary.
(3) Pull tester.

Inspection Criteria:
MIL-STD-883A Method 2017, Para. 3.1.6.

Notes/References:
(1) On thick film gold the wedge (2nd) bond must be covered by another (safety bond), or two wedge bonds in succession must be made.

Section: 1.4.4

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Wire Bond	Gold to Aluminum	Thermocompression Ball-Wedge

Process Qualification Tests:
(1) Bondability (Appendix A, Test No. 3).
(2) Visual Inspection.

Process Controls:
(1) Minimum of five bond loops pulled to destruction once per shift. Determine $\overline{X}$ and R (or S) and record.
(2) Monitor stage and capillary temperature, force and time if applicable.
(3) Visually inspect sample immediately after bonding.

Screens: (a) Mandatory:
(1) Visual inspection.
(2) Centrifuge.

(b) Optional:
(1) Nondestruct pull test.
(2) Temperature cycle.
(3) Mechanical shock.

Critical Parameters:	Potential Problems:
(1) Pull strength. (2) Bond resistance (after heat age). (3) Wire quality/consistency. (4) Substrate/chip cleanliness.	(1) Bond lift during bonding. (2) Capillary plugging. (3) Lifting/breaking of single wedge bond. (4) Formation of intermetallics if over-bonded.
Critical Previous Processes:	**Critical Subsequent Processes:**
(1) Aluminum deposition. (2) Cleaning of all surfaces.	(1) Burn-in or other high temperature. (2) Handling. (3) Cleaning.
Critical Tools:	**Inspection Criteria:**
(1) Bonding machine. (2) Capillary. (3) Pull tester.	MIL-STD-883A Method 2017, Para. 3.1.6.

Notes/References:
(1) On thick film gold the wedge (2nd) bond must be covered by another (safety bond), or two wedge bonds in succession must be made.

Section: 1.4.5

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Wire Bond	Gold to Gold	Thermocompression/ Ultrasonic

Process Qualification Tests:
(1) Bondability (Appendix A, Test No. 3).
(2) Visual Inspection.

Process Controls:
(1) Minimum of five bond loops pulled to destruction once per shift. Determine $\overline{X}$ and R (or S) and record.
(2) Monitor stage temperature, and tip energy, force and time.
(3) Visually inspect sample immediately after bonding.

Screens: (a) Mandatory:
(1) Visual inspection.
(2) Centrifuge.

(b) Optional:
(1) Nondestruct pull test.
(2) Temperature cycle.
(3) Mechanical shock.

Critical Parameters:
(1) Pull strength.
(2) Wire quality/consistency.
(3) Substrate/chip cleanliness.

Potential Problems:
(1) Bond lift during bonding.
(2) Capillary plugging.
(3) Lifting/breaking of single wedge bond.

Critical Previous Processes:
(1) Gold deposition/screening.
(2) Cleaning of all surfaces.
(a) Epoxy thickness.
(b) Chip flatness.

Critical Subsequent Processes:
(1) Handling.
(2) Cleaning (corrosive or residue depositing agents).

Critical Tools:
(1) Bonding machine.
(2) Bonding tool.
(3) Pull tester.
(4) Chuck or holding fixture.

Inspection Criteria:
MIL-STD-883A Method 2017, Para 3.1.6.

Notes/References:
(1) Honeywell survey.

Section: 1.4.6

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Wire Bond	Gold to Aluminum	Thermocompression/ Ultrasonic

Process Qualification Tests:
(1) Bondability (Appendix A, Test No. 3).
(2) Visual Inspection.

Process Controls:
(1) Minimum of five bond loops pulled to destruction once per shift. Determine $\overline{X}$ and R (or S) and record.
(2) Monitor stage temperature, and tip energy force and time.
(3) Visually inspect sample immediately after bonding.

Screens: (a) Mandatory:
(1) Visual inspection.
(2) Centrifuge.

(b) Optional:
(1) Nondestruct pull test.
(2) Temperature cycle.
(3) Mechanical shock.

Critical Parameters:
(1) Pull strength.
(2) Bond resistance (after heat age).
(3) Wire quality/consistency.
(4) Substrate/chip cleanliness.

Potential Problems:
(1) Bond lift during bonding.
(2) Capillary plugging.
(3) Lifting/breaking of single wedge bond.
(4) Formation of intermetallics if overbonded.

Critical Previous Processes:
(1) Aluminum deposition.
(2) Cleaning of all surfaces.
(3) Chip attach.
 (a) Epoxy thickness.
 (4) Chip flatness.

Critical Subsequent Processes:
(1) Burn-in or other high temperature processing.
(2) Handling.
(3) Cleaning.

Critical Tools:
(1) Bonding machine.
(2) Bonding tool.
(3) Pull tester.
(4) Chuck or holding fixture.

Inspection Criteria:
MIL-STD-883A Method 2017, Para. 3.1.6.

Notes/References:
(1) Honeywell survey.

Section: 1.4.7

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Electrical Connection Bonding	Gold - Beam Lead	TC Wobble Bonder

Process Qualification Tests:
(1) Visual Inspection.
(2) Bondability Test (Appendix A, Test No. 3).
(3) Temperature Cycling.
(4) Thermal Shock Test.

Process Controls:
Before each tool change or once per shift, bond 6 devices:
(A) Visually inspect at normal incidence - check deformation.
(B) Visually inspect at 10 degrees incidence - check bug-up*.
(C) Perform pull test - destructive.

Screens: (a) Mandatory: Visual inspection.

(b) Optional: Centrifuge.

Critical Parameters:	Potential Problems:
(1) Substrate temperature. (2) Interface temperature. (3) Duration for 1 Wobble. (4) Bonding forces.	(1) Breaking Si_3N_4 "Shelf" which surrounds chip. (2) Shearing of beam leads

Critical Previous Processes:	Critical Subsequent Processes:
(1) Film deposition. (2) Cleaning processes.	(1) Handling. (2) Cleaning (corrosive or residue depositing agents).

Critical Tools:	Inspection Criteria:
(1) TC wobble bonder. (2) Bonding tool.	MIL-STD-883A Method 2011, Condition F

Notes/References:
C. J. Dawes, Solid State Technology, 19, 23 (1976).
*Amount chip is raised above substrate by bonding action.

Section: 1.4.8

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Electrical Connection	Gold - Beam Lead	TC/US Wobble Bonder

Process Qualification Tests:
(1) Visual Inspection.
(2) Bondability Test (Appendix A, Test No. 3).
(3) Temperature Cycling.
(4) Thermal Shock Test.

Process Controls:
Before each tool change, or once per shift, bond 6 devices.
(A) Visually inspect at normal incidence check deformation.
(B) Visually inspect at 10 degrees incidence - check bug-up*.
(C) Perform pull test - destructive.

Screens: (a) Mandatory: Visual inspection.

(b) Optional: Centrifuge.

Critical Parameters:
(1) Substrate temperature.
(2) Interface temperature.
(3) Duration for 1 wobble.
(4) Bonding force.
(5) US energy.

Potential Problems:
(1) Breaking Si_3N_4 "Shelf" which surrounds chip.
(2) Shearing of beam leads.

Critical Previous Processes:
(1) Film deposition.
(2) Cleaning processes.

Critical Subsequent Processes:
(1) Handling.
(2) Cleaning (corrosive or residue depositing agents).

Critical Tools:
(1) TC/US wobble bonder.
(2) Bonding tool.

Inspection Criteria:
MIL-STD-883A Method 2011, Condition F.

Notes/References:
C. J. Dawes, Solid State Technology, 19, 23 (1976).
*Amount chip is raised above substrate by bonding action.

1.5 Substrate Attach

Section: 1.5.1

PROCESS:	MATERIAL(S):	METHOD/MACHINE
Substrate Attach	Epoxy	Manual

Process Qualification Tests:
(1) Full cure per vendor's specifications.
(2) Visual inspection after cure.
(3) Centrifuge.
(4) X-ray.
(5) Destructive Shear Test (Appendix A, Test No. 8).

Process Controls:
(1) Visually inspect a sample immediately after attach.
(2) Monitor epoxy quantity.
(3) Monitor cure temperature and time.
(4) Perform Destructive Shear Test, once per shift.

Screens: (a) Mandatory:
(1) Visual inspection.
(2) Centrifuge.

(b) Optional:
(1) Push-off test, nondestructive.
(2) Thermal shock.
(3) Temperature cycle.

Critical Parameters:
(1) Cleanliness of substrate and package.
(2) Oven profile.
(3) Epoxy quantity.

Potential Problems:
(1) Thermal mismatch.
(2) Substrate (or package) warping.
(3) Epoxy aging (prior to application).
(4) H_2O absorption of epoxy prior to cure.
(5) Outgassing. (6) Corrosivity.

Critical Previous Processes:
(1) Cleaning.
(2) Storage of epoxy.

Critical Subsequent Processes:
(1) High temperature applications.

Critical Tools:
(1) Curing oven.
(2) Tooling to hold substrate in place during cure.

Inspection Criteria:
MIL-STD-883A Method 2017, Para. 3.5.1.2.

Notes/References:
(1) Honeywell survey.
(2) C. E. T. White and H. C. Sohl, Solid State Technology, 18, 45 (1975).

Section: 1.5.2

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Substrate Attach	Solder - Pb/Sn	Manual

Process Qualification Tests:
(1) Visual Inspection.
(2) Centrifuge.
(3) X-ray.
(4) Destructive Shear Test (Appendix A, Test No. 8).

Process Controls:
(1) Monitor stage temperature and dwell time.
(2) Visually inspect a sample immediately after attach.
(3) Perform Destructive Shear Test, once per shift.

Screens: (a) Mandatory:
(1) Visual inspection.
(2) Centrifuge.

(b) Optional:
(1) X-ray.
(2) Thermal shock.
(3) Push-off test, nondestructive.

Critical Parameters:
(1) Stage temperature.
(2) Cleanliness of substrate and package.
(3) Dwell time.

Potential Problems:
(1) Voiding.
(2) Thermal mismatch.
(3) Dewetting.

Critical Previous Processes:
(1) Cleaning.
(2) Package plating.
(2) Substrate back plating.

Critical Subsequent Processes:
(1) Cleaning (flux).
(2) High temperature application.

Critical Tools:
(1) Furnace/hot plate.
(2) Fixtures.

Inspection Criteria:
MIL-STD-883A Method 2017, Para. 3.1.5.1.

Notes/References:
(1) Honeywell survey.
(2) C. E. T. White and H. C. Sohl, Solid State Technology, 18, 45 (1975).

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Substrate Attach	Eutectic Gold - Germanium	Manual

Process Qualification Tests:
(1) Visually inspect samples.
(2) Centrifuge.
(3) X-ray.
(4) Destructive Shear Test (Appendix A, Test No. 8).

Process Controls:
(1) Visually inspect a sample immediately after attach.
(2) Monitor temperature and time.
(3) Perform Destructive Shear Test, once per shift.

Screens: (a) Mandatory:
(1) Visual inspection.
(2) Centrifuge.

(b) Optional:
(1) Push-off test, nondestructive.
(2) Thermal shock.
(3) Temperature cycle.

Critical Parameters:
(1) Cleanliness of substrate and package.
(2) Furnace/oven profile.
(3) Preform thickness.

Potential Problems:
(1) Thermal mismatch.
(2) Substrate, package warping.

Critical Previous Processes:
(1) Cleaning.
(2) Certification of Au-Ge eutectic.

Critical Subsequent Processes:
(1) High temperature application.

Critical Tools:
(1) Curing oven.
(2) Fixturing.

Inspection Criteria:
MIL-STD-883A Method 2017, Para. 3.5.1.2.

Notes/References:
C. E. T. White and H. C. Sohl, Solid State Technology, 18, 45 (1975)

1.6 Package Seal

Section: 1.6.1

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Package Seal	Solder/Braze Gold - Tin	Resistance Heat

Process Qualification Tests:
(1) Seal Qualification Test (Appendix A, Test No. 10).
(2) Visual Inspection.

Process Controls:
(1) Hermeticity test a minimum of five packages at the start of each shift.
(2) Visually inspect a sample of each lot.
(3) Monitor temperature of head.

Screens: (a) Mandatory:
(1) Hermeticity test.
(2) Visual inspection.

(b) Optional:
(1) Thermal shock (liquid-liquid).
(2) Temperature cycle.
(3) PIND (Particle Impact Noise Detection).
(4) X-ray.

Critical Parameters:
(1) Head temperature.
(2) Cleanliness.
(3) Atmosphere.

Potential Problems:
(1) Trapped particles
(2) Inadequate hermeticity.
(3) Trapped flux.

Critical Previous Processes:
(1) Cleaning.
(2) Package manufacture/qualification.

Critical Subsequent Processes:
(1) Lead forming.
(2) Cleaning (flux removal).
(3) Repair.

Critical Tools:
(1) Fixtures.
(2) Head.

Inspection Criteria:
MIL-STD-883A Method 2009 and 1014.

Notes/References:
(1) Honeywell survey.
(2) Fogiel, Modern Microelectronics (Research and Education Association, NY, 1973).

Section: 1.6.2

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Package Seal	Kovar/Kovar	Seam Weld

Process Qualification Tests:
(1) Seal Qualification Test (Appendix A, Test No. 10).
(2) Visual Inspection.

Process Controls:
(1) Hermeticity test a minimum of five packages at the start of each shift.
(2) Visually inspect a sample of each lot.
(3) Monitor energy output at electrodes.

Screens: (a) Mandatory:
(1) Hermeticity test.
(2) Visual inspection.

(b) Optional:
(1) Thermal shock (liquid-liquid).
(2) Temperature cycle.
(3) PIND.
(4) X-ray.

Critical Parameters:
(1) Pressure.
(2) Energy.
(3) Planarity of seal area.
(4) Cleanliness.
(5) Atmosphere.

Potential Problems:
(1) Inadequate hermeticity.
(2) Trapped particles.

Critical Previous Processes:
(1) Cleaning
(2) Package manufacture/qualification.

Critical Subsequent Processes:
(1) Lead forming.
(2) Repair.

Critical Tools:
(1) Fixtures.
(2) Electrodes.

Inspection Criteria:
MIL-STD-883A Method 2009 and 1014.

Notes/References:
(1) Honeywell survey.
(2) Fogiel, Modern Microelectronics (Research and Education Association, NY, 1973).

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Package Seal	Glass - Devitrified	Hot Cap

Process Qualification Tests:

(1) Seal Qualification Test (Appendix A, Test No. 10).
(2) Visual Inspection.

Process Controls:

(1) Hermeticity test a minimum of five packages at the start of each shift.
(2) Visually inspect a sample of each lot.
(3) Monitor sealer temperature.

Screens:

(a) Mandatory:
(1) Hermeticity test.
(2) Visual inspection.

(b) Optional:
(1) Temperature cycle.
(2) Centrifuge.

Critical Parameters:

(1) Sealer temperature.
(2) Atmosphere.
(3) Glass quantity in seal area.

Potential Problems:

(1) Inadequate hermeticity.
(2) Package/lid alignment.

Critical Previous Processes:

(1) Package manufacture/qualification.
(2) Glass application.

Critical Subsequent Processes:

(1) Lead forming.

Critical Tools:

(1) Sealer.
(2) Sealing head.

Inspection Criteria:

MIL-STD-883A Method 2009 and 1014.

Notes/References:

(1) Honeywell survey.
(2) Fogiel, Modern Microelectronics (Research and Education Association, NY, 1973).

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Package Seal	Glass - Devitrified	Belt Furnace

Process Qualification Tests:
(1) Seal Qualification Test (Appendix A, Test No. 10).
(2) Visual Inspection.

Process Controls:
(1) Hermeticity test a minimum of five packages at the start of each shift.
(2) Visually inspect a sample of each lot.
(3) Monitor furnace profile.

Screens: (a) Mandatory:
(1) Hermeticity test.
(2) Visual inspection.

(b) Optional:
(1) Temperature cycle.
(2) Centrifuge.

Critical Parameters:
(1) Furnace profile.
(2) Atmosphere.
(3) Glass quantity in seal area.

Potential Problems:
(1) Inadequate hermeticity.
(2) Package/lid alignment.
(3) Damage to other components due to high furnace temperature.*

Critical Previous Processes:
(1) Package manufacture/qualification.
(2) Glass application.

Critical Subsequent Processes:
(1) Lead forming.

Critical Tools:
(1) Furnace.
(2) Fixtures.

Inspection Criteria:
MIL-STD-883A Method 2009 and 1014.

Notes/References:
* For limited use only.
(1) Honeywell survey.
(2) Fogiel, Modern Microelectronics (Research and Education Association, NY, 1973).

PROCESS:	MATERIAL(S):	METHOD/MACHINE:
Package Seal	Epoxy	Preform/Screen Print

Process Qualification Tests:

(1) Seal Qualification Test (Appendix A, Test No. 10).
(2) Visual Inspection.

Process Controls:

(1) Hermeticity test a minimum of five packages at the start of each shift.
(2) Visually inspect a sample from each lot.
(3) Monitor curing temperature.

Screens: (a) Mandatory:

(1) Hermeticity test.
(2) Visual inspection.

(b) Optional:

(1) Temperature cycle.
(2) Centrifuge.

Critical Parameters:

(1) Curing temperature.
(2) Atmosphere.
(3) Epoxy quantity in seal area.

Potential Problems:

(1) Inadequate hermeticity.
(2) Seals can only withstand temperatures to 125-150°C.

Critical Previous Processes:

(1) Package manufacture/qualification.
(2) Epoxy application.

Critical Subsequent Processes:

(1) Lead forming.

Critical Tools:

Inspection Criteria:

MIL-STD-883A

Notes/References:

E. Manfre, Circuits Manufacturing P. 32, April 1976.

2.1 Semiconductor Chips

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
Diode Chips	Gold Backed	20 x 20 to 100 x 100 mils (0.508 x 0.508 to 2.54 x 2.54 mm)

Critical Parameters:
(1) Specified electrical parameters at room temperature.
(2) Specified electrical parameters at maximum temperature.

Qualification Tests:

Mandatory:
(1) As required by program

Optional:
(1) Perform all of listed tests on first incoming lot.

Electrical Tests:

For each incoming lot:

Mandatory:
(1) Mount sample of one chip per lot. Measure specified parameters at 25°C.

Optional:
(1) Test 100% of each lot at room temperature without mounting.
(2) Test 100% of each lot at room temperature and at maximum specified temperature.

Visual Inspection Criteria:

Mandatory:
(1) MIL-STD-883A, Method 2010.2; recommend LTPD 15 maximum accept #1, sample of 25.

Optional:
(1) 100% as above.

Mechanical/Physical Tests:

(1) Chip attach - sample of 5.
Note: Test may be performed on visual rejects.
(2) Wire bond - Bond and pull wires to check for metallization quality. One wire per device minimum.
Note: Select sample of 5 chips from every incoming lot.

Notes/References:

Hybrid Microelectronics Standard Specification Guidelines (ISHM - SPA-001).

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
Transistor Chips	Gold Backed	20 x 20 to 100 x 100 mils (0.508 x 0.508 to 2.54 x 2.54 mm)

Critical Parameters:

(1) Specified electrical parameters at room temperature.
(2) Specified electrical parameters at maximum temperature.

Qualification Tests:

Mandatory:
(1) As required by program

Optional:
(1) Perform all of listed tests on first incoming lot.

Electrical Tests:
For each incoming lot:

Mandatory:
(1) Mount sample of one chip per lot. Measure specified parameters at 25°C.

Optional:
(1) Test 100% of each lot at room temperature without mounting.
(2) Test 100% of each lot at room temperature and at maximum specified temperature.

Visual Inspection Criteria:

Mandatory:
(1) MIL-STD-883A, Method 2010.2; recommend LTPD 15 maximum accept #1, sample of 25.

Optional:
(1) 100% as above.

Mechanical/Physical Tests:

(1) Chip attach - sample of 5.
Note: Test may be performed on visual rejects.
(2) Wire bond - Bond and pull wires to check for metallization quality. One wire per device minimum.
Note: Select sample of 5 chips from every incoming lot.

Notes/References:

Hybrid Microelectronics Standard Specification Guidelines (ISHM - SPA-001).

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
IC Chips	All	40 x 40 to 150 x 150 mils (1.02 x 1.02 to 3.81 x 3.81 mm)

Critical Parameters:

(1) Specified electrical parameters at room temperature.
(2) Specified electrical parameters at maximum temperature.

Qualification Tests:

Mandatory:
(1) As required by program.

Optional:
(1) Perform all of listed tests on first incoming lot.

Electrical Tests:

For each incoming lot:

Mandatory:
(1) Mount sample of one chip per lot. Measure specified parameters at 25°C.

Optional:
(1) Test 100% of each lot at room temperature without mounting.
(2) Test 100% of each lot at room temperature and at maximum specified temperature.

Visual Inspection Criteria:

Mandatory:
(1) MIL-STD-883A, Method 2010.2; recommend LTPD 15 maximum accept #1, sample of 25.

Optional:
(1) 100% as above.

Mechanical/Physical Tests:

(1) Chip attach - sample of 5.
Note: Test may be performed on visual rejects.
(2) Wire bond - Bond and pull wires to check for metallization quality. One wire per device minimum.
Note: Select sample of 5 chips from every incoming lot.

Notes/References:

Hybrid Microelectronics Standard Specification Guidelines (ISHM - SPA-001).

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
ROM/RAM Chips	All	All

Critical Parameters:
(1) Specified electrical parameters at room temperature.
(2) Specified electrical parameters at maximum temperature.
(3) Truth table functional parameters.

Qualification Tests:
Mandatory:
(1) As required by program.

Optional:
(1) Perform all of listed tests on first incoming lot.

Electrical Tests:
For each incoming lot:

Mandatory:
(1) Mount sample of one chip per lot. Measure specified paramecers at 25°C.

Optional:
(1) Test 100% of each lot at room temperature without mounting.
(2) Test 100% of each lot at room temperature and at maximum specified temperature.

Visual Inspection Criteria.
Mandatory:
(1) MIL-STD-883A, Method 2010.2; recommend LTPD 15 maximum accept #1, sample of 25.

Optional:
(1) 100% as above.

Mechanical/Physical Tests:
(1) Chip Attach - sample of 5.
Note: Test may be performed on visual rejects.
(2) Wire bond - Bond and pull wires to check for metallization quality. One wire per device minimum.
Note: Select sample of 5 chips from every incoming lot.

Notes/References:

Hybrid Microelectronics Standard Specification Guidelines (ISHM - SPA-001).

2.2 Passive Components

Section: 2.2.1

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
Capacitor Chips	Ceramic	All

Critical Parameters:
Capacitance
Dissipation Factor
Insulation Resistance
Dielectric Withstanding Voltage
Solderability

Qualification Tests:

All mechanical and electrical tests.

Electrical Tests:

Mandatory:
(1) Voltage Conditioning
(2) Capacitance
(3) Dissipation Factor
(4) Insulation Resistance
(5) Dielectric Withstanding Voltage

Optional:
(1) Voltage-Temperature Limits

Visual Inspection Criteria:
MIL-C-55681A
Section 3.19

MIL-STD-833A

Mechanical/Physical Tests:

(1) Solderability
(2) Thermal Shock and Immersion

Notes/References:

MIL-C-55681A

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
Resistor Chips	Semiconductor	NiCr Thin Film

Critical Parameters:

(1) DC Resistance
(2) Resistance - Temperature characteristics
(3) Solderability
(4) Passivation*

Qualification Tests:

Qualify as per
MIL-R-55342 (EL)
Paragraph 4.5

Electrical Tests:

DC Resistance
Resistance/Temperature characteristics
Short Time Overload

Visual Inspection Criteria:

MIL-STD-883A

Mechanical/Physical Tests:

(1) Thermal Shock
(2) Solderability
(3) High Temperature Exposure

Notes/References:

MIL-R-55342 (EL)
Also see MIL-R-83401

* Recommended

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
Resistor Chips	Ceramic	Thin Film

Critical Parameters:

(1) DC Resistance
(2) Resistance-Temperature Characteristics
(3) Solderability
(4) Passivation*

Qualification Tests:	Electrical Tests:
Qualify as per MIL-R-55342 (EL) Paragraph 4.5	DC Resistance Resistance/Temperature Characteristics Short Time Overload

Visual Inspection Criteria:	Mechanical/Physical Tests:
MIL-STD-883A	(1) Thermal Shock (2) Solderability (3) High Temperature Exposure

Notes/References:

MIL-R-55342 (EL)
Also see MIL-R-83401

* Recommended

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
Resistor Chips	Ceramic	Thick Film

Critical Parameters:

(1) DC Resistance
(2) Resistance-Temperature Characteristics
(3) Solderability
(4) Passivation*

Qualification Tests:

Qualify as per
MIL-R-55342 (EL)
Paragraph 4.5

Electrical Tests:

DC Resistance
Resistance/Temperature Characteristics
Short Time Overload

Visual Inspection Criteria:

MIL-STD-883A

Mechanical/Physical Tests:

(1) Thermal Shock
(2) Solderability
(3) High Temperature Exposure

Notes/References:

MIL-R-55342 (EL)
Also see MIL-R-83401

* Recommended

2.3 Substrates

Section: 2.3.1

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
Substrates	99.5% Al_2O_3	10 - 25 mils thick (0.254 - 0.635 mm)

Critical Parameters:
(1) Surface finish (<10 microinches/0.25 micron maximum, <3 microinches/0.075 micron preferred)
(2) Surface defect density
(3) Camber (<0.002 inch per inch)
(4) Dimensions

Qualification Tests:
Mandatory:
(1) Surface finish test using Dektak or Tallysurf.
(2) Thermal shock test.
(3) Strength test.
Optional:
(1) Check electrical parameters - loss tangent, dielectric constant, etc.
(2) Check thermal properties - TCE, conductivity.

Electrical Tests:
None

Visual Inspection Criteria:
Check for:
- Cracks, chips, similar defects
- Cleanliness
- Proper packaging

Mechanical/Physical Tests:
Mandatory:
(1) Dimensional inspection - thickness, camber, surface finish
Optional:
(1) Thermal shock test
(2) Strength test

Notes/References:
Notes: (1) Cleaning process for incoming substrates is critical to subsequent processing.

References:
(1) L. Maissel and R. Glang, Handbook of Thin Film Technology, (McGraw-Hill Book Co., N.Y. 1970).
(2) K. L. Chopra, Thin Film Phenomena, (McGraw-Hill Book Co., N.Y. 1970).
(3) NASA Report, P71-59.
(4) Frank Ura, Hewlett Packard Labs, Palo Alto, CA, Private Communication.

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
Substrates	Polished 99.5% Al_2O_3	10 - 25 mils thick (0.254 - 0.635 mm)

Critical Parameters:
(1) Surface finish (∿1 microinch/0.025 micron)
(2) Surface defect density
(3) Camber (<0.002 inch per inch)
(4) Dimensions

Qualification Tests:

Mandatory:
(1) Surface finish test using Dektak or Tallysurf
(2) Thermal shock test
(3) Strength test

Optional:
(1) Check electrical parameters - loss tangent, dielectric constant, etc.
(2) Check thermal properties, TCE, conductivity, etc.

Electrical Tests:

None

Visual Inspection Criteria:

Check for:
- Cracks, chips, similar defects
- Cleanliness
- Proper packaging

Mechanical/Physical Tests:

Mandatory:
(1) Dimensional inspection:
- Thickness, camber, surface finish

Optional:
(1) Thermal shock test
(2) Strength test

Notes/References:

Notes: (1) Cleaning process for incoming substrates is critical to subsequent processing.

References: (1) L. Maissel and R. Glang, Handbook of Thin Film Technology, (McGraw-Hill Book Co., NY 1970).
(2) K. L. Chopra, Thin Film Phenomena, (McGraw-Hill Book Co., NY, 1970).
(3) NASA Report, P71-59.
(4) Frank Ura, Hewlett Packard Labs, Palo Alto, CA, Private Communication.

Section: 2.3.3

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
Substrates	96% Al_2O_3	10 - 60 mils thick (0.254 - 1.524 mm)

Critical Parameters:

(1) Surface smoothness (∿25 microinches/0.625 micron)
(2) Camber (<0.004 inch per inch)
(3) Surface defects
(4) Dimensions

Qualification Tests:

Mandatory:
(1) Surface finish test using Dektak or Tallysurf
(2) Thermal shock test
(3) Strength test

Optional:
(1) Check electrical parameters - loss tangent, dielectric constant, etc.
(2) Check thermal properties - TCE, conductivity

Electrical Tests:

None

Visual Inspection Criteria:

Check for:
- Cracks, chips, similar defects
- Cleanliness
- Proper packaging

Mechanical/Physical Tests:

Mandatory:
(1) Dimensional inspection - thickness, camber, surface finish

Optional:
(1) Thermal shock test
(2) Strength test

Notes/References:

Notes: (1) Cleaning process for incoming substrates is critical to subsequent processing.

References: (1) L. Maissel and R. Glang, Handbook of Thin Film Technology, (McGraw-Hill Book Co., NY, 1970).
(2) K. L. Chopra, Thin Film Phenomena, (McGraw-Hill Book Co., NY, 1970).
(3) NASA Report, P71-59.
(4) Frank Ura, Hewlett Packard Labs, Palo Alto, CA, Private Communication.

Section: 2.3.4

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
Substrates	96% Glazed Al_2O_3	10 - 60 mils thick (0.254 - 1.524 mm)

Critical Parameters:

(1) Surface finish (<1 microinch/0.025 micron)
(2) Camber (<0.004 inch per inch)
(3) Surface defect density
(4) Dimensions

Qualification Tests:

Mandatory:
(1) Surface finish test using Dektak or Tallysurf
(2) Thermal shock test
(3) Strength test

Optional:
(1) Check electrical parameters - loss tangent, dielectric constant, etc.
(2) Check thermal properties - TCE, conductivity

Electrical Tests:

None

Visual Inspection Criteria:

Check for:
- Cracks, chips, similar defects
- Cleanliness
- Proper packaging

Mechanical/Physical Tests:

Mandatory:
(1) Dimensional inspection - thickness, camber, surface finish

Optional:
(1) Thermal shock test
(2) Strength test

Notes/References: (1) Sacrifice Thermal Conductivity

Notes: (2) Cleaning process for incoming substrates is critical to subsequent processing.

References: (1) L. Maissel and R. Glang, Handbook of Thin Film Technology, (McGraw-Hill Book Co., NY, 1970).
(2) K. L. Chopra, Thin Film Phenomena, (McGraw-Hill Book Co., NY, 1970).
(3) NASA Report, P71-59.
(4) Frank Ura, Hewlett Packard Labs, Palo Alto, CA, Private Communication.

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
Substrates	BeO	10 - 60 mils thick (0.254 - 1.524 mm)

Critical Parameters:

(1) Surface finish (8-15 microinches/0.2-0.375 micron)
(2) Surface defect density
(3) Camber (<0.004 inch per inch)
(4) Dimensions

Qualification Tests:

Mandatory:
(1) Surface finish test using Dektak or Tallysurf
(2) Thermal shock test
(3) Strength test

Optional:
(1) Check electrical parameters - loss tangent, dielectric constant, etc.
(2) Check thermal properties - TCE, conductivity

Electrical Tests:

None

Visual Inspection Criteria:

Check for:
- Cracks, chips, similar defects
- Cleanliness
- Proper packaging

Mechanical/Physical Tests:

Mandatory:
(1) Dimensional inspection - thickness, camber, surface finish

Optional:
(1) Thermal shock test
(2) Strength test

Notes/References:

(1) BeO must not be machined in lab; dust is highly toxic.
(2) Surface roughness often requires glazing.

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
Substrates	SiO_2 (Wafer)	3 - 25 mils thick (0.075 - 0.635 mm)

Critical Parameters:

(1) Surface finish (∿1 microinch/0.025 micron)
(2) Surface defect - scratches
(3) Dimensions

Qualification Tests:

All mechanical/physical tests and visual inspection.

Electrical Tests:

None

Visual Inspection Criteria:

Check for:
- Scratches, cracks, defects
- Cleanliness
- Proper packaging

Mechanical/Physical Tests:

Mandatory:
(1) Dimensional inspection - thickness, camber, surface finish

Notes/References:

Notes: (1) Cleaning process for incoming substrates is critical to subsequent processing.

References: (1) L. Maissel and R. Glang, Handbook of Thin Film Technology, (McGraw-Hill Book Co., NY, 1970).
(2) K. L. Chopra, Thin Film Phenomena, (McGraw-Hill Book Co., NY, 1970).
(3) NASA Report, P71-59.
(4) Frank Ura, Hewlett Packard Labs, Palo Alto, CA, Private Communication.

2.4 Packages/Lids

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
Package	Kovar	16 Pin DIP

Critical Parameters:
(1) Electrical Isolation
(2) Thermal Resistance (θ_{JA})
(3) Resistance to Corrosion
(4) Mechanical Strength
(5) Hermeticity
(6) EMI/TEMPEST*

Qualification Tests:
(1) Mechanical Shock Test
(2) Thermal Shock Test
(3) Thermal Cycle Test
(4) Vibrational Test (variable frequency)
(5) Lead to Ground Resistance
(6) Hermeticity Test
(7) Salt Atmosphere Test (Corrosion)
(8) Lead Strength

Electrical Tests:
(1) Lead to Ground Resistance
(2) Pin-Pin Isolation

Visual Inspection Criteria:
MIL-STD-883A Method 2009.1

Mechanical/Physical Tests:
(1) Mechanical Shock Test
(2) Thermal Shock Test
(3) Thermal Cycle Test
(4) PIND Test

Notes/References:
(1) M. Fogiel, Modern Microelectronics (Research and Education Association, NY, 1973).
(2) ISHM-SPA-001

* Depending on Application

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
Package	Ceramic	16 Pin DIP

Critical Parameters:
(1) Electrical Isolation
(2) Thermal Resistance (θ_{JA})
(3) Resistance to Corrosion
(4) Mechanical Strength
(5) Hermeticity
(6) EMI/TEMPEST*

Qualification Tests:
(1) Mechanical Shock Test
(2) Thermal Shock Test
(3) Thermal Cycle Test
(4) Vibrational Test (variable frequency)
(5) Lead to Ground Resistance
(6) Hermeticity Test
(7) Salt Atmosphere Test (Corrosion)
(8(Lead Strength

Electrical Tests:
(1) Lead to Ground Resistance
(2) Pin-Pin Isolation

Visual Inspection Criteria:
MIL-STD-883A Method 2009.1

Mechanical/Physical Tests:
(1) Mechanical Shock Test
(2) Thermal Shock Test
(3) Thermal Cycle Test
(4) PIND Test

Notes/References:

(1) M. Fogiel, Modern Microelectronics (Research and Education Association, NY, 1973).
(2) ISHM-SPA-001

* Depending on Application

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
Package	Kovar - Glass Leadout	All

Critical Parameters:
(1) Electrical Isolation
(2) Thermal Resistance (θ_{JA})
(3) Resistance to Corrosion
(4) Mechanical Strength
(5) Hermeticity
(6) EMI/TEMPEST*

Qualification Tests:
(1) Mechanical Shock Test
(2) Thermal Shock Test
(3) Thermal Cycle Test
(4) Vibrational Test (variable frequency)
(5) Lead to Ground Resistance
(6) Hermeticity Test
(7) Salt Atmosphere Test (Corrosion)
(8) Lead Strength

Electrical Tests:
(1) Lead to Ground Resistance
(2) Pin-Pin Isolation

Visual Inspection Criteria:
MIL-STD-883A Method 2009.1

Mechanical/Physical Tests:
(1) Mechanical Shock Test
(2) Thermal Shock Test
(3) Thermal Cycle Test
(4) PIND Test

Notes/References:

(1) M. Fogiel, Modern Microelectronics (Research and Education Association, NY, 1973).
(2) ISHM-SPA-001

* Depending on Application

3.1 Thick Film Pastes

Section: 3.1.1

MATERIAL:	TYPE:	CONFIGURATION/SIZE:
Thick Film Paste (Ink)	Conductor	All

Critical Parameters/Properties:

(1) Chemical/physical constituents
(2) Viscosity
(3) Age

Qualification Tests:

(1) Film Thickness - Optical Method (Appendix A, Test No. 1).
    or Optional:
    Film Thickness - Stylus Method (Appendix A, Test No. 2)
(2) Bondability (Appendix A, Test No. 3)
(3) Adhesion - Oiler Method (Appendix A, Test No. 4)

Electrical Tests:

(1) On fired sample: (a) Conductivity

Visual Inspection Criteria:

(1) Physical condition of container (must be sealed)
(2) Review of records (lot number, ship date, expiration date, etc.)

Mechanical/Physical Tests:

(1) Infrared analysis
(2) Viscosity test
(3) On fired sample: (a) Thickness
    (b) Porosity (SEM)
    (c) Bondability
    (d) Adhesion

Notes/References:

(1) ECOM Report 75-1331-1

MATERIAL:	TYPE:	CONFIGURATION/SIZE:
Thick Film Paste	Resistor	Ruthenium Oxide (and similar)

Critical Parameters/Properties:

(1) Chemical/physical constituents
(2) Viscosity
(3) Age

Qualification Tests:

Resistance Qualification Test (Appendix A, Test No. 11)

Electrical Tests:

(1) On fired sample:
    (a) Resistivity
    (b) TCR

Visual Inspection Criteria:

Mechanical/Physical Tests:

(1) Infrared analysis
(2) Viscosity test
(3) On fired sample:
    (a) Thickness
    (b) Surface composition (SEM)

Notes/References:

(1) ECOM Report 75-1331-1

Section:	3.1.3

MATERIAL:	TYPE:	CONFIGURATION/SIZE:
Thick Film Paste	Dielectric	All

Critical Parameters/Properties:

(1) Chemical/physical constituents
(2) Breakdown voltage after fire
(3) Mechanical strength after fire
(4) Resistance to solder leaching

Qualification Tests:

Dielectric Qualification Test (see Appendix A, Test No. 12)

Electrical Tests:

(1) On fired sample: Breakdown voltage

Visual Inspection Criteria:

(1) Color
(2) Condition of container (must be sealed)
(3) Review of records (lot number, ship date, expiration date, etc.)

Mechanical/Physical Tests:

(1) On fired sample:
 (a) Thickness
 (b) Mechanical puncture strength
(2) Resistance to solder leaching per MIL-STD-202, Method 208

Notes/References:

ECOM Report 75-1331-1

3.2 Epoxies

Section: 3.2.1

MATERIAL:	TYPE:	CONFIGURATION/SIZE:
Epoxy	Conductive	All

Critical Parameters/Properties:

(1) Adhesion
(2) Conductivity
(3) Outgassing
(4) Aging/curing characteristics
(5) Run-out characteristics
(6) Corrosivity

Qualification Tests:

Epoxy Qualification Test (see Appendix A, Test No. 13)

Electrical Tests:

(1) Conductivity/resistivity (volume)
(2) Conductivity stability (after temperature aging)

Visual Inspection Criteria:

(1) Physical condition of container (must be sealed)
(2) Review of records (lot number, ship date, expiration date, etc.)

Mechanical/Physical Tests:

(1) Adhesive shear strength
(2) Curing characteristics
(3) Outgassing/weight loss
(4) Viscosity when curing (run-out)
(5) Chemical analysis of constituents (IR spectroscopy)
(6) Filler content
(7) Corrosivity to aluminum
(8) Flexural yield temperature

Notes/References:

Section: 3.2.2

MATERIAL:	TYPE:	CONFIGURATION/SIZE:
Epoxy	Nonconductive	Bulk

Critical Parameters/Properties:
(1) Adhesion
(2) Outgassing
(3) Aging/curing characteristics
(4) Run-out characteristics
(5) Corrosivity

Qualification Tests:
(1) Epoxy Qualification Test (see Appendix A, Test No. 13)

Electrical Tests:
None

Visual Inspection Criteria:
(1) Physical condition of container (must be sealed)
(2) Review of records (lot number, ship date, expiration date, etc.)

Mechanical/Physical Tests:
(1) Adhesive shear strength
(2) Curing characteristics
(3) Outgassing/weight loss
(4) Viscosity when curing (run-out)
(5) Chemical analysis of constituents (IR spectroscopy)
(6) Filler content
(7) Corrosivity to aluminum
(8) Flexural yield temperature

Notes/References:

MATERIAL:	TYPE:	CONFIGURATION/SIZE:
Epoxy	Nonconductive	Film

Critical Parameters/Properties:

(1) Adhesion
(2) Outgassing
(3) Aging/curing characteristics
(4) Run-out characteristics
(5) Corrosivity
(6) Film thickness

Qualification Tests:

(1) Epoxy Qualification Test (see Appendix A, Test No. 13)

Electrical Tests:

None

Visual Inspection Criteria:

(1) Physical condition of container (must be sealed)
(2) Review of records (lot number, ship date, expiration date, etc.)

Mechanical/Physical Tests:

(1) Adhesive shear strength
(2) Curing characteristics
(3) Outgassing/weight loss
(4) Viscosity when curing (run-out)
(5) Chemical analysis of constituents (IR spectroscopy)
(6) Filler content
(7) Corrosivity to aluminum
(8) Flexural yield temperature
(9) Film thickness

Notes/References:

3.3 Solders

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
Solder	All	All

Critical Parameters:

(1) Composition
(2) Melting Point
(3) Ability to Wet Conductor Pads
(4) Flux
(5) Atmosphere Necessary for Reflow
(6) Thickness (Preform Only)

Qualification Tests:

(1) Melting Point Determination
(2) Composition
(3) Ability to Wet Conductors
(4) Shear Test
(5) Leaching/Scavenging (Pull) Test
(6) Thickness (Preform Only)

Electrical Tests:

None

Visual Inspection Criteria:

(1) Federal Specification QQ-S-571, "Solder; Tin Alloy; Lead-Tin Alloy; and Lead Alloy".

Mechanical/Physical Tests:

(1) Shear Strength
(2) Ability to Wet Conductors
(3) Leaching/Scavenging (Pull) Test
(4) Thickness (Preform Only)

Notes/References:

(1) C.E.T. White and H.C. Sohl, Solid State Technology 18, 45 (1975)
(2) QQ-S-571

3.4 Eutectics

Section: 3.4

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
Eutectic	All	Preform

Critical Parameters:

(1) Eutectic Temperature
(2) Composition/Purity
(3) Thickness and Dimensions

Qualification Tests:	Electrical Tests:
All mechanical/physical tests	None

Visual Inspection Criteria:	Mechanical/Physical Tests:
None	(1) Thermal Conductivity (2) Dimensions (3) Eutectic Temperature Determination

Notes/References:

C.E.T. White and H.C. Sohl, Solid State Technology 18, 45 (1975)

3.5 Bonding Wire

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
Bonding Wire	Gold	0.0007 - 0.002 inch (0.018 - 0.051 mm)

Critical Parameters:

(1) Diameter/Tolerance
(2) Temper - Stress Relieved or Annealed
(3) Purity
(4) Breaking Load
(5) Elongation

Qualification Tests:

All mechanical/physical tests.

Electrical Tests:

None

Visual Inspection Criteria:

Using 30X microscope, check wire surface for: stains, oils, lubricants, particles; also nicks, dents or bumps which exceed 10% of wire diameter.

Mechanical/Physical Tests:

(1) Chemical Composition (Vendor Certification)
(2) Dimensions and tolerances
(3) Breaking Strength*
(4) Elongation*

*ASTM F-219

Notes/References:

(1) ISHM-SPA-001
(2) Solid State Technology 18, 31 (1975)

Section: 3.5.2

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
Bonding Wire	Aluminum/Silicon (1%)	0.0007 - 0.002 inch (0.018 - 0.051 mm)

Critical Parameters:

(1) Diameter/Tolerance
(2) Composition/Purity
(3) Breaking Load
(4) Elongation
(5) Temper

Qualification Tests:

All tests, plus check bondability on certified substrate metallized with gold.

Electrical Tests:

None

Visual Inspection Criteria:

Using 30X microscope, inspect wire surface for: stains, oils, lubricants, particles; also check for nicks, dents or bumps which exceed 10% of the wire diameter.

Mechanical/Physical Tests:

(1) Chemical Composition - Vendor Certification
(2) Dimensions and tolerances
(3) Breaking Strength*
(4) Elongation*

*ASTM F-219

Notes/References:

(1) ISHM-SPA-001
(2) Solid State Technology 18, 31 (1975)

Section: 3.5.3

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
Bonding Wire	Aluminum	0.003 inch (0.076 mm)

Critical Parameters:

(1) Diameter/Tolerance
(2) Temper
(3) Purity
(4) Breaking Load
(5) Elongation

Qualification Tests:

All tests, plus check bondability on certified substrate metallized with gold.

Electrical Tests:

None.

Visual Inspection Criteria:

Using 30X microscope, inspect wire surface for: stains, oils, lubricants, particles; also check for nicks, dents, or bumps which exceed 10% of the wire diameter.

Mechanical/Physical Tests:

(1) Chemical Composition - Vendor Certification
(2) Dimensions and Tolerances
(3) Breaking Strength*
(4) Elongation*

*ASTM F-219

Notes/References:

(1) ISHM-SPA-001
(2) Solid State Technology 18, 31 (1975)

COMPONENT:	TYPE:	CONFIGURATION/SIZE:
Bonding Wire	Aluminum/ Magnesium	0.0007 - 0.002 inch (0.018 - 0.051 mm)

Critical Parameters:

(1) Diameter/Tolerance
(2) Temper
(3) Purity
(4) Breaking Load
(5) Elongation

Qualification Tests:

All tests, plus check bondability on certified substrates metallized with gold.

Electrical Tests:

None.

Visual Inspection Criteria:

Using 30X microscope, inspect wire surface for: stains, oils, lubricants, particles; also check for nicks, dents, or bumps which exceed 10% of the wire diameter.

Mechanical/Physical Tests:

(1) Chemical Composition - Vendor Certification
(2) Dimensions and Tolerances
(3) Breaking Strength*
(4) Elongation*

*ASTM F-219

Notes/References:

(1) ISHM-SPA-001
(2) Solid State Technology 18, 31 (1975)

4.0 Rework

4.1 Chip Removal

Section: 4.1.1

PROCESS: Chip Removal - Epoxy Attached

METHOD/MACHINE: Manual

Process Description:

Using a tiny chisel or dental pick, carefully separate chip from substrate. Localized heating (150°-180°C) from hot gas jet held under chip area of substrate will soften epoxy, but can cause degradation of Al to Au wirebonds. If no heat is used, considerable force is usually necessary for chip removal, thus great care must be taken so as not to damage metallization. NOTE: For large chips, laser sectioning may be necessary.

Process Controls:

(1) Operator Certification.

Screens:

(a) Mandatory: Visual inspection for metallization scratches or other damage, also be sure old chip and epoxy residue have been completely removed.

(b) Optional:

Critical Parameters:

(1) Number of times reworked.

Potential Problems:

(1) Metallization scratches
(2) Wire bond degradation if heat is applied.

Replacement Procedure:

See appropriate sheet in Section 1.3.

Inspection Criteria:

MIL-STD-883A

Critical Tools:

Optional:
(1) Hot gas jet for local heating
(2) Fine point tweezers

References:

Hybrid Microelectronics Standard Specification Guidelines (ISHM-SPA-001)

Rework Limitations:

Cannot be reworked if metallization is damaged.

PROCESS: Chip Removal - Solder Attached

METHOD/MACHINE: Manual

Process Description:

Using localized heating under substrate, raise temperature until solder has melted. Remove chip with tweezers.

Process Controls:

(1) Operator certification.
(2) Control substrate temperature.
(3) Control localization of applied heat.

Screens: (a) Mandatory: (1) Visual inspection for metallization scratches.

(b) Optional:

Critical Parameters:
(1) Number of times reworked.

Potential Problems:
(1) Metallization scratches/other damage.
(2) Reflow of solder on other chips.

Replacement Procedure:

See Sheet 1.3.10.

Inspection Criteria:

MIL-STD-883A

Critical Tools:

Hot gas jet for local heating

References:

Hybrid Microelectronics Standard Specification Guidelines (ISHM-SPA-001)

Rework Limitations:

Cannot be reworked if metallization is damaged.

4.2 Substrate Removal

Section: 4.2.1

PROCESS:
Substrate Removal - Epoxy Attached

METHOD/MACHINE:

Process Description:
If substrate is attached to a package, apply heat from bottom of package (raise temperature to ∿ 160°C), and lift substrate out of package when epoxy softens. If substrate is attached to a master interconnect board, apply local heat from hot gas jet directly to defective substrate; when epoxy softens, remove from master interconnect board.

NOTE: Care must be taken so as not to overheat wire bonds on master board.

Process Controls:
(1) Operator Certification

Screens: (a) Mandatory: Visual inspection per MIL-STD-883A.

(b) Optional:

Critical Parameters:

Potential Problems:
Wire bond degradation on master interconnect board.

Replacement Procedure:
See Section 1.5.1

Inspection Criteria:
MIL-STD-883A

Critical Tools:

References:
Hybrid Microelectronics Standard Specification Guidelines (ISHM-SPA-001)

Rework Limitations:
Cannot be reworked if metallization is damaged.

PROCESS:	METHOD/MACHINE:
Substrate Removal - Solder Attached	Manual

Process Description:

If substrate is attached to a package, apply heat from bottom of package and lift the substrate out when solder melts.
If substrate is attached to a master interconnect board, apply heat from hot gas jet directly to defective substrate; when solder melts, remove substrate from master interconnect board.

NOTE: Care must be taken so as not to overheat wire bonds on Master Board.

Process Controls:

(1) Operator certification.

Screens: (a) Mandatory: Visual inspection per MIL-STD-883A.

(b) Optional:

Critical Parameters:	Potential Problems: Wire bond degradation on a master interconnect board.
Replacement Procedure: See Section 1.5.2	**Inspection Criteria:** MIL-STD-883A
Critical Tools:	**References:** Hybrid Microelectronics Standard Specification Guidelines (ISHM-SPA-001)

Rework Limitations:

Cannot be reworked if metallization is damaged.

4.3 Wire Bond

PROCESS:	METHOD/MACHINE:
Wire Bond	All

Process Description:

Remove faulty wire bonds with tweezers (with aid of microscope). Determine whether there is sufficient room on metallization pads to apply new wire bonds. If not, see chip removal Section 4.1.

NOTE: Do not attempt to remove bond foot.

Process Controls:

(1) Operator certification
(2) Wire bond machine certification

Screens: (a) Mandatory: Refer to appropriate sheet in Section 1.4.

(b) Optional:

Critical Parameters:	Potential Problems:
(1) Extent of damage to metallized pads (2) See Section 1.4	No room left on pad to accept new wire bond - replace chip.

Replacement Procedure:	Inspection Criteria:
Refer to appropriate sheet in Section 1.4	MIL-STD-883A

Critical Tools:	References:
See Section 1.4	Hybrid Microelectronics Standard Specification Guidelines (ISHM-SPA-001)

Rework Limitations:

Pad size per MIL-STD-883A.

4.4 Open Package

PROCESS:	METHOD/MACHINE:
Open Package - Welded - Brazed	Lapping

Process Description:

Top of package may be removed by lapping technique, that is, by rubbing package top down against flat abrasive silicon-carbide sheet, using "Figure 8" motion. When top is worn sufficiently thin, top may be removed with X-acto knife.

NOTE: Package may be opened to improve bad seal or to rework circuitry-- latter is less common.

Process Controls:

Periodic visual inspection during lapping procedure.

Screens: (a) Mandatory: Visual inspection

(b) Optional:

Critical Parameters:	Potential Problems:
Flatness/condition of lapped surface	Package contamination
Replacement Procedure:	**Inspection Criteria:**
See appropriate sheet in Section 1.6.	MIL-STD-883A
Critical Tools:	**References:**
Flat silicon-carbide abrasive	Hybrid Microelectronics Standard Specification Guidelines (ISHM-SPA-001)

Rework Limitations:

More than one cycle not recommended.

Section: 4.4.2

PROCESS:
Open Package - Epoxy Seal

METHOD/MACHINE:
Heat

Process Description:

Heat package on hot plate to soften eposy, lift off lid.
Use lapping procedure to remove package defects.

NOTE: Package may be opened to improve a bad seal or to rework circuitry-- the latter is less common.

Process Controls:

(1) Control temperature of hot plate.

Screens: (a) Mandatory: Visual inspection

(b) Optional:

Critical Parameters:

Potential Problems:
(1) Wire bond degradation from heat
(2) Contamination

Replacement Procedure:
See appropriate sheet in Section 1.6.

Inspection Criteria:
MIL-STD-883A

Critical Tools:
Hot plate

References:
Hybrid Microelectronics Standard Specification Guidelines (ISHM-SPA-001)

Rework Limitations:
More than one cycle not recommended.

APPENDIX A

QUALIFICATION TESTS

INDEX - QUALIFICATION TESTS

1. Film Thickness - Optical Method
2. Film Thickness - Stylus Method
3. Bondability
4. Adhesion - Oiler Method
5. Film Thickness - Four Point Probe
6. Solderability/Wettability
7. Chip Adherence Strength
8. Destructive Shear
9. Infrared Thermal
10. Seal Qualification
11. Resistance Qualification
12. Dielectric Qualification
13. Epoxy Qualification

Test Number: 1

PART/COMPONENT/MATERIAL QUALIFICATION TEST

TEST NAME:	APPLICABLE PROCESSES:
Film Thickness - Optical Method	Substrate Fabrication - Thick Film

Objectives:
Assure consistency in application and firing of thick film pastes.

Parameters: Thickness:	Test Conditions:
Gold: 8 micrometers min* Platinum - Gold: 8 micrometers min* Resistors: 10 micrometers min*	Room temperature
Sample Size: 25 pieces from qualification lot	Test Vehicle: Sample production boards

Test Description:
Thickness measurements with Zeiss split field optics microscope or equivalent.

Test Details: (Continue on new sheet, if required)
Measure thickness per instructions supplied with instruments.

References:
*Note: For reference only.

Test Number: 2

PART/COMPONENT/MATERIAL QUALIFICATION TEST

TEST NAME:	APPLICABLE PROCESSES:
Film Thickness - Stylus Method	(1) Substrate Fabrication - Thick Film (2) Substrate Fabrication - Thin Film

Objectives:

(1) Assure consistency in application and firing of thick film pastes. (Alternate to optical method.)
(2) Assure proper control of thin film sputtering of evaporative processes.

Parameters:	Thickness	Test Conditions:
Thick Film Conductors (all)	8 micrometers	Room Temperature
Thick Film Resistors	10 micrometers	
Thin Film Conductors		

Sample Size:	Test Vehicle:
5 pieces from qualification lot.	Sample production boards.

Test Description:

The Tally-surf or stylus method of measuring thickness does so by mechanically sensing the steps of the metal thickness elevation above the uncoated portions of the substrate.

Test Details: (Continue on new sheet, if required)

(1) Thick Film: Run Tally-surf (or equivalent) stylus across several parallel conductor lines on the boards. Determine thickness from trace read-out.
(2) Thin Film: Etch several parallel conductor lines on the boards. Then run Tally-surf (or equivalent) stylus across several of the lines and determine thickness from trace readout.

References:

Test Number: 3

PART/COMPONENT/MATERIAL QUALIFICATION TEST

TEST NAME:	APPLICABLE PROCESSES:
Bondability	(1) Substrate Fabrication - Thick Film (2) Substrate Fabrication - Thin Film (3) Wire Bonding Process - All (Incl Beam Lead)

Objectives:
(1) Ensure that during the metallization processes no anomalies have been introduced which adversely affect the capability of the surface to accept and retain wire bonds of adequate strength.
(2) Qualifying the wire and beam lead bonding process.

Parameters:	Test Conditions:
(1) No. of bond lifts during bonding (2) Bond strength before and after storage (3) (Op) Bond resist. before and after storage	Storage at 125°C for 90 hours
Sample Size: Minimum 1 substrate Minimum 50 wire loops (100 boards)	**Test Vehicle:** (Note 1) Sample production boards or special test substrate manufactured with the same proc. and at the same time as the prod. boards

Test Description:
A number of wire bonds is made to sample substrates and half are pulled to destruction to measure bond strength. The remainder is heat aged to determine degradation after storage.

Test Details: (Continue on new sheet, if required)
(1) A qualified wire bonding operator is to make 50 1 mil aluminum wire bonds* using certified production bonder and standard production controls.
(2) (Optional) Measure resistance of wire loops and record.
(3) Pull 25 wire bonds and record pull strength and break mode. Acceptance limit is the same as currently used production $\bar{X}$ and R (or S) limits.
(4) Place board in air circulating oven at 125°C for 90 hours.
(5) After 90 hours, measure resistance of remaining 25 wire loops (optional).
(6) Pull remaining 25 wire bonds and record pull strength and break mode. Acceptance criteria may be set on the basis of experience with acceptable degradation. Recommended is no more than 50 percent bond strength decrease. No resistance increase. No more than 30 percent bond lifts.

Note 1: For qualification of wire bonding processes, use a known good thin film board, and the wire size and material to be qualified.

*This method may be adapted to beam leads.

References: (1) "Changes in strength and resistance after burn-in of aluminum wire bonds to thick and thin film gold" William R. Rodrigues de Miranda and R.G. Oswald - ISHM 1974. (2) "Changes in strength and resistance of aluminum to gold ultrasonic bonds after temperature, electrical and environmental stress" R.G. Oswald, W.R. Rodrigues de Miranda, C.W. White - ISHM 1975.

Test Number:
4

PART/COMPONENT/MATERIAL QUALIFICATION TEST

TEST NAME: Adhesion - Oiler Method	APPLICABLE PROCESSES: (1) Substrate Fabrication - Thick Film (2) Substrate Fabrication - Thin Film
Objectives: Measure the adhesion strength of the metal film to the substrate	
Parameters: None	Test Conditions: N/A
Sample Size: 1-3 substrates per lot	Test Vehicle: Sample production boards
Test Description: Probe conductor lines with tip of oiler or pin. Lines should remain adherent and should show scratches without metal flaking.	
Test Details: (Continue on new sheet, if required) N/A	
References:	

Test Number:
5

PART/COMPONENT/MATERIAL QUALIFICATION TEST

TEST NAME:	APPLICABLE PROCESSES:
Film Thickness - Four Point Probe	(1) Substrate Fabrication - Thick Film (2) Substrate Fabrication - Thin Film

Objectives:

Measure the thickness of the conductive film

Parameters:	Test Conditions:
Ohms per square resistivity/conductivity converted to film thickness.	Room ambient 500 mA measuring current
Sample Size:	**Test Vehicle:**
1 substrate per metallization lot	Actual substrate. Use path with greatest length to width ratio.

Test Description:

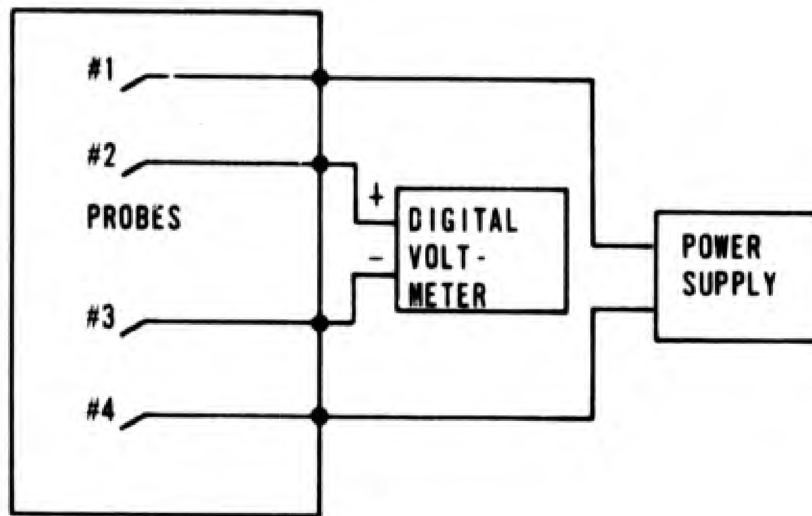
Film thickness is proportional to the resistance per square of film. The latter is measured by forcing a known current through a conductor path and measuring the voltage drop across a known number of squares, using a second set of probes inside the current probes.

Test Details: (Continue on new sheet, if required)

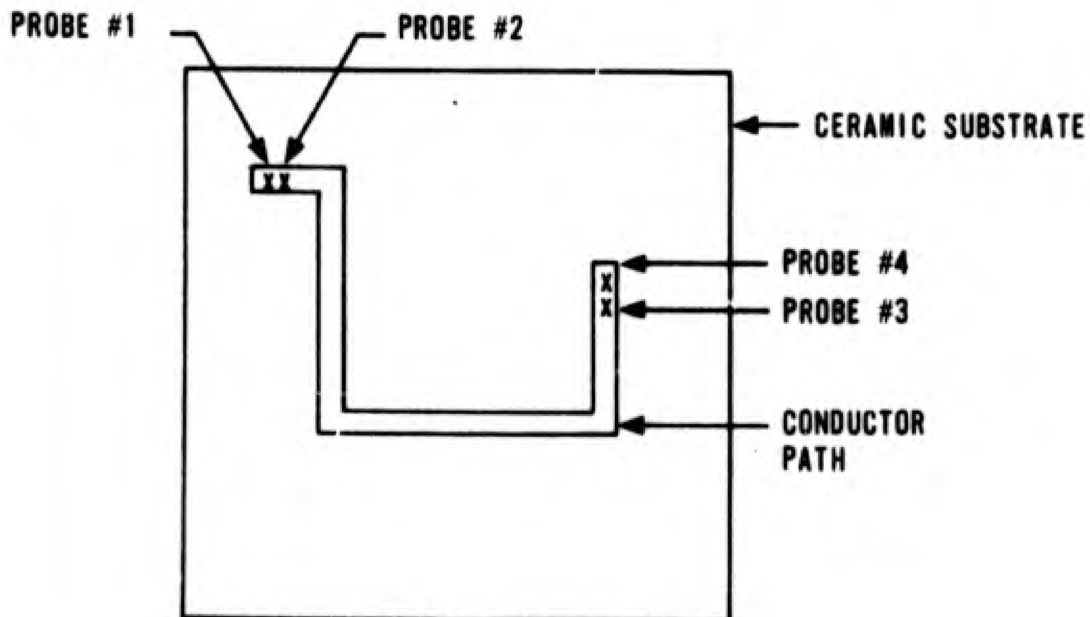
(1) On the sample board, locate the conductor path with the greatest length to width ratio. This will make resistivity measurement the easiest and most accurate since the actual number of squares of material can be calculated closely and the voltage drop resulting from forcing current through the line will be the highest.
(2) Adjust the current and voltage settings on the power supply to minimum. Turn on the supply and adjust the output voltage to 5V (increase the current limiting if necessary). Apply a jumper wire across the power supply and adjust the current up to 500 mA ±25 mA. This will limit the current applied to the conductor path during the following steps. Turn the power supply off and remove the jumper.
(3) Patch the power supply, voltmeter, and 4 point system together as shown.

References:

TEST DETAILS (Continued)



(4) Place the sample substrate under the probes and adjust the probes to contact the conductor path chosen, as shown:



(5) The distance between No. 1 and No. 2 probes and between No. 3 and No. 4 probes should be one square of material or greater to assure an accurate resistive reading.
(6) Apply power (500 mA) to the conductor path and note the voltage that results on the digital voltmeter.
(7) Using the drawing for the conductor layer being measured, calculate the number of squares of conductor material between the No. 2 and No. 3 probes.
(8) Use the formula VOLTAGE/#SQUARES x 2, to calculate the resistivity.
EXAMPLE: 0.50 volt/100 Squares x 2 = 0.010 Ω/□

Test Number:
6

PART/COMPONENT/MATERIAL QUALIFICATION TEST

TEST NAME:	APPLICABLE PROCESSES:
Solderability/Weldability	Substrate Fabrication - Thick Film

Objectives:
Determine capability of film surface to adhere to solder and to resist leaching.

Parameters:	Test Conditions:
Per MIL-STD-202, Method 208	Aging per MIL-STD-202, Method 208
Sample Size:	**Test Vehicle:**
5 boards	(1) Actual boards from first production run (2) (Optional) Specially designed test Boards (Ref 2)

Test Description:
See MIL-STD-202, Method 208.

Test Details: (Continue on new sheet, if required)
See MIL-STD-202, Method 208

References:
(1) MIL-STD-202, Method 208.
(2) DuPont "Method of Test for wire peel adhesion of soldered thick film conductors to ceramic substrates". March 1971.

Test Number: 7

PART/COMPONENT/MATERIAL QUALIFICATION TEST

TEST NAME: Chip Adherence Strength Test	APPLICABLE PROCESSES: Chip Attach (a) Eutectic (b) Epoxy (c) Solder
Objectives: Determine adequacy of chip attach process by determining adhesion strength of chip.	
Parameters: Pull force in grams. (Min 10X force experienced in 20K G-constant acceleration.)	Test Conditions: Room ambient
Sample Size: 25 chips on one or more substrates	Test Vehicle: Mechanical sample chips on 1/2 x 1/2" to 2x2" alumina substrates, prepared with chip attach pads per standard procedure

Test Description:
A pull is exerted on the attached chip in the vertical direction by means of a suitable machine recording the force and a hook arrangement engaging a loop wire cemented to the top surface of the chip.

Test Details: (Continue on new sheet, if required)
(1) Prepare Test Boards by screening and firing chip attach pads of suitable material and size.
(2) Attach chips by process to be qualified and cure if applicable.
(3) Inspect and mark those chips not meeting criteria.
(4) Attach wire loops (ℓ-shaped) with suitable cement and cure.
(5) Pull and record separation or breaking force and mode of separation.

References:
Final Report Contract DAAB07-75-C-1367.

Test Number: 8

PART/COMPONENT/MATERIAL QUALIFICATION TEST

TEST NAME:	APPLICABLE PROCESSES:
Destructive Shear Test	Chip Attach Component Attach Substrate Attach

Objectives:

Determine adequacy of component/chip/substrate attach process by determining shear strength of same.

Parameters:	Test Conditions:
Shear force in grams	Room ambient.
Sample Size: 25 chips on one or more substrates	**Test Vehicle:** Mechanical sample chips on 1/2 x 1/2" to 2 x 2" alumina substrates, prepared with chip attach pads per standard procedures.

Test Description:

A force is exerted downward on the chip edge at an angle from 60-80 degrees from the vertical, until the chip separates from the substrates or breaks.

Test Details: (Continue on new sheet, if required)

(1) Prepare Test Boards by screening and firing chip attach pads of suitable material and size.
(2) Attach chips by process to be qualified and cure, if applicable.
(3) Inspect and mark those chips not meeting criteria.
(4) With suitable equipment and a wedge shaped tool, exert an increasing force at the chip edge at an angle of 60-80 degrees from the vertical.
(5) Record force and mode of separation when chip yields.

References:

Final Report Contract DAAB-07-75-C-1367.

Test Number:
9

PART/COMPONENT/MATERIAL QUALIFICATION TEST

TEST NAME:	APPLICABLE PROCESSES:
Infrared Thermal Test	Chip Attach

Objectives:
Determine adequacy of chip attach process by measuring thermal conductance of the attach material (surface temperature of chip).

Parameters:	Test Conditions:
Chip surface temperature	Maximum specified operating power at room ambient or at temperature extremes
Sample Size:	**Test Vehicle:**
Up to 5 devices	Certified chips mounted on substrate

Test Description:
Chip surface temperature is measured by means of an Infrared Microscope during operation at known power and known substrate temperature.

Test Details: (Continue on new sheet, if required)
(1) Prepare test boards by screening and firing chip attach pads of suitable material and size, or use existing boards.
(2) Attach chips by process to be qualified and wire bond.
(3) Apply power and temperature to base.
(4) Read difference in temperature between material adjacent to chip and chip top surface.

References:
Final Report Contract DAAB 07-75-1367.

Test Number: 10

PART/COMPONENT/MATERIAL QUALIFICATION TEST

TEST NAME:	APPLICABLE PROCESSES:
Seal Qualification Test	Package Seal

Objectives:

Determine adequacy of package sealing operation

Parameters:	Test Conditions:
Leak Rate in standard cm^3 atm/s.	Per MIL-STD-883A Method 1014

Sample Size:	Test Vehicle:
Five devices or mechanical samples.	Actual device or mechanical sample.

Test Description:

Perform sealing operation per process to be qualified. Determine if leak rate is acceptable per standard hermeticity (seal) test. Then perform Temperature Cycling and Mechanical Shock followed by repeat of the hermeticity test.

Test Details: (Continue on new sheet, if required)

(1) Seal test per MIL-STD-883A, Method 1014.1.
(2) Temperature Cycling per MIL-STD-883A, Method 1010, Cond B*.
(3) Mechanical Shock per MIL-STD-883A, Method 2002, Cond B*.
(4) Seal test per MIL-STD-883A, Method 1014.

*Suggested for most applications. Conditions may change to reflect end use requirements.

References:

MIL-STD-883A, Method 1014.

Test Number: 11

PART/COMPONENT/MATERIAL QUALIFICATION TEST

TEST NAME:	APPLICABLE PROCESSES:
Resistance Qualification Test	Thick Film Paste

Objectives:

Determine the acceptability of the electrical properties of the resistor paste material.

Parameters:	Test Conditions:
(1) Sheet Resistance (ohms/square/cm) (2) TCR--Hot and Cold (ppm/°C) (3) Drift (percent)	As described.
Sample Size: Four resistors of following suggested sizes* (mils) for each test: 20x40, 50x50, 100x50, 150x50.	**Test Vehicle:** Suitable substrate with screened and fired resistors.

Test Description:

See below.

Test Details: (Continue on new sheet, if required)

(1) Sheet Resistance and Temperature Coefficient of Resistance (TCR): Sheet resistance and TCR shall be determined on at least 4 resistors and their overglaze screened and fired per suggested production procedures. The test procedure is as follows:

(a) Lead Attachment: Attach #22 wire (0.0253 inch (0.064 cm) nominal diameter) tinned copper wire leads to each termination by dipping (two 3-second dips) in 62 Sn/36 Pb/2 Ag solder at 215-220°C using a nonactivated flux.

(b) Resistance Measurement and Calculations: Resistance and temperature coefficient of resistance.

(1) Mount the test substrates on the terminal posts of a controlled temperature chamber.
(2) Connect a digital ohm-meter to the chamber.
(3) Adjust chamber temperature to 25°C and allow 30 minutes to attain temperature equilibrium.
(4) Measure and record sheet resistance ($R_{25°C}$) of test resistors.
(5) Raise chamber temperature to 125°C and allow 30 minutes to attain temperature equilibrium.

References:

DuPont Thick Film Technology Handbook, Resistor Test Method G1.5.5.

Note: * 0.05 x 0.1, 0.127 x 0.127, 0.254 x 0.127, 0.381 x 0.127 cm respectively

(6) Measure and record resistance at 125°C.

(7) Calculate "hot" temperature coefficient of resistance (TCR) for each test wafer.

$$\text{"Hot" TCR} = \frac{R_{125°C} - R_{25°C}}{R_{25°C}} \times 10{,}000 \text{ ppm/°C}$$

(8) Cool chamber to -55°C and allow 30 minutes to attain temperature equilibrium.

(9) Measure and record resistance at -55°C.

(10) Calculate "cold" temperature coefficient of resistance.

$$\text{"Cold" TCR} = \frac{R_{-55°C} - R_{25°C}}{R_{25°C}} \times (-12{,}500) \text{ ppm/°C}$$

(2) Drift: Drift shall be performed on at least 4 resistors and their overglaze screened and fired, onto an Al_2O_3 substrate, per suggested Production procedures. Two conductors shall be added to each resistor. Four point probes shall be attached; two to a voltmeter and two to a power supply to record the current applied. The probes are not to be removed until the final measurements are made. One ampere of current is fed through the resistors and their resistance is recorded. Place the substrate into a 125°C ±3°C oven for $84^{+0.5}_{-0}$ hours with the resistors under a no load condition. Remove from oven and repeat resistance measurements as above using one ampere current. Calculate percent resistance change (drift).

Test Number: 12

PART/COMPONENT/MATERIAL QUALIFICATION TEST

TEST NAME:	APPLICABLE PROCESSES:
Dielectric Qualification Test	Dielectric Paste Substrate Fabrication (Multilevel Systems)

Objectives:
Determine acceptability of physical and electrical properties of Dielectric Paste for use as multilayer insulator and for overglaze.

Parameters:	Test Conditions:
(1) Visual (pinholes and occlusions) (2) Breakdown Voltage (min 100V sugg.) (3) Resistance to leaching by solder	As described

Sample Size:	Test Vehicle:
Four substrates (2 vendor fired, 2 qualifier fired).	1/4 x 1/4 inch capacitor made from material under test and suitable conductor on alumina substrate

Test Description:

See below.

Test Details: (Continue on new sheet, if required)

(1) Visual Examination: Visual examination shall be made using an optical microscope at minimum of 30X magnification.

(2) Breakdown Voltage: Voltage shall be applied using conventional equipment designed to perform this function.

(3) Resistance to Solder Leaching: The fired dielectric shall be fluxed and dipped in accordance with MIL-STD-202, Method 208. After the sample has been fluxed it shall be solder dipped 15 times. Visually examine per 4.5.2.

References:
MIL-STD-202, Method 208.

Test Number:
13

PART/COMPONENT/MATERIAL QUALIFICATION TEST

TEST NAME:	APPLICABLE PROCESSES:
Epoxy Qualification	Material Evaluation/Chip Attach/ Substrate Attach

Objectives:

Determine acceptability of mechanical, thermal, electrical and chemical properties of epoxy to be used in production.

Parameters:	Test Conditions:
(1) Adhesion strength in grams (2) Weight loss in percent (3) Electrical Resistivity in ohm-cm*	As described. (4) Thermal Resistance, θ_{jc}
Sample Size: (1) 5 chips or small substrates, (2) 0.1 gram or other small quantity (cured), (3) 5 strips of epoxy (cured), (4) 5 mounted chips	**Test Vehicle:** (1) Chips mounted on substrates. (2) Bulk cured epoxy. (3) Epoxy strips on substrates. (4) Chips on substrate.

Test Description:

The following four independent tests are to be performed.

(1) Adherence Strength Test (Qualification Test No. 7 in this book) after conditioning.
(2) Outgassing or thermogravimetric analysis (TGA) with optional differential thermal analysis (DTA).
(3) Electrical Resistivity
(4) Thermal Resistance

Test Details: (Continue on new sheet, if required)

(1) Prepare samples, properly cure and submit to: (Per MIL-STD-883A)
 (a) High Temperature Storage per Method 1008, Condition B.
 (b) Temperature Cycling (or Thermal Shock) per Method 1010, Cond B (Method 1011,B)
 (c) Mechanical Shock (or Constant Acceleration) per Method 2002, Cond B (Method 2001, B).

 Then perform Qualification Test No. 7 of this book.

(2) TGA involves heating a cured sample of epoxy, either in a vacuum or in an inert gas, while monitoring its weight loss (compared to a completely inert mass) by means of an electrobalance. If TGA is performed in a vacuum, mass spectrometry may be used to identify the chemical composition of the material lost by the sample at any given temperature. Calculate weight loss in percent. Recommended value: Not to exceed 1 percent at 200°C.

 If TGA is performed in an inert atmosphere, DTA may be used to identify temperatures at which chemical reactions occur. DTA involves measuring the differential temperature between the sample and the inert control while carefully heating both at the same rate. If, at some temperature, the sample undergoes an exothermic reaction, the sample temperature will rise above the control temperature.

References:

*Conductive epoxies only.

(1) RFS David, Solid State Technology, 18; 40 (1975).
(2) NASA Report P71-59.

Conversely, an endothermic reaction will cause the sample temperature to fall below the control temperature.

(3) Perform electrical resistivity measurements. Recommended limit: not to exceed 5×10^{-4} ohm-cm at 50 mA.

(4) Thermal resistance (θ_{jc}) by means of infrared microscope temperature measurements of chips mounted on BeO or copper heat sink.