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INVESTIGATION OF TECHNOLOGICAL PROBLEMS IN GaAs

Science Center
Rockwell International Corporation

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INVESTIGATION OF TECHNOLOGICAL
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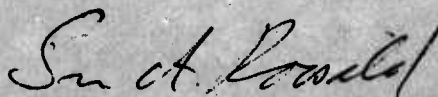
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demonstrated; resistivity of $4 \times 10^4 \Omega\text{-cm}$ was achieved in Cr-doped buffer layers by sensitive control of the bakeout temperature of the melt. Remarkable progress was made in ion implantation by demonstrating high reproducibility and uniformity of S implanted layers, and by achieving high doping efficiency in low and high dose Se implantation. FET devices made from Se implanted GaAs show negligible post-tuning drift characteristics in device noise figure compared to transistors made of LPE material. In the area of interest of IMPATT diodes, a strong dependence of the ionization rates on doping density was observed.

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1.0 INTRODUCTION

The activities described in this report are focused on basic technological problems affecting GaAs FET devices. The reason for choosing the FET as a target is that the FET is a device with great potential whose development into maturity has been hampered by serious material problems. Responding to such problems, the efforts reported here are concentrated on growth and characterization of semi-insulating GaAs and on preparation of ultra-thin device layers by liquid phase epitaxial growth and by ion implantation. FETs are fabricated and evaluated as final tests of the progress made in the areas of material development. A small effort on the study of avalanche phenomena, of interest for IMPATT diode applications, is also maintained.

The most significant accomplishments of this reporting period took place in ion implantation in which high uniformity and reproducibility of implanted profiles has been demonstrated. This result brings ion implantation into maturity as a technique for preparation of device quality layers. Measurements of noise transients on FET devices indicate that implanted layers may be superior to epitaxial layers not only in reproducibility and uniformity, but also in reducing drift problems in the devices.

2.0 HIGHLIGHTS

Highlights of the progress made in the various areas of research during the period 7-1-75 to 1-15-76 are presented. The organization of this section is the same as that of the report.

2.1 Epitaxial Material Growth and Characterization

Liquid phase epitaxial growth is carried out at Stanford University, the Science Center and Cornell University. The goal of Stanford's work is to grow high resistivity buffer layers. Emphasis of this work is on understanding the interactions between the growth system components, the melt bakeout temperature and the incorporation of impurities in the layer. Optimum growth conditions in a system in which the presence of C has been completely eliminated are reported. Resistivity as high as 4.4×10^4 ohm-cm were achieved with this system by fine control of the bakeout temperature of the melt.

The Science Center work addresses to the problem of growing ultra thin epitaxial layers. Layers grown with the "restricted melt" technique developed under this contract showed excellent uniformity and reproducibility. The typical standard deviation of thickness over 2.5cm^2 layers was 4% (for 5000Å layers). From wafer to wafer, five layers grown sequentially have an 11% standard deviation of their average thickness and 4% of the average carrier concentration.

Cornell recently started LPE growth of buffered FET structures. Their approach relies on high purity undoped buffer layers, with emphasis on developing a multilayer growth capability. Preliminary results on n-type and undoped layers are presented.

2.2 Semi-Insulating Substrate Material Growth

Crystal Specialties has a dual role supplying substrate materials for

all the activities in this program, and investigating growth of bulk semi-insulating GaAs. In this area inert gas backfill of the quartz growth ampoule was identified as responsible for degradation of crystalline quality. Improvement in yield from 32 to 58% was obtained by growing the crystals in pure As atmosphere.

2.2.1 Semi-Insulating Material Evaluation

This activity, carried out at the Science Center, covers two areas. In the first area, the study of bulk electrical properties, transport properties of samples with different Cr concentration, were compared with the Cr concentration, and analyzed in terms of models for the electrical compensation. It is shown that the "conventional" model in which deep Cr acceptors compensate residual Si donors is incorrect, and a more elaborate model which includes both a deep acceptor and a deep donor must be used. In the second area, the study of surface stability under heat treatment, preliminary results of a survey of substrate behavior and of ESCA and photoluminescence measurements are presented.

2.3 Ion Implantation

This activity is carried out in close cooperation between the Science Center and Caltech. Implantation and annealing are done at the Science Center while analysis of the implanted layers is carried out at Caltech. In sulfur implantation in semi-insulating substrates, uniformity of doping over a wafer is shown to be better than 5% in peak carrier concentration and depth. The reproducibility is also excellent. From wafer to wafer (from the same boule) the standard deviation of peak carrier concentration is 10% and the standard deviation of depth is 5%. In selenium implantation into semi-insulating GaAs, annealing with AlN caps, anneal temperatures were optimized for different doses. For low dose implants a doping efficiency of at least 75%

was achieved. Based on results of photoluminescence measurements, correlations between doping efficiency and formation of Ga vacancy-selenium complexes are discussed.

2.4 Effects of Material Properties on FET Performance

At the Science Center, $1\mu\text{m}$ Schottky barrier gate FETs were fabricated on active layers made by liquid phase epitaxy and by Se implantation. Long transients ($\tau \sim 10$ sec) were observed in the noise figure of the epitaxial transistors after changes of gate voltage. The implanted transistors showed negligible transients suggesting that transistors made on implanted layers may be less prone to post-tuning drift of their RF characteristics than transistors made on LPE layers.

2.5 Avalanche Parameters

At Cornell University, experimental measurements of the low frequency noise of IMPATT diodes have been successfully used to extract parameters like the intrinsic response time and the multiplication factors under operating conditions of the diode, which can be exploited to improve device design. Measurements of ionization rates as functions of the electric field show that the ionization rates are strongly dependent on the doping concentration. A tentative explanation based on the delay in promoting electrons to higher conduction bands before they reach enough energy to produce secondary pair generation is given.

3.0 RESULTS

3.1 Epitaxial Material Growth and Characterization

The LPE growth investigations under this contract have, over a period of time, evolved into three projects involving Stanford University, the Science Center, and Cornell University. For the benefit of the reader, a short overview of these projects, their unique approaches and goals, and their relationship to each other is given here.

Stanford's work has had, since the inception of the contract, the primary goal of growing high resistivity ($> 10^4$ ohm-cm) epitaxial layers for potential use as a substrate buffer for active device layers and for the purpose of providing well-known, characterized layers for implantation studies. Crucial to achieving this goal is an understanding of the interactions between the growth system components, the melt bakeout temperature, the chemical composition of the melt, and subsequent impurity incorporation in the layer. Based on their understanding of these interrelated factors, Stanford's approach has been to control the chemical composition of the melt through a series of systematic bakeouts at a specific temperature and to use Cr to help chemically and electrically compensate donor and acceptor species. Layers exceeding resistivities of 10^4 ohm-cm have been produced in a $\text{SiO}_2\text{-BN(C)-H}_2$ system. In this report, the results of some layers grown in a system in which the presence of C has been completely eliminated are outlined.

The Science Center's early work under this contract addressed the problems of growing ultra-thin epitaxial layers directly on GaAs semi-insulating substrates. Field Effect Transistors were used as the vehicle to access the quality of the layers, and the substrate-epitaxial layer interface. From this work evolved a novel state-of-the-art growth technique incorporating a "restricted"

January 22, 1976

melt and a vertical temperature gradient. Recent emphasis has been placed on demonstrating the uniformity and reproducibility of this method, and results are included in this report. The Science Center also undertook to produce buffer layer FETs, using Stanford's approach to obtaining high resistivity layers. However, due to the other commitments as well as a proposed multi-layer buffer FET effort at Cornell, this area of investigation has been given a lower priority. The LPE facilities at the Science Center are also involved in substrate annealing studies, and in epitaxial growth for preparation of samples for measurement of intrinsic material properties and substrate interface effects. Recently, it has been found (See Section 3.4.1) that the post tuning drift characteristics of FET devices fabricated from epitaxial material grown directly on semi-insulating substrates is inferior to those devices prepared by ion implantation. Thus, it appears that the buffer layer work at Stanford and Cornell may come to fruition as such a double layer structure would be the first logical approach in overcoming this drift problem for epitaxially prepared transistors.

Cornell University has recently become involved in the LPE program. Their goal is to grow buffered layer FET structures using approaches different from those used at both the Science Center and Stanford. As discussed in this report, active layers are grown in a more conventional manner to facilitate the incorporation of buffer layer growth. The Cornell approach for buffers is to use high purity undoped layers rather than high resistivity compensated layers as grown at Stanford.

3.1.1 LPE Activities at Stanford University - High Resistivity LPE GaAs

During the past six months, 43 LPE GaAs layers were grown in the recently constructed fused-quartz-pyrolytic boron nitride-hydrogen ($\text{SiO}_2\text{-BN-H}_2$) system and their properties were measured. It was found that for a bakeout temperature of 700°C and a hydrogen flow rate of 0.6 l/min, all layers were n-type

and had higher carrier densities ($\approx 2 \times 10^{15} \text{ cm}^{-3}$) than those layers previously grown in a $\text{SiO}_2\text{-BN(C)-H}_2$ system. The addition of chromium (Cr) to the melt had no effect on the properties of these layers. For a bakeout temperature of 800°C , the stabilized undoped melt yielded p-type layers with carrier densities in the range of $2 \times 10^{14} \text{ cm}^{-3}$ and resistivities in the range of $50 \sim 130 \text{ ohm-cm}$. When Cr was added to the melt, the layers had carrier densities ranging from 7×10^{11} to $4 \times 10^{14} \text{ cm}^{-3}$. The highest resistivity was $4.4 \times 10^4 \text{ ohm-cm}$ which is equivalent to a sheet resistance of $2.9 \times 10^7 \text{ ohm}/\square$.

Van der Pauw measurements¹ were made from 300 to 500K on three Cr-doped LPE GaAs layers (#1318, 1319, and 1619). Sample #1318 was a p-type layer grown on a Cr-doped semi-insulating substrate, #1319 was an n-type layer grown on an O_2 -doped substrate. Both layers had about the same carrier density ($\approx 6 \times 10^{13} \text{ cm}^{-3}$) and moderately high resistivities (180 ohm-cm for #1318 and 12 ohm-cm for #1319). Layer #1619 was grown on a Cr-doped substrate and has a very high resistivity ($4.4 \times 10^4 \text{ ohm-cm}$). The measurements on layer #1318 indicated a change from p-type to n-type at 420K. The measurements on layer #1319 show a sharp increase in carrier density from $6 \times 10^{13} \text{ cm}^{-3}$ at 297K to $1 \times 10^{17} \text{ cm}^{-3}$ at 470K, which is probably due to the effects of oxygen in the substrate. The temperature variation of conductivity of layer #1619 yielded an activation energy of $\approx 0.46 \text{ eV}$, which appears to be due to a deep acceptor level.

3.1.1.1 Growth Studies

In order to study the effects of only the bakeout temperature in the $\text{SiO}_2\text{-BN-H}_2$ system, all growths in the series reported here were made with the following growth conditions held constant: bakeout period, 15 hours; H_2 flow rate, 0.6 l/min ; growth temperature, 700°C ; and cooling rate, 4.5°C/min . For the first 11 growths, Table 3.1-1, the melt was baked out at 700°C before each

growth. No intentional doping was added. All of these layers were n-type with carrier densities in the range of $2 \times 10^{15} \text{ cm}^{-3}$ and $N_A/N_D \approx 0.7$. The 1500 series was then continued for 11 additional growths after 0.5 atomic % Cr had been added to the same melt (Table 3.1-2). The first three layers (#1506 to #1508) were grown after the melt had been baked at 700°C and they showed no change in their electrical properties. When the same melt was baked at 800°C , the layers (#1509 to #1512) had lower carrier densities ($\approx 5 \times 10^{14} \text{ cm}^{-3}$) with $N_A/N_D \approx 0.85$. One of the layers (#1511) was p-type but the next growth (#1512) became n-type again. The Cr-doped melt was then baked at 750°C and 4 additional growths were made (#1513 to #1516). These layers were n-type with carrier densities in the range of $5 \times 10^{14} \text{ cm}^{-3}$ and $N_A/N_D \approx 0.8$.

A new melt was prepared for the 1600 series of growths. The bakeout temperature was 800°C . For the first 10 growths, Table 3.1-3, no intentional dopants were added to the melt. After 75 hours of accumulated bakeouts, the undoped melt tended to stabilize and the layers grown thereafter were p-type with carrier densities in the range of $2 \times 10^{14} \text{ cm}^{-3}$. The resistivities of these layers ranged from 50 ohm-cm to 130 ohm-cm. Therefore, it appears that the bakeout transition temperature of the $\text{SiO}_2\text{-BN-H}_2$ system is $\lesssim 800^\circ\text{C}$. After 0.5 atomic % of Cr was added to the same melt, 12 layers were grown as shown in Table 3.1-4. Among these growths, 7 layers were n-type, which may be due to the introduction of donor impurities in the Cr. As the accumulated bakeout period increased, the electron densities decreased from $3 \times 10^{14} \text{ cm}^{-3}$ (#1611) to $\sim 5 \times 10^{13} \text{ cm}^{-3}$ (#1618). The following growth (#1619) yielded a semi-insulating layer with a room temperature resistivity of 4.4×10^4 ohm-cm and carrier density of $7.3 \times 10^{13} \text{ cm}^{-3}$. However, two additional growths (#1620 and #1621) yield layers that were p-type with carrier densities of $\approx 3 \times 10^{14} \text{ cm}^{-3}$. With a shorter bakeout period of 10

TABLE 3.1-1

PROPERTIES OF UNDOPED EPITAXIAL GaAs LAYERS GROWN IN A SiO_2 -BN- H_2 SYSTEM
GROWTH SERIES 1400 AND 1500

Growth Conditions: Bakeout Temperature: 700°C ; Bakeout Period: 15 hours
Growth Temperature: 700°C ; Cooling Rate: $4.5^\circ\text{C}/\text{min}$.
 H_2 Flow Rate: $0.6 \text{ l}/\text{min}$.

Growth No.	Mobilities @ $300/77^\circ\text{K}$ ($\text{cm}^2/\text{V}\text{-sec}$)	Carrier Densities @ $300/77^\circ\text{K}$ (cm^{-3})	Resistivity @ 300°K (ohm-cm)	Conductivity Type
1401	8,000/29,000	$2.0/1.6 \times 10^{15}$	0.4	n
1402	6,000/24,000	$3.6/2.8 \times 10^{15}$	0.3	n
1403	6,900/35,000	$2.2/1.8 \times 10^{15}$	0.4	n
1404	6,500/35,000	$2.0/1.7 \times 10^{15}$	0.5	n
1405	8,100/53,000	$9.7/9.0 \times 10^{14}$	0.8	n
1406	6,500/42,000	$1.1/1.1 \times 10^{15}$	0.8	n
1501	6,500/42,000	$2.1/1.6 \times 10^{15}$	0.5	n
1502	6,900/47,000	$1.0/0.9 \times 10^{15}$	0.9	n
1503	6,400/41,000	$1.4/1.2 \times 10^{15}$	0.7	n
1504	6,500/44,000	$1.3/1.2 \times 10^{15}$	0.8	n
1505	5,200/33,000	$1.8/1.4 \times 10^{15}$	0.7	n

TABLE 3.1-2

PROPERTIES OF Cr-DOPED EPITAXIAL GaAs LAYERS GROWN IN A SiO_2 -BN- H_2 SYSTEM
GROWTH SERIES 1500

Growth Conditions: Bakeout Period: 15 hours; Growth Temperature: 700°C
Cooling Rate: 4.5°C/min; H_2 Flow Rate: 0.6 l/min.
Dopant: Cr (0.5 atm. %)

Growth No.	Bakeout Temp. (°C)	Mobilities @ 300/77°K ($\text{cm}^2/\text{V-sec}$)	Carrier Densities @ 300/77°K (cm^{-3})	Resistivity @ 300°K (ohm-cm)	Conductivity Type
1506	700	6,300/41,000	$2.0/1.7 \times 10^{15}$	0.5	n
1507	700	6,600/34,000	$3.3/2.8 \times 10^{15}$	0.3	n
1508	700	6,600/49,000	$1.5/1.3 \times 10^{15}$	0.7	n
1509	800	5,000/24,000	$2.3/1.9 \times 10^{15}$	0.6	n
1510	800	5,100/32,000	$3.0/2.8 \times 10^{14}$	4.0	n
1511	800	260/ -	$5.5 \times 10^{14} / -$	43	p
1512	800	5,300/33,000	$5.5/5.1 \times 10^{14}$	2.1	n
1513	750	7,200/38,000	$4.9/4.4 \times 10^{14}$	1.8	n
1514	750	7,100/39,000	$4.3/3.8 \times 10^{14}$	2.0	n
1515	750	6,900/52,000	$5.2/5.0 \times 10^{14}$	1.8	n
1516	750	(Grown on p+ substrate)			n

TABLE 3.1-3

PROPERTIES OF UNDOPED EPITAXIAL GaAs LAYERS GROWN IN A SiO_2 -BN- H_2 SYSTEM
GROWTH SERIES 1600

Growth Conditions: Bakeout Temperature: 800°C ; Bakeout Period: 15 hours
Growth Temperature: 700°C ; Cooling Rate: $4.5^\circ\text{C}/\text{min}$.
 H_2 Flow Rate: $0.6 \text{ l}/\text{min}$.

Growth No.	Mobilities @ $300/77^\circ\text{K}$ ($\text{cm}^2/\text{V}\cdot\text{sec}$)	Carrier Densities @ $300/77^\circ\text{K}$ (cm^{-3})	Resistivity @ 300°K (ohm-cm)	Conductivity Type
1601	6,200/46,000	$6.4/3.9 \times 10^{14}$	1.6	n
1602	6,400/48,000	$5.7/4.0 \times 10^{14}$	1.7	n
1603	6,700/50,000	$7.2/5.4 \times 10^{13}$	13	n
1604	450/10,400	$2.6/2.4 \times 10^{14}$	53	p
1605	7,400/66,000	$8.5/7.8 \times 10^{13}$	10	n
1607	350/5,800	$3.6/3.2 \times 10^{14}$	50	p
1608	370/7,200	$2.1/1.0 \times 10^{14}$	82	p
1609	On n^+ substrate			p
1610	270/5,600	$1.9 \times 10^{14} / 8.3 \times 10^{13}$	130	p

TABLE 3.1-4
 PROPERTIES OF Cr-DOPED EPITAXIAL GaAs LAYERS GROWN IN A SiO_2 -BN- H_2 SYSTEM
 GROWTH SERIES 1600

Growth Conditions: Bakeout Temperature: 800°C ; Bakeout Period: 15 hours
 Growth Temperature: 700°C ; Cooling Rate: $4.5^\circ\text{C}/\text{min}$.
 H_2 Flow Rate: $0.6 \text{ l}/\text{min}$; Dopant: Cr (0.5 atm %)

Growth No.	Mobilities @ $300/77^\circ\text{K}$ ($\text{cm}^2/\text{V}\text{-sec}$)	Carrier Densities @ $300/77^\circ\text{K}$ (cm^{-3})	Resistivity @ 300°K (ohm-cm)	Conductivity Type
1611	6,300/68,000	$3.1/3.0 \times 10^{14}$	3.2	n
1612	5,500/81,000	$6.3/6.7 \times 10^{13}$	18	n
1613	410/ -	4.2×10^{14} / -	37	p
1614	7,300/ -	2.2×10^{14} / -	3.9	n
1615	320/ -	2.0×10^{14} / -	95	p
1616	6,400/74,000	$4.7/5.4 \times 10^{13}$	21	n
1617	7,700/75,000	$3.9/4.0 \times 10^{13}$	21	n
1618	7,400/79,000	$5.0/6.9 \times 10^{13}$	17	n
1619	200/ -	7.3×10^{11} / -	4.4×10^4	n
1620	460/ -	3.9×10^{14} / -	35	p
1621	420/ -	2.8×10^{14} / -	53	p
1622	390/ -	3.6×10^{13} / -	390	p

hours, the following growth (#1622) was a p-type layer and had a hole density about one order of magnitude less than the previous two growths ($3.6 \times 10^{13} \text{ cm}^{-3}$) and a resistivity of 390 ohm-cm with a sheet resistance of $\approx 2 \times 10^5 \text{ ohm}/\square$. This suggests that the bakeout period is very critical at this bakeout temperature if semi-insulating layers are to be grown reproducibly. In the 1600 series, all the n-type layers grown from the Cr-doped melt had higher carrier densities at 77K at 300K. This phenomenon was not observed for n-type layers grown from the undoped melt in the same series. The reason is not clear at this stage, however, it may be due to deep traps introduced by the Cr-doped melt in which the trapping of electrons are more efficient at 300K than at 77K.

3.1.1.2 Temperature Dependent Hall Effect Measurements

Van der Pauw measurements were made on layer #1318, grown from a Cr-doped melt on a Cr-doped semi-insulating substrate. The melt was baked out in the $\text{SiO}_2\text{-BN(C)-H}_2$ system at 700°C , the transition temperature for this system. At 300K the measurements showed that the sign of Hall coefficient, R_H , was positive (p-type). The carrier density was $6 \times 10^{13} \text{ cm}^{-3}$, assuming that $p \gg n$, the Hall mobility was $570 \text{ cm}^2/\text{Vsec}$ and the resistivity was 180 ohm-cm. The measurements were then made as a function of temperature from 300 to 600K (Fig. 3.1.1). For $T < 413\text{K}$, R_H became negative (n-type) and $|R_H|$ increased rapidly until $T \approx 500\text{K}$ where the layer became intrinsic. The Hall mobility decreased from $570 \text{ cm}^2/\text{Vsec}$ at 300K to $20 \text{ cm}^2/\text{Vsec}$ at 423K and then increased as T increased. These results suggest that the transport properties can be explained by a mixed model.² Further investigation will be carried out in the near future.

Layer #1319 was grown on an oxygen-doped semi-insulating GaAs sub-

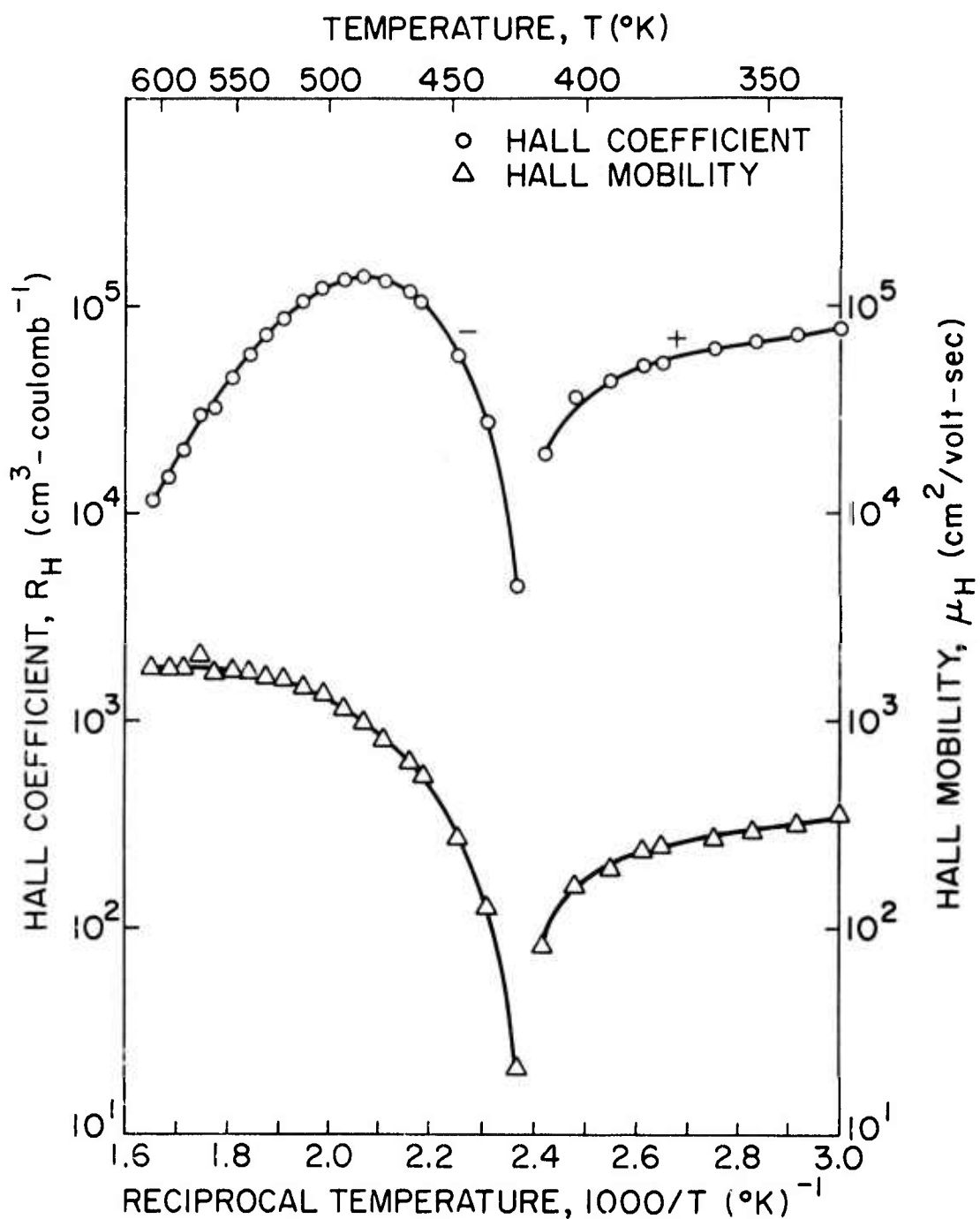


FIG. 3.1.1 Hall coefficient and Hall mobility variation with temperature for Cr-doped GaAs epi layer #1318.

strate under the same conditions. Van der Pauw measurements were made on this n-type layer from 300 to 500K. At 300K the electron density was $6 \times 10^{13} \text{ cm}^{-3}$. Above 370K the electron density increased rapidly and became $1 \times 10^{17} \text{ cm}^{-3}$ at 450K (see Fig. 3.1.2). The measurements showed no hysteresis with temperature. The activation energy calculated from the slope of $\log (RT^{3/2})$ vs. $1/T$ was ≈ 1.7 eV. This anomalously large activation energy is due to the combined changes in properties of the layer and the substrate. In this temperature range, the resistivity of the O_2 -doped substrate decreases. Further measurements will be carried out on O_2 -doped semi-insulating substrates to justify this explanation.

Semi-insulating layer #1619 was grown in a Cr-doped melt on a Cr-doped semi-insulating substrate. The melt was baked out at 800°C in the $\text{SiO}_2\text{-BN-H}_2$ system. Van der Pauw measurements on this layer were very difficult due to surface leakage problems. However, we found that the surface conductivity could be reduced by heating the sample above 150°C in a good vacuum ($< 10^{-4} \text{ mm Hg}$) and making the measurements with the sample in vacuum. At room temperature, the resistivity of this semi-insulating layer was $4.4 \times 10^4 \text{ ohm-cm}$ and the carrier density was $7.1 \times 10^{11} \text{ cm}^{-3}$. However, the actual resistivity may be larger than this value since the resistance of the semi-insulating substrate, due to its relatively large thickness (about 30 times larger than the thickness of the epitaxial layer) strongly influences the measured resistivity value. If we take the resistance of the substrate into account, assuming that the resistivities of both the layer and the substrate are the same, then the resistivity of the layer is $\sim 1 \times 10^6 \text{ ohm-cm}$. By coincidence, this is approximately the resistivity of the substrate. Therefore, we can assume that the resistivity of the layer is approximately $1 \times 10^6 \text{ ohm-cm}$. Van der Pauw measurements were attempted on this layer in the temperature range from 300 to 440K but the results were not

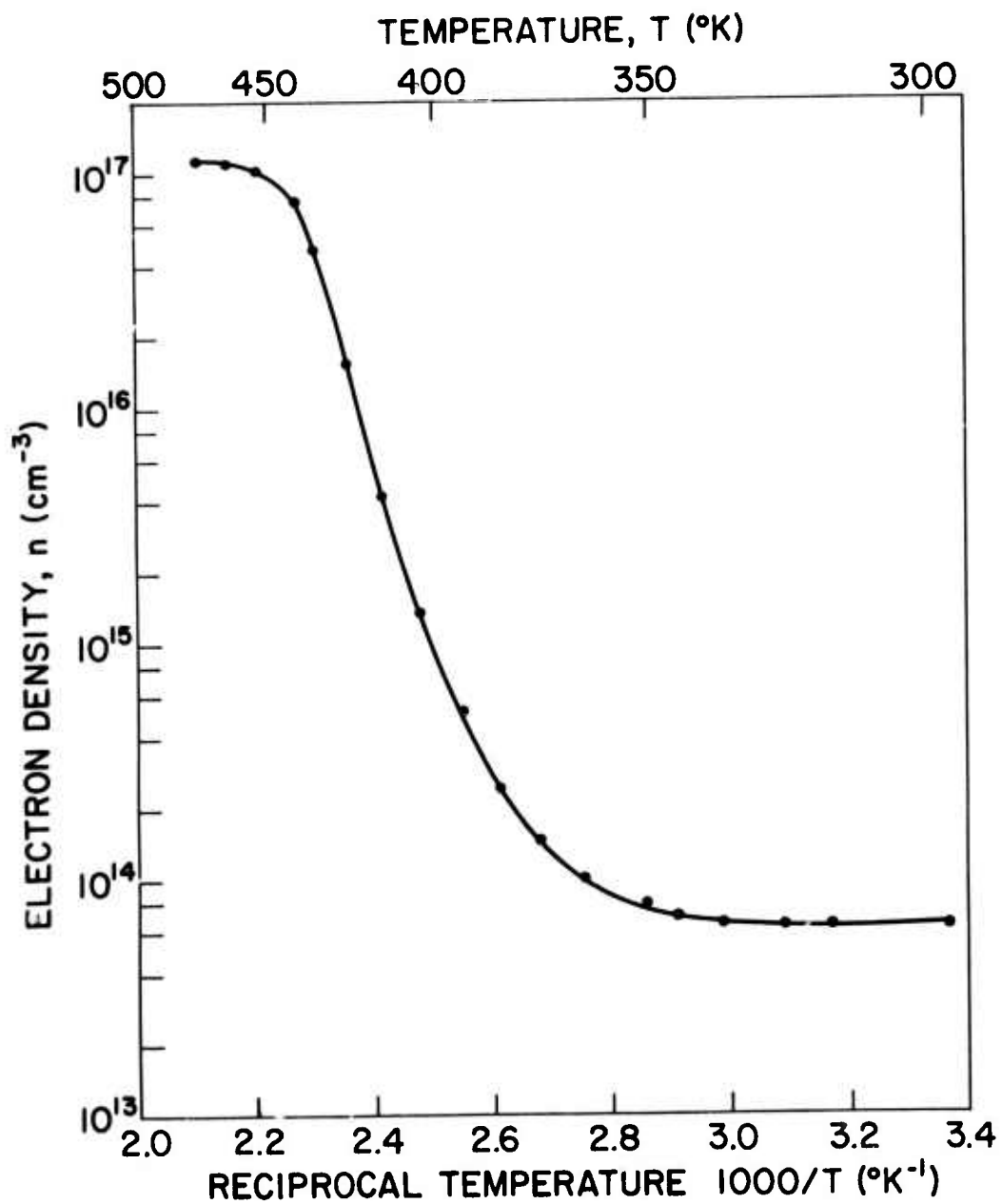


FIG. 3.1.2 Electron density variation with temperature for Cr-doped GaAs epitaxial layer #1319.

accurate. The conductivity increased from $2.1 \times 10^{-5} \text{ (ohm-cm)}^{-1}$ at 300K to $1.5 \times 10^{-4} \text{ (ohm-cm)}^{-1}$ at 440K (see Fig. 3.1.3). The activation energy estimated from the straight line portion of this plot (400-440K) was 0.46 eV. The precise energy level of the deep impurity may differ from this value since the effects of the semi-insulating substrate were not taken into account.

3.1.2 LPE Activities at the Science Center. Restricted Melt-Temperature Gradient Growth Method

At the Science Center, a continuing development program has been underway to improve the uniformity and reproducibility of ultra-thin GaAs LPE epitaxial layer growth. Early work under this contract resulted in a novel state-of-the-art technique incorporating a "restricted" melt and a vertical temperature gradient. In this scheme, (Fig. 3.1.4) the As saturated Ga melt is confined to a thickness on the order of 1mm by a GaAs "slab" or roof. This limits the total amount of As available with respect to "semi-infinite" or thick melts, insures that the solution remains saturated, and greatly reduces convection currents in the melt resulting in a lower, more uniform growth rate. The vertical temperature gradient created by imposition of nitrogen gas below the graphite platform greatly enhances nucleation density resulting in thin, smooth layers with a minimum of undercooling.

This growth technique initially gave excellent results, but the repeatability was less than optimum. While there was some evidence indicating that substrates from different sources effected the growth rate differently, we now believe these effects, if they exist, are of second order with respect to such factors as crystal preparation, orientation, and the precise thermal conditions in a growth cycle. It was felt that one cause of the thickness repeatability problem was the existance of lateral temperature gradients which formed

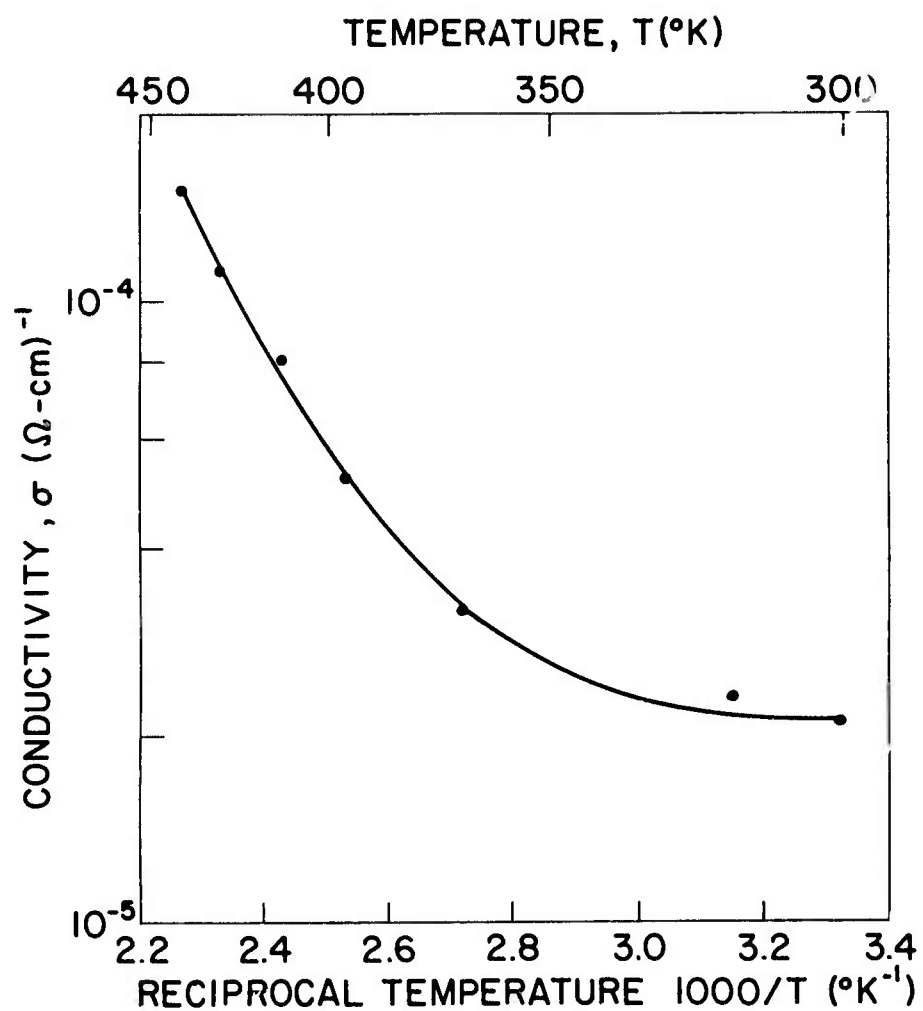


FIG. 3.1.3 Conductivity variation with temperature for Cr-doped semi-insulating GaAs epitaxial layer #1619.

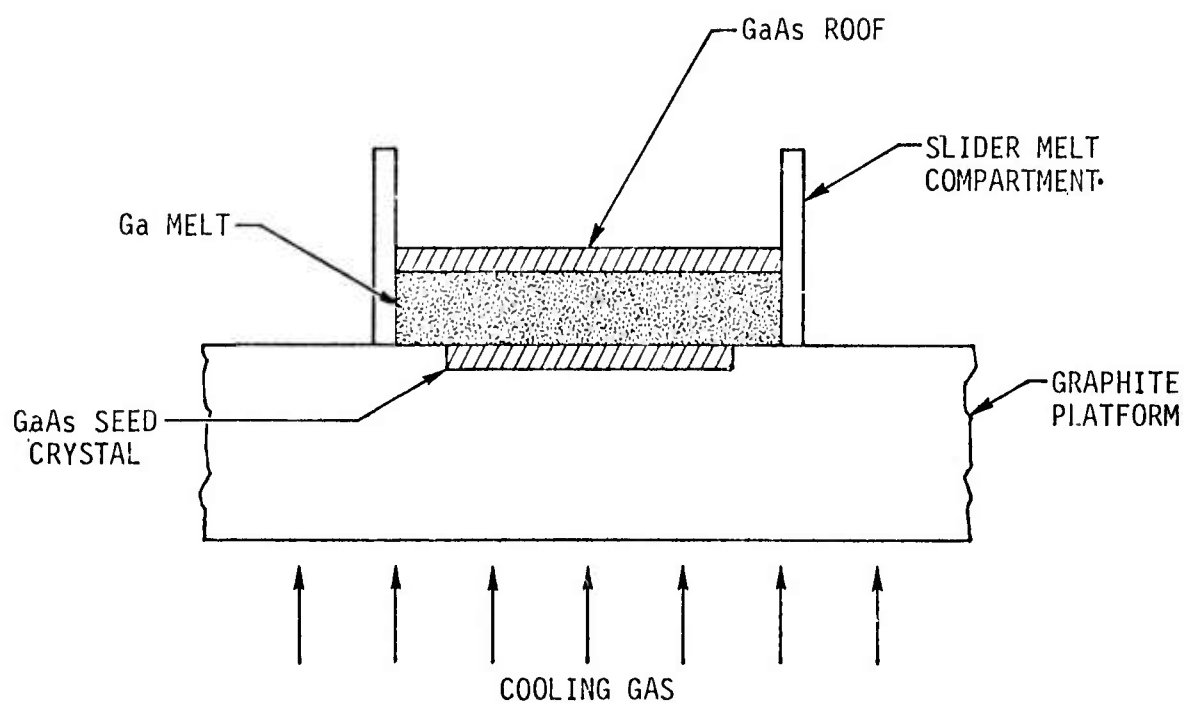


FIG. 3.1.4 Schematic representation of the restricted melt.

in the melt at the onset of the intentionally imposed vertical gradient. To circumvent this problem, several changes were made in the growth system.

We regard boat design as a highly important factor to the success of growing thin, uniform epitaxial layers with good surface morphology. Shown in Fig. 3.1.5 is an exploded view of our most recent design. The boat consists of a thick graphite slab with a substrate recess, and a three compartment slider which is held to the slab with graphite rails. The center compartment of the slider contains a plug which resides over the slice during the saturation period, presenting a thermal mass to the GaAs surface which more closely approximates the thermal conditions at the beginning of growth. The two melt compartments were flexibly designed to allow either restricted (thin) or unrestricted (semi-infinite) melts. These compartments have a lateral cross-section which is considerably larger than the substrate area. We have found this to be an effective means to prevent edge buildup of epitaxial material which interferes with device photolithographic processing, as well as giving uniform layer thickness to the periphery of the wafer edge. Both melts are provided with a graphite cover to prevent the tendency of Ga to "ball" due to increased surface tension at elevated temperatures. Our observations of epitaxial growth from unrestricted melts in transparent furnaces led us to the conclusion that, for large area melts, such a cover is necessary to prevent nucleation stripes which result from the unsupported melt "wiggling" like a blob of "Jello" on a flat plate. Auxiliary scrapers are provided to aid in wiping any residual Ga melt remaining on the slice.

When assembled in the growth system, a quartz cooling box extends under the entire graphite platform. The intent was to present, as far as possible, a uniform path for heat flow from top to bottom while maintaining

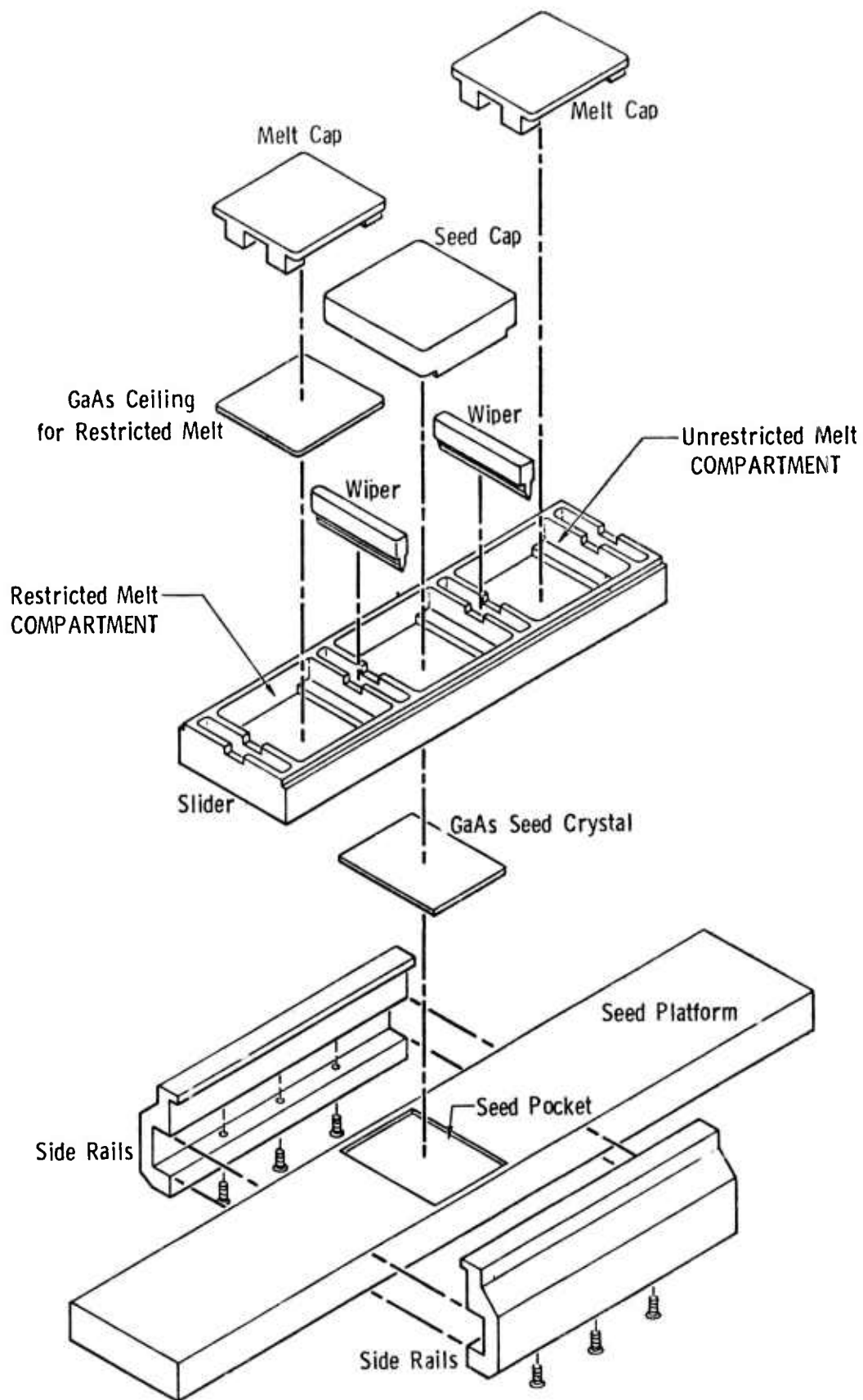


FIG. 3.1.5 Exploded view of LPE GaAs boat incorporating a restricted and unrestricted melt.

uniform lateral temperatures. To enhance this latter aspect, an anisotropic slab of graphite with high lateral thermal conductivity was tested. This, however, greatly decreased the available vertical temperature gradient due to its ten times lower thermal conductivity in the vertical direction as compared to normal isotropic graphite. Thus, its use has been very limited.

In initial LPE growths under this contract, a growth temperature of 675°C was chosen to give a slow growth rate ($\sim 0.25\mu\text{m}/\text{min}$). However, our subsequent experience has suggested that in the vicinity of this and lower temperatures, hot H_2 is not as effective in completely removing the small amounts of residual oxides which inevitably form on GaAs during brief exposures to air even after final cleaning in hot HCl . This had intermittently led to nucleation problems and affected thickness reproducibility. More recently, growths were performed at 775°C to be compatible with buffer layer growths, but resulted x3 higher growth rates.³ For the single-layer epitaxial growth reported here, a more optimum temperature of 725°C was chosen. This temperature gives a reasonable growth rate with excellent surface morphology.

In order to demonstrate the uniformity and reproducibility of LPE growths in this new system, a series of five epitaxial layers were grown in succession with all growth parameters held constant. (One exception, layer F8J51, had a shorter growth time and thus, is not shown in the following data.) The morphology was excellent having mirror like surfaces which were essentially featureless under high magnification. A critical test routinely performed at the Science Center is to measure the doping profile, by standard C-V techniques, at the center and the extreme four corners of the substrate. These results are shown in Table 3.1-5. This test normally gives a slightly pessimistic evaluation of the uniformity, as the wafer corners are not necessarily representative of the average characteris-

Table 3.1-5 Data from Five LPE Layers Grown Under Identical Conditions

Run No.	Carrier Concentration N_D (cm^{-3})	Thickness t (μm)	$N_D t$ Product (cm^{-2})
F8J50	$6.8 (.2) \times 10^{16}$	.46 (.04)	$3.1 (.3) \times 10^{12}$
F8J52	$6.3 (.2) \times 10^{16}$	.46 (.05)	$2.7 (.2) \times 10^{12}$
F8J53	$6.1 (.2) \times 10^{16}$	.51 (.05)	$3.1 (.4) \times 10^{12}$
F8J54	$5.7 (.1) \times 10^{16}$	.54 (.05)	$3.1 (.3) \times 10^{12}$
F8J55	$6.1 (.1) \times 10^{16}$	.48 (.02)	$3.0 (.2) \times 10^{12}$
Average of the Means	6.2×10^{16}	.49	3.0×10^{12}
Standard Deviation	0.4×10^{16}	.03	0.2×10^{12}

NOTES: 1. Data are derived from capacitance - voltage measurements and represent the averages of five points measured at the center and four corners of the wafer. Standard deviations are given in parenthesis.

2. Wafer area $\sim 2.5 \text{ cm}^2$

tics across a given slice. Nevertheless, the results are quite good, showing a worst case percent standard deviation in thickness of 11% with the carrier concentration deviation of 4% within the estimated precision of the measurement. A more realistic statistical evaluation of the thickness uniformity of one of these layers, F8J53, measured at 52 points equally spaced over the entire surface of the 2.5cm^2 wafer, is given in the histogram of Fig. 3.1.6. As expected, the results are much better, giving a standard deviation in thickness of under $200\text{\AA}$. Reproducibility of t and N_D from run to run is better than 10% as given by the average of the mean data from each wafer in Table 3.1-5.

To put this data in perspective for FET applications, the product of the carrier concentration and thickness is also shown in Table 3.1-5. The $N_D t$ product is a better material property to monitor than either N_D or t as it is related to the saturation current density in an FET device. The product is also less sensitive to certain systematic errors in the C-V measurement from slice to slice, which tend to move the apparent t and N_D results in opposite directions. The uniformity of $N_D t$ over single wafers is on the order of 6 to 12% while the average characteristics are reproducible to within 6%. These results represent a significant advancement in the technology of GaAs crystal growth. To our knowledge, the uniformity and reproducibility of these sub-micron thick layers has not been equaled in any reported literature on liquid phase epitaxy.

3.1.3 LPE Activities at Cornell University. Ultra-thin Epitaxial Layers and Buffer Layers

3.1.3.1 Surface Morphology

The dominant problems associated with submicron thick epitaxial layers are the thickness uniformity and the reproducibility which are common to both LPE

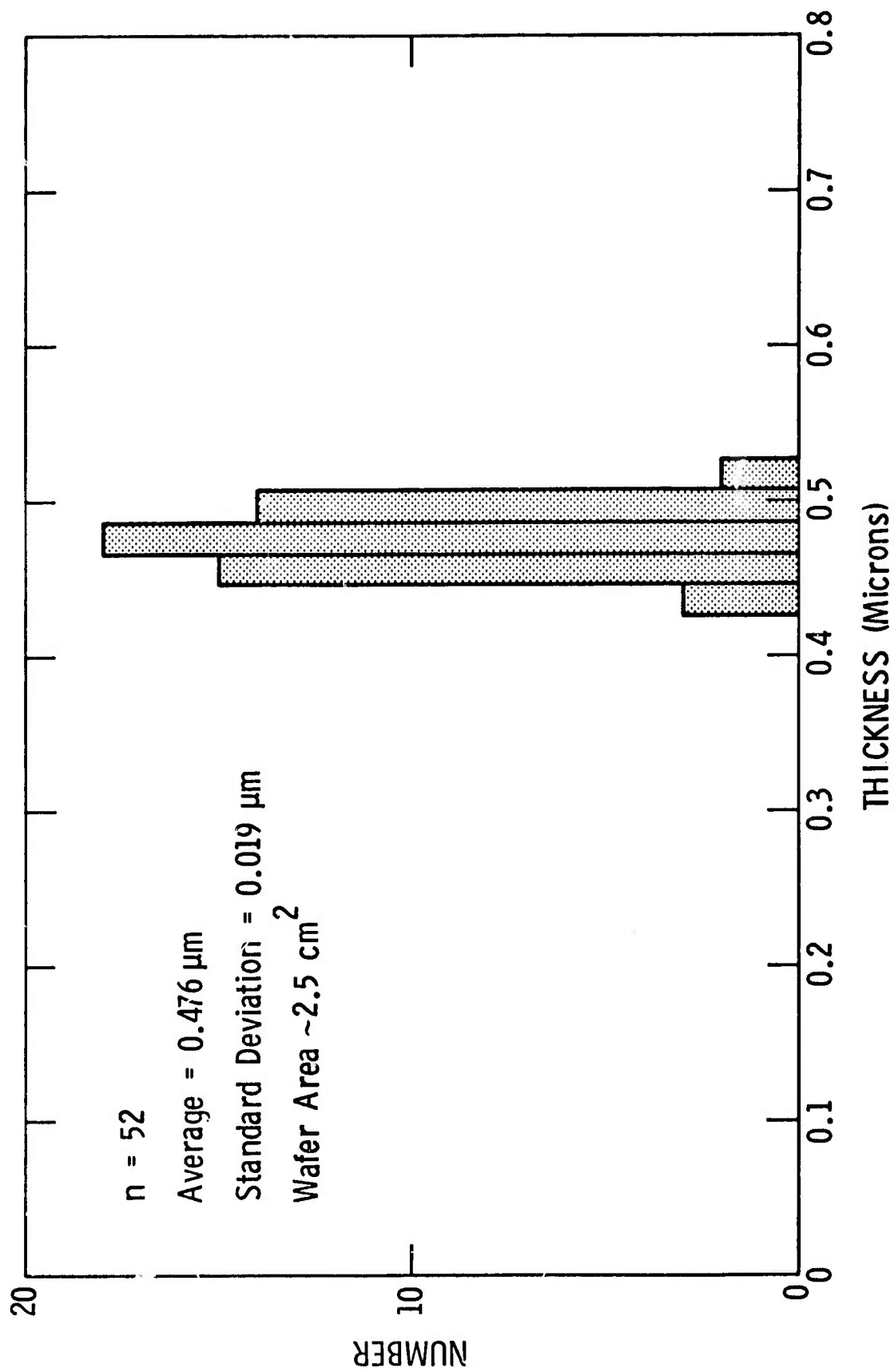
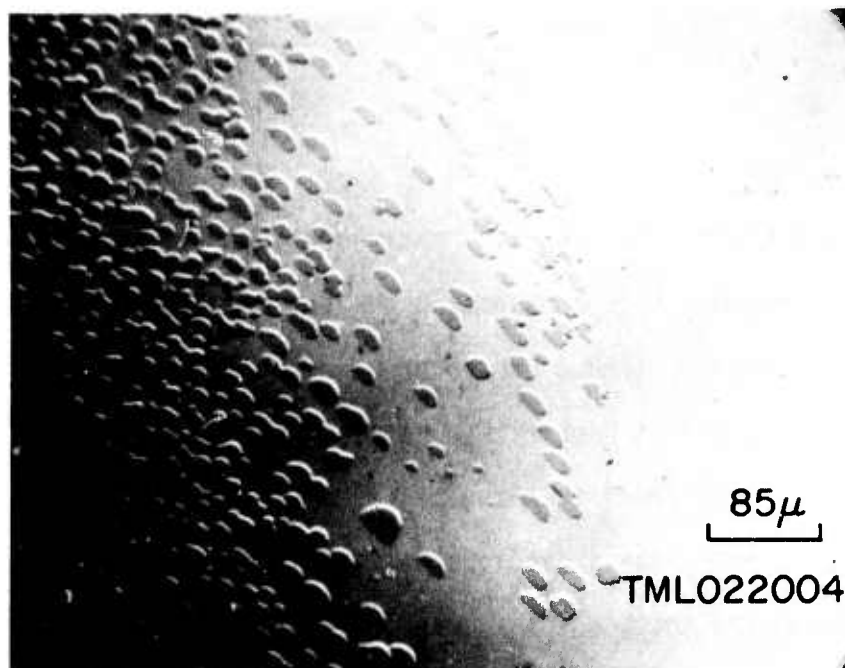


FIG. 3.1.6 Histogram of the thickness of a typical LPE GaAs wafer.

and Vapor Phase Epitaxy (VPE) techniques. It will be shown that in the case of LPE, these problems are predominantly caused by nonuniform wetting, which can be overcome by techniques to be described. Nonsimultaneous wetting, in the very beginning moments of growth, which is, in general, caused by a residual or deposited oxide layer on the surface of the substrate, results in nonuniform layer thickness. In our experiments oxide layer formation is prevented by making the system vacuum tight and limiting the water vapor content in the reactor. Any native oxide and surface impurities present are imbedded in an intentionally grown porous oxide layer and are removed when it is stripped off with 50% aqueous HCl. Cl in a surface layer, along with a small remaining amount of oxygen, are easily removed in the hot hydrogen in the furnace.

Barrera⁴ has indicated that he achieved better wetting with the reactor leak tight, and he concluded that in a leaky reactor, oxide deposition on the substrate surface prior to epi-layer deposition was the prime wetting problem. The second important aspect related to the oxide layer is that the native oxide and the remaining organic impurities should be removed and replaced by a layer more easily removed at lower furnace temperature in hydrogen. The etch in 5:1:1 for four minutes removes approximately 4 μ m of material from each side to assure that minor work damage from polishing is eliminated. We have observed that this etch leaves a thin oxide layer (about 30-40Å) and does not remove some organic based impurities. Experiments at 735°C, 750°C and 780°C have been carried out to investigate the initial growth phase and the degree of wetting. Figure 3.1.7(a) shows a layer grown for a very short time at 735°C on a substrate which had undergone the earlier standard cleaning process. Supercooling of 1/4°C was applied to initiate a downward temperature ramp and the substrate was quickly slid under the melt, being kept there for 5 sec. while the slope of the ramp cooling was main-

FIG. 3.1.7 (a)



Photomicrograph (Nomarski phase contrast) of a layer grown at 735°C on a substrate which had undergone only a standard cleaning procedure. Growth time $t = 5$ sec; linear cooling $\alpha = 1^{\circ}\text{C}/\text{min}$, supercooling $1/4^{\circ}\text{C}$. Notice the formation of nucleated growth centers and nonuniform wetting.

FIG. 3.1.7 (b)



Photomicrograph (Nomarski phase contrast) of a layer grown at 735°C on a substrate that had undergone a porous oxide-HCl treatment in addition to standard cleaning. Growth parameters were unchanged from that shown in 3.1.7(a). The improvement in the wetting is remarkable.

tained at $1^{\circ}\text{C}/\text{min}$. It is clear that the growth was only initiated on small islands; moreover, this photographs the region of highest density of these nucleation centers. There was no growth at all on most of the substrate. The wetting was better at higher temperatures, but was worse at lower temperatures.

We have found that the best results are achieved by growing an approximately $150\text{\AA}$ amorphous and porous oxide layer in room temperature DI water for 20 minutes. The thickness has been measured from the step height using a Taly-step. The same thickness can be obtained in warm water in a shorter period of time. However, precaution must be taken as the oxide layer tends to become polycrystalline at higher temperatures and cannot be easily and uniformly removed in HCl.

The stripping process, which uses 50% aqueous HCl for a minimum of 5 minutes, not only removes the freshly grown porous oxide layer but also removes any residual native oxide along with much of the organic impurities on the outer surface. A very quick DI water rinse is applied and the substrate is loaded into the reactor after the water is blown off with high purity gaseous nitrogen. The substrate is not exposed to air for more than about 10 sec because new native oxide tends to grow quickly.

Experiments similar to those described earlier have been carried out to study the early growth phase and, therefore, the effect of HCl treatment. In Fig. 3.1.7 (b) a photomicrograph of a layer grown at 735°C on a substrate which had gone through porous oxide-HCl treatment is shown with the obvious improvement.

3.1.3.2 As Profile, Growth Rate and Layer Thickness

In the growth of thick layers such as Gunn diode layers, a deviation of about $\pm 1\text{--}2^{\circ}\text{C}$ in the saturation of the melt with As will have a small effect on the final layer thickness since a total temperature drop of around 20°C takes

place. By contrast, for the growth of submicron ($0.2\mu\text{m}$) epilayers, the total temperature drop can be as low as 1.5°C , (780°C , with cooling rate $\alpha = 1^\circ\text{C}/\text{min}$, supercooling $\Delta T = 0$). Therefore, it is clear that one cannot afford any under or oversaturation of the melt. Only when a "source-seed" crystal has been under the melt for an hour or more can one achieve repeatable thicknesses by controlling the growth rate on oxide-free substrates.

The growth rate is the other mechanism that is of vital consequence to the parameters of the grown layer. Submicron layers with thicknesses of about $0.2\mu\text{m}$ have been grown at temperatures of 780°C , 750°C , 735°C and 700°C . The ramp cooling rate was in all cases $\alpha = 1^\circ\text{C}/\text{min}$ and in certain cases, supercooling of $\Delta T = 3^\circ\text{C}$ was applied. Our experiments show that with high growth rate, control over the thickness repeatability becomes poorer. Moreover, surface imperfections, such as cusps and terraces, become more pronounced. Growth rates as high as $8000\text{\AA}/\text{min}$ and as low as $100\text{\AA}/\text{min}$ have been employed to grow about $0.2\mu\text{m}$ active layers. In the case of $8000\text{\AA}/\text{min}$ growth rates, terracing, meniscus lines, severe edge buildup and cusps have been observed. On the other hand, $100\text{\AA}/\text{min}$ growth rates have yielded a much smoother surface with almost no edge buildup, terracing, and lines; but, the density of cusps has increased remarkably. Our observations indicate that the best surfaces with the least surface features can only be achieved when the rate is kept within $800\text{--}1000\text{\AA}/\text{min}$ for submicron layers. However, this does not hold for layers with a thickness of more than $5\mu\text{m}$.

These phenomena can be explained by examining the As concentration profile, the slope of which, at the substrate-solution interface, determines the growth rate. In Fig. 3.1.8 is a set of calculated As profiles vs. segment number (distance) at 735°C . Curve b shows the As profile at the end of a $0.2\mu\text{m}$ layer growth when a supercooling of 3°C was applied. The As profile at the beginning

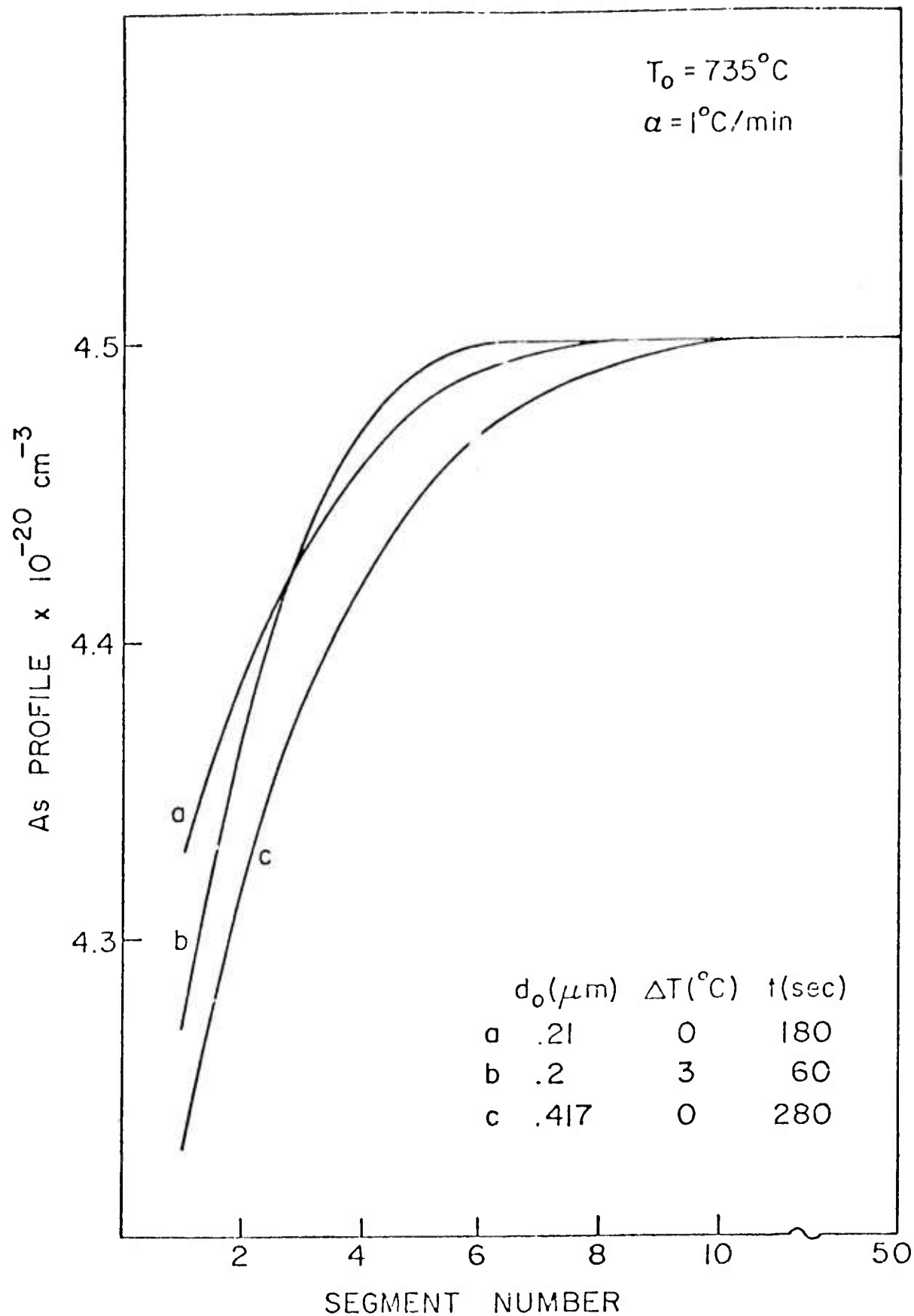


FIG. 3.1.8 Calculated As profile at 735°C as a function of position (segment number) in the end of growth.

of the growth is extremely steep and is still quite steep at the end of growth. Shown as Curve a in Fig. 3.1.8 is the As profile at the end of the growth of the first $0.2\mu\text{m}$ thick layer on the "source-seed" with no supercooling. The profile is not steep even during early growth because there is no sudden excess As concentration. Shown as Curve c in Fig. 3.1.8 is the As profile at the end of the $0.2\mu\text{m}$ layer grown on the main substrate (as opposed to the beginning profile, Curve a). It is clear that the As profile follows a very nice and controllable variation from the beginning to the end.

Fig. 3.1.9 shows the calculated growth rate versus time at 735°C for 3°C supercooling with a cooling ramp, and with only the cooling ramp.

Fig. 3.1.10 shows the computed thickness versus growth time for the condition of Fig. 3.1.9. In addition, the measured thicknesses, determined by a standard C-V profiling technique, are also shown.

3.1.3.3 High Purity Buffer Layers

An investigation has been commenced to determine the feasibility of growing buffer layers from undoped melts for FET devices. Single layers with thicknesses ranging from 5 to $15\mu\text{m}$ have been grown at 750°C , 735°C , 700°C , and 665°C on Crystal Specialties, Laser Diode, and Texas Materials substrates to investigate the behavior of background impurities with both baking and growth temperatures. It has been observed that there is a strong correlation between the total background carrier concentration and baking time (and also growth temperature) unlike what Mattes et al⁵ reported.

Shown in Fig. 3.1.11 is a set of curves showing the dependence of total ionized carrier concentration on this "between-run" baking time. In selecting baking time between the runs, no particular pattern has been followed. The data points for each curve corresponding to a particular baking and growth

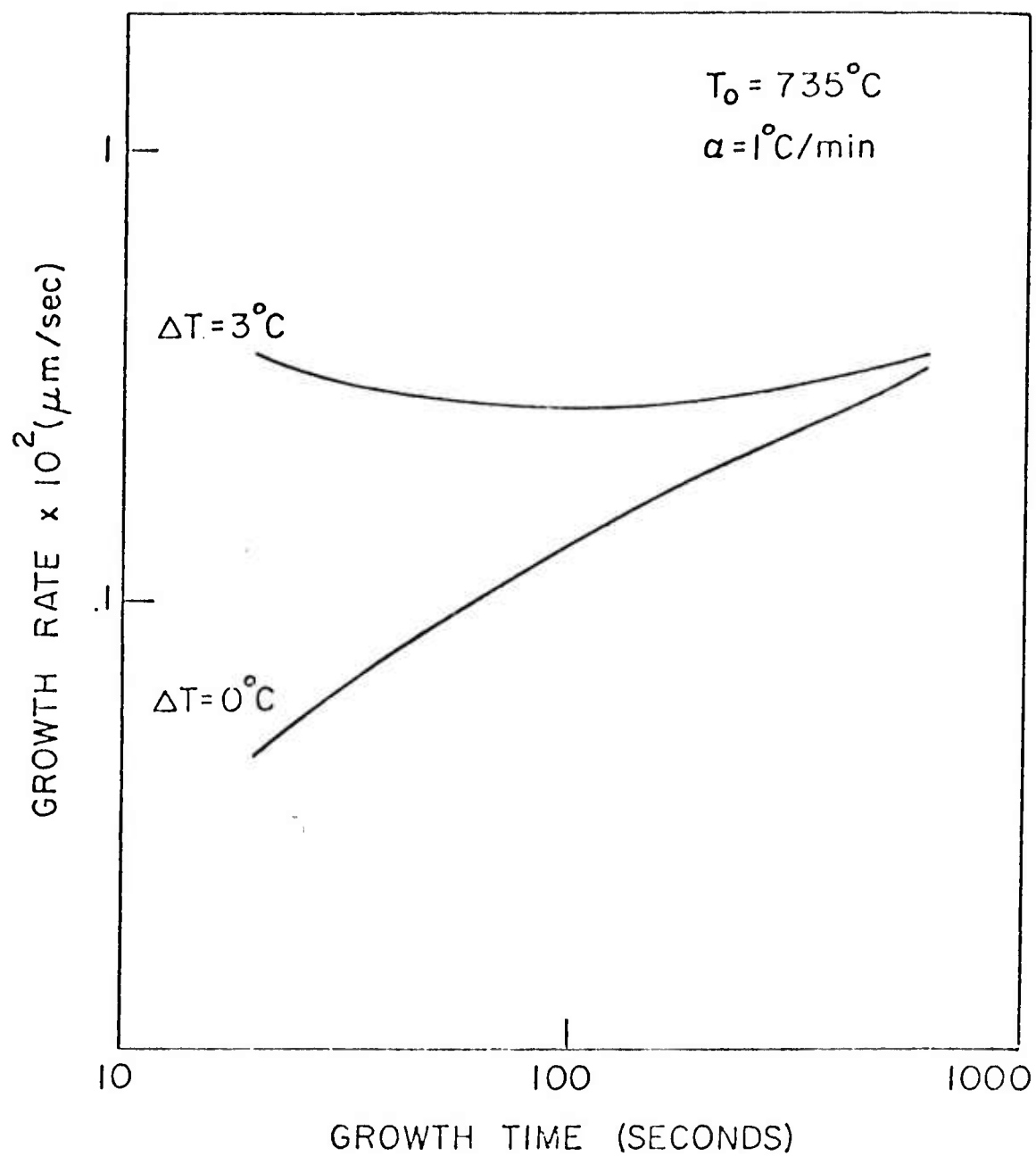


FIG. 3.1.9 Growth rates as a function of growth time at 735°C both with and without a supercooling of 3°C and with a cooling ramp.

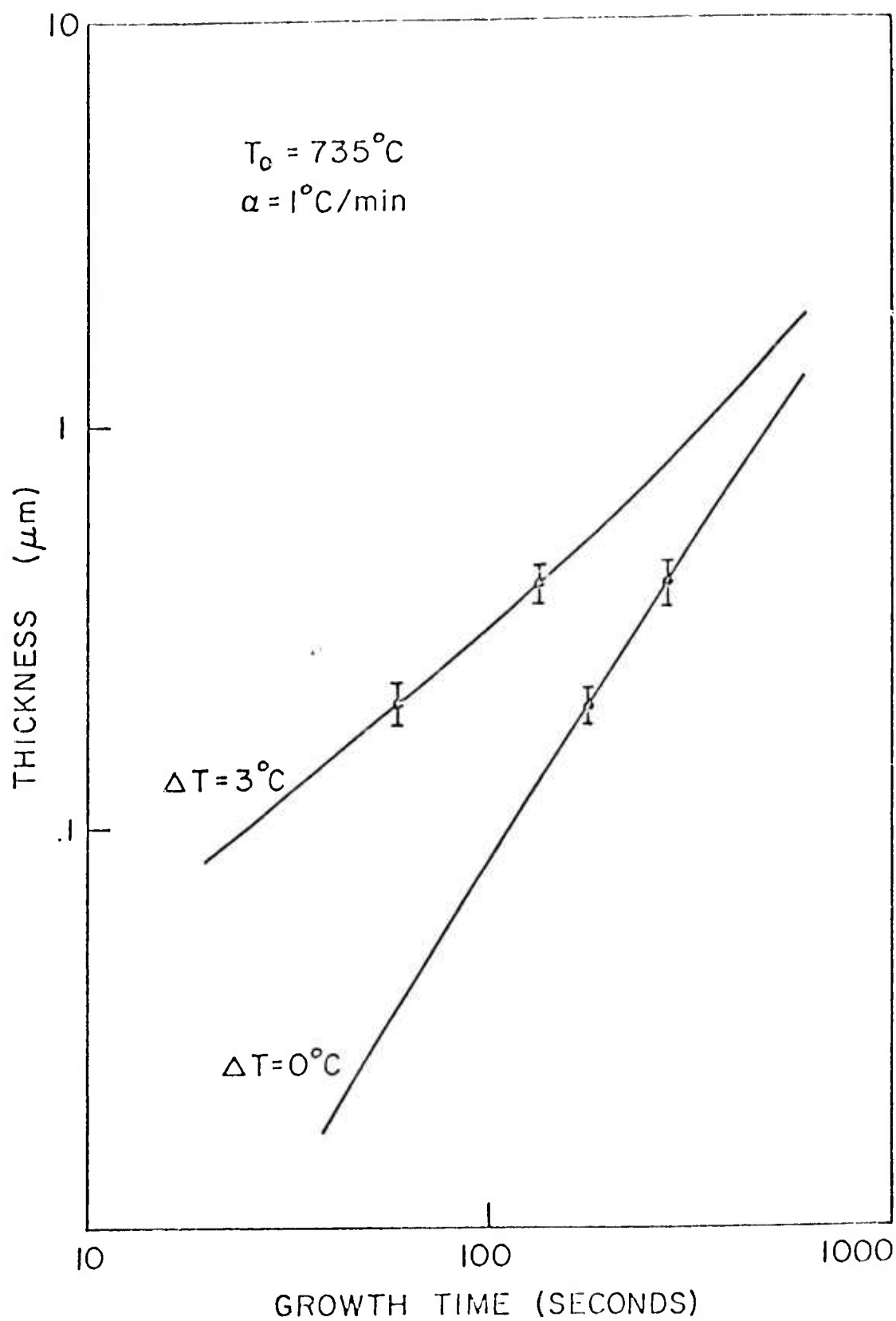


FIG. 3.1.10 Thickness vs. growth time at 735°C for the conditions of Fig. 3.1.9.

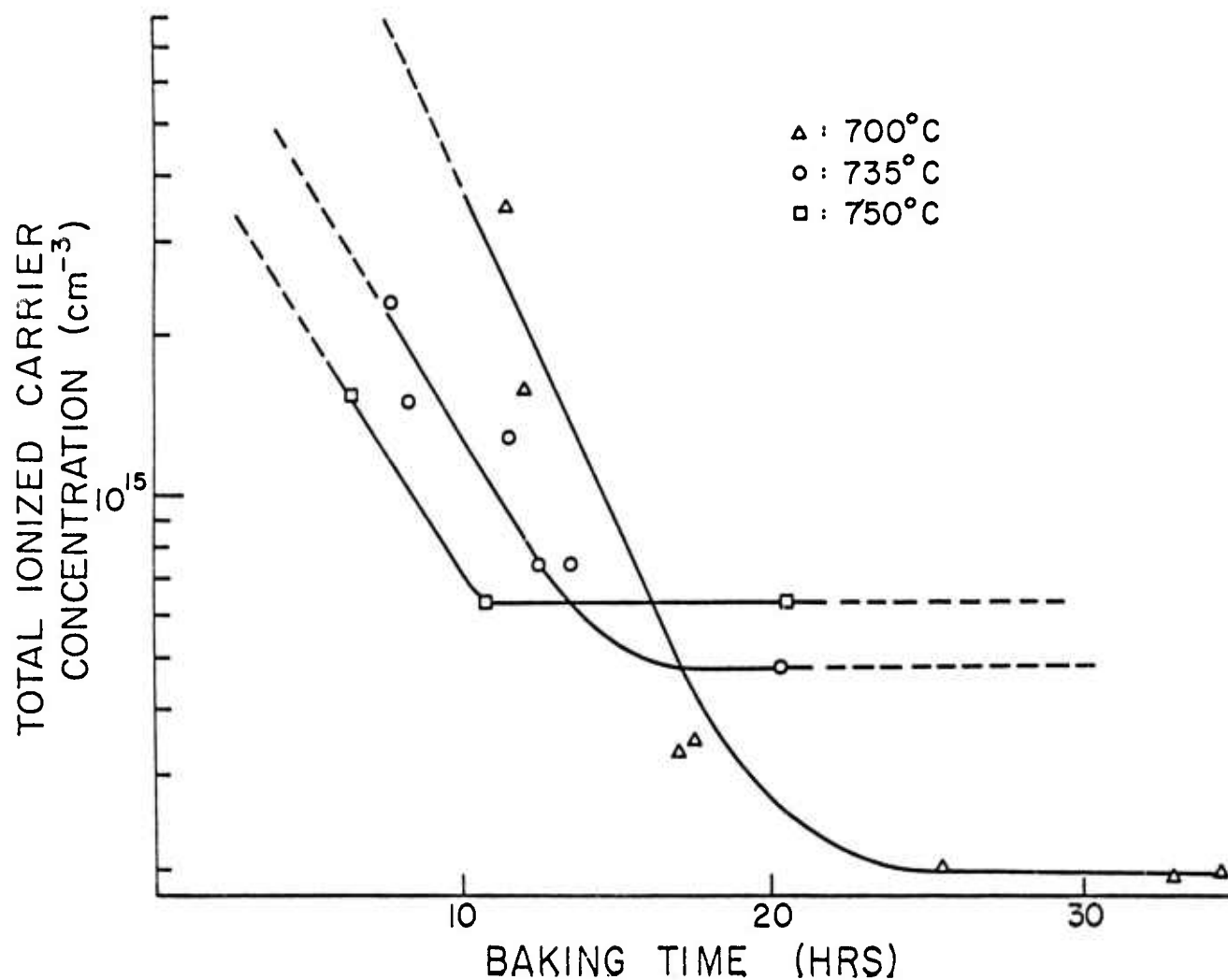


FIG. 3.1.11 Total impurity concentration as a function of baking time between runs. Notice that the total impurity concentration drops rapidly with baking time and reaches an equilibrium determined by the distribution coefficient and the water vapor content.

temperature have been taken randomly from a number of melts. Therefore, the data points are only dependent upon between-run baking time. Illustrated in Fig. 3.1.12 is a set of curves plotting the dependence of total donor concentration on between-run baking time. If desired, total acceptor concentration can be deduced by using Figs. 3.1.11 and 3.1.12. As can be seen, each time the reactor is opened up for loading, a charge of impurities is introduced and trapped inside the reactor. It takes between 10 hours (at 750°C) and 25 hours (at 700°C) to remove most of these impurities. In other words, the impurity concentration drops rapidly with baking time and reaches an equilibrium after 10 hours at 750°C and 25 hours at 700°C. The equilibrium values of $N_D + N_A$ (total carrier concentration) are $6.4 \times 10^{14} \text{ cm}^{-3}$ at 750°C with an associated liquid nitrogen (LN_2) mobility of 105,000 $\text{cm}^2/\text{V-sec}$, $4.8 \times 10^{14} \text{ cm}^{-3}$ at 735°C with an associated LN_2 mobility of 120,000 $\text{cm}^2/\text{V-sec}$, and $1.9 \times 10^{14} \text{ cm}^{-3}$ at 700°C with an associated LN_2 mobility of 170,000 $\text{cm}^2/\text{V-sec}$.

The system components dealt with are C (graphite), H_2 , SiO_2 , O_2 , and unknown impurities that come in Ga and source GaAs. Mass spectrum analysis done by the manufacturer indicate that the impurities in Ga are not much of a problem. Therefore, the chemical reaction between the growth components during baking are believed to be responsible for the behavior shown in Figs. 3.1.11 and 3.1.12. Hicks and Green⁶ have grown layers in a Spectrosil (high quality quartz) boat. In such a system, the graphite is eliminated and so one should not take C into account. Hicks and Green made some thermodynamic calculation of the chemical reactions and found a theoretical expression for Si contamination induced from the quartz walls and the boat. They also indicated that Si contamination varies inversely with water vapor content in the Spectrosil-quartz system. Hicks and Marley⁷ have reported the highest purity layers in such a system. Si

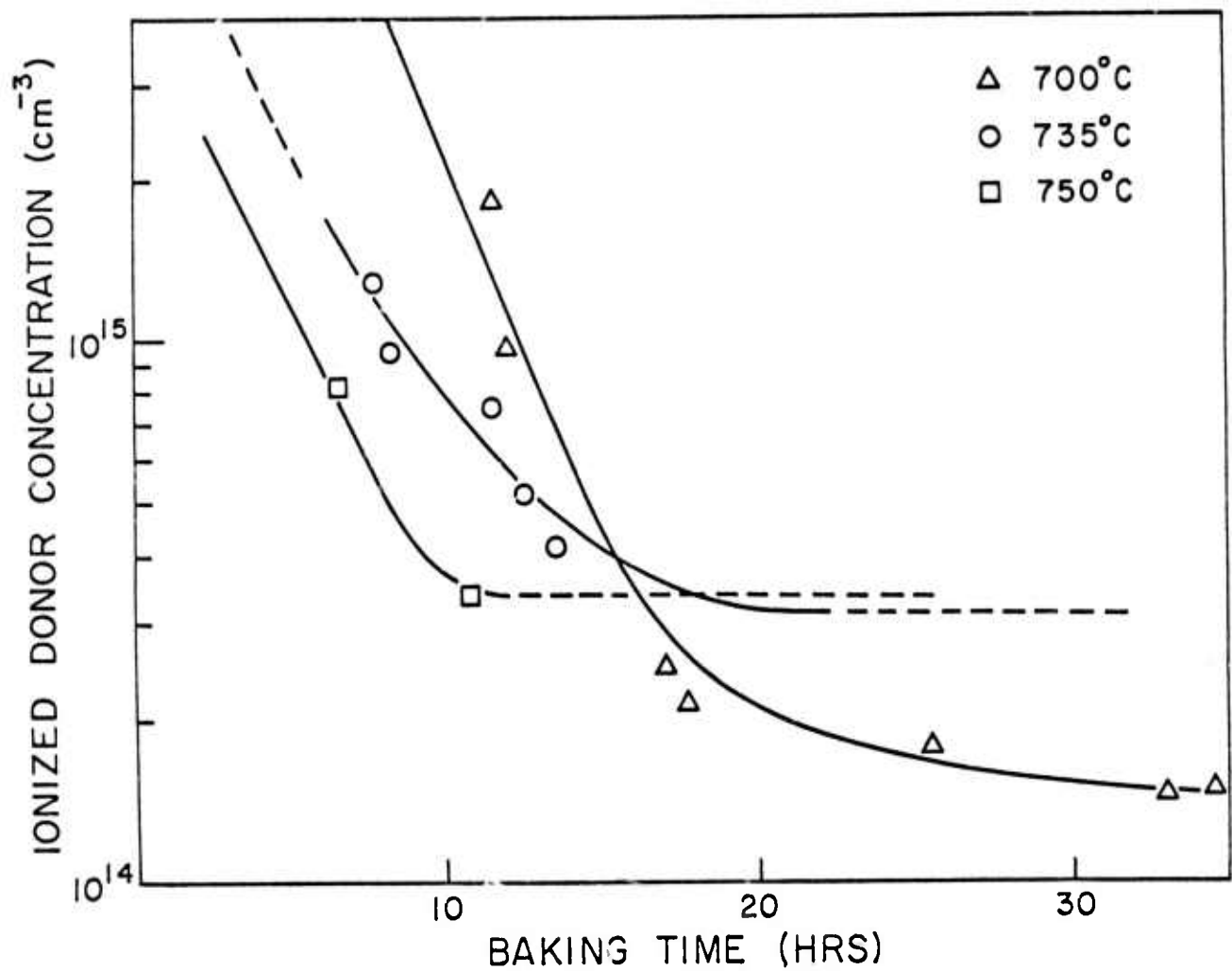


FIG. 3.1.12 Ionized donor concentration as a function of baking time between runs. The ionized acceptor concentration can be deduced by comparison with Fig. 3.1.13 which gives the total ionized impurity concentration.

contamination calculated by Hicks and Green as a function of reciprocal of the temperature is shown in Fig. 3.1.13. The difference between the Spectrosil growth components and ours is the fact that we utilize a graphite boat. This, therefore, suggests the possibility of C contamination. The fact that a charge of impurities is introduced each time the reactor is opened up for loading may indicate that O_2 somehow places C in the melt.

Experimentally found equilibrium values of $N_D + N_A$ and the difference between these values and Si are plotted against the reciprocal of baking temperature and shown in Fig. 3.1.13. We believe that this difference is caused by C which forms CO at the growth temperatures. In fact, Mullin⁸ has detected a major line of C in LPE grown GaAs. If the $N_D + N_A$ line (Fig. 3.1.13) is extrapolated down to 665°C (dashed lines), one would expect a value of $8 \times 10^{13} \text{ cm}^{-3}$ for $N_D + N_A$ and 200,000 $\text{cm}^2/\text{V-sec}$ for LN_2 mobility. The layers, grown at 665°C after a baking time of 35 and 50 hours, exhibit LN_2 mobilities of 91,000 $\text{cm}^2/\text{V-sec}$ or lower. This is attributed to the fact that the temperature is not high enough to break the crust of a possible oxide layer on the top surface of the melt which, in turn, confines the impurities inside the melt. In addition, a number of layers grown at 700°C from a melt which had excess GaAs crystal on the top surface have yielded very low mobilities. This experiment also suggests that GaAs crust prevents impurities from diffusing onto the melt surface and being carried away by H_2 . In order to achieve about 200,000 $\text{cm}^2/\text{V-sec}$ LN_2 mobility in a graphite boat system, it is necessary to add just enough GaAs source-crystal to saturate the melt (slightly undersaturation is preferred because of the wetting problems). The melt then should be baked at about 714°C for a long enough time and the growth must be made at 665°C. Moreover, if the melt is left cold for more than 3-4 days, the results become unrepeatable.

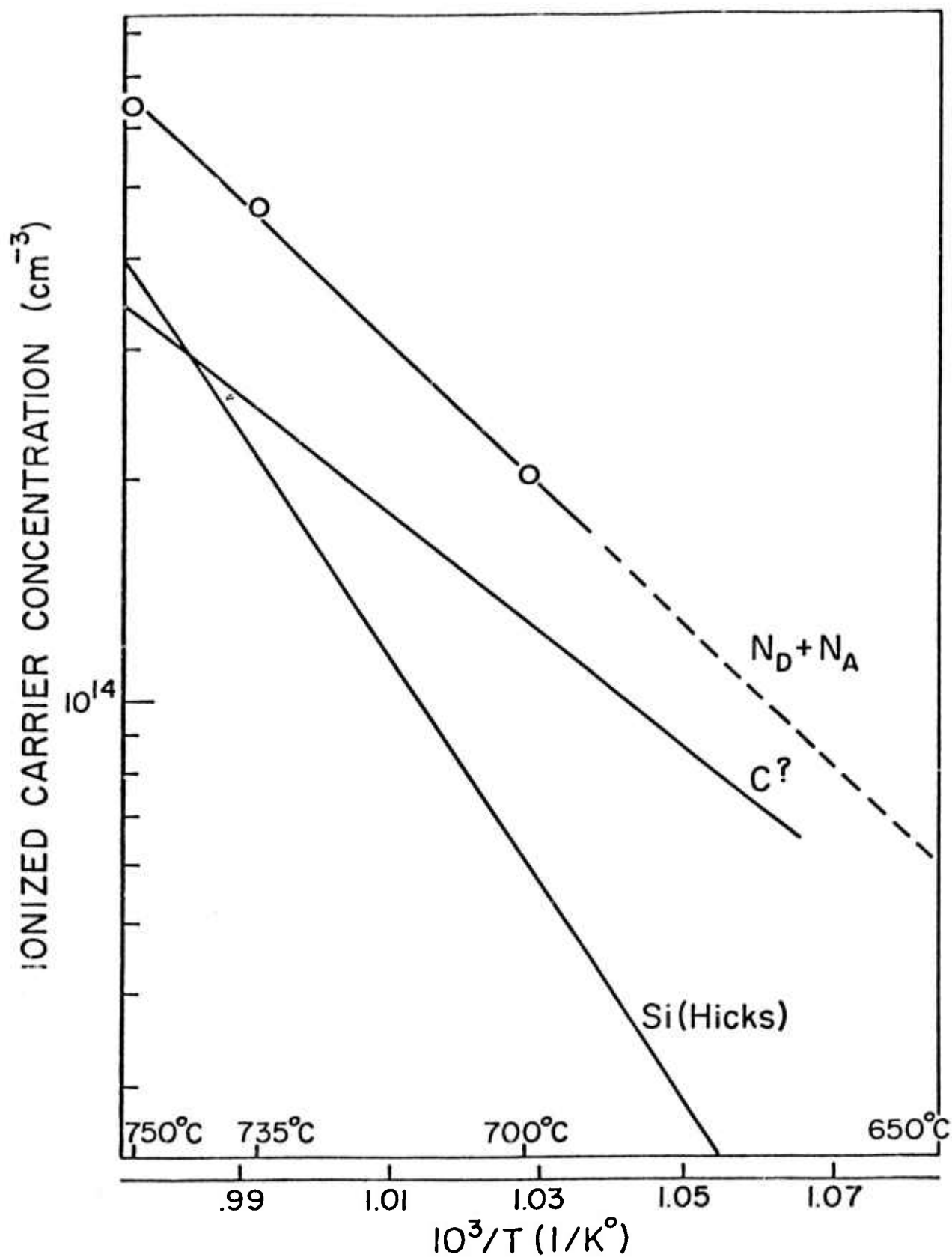


FIG. 3.1.13 Total carrier density against the reciprocal of baking temperature. (Si data from Hicks and Green⁶, and the difference between $N_D + N_A$ and the Si curve is attributed to C contaminations (mainly donors).

Buffered FET layers have been grown at 700°C and 750°C with acceptable surface morphology. Ge doped p⁻ buffered FET layers have also been grown. The electrical properties of p⁻ buffer layers will be studied.

The remaining difficulties can be summarized as follows: approximately 30 hours of baking (at 700°C) is required to achieve a total carrier concentration of less than 2×10^{14} . In this baking process, the surface of GaAs substrate degrades as reported by Chiang and Pearson⁹. Our experiments showed that such a degradation occurs even at temperatures as low as 700°C. On the other hand, total carrier concentrations in the mid 10^{13} cm^{-3} and net carrier concentrations in the low 10^{13} cm^{-3} are required by FET buffer layers. Therefore, it is necessary to consider boron nitride and Spectrosil boats. The latter is of particular importance, since one can achieve p⁻ buffers with net acceptor concentrations of low 10^{13} cm^{-3} without any intentional dopant.

3.1.3.4 Evaluation of FET Epitaxial Layers Grown at Cornell University

A series of epitaxial layers grown at Cornell for FET applications were sent to the Science Center for evaluation. The morphology and electrical characteristics of these layers were examined and are reported here.

The first three layers sent (CS011708, LD042203, LD042206) were grown at temperatures between 735°C and 785°C after relatively long saturation period (~ 16 hours). This may account for the relatively poor surface morphology. A high density ($\sim 10^5 \text{ cm}^{-2}$) of cusps or pits were observed under phase contrast microscopy. Anomalous capacitance voltage effects were observed indicating a probably high density of interface defects. In fact, an uncovered region of the semi-insulating substrate (the substrate in the Cornell system is slightly larger than the melt) exhibited an appreciable conductivity (33Ω between .025"

diameter Al dots) indicating that thermal conversion had taken place. For the one sample for which profile measurements were possible, the doping and thickness variations were 4 to $6.2 \times 10^{16} \text{ cm}^{-3}$ and 0.24 to $0.35 \mu\text{m}$, respectively, over the 1 cm^2 area of the layer.

A more recent sample sent for evaluation (LD042408) showed vastly improved surface morphology. Our standard measurement of the doping profile (at the center and four corners of the slice) gave carrier concentration and thickness variations of 3.8 to $4.1 \times 10^{16} \text{ cm}^{-3}$ and 0.33 to $0.52 \mu\text{m}$, respectively. The mean thickness at 20 points across the slice was $0.46 \mu\text{m}$ with a percent standard deviation of 15%. This slice is presently being processed into FETs.

3.2 Semi-Insulating Substrate Material

3.2.1 Material Growth at Crystal Specialties

During the recent report period, considerable progress has been made in understanding some of the basic problems of crystal growth by the horizontal Bridgman method.

It has been a common practice to backfill the quartz growth ampoule to one atmosphere of inert gas. This was done to suppress turbulence of the melt which is caused by arsenic escaping erratically from the colder portions of the liquid as the crystal is grown. An inert gas backfill also has the effect of suppressing evaporation of GaAs onto the top portion of the quartz envelope, thus causing a decrease in the visibility of the growing ingot. Nitrogen, helium, and argon have been used for this purpose.

Higher dislocation counts, slip, lineage and poly generation is in part attributed to the use of an inert gas above the melt. It is felt that the degradation of crystalline quality is caused by gases in the liquid being in-

incorporated into the growing crystal as an inactive impurity.

Table 3.2-1 shows the results of single crystal yield when crystals grown in an N_2 atmosphere are compared to those grown in a pure As atmosphere. When N_2 was no longer used as a backfill gas, the single crystal yield went from 32% to about 58%. It is of particular interest to note that when N_2 was not used as a backfill gas, we were able to compensate without the addition of O_2 to the melt. It must be emphasized, however, that O_2 at a low level is still present from residual O_2 on the Ga, As and quartz walls.

Table 3.2-2 is a comparison of the mass spectrographic analyses of crystals grown with N_2 and O_2 backfills with that of a crystal grown when no nitrogen or oxygen additions were made. The analysis does not yield any information which would indicate why O_2 is no longer needed to accomplish compensation.

It is felt that any other than As in the growth chamber will have this degenerate effect upon crystal growth. Crystals grown in carbon boats are affected in this same way, since CO and CO_2 are generated from residual O_2 and from O_2 generated by reduction of the quartz. O_2 additions to the melt are not as serious since the compound Ga_2O_3 is formed, producing a low vapor pressure of O_2 .

This information can be extremely useful in predicting the proper boat materials. Boats which can generate gases within the growth ampoule are not desirable. Table 3.2-3 shows the results expected with the most common boat materials. This information appears to confirm what many investigators have suggested, that carbon cannot be used successfully in producing high quality GaAs by the horizontal Bridgman method. Although we have not yet used BN without the presence of an N_2 backfill, it is expected that when we do, we will find that the lineage, slip and poly generation still exist because of the N_2 generated from

TABLE 3.2-1
YIELD COMPARISONS FOR CRYSTALS GROWN IN
 N_2 WITH THOSE GROWN IN VACUUM

Total Number of Runs	Backfill gas	Oxygen Addition	Compensated	Single
38	N_2	100 m Torr O_2	92%	32%
3	None	100 m Torr O_2	100%	67%
19	None	None	100%	58%

TABLE 3.2-2

MASS SPECTROGRAPHIC ANALYSIS OF Cr-DOPED GaAs
(RESULTS IN ATOMIC PARTS PER MILLION)

Impurity	One Atmosphere N ₂ Backfill 100 mTorr O ₂ Addition			No N ₂ Backfill No O ₂ Addition	Detection Limits
	Sample No.			Sample No.	
	2004	2000	2132	2440	
C	0.91	7.7	1.4	0.82	0.05
N	0.05	0.05	0.05	0.10	0.05
O	2.3	3.4	2.0	.72	0.05
F	ND	ND	ND	0.019	0.01
Na	2	2	2	----	2.0
Al	1.8	2.1	1.4	0.082	0.1
Si	ND	0.07	2.7	0.30	0.07
P	0.77	0.82	1.1	0.032	0.06
S	0.1	0.1	1.2	----	0.1
K	0.68	0.54	0.59	0.037	0.01
Cr	0.68	1.7	12	0.58	0.1
Cu	2.9	ND	2.1	ND	0.1

TABLE 3.2-3

EVALUATION OF BOAT MATERIAL BASED ON GAS GENERATION

Boat Material	Gas Generation from Oxidization	Expected Results
Carbon	$O_2 + 2C \rightarrow 2 CO$	Poor
Boron Nitride	$3O_2 + 4BN \rightarrow 2B_2O_3 + 2N_2$	Poor
Aluminum Nitride	$3O_2 + 4AlN \rightarrow 2Al_2O_3 + 2N_2$	Poor
Quartz	None	Good except Si contamination and tendency to wet quartz.
Aluminum Oxide	None	Good except GaAs wets Al_2O_3

the BN boat.

It might be suggested that the solution to this problem is to eliminate all of the residual O_2 , thus preventing the reduction of these boats. This might be possible but would not be practical when producing semi-insulating GaAs. As was pointed out in previous reports,^{3,17} the presence of some O_2 is necessary to prevent the dissociation of quartz which would produce Si contamination. It appears that at least for the time being we must be satisfied with quartz as the boat material.

We suggest that much of the remaining growth problems related to low dislocation material could be associated with carbon within the growth chamber. It is quite possible that carbon is coming from back streaming of oil vapors from the high vacuum system. The pump used for evacuating is a turbo molecular pump chosen for its reported low back streaming characteristics. We think that the back streaming of this pump is not as low as has been reported.

In addition to the work described above, Crystal Specialties has supplied polished wafers to Rockwell International Science Center as requested.

3.2.2 Semi-Insulating Material Evaluation at the Science Center

This activity consists of two parts. One is the study of bulk electrical properties of the material in order to determine the type of conductivity, to measure the density of deep impurities, and to develop a model for the electrical compensation. This information is needed in order to understand what type of junction is formed between substrates and device layers. This is also basic information, required for understanding and improvement of doping techniques in bulk growth of substrate material. The other part of the material evaluation activity is the study of stability of surface layers of substrate materials under heat treatment. This surface study is necessary because all substrates have to

sustain some heat treatment when used for epitaxial growth. Alterations in a surface layer of the substrate are potential sources of defects at the interface between substrate and device layers.

3.2.2.1 Bulk Electrical Properties of Semi-Insulating GaAs

Two models for the electrical compensation of Cr-doped semi-insulating GaAs will be discussed. In the first model the background impurities, presumably Si donors with density N_D , are compensated by Cr acting as a deep acceptor with a density N_A larger than N_D . This is shown schematically in Fig. 3.2.1 (a) where the density of free electrons n , the density of free holes p , the density of ionized donors N_D^+ , and the density of ionized acceptors N_A^- are plotted on a logarithmic scale as functions of the position of the Fermi level in the band gap.¹⁰

The condition of charge neutrality is

$$n + N_A^- = p + N_D^+ \quad (3)$$

Eq. (3) can be simplified for semi-insulating material because the Fermi level is near the middle of the gap. In this case, Fig. 3.2.1 shows that n and p are much smaller than N_A^- and N_D^+ . Therefore, n and p can be neglected in Eq. (3), which becomes $N_A^- = N_D^+$. With this simplification, the intersection of the curves for N_A^- and N_D^+ at point F in Fig. 3.2.1 determines the position of the Fermi level. This condition can be written as

$$\frac{N_A}{1 + \exp\left[\frac{(E_A - E_F)}{kT}\right]} = N_D \quad (4)$$

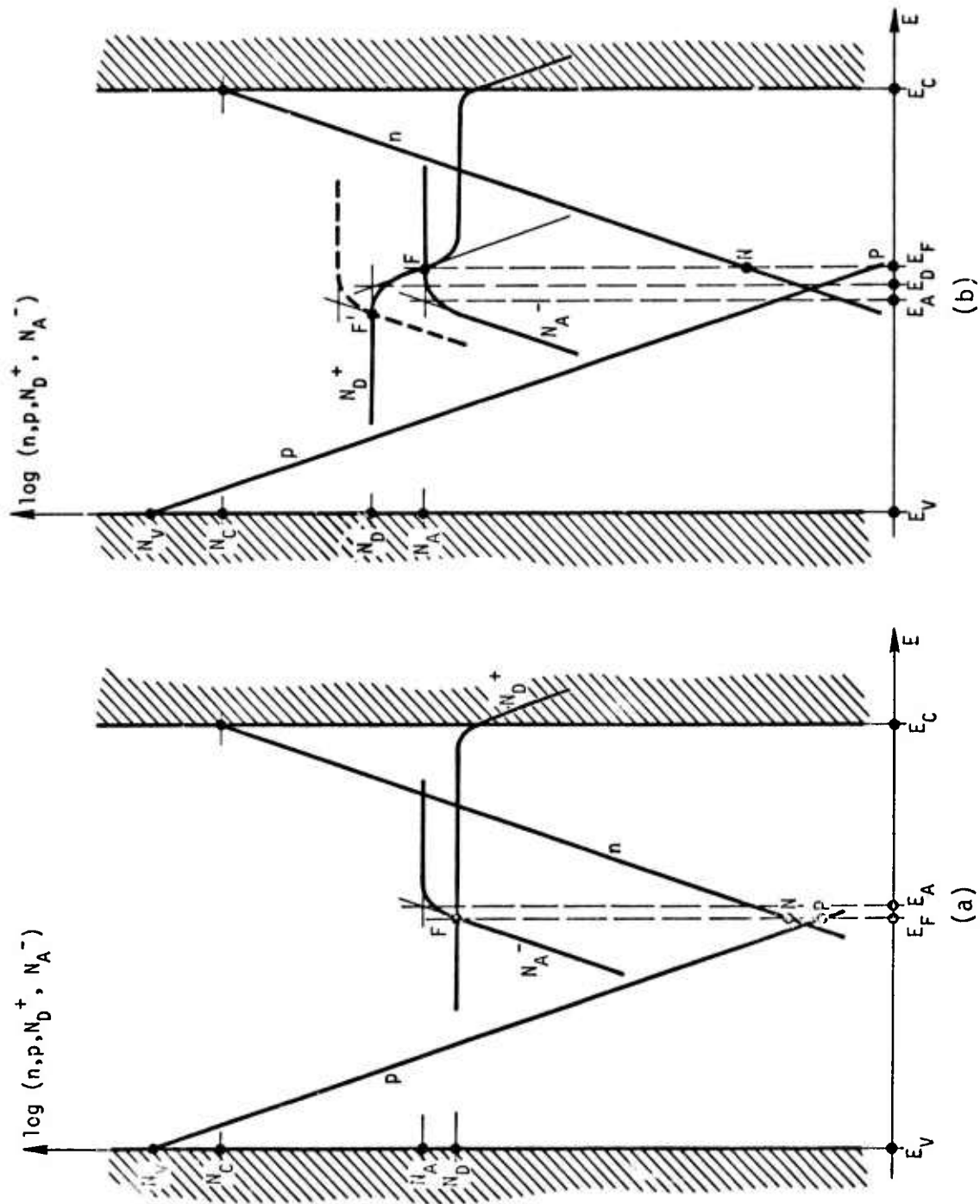


FIG. 3.2.1.1 Graphic representation of n, p, N_D^+ and N_A^- as functions of the Fermi level; (a) for the deep-donor model, (b) for the deep-acceptor model.

with the approximation $N_D^+ \simeq N_D$.

Eq. (4) and Fig. 3.2.1 show that the Fermi level lays just below E_A , its distance from E_A being determined by the compensation ratio N_A/N_D . Changes of this ratio can displace the Fermi level slightly up or down in the gap and alter the values of n and p which are represented by points N and P in Fig. 3.2.1(a). Such range in the position of the Fermi level must account for the existence of Cr-doped semi-insulating GaAs with either n- or p-type conduction.^{11,12} However, this range is narrow because N_A must be larger than N_D . This model was suggested among other alternatives in the early work of Cronin and Haisty,¹³ and has been used rather widely in the literature^{11,12,14-16} despite lacking conclusive tests or discussions.

The second model, proposed here, is schematically described in Fig. 3.2.1(b). Here too, as in the previous model, Cr acceptors with density N_A compensate a lower concentration of shallow background donors. But, in addition, there is a deep donor level associated with oxygen impurities. The density N_D of such deep donors may be larger or smaller than N_A . In Fig. 3.2.1(b) the composite curve representing N_D^+ is obtained by superposition of a simple curve for the shallow donors and another for the deep donors. The Fermi level is at F, the intersection of the curves representing N_D^+ and N_A^- . This condition can be written as

$$\frac{N_D}{1 + \exp\left[\left(E_F - E_D\right)/kT\right]} = N_A \quad , \quad (5)$$

with the approximations $N_A^- \simeq N_A$. The position of the Fermi level (point F) is

independent of the density of shallow donors provided that such density is well below N_A .

Fig. 3.2.1(b) was drawn for the case $N_D > N_A$. In this case the Fermi level (point F) is above E_D , its position being determined by the ratio of the densities of deep donors and deep acceptors N_D/N_A . If N_D/N_A decreases, F moves toward the deep donor level E_D . If N_A becomes larger than N_D , the situation can be easily visualized in Fig. 3.2.1(b) by raising the curve that represents N_A^- above that for N_D , to the position shown with a thin dashed line. The intersection of N_D^+ and N_A^- , which determines the Fermi level, is now at F'. Therefore, depending on whether $N_D > N_A$ or $N_A > N_D$, the Fermi level may move from above E_D to below E_A . The practical range over which the Fermi level may vary with the impurity concentrations is broader than in the first model, making this model more adequate to explain the existence of either n- or p-type semi-insulating material.

The main reason for considering the two-deep-level model, despite its complexity, is the observation that O must always be present in the growth ampoule in order to successfully grow high resistivity Cr-doped crystals.¹⁷ Besides the well-known role of inhibiting the dissociation of quartz in the ampoule,¹⁸ oxygen is likely to participate in the electrical compensation. In fact, oxygen has been used to obtain semi-insulating GaAs before Cr started being used as a dopant. The two-deep-level model proposed here is similar to the model proposed by Blanc and Weisberg¹⁹ and demonstrated by Haisty et al²⁰ for oxygen doped semi-insulating GaAs. The main difference is that in Blanc and Weisberg's model, the role played here by the deep Cr-acceptor level was played by a shallow acceptor.^{19,20}

In order to test the two models discussed above, transport properties

of samples with low and high Cr concentration were compared. The low- and high-Cr samples were taken from boule #1718 and #2000 supplied by Crystal Specialties. An advantage of choosing these particular samples is that specimens from neighboring wafers from the same boules had been used rather extensively for experiments described in previous reports.^{5,17} Table 3.2-4 shows the results of a mass spectrographic analysis of the two boules.²¹ The low-Cr material, boule #1718, contains $5 \times 10^{15} \text{ cm}^{-3}$ Cr atoms. This is the lowest Cr concentration Crystal Specialties can presently use for high-resistivity material.³ The high-Cr material, boule #2000, contains $5.8 \times 10^{16} \text{ cm}^{-3}$ Cr atoms. We consider this the highest acceptable Cr concentration because boule #2000 has some incipient precipitation of Cr discovered by secondary ion mass spectroscopy at Cornell University.³ We conclude that boules #1718 and #2000 are at the two boundaries of the range of Cr concentration compatible with precipitate-free, high resistivity substrate material. This range is remarkably small, spanning only one order of magnitude.

Room temperature resistivity and Hall measurements were made on the high- and low-Cr samples. A Van der Pauw configuration with evaporated and alloyed In contacts was employed. The current through the samples was measured with a Keithley 419 picoammeter and the voltages with a Keithley 602 floating electrometer.

Table 3.2-5 summarizes the results from the resistivity-Hall measurements. Both the high- and low-Cr samples have high-resistivity, $3.4 \times 10^8 \text{ ohm-cm}$ and $3.8 \times 10^8 \text{ ohm-cm}$ respectively. The low-Cr sample is n-type with a free electron density $n = 3.6 \times 10^{16} \text{ cm}^{-3}$. The Hall mobility is $5200 \text{ cm}^2/\text{V-sec}$.

The high-Cr sample has a negative Hall constant as if it were n-type,

TABLE 3.2-4
MATERIALS FOR BULK STUDIES
(Impurity densities in cm^{-3})

	Low-Cr Boule #1718	High-Cr Boule #2000
C	1.1×10^{16}	1.2×10^{16}
N	2×10^{15}	2×10^{15}
O	4.2×10^{16}	5.8×10^{16}
Al	2×10^{15}	2×10^{15}
Si	3×10^{15}	1×10^{15}
S	2×10^{15}	4×10^{15}
K	2×10^{15}	2×10^{15}
Cu	2.8×10^{16}	N.D.
Cr	5×10^{15}	5.8×10^{16}

TABLE 3.2-5

RESULTS OF RESISTIVITY-HALL MEASUREMENTS AT ROOM TEMPERATURE

	Low-Cr Boule #1718	High-Cr Boule #2000
ρ (ohm-cm)	3.4×10^8	3.8×10^8
R_H (cm ³ C ⁻¹)	-1.76×10^{12}	-1.24×10^{11}
μ_H (cm ² V ⁻¹ sec ⁻¹)	5200	320
Type	n	p
n (cm ⁻³)	3.6×10^6	4.6×10^5 *
p (cm ⁻³)		2.7×10^7 *
μ_e (cm ² V ⁻¹ sec ⁻¹)		5200 *
μ_h (cm ² V ⁻¹ sec ⁻¹)		520 *

* Calculated assuming $b = \mu_e / \mu_h = 10$

but, if this were true, the Hall mobility would be only $320 \text{ cm}^2/\text{V-sec}$. The small negative Hall constant is an indication of mixed conduction. When the contribution of both electrons and holes is considered, the full expression for the Hall constant for low magnetic field,

$$R_H = \frac{1}{q} \frac{p - nb^2}{(p + nb)^2} \quad , \quad (6)$$

must be used.²² Here, q is the elementary charge and $b \equiv \mu_e/\mu_h$ is the ratio between electron and hole mobility. Since p and n are related by the condition $np = n_i^2$, where n_i is the intrinsic carrier concentration, Eq. (6) yields values of n and p , if b is known. Once n and p are known, the mobilities can be calculated from the value of the resistivity ρ , since

$$\rho = (qn\mu_e + qp\mu_h)^{-1} \quad . \quad (7)$$

Using for b the value $b = 10$ reported for semi-insulating GaAs,¹¹ the values of n , p , μ_e and μ_h listed in Table 3.2-5 for the high-Cr sample are obtained. When such values are substituted into Eq. (7), the term $qp\mu_h$ becomes 6 times larger than $qn\mu_e$ showing that most of the current is carried by holes. Therefore, the high-Cr material is p-type despite the negative value of the Hall constant.

A value for b could be determined by studying the dependence of the Hall constant and the resistivity on the magnetic field.^{1,11} However, our basic conclusions on the type of conductivity and even the numerical results do not depend critically on the value assigned to b . In fact, increasing or decreasing the estimated value of b by 50%, the calculated mobilities change by only 14%;

n and p change much more, 50%, but even such a change would have no critical effect on the results because the values of n and p in Table 3.2-5 differ by two orders of magnitude. For the intrinsic carrier concentration, the room temperature (298K) value of $n_i = 3.6 \times 10^6 \text{ cm}^{-3}$ determined by transport measurements¹¹ was used. The value $n_i = 1.8 \times 10^6 \text{ cm}^{-3}$ calculated from the effective masses of electrons and holes determined by optical measurements²³ would yield unrealistic high values for the mobilities.

The resistivity of the low- and high-Cr samples was measured as a function of temperature. The results are plotted in Fig. 3.2.2. The resistivity decreases very rapidly when the temperature is increased, to the extent that the resistivity falls into the 10^3 - 10^4 ohm-cm range at 200°C. This resistivity drop of the substrate material must be taken into consideration for the design of microwave devices, particularly power devices which are required to operate at high temperature.

For the analysis of the low-Cr data, only the contribution of the electrons to the current needs to be considered because the material is n-type. Therefore, Eq. (7) for the resistivity is reduced to

$$\rho = (q\mu_e n)^{-1} \quad . \quad (8)$$

The free electron concentration n depends on the distance between the Fermi level and the conduction band $E_C - E_F$ through the familiar expression

$$n = N_C \exp \left[- (E_C - E_F) / kT \right] , \quad (9)$$

where T is the temperature, N_C is the effective density of states,

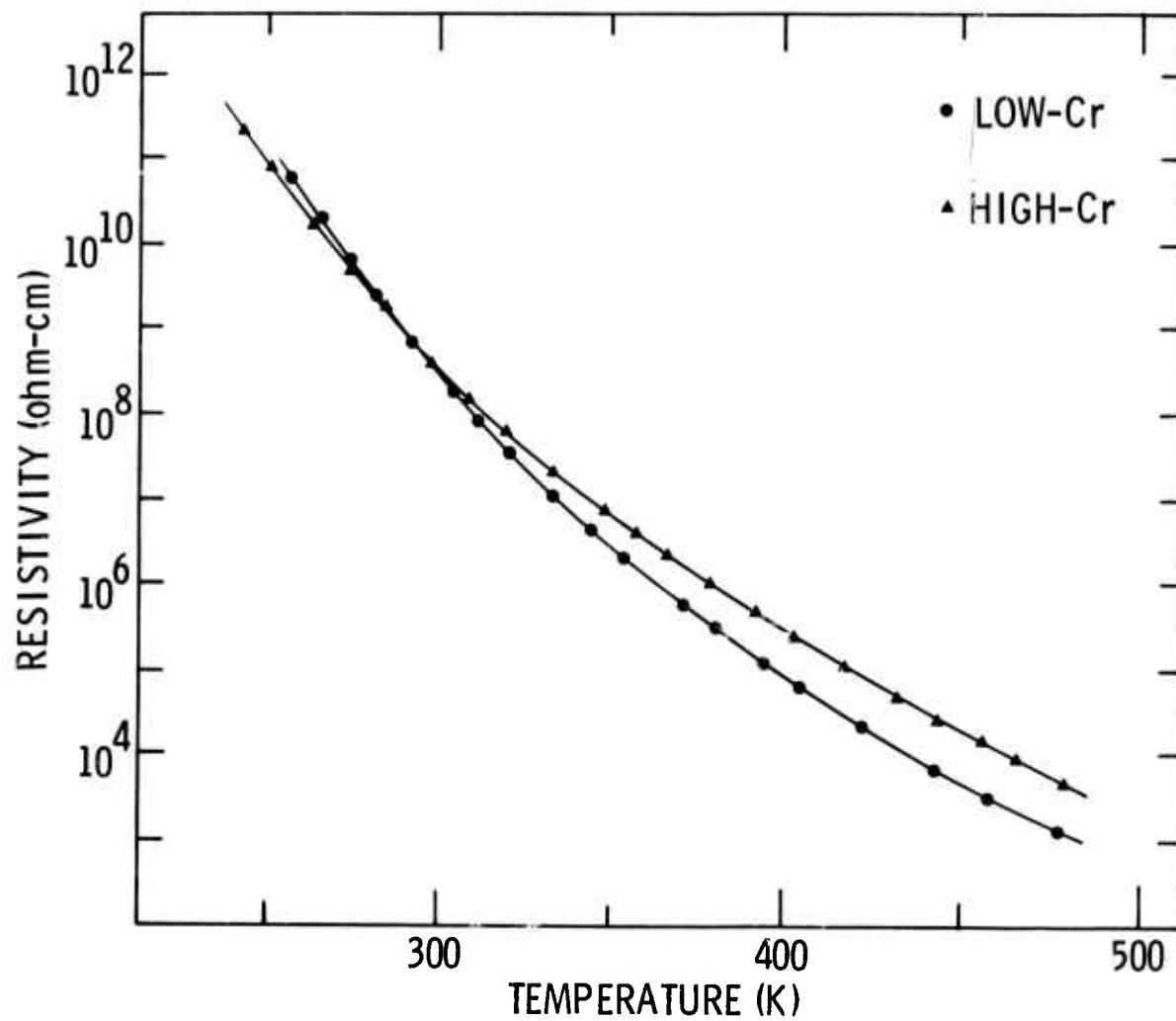


FIG. 3.2.2 Resistivity vs. temperature for the low-Cr (CS1718) and high-Cr (CS2000) samples.

$N_C = 2(2\pi m_e kT/h^2)^{3/2}$; m_e is the electron effective mass and h is Planck's constant.

Eqs. (8) and (9) are valid for any n-type material. In order to proceed further with the analysis by determining how $E_C - E_F$ depends on the temperature T , it is necessary to introduce a model for the impurity levels in the crystal. For the model with only a deep acceptor described in Fig. 3.2.1(a), the exponential in Eq. (9) may be written as the product of two exponentials by decomposing $E_C - E_F = (E_A - E_F) + (E_C - E_A)$:

$$\exp[(E_C - E_F)/kT] = \exp[(E_A - E_F)/kT] \exp[(E_C - E_A)/kT]. \quad (10)$$

An expression for $\exp[(E_A - E_F)/kT]$ can be obtained from Eq. (4) and substituted into Eq. (10). Thus, collecting Eqs. (10), (9) and (8), the final expression for the resistivity ρ for the deep acceptor model becomes

$$\rho = (q\mu_e N_C)^{-1} \left(\frac{N_A}{N_D} - 1 \right) \exp[(E_C - E_A)/kT], \quad N_A > N_D. \quad (11)$$

For the deep-donor deep-acceptor model described in Fig. 3.2.1(b), a similar derivation based on Eq. (5) instead of Eq. (4) leads to

$$\rho = (q\mu_e N_C)^{-1} \left(\frac{N_D}{N_A} - 1 \right) \exp[(E_C - E_D)/kT], \quad N_D > N_A. \quad (12)$$

This equation is valid only if $N_D > N_A$. In the case when $N_A > N_D$, which leads to position F' for the Fermi level in Fig. 3.2.1(b), the considerations made for the case of Fig. 3.2.1(a) apply, leading again to Eq. (11). It should become clear at this point that Eq. (11) applies to the case $N_A > N_D$ while Eq. (12) applies to the case $N_D > N_A$, regardless of the model. However, the model with only a

deep acceptor level (Fig. 3.2.1(a)) is compatible only with the condition $N_A > N_D$ and, therefore, only Eq. (11) applies to this model. It should also be pointed out that the coefficients that multiply the exponentials in Eqs. (11) and (12) become identical to one another when $N_A/N_D \gg 1$ or $N_D/N_A \gg 1$ respectively. As to the exponentials, the activation energies are just the depth of the acceptor and donor level respectively, a well-known feature of extrinsic semiconductors.

Three "constants" in Eqs. (11) and (12) are temperature dependent, namely N_C , μ_e and $E_C - E_A$ (or $E_C - E_D$). This temperature dependence should be made explicit in order to apply the equations to the analysis of the experimental values of ρ vs. T . N_C is just proportional to $T^{3/2}$. Therefore, it is sufficient to multiply ρ by $T^{3/2}$ in order to eliminate the effect of the temperature dependence of N_C . The electron mobility μ_e poses a more difficult problem. However, μ_e will be assumed to be independent of the temperature in the range of our measurements (230-480K). Such an assumption, based on the hypothesis that the mobility is determined by impurity scattering, is supported by the measurements of mobility in Ref. 11. For the temperature dependence of $E_C - E_A$ and $E_C - E_D$, it is not known how the depth of deep levels changes with temperature. Under this circumstance, the best approach is to assume that the depth of the deep levels varies proportional to the energy gap. Therefore, a corrective factor $E_g(T)/E_g(298K)$ must be introduced in the exponentials of Eqs. (11) and (12). This factor will be treated as a correction of the temperature scale. In conclusion, when all three effects discussed in this paragraph are considered, it is expected that in a plot of $\log(\rho T^{3/2})$ vs. $(1/T) [E_g(T)/E_g(298K)]$ the experimental points fall on a straight line.

In Fig. 3.2.3 the product $\rho T^{3/2}$ is plotted against $(1/T) [E_g(T)/E_g(298K)]$

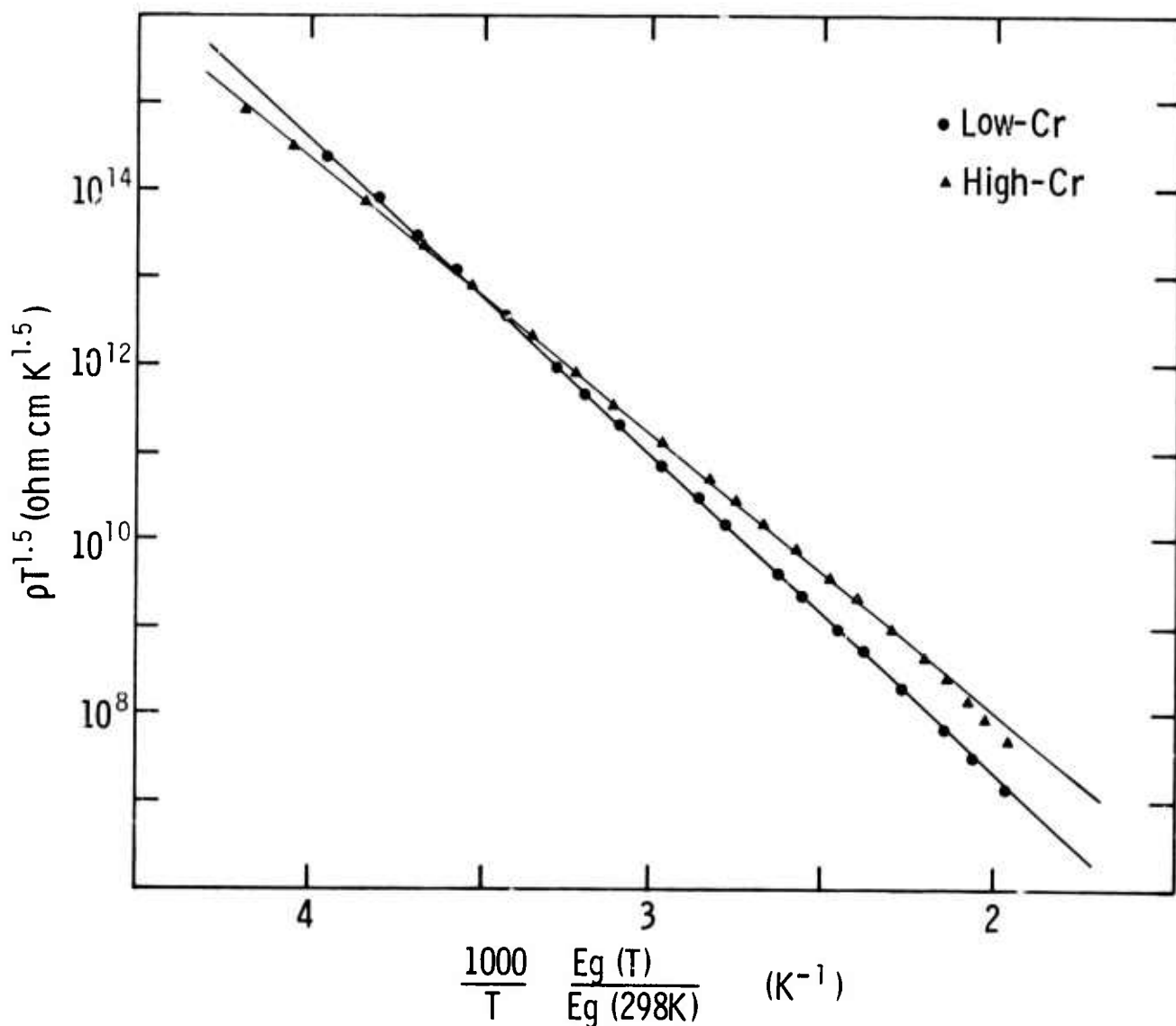


FIG. 3.2.3 $\rho T^{1.5}$ vs. $1/T$ for the low-Cr (CS1718) and the high-Cr (CS2000) samples. The horizontal scale was corrected for the variation of the band gap with temperature using the expression for $E_g(T)$ in Ref. 24.

for the low- and high-Cr samples. The fit of the low-Cr data with a straight line is perfect, suggesting that the criteria proposed in the paragraph above are correct. Since N_C is known,²³ and μ_e was determined with the Hall measurement discussed earlier in this section (Table 3.2-5), not only the activation energy but also N_D/N_A can be calculated from the results of the least square fit applied to Eqs. (11) and (12). The values $N_D/N_A = 14$ and $E_C - E_D = 0.72$ eV are obtained from the two parameters of the least square fit applied to Eq. (12). Eq. (11) must be ruled out because it is incompatible with the condition $N_D > N_A$.

The deep acceptor model (Fig. 3.2.1(a)) does not apply because this model requires $N_A > N_D$ or otherwise the material would not have high resistivity. The observation that $N_D > N_A$ leads instead to the conclusion that the deep-donor deep-acceptor model (Fig. 3.2.1(b)) is the valid one. This conclusion, and the proposition that the deep donor level is associated with 0 are supported by the measured value of the activation energy ($E_C - E_D = 0.72$ eV), which is in agreement with the activation energy of the deep donor in 0-doped semi-insulating GaAs (without Cr).^{20,25}

Since the basic conclusion, that the valid model is the deep-donor deep-acceptor model, depends on the value of N_D/N_A , it was tested how sensitive the value of N_D/N_A was to the assumptions made for the dependence of μ_e and $E_C - E_D$ on the temperature. Both the effects of assuming that the mobility decreases with temperature following $\mu_e \propto T^{-1.5}$ instead of remaining constant, and of assuming that the depth of the impurity level does not change at all with temperature instead of scaling with the gap, were evaluated as tests of worst possible circumstances. In both tests the effect on N_D/N_A was large, a one order of magnitude change, but N_D/N_A increased in both cases. Another point to consider is the effect of the degeneracy of the impurity levels

which was not taken into account in our analysis because of lack of information on deep levels. If a degeneracy factor is introduced in Eqs. (4) and (5),¹⁰ the resulting value of $N_D/N_A - 1$ must be multiplied by the degeneracy of the deep donor level. Again this would lead to an increase of N_D/N_A . In conclusion, a large error margin must be allowed for N_D/N_A , but the value $N_D/N_A = 14$ is a lower bound. Therefore, the basic conclusion, that $N_D > N_A$, is sound.

For the analysis of the ρ vs. T data of the high-Cr material, a least square fit with a straight line in Fig. 3.2.3 is not satisfactory, particularly for the data points at high temperature. This indicates that, although the high-Cr material is p-type (see Table 3.2-5), the contribution of the electrons to the electric current cannot be neglected at high temperature. Therefore, the full expression of the resistivity (Eq. (7)) must be considered, leading to the general equation

$$\rho^{-1} = q\mu_h N_V \exp \left[-(E_F - E_V)/kT \right] + q\mu_e N_C \exp \left\{ -[E_g - (E_F - E_V)]/kT \right\}, \quad (13)$$

where $N_V = 2(2\pi m_h kT/h^2)^{3/2}$ is the effective density of states in the valence band and m_h is the hole effective mass. At this point it is assumed that for the high-Cr case being considered $N_A > N_D$ so that the Fermi level is closer to the valence band than in the low-Cr material. Under this circumstance, there is no distinction between the behavior of the two models of Fig. 3.2.1, and for both models the Fermi level is determined by Eq. (4). Following the same steps which led to Eqs. (11) and (12) in the low-Cr case, the following expression for the conductivity ρ^{-1} is obtained:

$$\rho^{-1} = q\mu_h N_V \left(\frac{N_A}{N_D} - 1 \right) \exp \left[-(E_A - E_V)/kT \right] + q\mu_e N_C \left(\frac{N_A}{N_D} - 1 \right)^{-1} \exp \left\{ -[E_g - (E_A - E_V)]/kT \right\} \quad (14)$$

Eq. (14) has a structure similar to Eqs. (11) and (12), with two terms instead of one. The same considerations made in the low-Cr case apply to the temperature dependence of N_V , N_C , μ_h , μ_e and $E_A - E_V$. The values of μ_e and μ_h are taken from Table 3.2-5. N_C , N_V , q and E_g are known. This leaves only two unknown parameters in Eq. (14), namely $N_A/N_D - 1$ and $E_A - E_V$.

The result of a nonlinear least square fit of the high-Cr data of Fig. 3.2.2 to Eq. (14) is shown in Fig. 3.2.4. The fit is excellent. To obtain such a good fit in spite of the constraint imposed by leaving only two adjustable parameters in Eq. (14) is an indication that the model was correctly chosen. The values of the fitting parameters are $N_A/N_D - 1 = 0.06$ and $E_A - E_V = 0.60$ eV. The depth of the deep acceptor level measured from the conduction band is $E_C - E_A = E_g - (E_A - E_V) = 0.84$ eV. This value is in agreement with the depth of the deep Cr acceptor level determined by optical experiments.²⁶ The result $N_A/N_D = 1.06$ is one order of magnitude higher than the value obtained for the low-Cr material, where $N_D/N_A = 14$. This increase of N_A/N_D from the low-Cr to the high-Cr material follows the one order of magnitude increase of Cr concentration from the low to the high-Cr material (Table 3.2-4). The value for N_A/N_D is consistent with the assumption $N_A > N_D$ made in the derivation of Eq. (14), but it is very close to one. Therefore, some tests similar to those discussed earlier in this Section for the low-Cr material will be made in order to determine how sensitive the numerical result for N_A/N_D is to the value assigned to the mobility ratio, to the temperature dependence of the mobility, and to the degeneracy of the deep acceptor level.

In summary, the ρ vs. T data from the low and high-Cr material are well interpreted with a two-deep-level model proposed here. This model has a deep donor level, probably associated with 0, and a deep Cr acceptor level. The

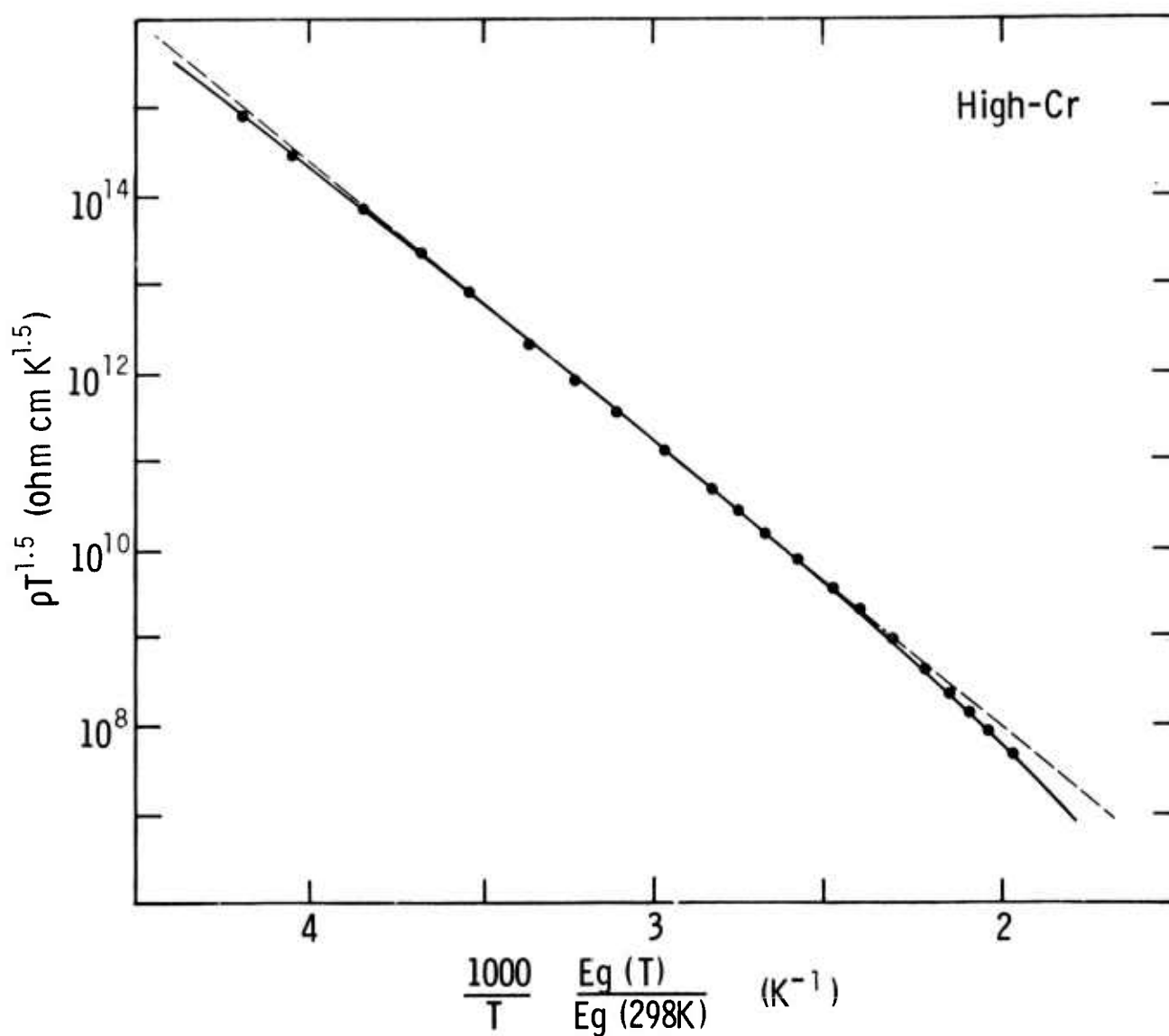


FIG. 3.2.4 Result of a nonlinear least square fit of the high-Cr data of Fig. 3.2.2. Values of the fitting parameters: $N_A/N_D = 1.06$, $E_C - E_A = 0.82 \text{ eV}$. The dashed line represents a linear least square fit, for comparison with the nonlinear fit.

more "conventional" model which has only one deep level, the Cr-acceptor, must be excluded in view of the data from the low-Cr material.

Finally, it is interesting to compare the results from the transport measurements discussed in this Section with the results of other measurements discussed in previous reports.^{3,17} In previous work, n-i-n and p-i-p samples of the same low and high-Cr material used for the experiments described in this Section were studied with a combination of standard injection measurements and a technique developed at the Science Center for profiling the potential across biased samples with an Auger Electron Spectrometer in a Scanning Electron Microscope.^{17,27} These measurements yielded separate values of N_D and N_A , while the transport measurements described in this Section yield ratios of these two quantities. In Table 3.2-6 the results from the earlier measurements are summarized. These results must still be considered preliminary because the voltage profiles of the low-Cr n-i-n sample and the high-Cr p-i-p sample are not quite understood.³ Yet, the agreement with the results from the transport measurements shown in the last column of Table 3.2-6 is very encouraging. This agreement is better than what would be expected after an estimate of experimental errors, particularly for the low-Cr case.

3.2.2.2 Effects of Heat Treatment on Semi-Insulating GaAs

Studies have been initiated on the effect of heat treatment on semi-insulating GaAs. This is an important problem because the substrate material always undergoes some annealing in the epitaxial growth process. Typically for liquid phase epitaxy, the substrate is heated at a temperature between 700°C and 775°C for at least one hour in a H_2 atmosphere before the layer is grown. In addition, heat treatment study of capped but unimplanted substrates may supply information relevant for low-dose ion implantation, a case where substrate effects

TABLE 3.2-6 SUMMARY OF RESULTS FROM MEASUREMENTS ON n-i-n AND p-i-p
SAMPLES. COMPARISON WITH RESULTS FROM ρ vs. T MEASUREMENTS

MATERIAL	SAMPLE	MEASUREMENT	RESULTS	FROM ρ vs. T
Low-Cr n-type	p-i-p	Potential Profile	$N_D - N_A = 5.7 \times 10^{13} \text{ cm}^{-3}$	14
	n-i-n	V_{TFL}^* $N_D = (N_D - N_A) + N_A$	$N_A = 7.4 \times 10^{12} \text{ cm}^{-3}$ $N_D = 6.4 \times 10^{13} \text{ cm}^{-3}$	
High-Cr p-type	n-i-n	Potential Profile	$N_A - N_D = 6.5 \times 10^{12} \text{ cm}^{-3}$	1.06
	p-i-p	V_{TFL} $N_A = (N_A - N_D) + N_D$	$N_D = 2.7 \times 10^{13} \text{ cm}^{-3}$ $N_A = 3.3 \times 10^{13} \text{ cm}^{-3}$	

* V_{TFL} is the Trap Filled Limit Voltage, obtained from the I-V characteristic.

are likely to be observed.

A survey of a wide variety of substrates was undertaken. A quick test that consists of measuring the electrical resistance between two concentric Al contacts evaporated on the substrate was employed.²⁸ The Al contacts tend to form non-ohmic contacts on the substrate, but the resistance of the material can be inferred from the ohmic portion of the I-V characteristics near the origin. This test is rather insensitive to small changes in the resistance of a sheet of material near the surface because such sheet is always in parallel with the bulk of the material. In addition, surface leakage may affect the resistance between the contacts in high resistance samples. Yet the simplicity of the test makes it convenient for a quick survey.

The results of our survey are summarized in Fig. 3.2.5, where resistance between contacts is plotted against anneal temperature. The length of heat treatment was 2 hours for all samples, except for those annealed at 700°C. The latter were annealed for only 45 minutes in order to duplicate the heat treatment experienced in our typical epitaxial growth procedure. Fig. 3.2.5 shows a definite downtrend of the resistance as the annealing temperature is increased. The sample treated at 775°C shows a total loss of its semi-insulating properties. A $\sim 0.3\mu\text{m}$ thick p-type layer was observed in a C-V profile with average $N_A - N_D = 1.1 \times 10^{16} \text{ cm}^{-3}$ determined by a Van der Pauw-Hall measurement. Even the short 700°C treatment produced some changes. The decrease of resistance shown in Fig. 3.2.5 for the 700°C annealed samples is within the measurement error, but its systematic downtrend indicates that there is indeed a change. A similar resistance measurement was performed on Crystal Specialties substrates capped with Si_3N_4 and annealed at 850°C for 30 minutes. Substrates from boule 2109 and 2000 showed no appreciable loss of resistance, while samples from boule 2004 gave scattered results varying

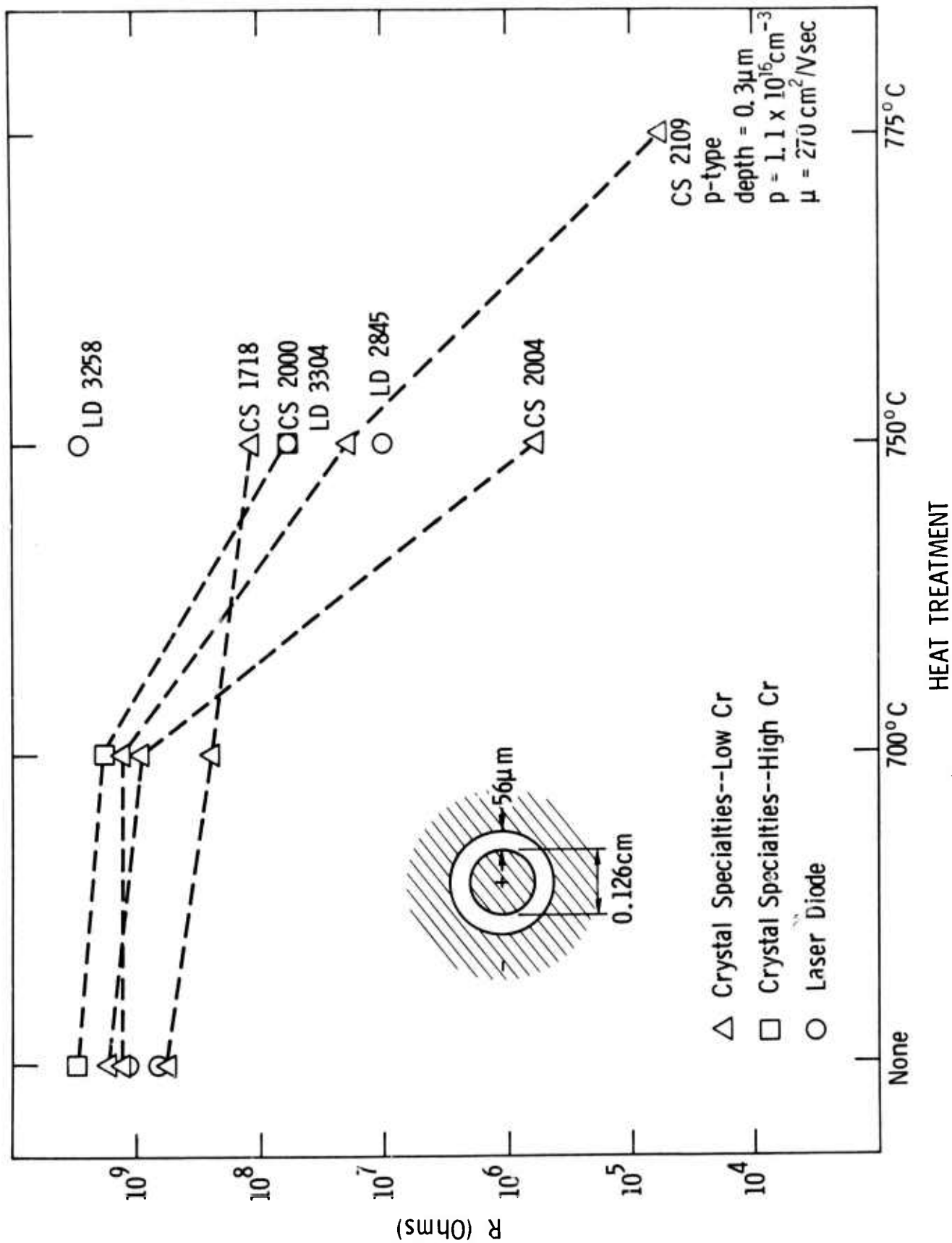


FIG. 3.2.5 Resistance between Al contacts on heat treated semi-insulating GaAs versus anneal temperature. The contact dimensions are shown in the insert.

from no change of resistance to a decrease as large as 5 orders of magnitude. Notice that boule 2004 also showed poor performance in the annealing tests reported in Fig. 3.2.5.

The samples from boule 2109 were chosen for further study by ESCA and photoluminescent measurements. The ESCA spectra of samples CS2109 not annealed and annealed at 750°C and 775°C turned out to be all identical. The main chemical species observed were Ga and As with no prominent stoichiometric deviation. O and C were also observed, as might be expected. The lack of distinction between spectra from annealed and unannealed samples is not surprising since the sensitivity of ESCA is not better than ~ 0.1%. However, this result is significant because it rules out the possibility that changes induced by heat treatment are large and localized in the top monolayers of material.

Photoluminescence measurements at 77K are being carried out on the same samples used for the ESCA measurements. Fig. 3.2.6 compares the spectrum of the sample annealed at 775°C (curve a) with the one that was not annealed (curve b). The intensity of the luminescent emission from unannealed semi-insulating GaAs (curve b) is very low indicating that non-radiative transitions dominate the recombination process. The gap luminescence peak²⁹ at 1.508 eV is greatly enhanced by annealing (curve a). A broad peak appears at 1.39 eV in the heat treated sample. This structure may correspond to a Si-As vacancy complex.³⁰

3.3 Ion Implantation

3.3.1 Sulfur Implantation

N-type layers produced by implantation of 100 keV sulfur ions into semi-insulating GaAs substrates have proven to be useful for the fabrication of

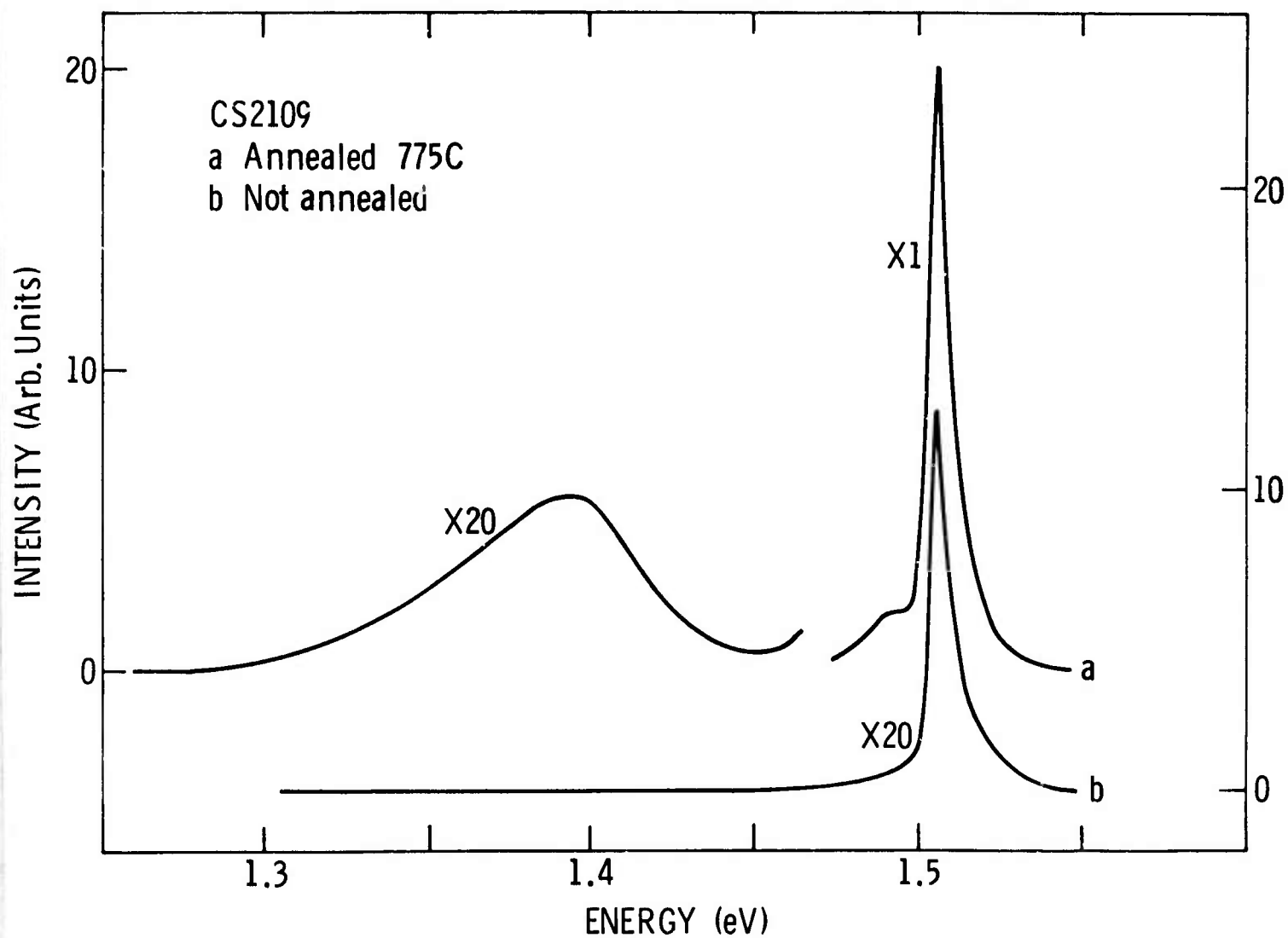


FIG. 3.2.6 Photoluminescence spectrum of a semi-insulating GaAs sample at 77K, showing the effect of heat treatment.

FETs. The devices fabricated in a given layer have been found to be quite uniform in their characteristics. We have examined the reproducibility of the doping profiles resulting from sulfur implantation into different wafers taken from the same boule of semi-insulating GaAs. Profile measurements were carried out using Schottky barrier C-V techniques. Data for a group of samples with the same implant and anneal conditions (7×10^{12} 100 keV S ions/cm² implanted at 350°C, annealed at 850°C for 30 min with a Si₃N₄ cap) show that the scatter in the value of $N_{\max}$, the maximum observed carrier concentration, was about $\pm 10\%$. The scatter in the depth at which the electron concentration was 70% or 10% of $N_{\max}$, is less than 5%. These data indicate that the reproducibility of the electron concentration profiles resulting from sulfur implantation into different samples from the same boule of semi-insulating material is quite good.

Uniformity of doping over a given wafer has also been examined. Fig. 3.3.1 shows the distribution in $N_{\max}$ and the distribution in the depth at 10% of $N_{\max}$ obtained by measuring a large number of Schottky barriers over a single sulfur implanted wafer. It can be seen that nearly all the values of $N_{\max}$ are contained within a range of 5% of either side of the most probable value. The spread in the depth at 10% of $N_{\max}$ is equally narrow. This shows that the uniformity over a given wafer can be quite good. This uniformity correlates well with the observed uniformity in characteristics of devices fabricated in similar layers.

We have recently begun to investigate the implantation of sulfur at energies higher than 100 keV. Fig. 3.3.2 shows electron concentration profiles for samples implanted with 400 keV sulfur ions at room temperature or at 350°C. These profiles show doping at depths well beyond that expected from the LSS range theory. This is also observed in the 100 keV work. In the present case, the

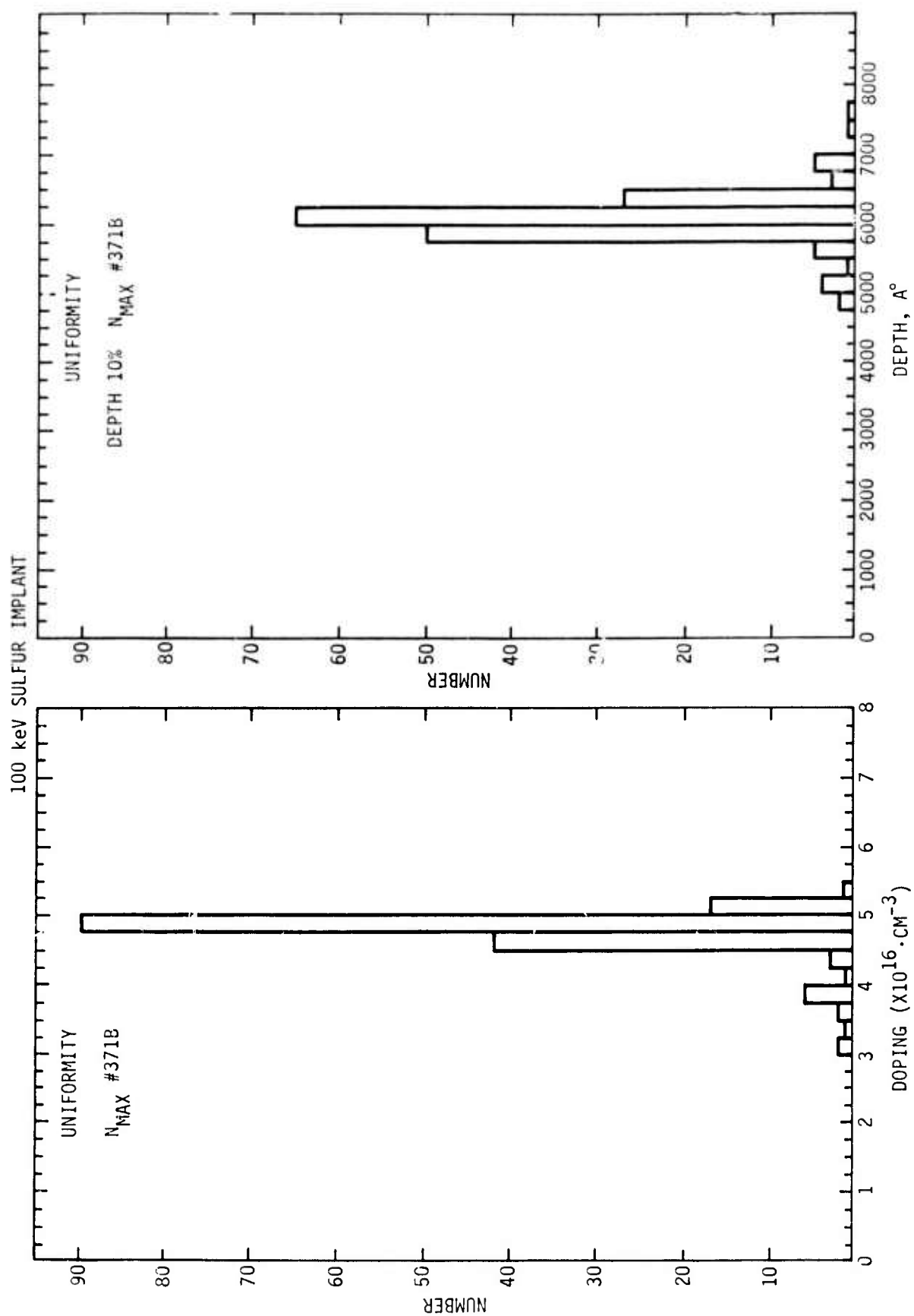


FIG. 3.3.1 Distribution of the maximum value of electron concentration obtained from Schottky barrier C-V measurements, and of the depth at which the electron concentration reached 10% of that maximum value, measured over a single S implanted layer. The implantation was carried out at 350°C with 100 keV S ions to a dose of $7 \times 10^{12} \text{cm}^{-2}$. Annealing was performed at 850°C for 30 minutes using a Si_3N_4 cap.

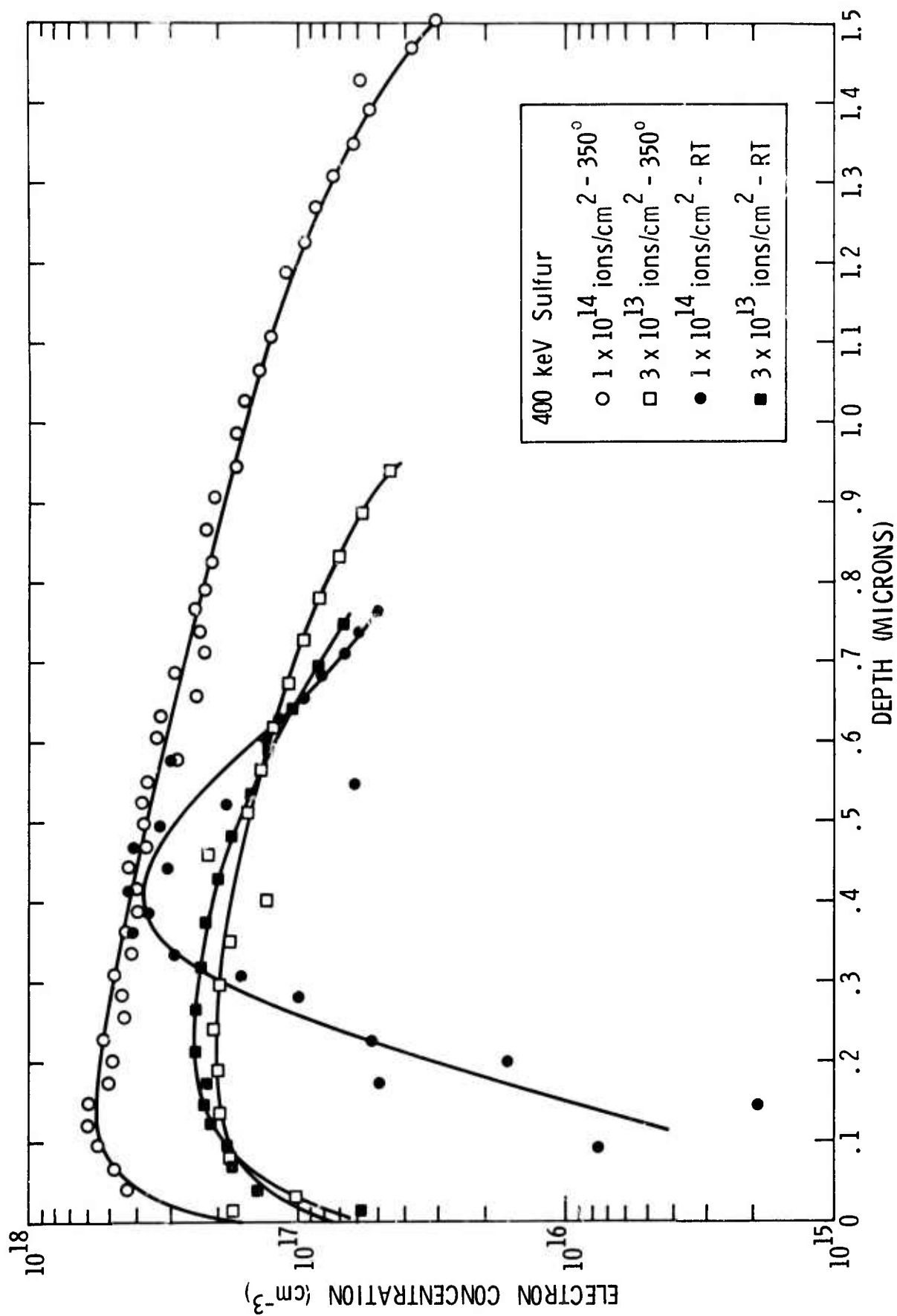


FIG. 3.3.2 Electron concentration profiles for semi-insulating GaAs samples implanted with 400 keV S ions to the indicated doses at the indicated implantation temperatures. The samples were annealed at 850°C for 30 minutes using a Si₃N₄ cap.

implanted doses are somewhat higher than those employed at 100 keV and it seems that the deviation from the LSS theory increases as the implantation dose is increased.

Previous results for the implantation of low doses of 100 keV sulfur ions indicated there was little difference in the electron concentration profiles obtained for implantation at room temperature or at 350°C. The results in Fig. 3.3.2 indicate that at a dose of 3×10^{13} ions/cm², the profiles are not greatly effected by the implantation temperature, however, when the dose is increased to 1×10^{14} ions/cm², a significant difference is observed between the room temperature and the 350°C implants. Total activation of the room temperature implant is significantly lower than that for the hot implant and the electron concentration profile is much narrower for the room temperature implant. Mobility profiles for these samples are shown in Fig. 3.3.3. As was the case for the electron concentration results, the mobility profiles for the samples implanted with 3×10^{13} ions are similar for both the room temperature and 350°C implants. However, there is a significant difference in the profiles for the samples implanted with 1×10^{14} ions/cm². In particular, the mobility for the sample implanted with 1×10^{14} ions/cm² at room temperature has a minimum in the mobility at about 2-3000Å. This is approximately the depth at which the disorder introduced during implantation would be expected to be a maximum, and suggests that the difference between room temperature and 350°C implants at this dose is at least partly due to the presence of unannealed defects. Thus, it seems that for sulfur implantation at low enough doses, the results may not be greatly effected by implantation temperature, whereas when the dose becomes high enough, significant differences between hot and room temperature implants may be expected.

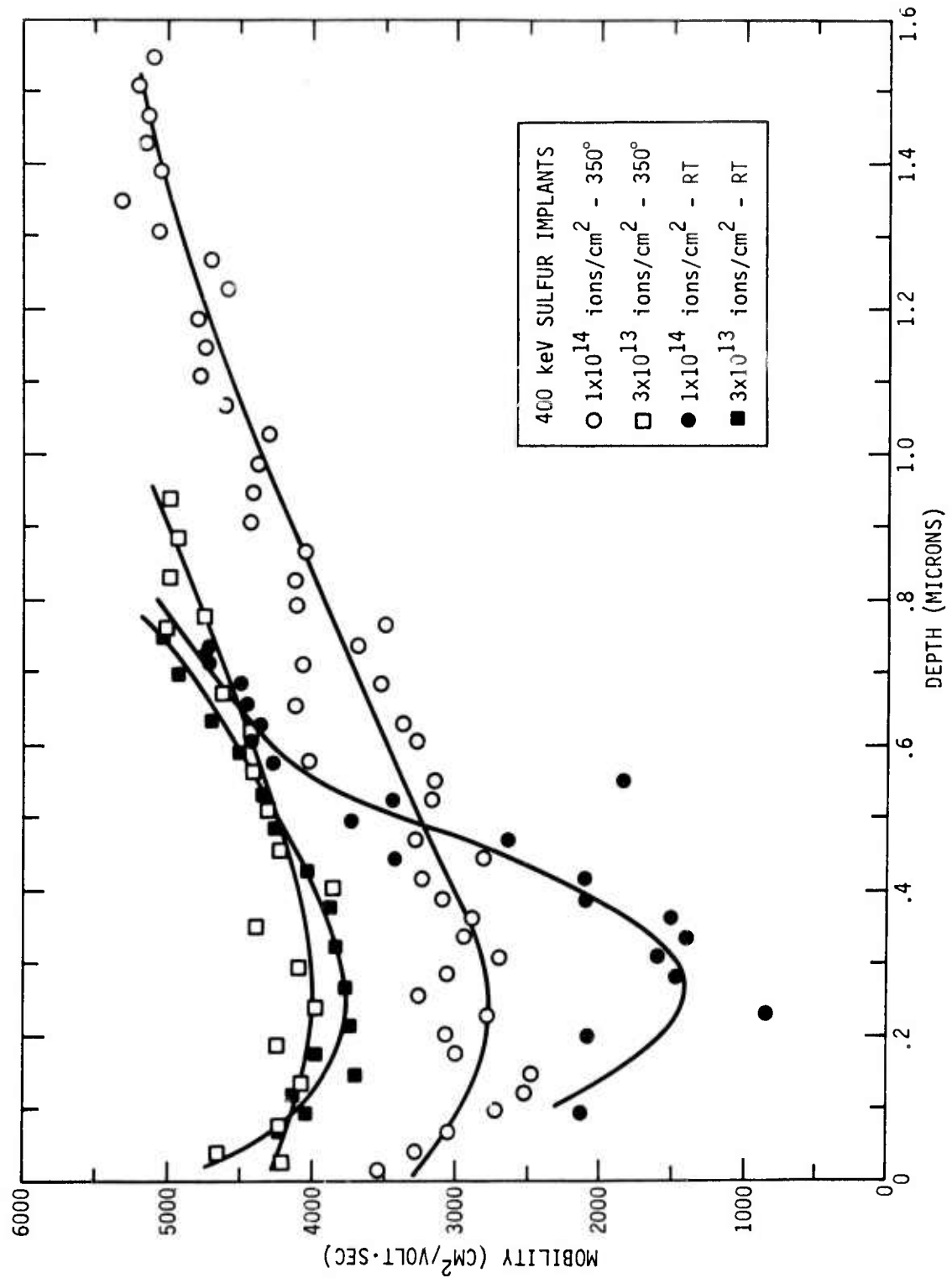


FIG. 3.3.3 Mobility profiles corresponding to the electron concentration profiles of Fig.3.3.2.

3.3.2 Selenium and Tellurium Implantation

Further investigations of high dose selenium and tellurium implants have been carried out using aluminum oxy-nitride* as the annealing cap. Fig. 3.3.4 presents results on the sheet electron concentration (n_s) measured in tellurium or selenium implanted samples as a function of the implanted dose. Data obtained from samples annealed with a silicon nitride cap are also shown for comparison. For a given cap, the selenium implanted samples yield higher values of n_s at a given dose than do the tellurium implanted samples. For both selenium and tellurium, samples annealed using an aluminum oxy-nitride cap give higher values of n_s than samples implanted with the same dose of selenium or tellurium and annealed with a Si_3N_4 cap. The selenium implantation results show a saturation in the value of n_s above doses of about $1 \times 10^{14} \text{ Se ions/cm}^2$ for 900°C anneals using either cap material. A similar saturation is apparent in the data for tellurium implanted samples annealed with a Si_3N_4 cap. For selenium implants annealed with aluminum oxy-nitride at 900°C , a decrease in the value of n_s is observed at doses above $5 \times 10^{14} \text{ cm}^2$. This decrease is eliminated by employing anneal-temperatures of 950°C .

The results in Fig. 3.3.4 indicate that higher doping can be obtained by employing selenium implantation than by using tellurium implantation. In the remainder of this Section, we will concentrate on further details of the selenium implantation results. Profiles of electron concentration and mobility obtained from tellurium implantation have been shown in the proceeding technical

* We have previously referred to this material as aluminum nitride, although it contains almost equal amounts of oxygen and nitrogen. We have decided to use the term aluminum oxy-nitride, since it is more descriptive of the composition of the material.

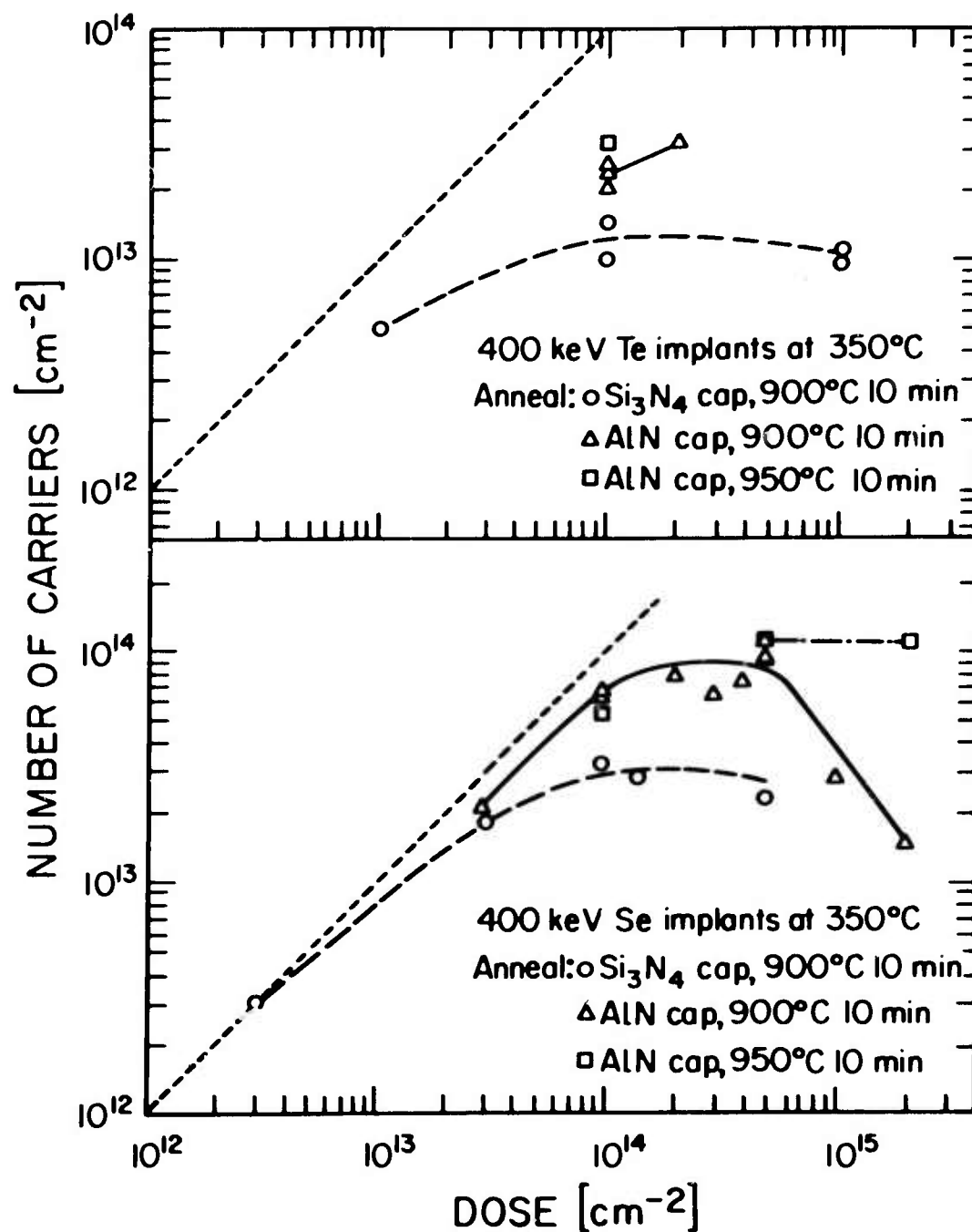


FIG. 3.3.4 Sheet electron concentration vs. implanted dose for 400 keV Se and Te implants carried out at 350°C. Annealing conditions for the various samples are indicated on the figure.

report.³ A comparison of electron concentration and mobility profiles for selenium implanted samples using the two different annealing caps is shown in Fig. 3.3.5. The electron concentration profile obtained using Si_3N_4 reaches a maximum electron concentration of about $1 \times 10^{18} \text{ cm}^{-3}$ and is relatively flat over a depth of several thousand Å. The profile obtained when an aluminum oxy-nitride cap was used, reaches a maximum electron concentration of about 3×10^{18} and exhibits a more peaked distribution than that obtained from the sample annealed with a Si_3N_4 cap. The mobility measured in the sample annealed with aluminum oxy-nitride is also higher than that obtained from the sample annealed with Si_3N_4 . This difference in mobility has been observed for several different selenium doses as shown in Table 3.3-1.

The profiles obtained in selenium implanted samples for various doses using an aluminum oxy-nitride cap and an annealing temperature of 900°C are shown in Fig. 3.3.6. The maximum electron concentration increases with increasing dose up to $5 \times 10^{14} \text{ cm}^{-2}$ and then shows a decrease for doses of 1 or $2 \times 10^{15} \text{ cm}^{-2}$. For these two highest dose implants, the maximum electron concentration occurs at a depth well beyond the projected range of the implanted selenium ($\sim 1370\text{Å}$). At depths comparable to this projected range where most of the implanted selenium should be located, the electron concentration for doses of 1×10^{15} and 2×10^{15} is lower than that for any of the other doses for which data is shown. As pointed out in the previous report³, annealing these high dose samples to higher temperatures results in improved activation of the implanted selenium at depths comparable to the projected range. In Fig. 3.3.6, two profiles are shown for an implantation dose of $5 \times 10^{14} \text{ cm}^{-2}$. The sample material was taken from different boules of chrome doped GaAs but, otherwise, the implantation and anneal conditions were similar. The reproducibility of the electron concentration near

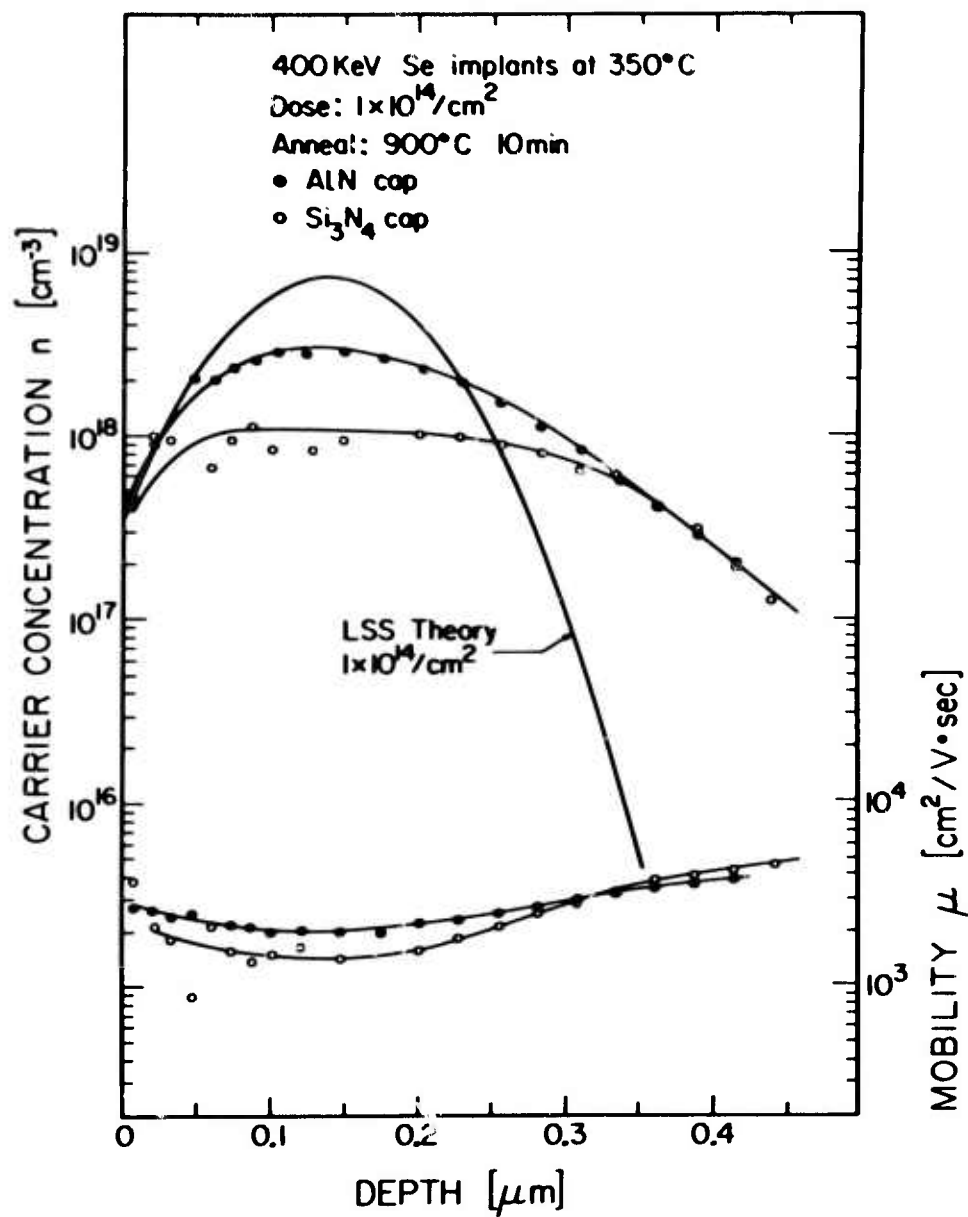


FIG. 3.3.5 Electron concentration and mobility profiles for semi-insulating GaAs samples implanted with 400 keV Se ions at 350°C to a dose of $1 \times 10^{14} \text{cm}^{-2}$. Annealing was carried out at 900°C for 10 minutes with the annealing cap indicated on the figure.

TABLE 3.3-1

CARRIER CONCENTRATION AND MOBILITY AT THE LSS PROJECTED
 RANGE FOR 400 keV Se. SAMPLES WERE ANNEALED AT 900°C
 USING Si_3N_4 OR ALUMINUM OXY-NITRIDE CAPS.

DOSE (cm^{-2})	Si_3N_4		ALUMINUM OXY-NITRIDE	
	$n(\text{cm}^{-3})$	$\mu(\text{cm}^2/\text{V-sec})$	$n(\text{cm}^{-3})$	$\mu(\text{cm}^2/\text{V-sec})$
3×10^{13}	7×10^{17}	2500	1×10^{18}	2900
1×10^{14}	1×10^{18}	1500	3×10^{18}	2000
5×10^{14}	5×10^{17}	1100	3.6×10^{18}	1200

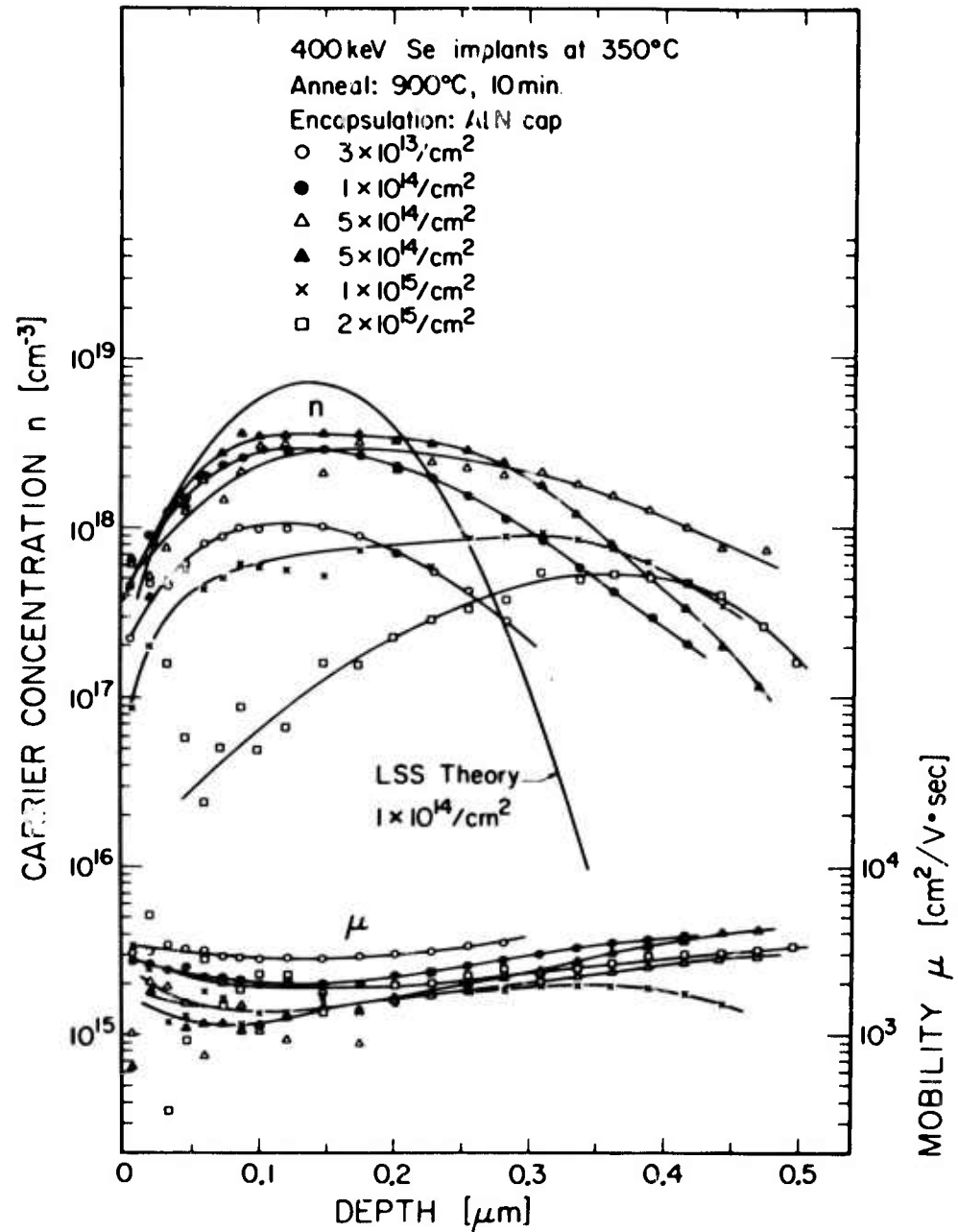


FIG. 3.3.6 Electron concentration and mobility profiles for semi-insulating GaAs samples implanted with 400 keV Se ions at 350°C to the doses indicated on the figure. Annealing was carried out at 900°C for 10 minutes using an aluminum oxy-nitride cap.

the peak region was quite reasonable, but at greater depth these profiles deviated somewhat from each other. It is not clear whether this difference is due to differences in selenium penetration because of diffusion or channeling effects, or to differences in substrate behavior.

During implantation, the GaAs samples are tilted about 10° from the beam direction in order to minimize axial channeling. However, no special precautions are taken with regard to the planar orientation so that planar channeling in some samples may be possible. Fig. 3.3.7 shows profile results from two samples implanted with a dose of 1×10^{14} Se ions/cm². One sample was aligned by proton backscattering so that the beam was incident parallel to {110} planes. The other sample was oriented by backscattering so as to minimize all planar channeling effects and is labeled "random". The electron concentrations obtained in the region of the peak are about the same for both samples but the data for the sample which was aligned for planar channeling shows a somewhat deeper tail than the data for the random implant. This indicates that channeling may contribute to the rather deep penetration of the doping observed in some selenium implants. The random curve, however, also extends somewhat beyond the selenium distribution predicted by the LSS theory. This suggests the diffusion may also play a role in the deep penetration of the doping. It is likely that this is not normal diffusion of the selenium, but enhanced diffusion due to the defects which are present in the sample following implantation.

Electron concentration and mobility profiles for samples implanted with a dose of 5×10^{14} Se ions/cm² and annealed at different temperatures are shown in Fig. 3.3.8. A large increase in the carrier concentration is seen to occur when the annealing temperature is increased from 850° to 900° C. An increase in the mobility in the region of the selenium projected range also occurs

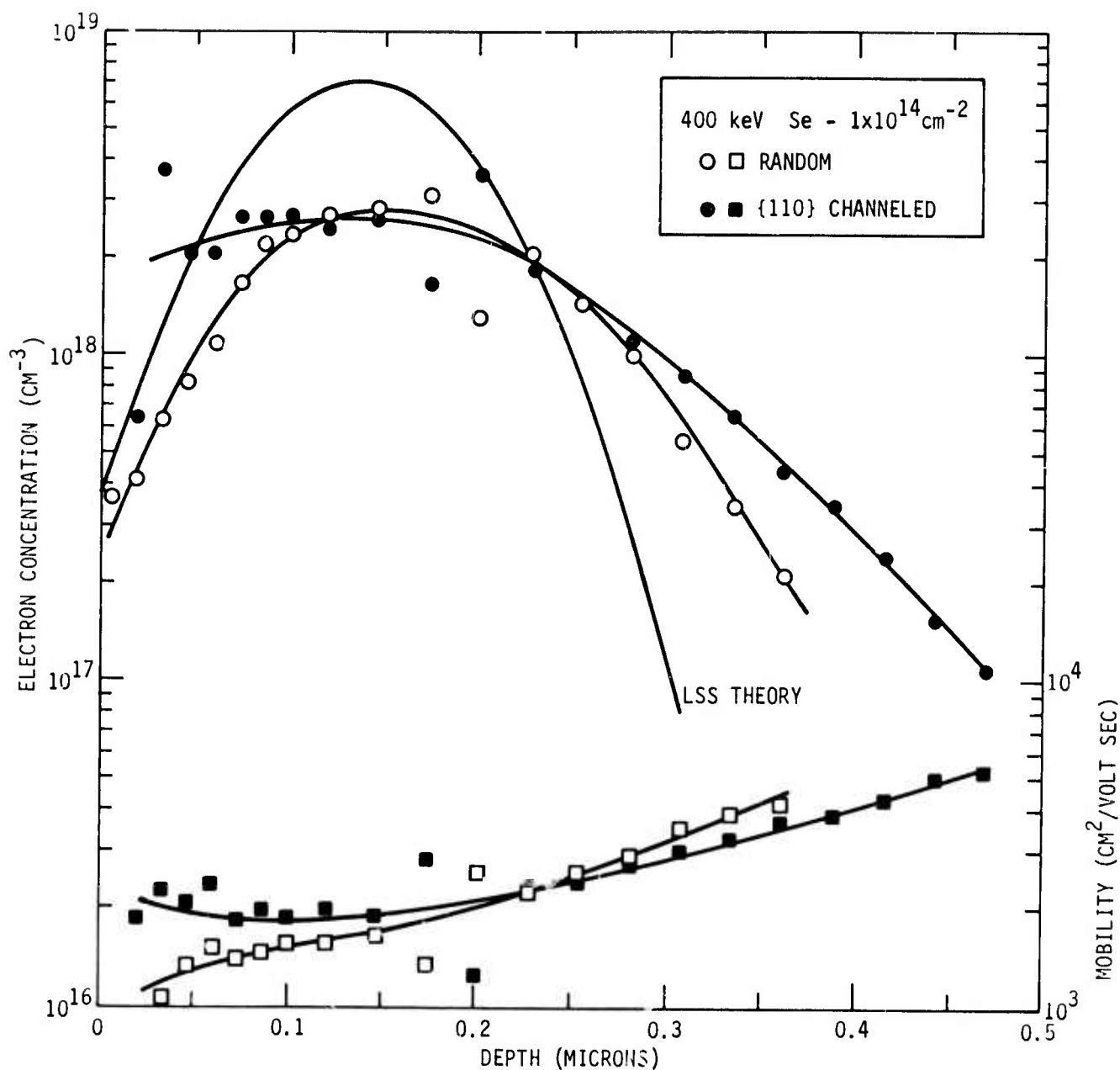


FIG. 3.3.7 Electron concentration and mobility profiles for semi-insulating GaAs samples implanted at 350°C with 1×10^{14} 400 keV Se ions. The sample labeled "random" was implanted with the beam incident in a direction chosen to minimize planar and axial channeling. The sample labeled "110 channeled" was implanted with the beam aligned parallel to 110 planes. The alignments were determined by proton backscattering. Annealing was carried out at 900°C for 10 min using an aluminum oxy-nitride cap. The range distribution for 400 keV Se ions as determined from the LSS theory is also indicated on the figure.

with this increase in annealing temperature. In the region of the tail of the profiles, that is at depths of greater than about 2-3000Å, the differences in electron concentration for the different samples are not as great as they are in the neighborhood of the projected range of the selenium. This indicates that higher annealing temperatures are required to achieve high activation of the selenium at the depth where its concentration is highest.

The data from Fig. 3.3.8 are presented in a different way in Fig. 3.3.9 where the mobility is plotted vs. carrier concentration for the different profiles presented in Fig. 3.3.8, and a comparison is made with the mobility data of Sze and Irvin³¹ for GaAs. It can be seen that as the depth increases, the mobility approaches fairly closely to the Sze and Irvin curve with the exception of the data for the sample annealed at 950°C. The behavior of the data for this sample is not understood at present.

Doping efficiency vs. anneal temperature is plotted for several different implant doses in Fig. 3.3.10. It can be seen that for doses of 1×10^{14} and 5×10^{14} , there is a significant increase in doping efficiency when the anneal temperature is increased from 850°C to 900°C. For a dose of $2 \times 10^{15} \text{ cm}^{-2}$ a similar increase in doping efficiency occurs at a higher temperature, that is, between 900 and 950°C. On the other hand, at a dose of $3 \times 10^{13} \text{ cm}^{-2}$, the doping efficiency is as high at 850°C as it is at 900°C. The anneal temperature required to obtain the highest observed doping efficiency for any particular dose is, therefore, seen to be a fairly strong function of the dose of the implanted selenium. The mechanisms responsible for this dependence of annealing temperature on dose are not entirely clear at present. An indication of one of the factors involved, however, is seen in Fig. 3.3.11 where photoluminescence data for two samples implanted with doses of $1 \times 10^{14} \text{ Se ions/cm}^2$ are presented. One sample was anneal-

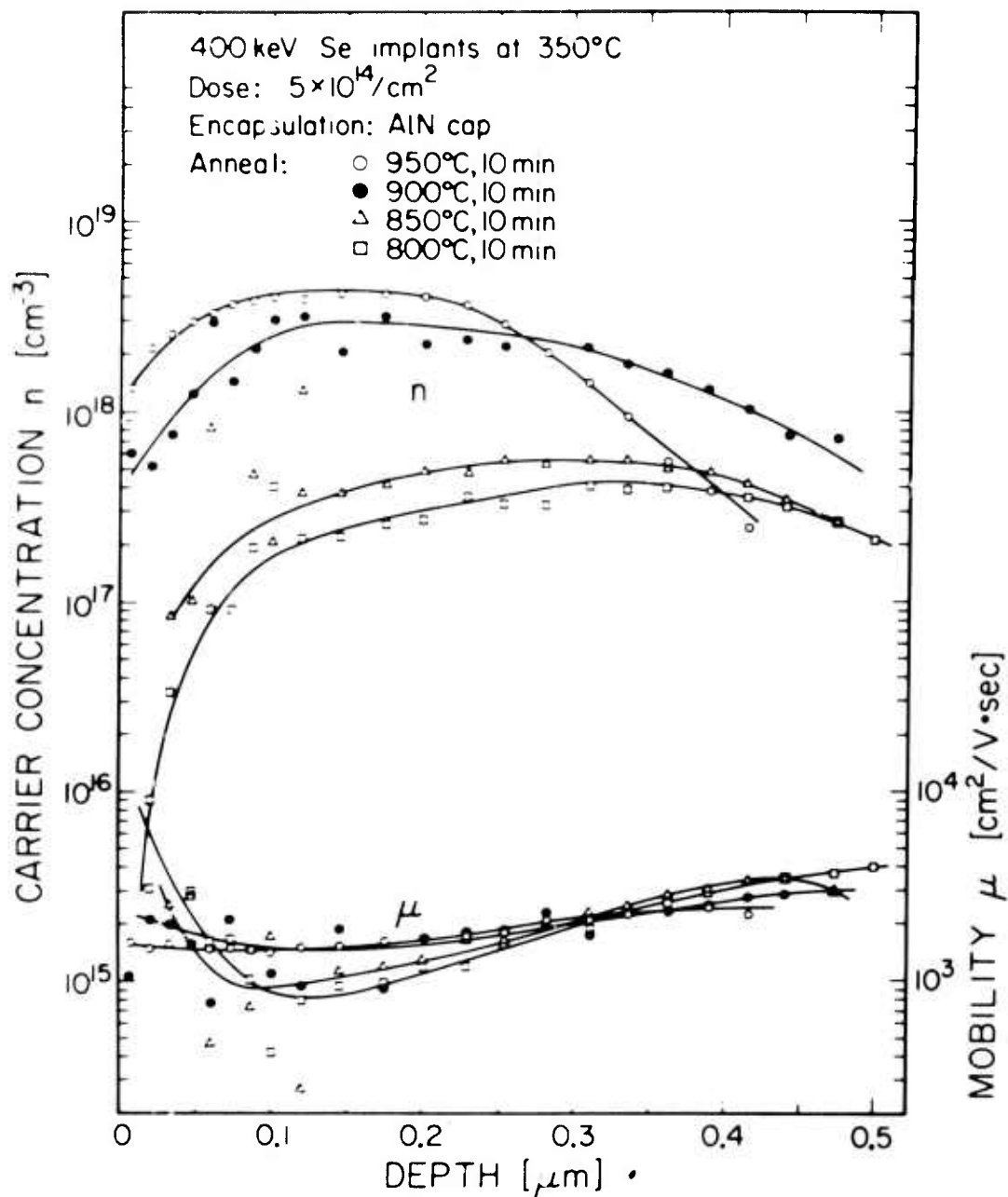


FIG. 3.3.8 Electron concentration and mobility profiles for semi-insulating GaAs samples implanted with 400 keV Se ions at a temperature of 350°C to a dose of $5 \times 10^{14} \text{cm}^{-2}$. Annealing was carried out using an aluminum oxy-nitride cap at the temperatures indicated on the figure for a period of 10 minutes.

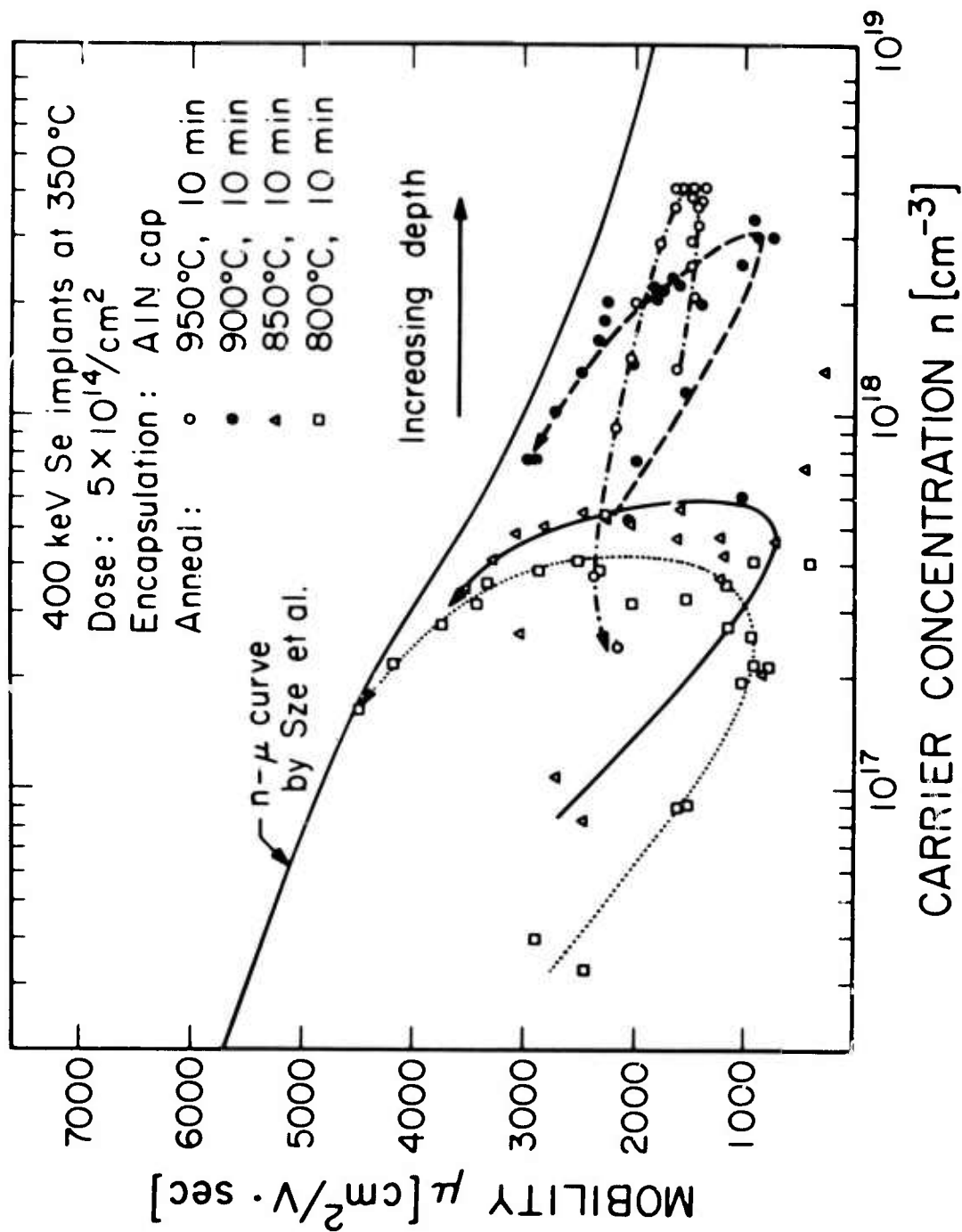


FIG. 3.3.9 Mobility vs. carrier concentration plotted for the data shown in Fig. 3.3.8.

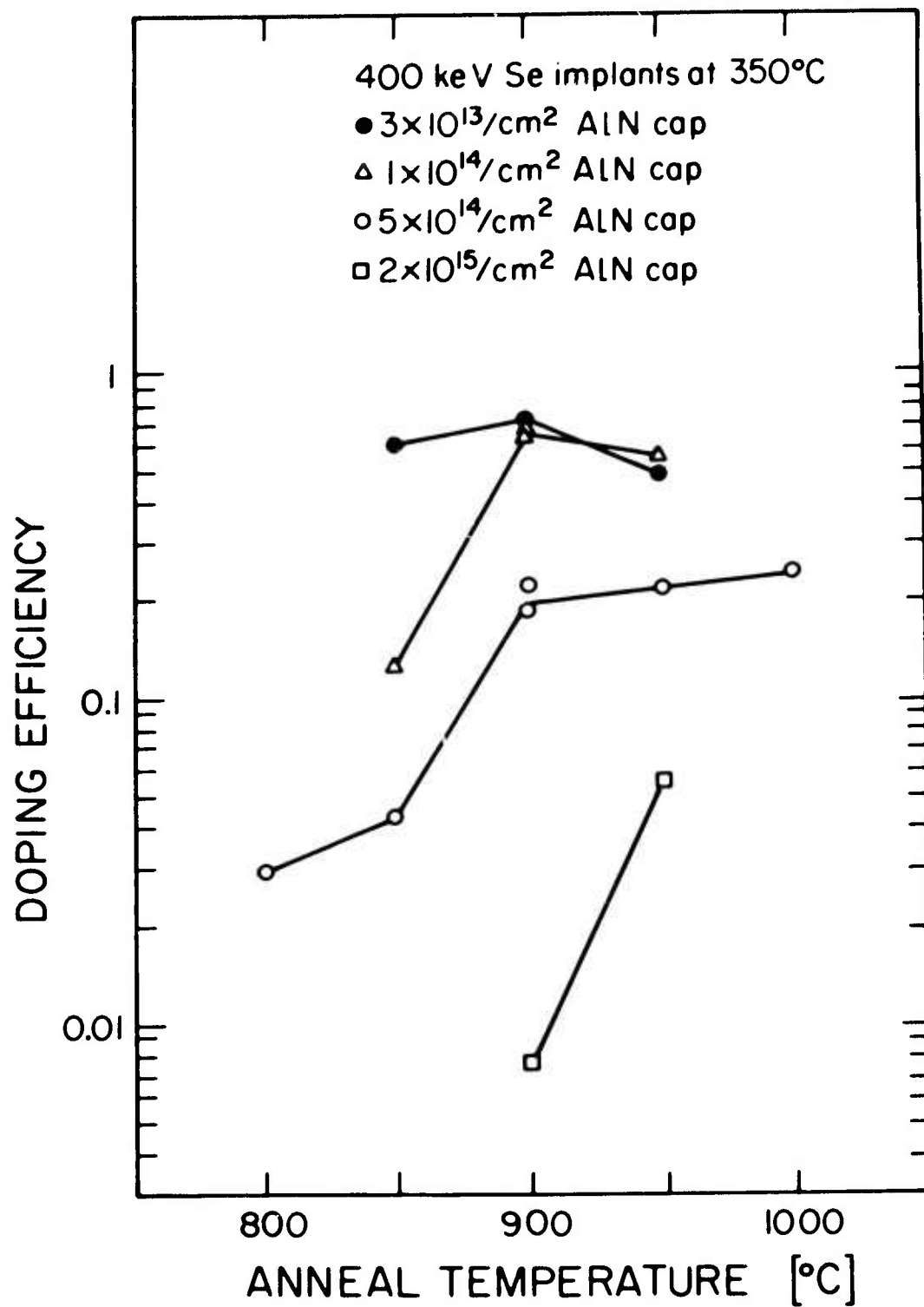


FIG. 3.3.10 Doping efficiency vs. annealing temperature for semi-insulating GaAs samples implanted at 350°C with 400 keV Se ions to the doses indicated on the figure. Annealing was carried out using an aluminum oxy-nitride cap.

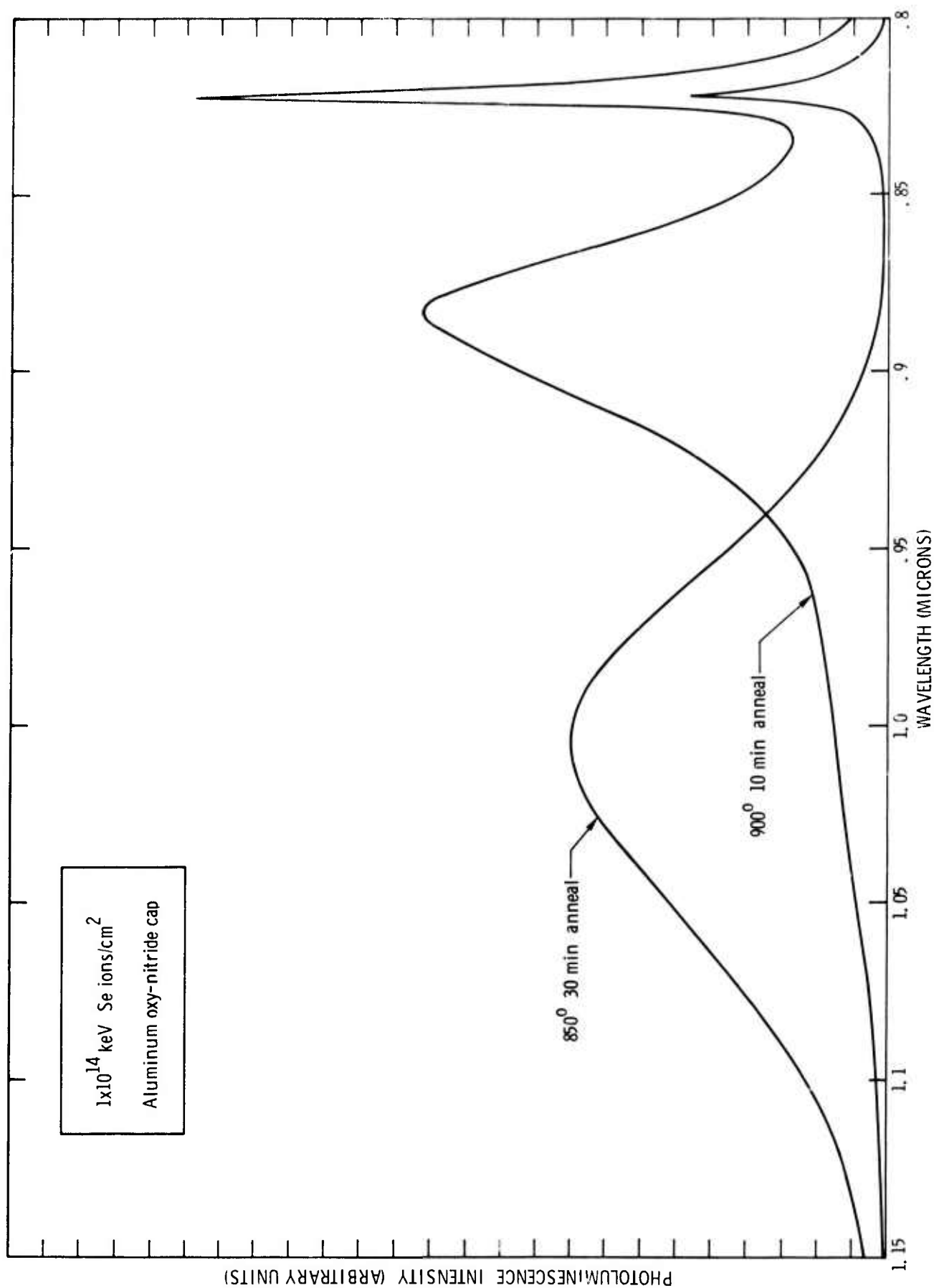


FIG. 3.3.11 Photoluminescence spectra obtained from semi-insulating GaAs samples which were implanted with 400 keV Se ions at a temperature of 350°C to a dose of 1×10^{14} cm⁻². Annealing was carried out using an aluminum oxy-nitride cap at the temperatures and for the times indicated on the figure.

ed at 850°C with an aluminum oxy-nitride cap, and the other annealed at 900°C with the same type of cap. The data for the sample annealed at 850°C shows a very large photoluminescence peak at a wavelength of $1\mu\text{m}$. This peak is believed to be associated with gallium-vacancy-selenium acceptor complexes in the sample. The data for the sample annealed at 900°C shows a very large decrease in the intensity of this gallium-vacancy-selenium complex. At the same time a peak appears at a wavelength of about $8900\text{\AA}$. We believe that this peak may be associated with arsenic vacancy complexes in the GaAs. These results indicate that the large increase in doping efficiency observed in this range of anneal temperature for a dose of 1×10^{14} is associated with a significant decrease in the number of gallium-vacancy-selenium complexes present in the sample following anneal at 900°C as compared to the number of such complexes present following anneal at 850°C.

The results presented in this report and the proceeding one show that selenium implantation, together with the use of aluminum oxy-nitride as an annealing cap, is capable of producing highly doped regions in GaAs. There are several features of the behavior of implanted selenium in GaAs which one would like to understand. These include the dependence of annealing temperature upon the implanted dose, the fact that carrier concentrations higher than about 4×10^{18} have not been observed even at the highest doses, and the differences in carrier concentration observed depending on whether the annealing is carried out using an aluminum oxy-nitride cap or a silicon nitride cap. It is not possible to completely understand these points at the present time, however, some suggestions of factors which may be important can be made.

It is clear that, in order to achieve high doping efficiency and high electron concentrations in GaAs by selenium implantation, the concentration of

gallium-vacancy-selenium complexes in the implanted layer must be low. However, a low concentration of these complexes does not necessarily guarantee as high an electron concentration as might be expected from work on melt grown, selenium doped, GaAs. For example, photoluminescence measurements on a sample implanted with a dose of 5×10^{14} Se ions/cm² and annealed at 950°C with an aluminum oxy-nitride cap (profile shown in Fig. 3.3.9) show almost no emission at 1μm, indicating a very low concentration of gallium-vacancy-selenium complexes. However, the maximum electron concentration measured for this sample is only about 4×10^{18} cm⁻³. Data for melt grown, selenium doped, GaAs indicate that a maximum electron concentration of about 6×10^{18} cm⁻³ would be expected at the peak of the selenium distribution where the selenium concentration should be about 3.5×10^{19} .³² This tends to indicate that some factor other than gallium-vacancy-selenium acceptor complexes plays a role in limiting the maximum electron concentration attained. It is, of course, possible that the implanted selenium is not all located on substitutional lattice sites. This question has not been examined directly but lattice location measurements for implanted tellurium using channeling techniques indicate that the tellurium is highly substitutional following hot implantation and following subsequent annealing. Another possibility is that as the dose of selenium is increased, damage effects become more important, and a significant amount of the implanted selenium is compensated by unannealed damage centers. The presence of such compensating damage centers could also play a role in the increased annealing temperature required for samples implanted with doses above 10^{15} ions/cm². Further experiments would be required to determine whether or not such compensating centers are actually present in implanted GaAs samples following annealing.

Photoluminescence data presented in this report and in the proceeding

one suggest that arsenic vacancies may be introduced into the sample during annealing with an aluminum oxy-nitride cap. The introduction of these vacancies may facilitate the disassociation of gallium-vacancy-selenium complexes leading to higher observed doping efficiencies. On the other hand, the photoluminescence data do not show any indication of arsenic vacancy introduction when annealing is carried out with a silicon nitride cap. This may partially account for a lower doping observed when silicon nitride is used as the annealing cap. However, it is not clear at present whether or not there may be other factors involved in the difference observed between samples annealed with silicon nitride and samples annealed with aluminum oxy-nitride.

3.4 Theoretical and Experimental Investigation of the Effect of Material Parameters on Device Performance

3.4.1 Characterization of FETs Fabricated on Ion Implanted and LPE Materials - Science Center

As stated in our previous report,³ the activity at the Science Center in this area has been to compare MESFET devices made from liquid phase epitaxy and ion implantation. The measurements are of rf gain and noise figure and of variation of these with bias level. In addition, measurement of noise at low-frequency has been used because this is a comparatively simple test to perform and might indicate to some degree the quality of a MESFET in a quick manner.

In this report, some preliminary data on noise figure measurements at 10 GHz and their dependence on bias levels will be presented. This dependence may be indicative of the presence of interface states in epitaxial layers.

The data presented here have been obtained from a comparison of epitaxial and ion implanted transistors where the substrate material used in both cases has been monitored. In the case of the epitaxial transistors (batch 43a),

the epitaxial layer was grown onto a substrate of low chromium content. This substrate was Crystal Specialties #1718 and is described in Section 3.2.2.1. The ion implanted MESFETs (numbered 523) employed a selenium-implanted layer in a substrate which had a $7.8 \times 10^{15} \text{ cm}^{-3}$ chromium content (Crystal Specialties #2004).³ Substrate #2004 had shown the tendency to form a conducting layer in heat treatment tests (see Section 3.2.2.2). This is a potential cause of interface problems in MESFETs of epitaxial origin.

MESFETs 523 #1 and 43a #6 were measured for noise figure at 10 GHz. Both showed good noise figures (≈ 3.8 dB for 523 #1, and ≈ 4 dB for 43a #6). The key observation is depicted in Fig. 3.4.1 where the effects of perturbation in gate bias away from optimum (for noise) produce different effects in each device. In the device of ion implanted origin, the noise figure returns to the steady state optimum with little delay, whereas in the epitaxial device upon return of the gate bias to its steady state, there is considerable delay in the return of the noise figure. Furthermore, the noise figure may return to its steady state from a higher or lower value according to which way the gate bias was perturbed. This effect is of considerable interest and is being studied further. Presently, it is thought to have its origin in the presence or absence of interface states at the active layer-insulating bulk boundary where the deep centers described by Asai, et al.,³³ may play an important part.

3.4.2 Determination of Diode Microwave Parameters from Low Frequency Noise Data and Microwave Admittance Measurements - Cornell University

The theoretical development of the short circuit current fluctuations in an avalanche junction diode that was presented in the last semi-annual report³ demonstrated that the multiplication and saturation current could be determined at the noise peak. A surprising feature common to the variety of

TIME CONSTANT EFFECTS IN NOISE FIGURE IN GaAs FETS

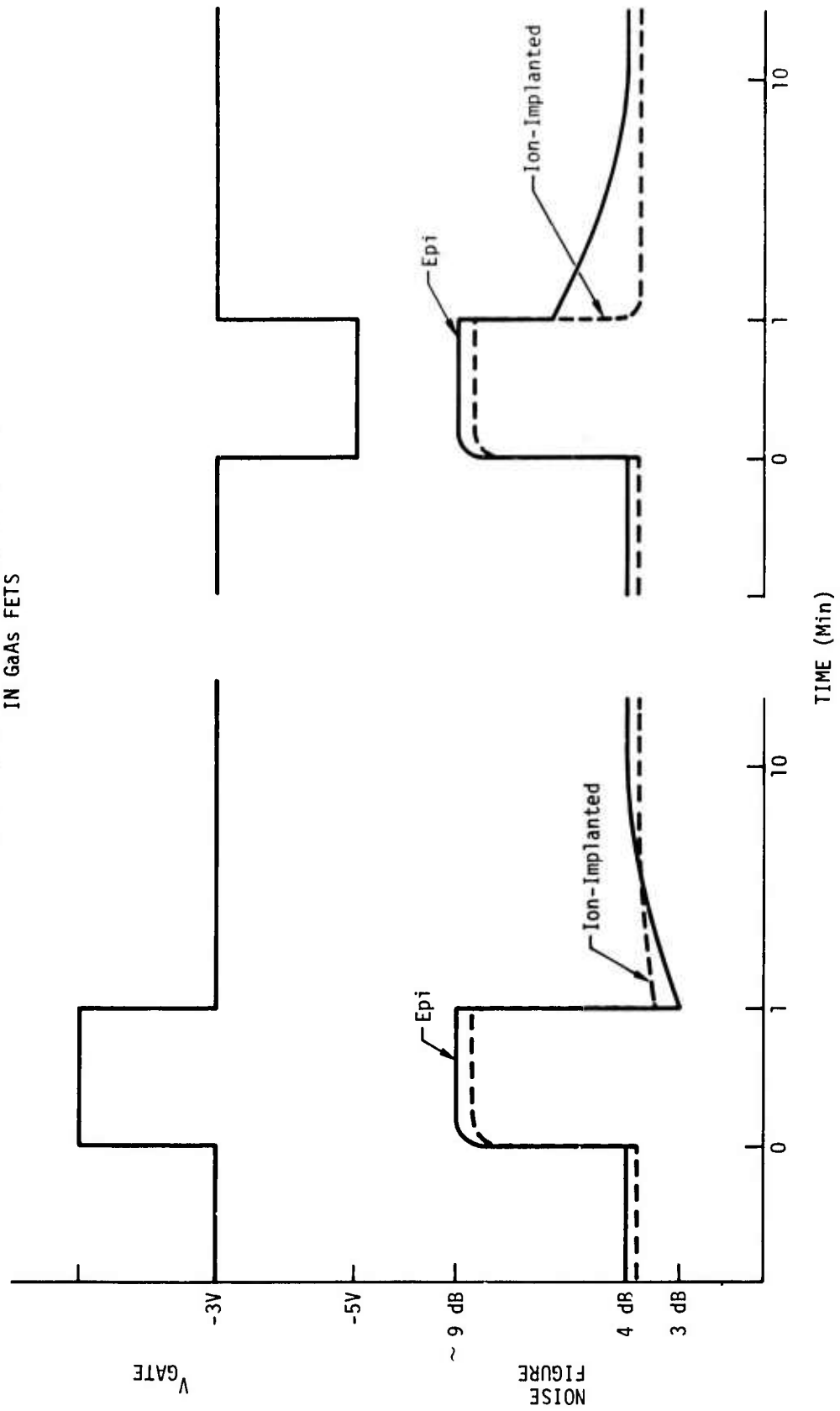


FIG. 3.4.1 Time Constant Effects in Noise Figure
in GaAs FETs.

diodes measured was the relatively low values of multiplication and high saturation current. GaAs diodes, in spite of the larger bandgap compared to that of silicon, had saturation currents approximately an order of magnitude larger than silicon diodes.

A tacit question that was not addressed explicitly was how the multiplication and saturation current characteristic of the operating range of the diode were related to the values obtained at the noise peak. A related question is why the large variation in junction temperature seemingly does not effect the fitting of the experimental curves. The answer to both of these questions lies in the fact that very quickly after the noise peak is past, the mean square current fluctuations become proportional to the reciprocal of the bias current. Thus, only the product of the strongly temperature dependent multiplication and saturation current can be observed. The only other strongly temperature dependent parameter is the scattering limited velocity, and its temperature dependence is not strong enough to seriously affect the fitting of the experimental curves.

An explicit picture of how the multiplication and saturation current vary over the operating range of the diode can be obtained utilizing the results of the noise analysis. If one assumes that at the noise peak the junction temperature is essentially at room temperature, the junction temperature at higher bias currents can be calculated from the thermal impedance of the mount and the electrical dissipation. The particular temperature dependence of the saturation current can be separately measured below breakdown so that the saturation current as a function of the bias current can be calculated. Dividing the bias current by the saturation current then yields the multiplication. The results of such a calculation are shown in Fig. 3.4.2 for one of the silicon diodes. Although the multiplication is relatively high at low bias currents, it falls to a value less

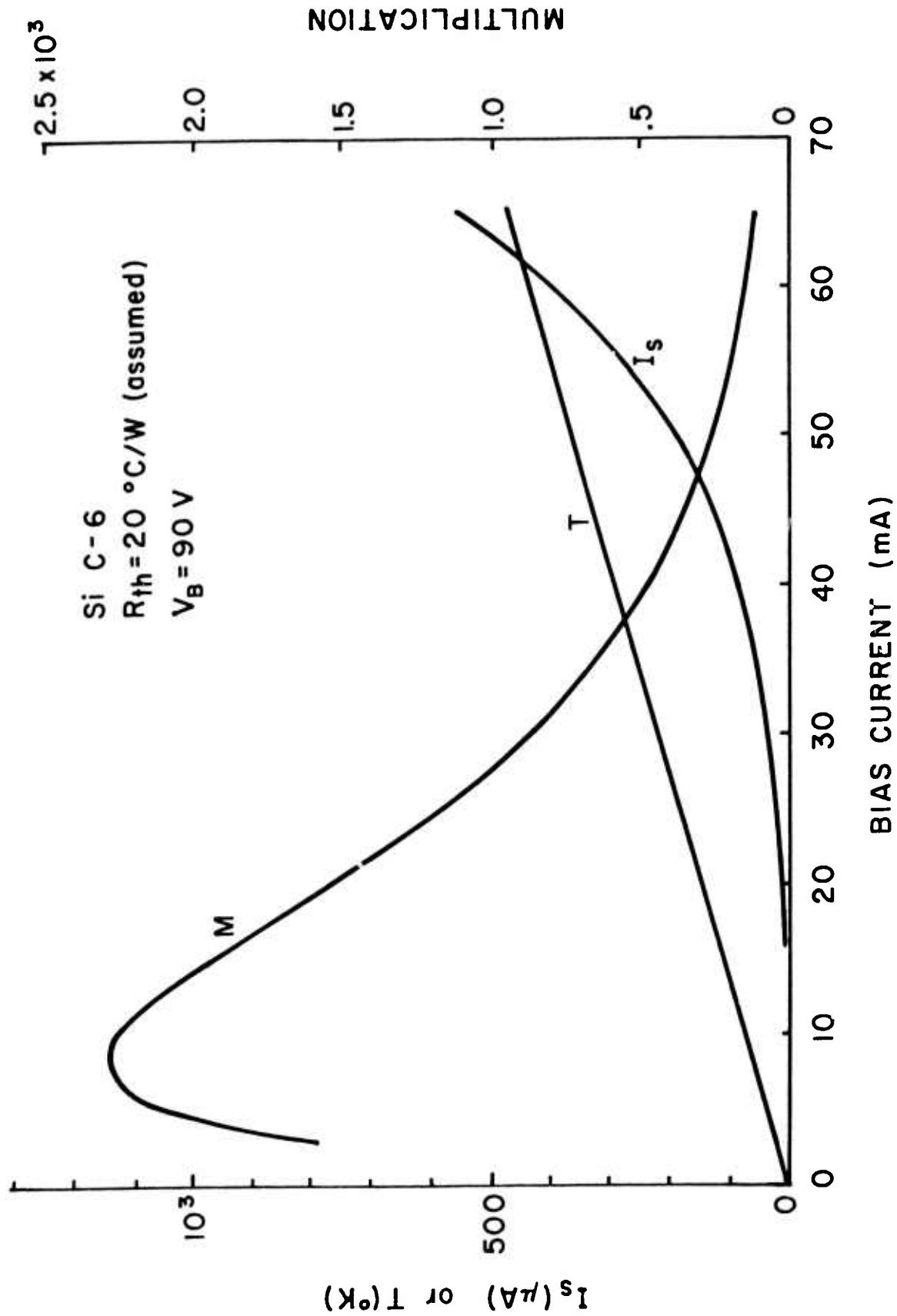


FIG. 3.4.2 Variation of multiplication and saturation current in an IMPATT diode as a function of the bias current.

than a hundred at a bias corresponding to approximately half its rated power output.

The first noise measurements were taken at 30 MHz where the intrinsic response time of the avalanche has a negligible effect upon the noise. At higher frequencies the effect of τ_1 is to reduce the noise monotonically. The analytical determination of the intrinsic response time is relatively simple. The expression previously derived³ for the short circuit noise current in an avalanche diode was

$$\langle i^2 \rangle = a' I^3 / \left[(1 + b' I^2)^2 + c' I^2 (1 - d' I) \right], \quad (15)$$

where $a' = 2e\Delta f / I_S^2$, $b' = |a_1| \tau_1 (w - x_1)^2 / 2\epsilon w v_s A I_S$, $c' = (\omega \tau_1 / I_S)^2$, and $d' = |a_1| (w - x_1)^3 / 3\epsilon w v_s^2 A$. Examination of Eq. (15) shows that the only frequency dependent term is c' ; the intrinsic response time is obtained by merely inverting Eq. (15) and differentiating with respect to ω^2 ,

$$\tau_1^2 = \frac{a' I}{(1 - d' I)} \frac{d}{d\omega^2} \left(\frac{1}{\langle i^2 \rangle} \right), \quad (16)$$

where $a' = 2e\Delta f$. The change in Eq. (15) with frequency is illustrated in Fig. 3.4.3 where an intrinsic response time of 3 ps has been assumed.

The following two graphs, Figs. 3.4.4 and 3.4.5 show recorder tracings of the short circuit noise current of a silicon diode at 30 and 420 MHz. Applying Eq. (16) to the data of Figs. 3.4.4 and 3.4.5 yields an intrinsic response time of 4 ps. A numerical calculation of the intrinsic response time using the "Quasistatic" approximation^{34,35} gives $\tau_1 = 2.7$ ps without taking into account high field diffusion effects. Including diffusion would increase the response

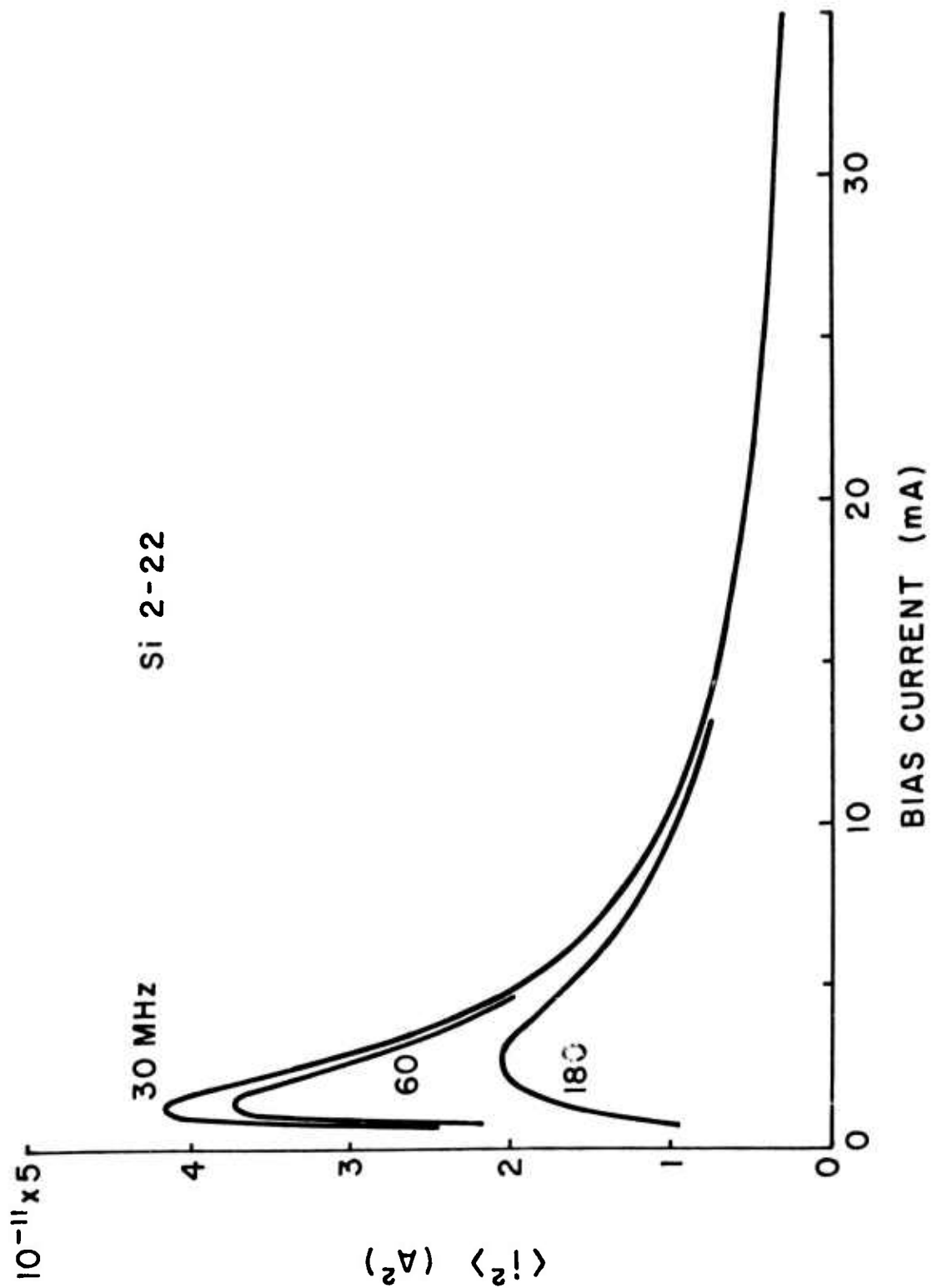


FIG. 3.4.3 Calculated mean square current fluctuation vs. bias current for 30, 60, and 180 MHz.

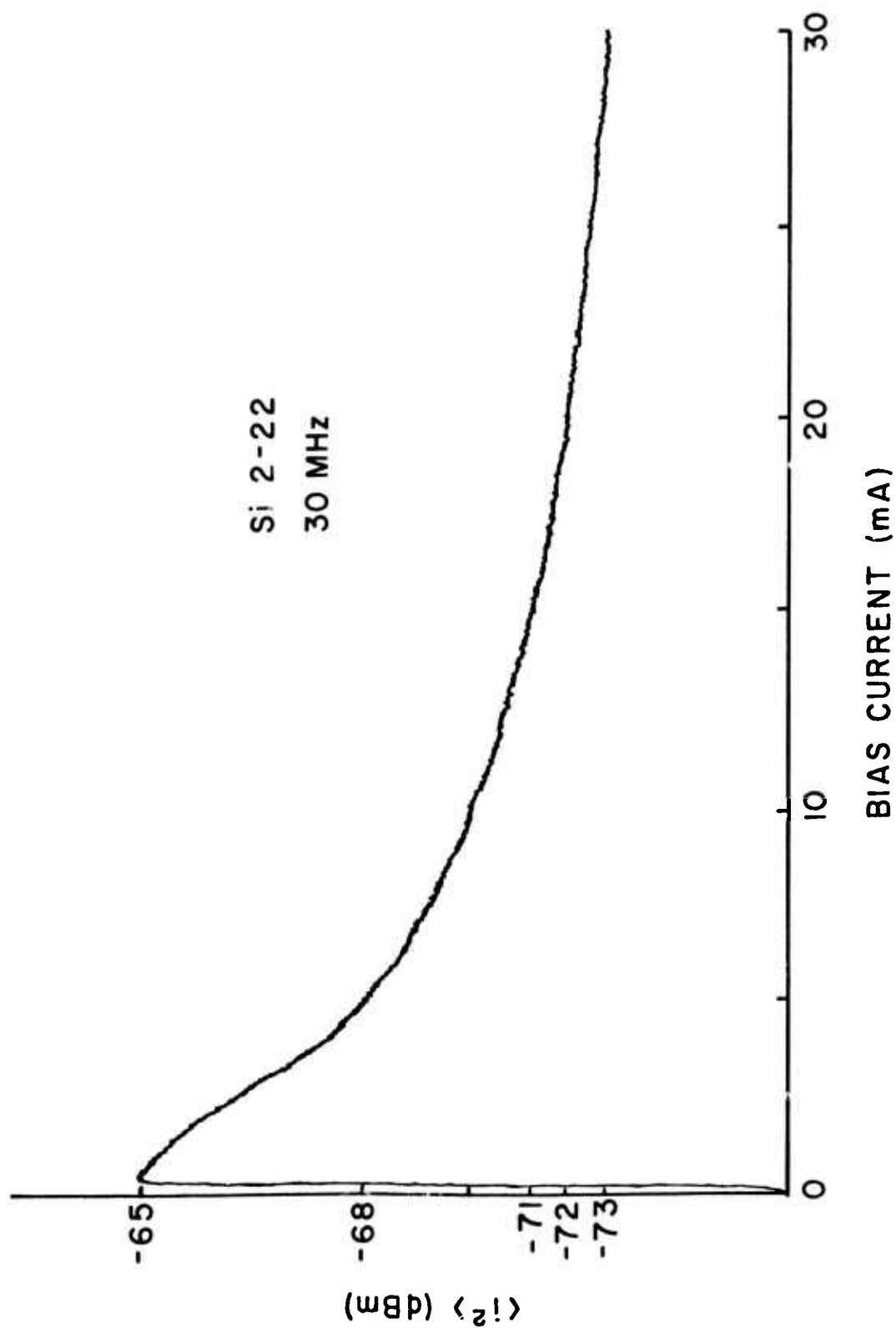


FIG. 3.4.4 Experimental mean square current fluctuation vs. bias current at 30 MHz for diode Si 2-22.

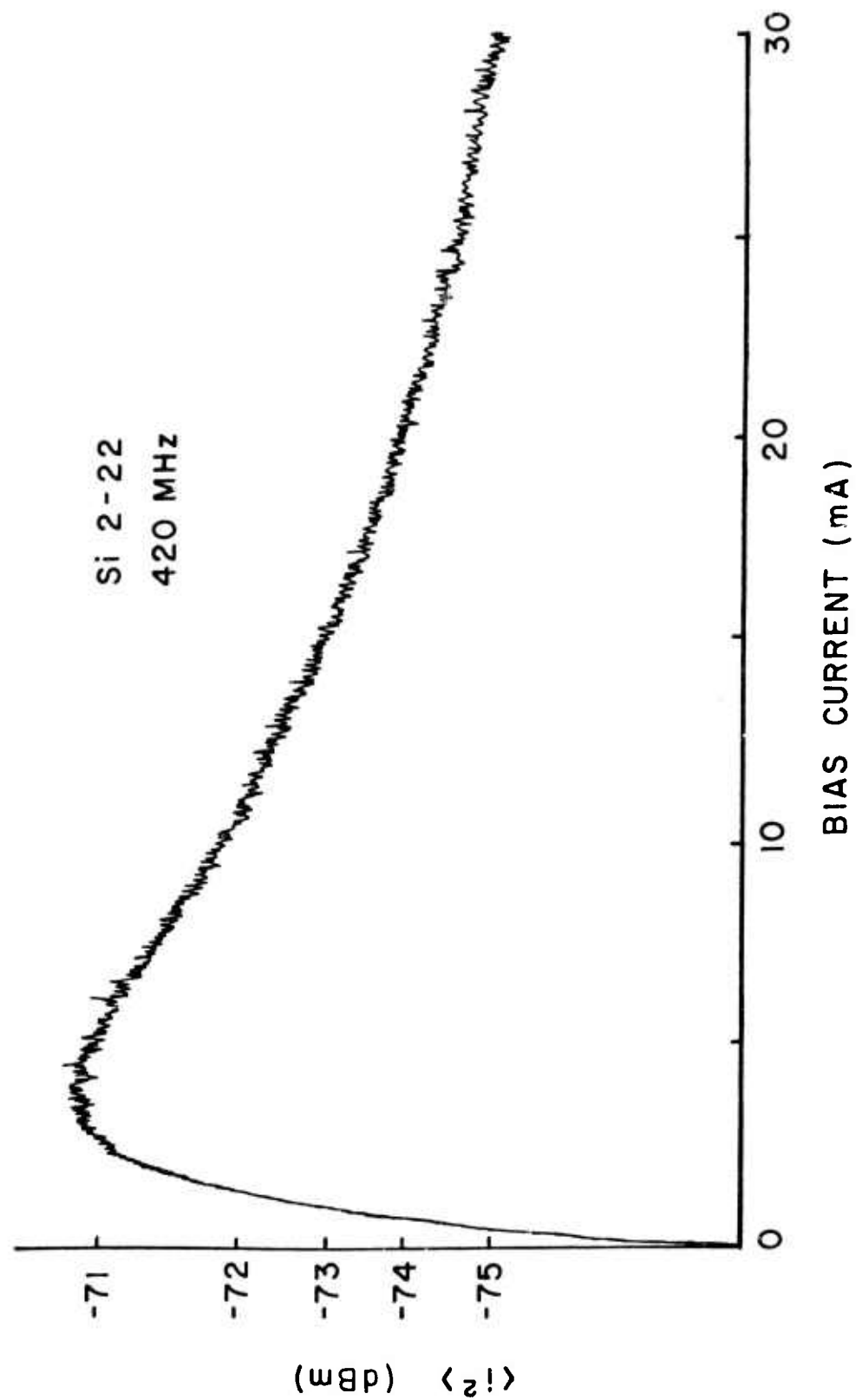


FIG. 3.4.5 Experimental mean square current fluctuation vs. bias current at 420 MHz for diode Si 2-22.

time giving reasonable agreement between theory and experiment. Having shown reasonable agreement in silicon, we proceed to the data on GaAs diodes where we shall see that although the parameters derived from the noise and microwave admittance measurements are in good agreement, the measured intrinsic response time is much higher than theoretical estimates.

Figure 3.4.6 shows the short circuit noise current at 30 and 420 MHz for a flat profile GaAs C-band diode. The intrinsic response time derived from this data gives $\tau_1 = 15.1$ ps. Qualitatively one can see that the steeper field dependence of the ionization rates in GaAs which reduces the effective avalanche width in a flat profile diode by almost a factor of four, will give a calculated response time of one picosecond or less. Thus, the discrepancy between experiment and theory is quite large. In the section on ionization rates, a new phenomenon is discussed that we believe is responsible for this discrepancy in the intrinsic response times.

An important part of the material evaluation depends on fitting the microwave admittance data. Figs. 3.4.7 and 3.4.8 show the conductance and susceptance data taken on the C-band diode along with a least squares numerical fit. All the relevant material and diode parameters corresponding to the numerical fit and those derived from the noise measurements are given in Table 3.4-1.

Since the Read structure is expected to perform much better than an IMPATT as regards efficiency and linearity, an analysis similar to that done for the flat profile diode has been done for a LO-HI-LO Read structure that has a hard punch-on. Figs. 3.4.9 and 3.4.10 show the short circuit noise current at 30 MHz and the theoretical fit which gives a multiplication at the noise peak of $M = 434$ and a saturation current of $16\mu\text{A}$. From the 420 MHz noise data an intrinsic response time of 3.3 ps is found. Fig. 3.4.11 shows the space charge

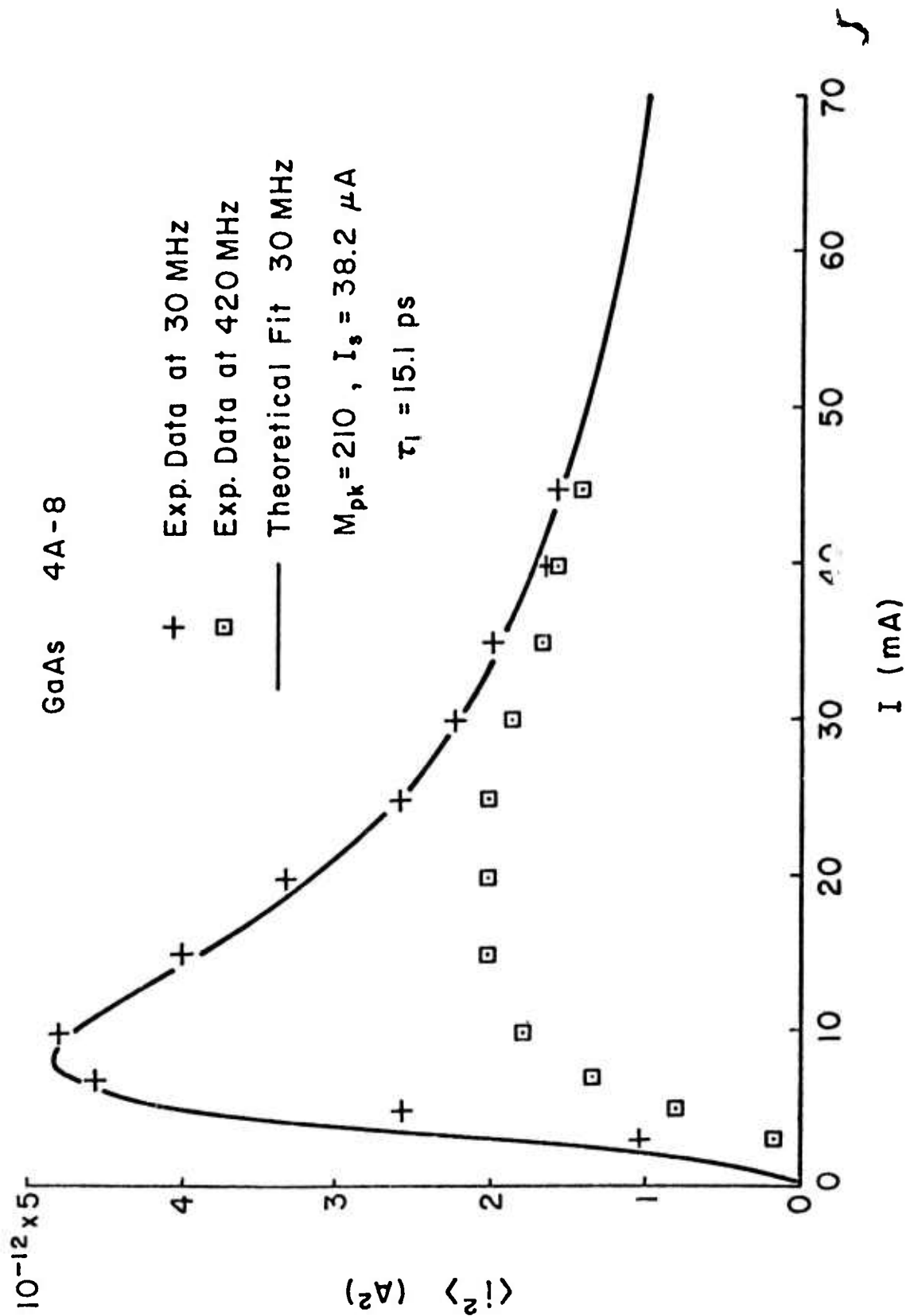


FIG. 3.4.6 Short circuit current noise of a flat profile GaAs diode vs. bias current at 30 and 420 MHz.

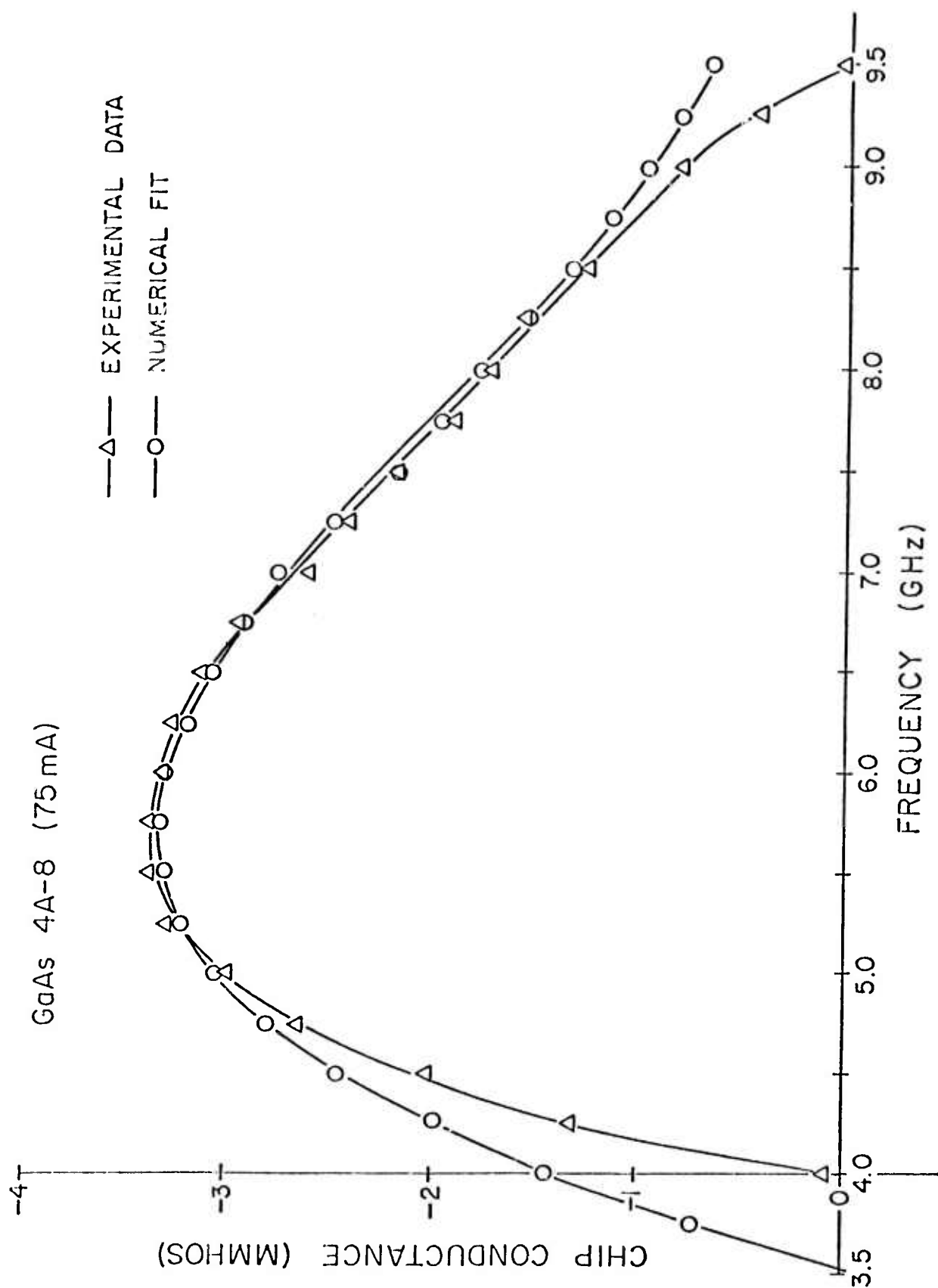


FIG. 3.4.7 Least squares numerical fit of the chip conductance vs. frequency at a bias current of 75 mA.

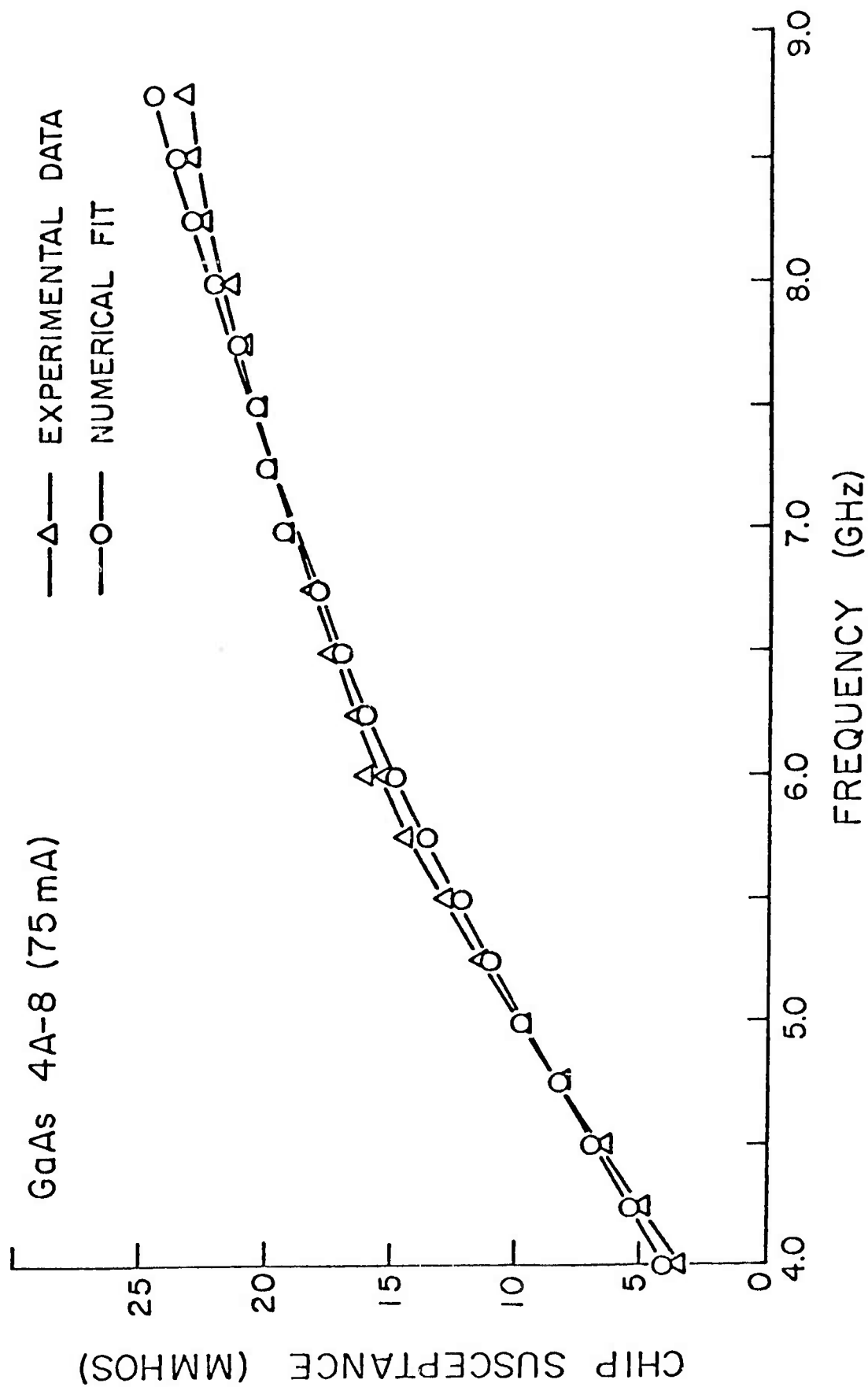


FIG. 3.4.8 Least squares numerical fit of the chip susceptance vs. frequency at a bias current of 75 mA.

TABLE 3.4-1
MATERIAL AND DIODE PARAMETERS
DERIVED FROM NOISE AND
ADMITTANCE MEASUREMENTS

DIODE	GaAs 4A-8	GaAs 676-10-2
Current (mA)	75	40
x_1/w	0.12	0.07
w (μm)	5.97	6.34
A (cm^2)	2.52×10^{-4}	4.95×10^{-4}
v_s (cm/s)	7.4×10^6	8.0×10^6
β	.78(3.75 GHz)	.29(5.25 GHz)
$M\tau_1$ (sec)	4.85×10^{-10}	4.0×10^{-10}
R_s (Ω)	0.50	0.69
Q_p	1.3(3.75 GHz)	0.6(5.25 GHz)
M_{pk}	210	434
I_s (μA)	38.2	16.0
τ_1 (ps)	15.1	3.3

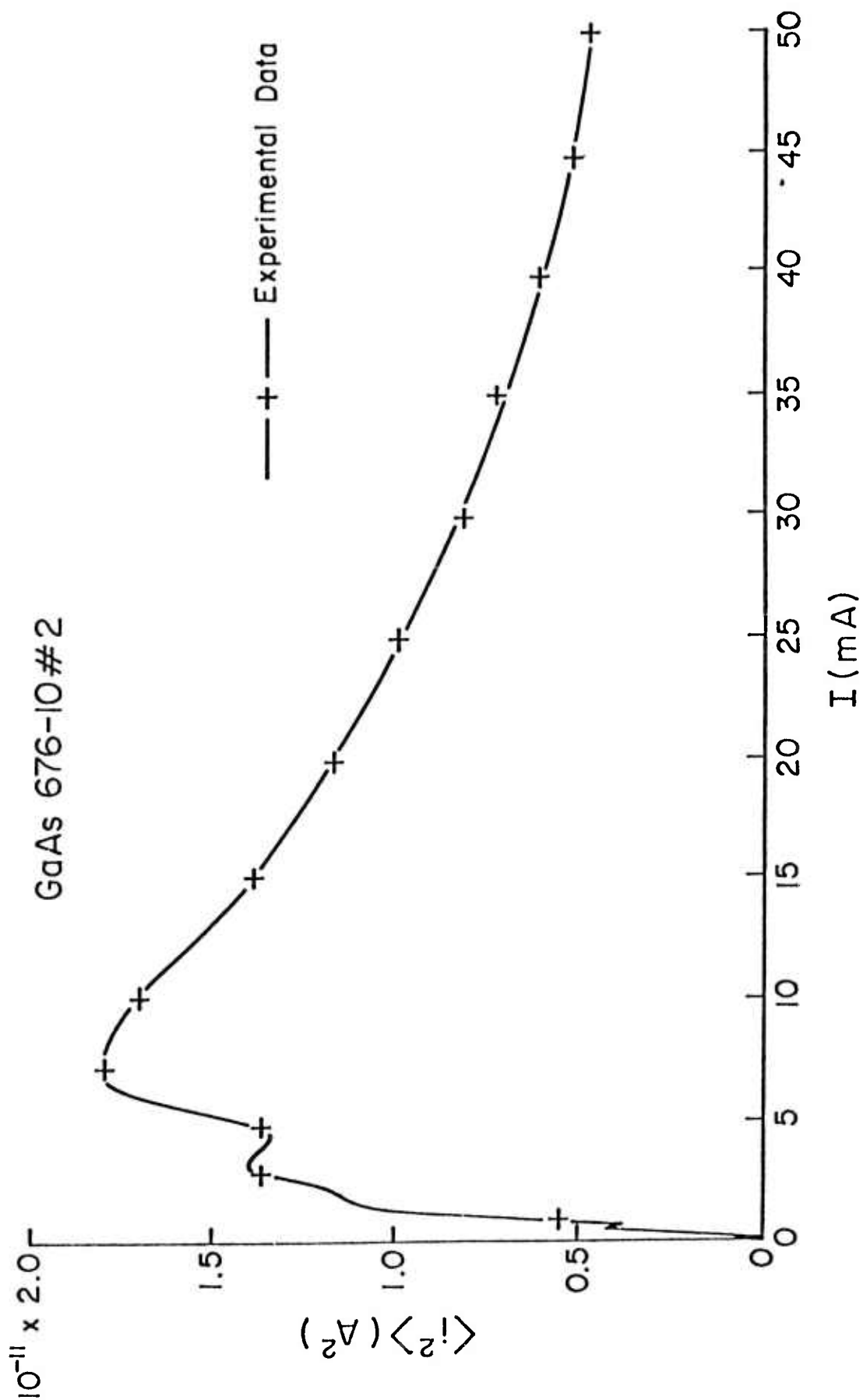


FIG. 3.4.9 Short circuit noise current at 30 MHz of a C-band, hard punch-on, L0-HI-L0, GaAs Read structure.

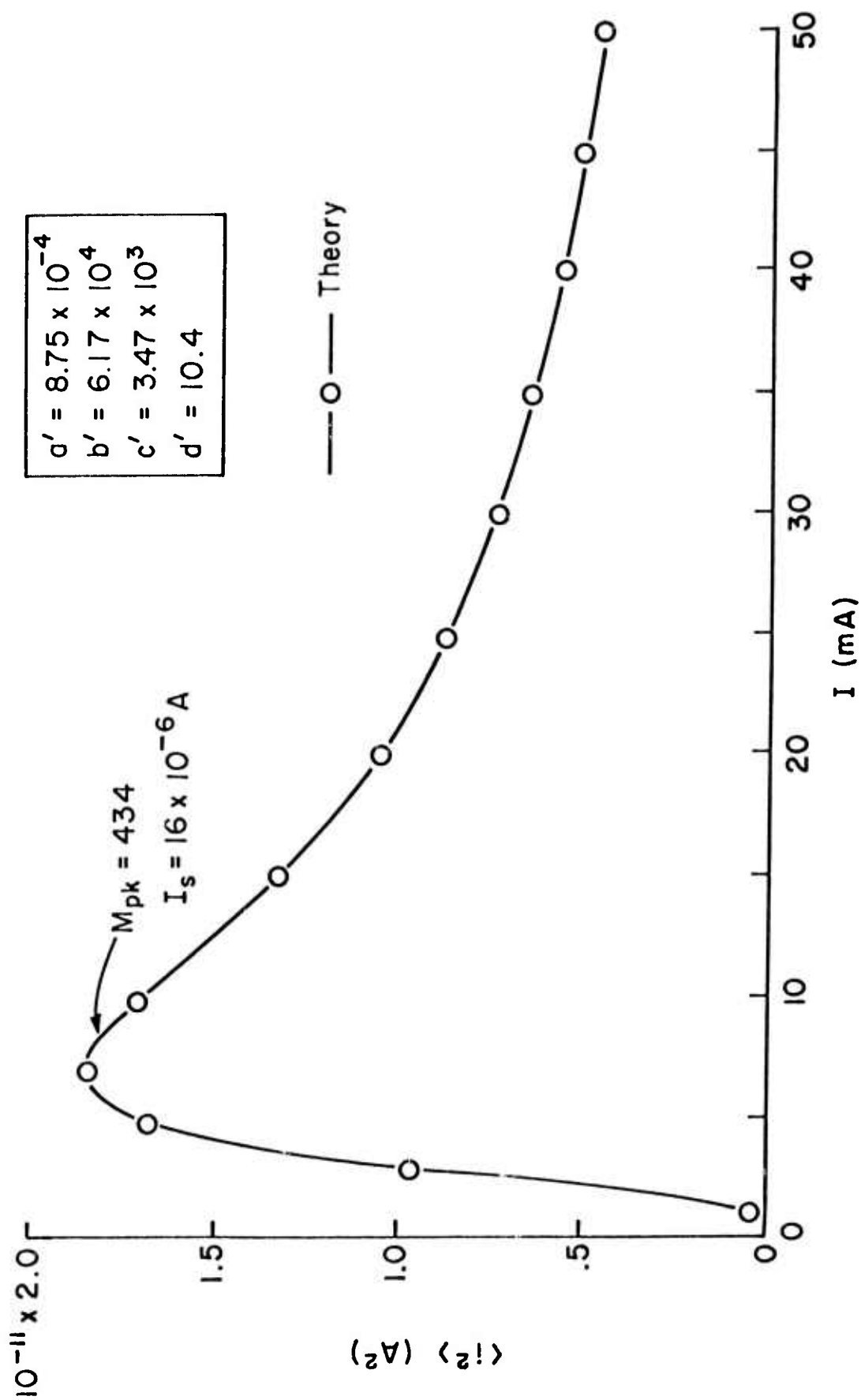


FIG. 3.4.10 Numerical fit of the noise data of Fig. 8.

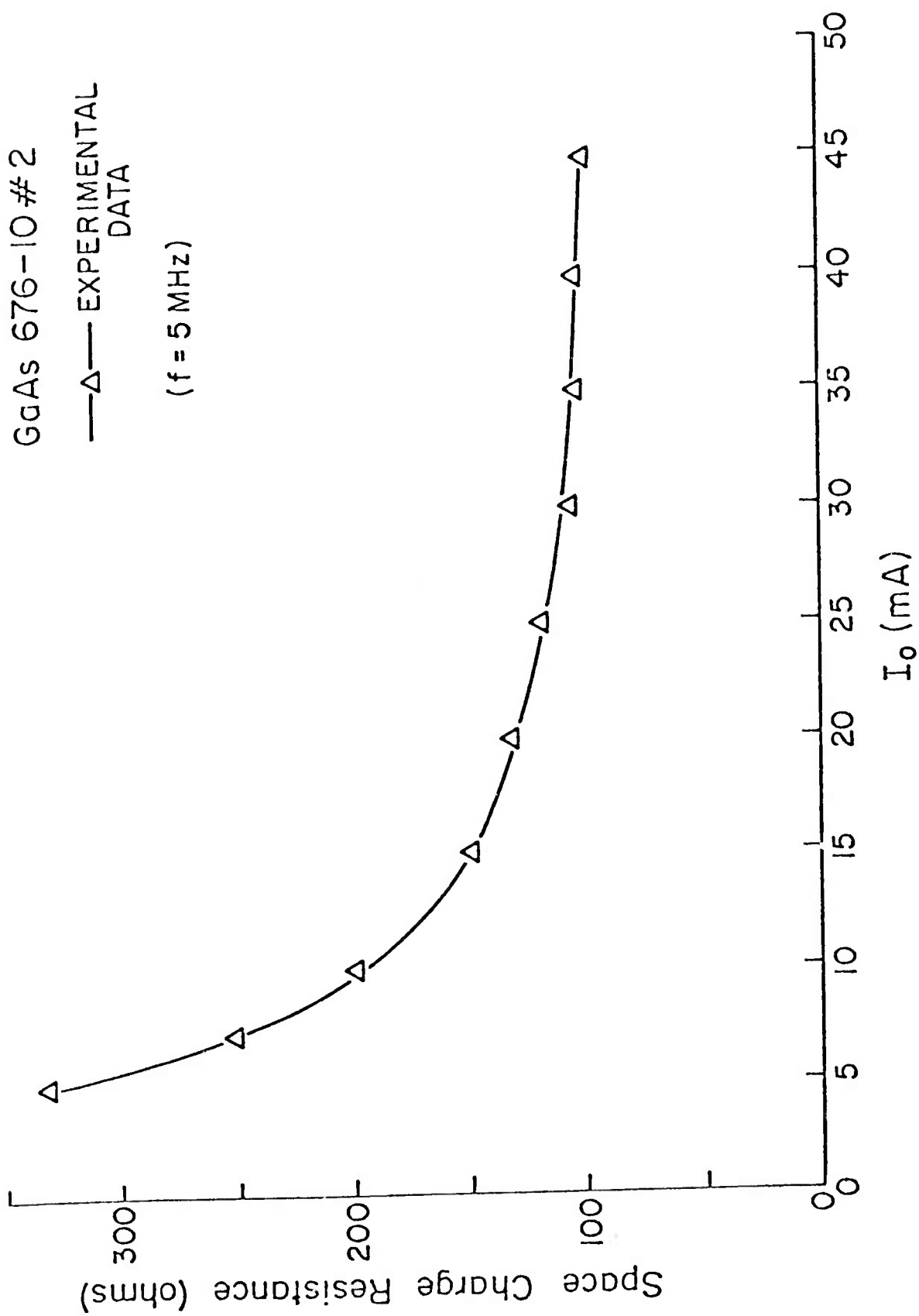


FIG. 3.4.11 Space charge resistance as a function of bias current including contact series resistance.

resistance as a function of bias current. The sharp increase at low bias currents is evidence that the avalanche is inhomogeneous; at higher currents space charge smoothing produces a reasonably constant resistance. In connection with the temperature variation of saturation current and multiplication, the temperature dependence of the saturation current below breakdown was measured and is shown in Fig. 3.4.12. The activation energy is seen to be 0.47 eV. This temperature dependence of the saturation current along with the measured thermal impedance of the diode can then be used to find the variation of the multiplication with bias current (Fig. 3.4.13). This current dependence of the multiplication is then used to numerically fit the admittance vs. frequency data shown in Figs. 3.4.14 and 3.4.15. Finally, all the parameters used in the numerical fitting are given in Table 3.4-1. Note that the multiplication at the specified bias current is very low; it is about 33 for the flat profile diode and about 100 for the Read structure.

3.4.3 The Effect of Lateral Variations of Avalanche Field and Saturation Current on the Local Current Density in the Presence of Space Charge Smoothing - Cornell University

It has been generally accepted that inhomogeneities in the electric field and the carrier generation rate were effectively smoothed out by space charge in the avalanche region when operating current densities exceeded a few hundred amperes per square centimeter. In reaching that conclusion it was tacitly assumed that the saturation current would be comparable to that found in bulk material and, therefore, the multiplication was quite high. It was acknowledged that the reverse current in mounted diodes was always much higher than could be accounted for by bulk generation, but then it was difficult to determine how much surface leakage current there was in addition to the bulk component. Microwave admittance measurements on Read structures gave some in-

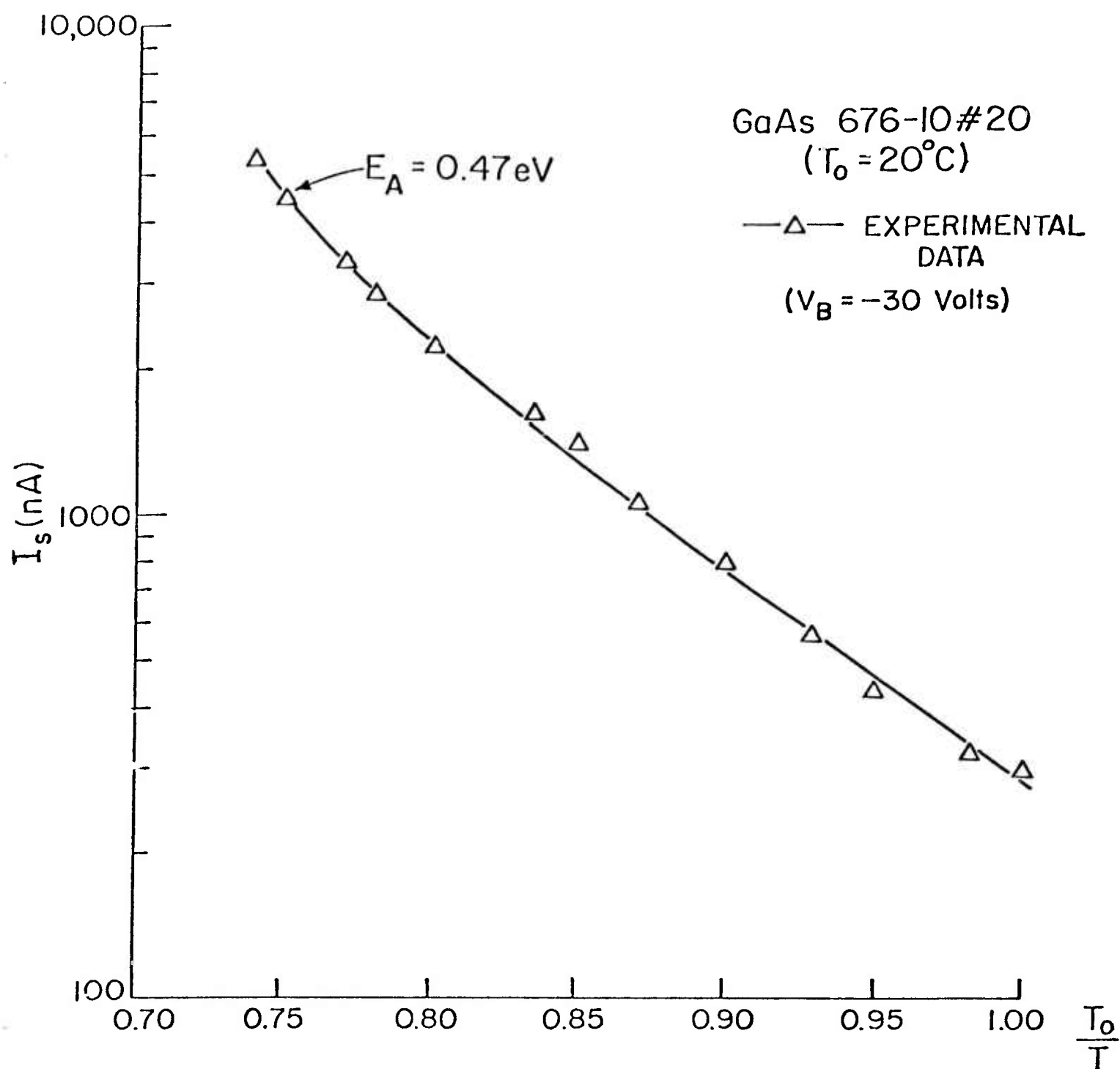


FIG. 3.4.12 Temperature dependence of the saturation current of the C-band Read diode below breakdown.

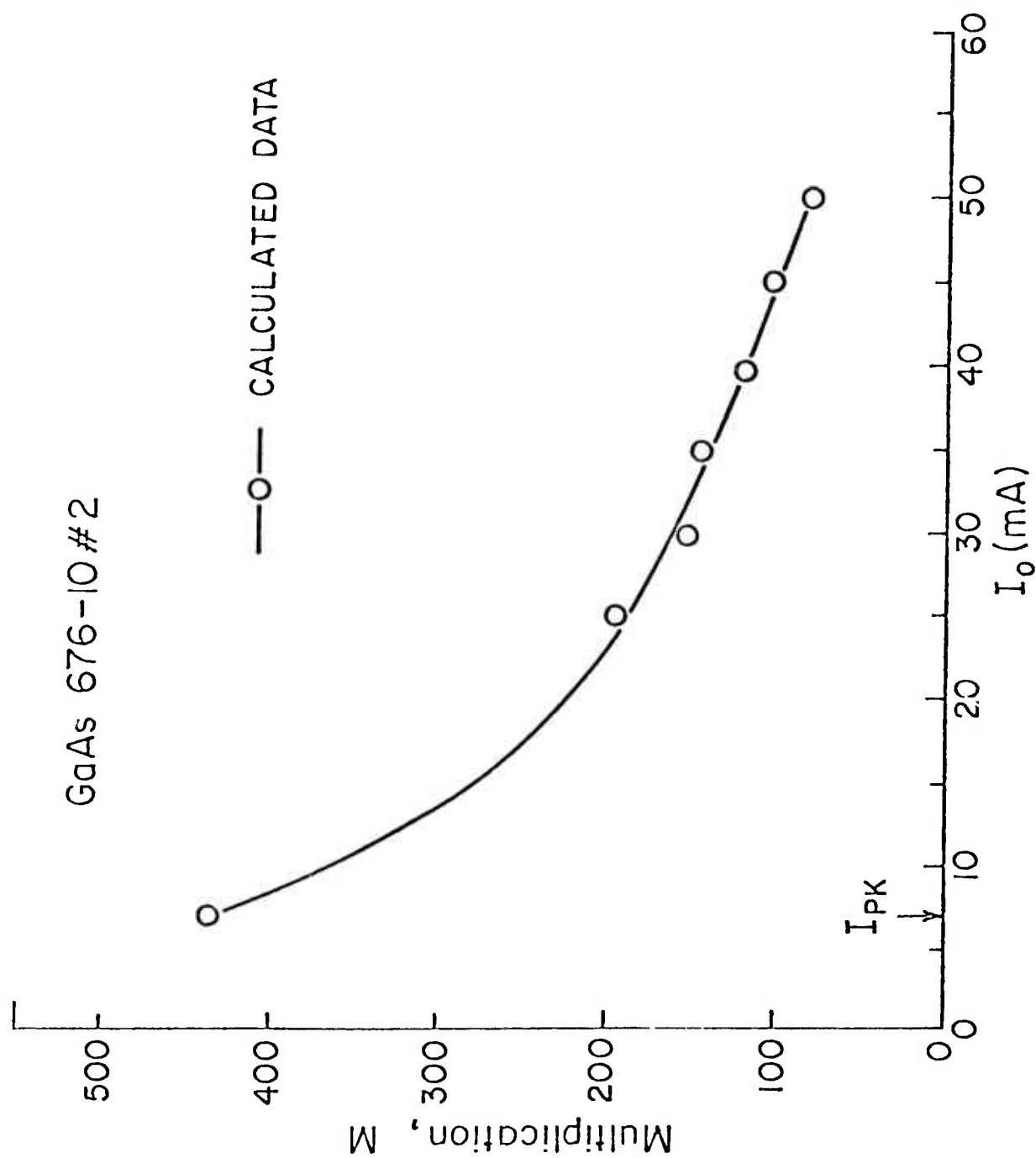


FIG. 3.4.13 Calculated multiplication as a function of bias current of the C-band Read diode.

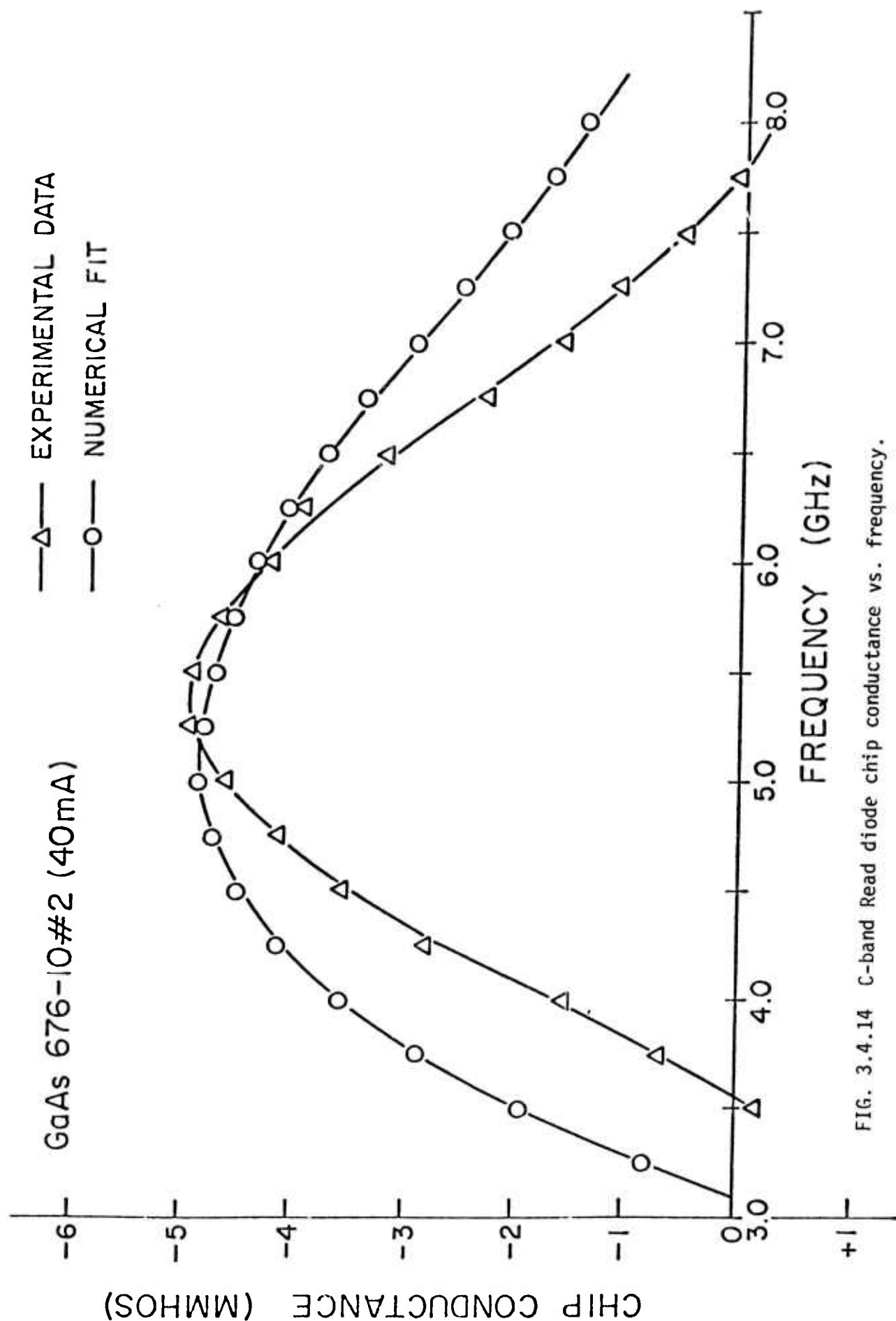


FIG. 3.4.14 C-band Read diode chip conductance vs. frequency.

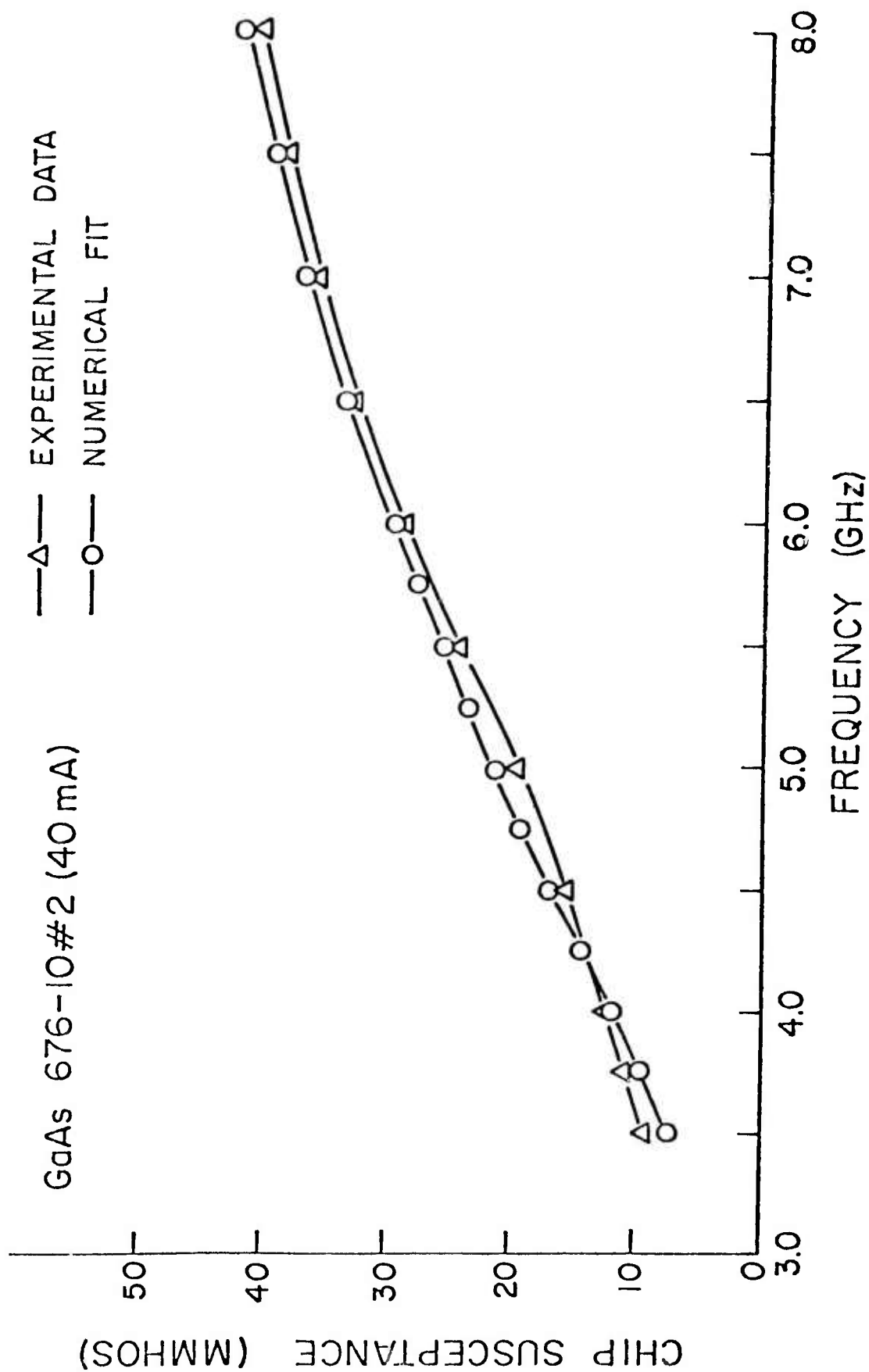


FIG. 3.4.15 C-band Read diode chip susceptance vs. frequency.

dication that the multiplication was very low because there was no well defined avalanche resonance. The success of the low frequency avalanche noise analysis, however, leaves little room for doubt that the multiplication is indeed very low under normal operating conditions and that the saturation currents range from 10^3 to 10^5 times what would be expected using very good bulk lifetimes. In the light of this new evidence on multiplication and saturation current the efficiency of space charge smoothing of inhomogeneities should be re-examined.

To quantify the relation between current density variations and the corresponding variations in peak avalanche field, the "Balance" equation is useful

$$E = E_p - \left[V - V_p - (Jw^2/2\epsilon v_s) \right] / w, \quad (17)$$

where E_p and V_p are the punch-through values of avalanche field and diode voltage respectively. Reworking Eq. (17) to obtain normalized variations of the avalanche field the following expression can be obtained

$$d = d' - w(J - M_0 J_s) / 2\epsilon v_s E_0 = (E - E_0) / E_0, \quad (18)$$

where $d' = (E_p - E_{p0}) / E_0 - (V_p - V_{p0}) / wE_0$ is the avalanche field variation caused by fixed chemical impurities in the active region. Note that in the limit $J = M_0 J_s$, $d = d' = 0$, and in the limit $M_0 = 1$, $J_s = 0$, $d = d'$. In Eq. (18) the subscript 'o' is used to denote an average value or alternatively a reference value. Although Eq. (18) can be readily understood from Eq. (17), it is still not appropriate for comparing current variations. These current variations,

however, can be derived using the following expression

$$I \equiv M_0 J_s / J = 1 + M_0 a d \quad , \quad (19)$$

where $a = E_C \partial(1/M) / \partial E_C$ is evaluated at breakdown. One can then derive the following quadratic equation

$$I^2 + (A' - u^{-1})I - A' = 0 \quad , \quad (20)$$

relating the normalized current variations I to the variations that would exist without the space charge smoothing $u = M'/M_0$, M' being the multiplication corresponding to d' in the absence of space charge. The constant $A' = M_0^2 J_s |a| w / 2e v_s E_0$ essentially represents various operating current densities in the diode. Fig. 3.4.16 gives a plot of Eq.(20) for assumed values of the diode parameters that are typical of IMPATTs. For saturation current densities similar to those derived from the noise measurements, $A' = 180$ corresponds to a multiplication of 10^3 and it is obvious that space charge smoothing is very effective at this level. For multiplications less than 10^2 , however, corresponding to our most recent data, an A' of .18 to 1.8 would be more appropriate and in this range of A' , space charge smoothing is not very effective.

In order to develop a similar result for variations in the saturation current, Eq. (17) is again the most convenient starting point. The situation is now somewhat simpler in that the avalanche field variations can be set equal to zero (i.e. $d' = 0$). Again, dimensionless variables representing ratios of

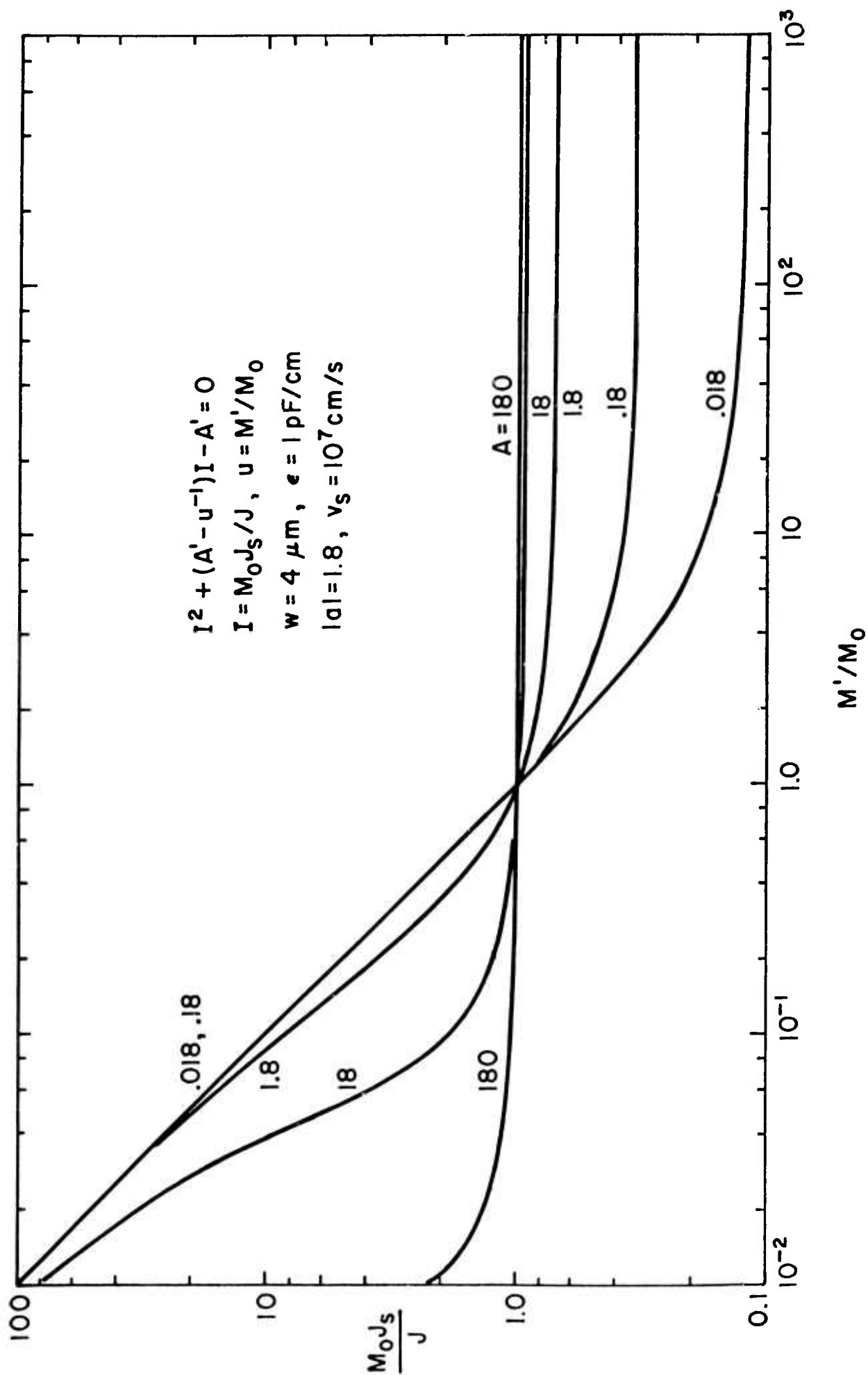


FIG. 3.4.16 Normalized current variation with space charge smoothing as a function of the current variation without space charge smoothing that would result from doping inhomogeneities.

currents are introduced;

$$I_j = MJ_s/M_0 J_{s0} \quad , \quad (21)$$

being the ratio of the current obtained with a different J_s and including the effect of space charge to the current obtained in the absence of space charge from the average value of saturation current, J_{s0} . The voltage across both portions of the diode is assumed to be constant. The second dimensionless current, defined as

$$u_j = J_s/J_{s0} \quad , \quad (22)$$

is just the ratio of the primary saturation currents in the two regions of the diode. With these two definitions, Eqs. (21) and (22), a quadratic equation is obtained

$$A'I^2 + I_j - u_j = 0 \quad , \quad (23)$$

and again $A' = M_0^2 J_{s0}^2 a |w/2\epsilon E_0 v_s$. Assuming the same diode parameters used to evaluate Eq.(20) and introducing a saturation current density $J_{s0} = .05 \text{ A/cm}^2$, Eq. (23) was evaluated and the results plotted in Fig. 3.4.17. It is apparent that multiplications in excess of 10^3 provide adequate space charge smoothing, but for multiplications of 10^2 or less, space charge smoothing is virtually non-existent.

Inhomogeneities in the impurity distribution over the area of epitaxial

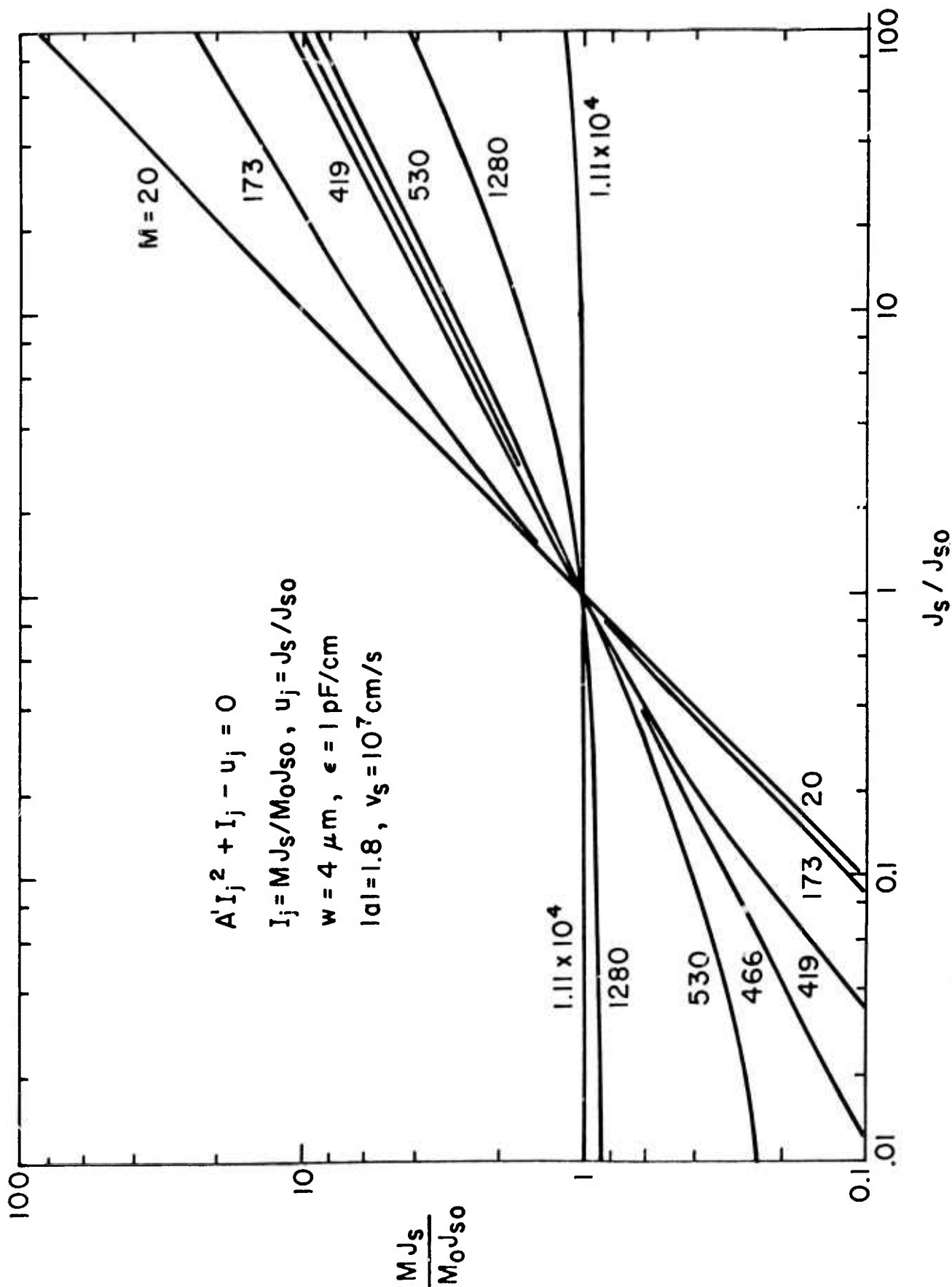


FIG. 3.4.17 Normalized current variation with space charge smoothing as a function of the current variation without space charge smoothing that would result from inhomogeneity of the generation rate over the area of the diode.

layer are quite visible from multiplication studies, microplasma defects are apparent in the low frequency noise data, and lastly, the effects of inhomogeneity have been observed in microwave admittance measurements in the neighborhood of avalanche resonance. The present advances in experimental and theoretical technique provide a good basis for relating material and microwave device parameters and to evaluate the practical consequences of material inhomogeneity.

3.4.4 GaAs Ionization Coefficients - Cornell University

In the last semi-annual report³ recordings of multiplication in epitaxial wafers of different doping were given that showed a reversal of the ionization rates of the holes and electrons. In the lightly doped sample ($N_d = 3 \times 10^{15} \text{ cm}^{-3}$), the multiplication due to excitation by electrons exceeded that due to excitation by holes, while in the heavily doped wafer ($N_d = 1.4 \times 10^{16} \text{ cm}^{-3}$) the hole multiplication exceeded the electron multiplication. Since the electron and hole multiplication are related to the respective ionization coefficients by the expression

$$(M_n/M_p) = \exp \left[\int_0^w (\alpha - \beta) dx \right], \quad (24)$$

one can conclude that the larger multiplication corresponds to the larger ionization rate; for example if $M_n > M_p$ then the electron ionization coefficient, α , exceeds the coefficient for holes, β . When the ionization rates were calculated from that multiplication data, however, a continuous curve for the ionization rate of electrons, for example, was not obtained. In the belief that a single, continuous curve should have been obtained, a great deal of experimentation was done with different Schottky barrier metallizations, p-n junctions, and surface passivation techniques in order to improve the reliability of the data.

The multiplication uniformity of Schottky barrier and epitaxial grown junction diodes was evaluated by measuring photocurrent response to a scanner laser beam. Fig. 3.4.18 shows the photocurrent response of a gold Schottky barrier diode on an n-GaAs epitaxial layer of approximately $2\mu\text{m}$ thickness and a doping level of about $3 \times 10^{15}/\text{cm}^3$. The junction is biased at 2V so the junction multiplication is unity. There is a greater response at the periphery of the diode because of the capacity of the metalization. In the center of the diode there is a region of higher photocurrent that is due to a slight scratch in the metalization. Note that the peripheral response is reasonably uniform around the diode. In Fig. 3.4.19 the photoresponse of this diode is shown for a reverse bias of 17.8V. The nonuniformity of the multiplication is quite pronounced. The left hand periphery and the scratch in the center shows a multiplication of about 1.5 while the peak photoresponse in the upper right edge shows a multiplication peak of about 25. There were no visible physical defects associated with the region of high multiplication so it is believed to be associated with a variation in layer doping. In Fig. 3.4.20 the multiplied photoresponse of a grown p-n junction is shown, similar to that of Fig. 3.4.19. Here too there is some enhanced photoresponse at the periphery of the junction but the multiplication is reasonably uniform except for a sharply localized region on the lower right edge which is associated with a physical defect in the layer. The dotted line extending from the bottom edge upwards is the shadow of the contacting point. Note that there is much less difference in photoresponse between the periphery and the center because the p-layer is much less opaque than the Schottky barrier metalization. It should also be remarked that the diode of Fig. 3.4.20 was only one of more than a dozen such diodes on the same wafer that was of sufficient uniformity

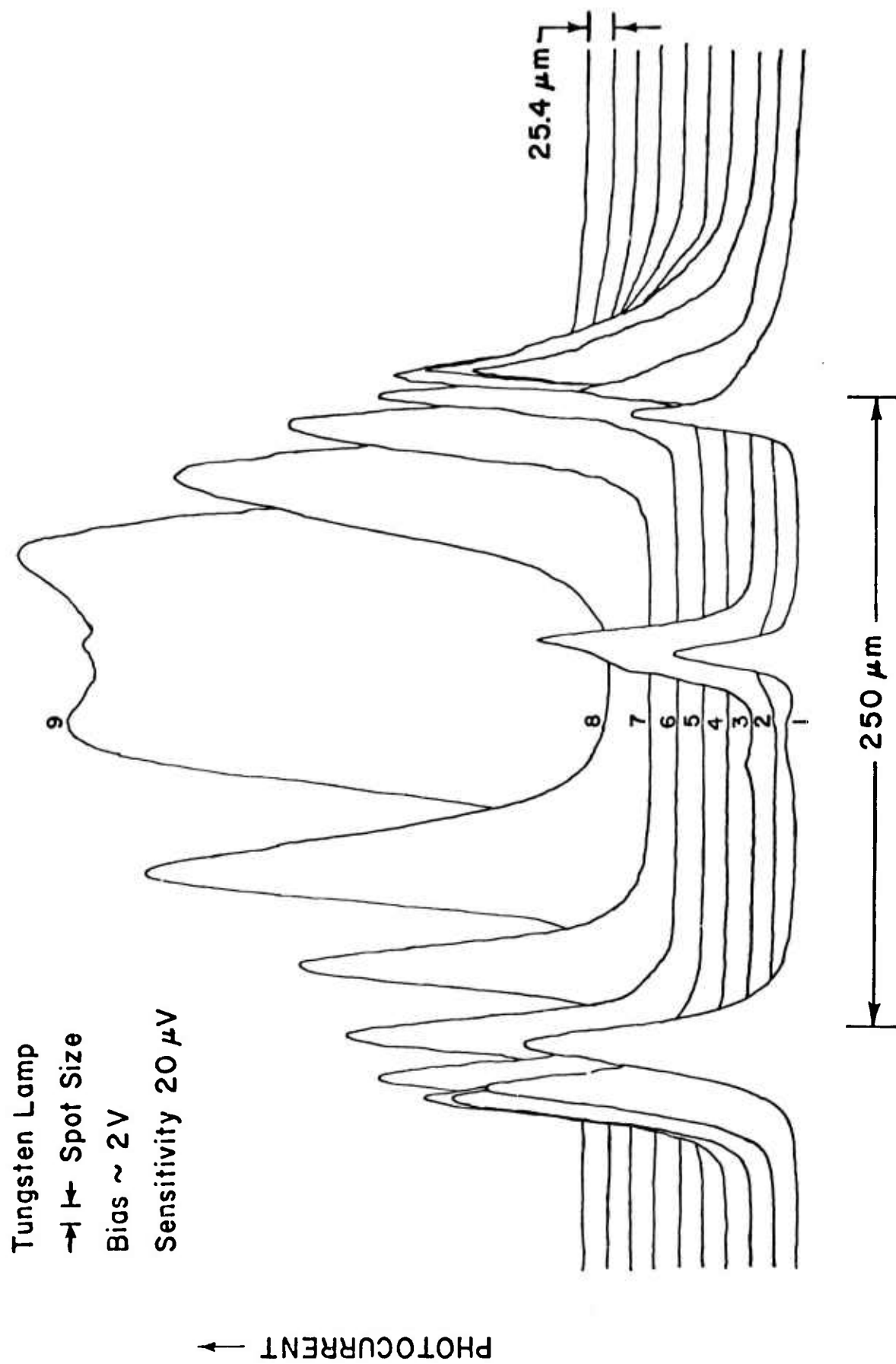


FIG. 3.4.18 Photocurrent response of a gold Schottky barrier diode on n-type GaAs biased at 2V.

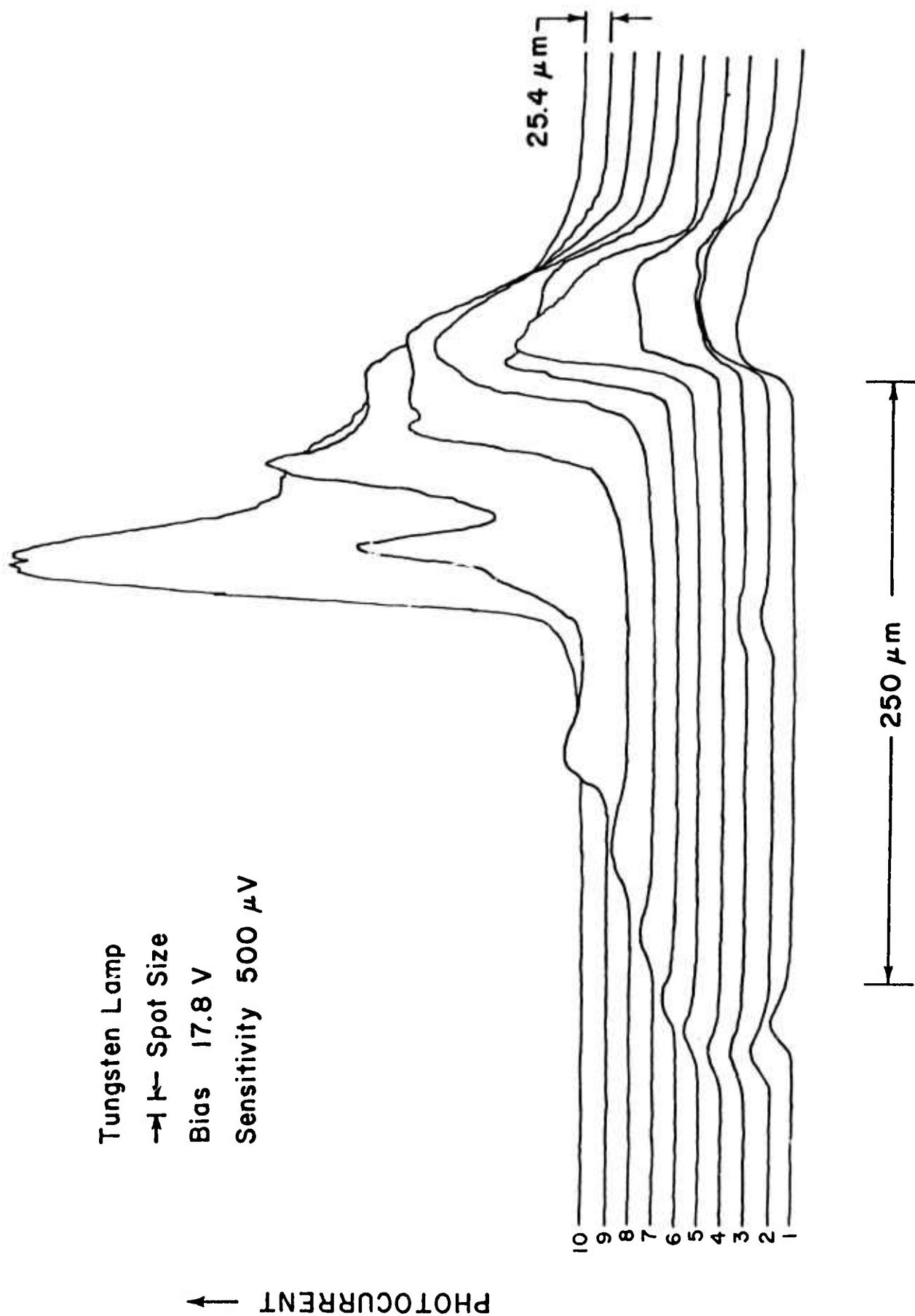


FIG. 3.4.19 Photocurrent response of the diode in Fig. 3.4.18 for a reverse bias of 17.8V.

P-N Junction
 6 μm Spot Size
 Bias 15.4 V
 Sensitivity 1 mV

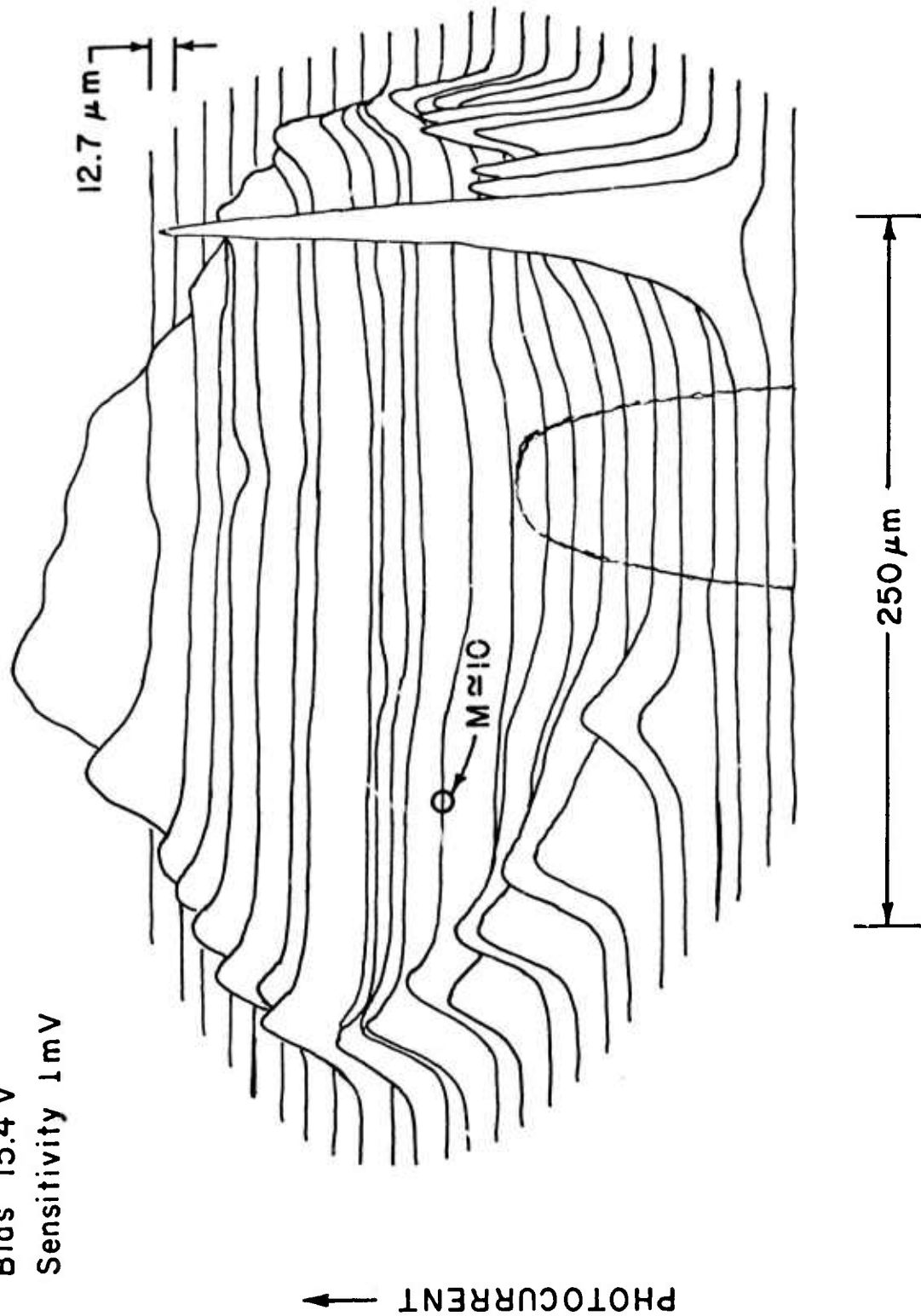


FIG. 3.4.20 Photocurrent response of a grown p-n junction reverse biased at 15.4V.

for obtaining reliable ionization rate data. The nonuniformity of the Schottky barrier diodes were all typical of that shown in Fig. 3.4.19. At present finding diodes as uniform as that in Fig. 3.4.20 is a highly selective process.

The latest series of results for the electron ionization coefficient are shown in Fig. 3.4.21. For comparison, the results of Stillman et al³⁶ are also shown. What is immediately obvious, and puzzling, is that a given ionization rate can be obtained in two differently doped samples at quite different electric field strengths. The persistence of this result coupled with the anomalously high intrinsic response time has led us to seek an alternative explanation.

A possible explanation can be deduced by examining the band structure diagram of GaAs.³⁷ For an electron in the $\Gamma_1 - X_1$ conduction band, corresponding to the orientation of our samples, it is not energetically possible to generate an electron-hole secondary pair.³⁸ Secondary pair generation requires an interband transition to $\Gamma_{15} - X_3$. If this interband transition time is comparable to the time an electron spends traversing the high field region of a narrow junction, then one can expect the effective ionization rate to depend on the width and, consequently, on the doping of the junction. Thus, for a given junction width one sees a field dependence of the ionization rate that is characteristic of the threshold energy and phonon losses of electrons that have made the interband transition, but if the junction width is reduced, then fewer electrons can make the interband transition although those that do have essentially the same field dependence for generating secondaries. Finally, we see that for a given junction width the ionization field dependence is strong enough to give a very narrow effective ionization zone width while the interband transition time can limit the

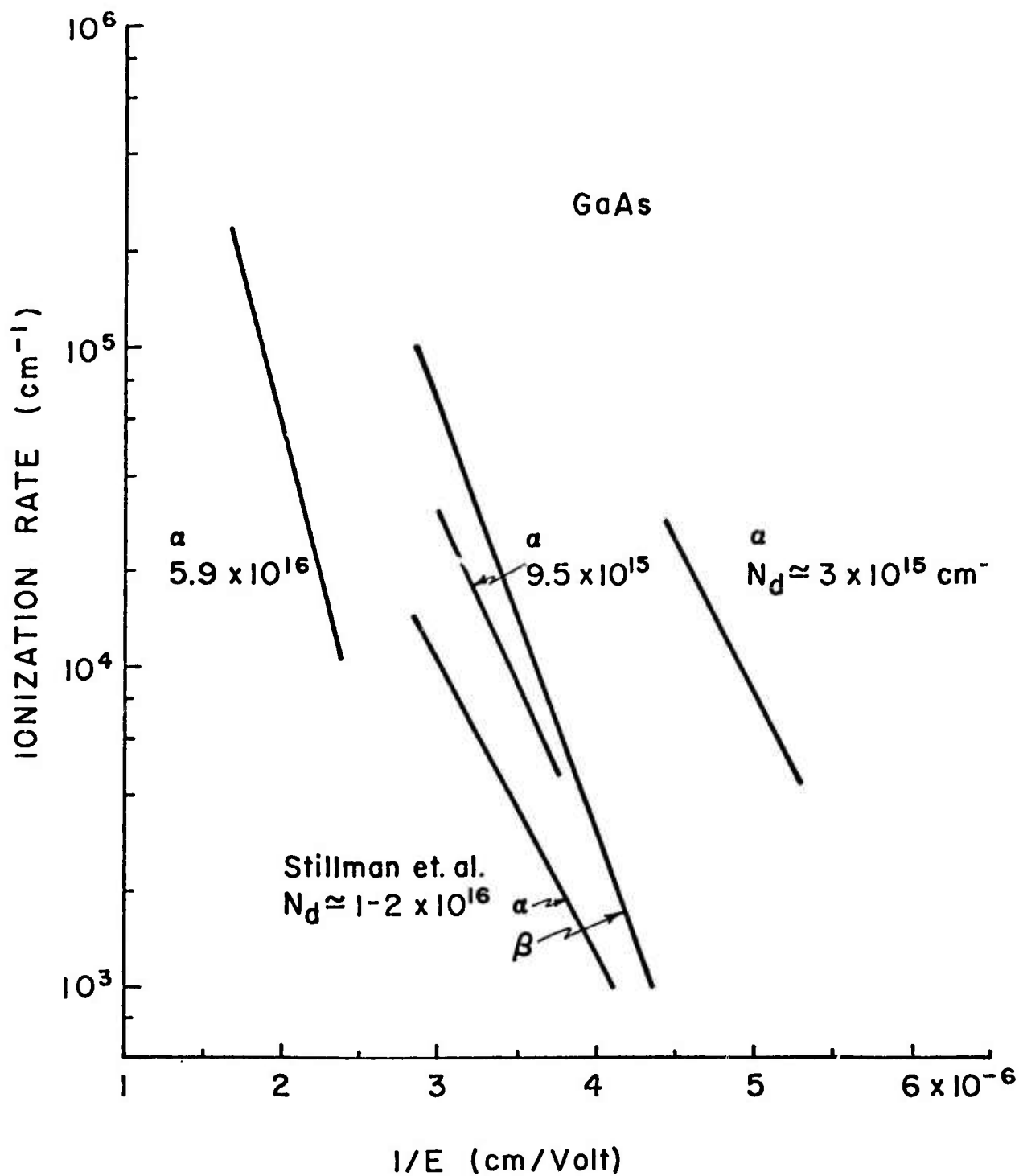


FIG. 3.4.21 Electric field dependence of ionization rates for several levels of doping.

rate of build-up of the avalanche, thus leading to a much increased intrinsic response time. The hole ionization rate, of course, should not be affected by an interband transition rate and its measurement in different samples should give a smooth curve. That smooth curve would explain the crossover observed in the multiplication curves.

January 22, 1976

SC5017.7SAR

4.0 FUTURE PLANS

4.1 Epitaxial Material Growth and Material Characterization

4.1.1 LPE Activities at Stanford University - High Resistivity LPE GaAs

A. Further studies of the effects of growth conditions on the properties of epitaxial layers grown in the $\text{SiO}_2\text{-BN-H}_2$ system will be conducted in order to find the optimum conditions for the growth of semi-insulating GaAs layers.

B. Studies of voltage breakdown in the semi-insulating epitaxial layers will be carried out to determine the breakdown mechanism.

4.1.2 LPE Activities at the Science Center

The LPE effort at the Science Center will continue to support areas of this contract dealing with measurement of intrinsic material properties, and substrate annealing and interface effects using FETs as a test vehicle. At this moment, it is unclear if multiple layer buffered FET growths will be continued, as similar work has been proposed at Cornell University.

4.1.3 LPE Activities at Cornell University

The growth of FET active channels directly on buffer layers grown in the same operation will be undertaken. The use of lightly doped p-type buffers, as well as lightly doped n-type buffers, will be tried to reduce conductivity and to cause carrier depletion at the critical interface between buffer and channel. Measurement of net donor density and mobility from point to point through the channel, at the critical interface, and in the n-type buffers will also be taken. Finally, buffered FET layers will be made and shipped to the Science Center for FET processing.

4.2 Semi-Insulating Substrate Material

4.2.1 Material Growth at Crystal Specialties

In light of the recent information on possible carbon contamination, the present technique of pumping and outgassing of the quartz ampoules will be reviewed and modifications made to further reduce carbon as a possible source of contamination. Liquid nitrogen traps and furnaces for outgassing of the ampoules will be added. Crystals grown by backfilling the ampoules with N_2 , He, and $C + O_2$ will be compared with those using no backfill gases.

4.2.2 Material Evaluation at the Science Center

The study of bulk properties of the material by measurement of transport properties will be continued. Study of the effects of heat treatment will be further pursued. Photoluminescence measurements will be made on several samples. The temperature dependence of the spectra will be measured. Samples will be profiled by step-by-step etching. Studies of the behavior of substrates at the operating temperature of high-power devices will be initiated.

4.3 Ion Implantation

The effects of using different semi-insulating materials on the results of 100 keV sulfur implantation will be explored. Higher energy sulfur implants will be investigated in more detail. Lattice location experiments on implanted sulfur will be initiated using channeling techniques. Proton induced X-rays will be used to detect the interaction between the channeled beam and the sulfur atoms. The annealing of amorphous layers will be further investigated.

4.4 Material Characterization - Theoretical and Experimental Investigation of Material Parameters on Device Performance

4.4.1 Science Center Activity

Study of dependence of the noise figure of MESFETs on bias levels,

and associated transient effects will be further pursued. Comparison of implanted and epitaxial transistors will be continued.

4.4.2 Cornell University Activity

Furthur work will be devoted to determine the intrinsic response time of GaAs diodes, both flat profile and Read types, from low frequency measurements. The large values obtained from our preliminary measurements are apparently in reasonable agreement with unpublished data of R. Kuv^oas obtained from microwave admittance measurements. The second area of work is the quantification of the electron and hole ionization rates vs. doping. Since a tentative explanation of the anomalous electron ionization rate in GaAs has been proposed and the implications of that explanation are important for device analysis and modeling, efforts will be concentrated on measuring electron and hole ionization coefficients over the same range of doping in order to more fully understand the effect of the conduction band structure.

5.0 REFERENCES

- ¹L. J. Van der Pauw, Philips Res. Reports 13, 1 (1958).
- ²A. T. Philadelphus and P. C. Euthymiou, J. Appl. Phys. 45, 955 (1974).
- ³F. H. Eisen, J. A. Higgins, A. A. Immorlica, Jr., R. L. Kuv^oas, B. W. Ludington, B. M. Welch, C. P. Wen and R. Zucca, "Investigation of Technological Problems in GaAs," Semi-annual Technical Report No. 1, AFCL-TR-75-0435, October 15, 1975, Contract No. F19628-75-C-0113.
- ⁴J. Barrera, private communication.
- ⁵B. L. Mattes, Y. M. Houg and G. L. Pearson, J. Vac. Sci. Technol. 12, 869 (1975).
- ⁶H. G. B. Hicks and P. D. Green, Proc. Int. Symp. on GaAs and Related Compounds, The Institute of Physics, London and Bristol (1970), p 92.
- ⁷H. G. B. Hicks and D. F. Manley, Sol. State Comm. 7, 1463 (1969).
- ⁸J. B. Mullin, private communication.
- ⁹S. Y. Chiang and G. L. Pearson, J. Appl. Phys. 46, 2986 (1975).
- ¹⁰W. Shockley in Electrons and Holes in Semiconductors, Van Nostrand, (1950), p 465.
- ¹¹D. C. Look, J. Phys. Chem. Solids 36, 1311 (1975).
- ¹²M. Ilgms and H. J. Queisser, Phys. Rev. 12, 1443 (1975).
- ¹³G. R. Cronin and R. W. Haisty, J. Electrochem. Soc. 111, 874 (1964).
- ¹⁴T. Inoue and M. Ohyama, Sol. St. Comm. 8, 1309 (1970).
- ¹⁵S. S. Li and C. I. Huang, J. Appl. Phys. 43, 1757 (1972).
- ¹⁶P. L. Hower, W. W. Hooper, D. A. Tremere, W. Lehrer and C. A. Bittman, in Proceedings of the Second International Symposium on GaAs, Institute of Physics and Physical Society, (1968), p 187.
- ¹⁷F. H. Eisen, B. M. Welch, C. P. Wen and R. Zucca, "Investigation of

Technical Problems in Gallium Arsenide," Semi-annual Technical Report No. 3, AFCRL-TR-75-0093, February 5, 1975, Contract No. F19628-74-C-0038.

¹⁸N. G. Ainslie, S. E. Blum, and J. F. Woods, J. Appl. Phys. 33, 2391 (1962); J. F. Woods and N. G. Ainslie, J. Appl. Phys. 34, 1469 (1963).

¹⁹J. Blanc and L. R. Weisberg, Nature 192, 155 (1961).

²⁰R. W. Haisty, E. W. Mehal and R. Stratton, J. Phys. Chem. Solids 23, 829 (1962).

²¹Measured by Micro-Trace Analytical Services, City of Industry, CA.

There are some discrepancies between the results for sample #2000 in Table 3.2-4 and those from an earlier analysis reported in Table 3.2-4 of Ref. 3. The recent values were used because the specimens for the recent analysis were located in the boule close to the specimens used for the experiments. However, it is not known to what extent the discrepancy is due to inhomogeneity of the impurity distribution in the material or to limitations of the mass spectrographic analysis technique.

²²See for example, L. H. Putley, "The Hall Effect and Related Phenomena," Butterworth (1960).

²³D. D. Sell and H. C. Casey, J. Appl. Phys. 45, 800 (1974).

²⁴M. B. Panish and H. C. Casey, J. Appl. Phys. 40, 163 (1969).

²⁵C. H. Gooch, C. Hilsum and B. R. Holeman, J. Appl. Phys. 32, 2069 (1961).

²⁶C. E. Jones and A. R. Hilton, J. Electrochem. Soc. 113, 504 (1966); R. F. Broom, J. Appl. Physics 38, 3483 (1967); G. P. Peka and Y. I. Karkhanin, Sov. Phys. Semicond. 6, 261 (1972); D. Bois and P. Pinard, Phys. Rev. B9, 4171 (1974).

- ²⁷J. R. Waldrop, R. Zucca and C. P. Wen, Appl. Phys. Lett. 26, 322 (1975);
J. R. Waldrop and J. S. Harris, J. Appl. Phys. 46, 5214 (1975).
- ²⁸J. Barrera, Proceedings of the Fifth Biennial Cornell Electrical Engineering Conference, Cornell University (1975), p 135.
- ²⁹M. I. Nathan and G. Burns, Phys. Rev. 129, 125 (1963).
- ³⁰E. W. Williams and C. T. Elliot, J. Phys. D 2, 1657 (1969).
- ³¹S. M. Sze and J. C. Irvin, Solid State Electron. 11, 599 (1968).
- ³²L. J. Vieland and I. Kudman, J. Phys. Chem. Solids 24, 437 (1963).
- ³³S. Asai, S. Ishioka, H. Kurono, S. Takahashi, and H. Kodema, J. Japan Soc. Appl. Phys. 42, 71 (1973).
- ³⁴R. Kuvás^o and C. A. Lee, J. Appl. Phys. 41, 1743 (1970).
- ³⁵D. R. Decker, IEEE Trans. Elec. Dev. ED-21, 469 (1974).
- ³⁶G. E. Stillman, C. M. Wolfe, J. A. Rossi, and A. G. Foyt, Appl. Phys. Lett. 24, 471 (1974).
- ³⁷M. L. Cohen and T. K. Bergstresser, Phys. Rev. 141, 789 (1966).
- ³⁸C. L. Anderson and C. R. Crowell, Phys. Rev. B5, 2267 (1972).

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