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INVESTIGATION OF DEFECTS AND IMPURITIES IN SILICON-ON-SAPPHIRE

Rockwell International Corporation

ROME AIR DEVELOPMENT CENTER
AIR FORCE SYSTEMS COMMAND
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report covers the second six months of a program to investigate the effects of defects and impurities in SOS materials on the electrical characteristics and radiation tolerance of CMOS/SOS devices. Additional chemical surface-etch experiments and IMMA analyses were completed during this phase of the program. This phase of the study focused on fabricating CMOS/SOS devices on the various substrate groupings examined in the first phase

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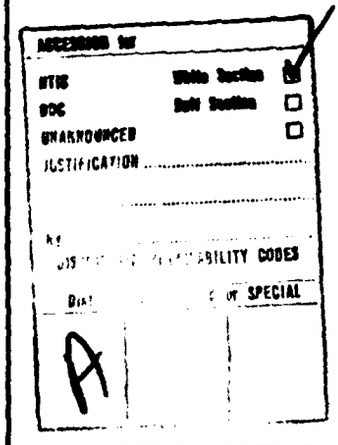
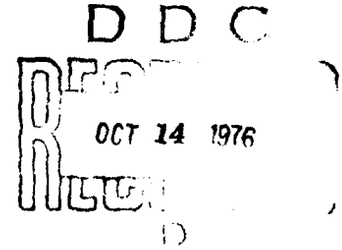
20. ABSTRACT (Continued)

of this study. Electrical parameter data and radiation hardness data were obtained for the CMOS/SOS devices and correlated with SOS material characteristics.





SECTION I

INTRODUCTION

This report describes work performed from July 15, 1975 to January 31, 1976 on AFCRL Contract No. F19628-75-C-0108. The objective of this program is to investigate the possible effects of defects and impurities in silicon-on-sapphire (SOS) substrates and films on the electrical and radiation parameters of devices fabricated in this material.[1]

The first Scientific Report (July 1975) discussed the physical nature of the sapphire substrates obtained from three suppliers--Union Carbide, Tyco, and Crystal Systems. These sapphire samples were analyzed by X-ray diffraction, selective etch and Ion Microprobe Mass Analyzer (IMMA) techniques to determine relative defect and impurity levels.

Efforts during the second phase of the program, reported herein, have attempted to determine the role which sapphire defects and surface impurities imbedded in the silicon film have on MOS/SOS electrical parameters and radiation hardness.[2]

Following the introduction, Section II of this report describes the results of sapphire analyses that were not completed in time for inclusion in the first Scientific Report. This section includes X-ray topograph, selective etch, and IMMA data obtained for the Tyco sapphire polished by Tyco. These results are followed by a description of an experiment conducted in an attempt to determine impurity levels in the sapphire bulk. The section is concluded with a short discussion of the cooperative effort with National Bureau of Standards.

Section III begins the discussion pertinent to the second phase of the program. This section discusses the silicon epitaxy, pre-silicon deposition cleaning procedures and the silicon impurity characterization.

Section IV describes the test vehicle fabrication and characterization. Following a short description of the process procedures, this section presents the electrical wafer map data, followed by IMMA data for selected devices of interest to determine if electrical behavior could be related to impurity levels and/or location. Radiation hardness data are then presented from wafers representative of each group of sapphire and silicon variation.

The final section of the report summarizes the results of the first 12 months of the program. This summary includes an evaluation of the material analysis techniques used in this study and attempts to correlate the analytical results with the electrical and radiation characteristics observed in Section IV.

SECTION II

SAPPHIRE ANALYSIS

1. TYCO (WITH TYCO POLISH) SAPPHIRE ANALYSIS

The previous scientific report did not include the sapphire analysis of the Tyco sapphire polished by Tyco. Since the completion of that report, Tyco samples have been analyzed using the same techniques used previously--selective etch, X-ray topography and IMMA analysis.

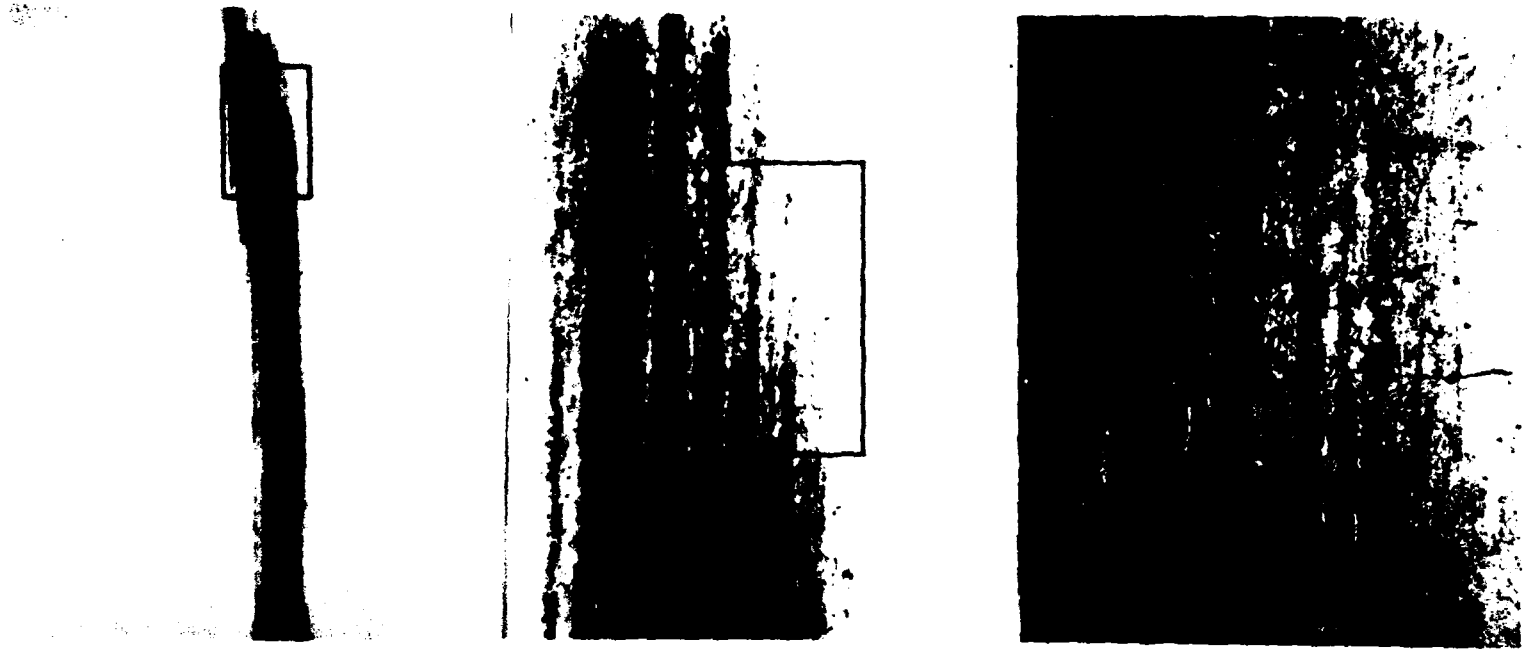
The results for the selective etch analysis showed a surface similar to that previously reported for Crystal Systems wafers polished by Insaco. A dislocation density of 9×10^5 cm^{-2} was observed for the Tyco sapphire with bands of dislocations being present, as in the case of the Tyco sapphire polished by Union Carbide. No grain boundaries were observed, as in the case of the Crystal Systems sapphire. There was also considerable subsurface damage--probably due to the lack of a high-temperature anneal prior to analysis.

The X-ray topographs of the Tyco sapphire are shown in Figure 1. The topographs show a considerable number of polishing scratches ranging from fairly large scratches that show up in the 5.5X photomicrographs to the finer scratches observed in the 25X and 55X photomicrographs. The defect densities range between 10^4 - 10^6 defects/cm^2, depending on the sampled area.

A comparison of Union Carbide, Tyco and Crystal Systems sapphire evaluated using the X-ray topograph and selective etch techniques is given in Table I. Upon close examination, the "readily observable scratches" on Crystal Systems/Insaco polish samples appear to be from deep saw marks formed during the wafer slicing operation and should not be associated with the polishing cycle, as inferred in the previous report.

An IMMA elemental mass scan for the Tyco material is shown in Figure 2. The large peak at mass number 13.5 corresponds to doubly ionized aluminum (Al^{++}), and it is associated with surface charge-up of the sapphire.[3]

Finally, a frequently observed phenomenon in sapphire substrates is the presence of hexogonally appearing inclusions. These inclusions, shown in Figure 3 for Tyco material, are actually cubic in geometry, as shown in the photograph where the incident light is reflected off of one face. Inclusions of this nature are virtually always found beneath the sapphire surface so that they do not appear to interfere with the deposited silicon film.



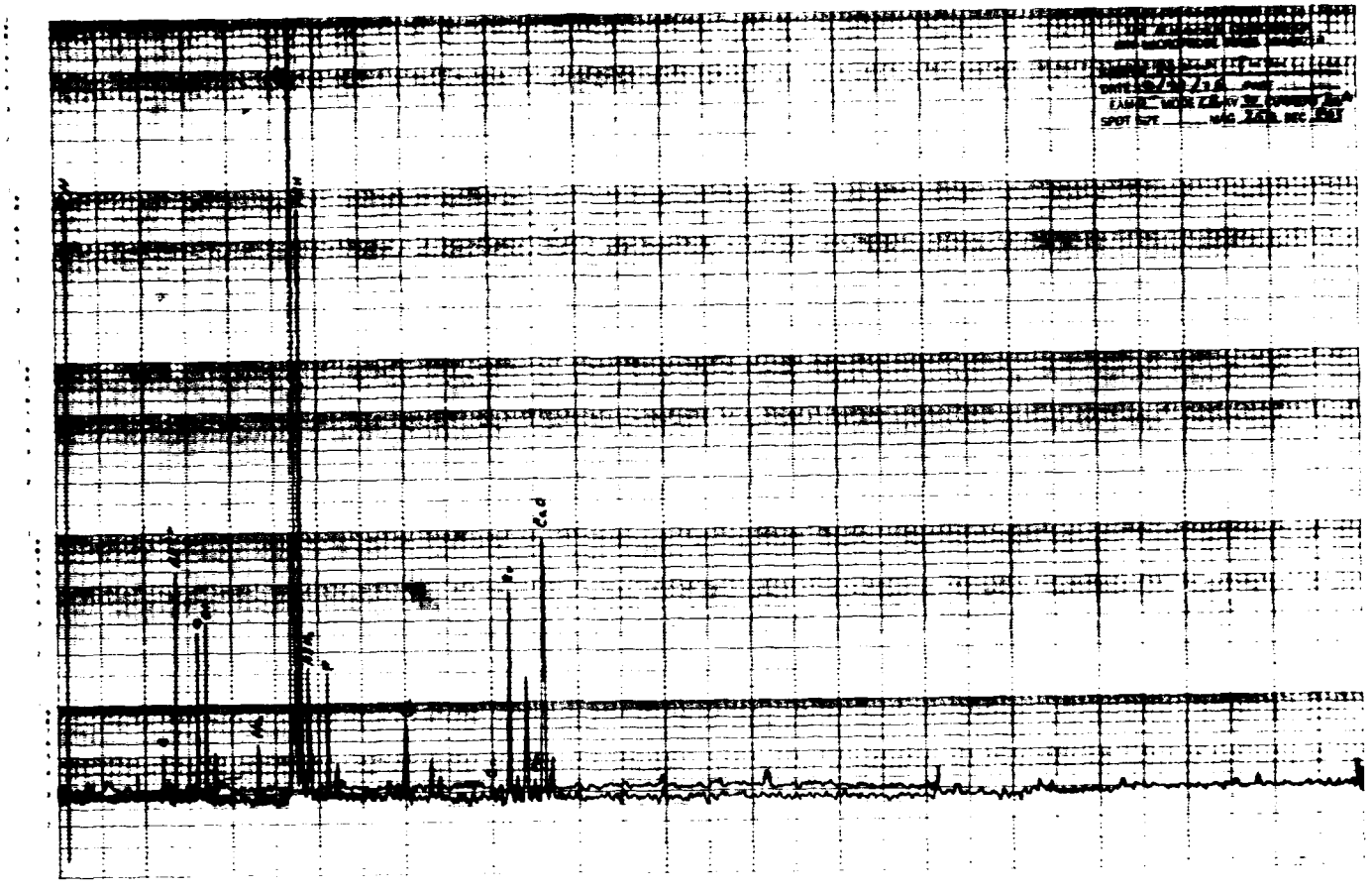
5.5X 25X 55X

Figure 1. FeKα Double Crystal Reflection Topograph of Tyco Wafer Polished by Tyco

Table I. SOS Wafer Quality

	Vendor/Polisher				
	U.C./U.C.	Tyco/Tyco	Tyco/U.C.	C.S./U.C.	C.S./Insaco
Surface Defects (H_3PO_4 Selective Etch)	10^4-10^5 cm^{-2}	10^5-10^6 cm^{-2}	10^5-10^6 cm^{-2}	10^5-10^6 cm^{-2}	10^5-10^6 cm^{-2}
Scratches (X-ray Topography)	Few Detectable	Numerous Scratches Ranging From Coarse to Very Fine	Few Detectable	None Detectable	Readily Observable Scratches--Mainly Saw Marks
Dislocations (X-ray Topography)	10^3-10^4 cm^{-2}	10^4-10^6 cm^{-2}	10^4-10^6 cm^{-2}	10^4-10^6 cm^{-2}	10^4-10^6 cm^{-2}
Dislocation Banding (H_3PO_4 Selective Etch)	None Observed	Some Banding Observed	Some Banding Observed	Prominent Banding Observed	Prominent Banding Observed
Grain Boundaries (H_3PO_4 Selective Etch)	None Observed	None Observed	None Observed	Numerous Sites Observable	Numerous Sites Observable

Mass Spectrometer Response, 0.1 μA Full Scale



1 Atomic Mass Unit Per Division

Figure 2. Elemental Scan of Tyco Sapphire Polished by Tyco

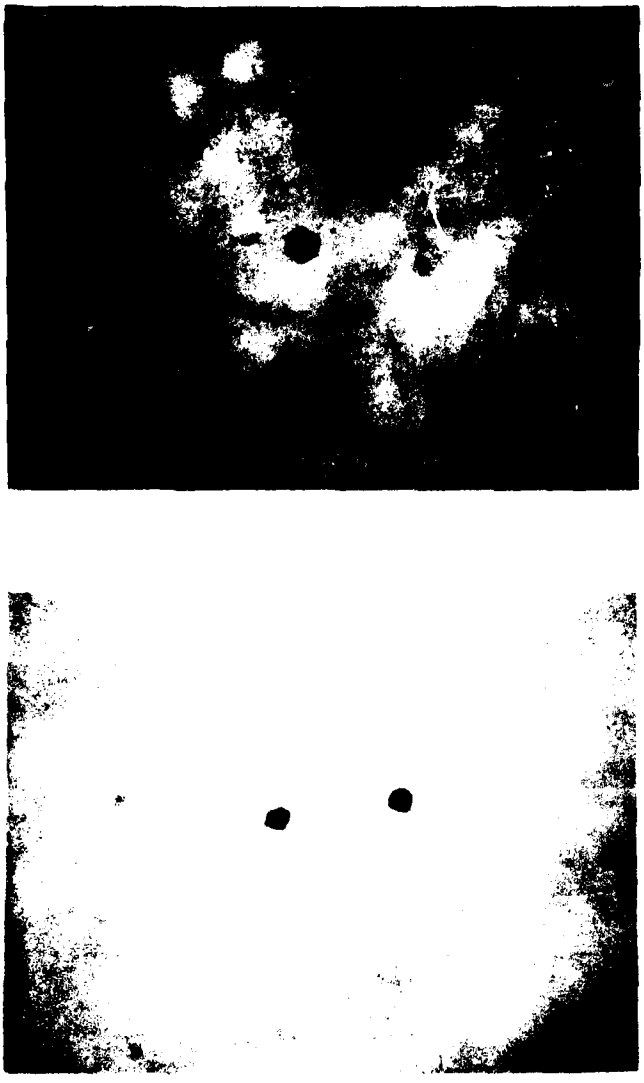


Figure 3. Cubic Inclusion in Tyco Sapphire (560X)

2. BULK SAPPHIRE IMMA EXPERIMENTS

IMMA experiments were conducted in an attempt to obtain information on impurity concentrations below the surface of the sapphire wafers. Earlier experiments performed during the first half of the contract were confined to the near-surface region because the ion-beam was restricted to low currents and surface charge-up of the specimen was not completely eliminated.

Samples to be analyzed were cleaned and mounted in the normal manner, and approximately 500 Å of gold was deposited on the surface to minimize surface charge-up. An elemental scan was made at the surface and then the beam current was increased to the maximum limit for the $^{16}O^-$ ion beam. Successive elemental scans were made after the sample had been sputtered for 10, 20 and 30 minutes. The data from these scans are presented in Figures 4, 5, 6, and 7.

Following the IMMA experiments, the depth of the crater resulting from the beam sputtering was measured with a Sloan Dektak and was found to be approximately 600 Å deep, indicating that the sputtering rate of sapphire at the maximum ion-beam current was of the order of 0.3 Å per second. Based on the depth measurement, most of the contaminants were found in the first few hundred angstroms of the surface of the material. From these results, we conclude that an analysis of the sapphire material which would consume a sufficient amount of material to represent a "bulk" analysis would be prohibitively expensive, because of the slow sputtering rate. Hence, no further attempts were made at determining bulk sapphire impurity levels using IMMA.

3. ALTERNATIVE SAPPHIRE IMPURITY ANALYSIS

In the first Scientific Report submitted in July 1975, it was mentioned that an attempt was being made at the Semiconductor Characterization Laboratory of the National Bureau of Standards to obtain impurity characterization data on bulk sapphire from samples of each vendor-type available to this program at that time. The samples were to have been characterized using flame-emission spectroscopy and neutron activation analysis. It was intended that this data would be compared with IMMA analysis data obtained from identical samples of material. To accomplish this, one wafer of each available vendor-type was cut in half, and one-half of the wafer was hand-carried to NBS. The remaining halves were each cut in half again, and one-quarter wafer of each vendor-type was submitted for IMMA analysis. The remaining quarter wafers were subjected to chemical surface etching to obtain defect density data. NBS was unable to obtain accurate data from flame-emission spectroscopy analysis, because of their inability to achieve a sufficiently clean surface. Hence, NBS supplied only data on neutron activation analysis. The neutron activation analysis data did not correlate to any significant extent with IMMA analysis data. IMMA analysis on the sapphire

Mass Spectrometer Response, 0.1 μA Full Scale

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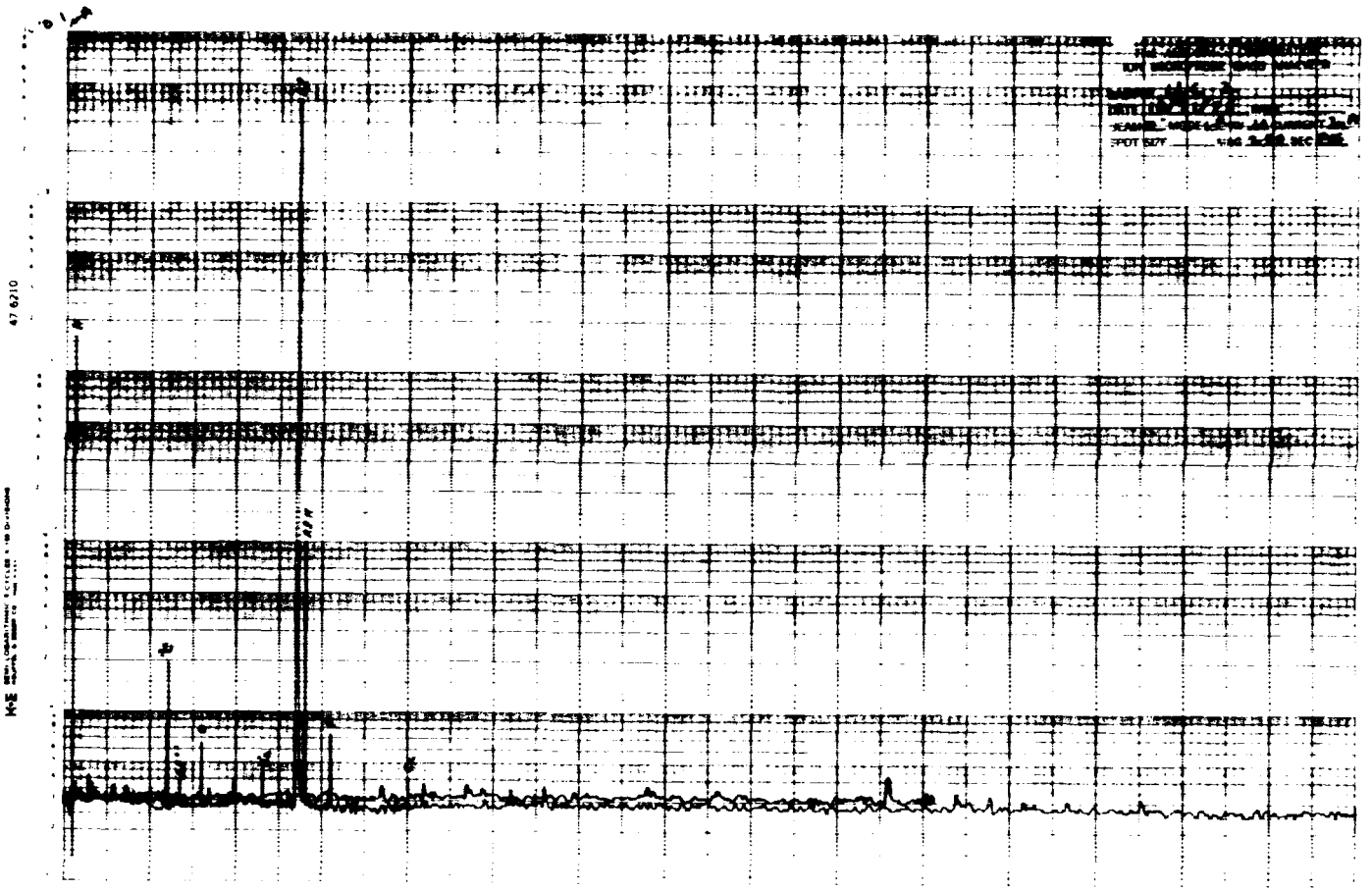

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Figure 4. IMMA Elemental Scan of Union Carbide Sapphire at Surface

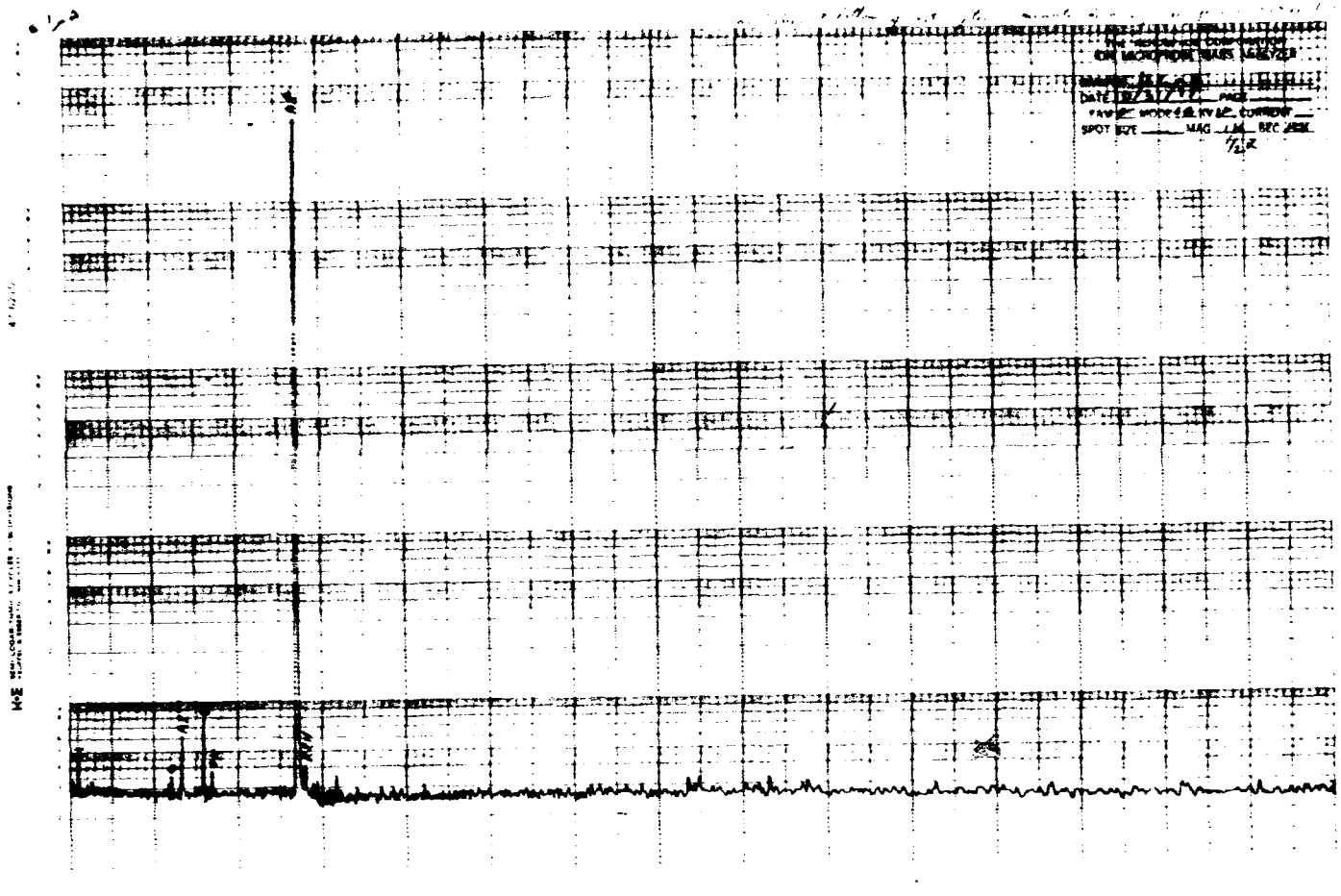


Figure 5. IMMA Elemental Scan of Union Carbide Sapphire After 10 Minutes

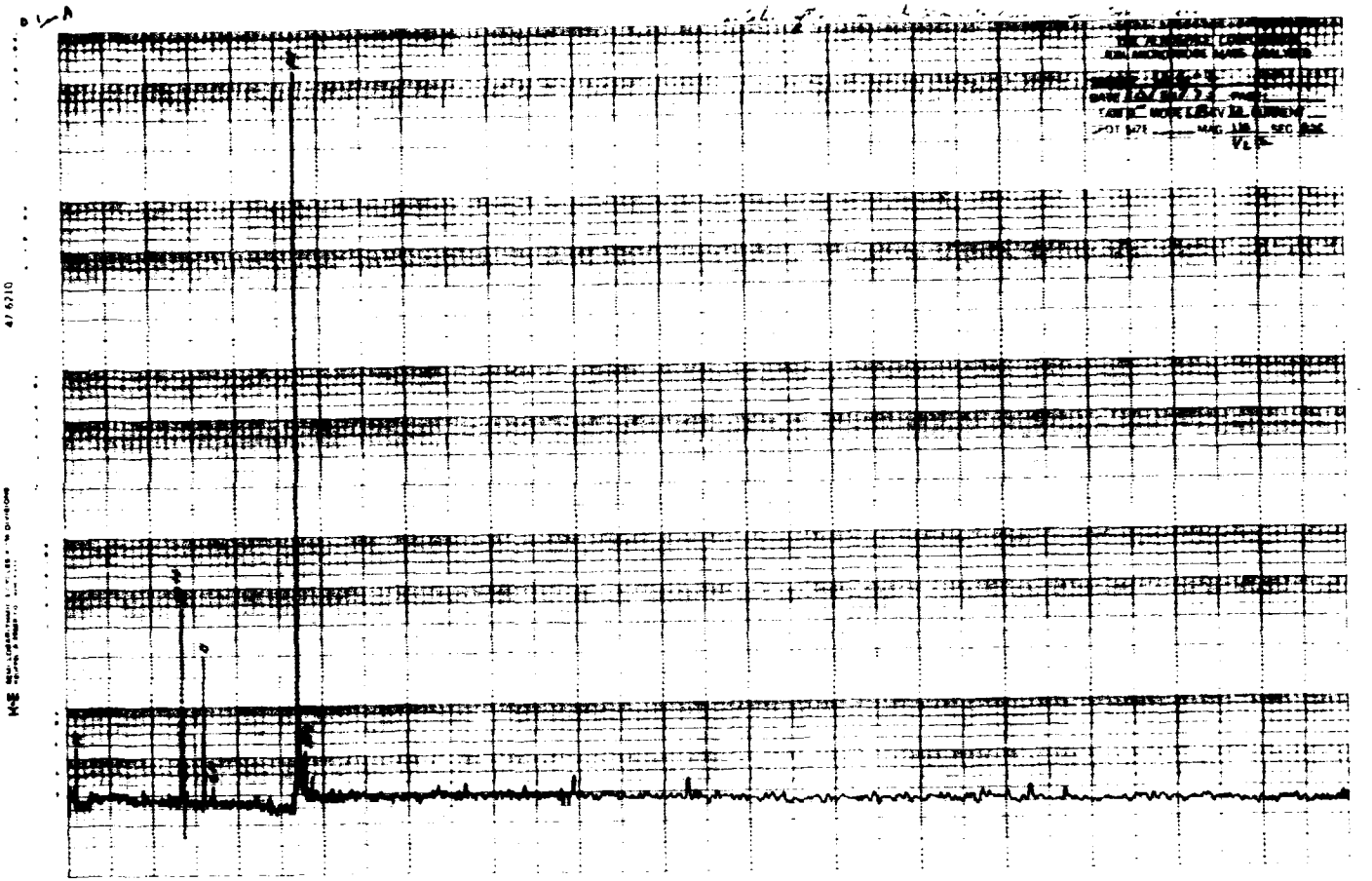


Figure 6. IMMA Elemental Scan of Union Carbide Sapphire After 20 Minutes

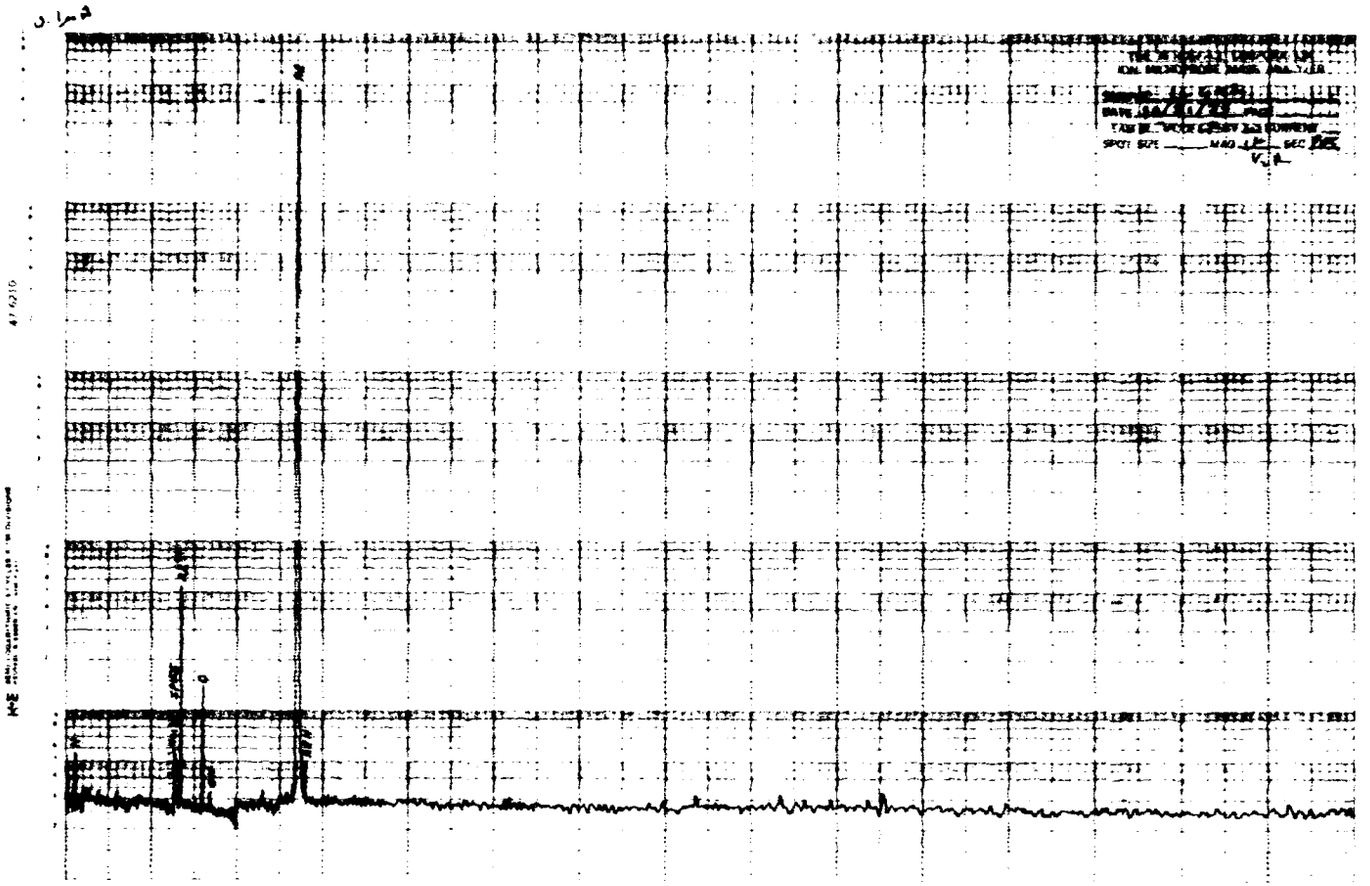


Figure 7. IMMA Elemental Scan of Union Carbide Sapphire After 30 Minutes

specimens indicated the presence of sodium, aluminum, potassium, calcium, chromium and iron. The neutron activation analysis data from NBS covered calcium, scandium, chromium, manganese, iron, cobalt, molybdenum and antimony. Most of the impurities listed in the NBS data indicate concentrations well below the 0.1 ppm level which is accepted as the lower limit of detection sensitivity of the IMMA. The sapphire analysis experiments performed with the IMMA also indicate that almost all of the contaminants found were confined to the surface of the material.

Concluding from these results, one reason for the difference between the IMMA and NBS analyses may be the manner in which the samples are cleaned and prepared.

SECTION III

SILICON-ON-SAPPHIRE

1. SILICON FILM DEPOSITION

Following the sapphire substrate characterizations with the selective etch and X-ray topography techniques, thin silicon films were deposited on the various sapphire substrate groupings. Each sapphire grouping, consisting of three sapphire sources--Union Carbide (U.C.), Tyco (T), and Crystal Systems (C.S.)--with the polishing variations supplied by Union Carbide, Tyco and Insaco, was divided into two groups with each group receiving a silicon deposition from a different source. The first group received silicon epitaxy from Union Carbide as described in the previous Scientific Report. The second group was to receive the silicon films from Rockwell International. The Rockwell facility, because of other conflicting commitments, was unable to supply the required high quality films. Wafers which had the Rockwell film, therefore, were stripped, except for some with U.C. sapphire (these wafers are discussed separately below).

An alternate silicon deposition source was found in Hewlett Packard, who showed considerable interest in the SOS films study and offered to supply the silicon films for the second group of wafers. The silicon films deposited at Hewlett Packard were carried out in an Applied Materials vertical reactor. The wafers were first precleaned in a low sodium detergent solution with an III wafer scrubber. The preclean was then followed by a standard sulphuric acid-hydrogen peroxide clean to remove any organic material left from the scrubbing cycle. The wafers were finally rinsed in deionized water and spin-dried in dry N_2. The sapphire substrates were then cleaned in the reactor during a short prefiring cycle in H_2 at an elevated temperature >1100°C. Following the prefiring, the silicon films were deposited at 950 to 970°C to a thickness of ~.9 μ and doped with phosphorus to a doping level of ~1 x 10^{15} cm^3.

2. SILICON ANALYSIS

Silicon films deposited by Union Carbide and Hewlett Packard were analyzed using IMMA. Almost without exception, the contaminants found in the epitaxial silicon films were either on the surface or were distributed throughout the epitaxially deposited silicon layers. IMMA surface mapping analysis indicates that these contaminants consist primarily of residual polishing components and sapphire debris remaining in scratch regions on the surface of the sapphire substrate. Figure 8 shows an IMMA surface map of a sample of Union Carbide epitaxial silicon on Union Carbide sapphire. The individual elemental surface maps were made on the basis of overall impurity levels revealed by an initial elemental scan of the area of interest. The area mapped in Figure 8 was

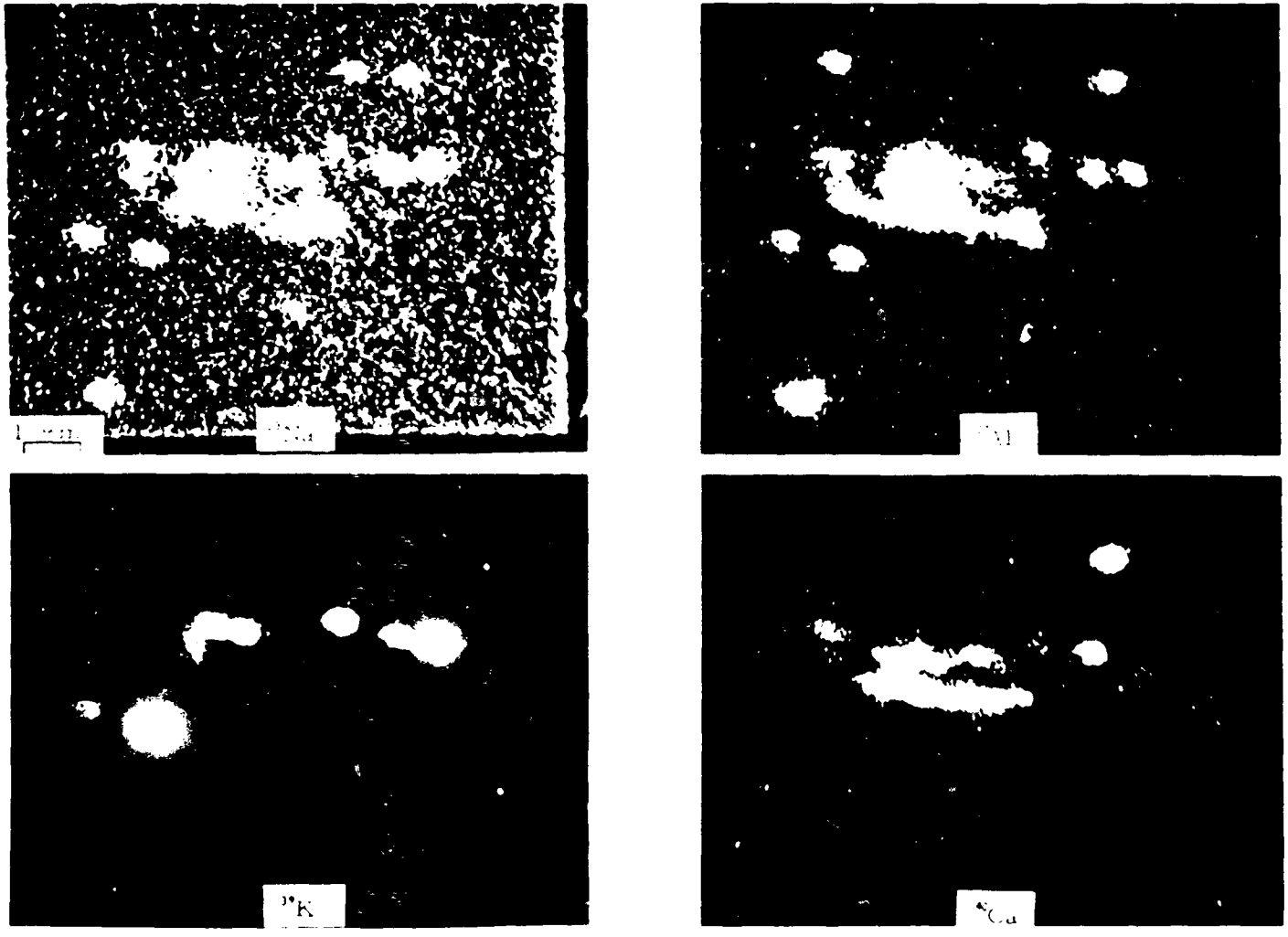


Figure 8. IMMA Elemental Surface Map of Union Carbide SOS Material

subsequently examined with a scanning electron microscope which revealed an apparent defect in the sapphire substrate. An SEM photomicrograph of the area is shown in Figure 9(a) and 9(b). The photograph in Figure 9(a) shows a shadowy line, marked by arrows on either side of the photograph, which appears to be a defect in the sapphire substrate. The light colored irregularity in the center of Figure 9(a) corresponds very closely with the surface maps of Figure 8.

As noted earlier in this report, it was not possible to obtain the required films from the in-house source. Samples from one run, however, were saved as examples of "poorer" quality SOS films, resulting from inadequate process control. Figures 10 and 11 show IMMA surface maps and SEM photomicrographs of typical epitaxial silicon films that were obtained. In both figures, the main contaminant is aluminum appearing as particulate matter introduced during sapphire preparation.

Epitaxial silicon films were deposited by Hewlett Packard on sapphire wafers from each of the three vendors, and these wafers were used as the second-source of epitaxial films. The silicon films furnished by Hewlett Packard were comparable in surface quality to those received from Union Carbide. An IMMA elemental scan and surface map of a Hewlett Packard silicon film grown on Crystal Systems sapphire, polished by Insaco, showed a high degree of contamination. Subsequent optical examination at 560X revealed a very fine scratch or defect running through the area of the IMMA raster. A surface map of an adjacent area on the same specimen showed no particulate or localized contamination sites.

Particulate contaminants were found to be present in the epitaxial silicon films obtained from all sources. However, it should be pointed out that the examples presented in this report represent the extreme in most instances. No attempt was made to seek out sites of contamination in any of the materials analyzed, and where contaminant sites were found, it was usually possible to move to a different location on the sample and find relatively clean areas. Of the epitaxial films examined under this contract, the Union Carbide and Hewlett Packard films were of comparable quality. The in-house material was of generally poorer quality with a high degree of particulate contamination present over the entire wafer surface.

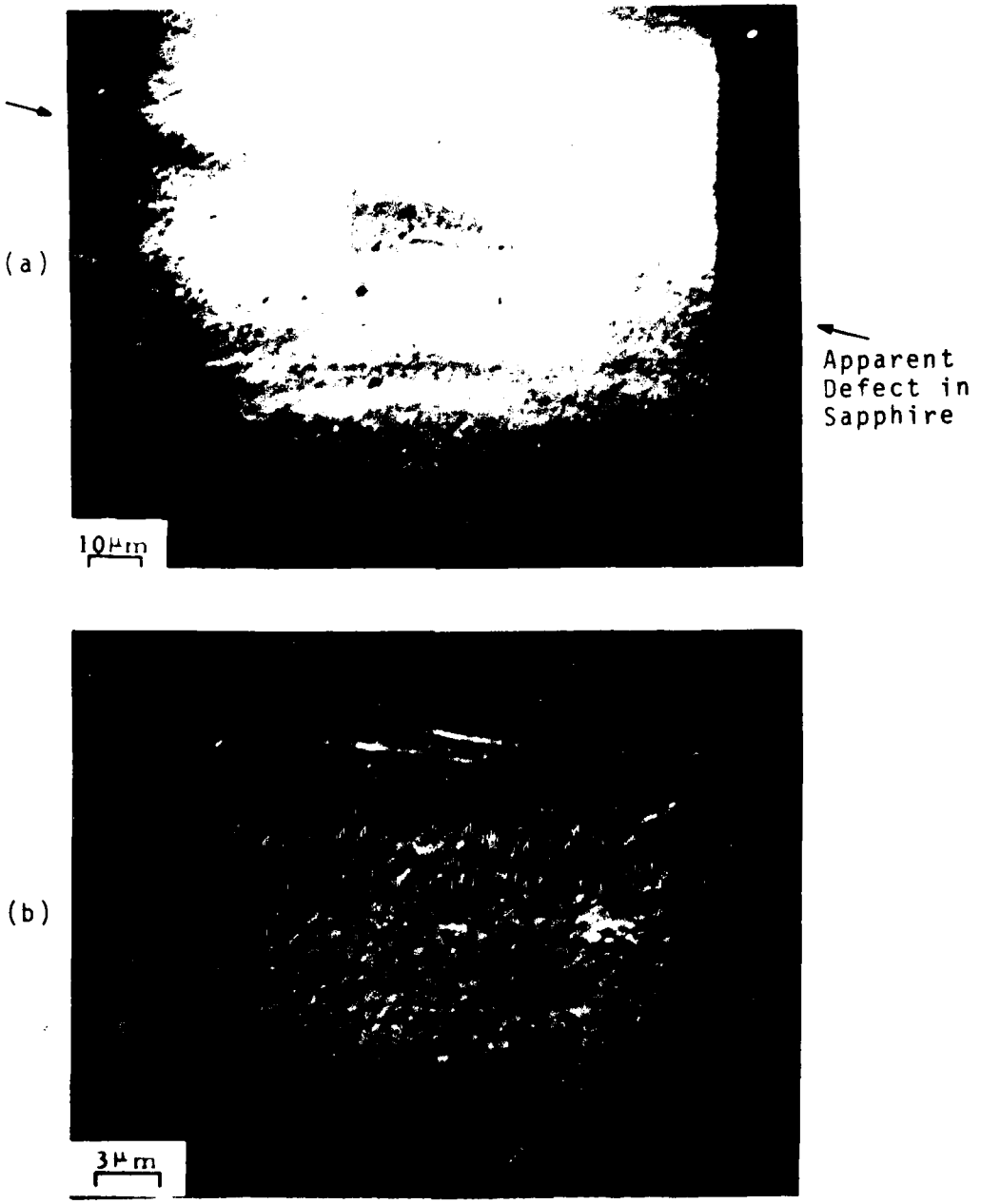


Figure 9. Scanning Electron Microscope Display of IMMA Surface Map Area

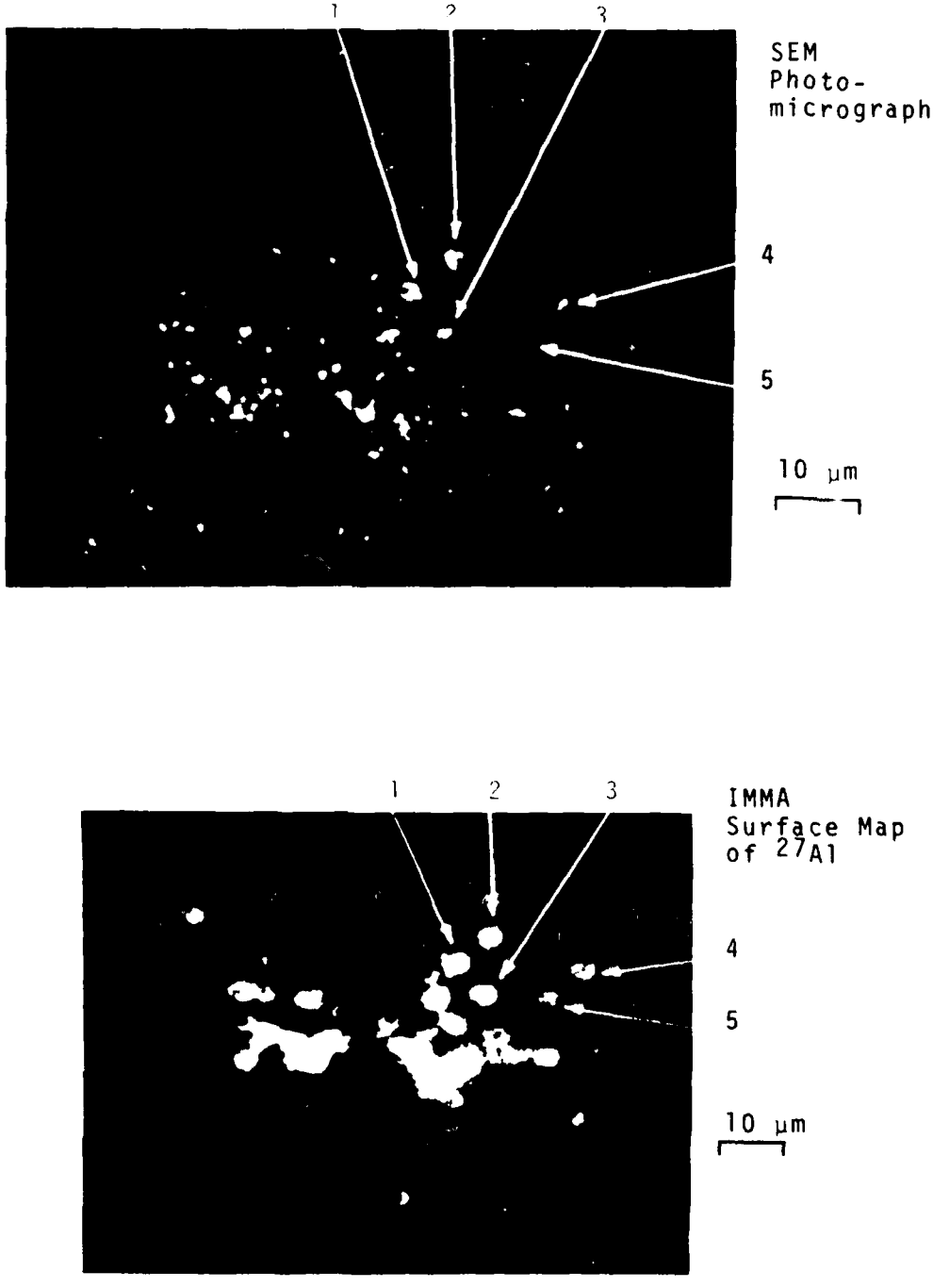


Figure 10. Comparison of IMMA and SEM Observations of Epitaxial Silicon-on-Sapphire

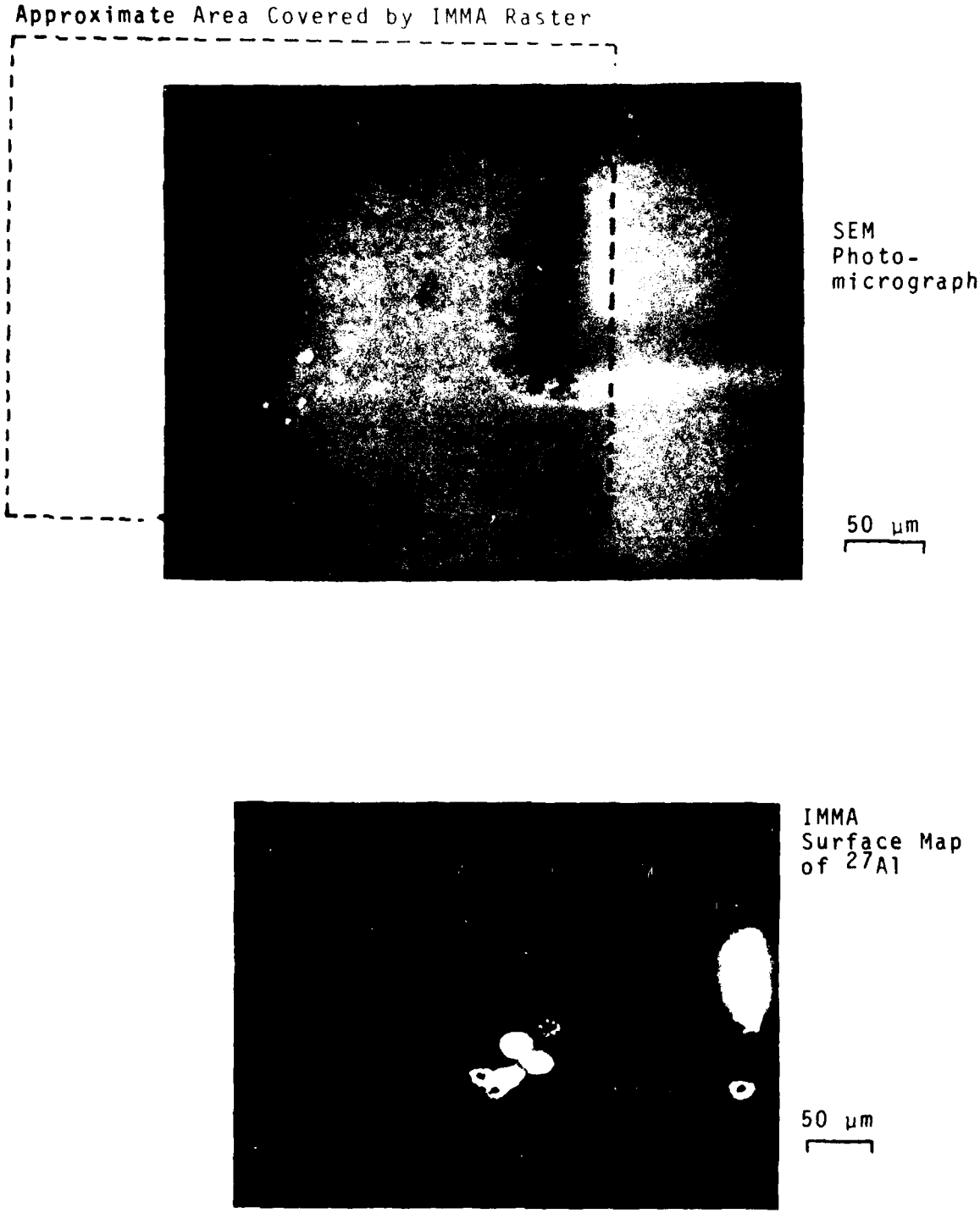


Figure 11. Comparison of IMMA and SEM Observations of Epitaxial Silicon-on-Sapphire

SECTION IV

TEST DEVICE CHARACTERIZATION

1. DEVICE FABRICATION

The basic processing of the 4007 circuits was outlined in the July 1975 Scientific Report. For the fabricated devices, there was one change to the original processing schedule relating to the p-well ion implant conditions. This change consisted of delaying the p-well ion implant to just before the gate oxidation step and included an additional ion implant of the surface regions of the islands to minimize island edge effects. The additional implant dose was 5×10^{12} cm^{-2} for the first lots reported (503, 504, 505), but was changed to 3×10^{12} cm^{-2} for the last two lots (506, 507). The different implant levels explain the higher initial threshold voltages observed for the former lots.

All lots fabricated showed excellent bias-temperature stability for the stress conditions of 260°C for 30 minutes with + or -10 volts gate bias (all other terminals grounded). The temperature-induced threshold changes were generally less than $\pm$.1 volt.

Wafers from lots where the fewest processing problems were evident after optical screening were chosen for further electrical and radiation testing. These lots were 503, 504, 506 and 507. Lots 501 and 502 were judged to be unacceptable for the purposes of this program. Lot 503 had a relatively poor metal etch but also had a much poorer circuit yield than the other lots, with many devices failing leakage tests. Table II shows the results of the optical screening for the various wafer groups in the program.

Lot 505 consisted mainly of wafers processed for internally-funded research pursuits. Data from one wafer from this group with silicon epitaxy from Rockwell are shown to demonstrate results of a poor silicon film on backchannel radiation hardness.[4]

2. DEVICE CHARACTERIZATION

a. C-V Measurements

C-V measurements were made on 10 x 10 mil test capacitors contained on all the processed wafers. Information obtained from these measurements included the oxide thickness and doping levels for both the n- and p-base regions of the complementary transistors.

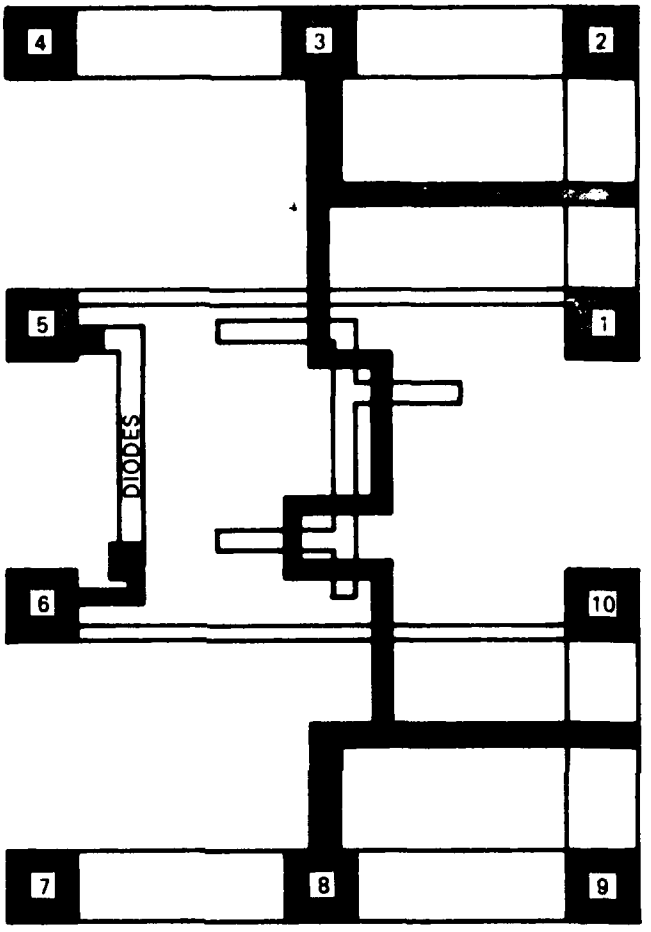
b. Process Evaluation Test Structure Measurements

Each 4007 wafer contains a number of process evaluation test patterns shown in Figure 12. Seven test patterns were chosen

Table II. Comparison of Wafer Lot Processing for Lots 503 - 507

Lot No.	503	504	505	506	507
Wafer Group					
Lab Stock U.C./U.C./U.C.	UA - M	A	-	-	-
U.C./U.C./U.C.	UA - M	A	-	-	-
U.C./U.C./H.P.	-	-	-	A	A
U.C./U.C./R.I.	-	-	A	-	-
Tyco/U.C./U.C.	A	UA - M	-	-	-
Tyco/U.C./H.P.	-	-	-	A	UA - P
Tyco/Tyco/U.C.	-	-	-	A	UA - N
Tyco/Tyco/H.P.	-	-	-	A	A
C.S./U.C./U.C.	UA - M	A	-	-	-
C.S./U.C./H.P.	-	-	-	A	A
C.S./Ins./U.C.	UA - M	A	-	-	-
C.S./Ins./H.P.	-	-	-	A	A

A - Acceptable processing
UA - Unacceptable processing
P - p-channel leakage
N - n-channel leakage
M - metal etch problems



1. P CH DRAIN (0.3x3) AND P^+ RES
2. P CH SOURCE
3. P CH GATE AND METAL CONTINUITY
4. P CH DRAIN (3x3)
5. GP DIODE AND P^+ RES
6. GP DIODE AND N^+ RES
7. N CH DRAIN (3x3)
8. N CH GATE AND METAL CONTINUITY
9. N CH SOURCE
10. N CH DRAIN AND N^+ RES

Figure 12. 10 Pad Test Circuit

for characterization on each wafer as shown in Figure 13. The data obtained by probing these test devices were reduced by computer to produce the following process related characterization:

- Metal continuity - resistance of a 0.5 mil metal line which runs over eight silicon edge steps (Pads 3 and 8).

- P^+, N^+ sheet resistance - resistance between Pads 1 and 5 and Pads 6 and 10, respectively.

- Gate protection Zener diode leakage current and breakdown - current with +12 V applied between Pads 5 and 6; and voltage between Pads 5 and 6 with 1 μA injected into terminal 5 or 6, respectively.

- Gate and drain leakage and breakdown voltage of 3 x 3 mil and 0.3 x 3 mil p- and n-channel transistors - gate current with +20 V applied between gate and drain/source; drain current with 5 V turn-off voltage applied between gate and source and 10 V applied between drain and source; and voltage between drain and source with 5 V gate to source turn-off voltage and 10 μA injected into drain, respectively.

- Low voltage parameters (V_D = 0.1 V) including channel mobility and channel length - mobility determined from computer least squares fit to I_D - V_G characteristics; channel length determined from ratio of transconductances for 3 x 3 mil and 0.3 x 3 mil transistors.

- Operating parameters including threshold voltage, leakage current and channel "on" current with drain voltages of 2, 8, 10 and 12 volts. Operating threshold determined by least squares fit and extrapolation of I_D - V_G characteristics; channel "on" current measured with gate-to-source voltage of 10 volts.

Data obtained from the process evaluation test structures for lots 504 and 507 are summarized in Table III. These data were used to determine which wafers should be considered for detailed wafer mapping.

c. Wafer Mapping

The wafer shown in Figure 13 contains a number of test circuits and 4007H dual complementary pair plus inverter circuits. The process evaluation test structure (test 10 pattern) has been previously discussed. Circuits identified as 4007C, P, and E in Figure 13 represent special versions of the circuit featuring

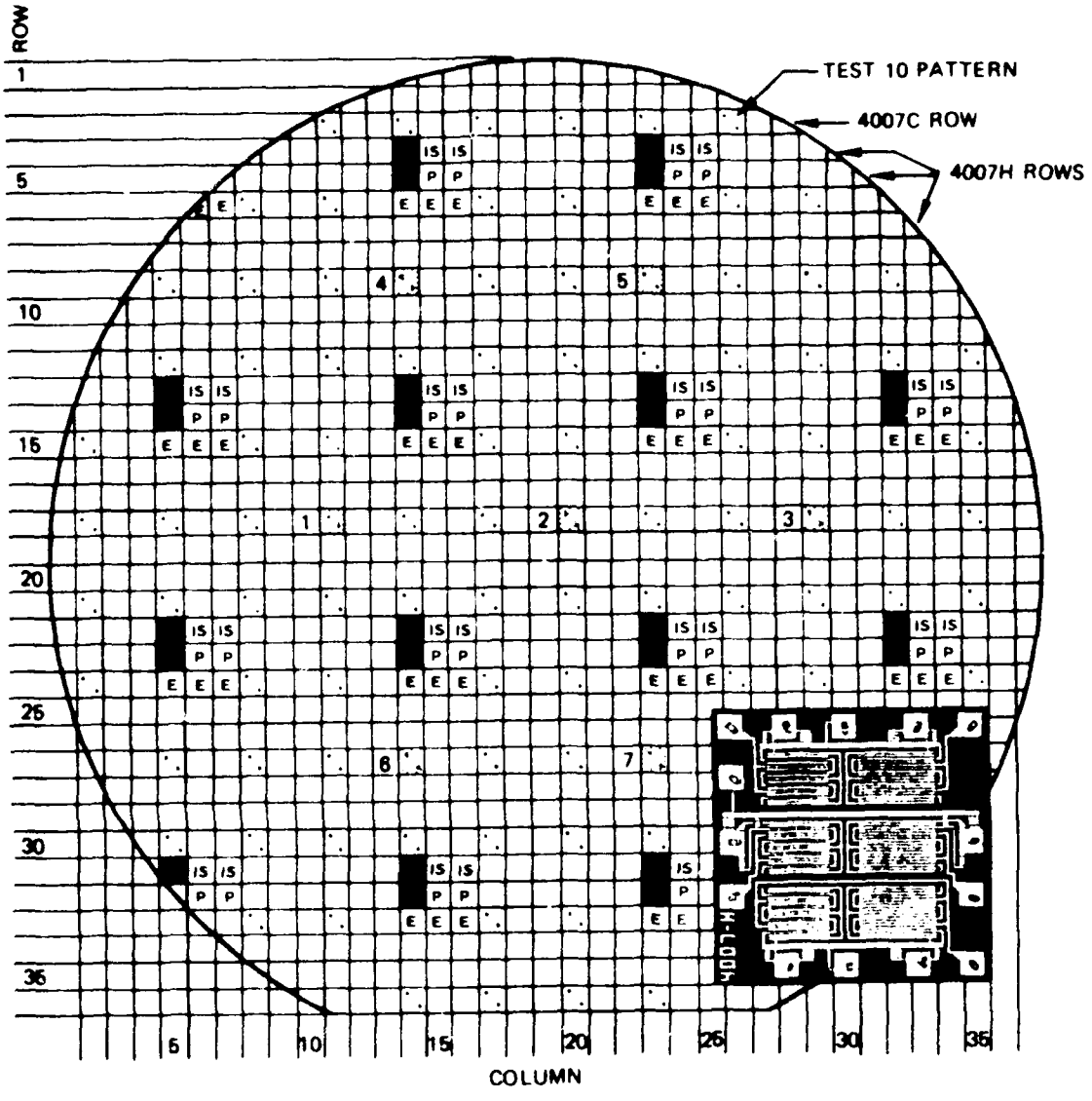


Figure 13. Wafer Die and Inverter Location

Table III. AFCRL Wafer Test Data

Test 10 Data Summary

	Wafer	Vendor - Polisher - Epi	V_{TN}	V_{TP}	I_{LN} nA	I_{LP} nA	BV_N	BV_P	L_N	L_P	μ_N	μ_P
LOT 504 UC EPI	1,2	UC - UC	1.94	-2.23	101.6	0.79	16.0	>24	7.00	6.33	356	206
	4	CS - UC	1.96	-2.29	8.7	0.82	16.3	>24	6.81	6.30	349	198
	5	CS - Insaco	1.75	-2.18	123	0.58	15.3	>24	6.70	6.10	360	216
	7,8	Tyco - UC	2.28	-2.42	1067	0.62	17.1	>24	6.88	6.50	316	186
	9,10	Lab Stock	1.96	-2.00	53.2	1.80	16.2	>24	6.86	6.23	351	201
LOT 507 HP EPI	1,2	Tyco - Tyco - UC	1.19	-2.26	4152	1.25	16.7	>24	6.41	6.42	387	210
	3,4	CS - UC	1.42	-2.06	32.6	1.30	16.6	>24	6.04	6.36	344	196
	5,6	CS - Ins.	1.34	-2.06	27.6	1.27	17.0	>24	6.11	6.61	338	192
	7,8	Tyco - UC	1.12	-1.95	7.7	0.57	17.2	>24	6.24	6.48	364	206
	9,10	Tyco - Tyco	1.33	-2.15	3.2	0.57	17.0	>24	6.42	6.70	340	198
	11,12	UC - UC	1.32	-2.07	41.5	0.63	17.6	>24	6.63	6.69	348	195

	Row	Col.	I_{LP}	I_{LN}	V_{OUT} High	V_{OUT} Low
	19	10	.1215E-07	.1927E-05	9.655	.258
	19	10	.1112E-07	.1276E-05	9.638	.259
	19	10	.2602E-07	.3632E-07	9.642	.272
	19	11	.1163E-07	.3514E-07	9.653	.259
	19	11	.1114E-07	.3057E-07	9.645	.258
	19	11	.2373E-07	.3646E-07	9.649	.275
	19	12	.1126E-07	.3056E-07	9.649	.258
	19	12	.1134E-07	.3252E-07	9.641	.260
	19	12	.2171E-07	.2741E-05	9.645	.274
	19	13	.1145E-07	.6703E-06	9.652	.260
	19	13	.1182E-07	.2959E-07	9.641	.257
	19	13	.2009E-07	.2850E-07	9.650	.271
Inverter 2	19	14	.1144E-07	.3376E-07	9.647	.262
Inverter 1	19	14	.1176E-07	.3789E-07	9.630	.261
Inverter 3	19	14	.1744E-07	.1780E-05	9.642	.275
	19	15	.1162E-07	.3563E-06	9.649	.261
	19	15	.1241E-07	.3555E-07	9.630	.260
	19	15	.1689E-07	.3219E-07	9.648	.276
	19	16	.1224E-07	.3339E-07	9.655	.257
	19	16	.1161E-07	.3405E-07	9.644	.256
	19	16	.1575E-07	.1623E-06	9.656	.267
	19	17	.1236E-07	.3266E-07	9.657	.258
	19	17	.1206E-07	.3391E-07	9.641	.256
	19	17	.1551E-07	.1287E-06	9.655	.271
	19	18	.1437E-07	.3517E-07	9.651	.257
	19	18	.1337E-07	.4257E-07	9.641	.255
	19	18	.1578E-07	.3185E-07	9.649	.273
	19	19	.1336E-07	.3358E-07	9.654	.265
	19	19	.1314E-07	.3645E-07	9.646	.263
	19	19	.1689E-07	.4877E-07	9.658	.272
	19	20	.1325E-07	.3532E-07	9.649	.269
	19	20	.1370E-07	.3521E-07	9.637	.266
	19	20	.1610E-07	.7477E-06	9.647	.281

Figure 14. Wafer Map Printout Sample

diode-clamped body regions, separate body terminals, and edgeless transistors, respectively. The structure designated IS represents a circuit for determining propagation delay through CMOS/SOS inverter strings. The blackened areas represent patterns, useful for IMMA analysis, consisting of a 40 x 40 mil n-type starting material region and a similar sized region of p-well implanted material.

The following wafer map data are presented for the standard 4007H circuits (see inset Figure 13) designated by the unmarked squares in Figure 13. To facilitate computer-aided data acquisition, only rows consisting entirely of 4007H circuits were probed--neglecting those rows containing 4007H circuits in combination with one or more of the special circuits or test structures described above.

Each of the three structures (dual complementary pair plus inverter) in the 4007H circuit was checked for functionality (static switching between high and low states with a 10 volt power supply voltage and a 3 mA load) and for n- and p-channel junction leakages (gate shorted to the source and 10 volts applied between the drain and source terminals). The results of each test were printed out as shown in Figure 14. The first two entries identify the row-column location of the die being tested, followed by the p- and n-channel leakages in amperes, respectively, and then the magnitudes of the high and low output states, respectively. Three lines of data are shown for each location--each line designating the particular structure tested in the order 2, 1, 3, as shown in the inset of Figure 13.

In addition to the printed data, all measurements were recorded on paper tape. Following probing, the data were read into a TSO computer terminal for editing and screening with respect to several pass-failure criteria. A typical computer print-out for one set of pass-fail criteria is shown in Figure 15. A coded distribution map, an alternate form of computer output, is shown in Figure 16.

In Figure 15, the first data items ($1e^{-7}$, $1e^{-7}$, 9.5, 0.7) represent the p-channel leakage, n-channel leakage, high output voltage, and low output voltage screening criteria, respectively. Following the screening criteria, the number of circuits failing the indicated combinations of the screening criteria are given. Following this listing, a failure distribution is given for each of the four parameters (low and high output voltages--p- and n-channel leakages). For example, the lines beginning with <0.5, <1.0, ... and 1597, 34, ... are interpreted as 1597 circuits had low output state voltages <0.5 volt, 34 circuits had low output voltages between 0.5 and 1.0 volt, etc.

Figure 16 displays the wafer probe data with respect to the relative location of the individual circuits within the wafer. The screening criteria are listed in the upper left side of the

```
run afcl1.fort.fort
G1 COMPILER ENTERED
SOURCE ANALYZED
PROGRAM NAME = MAIN
*  NO DIAGNOSTICS GENERATED
TYPE IN THE P-CH AND N-CH  CRITERIA ?
?
1e-7,1e-7,9.5,0.7
NUM. OF HIGH AND LOW VOLTAGE FAIL =  80
         NUM. OF HIGH VOLTAGE FAIL =  54
         NUM. OF LOW VOLTAGE FAIL =  73
       NUM. OF N-CH AND P-CH FAIL =  26
                 NUM. OF P-CH FAIL =  57
                 NUM. OF N-CH FAIL= 189
            TOTAL NUM. OF P-CH PASS=1510      83.89
            TOTAL NUM. OF N-CH PASS=1378      76.56
     TOTAL NUM. OF INVERTERS PASS=1300      72.22
                 NUM. OF DIE PASS= 313      52.17
NHC0011 EXECUTION TIMES=     11
READY
run afcl2.fort.fort
G1 COMPILER ENTERED
SOURCE ANALYZED
PROGRAM NAME = MAIN
*  NO DIAGNOSTICS GENERATED
TYPE IN THE P-CH AND N-CH  VOLTAGE ?
?
9.5,0.7
 HIGH & LOW =  80   HIGH ONLY=  54   LOW ONLY    73
     <0.5      <1.0      <1.5      <2.0      >2.0
     1597        34         3         2       138
     92.0      <8.5      <4.0      <2.5      >2.5
      111         5        22        18      1623
   P-CHANNEL LEAKAGE CURRENT
<1E-8 <1E-7 <1E-6 <1E-5 <1E-4 <1E-3 >1E-3
  403   1020     40     32      3      6      2
   N-CHANNEL LEAKAGE CURRENT
<1E-8 <1E-7 <1E-6 <1E-5 <1E-4 <1E-3 >1E-3
   23   1285    115     65     23     10      2
NHC0011 EXECUTION TIMES=     12
```

Figure 15. Wafer Pass-Fail Summary Listing

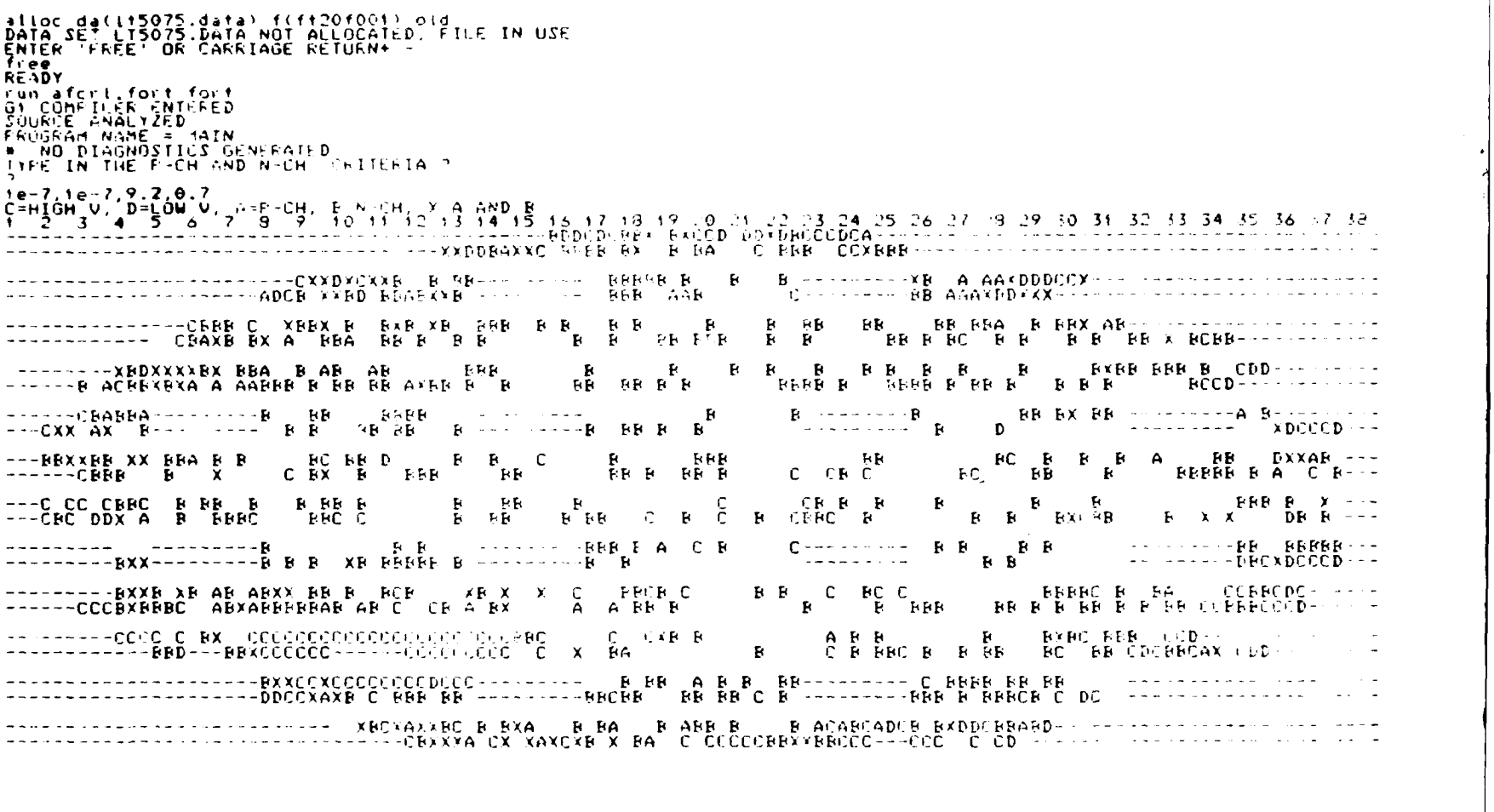


Figure 16. Wafer Pictorial Distribution Map

figure. Column locations of the circuits are designated 1-38 across the page. The failure mode of each circuit is designated by the following code:

A = p-channel leakage failure only

B = n-channel leakage failure only

C = high output state failure only

D = low output state failure only

X = A and B failures only

Blank = no failures

Table IV summarizes the results of all wafer map data acquired to date. Each wafer was assumed to contain 600 testable dice (1800 circuits).

d. IMMA Device Analysis

Experiments were conducted on 4007H inverter circuits in an attempt to determine the cause of excessive leakage currents in n-channel devices. The circuits analyzed were fabricated from Union Carbide silicon. In one case, the substrate was Union Carbide sapphire, polished by Union Carbide; the other film was grown on Crystal Systems sapphire, polished by Insaco.

The circuits were prepared for analysis by first stripping the silox overcoating and contact metallization. The sample was cleaned and mounted in the standard manner and then it was given a coating of approximately 500 Å of gold to provide a current path across the sapphire substrate from the silicon island to the metal sample holder.

IMMA examination of the circuits on Union Carbide sapphire showed uniform, low concentrations of contaminants over the entire n-channel devices. The set of surface maps shown in Figure 17 covers an area approximately 75 x 60 μm on one corner of an n-channel device. All eight channel edges were examined and found to be free of any localized sites of contamination.

Figure 18 shows two different areas on circuits fabricated on the Crystal Systems/Insaco sapphire prior to stripping of silox and metal. The diagonal lines running through the circuits appear to be saw marks which remain after sapphire polishing. Surface map analysis of the failed devices showed that there were no differences in contamination levels in the saw marks and surrounding material. However, in the p-channel device, the ion-beam sputtered through the silicon more rapidly over the saw marks than in the surrounding area. This result indicates that one mechanism that should be further studied to explain the excessive n-channel leakage is phenomena associated with structural irregularities in the silicon caused by the nonuniformity in the surface of the substrate. Such irregularities may enhance

Table IV. Summary of Wafer Probe Data for 4007H Circuits

Lot	Wafer	Vendor/Polisher	Die Yield	Inverter Yield	n-Channel Yield	p-Channel Yield	Comments
503	1	UC/UC	2.7	23.4	36.7	56.2	
	4	CS/UC	1.2	21.1	35.7	62.4	
	5	Tyco/UC	21.7	52.8	66.9	72.9	
	8	CS/Insaco	6.3	30.6	45.7	64.4	
	9	Lab Stock	0.0	10.8	18.1	46.2	
504	1	HC/UC	8.3	36.7	45.9	63.9	
	2	UC/UC	23.3	50.3	59.5	77.6	
	4	CS/UC	29.2	55.7	62.2	76.3	
	5	CS/Insaco	52.0	72.2	76.6	83.9	
	7	Tyco/UC	0.0	0.1	0.3	39.2	Bad Metal
	8	Tyco/UC	6.8	27.9	46.5	49.8	
	10	Lab Stock	27.3	56.6	64.4	79.8	
507	4	CS/UC/HP	21.5	50.8	55.2	78.1	
	5	CS/Insaco/HP	19.8	50.3	53.2	77.6	VOH >9.2 Volts
	7	Tyco/UC/HP	10.3	36.0	53.0	67.1	2/3 Wafer
	10	Tyco/Tyco/HP	12.2	31.8	47.3	51.8	
	12	UC/UC/HP	12.5	31.6	41.1	52.2	
506	1	Tyco/Tyco/UC	13.3	48.1	54.9	60.8	
	4	CS/UC/HP	20.5	47.6	54.1	74.5	
	5	CS/Insaco/HP	30.5	58.9	63.7	82.3	
	7	Tyco/UC/HP	44.8	69.6	73.7	82.0	
	10	Tyco/Tyco/HP	25.3	55.1	65.0	71.7	
	12	UC/UC/HP	38.0	63.4	64.8	73.7	

Pass Criteria:

VOH	>9.5 V	(3 mA Load)
VOL	>0.7 V	(3 mA Load)
ILP	≤100 nA	With V_{DS} = +10 V
ILN	≤100 nA	With V_{DS} = +10 V

Assume: 600 Dice
1800 Inverters

Table IV. Summary of Wafer Probe Data for 4007H Circuits
(Continued)

Lot	Wafer	Vendor/Polisher	Die Yield	Inverter Yield	n-Channel Yield	p-Channel Yield	Comments
503	1	UC/UC	8.0	35.4	48.6	63.3	
	4	CS/UC	6.3	35.4	49.9	69.1	
	5	Tyco/UC	30.7	60.5	72.5	77.2	
	8	CS/Insaco	14.5	42.2	56.2	71.0	
	9	Lab Stock	2.2	23.9	31.9	55.5	
504	1	HC/UC	19.7	51.4	60.0	70.6	
	2	UC/UC	42.2	66.1	72.9	84.8	
	4	CS/UC	43.8	65.4	71.3	78.7	
	5	CS/Insaco	61.0	78.2	82.1	85.4	
	7	Tyco/UC	1.5	6.1	10.9	47.5	Bad Metal
	8	Tyco/UC	12.2	39.3	57.2	58.5	
	10	Lab Stock	44.0	68.4	73.8	84.6	
507	4	CS/UC/HP	35.3	61.5	66.8	79.1	
	5	CS/Insaco/HP	36.0	63.9	66.7	81.1	VOH >9.2 Volts
	7	Tyco/UC/HP	21.3	46.8	64.5	72.0	2/3 Wafer
	10	Tyco/Tyco/HP	23.3	39.8	54.4	56.0	
	12	UC/UC/HP	21.5	39.1	49.5	53.1	
506	1	Tyco/Tyco/UC	29.7	58.6	60.4	67.7	
	4	CS/UC/HP	42.8	63.1	69.2	76.4	
	5	CS/Insaco/HP	53.7	73.8	77.4	84.4	
	7	Tyco/UC/HP	58.8	77.7	79.3	85.8	
	10	Tyco/Tyco/HP	37.5	66.1	71.7	77.9	
	12	UC/UC/HP	46.3	68.4	69.9	74.3	

Pass Criteria:

VOH	>9.5 V	(3 mA Load)
VOL	>0.7 V	(3 mA Load)
ILP	≤500 nA	With V_{DS} = +10 V
ILN	≤500 nA	With V_{DS} = +10 V

Assume: 600 Dice
1800 Inverters

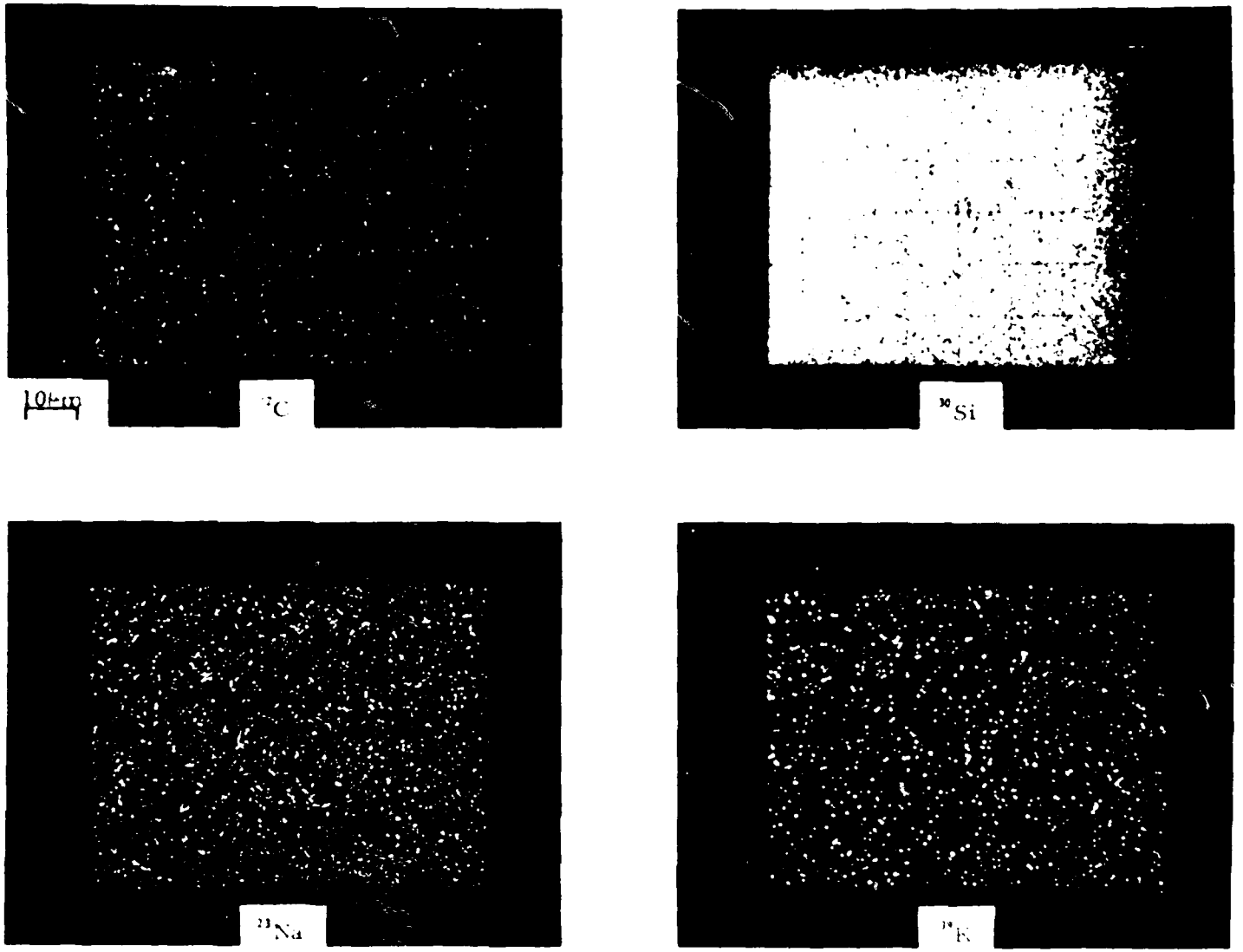
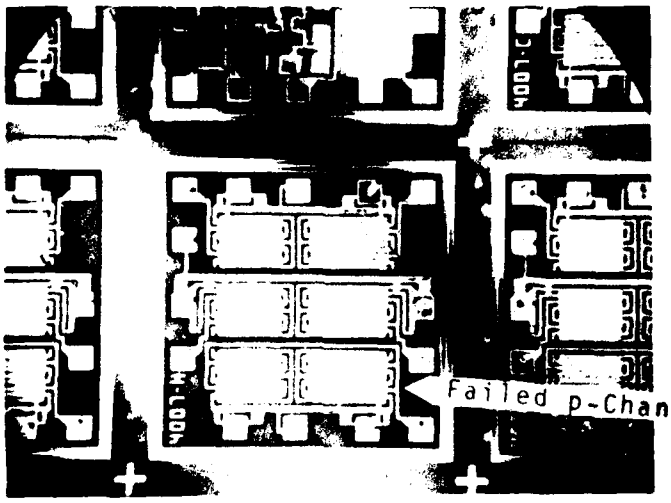


Figure 17. IMMA Surface Map of n-Channel Region of 4007 Device



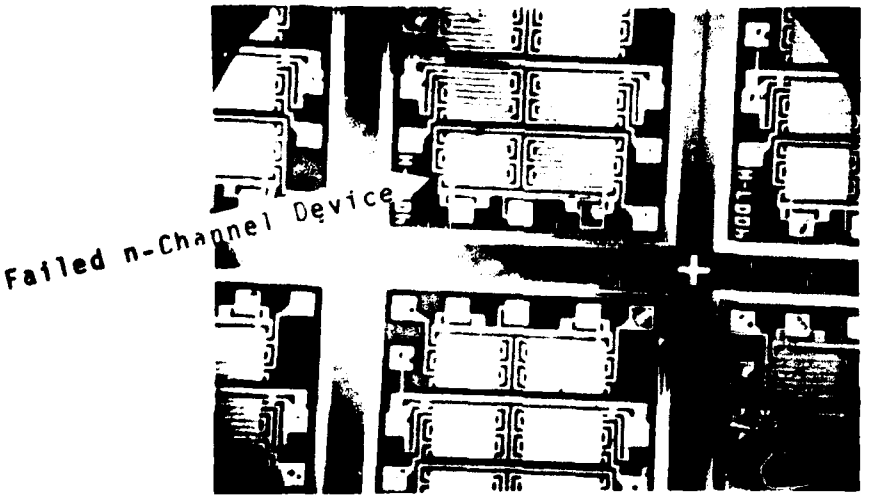


Figure 18. 4007 Circuits Fabricated on Crystal Systems Sapphire, Showing SAW Marks Running Through Failed Circuits

diffusions from the source-drain regions causing increased leakage and affecting eventual device yield.

Surface map analysis was also performed on the 1 mm square test areas, described above, representing starting and p-well implanted regions.* These test areas were not subjected to all the processing steps used in circuit fabrication and as a result very little of the original surface was consumed. A high degree of contamination was found in these areas, much of it being localized at point-sites. Surface maps are shown in Figures 19 and 20 for the Union Carbide and Crystal Systems substrates, respectively, with Union Carbide silicon epitaxy.

The IMMA results indicate that most of the initial contamination sites, observed on the starting SOS material, were removed during the several oxidation and subsequent etching and diffusion cycles carried out during the fabrication of the circuits.

3. RADIATION CHARACTERIZATION

Devices representative of the fabricated wafers were characterized prior to and following Co^{60} exposure under various bias conditions. The primary purpose of these experiments was to determine the gate oxide radiation hardness by monitoring the shifts in threshold voltage and to determine the hardness of the sapphire-silicon interface by measuring the increases in drain leakage current with increasing ionizing radiation dose. Characterization data have been obtained for lots 504, 505 and 507. At this time, the processing of lot 506 has just been completed and electrical characterization started. Therefore, this lot will not be discussed extensively here.

The dice selected for radiation testing were taken from a row located near the center of the wafer and parallel to the orientation flat. Three fully functional dice were selected from the left, center and right-hand side of the wafer on the basis of the wafer mapping.

The threshold voltage shift data were obtained from the shifts in conductance versus gate voltage curves. The conductance measurements were made with the source at +0.1 volts, the drain connected to the input of an operational amplifier, and the gate swept with a positive or negative ramp.

Each complementary pair in the 4007H circuit was connected as an inverter and together with the remaining inverter, biased in one of four conditions. One inverter had its gate biased at -10 volts with the sources and drains tied to ground. Another had

*Each sample was comprised of a group of circuits taken intact from the wafer. The Union Carbide sample contained 44 circuits and the Crystal Systems sample contained 35 circuits.

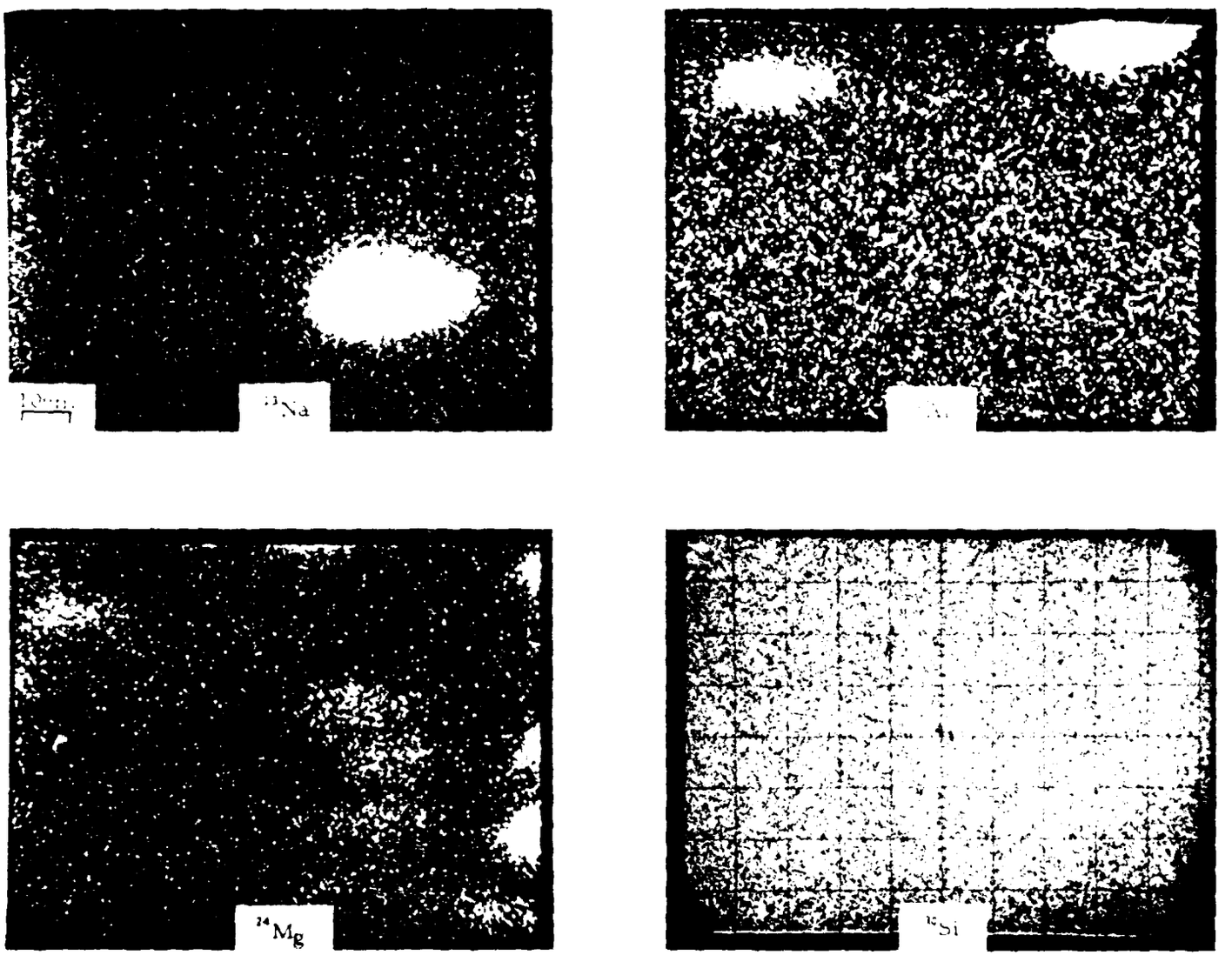


Figure 19. IMMA Surface Map of 1 mm^2 Test Pad on Union Carbide Sapphire with Union Carbide Epitaxial Silicon

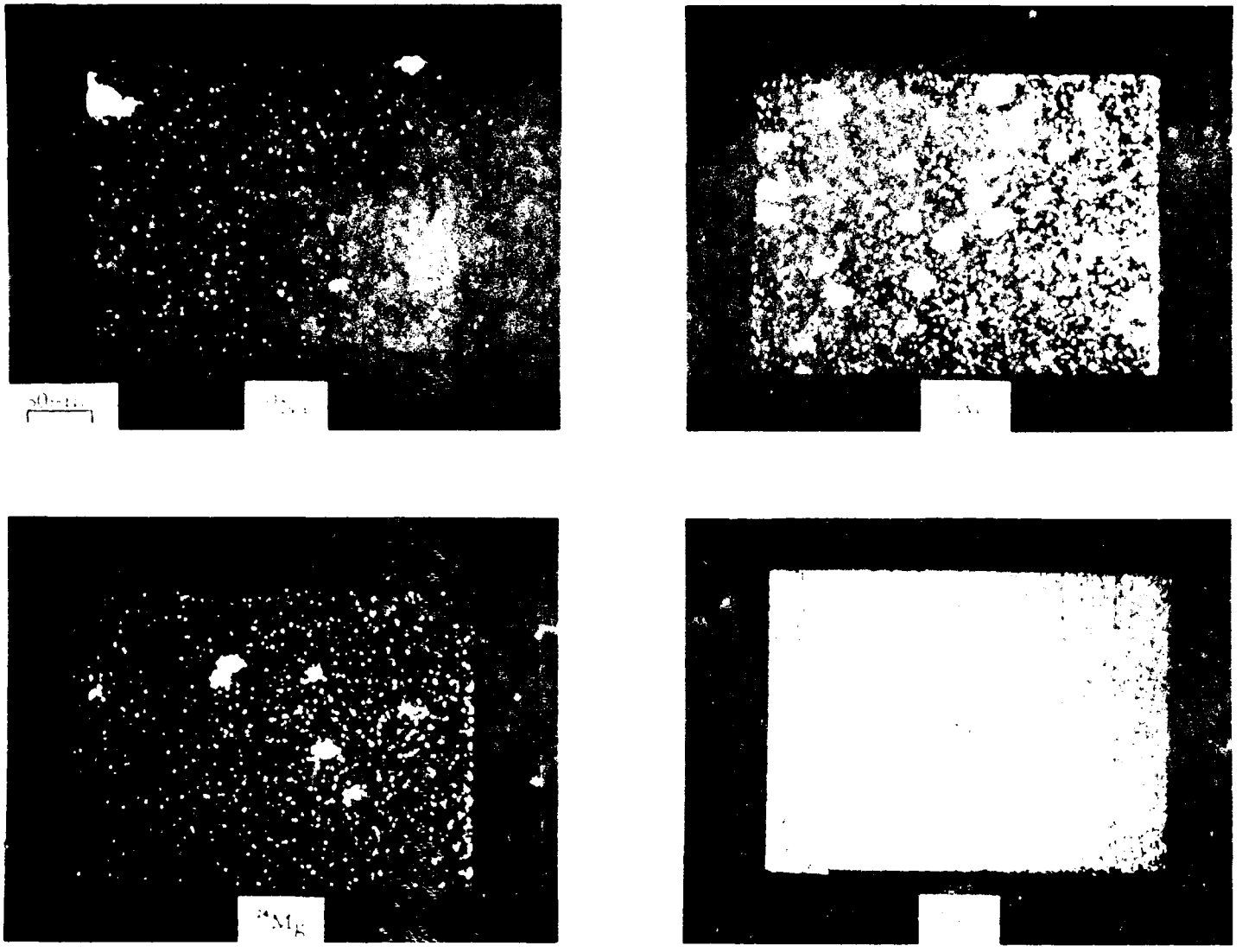


Figure 20. IMMA Surface of 1 mm^2 Test Pad on Crystal Systems Sapphire Polished by Insaco With Union Carbide Epitaxial Silicon

the drain of the p-channel at -10 volts with the gate and source at ground. A third inverter had the gate at +10 volts and all other terminals grounded. The fourth inverter had the n-channel drain set at +10 volts with all the terminals grounded. These four bias conditions are shown in Figure 21.

Measurements were made of the conductance using the output of the operational amplifier tied to the drain of the device being tested to drive the vertical Y axis of an X-Y recorder, while the ramp used to sweep the gate was connected to the horizontal X axis.

The drain junction leakage measurement was made by grounding the gate and source and measuring the current in the drain with +10 volts for the n-channel devices and -10 volts on the drain for the p-channel devices. These two test conditions are shown in Figure 22.

The two measurements--conductance and drain junction leakage--were made prior to the first irradiation and after a series of radiation doses (.01, .1 and 1.0 megarads). Figures 23 through 26 show the radiation-induced shifts for each of the four bias conditions described above after exposure to a total ionizing dose of one megarad. Differences in radiation response of the devices fabricated on the various substrate combinations are observed. The Hewlett Packard material showed the best overall radiation response from the standpoint of gate oxide hardness. The results are very nearly the same for each bias condition for the various material groupings. This was not quite the case for the Union Carbide silicon films, which showed some variation from material group to material group.

The radiation-induced drain leakage results for lots 504, 505 and 507 are shown in Figure 27. The results from lot 504 with the Union Carbide films was excellent for the Tyco, Crystal Systems, and Union Carbide (lab stock). The excellent results observed for lot 504 were confirmed by leakage data from lot 503, although these data are not shown here. The U.C. films tended to be the cleanest silicon depositions. The Rockwell films in lot 505 showed the worst response and by far had the worst silicon cleanliness. The Hewlett Packard results were intermediate--they ranged from good to poor.

Results observed here tend to show the same trends as those observed for other internally-funded material research projects. It was found that the more contaminated the silicon films, the worse the radiation-induced backchannel leakages. The cleanliness of this silicon film does not seem to affect the radiation hardness of the gate oxide, however.

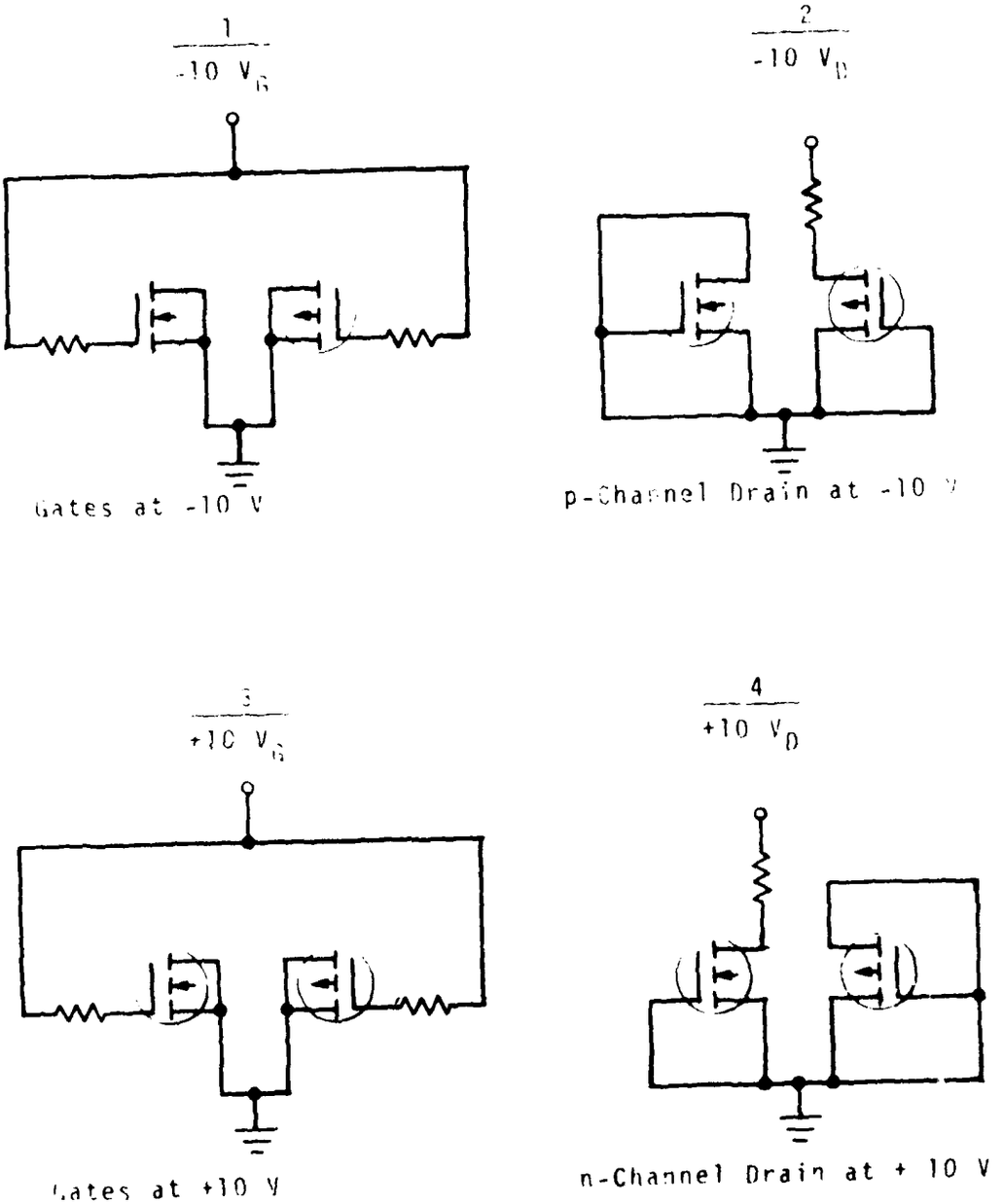


Figure 21. Bias Conditions Used During Co^{60} Irradiation

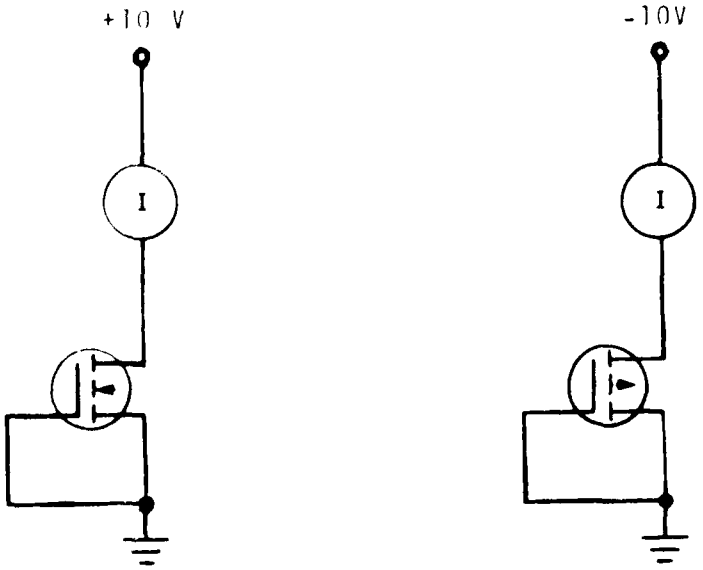


Figure 22. Drain Leakage Measurement

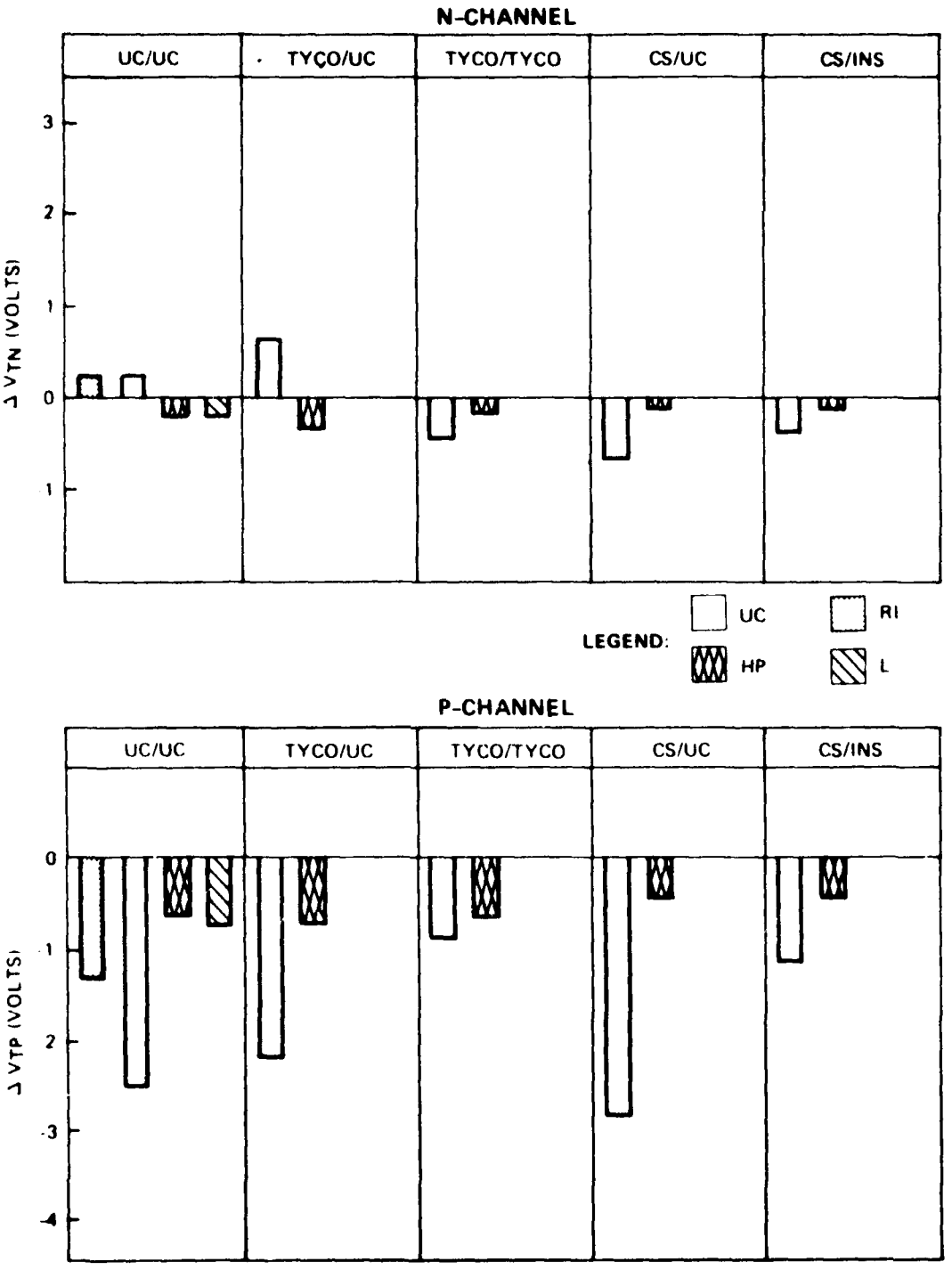


Figure 23. Radiation-Induced Threshold Voltage Shift Data After 10^6 rads(Si) and V_G = -10 Volts

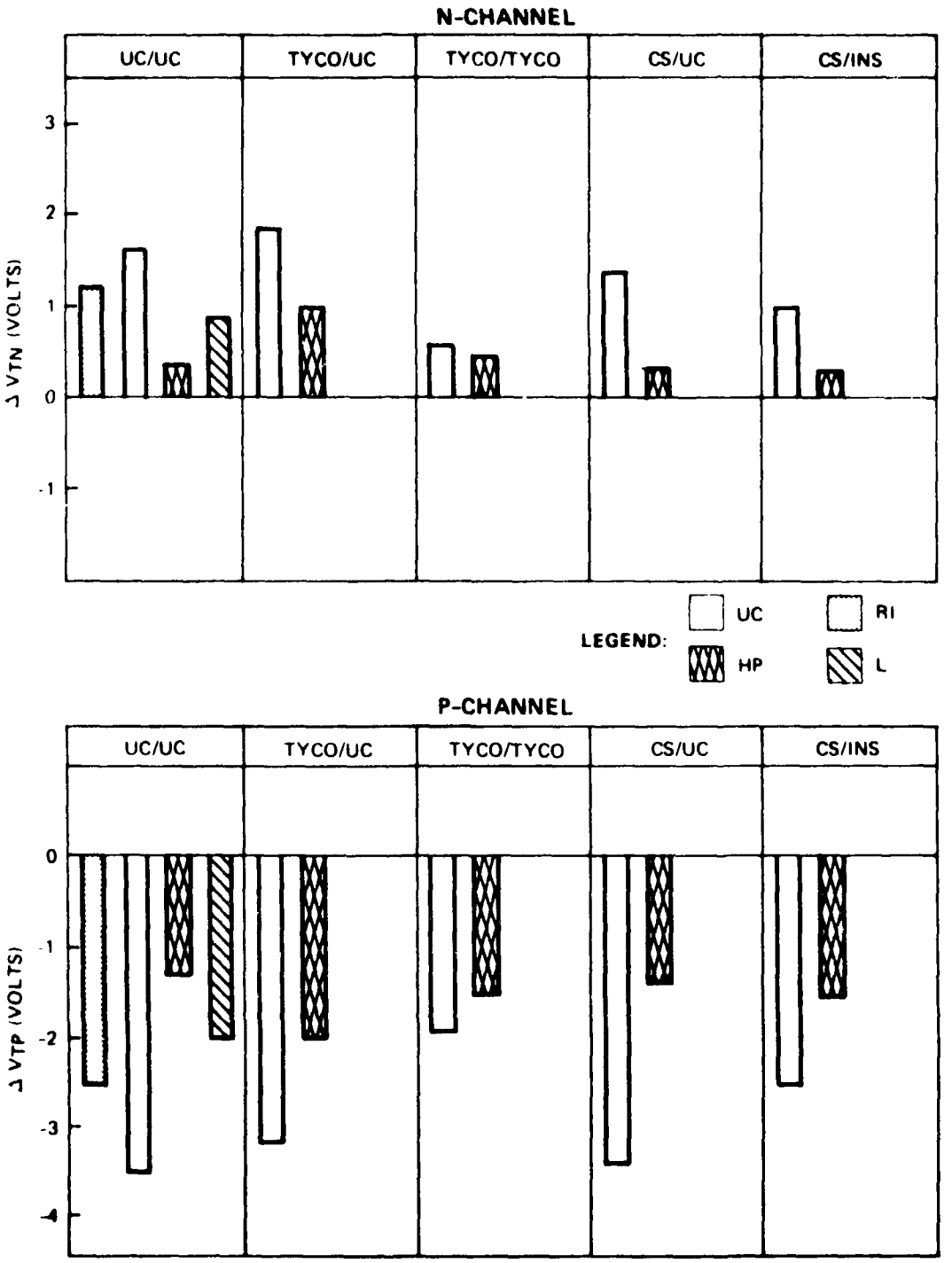


Figure 24. Radiation-Induced Threshold Voltage Shift Data After 10^6 rads(Si) and V_{DP} = -10 Volts, V_{GN} = 0 Volts

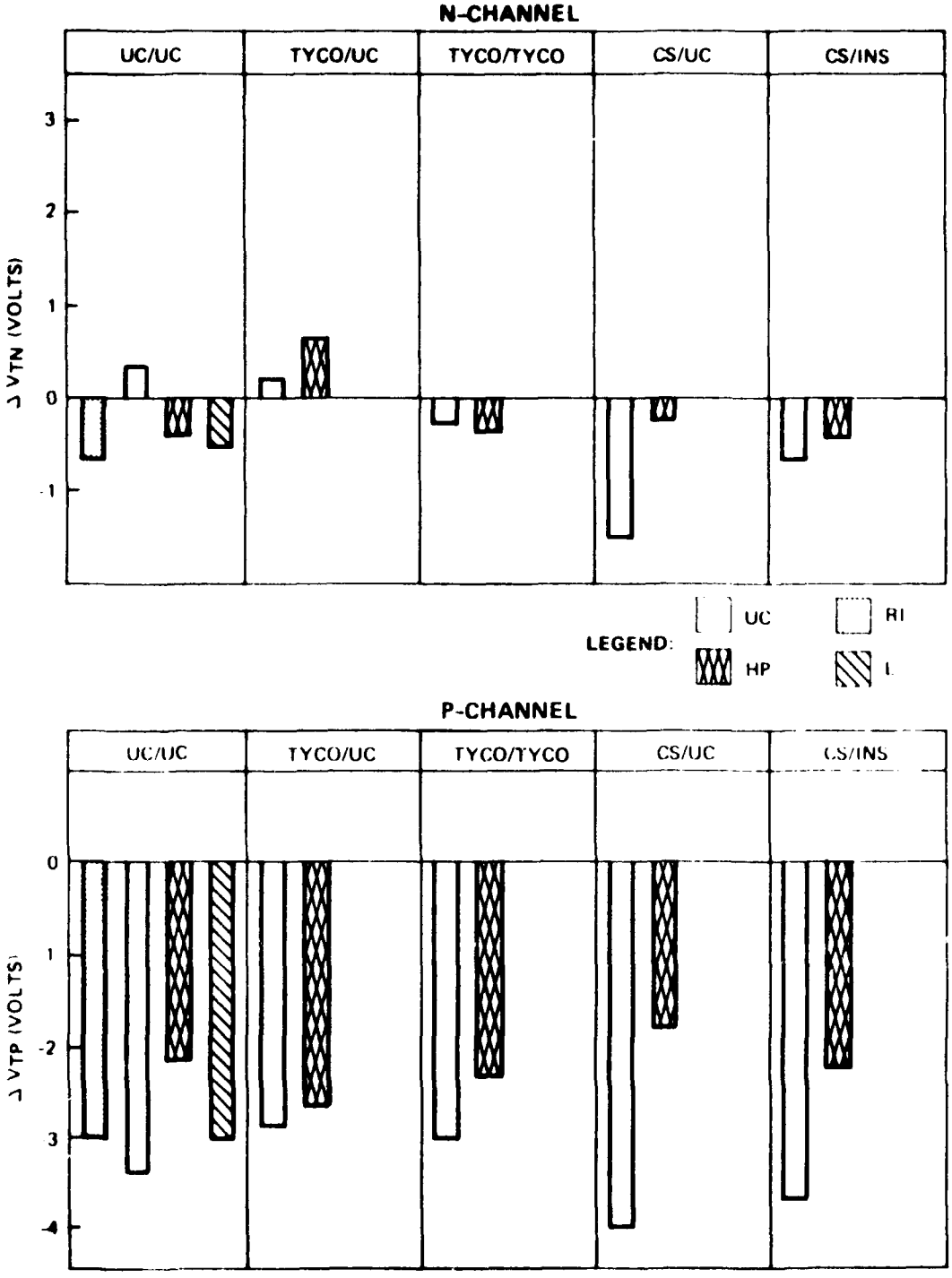


Figure 25. Radiation-Induced Threshold Voltage Shift Data After 10^6 rads(Si) and V_G = +10 Volts

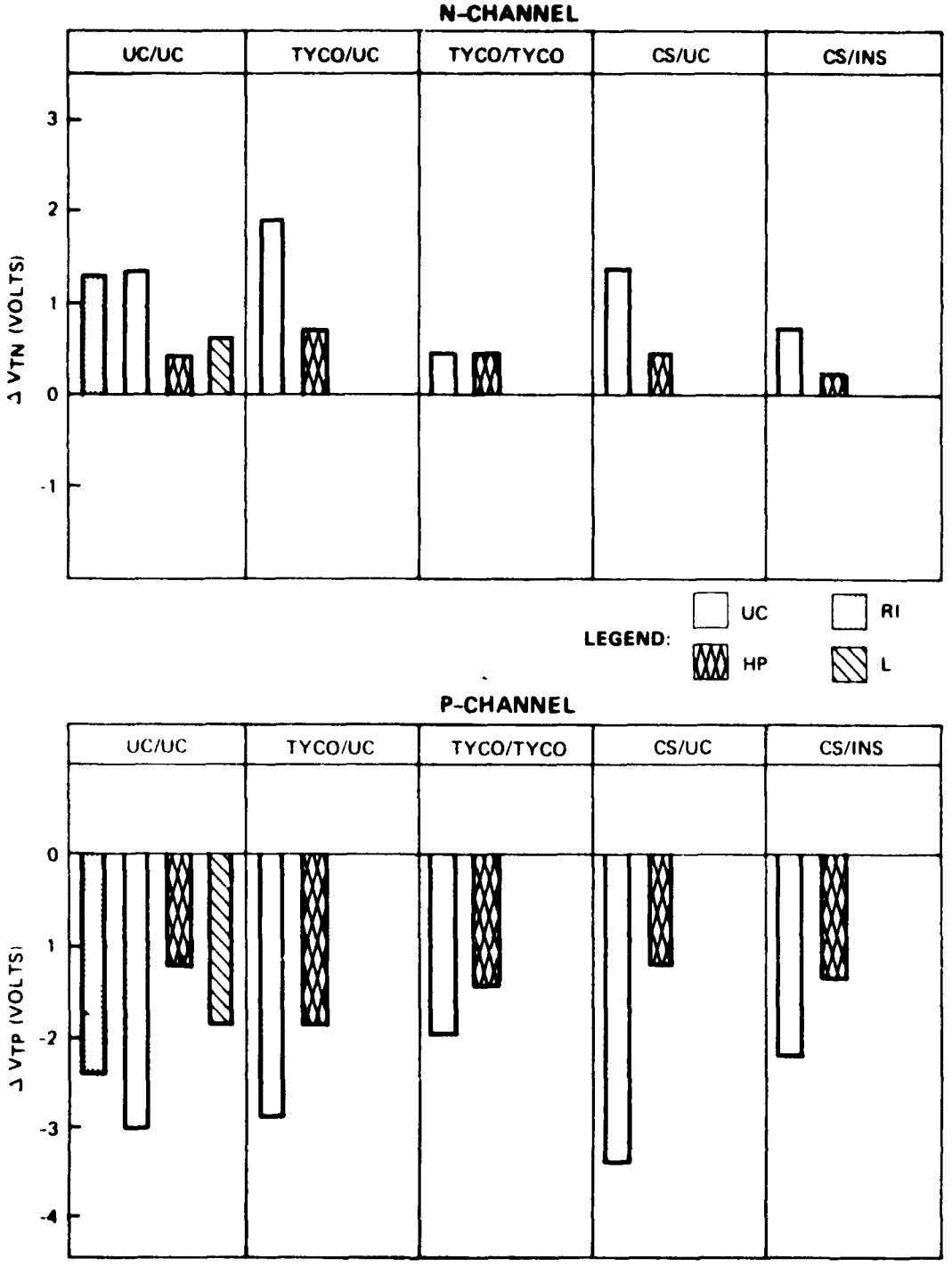


Figure 26. Radiation-Induced Threshold Voltage Shift Data After 10^6 rads(Si) and V_{DN} = +10 Volts, V_{GP} = 0 Volts

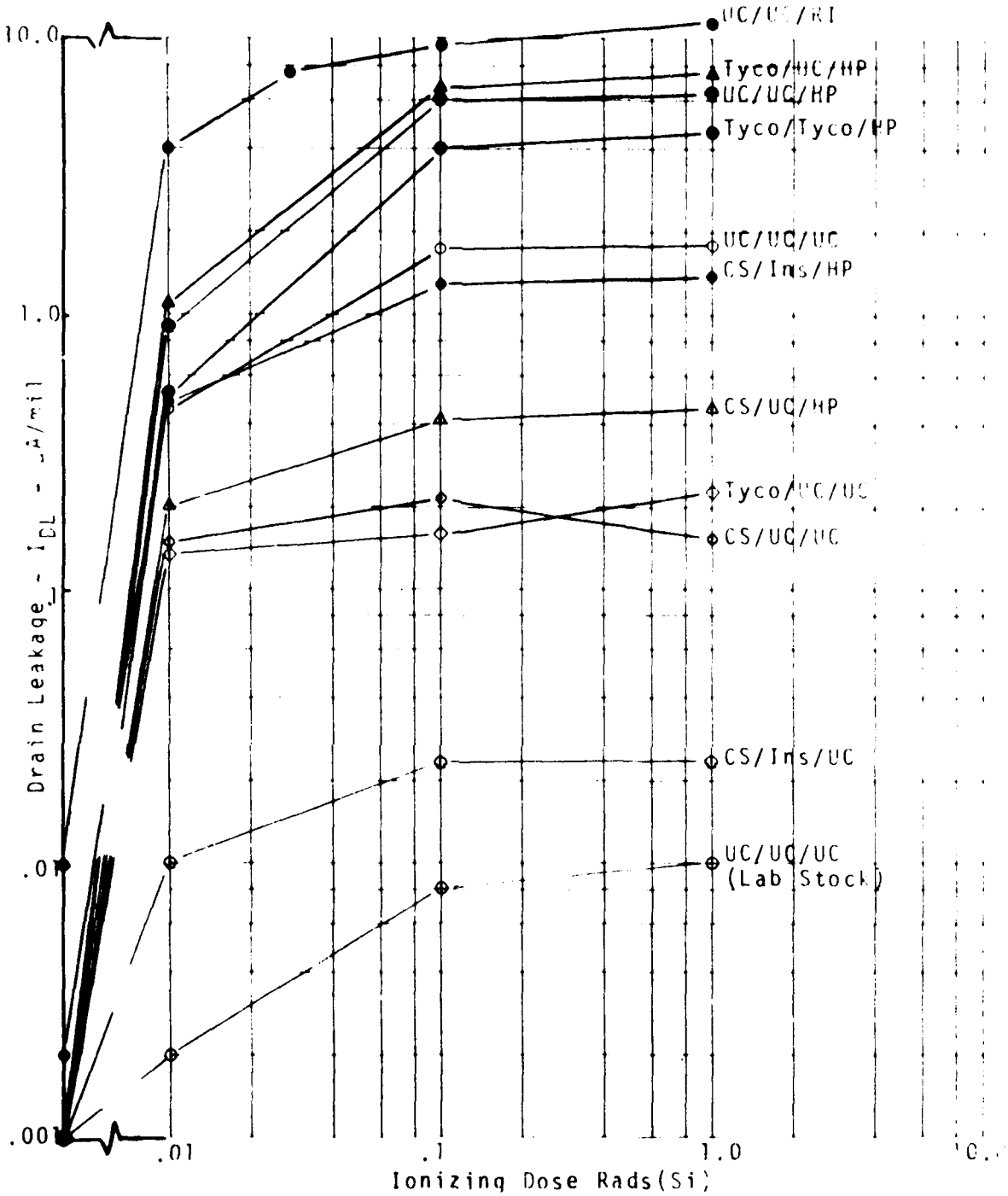


Figure 27. Radiation induced drain leakage current, I_{DL}, for the condition V_{DD} = +10V, V_G = V_S = 0 V on n-channel devices fabricated on Union Carbide (UC), Rockwell International (RI), and Hewlett Packard (HP) silicon epitaxies. Each point is the average of three samples across each wafer.

SECTION V

SUMMARY AND CONCLUSIONS

The work to date has included the characterization of sapphire substrates from three vendors--Union Carbide, Tyco and Crystal Systems--using selective etch, X-ray diffraction topography and Ion Microprobe Mass Analysis (IMMA). The results from these analyses show a wide variation in sapphire quality and surface smoothness. Of the samples evaluated, the Union Carbide sapphire shows the least defects in the sapphire and the Union Carbide polish yields the fewest scratches. The IMMA results for all samples show contaminates concentrated within several hundred angstroms of the sapphire surface. Scanning-Electron-Microscope (SEM) photomicrographs show that impurities are often present in the deposited silicon films. The major source of these impurity inclusions appears to be debris left in scratches after polishing. Generally, the debris consist of micron-size sapphire chips and remnants of polishing compounds--with some residue possibly left after the final rinsing step.

Silicon films from two different sources [Union Carbide (UC) and Hewlett Packard (HP)] were deposited on sapphire substrates from the three vendors indicated above. Each sapphire vendor type had two polishing variations--the vendor-furnished polish and a Union Carbide polish. Also, some relatively low quality silicon films were deposited by Rockwell on one group of Union Carbide sapphire wafers.

All of the silicon films were found to possess discrete inclusions of impurities, in varying degrees. These inclusions appear vividly in surface maps generated using the IMMA technique. This particular technique has proven valuable in determining the quality of the deposited silicon film, since many of the impurities, which are observed with the IMMA, either are transparent or are too small to be observed optically. The corresponding impurity sites, however, do appear in SEM photomicrographs and can be correlated with the IMMA surface maps.

To evaluate the effects of impurities and crystal imperfections in silicon and sapphire upon the finished device characteristics, 4007 type circuits were fabricated on the SOS material using a simple, radiation-hard process procedure. Two wafers from each sapphire and polishing group were included in each device processing lot, to improve the probability of obtaining at least one processed wafer for each material variation. For the most part, this approach was successful. The electrical test data indicated that good electrical characteristics were consistently obtainable for most groupings of SOS material--almost independent of sapphire substrate quality. However, the Tyco group of wafers seemed, in general, to yield below-average results, either because of the material or the processing. Tyco material

polished by Tyco and having Union Carbide silicon films (Tyco/Tyco/UC) showed very poor results. This particular group showed problems on every wafer (lots 506 and 507) indicating that the silicon on these substrates may have been of poor quality. Only one wafer in the Tyco/UC/UC group was found to be good (lot 503). The Tyco/UC/HP group and the Tyco/Tyco/HP group, however, yielded satisfactory devices.

The wafer maps for leakage currents showed that all groups of material were capable of producing good CMOS/SOS circuits. The yields found on some Crystal Systems wafers, with Insaco polish showed that very high yields could be achieved on material which had earlier shown a high defect density with highly scratched surfaces; however, it appears that devices lying along, or adjacent to, deep saw cuts tended to fail more readily than those between the saw marks.

The wafer mapping also showed that the defects were randomly distributed which tends to rule out most processing-related problems and is probably a reflection of either material problems (such as defects in silicon films serving as enhanced diffusion conduits between source-drain regions) or mask defects. To eliminate the latter variable, devices were selected which showed neither apparent processing nor mask defect problems, as evidenced by electrical probe data and optical examination. The IMMA results on these carefully chosen dice, which generally included only one failed device among several good devices, showed no impurity inclusions. These results were very surprising. However, contamination, as found in the pre-processing surface maps, was present in the 1 mm square silicon test area on the same sample. This result was true in nearly every wafer examined, implying that impurity inclusions were removed in the device areas which went through all the processing steps. The large silicon test areas were covered with a thick silox layer during the entire processing cycle, except during two short oxidation steps.

Radiation results showed that there is no particular correlation between backchannel hardness and the gate threshold hardness. This conclusion appears to be true when comparing the Union Carbide and the Hewlett Packard silicon films. Devices fabricated with the Union Carbide deposition showed the best backchannel results, while the Hewlett Packard films showed the best oxide hardness with good to poor backchannel hardness.

In conclusion, this program has further verified previous observations that the silicon epitaxial films containing the highest concentrations of impurities generally produce devices with higher initial drain-leakages and higher post-irradiation leakage currents. Several films, grown by various organizations on various sapphire wafers, were evaluated. Although wide variations were observed, even for a given wafer and film, the following qualitative statements can be made. The experimental Rockwell film (lot 505) showed the highest contamination level,

and the devices fabricated in that film generally exhibited the greatest backchannel leakages. The Union Carbide film (lot 504) was the "cleanest," and the corresponding devices generally exhibited the least backchannel leakages. All other films and corresponding devices tended to be intermediate in contamination levels and leakages, respectively.

The results of the program also tend to discourage the use of sapphire selective etch and X-ray topographs to determine the quality of the eventual silicon film. It appears more likely that the eventual quality of the silicon films depends more on the cleanliness of the sapphire surface, as far as particulate impurities are concerned, than on the substrate defect count--except possibly for gross defects, such as gross misorientation in the sapphire, deep grooves, etc. The cleanliness of the sapphire film, as shown with the IMMA surface map technique, appears to be a reflection of pre-epitaxial cleaning procedures.

CONTRIBUTING PERSONNEL

In accordance with Paragraph III of the Outline of Reporting Procedures for Contractors, the Rockwell scientists and engineers who contributed to the research reported on herein are listed below.

J. L. Peel	Principal Investigator
M. D. Barry	Associate Principal Investigator
L. A. Moudy	X-ray Analysis
H. L. Glass	X-ray Analysis
M. F. Ehman	Chemical Etch Analysis
L. G. Green	Automated Device Testing
F. F. Mittelbach	Automated Device Testing
T. J. Oki	Computer Programming Support
R. S. Halverson	Radiation Testing

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