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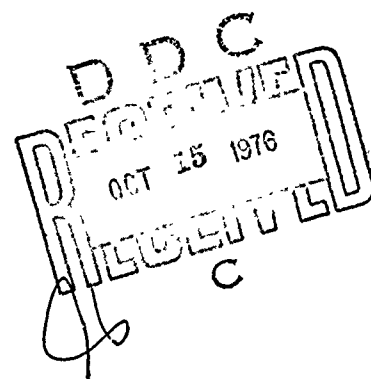


ASSESSMENT OF SOLID STATE REPLACEMENT OF TWT AMPLIFIERS
FOR SATELLITE COMMUNICATIONS

Cornell University

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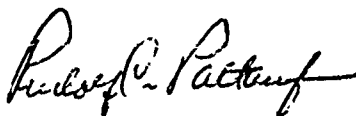
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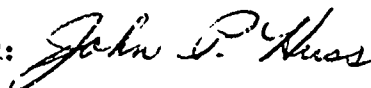
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) This report summarizes the present state-of-the-art achievements of GaAs FET transistors, assesses their probable capabilities and the associated technology problems. Designs of FET high power amplifiers are included and it is noted that measured intermodulation distortion in these amplifiers is higher than anticipated. Finally it is shown that efficient high power GaAs Read diodes of the hard punch-on variety can satisfy the TWTA distortion specifications.		

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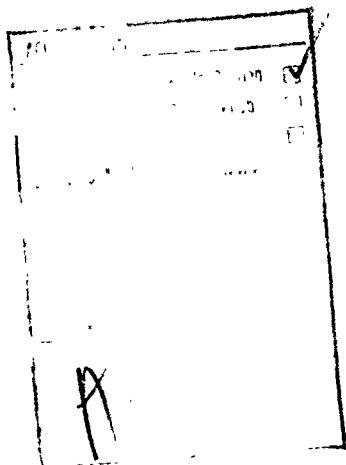
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→ Thus an FET/Read diode hybrid amplifier is proposed that should meet all specifications except that of overall efficiency which would probably be reduced to 20-25%.
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SECTION A

SOLID STATE TWTA REPLACEMENT: THE ROLE OF THE FET

Jeffrey Frey

The basic performance level that must be met by the desired TWT replacement is, at 7.5 GHz: 10W output power at 29% efficiency with 55dB small signal gain. In an attempt to delineate the role of the FET in achieving such a spec, this section will consist of two parts: I, in which the FET's latest and best results, in TWT-type (linear) applications, will be summarized; and II, in which limits on FET performance will be investigated. Part I will therefore indicate how much of the desired spec can be met today--or how much of a complete solid-state TWT system can be based on FETs--and Part II will indicate whether the spec can ever be met by FETs, and what work will be required to reach FET performance levels.

I. Performance of FETs and FET Subsystems as of January 1976A. Performance of single laboratory devices

An interesting preliminary question is, "how close can a single FET come close to meeting the spec today?" The answer is contained in Table I which includes the latest available data for single FET linear performance. In that

Laboratory	Output Pwr	Lin. Gain	Power-Added Efficiency	Source Periphery	Freq.	M _f	Projected Output Power (7.5 GHz)
TI	1.86W	4dB	39%	2400μ	8 GHz	49.6	2.12W
RCA	.52	7.6	13.6	1600	11	39.6	1.1
RCA	.20	7.5	13.0	785	12	36.7	0.5
RCA	1.0	5.5	16.3	3000	9	26.3	1.5
Fujitsu	2.2	4	21.6	5200	8	27.1	2.5
TI	.32	4	16	1200	9	21.3	.45

TABLE I. Individual FET Performance
Class A Operation
January 1976

table a figure of merit M_f has been calculated, as

$$M_f = P_A f^2 / W$$

P_A = power-added, mW

f = frequency, GHz

W = source periphery, microns.

On the basis of this figure of merit, the projected power output at 7.5 GHz has been listed.

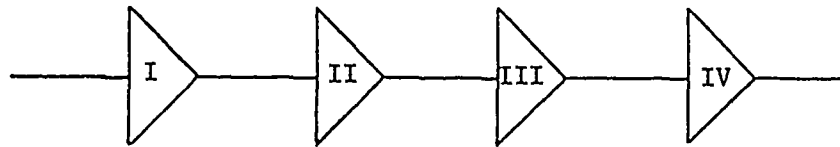
Table I shows that the maximum power output at 7.5 GHz that should be achievable with a single FET now in existence (the Fujitsu device) should be of the order of 2.5W. This power level should be achievable at a linear gain of around five dB or less with a power-added efficiency of the order of 20-30%. It should be noted that the intermodulation distortion products of all of the devices of Table I are within the distortion limits required by the spec.

Thus, it is certain that a single FET cannot meet the spec today; furthermore, since the gain at high power outputs of FETs is so low, it may never be possible for a single device to meet the spec.

B. Performance of FET subsystems

Since it seems unreasonable to expect a single FET to meet the entire spec today, the TWT replacement "system" can be considered as a cascade of subsystems and the performance of the FET in each subsystem investigated. With

some foresight, the amplifying system can be broken down, for example, into a cascade of four stages, as shown below:



Gain	32dB	10dB	8dB	5dB	55dB
Pwr Level	31.6 μ W	50mW	500mW	3.16W	10W
Pwr-Added					
Efficiency	15%	20%	30%	30%	
DC Input Pwr	330mW	2.25W	8.9W	22.8W	= 34.28W
O/all efficiency					29.2%

The question to be answered is then "how much of the postulated system can be realized now using FETs?" The answer is implicit in Table II, which gives best results as of January 1976 for FET subsystems. It can be seen that FET subsystems are now achieving performance levels close enough to those required for parts of the postulated system to indicate that, were effort specifically placed on achieving the performance goals set out for stages I and II in that system, they probably could be achieved today. For example, RCA has produced a 5-transistor 2-stage circuit that already approximates the performance of stages I and II of the postulated system, as follows:

	RCA	RCA	HP	RCA-Canada	Spec
Frequency	7.25-7.75 GHz	4.4-5.0	11.7-12.2	10.95-11.7	7.25-7.75
Sat. Output Pwr	1.02W	1.0	10mW	20mW	10W
Linear Gain	6.7dB	34	18	18	55
Variation of Output Pwr	.3dB	.4	NA	.4	.5
Variation of Lin. Gain	.7dB	.4	.5	NA	.7
Input VSWR	1.4:1	NA	1.6	Circulator	1.25:1
Output VSWR	1.2:1	NA	1.02:1	Circulator	2:1
imr ₃ at Sat.	-22dB	NA	NA	-29	-9.5
Efficiency at Sat.	33%	16%	NA		29%
Comments	2 FETs in Hybrid ckt	3 FET preamp and 2 FET output stage	3 FETs	6 FETs	

TABLE II. FET Subsystem Performance
January 1976

	RCA	Postulated I and II
f	4.4-5 GHz	7.25 - 7.75 GHz
Bandwidth	12.8%	6.7%
Power Out	1W	500 mW
Linear Gain	34dB	42dB
Efficiency	16%	19%

It seems clear that, with tradeoffs possible between gain and power output, the technology to produce at least stages I and II (postulated), using FETs, is at hand.

C. Conclusions: Specs that can be met today using FETs

The entire solid state TWTA replacement will probably require more than one active solid-state device. Current FET technology does not seem capable of providing an all-F. TWTA replacement. However, the preamp and driver stages of a multi-stage TWTA replacement can probably be made, well within spec, using today's FET device and circuit technology. The only current solid state technology appropriate for the output stages, which are required to produce 10W output power with 13dB gain and 30% efficiency, may well be the Read IMPATT diode.

II. Limits on FET Output Stage Performance

In predicting large-signal limits of FET operation--in

particular, limits of gain and power output--it is important to use a device model neither too general to give concrete answers, nor too detailed to allow of reasonably simple calculations. Thus we shall not here use the basic one-dimensional approach of E.O. Johnson, who calculated limits of the product $P_m X_c f_T$ based only on saturation velocities and breakdown voltages. Rather, we shall, following R. Dean of RCA, develop a simple two-dimensional model that allows determination of the effects of gate length, drain-gate spacing, source-drain spacing, and maximum voltage, on output power and gain. This model also yields values for maximum expected power output and gain; since much current development in power FETs is involved with increasing V_{max} , (maximum drain voltage) we have here calculated output power and gain as a function of V_{max} , with gate length ℓ_g and drain-gate spacing ℓ_D as parameters.

A. Large-signal FET model

This model allows the development of expressions for input current, based on the rate of change of the charge on the gate; for time-varying channel series resistance, based on a conception of the channel as an open-circuited transmission line; and for output power, based on linearized output characteristics.

When a gate voltage is applied such that the active channel thickness is uniform over the length of the channel, and is equal to X_0 , the charge on the gate is $Q_0 = ncZX_0 \ell_g$.

Thus the input rf current makes the gate charge vary as

$$Q_g = 1/2 Q_o (1 - \sin \omega t) \quad (1)$$

The input current is thus

$$I_m = \frac{dQ_g}{dt} = -\frac{\omega}{2} Q_o \cos \omega t \quad (2)$$

The varying channel resistance $R_c(t)$ is determined by considering the channel as an open-circuited transmission line of length L , and resistance r and capacitance c per unit length. The input impedance of such a line is

$$Z_{in} = Z_o (\tanh \sqrt{j\omega r c} L)^{-1} \quad (3)$$

with

$$Z_o = \sqrt{r/j\omega c} \quad (4)$$

A series expansion of the argument of the tanh function leads to the expression

$$Z_{in} = \frac{R}{3} + \frac{1}{j\omega C} \quad (5)$$

in which R = total channel resistance = rL and C = total channel capacitance = cL . The conclusion to be drawn from Eq. (5) is that the ac channel resistance, the real part of Z_{in} , is of the order of one-third total channel resistance R under the gate. From geometrical considerations and Ohm's law for the semiconductor,

$$R = \frac{1}{\sigma} \frac{\ell_g}{X_O Z} = \frac{\ell_g}{N_d e \mu X_O Z} = \frac{\ell_g^2}{Q(t) \mu}$$

Thus

$$R(t) = \text{Re}(Z_{in}) = \frac{2}{3} \left[\frac{\ell_g^2}{\mu Q_O} \right] (1 - \sin \omega t)^{-1} \quad (6)$$

The average input power is obtained by averaging the input $I^2 R$ product:

$$P_{in} = \frac{1}{T} \int_{-T/2}^{T/2} I_{in}^2 R(t) dt = \frac{1}{6} \frac{\omega^2}{\mu} \ell_g^2 Q_O \quad (7)$$

The maximum output power can be calculated in terms of the maximum permissible drain voltage, and the output current, if output conductance is taken as negligible. The maximum possible rf output voltage swing is

$$V_{OUT} = 1/2 V_{max} \cos \omega t \quad (8)$$

An approximate relationship between output and input rf currents is generally taken to be $I_{OUT} = \frac{v}{\ell_g \omega} I_{in}$. Taking v as the maximum velocity reachable by the carriers between gate and drain, we have from (2),

$$I_{OUT} = -1/2 Q_O \frac{v_m}{\ell_g} \cos \omega t \quad (9)$$

Thus,

$$P_{out} = \frac{1}{T} \int_{-T/2}^{T/2} I_{OUT} V_{OUT} dt = \frac{1}{8} \frac{Q_O v_m V_{max}}{\ell_g} \quad (10)$$

Two additional performance-degrading elements are important: a finite output conductance G_o across the load; and the spreading resistance from the source end of the channel. The former effect can be incorporated in a multiplying factor F_G ,

$$F_G = 1 - \frac{G_o \ell_g V_{\max}}{Q_o v_m} .$$

This factor reduces output power, the total expression for which should be:

$$P_{OUT} = \frac{1}{8} \frac{v_m V_{\max} Q_o F_G}{\ell_g} \quad (11)$$

The spreading resistance can be included by multiplying the input power by a multiplying factor S_R ,

$$S_R = 1 + \frac{\ell_s}{\ell_g} .$$

Thus, the total expression for input power should be

$$P_{in} = \frac{\omega^2}{6\mu} \ell_g^2 Q_o S_R \quad (12)$$

Eq. (11) gives output power; power gain is given by

$$\frac{P_{OUT}}{P_{in}} = \frac{3}{4} \frac{\mu v_m}{\omega^2 \ell_g^3} V_{\max} \frac{F_G}{S_R} \quad (13)$$

The output conductance G_o is needed in Eq. (11). A measure of this quantity can be obtained by writing an

expression for G_o by analogy to that usually taken for g_m :

$$g_m = \omega_T C_g \quad (14)$$

$$G_o \sim \omega_T C_{dg} \quad (15)$$

C_{dg} can be obtained from the geometry of the device and simple parallel-plate capacitance considerations. ω_T can be obtained from Eq. (14). The result is:

$$G_o = \frac{eNv_m X_o (t - X_o) Z}{2\ell_g V_p} (\ell_g + X_o) \left[\frac{\omega}{v_m} + \frac{1}{\ell_D + \ell_g} \right] \quad (16)$$

B. Gain and Power Calculations

The above equations have been used to calculate output power and gain values, and dependence on maximum permissible drain voltage. The plots (Figs. 1 and 2) have been done for a "typical" power FET:

$$N_D = 5 \times 10^{16} / \text{cm}^3$$

$$\mu = 5000 \text{ cm}^2 / \text{V/sec}$$

$$t = 2500 \text{ \AA}$$

$$V_p = 2.5 \text{ V}$$

$$Z = 2000 \mu = 2 \text{ mm}$$

$$\ell_S = 1 \mu \quad \ell_D = 2 \mu, \quad .5 \mu < \ell_g < 2 \mu$$

$$X_o = t/2 = 1250 \text{ \AA}$$

$$v_m = 10^7 \text{ cm/sec.}$$

The range of maximum voltages is taken from 10V (easily

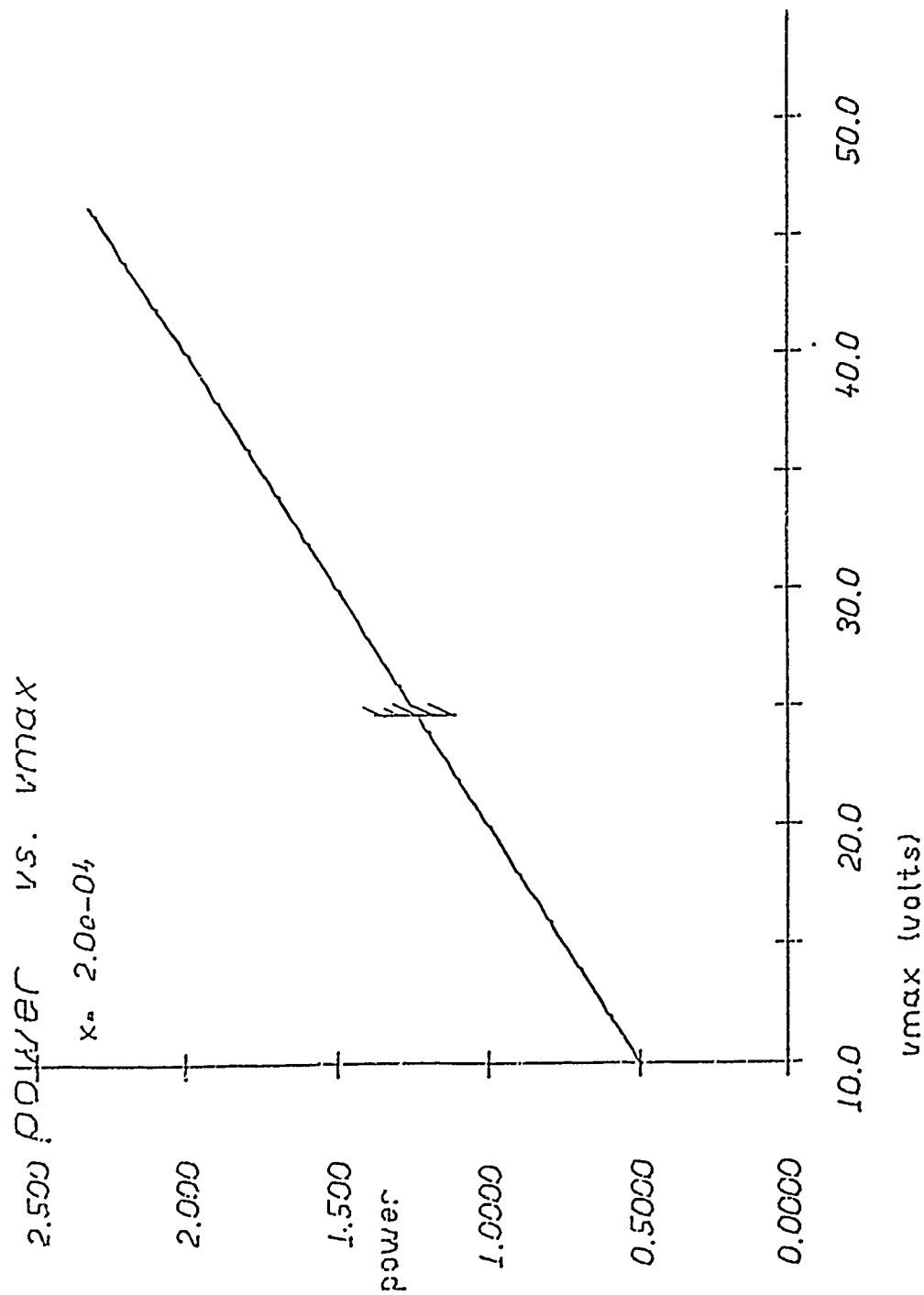


Figure 1. Output P_{out} as a function of maximum drain-gate voltage for a sample FET: $N_D = 5 \times 10^{16} / \text{cm}^3$, $t = 2500 \text{ \AA}$, $V_p = 2.5 \text{ V}$, $Z = 2 \text{ mm}$, ℓ_g between .5 and 2μ . The vertical line indicates breakdown voltage for this doping.

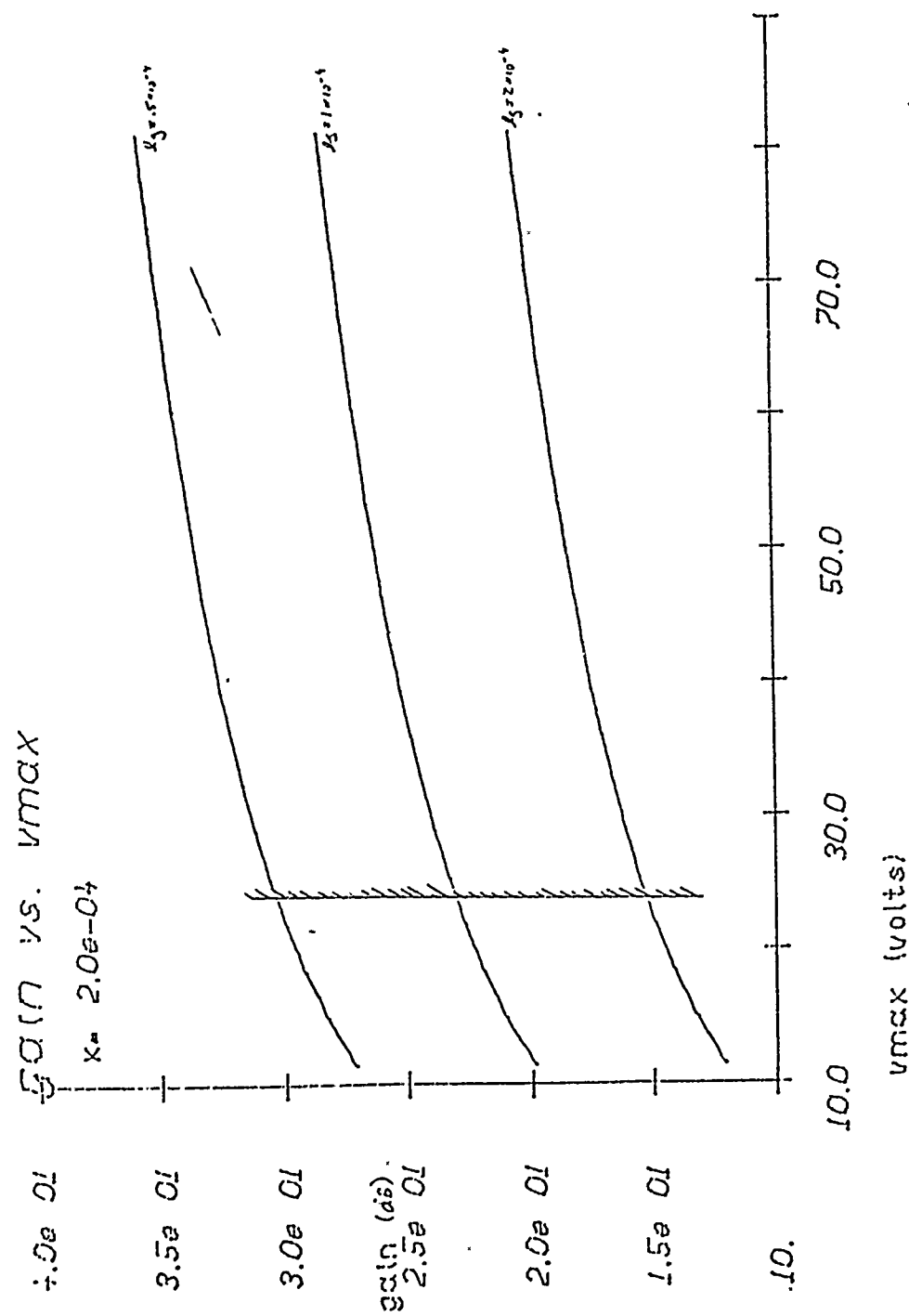


Figure 2. Power gain as a function of V_{max} for the device of Figure 1.

achievable today) to 50V (within the realm of possibility but not yet reached). Parameters are channel length ℓ_g and gate-drain spacing ℓ_D , which affects both output conductance and maximum voltage, as long as breakdown occurs between gate and drain, and not primarily through epilayer interface or drain edge effects.

For the parameters of the calculation, output power is seen to be virtually a linear function of $V_{\max}$, independent of ℓ_g and ℓ_D ; and power gain is essentially independent of ℓ_D . For this doping, the Schottky barrier breakdown voltage is 24V, so the curves should be considered stopped at that point. The maximum power gains available are 30dB (.5 μ gate); 23dB (1 μ gate); 15dB (2 μ gate). The maximum power output is 1.4W.

The lack of dependence of these results on ℓ_D , i.e., output conductance, indicates that the multiplying factors F_G and S_R can be taken as unity for calculating performance limits. Further, curve-fit expressions can be found to represent the dependence of $V_{\max}$ and μ on doping. Expressions that fit experimental results fairly well are:

$$V_{\max} = V_B = 100(1 + 1.8 \times 10^{-16} N_D)^{-.65} \quad (17)$$

and

$$\mu \approx \frac{10000}{1 + \left(\frac{N_D}{5 \times 10^{16}} \right)^{1/4}} \quad (18)$$

Inserting (17) and (18) into (11) and (13), taking $F_G = S_R \cong 1$, one obtains:

$$P_{OUT} = 2 \times 10^{-12} (1 + 1.8 \times 10^{-16} N_D)^{-.65} N_D \text{ per mm gate width} \\ \text{per micron epi thickness} \quad (19)$$

$$GAIN = \frac{3.4 \times 10^{-9}}{l_g^3} \left[\frac{(1 + 1.8 \times 10^{-16} N_D)^{-.65}}{1 + (.2 \times 10^{-16} N_D)^{1/4}} \right] \quad (20)$$

These limiting-value equations are plotted in Figs. 3 and 4 respectively. From these curves, it is evident that, at least for the standard FET geometry of the model, a tradeoff exists between gain and power output. It is also apparent that experimental power results for this geometry are approaching these limits; it also appears that much remains to be done to achieve limiting power gain values at these power levels.

C. Conclusions: Future FET Developments

Figures 3 and 4 indicate that, with a reasonable (say, 2μ) gate length, FETs should eventually be capable of reaching up to 2.9 watts of output power per mm gate width per micron of channel thickness, with a power gain of up to 17dB. For a reasonable channel thickness of 0.4μ , and a gate width of 2.5mm, the total output power could be as much as 2.9W. The analysis presented here, however,

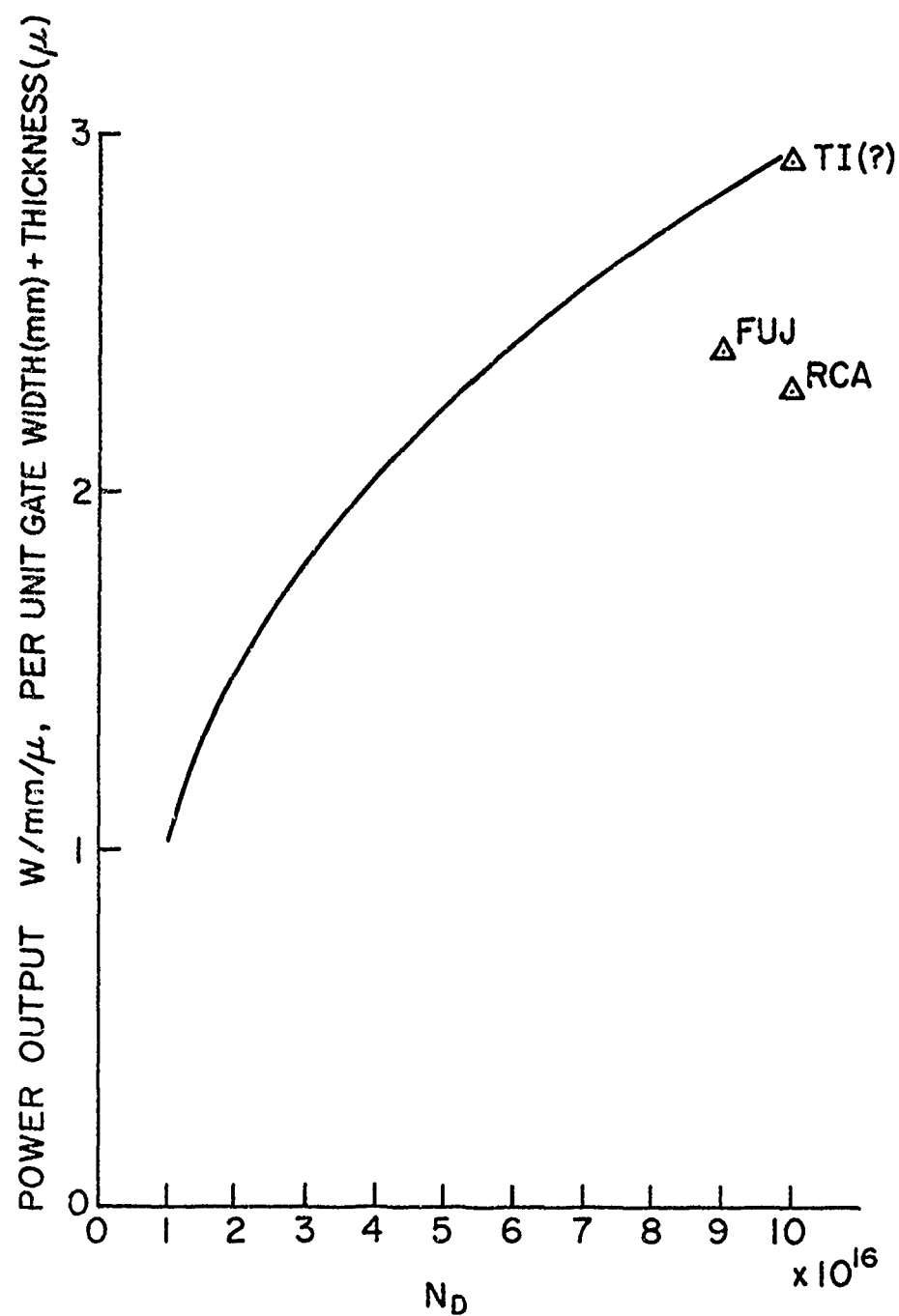


Figure 3. Normalized maximum output power vs. epi-layer doping for a standard-geometry FET. Experimental results are given but the thickness of the epi-layer of the TI device is not known.

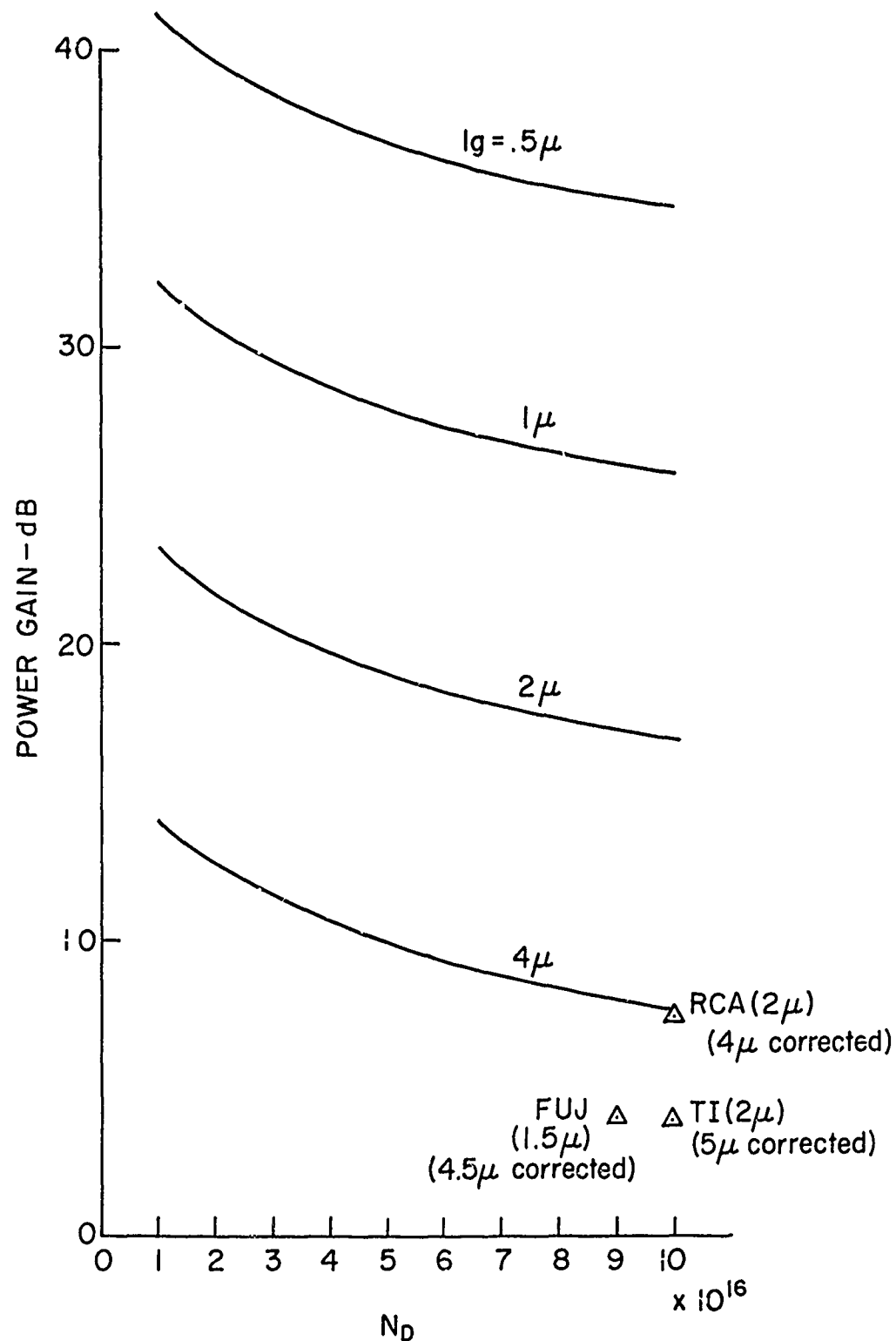


Figure 4. Power gain vs. epilayer doping for a standard geometry FET, as a function of gate length. Experimental points are given with metallurgical gate lengths, and total source-drain spacing in parentheses.

neglects many parasitic elements, and also neglects problems of thermal effects. If these factors reduce (very roughly) the output power and gain to half of the limiting values, powers of the order of 1.5W with gain in excess of ten dB should be achievable at 7.5 GHz. Thus, stage III of the postulated system looks feasible, and might even be combined with stage II; stage IV, the 10W output stage, does not appear to be a reasonable prospect using standard (uniform doping; uniform channel thickness) technology.

Areas of technology in which development can be pursued in order to make performance levels of the postulated stages II and III include: development of two-dimensional FET models to develop design guidelines to increase breakdown voltage; improvement of epilayer/substrate interfaces to increase breakdown voltages; use of ion implantation and/or selective epitaxy to reduce source and (especially) drain contact resistance, and increase breakdown voltage; development of self-aligned gate techniques to facilitate production of short gates with high yield; and development of improved heat sinking techniques.

SYMBOL TABLE

C_{dg}	= drain-gate capacitance
C_g	= gate-channel capacitance
e	= electronic charge
ℓ_D	= drain-gate spacing
ℓ_g	= gate length
ℓ_s	= source-gate spacing
N_D	= donor density in channel
t	= channel thickness (geometrical)
v_m	= maximum carrier velocity
V_p	= pinchoff voltage
Z	= channel width
μ	= electron mobility in channel
ω_T	= current-gain cutoff frequency

SECTION B

FET/READ-IMPATT HYBRID AMPLIFIER FOR TWTA REPLACEMENT

C. A. Lee and G. C. Dalman

I. Introduction and Summary

The replacement of traveling-wave tube amplifiers in communication transmitters by solid state amplifiers has been a subject of much development and debate within the last few years. A recent report of a panel session on this subject¹ indicates that IMPATT devices have been used successfully in systems of limited bandwidth and at low powers of the order of a few watts. In spite of a final output stage efficiency of about 20% the overall efficiency of an all IMPATT amplifier is only 6-7%.

We estimate that most of the shortcomings of IMPATT amplifiers can be overcome with an FET-Read IMPATT hybrid amplifier. Use of the transistor in the front end stages improves the overall noise figure considerably as well as the efficiency because the transistors are more efficient at lower power levels. The Read diode is used in the final output power stage for two important reasons. The first is that present GaAs Read devices can produce more than 10W from a single four mesa device at efficiencies greater than 30%. The second is that the Read structure can have a vanishingly small electronic susceptance which permits operating the device in a broadband circuit and, in addition, this small electronic susceptance significantly improves

¹ Microwave Journal, February 1975.

the linearity over that of the usual flat profile IMPATT. The device requirements are demanding, but we believe those requirements can be met by selected devices from those presently manufactured.

An important feature of this report is the inclusion of the theoretical development relating the distortion specifications to the device parameters. Much of one's use of the literature on intermodulation distortion is hampered by not understanding what specific device parameters are responsible for the nonlinear behavior. Once these parameters are identified, however, then the problems of device design can be attacked.

Our point of view, therefore, in proposing an FET/Read hybrid amplifier which we believe will meet specific requirements of a TWT amplifier is that device design and the maintenance of material properties in fabrication are crucial factors in achieving success. A particularly important feature of device design is the electronic susceptance. In the most common IMPATT design (flat profile, n-silicon) this electronic susceptance is typically 2.5-3 times the negative electronic conductance. Such a large value of the electronic quality factor, $Q_p \equiv B_e/G_e$, is the principal reason for the relatively low gain of the output stage (typically 5-6dB), the limited bandwidth, and the relatively high degree of intermodulation distortion. It is not generally appreciated that by proper design of the electric field distribution

in the avalanche and drift regions that the electronic quality factor, or the electronic susceptance, may be reduced to zero and even made negative. Thus by proper choice of diode design we have come to the conclusion that the TWT amplifier specifications can be met by an FET/Read hybrid design in all respects except that of the overall amplifier efficiency. We estimate that with present state-of-the-art devices the best amplifier efficiency would lie in the range of 20-25% instead of 30%.

Having briefly stated our conclusions a short description of the main sections of the report will serve as a useful guide to the developments supporting these conclusions. In the second section of the report the various specifications of the TWT amplifier are reviewed and discussed. From these specifications the two most important ones, intermodulation distortion and phase deviation with input power are dealt with in some detail in Section III. In this section a relatively simple analytical derivation is presented which relates the intermodulation products to variation of the electronic admittance with r.f. voltage. The advantage of this analysis is that one can clearly see and estimate the effects of the large electronic susceptance found in most present day devices. Following the simple analysis is a graphical analysis of an actual GaAs hard

punch-on Read structure utilizing a measured Rieke diagram taken at high power levels. Both of these methods, utilizing data on actual diodes, give values of intermodulation products which are safely within the specifications for the TWT amplifier.

The third part of section 3 gives a derivation of the relation between phase deviation as a function of input power and the variation of electronic susceptance with r.f. voltage. This variation of electronic susceptance is relatively easy to measure in a single tuned amplifier circuit. Our measurements on various IMPATTs indicates that $5^{\circ}/\text{dB}$ can be readily achieved even with flat profile IMPATTs.

In the last section (4) we review aspects of the problem needing further study. For example, one should proceed immediately with the testing of a C-band penultimate and final stage amplifier utilizing presently available selected devices. Measurements should be made of the gain, efficiency, intermodulation distortion (3^{d} order), and noise figure as a function of input power. A prime question is what efficiency can be achieved with present devices while meeting the specifications on linearity. Further, there is a suggested study of the Schottky barrier metallurgy that is important for reliability. There is also the problem of identifying the material parameters necessary for high efficiency operation. Maintenance of these material parameters in the fabrication of Read diodes is at present

a difficult and elusive problem. Specific problems in this area are uniformity of epitaxial layers, control of saturation current (deep levels), interface defects or traps, and the metallurg. of ohmic, non-injecting contacts. Finally there is a suggested review of the GaAs bipolar transistor. In past studies good injection efficiency was a limitation but heterojunction and improved ion-implantation technology can now provide a solution to that problem. The improvement in performance of the GaAs FET that is principally due to ballistic transport of the electrons in the channel region will yield a similar improvement in the bipolar device.

II. Review of Amplifier Specifications

In this section the specifications of the traveling wave tube amplifier are reviewed. Those specifications which the proposed hybrid FET/IMPATT amplifier can meet at the present time are identified. A discussion of those which cannot be met without further technical development is also presented. There do not appear to be any specifications which cannot be met because of technical limitations.

Those specifications that can be met today are as follows:

(a) Effect of overdrive.

Based on our experience with experimental reflection amplifiers incorporating the most recently designed Hughes Si and Raytheon GaAs diodes we do not anticipate diode damage or failure if the amplifier is driven to all levels to 12dB above the saturated drive levels. No serious instabilities have been observed at very large signals.

(b) Stability to all loads.

With an isolator incorporated into its output line, the amplifier will be stable against all phase changes.

(c) Effect of supply voltage changes.

Suitable current regulated and voltage regulated power supplies will be used to prevent damage to the amplifier as the voltage is varied over a range of 0 to 33 volts.

(d) Temperature effects.

It is not anticipated that any permanent damage to the amplifier will result over a 40°F to 175°F range, for any rf drive less than that corresponding to 12dB above the saturated drive level.

(e) Spurious output signals

Based on our experimental studies to date we believe that with an input drive signal 2dB beyond saturation level all coherent components, including harmonics, will be less than 10dB below the carrier. All nonharmonic components in a 20 KHz band will be more than 60dB below the carrier. The residual AM signals will be 50dB below the carrier for drive levels from the saturation value to 10dB below saturation. We also anticipate that the PM will be less than 10milliradians peak-to-peak over a frequency band between 100 Hz to 1 MHz each side of the carrier.

(f) Phase change.

As discussed in the section which follows, it is anticipated that for any input power up to saturation the phase change, with drive, will be less than $4^{\circ}/\text{dB}$ and less than $47^{\circ}/30\text{dB}$.

(g) Recovery time and time delay distortions.

The stored electrical energy in the amplifier and its total electrical length is so small that we do not anticipate meeting the rise and fall time specifications and the time delay distortion specifications.

(h) Noise figure

The overall noise figure of the hybrid amplifier will be determined by the FET preamplifier. The noise figure will be much less than the specified 30dB maximum.

(i) Insertion loss.

A high degree of isolation will be present in the FET preamplifier stage so that no difficulty is anticipated in meeting the 70 dB minimum insertion loss specification over a 4 to 12 GHz range.

(j) Dimensions

The overall dimensions of the hybrid amplifier should be quite small and it is anticipated that the maximum dimensions of 14" x 4.5" x 5" can be met. The largest part of the amplifier will be heat radiators.

(k) Intermodulation distortion

As discussed in the sections which follow, it is anticipated that the intermodulation specifications can be met by careful design.

Those specifications that would require some further development to be met are:

(a) Reliability

Basically both the FET and IMPATT devices used are inherently long-life and reliable devices. It is suggested, however, that environmental tests and accelerated life tests should be conducted to establish the overall reliability of the proposed amplifier. No serious problems are anticipated.

(b) Circuit related specification

The proposed amplifier consists of a combination of two state-of-the-art devices. A careful study of the gain slope requirement, the gain features requirement, and the 5dB compression in gain specification should be made after experimental models of the proposed amplifier are fabricated. No serious difficulties are anticipated, however.

Cornell could contribute to the development of the proposed amplifier by conducting both experimental and theoretical studies of the large signal properties of the FET penultimate amplifier stage and the IMPATT output stage including: intermodulation characteristics; phase characteristics; efficiency, large signal diode properties; and reliability under different environmental conditions.

The work would be directed towards the goal of obtaining a hybrid amplifier design that would meet all of the design requirements listed in the specifications sheet.

III.a Analysis of 3^d Order Intermodulation Products

At first glance it would seem that to analyze intermodulation distortion one would have to tackle the nonlinearities of the avalanche at the fundamental and second harmonic frequencies. The third order intermodulation component sought is the difference frequency between the carrier frequency and the second harmonic of either an upper or lower sideband. Fortunately there is a simpler approach which utilizes the admittance variation with input power or r.f. voltage across the diode chip. One assumes an incident signal

$$V_o \cos \omega_1 t + V_o \cos \omega_2 t , \quad (1)$$

or

$$2V_o \cos pt \cos \omega_o t , \quad (2)$$

where $p = \frac{1}{2} (\omega_2 - \omega_1)$, and $\omega_o = \frac{1}{2} (\omega_1 + \omega_2)$. These two microwave signals ω_1, ω_2 modulate the envelope at frequency p , which is a much smaller frequency. Being smaller we can regard the admittance as being modulated at the frequency p . Now if the admittance is not a function of the voltage then the chip voltage amplitude will vary sinusoidally at frequency p , but since the admittance is modulated then harmonics at $3p, 5p$ etc. will be generated in the chip voltage. Our task is to identify the amplitude of this third harmonic and compare the power in it to that at the fundamental frequency p .

First let us describe an amplifier model; a schematic of a suitable amplifier is shown in Fig. 1. The transfer matrix,

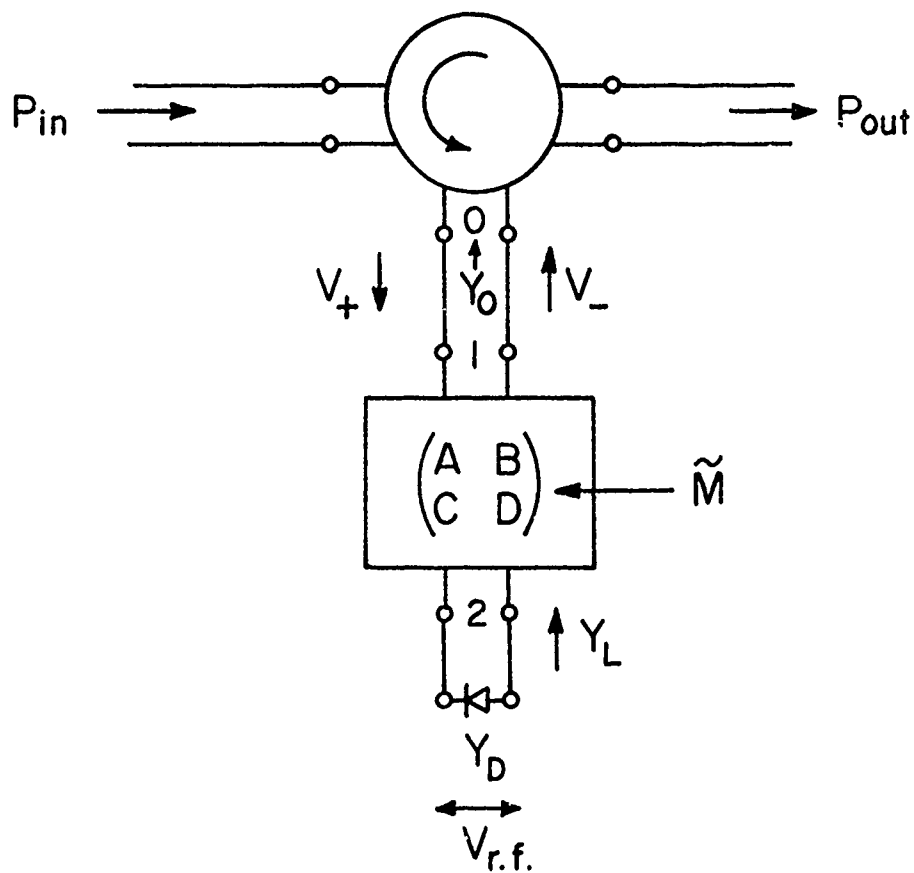


Figure IIIa-1.

$\tilde{M}$, of Fig. 1 is an admittance matrix which transforms (I_1, V_1) into (I_2, V_2) ,

$$(I_1, V_1) \begin{pmatrix} A & B \\ C & D \end{pmatrix} = (I_1 A + V_1 C, I_1 B + V_1 D) = (I_2, V_2) \quad (3)$$

If the matrix $\tilde{M}$, which represents some network of slugs, is lossless then B and C are pure imaginary and the $\det \tilde{M} = 1$. The reverse transformation from terminals (2) to terminals (1) is the complex conjugate of the inverse of $\tilde{M}$ (i.e., $\tilde{M}^{-1*}$) and is given by

$$(I_2, V_2) \begin{pmatrix} D & B \\ C & A \end{pmatrix} = (I_2 D + V_2 C, I_2 B + V_2 A) = (I_1, V_1) \quad (4)$$

and the admittance from (2) towards (1) is

$$Y_L = \frac{I_2}{V_2} = \frac{I_1 A + V_1 C}{I_1 B + V_1 D} = \frac{Y_o A + C}{Y_o B + D} = \frac{A + Z_o C}{B + Z_o D} \quad (5)$$

The reflection coefficient at terminals (1) is

$$\rho_1 = \frac{Y_o - Y_1}{Y_o + Y_1} = \frac{Y_L^* - Y_D}{Y_L + Y_D} e^{-j\theta} \quad (6)$$

where

$$e^{-j\theta} = \frac{-Y_o B + D}{Y_o B + D} \quad (7)$$

Note that C has the dimension of admittance, B has the dimension of impedance, and A and D are numbers.

Coming back to the signal incident upon the diode, we take the amplitude of the carrier to be

$$V_+ = 2V_o \cos pt \quad . \quad (8)$$

The incident power on the diode is

$$P_{in} = V_+^2 G_L / 2 = 2V_o^2 G_L \cos^2 pt \quad , \quad (9)$$

and the average incident power is given by

$$\bar{P}_{in} = V_o^2 G_L \quad . \quad (10)$$

The next step is to derive the relation between V_{rf} and P_{in} . This may be done by considering that the r.f. diode current is the sum of the incident and reflected waves

$$I_{rf} = I_+ + I_- = I_+(1 - \rho_2) = (jB_L + Y_D)V_{rf} \quad , \quad (11)$$

where the reactive part of Y_L is associated with the diode admittance because of the form of Eq. (6) which may be re-written as

$$\rho_1 = \frac{G_L - (B_L + Y_D)}{G_L + (B_L + Y_D)} e^{-j\theta} \quad . \quad (12)$$

Inserting the reflection coefficient at (2) into Eq. (11) we obtain

$$V_{+G_L} = V_{rf} \frac{jB_L + Y_D}{1 - \frac{G_L - (jB_L + Y_D)}{G_L + (jB_L + Y_D)}} = V_{rf} \frac{Y_L + Y_D}{2} \quad (13)$$

Using Eq. (9) and (13) we obtain the relation between the input power and the diode r.f. voltage

$$16V_o^2 G_L^2 \cos^2 p_t = |V_{rf}|^2 |Y_L + Y_D|^2 \quad (14)$$

Putting Eq. (14) into the usual normalized form

$$\cos^2 p_t = \frac{1}{16} \frac{|V_{rf}|^2}{V_o^2} |(1+g)+jb|^2 = u^2 [(1+g)^2 + b^2] \quad (15)$$

where $g \equiv G_D/G_L$, and $b \equiv (B_L + B_D)/G_L$.

When one now considers the voltage variation of g and b , it can be seen that there must be harmonic components of the voltage on the right hand side of Eq. (15) that add up to the sinusoidal variation on the left hand side. Theoretically and in practice one finds the conductance to vary with the r.f. voltage as

$$g = g_{ss} + g_2 u^2 + g_3 u^3 + g_4 u^4 \quad (16)$$

where $u^2 = |V_{rf}|^2 / 16V_o^2$ and a similar expansion is obtained for b . Note that the linear term in Eq. (16) is missing

because modulation of the admittance at large signals arises partly from internal rectification which only involves even powers of the voltage and from the nonlinear response of the avalanche current which contributes the cubic term and higher order odd powers.

The relation between Eq. (15) and the usual expression for reflection amplifier gain can be seen quite readily if one, for the moment, neglects the amplitude dependence of the admittance. Using Eq. (8) in Eq. (16) one obtains

$$|V_+|^2 = \frac{1}{4}|V_{rf}|^2 |(1+g)+jb|^2 \quad (17)$$

In complex terms Eq. (17) can be written

$$V_+ = \frac{1}{2}V_{rf}[(1+g)+jb] = \frac{1}{2}(V_+ + V_-)[(1+g)+jb] \quad (18)$$

Solving for the output voltage

$$V_- = V_+ \frac{(1-g)-jb}{(1+g)+jb}, \quad (19)$$

and finally taking the absolute value again

$$G = \left| \frac{V_-}{V_+} \right|^2 = \frac{(1-g)^2 + b^2}{(1+g)^2 + b^2} \quad (20)$$

which is the usual expression for the power gain.

The problem of finding the third order intermodulation products (IMP) is now reduced to reverting the power series

in u , represented by Eq. (15), to express u as a power series in $|\cos pt|$. Having reverted the series one then finds the fundamental and third harmonic terms in the modulation frequency. The third harmonic term yields the IMP by the trigonometric expansion

$$\cos 3pt \cos \omega_0 t = \frac{1}{2} \{ \cos(2\omega_2 - \omega_1)t + \cos(2\omega_1 - \omega_2)t \}. \quad (21)$$

One must remember that the reverted series is in terms of the absolute value of $|\cos pt|$ so that the fundamental and third harmonic terms are given by the expressions

$$u^{(1)} = \frac{4}{\pi} \int_0^{\pi/2} u(|\cos \theta|) \cos \theta d\theta \rightarrow \text{Fundamental component}, \quad (22)$$

$$u^{(3)} = \frac{4}{\pi} \int_0^{\pi/2} u(|\cos \theta|) \cos 3\theta d\theta \rightarrow 3^{\text{d}} \text{ harmonic component}. \quad (23)$$

Finally, the magnitude of the IMP relative to the carrier in decibels is given by the expression

$$20 \log \left| \frac{u^{(3)}}{u^{(1)} - u_+^{(1)}} \right| \rightarrow 3^{\text{d}} \text{ order IMP} \quad (24)$$

where we have subtracted the amplitude of the normalized incident voltage wave ($u_+^{(1)} = .5$) from the fundamental component of the chip voltage.

We can now use Eq. (24) to guide us in designing or

selecting devices which will satisfy the intermodulation specification of the TWTA. As an illustrative example let us take an amplifier with a small signal gain of 10dB and a large signal gain of 5dB. In addition, we shall assume that the diode used in the amplifier is a well designed Read structure with negligible electronic susceptance. For these conditions $g_{ss} = -.5195$ and this decreases at the 5dB compression level to $g_m = -.2801$. At maximum amplitude the normalized voltage is

$$u_m = (1+g_m)^{-1} = 1.3891 \quad . \quad (25)$$

Then for a variation of g similar to that in many IMPATTs we take

$$(g/g_{ss}) = 1 - .8260\zeta + .3652\zeta^3 \quad (26)$$

where $\zeta \equiv u/u_m$. A plot of Eq. (26) is shown in Fig. 2. When Eq. (26) is used in Eq. (15) one obtains the plot shown in Fig. 3.

Reverting the series used to plot the graph in Fig. 2 gives the following polynomial

$$u = 2.08836y - .064983y^2 - 4.64604y^3 + 10.9054y^4 - 12.5066y^5 + 7.41970y^6 - 1.80679y^7 \quad , \quad (27)$$

where $y = |\cos\phi|$. The large coefficients of Eq. (25) and the high order make it clear that the reversion process is best

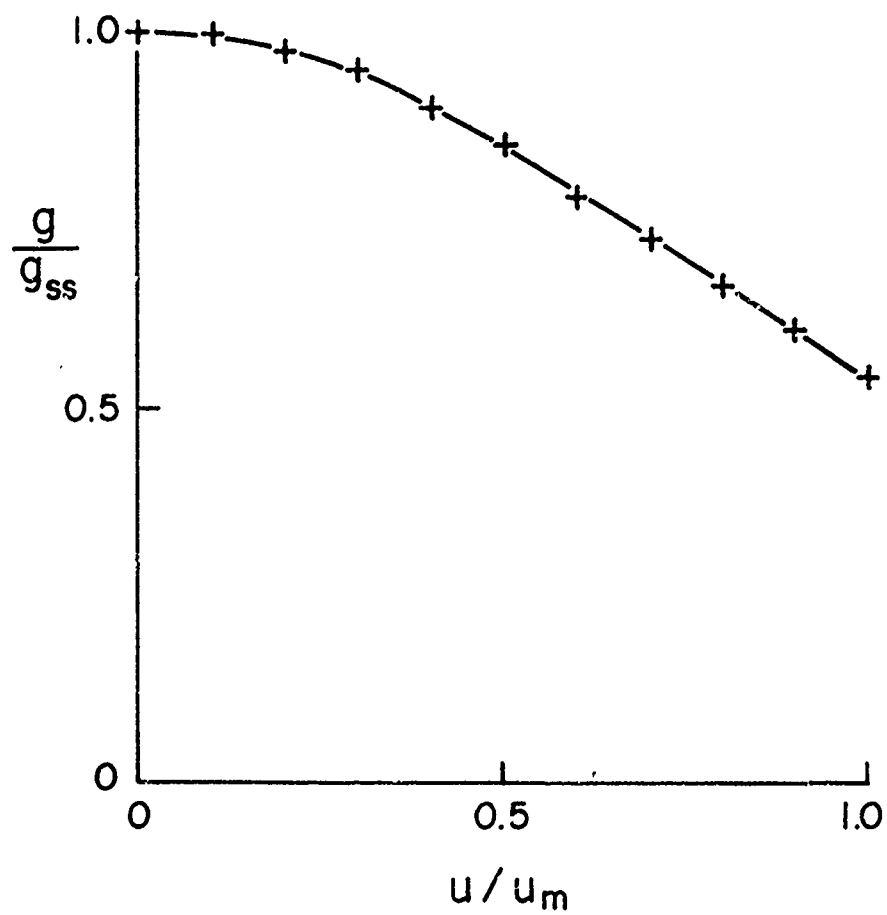


Figure IIIa-2

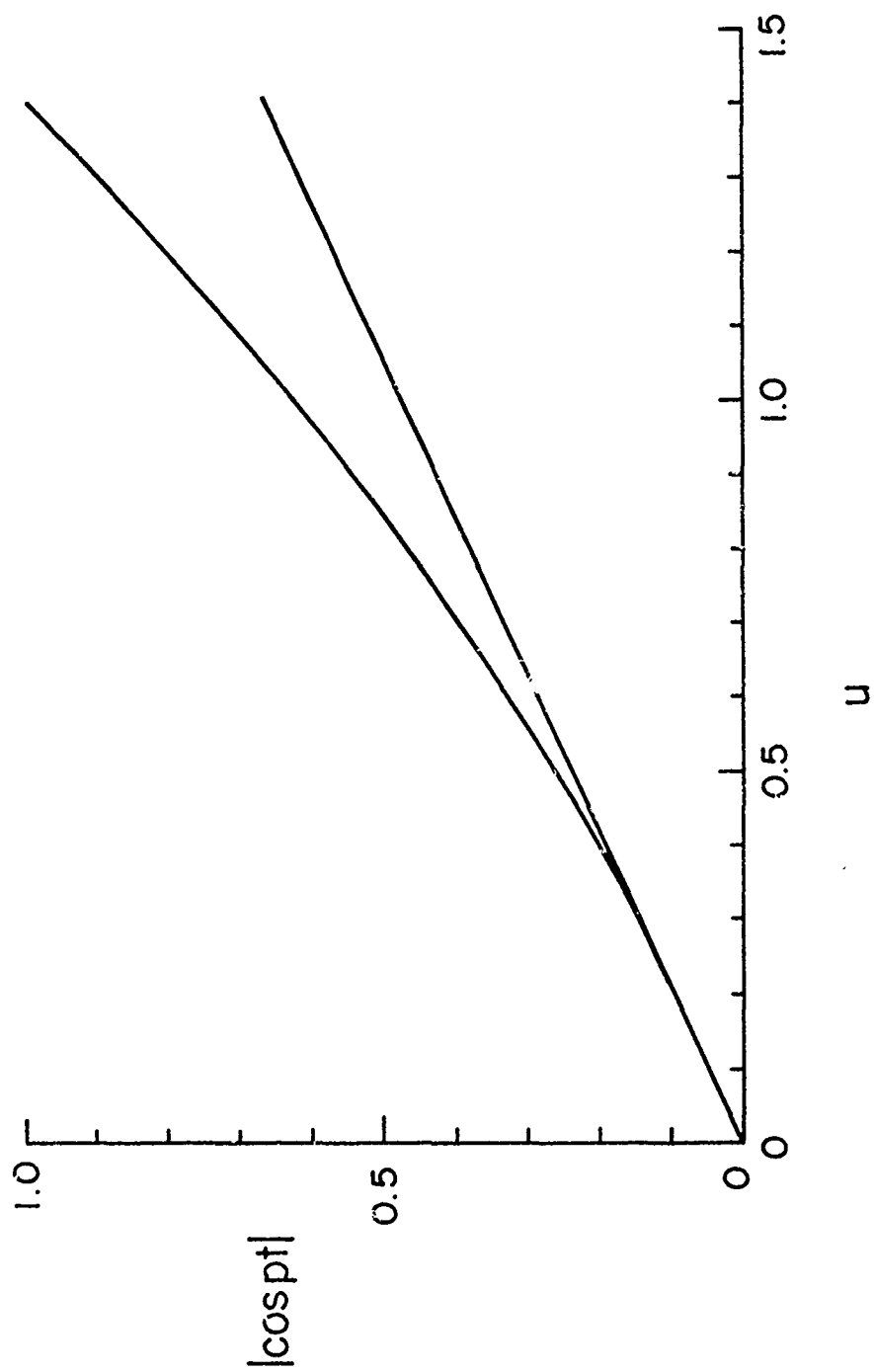


Figure IIIa-3.

done numerically. Using Eq. (27) to evaluate the integrals of Eqs. (22) and (23) we find the IMP for this example to be

$$20 \log \left| \frac{u_{-}^{(3)}}{u_{-}^{(1)} - u_{+}^{(1)}} \right| = -19.7 \text{ dB.} \quad (28)$$

The rationale for the above choice of parameters is that the TWTAs specifications require a saturated gain of 50dB which is 5dB less than the small signal gain. The third order IMP are to be -9.5dB at the saturation level or at the 5dB compression point. With the expectation that the nonlinearities of the avalanche device would be more severe, all of the gain compression was absorbed in the last stage. Thus the preceding input stages are assumed to have 45dB gain and to have negligible gain compression. The relatively low gain chosen for the output stage permits obtaining essentially the full output power and efficiency of the Read diode.

Knowing that the electronic susceptance is the most probable cause of a high level of IMP we can use the analysis developed here to estimate what degradation it introduces. The usual silicon flat profile IMPATT has an electronic susceptance of about three times its negative electronic conductance ($Q_p \approx 3$). This large value of Q_p makes it marginal for such a diode to meet the required

-10dB of the IMP below the carrier. Thus it is essential to use a device where $Q_p \leq .5$ for large and small signals. We have measured hard punch-on Read structures of GaAs for which $Q_p \leq .6$ at small and moderate signal levels (1 watt). If these devices can be shown to maintain this low level of electronic susceptance at higher power levels then the IMP specification for the TWTA of -10dB with respect to the carrier at the 5dB compression point can indeed be met. In the following section a graphical analysis using experimental data gives greater weight to this conclusion.

III.b Estimation of IMPATT Amplifier Intermodulation Products Using a Graphical Analysis

In this section an estimation of the intermodulation products to be expected from the IMPATT amplifier stage is given, using a graphical technique. The analysis requires a knowledge of the large signal admittance properties of the diode. Using admittance data¹ obtained on a GaAs Raytheon Read diode it was found that at the 5dB compression point the intermodulation products readily meet the -10dB below the carrier requirement. It should be noted that the calculations were based on measured large signal properties of a single diode. The results strongly suggest, however, that it is possible to meet the overall intermodulation specification. They also suggest that further studies of the diode and circuit design parameters controlling intermodulation be undertaken.

Included below is a brief outline of the method used to determine the intermodulation products. A summary of the results calculated for the Raytheon Read diode is also given. Briefly, in this method it is assumed that the gain characteristic of the amplifier is modulated at a frequency equal to half the difference of the two microwave input signals. This modulation results in sidebands at the microwave frequency, one of which is spaced below the lower frequency input signal by an amount equal to the frequency difference of the input signals and another which is spaced above the higher frequency input signal by the same amount. For simplicity it is assumed that the amplitudes of the two input signals are equal. It is also assumed that the reactive part of the Read diode admittance can be neglected.

We do not believe that this assumption drastically underestimates the intermodulation products since it is known that certain GaAs Read diode structures do have a negligibly small susceptance.

The admittance of the chip is

$$Y_e = -G_s F_r$$

where G_s is the small signal chip conductance and F_r is a large signal compression factor. For the Raytheon Read diode No. 605-BC-64 this factor is, approximately

$$F_r = 1 - 3\alpha^2 + 2\alpha^3 \quad (\alpha \leq 0.6)$$

where α equals the chip voltage divided by the bias voltage.

In terms of F_r , the voltage gain of the amplifier, assuming a simple parallel resonant circuit, is:

$$G_v = \frac{\frac{Q_d}{Q_x} - \frac{Q_d}{Q_o} + F_r}{\frac{Q_d}{Q_x} + \frac{Q_d}{Q_o} - F_r}$$

where Q_x = external Q of the amplifier

Q_d = small signal diode Q (imbedded in the circuit)

Q_o = internal Q of the amplifier.

In terms of α , the input power can be computed from

$$P_i = G_s V_b^2 \frac{F_r - \frac{Q_d}{Q_o}}{2(G_v^2 - 1)} \alpha^2$$

where V_b is the bias voltage. The corresponding value of the

output power is

$$P_o = G_v^2 P_i$$

A power output curve vs. power input curve can be constructed from these equations if Q_d/Q_x and Q_d/Q_o are known. If we assume $Q_d/Q_o = 0.1$ and choose $Q_d/Q_x = 1.73$ to make the small signal gain equal to 10dB, we obtain the output power vs. input power characteristic shown in Figure 1. For the conditions assumed for this diode the power output at the 5dB compression point is approximately 2.3 watts. Since this diode is a single mesa type, it is anticipated that with a 4 mesa device, 8 to 9 watts per device is a reasonable expectation.

To determine the intermodulation products of the amplifier the graph of Figure 2, showing the output voltage of the amplifier vs. the input voltage, was constructed. Use was made of the equations given above and the input voltage equation:

$$V_+ = (2Z_o P_i)^{1/2} = 10 P_i^{1/2} ,$$

where it has been assumed that the characteristic impedance of the input line Z_o , is 50 ohms. The envelope of the input voltage is assumed to be

$$V_+ = 10 \cos pt$$

and the envelope of the output wave, as determined using Figure 2, is shown in Figure 3. For simplicity only the first quarter cycle is shown.

OUTPUT POWER vs INPUT POWER

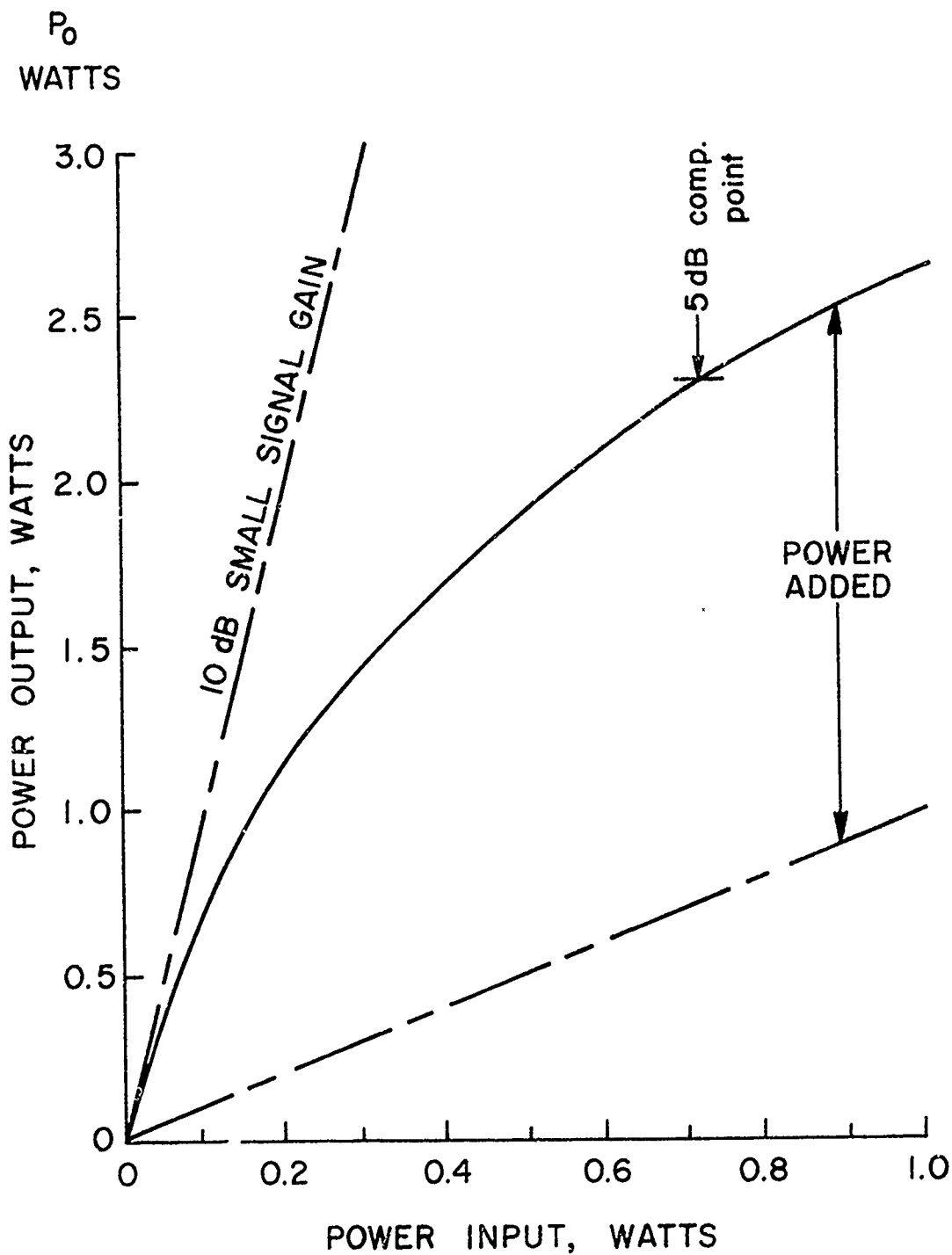


Figure IIIb-1.

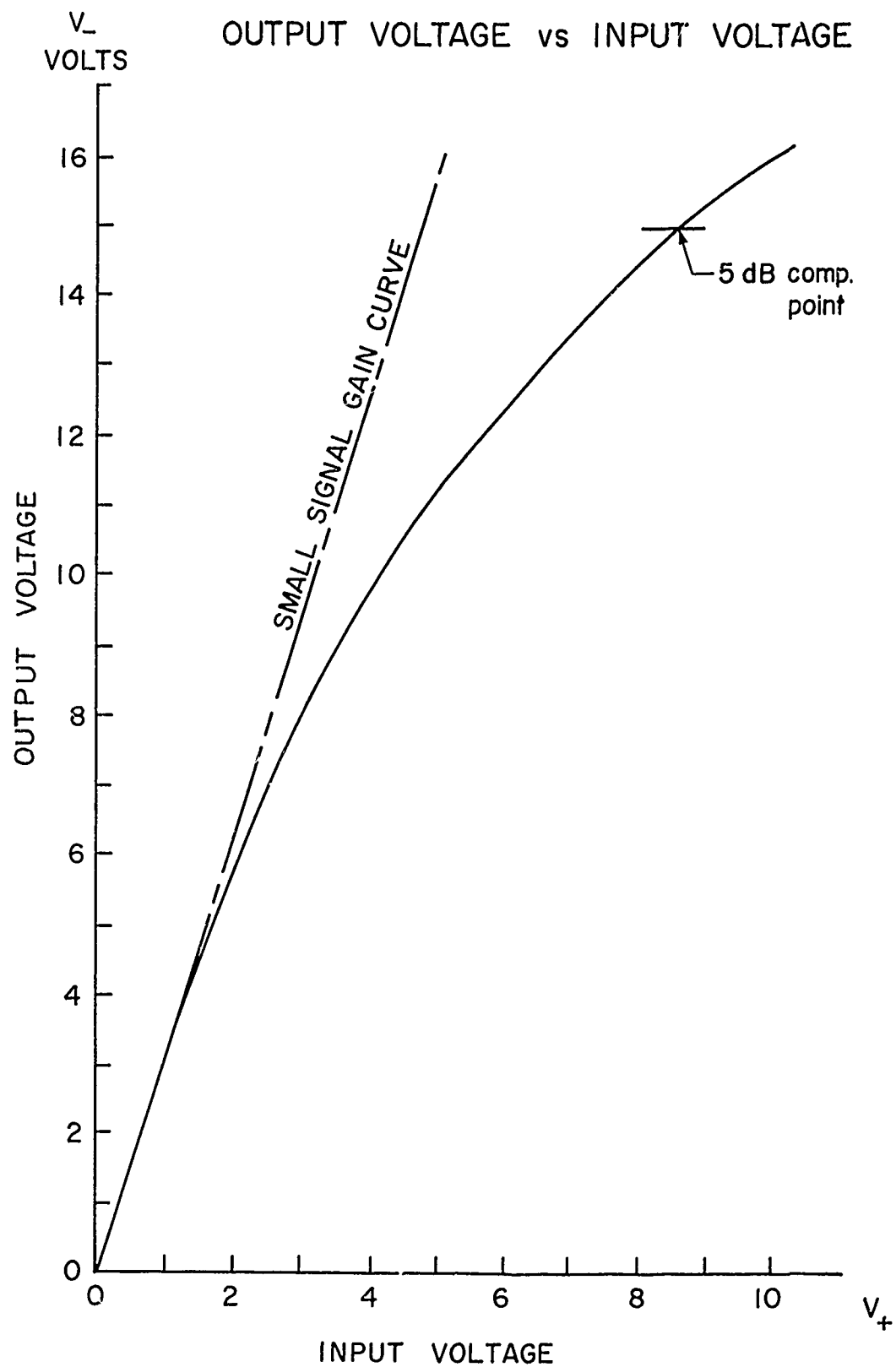


Figure IIIb-2.

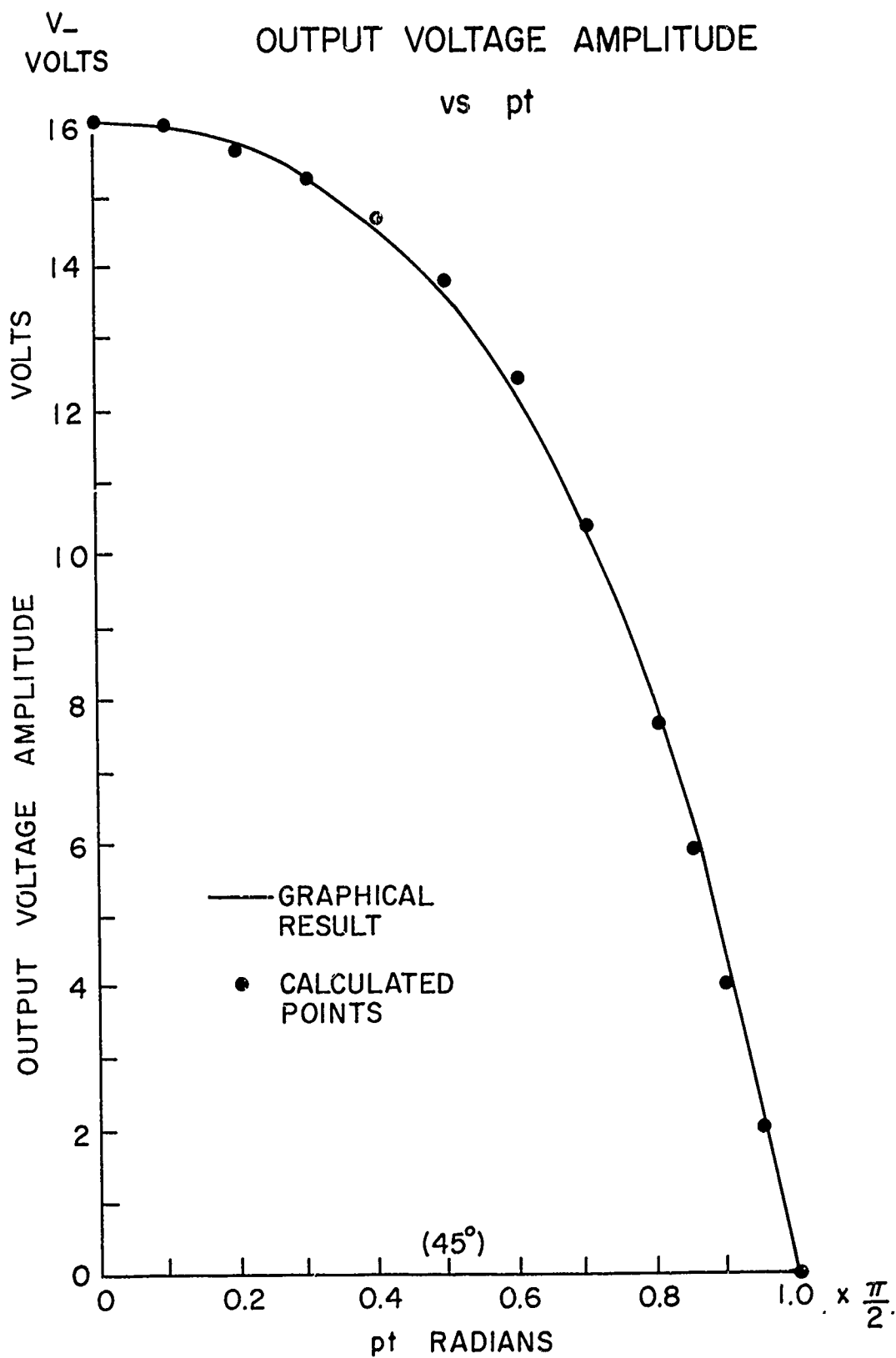


Figure IIIb-3.

It is evident from the flat top of the curve of Figure 3 that higher order harmonic voltages are present in the output voltage envelope. As discussed earlier, these harmonics give rise to the intermodulation products. A numerical Fourier analysis, using Simpson's Rule, was performed on the output wave envelope and the amplitudes of the first and third harmonics were found to be 17.7 volts peak and -2.17 volts peak. This corresponds to a third order intermodulation product of -18.2 dB. This value, calculated at the 5dB compression point, is well below the maximum allowed value of -10dB.

An alternative method of calculating the intermodulation products is as follows: for the case of cosine wave modulation, corresponding to equal two tone microwave input signals, the output signal is assumed to be:

$$V_- = V_1 \cos pt + V_3 \cos pt + V_5 \cos 5pt$$

If we let $pt = 0, 36^\circ$ and 60° we obtain three equations:

$$V_{-(0^\circ)} = V_1 + V_3 + V_5$$

$$V_{-(36^\circ)} = 0.81 V_1 = 0.31V_3 - V_5$$

$$V_{-(60^\circ)} = 0.5V_1 - V_3 + 0.5V_5$$

The values of the voltages on the left hand side of these equations can be determined using Figure 2 using the corresponding values of the input voltages:

$$V_{+(0)} = V_o$$

$$V_{+(36^\circ)} = 0.81 V_o$$

$$V_{+(60^\circ)} = 0.5 V_o$$

The amplitudes V , V_3 and V_5 are then found by solving the above set of simultaneous equations. Taking $V_o = 10$ watts and using Figure 2 we find that the output voltage amplitude is

$$V_- = 17.73 \cos pt - 2.13 \cos 3pt + 0.404 \cos 5pt$$

The values of V_- calculated using this equation, shown plotted as points in Figure 3, are in good agreement with the graphical determined result shown in the figure. Using the calculated output voltage amplitudes, the 3rd order intermodulation product is found to be -18.4 dB which is in excellent agreement with the previously calculated value, and the 5th order product is found to be -32.85 dB.

Reference:

1. S. C. Wang, "IMPATT Diode Oscillator Load Characteristics," M. S. Thesis, Cornell University, August, 1975.

III.c Relation of Phase Shift with Input Power to IMPATT Diode Parameters

To calculate the phase shift of a reflection amplifier with input power it is first necessary to find the relation between phase shift and the electronic admittance of the diode. First we recall that the reflection coefficient of an amplifier is given by,

$$\rho = \frac{V_-}{V_+} = \frac{(1-g)-jb}{(1+g)+jb} \quad , \quad (1)$$

where g , b are defined as in Eq. (15) of Section 3(a). Putting Eq. (1) into polar form

$$\rho = \frac{(1-g)^2+b^2}{(1+g)^2+b^2} e^{-j\{\tan^{-1} \frac{b}{1-g} + \tan^{-1} \frac{b}{1+g}\}} \quad (2)$$

from which we take the phase angle to be

$$\theta = \tan^{-1} \frac{b}{1-g} + \tan^{-1} \frac{b}{1+g} \quad . \quad (3)$$

Differentiating Eq. (3) with respect to the amplitude of the ac chip voltage we find the maximum value of the derivative to occur at $b \approx 0$ where

$$\frac{d\theta}{dV_c} = \frac{2}{1-g^2} \frac{db}{dV_c} \quad . \quad (4)$$

Now the susceptance of a singly tuned amplifier is given by

$$b = 2\delta Q_x + \frac{\omega C_e'}{\omega_o C_{eq}} \quad (5)$$

where $\omega C_e' = B_e$ is the electronic susceptance, dependent upon the chip voltage amplitude, and C_{eq} is the equivalent capacitance of the resonant cavity in which the diode is embedded. Using Eq. (5) in Eq. (4)

$$\frac{d\theta}{dV_c} = \frac{2}{1-g^2} \cdot \frac{1}{\omega_o C_{eq}} \frac{dB_e}{dV_c} \quad (6)$$

To obtain the derivative of θ with respect to the input power in dB we need to evaluate

$$\frac{d[10 \log P_{in}]}{dV_c} = 10 \log e \frac{d(\ln P_{in})}{dV_+} \cdot \frac{dV_+}{dV_c} \quad (7)$$

Using the relation

$$V_+ = \frac{1}{2} (1+g)V_c \quad (8)$$

in Eq. (7) we obtain

$$\frac{d[10 \log P_{in}]}{dV_c} = \frac{20 \log e}{V_c} \left[1 + \frac{V_c}{1+g} \frac{dg}{dV_c} \right] \quad (9)$$

Then dividing Eq. (6) by Eq. (9) we obtain the desired derivative

$$-\frac{d\theta}{d(10 \log P_{in})} = \frac{180}{20\pi \log e} \cdot \frac{2}{(1-g)^2 \left[1 + \frac{V_c}{1+g} \frac{dg}{dV_c} \right] \omega_o C_{eq}} \cdot V_c \frac{dB_e}{dV_c} \quad (10)$$

Using the measured variation of susceptance and conductance versus chip voltage shown in Figs. 1 and 2 for an X-band silicon IMPATT we find

$$V_c \frac{dB_e}{dV_c} = .012 \text{ S}, \quad (11)$$

and

$$V_c \frac{dG_d}{dV_c} \sim 2 \times 10^{-3} \text{ S}. \quad (12)$$

Then taking $\omega_o C_{eq} = 4\pi \times 10^{-2} \text{ S}$, $\epsilon_m = -.2801$, $Q_x = 30$, we can evaluate Eq. (10) and obtain

$$\frac{d\theta}{d(10 \log P_{in})} \sim -.8^\circ/\text{dB} \quad (13)$$

which is an order of magnitude less than the required $5^\circ/\text{dB}$. Under circumstances where the diode is driven hard, the variation of electronic susceptance can increase perhaps an order of magnitude and while this phase distortion limit may not be exceeded, the third order IMP will almost certainly be the limiting factor.

We conclude from the above calculation that the limit of $5^\circ/\text{dB}$ of input power can easily be met in an avalanche diode output amplifier stage.

HUGHES IMPATT 250
f ~ 9.6 GHz

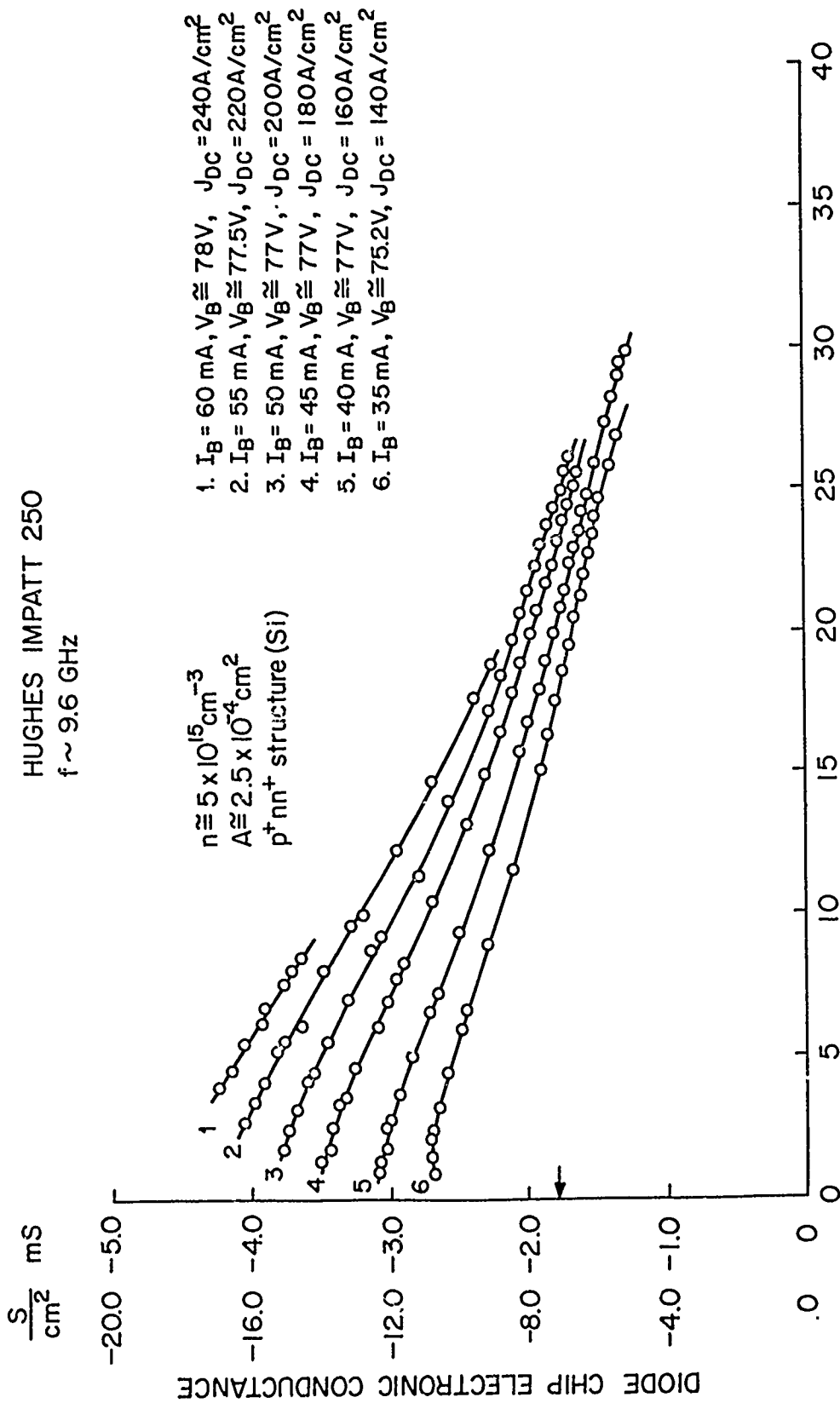


Figure IIIc-1.

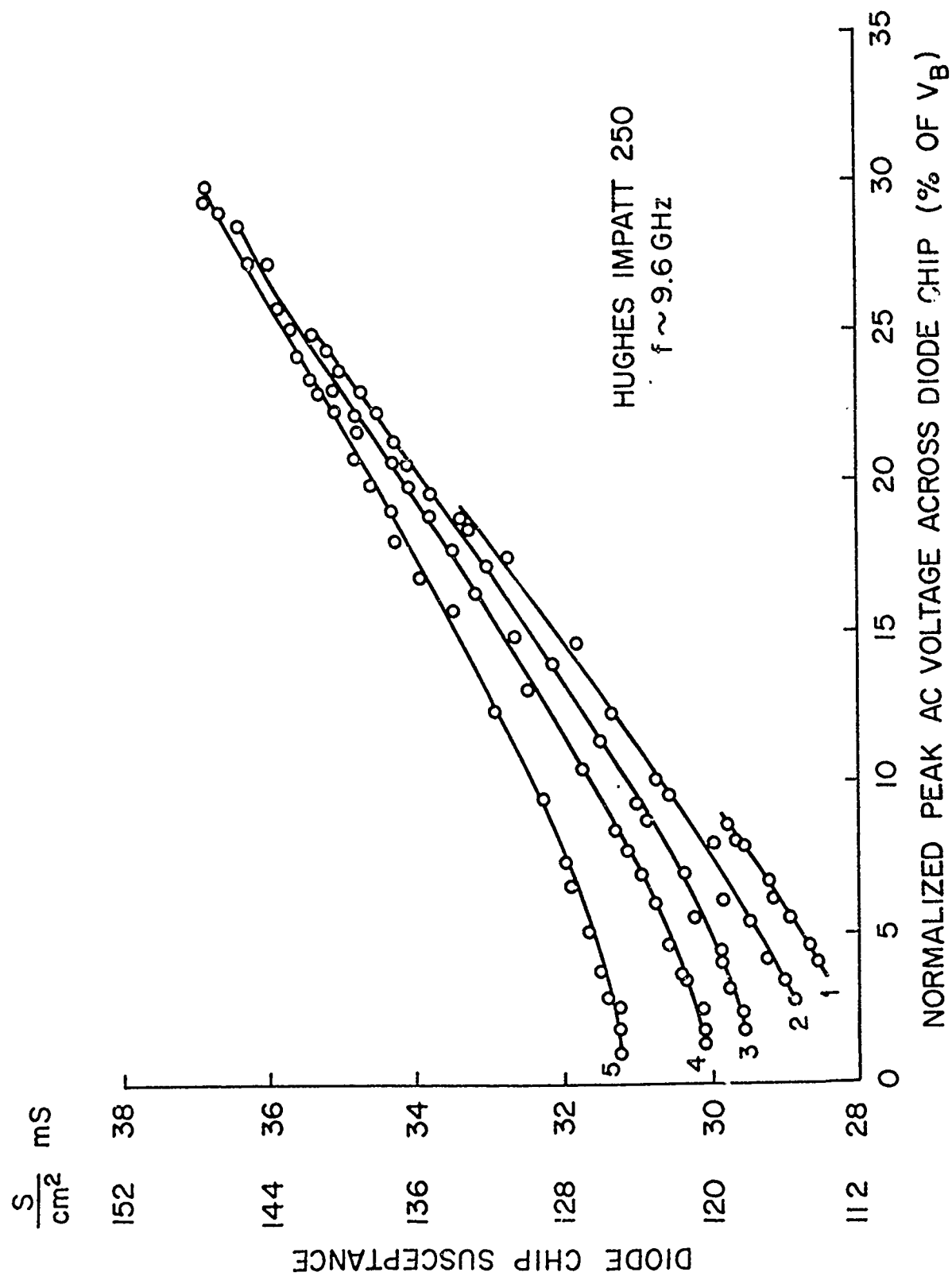


Figure IIIc-2.

IV. Development Requirements for Solid State TWTA Replacement

The preceding sections have reviewed the required specification that the proposed FET/Read hybrid amplifier would have to meet. The conclusion of the theoretical and experimental analysis was that the TWTA specifications can be met by selected but presently manufactured GaAs Read diodes and state-of-the-art FET transistors. Some sacrifice in the overall efficiency of 30% will probably have to be made.

In the light of these conclusions funds presently allocated to the Cornell microwave group by RADC will be applied to testing the final stage of the proposed hybrid amplifier with particular emphasis on maximizing the output power, efficiency, and linearity. If time and funds permit the testing will include the penultimate FET driver stage. It is hoped that this effort will provide a firm feasibility demonstration of the proposed hybrid design.

Going beyond the immediate feasibility demonstration of the hybrid amplifier there are a number of important areas for development. The first of these is the Schottky barrier metallurgy used in the avalanche diode. It is known that a platinum barrier yields the most efficient diodes, but the Pt-GaAs is not stable at operating temperatures. Grown p-n junctions provide a solution for a stable interface, but at some sacrifice in efficiency and constructional complexity.

Research done at Cornell on various Schottky barrier metallizations has uncovered some promising combinations that retain the desirable electrical characteristics of platinum but maintain a stable interface. Funding of this investigation should continue.

The extensive measurement and modeling program carried out at Cornell for many years can now identify the material parameters in devices that are necessary for high level performance. Recent measurements on avalanche diodes indicate that material parameters essential for high efficiency are not maintained reliably with present manufacturing procedures. In this area a program is needed which will integrate for both transistor and avalanche devices these analytical measurements with device technology development covering diffusion methods, ion implantation, and contact metallurgy. Specific problems that have been identified with high temperature processing are the control of background impurities which affect the saturation current of the diode and the uniformity of the generation rate over the area of the device. Epitaxial growth has additional problems of interface defects and traps as well as background impurity control. Contacting metallurgy is particularly important to controlling the saturation current in avalanche diodes which has been found to be two to three orders of magnitude higher in devices than in bulk material. It is still desirable to seek simple metallization techniques for ohmic, non-injecting chemically stable contacts.

Finally we propose a re-examination of the microwave performance of the GaAs bipolar transistor, particularly its power capabilities because the geometry of the bipolar device is more suited to high power. The improvement in performance of the FET which is due to ballistic transport of the electrons in the channel region should also be found in the bipolar device. In past studies good injection efficiency was difficult to achieve but the heterojunction techniques used with lasers and improved donor ion implantation techniques can now provide a solution for obtaining high injection efficiency. We propose that ballistic transport improvement of the GaAs bipolar transistor be investigated.

FIGURE CAPTIONS

Figure Number

- IIIa-1. Schematic drawing of reflection amplifier model used for calculating intermodulation distortion.
- IIIa-2. Plot of assumed variation of normalized chip conductance as a function of chip voltage. The normalized chip voltage u_m corresponds to the 5dB gain compression specification.
- IIIa-3. Plot of the reverted series of Eq. (27) showing the relation between the normalized chip voltage and the normalized voltage wave incident upon the amplifier.
- IIIb-1. Graph of computed output power vs. input power for a punch-through GaAs Read diode based on measured conductance vs. chip voltage variation. The indicated 5dB compression point corresponds closely to the saturated added power of the amplifier.
- IIIb-2. Calculated output voltage (V_-) vs. input voltage (V_+) based on curve in Fig. IIIb-1.
- IIIb-3. Amplifier output voltage for assumed input voltage $V_+ = 10 \cos pt$.
- IIIc-1. Measured variation of chip electronic conductance vs. normalized chip voltage for a flat profile silicon IMPATT.
- IIIc-2. Measured variation of total chip susceptance as a function of chip voltage for the same diode of Fig. IIIc-1.

SECTION C

DESIGN OF HIGH-POWER SOLID-STATE AMPLIFIERS FOR TWTA REPLACEMENT

Walter H. Ku

I. Introduction

Recent advances in device technology have predicted two of the most promising microwave solid-state devices for high-power and high-efficiency amplification. These are the GaAs FETs and GaAs Read IMPATT diodes. The state-of-the-art development of these devices has reached the point where serious considerations can be given for these devices to be designed as linear amplifiers for TWTA replacement in medium power (1-10W) system applications.

Before the feasibility for TWTA replacement can be established, a number of technical problems involving high-power amplifier design must be solved. These include the problem of device characterizations under large-signal operating conditions, design of high-power amplifiers with gain-bandwidth constraints, and the difficult problem of predicting and reduction of distortion characteristics of high-power solid-state amplifiers. In the following sections, the design of both GaAs FET amplifiers and IMPATT diode reflection amplifiers will be discussed. Since the specified power output is 10W at 7.5 GHz and the gain required is 55 dB, amplifiers must be cascaded. In the case of the GaAs power FET amplifiers, the final stages must be power combined. The design of cascaded and quadrature hybrid combined solid-state amplifiers will be presented. For both GaAs FETs and IMPATT diodes operating

under high-power conditions, the nonlinear device characteristics become important design consideration. A general study of nonlinear distortion characteristics of solid-state amplifiers will be presented. A general approach without assuming that the nonlinearities are zero-memory will be used. In the case of the FET, a simplified nonlinear model will be used.

II. High-Power FET Amplifiers

This section presents the results of design of high-power GaAs FET amplifiers for the prescribed 7.25-7.75 GHz. The FETs considered are those reported by RCA, Fujitsu, and T.I. The amplifier designs are based on both measured device scattering parameters as well as device equivalent circuits. The design approach used is that of first deriving unilateral lumped and distributed equivalent circuits of the FET and then design the input and output matching networks. This initial design is then optimized using the actual measured device parameters. It is noted that the scattering parameters for a large-signal FET may be functions of the RF signal level and the optimized design needs to be further modified to account for the variations of the device characteristics.

The proposed FET amplifier configuration for TWTA replacement is that of a cascaded amplifiers with the final stage consisting of four quadrature hybrid combined FET amplifier as shown in Figure 1. Assuming that each amplifier is capable of delivering 2.5 - 2.9W of output power, from 7.25 - 7.75 GHz, then the combined power output will meet the required 10W specification. Because of the cascading, each FET amplifier module will be designed to cover a wider bandwidth than the required 500 MHz bandwidth. In Figure 1, we used quadrature hybrids for both power divider and combiner although Wilkinson-type of 4-way combiner could also be used.

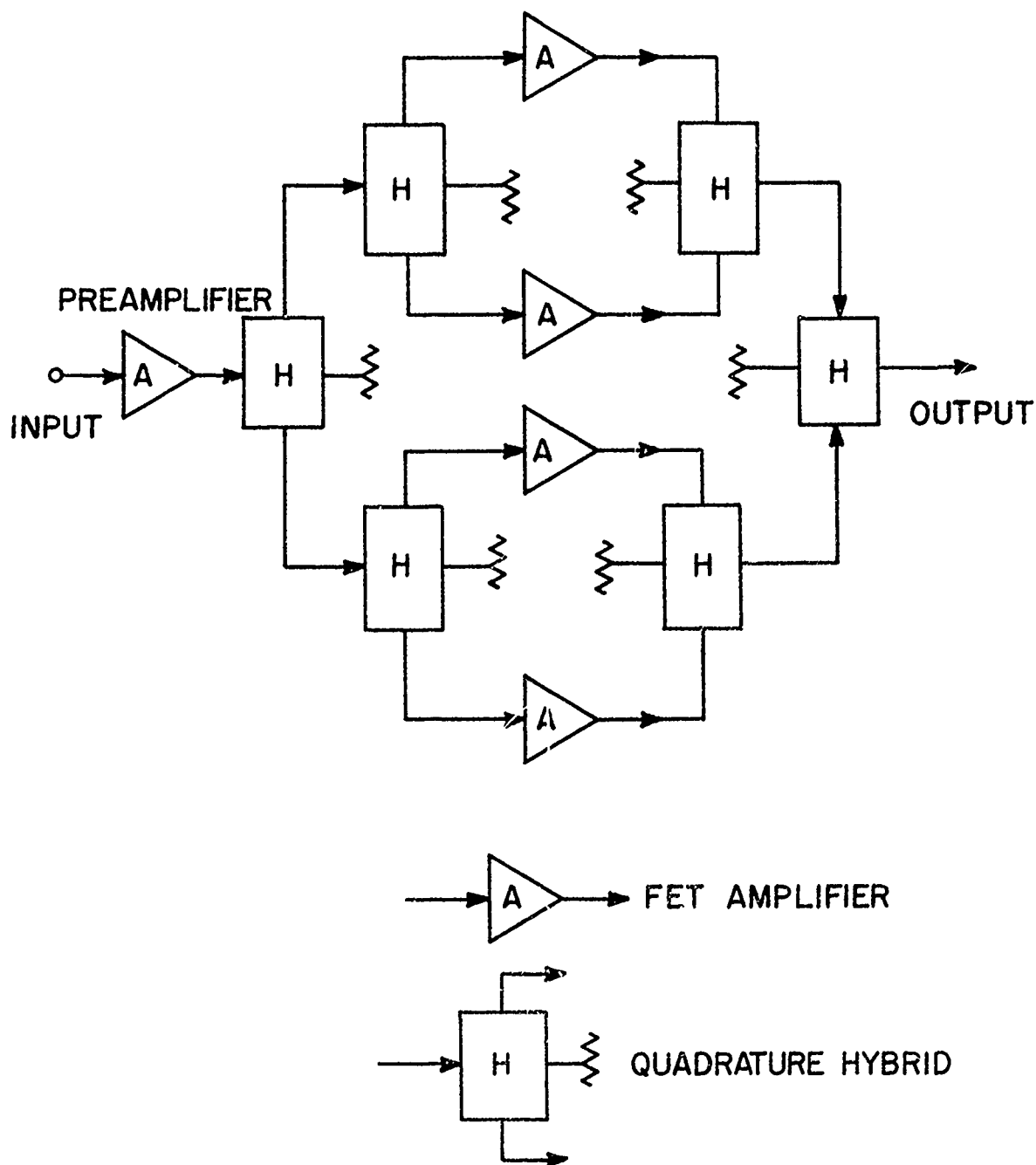


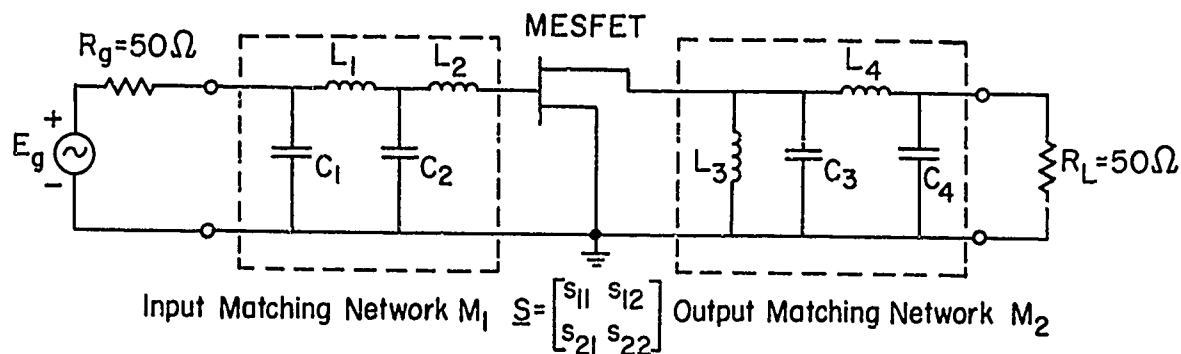
Figure 1.

Typical single-stage lumped and distributed FET amplifier modules are presented in Figure 2.

2.1 FET Amplifier Design Using a Medium-Power RCA GaAs FET

Recently, RCA Laboratories have reported on medium-power GaAs MESFETs with output power of 1W at 9 GHz with power added efficiency of 16% (linear gain of 5.5 dB) from a single MESFET pellet.¹ Power added efficiencies of 35% at 4 GHz and 21% at 9 GHz have also been reported by RCA. Using a single 1-cell RCA MESFET, an amplifier covering 7.25-7.75 GHz has been presented¹ with a gain of 6.5 ± 0.5 dB and an output power of 130 mW at 1 dB gain compression at 7.5 GHz. In a balanced amplifier configuration, an output of 260 mW was obtained with a 10% power-added efficiency. A high-efficiency balanced amplifier for the same frequency band has been reported with an output power of 1.02W at 1 dB gain compression with 37% power added efficiency. The small-signal gain was 6.65 ± 0.45 dB.²

Based on the measured scattering parameters of packaged RCA MESFET³ presented in Table 1, the stability factor K , maximum available gain (MAG), and unilateral gain G_U of this device have been calculated (Table 2). The amplifier configuration used is similar to the distributed design shown in Figure 2(b). The optimized amplifier response is tabulated in Table 3. The preliminary design presented demonstrated



$$C_1 = 0.476 \text{ pF}$$

$$L_1 = 0.935 \text{ nH}$$

$$C_2 = 2.150 \text{ pF}$$

$$L_2 = 0.126 \text{ nH}$$

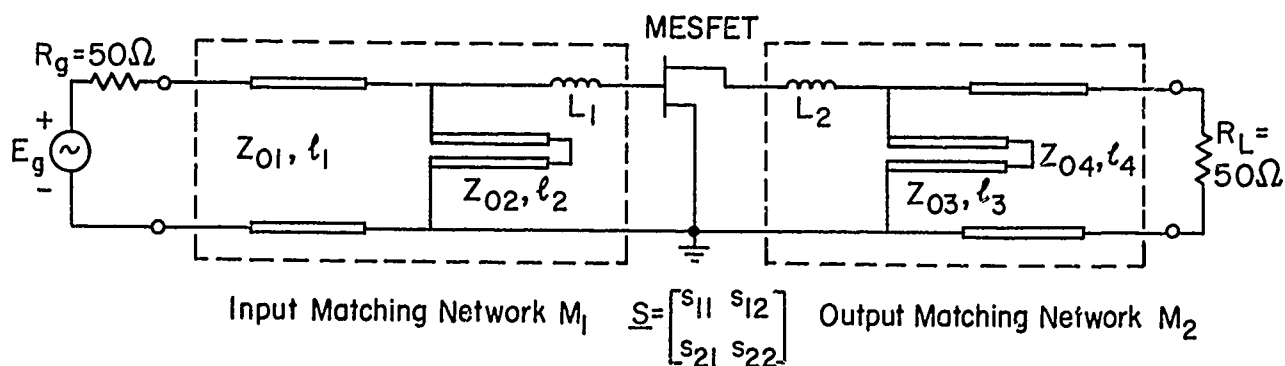
$$L_3 = 0.396 \text{ nH}$$

$$C_3 = 0.035 \text{ pF}$$

$$L_4 = 0.699 \text{ nH}$$

$$C_4 = 0.476 \text{ pF}$$

(a) LUMPED DESIGN



(b) DISTRIBUTED DESIGN

Figure 2

TABLE 1
MEASURED SCATTERING PARAMETERS OF PACKAGED RCA MESFET

FREQ. (GHz)	$ s_{11} $	$\angle s_{11}^\circ$	$ s_{21} $	$\angle s_{21}^\circ$	$ s_{12} $	$\angle s_{12}^\circ$	$ s_{22} $	$\angle s_{22}^\circ$
4	0.819	-161	2.453	+48	0.058	-14	-.653	-66
5	0.820	+167	1.910	+16	0.051	-38	0.561	-96
6	0.816	+158	1.668	-3	0.053	-43	0.644	-115
7	0.735	+117	1.698	-34	0.057	-71	0.563	-133
8	0.830	+81	1.285	-70	0.049	-107	0.411	+170

TABLE 2
STABILITY FACTOR (K), MAXIMUM AVAILABLE GAIN (MAG),
AND UNILATERAL GAIN (G_U) OF PACKAGED RCA MESFET

FREQ. (GHz)	K	MAG (dB)	G_U (dB)
4	0.818	---	15.03
5	1.225	12.87	12.11
6	1.141	12.69	11.53
7	1.664	9.98	9.63
8	1.967	8.58	8.05

TABLE 3

OPTIMIZED GAIN RESPONSE OF FET
AMPLIFIER USING A PACKAGED RCA MESFET

FREQ (GHz)	OPTIMIZED GAIN (dB)
7.0	7.73
7.1	7.91
7.2	8.02
7.3	8.08
7.4	8.14
7.5	8.20
7.6	8.22
7.7	8.19
7.8	8.04
7.9	7.72
8.0	7.18

that preamplifiers using medium-power (1W) FETs can be designed to have a gain of 7-8 dB covering the 7.25 - 7.75 GHz band.

3.1 FET Amplifier Design Using a High-Power Fujitsu GaAs FET

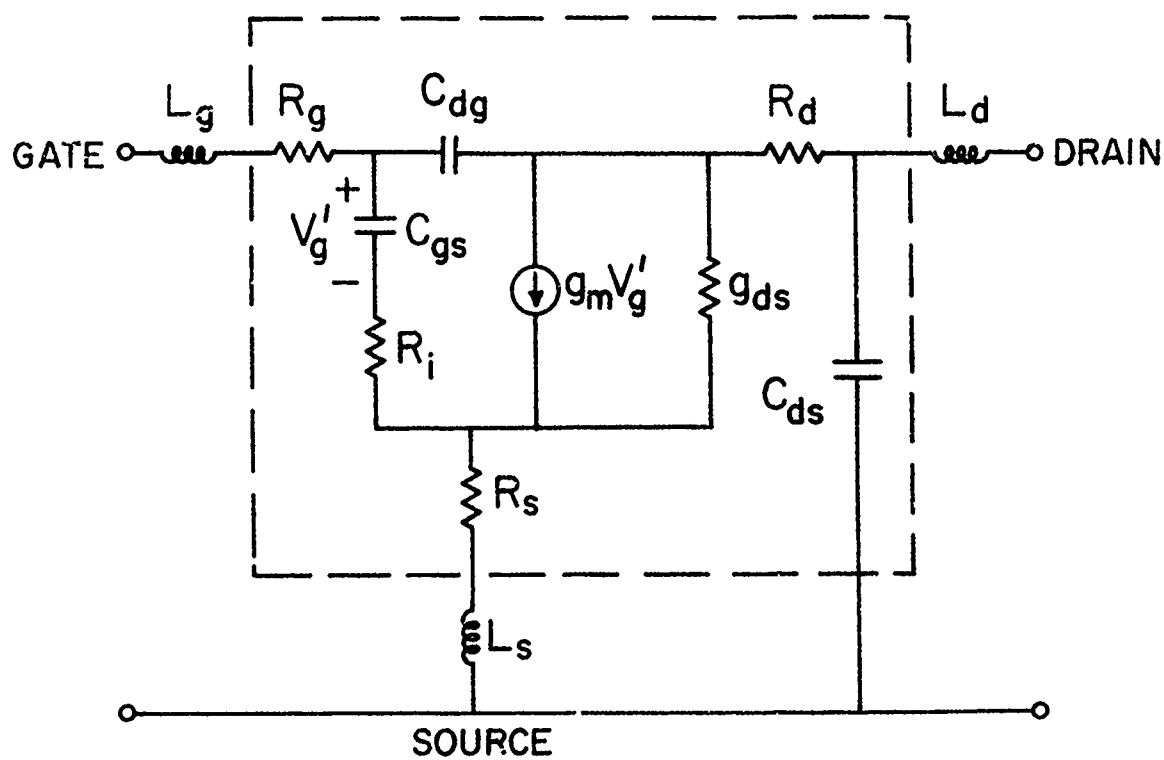
Fujitsu announced recently a high-power GaAs MESFET with a 2.2W output power at 1 dB gain compression with 4.2 dB linear gain and 21.6% power added efficiency at 8 GHz.⁴ A commercially available state-of-the-art device from Fujitsu, FLC 30, is capable of 1.9W at 8 GHz with 4dB gain and 24% power added efficiency.

Using an equivalent circuit as shown in Figure 3, Fukata derived the following parameters for the Fujitsu MESFET:

$g_m = 240 \text{ m}\Omega$	$C_{gs} = 6 \text{ pF}$
$G_D = 20 \text{ m}\Omega$	$C_{dg} = 0.3 \text{ pF}$
$R_i = 1.5\Omega$	$C_{ds} = 0.8 \text{ pF}$
$R_s = 0.5\Omega$	$L_g = 0.12 \text{ nH}$
$R_D = 0.8\Omega$	$L_s = 50 \text{ pH}$
	$L_d = 0.1 \text{ nH}$

The corresponding scattering parameters from 7 to 8 GHz are listed in Table 4 and the calculated K, MAG, and G_U are presented in Table 5 and Figure 4.

A lumped FET amplifier using the Fujitsu FET has been designed. The element values of the matching networks are



SMALL-SIGNAL GaAs MESFET MODEL

Figure 3.

TABLE 4
CALCULATED SCATTERING PARAMETERS OF FUJITSU GaAs FET

FREQ. (GHz)	$ s_{11} $	$\angle s_{11}^\circ$	$ s_{21} $	$\angle s_{21}^\circ$	$ s_{12} $	$\angle s_{12}^\circ$	$ s_{22} $	$\angle s_{22}^\circ$
7.0	0.8749	170.03	0.5221	32.73	0.0547	14.55	0.6762	-154.90
7.1	0.8748	169.69	0.513	32.07	0.0549	14.55	0.6808	-155.29
7.2	0.8746	169.36	0.504	31.41	0.0551	14.56	0.685	-155.68
7.3	0.8744	169.03	0.496	30.77	0.0553	14.56	0.690	-156.07
7.4	0.8743	168.71	0.487	30.13	0.0555	14.57	0.694	-156.46
7.5	0.8741	168.38	0.478	29.49	0.0557	14.57	0.698	-156.84
7.6	0.8740	168.06	0.471	28.87	0.0559	14.57	0.703	-157.22
7.7	0.8738	167.74	0.464	28.26	0.0561	14.57	0.707	-157.61
7.8	0.8736	167.43	0.456	27.65	0.0563	14.57	0.711	-157.99
7.9	0.8735	167.11	0.449	27.05	0.0565	14.57	0.715	-158.37
8.0	0.8733	166.80	0.442	26.56	0.0567	14.56	0.718	-158.75

TABLE 5
STABILITY FACTOR (K), MAXIMUM AVAILABLE GAIN
(MAG), AND UNILATERAL GAIN (G_U) OF FUJITSU
GaAs FET

FREQ. (GHz)	K	MAG (dB)	G_U (dB)
7.0	1.74	4.79	3.31
7.1	1.75	4.69	3.20
7.2	1.75	4.58	3.09
7.3	1.76	4.47	2.99
7.4	1.76	4.37	2.89
7.5	1.76	4.27	2.79
7.6	1.77	4.18	2.69
7.7	1.77	4.08	2.59
7.8	1.77	3.99	2.49
7.9	1.77	3.90	2.40
8.0	1.78	3.81	2.31

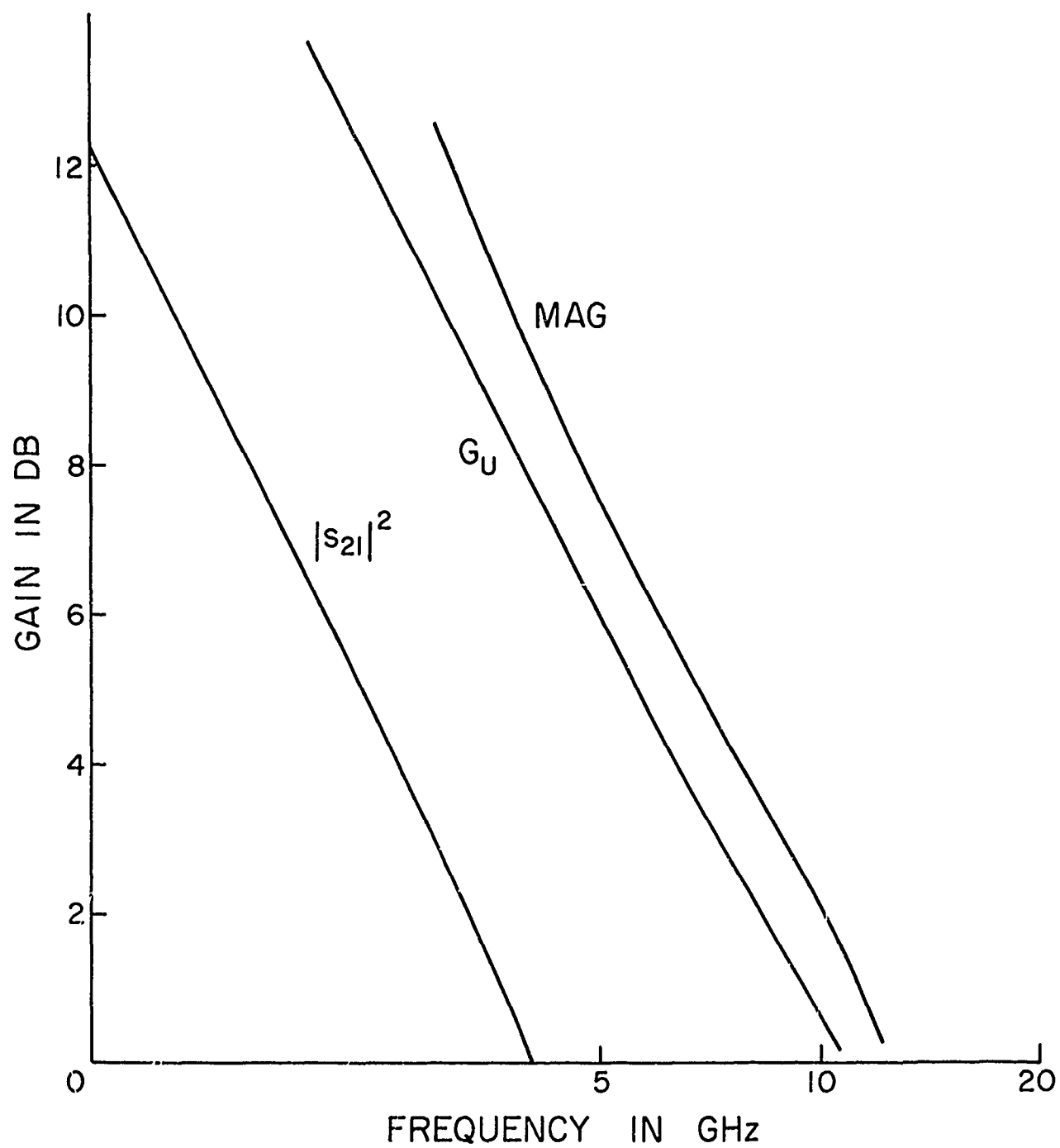


Figure 4

listed in Figure 2(a). The optimized gain response is listed in Table 6 and plotted in Figure 5. This design has also been converted to a distributed realization using cascaded lines and open- and short-circuited shunt stubs. Over the 7-8 GHz band, the amplifier response is flat with 3.75 ± 0.1 dB. The input and output VSWR are less than 2.65:1 and 1.47:1 respectively. The optimized distributed-parameter FET amplifier is shown in Figure 5'.

TABLE 6

OPTIMIZED GAIN RESPONSE OF FET
AMPLIFIER USING A FUJITSU GaAs FET

FREQ. (GHz)	OPTIMIZED GAIN (dB)
7.0	3.71
7.1	3.74
7.2	3.78
7.3	3.80
7.4	3.82
7.5	3.84
7.6	3.85
7.7	3.83
7.8	3.80
7.9	3.74
8.0	3.64

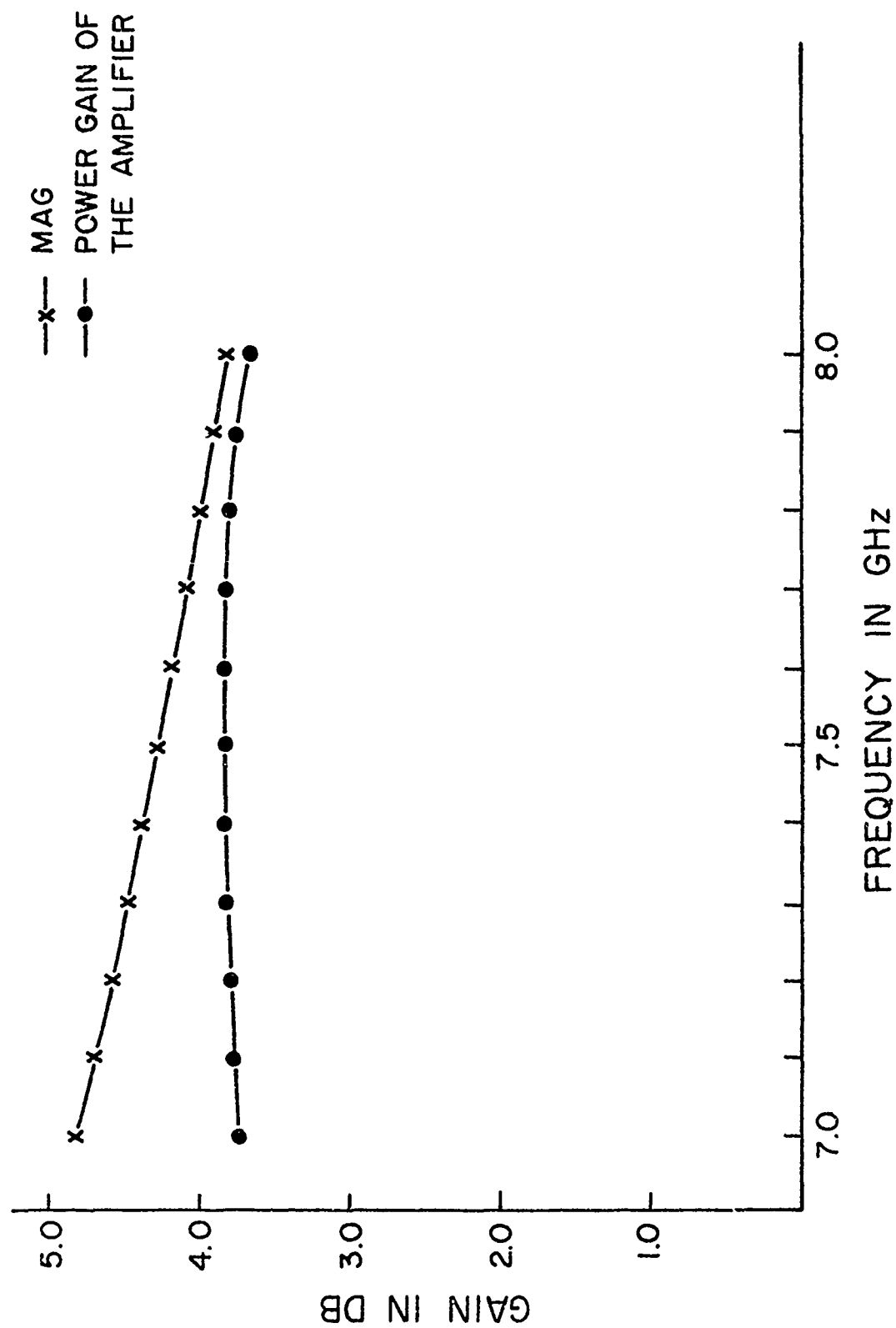
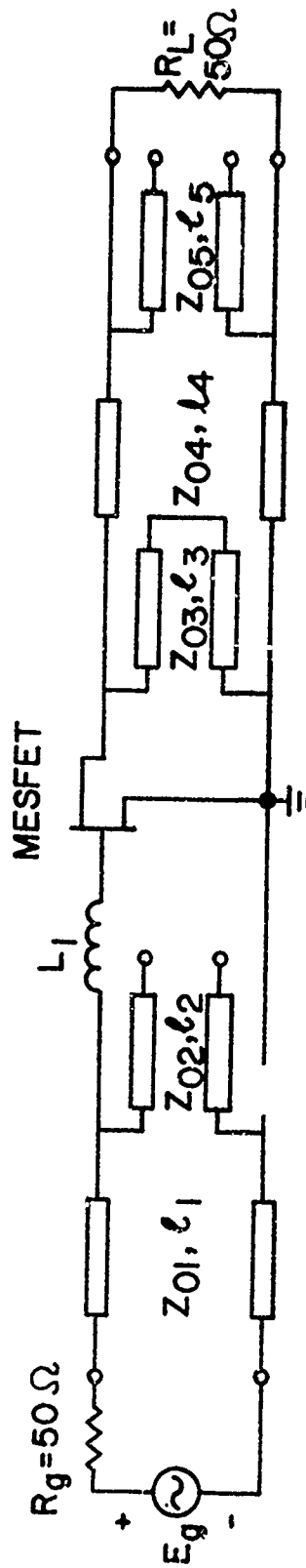


Figure 5.



$$Z_{01} = 25.4 \Omega, \ell_1 = 0.78 \text{ cm}$$

$$Z_{02} = 13.9 \Omega, \ell_2 = 0.58 \text{ cm}$$

$$L_1 = 0.024 \text{ nH}$$

$$Z_{03} = 30.0 \Omega, \ell_3 = 0.38 \text{ cm}$$

$$Z_{04} = 99.8 \Omega, \ell_4 = 0.21 \text{ cm}$$

$$Z_{05} = 48.1 \Omega, \ell_5 = 0.55 \text{ cm}$$

Figure 5'.

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III. Nonlinear Models of FETs

At low frequencies nonlinear distortion in FET amplifiers has been investigated based on a power series approach which is valid only for a zero memory nonlinearity. This assumption is incorrect at higher frequencies and must be deleted to obtain accurate results.

A method of eliminating this restriction is to develop device models including nonlinear resistance and reactances, and then use these to predict amplifier distortion. Hickman and Hodges¹ developed such a model, which is incorporated (with slight changes) in the circuit analysis program SPICE².

The DC characteristics of the model are defined by the parameters V_{TO} and β , which determine the variation of drain current with gate voltage, λ , which determines the output conductance and is the saturation of the two gate junctions. Two ohmic resistances, R_D and R_S , are included. Charge storage is modeled by the nonlinear depletion layer capacitances for both gate junctions which vary as the $-1/2$ power of junction voltage and are defined by the parameters C_{GS} , C_{GD} , and the gate junction potential ϕ_B . The parameters in the JFET model are listed as follows:

V_{TO}	Threshold voltage
β	Transconductance parameter
λ	Channel length modulation parameter
R_D	Drain ohmic resistance
R_S	Source of ohmic resistance
C_{GS}	Zero bias gate-source junction capacitance
C_{GD}	Zero bias gate-drain junction capacitance

ϕ_B Gate junction potential
 I_S Gate junction saturation current.

In this model the two parasitic ohmic resistances, R_D and R_S , are assumed to be constant. The equation for internal drain current, I_D , is taken as a simple square-law relation with an added parameter to model channel width modulation.¹ The three DC parameters which determine the JFET operation are V_{TO} , β and λ . The parameter V_{TO} is commonly referred to as the "pinchoff" voltage. The output conductance is assumed to vary linearly with drain current with a constant of proportionality λ . The two gate junctions are modeled as ideal diodes. The charge storage elements, Q_{GS} and Q_{GD} are modeled as ideal step junction depletion capacitances.

The SPICE program, with its nonlinear FET model, can be used to numerically evaluate the time domain response of an amplifier. Fourier analysis can then be used to determine the harmonic response with a sine wave input. Computation must be continued long enough for the amplifiers transient response to decay, which can be quite long; however, techniques are available for reducing the amount of computation required³. If third order effects must be considered (i.e., intermodulation and cross-modulation) this technique can require large amounts of computation and can result in large numerical errors.

Miller and Meyer⁴ have developed a similar technique based on a different model of the FET. They have studied the nonlinearity and cross-modulation of FETs at frequencies up to

450 MHz on the basis of a 30 point measurement of incremental transconductance as a function of gate to source voltage, V_{GS} . The measured data was fitted by an eighth order Taylor series and integrated analytically to obtain a nonlinear relationship between the static drain current, I_D , and V_{GS} . This technique was determined to be more accurate than direct measurement, and even fifth order terms had a significant effect on the calculated amplifier response.

Figure 2 shows the nonlinear model used by Miller and Meyer. The drain current depends on the gate voltage according to the nonlinear relationship $I_D = f(V_G)$ where f is determined experimentally. The gate to source capacitance, $C_{GS}(V_G)$, was experimentally determined to be of the form $C_{GS}(V_{GS}) = C_{GS}(0)(1+bV_G)$, where $C_{GS}(0)$ and b are constants. The source resistance, R_S , and the gate to drain capacitance, C_{GD} , were assumed to be constant. Again nonlinear distortion effects were studied by Fourier analyzing the time domain response.

Recently, Khadr and Johnston⁵ developed a more accurate nonlinear model of the FET. In their model, shown in Figure 7, I_D and C_{GS} are determined from the DC device theory and then expanded in a Taylor series around the bias point of the transistor. In addition, C_{GD} and the drain resistance, R_D , are considered to be nonlinear elements which must be experimentally determined. All Taylor series were truncated

after the cubic term, but the same techniques would apply if higher orders were retained.

Unlike the previous cases, nonlinear distortion was studied in the frequency domain by first calculating the linear response and then using this to determine the value of the second order sources. The linear and second order response can then be used to determine the third order sources. The process is based on the assumption that the nonlinear effects are small, but appears to be valid at larger power levels as well. The authors suggest that larger signal levels could be used if approximation techniques other than Taylor series are used to obtain the truncated series expansion, such as averaging of several Taylor series.

The distortion analysis technique used by Khadr and Johnston is equivalent to deriving a Volterra expansion from their model and applying it to the nonlinear analysis. The modeling approach is more feasible than direct measurement of the Volterra transfer functions due to the large amount of data that would be needed from direct measurement. The model also gives more insight into the causes of the nonlinear effects, and therefore is more useful in attempting to reduce the distortion.

Based on the Volterra nonlinear transfer functions, amplifier distortion is easily calculated⁶. If an input signal to the amplifier is assumed to be of the form

$$V_{in} = V \cos \omega_1 t + V \cos \omega_2 t$$

in which ω_1 and ω_2 are assumed to be incommensurate, then the magnitude of the third-order intermodulation distortion (IMD) at frequencies $2f_1 - f_2$ and $2f_2 - f_1$ in dB is

$$D_{IM3} = 20 \log \left[\frac{3}{4} \frac{|H_3(j\omega_1, j\omega_2, -j\omega_2)|}{|H_1(j\omega_1)|} V^2 \right] \text{dB},$$

where $H_n(j\omega_1, j\omega_2, \dots, j\omega_n)$ is the n^{th} order Volterra kernel. Cross-modulation distortion (CMD) can also be calculated. Assume the input signal to the FET amplifier is of the form $V_{in} = V_1 \cos \omega_1 t + V_c (1+m \cos \omega_m t) \cos \omega_c t$. The desired output signal of the amplifier at ω_1 is modulated by the modulating frequency of the spurious AM signal, and the resulting output signal is either an AM signal, a PM signal, or a combination of both. The output signal is given by

$$V_{out} = |H_1(j\omega_1)| V_1 [1 + K \cos \theta \cos \omega_m t] \cos(\omega_1 t + \gamma + K \sin \phi \cos \omega_m t).$$

In this expression, H_1 is the first order Volterra kernel and K can be expressed in terms of H_1 and H_3 as

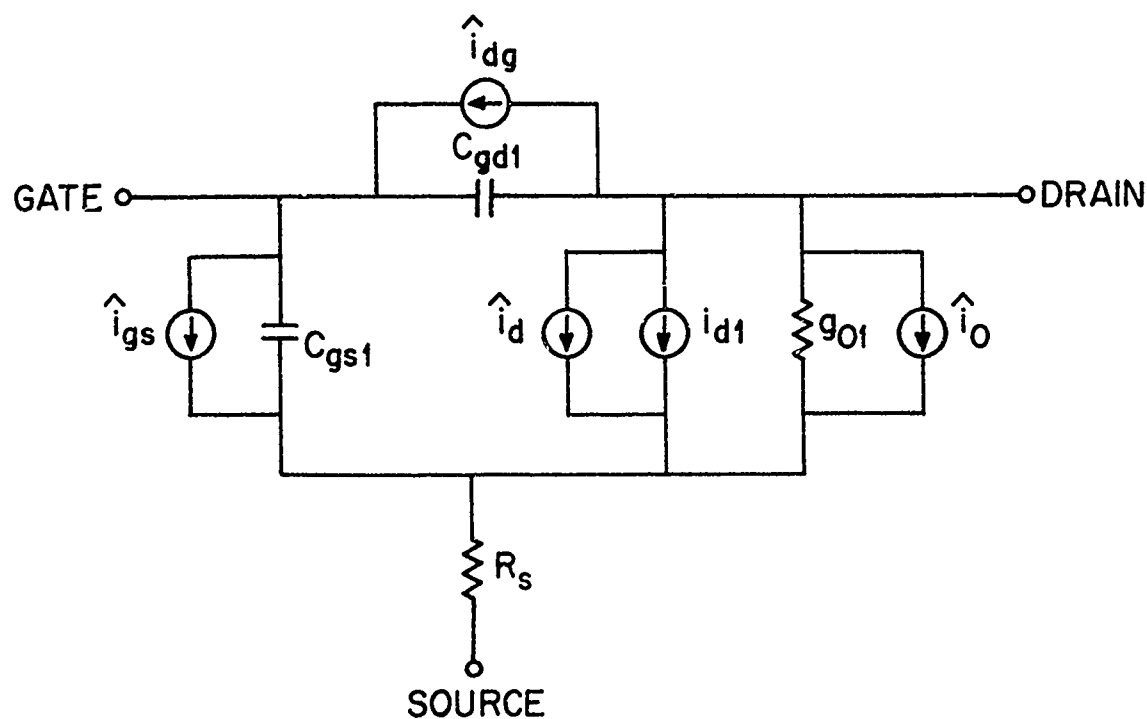
$$K = 3mV_c \frac{|H_3(j\omega_c, -j\omega_c, j\omega_1)|}{|H_1(j\omega_1)|}$$

with an added parameter to model channel width modulation.¹ The three DC parameters which determine the JFET operation are V_{T0} , β and λ . The parameter V_{T0} is commonly referred to

as the "pinchoff" voltage. The output conductance is assumed to vary linearly with drain current with a constant of proportionality λ . The two gate junctions are modeled as ideal diodes. The charge storage elements, Q_{GS} and Q_{GD} are modeled as ideal step junction depletion capacitances.

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SIMPLIFIED NONLINEAR FET MODEL

Figure 7.

Intermodulation Characteristics of GaAs FET Amplifiers

The nonlinear models of FET have been briefly discussed in the previous subsections. In order to use the existing computer program such as SPICE, the FET parameters must be known through measurements and device parameters. At present these are not available and a few trial runs of the program have consistently lead to intermodulation results which are much smaller than published results. This is partly due to the assumption that the nonlinear distortion terms are small and superposition of nonlinear contribution is valid.

Measured results by Hewlett Packard, TI, and Fujitsu have shown that the dominating third-order intermodulation products are of the order of 20-25 dB at 1 dB gain compression point. However, a recent paper presented by Franco Sechi at the 1976 ISSCC has shown that the C/I ratio could be as high as 15 dB at a power output of 700 mW and 10% power added efficiency at 4.6 GHz.

A representative third-order intermodulation characteristic for a packaged GaAs FET measured at L-band by Allen Podell of Hewlett-Packard is shown in Figure 8. Similar devices have been used in two amplifiers fabricated at Cornell University covering the 4-8 GHz band. It is planned to measure the IM characteristics of these amplifiers for 7-8 GHz and refine the nonlinear FET models to correlate the measured

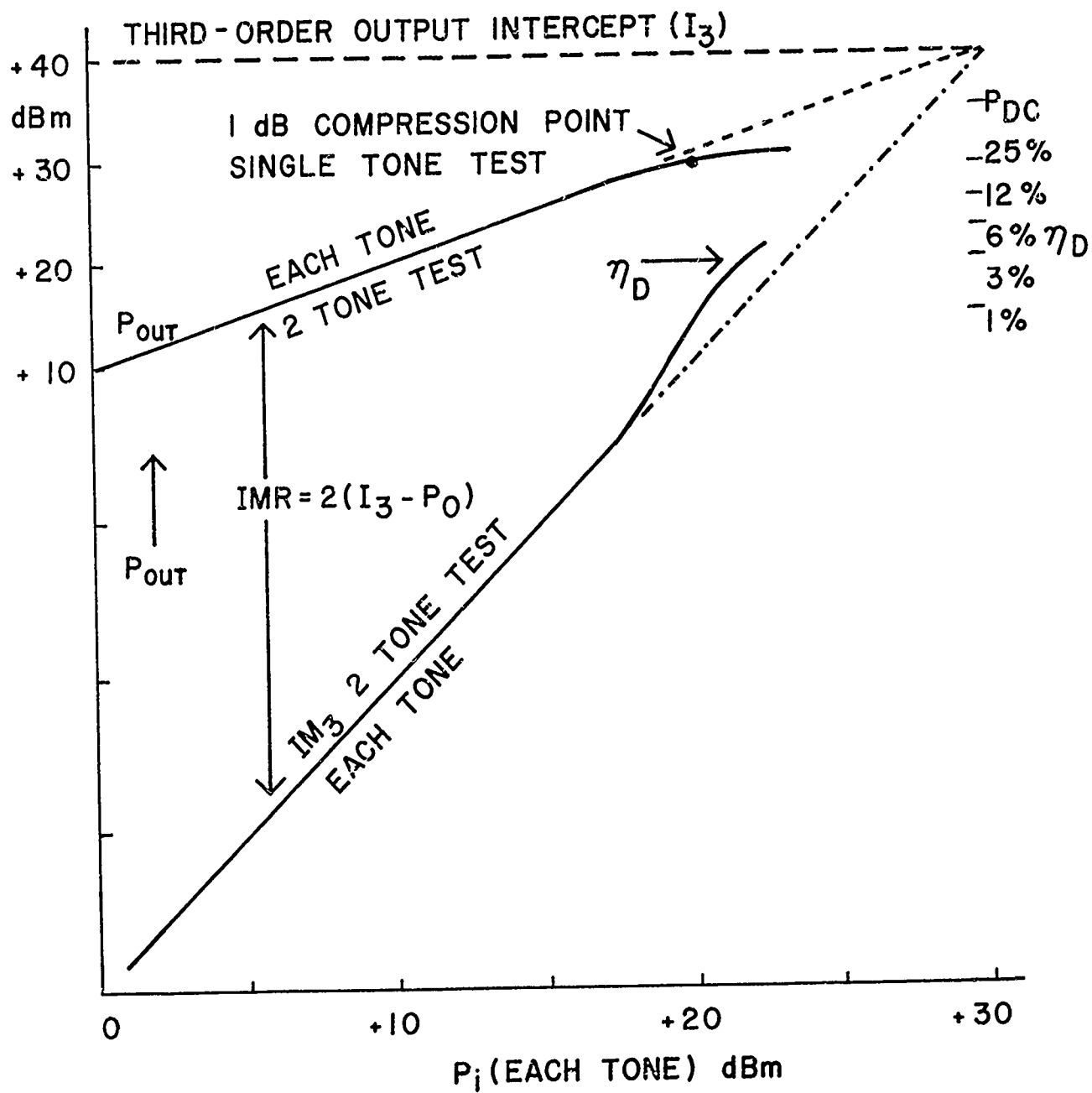


Figure 8

results. Circuit techniques such as feedback and feedforward will be investigated for possible reduction of nonlinear distortions.

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- Figure 5 Optimized gain-response of FET amplifier using a Fujitsu MESFET.
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SECTION D
HIGH POWER FET TECHNOLOGY LIMITS
by
L. F. Eastman

I. INTRODUCTION

In order to obtain 10W of output power from an FET amplifier with low nonlinearity, high efficiency and high reliability, it will be necessary to obtain 5W per device from each of two devices. The power from these two devices can be combined in a hybrid with good efficiency without too much trouble from impedance matching networks.

In order to obtain 5W per device, it will be necessary to obtain 1W per millimeter of gate width, in order not to have too low an input impedance level and not to have too much efficiency lost in the device. To date, up to .78W per millimeter gate width has been obtained at 8 GHz for 2.4mm gate widths and .52W per millimeter at 8 GHz for 4.8mm gate widths.¹ The efficiency levels were 39% and 25% respectively and 2μ gate lengths were used. Gain was 4dB.

The nonlinearity of power FET devices is already very low, with (-) 20dB intermodulation products at 30% power-added efficiency with about 1dB gain compression².

The remainder of this contribution covers the key technology limits for high power, high efficiency, low nonlinearity, reliable FET devices. Suggestions for development efforts to improve these limits are also made, and the full

specifications could be repeatably met in about 3 years if these efforts are pursued. Areas covered are: the active layer properties, including the doping profile for linearity improvement; the buffer layer, including impurity type for best performance; the contacts needed, including their geometry relative to the channels for high bias voltage operation; and finally a summary of the overall means of obtaining the desired performance.

II. ACTIVE LAYER

The active channel layer must have high performance. The mobility profile and doping profile can be measured and related to device performance. For $1 \times 10^{17}/\text{cm}^3$ net donor density a mobility of about $5,000 \text{ cm}^2/\text{v-s}$ is expected. If this mobility drops off severely near the interface with the substrate, device gain and efficiency suffers. If deep donors are present in the active layer, they become ionized at high bias fields causing noise and other problems. Using buffer layers as described in the next section, epitaxially grown just before the active layer, it is often possible to eliminate most of these problems. In addition, excess conductivity and breakdown that can occur just inside the semi-insulating substrate will be electrically insulated from the active layer by such a buffer layer.

When there is the usual uniform electron concentration in the active channel in the direction of epitaxial growth, there are nonlinearities in the device operation. The channel (drain) current is reduced from its full value by an amount proportional to the gate depletion distance. This depletion distance is proportional to the square root of the sum of the gate bias plus the gate metal barrier voltage. For aluminum gates, this barrier voltage is about 70-.80 volts. The depletion capacitance of the gate is reciprocally proportional to the depletion distance. Thus the device drain current drops in a nonlinear, concave manner with increasing gate bias voltage magnitude. Since the gate capacitance also varies in a nonlinear manner, neither the input impedance nor the output alternating current is linear with microwave input drive voltage magnitude. There would be a more linear relation between an input alternating current, from a current source, and an output alternating current, but such a mismatch condition would reduce power gain.

It has been proposed^{3,4} that a more heavily doped active channel be covered with a more lightly doped layer for improved device performance. This especially improves the device linearity, but might increase the gate bias voltage amplitude requirement, unless the total thickness of the above two layers is about half as thick as the usual uniformly doped layer. Figure 1 shows the variation of device current with bias voltage for an ordinary, uniformly doped channel (A).

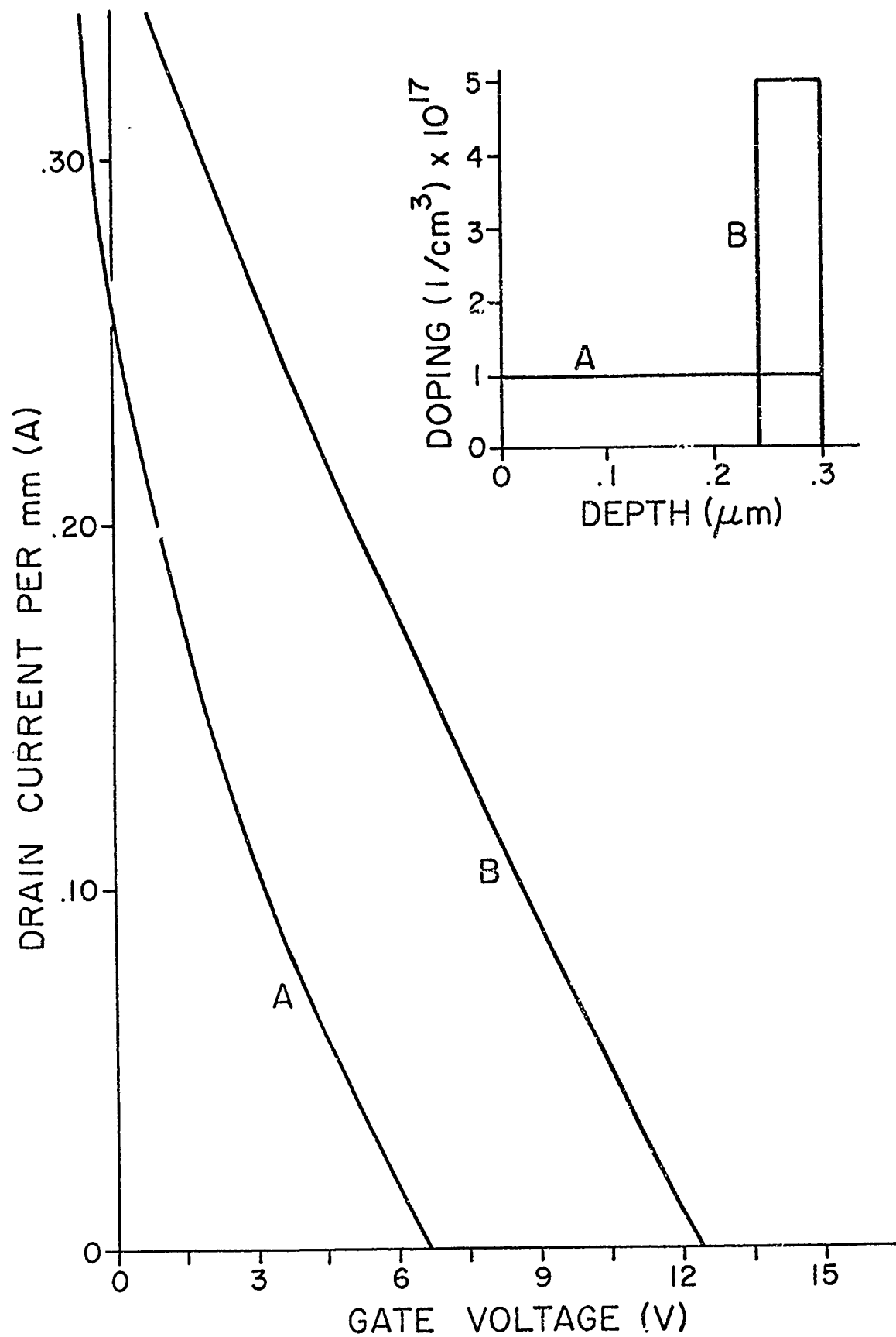


Figure 1

It also shows the increased linearity of a thin buried channel covered with an undoped layer (B). Both curves represent channels with $3 \times 10^{12}/\text{cm}^2$ product of N times thickness. Over the full channel current swing there is now a 10:1 or more reduction of intermodulation products, if clipping of the current wave shape is avoided. Such a buried channel geometry would also "passivate" the surface against spurious conduction or breakdown at high bias voltage levels. Such a profile has not been tried and may not yet be optimum for best device all around performance, so the development of an optimized profile needs to be pursued, especially for linearity.

III BUFFER LAYER

If a high-resistivity buffer layer is grown just before an active FET channel is grown, many improvements are possible. The most important improvement is the elimination of the thin conduction layer, caused by "conversion" of that surface portion of the substrate during baking in hydrogen just before epitaxial growth. The conversion varies from one semi-insulating substrate to another, but always occurs due to the deviation from stoichiometry, caused by the diffusion of vacancies, and due to fast impurity diffusion in the region where these vacancies occur. Such a converted layer not only causes anomalous conduction, but also has a

high-field breakdown and causes a drift of device parameter values with time during operation.

The properties of a high resistivity buffer layer can also be much better than those of semi-insulating substrate. For example chrome-doped semi-insulating substrates have electron mobility values well below $5,000 \text{ cm}^2/\text{v-s}$ compared to $9,000 \text{ cm}^2/\text{v-s}$ or more for high purity buffer layers. In addition, high resistivity buffer layers that are very pure, with little or no chromium added, have no deep levels to easily ionize with high electric fields near the active channel or with high operating temperature. The fact that an epitaxial buffer layer can be grown just seconds before the active channel also prevents any surface layer degradation or conversion.

It is presently possible to grow N or P type buffer layers at or below $1 \times 10^{14}/\text{cm}^3$ net carriers, without closely compensating impurities, by liquid phase epitaxy (LPE) and it is easiest to grow N type buffers with such carrier densities by vapor phase epitaxy (VPE). Such N type layers would not have less than about $150,000 \text{ cm}^2/\text{v-s}$ mobility at 77°K . In LPE it now requires about 24 hrs baking time at 700°C , after exposure of the melt to air, to get such results. This in turn causes conversion of any substrate necessarily present during this bake. LPE can easily allow 5 or $10\mu\text{m}$ thickness

for such a buffer layer to insulate the active channel from the converted surface of the substrate. In VPE it has been occasionally possible to make 3-5 μ m thickness buffer layers that are more closely compensated so that the net shallow donor density is at or below $2 \times 10^{13}/\text{cm}^3$. The growth condition (increase of the mole fraction of arsenic trichloride) has been used to cause this close compensation, but the process is far from being reproducible and is highly dependent on the substrate chemistry.

In both LPE and VPE it has been possible to get 250,000 $\text{cm}^2/\text{v-s}$ mobility at 77°K under research laboratory conditions not yet readily reproduced in device form. Such N type layers have less than $1 \times 10^{13}/\text{cm}^3$ net donors and are not closely compensated. In the future, buffer layers must be developed that reproducibly yield carrier densities in the low $10^{13}/\text{cm}^3$ range or less. It would also be much more useful to have a shorter melt bake time each run in LPE. It is suggested that such a technology be pursued in order to give reproducible, high performance buffer layers for FET devices.

It is possible to use chromium doping in lightly doped N type buffer layers to get resistivity levels exceeding $10^6 \Omega \text{ cm}$ by either LPE or VPE. In LPE it might still require long bake times to lower the donor density each run. In VPE such chromium doping is possible but is not repeatable

run after run. In addition to all this, the electrons trapped by the chromium, to make high resistivity material, are freed by electric fields much lower in magnitude than those required for the usual avalanche process. Increased noise and other problems would result from such use of chromium.

One other possibility for increasing buffer resistivity and reducing output circuit conductance, is by making the buffer layer very lightly P type. The mobility of holes is only about 4% of that for electrons, raising the resistivity. In addition, a few microns of such a P type buffer layer would be depleted, especially under the drain, removing the conductivity from that portion of the buffer.

CONTACT AND CHANNEL GEOMETRY

The channel maximum current in FET devices is limited by the high field velocity ($.8 \times 10^7$ cm/s in GaAs) and the product of donor concentration times channel thickness ($N \times T$). The value of $N \times T$ product that is commonly used is 3×10^{12} /cm². Values a little higher than this can be used, if needed, but higher values of gate pinch-off voltage are required, and these values would approach the gate bias voltage at which avalanche breakdown would occur. The channel maximum current, obtained when the gate is forward biased an amount equal to the Schottky-barrier voltage (.70-.80V for aluminum on GaAs)

is about .384A for each millimeter of gate width at room temperature. This value drops .11%/°C as the temperatures rises. In order to get maximum nearly-sinusoidal current swing, the dc bias would be .192A/mm at room temperature and the peak value of the alternating current would also be .192A/mm. In order to get 1W/mm output power with 3.5W/mm input power, the drain-source alternating voltage needs a peak value of at least 10.4V with up to 18.2V D.C. bias at room temperature. It would be expected, however, that about a 10% drop in channel current would result from self heating, so in operation, .175A/mm D.C. bias and peak A.C. current would result. Thus 11.5V A.C. or more and 20V D.C. bias voltage are required, yielding a maximum instantaneous voltage of at least 31.5V.

There is a minimum value of instantaneous voltage required to keep the maximum channel current. This "saturation" voltage is 3,500 V/cm times the channel length, approximately, being about 2.0-2.5V for a 6 μ m channel.

There is a maximum instantaneous voltage in the channel also. This voltage is the value that causes too high an electric field at the drain contact and thus causes high drain current due to a hole injecting avalanche breakdown at this contact at some isolated spot along the channel. This breakdown voltage, and the degradation of the device at such a breakdown, are critically dependent on the type of contact and

its geometry. Figure 2 shows a series of such contacts that have been used. In 2a is the usual direct alloyed metal contact on the surface of the channel. For frequencies up to 8 GHz, the gate would be about $1.5\mu\text{m}$ long. The spacing of the drain from the gate is shown to be $3\mu\text{m}$, while the spacing of the source from the gate is shown to be $1.5\mu\text{m}$. Such devices normally break down with values of instantaneous voltage, between drain and source, exceeding about 18V and easily degrade and burn out when such a breakdown occurs. In such a geometry it is nearly impossible to avoid an irregular feathered edge of nearly invisible thickness, of drain metal along the channel surface toward the gate. The high electric fields, due to current crowding at drain edge, cause localized breakdown, followed by overheating and further melting and transport of the metal.

In Figure 2b, an N^+ contact layer of GaAs has been grown and etched through at the channel location. Now the feathered metal edge of the drain contact is on the N^+ contact where very low electric fields are present. It would even be possible to recess the metal contact from the edge of the N^+ GaAs contact to prevent any metal from reaching the active channel. In this case there still is current crowding coming into the N^+ contact at the drain, but the resistivity of the N^+ contact is 1000 times higher than that of the contact metal, limiting the localized current density at any

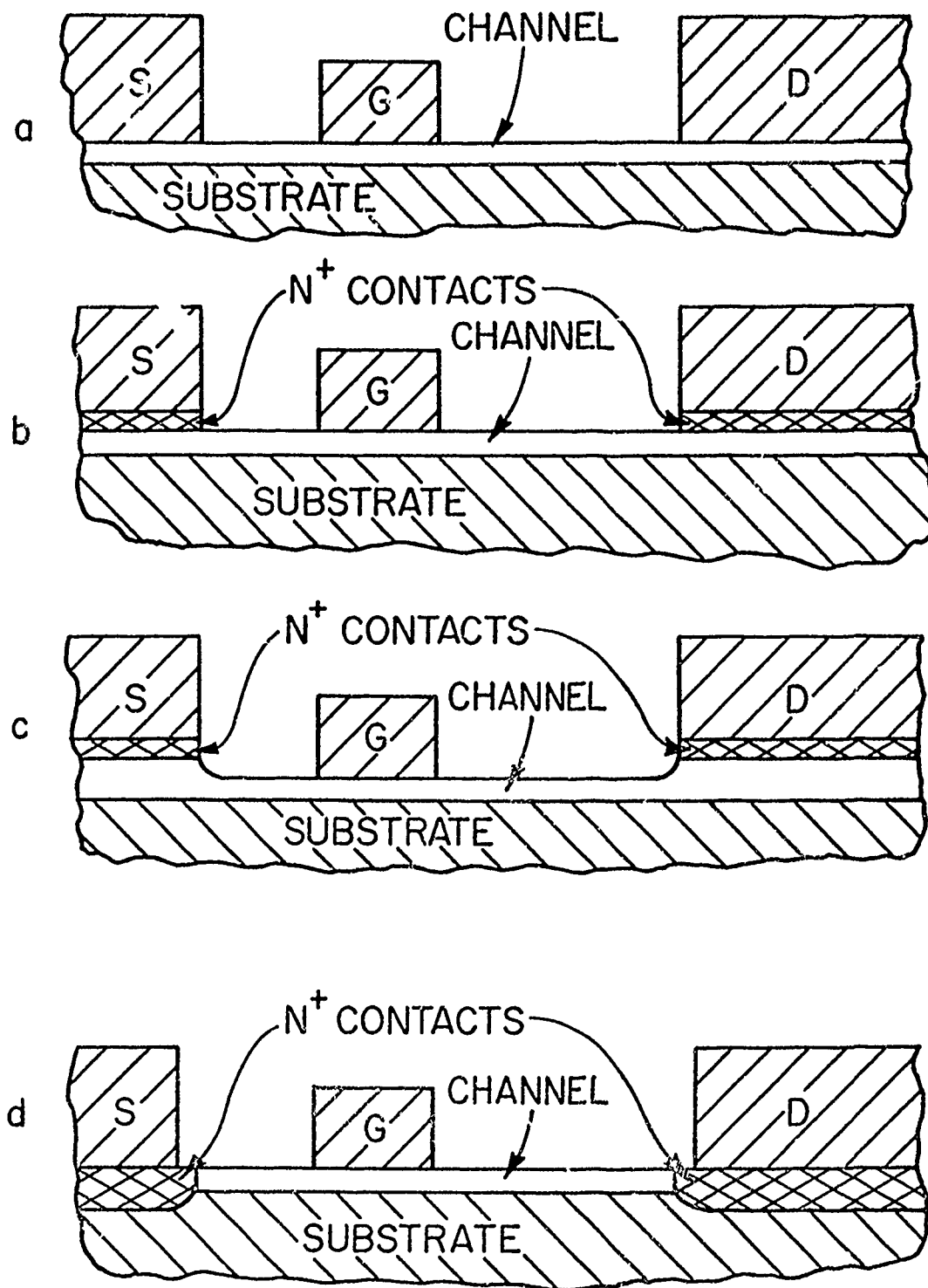


Figure 2

breakdown point, due to the resistance in the contact. Geometries like that in Figure 2b have given an average of 30V breakdown voltage⁵ and degrade much less readily. A few such devices could withstand 40V before breaking down. Thus for a 6 μ m total channel length, the geometry of 2a yields an average electric field limit of 30,000 v/cm, and for 2b an average electric field limit of 50,000v/cm.

By using a thinned channel between the N⁺ contacts, as shown in Figure 2c, fields of 50,000v/cm and greater can be withstood without breakdown. RCA⁶ has been able to get over 20V breakdown with only 1.5 μ m separation of drain and source N⁺ contacts. The amount of thinning and the shape of the flare in the channel thickness near the drain contact are both important in avoiding a breakdown condition near the drain.

Finally, Figure 2d shows buried N⁺ contacts, due to mesa etching and regrowth of the N⁺ epitaxial material by selective epitaxy. Such a technique should eliminate all current crowding at the drain and allow average channel fields up over 100,000 v/cm at breakdown. Fujitsu plans to present a paper at 1976 ISSCC using buried contacts. In that paper they plan to present data as follows: 4 GHz operation yields 2.2W for 1.3mm wide gate, and 4.0W for 2.6mm wide gate; 6 GHz operation yields 2.5W for 2.6mm wide gate;

(all at 13.5 V D.C. bias voltage and about 30% power added efficiency); and 8 GHz operation yields 2.2W at the 1db gain compression point with 21.6% power-added efficiency. Since a 3 μ m total channel length and 1 μ m gate lengths were used by Fujitsu and it can be assumed that a 1.5V saturation voltage was present, a 12V peak voltage could occur, yielding as much as 25.5V instantaneous peak voltage. This would yield 85KV/cm maximum average electric field without breakdown.

Special care may be required in the geometry of figure 2d to avoid a higher current rise and a drop back yielding Gunn oscillations.

V. SUMMARY OF MEANS OF OBTAINING POWER AT THE 10W LEVEL IN LINEAR, EFFICIENT FET AMPLIFICATION AT 7.5 GHz.

Some of the best data obtained to date at 8 GHz and above have been presented in tabular form by Texas Instruments.¹ Figure 3 is a plot of these data, showing the reduction in power-added efficiency with operating frequency for a fixed modest level of gain (4dB). The dc drain bias used was about four times the drain bias needed to saturate the drain current. The operation is not limited to class A operation, and is listed as class AB. Different gate widths, of 2400 and 4800 μ m were used. From these data, a very consistent pattern of performance can be seen. First, the maximum frequency appears to drop linearly with increasing gate width, dropping to two thirds of its value

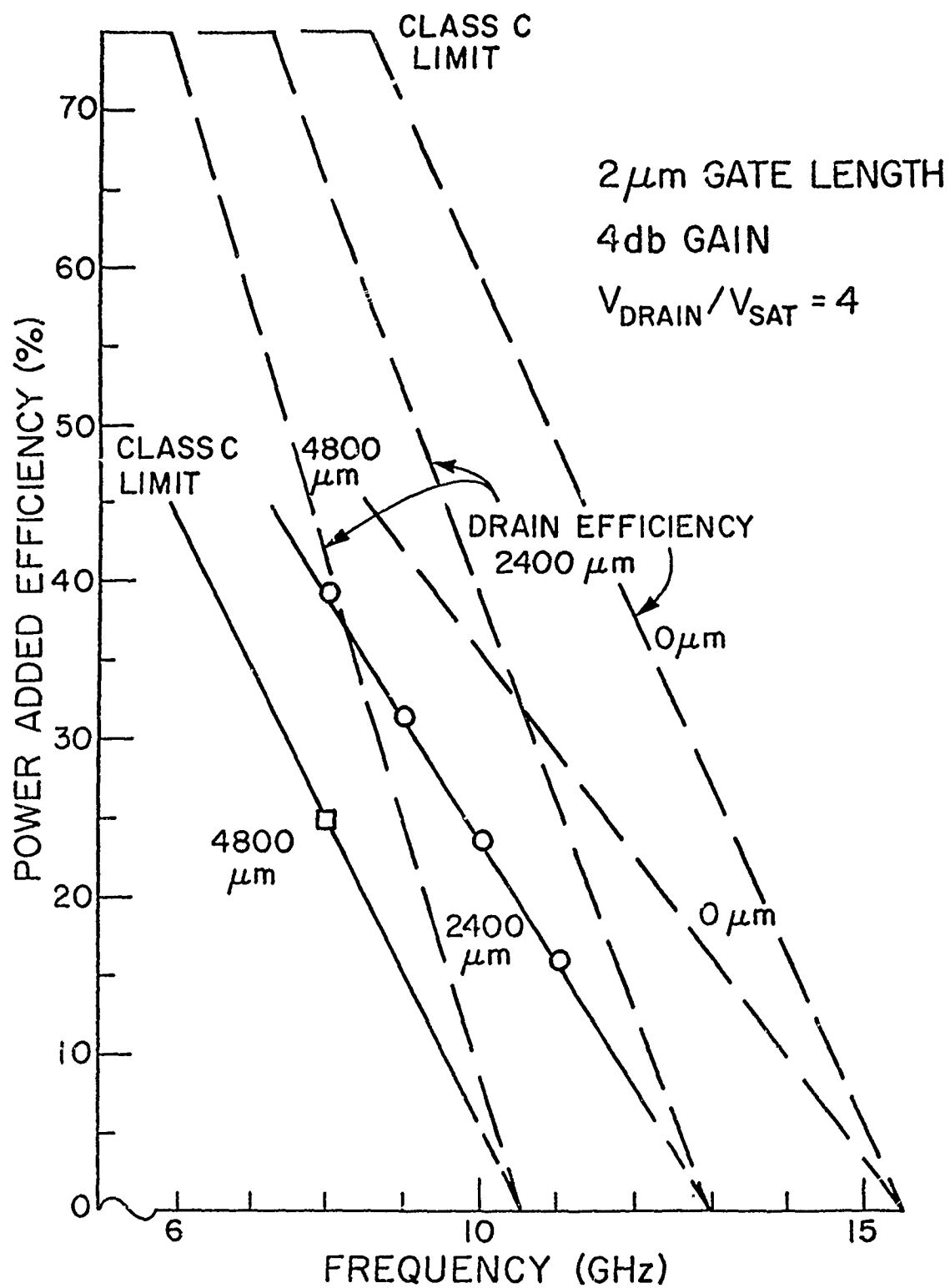


Figure 3

for negligible gate width (30 GHz), when the gate width is 4800 μm . This may depend to some degree on individual gate finger lengths, metals used, and on the wires bonded for interconnections. The drain efficiency expected is also plotted versus frequency for these cases. The theoretical upper limits, in both cases, for class C efficiency are shown for this $V_{\text{DRAIN}}/V_{\text{SAT}}=4$ value. In the Class AB case the power-added efficiency at 4dB gain seems to drop from its full value, near one quarter of maximum frequency, to zero value near one half of maximum frequency. It is expected that other classes (A, B, and C) of operation would vary similarly.

Since it is possible to calculate increases in the maximum available gain, at any frequency, if the gate length is shortened, it is possible to calculate a curve of efficiency versus frequency for higher values of gain. Such curves are shown in Figure 4 for a $V_{\text{Drain}}/V_{\text{Sat}}$ value of 8.

In experiments at Bell Laboratories using 1.5 μm gates at 6 GHz, adding gate width to 3mm total has been attempted at no loss in power output nor in power-added efficiency.⁵ Only a small decrease in gain was found. In the 8 GHz results with 1 μm gate to be reported by Fujitsu at ISSCC in February 1976, adding gate width to 5mm has been attempted, also with no loss in power output nor power-added efficiency⁷. In the Bell Laboratories experiment, 15V_{DC} bias and .270A for 3mm gate width, yielded 50% drain efficiency at 7dB gain (1dB gain compression) yielding 40% power added efficiency,⁵ at 6 GHz.

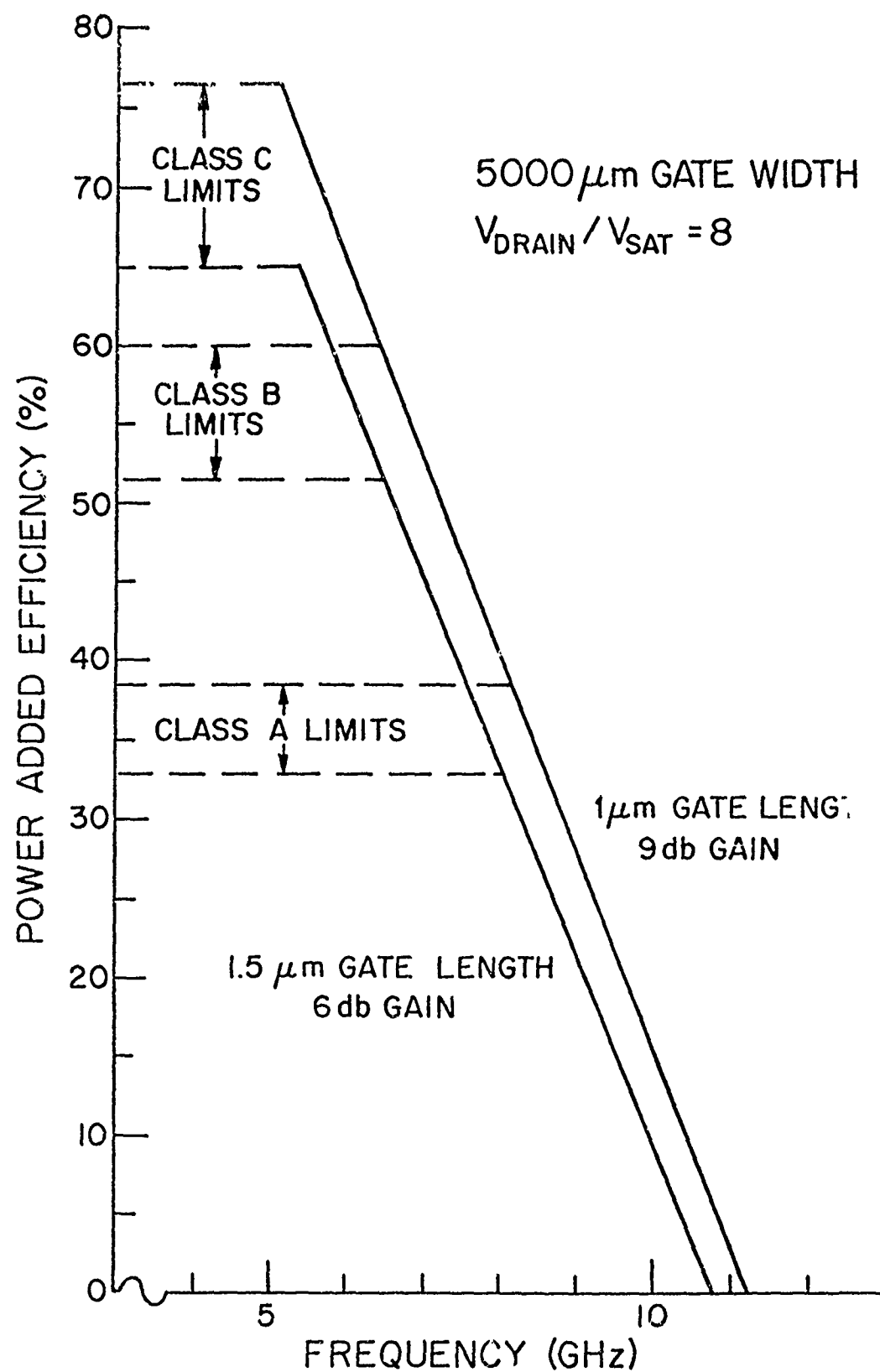


Figure 4

This resulted in 2W output power for the 3mm gate width. With wide gates, low parasitic capacitance is needed for high g_m/C .

In all high power FET devices developed to date, the product of doping density times layer thickness is near $3 \times 10^{12}/\text{cm}^3$. Such a layer with $6 \times 10^{16}/\text{cm}^3$ doping and $.5\mu\text{m}$ thickness would work well with $1.5\mu\text{m}$ gate lengths at 7.5 GHz. Just over 40% drain efficiency with just over 30% power-added efficiency is possible with 6dB gain. If such an FET is $6\mu\text{m}$ long and is developed to take more than 30V instantaneous voltage between drain and source when nearly pinched off, it will be able to generate at least 1W/mm gate width. In order to yield the highest output power, such a device should be operated near $.175\text{A/mm}$ gate width, which is about half of full channel current. It should also operate near 16V DC bias between drain and source. This would yield 2.8W input power and 1.12W output power per mm gate width.

In order to dissipate the full 2.8W without drive, and less with drive, the thermal resistance of the FET should not exceed about $40^\circ/\text{W}$. By thinning the semi-insulating substrate to about $.004''$, such a low thermal resistance should be possible.

If even higher gain is desired, a $1\mu\text{m}$ gatelength would yield 9dB gain at over 30% power-added efficiency as shown in Figure 4 for $5000\mu\text{m}$ gate width. In order to maintain high voltage between the drain and source, for obtaining high

power, the drain-source spacing would have to be maintained at 6 μ m. The 1 μ m gate would be located only about 1 μ m from the source to help maintain high drain voltage without breakdown. The doping density times thickness product would again be $3 \times 10^{12}/\text{cm}^2$ to maintain the magnitude of the drain current.

If much more linearity is required, the method described in Figure 1 can be used. The high resistivity outer layer, under the gate, will help hold off very high drain-gate voltages for high power devices. Such a buried-channel FET has recently been constructed⁸ at the Technical University in Aachen, Germany. It does show extreme linearity of current modulation with bias voltage, as expected, and shows high gain.

Whether or not the buried-channel method is used, a high resistivity buffer layer is required for high performance and N^+ contacts are also required, whether or not they are buried, for both high performance and high reliability.

In summary, 5mm gate width or more per FET device, with 1W per mm power output, is definitely possible with 30% or more power-added efficiency at 6dB or more gain after about three years development effort in one or more laboratories. Two such devices with a power combining hybrid can yield 10W at 7.5 GHz. These results can be obtained with about 1dB gain compression from 7dB or more small signal gain and with intermodulation products well within the present specifications. Such high power devices can likely be developed to have more than 10^7 hours expected lifetime also.

LIST OF FIGURES

- Figure 1. The drain current vs. gate voltage for an ordinary FET doping profile (A), and for a doping profile (B) that causes substantial improvement in device linearity.
- Figure 2. The various geometries of FET channels and contacts showing (a) usual, (b) N^+ contacts for improved reliability, (c) flared channel near contacts for higher drain bias voltage, and (d) buried contacts for very high drain bias voltage.
- Figure 3. Power added efficiency (and associated drain efficiency for 4dB gain, and a drain voltage to saturation voltage ratio of 4, versus frequency for various gate widths as determined by Texas Instruments for a $2\mu\text{m}$ gate length.
- Figure 4. Predicted values of power added efficiency versus frequency for $1.5\mu\text{m}$ and $1\mu\text{m}$ gate lengths and for 3dB and 9dB gain, respectively, and for a drain voltage to saturation voltage ratio of 8 for $5000\mu\text{m}$ wide gates.

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