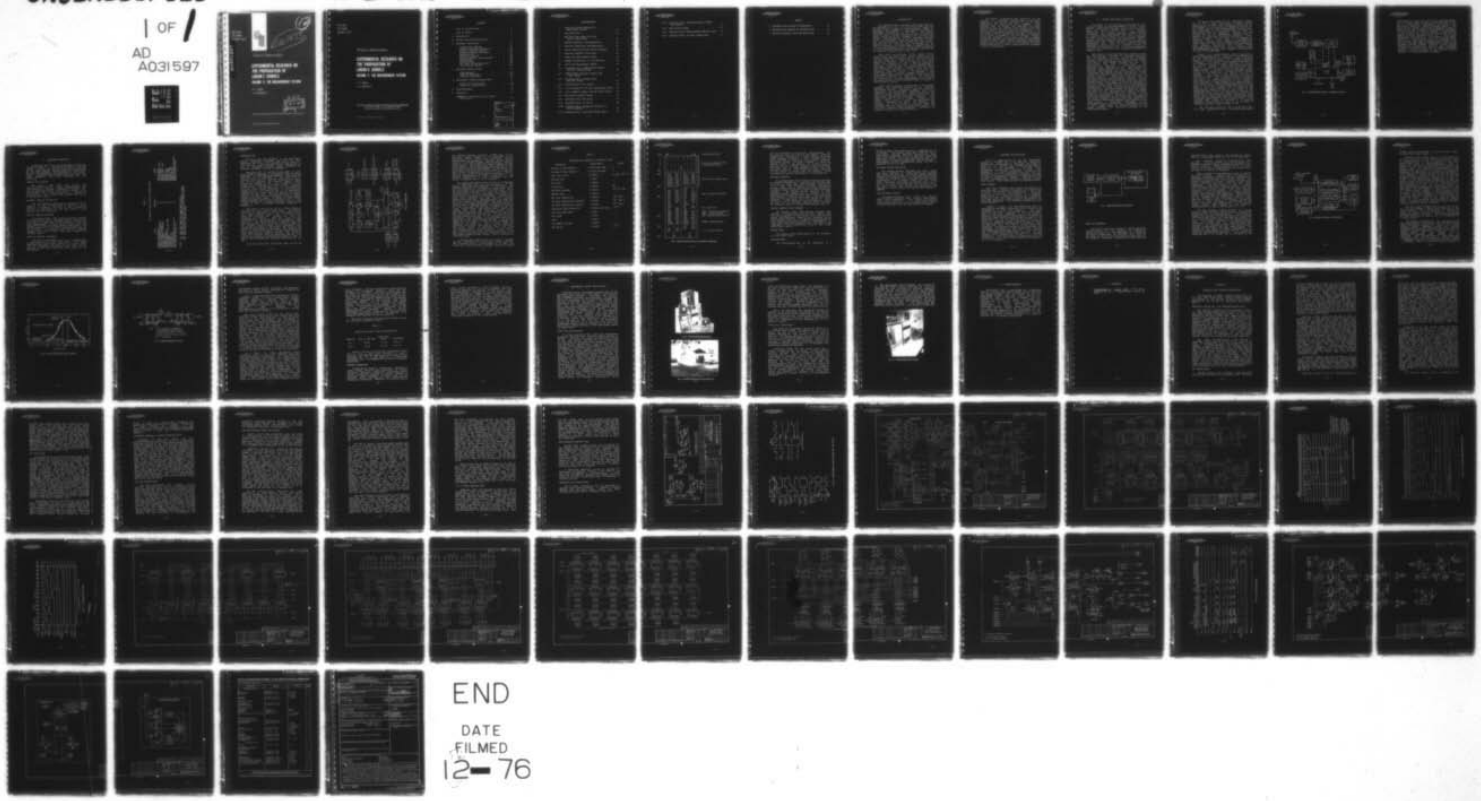
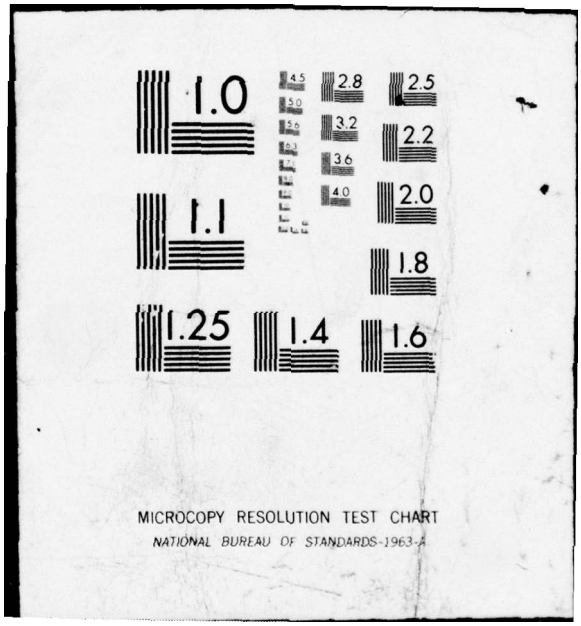
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Technical Memorandum

EXPERIMENTAL RESEARCH ON THE PROPAGATION OF LORAN-C SIGNALS

VOLUME C: THE MEASUREMENT SYSTEM

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Technical Memorandum

EXPERIMENTAL RESEARCH ON THE PROPAGATION OF LORAN-C SIGNALS

VOLUME C: THE MEASUREMENT SYSTEM

S. F. ODEN
J. A. PERSCHY

THE JOHNS HOPKINS UNIVERSITY ■ APPLIED PHYSICS LABORATORY
Johns Hopkins Road, Laurel, Maryland 20810
Operating under Contract N00017-72-C-4401 with the Department of the Navy

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CONTENTS

List of Illustrations 4

List of Tables 6

1. Introduction 7

2. System Functional Description 9

3. Equipment Description 13

   Loran-C Loop Antenna 13
   Wideband Variable Attenuator 13
   Loran-C Tuned RF Receiver 13
   Analog-to-Digital Converter 13
   Interface Unit 15
   Buffered Formatter 20
   Digital Magnetic Tape Recorder 20
   Tuning Meter 20
   Oscilloscopes 20
   Low Noise Cesium Beam Clock 21
   Time Interval Counter 21

4. Equipment Modifications 22

   Loop Antennas 22
   Tuned RF Receivers 23
   Buffered Formatters 30

5. Measurement System Installations 32

   Fixed Site Installation 32
   Field Site Installation 34

6. Acknowledgments 36

7. Reference 37

Appendix A, Interface Unit Circuits
   Description 39

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ILLUSTRATIONS

1	Functional Block Diagram of a Measurement System	11
2	Interface Unit	16
3	Raw Data Tape Format for Each Block of Recording	19
4	Antenna Resonance Instrumentation	23
5	Receiver Comparison Instrumentation	25
6	Loran-C Receivers Gain versus Frequency	27
7	Receiver Bandpass Filter Data	28
8	Fixed Site Measurement System	33
9	NAVOBSY Building No. 54 and USAF Van	33
10	Field Site Measurement System	35
A-1	Interface Unit, 5-MHz/10-MHz Doubler and UTC 1-second Reset	49
A-2	5-MHz/10-MHz Frequency Doubler and 1-pps Timing	51
A-3	Interface Unit, Slewing Logic and GRI Timing	53
A-4	Interface Unit, GRI Timing	55
A-5	2.5-μs Timing for GRI and Tape Format Logic	57
A-6	A to D Sample Trigger and GRI Clock Timing	59
A-7	GRI Preset Counter Timing	61
A-8	Interface Unit, UTC Clock	63
A-9	Interface Unit, UTC Clock	65
A-10	Interface Unit, Digiswitch Parallel to Serial Register	67
A-11	Interface Unit, Tape Multiplexer Logic	69

A-12 Interface Unit, Tape Multiplexer Timing and Control 71

A-13 Tape Format Timing 73

A-14 Interface Unit, Miscellaneous Monitor Logic. 75

A-15 Interface Unit, DC Power Connections . . 77

TABLES

1 Equipment Used during the Experiment . . . 14

2 Recorded Data Handled by Interface Unit . . 18

3 Austron Receivers' Gain and Self-Noise . . 30

1. INTRODUCTION

The Applied Physics Laboratory (APL) has conducted an experiment for the U.S. Air Force (USAF) and the Defense Advanced Research Projects Agency (DARPA) to determine the validity of one facet of the theory of groundwave propagation at 100 kHz. The theory indicates that, if proper account is taken of group and phase velocities in the propagation of pulses of the Loran-C radio navigation service, geodetic position should be computable using the vacuum speed of light and the time of arrival of the pulse and the carrier. Specifically, the test goal was to determine if an analytic function can be developed for operational use that relates secondary phase factor (SPF) to envelope to cycle difference (ECD) so that geodetic position can be computed accurately and in real time.

Test data were obtained in the eastern United States using the East Coast Loran-C chain and two identical measurement systems, one in a mobile test van and the other at a fixed site at the U.S. Naval Observatory (NAVOBSY). The van occupied 10 field sites during the course of the test. APL was assisted in this test by NAVOBSY and the Defense Mapping Agency Topographic Center (DMATC). The positions of all sites were precisely surveyed by DMATC using the Navy Navigation Satellite System. The sites are on ray paths from Loran-C stations through NAVOBSY. A team from NAVOBSY executed time transfers to each field site during the collection of loran data. The collected data include very accurate measurements of the Loran-C groundwave phase and pulse envelope times of arrival at the 10 pairs of sites.

This report contains a description of the design, assembly, and electrical matching of two identical measurement systems. Particular emphasis is given to describing the APL-designed Interface Unit (IU) component of the system. Also, modifications that were made to purchased equipments to enable matching of two measurement systems are described in detail. This report is Volume C of four volumes. Volume A is the summary report, Volume B covers test operations, and Volume D documents the data, the analysis, and findings. All of the volumes are written under the assumption that the reader is reasonably familiar with the Loran-C system of radionavigation. Reference 1 is suggested reading for those who are not.

As a result of extensive data analysis, it was possible to establish statistically significant measures of SPF and ECD for each of the 12 tests conducted at the field sites and at NAVOBSY. It was possible also to define the amplitude and phase modulations that are applied to the carrier to form the Loran-C pulse that is actually transmitted. The functional relationship between ECD and SPF, which, it was hoped, would be derived from the data taken during all 12 tests, is presently not well defined. However, trends are observed in the data that tend to support the hypothesis that the desired functional relationship exists, at least under certain conditions. Additional analysis and perhaps tests will be necessary to define these conditions or to prove conclusively the existence of such a relationship.

2. SYSTEM FUNCTIONAL DESCRIPTION

The concept of the experiment, developed by APL, called for very accurate measurements of the Loran-C signals transmitted from East Coast Loran-C stations. Also, the Loran-C signals had to be recorded undistorted at widely varying signal-to-noise conditions. These measurements would have to be made at precisely surveyed pairs of test sites located on ray paths from the Loran-C stations through NAVOBSY. Further, precise timing would be required in order to identify the same Loran-C pulses as they passed each measurement site. Thus, two very carefully matched measurement systems would be required so that the received Loran-C signals could be accurately measured, converted to digital form, and preserved faithfully on magnetic tape.

The concept of the experiment was presented by APL and discussed and finalized at planning conferences held on 7 November 1973 and 7 March 1974. Attendees included representatives of the Defense Mapping Agency, Institute for Telecommunication Sciences, U.S. Coast Guard (USCG), USAF, DARPA, NAVOBSY, and APL. The organizations that were to participate in the experiment were identified at the above conferences. They were DMATC, NAVOBSY, and APL. Additionally, an informal understanding was achieved with the USCG representatives regarding advance coordination of data acquisition time periods to ensure availability of the Loran-C service. DMATC was given the task of accomplishing the required precise surveys, and this was done using the Navy Navigation Satellite System. NAVOBSY was given the task of providing the source of precise timing, and NAVOBSY did this by providing two low noise cesium beam clocks for the two measurement systems and a portable low noise cesium beam clock for executing time transfers between the test site pairs. The details of the participation of DMATC and NAVOBSY personnel in the experiment and results of their efforts are described in Volume B of TG 1298. APL was given the responsibility for overall test coordination; the design, assembly, checkout, and field operation of two identical measurement systems; data analysis; and a final report. A functional description of the measurement system is given below. Subsequent sections of this volume expand on pertinent aspects of the design, assembly, and electrical matching of two measurement systems.

The design philosophy for the measurement system was to use as many commercially available system components as possible and integrate them with an APL-designed IU. All the system components would be of the highest quality and have measurement precision such that discussion of the recorded data in terms of nanoseconds would be realistic. Further, it was decided that the two measurement systems would be operated in carefully controlled environments. Thus, system components did not have to be capable of operation over a wide range of environmental conditions. However, the two systems would have to be finely tuned to make them as identical as possible so that equipment effects on the Loran-C signal measurements would be minimal in both systems. Two such measurement systems were designed and assembled for use in the experiment.

Figure 1 is the functional block diagram of a single measurement system. The Loran-C signal received by the loop antenna is delivered to the fixed gain Loran-C tuned RF receiver via a wideband variable attenuator. The purpose of the wideband attenuator is to standardize the Loran-C pulse amplitude, as seen by the Loran-C receiver, without distorting the signal waveform or causing a phase shift that varies with signal strength. At least 3 dB of attenuation always remains in the attenuator to minimize mismatch effects between the antenna and the input to the Loran-C receiver. The output of the Loran-C receiver is adjusted to give a Loran-C pulse amplitude of between ±0.5 and ±1.0 V. This normalized output voltage is delivered to the analog-to-digital (A to D) converter, which digitizes voltage samples from sample points on the Loran-C pulse. Sample triggers generated by sample gates in the IU open a sample-and-hold circuit in the input of the A to D converter, and the converter then digitizes the analog voltage at the output of the sample-and-hold circuit to 13 bits plus a sign bit. The digitized Loran-C data are combined with a synchronous output from a UTC (Universal Time Coordinated) clock within the IU, along with fixed data entered previously via manual digiswitches on the IU control panel. This combined data stream is provided to a buffered formatter, which allows the data to be recorded on computer-compatible digital magnetic tape.

The precision timing for the IU is derived from a low noise cesium beam clock. The cesium beam clock's

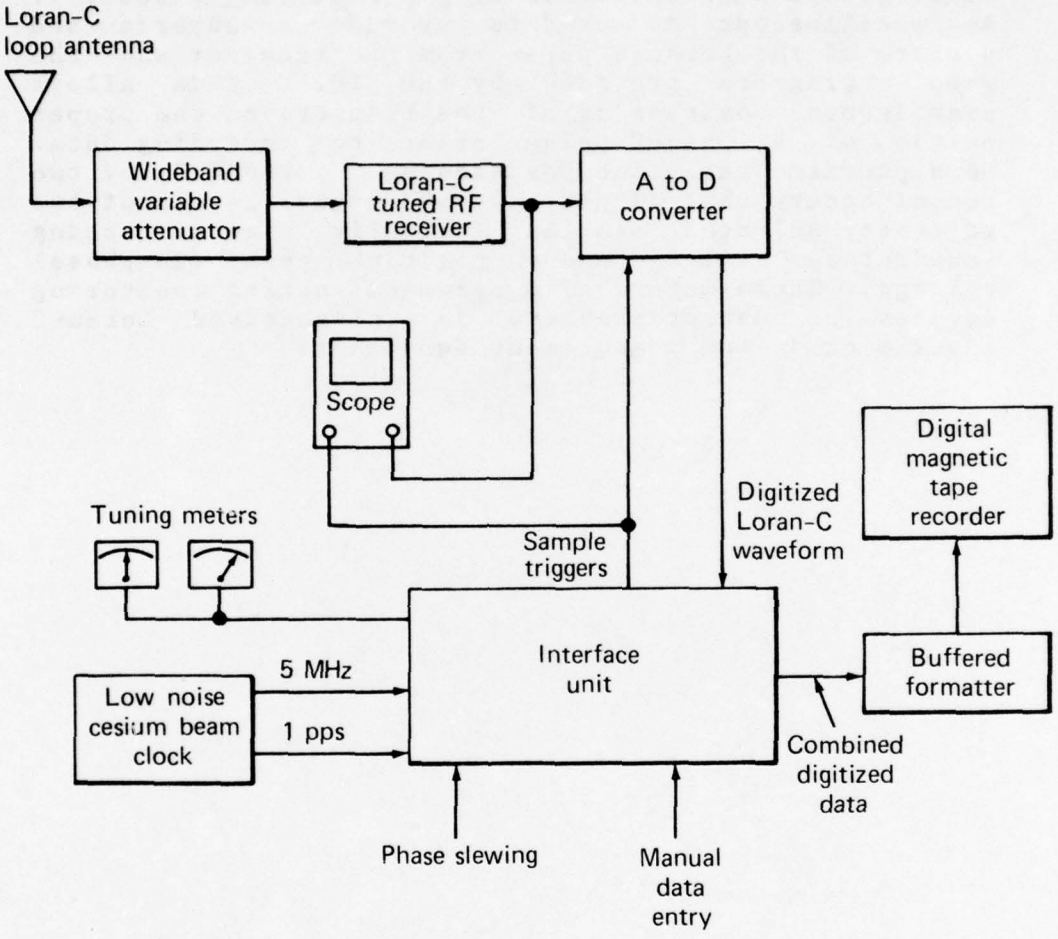


Fig. 1 Functional Block Diagram of a Measurement System

5-MHz signal is the source for the IU counting chains, and the 1-pps signal is used to synchronize the IU UTC clock. Timing of the sample gates is derived from a GRI (group repetition interval) preset counter. The phase of the preset counter can be adjusted in plus or minus 0.1-μs time intervals by phase-slewing circuitry. An oscilloscope is used to provide a superimposed picture of the Loran-C pulse from the receiver and the sample triggers provided by the IU. This allows unambiguous positioning of the triggers on the proper portion of a Loran-C pulse prior to recording data. More precise real-time positioning is provided by two tuning meters that display average signal levels of two adjacent, selected samples (normally a zero crossing (quadrature) voltage and a positive peak (in-phase) voltage). These meters also serve as useful monitoring devices to detect problems in the received Loran-C signals or in the measurement equipment.

3. EQUIPMENT DESCRIPTION

Equipments used in the two measurement systems are listed in Table 1. Also listed in Table 1 are the cesium clock and time interval counter that were used as the time transfer system during test operations. The selected equipments are described in more detail below. Manufacturers' specifications are given for those equipments that were purchased for the experiment.

LORAN-C LOOP ANTENNA

The Austron model 2021L loop antenna has directivity and does not require a ground plane. The loop antenna has physical dimensions of 34 by 34 in. and an equivalent height of 0.7 cm at 100 kHz (50-Ω termination) and a 3-dB bandwidth at 100 kHz of 50 to 150 kHz. Each antenna was supplied with 100 ft of RG-58/U 50-Ω cable.

WIDEBAND VARIABLE ATTENUATOR

The Kay Elemetrics model 461B attenuator has a range of 132 dB in 1-dB steps by means of slide switches, a bandwidth from DC to 4 GHz, an insertion loss of 0.1 dB from DC to 250 MHz, and 1% ± 0.1% accuracy from DC to 250 MHz.

LORAN-C TUNED RF RECEIVER

The Austron model 2082 tuned RF receiver consists of an adjustable 120-dB amplifier tuned to the Loran-C frequency, a three-pole 35-kHz bandpass filter, and four independently tunable notch filters with 3-dB bandwidth of 3-kHz and 30-dB minimum notch depth. The center frequency of each filter is adjustable from 70 to 130 kHz. The antenna input has 50-Ω nominal impedance, and the RF output is the Loran-C signal from a 1000-Ω source.

ANALOG-TO-DIGITAL CONVERTER

The Preston model GMAD-1-14B A to D converter has a resolution of 13 bits plus sign. The input sample-and-hold amplifier is set for ±1 V full scale, and the conversion interval is less than 2.5-μs. Accuracy is specified as ±0.02% full scale by the manufacturer.

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Table 1

Equipment Used during the Experiment

Item	Quantity	Model
Loran-C Loop Antenna	2	Austron 2021L
Wideband Variable Attenuator	2	Kay Elemetrics 461B
Loran-C Tuned RF Receiver	2	Austron 2082
Analog-to-Digital Converter	2	Preston GMAD-1-14B
Interface Unit	2	APL/JHU
Buffered Formatter	2	Kennedy 9232
Digital Magnetic Tape Recorder	2	Kennedy 9000
Tuning Meter	4	Triplett 320G
Oscilloscope (1)	1	Tektronix 7603
Oscilloscope (2)	1	Tektronix 545
Low Noise Cesium Beam Clock (3)	3	Hewlett-Packard E44-5061A
Time Interval Counter (4)	1	Hewlett-Packard 5345A

Notes: (1) Used with fixed site measurement system
(2) Used with field site (USAF van) measurement system
(3) One of three clocks used with time transfer system
(4) Used with time transfer system

INTERFACE UNIT

The IU is the only equipment in the measurement system completely designed and built by APL. Therefore, the IU will be described in some detail in this section. A more detailed circuit description of the IU, including pertinent timing diagrams and schematic drawings, is given in Appendix A.

Basically, the IU combines three types of data into a format acceptable to the magnetic tape recording equipment: (1) digitized measurements of Loran-C pulses from the A to D converter; (2) UTC time from an internal clock; and (3) manually entered fixed data. The IU also provides the required sample trigger conversion commands to the A to D converter at the proper time of reception of a Loran-C pulse. The basic frequency and time references for the IU are supplied by a low noise cesium beam clock. A detailed block diagram of the IU is given in Fig. 2. All significant elements of the IU are shown, as well as all inputs, outputs, and data flow. The rack-mountable IU chassis contains all the circuitry indicated in this diagram except the IU power supply. A separate IU power supply chassis provides the DC power required by the IU. The drawing numbers and corresponding closed dashed lines in Fig. 2 refer to detailed drawings presented in Appendix A.

The basic clock in the IU is a 10-MHz frequency obtained from the cesium 5-MHz output. This clock, which has a resolution of 100 ns, is counted down in two separate divider chains. One is a fixed count chain that produces the internal UTC clock for recording and display. This UTC clock is kept synchronized to the cesium UTC clock by special 1-pps circuitry. The second chain is a variable count type used to position the data-taking system (in time) on the received Loran-C pulse. This presettable data timing logic is based on the Loran-C GRI, which is the period of pulse group transmissions. For example, the East Coast chain monitored in the experiment transmits pulse groups with a 0.0993-s period. The IU front panel GRI switches allow any presently used GRI to be tracked by setting the desired period ahead of time. A 100-μs clock provides the required resolution for any GRI.

Once the correct GRI period has been set in the

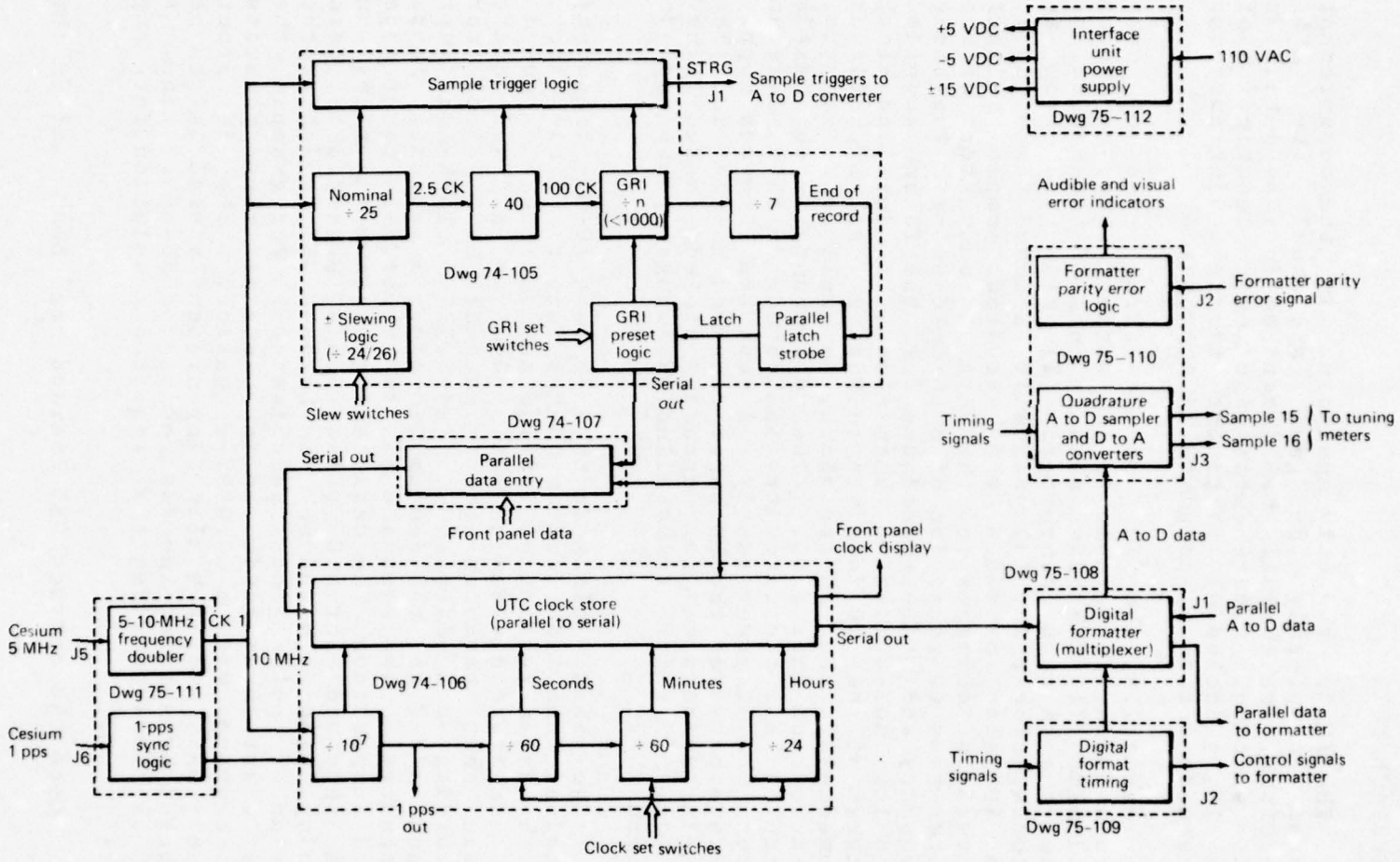


Fig. 2 Interface Unit

IU, special slewing circuitry allows the A to D converter sample triggers to be positioned on the particular Loran-C pulse to be digitized. This is accomplished by temporarily altering the GRI counter chain to a division slightly less or greater than the nominal value. This slides the sample triggers in time with respect to the Loran-C pulse until they are in the proper position. Since measurements are desired at zero crossings and peaks of the 100-kHz Loran-C pulse, the basic clock for sampling is one with a 2.5-μs period. Only the first pulse of each group is sampled, and 32 voltage measurements are taken on each pulse. The first 16 samples are at 2.5-μs intervals, and the second 16 samples are at 7.5-μs intervals.

The sample measurement logic of the IU is designed to be compatible with the characteristics of the magnetic tape recording equipment. In particular, the buffered formatter is configured to receive and store data in blocks of 512 characters of 8 bits each. Since one measurement from the A to D converter consists of a parallel word of 13 bits plus sign, two 8-bit tape characters are required per measurement. Therefore, 64 8-bit tape characters are used for the 32 voltage samples taken each GRI. This means that one tape data block can contain the measurements made from seven GRI periods, or 448 8-bit characters. Accordingly, the IU logic formats a combined digital data record consisting of data from seven GRI periods, a reading of the UTC clock, and all front panel stored data. During the seventh GRI, after the digitized Loran-C pulse measurements have been sent to the formatter, the clock and front panel data are read out of a series of IU storage registers and sent to the formatter as 8-bit characters. This recording is accomplished before the beginning of the next GRI sampling time. The various types of data handled by the IU for recording are summarized in Table 2. Table 2 also shows the resolution with which each type of data is recorded. The actual format of recorded data for each 512-character block is shown in Fig. 3. Each line in Fig. 3 represents one 8-bit character or byte. Since each digit of the UTC clock and front panel data is in BCD (binary-coded-decimal) format, 1 byte contains two 4-bit BCD codes.

A special data sampler circuit is used to provide monitor information on Loran-C data being recorded. The digitized values of two samples 2.5 μs apart are stored and passed through averaging digital-to-analog

Table 2

Recorded Data Handled by Interface Unit

Parameter	Digits/Bits	Units
Voltage of Odd Samples, x	13 bits and sign	V
Voltage of Even Samples, y	13 bits and sign	V
Time (UTC clock)	13 digits	h, min, 10^{-7} s
Station Code	1 digit	-
Site Code	2 digits	-
Attenuation	2 digits	dB
Barometer Reading	5 digits	10^{-3} in. Hg
Weather Code	2 digits	-
Wet Bulb Temperature	3 digits	10^{-1} deg C.
Dry Bulb Temperature (outside)	3 digits	10^{-1} deg C.
Dry Bulb Temperature (inside)	3 digits	10^{-1} deg C.
Predicted Time Calibration	9 digits and sign	10^{-9} s
Data Recording Mode	1 digit	-
Note Code	1 digit	-
Year	1 digit	-
Day Number (Julian)	3 digits	-
GRI Period	4 digits	10^{-4} s

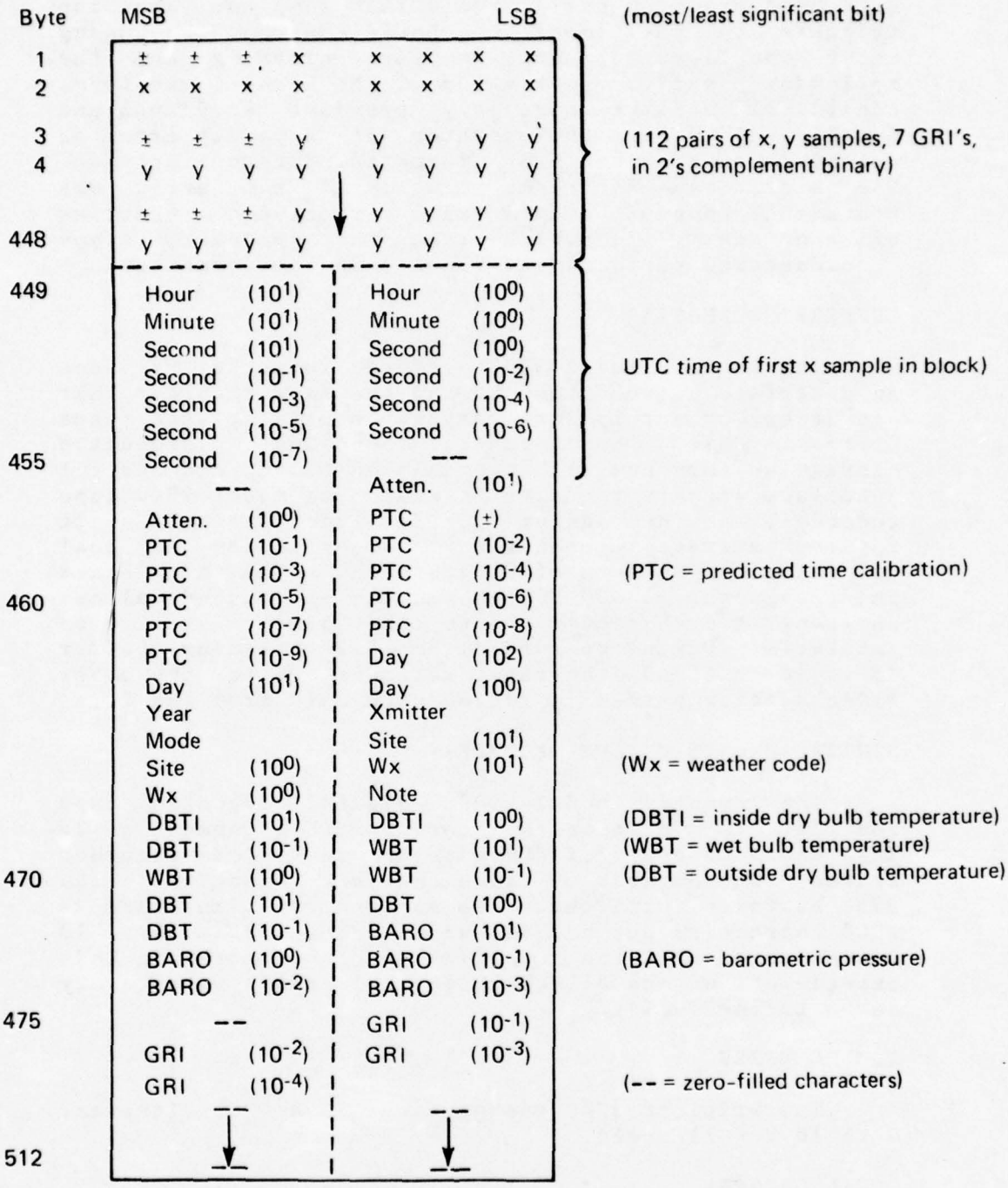


Fig. 3 Raw Data Tape Format for Each Block of Recording

(D to A) converters to drive two tuning meters. The data used are from the 15th and 16th samples. When the triggers are positioned on a Loran-C pulse, the tuning meter displays represent a zero crossing and the following positive peak value of the Loran-C waveform. Additional monitor circuitry provides a visual and audible alarm to the operator if a parity error is detected in the buffered formatter internal storage. The alarm may be reset manually if the error was transient; however, a firm failure precludes resetting of the alarm, in which case the operator stops recording and performs maintenance on the formatter.

BUFFERED FORMATTER

The Kennedy model 9232 buffered formatter provides an interface between the IU and the tape recorder that can accept or supply data asynchronously at data rates 0 to 1 MHz. The formatter contains intermediate storage buffers and all specialized timing and control interface signals required to drive the model 9000 tape recorder. The buffer portion consists of shift register storage elements and is organized as dual 512-character buffers of 8 bits each. The high-speed shift register, 1 000 000 characters per second, allows shifting two characters into the buffer at 2.5-μs intervals. During operation, one 512-character buffer is read out to the tape recorder, while the other 512-character buffer is filled with data from the IU.

DIGITAL MAGNETIC TAPE RECORDER

The Kennedy model 9000 digital magnetic tape recorder is a nine-track recorder with a speed of 25 in/s and a capacity of 800 bits per inch. This recorder writes IBM-compatible tapes and is a companion to the 9232 buffered formatter. The maximum recording rate is 7000 characters per second, which is approximately 10 times faster than the recording rate, required in this experiment, of one 512-character block of data every seven Loran-C GRI's.

TUNING METER

The Triplett 320G tuning meter is a DC voltmeter, 0 to 10 V full scale.

OSCILLOSCOPES

One oscilloscope used in the experiment is a

Tektronix model 7603 mainframe with a bandwidth of DC to 100 MHz. Two plug-ins were used with the 7603: a dual-channel vertical amplifier preamplifier, model 7A18, with a bandwidth of DC to 75 MHz, and a dual time base, model 7B53A. The second oscilloscope used in the experiment is a Tektronix model 545 with one plug-in, a dual-channel vertical preamplifier, model CA, with a bandwidth of DC to 24 MHz.

LOW NOISE CESIUM BEAM CLOCK

The Hewlett-Packard E44-5061A low noise cesium beam clock consists of a 5061A cesium beam standard with option 001 clock and option 004 cesium beam tube fastened with side brackets to a K02-5060A power supply to make one portable unit. The power supply provides approximately 7 h of standby power for the cesium clock. The power supply may be operated from 6 or 12 VDC, 24 to 30 VDC, or 115/230 VAC ±10% at 50 to 400 Hz. All three clocks used during the experiment were supplied on loan to APL by the Time Service Division of NAVOBSY.

TIME INTERVAL COUNTER

The Hewlett-Packard model 5345A time interval counter makes single-shot time interval measurements with 2-ns resolution. For repetitive signals, subnanosecond resolution can be achieved through use of a noise modulated clock and time interval averaging.

4. EQUIPMENT MODIFICATIONS

Prior to installation of the two measurement systems at NAVOBSY and in the USAF van, laboratory checkout was accomplished to determine the degree to which the two systems were matched and the ease of operation of the equipment. Following this, appropriate modifications were made to some of the equipments to achieve satisfactory operation and matching of the two measurement systems. The loop antennas and tuned RF receivers were modified to match in the two measurement systems. Additionally, the buffered formatters were modified by adding a parity check option. These modifications are described below.

LOOP ANTENNAS

The loop antennas were tested as received to determine their resonant frequencies, which were found to be 90.1 kHz and 91.6 kHz, respectively. Use of the antennas, as received, would result in a different phase delay for signals received by both antennas. Therefore, steps were taken to modify the antennas so that they would have matched resonant frequencies at an acceptable bandwidth. The bandwidth selected was from 80 to 120 kHz.

Figure 4 shows the instrumentation used to determine the resonant frequencies of the antennas and subsequently to match the antennas. The 20-dB attenuator was used to provide the input measurement point V1 and a 50-Ω impedance to the loop antenna. Resonance was determined by selecting the frequency at which zero phase shift existed between the input to the attenuator, V1, and the input to the antenna, V2. As would be expected, phase comparison at resonance provided a sensitive determination of resonance, while the amplitude ratio of V1 and V2 varied little near resonance. The resonant frequency of the antennas was determined primarily by the nonprecision 0.022-μF low-temperature-coefficient capacitor. By tailoring the low-temperature-coefficient capacitor in each antenna, both antennas were retuned to a resonant frequency of 96.8 kHz giving half power points at 80 and 120 kHz. Also, each antenna exhibited an impedance of 12 Ω at resonance.

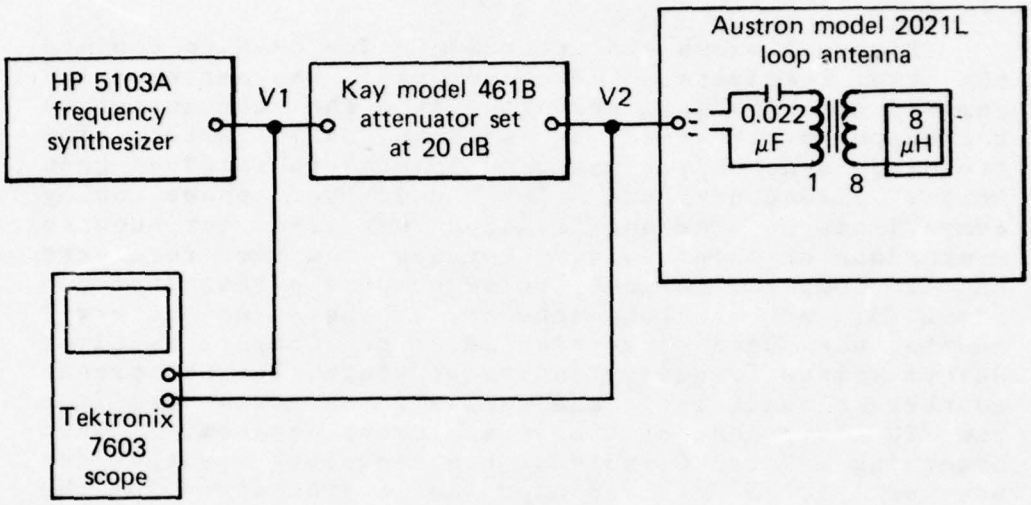


Fig. 4 Antenna Resonance Instrumentation

TUNED RF RECEIVERS

The two receivers were tested to compare pertinent characteristics for the frequency and temperature ranges of interest in the experiment. As a result of the initial comparisons, the receivers, which were not specified by APL to be factory-matched, were found to be somewhat mismatched. Therefore, the modifications

discussed below were made to the receivers to match them to an acceptable degree for use in the experiment.

The following receiver characteristics were measured: gain at 100 kHz, phase delay through the receivers with and without interference frequency notch filters activated, center frequency drift in phase delay as a function of changing operating temperatures, and gain as a function of frequency.

Figure 5 shows the instrumentation used to compare the two receivers. Receiver gain was measured by comparing the signal strength into the attenuator to the output of the receiver with an RMS voltmeter. The frequency synthesizer was used to measure receiver gain versus frequency and also used for phase delay comparisons. The oscilloscope was used for coarse comparison of phase delays between the two receivers and to compare Loran-C pulse outputs either from the simulator or the loop antenna. The time interval counter was used as a phase meter to compare receiver delays versus frequency and temperature. The GRI preset counter slewing logic and sample gates used were from the IU component of the measurement system. When observing a Loran-C pulse, the frequency synthesizer was set to 5 MHz and used as a substitute for the cesium clock that was normally used to clock the GRI preset counter. Cable lengths for the comparison instrumentation in Fig. 5 were matched to 1/4 in.

The time interval counter was used as a phase meter to compute receiver delays versus frequency and temperature in the following manner. The differences between the frequency synthesizer output zero crossings and the receiver output zero crossings were summed over 1 s, which resulted in less than 1-ns deviation due to noise. The counter was set to the gated averaging start-stop counter mode. The positive-going zero crossing of the synthesizer signal into the attenuator started a measurement, and the negative-going zero crossing of the receiver stopped a measurement. To resolve cycle ambiguity, the delay was first observed using the Loran-C pulse simulator. This observation indicated that 1-1/2 cycles had to be added to the

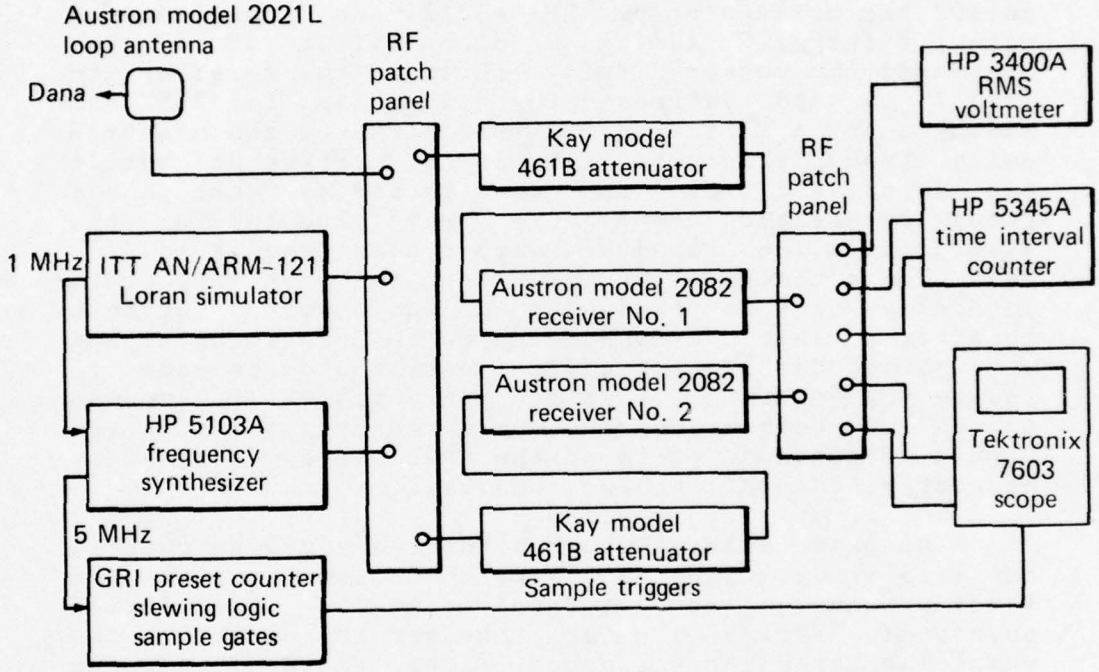


Fig. 5 Receiver Comparison Instrumentation

average interval measurement of the start-stop counter to obtain the correct answer.

Initially, the maximum gain of both receivers was in excess of 130 dB. It was decided to reduce the gain to approximately 100 dB by replacing the gain potentiometer with a fixed attenuator in order to reduce the effect of receiver-generated noise. To characterize the receivers initially, one receiver was checked with the comparison instrumentation. The measured delay was 17.476 μs at 100 kHz. The frequency dispersion in the receiver in the frequency range of 97 to 103 kHz was +40 ns per kHz and 242 ns total (without notch filters). Adding a notch filter at 88 kHz decreased the measured delay through the receiver to 17.307 μs and increased the dispersion to 265 ns. Adding a notch filter at 122 kHz increased the measured delay through the receiver by 65 ns. Frequency drift was determined for the two receivers through a receiver-operating temperature range expected for the experiment. The receivers were cycled from 18 to 27°C in a Tenny thermal chamber. A center frequency drift in delay of 9 ns per degree C was observed for both receivers. This was considered to be unacceptable, and it was decided that modifications would be made to reduce the drift. Finally, the frequency response curves of both receivers were measured and plotted. Figure 6 contains plots of the gain versus frequency characteristics of the two receivers.

The phase delay through both receivers was matched at 17.5 μs by adding a 900-pF shunt capacitor at the fixed attenuator tap in receiver No. 2. The plotted points in Fig. 6 are for receiver No. 2 after the phase-lag capacitor was added. The frequency response for both receivers, as shown in Fig. 6, is wideband for a Loran-C pulse.

The resonant frequencies of the bandpass filters were then matched at 98.45 kHz. This was accomplished using information obtained from Austron, Inc., which included nominal component values and resonant frequency of the receiver bandpass filter (see Fig. 7). Capacitors had been selected by Austron for the nominal values shown but not matched on a component-for-component basis between the two receivers. New, matched pairs of capacitors were installed at APL, and the resonant tuning procedure recommended by Austron for each section of the filters was followed. That is, the three resonant elements of

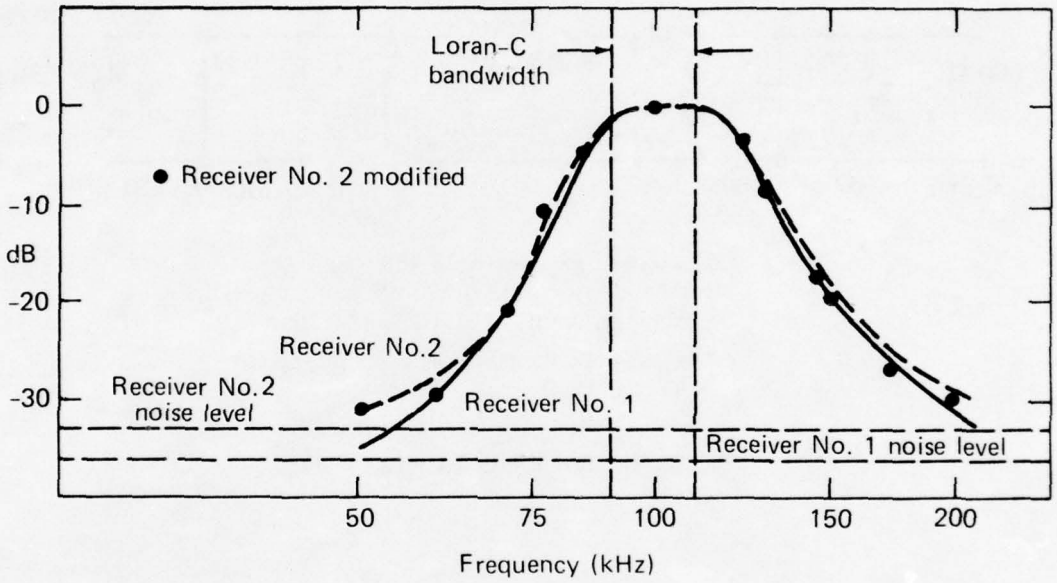
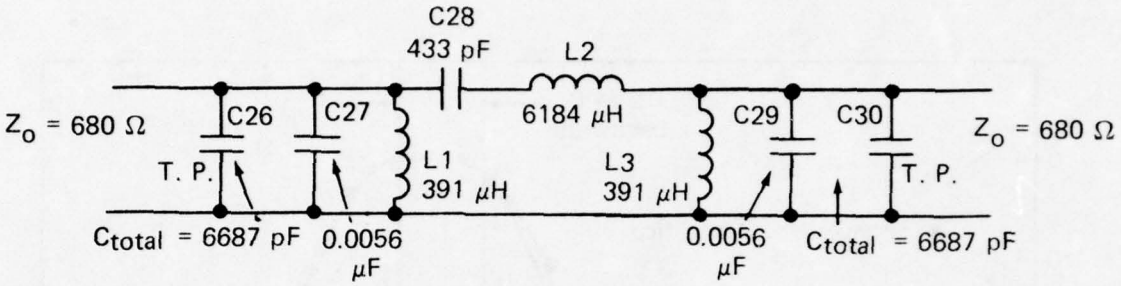


Fig. 6 Loran-C Receivers Gain versus Frequency



Note: 1. Tune each section to 98.456 kHz for bandpass filter with 3-dB points symmetric about 100 kHz, ±17.5 kHz

2. Identical resonance of sections important

3. T. P. = tailor point

Fig. 7 Receiver Bandpass Filter Data

the bandpass filters in both receivers were separated and tuned to 98.45 kHz by adjusting the tunable cup core for each resonant element.

Next, a mismatch between the receivers due to four mismatched pairs of 0.1-μF nonprecision ceramic coupling capacitors in emitter circuits between amplifier stages was corrected. Each of these capacitors had a reactance of 16 Ω at 100 kHz and a large temperature coefficient. Therefore, the 0.1-μF capacitors were replaced with low-temperature-coefficient 2.2-μF capacitors in series with 16-Ω precision resistors.

The next problem solved was the phase shift difference caused by pairs of notch filters when they were set at the same frequency in both receivers. These phase shift differences were eliminated at possible filter operating frequencies by an iterative procedure. First, both notch filters were tuned to the same frequency. Then, the inductance of one of the tunable cup cores associated with the pair of notch filters was changed in the direction that reduced the amount of the difference in phase lead or lag between the two receivers when the filters were switched into operation. Next, the variable capacitor associated with the notch filter in which inductance had been changed was retuned to bring the pair of notch filters back to the same notch frequency. The net effect of this procedure was to match the cup core inductance of pairs of notch filters between the two receivers. This matching procedure worked well for notch filter pairs 2, 3, and 4, but filter pair 1 could not be matched, possibly because of differences in cup core inductance.

As a result of further measurement system colocation tests at APL, the following additional modifications were accomplished. The receiver-A to D converter interface was changed from a single-ended to a differential connection. The A to D input already had a differential input capability, but the receiver's normal configuration was single-ended with a coax BNC output (signal grounds, chassis ground, and AC third wire all common). The receiver chassis (same as the signal output ground) was made independent of any contact with the system or AC third wire ground. The two sides of the output were then sent via a shielded twisted pair cable to the differential A to D input. Next, a 1000-Ω resistor was added across the receiver output in each receiver as a DC bias resistor for the A

to D converter. This was required for interconnection between the AC-coupled receiver output and the DC-coupled A to D input. Addition of this resistor had the effect of reducing gain at 100 kHz by about 5 dB. Then, the low side of the antenna input connection was floated from the receiver chassis so that the antenna lead just connected to the receiver input stage transformer winding. A 4.7-μF capacitor was placed between the low side of the antenna and receiver chassis. This modification eliminated a bias voltage that was caused by currents generated in the antenna-receiver connection. Finally, a further improvement in receiver output purity was achieved by providing 24-VDC power directly to the receiver. This completed modifications of the two receivers.

The final fixed gain and self-noise values for the two receivers are given in Table 3.

Table 3

Austron Receivers' Gain and Self-Noise

Receiver	Gain at 100 kHz	Self-Noise Output	Self-Noise
No. 1	94 dB	4.7 mV	0.09 μV
No. 2	92 dB	5.4 mV	0.14 μV

Finally, the two receivers were temperature-cycled from 17 to 32 C with notch filters 2, 3, and 4 activated. The observed temperature coefficient of both receivers was 1.5 ns per degree C, a significant improvement over the temperature coefficient initially determined.

BUFFERED FORMATTERS

During system checkout, intermittent operation of buffer memory circuits was encountered on several occasions. Therefore, appropriate replacement memory circuit boards were obtained as spares. However, in the normal mode of operation, a failure could not be detected during recording but only after-the-fact during data processing. Therefore, an available parity

check option was added to both formatter units to provide a detection of the type of problem that had been experienced. Installation of the parity check option consisted of changes to several circuit boards and the chassis back-plane wiring. Further, it was necessary to bring out the new memory error signal to the IU interface connector. A description of the error circuitry included in the IU is given in the discussion of the IU design in Appendix A. The parity check logic checks parity between the input and output of the 512-character storage register chains. During operation, a parity error produces a pulse that is sent to the IU error detection logic, where a flip-flop is set in order to remember the error. This formatter error signal is off-line. Thus, the tape recorder continues to operate in the normal manner.

5. MEASUREMENT SYSTEM INSTALLATIONS

Although the two measurement systems used in the experiment were identical, their physical installations were necessarily different. The fixed site location was at NAVOBSY throughout the experiment. Its physical layout was unchanged, and the same survey monument was used for positioning the antenna. The field site measurement was at a different location for each test day. The main concern for this measurement system installation was maintaining a reliable working system despite frequent movement of the system. In the measurement system installations, all corresponding interconnecting cables between the loop antenna, receiver, and A to D converter were made equal in length and of the same material in both systems so as to minimize signal delay differences. Also, receiver No. 1 was used in the fixed site and measurement system, and receiver No. 2 was used in the field site measurement system. Specific comments on the particular installation characteristics of each measurement system are given below.

FIXED SITE INSTALLATION

The final location of the fixed site measurement system was selected after extensive system checkout at NAVOBSY. Initially, the fixed site system was located in the Time Service Building, No. 78, because this building contains the master clock ensemble. The fixed site system was supplied with 1-pps and 5-MHz signals directly from the master clock ensemble. Thus, in this arrangement, no dedicated cesium clock was required for the fixed site system. However, during system checkout in early 1975, unsatisfactory performance of the fixed site system was caused by coherent radiation from the master clock distribution system in Building 78. Therefore, the fixed site system was moved to nearby Building 54, in which there was no other operating equipment, and a dedicated cesium clock was provided so the system could operate independently. The entire system was placed in an RF screen room already present in Building 54. This installation, which remained in place throughout the experiment, is shown in Fig. 8. The only electrical connection between the fixed site system and the local NAVOBSY electrical system was for primary 110-VAC power. To provide further independence from external problems, an isolation transformer was placed between all equipment, including the cesium

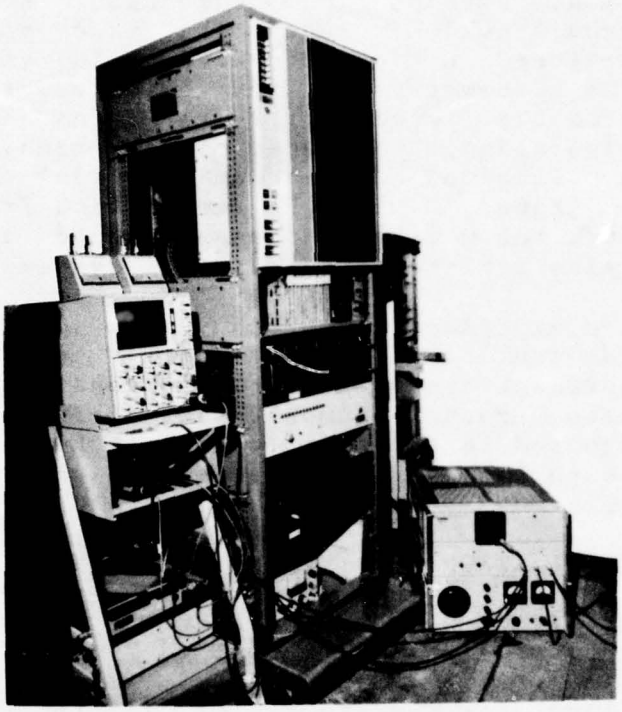


Fig. 8 Fixed Site Measurement System

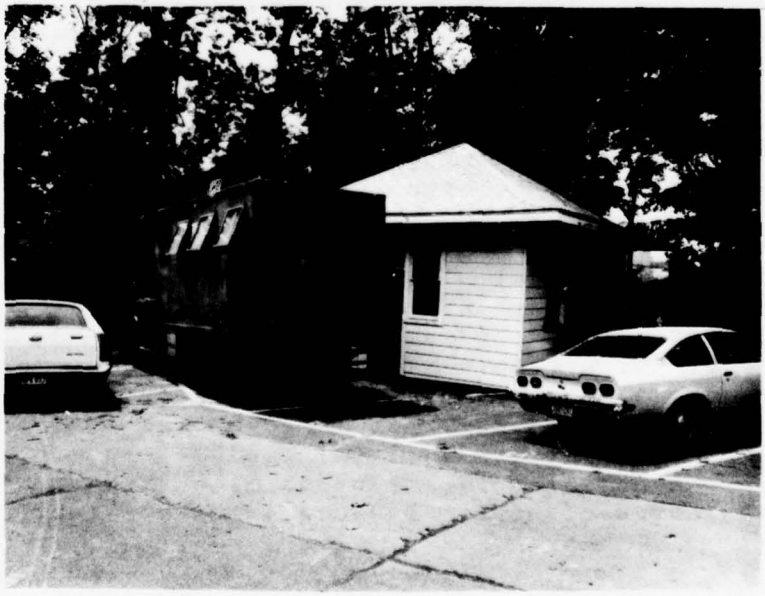


Fig. 9 NAVOBSY Building No. 54 and USAF Van

clock, and Building 54 power lines. The equipment rack and the screen room frame were both connected to a ground rod just outside the building. Equipment located in the rack included the tape recorder, buffered formatter, A to D converter, IU and power supply, and the DC power supply for the receiver. Since modifications to the receiver resulted in an isolated chassis configuration, the receiver was removed from the rack and placed on insulating material to avoid contact with ground. The RF connection from the antenna, through the wideband attenuator, and into the receiver was also isolated entirely from system ground.

Since the experiment was conducted during warm weather, an air conditioner in Building 54 was used to keep the measurement system temperature constant during data acquisition periods. A monitoring thermometer was thermally connected to the front panel of the receiver, since the temperature of that equipment was of the greatest concern.

FIELD SITE INSTALLATION

The field site measurement system was installed in a 19 000-lb gross weight van supplied by the U.S. Air Force. The van is shown in Fig. 9 parked next to NAVOBSY Building 54. The source of 115-V, 60-Hz AC power was a 15-kW Onan generator located in the rear of the van. Two additional generators were available for 115-V, 400-Hz AC power and 28-VDC power. The van also included a heating and air conditioning system that maintained constant temperature in the equipment area during data acquisition periods.

Electrical power for the cesium clock was a primary concern in the van system. During attended operation on-site, the van generator supplied the required 115 VAC. When the van was parked and unattended, an extension cord was used to obtain AC power from some local source at each site visited. Whenever the van was in transit, 12-VDC power was obtained for the cesium clock from the van battery/generator system. Two charged 12-V automotive batteries were also kept in the van for use in case the van had to be parked where no AC power was available. The 7-h standby battery in the cesium clock power supply was available to maintain the cesium clock during changeover of power sources or in any emergency situation.

The measurement system equipment was mounted in two adjacent racks in the van (see Fig. 10). One rack contained the tape recorder and buffered formatter, while the second rack contained the IU and its power supply, the A to D converter, and the cesium clock. The receiver was also mounted in this rack during van movement but was placed on insulating material on top of the rack during data acquisition periods. The racks themselves were braced and shock-mounted in the van in accordance with the shock and vibration conditions expected during movement. The oscilloscope was separately shock-mounted on a rear platform in the van.

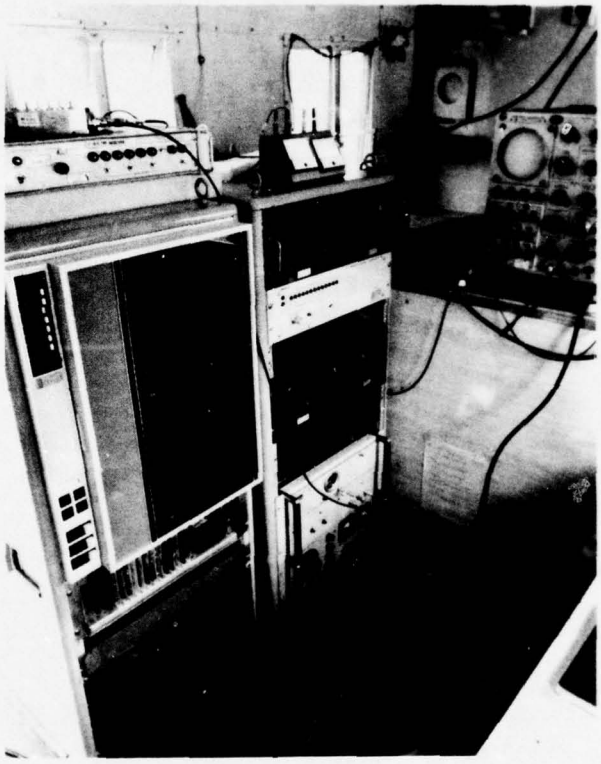


Fig. 10 Field Site Measurement System

6. ACKNOWLEDGMENTS

The authors wish to acknowledge the outstanding support of several individuals during various phases of the design, assembly, and installation of the two measurement systems. They are G.M.R. Winkler, W.J. Klepczynski, and K. Putkovich of NAVOBSY; and L.F. Fehlner, T.A. McCarty, R.G. Roll, T.W. Jerardi, C.M. DeLoriea, and L.W. Bennett of APL. Their excellent suggestions for system implementation helped significantly to produce two superbly matched measurement systems. Special thanks are extended to J.E. Berg and E.E. Gick, who fabricated all the special-purpose components of the measurement systems. Finally, the detailed circuit information for the loop antennas and Loran-C receivers provided by C. Stone of Austron, Inc., is greatly appreciated.

7. REFERENCE

1. Radionavigation Journal 1975, Wild Goose Association, Inc., 4 Townsend Road, Acton, MA 01720.

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Appendix A

INTERFACE UNIT CIRCUITS DESCRIPTION

This appendix provides a detailed description of the IU at the circuit level. Several timing diagrams are included in this section, as well as the schematic diagrams of the IU and its associated power supply unit.

FREQUENCY DOUBLER AND 1-pps SYNCHRONIZATION LOGIC

The detailed schematic for the frequency doubler and 1-pps synchronization logic is given in Fig. A-1. Associated timing diagrams are shown in Fig. A-2. Doubling of the basic cesium 5-MHz signal provides the desired 0.1-μs resolution in the IU UTC clock and also allows an integer division of 25 to produce the 2.5-μs sampling interval needed. Advantage is taken of the symmetry of the cesium sine-wave output, using two ground-reference comparators to produce a stable logic transition for each 5-MHz zero crossing. One-shots and gates are then used to form a final 10-MHz signal with approximately 50% duty cycle. The clock edges contributed by the one-shots are not critical, since the clock polarity is configured so that successive counter circuits are clocked on the stable edges only.

The 1-pps synchronization logic performs a resetting function for the UTC clock so that its 1-s count is synchronized with the cesium clock 1-pps output. To reduce ambiguity, the cesium pulse is adjusted in phase to coincide with the negative-going edge of the -CK 1 10-MHz clock. Then, the next edge of -CK 1 (stable edge) sets one flip-flop, and a second flip-flop is set one clock period later. The reset pulse gated from these two flip-flops (-CCK) is provided to the synchronous clear inputs of the UTC counter chain up through the 1-s stage, and these stages are all reset by the next positive-going -CK 1 edge. It may be noted that the width of the cesium 1-pps pulse is not a factor, and also that the pulse is really redundant after the first synchronization.

GRI TIMING LOGIC

The GRI timing logic contains a counting chain whose period may be set to the desired GRI, and whose

sampling triggers may be moved in time to coincide with a desired Loran-C pulse. The detailed logic schematics for functions related to GRI timing are found in Figs. A-3 and A-4. The first circuit of interest is the nominal ÷25 logic that produces the 2.5-μs clock (2.5 CK) from the basic 10-MHz clock, plus providing a ÷24/26 capability for slewing. Associated with this logic is the slewing logic, which changes the GRI clock to a 2.4- or 2.6-μs period temporarily. Operation of the ÷24/25/26 circuit may be most easily seen by referring to the timing waveforms given in Fig. A-5. (In all drawings, a decade divider output is designated by its function in the total circuit; e.g., 25QA1 means the Q stage of the first decade in the ÷25 counter.) As shown, OR-gate B2-6 provides the basic gating pulse for the 2.5 CK, depending on which division option is enabled by the slewing circuit.

When one of the three slew switches is held in either a plus or minus position (center position off), one AND-gate is enabled that allows a pulse train through to repetitively set one of the two initial flip-flops. The pulse train periods are derived from various stages in the UTC clock, with FAST slew giving a 100-kHz pulse rate, MEDIUM slew a 1.0-kHz rate, and SLOW slew a 10-Hz rate. Once a flip-flop is set, the next pulse from gate B2-6 sets a second flip-flop (one of two possible); the state of these two secondary flip-flops then determines which divide ratio is used for 2.5 CK. The next pulse from gate B2-6, which arrives 2.4 or 2.6 μs later, resets the initial flip-flop so that the whole sequence of offset division proceeds at the selected slew rate. In the absence of any attempt to slew, the initial and secondary flip-flops are reset in a few microseconds, and the normal ÷25 mode is enabled. Also, if tape recording is in progress (RECORD switch on), the secondary flip-flops are held in a forced reset state to avoid accidental slewing.

Three other timing signals are derived in the ÷25 logic: -CNT 6, -CNT 12, and -CNT 19. These are reset pulses used to clear flip-flops in the tape multiplexer timing and control logic to be described later. Here, it may be simply noted that -CNT 12 pulses come approximately halfway between 2.5 CK pulses, and -CNT 6 and -CNT 19 are approximately halfway between -CNT 12 and 2.5 CK.

The 2.5-μs clock (2.5 CK) is further divided by a

fixed ÷40 circuit to produce the 100-μs clock providing the basic GRI resolution (100 CK). Before examining the rest of the GRI counter, the development of the A to D sample triggers will be discussed with the aid of the A to D sample trigger and GRI clock timing diagram of Fig. A-6. At the beginning of a GRI (signalled by the trailing edge of an ENDGRI pulse), a sample trigger flip-flop (STFF) is set, along with a second control flip-flop C3-5. STFF brackets all 32 sample triggers generated for one GRI, while C3-5 brackets only the first 16 triggers. With these two flip-flops set, the next 16 2.5 CK pulses are sent out as A to D sample triggers (STRG). At this point, flip-flop C3-5 is reset by count-16 gating on the ÷40 circuit, and STRG pulses are momentarily blocked. However, a feedback ÷3 counter is enabled at the same time, so that 16 more STRG pulses are enabled with a 7.5-μs spacing. Thus, the first 16 triggers initiate A to D samples every quarter-cycle of the Loran-C pulse, while the second 16 initiate samples only every three-quarters of a cycle. At the end of STRG 32, the STFF flip-flop is reset, and no more sample triggers are generated during the current GRI.

Returning to the GRI counter logic, the 100-μs clock, 100 CK, is provided to a four-decade preset counter to provide for GRI's up to 0.1 s (÷1000), with a setting resolution of 100 μs. A 16-stage digital comparator compares the output of this counter with the GRI number (BCD) set into front panel digiswitches. Refer to the GRI preset counter timing in Fig. A-7 in which an example is shown for a GRI of 15 (0.0015 s). When the counter and switch numbers are equal, an end-of-GRI pulse (ENDGRI) is generated, and the ÷1000 counter is set up for the next count; note that the counter is preset to a count of "one" for proper logic functioning. It may be recalled that the IU is designed to take samples for seven GRI's and then record the clock time and front panel data to complete one tape record. Figure A-7 is drawn to show the sixth GRI of a record just ending and the timing of the entire seventh GRI. A GRI ÷7 counter is used to count the GRI's for one record. After the sixth GRI, the counter state enables a last-GRI level, LSTGRI; this signal is used in the tape timing logic. With LSTGRI true, the next ENDGRI is gated through to produce an end-of-record pulse, ENDREC; on its trailing edge, the ÷7 counter is cleared.

The last GRI timing circuit of interest is the

parallel latch strobe, PLTCH, that is used to store the current UTC clock reading and all front panel digiswitch data. A control flip-flop is set by 2.5 CK after being enabled by ENDREC. This flip-flop then allows the next 50-ns 2.5 CK pulse to pass through as PLTCH; the flip-flop is reset by the same clock pulse. The storage latches themselves will be described in a later section. It should be noted that the UTC clock time stored by PLTCH is actually the time at the beginning of the next series of GRI measurements; this clock reading is not read out to the tape recording equipment until after the recording of A to D data for that record that follows. It will be shown later that recording of the stored clock time occurs during the seventh GRI but before ENDREC occurs.

UTC CLOCK LOGIC

The IU UTC clock is counted from the cesium 5-MHz signal (doubled to 10 MHz in the IU) and synchronized to the cesium 1 pps each second. It is manually set to correct UT, to the nearest second, via front panel digiswitches and a "TIME SET" pushbutton. The logic schematics for the IU UTC clock are given in Figs. A-8 and A-9. The first clock section consists of a ÷10 counter that divides the 10-MHz clock, CK 1, down to 1.0-Hz. A buffered 10 MHz is developed to drive all decade dividers after the first decade to limit the number of synchronous dividers in a chain to the recommended number. The CK 1 to the first decade is accordingly delayed slightly so that all decade outputs will change at the same time. It may be noted that the three slew rate clocks for the GRI slewing logic (TFST, TMED, and TSLW) are derived from this counter. Another output here is an IU-generated 1-pps signal to be used in clock time transfer measurements. Outputs from counter stages are presented to a set of shift registers as parallel input data, to be stored upon the arrival of the parallel latch strobe PLTCH. The shift register segments are connected in a serial fashion for readout to the tape multiplexer logic.

The second portion of the UTC clock logic divides the 1.0-Hz signal on down to seconds, minutes, and hours. Synchronous decade division continues as in the first portion, except that here feedback logic limits the sections to counts of 59 s, 59 min, and 23 h. Also, the parallel load inputs of these six decades are used to allow setting of the clock manually. The "TIME SET" flip-flop blocks carries between the sections

while it loads the dialed time; releasing the pushbutton allows the counter to continue. The outputs of these decades are presented to the parallel-to-serial registers for storage, as described above, and also to front panel display drivers/LED displays.

DIGISWITCH PARALLEL TO SERIAL REGISTER LOGIC

Strobing of the UTC clock time into parallel-to-serial registers at the end of a record has been described above. All front panel digiswitch data, with the exception of the UTC clock set switches, are stored in similar registers by the same parallel latch strobe PLTCH. All of these registers, including the UTC registers, are connected in a single serial string for readout to tape via the tape multiplexer logic described in the next section. Once readout begins, the UTC data are sent out first, followed by the front panel data. Figure A-10 is a logic schematic showing most of the front panel digiswitch registers. The serial output of this register chain, DSER, is sent to the serial input of the UTC register chain. Serial input data to these registers, BPS, come from registers shown in Fig. A-4, which includes the GRI number and the least significant decade of barometric pressure. Since the serial clock for all registers is 2.5 CK, a serial clock inhibit, SCI, is used to hold all register contents until the proper time. This inhibit/enable signal will be discussed in the tape multiplexer timing and control section below.

TAPE MULTIPLEXER LOGIC

The tape multiplexer logic receives a 14-bit parallel data word from the A to D converter (13 bits plus sign) and the serial data stream generated within the IU itself and formats these into a series of 8-bit parallel characters to be sent to the tape formatter unit. The multiplexer logic is given in Fig. A-11. Each A to D data word is first stored so that it can be sent as two consecutive 8-bit characters. The first character contains the sign bit (placed in the three most significant bit positions) and the upper five data bits (2^{12} down through 2^{8}), while the second character contains the eight lower-order bits (2^{7} down through 2^{0}). Serial data, CSER, are shifted into an 8-bit serial-to-parallel register continuously by 2.5 CK. The two stored A to D segments and the output of this register are sent to an 8-bit 3:1 multiplexer; the

particular character enabled through to the tape formatter inputs WD0-WD7 is determined by the two multiplexer select lines, ASEL and BSEL. The timing for multiplexer operation is described below.

TAPE MULTIPLEXER TIMING AND CONTROL

Control of the tape multiplexer logic and timing for data transfer to the tape formatter unit are accomplished in the tape multiplexer timing and control logic. Figure A-12 is a logic schematic of these functions. Figure A-13 shows the timing for a seventh GRI, including storage and transmission of the last GRI A to D samples plus transmission of the IU serial data.

Handling of the 32 A to D samples is the same for every GRI. At the beginning of the GRI, the sample trigger flip-flop STFF is set; then flip-flops FF1 and FF2 are set by the next two 2.5 CK pulses, respectively. Since the -DIV/3 level from the GRI timing logic is true for the first 16 sample triggers, flip-flop FF3 is also set at the same time as FF2. These conditions produce a binary "01" code on the ASEL, BSEL lines, causing the tape multiplexer logic to present the most significant portion of the A to D word to the tape formatter. Notice that the timing is such that this occurs after the first A to D sample has been stored. Since both halves of the A to D word must be transmitted within one 2.5-μs period, the CNT 12 pulse from the GRI timing logic is used to reset FF3 after 1.25 μs. This produces a binary "00" code on ASEL, BSEL so that the least significant portion of the A to D word is passed through the multiplexer to the tape formatter. The process continues for the first 16 A to D samples; for the second 16 A to D samples, the DIV/3 level causes FF3 to be set only every 7.5 μs to correspond to the different A to D sample rate.

As the various 8-bit characters are being presented to the tape formatter unit, a data strobe must be generated to tell the formatter that a character is present and stable for writing into the formatter's own buffer. These write-data strobes, WDS, are generated by several different flip-flops in the tape multiplexer timing logic. For strobing of A to D samples, flip-flops FF4 and FF5 are used to produce the pair of WDS pulses required for each two-character A to D word. FF4 is set by the leading edge of FF3, and FF5 is set by the trailing edge of FF3, corresponding to the enabling of the two A to D data portions in the

multiplexer. Since the outputs of FF4 and FF5 must be combined into one WDS line, these flip-flops are reset by CNT 6 and CNT 19 pulses about 650 ns after being set. The particular speed option of the tape formatter being used requires that its input data be stable approximately 250 ns before the leading edge of WDS, and that the width of WDS be at least 500 ns. To accomplish this, a one-shot delay circuit was added; the first one-shot sets up a 300-ns delay in WDS, while the second one-shot produces a WDS pulse width of 600 ns.

The STFF is reset as the 32nd sample trigger goes to the A to D converter. Control flip-flop FF1 is then reset 2.5 μs later as the 32nd sample is stored. FF3 is allowed to go through one more cycle to transmit this last A to D sample, and then FF2 and FF3 are reset until the next GRI; strobe flip-flops FF4 and FF5 are also inhibited now from generating any more WDS pulses this GRI. With FF2 and FF3 reset, ASEL and BSEL are now a binary "10" code that directs the tape multiplexer to present the output of the serial-to-parallel converter to the formatter. As FF2 is reset, it sets enable flip-flop FF6; the serial clock inhibit line SCI that has prevented shifting of data in all of the data holding registers is now released, and data begin to enter the serial-to-parallel register at a 2.5-μs rate. At the same time, a ÷8 circuit begins to count the 2.5 CK pulses. As the eighth bit of the first serial-to-parallel character is shifted into that register, a gated pulse from the ÷8 circuit sets strobe flip-flop FF7; the leading edge of FF7's output triggers the WDS one-shot circuit, and the 8-bit character is taken by the tape formatter unit. The ÷8 counter is also reset, and FF7 is reset by the next 2.5 CK pulse. This sequence of eight shift clock pulses followed by a WDS strobe continues until all serial data are sent to the tape formatter.

The record length of the particular tape formatter unit used is 512 8-bit characters; when a formatter buffer has been filled, the formatter switches the incoming data to a second buffer memory while it sends the previous record to the tape deck. This allows a continuous stream of data to be sent by the IU in 512-character groups. As previously mentioned, one record is set up to contain A to D samples from seven consecutive GRI's plus the UTC clock time and front panel data. Since 32 samples are taken each GRI and

two 8-bit characters are required for each sample, 32 x 2 x 7 = 448 characters of the record length are used up for A to D samples. This leaves 64 characters of the 512 available for the serial data. Only 29 characters are required for the UTC clock data and front panel data; the remaining characters include some hard-wired zero characters interspersed in the real data and some zero characters at the end of the serial data stream. The tape multiplexer timing circuitry contains logic for determining that 512 characters have been sent, so that the IU can send an end-of-record command, EORC, to the tape formatter. Figure A-13 shows that, after STFF is set in the seventh GRI, the last (64th) serial character data strobe is set by the 578th 2.5 CK pulse. A logic gate in the GRI timing logic (Fig. A-4) senses this and sends a reset signal, CSCI, to clear FF6 and restore the SCI. After the 64th character has been strobed, a clock signal 40QA1 from the GRI ÷40 counter is enabled by CSCI to produce the desired EORC pulse to the formatter. FF8 is required to ensure only one EORC per record; it is set when FF6 is set and is reset on the trailing edge of the EORC pulse.

Both the WDS and the EORC are gated by one side of the "RECORD" front panel switch so that these commands, which are continuously generated, are sent to the formatter only when recording is desired. Note that the WDS test point, TP7, may be used even if not recording. A fixed rewind command level, REWC, is sent to the formatter for proper operation. A front panel "FILE" pushbutton is used to send an end-of-file command, EOFC, to the formatter when a data run is complete; note that this command may be set only when the "RECORD" switch is off.

A TO D SAMPLE MONITOR LOGIC

Sampling logic was included in the IU to permit continuous visual monitoring of two adjacent A to D sample values 2.5 μs apart. Normally, the values monitored would be the quadrature samples produced by the 15th and 16th sample triggers to the A to D converter (third zero crossing and next positive peak of a Loran-C pulse). A logic schematic of this circuitry is given in Fig. A-14. Since only moderate resolution is required by the monitors, the sign bit and upper seven A to D data bits are used. Inputs to the monitor storage registers are from the A to D storage registers in the tape multiplexer logic. When

the GRI timing logic has been slewed to the proper place on the Loran-C pulse, monitor gating produces two latch strobes shortly after the storage of the 15th and 16th samples in the tape multiplexer. The monitor register contents are updated each GRI. The outputs of these two registers are D to A converted and averaged in 2-s integrators to provide a useful analog output to two external voltmeters. The D to A converters have a unipolar 0- to 10-V output, so +5 V on a meter (mid-scale) represents a zero voltage reading by the A to D converter.

TAPE RECORDING MONITOR LOGIC

Special logic is shown in Fig. A-14 to indicate to the operator that a parity error has occurred in the tape formatter buffer memory. The formatter itself detects the error and sends a pulse to the IU. Here the pulse sets a flip-flop for retention of the error detection. A special alarm circuit is enabled by the flip-flop output; it produces both a visual indication via a front panel LED and a 1-kHz tone via a local speaker to alert the operator. If the operator can clear the fault indication by pushing the error "RESET" button on the front panel, the error was a transient one and recording is not stopped.

A "File Mark Reminder" circuit is included to ensure that the operator records a file mark on the tape after he completes a recording cycle. A front panel LED is turned on whenever the "RECORD" switch is turned on, and the "FILE" switch must be depressed to turn the LED off.

INTERFACE UNIT POWER SUPPLY

All DC power required by the IU is provided by a separate power supply chassis. A schematic drawing showing both the power supply wiring and power distribution within the IU is given in Fig. A-15.

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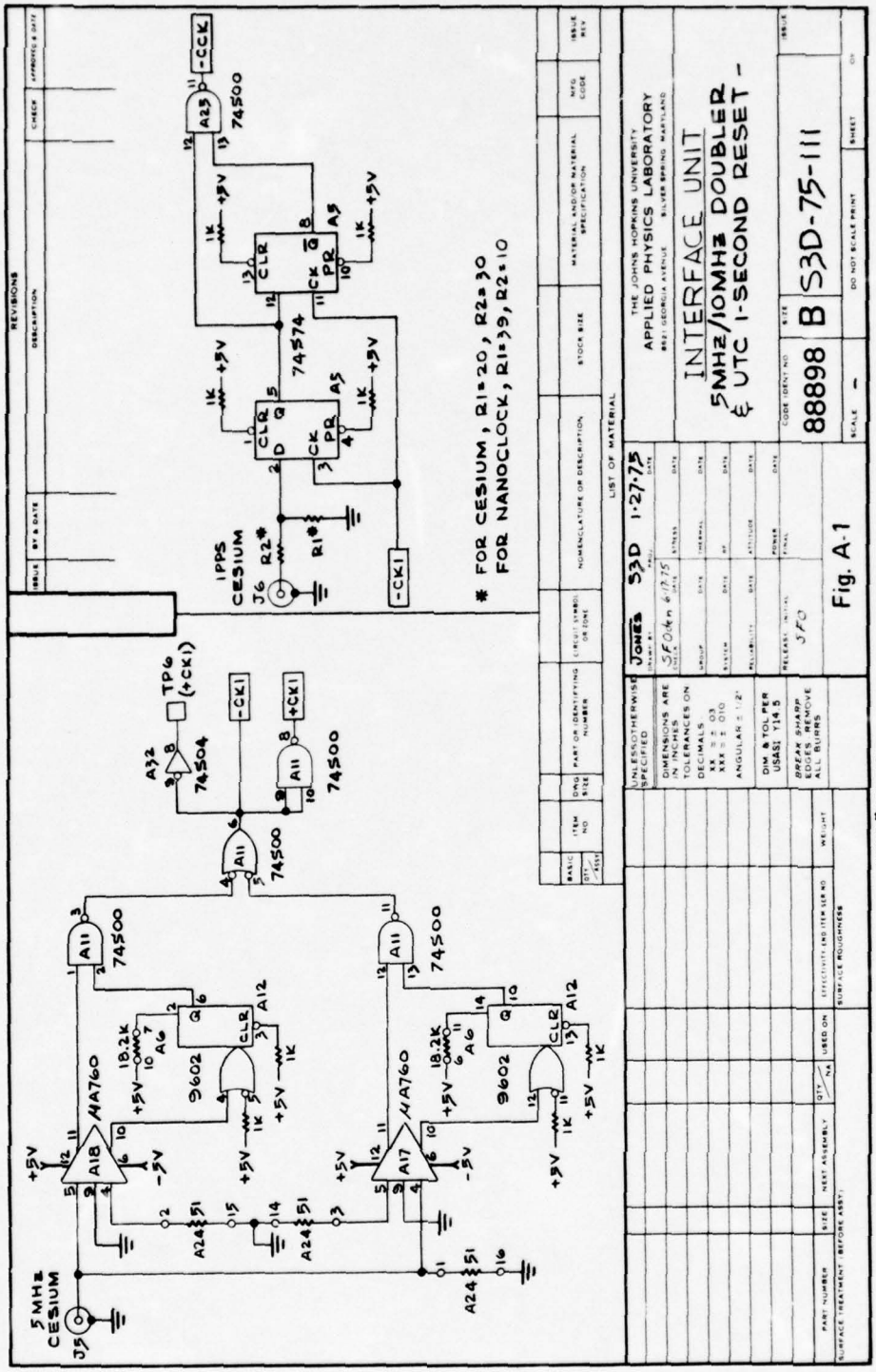
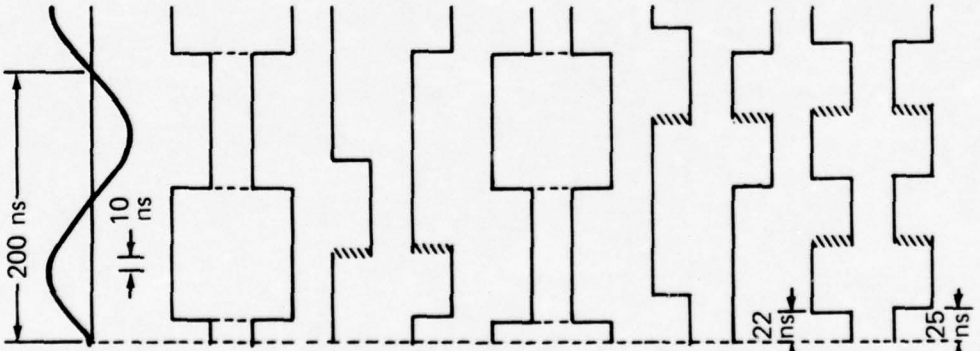


Fig. A-1

FORM # SDO-201

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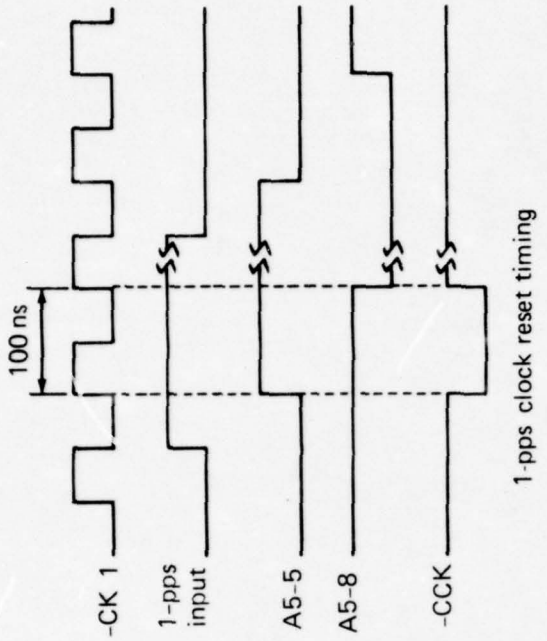
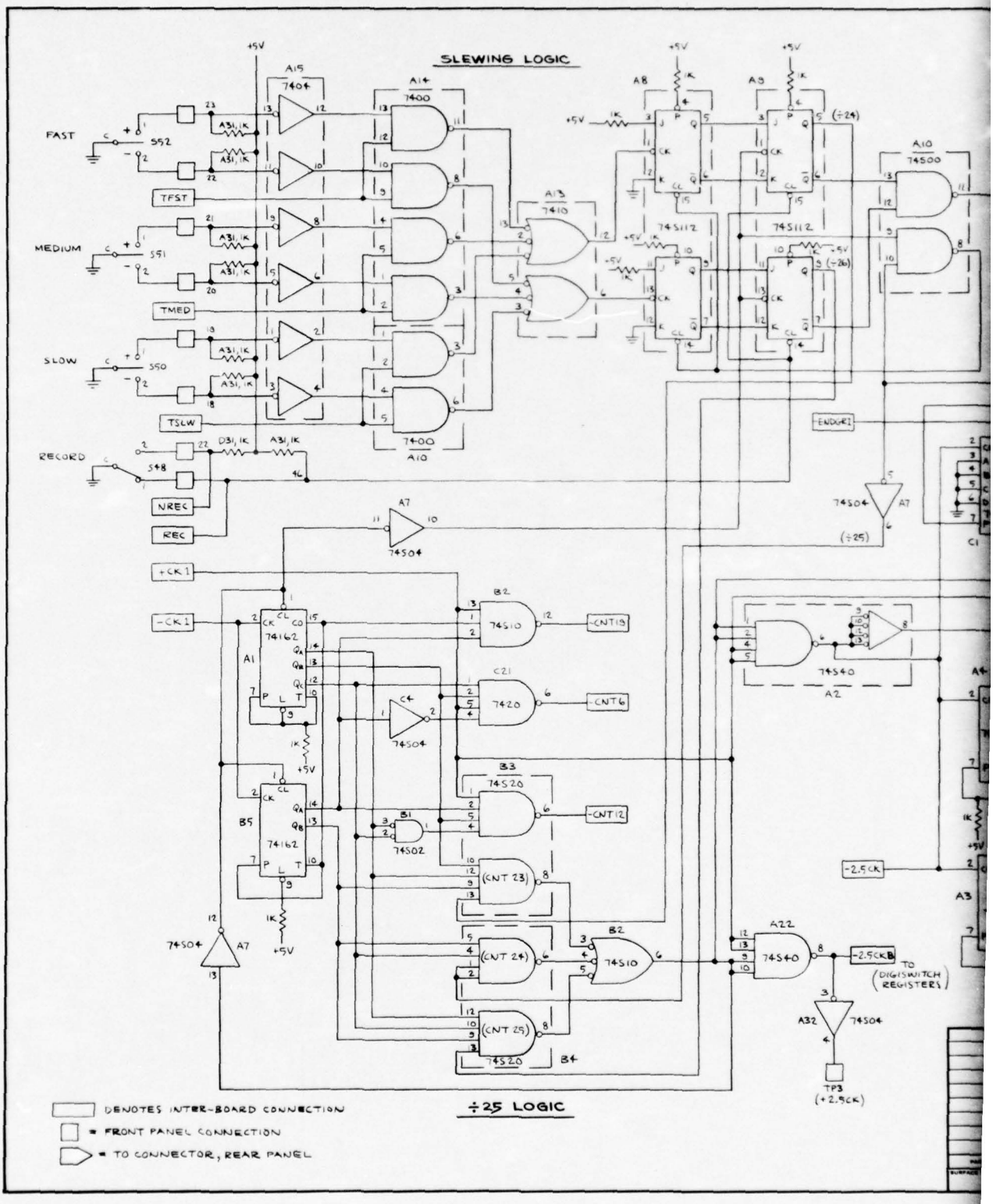
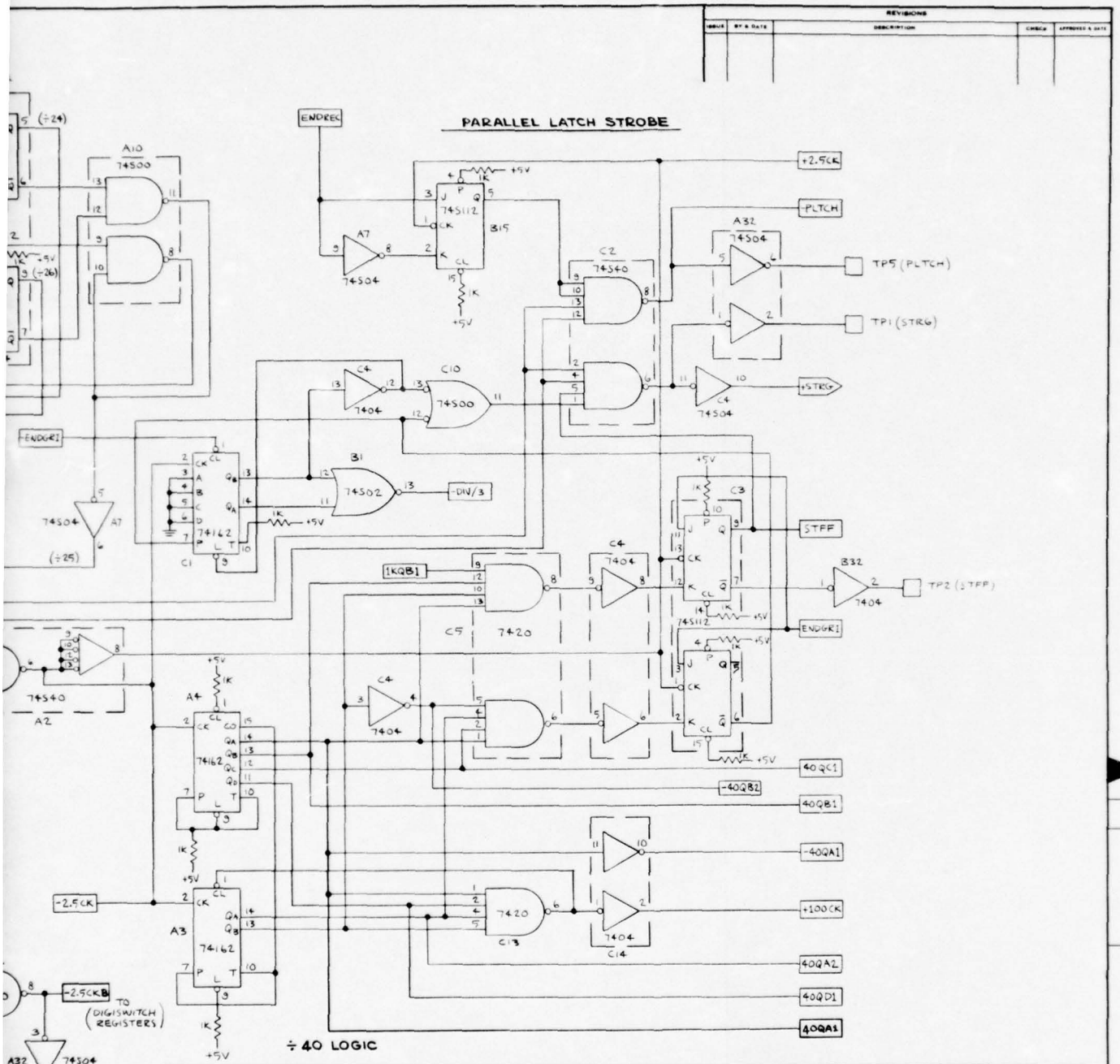


Fig. A-2 5-MHz/10-MHz Frequency Doubler and 1-pps Timing

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UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS
XX ± .03
XXX ± .010
ANGULAR ± 1/2°
DIM & TOL PER USASI Y14.5
BREAK SHARP EDGES REMOVE ALL BURRS

WM WERNER S3D 11-12-74
SEQden 6-17-75
RELEASE INITIAL SFO

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INTERFACE UNIT
SLEWING LOGIC & GRI TIMING

CODE IDENT NO 88898 | SIZE D | S3D-74-105 | ISSUE

SCALE | DO NOT SCALE PRINT | SHEET 1 OF 2

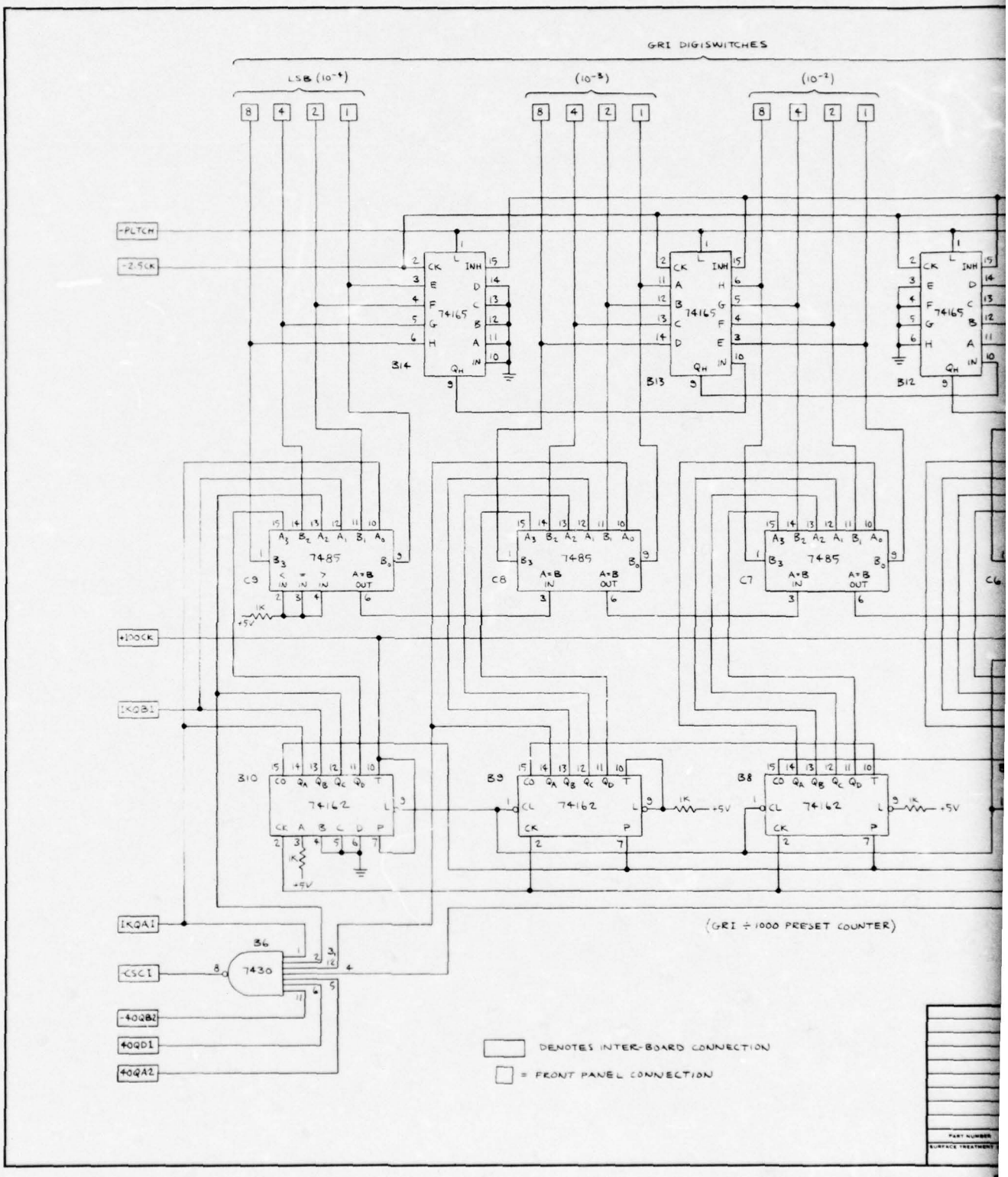
PART NUMBER | SIZE | NEXT ASSEMBLY | QTY/NA | USED ON | EFFECTIVITY (PO ITEM SER NO) | WEIGHT
SURFACE TREATMENT (BEFORE ASSY) | SURFACE ROUGHNESS

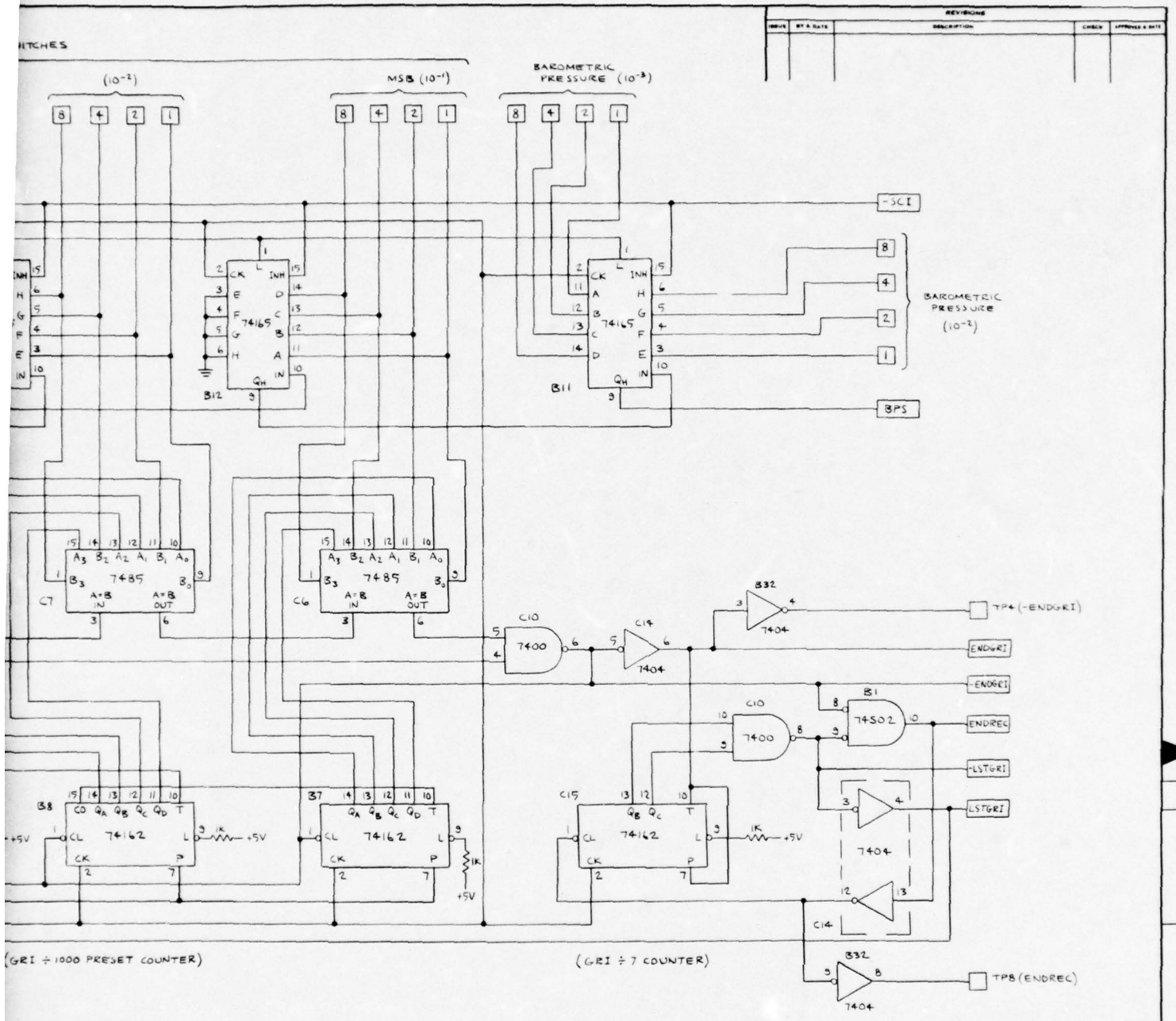
Fig. A-3

FORM ● SDO-401

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LAUREL MARYLAND





UNLESS OTHERWISE SPECIFIED	WM WERNER S3D 11-20-74
DIMENSIONS ARE IN INCHES	S.F. Oden 6-17-75
TOLERANCES ON DECIMALS XX ± .03 XXX ± .010 ANGULAR ± 1/2°	
DIN & TOL PER USASI Y14.5	
BREAK SHARP EDGES REMOVE ALL BURRS	
RELEASE: INITIAL SFO	FINAL

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INTERFACE UNIT
GRI TIMING

CODE IDENT NO	SIZE		ISSUE
88898	D	S3D-74-105	
SCALE	DO NOT SCALE PRINT	SHEET 2 OF 2	

Fig. A-4

FORM # SDO-401

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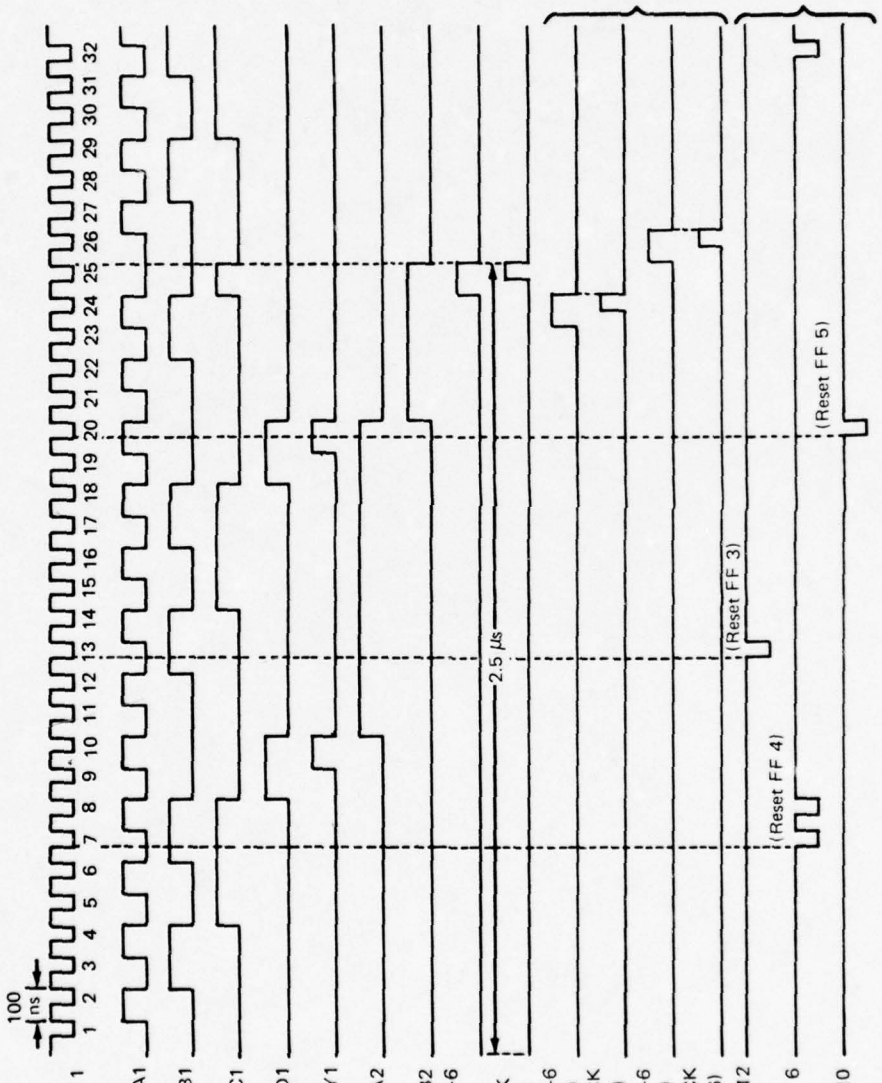


Fig. A-5 2.5-μs Timing for GRI and Tape Format Logic

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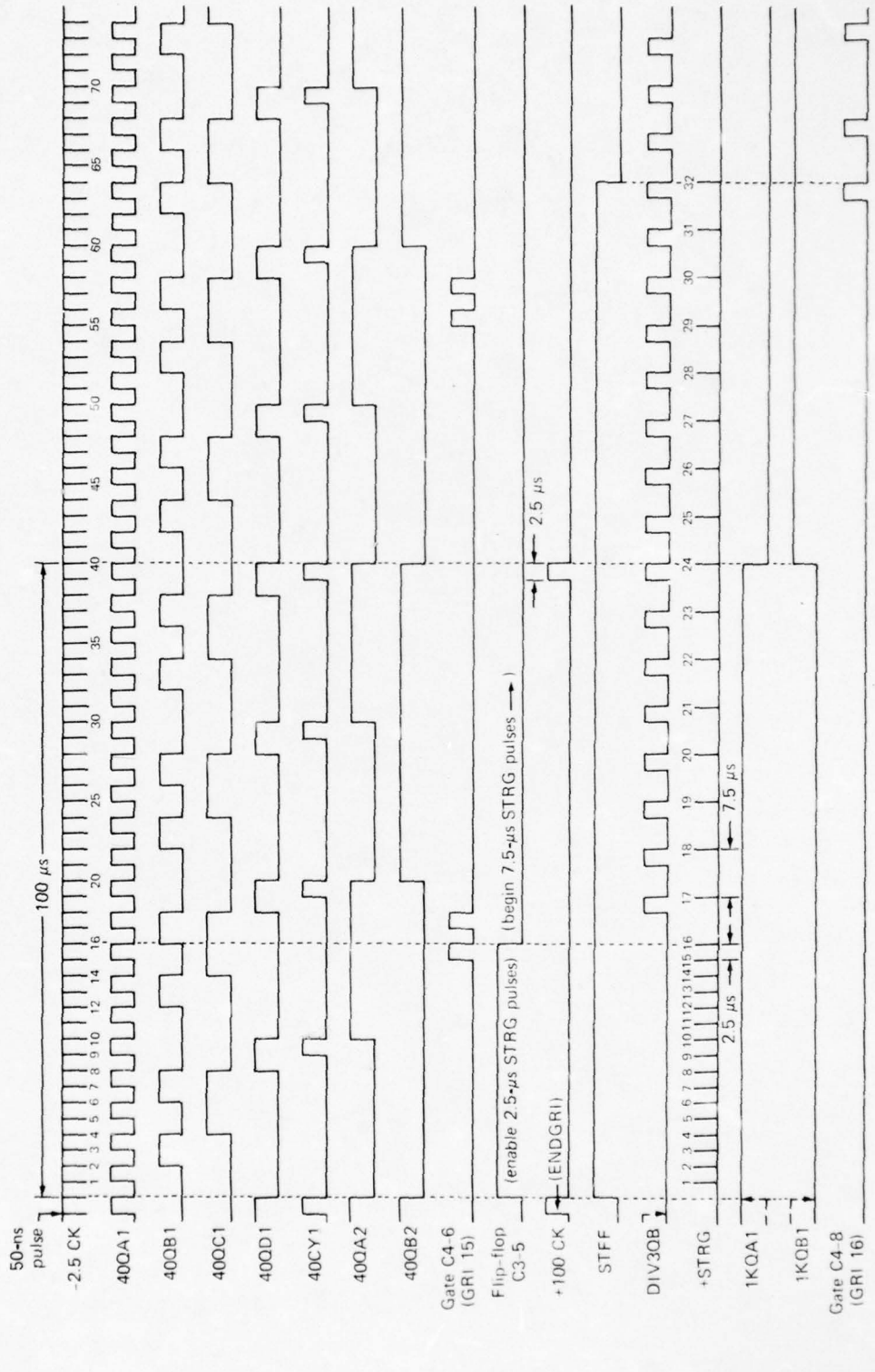


Fig. A-6 A to D Sample Trigger and GRI Clock Timing

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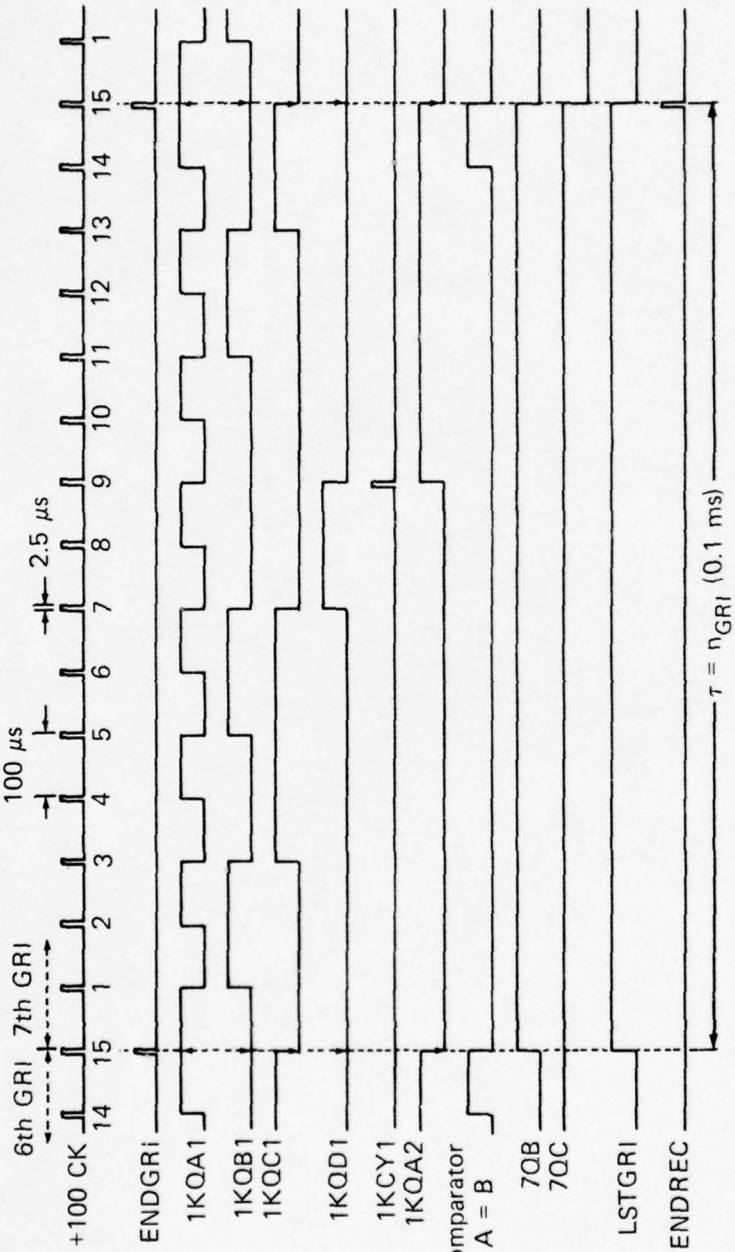
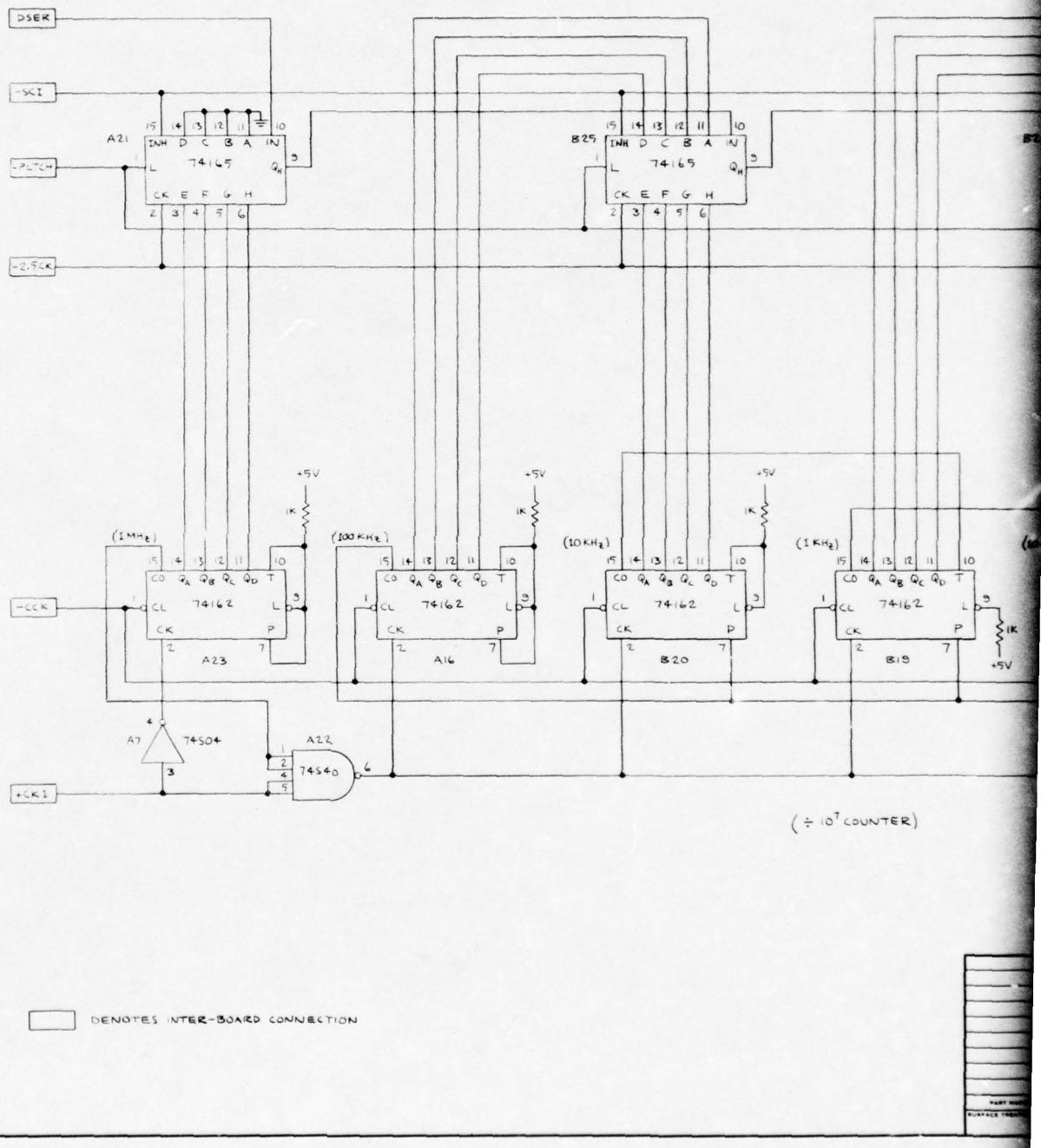


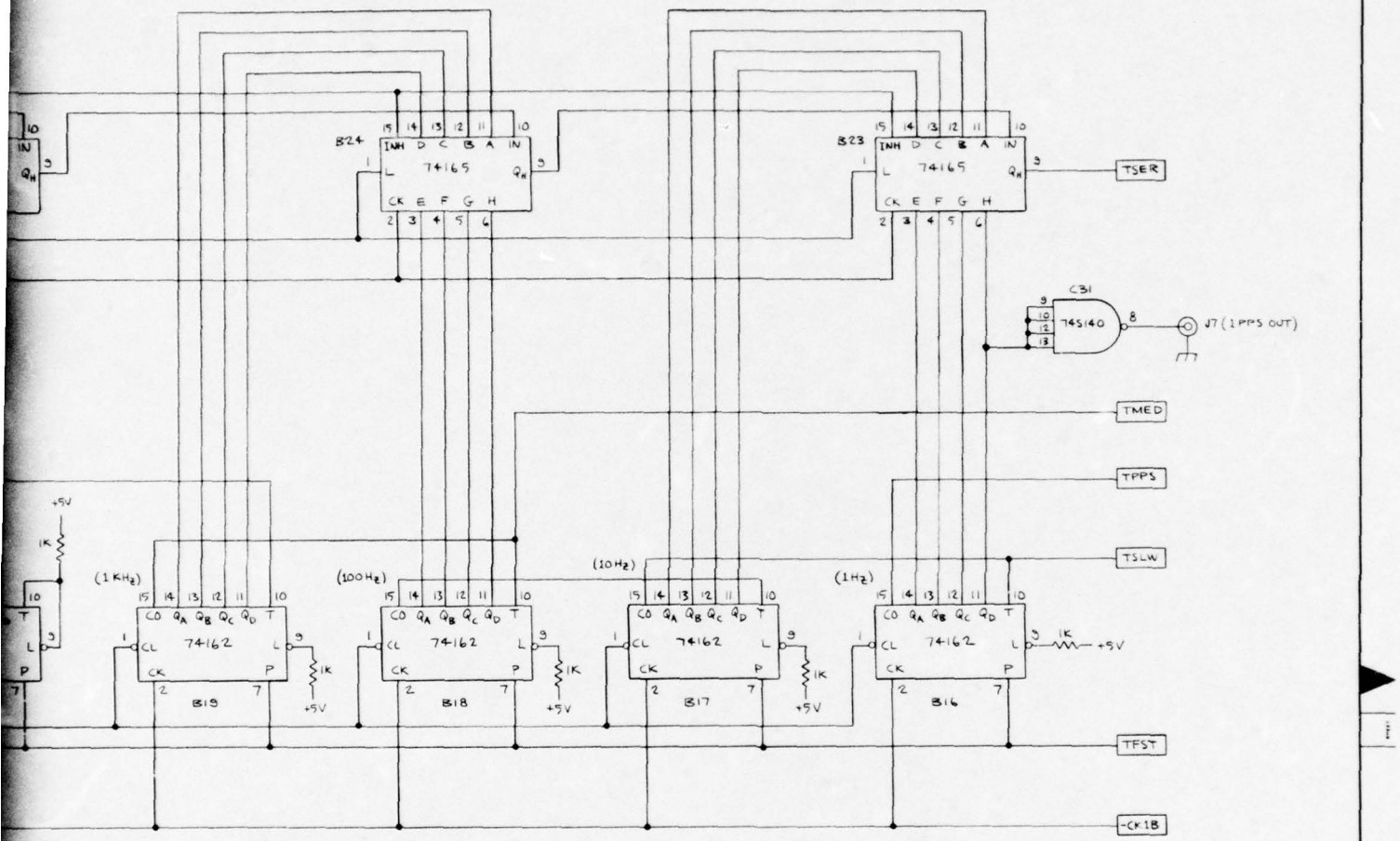
Fig. A-7 GRI Preset Counter Timing

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(÷ 10^7 COUNTER)

LIST OF MATERIAL

BASIC QTY. / SHT	ITEM NO.	DWG SIZE	PART OR IDENTIFYING NUMBER	CIRCUIT SYMBOL OR ZONE	NOMENCLATURE OR DESCRIPTION	STOCK SIZE	MATERIAL AND/OR MATERIAL SPECIFICATION	MFG CODE	ISSUE REV

PART NUMBER	SIZE	NEXT ASSEMBLY	QTY / NA	USED ON	EFFECTIVITY-END ITEM SER NO.	WEIGHT
SURFACE TREATMENT (BEFORE ASSY)					SURFACE ROUGHNESS	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS
XX = ± .03
XXX = ± .010
ANGULAR ± 1/2°
DIM & TOL PER USASI Y14.5
BREAK SHARP EDGES. REMOVE ALL BURRS

DRAWN BY: W^S WEENER S3D 11-27-74
CHECK: S F Oden 6-17-75
RELEASE: INITIAL S F O

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INTERFACE UNIT
UTC CLOCK

CODE IDENT NO. 88898 | SIZE D | S3D-74-106 | ISSUE

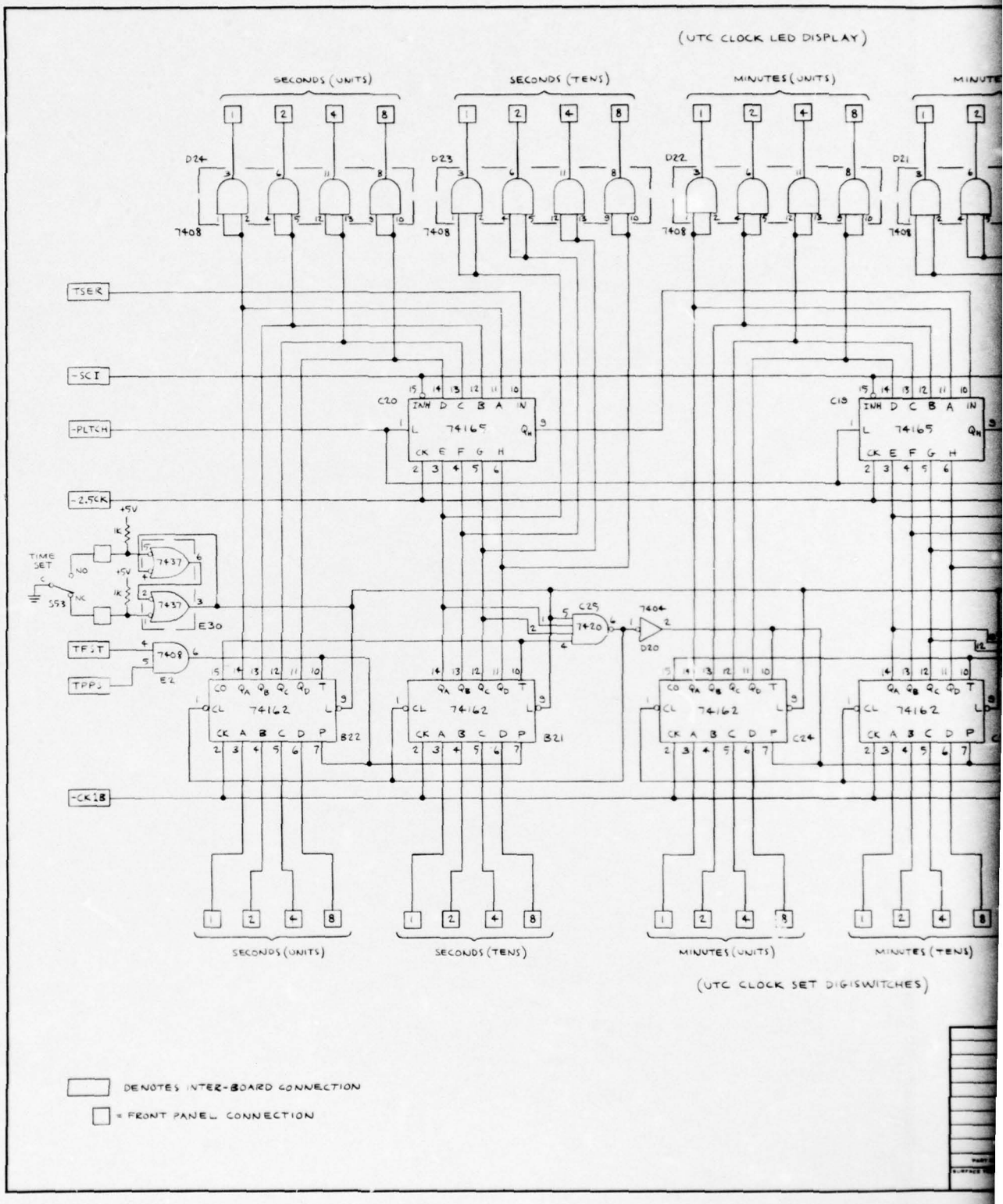
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Fig. A-8

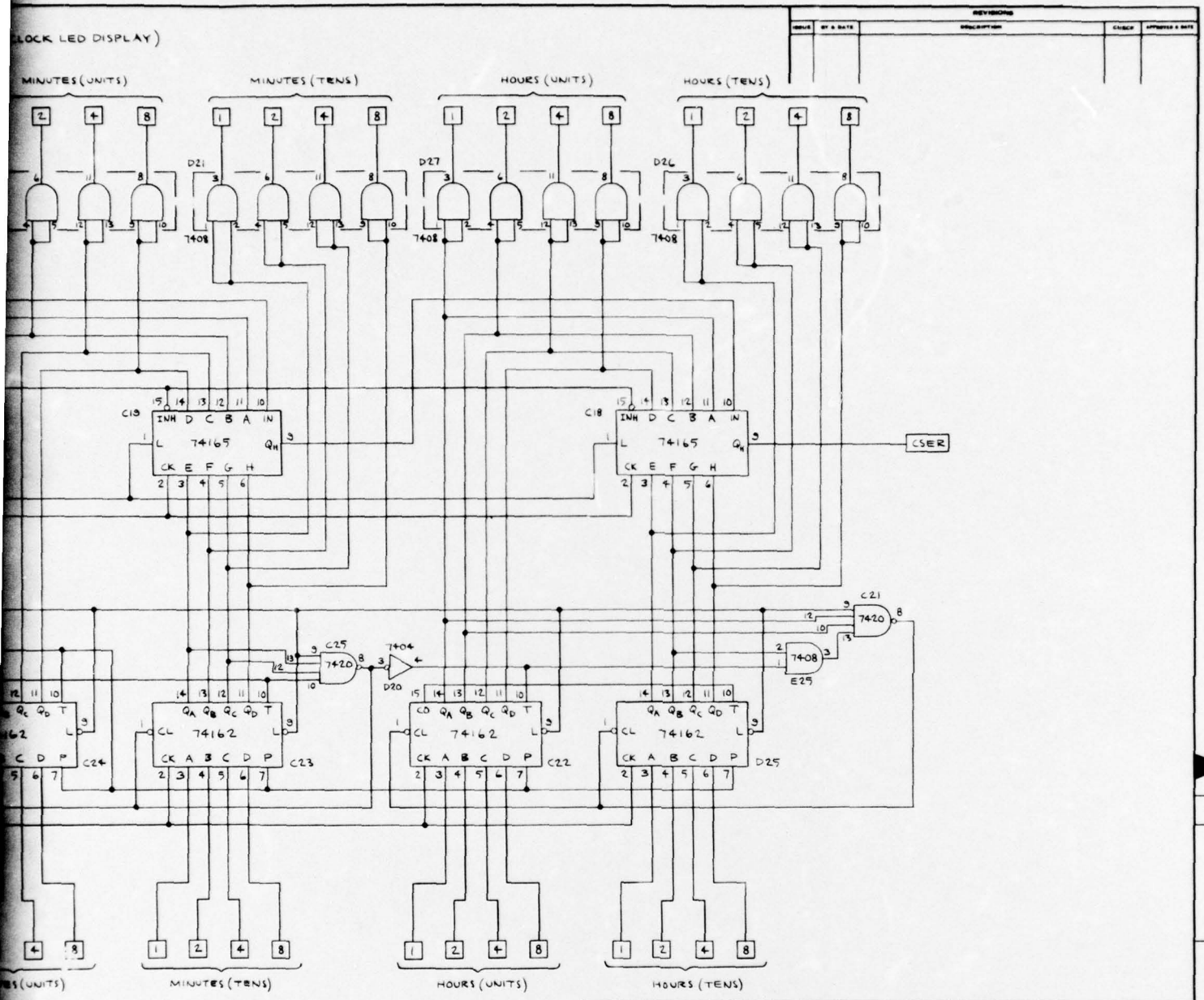
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CLOCK LED DISPLAY)



TC CLOCK SET DIGISWITCHES)

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BASIC QTY/ASSY	ITEM NO.	DWG SIZE	PART OR IDENTIFYING NUMBER	CIRCUIT SYMBOL OR ZONE	NOMENCLATURE OR DESCRIPTION	STOCK SIZE	MATERIAL AND/OR MATERIAL SPECIFICATION	MFG CODE	ISSUE REV
					LIST MATERIAL				

PART NUMBER	SIZE	NEXT ASSEMBLY	QTY/NHA	USED ON	EFFECTIVITY (SEE ITEM SER NO)	WEIGHT
SURFACE TREATMENT (BEFORE ASSY)					SURFACE ROUGHNESS	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS
XX ± ± .03
XXX ± .010
ANGULAR ± 1/2°
DIM & TOL PER USASI Y14.5
BREAK SHARP EDGES REMOVE ALL BURRS

DRAWN BY: WM WERNER S3D 12-5-74
CHECK: SFOden 6-17-75
GROUP / SYSTEM / RELIABILITY / PROJ / STRESS / THERMAL / WT / ATTITUDE / POWER
RELEASE INITIAL: SFO FINAL

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INTERFACE UNIT
UTC CLOCK

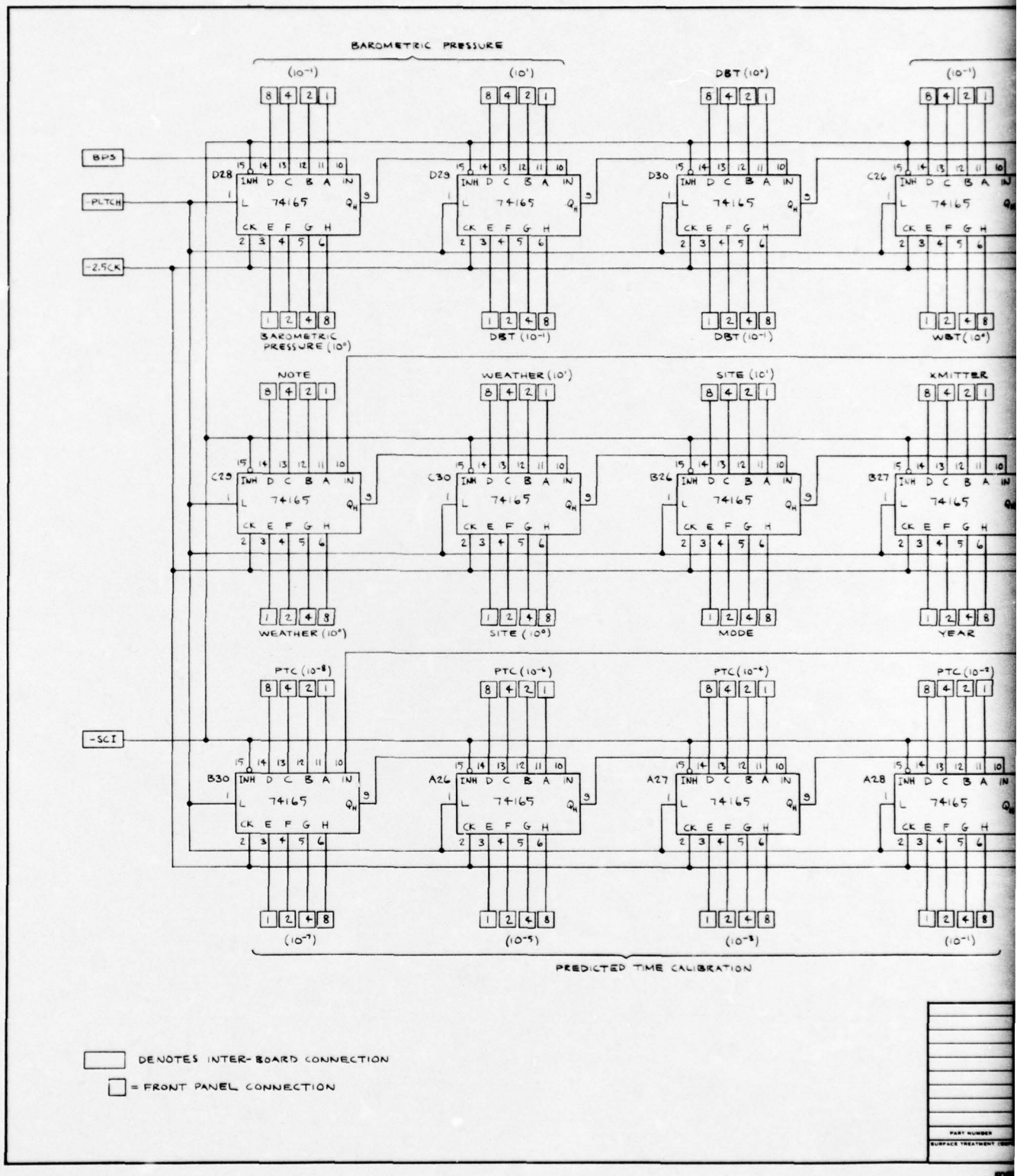
CODE IDENT NO 88898 | SIZE D | S3D-74-106 | ISSUE
SCALE | DO NOT SCALE PRINT | SHEET 2 OF 2

Fig. A-9

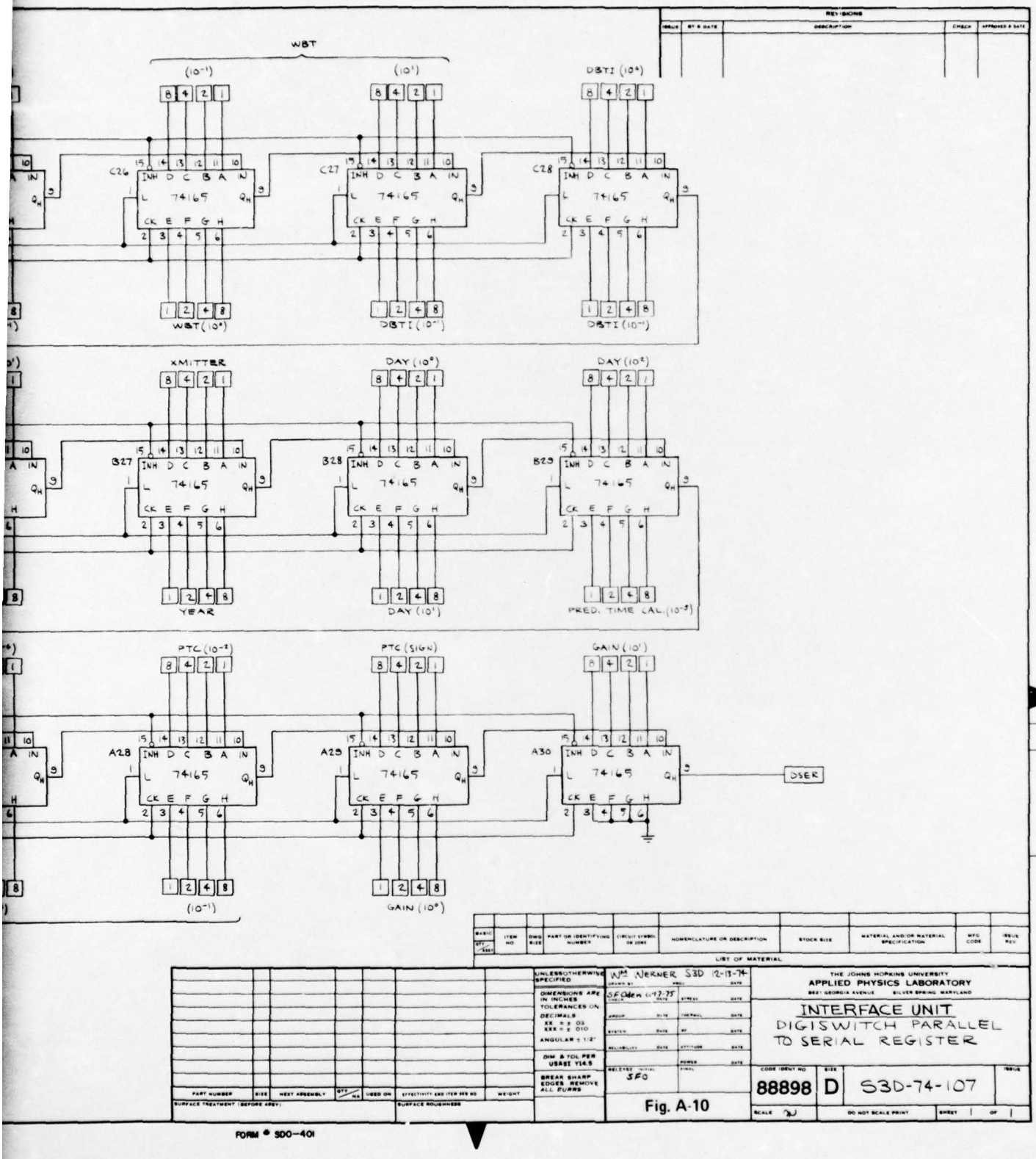
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BASIC QTY/ASSY	ITEM NO	DWG SIZE	PART OR IDENTIFYING NUMBER	CIRCUIT SYMBOL OR LOCATE	NOMENCLATURE OR DESCRIPTION	STOCK SIZE	MATERIAL AND/OR MATERIAL SPECIFICATION	MFG CODE	ISSUE REV

PART NUMBER	SIZE	NEXT ASSEMBLY	QTY/NA	USED ON	EFFECTIVITY AND ITEM REV NO	WEIGHT
SURFACE TREATMENT (BEFORE ASSY)					SURFACE ROUGHNESS	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS
XX ± .03
XXX ± .010
ANGULAR ± 1/2°
DIM & TOL PER USASI Y14.5
BREAK SHARP EDGES. REMOVE ALL BURRS

DRAWN BY: Wm. NERNER S3D 12-13-74
CHECK: S.F. Oden 6-12-75
GROUP
SYSTEM
RELIABILITY
PROJ
STRESS
THERMAL
RF
ATTITUDE
POWER
FINAL
RELEASE INITIAL: SFO

Fig. A-10

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INTERFACE UNIT
DIGISWITCH PARALLEL
TO SERIAL REGISTER

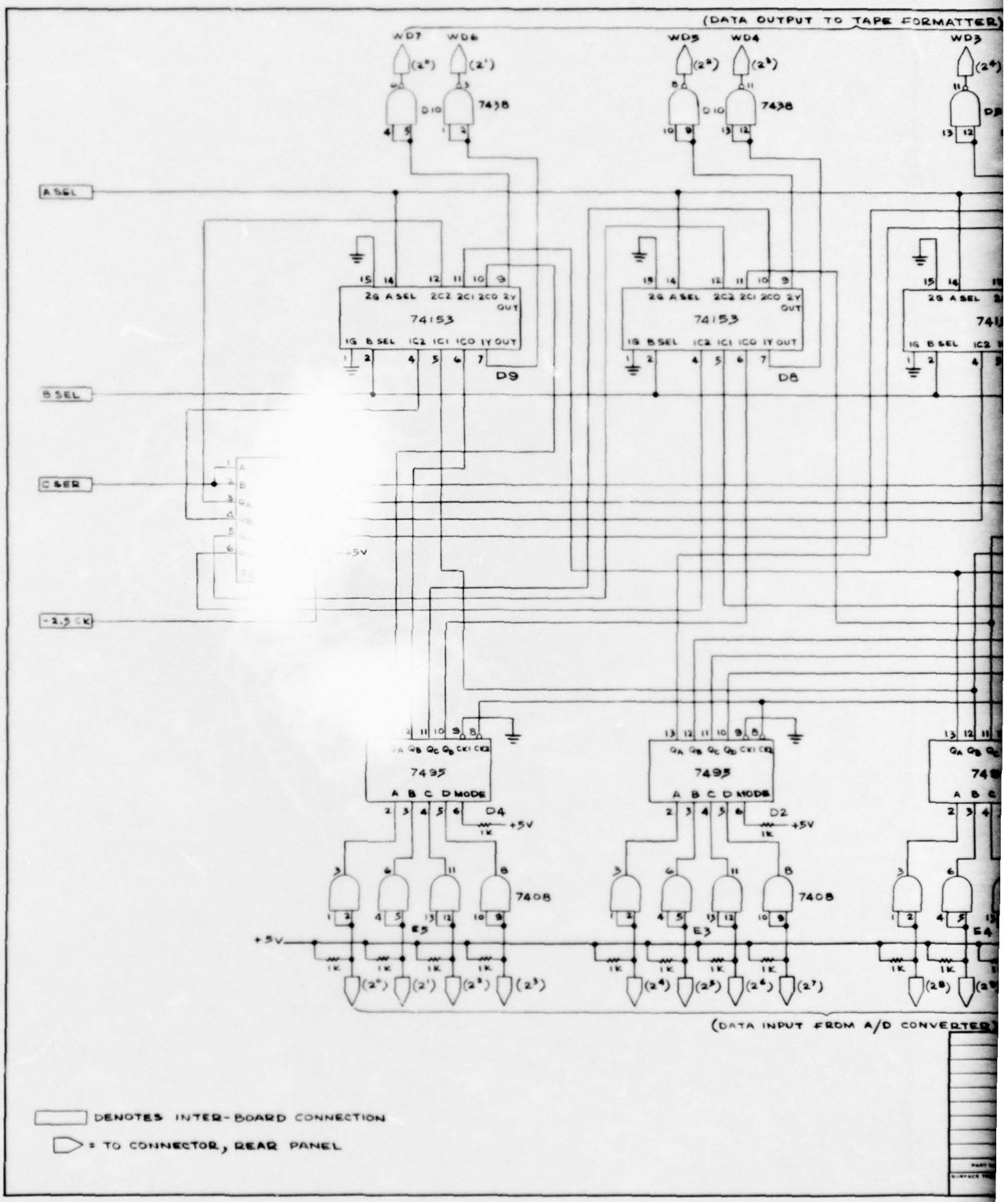
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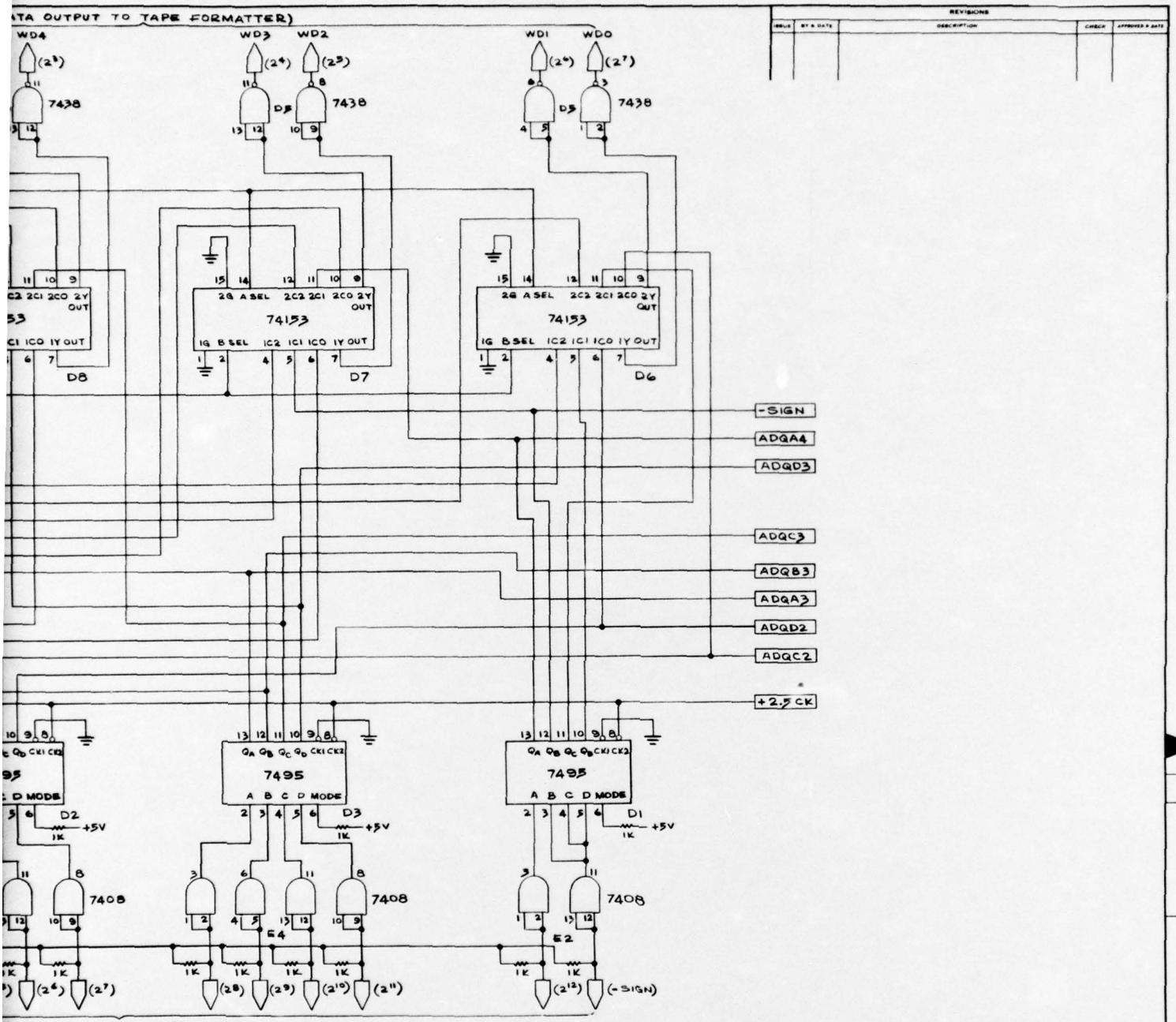
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UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS
XX = ± .03
XXX = ± .010
ANGULAR ± 1/2°
DIM. & TOL PER USASI Y14.5
BREAK SHARP EDGES REMOVE ALL BURRS

JONES S3D 1-9-75
SFOden 6-17-75
SFO

Fig. A-11

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INTERFACE UNIT
TAPE MULTIPLEXER LOGIC

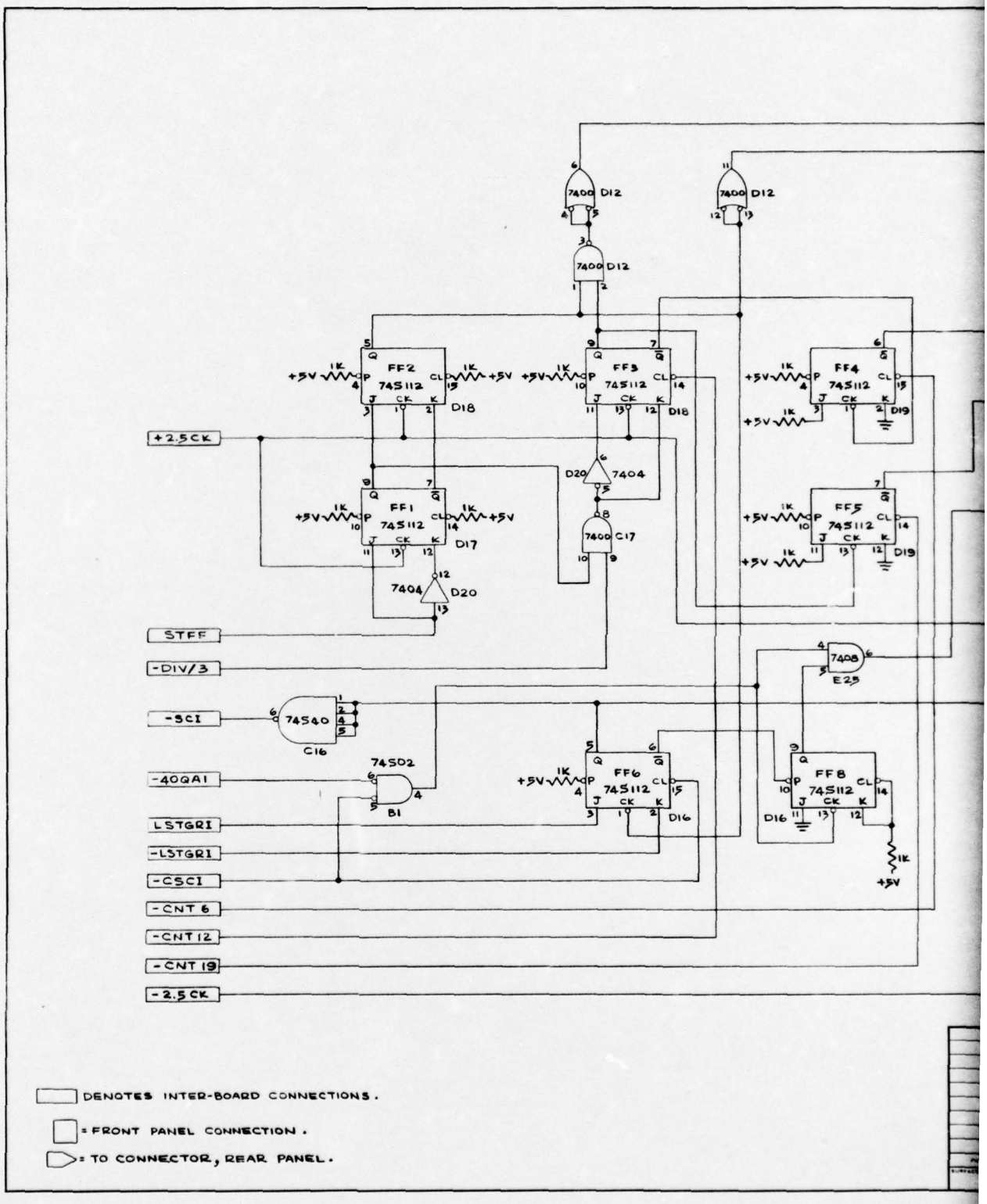
CODE IDENT NO. 88898 | SIZE D | S3D-75-108 | ISSUE

SCALE — | DO NOT SCALE PRINT | SHEET 1 OF 1

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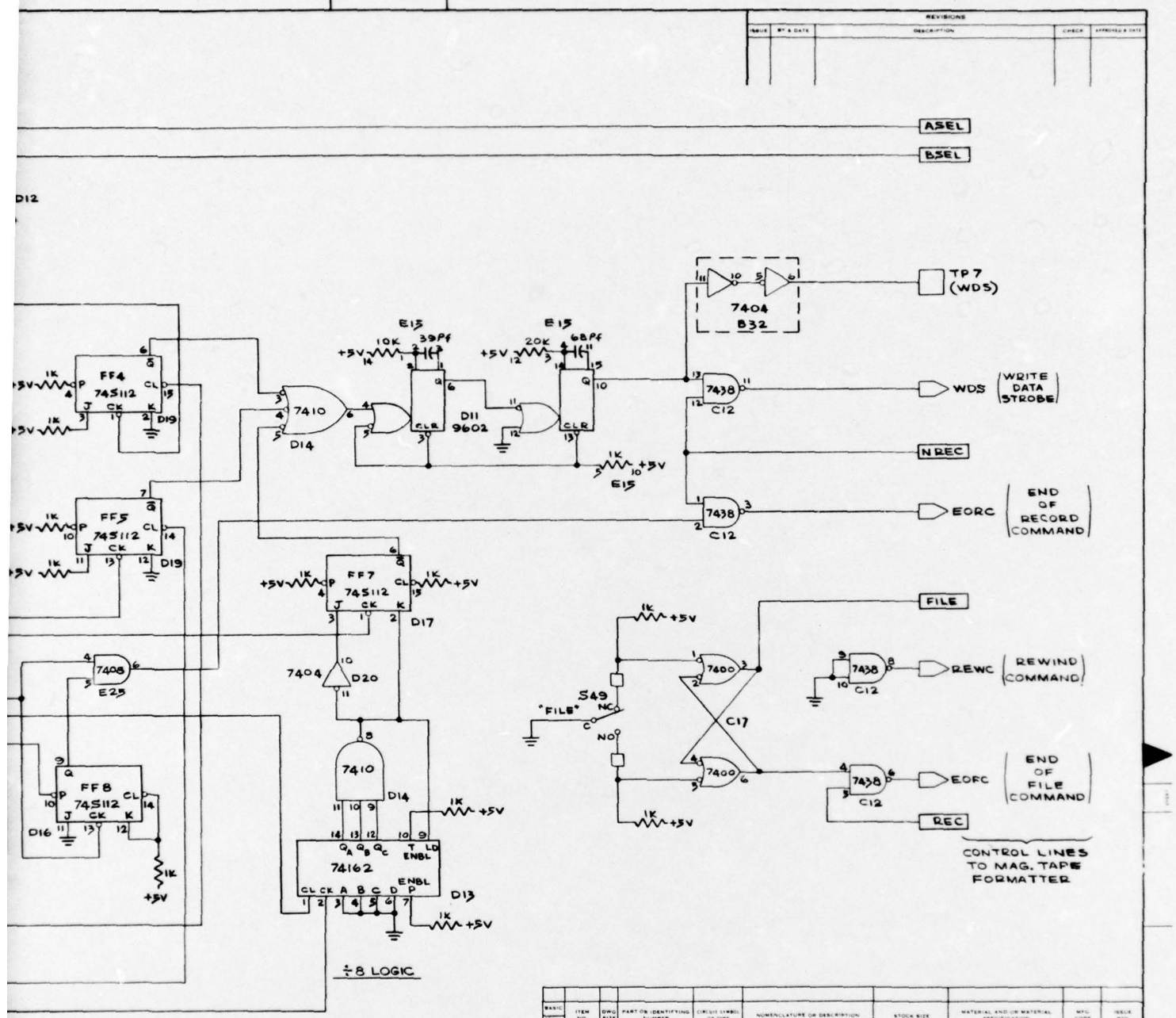

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D16
7410
D14
7404
D20
7408
E23
E13
10K
39Pf
E15
20K
68Pf
D11
9602
1K
+5V
7404
B32
TP7
(WDS)
7438
C12
WDS
WRITE DATA STROBE
NREC
EORC
END OF RECORD COMMAND
7400
C17
S49
"FILE"
NC
NO
FILE
REWC
REWIND COMMAND
EOFC
END OF FILE COMMAND
REC
CONTROL LINES TO MAG. TAPE FORMATTER
74162
ENBL
÷8 LOGIC
LIST OF MATERIAL
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS
ANGULAR ± 1/2°
DIM & TOL PER USAS Y14.5
BREAK SHARP EDGES. REMOVE ALL BURRS
JOHNS S3D 1-23-75
SFOden 6-17-75
SFO
THE JOHNS HOPKINS UNIVERSITY
APPLIED PHYSICS LABORATORY
8621 GEORGIA AVENUE SILVER SPRING, MARYLAND
INTERFACE UNIT
TAPE MULTIPLEXER
TIMING & CONTROL
CODE IDENT NO 88898
SIZE D
S3D-75-109
SCALE —
DO NOT SCALE PRINT
SHEET
FORM # SDO-401

Fig. A-12

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LAUREL, MARYLAND

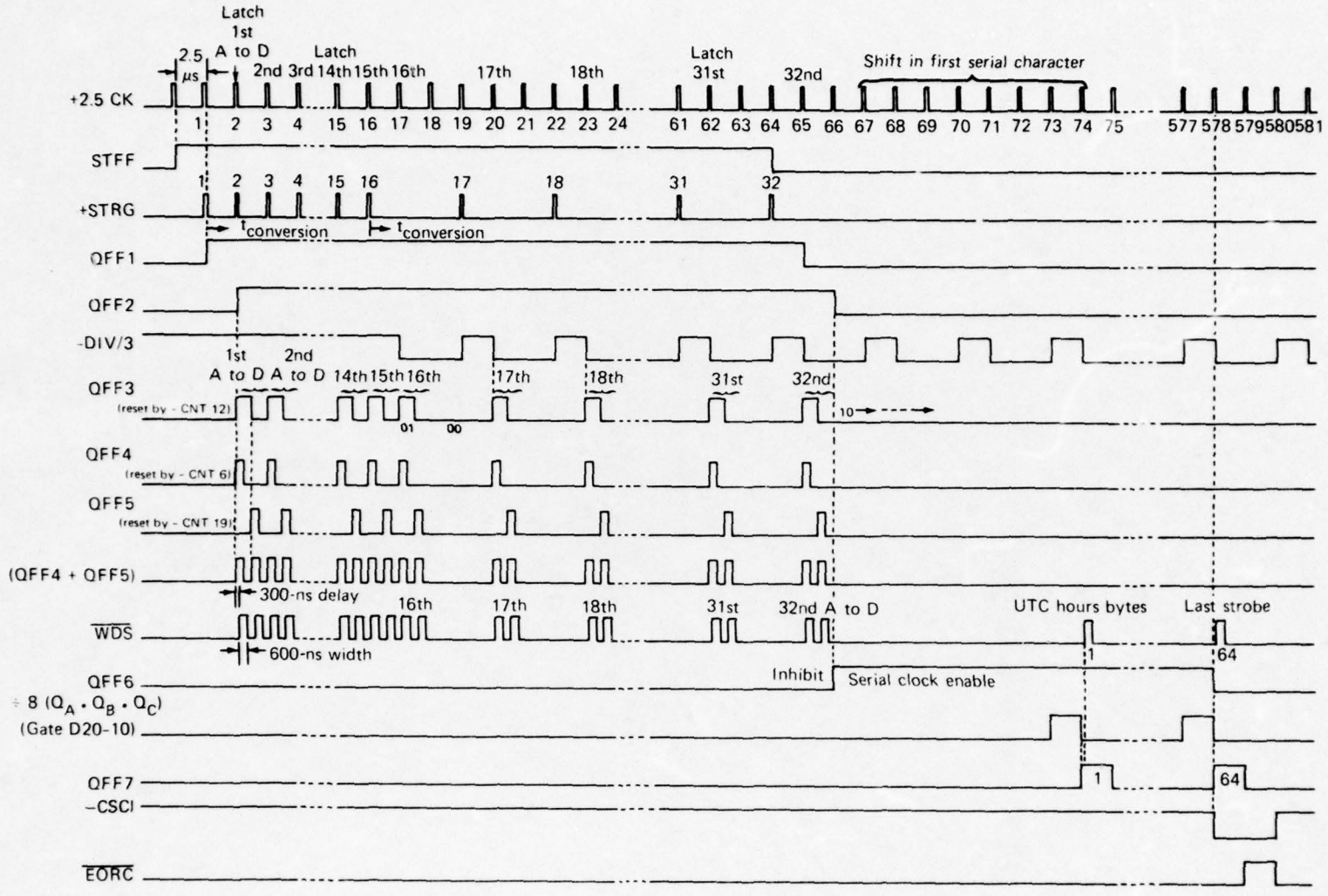
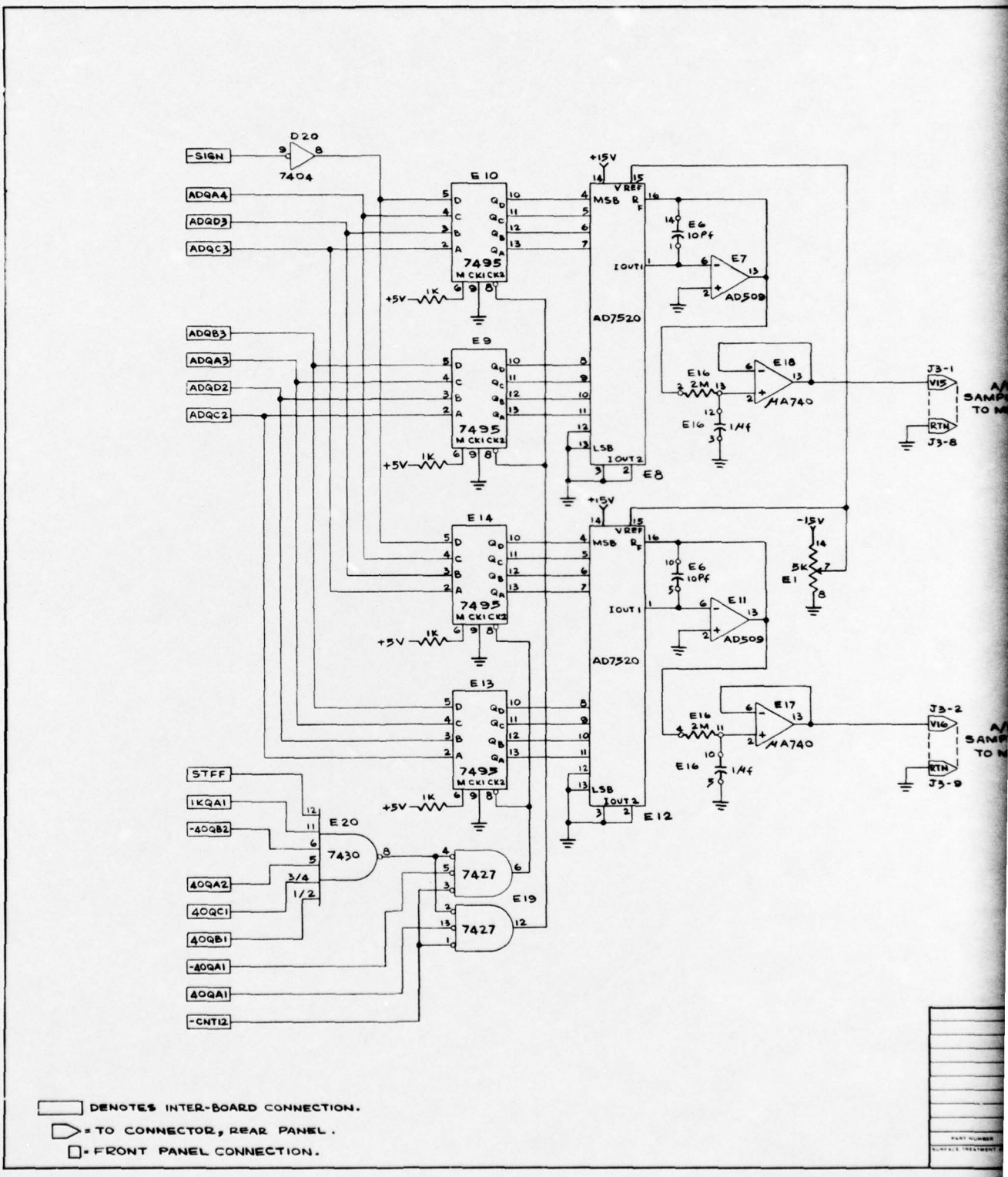


Fig. A-13 Tape Format Timing

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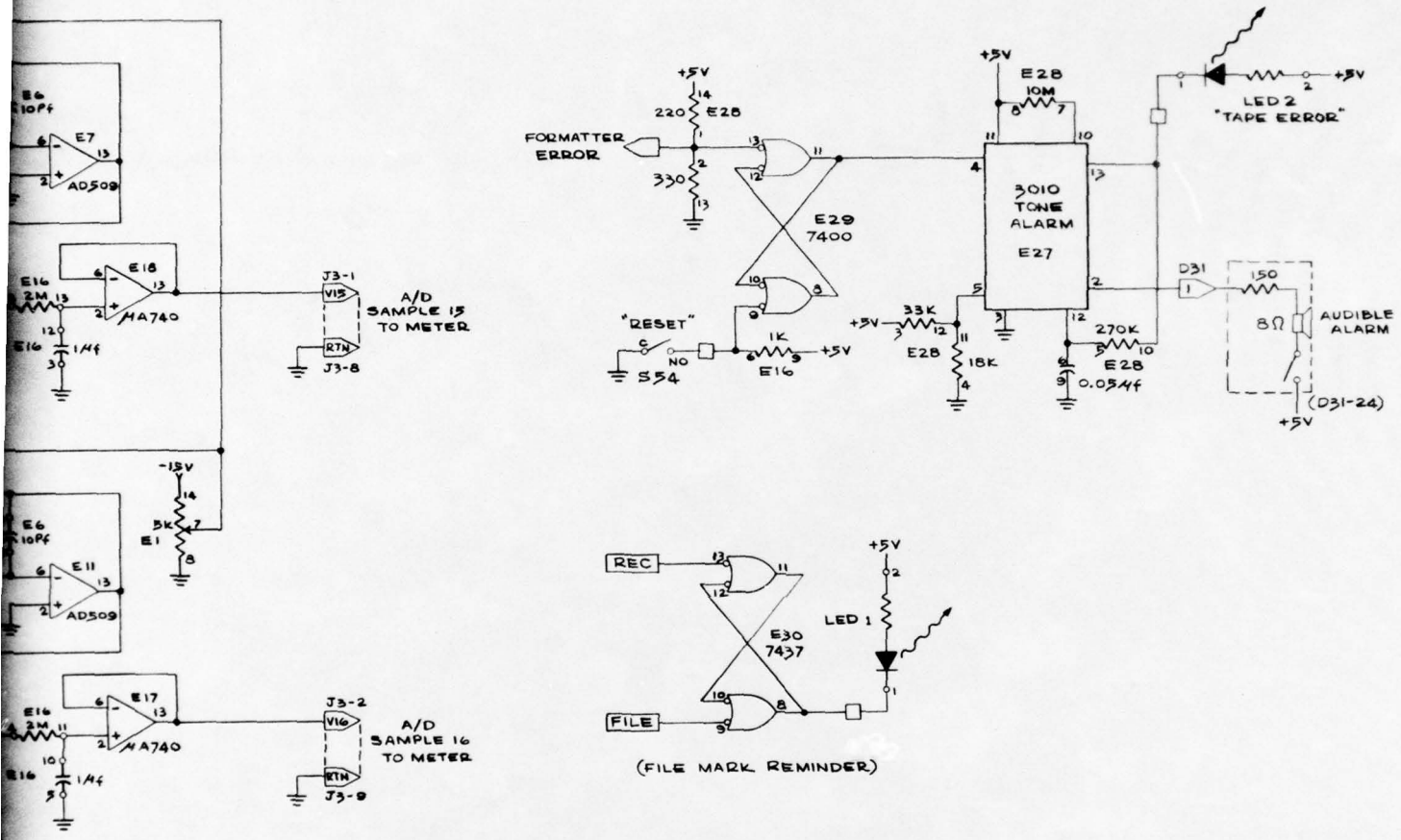
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MARK	ITEM NO.	DWG SIZE	PART OR IDENTIFYING NUMBER	CIRCUIT SYMBOL OR ZONE	NOMENCLATURE OR DESCRIPTION	STOCK SIZE	MATERIAL AND/OR MATERIAL SPECIFICATION	MFG CODE	ISSUE REV
QTY / ASSY									

LIST OF MATERIAL

PART NUMBER	SIZE	NEXT ASSEMBLY	QTY / NA	USED ON	EFFECTIVITY END ITEM SER NO	WEIGHT
SURFACE TREATMENT (BEFORE ASSY)					SURFACE ROUGHNESS	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON:
DECIMALS
XX ± ± .03
XXX ± ± .010
ANGULAR ± 1.2°
DIM & TOL PER US "Y" Y14.5
BREAK SHARP EDGES, REMOVE ALL BURRS

DRAWN BY	JONES	S3D	1·23·75
CHECK	SFOden 6-17-75	STRESS	DATE
GROUP	DATE	THERMAL	DATE
SYSTEM	DATE	EE	DATE
RELIABILITY	DATE	ANTENNA	DATE
SDO	DATE	POWER	DATE
RELEASE INITIAL	SFO	FINAL	

Fig. A-14

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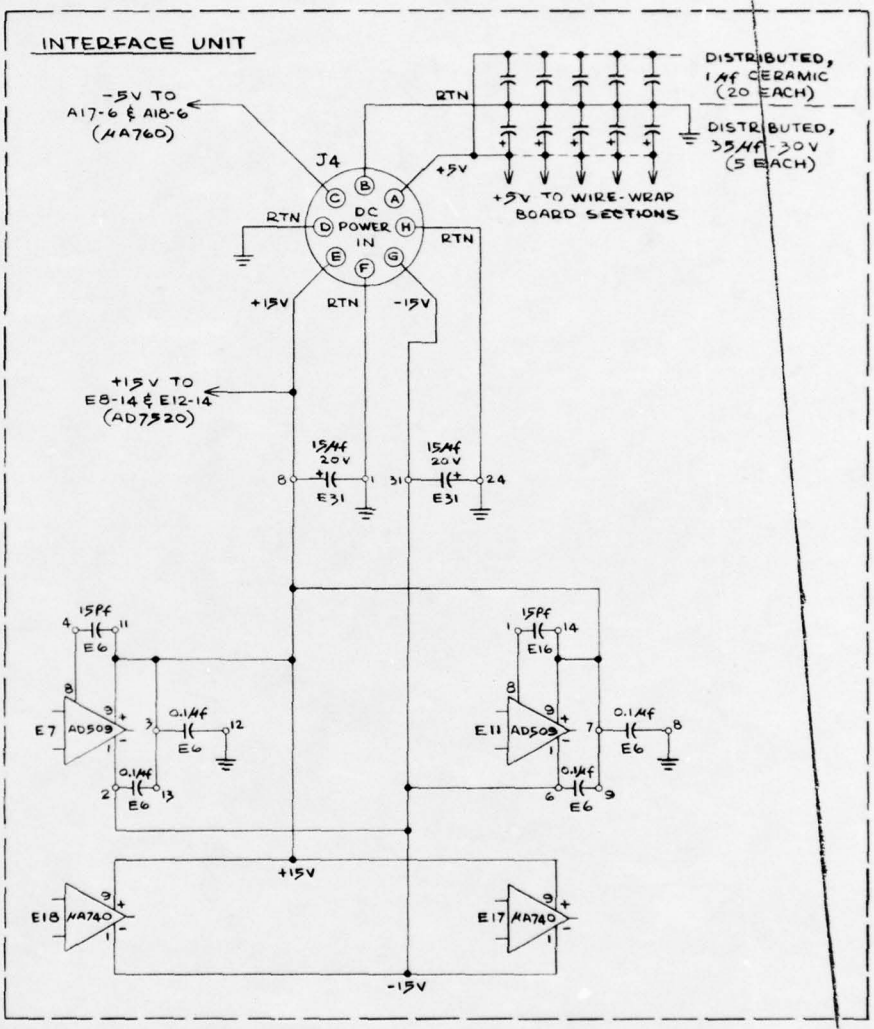
INTERFACE UNIT
MISCELLANEOUS MONITOR LOGIC

CODE IDENT NO	SIZE		ISSUE
88898	D	S3D-75-110	
SCALE —	DO NOT SCALE PRINT		SHEET OF

FORM # SDO-401

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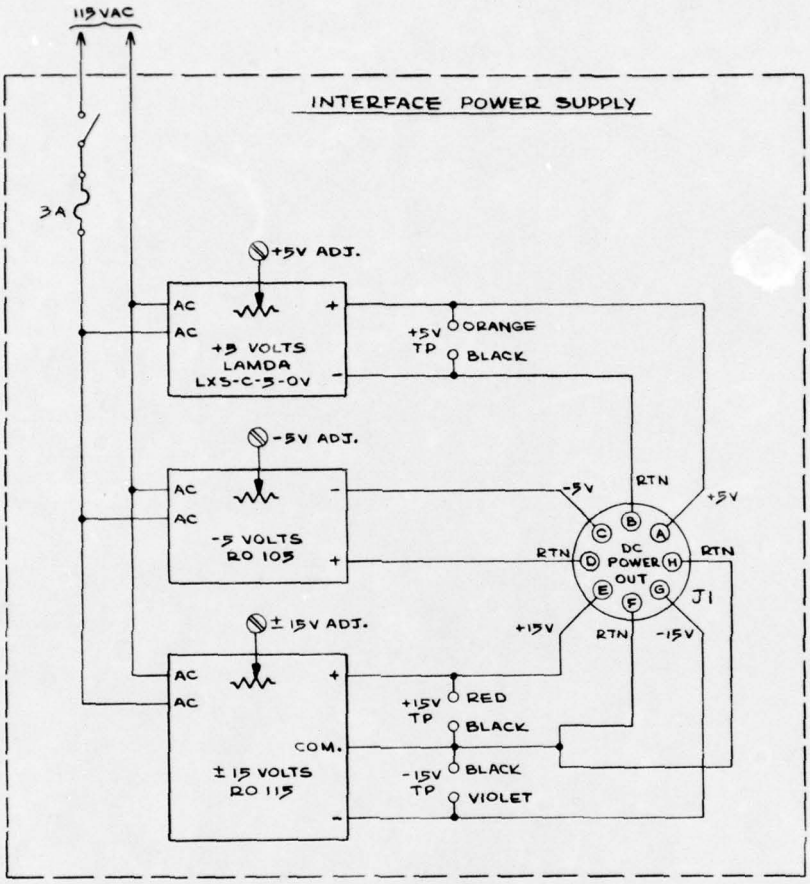
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TRIBUTED,
CERAMIC
D EACH)

TRIBUTED,
Mf -30V
S EACH)



BASIC QTY -XXXX	ITEM NO.	DWG SIZE	PART OR IDENTIFYING NUMBER	CIRCUIT SYMBOL OR JOINT	NOMENCLATURE OR DESCRIPTION	STOCK SIZE	MATERIAL AND/OR MATERIAL SPECIFICATION	MFG CODE	ISSUE REV.

LIST OF MATERIAL

PART NUMBER	SIZE	NEXT ASSEMBLY	QTY	USED ON	EFFECTIVITY END ITEM SER NO	WEIGHT

SURFACE TREATMENT BEFORE ASSY. — SURFACE ROUGHNESS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS
XX ± .03
XXX ± .010
ANGULAR ± 1/2°
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This report describes the design, assembly, and electrical matching of two identical measurement systems that were used in an experiment conducted by APL for the U.S. Air Force and the Defense Advanced Research Projects Agency to determine the validity of one facet of the theory of groundwave propagation at 100 kHz. It is Volume C of four volumes. Volume A is the summary report, Volume B covers test operations, and Volume D documents the data and analysis.

The goal of the experiment was to determine if an analytic function could be developed for operational use that relates secondary phase factor (SPF) to envelope to cycle difference (ECD) so that geodetic position can be computed accurately and in real time. Field test data were collected and analyzed and show trends that tend to support the hypothesis that the desired functional relationship exists, at least under certain conditions. Additional analysis and perhaps tests will be necessary to define these conditions or to prove conclusively the existence of such a relationship.

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