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BARRIER DIODE MICROCIRCUITS

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RADC-TR-76-292
Final Technical Report
September 1976

RELIABILITY EVALUATION OF SCHOTTKY BARRIER DIODE MICROCIRCUITS

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RELIABILITY EVALUATION OF SCHOTTKY
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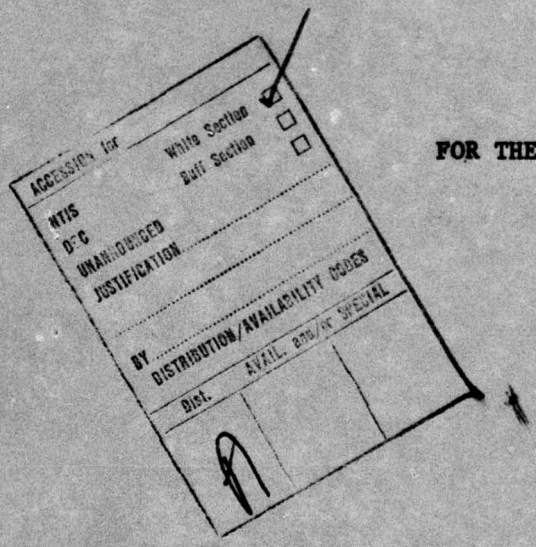
This report has been reviewed and approved for publication.

APPROVED: John R. Haberer

JOHN R. HABERER
Project Engineer

APPROVED: Joseph J. Naresky

JOSEPH J. NARESKY
Chief, Reliability & Compatibility Division



FOR THE COMMANDER: John P. Huss

JOHN P. HUSS
Acting Chief, Plans Office

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The objective of this study has been the analysis and reliability evaluation of modern Schottky Barrier Diode clamped microcircuits for use in high speed digital applications. The selected devices included SSI and MSI integration, single layer metallization, in both the regular and low power versions from two major vendors. All devices in the study utilized a trimetal system consisting of pure aluminum as the main conductor, titanium-tungsten as a barrier metal, and platinum-silicide for the Schottky and ohmic contacts. → next page

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All devices were subjected to long term high temperature storage and high temperature static operation to establish activation energies and to calculate failure rates at maximum operating temperature ranges. The low power Schottky 54LS00 from both Vendors A and B were additionally subjected to dynamic long term accelerated testing for comparison purposes.

Detail construction analysis and electrical characterization, including thermal resistances, were performed on all device types.

Units which failed during the performance of life testing were electrically categorized and physically analyzed to establish failure modes and mechanisms.

EVALUATION

The objective of this study was to provide reliability evaluation testing on representative digital microcircuits of the Schottky diode clamped generic type for the purpose of assuring adequate test methods, reliability prediction and specification for high reliability Air Force electronics. Data obtained from this effort includes device processing information, materials, design characteristics, electrical measurement characterization, test methods, burn-in procedures, specifications and reliability data. The results of this program will be used to assure the reliability of Schottky microcircuits by providing inputs to the various Government high reliability test and specification documents including Mil-Std-883 and MIL-M-38510.

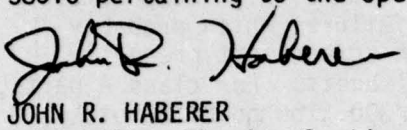
The results of this study point out the value of high temperature accelerated testing for detecting early life failures which probably would not have been detected using the burn-in screen test presently specified in the applicable Mil-M-38510 slash sheets. For class A parts, Mil-M-38510/70 (standard power Schottky) and /300 (low power Schottky) in their present form require a burn-in screen test per Mil-Std-883 test condition D or E at T_A = 125°C minimum for 240 hours. A worst case analysis of the atypical or early life failures indicates that a maximum junction temperature of about 225°C would be required to detect these failures within the presently specified 240 hour burn-in period. This observation supports other work in the area of accelerated testing and indicates that the proposed implementation of this procedure in Mil-M-38510 should be completed as soon as possible.

Failure rates related to the primary failure mechanisms observed in this study were extrapolated to an ambient temperature of 125°C for the devices operated with the loading specified in the life test circuits. For most testing, no failures were observed at the completion of the life tests extending to nearly 2500 hours at junction temperatures of up to 275°C. Worst case calculations show failure rates for these parts to be better than 0.0001%/1000 hours which indicates a mature reliable product. One exception noted exhibited extremely high failure rates on the order of 0.43%/1000 hours related to electromigration caused primarily by nominal current densities exceeding 2.5×10^5 A/cm^2 and poor glassivation.

No major problems were identified related to the technology used in the fabrication of these Schottky clamped microcircuits. Measurements indicated that the Schottky clamps were stable over the life test duration and no problems were observed with the trimetal system used on these devices. The life test comparison between static and dynamic life test configurations under identical environmental conditions did not result in any failures for either mode of operation, hence it was not possible to assess the relative effectiveness of the static versus dynamic stress testing.

In general, both the standard power and low power Schottky clamped microcircuits appear to be a mature technology capable of performing adequately in high reliability applications if caution is used in selecting devices to avoid the problems identified in this report. In particular, it appears that electromigration failures could be encountered and it is recommended that the current density not be allowed to exceed that specified in Mil-M-38510. Also, depending on the specific part, Schottky clamped microcircuits are susceptible to damage due to static discharge and proper handling procedures should be followed to prevent possible device degradation or failure.

All of the observations and conclusions resulting from this study will be used to provide guidance for future revision of any of the general test methods and procedures of Mil-Std-883 and the detail slash sheets of Mil-M-38510 pertaining to the specification of Schottky clamped microcircuits.



JOHN R. HABERER
Reliability Physics Section
Reliability Branch

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I. INTRODUCTION

The overall program contained approximately 715 devices with date codes ranging from 7330 to 7452.

In order to accomplish a comparative analysis it was planned to secure devices from three vendors. At the time of the procurement of parts for the study, only two sources were able to supply the parts requested (54S00, 54S138, 54LS138). The third manufacturer was unable to deliver Schottky devices, because their Schottky product was in redesign.

The loss of the third vendor (Vendor C) necessitated two major changes in the scope of the study. 1. Vendor C part types were eliminated and replaced by low power Schottky devices from Vendors A and B. 2. For these low power Schottky devices, the limit and long term life test was expanded to include high temperature dynamic operation.

These changes were beneficial in that it was now possible to accomplish a comparison between the standard and low power Schottky versions in both low and medium complex circuit configurations. Initially, all devices were hermetically and parametrically tested. The electrical parameters were obtained using a Fairchild 5000D tester. All units were received with tin plated leads. The tin was removed and leads were gold plated to prevent oxidation at higher temperatures.

Following the plating operation, devices again were checked for hermeticity and electrical D.C. parameters data logged per MIL-M-38510/70 for the 54S00 and Vendor A's specification for all other types. This was necessary because the 54S138 and 54LS138 were not included in the MIL-M-38510 slash sheets. The parts were grouped as shown in the test plan of Table 1.

The junction temperatures experienced in the oven ambients referred to in Table 1 are summarized in Table 2. These junction temperatures were computed from thermal resistance measurement Θ_{JAF} in the actual oven environment and the average power dissipation at that ambient temperature.

Based on the parametric tests, three devices each were selected for V_{OH} (low, medium and high) based on data logged values at a load current of 1mA for the standard and 400μA for the low power Schottky. These devices were used throughout the electrical evaluation.

Input/output transfer characteristics were obtained on samples for all device types with V_{CC} = 5.0V; 4.5V and 5.5V and at ambient temperatures of -55°C, 25°C and 125°C. The outputs were loaded with a diode-resistor network (shown in Appendix A).

Propagation delay measurements were performed at nominal supply voltage of V_{CC} = 5.0V and two output load conditions for the S138 and LS138 at ambient temperatures of -55°C, +25°C, and +125°C. In addition to the specified propagation delay measurements in the MIL-M-38510/70 and /300 transient time measurements were taken under above stated conditions.

The life test portion of the program consisted of limit and long term testing. Devices from each type and vendor were subjected to high temperature storage, and high temperature/ static bias conditions. The 54LS00 from Vendors A and B were also subjected to high temperature dynamic operation for both limit and long term life testing.

During the performance of the long term operating life test, all Vendor A's devices, as well as Vendor B's 9LS00, were subjected to three different ambient temperature environments. The 9S00 and 93S138 of Vendor B were subjected to two temperature environments. Equivalent stress conditions for voltage, temperature and loads were used for similar devices from both vendors in order to obtain a more direct reliability performance comparison.

Where sufficient data points were available, mean time to failure (MTF), standard deviation σ, and activation energies, E_a, were calculated. Assumptions for σ and E_a were made in cases of insufficient data.

Failure rates for all devices were calculated at the anticipated maximum operating temperatures.

A detail construction analysis was performed on all device types including mapping of the topology and verification of electrical schematics.

Failure analysis consisted of grouping of failure modes and the detailed determination of failure mechanisms on a sample for each group. During failure analysis, extensive use was made of the scanning electron microscope and micro sectioning, where necessary.

TABLE 1: Schottky Test Plan

Standard Schottky TTL

Vendor	Device	Long Term Testing: Storage 250°C	Storage 300°C	HTRB* T_{A1}	HTRB* T_{A2}	HTRB* T_{A3}	HTRB* T_{A4}	Limit Testing: Storage	Limit Testing: HTRB	Therm. Resis.	E.E. & C.A. ***	Total
A	54S00	15	15		15	15	15	5	5	5	5	95
B	9S00	15			15	15		5	5	5	5	65
A	54S138	15	15	15		15	15	5	5	5	5	95
B	93S138	15		15		15		5	5	5	5	65
											TOTAL	320

Low Power Schottky

Vendor	Device	Long Term Testing: Storage 250°C	Storage 300°C	HTRB T_{A2}	HTRB T_{A3}	HTRB T_{A4}	Dyn.** T_{A2}	Dyn.** T_{A3}	Dyn.** T_{A4}	Limit Testing: Stor.	HTRB	Dyn.	Therm. Resis.	E.E.& C.A ***	Total
A	54LS00	10	10	15	15	15	15	15	15	10	10	10	5	5	150
B	9LS00	10	10	15	15	15	15	15	15	10	10	10	5	5	150
A	54LS138	15	15	15	15	15				5	5	5	5	5	95
														TOTAL	395

*For calculated T_J see Table 2.
**MIL-STD-883, Method 1015, Condition D
***Electrical Evaluation and Construction Analysis

TABLE 2: Calculated Junction Temperature

Vendor	Device Type	Ambient Temperature				
		T_{A1}=195°C	T_{A2}=220°C	T_{A3}=250°C	T_{A4}=275°C	
A	54S138	209		265	290	T_J(°C)
B	93S138	209		265		T_J(°C)
A	54S00		227	257	282	T_J(°C)
B	9S00		228	258		T_J(°C)
A	54LS00		221	251	276	T_J(°C)
B	9LS00		221	251	276	T_J(°C)
A	54LS138		222	252	277	T_J(°C)

II. GENERAL INFORMATION

A. Delivery Times

The initial proposal included devices from three vendors that were purported to be off-shelf items with short deliveries. This was not the case for one of the vendors (Vendor C). His Schottky product was in redesign. Therefore, the plan had to be altered. With RADC's approval, the scope of the study was changed and Vendor C's devices were substituted by Vendor A and B's low power Schottkies. Table 3 shows delivery times for all parts included in the study. As can be seen delivery times for many of the parts were very long.

TABLE 3: Delivery Times

Vendor	Type	Ordered	Delivery Times In Weeks
A	54S00	5/74	11
B	9S00	5/74	10
A	54S138	5/74	10
B	93S138	5/74	26
A	54LS00	11/74*	17
B	9LS00	11/74*	9
A	54LS138	7/74	5

*Late order due to test plan change.

B. Hermetic Testing

All devices used in life tests were hermetically tested. For fine leak test, a Norton Mass Spectrometer Leak Detector and a limit of $<5 \times 10^{-7}$ cc/sec was used as an acceptance criteria.

For gross leak testing, the weight method was used with a rejection criteria of a weight gain greater than $.5 \times 10^{-3}$ grams.

C. Gold Plating

It was anticipated that by using tin plated external leads at proposed high operating and storage temperatures over +200°C, the tin would melt/oxidize resulting in increased contact resistance during electrical and operating life testing. In order to prevent these problems all device leads were tin stripped and nickel plated followed by gold plating. A detail procedure is outlined in Appendix I.

III. ELECTRICAL

A. Parametric Testing

A Fairchild 5000D tester was used for all DC testing during the study. Data logging was accomplished in the form of hard copy print-outs.

The tests performed included:

High level supply current	I_{CCH}
Low level supply current	I_{CCL}
High level output voltage	V_{OH}
Low level output voltage	V_{OL}
Input clamp voltage	V_{IC}
Collector cut-off current	I_{CEX}
High level input current	$I_{IH1,2}$
Low level input current	I_{IL}
Short circuit output current	I_{OS}

Limits and conditions used for electrical testing of the 54S00 were according to MIL-M-38510/70. For the low power Schottky devices Vendor A's specifications were used since the /300 military specification was not released until 9/19/75. Both S138 and LS138 also were tested to Vendor A's specification.

Subsequent comparison of the recently issued 38510/300 and the testing performed revealed that the I_{CEX} test was eliminated in the military specification. In parametric testing of Vendor A's final shipment of 54LS00 all units failed the short circuit current test with the specified maximum limit of 40mA.

A design change of significant magnitude became evident during construction analysis of both the old and new versions of the Vendor A's 54LS00. In the newly redesigned part the limiting resistor in the collector of the upper transistor of the totem pole output stages had been changed from 200Ω to 50Ω. As a result of this change the short circuit output current I_{OS} was drastically increased requiring a specification change in its maximum limit from I_{OS} = 40mA max to I_{OS} = 130mA max.

The change was made to improve the line driving capability of these low power Schottky devices. A comparison of transition and propagation delay times is indicated in Table 6.

B. Schottky Diode TTL Circuits

A significant feature of the Schottky clamped circuit over the standard TTL is the use of a base-collector diode clamp: the Baker clamp (Figure 1).

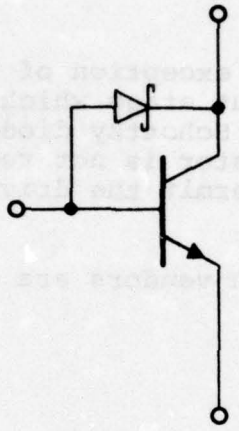


FIGURE 1: Baker clamp

The clamp between base and collector of the transistor consists of a Schottky barrier diode which prevents the transistor from saturating. Since the transistor is held out of saturation no excess base charge is stored and, therefore, the storage time is eliminated.

The main feature of the clamping diode is a forward voltage characteristic lower than the base to collector junction forward voltage drop, keeping the transistor out of saturation by bypassing excess base current. The Schottky barrier diode, a metal to semiconductor junction, has a negligible stored charge. The switching time of these diodes is very much faster than those of equivalent PN junctions. By incorporating the Schottky clamp, the need for gold doping used in regular TTL is no longer required.

C. Practical Standard Schottky TTL Circuits

The standard Schottky circuits utilize multiple emitter inputs with individual Schottky clamping diodes to the substrate (ground).

The input clamping is implemented with these Schottky barrier diodes to protect against negative-going excursions on the inputs. Because of the fast recovery time and its lower forward voltage drop, the Schottky input diode provides a significant improvement in clamping action over a conventional PN junction diode.

All transistors, with the exception of the upper transistor in the totem pole of the output stage which is in the Darlington configuration, have Schottky diode clamps. A Schottky clamp for this transistor is not required since the driving transistor does not permit the driven transistor to go into saturation.

Practical circuits of both vendors are shown in Figures 2 and 3.

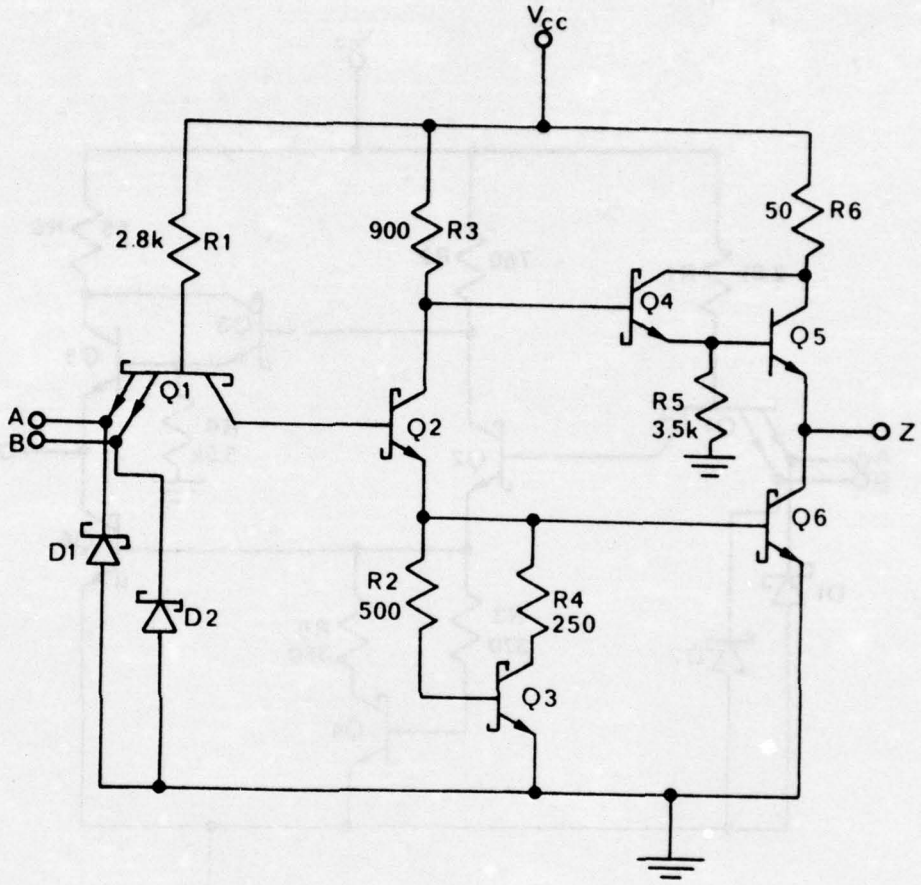


FIGURE 2: Typical gate design of Vendor A's 54S00.

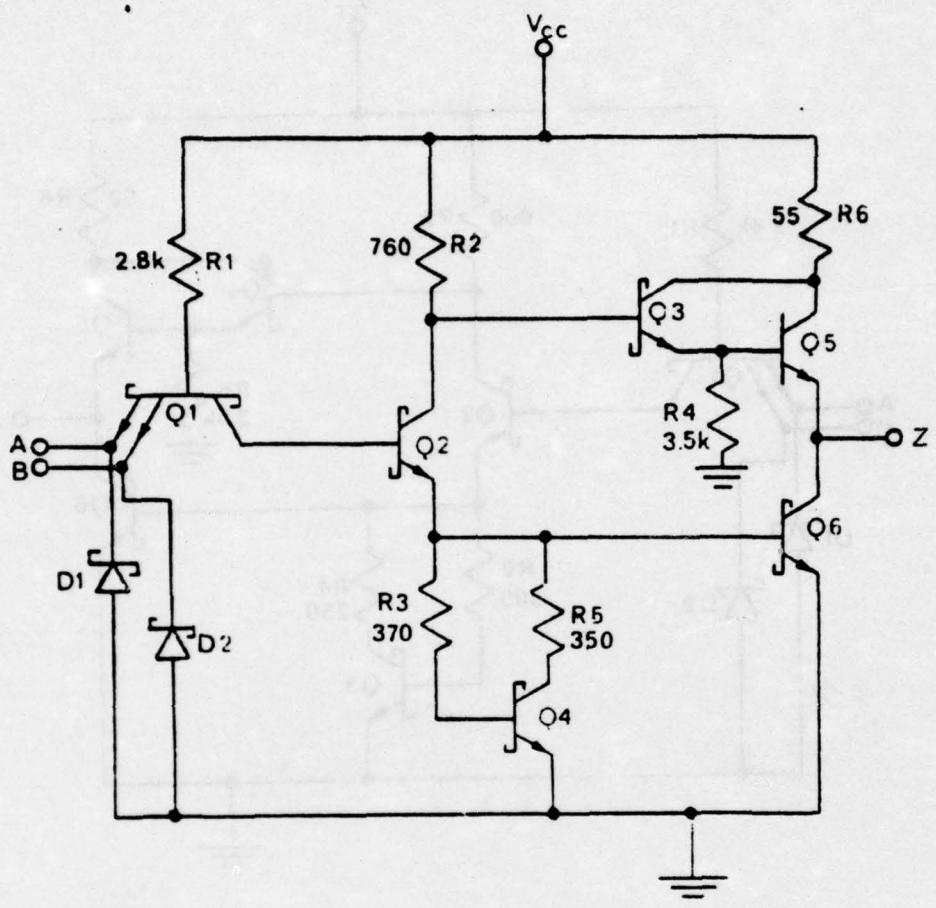


FIGURE 3: Typical gate design of Vendor B's 9S00.

D. Low Power Schottky Circuits

Low power Schottky circuits differ from the standard version significantly in design and performance. The multi-emitter input structure of the standard power devices is replaced by a DTL-type input circuit, as shown in Figures 4 and 5.

As a result, the input breakdown voltage is increased to better than 15V which makes direct interfacing from CMOS to the low power Schottky possible.

The base resistor of the pull-up transistor (R_4 of Figure 4, R_3 of Figure 5) is returned to the output terminal for power conservation. Also, a speed-up diode supplying additional current to the phase splitter transistor during high to low output voltage transitions is used (D_5 in Figures 4 and 5). In addition, this diode limits the maximum output voltage to one diode drop above V_{CC}.

The main feature of the low power TTL Schottky device is that the circuit resistor values are larger than the standard Schottky devices by a factor of 10. Hence, reduced power consumption is realized.

The lower internal power dissipation causes a lower rise in chip temperature above ambient, which simplifies thermal design. Also, a lower operating junction temperature increases the mean time to failure. The overall reduction in internal currents lowers the chances of failure resulting from electro-migration.

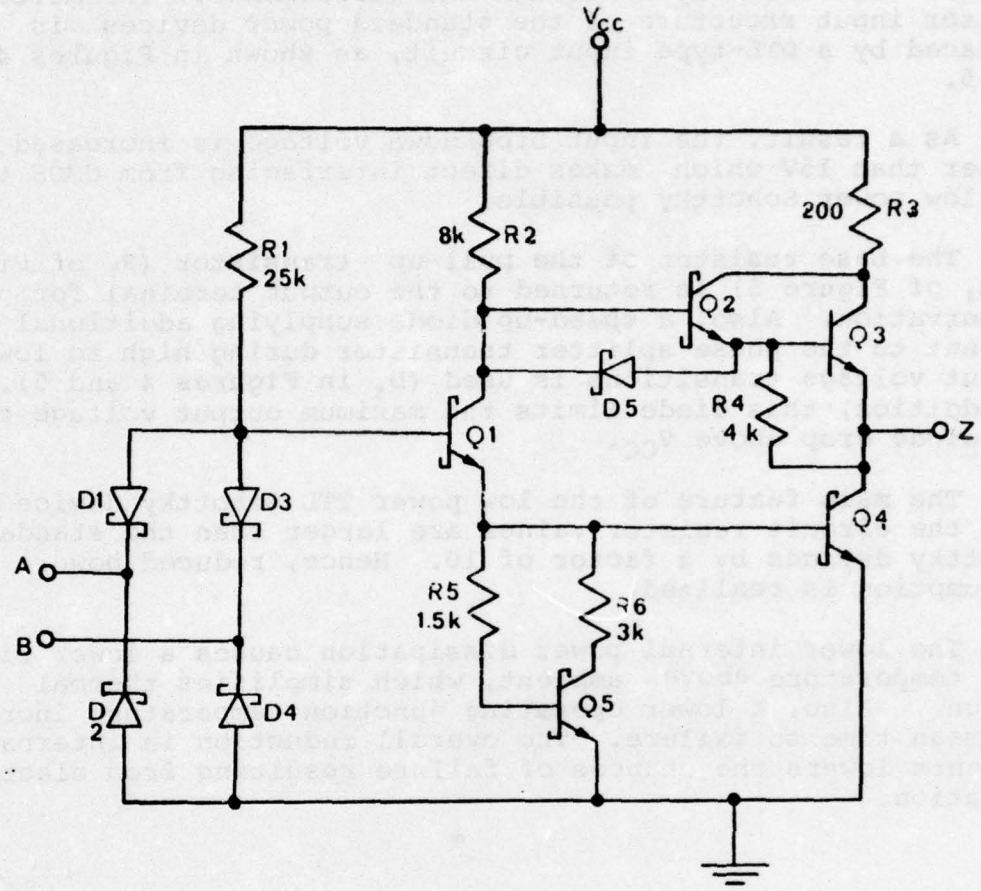


FIGURE 4: Typical low power Schottky gate design for Vendor A's 54LS00.

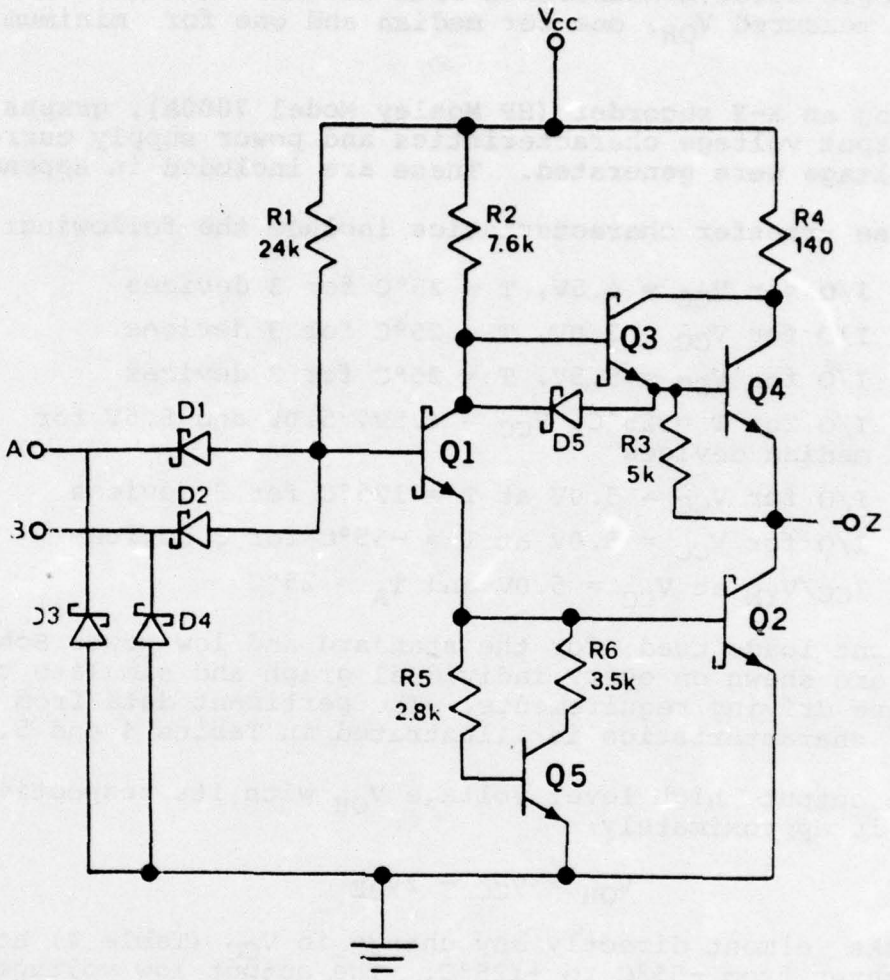


FIGURE 5: Typical low power Schottky gate design for Vendor B's 9LS00.

E. Input/Output Transfer Characteristics

Three devices were selected from each vendor type based on V_{OH} logic level measurements from initial data (one for maximum measured V_{OH}, one for median and one for minimum V_{OH}).

Using an X-Y recorder (HP Mosley Model 7000A), graphs of input/output voltage characteristics and power supply current/input voltage were generated. These are included in Appendix A.

These transfer characteristics include the following:

a. I/O for V_{CC} = 4.5V, T = 25°C for 3 devices

b. I/O for V_{CC} = 5.0V, T = 25°C for 3 devices

c. I/O for V_{CC} = 5.5V, T = 25°C for 3 devices

d. I/O for T = 25°C, V_{CC} = 4.5V, 5.0V and 5.5V for median devices

e. I/O for V_{CC} = 5.0V at T = 125°C for 3 devices

f. I/O for V_{CC} = 5.0V at T = -55°C for 3 devices

g. I_{CC}/V_{IN} at V_{CC} = 5.0V and T_A = 25°C

Output loads used for the standard and low power Schottky devices are shown on every individual graph and simulate their respective driving requirements. The pertinent data from the transfer characteristics is illustrated in Tables 4 and 5.

The output high level voltage V_{OH} with its respective load current is approximately:

$$V_{OH} \simeq V_{CC} - 2V_{BE}$$

and tracks almost directly any change in V_{CC} (Table 4) at temperatures from -55°C to +125°C. The output low voltages V_{OL} under maximum load conditions are within specified limits and vary less than 35mV per volt change of V_{CC} over temperatures ranging from -55°C to +125°C.

Table 5 shows V_{OH} and V_{OL} changes as a function of temperature. For typical devices operating under specified load conditions and a power supply voltage of +5.0V output high voltage (V_{OH}) changes of 3.6 to 3.8mV/°C for the low power Schottky and 3.2 to 3.7mV/°C for standard Schottky devices

TABLE 4: V_{OH} and V_{OL} Versus Supply Voltage V_{CC}

Vendor	Type	V_{OH}/V_{CC} (mV) at 25°C	V_{OH}/V_{CC} (mV) at 125°C	V_{OH}/V_{CC} (mV) at -55°C	V_{OL}/V_{CC} (mV) at 25°C	V_{OL}/V_{CC} (mV) at 125°C	V_{OL}/V_{CC} (mV) at -55°C
A	54LS138	1000	1000	1000	35	30	35
A	54S138	1000	1000	1000	35	30	35
B	9S00	1000	1000	1000	35	30	35
B	93S138	1000	1000	1000	35	30	35
B	9LS00	1000	1000	1000	35	30	35
A	54LS00	1000	1000	1000	35	30	35
A	54S00	1000	1000	1000	35	30	35

TABLE 5: V_{OH} and V_{OL} Versus Ambient Temperature

Vendor	Type	V_{CC} = 5.0V V_{OH} vs. Temperature	V_{CC} = 5.0V V_{OL} vs. Temperature
A	54LS138	+3.8mV/°C	-.39mV/°C
A	54S138	+3.3mV/°C	-.42mV/°C
B	9S00	+3.2mV/°C	-.33mV/°C
B	93S138	+3.7mV/°C	-.30mV/°C
B	9LS00	+3.7mV/°C	-.45mV/°C
A	54LS00-New	+3.6mV/°C	-.39mV/°C
A	54LS00-Old	+3.7mV/°C	-.30mV/°C
A	54S00	+3.2mV/°C	-.36mV/°C

were recorded. The magnitude of ΔV_{OL} per °C is ten times smaller than the V_{OH} change and ranges from .30 to .45mV/°C. It should be noted that the changes in V_{OH} and V_{OL} with temperature oppose each other resulting in a larger output voltage swing at elevated temperatures under the same load conditions.

Graphs showing supply current versus input voltage of all devices are included in Appendix A. The curves were taken with only one output loaded as shown in the graph which also is the only output being exercised. One input was switched while all others were floating. The I_{CC} current measured is the sum total of three gates where unloaded output stages were always in a low state and one, the fourth, being exercised. The current spike shown in these graphs is totally due to the current contribution of one gate only and is a result of the output transistor overlap during transition periods. By viewing the individual graphs, it can be seen that the current spike is dependent on the direction of the input voltage in its amplitude and respective position. This seems to be true for all devices in varying degrees.

F. Switching Time Measurements

Switching time measurements consisting of transition and propagation delay time were performed on three devices per part type (one low V_{OH}, one high and median).

The standard output load as per MIL-M-38510/70 and /300 shown in Figure 6 was used for all device types.

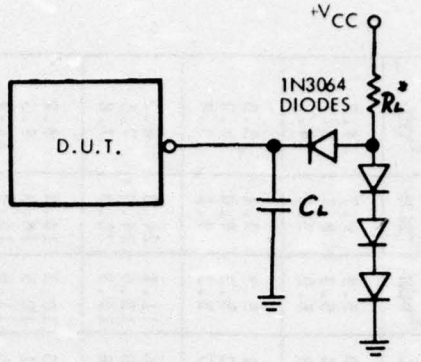


FIGURE 6: Output Load for Switching Time Measurements

C_L = 50pF

*R_L = 280Ω for standard Schottky device

*R_L = 2KΩ for low power Schottky device

Both standard and low power 138 type devices not yet included in military slash sheets were tested with the load in Figure 6 and C_L = 15pF as per Vendor A's specification.

A comparison chart for the S00 and LS00 for both Vendor A and B is shown in Table 6. The results indicate no noticeable difference in switching time between the two vendors over the entire temperature range for the standard Schottky parts.

Vendor A's 54LS00 were categorized into two groups: old and new design. The new design, having a smaller chip area and the most significant change, is a decrease from 200Ω to approximately 50Ω in value of the resistor in the collector of the Darlington pair resulting in a vastly improved transition time t_{TLH} from about 26n sec. in the old version, to about 12n sec. in the new design. An improvement of 4ns also was achieved as a result of the redesign in propagation delay, both for t_{PLH} and t_{PHL}.

In comparing the new design LS00 of Vendor A to Vendor B, propagation delays are within 2.5 nsec of each other over the entire temperature range.

TABLE 6: SCHOTTKY SWITCHING SPEED

VENDOR	DEVICE TYPE		SER. NO.	SWITCHING SPEED IN NANOSECONDS											
				-55°C				+25°C				+125°C			
				t_{PHL}	t_{PLH}	t_{TLH}	t_{THL}	t_{PHL}	t_{PLH}	t_{TLH}	t_{THL}	t_{PHL}	t_{PLH}	t_{TLH}	t_{THL}
B	9S00	MAX	13	6.0	5.0	7.0	4.1	5.5	5.1	7.3	3.6	6.0	5.9	9.7	4.3
			12	7.0	4.9	7.0	4.6	6.0	5.1	7.2	4.2	5.4	5.3	8.7	3.7
		MIN	14	6.8	5.0	7.1	5.4	6.0	5.0	7.2	4.3	5.8	5.9	9.8	4.3
A	54S00	MAX	16	5.9	5.1	7.3	3.9	5.4	5.0	7.6	3.1	5.1	5.3	9.4	3.0
			10	6.0	5.0	7.2	4.1	5.5	4.9	7.2	3.5	5.3	5.3	8.0	3.2
		MIN	1	7.2	5.6	7.3	4.1	5.8	5.2	7.3	4.1	5.7	5.3	8.1	3.8
B	9LS00	MAX	72	10.0	9.8	18.3	7.0	8.1	9.8	19.5	6.3	7.6	11.4	24.0	6.2
			64	11.2	10.3	16.2	8.3	9.5	10.2	18.7	7.3	8.8	12.0	24.0	7.5
		MIN	114	11.9	10.6	15.5	9.8	9.9	10.3	17.6	8.0	8.8	12.3	25.0	7.8
A	New Design 54LS00	MAX	50	12.5	9.9	10.0	10.8	10.6	9.7	11.5	8.5	10.3	10.3	14.8	8.2
			11	12.7	9.5	10.1	11.2	11.2	9.9	11.1	9.4	11.1	10.5	15.3	9.3
		MIN	31	14.6	12.1	13.5	14.6	11.6	10.7	13.1	11.5	11.6	11.8	16.3	11.3
A	Old Design 54LS00	MAX	116	16.8	14.0	26.2	11.9	14.2	12.6	26.8	10.6	13.9	13.8	30.0	11.2
			114	18.8	13.2	24.8	14.0	16.7	12.6	26.4	12.5	16.4	16.1	28.0	13.7
		MIN	117	18.8	13.7	23.8	16.0	16.6	13.0	25.7	13.9	16.6	14.3	29.0	15.7

In summary all standard S00 tested are well within specified limits of both vendor specification and the applicable slash sheet of MIL-M-38510. All propagation delays for the low power LS00 devices tested ranged up to 60% of the maximum values specified.

Data comparing the S138 from both vendors and Vendor A's 54LS138 over temperature and two load conditions is included in Tables 7, 8, and 9. No noticeable differences in propagation delay were seen between Vendor A's and Vendor B's S138 devices. Both vendor types were within the limits of Vendor A's specification.

TABLE 7: *Schottky Switching Time in Nanoseconds*

Delay Level	Parameter	Type Input Pin No.	Type Output Pin No.	Vendor A 54LS138 Ser. No. 47 Max.	Ser. No. 31 Med.	Ser. No. 38 Min.	Temp. °C	Load Cap.
2	t_{PLH}	4	10	13.6	14.8	15.5		
	t_{PHL}			22.3	23.9	24.0		
3	t_{PLH}	6	10	18.7	20.2	20.2		
	t_{PHL}			25.8	27.7	29.3		
2	t_{PLH}	1	11	13.4	14.8	15.3		
	t_{PHL}			17.4	18.9	19.3		
3	t_{PLH}	1	10	18.1	19.6	19.7		
	t_{PHL}			24.2	26.2	27.4	+25	15pf
2	t_{TLH}	4	10	16.9	16.0	14.8		
	t_{THL}			7.1	8.0	9.7		
3	t_{TLH}	6	10	16.2	15.5	14.6		
	t_{THL}			7.0	8.0	9.7		
2	t_{TLH}	1	11	16.2	16.0	15.9		
	t_{THL}			7.2	8.0	8.8		
3	t_{TLH}	1	10	16.1	15.1	14.0		
	t_{THL}			6.6	7.7	9.6		

TABLE 7: Schottky Switching Time in Nanoseconds

(Continued)

Delay Level	Parameter	Type Input Pin No.	Type Output Pin No.	Vendor A 54LS138 Ser. No. 47 Max.	Ser. No. 31 Med.	Ser. No. 38 Min.	Temp. °C	Load Cap.
2	t_{PLH}	4	10	18.5	19.6	20.0		
	t_{PHL}			27.0	29.4	31.0		
3	t_{PLH}	6	10	23.1	24.6	24.6		
	t_{PHL}			30.6	33.4	36.4		
2	t_{PLH}	1	11	18.2	19.4	19.6		
	t_{PHL}			22.6	24.6	25.4		
3	t_{PLH}	1	10	22.8	24.4	24.2		
	t_{PHL}			29.0	31.8	34.8	+25	50pf
2	t_{TLH}	4	10	27.6	26.7	25.6		
	t_{THL}			12.2	14.5	18.8		
3	t_{TLH}	6	10	27.2	26.6	25.4	+25	50pf
	t_{THL}			12.1	14.5	19.1		
2	t_{TLH}	1	11	29.8	28.1	27.0		
	t_{THL}			12.8	15.1	16.5		
3	t_{TLH}	1	10	27.6	26.8	25.7		
	t_{THL}			12.0	14.7	19.1		

TABLE 8: SCHOTTKY SWITCHING TIME IN NANOSECONDS

DELAY LEVEL	PARA-METER	TYPE INPUT PIN NO	TYPE OUTPUT PIN NO	VEN. A 5451138J SER. NO. 27 MAX	28 MED	33 MIN	VEN. B 9351138 SER. NO. 19 MAX	40 MED	47 MIN	TEMP °C	LOAD CAP.
2	t_{PLH}	4	10	6.4	6.5	6.8	6.6	7.2	7.1		
	t_{PHL}			8.3	7.9	8.5	7.2	7.7	7.6		
3	t_{PLH}	6	10	7.9	8.0	8.4	8.0	8.5	8.3		
	t_{PHL}			9.5	8.8	9.7	8.4	9.0	8.8		
2	t_{PLH}	1	11	6.2	6.2	6.7	6.1	6.4	6.3		
	t_{PHL}			6.6	7.0	7.6	8.9	9.3	9.2		
3	t_{PLH}	1	10	8.6	8.3	8.8	7.1	7.3	7.2		
	t_{PHL}			9.6	9.5	10.5	8.2	8.6	8.5	+25	15pf
2	t_{TLH}	4	10	6.2	6.2	6.3	5.8	5.7	5.7		
	t_{THL}			2.5	2.7	3.0	2.2	2.3	2.5		
3	t_{TLH}	6	10	7.6	7.7	8.0	5.9	5.9	5.8		
	t_{THL}			2.5	2.8	3.0	2.2	2.4	2.4		
2	t_{TLH}	1	11	6.3	7.5	7.9	5.9	5.6	5.6		
	t_{THL}			2.4	3.0	3.3	2.8	2.6	2.6		
3	t_{TLH}	1	10	6.5	6.4	6.7	5.8	5.7	5.7		
	t_{THL}			2.4	2.8	2.7	2.2	2.3	2.4		
2	t_{PLH}	4	10	8.0	8.0	8.4	8.0	8.5	8.3		
	t_{PHL}			10.3	10.0	10.7	8.9	9.5	9.5		
3	t_{PLH}	6	10	9.5	9.5	10.0	9.3	9.9	9.5		
	t_{PHL}			11.0	10.8	11.8	9.9	10.7	10.6		
2	t_{PLH}	1	11	7.8	7.8	8.3	7.5	8.0	7.9		
	t_{PHL}			8.3	9.0	9.9	10.6	11.2	11.3		
3	t_{PLH}	1	10	10.3	9.8	10.4	8.4	8.7	8.6		
	t_{PHL}			11.5	11.6	12.5	9.7	10.3	10.4	+25	50pf
2	t_{TLH}	4	10	8.9	9.0	9.4	8.7	8.6	8.5		
	t_{THL}			4.8	5.6	5.6	4.6	5.0	5.2		
3	t_{TLH}	6	10	10.0	10.5	11.5	8.9	8.8	8.7		
	t_{THL}			4.5	5.3	5.4	4.4	4.8	5.1		
2	t_{TLH}	1	11	9.0	10.0	11.3	8.7	8.6	8.6		
	t_{THL}			4.7	5.6	6.0	4.4	4.6	4.8		
3	t_{TLH}	1	10	9.4	9.3	9.6	9.2	9.0	9.0		
	t_{THL}			4.3	5.0	5.2	4.3	4.9	5.1		

TABLE 9: SCHOTTKY SWITCHING TIME IN NANOSECONDS

All Measurements: Delay Level 3: Input Pin 6 to Output Pin 10

Switching CRKT Per A Spec. (No MIL yet).
[XCEPT LS138 Sense Levels were +1.5V to 1.5V
(or +1.3V to +1.3V as indicated)]

DEVICE TYPE	SER. NO.	$C_T = C_L = 15pf$ T_{PLH}	T_{PHL}	T_{TLH}	T_{THL}	$C_T = C_L = 50pf$ T_{PLH}	T_{PHL}	T_{TLH}	T_{THL}	R_L & TEMP.
A 54S138	27	7.4	9.2	6.2	2.8	8.8	11.0	8.9	4.4	
	28	7.7	9.2	6.5	3.2	8.9	11.3	9.0	5.2	
	33	7.9	10.0	7.1	3.0	9.4	12.0	9.5	5.2	280Ω
B 93S138	19	8.0	8.8	5.7	2.4	9.1	10.2	8.6	4.8	-55°C
	40	8.5	9.8	6.3	2.6	9.8	11.6	8.6	4.3	
	47	8.3	9.4	5.6	2.7	9.6	11.2	8.6	4.7	
A 54S138	27	7.9	9.9	7.6	2.3	9.6	11.6	10.0	4.5	
	28	7.9	9.2	7.7	2.6	9.1	11.1	10.5	5.3	
	33	8.3	10.2	8.0	2.7	9.6	12.2	11.5	5.4	280Ω
B 93S138	19	7.9	8.7	5.9	2.2	8.9	10.2	8.9	4.4	+25°C
	40	8.4	9.5	5.9	2.4	9.6	11.2	8.8	4.8	
	47	8.2	9.3	5.8	2.4	9.2	10.9	8.7	5.1	
A 54S138	27	10.6	13.4	8.3	2.6	12.2	15.3	11.7	4.5	
	28	10.1	12.2	7.8	2.8	11.5	14.1	11.6	5.0	
	33	10.6	12.9	8.7	2.8	12.1	14.8	12.0	5.0	280Ω
B 93S138	19	8.4	9.7	6.6	2.5	10.0	11.4	9.6	4.0	+125°C
	40	9.0	10.3	6.9	2.4	10.5	12.1	9.2	4.6	
	47	8.7	9.8	6.2	2.6	10.1	11.8	9.0	4.5	
A 54LS138 NOTE: T_{PLH} & T_{PHL} from +1.5V to 1.5V.	47	18.3	25.9	14.4	6.3	23.1	29.7	24.9	11.6	2KΩ
	49	20.7	29.1	15.5	7.3	25.2	33.6	24.3	14.0	-55°C
	32	20.0	30.3	14.9	7.8	25.2	35.8	25.1	15.3	
	47	19.4	24.9	16.6	6.2	24.7	29.2	28.2	10.8	
	49	21.1	27.7	16.4	7.1	25.9	32.2	26.8	12.8	2KΩ
	32	20.0	27.0	15.6	7.4	25.2	31.8	28.4	13.8	+25°C
	47	24.5	26.4	22.4	6.9	29.0	30.5	33.6	12.1	
	49	25.0	28.9	21.0	7.8	30.3	34.0	33.5	13.9	2KΩ
	32	21.9	27.2	19.7	8.3	27.2	32.5	33.8	15.1	+125°C
A 54LS138 T_{PLH} & T_{PHL} from +1.3V to +1.3V	47	17.2	27.6	14.4	6.3	20.7	33.3	24.9	11.6	
	31	19.1	30.3	15.5	7.3	22.7	36.6	24.3	14.0	2KΩ
	38	18.4	31.3	14.9	7.8	21.9	37.6	25.1	15.3	-55°C
	47	18.5	26.8	16.6	6.2	23.1	31.2	28.2	10.8	
	31	20.2	29.6	16.4	7.1	24.7	34.7	26.8	12.8	2KΩ
	38	19.0	29.1	15.6	7.4	23.7	34.7	28.4	13.8	+25°C
	47	22.8	27.9	22.4	6.9	28.1	33.9	33.6	12.1	
	31	23.1	30.7	21.0	7.8	27.1	36.7	33.5	13.9	2KΩ
	38	20.1	29.0	19.7	8.3	24.6	35.8	33.8	15.1	+125°C

G. Thermal Resistance Measurements

For purposes of calculations of junction temperatures while dissipating power during limit and operational life testing the thermal resistance of all device types was measured. All measurements were made using the substrate diode junction as a temperature reference. A constant current of 1mA was used for calibration and measurement.

The device dissipation was accomplished by the use of an emitter follower circuit driven by a Data pulse 110 generator (Figure 7). The repetition rate was such that the device under test was powered for greater than 99.5%. For a period of 30 μs power was removed during which a measurement was made. To prevent possible overloading of the type W plug-in and achieve better accuracy a special sampling network was employed.

Three measurements were made and the results shown in Tables 10 and 11.

Θ_{JC} - junction to case; utilizing FC77 fluorocarbon liquid as heat sink

Θ_{JA} - junction to stagnant air at 25°C using an enclosure having a cavity of 1.5' x 1.5' x 1'. Sockets used are Robinson-Nugent; high temperature 16 pin IC-163-S2-HT (device inserted not flush to socket).

Θ_{JAF} - junction to air at +25°C in the life test oven environment and actual life test fixture. For this specific measurement only a few selected devices of the standard Schottky types were included. Results range from 46°C/W to 67°C/W.

Thermal resistance measurements Θ_{JC} and Θ_{JA} (stagnant air) are for reference information only.

Results for thermal resistance Θ_{JAF} were used to calculate junction temperatures for both limit and long term life testing.

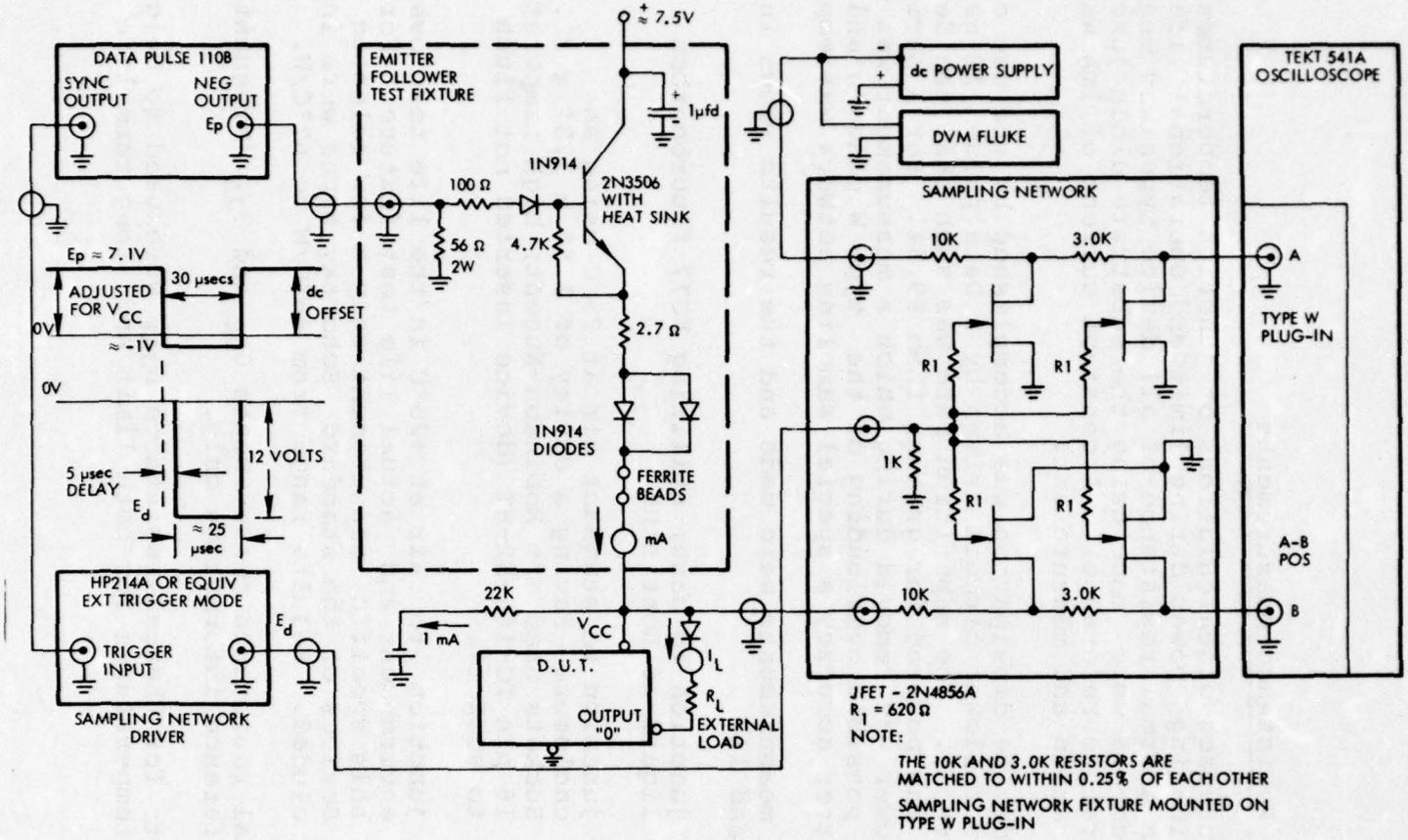


FIGURE 7: Thermal resistance test circuit.

As indicated in Table 10, average values for junction to case measurements of all types and vendors tested ranged from 18°C/W to 33°C/W and therefore are well within the specified limits of vendor and military specification. Table 11 shows maximum, average and minimum values of thermal resistance both junction to case θ_{JC} and junction to still air θ_{JA}. Deviations from the average values of θ_{JC} are within acceptable limits indicating a uniform die attach method.

TABLE 10: Comparison Chart of θ_{JC} and θ_{JA}

Vendor	Type	θ_{JA}[a]	θ_{JC}
A	54S00	102°C/W	33.4°C/W
B	9S00	100°C/W	31.6°C/W
A	54LS00 Old design	106°C/W	22°C/W
A	54LS00 New design	102°C/W	27°C/W
B	9LS00	102°C/W	25°C/W
A	54S138	92°C/W	30°C/W
B	93S138	101°C/W	31°C/W
A	54LS138	74°C/W	18°C/W

[a]Still air conditions.

TABLE 11

θ_{JC} [°C/W]

Vendor	Device Type	Maximum °C/W	Average °C/W	Minimum °C/W
A	54S00	37	33	28
B	9S00	37	31	28
A	54LS00 Old design	30	22	17
A	54LS00 New design	32	27	23
B	9LS00	27	25	22
A	54S138	31	30	28
B	93S138	43	31	24
A	54LS138	20	18	16

θ_{JA} [°C/W]

Vendor	Device Type	Maximum °C/W	Average °C/W	Minimum °C/W
A	54S00	106	102	98
B	9S00	105	100	95
A	54LS00 Old design	109	106	100
A	54LS00 New design	111	102	97
B	9LS00	106	102	99
A	54S138	96	92	90
B	93S138	111	101	91
A	54LS138	80	74	70

IV. CONSTRUCTION ANALYSIS

A complete construction analysis including an electrical schematic verified by chip mapping, detail identifications of components of interest, metallization systems and sketches of important cross sections of the following devices are shown in individual reports in the appendix.

Vendor A: 54S00
54S138
54LS00 (old and new design)
54LS138

Vendor B: 9S00
9LS00
93S138

All standard and low power quadruple dual input nand gates in the study utilize a 14 lead ceramic dual-in-line package (TO-116), while the S138 and LS138 are packaged in a 16 lead ceramic dual-in-line package.

The kovar leads were tin plated externally. Internal wire bonds on all devices were accomplished using 1 mil aluminum wire 99.9% pure. Schottky device chip areas range from .83 mm^2 to 3.4 mm^2. Die thickness between vendors and types vary from .17 to .25 mm. A direct relationship between die size and circuit complexity is evident.

The final selection of Schottky parts was made to include device types from two vendors with low and medium complex circuitry in both standard and low power versions.

All device types have glassivation covering the entire chip with exposed bonding pads only. The surface glassivation for Vendor B's devices is phosphorous doped for thermal expansion purposes, while Vendor A's glassivation does not contain any dopants. A single layer metallization is used for all types, with diffused underpasses where required. A trimetal system containing titanium-tungsten as a barrier and aluminum as the main conductor is used throughout. No dopants were used in the aluminum in any devices analyzed. 99.9% purity is quoted by both vendors. Platinum silicide contacting areas of highly doped N regions result in ohmic contacts while platinum silicide contacting areas of low doping material form the Schottky barrier diodes.

Measurements of metallization width and thickness were made by the use of high magnification photographs and cross sections of selected devices. From the above measurements cross sectional areas were calculated. These cross sectional areas are nominal and do not reflect any thinning at oxide steps or defects. Current densities were computed for all vendor device types and found to be highest in the emitter metallization of the bottom transistor in the output circuits. Vendor A's nominal current density was 2.5×10^5 A/cm^2 for the 54S00. This value exceeds the maximum worst case current density permitted in MIL-M-38510 of 2×10^5 A/cm^2.

Vendor A's 54LS00 low power quadruple two input nand gates were of two different designs. The older design occupies a chip area of 1.8 mm^2 and uses a current limiting resistor of 200Ω in the collector of the output Darlington pair. The newer design with a chip area of 1.1 mm^2 using approximately the same device dimensions in a more condensed fashion has a collector resistance of approximately 50Ω in the Darlington pair.

Tables 12 and 13 list important features and basic differences between all device types included in the study as they relate to different vendors.

TABLE 12

Vendor	Device Type	Chip Dimensions Length (mm)	Width (mm)	Thickness (μm)	Area	Underpasses Used	Contact	Metallization Used
A	54S00	1.04	1.04	218	1.08	No	PT.Silicide	Ti-W-Al
B	9S00	1.10	1.04	242	1.14	No	PT.Silicide	Ti-W-Al
A	54S138	1.75	1.38	230	2.42	No	PT.Silicide	Ti-W-Al
B	93S138	1.99	1.69	250	3.36	Yes	PT.Silicide	Ti-W-Al
A	54LS00 Old Design	1.32	1.32	220	1.74	No	PT.Silicide	Ti-W-Al
A	54LS00 New Design	1.10	.97	170	1.07	No	PT.Silicide	Ti-W-Al
B	9LS00	1.20	.69	240	.83	No	PT.Silicide	Ti-W-Al
A	54LS138	1.85	1.55	240	2.87	No	PT.Silicide	Ti-W-Al

TABLE 12 (continued)

Vendor	Device Type	EPI Thick-ness (μ)	Barrier Metal Thick-ness (Å)	Surface Glass-ivation Thick-ness (μ)	Deposited SiO_2 Dopants	Thermal Oxide Present ?
A	54S00	3.0	3000	2.0	None	Yes
B	9S00	4.4	3000	2.3	Phosphorus	Yes
A	54S138	3.2	4000	.6	None	Yes
B	93S138	3.2	4000	1.5	Phosphorus	Yes
A	54LS00 Old design	Not Measured	Not Measured	1.2	None	Yes
A	54LS00 New design	4.0	4000	1.8	None	Yes
B	9LS00	3.0	4000	1.1	Phosphorus	Yes
A	54LS138	3.2	4000	1.2	None	Yes

TABLE 13

Current Density Calculations

Vendor	Device Type	Metallization Width (μ)	Highest Current Density Metallization	Aluminum Metallization Thickness (μ)	Cross Sectional Area (μm^2) Nominal	Output Load Current (mA)	Current Density (A/cm^2)
A	54S00	6.3	Emitter	1.4	8.82×10^{-8}	22[a]	2.5×10^5
B	9S00	7.6	Emitter	1.4	10.64×10^{-8}	22[a]	2.1×10^5
A	54S138	8.5	Emitter	2.0	17.0×10^{-8}	22[a]	1.3×10^5
B	93S138	9.0	Emitter	1.6	14.4×10^{-8}	22[a]	1.5×10^5
A	54LS00 Old design	18.0	Collector	2.0	36.0×10^{-8}	4	1.1×10^4
A	54LS00 New design	21.0	Collector	2.0	42.0×10^{-8}	4	9.5×10^3
B	9LS00	10.6	Emitter	2.0	21.2×10^{-8}	4	1.9×10^4
A	54LS138	11.4	Collector	1.6	18.24×10^{8}	4	2.2×10^4

[a]Note: The current of 22mA consists of 20mA external load current I_{OL} plus 2mA of internal base drive.

V. LIFE TESTING

A. Life Test Configuration

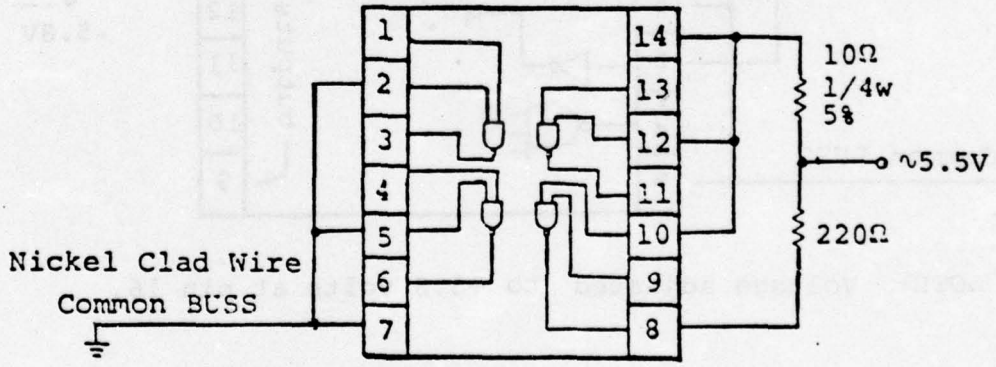
The life test is broken down into two major areas: one, as originally proposed, consists of various HTRB modified configurations and is identified as (1), and the other consists of (2) a dynamic test to HTRB comparison which is limited to 54LS00 from two vendors only.

During the performance of the life test the V_{CC} power supplies were adjusted so that +5.3V were obtained at the device V_{CC} terminal (14 or 16). Also, individual device I_{CC} currents were determined by measuring the voltage drop across the 10 ohm limiting resistor. These current verifications were performed at 30 minutes and 4 hours at the initial step and at 2 hours at all subsequent time periods. Every external loaded output of each device was verified as to the proper operations.

Since device currents were verified at various times into the tests and found to be stable at all test temperatures selected, it can be stated that no thermal runaway or latch up occurred.

1. HTRB Configurations

a. Standard 54S00: The 54S00 consists of 4 dual input NAND gates. In order to determine whether or not electromigration occurs, one output is loaded using a 220Ω resistor to V_{CC} resulting in approximately 22mA. All remaining outputs are left open (Figure 8). The inputs are wired in such a way that all possible bias configurations are satisfied. Using this approach two outputs are forced into a high state while two outputs are in the low state one of which is loaded with 22mA.

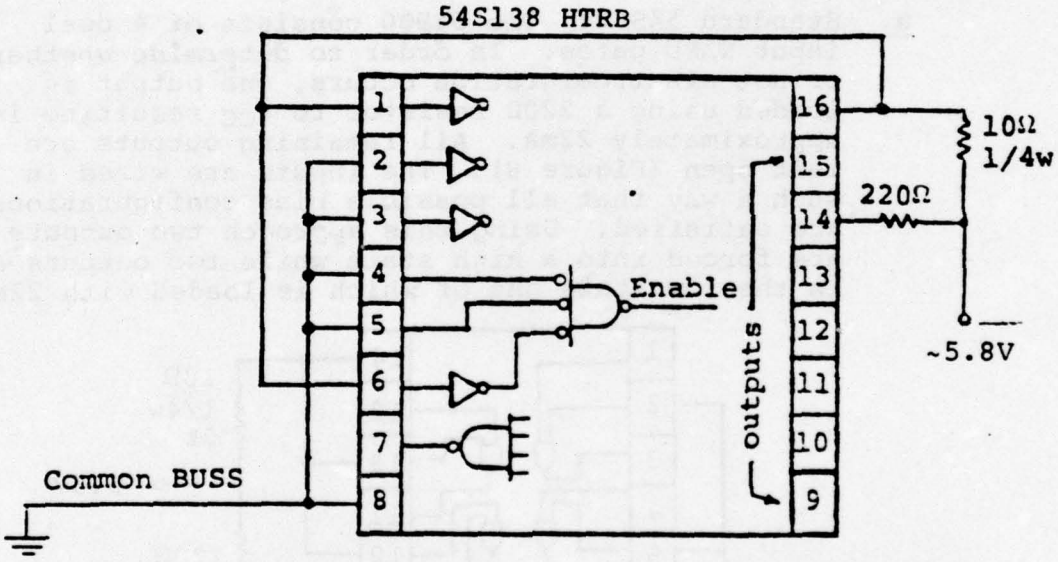


NOTE: Voltage adjusted to +5.3 volts at pin 14.

FIGURE 8

An additional reason for the above configuration having two outputs in the high and two outputs in the low state is to prevent thermal runaway of the devices at temperatures above 250°C because the internal dissipation increases when outputs are in the low state.

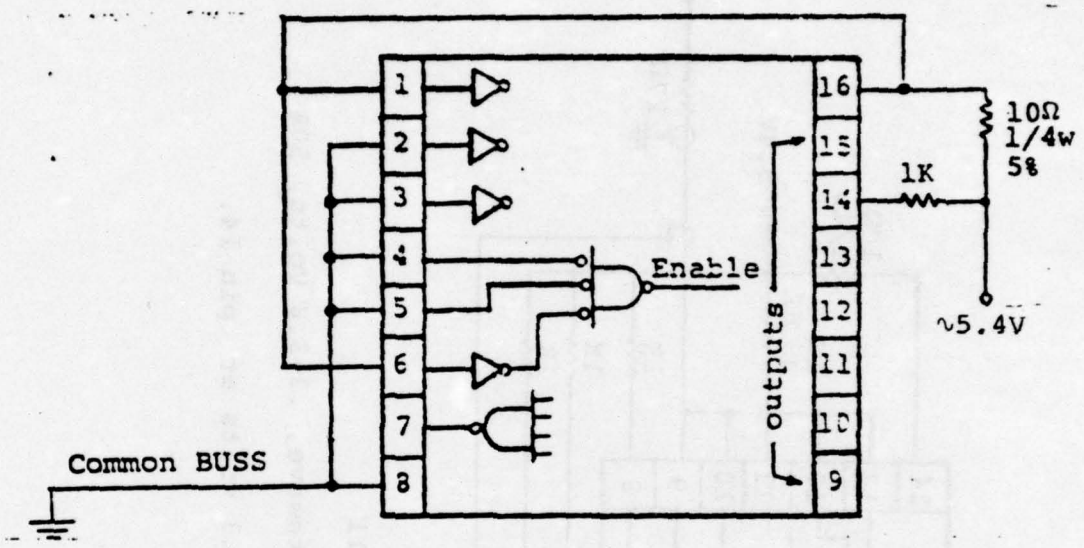
b. Standard 54S138: The device is a 1 of 8 decoder/demultiplexer having 8 outputs and six inputs. The device is biased such that only output 14 is in a low state (Figure 9). This output is loaded with 22mA to detect electromigration, should it occur. In order to achieve the output conditions as outlined, 4 inputs are tied to ground while 2 are tied to V_{CC}. With this both possible input bias conditions are covered.



NOTE: Voltage adjusted to +5.3 volts at pin 16.

FIGURE 9

c. Low Power 54LS138: The 54LS138 is biased in the same manner as the standard 54S138 with the exception of a lower output load of 5mA (Figure 10).



NOTE: Voltage adjusted to +5.3 volts at pin 16.

FIGURE 10

2. HTRB and Dynamic Comparison

The 54LS00 consists of 4 dual input NAND gates.

a. 54LS00 Dynamic Configuration: The biasing of this device follows the recommended circuit configuration of MIL-M-38510/300 and MIL-STD-883 Method 1015, test condition D. All outputs are loaded using 1k resistors (Figure 11).

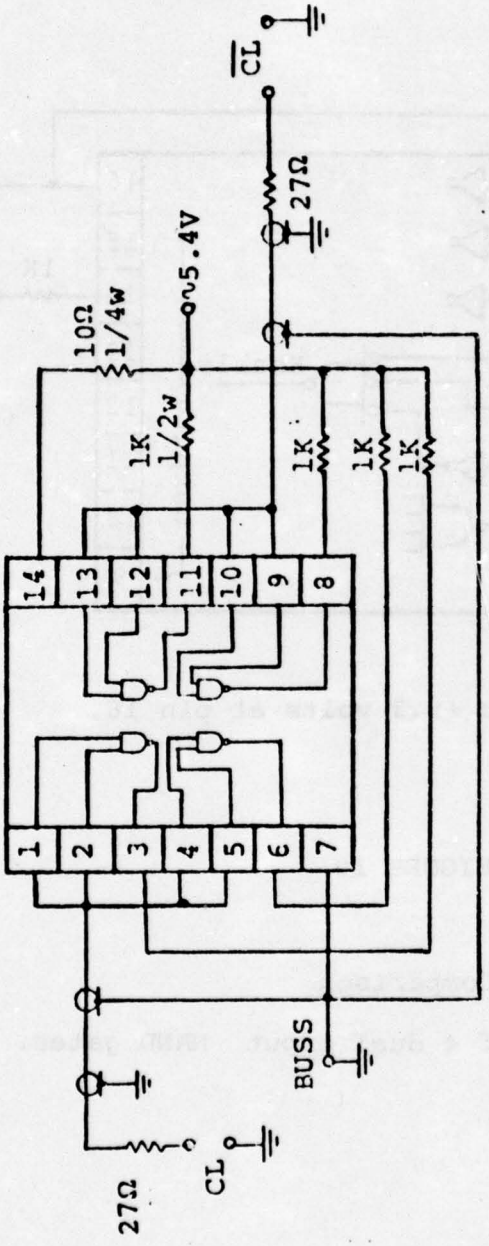
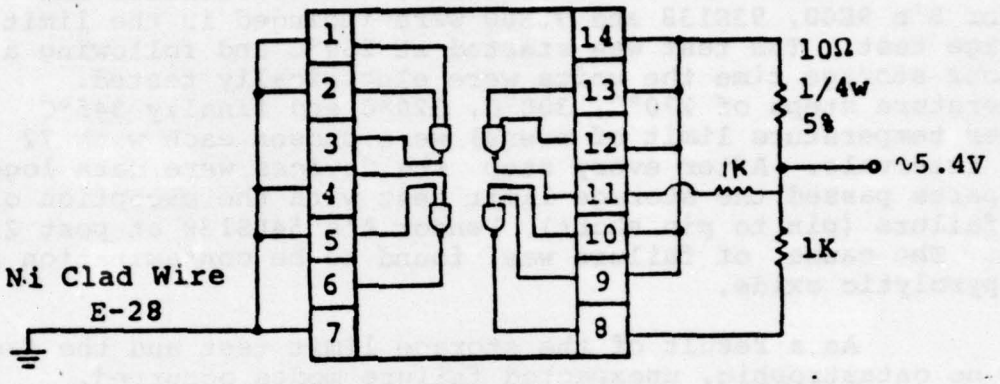


FIGURE 11

NOTE: CP or $\overline{CP}$ = 100 KHz squarewave, .3-3.8 Volts, 50% duty cycle.
Voltage adjusted to +5.3 volts at pin 14.

b. 54LS00 HTRB Configuration: To achieve a valid comparison with the dynamic circuit, two outputs are biased in a high state while two are forced low and also loaded with 1k resistors. The inputs are either both tied to ground or V_{CC} (Figure 12).



NOTE: Voltage adjusted to +5.3V at pin 14.

FIGURE 12

B. Limit Tests

1. Storage Limit

Specific literature research and information gathered from vendors resulted in a tentative selection of +250°C and +300°C for the long term storage life test. Limit testing was performed to verify the selection of these temperatures.

Vendor A's 54S00, 54S138, 54LS00, 54LS138 and Vendor B's 9S00, 93S138 and 9LS00 were included in the limit storage test. The test was started at 250°C and following a 72 hour storage time the units were electrically tested. Temperature steps of 270°C, 300°C, 320°C and finally 345°C (upper temperature limit of ovens) were chosen each with 72 hour intervals. After every step the devices were data logged. All parts passed the storage limit test with the exception of one failure (pin to pin short), Vendor A's 54LS138 at post 250°C test. The cause of failure was found to be contamination in the pyrolytic oxide.

As a result of the storage limit test and the fact that no catastrophic, unexpected failure modes occurred, temperatures of +250°C and 300°C were selected for the long term storage test.

2. Operating Life

All low power Schottky devices 54LS00, 9LS00 and 54LS138 were limit tested in a 72 hour interval at ambient temperatures of 235°C, 250°C, 270°C, 280°C and 288°C in reverse bias voltage configuration. In addition to the HTRB, two groups each of 10 devices for the 54LS00 and 9LS00 were operated in a dynamic mode at 100KHz in temperature steps and intervals as above. No failures occurred.

The standard Schottky devices were limit tested at 225°C, 240°C, 255°C, 265°C, 275°C and 285°C in steps of 72 hours using a reverse bias configuration only. With the exception of one of Vendor A's 54S00 failing the final ambient temperature step of 285°C (T_J = 294°C), no other failures were recorded. The failed device exceeded the V_{OL} limit of .5V and subsequent failure analysis showed the effects of electro-migration in the emitter metallization of the loaded (22mA) output transistor.

All units were data logged following each temperature interval.

C. Long Term Life Tests

1. Storage Long Term Life

Long term storage life tests were conducted according to the test plan in Table 1. This shows that all device types were subjected to a +250°C environment for a total of 3500 hours. Vendor A's 54S00, 54S138, 54LS138, 54LS00 as well as Vendor B's 9LS00 were additionally subjected to +300°C long term storage for a total of 2700 hours. The results are summarized in Table 14.

During the performance of the 250°C long term storage testing devices were tested at accumulated times of 25*, 50*, 100, 250, 680, 1000, 1500, 2216, 2700* and 3500* hours. Devices in the 300°C long term storage environment were tested at accumulated times of 25*, 50*, 100, 250, 500, 1336, 1800* and 2700* hours. Device failures during the performance of long term storage occurred in only three types: Vendor A's 54S138, 54LS138 and Vendor B's 93S138.

Vendor B's 93S138 failed at the end of long term testing in the 250°C environment at an accumulated time of 3500 hours. Electrical tests performed on this device indicated an increase in power supply current of approximately 22mA and, additionally, an increase in input low current exceeding the maximum limit of 2mA. The failure mechanism was determined to be metal penetration through oxide pin holes.

Vendor A's 54LS138 was rejected during electrical test after only 25 hours of long term storage at 300°C for increase in power supply current. The associated failure mechanism was related to contamination in the oxide. Since the failure occurred at 25 hours, while no other failure was recorded to the end of the test, the device was classified as an early life failure and therefore excluded as a data point for failure rate calculations. Because of limited real time failures experienced during the test phase the following assumptions were made in order to perform failure rate calculations (exclusive of Vendor A's 54S138):

*Note: At indicated test times, all device parameters were data logged.

TABLE 14: Results of Storage Life Tests

Vendor	Device Type	Storage Temperature +250°C [3500 hours duration] Devices Under Test	Total Failures	Remarks	+300°C [2700 hours duration] Devices Under Test	Total Failures	Remarks
A	54S00	15	0	-	15	0	-
B	9S00	15	0	-	-	-	-
A	54S138	15	(3)[a]	-	13	(2)[b]	-
B	93S138	15	1	1 failure at 3500 hrs.	-	-	-
A	54LS00	10	0	-	10	0	-
B	9LS00	10	0	-	10	0	-
A	54LS138	15	0	-	13	1	1 failure at 25 hours

NOTES: [a]Possible damage as result of electrostatic discharge.

[b]1 device failed with possible damage resulting from electrostatic discharge.
1 device considered "freak" (only device showing corrosion)

a) A standard deviation of $\sigma = 1.0$ typical for a matured and reliable product.

b) An activation energy of Ea = 1.0eV for surface related problems was used for worse case calculations.

c) One device failure was assumed at the end of the storage life test at the highest temperature environment and with the already assumed standard deviation of $\sigma = 1.0$, mean times to failure were calculated.

The calculated worst case failure rates are shown in Table 15 at two temperatures of +165°C and +125°C, for two time intervals of 10^4 and 10^5 hours. Vendor B's 9S00 failure rates appear inferior to Vendor A's 54S00 at 10^5 hours and a junction temperature of +165°C. No failures occurred at +250°C for both device types. Vendor A's 54S00 was additionally subjected to +300°C storage, where also no failures occurred and therefore the calculated failure rates would be superior.

One device of Vendor A's 54S138 unit number 70, which failed at 1800 hours for I_{IL}, was found to have an open metallization due to corrosion. The device previously passed all hermeticity tests and was considered a freak particularly since no traces of corrosion were found in any other units examined.

Four additional failures shown but not counted in Table 14 failed electrical test for high input leakage at pin 1 only. This failure mode and mechanism is explained in a separate section and believed to be damage resulting from electrostatic discharge caused possibly during handling of these devices.

2. Operating Life Static

The life test data is summarized in various tables and plotted as a function of time (log scale) versus cumulative percentage on normal probability scale for Vendor A's 54S00 where sufficient data points were available. The graph contains three curves for varying temperature stress keeping voltage and load current constant. Above plot was used for calculating the standard deviation σ and for determining the median life time.

TABLE 15: Calculated Failure Rates
(Storage Conditions)

Vendor	Device Type	Failure Rates				Based on Storage Life Test Temperature of:
		$T_A = T_J = +165°C$		$T_A = T_J = +125°C$		
		10^4 hours [%/1000 hours]	10^5 hours [%/1000 hours]	10^4 hours [%/1000 hours]	10^5 hours [%/1000 hours]	
A	54S00	<.0001	<.0001	<.0001	<.0001	300°C
B	9S00	<.0001	.01	<.0001	<.0001	250°C
A	54LS00	<.0001	<.0001	<.0001	<.0001	300°C
B	9LS00	<.0001	<.0001	<.0001	<.0001	300°C
A	54S138	<.0001	<.0001	<.0001	<.0001	300°C
B	93S138	<.0001	.01	<.0001	<.0001	250°C
A	54LS138	<.0001	<.0001	<.0001	<.0001	300°C

For deviation of activation energy and median life predictions at operating junction temperatures, a regression curve following an Arrhenius relationship was drawn.

Failure rate calculations were based on extrapolated median life times and derived standard deviation at junction temperatures of +125°C and +165°C following Bell Telephone (D.S. Peck) publications.

a. Vendor A 54S00

The operating life test data results are shown in Table 16. Graphical displays of the data as shown in Figure 13 are based on the best fit line at one of the three temperature stress levels to establish the standard deviation ($\sigma = 1.12$). For the other two stress levels the lines were drawn using the same sigma. Where sufficient data points were available the use of constant σ for varying temperature stress levels appeared to be justified.

The regression curve as shown in Figure 14 allows determination of median life times at lower junction temperatures. The calculated activation energy Ea was .56eV. The observed failure mode was increased emitter resistance and the associated failure mechanism was found to be aluminum void and hillock formation as a result of electromigration. Previously calculated nominal current densities were 2.5×10^5 A/cm^2.

At operating junction temperatures of +165°C, +125°C and ambient temperature of +125°C, the following failure rates were computed for a time duration of 10^4 and 10^5 hours (see Table 17).

TABLE 16: Vendor A 54S00 Operating Life Results

Total No. of Hours Accumulated	T_J = 227°C		T_J = 257°C		T_J = 282°C	
	Accum. # of V_{OL} Rejects	Accum. %	Accum. # of V_{OL} Rejects	Accum. %	Accum. # of V_{OL} Rejects	Accum. %
25	0	0	0	0	0	0
50	0	0	0	0	0	0
100	0	0	0	0	0[a]	0
250	0	0	0	0	0	0
500	0	0	1	6.7	0	0
1000	0	0	2	13.3	4	28.6
1596	-	-	6	40	7	50
1620	2	13.3	-	-	-	-
2400	-	-	6	40	7	50
2568	3	20	-	-	-	-

[a]Note: One additional device failure was observed at 100 hours. The failure mode, recorded as I_{CEX} reject, was different than the predominant failure mode of all devices shown in the table. The major failure mode was found to be an increase in V_{OL}.

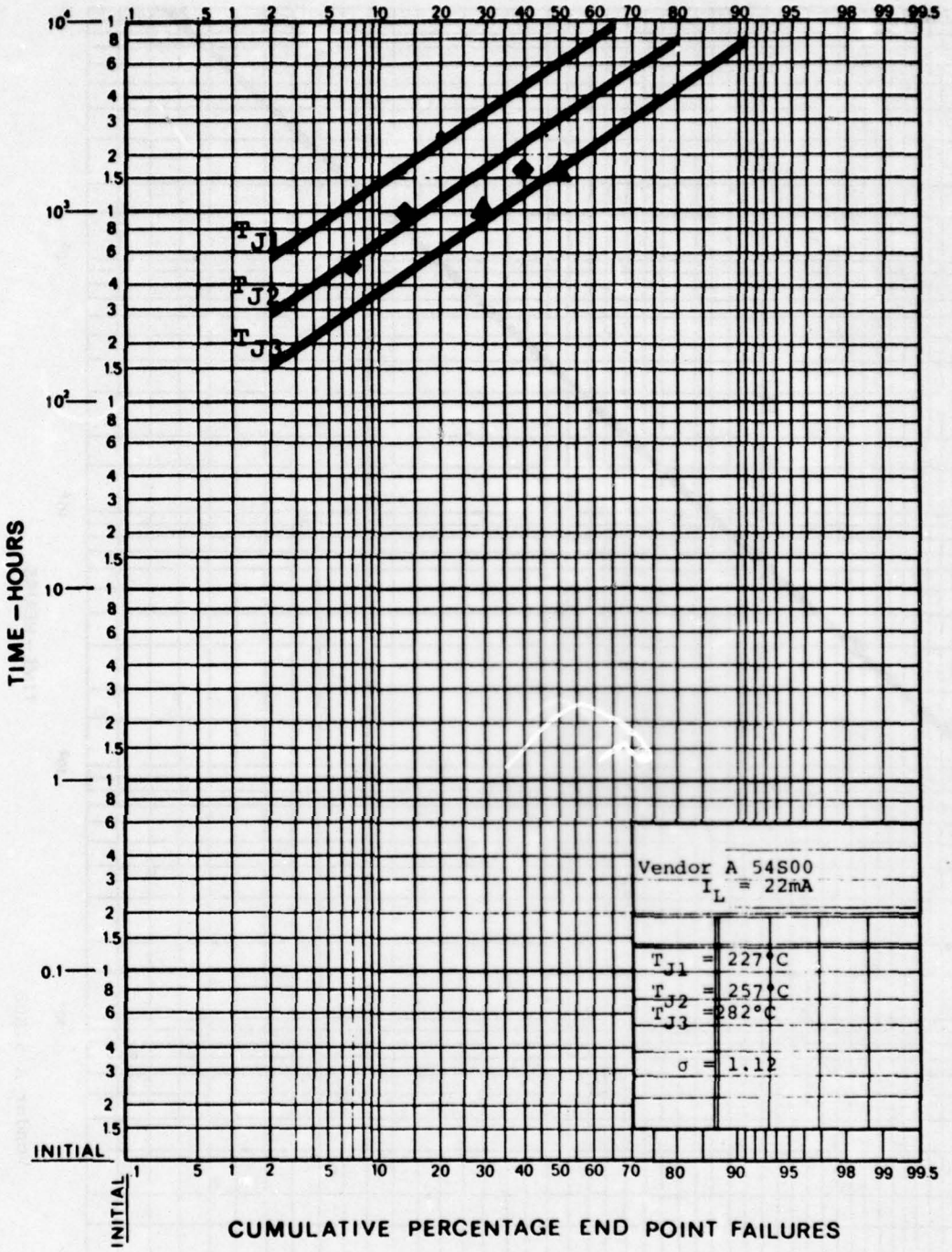


FIGURE 13: Graphic Display of Life Test Results

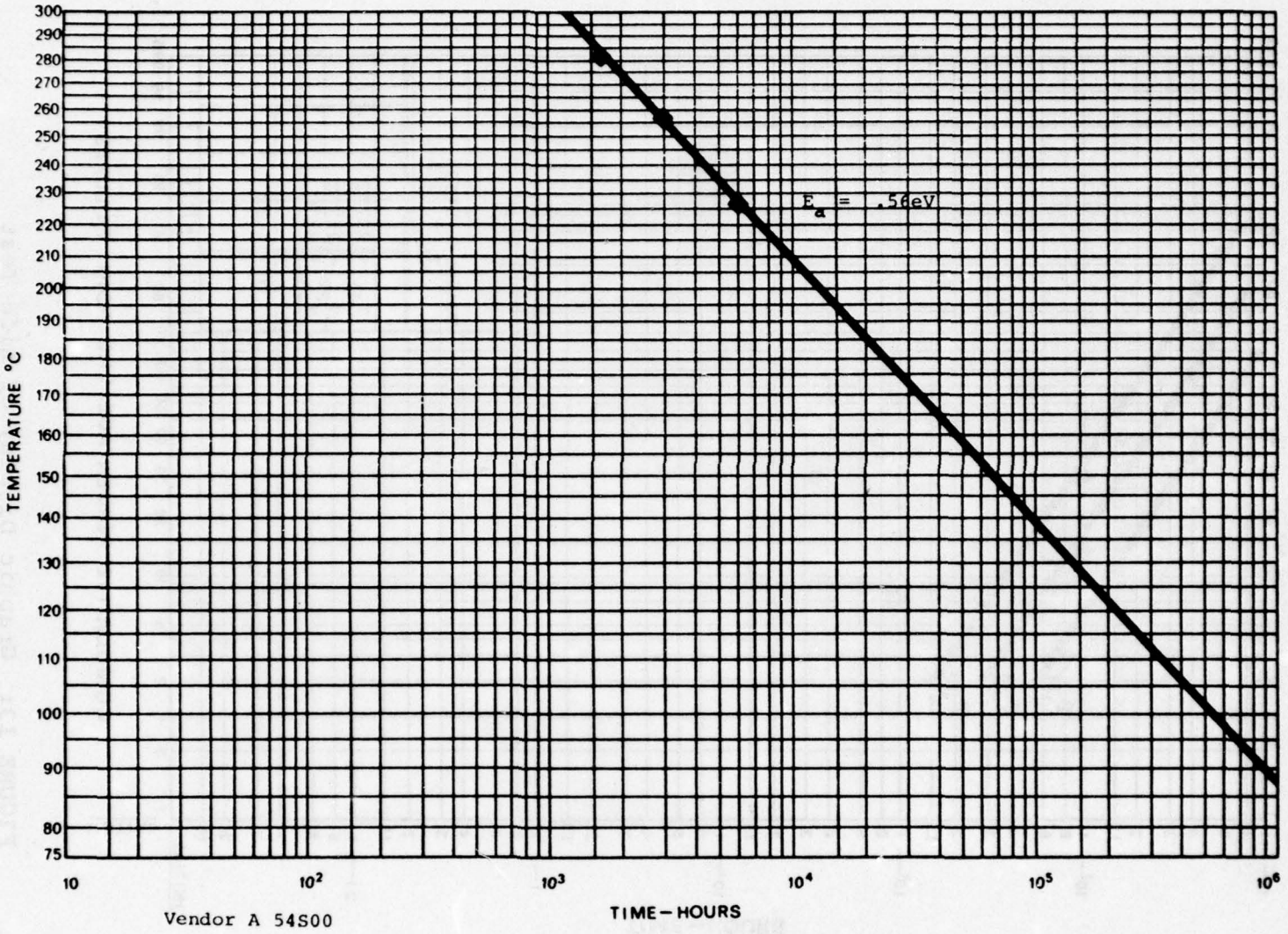


FIGURE 14: Regression Curve

TABLE 17: Operating Life Failure Rates
Vendor A 54S00

Failure Rates [%/1000 hours] 10^4 hours	10^5 hours	Remarks
.11	.43	T_J = +125°C
.81	.84	T_A = +125°C
1.75	1.50	T_J = +165°C

b. Vendor A 54S138

The results of the life test data is shown in Table 18. One device failure which occurred at 50 hours (T_J = 265°C) for excessive power supply current was considered an early life failure. One additional device failure detected at 250 hours (T_J = 290°C) rejected for increase in leakage current at the input 3 clamping diode was considered a "freak", since no additional failures occurred to the end of the operational life test. All other device failures shown displayed an increase in leakage current at pin 1 and were believed to have been damaged during handling as a result of electrostatic discharge. The failure mechanism is discussed in another section.

For calculations of failure rates one failure was assumed at the end of the test using a standard deviation σ = 1.0 and an activation energy of Ea = 1.04eV. The resulting failure rates are shown in Table 19 for T_J = +125°C, T_A = +125°C and T_J = +165°C.

TABLE 18: Vendor A 54S138 Operating

Total No. of Hours Accumulated	T_J = 209°C		T_J = 265°C		T_J = 290°C	
	Accum. # of Rejects	Accum.	Accum. # of Rejects	Accum.	Accum. # of Rejects	Accum.
25	0	0	0	0	0	0
50	0	0	(1)[a]	0	0	0
100	0	0	(1)	0	0	0
250	0	0	(1)	0	(1)[b]	0
500	0	0	(2)[c]	0	(1)[c]	0
1000	0	0	(4)[c]	0	(2)[c]	0
1500	0	0	-	-	-	-
1596	-	-	(6)[c]	0	(3)[c]	0
2000	0	0	-	-	-	-
2400	(3)[c]	0	(6)[c]	0	(3)[c]	0
3500	(3)[c]	0				

Notes:

a. Device failure considered early life due to excessive power supply current.

b. Device failure for degradation of input Schottky clamp diode on pin 3 was considered a "freak" since no additional failures occurred to the end of the life test with the failure mechanism.

c. All device failures shown are believed to have been damaged as a result of electrostatic discharge.

TABLE 19: Operating Life Failure Rates
Vendor A 54S138

Failure Rates [%/1000 hours] 10^4 hours	10^5 hours	Remarks
<.0001	<.0001	T_J = +125°C
<.0001	<.0001	T_A = +125°C
<.0001	.0003	T_J = +165°C

c. Vendor A 54LS00

Devices subjected to HTRB at a junction temperature of +221°C completed 2568 hours without failures. Similarly, on devices subjected to +251°C and +276°C, no failures were recorded to the end of the test at 2400 hours.

To calculate failure rates, one failure was assumed at T_J = 276°C and 2400 hours. A standard deviation σ = 1.0 and an activation energy of E_a = 1.04eV (surface effects) were used in the calculation. In Table 20 the resulting failure rates are quoted for three temperature and time durations of 10^4 and 10^5 hours.

TABLE 20: Operating Life Failure Rates
Vendor A 54LS00

Failure Rates [%/1000 hours] 10^4 hours	10^5 hours	Remarks
<.0001	<.0001	T_J = 125°C
<.0001	<.0001	T_A = 125°C
<.0001	.0011	T_J = 165°C

d. Vendor A 54LS138

The results of the operating life test are shown in Table 21 covering all failure modes observed. The three device failures, having been recorded at 25 hours, were considered early life failures and therefore, were not included in failure rate predictions. The unit rejected from the lowest temperature environment failed during functional test. None of the outputs could be switched to the low state. Surface contamination is believed to be the cause of the failure. From the additional two recorded failures one was rejected for high input leakage as a result of channeling while the other failed for excessive power supply current due to contamination of the pyrolytic oxide.

For failure rate calculation, one device failure was assumed at the end of 2400 hours at the highest temperature environment. A standard deviation $\sigma = 1.0$ and an activation energy $E_a = 1.04$eV were used in the calculations.

Failure rates are presented in Table 22 for $T_J = 125°C$ and 165°C and also for $T_A = 125°C$.

TABLE 21: Vendor A 54LS138 Operating Life Test Results

Total No. of Hours Accumulated	T_J = 222°C		T_J = 252°C		T_J = 277°C	
	Accum. # of Rejects	Accum. %	Accum. # of Rejects	Accum. %	Accum. # of Rejects	Accum. %
25	(1)[a]	0	0	0	(2)[a]	0
50	(1)	0	0	0	(2)	0
100	(1)	0	0	0	(2)	0
250	(1)	0	0	0	(2)	0
500	(1)	0	0	0	(2)	0
1000	(1)	0	0	0	(2)	0
1596	-	-	0	0	(2)	0
1620	(1)	0	-	-	-	-
2400	-	-	0	0	(2)	0
2568	(1)	0	-	-	-	-

Note: a. Early life failures

TABLE 22: Operating Life Failure Rates
Vendor A 54LS138

Failure Rates [%/1000 hours]		Remarks
10^4 hours	10^5 hours	
<.0001	<.0001	T_J = 125°C
<.0001	<.0001	T_A = 125°C
<.0001	.0019	T_J = 165°C

e. Vendor B 9S00

During the performance of high temperature testing at junction temperatures of T_J = 228°C and 258°C no failures were recorded at the end of the test of 2568 hours and 2400 hours respectively. One device failure assumed at the end of the highest temperature test, a standard deviation of σ = 1.0 and two activation energies have been used for the calculations. E_a = 1.04eV for surface related effects and E_a = 1.2eV quoted in literature for glassivated conductors. The additional calculation of failure rates using activation energies of 1.2eV was presented for comparison purposes to Vendor A's 54S00 devices whose failure mechanism was found to be void and hillock formation in the aluminum. Since Vendor B's 9S00 also resulted in high nominal calculated current densities of $1.9 \times 10^5 A/cm^2$ a second calculation was made. The resulting failure rates are shown in Table 23.

TABLE 23: Operating Life Rates, Vendor B 9S00

Failure Rates [%/1000 hours]		Remarks	
10^4 hours	10^5 hours		
<.0001	<.0001	T_J = 125°C	
<.0001	.0004	T_A = 125°C	E_a = 1.04eV
<.0001	.01	T_J = 165°C	
<.0001	<.0001	T_J = 125°C	
<.0001	<.0001	T_A = 125°C	E_a = 1.2eV
<.0001	.0011	T_J = 165°C	

Note: The above values are for comparison purposes only but for surface related problems these are the worst case failure rates which can be guaranteed by the test.

f. Vendor B 93S138

No failures were recorded during the performance of HTRB to the end of the life test at 3500 hours at T_J = 209°C and 2400 hours at T_J = 265°C. The assumption for failure rate calculations were: one failure at the end of the highest temperature environment, standard deviation σ = 1.0 and an activation energy E_a = 1.04eV. The resulting failure rates are shown in Table 24:

TABLE 24: Operating Life Failure Rates, Vendor B 93S138

Failure Rates		Remarks
10^4 hours	10^5 hours	
<.0001	<.0001	T_J = 125°C
<.0001	.0043	T_A = 125°C
<.0001	.0043	T_J = 165°C

g. Vendor B 9LS00

Devices were subjected to three temperature environments +220°C, 250°C and 275°C. The tests were concluded at 2568 hours, 2400 hours and 2400 hours respectively. Only one failure was recorded during the long term HTRB life testing. The device was rejected for excessive I_{CEX} at 500 hours at the median temperature of 251°C. It was considered atypical since no additional failures occurred to the end of the test.

Failure rate calculations are based on the assumption of one failure at the end of the test at 275°C, σ = 1.0 and E_a = 1.04eV.

The results are summarized in Table 25.

TABLE 25: Operating Life Failure Rates, Vendor B 9LS00

Failure Rates [%/1000 hours]		Remarks
10^4 hours	10^5 hours	
<.0001	<.0001	T_J = 125°C
<.0001	<.0001	T_A = 125°C
<.0001	.0011	T_J = 165°C

3. Operating Life Dynamic

a. Vendor A 54LS00

Three groups of 15 devices each were subjected to high temperature dynamic operation in a configuration shown in Figure 11. Units operating at a junction temperature of +221°C did not experience any failures to the end of the test at 2568 hours. Even at junction temperatures of +251°C and 276°C, no device failures were observed. The stress testing at these temperatures was concluded at an elapsed time of 2400 hours. Post inspection of devices did not yield any failure mechanisms in progress.

Therefore, in order to obtain failure rate predictions, a device failure was assumed to have occurred at the highest environmental temperature at the conclusion of the test. A standard deviation of $\sigma = 1.0$ (implying a mature process) and an activation energy of $E_a = 1.04$eV (surface related) were also assumed. These assumptions lead to a worst-case failure rate and, hence, is very conservative. The results are summarized in Table 26.

TABLE 26: Operating Failure Rates (Dynamic/Worst Case)
Vendor A 54LS00

Failure Rates [%/1000 hours]		Remarks
10^4 hours	10^5 hours	
<.0001	<.0001	T_J = 125°C
<.0001	<.0001	T_A = 125°C
<.0001	.0011	T_J = 165°C

b. Vendor B 9LS00

According to the test plan in Table 1, Vendor B's 9LS00 was also subjected to a high temperature dynamic life stress test. During this long term testing, the units were operated in the same configuration as Vendor A's 54LS00.

No device failures were recorded to the end of the test at the lowest junction temperature of +221°C and 2568 hours. Tests for devices operating at junction temperatures of +251°C and 276°C were concluded at an accumulated time of 2400 hours. One device failure was observed at 2400 hours in the 250°C environment (T_J = 251°C). The failure mode as recorded was an increase of input leakage. Analysis revealed this to be caused by channeling. The device failure was considered atypical since no failures occurred at the higher temperature.

For failure rate calculations, the same assumptions were made as for the Vendor A case in the last section, even though a surface related failure was observed at T_J = 251°C and was considered atypical.

One failure at the end of the test at T_J = 276°C;
Standard deviation σ = 1.0;
Activation energy E_a = 1.04eV.

The resulting failure rates are summarized in Table 27.

TABLE 27: Operating Failure Rates (Dynamic), Vendor B 9LS00

Failure Rates [%/1000 hours]		Remarks
10^4 hours	10^5 hours	
<.0001	<.0001	T_J = 125°C
<.0001	<.0001	T_A = 125°C
<.0001	.0011	T_J = 165°C

4. Discussion of Results

A failure rate comparison chart for all devices included in the study is shown in Table 28. Three temperatures were chosen for comparison purposes. A junction temperature of +165°C was selected since the maximum operating ambient temperature as per MIL-M-38510/70 and 300 is stated to be +125°C. This temperature was chosen because at +125°C ambient Vendor B's 93S138 junction temperature reached +165°C. Under worst case conditions defined as highest power consumption and still air environment all other device types did not exceed a junction temperature of +165°C.

All devices of both low and standard power version with the exception of Vendor A's 54S00 can be considered reliable product and meet the reliability standards outlined in the MIL-HDBK-217B.

At junction temperatures of +125°C failure rates are less than .0001%/1000 hours for all devices with the exception of Vendor A's 54S00. The failure rates for Vendor A's 54S00 are in the order of 1.75%/1000 hours at T_J = 165°C. The high failure rate was the result of electromigration causing high V_{OL}.

TABLE 28: FAILURE RATE COMPARISON CHART

VENDOR	TYPE	T_J = 125°C		T_A = 125°C*		T_J = 165°C		REMARKS
		at 10^4 hrs	at 10^5 hrs	at 10^4 hrs	at 10^5 hrs	at 10^4 hrs	at 10^5 hrs	
A	54S00	.11	.43	.81	.84	1.75	1.50	HTRB (Electro-migration
		<.0001	<.0001	<.0001	<.0001	<.0001	<.0001	Storage $T_A=T_J$
B	9S00	<.0001	<.0001	<.0001	.0004	<.0001	.01	HTRB
		<.0001	<.0001	<.0001	<.0001	<.0001	.01	Storage $T_A=T_J$
A	54S138	<.0001	<.0001	<.0001	<.0001	<.0001	.0003	HTRB
		<.0001	<.0001	<.0001	<.0001	<.0001	<.0001	Storage $T_A=T_J$
B	93S138	<.0001	<.0001	<.0001	.0043	<.0001	.0043	HTRB
		<.0001	<.0001	<.0001	<.0001	<.0001	.01	Storage $T_A=T_J$
A	54LS00	<.0001	<.0001	<.0001	<.0001	<.0001	.0011	HTRB
		<.0001	<.0001	<.0001	<.0001	<.0001	.0011	Dynamic Oper.
		<.0001	<.0001	<.0001	<.0001	<.0001	<.0001	Storage $T_A=T_J$
B	9LS00	<.0001	<.0001	<.0001	<.0001	<.0001	.0011	HTRB
		<.0001	<.0001	<.0001	<.0001	<.0001	.0011	Dyanmic Oper.
		<.0001	<.0001	<.0001	<.0001	<.0001	<.0001	Storage $T_A=T_J$
A	54LS138	<.0001	<.0001	<.0001	<.0001	<.0001	.0019	HTRB
		<.0001	<.0001	<.0001	<.0001	<.0001	<.0001	Storage $T_A=T_J$

NOTE:

*Junction temperature at the +125°C ambient environment was calculated for still air conditions and worst case power consumption.

Values are in percent per 1000 hours.

Low power Schottky devices of Vendor A and B's quadruple two input positive NAND gates were operated during long term life test in both HTRB and dynamic mode for comparison purposes and performed under identical conditions. With the exception of the atypical failures for Vendor B's 9LS00 discussed earlier (one during dynamic and one during HTRB), no other failures occurred. Therefore, the effectiveness of static versus dynamic stress testing on low power Schottky devices can not be measured.

VI. CRITERIA FOR FAILURE AND RESULTS

Devices rejected when tested on the Fairchild 5000 tester exceeding specified limits were individually verified through bench testing. Subsequently, all devices were checked for hermeticity. Failed units were classified as to failure mode. All devices having failed as a result of operating life test were subjected to high temperature baking as part of the electrical analysis procedure.

A. Major Failure Modes and Electrical Analysis

1. Increase in V_{OL}

In order to display this mode the failing devices were biased with +4.5V V_{CC} and the inputs were electrically addressed so that all outputs were in the low state. A Tektronix 576 curve tracer was used to display output voltage versus output current. The photograph in Figure 15 shows the characteristics of three good and one failing output. The initial slope of the passing outputs suggests a value of 7 ohms while the failing output results in 37 ohms. The increase in offset voltage (low collector current) evident in the photograph suggested the increase of resistance to be in the emitter. Detail analysis conducted later verified the cause of failure to be in the emitter metallization.

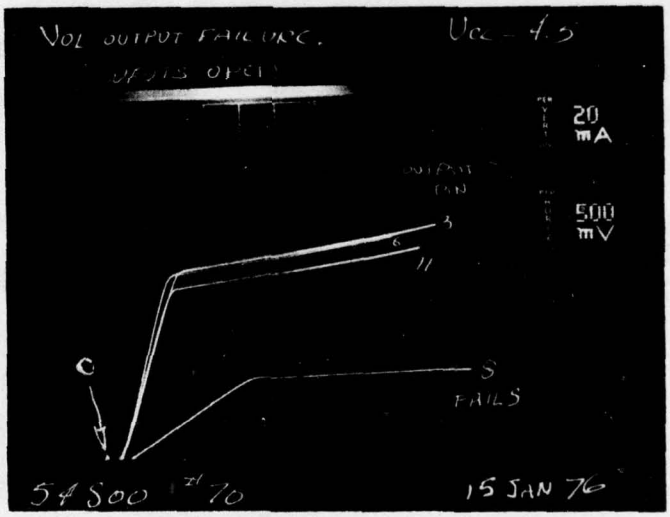


FIGURE 15: Vendor A 54S00 #70, dc 7330A, Operating Life, Post 1600 hours at T_J = 282°C.
Output voltage versus output current for three electrically good (pin 3, 6 and 11) and one (pin 8) failing output.

2. Input Leakage

Failing devices were verified by the use of a Tektronix 576 curve tracer while V_{CC} was biased with +5.5V. The curve tracer display of Figure 16 shows the input characteristics of a failing (pin 1) and good input (pin 2).

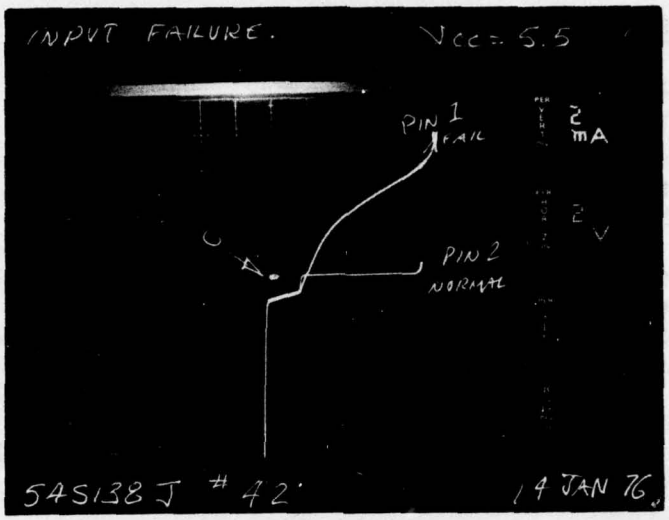


FIGURE 16: Vendor A 54S138 #42, dc 7444, Operating Life Post 2400 hours at T_J = 209°C.
Input characteristics of a good input (pin 2) and a failing input (pin 1).

Further failure analysis involved curve tracer displays of unbiased devices from V_{CC} to input pin 1. Two distinct different forward voltage characteristics were observed. The photograph in Figure 17a displays these characteristics. One shows the normal base-emitter forward voltage drop of the input transistor with a threshold of approximately .6V while the other two rejected devices (both at pin 1) show a threshold voltage of about .3V. This suggested that a resistive path between collector and emitter of the input transistor existed. This is shown in Figure 17b.

To demonstrate the existence of a collector to emitter resistive shunt at the input transistor, device #74 was opened and microprobed between points A and B of Figure 19b. The curve tracer display of the I/V characteristic between these two points is shown in Figure 18.

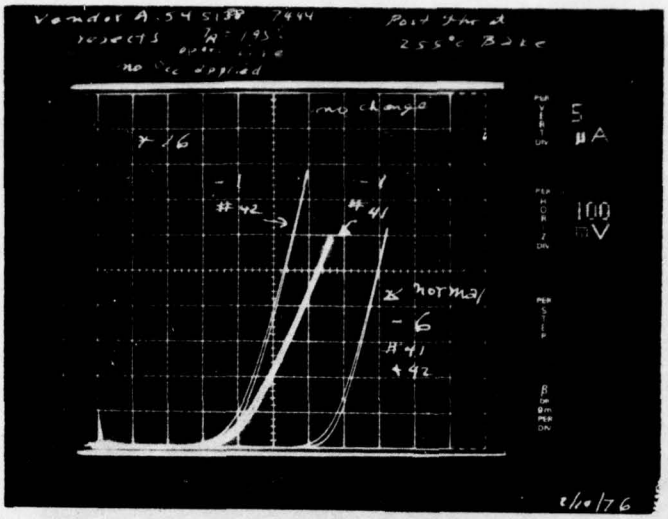


FIGURE 17a

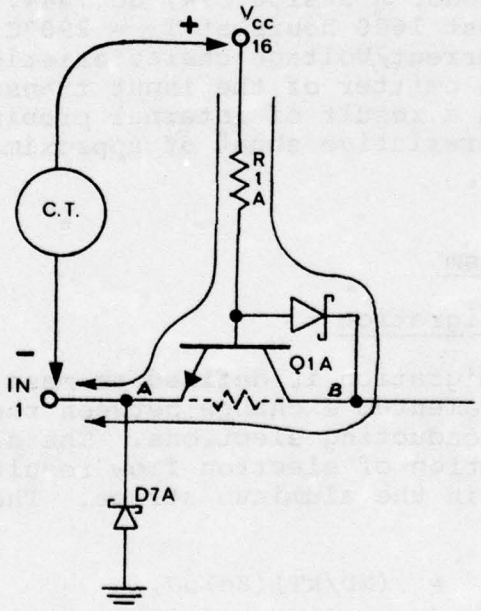


FIGURE 17b

FIGURE 17: Vendor A 54S138 #41, 42, dc 7444, Operating Life Post 2400 hours at T_J = 209°C.
V_{CC} (pin 16) to input (pin 1 and 6) characteristics.
Trace of pin 6 shows V_{BE} of the input transistor.
Trace of pin 1 shows V_F of Schottky diode.

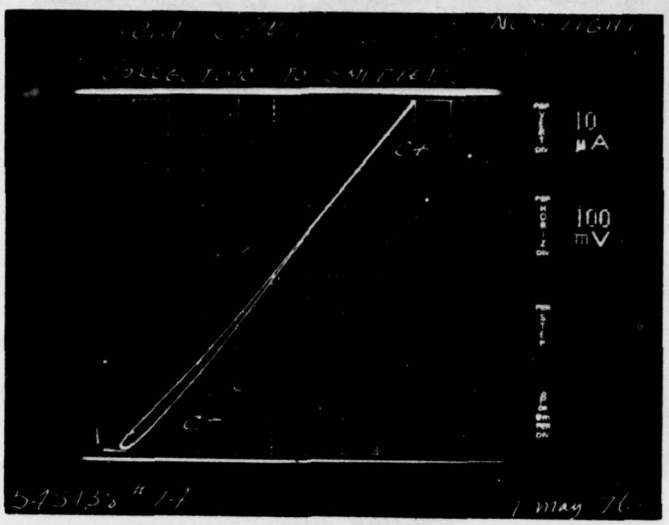


FIGURE 18: Vendor A 54S138 #74, dc 7444, Operating Life Post 1600 hours at T_J = 290°C. Current/Voltage characteristics from collector to emitter of the input transistor of Q_{1A} as a result of internal probing. Photo shows a resistive shunt of approximately 8KΩ.

B. Failure Mechanism

1. Electromigration

Electromigration is defined as mass transport of aluminum metal by momentum exchange between thermally activated aluminum ions and conducting electrons. The aluminum ions travel in the direction of electron flow resulting in hillock and void formation in the aluminum stripe. The net ionic flux, J, is given by

$$J = (ND/kT)(Ze)\rho J,$$

after Huntington and Grone[1], where

N = density of ions

$D = D_o \exp(-Q/kT)$, the diffusion coefficient, where Q = the activation energy for diffusion

k = Boltzmann's constant

T = absolute temperature

Ze = the effective electric charge of the migrating ion, and

ρ = the resistivity of the conductor

J = current density

This expression is applicable to bulk single crystals for which Q and D are well defined. However, Q and D are not as well defined for polycrystalline films.

Model calculations carried out by Black[2] and others[3] have determined mean time to failure (MTF) versus current density J and absolute temperature T to be expressible as:

$$MTF = Aj^{-n} \exp(Q/kT),$$

where: A = a constant dependent upon geometry and structure

$1.0 < n < 3.0$

Q = the appropriate activation energy

Factors influencing MTF other than J and T include current density gradient, temperature gradient, grain size microstructure, geometry, and the presence and nature of a glass coating over the chip surface.

The effects of electromigration observed on devices having been rejected for V_{OL} were confined to the emitter metallization of the output transistor. The bottom output transistor was externally loaded with 22mA. These transistors are NPN so that the direction of the electron flow is from ground to emitter. It was anticipated that aluminum accumulation would occur along the emitter conductor and possibly aluminum depletion in the collector metallization. However, most of the voiding occurred along the emitter metallization at some distance from the observed hillock.

Electrical malfunction was recorded only for pin 8. However, the emitter metallization of the output transistor associated with pin 11 also exhibited visual effects of electromigration. This transistor was in the low state during operational life test, but, although not externally loaded, its emitter current was equal to its total base current.

This assumption should be valid since the Vendor A's 54S00 did not show any increase of I_{CC} at +250°C ambient (T_J = 257°C) over the measured current at +25°C. The photograph shown in the report highlights the effects of electromigration which occurred in the emitter metallization of an externally unloaded output pin 11 from an +250°C ambient environment.

Photos in Figures 19 and 20 indicate the general location of void and hillock formation in the emitter metallization of pin 8 and a close up of a typical hillock.

In Figures 21 and 22 the location of hillocks are shown and a close up of a hillock associated with pin 11.

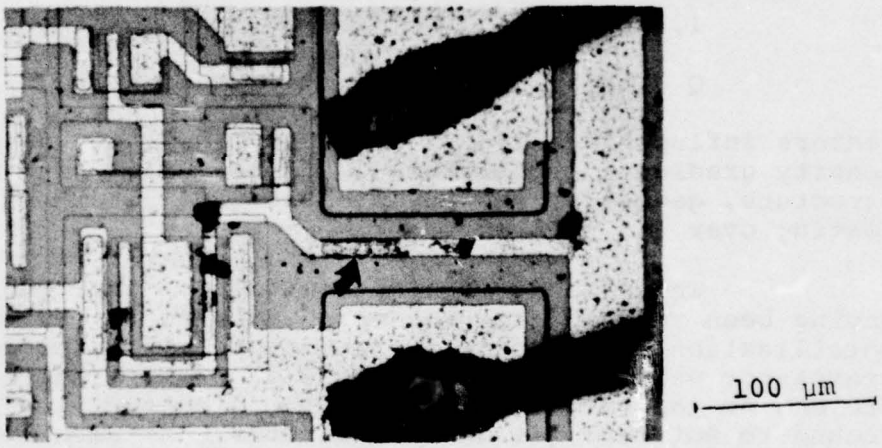


FIGURE 19: Vendor A 54S00 #53, dc 7330A, Operating Life Post 1600 hours at T_J = 257°C.

Optical overall view of pin 8 transistor emitter metallization which exhibits several hillocks and a large void (arrow).

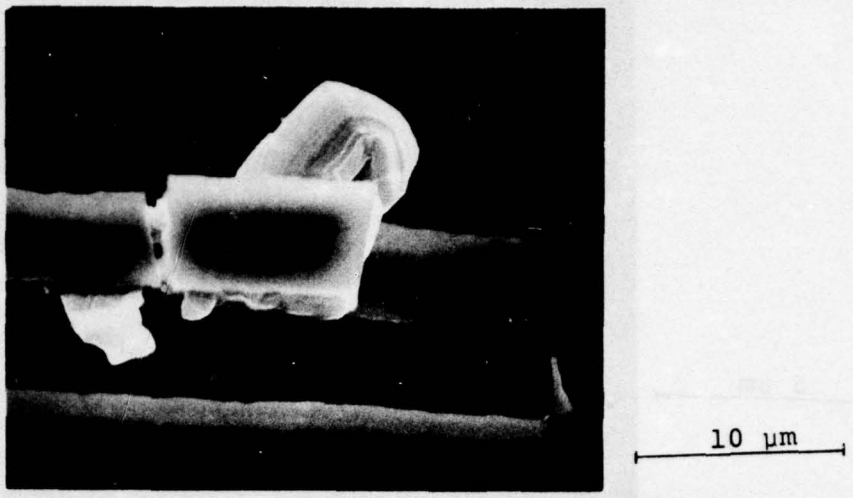


FIGURE 20: Vendor A 54S00 #53, dc 7330A, Operating Life Post 1600 hours at T_J = 257°C.
SEM close up of one of the hillocks. The aluminum is "growing" out from under the cracked glassivation.

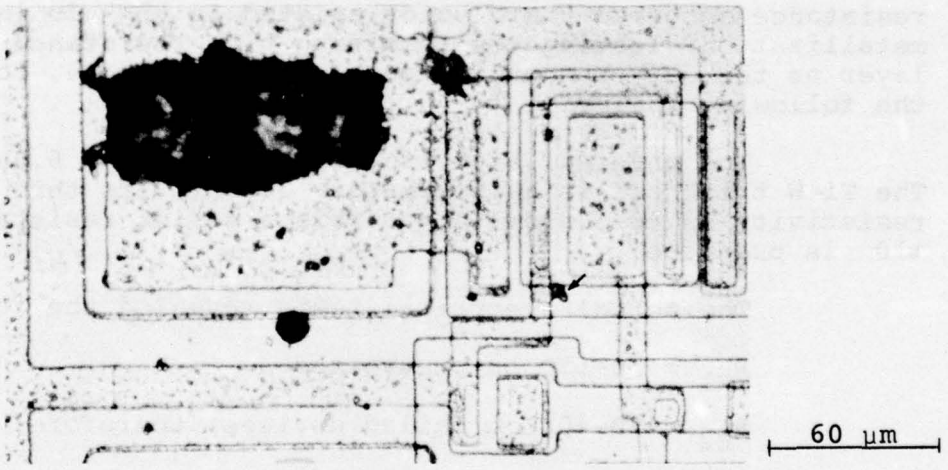


FIGURE 21: Vendor A 54S00 #53, dc 7330A, Operating Life Post 1600 hours at T_J = 257°C.
Optical view of pin 11 transistor emitter metallization showing just one large hillock and no void formation.

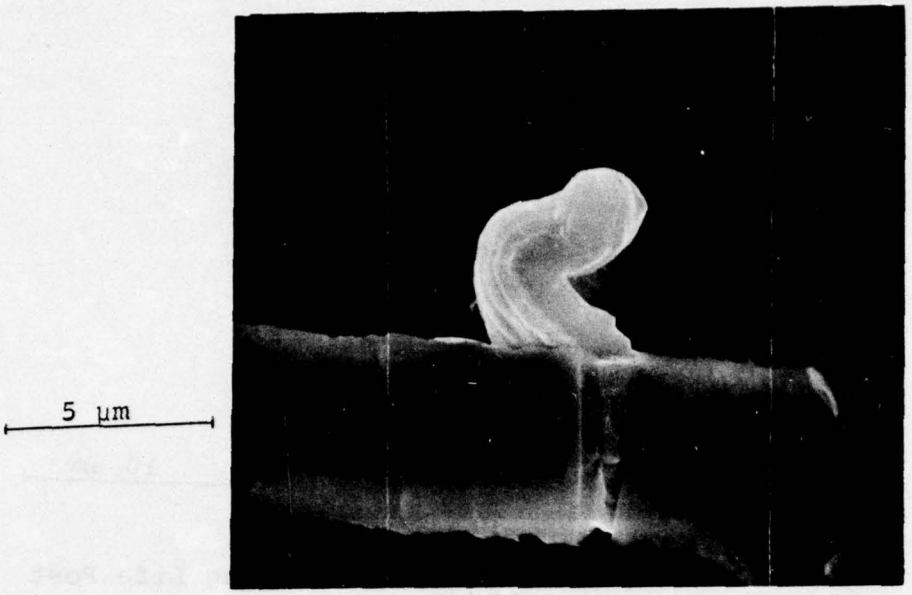


FIGURE 22: Vendor A 54S00 #53, dc 7330A, Operating Life Post 1600 hours at T_J = 257°C.
SEM close up view of electromigration induced hillock in pin 11.

It should be noted that an increase in emitter resistance occurred where voids existed in the aluminum metallization, leaving the remaining high resistance Ti-W layer as the only conductive path. As an example, consider the following analysis.

The physical size of a typical void is 6.0µm x 36.0µm. The Ti-W thickness is approximately 3000Å. Its thin film resistivity is 40-50µΩcm. From this a series resistance of ∿10Ω is predicted.

The actual electrical tests revealed the following:

R_{E1} = 10-15Ω on unstressed

R_{E2} = 20-40Ω on failed devices, therefore;

$\Delta R_E = R_{E2} - R_{E1}$ = 10Ω - 25Ω.

It is seen that the increase, ΔR_E is of the order of that predicted by the proposed mechanism.

Substantial hillock formation, glass upheaval, and aluminum accumulation as illustrated in Figures 23, 24, 25 and 26 was indeed observed in the emitter together with voids. Typically, the amount of aluminum accumulation far exceeded the amount of material available from the voids formed. It is assumed, then, that the large aluminum build up was possible because of the proximity of the relatively vast supply of aluminum in the ground metallization.

The reason why a hillock formation occurs at a particular site is not known but believed to be related to surface irregularity, inhomogeneity in the metallization, geometrical consideration, etc. Hillock formation continues with the aluminum being supplied by the ground metallization until the supply of aluminum from the ground metallization is essentially cut off. This occurs when a hillock bridges the conductor, such as is shown in Figure 19. Hillock growth continues, but now at the expense of the aluminum leeward of the blocking hillock(s) with eventual void formation and electrical malfunction.

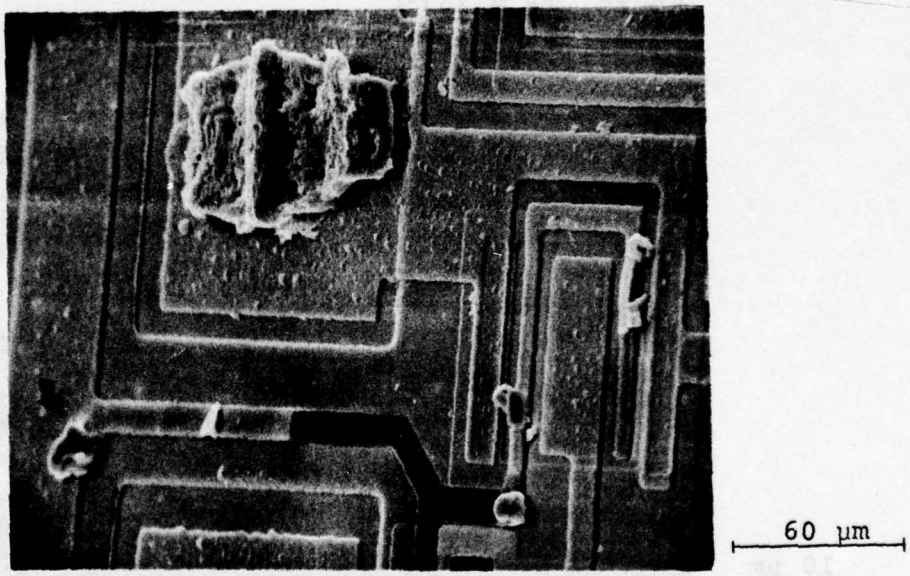


FIGURE 23: Vendor A 54S00 S/N #53, Operating Life Post 1600 Hours, T_J = 257°C.
An overall view of the pin 8 metallization. The large aluminum accumulation at the arrow actually caused the failure by cutting off aluminum supply. Evidence of void formation is a darkening of the glass over the void.

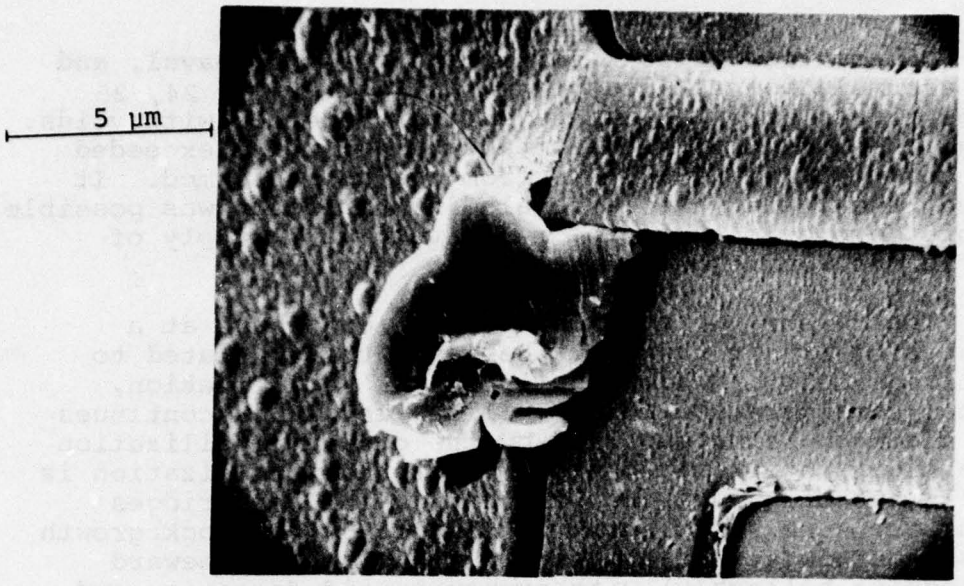


FIGURE 24: Vendor A 54S00 S/N #53, Operating Life Post 1600 Hours, T_J = 257°C.
Close-up view of aluminum accumulation near ground metallization stripe.

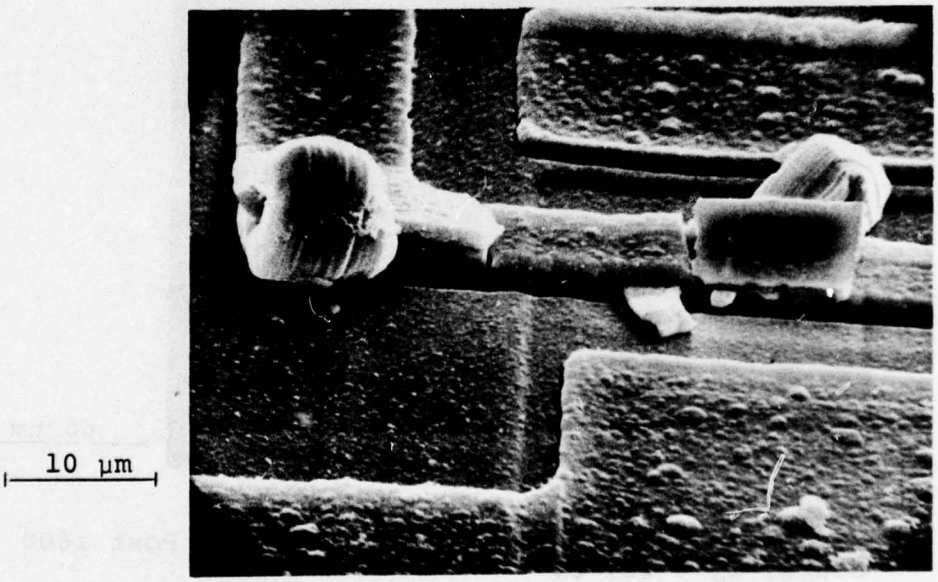


FIGURE 25: Vendor A 54S00 S/N #53, Operating Life Post 1600 Hours, T_J = 257°C.
SEM close-up of a double hillock formation.

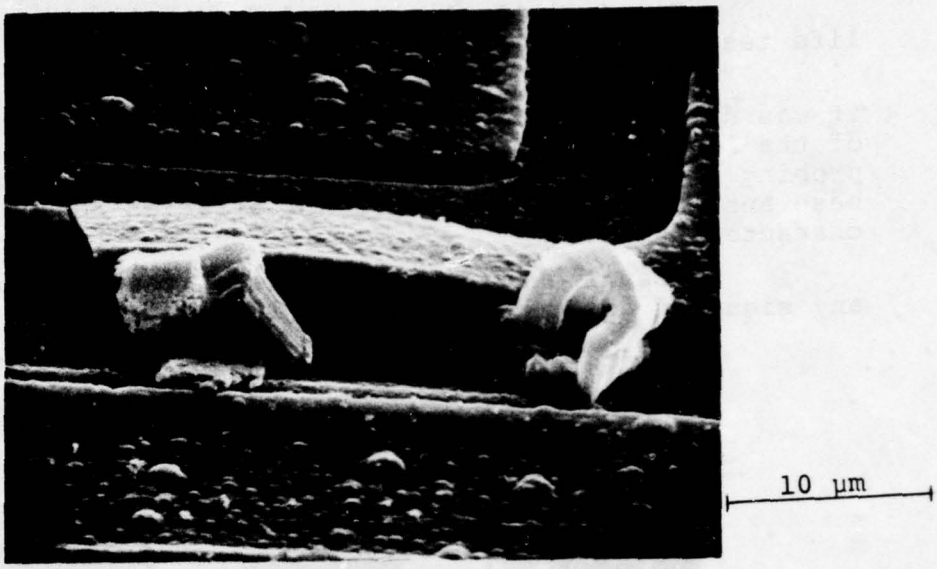


FIGURE 26: Vendor A 54S00 S/N #53, Operating Life Post 1600 Hours, T_J = 257°C.
SEM close-up of other double hillock formation.

2. Electrostatic Discharge Damage

The failure mechanism associated with the failure mode which manifested itself as an emitter-collector shunt and resulted in excessive input leakage current was unique to Vendor A's 54S138.

No detail explanations are given to describe the mechanism, since it is not fully understood. Observations made will, however, lead to the conclusion that the failure was induced by excessive current as a result of electrostatic discharge.

Device failures displaying this type of damage were first observed after a minimum of 500 hours of life testing. With increasing life test time, more failures involving this mode and mechanism occurred on devices subjected to both HTRB and storage at all environmental temperatures.

The failure mode as previously described in paragraph VII.A.2 was only found to have occurred at pin 1. Pin 1 being a corner pin of the package and as such is more susceptible to initial contact during handling than the remaining pins. None of the other three corner pins are signal inputs for the 54S138.

Pin 6 similarly powered during long term operational life test did not display this failure mode.

During the electrical portion of the failure analysis it was determined that a shunt path from emitter to collector of the input transistor associated with pin 1 existed. Internal probing within the chip proved that both junctions, emitter-base and collector-base, were not affected and display normal characteristics.

Visual examination of the chip surface did not reveal any signs of damage as indicated in Figure 27.

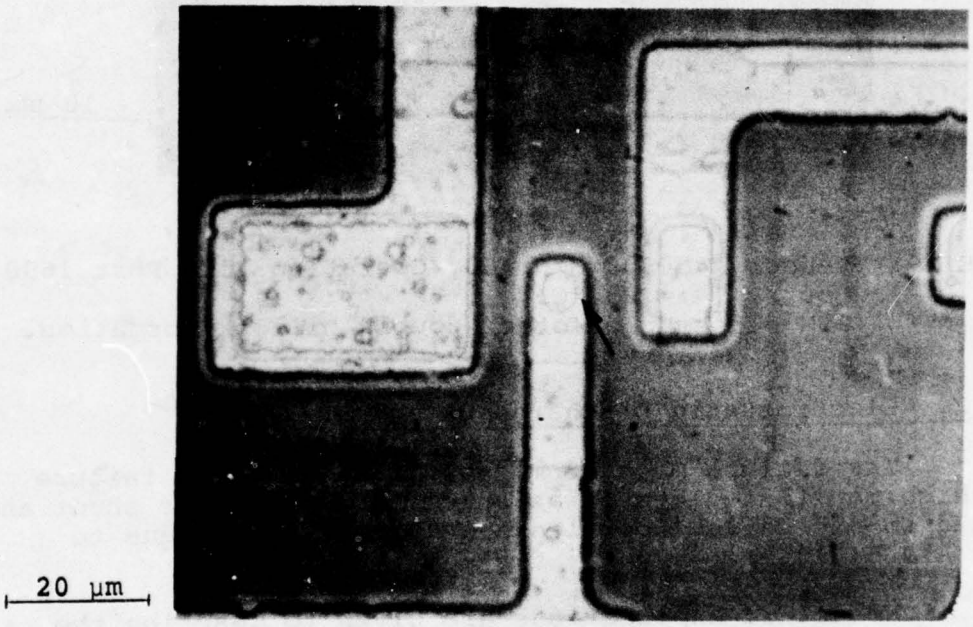


FIGURE 27: Vendor A 54S138 S/N 23, dc 7444, Storage Life Test Post 2700 hours at T_A = 250°C.
Q_{1A} does not reveal any visual evidence of defect. Surface glassivation has not been removed. Arrow points to visual area of defect.

In order to show the area of damage it was necessary to remove both surface glassivation and metallization. Figure 28 shows the area where the damage occurred. A SEM close-up of the damaged region is shown in Figure 29.

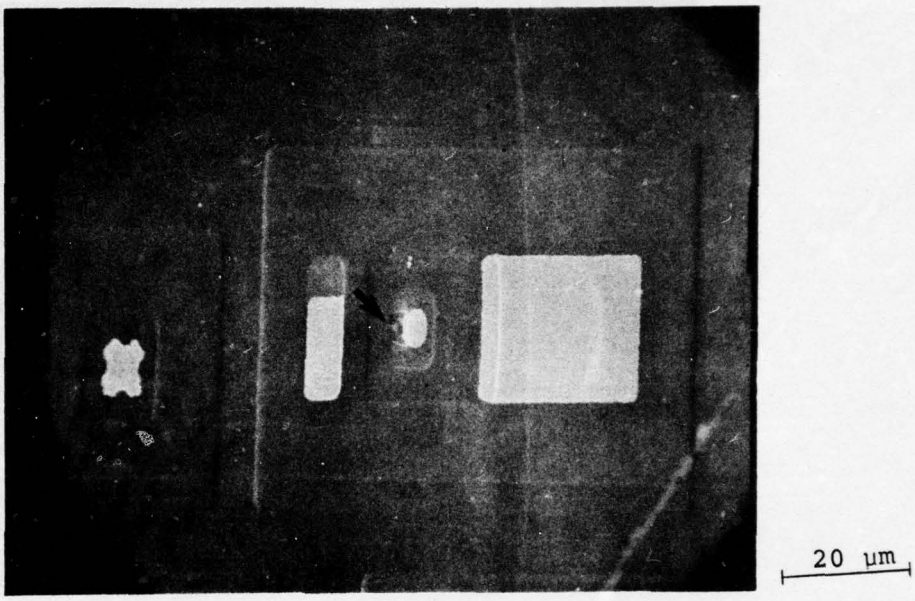


FIGURE 28: Vendor A 54S138, S/N 30, dc 7444, Operating Life Post 2400 hours at T_J = 209°C

Q_{1A} emitter contact, arrow showing area of damage. Glassivation and metallization removed.

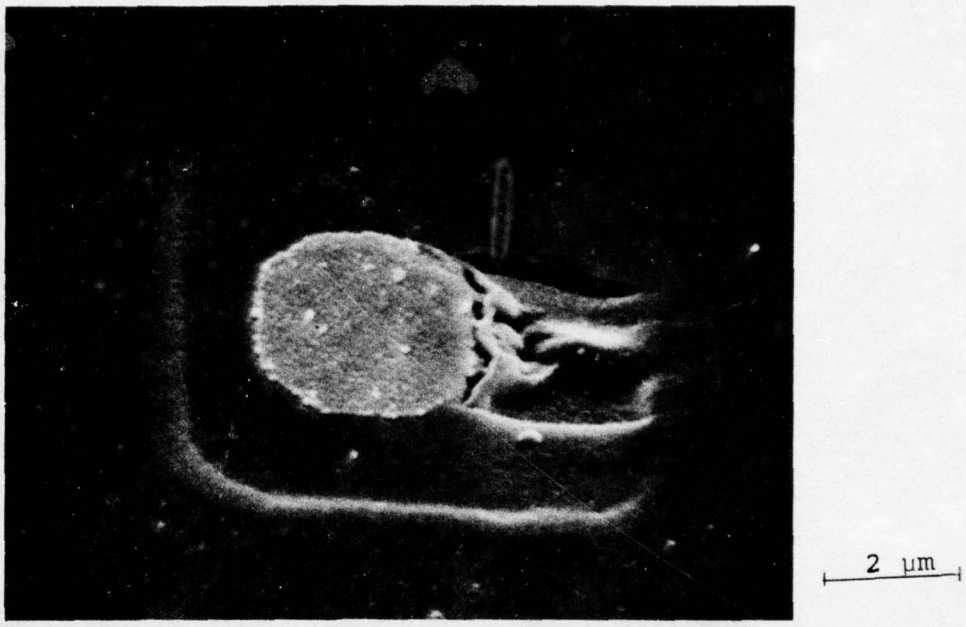


FIGURE 29: Vendor A 54S138 S/N 30, dc 7444, Operating Life Post 2400 hours at T_J = 209°C.
SEM close-up view of Q_{1A} emitter area of damage.

For further analysis cross sections were performed on several devices. The results are shown in Figures 30 and 31 and indicate a channel from the N+ emitter diffusion to the N- collector.

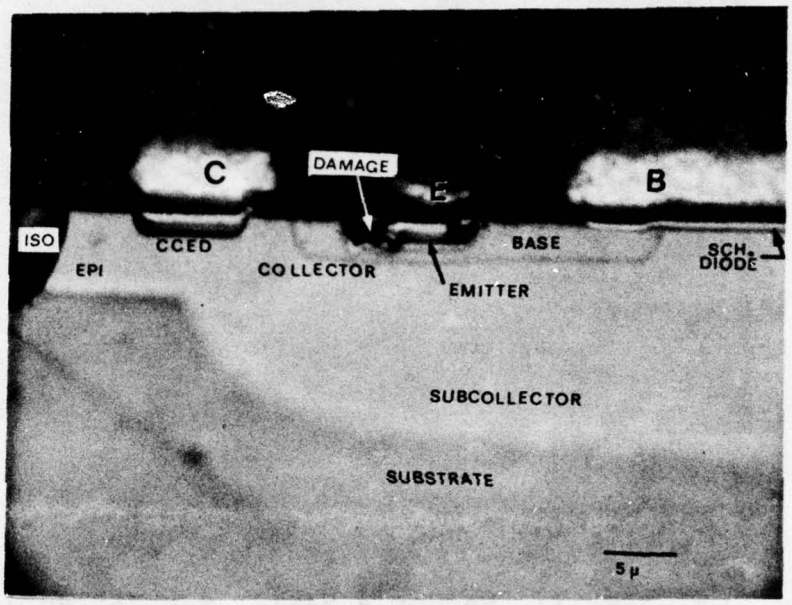


FIGURE 30: Vendor A 54S138 S/N 76, dc 7444, Operating Life Post 500 hours at T_J = 290°C.

Angle cross section through Q_{1A} emitter diffusion. First picture.

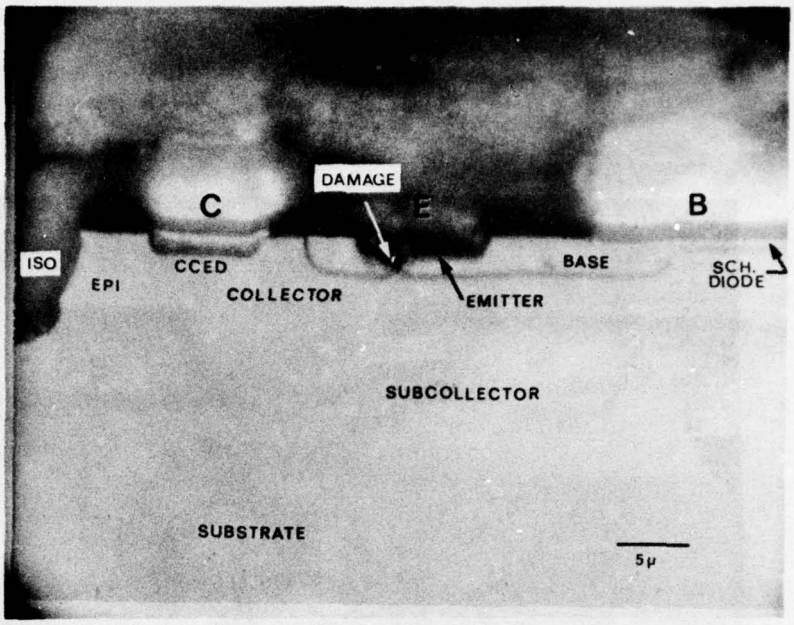


FIGURE 31: Vendor A 54S138 S/N 76, dc 7444, Operating Life Post 500 hours at T_J = 290°C.

Second picture.

All reject devices of Vendor A's 54S138 were identified with the location of damage as shown in Figure 32.

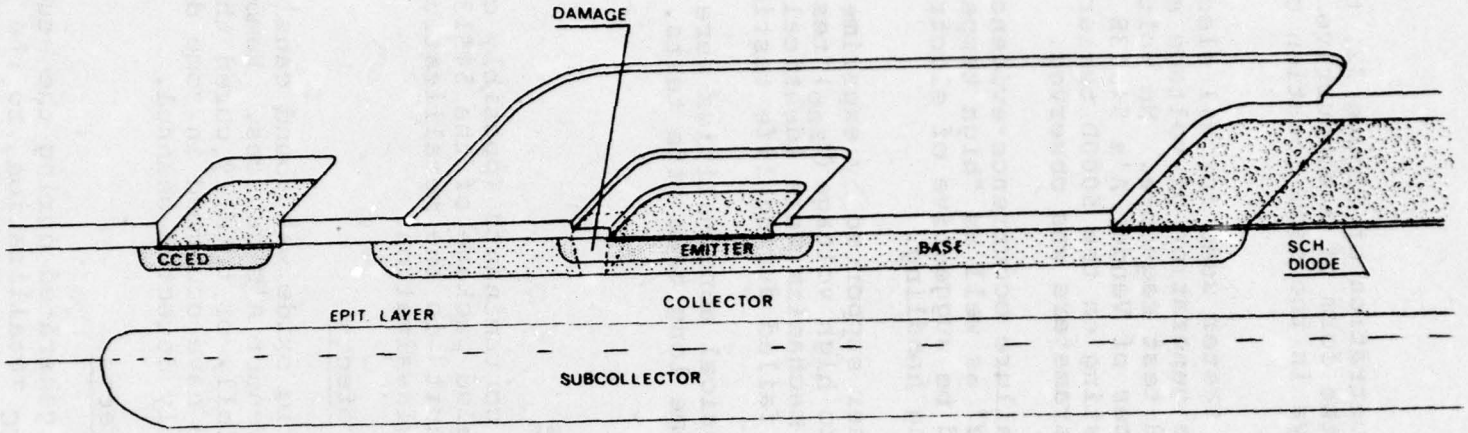


FIGURE 32: Illustration of Q_{1A} showing exact location of damage.

As shown in the illustration of Figure 32, the observed region of damage in the form of a conductive path from emitter to collector was always in the same location on every failed device.

The Fairchild 5000D tester used for all electrical tests was checked for possible generation of voltage spikes specifically during the 54S138 test sequence. No voltage spikes were found. Good devices of Vendor A's 54S138 also were subjected to repeated testing on the 5000D tester. No deterioration of any device parameters was observed.

The randomness of failure occurrence evidenced in both "high temperature storage" as well as "high temperature reverse bias" conditions would be suggestive of electrostatic discharge damage induced during handling.

This belief is further supported by experimental results of devices subjected to high voltage (V_{Zap}) tests of the inputs whose failure mode and mechanism were identical to that observed on the devices which failed during life testing.

No electrical or physical abnormalities were observed on devices which passed the same long term life tests.

3. Miscellaneous

a. Corrosion Defects

Remaining corrosive contaminants (possibly chlorinated solvent) in a hermetically sealed package of the 54S138 of Vendor A caused an opened circuit in the metallization at a bonding pad not covered with glassivation.

b. Surface Related Defects

Contaminated pyrolytic oxide was found causing pin to substrate leakage on some of Vendor A's devices. Removing of the surface glassivation partially or totally cured the shunt. Also channelling was found to have occurred in some devices. Baking did remove the previously detected channel.

c. Oxide Related Defects

These failures were generated during the study displaying shunt path from the V_{CC} metallization to the silicon substrate. These are believed to be caused by metal penetration through either random pin holes or other oxide defects.

C. Failure Analysis Results

1. Vendor A 54S00

The major failure mechanisms unique to this specific device was found to be void and hillock formation as a result of electromigration in the emitter metallization of the output transistor.

This failure mechanism was anticipated since already during construction analysis nominal current densities in the emitter metallization of 2.5 X 10^5A/cm^2 were calculated. This exceeds the MIL-M-38510 specified maximum limit of 2 X 10^5A/cm^2.

Electromigration related failure which resulted during operational life test at all three temperatures as illustrated in Figures 33 and 34 for the low temperature environment, 35 and 36 for median temperature environment and 37 and 38 for high temperature environment.

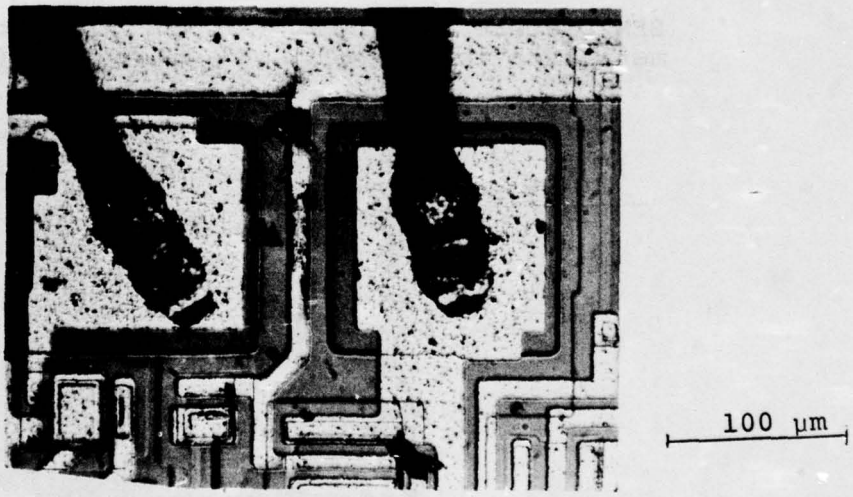


FIGURE 33: Vendor A 54S00, S/N 28, dc 7330A, Operating Life; Failed Post 1620 hours at T_J = 227°C

Pin 8 emitter metallization shown. The arrow indicating the void and two large hillocks can be seen.

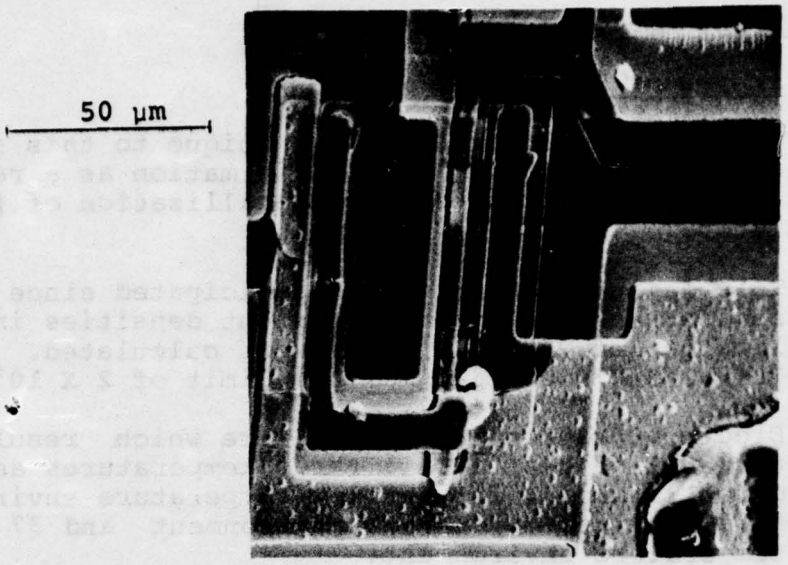


FIGURE 34: Vendor A 54S00, S/N 28, dc 7330A, Operating Life Failed Post 1620 hours at T_J = 227°C

SEM picture showing one of the hillocks at pin 8 metallization.

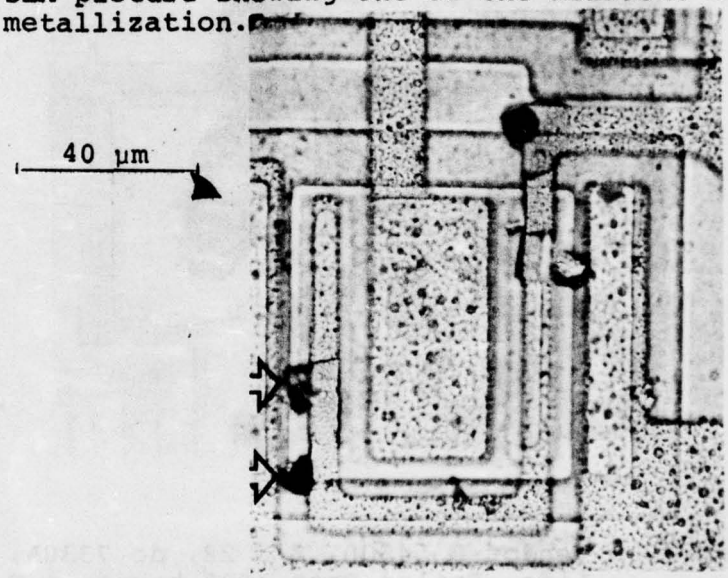


FIGURE 35: Vendor A 54S00, S/N 53, dc 7330A, Operating Life Failure Post 1600 hours at T_J = 257°C

Pin 8 metallization showing four large hillocks.

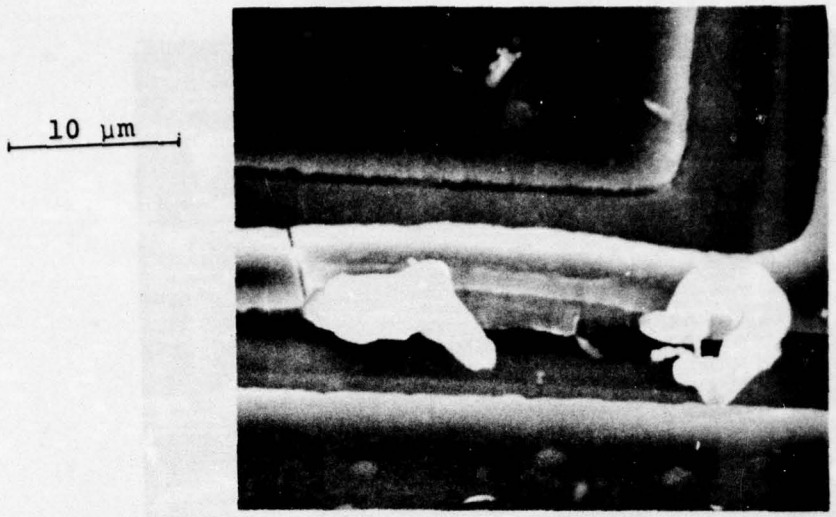


FIGURE 36: Vendor A 54S00 S/N 53, dc 7330A, Operating Life Failure Post 1600 hours at T_J = 257°C

SEM close-up showing two hillocks, location indicated by arrow in Figure 35.

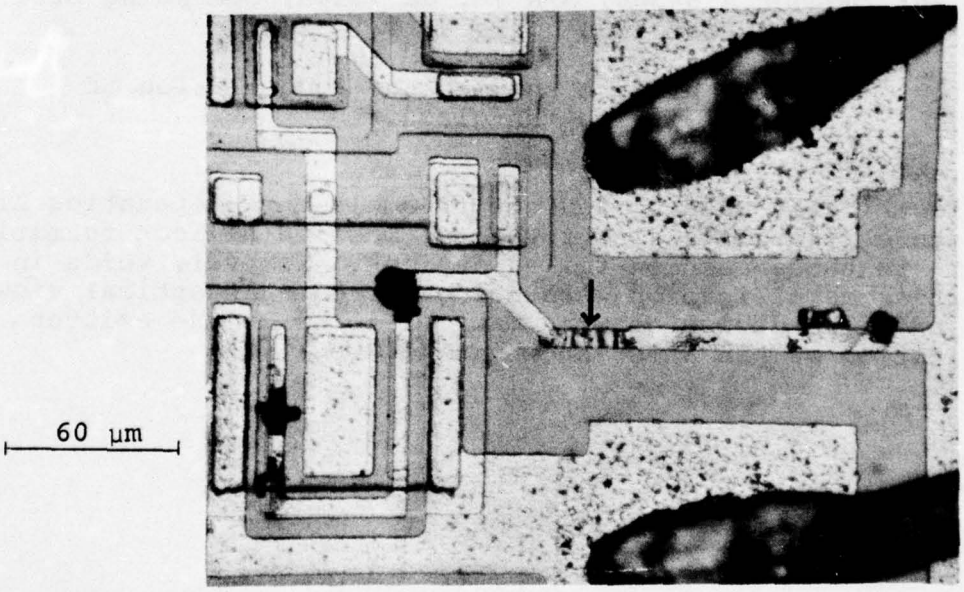


FIGURE 37: Vendor A 54S00 S/N 69, dc 7330A, Operating Life Failed Post 1000 hours at T_J = 282°C
Pin 8 metallization showing one large void (indicated by arrow) and many hillocks.

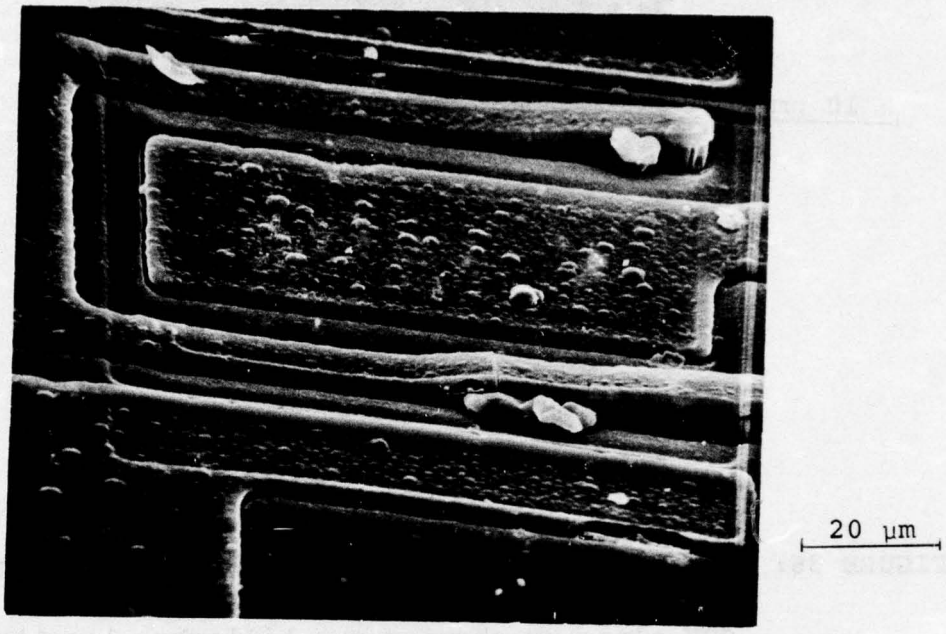


FIGURE 38: Vendor A 54S00, S/N 70, dc 7330A, Operating Life Failed Post 1600 hours at T_J = 282°C

The SEM picture showing the accumulation of aluminum lifting the glass.

Electrically passing devices from all three operating high temperature life tests also revealed massive hillock formations similar to those seen on failed devices. However, voids in the emitter metallization were not observed. An optical view of an unfailed device showing many hillocks in the emitter metallization of pin 8 is shown in Figure 39.

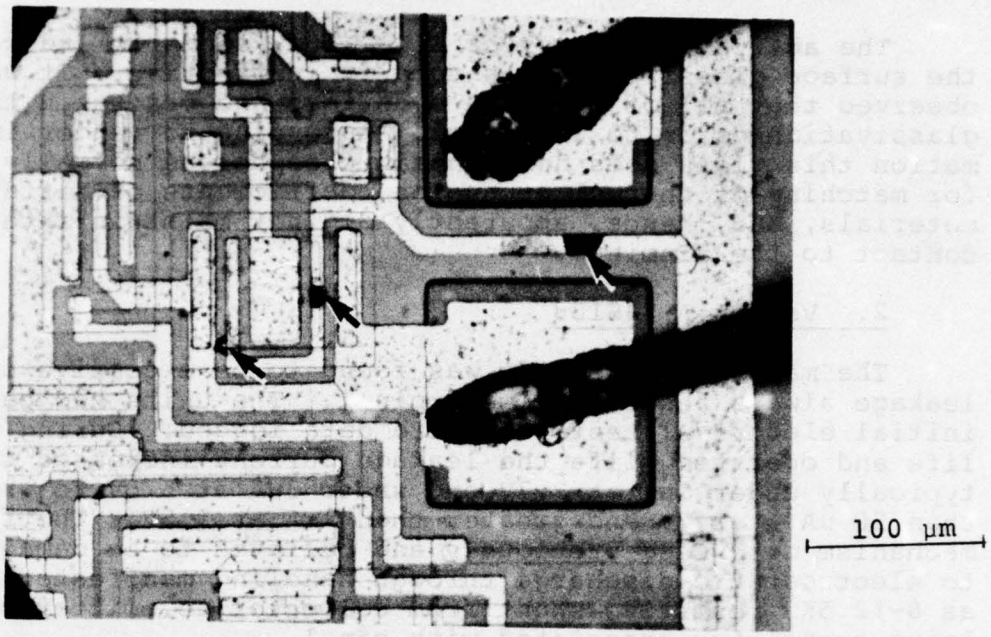


FIGURE 39: Vendor A 54S00 S/N 60, dc 7330A, Operating Life Passing Post 2400 hours at T_J = 282°C

Unfailed unit showing hillocks but no voids.

Evidence of mass transport of aluminum in form of the hillock formations was also seen in the emitter metallization associated with pin 11. During the performance of high temperature operating life test the output of pin 11 was also biased into a low state. No external load was applied, only the internal maximum base drive of about 5mA was flowing through the output transistor for devices subjected to ambient temperatures of +250°C or below. This current would result in a current density in the emitter metallization of about .7 x 10^5 A/cm^2 and yet with this density effects of electrimigration were observed. Previous results from limit testing and also special bench testing for Vendor A's 54S00 indicated that at +250°C ambient temperature no increase in total I_{CC} was found (note: Vendor B's 9S00 devices exhibited typical increases in total I_{CC} of 10mA at +250°C and 16mA at +275°C above their room temperature currents, yet no effect of electromigration was evident).

The activation energy calculated from the life test data shows E_a = .56eV. J. R. Black[4] quotes values for unglassivated aluminum from .48eV for small grain to .84eV for large grained aluminum. For large grain passivated aluminum E_a is quoted to be 1.2eV.

The activation energy of E_a = .56eV seems to indicate that the surface glassivation was totally ineffective. It was observed that all of Vendor A's devices had cracks in the glassivation prior to life test. According to vendor information this glass does not contain phosphorous normally used for matching of thermal expansion coefficients of different materials, and, hence, apparently did not maintain integral contact to the aluminum.

2. Vendor A 54S138

The major failure mode was found to be excessive input leakage always associated with pin 1. The units had passed the initial electrical tests and were data logged. During storage life and operating life the leakage current increased from typically under 1μA at 2.7V and under 3μA at 5.5V to greater than 50 μA at 2.7V and greater than 1mA at 5.5V. The failure mechanism discussed previously and believed to be damage due to electrostatic discharge through handling manifested itself as 8-12.5KΩ resistive shunt from collector to emitter of the input transistor associated with pin 1.

It should be noted that during all initial electrical testing no damage occurred. Limit testing performed for both storage and operational conditions did not reveal this type of failure. The first device failure of this type was logged at 500 hours at T_J = 290°C during the performance of long term operational life test. As a result of the failure mechanism discussed, special handling procedures should be initiated.

Although not contributing to failure, evidence of electromigration was also noted in the form of hillock formation in the emitter metallization of the loaded output transistors of pin 14. This was found primarily in the ground metallization.

3. Vendor A 54LS00

During the performance of all limit and all long term life testing no failures occurred. Device samples from all environments were opened and visually examined for defects. Inspection of the metallization did not reveal any hillock formation suggestive of electromigration. The maximum calculated current density in the collector metallization of the output transistor at the pins 8 and 11 loaded during HTRB was 1.4 X 10^4A/cm^2.

The quality of the surface glassivation was examined and cracking of this glassivation was found in 5 out of 8 devices of varying severity. Similar damage was seen on devices not subjected to temperature stress.

4. Vendor A 54LS138

Five devices failed during the performance of limit and long term life testing. In every case these units failed at the first interim test step and, therefore, were considered early life failures. This failure mode was recorded as a resistance shunt path from various pins to substrate. These rejects are attributed to surface problems as a result of contamination in or under the pyrolytic oxide. Subsequent stripping of the oxide removed or lessened the leakage path.

The protective surface glassivation also revealed minor cracks in various places.

No evidence was found in either the passing or the failing devices that would be suggestive of an electromigration related problem in the metallization. The worst case calculated nominal current density found in the collector of output transistor in the life test was $2.8 \times 10^4 A/cm^2$.

5. Vendor B 9S00

No failures occurred during the performance of limit and long term testing. At the conclusion of long term testing the devices examined did not show any evidence of cracking of the surface glassivation. Specific attention was given to the examination of the aluminum metallization for evidence of electromigration, since previous calculations had yielded nominal current densities of $2.1 \times 10^5 A/cm^2$ in the emitter metallization of the output transistors during life testing. The devices examined after 2400 hours of operation at a junction temperature of $T_J = 258°C$ did not show any evidnece of electromigration.

6. Vendor B 93S138

One failure was experienced during 250°C long term storage. It manifested itself electrically as a resistive shunt from pin 8 to pin 16. The suspected cause was a pin hole in the thermal oxide under the bonding pad allowing metal penetration to the p+ isolation diffusion. The normal oxide thickness measures about 4000Å.

No cracks were observed in the surface glassivation.

The aluminum metallization was visually inspected and no evidence of electromigration was found.

7. Vendor B 9LS00

A total of two failures were recorded during the study. One device failed at 2400 hours during dynamic life test. The failure mode was found to be an increase in input leakage as a result of channelling. The other device failed during HTRB after 500 hours. Electrically it was found to have an ohmic shunt from pin 11 to ground. Further analysis indicated that this was caused by aluminum penetration through a pin hole defect in the oxide beneath a bonding pad. No cracks in the glassivation over the entire chip or electromigration related defects were found in the metallization during the inspection of the failed and passing devices.

D. Discussion

The study revealed that failures or visual damage resulting from electromigration was restricted to Vendor A's standard Schottky TTL devices only. The 54S00 was rejected for increase in V_{OL} due to void formation in the emitter metallization. The 54S138 although not rejected for mechanisms related to electromigration did show clear evidence of hillock formations.

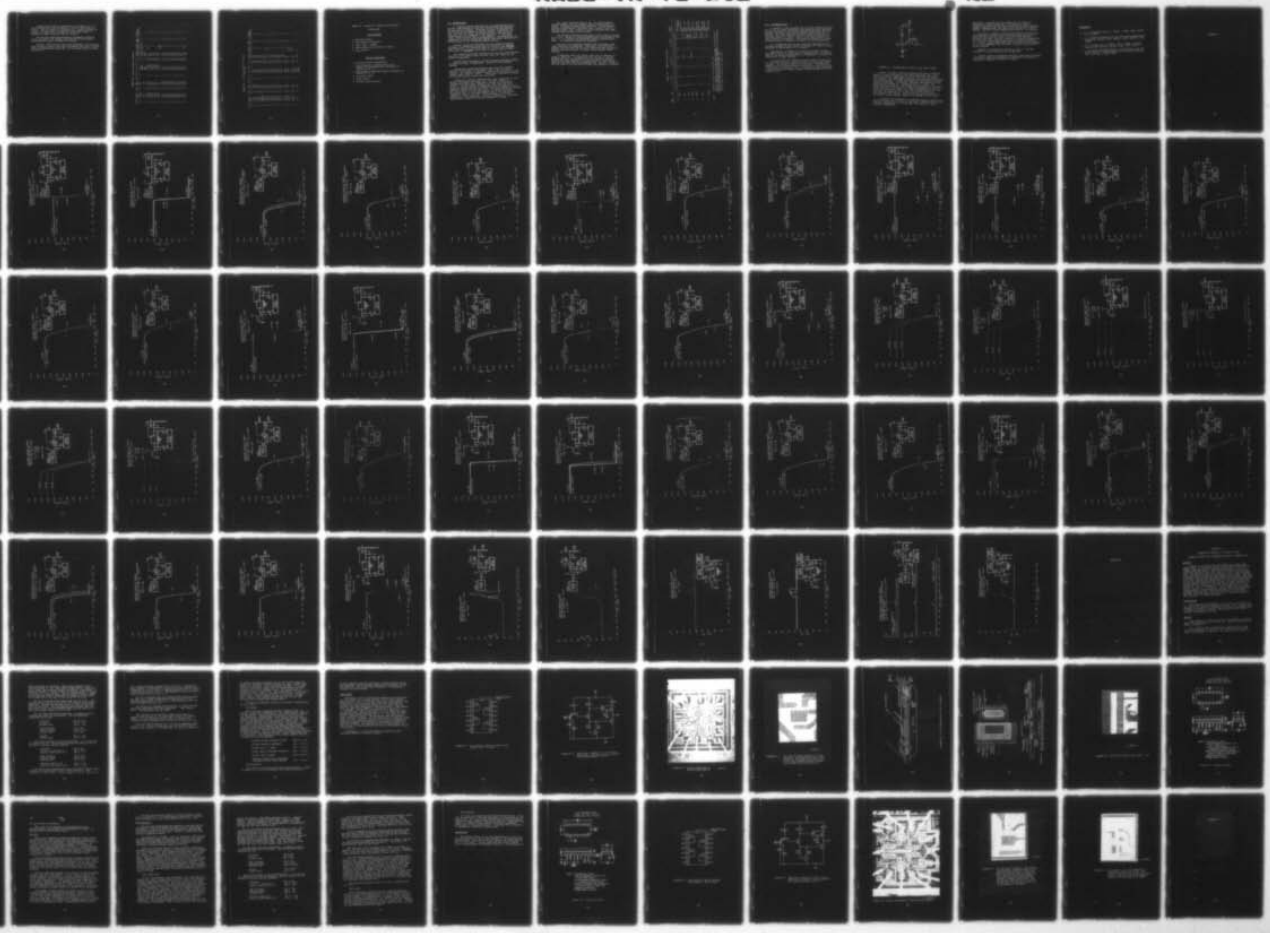
No indication of any damage due to electromigration was found in equivalent devices from Vendor B. Vendor B's 9S00 had a nominal current density of $2.1 \times 10^5 A/cm^2$ compared to Vendor A's $2.5 \times 10^5 A/cm^2$. Since no dopends are used in the aluminum which could contribute to the improved performance, it appears that the uncracked surface glassivation covering the entire metallization on Vendor B's chips did prevent the formation of hillocks and voids.

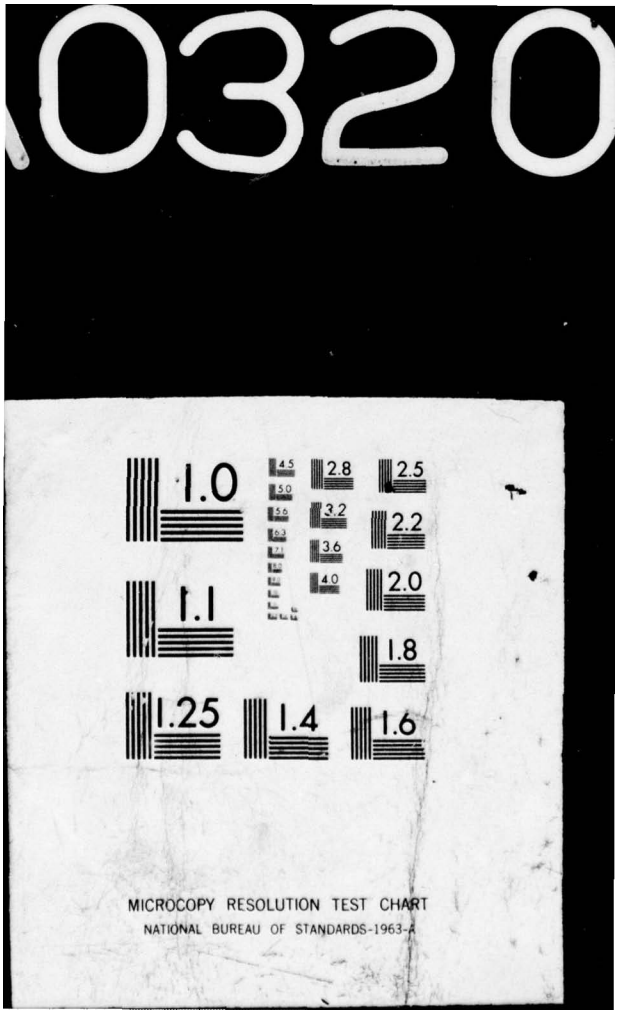
No effects of electromigration were found in any of the low power Schottky devices. It is interesting to note that the lower current densities were due to the lower total current as well as increased metallization cross-sectional areas over those in the standard devices. In all cases the nominal calculated output current densities of the low power Schottky was found to be approximately one-tenth of the current density found in the standard Schottky family.

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RELIABILITY EVALUATION OF SCHOTTKY BARRIER DIODE MICROCIRCUITS.(U)
SEP 76 E T LEWIS, D BARTELS , A A CAPOBIANCO F30602-74-C-0213
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MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

Comparing the surface glassivation of Vendor A to B it can be noted that none of Vendor B's devices exhibited any cracks. Most of Vendor A's glassivation showed evidence of cracks on temperature stressed and unstressed chips. A phosphorous doped glass is used by Vendor B.

The failure mechanism previously discussed in section VI B2 believed to be damage resulting from electrostatic discharge was unique to Vendor A's 54S138.

Devices which failed during the performance of the study were grouped by device type and environment and their failure modes and mechanisms identified. All pertinent data is shown in Table 29.

TABLE 29: LISTING OF SCHOTTKY TTL REJECTS

Vendor	Device Type	Unit No.	Date Code	Hermiticity	Life Test	T_J °C	Time of Failure	Pin No. Failed	Failure Mode	Failure Mechanism
A	54LS138	2	7351	P	Limit Storage	250	1st step 72 hrs.	all pins to 8	A	1
A	54S00	2	7330A	F	Limit Oper.	294	final step	8	B	2
A	54LS138	94	7351A	P	Storage	300	25	16/8	A	1
A	54S138	45	7444	P	Storage	300	1800	1	C	3
A	54S138	70	7444	P	Storage	300	1800	1	D	4
A	54S138	12	7444	P	Storage	250	2216	1	C	3
A	54S138	15	7444	P	Storage	250	2700	1	C	3
A	54S138	23	7444	P	Storage	250	2700	1	C	3
B	93S138	77	7503	P	Storage	250	3500	2 and 16/8	A	5
A	54S00	28	7330A	P	Oper.	227	1620	8	B	2
A	54S00	30	7330A	P	Oper.	227	2568	8	B	2
A	54S00	32	7330A	P	Oper.	227	1620	8	B	2
A	54S00	44	7330A	F	Oper.	257	1000	8	B	2
A	54S00	51	7330A	P	Oper.	257	1600	8	B	2
A	54S00	52	7330A	P	Oper.	257	1600	8	B	2
A	54S00	53	7330A	P	Oper.	257	1600	8	B	2
A	54S00	113	7448	P	Oper.	257	1600	8	B	2
A	54S00	114	7448	P	Oper.	257	500	8	B	2
A	54S00	59	7330A	P	Oper.	282	1600	8	B	2
A	54S00	62	7330A	F	Oper	282	1000	8	B	2
A	54S00	63	7330A	P	Oper.	282	1600	14/8	A	1
A	54S00	68	7330A	F	Oper.	282	1000	8	B	2

TABLE 29: LISTING OF SCHOTTKY TTL REJECTS
(Continued)

Vendor	Device Type	Unit No.	Date Code	Hermiticity	Life Test	T_J °C	Time of Failure	Pin No. Failed	Failure Mode	Failure Mechanism
A	54S00	69	7330A	P	Oper.	282	1000	8	B	2
A	54S00	70	7330A	P	Oper.	282	1600	8	B	2
A	54S00	106	7448	P	Oper.	282	1000	8	B	2
A	54S00	109	7448	P	Oper.	282	108	3	E	6
A	54S138	30	7444	P	Oper.	209	2400	1	C	3
A	54S138	41	7444	P	Oper.	209	2400	1	C	3
A	54S138	42	7444	P	Oper.	209	2400	1	C	3
A	54S138	51	7444	P	Oper.	265	50	16/8	A	5
A	54S138	54	7444	P	Oper.	265	1600	1	C	3
A	54S138	56	7444	F	Oper.	265	500	1	C	3
A	54S138	57	7444	P	Oper.	265	1600	1	C	3
A	54S138	58	7444	P	Oper.	265	1000	1	C	3
A	54S138	65	7444	P	Oper.	265	1000	1	C	3
A	54S138	74	7444	P	Oper.	290	1600	1	C	3
A	54S138	76	7444	P	Oper.	290	250 500	3 1	C C	1 3
A	54S138	82	7444	P	Oper.	290	1000	1	C	3
A	54LS138	24	7351A	P	Oper.	222	25	8	A	1
A	54LS138	60	7351	P	Oper.	277	25	4,5,6 to 8	C	6
A	54LS138	66	7351	P	Oper.	277	25	16/8	A	1
B	9LS00	56	7410	P	Oper. H.T.R.B	251	500	11	A	5
B	9LS00	34	7410	P	Oper Dynamic	251	2400	13	C	6

TABLE 29: Listing of Schottky TTL Rejects

(Continued)

Failure Modes

A Resistive shunt

B High emitter resistance

C High input leakage

D Metallization open circuit at input

E I_{CEX} failure

Failure Mechanisms

1 Pyrolytic oxide contamination

2 Void formation in metallization as a result of electromigration (discussed in section VI, B, 1)

3 Electrostatic discharge damage (discussed in section VI, B, 2)

4 Corrosion defect

5 Oxide defect

6 Surface related defects

VII. OBSERVATIONS

A trimetal system consisting of titanium-tungsten as a barrier and aluminum as the main current carrying conductor is used by both vendors. Platinum silicide is employed for ohmic contacts and Schottky barrier diodes. Results of the life test did not reveal any deterioration of the Schottky characteristic as evidenced in the stability of the input clamp diode and also the V_{OL} measurements. No penetration of aluminum or silicon through the barrier was noted indicating the effectiveness of the titanium-tungsten barrier.

Current densities calculated for the standard Schottky devices are normalized values and are close to the maximum specified limit in the MIL-M-38510 of $2 \times 10^5 A/cm^2$. However, this limit is exceeded in the case of Vendor A and B's S00.

The normalized current densities for the low power Schottky devices in the output stage are well below the limit by one order of magnitude.

Normal power consumption of the low power Schottky devices is about one-tenth of equivalent devices in the standard version.

Propagation delay measurements show that the standard Schottky is one-half the switching time of the low power version. For example, propagation delays for the S00 from both vendors range from 5-6 nsec. , while their equivalent devices in the LS00 version range from 10-12 nsec.

Vendor A's previous 54LS00 design, and classified as "old design" throughout the study, was 3-5 nsec. slower in propagation delays when compared to Vendor A's redesigned version. The new design occupies 38% less chip area as a result of closer packing of components and yet keeping active component dimensions the same size. The main difference between the two versions is that the resistor in series with the Darlington pair is now approximately 50Ω in the new design compared to 200Ω in the old. This decrease in limiting resistance, while improving the drive capability, required a specification change for I_{OS} from 6-40mA to 6-130mA.

The input circuitry used in the low power Schottky devices differs from the standard version significantly in design. The multi-emitter input structure of the standard devices is replaced by a DTL-type input circuit using a Schottky diode. This permits a direct interface with CMOS devices which operate up to 15 volts.

The surface glassivation employed by both vendors differed in quality. Vendor A's surface glassivation was cracked in the majority of stressed and unstressed devices analyzed while Vendor B's protective glass was undamaged.

The life test comparison between HTRB and dynamic mode under identical environmental conditions utilizing both Vendor A and B's LS00 did not yield sufficient data points to measure the effectiveness of static versus dynamic stress testing.

A comparison chart of failure rates for all devices is shown in Table 30. In summarizing the results, it can be pointed out that the reliability of the low power Schottky devices from both vendors is of equal quality. This is also true for the S138 from both manufacturers. However, Vendor B's S00 was found to be much more reliable than Vendor A's version.

TABLE 30: SUMMARY OF FAILURE RATES

VENDOR	TYPE	T_J = 125°C		T_A = 125°C**		T_J = 165°C		REMARKS
		at 10^4 hrs	at 10^5 hrs	at 10^4 hrs	at 10^5 hrs	at 10^4 hrs	at 10^5 hrs	
A	54S00	.11	.43	.81	.84	1.75	1.50	HTRB (Electro-migration)
		*	*	*	*	*	*	Storage $T_A=T_J$
B	9S00	*	*	*	.0004	*	.01 ***	HTRB
		*	*	*	*	*	.01 ***	Storage $T_A=T_J$
A	54S138	*	*	*	*	*	.0003	HTRB
		*	*	*	*	*	.0001	Storage $T_A=T_J$
B	93S138	*	*	*	.0043***	*	.0043***	HTRB
		*	*	*	*	*	.01	Storage $T_A=T_J$
A	54LS00	*	*	*	*	*	.0011***	HTRB
		*	*	*	*	*	.0011***	Dynamic Oper.
		*	*	*	*	*	*	Storage $T_A=T_J$
B	9LS00	*	*	*	*	*	.0011***	HTRB
		*	*	*	*	*	.0011***	Dyanmic Oper.
		*	*	*	*	*	*	Storage $T_A=T_J$
A	54LS138	*	*	*	*	*	.0019***	HTRB
		*	*	*	*	*	*	Storage $T_A=T_J$

NOTE: *Represents failure rates of less than .0001

**Junction temperature at the +125°C ambient environment was calculated for still air conditions and worst case power consumption.

***Failure rates indicated are the worst case numbers which can be guaranteed by the life test conditions of time and temperature.

Values are in percent per 1000 hours.

VIII. RECOMMENDATIONS

In general it can be stated the low power Schottky devices due to its low power consumption and therefore lower operating junction temperature for a given ambient environment are more reliable than their equivalent standard Schottky devices. In addition, the study revealed that the current density of the low power devices is about a factor of 10 lower compared to their standard counterpart. This also contributes to a higher reliability due to lessening of effects of electromigration.

It is suggested that current densities observed in all standard Schottky devices should not exceed the current density specified in MIL-M-38510 of $2 \times 10^5 A/cm^2$.

Specifically in Vendor A's 54S00 an increase in cross sectional area of the metallization combined with an improvement of the surface glassivation is recommended to better the reliability of these devices.

In using Vendor B's 93S138 attention should be given not to exceed on any input potentials above the V_{CC} power supply voltage. The reason is that all inputs use a N^+ underpass shorted to its P base diffusion and forming a junction to the N-tub which is connected to V_{CC}. Electrically this represents a diode as shown in Figure 40 whose forward direction is from input to V_{CC}.

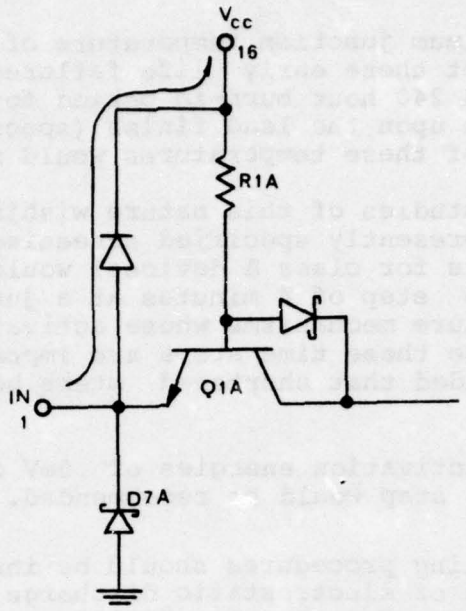


FIGURE 40: Illustration of input to V_{CC} shunt diode.

Device failures during the study which were considered early life were detected at the first electrical test at 25 hours at junction temperature of 222°C and 277°C for Vendor A's 54LS138. All these above failures were detected during long term life testing in a HTRB configuration with surface related failure mechanisms. Activation energies associated with this mechanism are quoted in literature as E_a = 1.04eV. For worst case calculations, the assumption was made that the device failed exactly at 25 hours at a junction temperature of 222°C. Using the activation energy of 1.04eV extrapolations show that the time to failure at T_A = 125°C (T_J = 127°C would be approximately 8500 hours. Device failures which occurred at T_J = 277°C would require times far in excess of 8500 hours.

In order to be detected by a possible screening method the device failures had to occur in less than 4 minutes with a 277°C junction temperature or in less than 44 minutes at a 222°C junction temperature.

Conversely, a minimum junction temperature of +225°C is necessary to detect these early life failures within a normally specified 240 hour burn-in period for class A devices. However, dependent upon the lead finish (specified in MIL-M-38510), the use of these temperatures would not be feasible.

For future studies of this nature wishing to verify the effectiveness of presently specified screening methods (T_A = 125°C for 240 hours for class A devices) would require a maximum first time step of 4 minutes at a junction temperature of 277°C for failure mechanisms whose activation energy E_a is 1.04eV. Since these time steps are impractical to achieve, it is not recommended that shortened steps be incorporated in future studies.

However, if activation energies of .5eV or less are involved, a 4 hour step would be recommended.

Special handling procedures should be instituted to prevent damage as a result of electrostatic discharge as evidenced on many device failures of Vendor A's 54S138.

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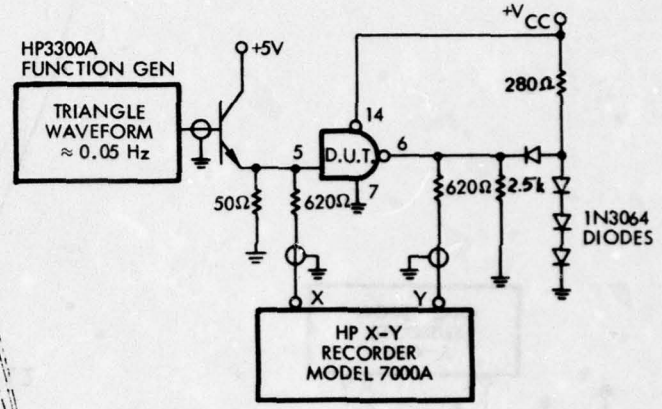
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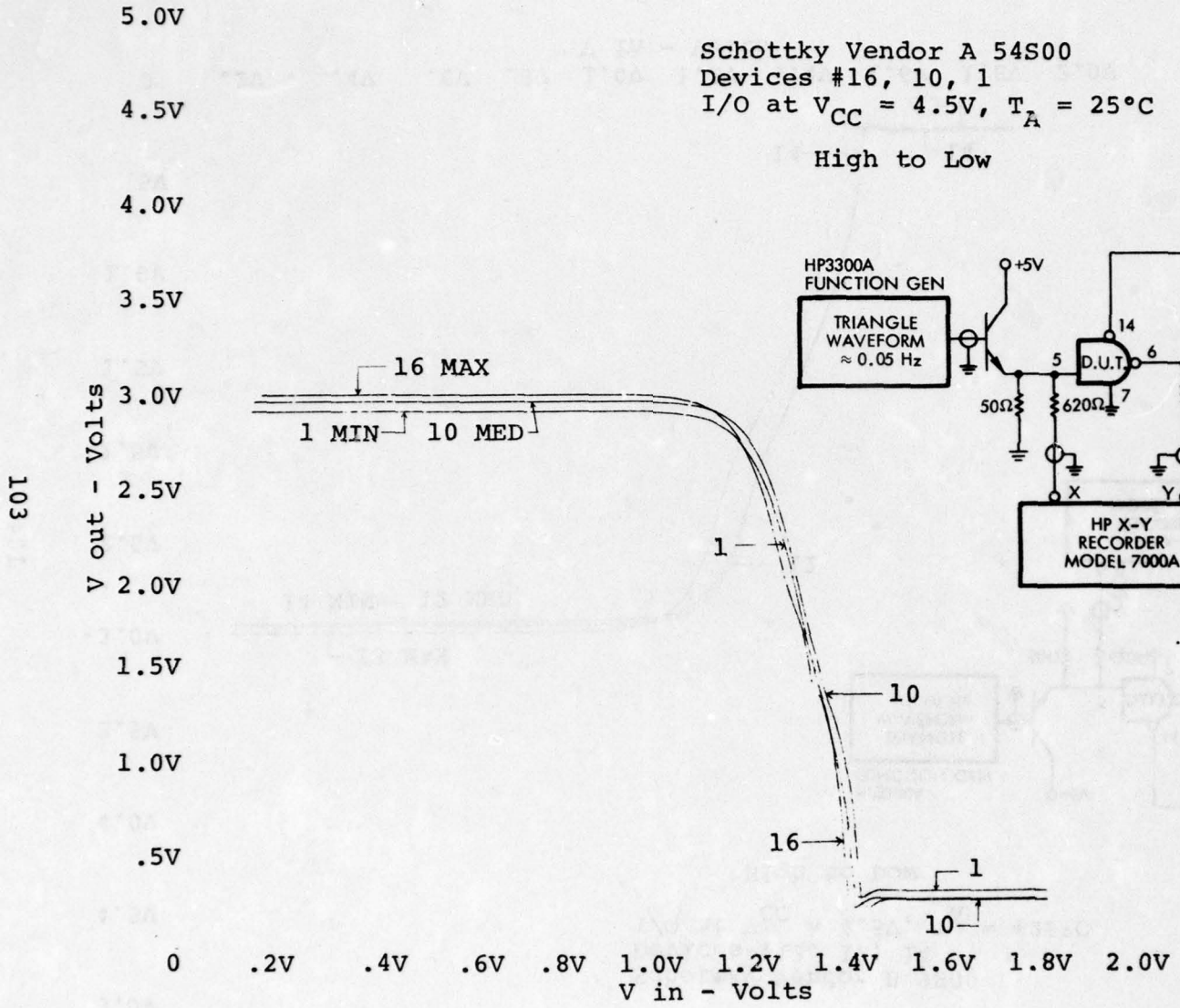
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APPENDIX A

Schottky Vendor A 54S00
Devices #16, 10, 1
I/O at V_{CC} = 4.5V, T_A = 25°C

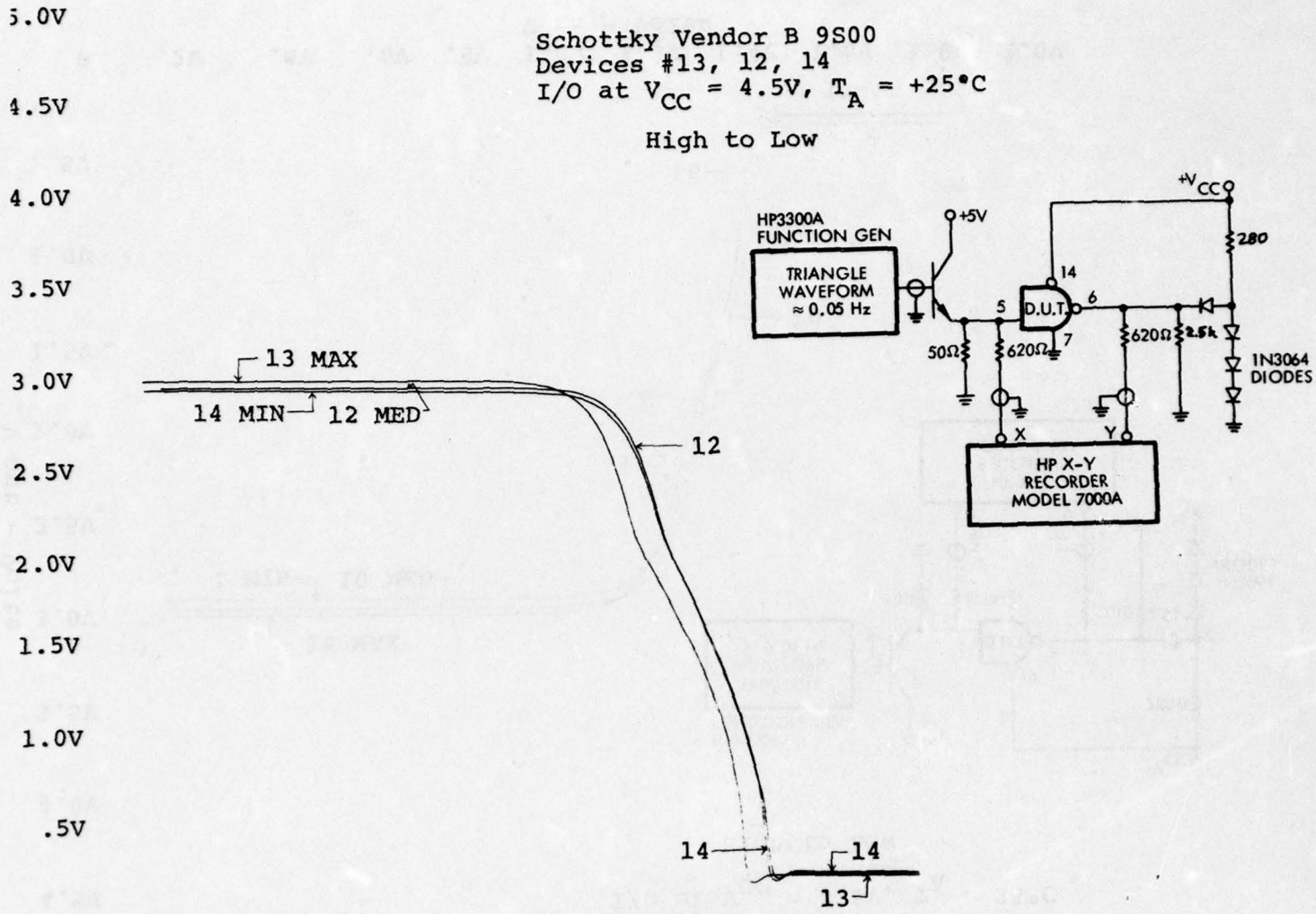
High to Low





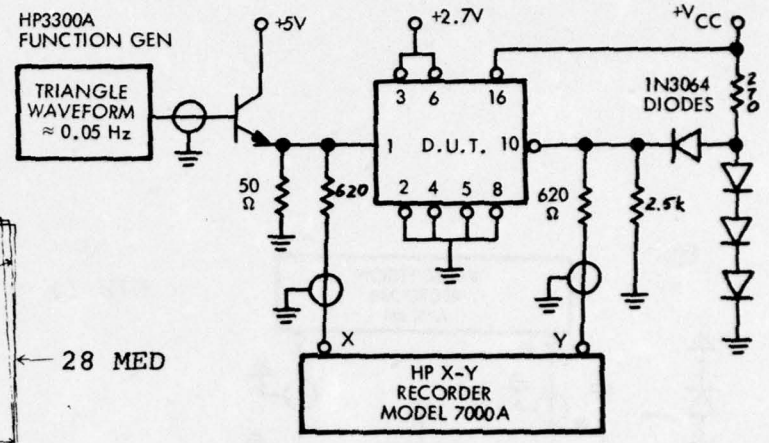
Schottky Vendor B 9S00
Devices #13, 12, 14
I/O at V_{CC} = 4.5V, T_A = +25°C

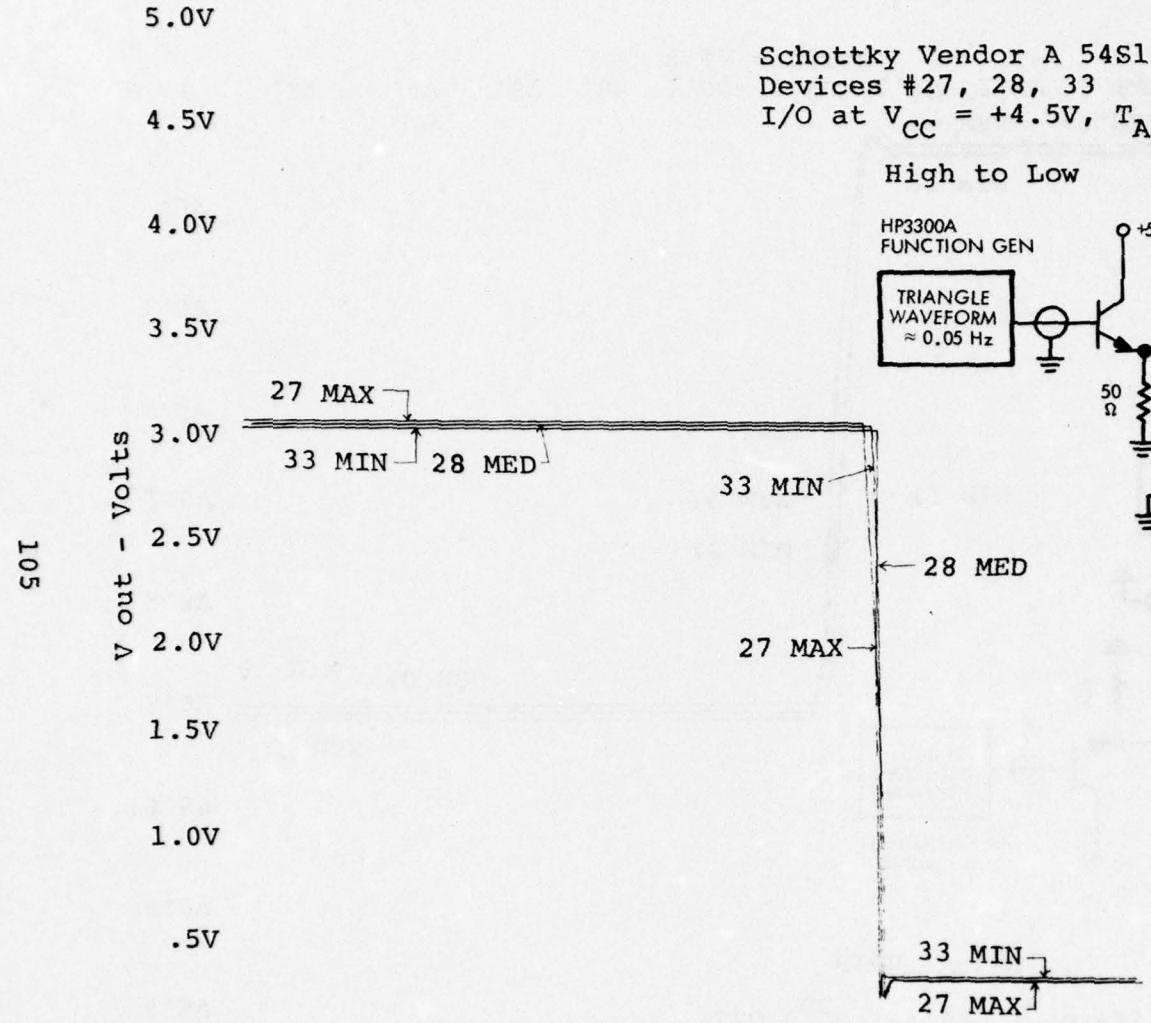
High to Low



Schottky Vendor A 54S138
Devices #27, 28, 33
I/O at V_{CC} = +4.5V, T_A = +25°C

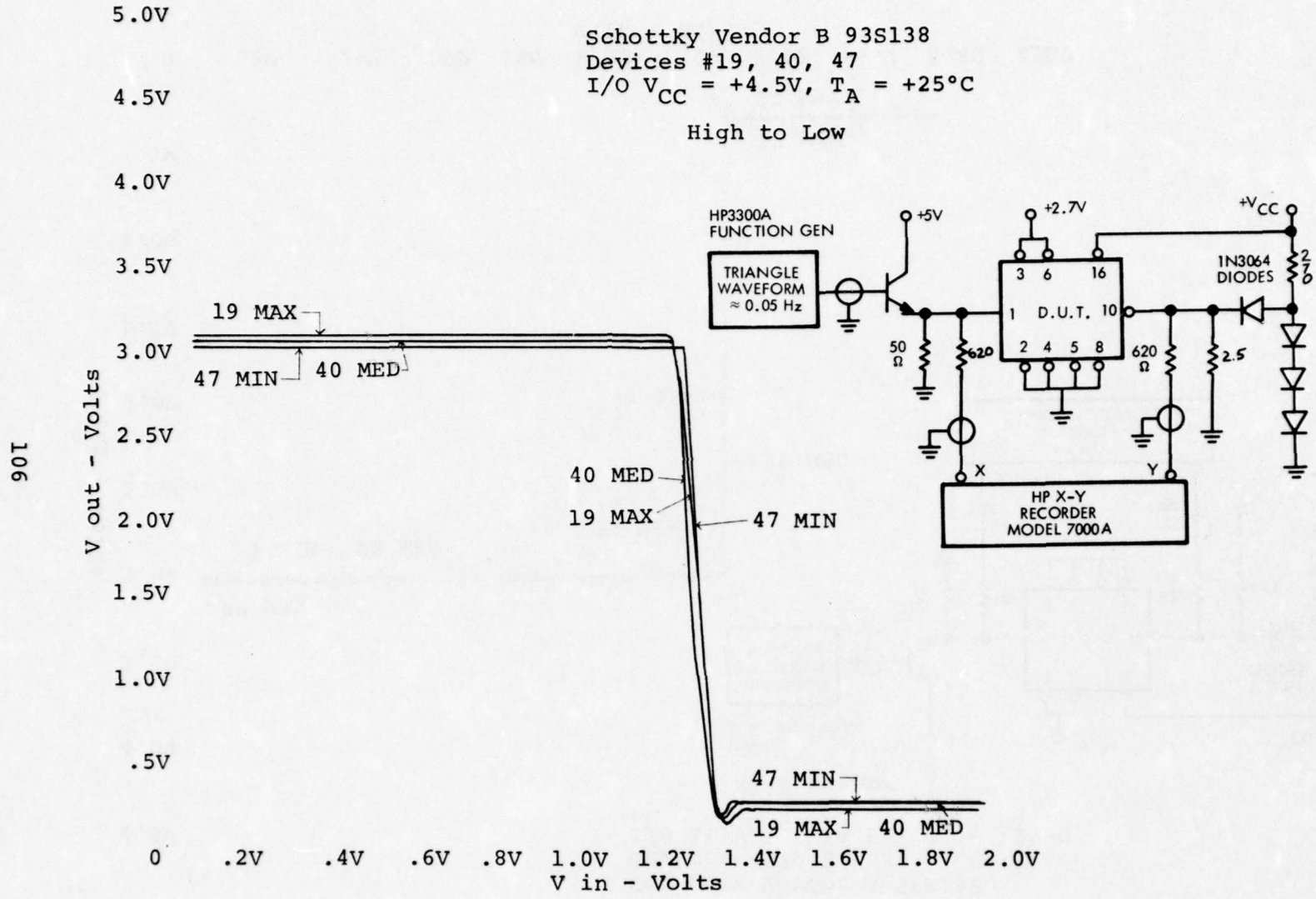
High to Low





Schottky Vendor B 93S138
Devices #19, 40, 47
I/O V_{CC} = +4.5V, T_A = +25°C

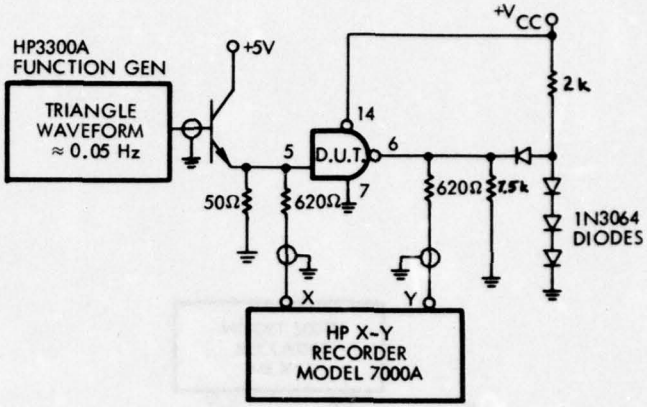
High to Low

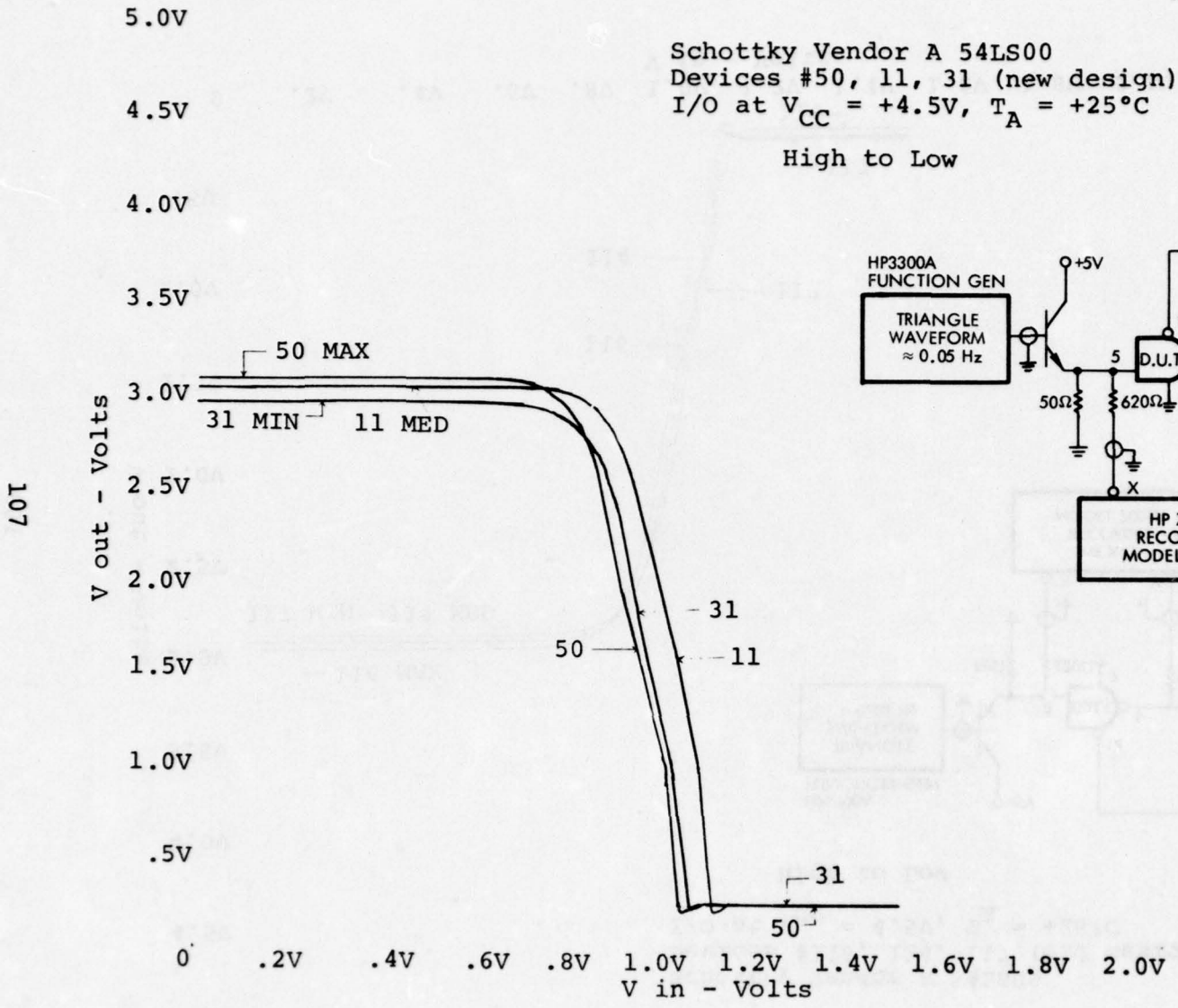


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Schottky Vendor A 54LS00
Devices #50, 11, 31 (new design)
I/O at V_{CC} = +4.5V, T_A = +25°C

High to Low

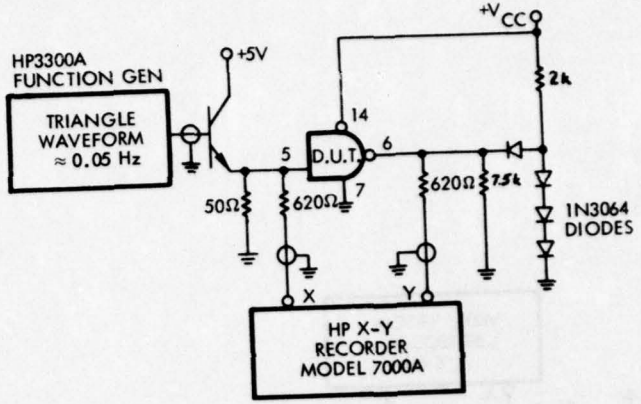


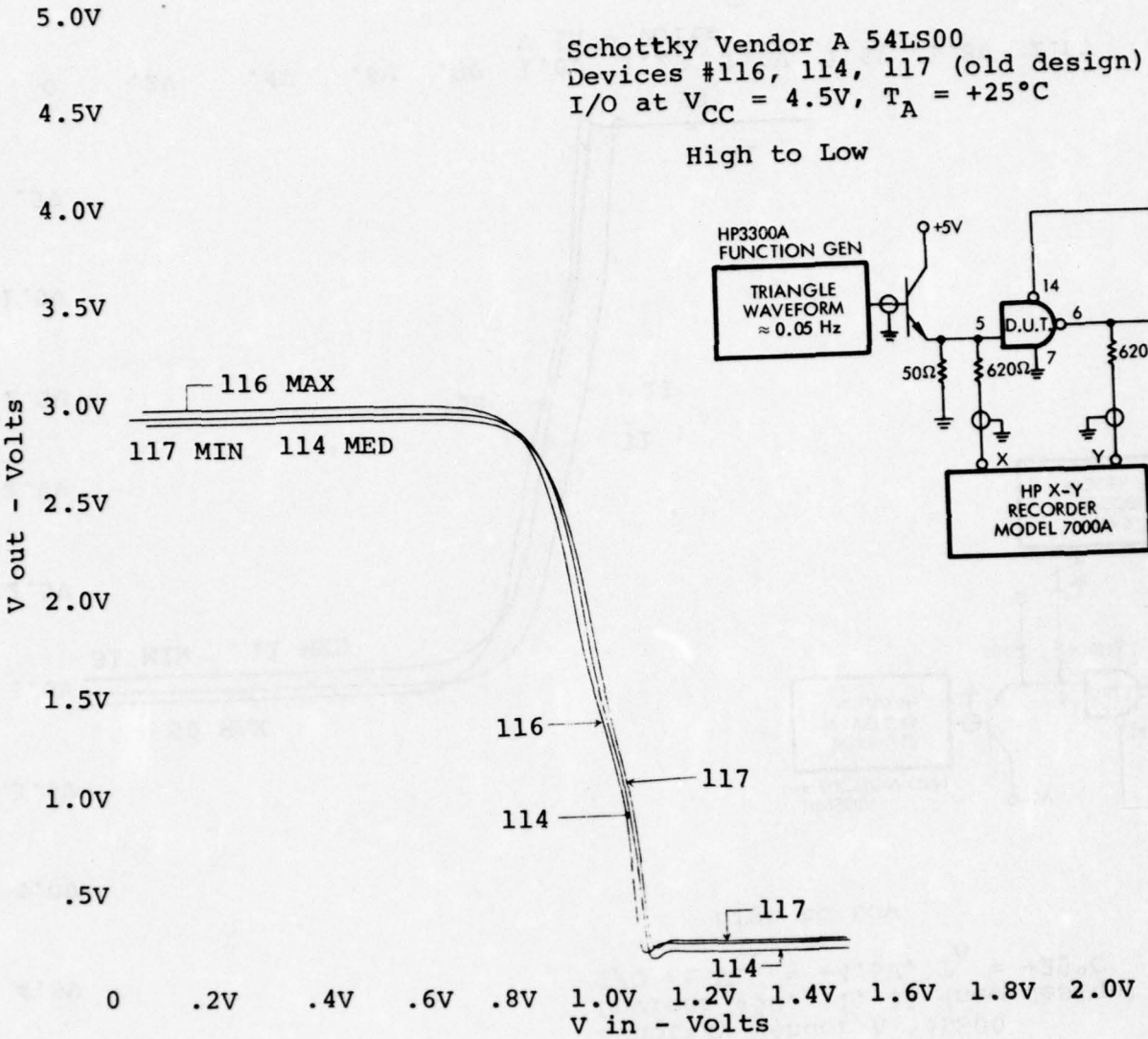


107

Schottky Vendor A 54LS00
Devices #116, 114, 117 (old design)
I/O at V_{CC} = 4.5V, T_A = +25°C

High to Low

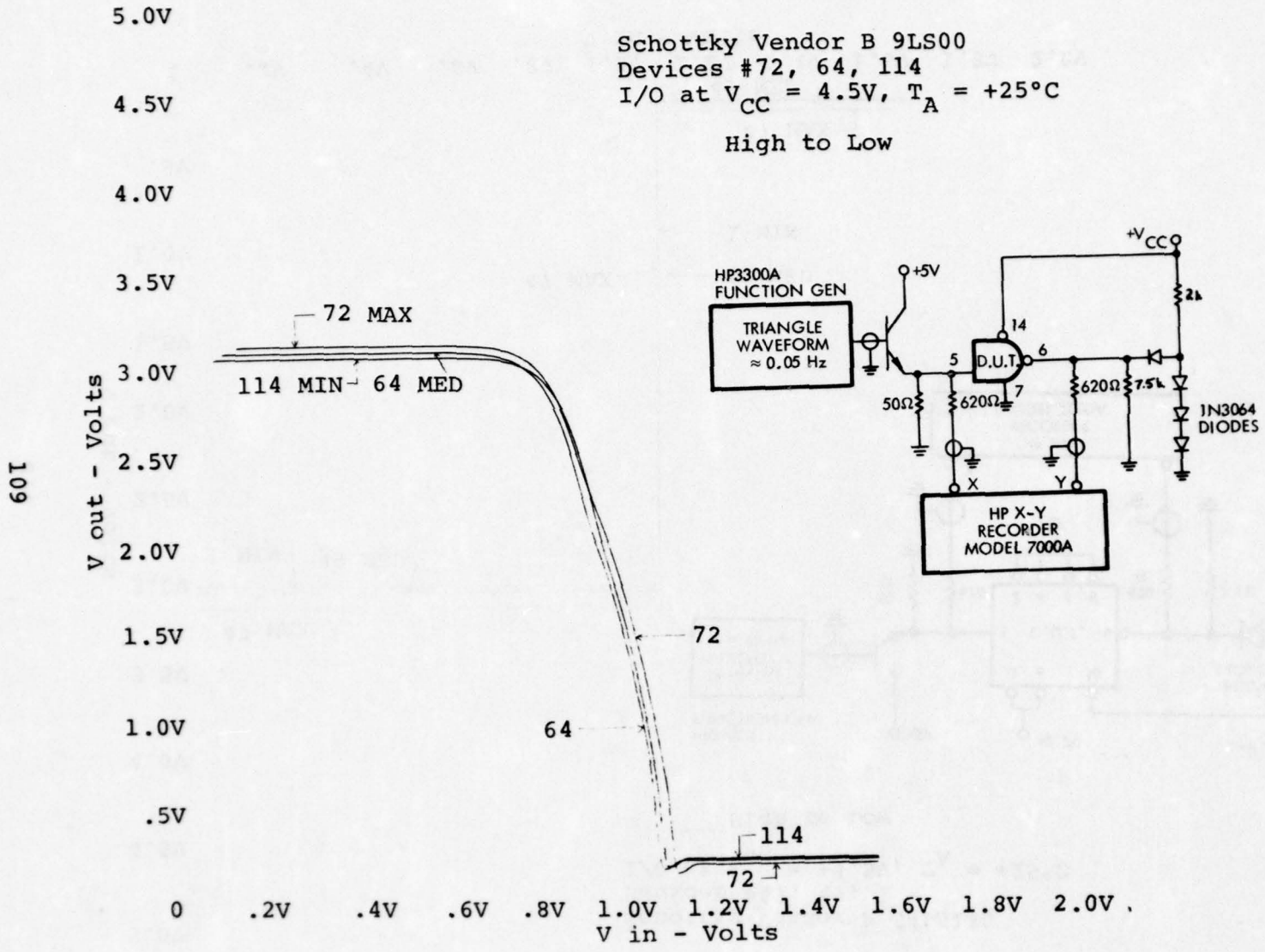




108

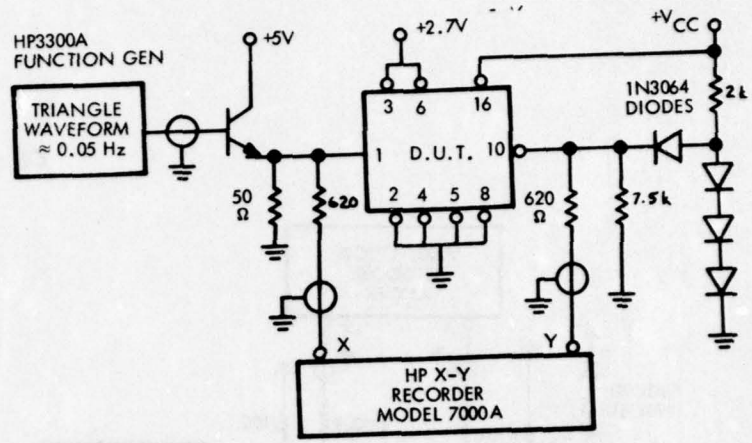
Schottky Vendor B 9LS00
Devices #72, 64, 114
I/O at V_{CC} = 4.5V, T_A = +25°C

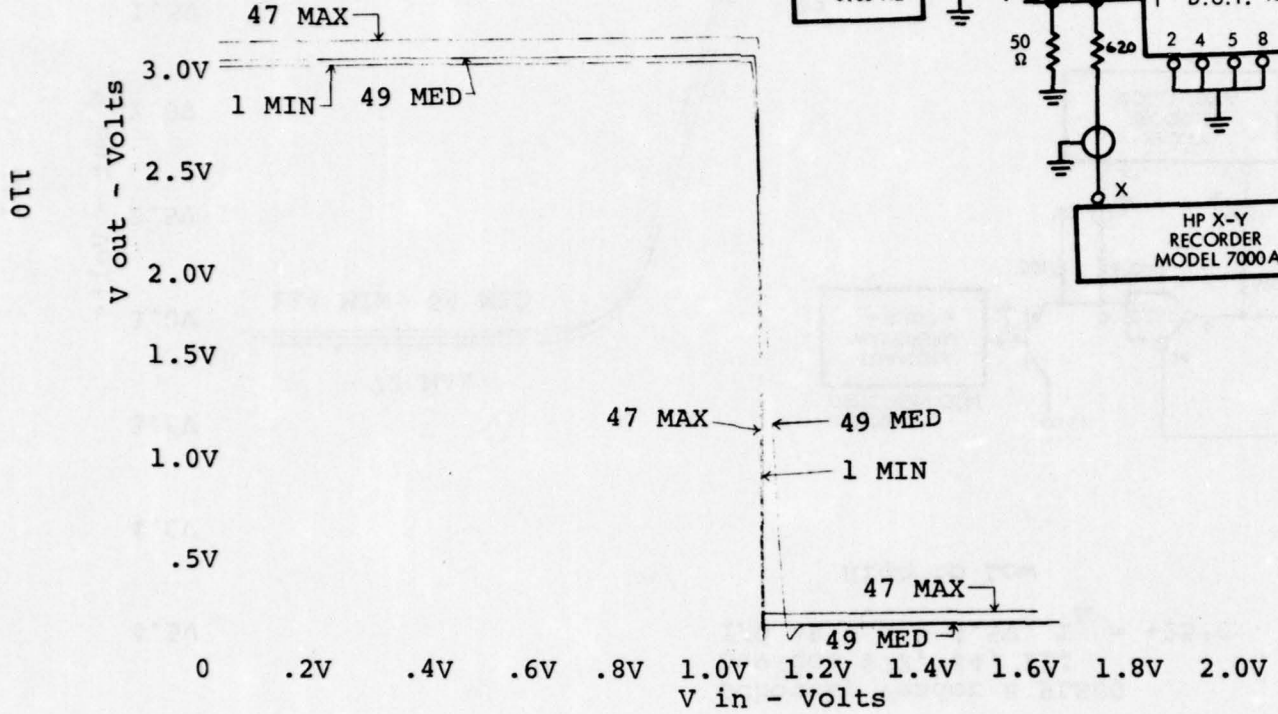
High to Low



Schottky Vendor A 54LS138
Devices #47, 49, 1
I/O at V_{CC} = +4.5V, T_A = +25°C

High to Low

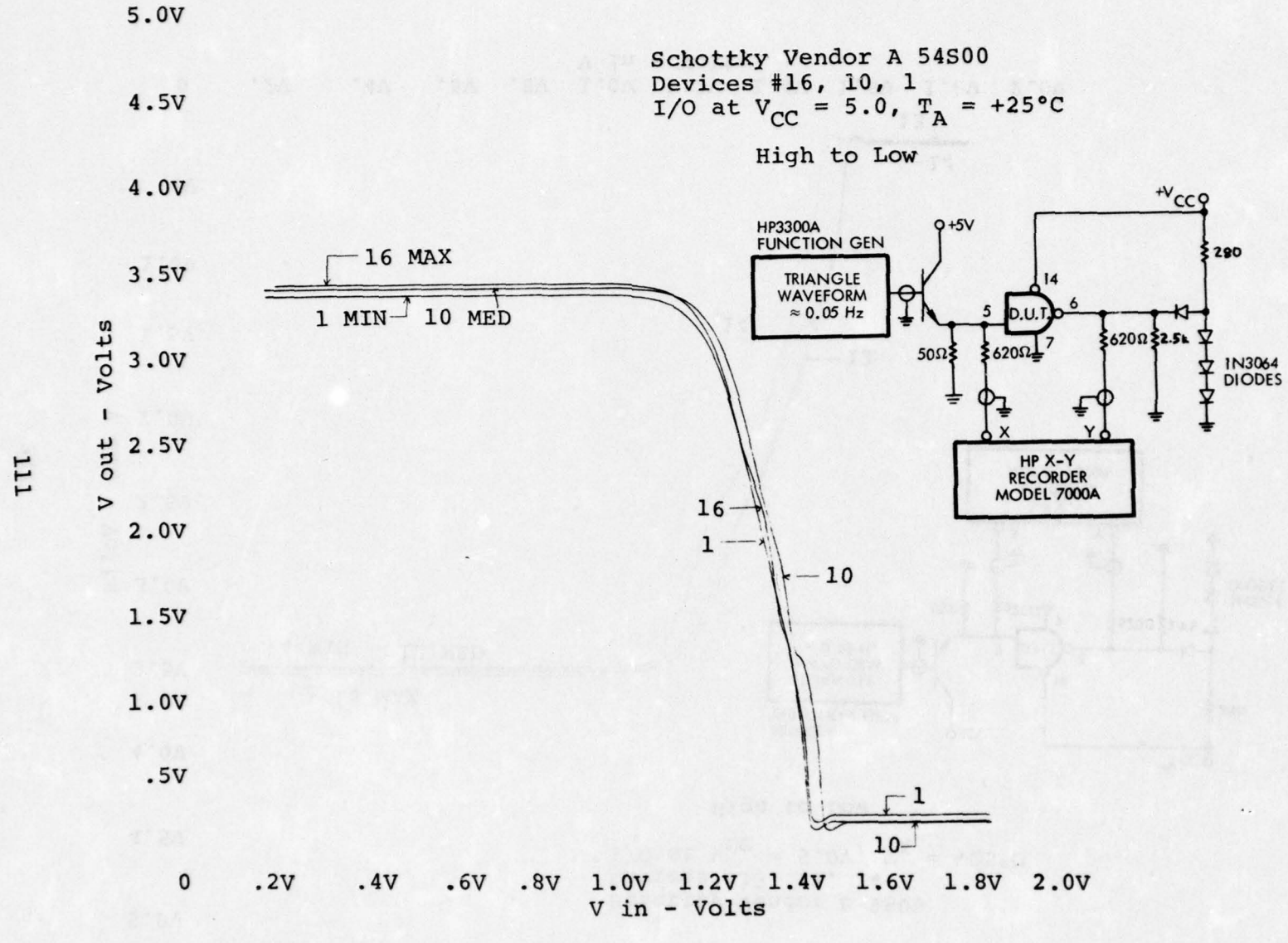




110

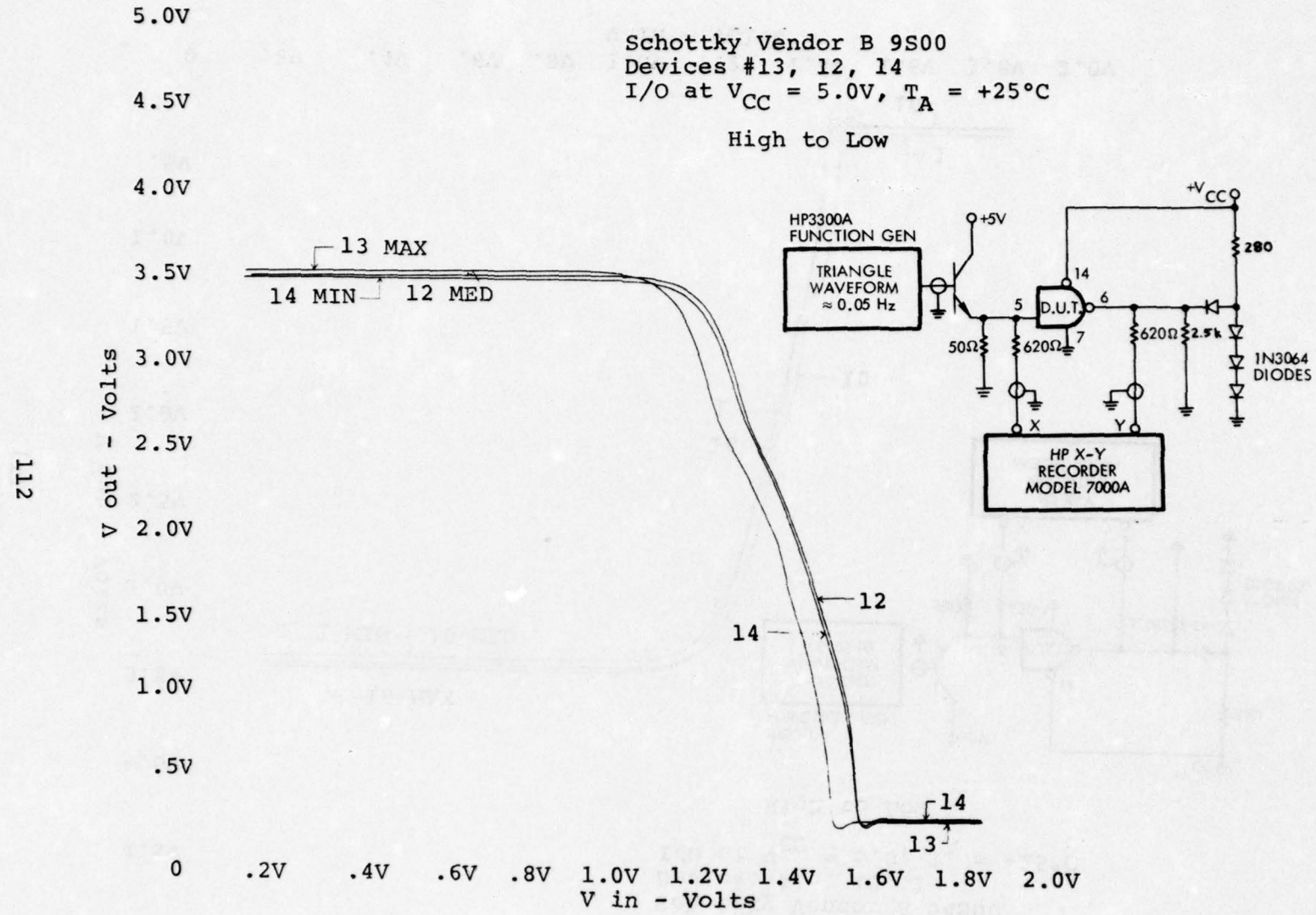
Schottky Vendor A 54S00
Devices #16, 10, 1
I/O at V_{CC} = 5.0, T_A = +25°C

High to Low



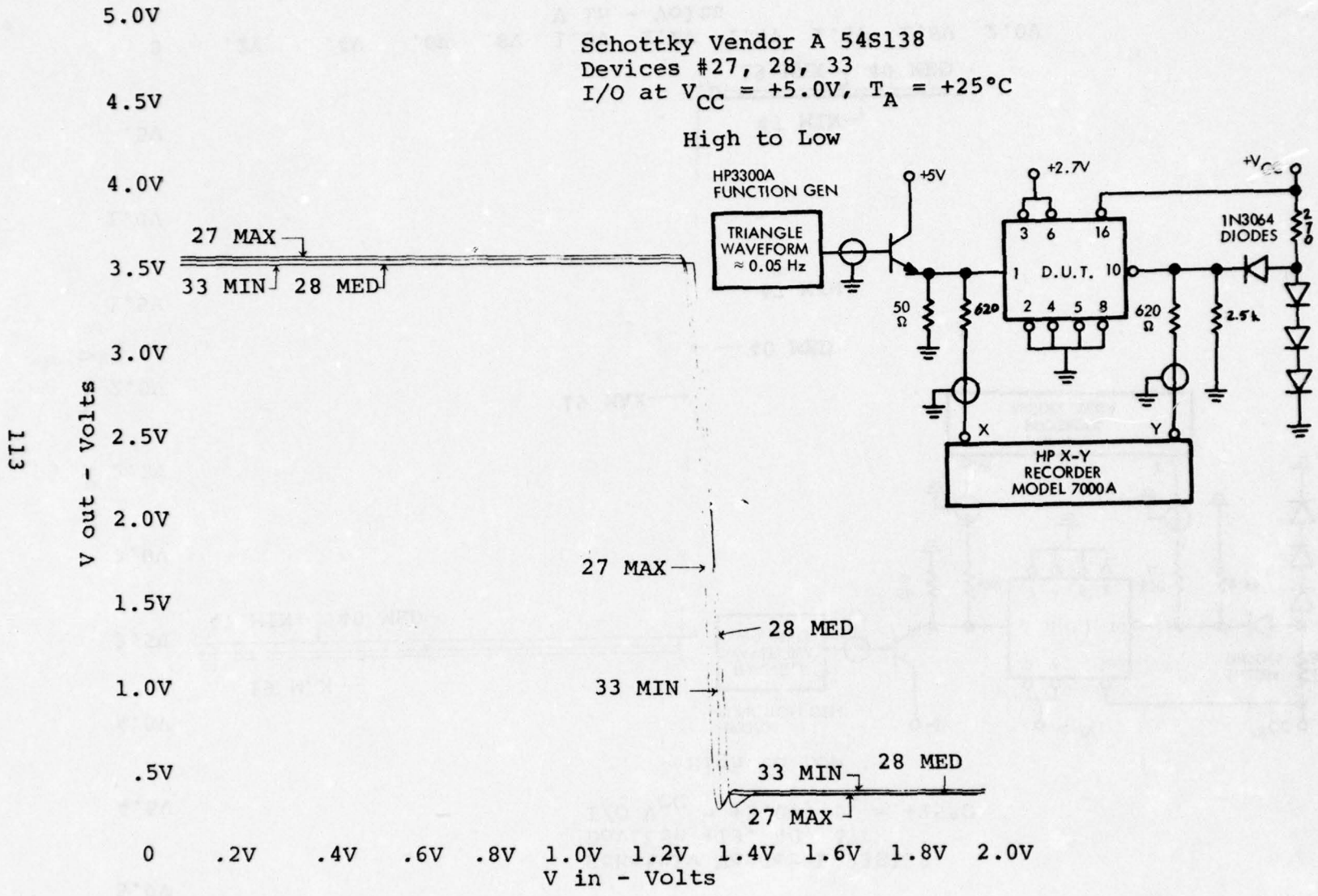
Schottky Vendor B 9S00
Devices #13, 12, 14
I/O at V_{CC} = 5.0V, T_A = +25°C

High to Low



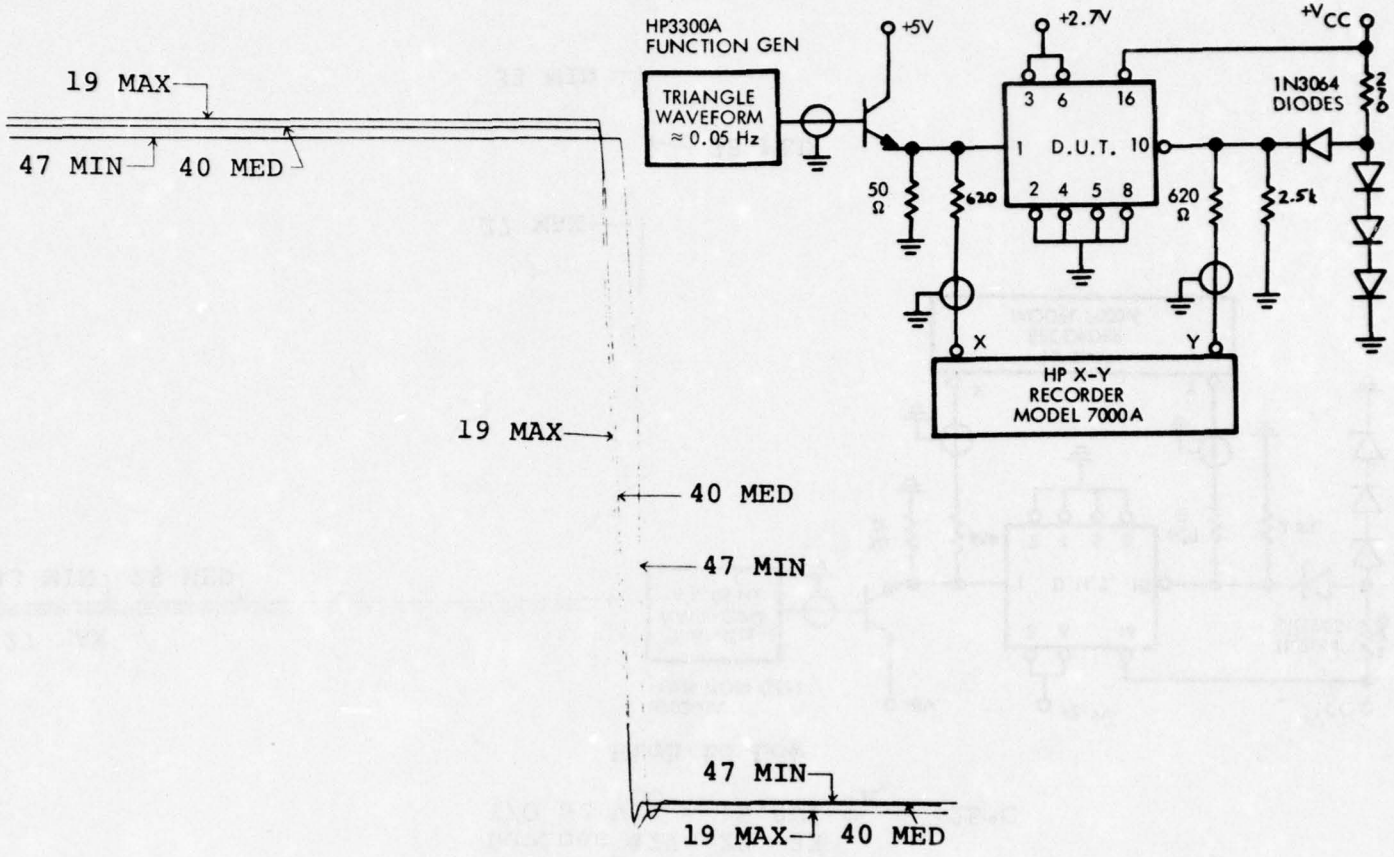
Schottky Vendor A 54S138
Devices #27, 28, 33
I/O at V_{CC} = +5.0V, T_A = +25°C

High to Low



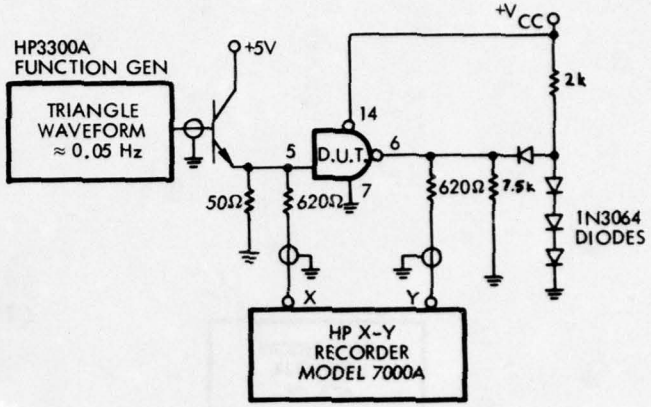
Schottky Vendor B 93S138
Devices #19, 40, 47
I/O V_{CC} = +5.0V, T_A = +25°C

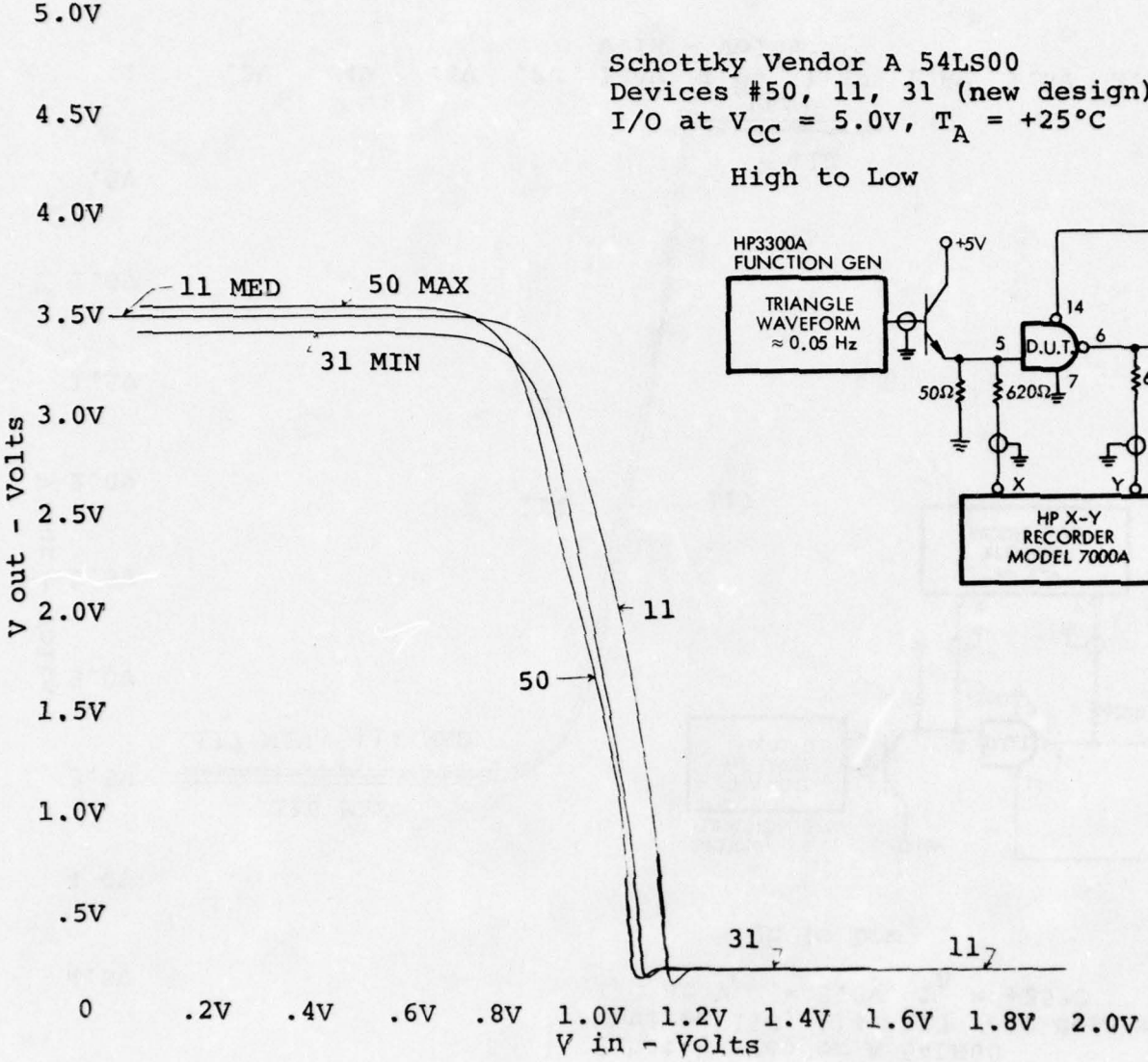
High to Low



Schottky Vendor A 54LS00
Devices #50, 11, 31 (new design)
I/O at V_{CC} = 5.0V, T_A = +25°C

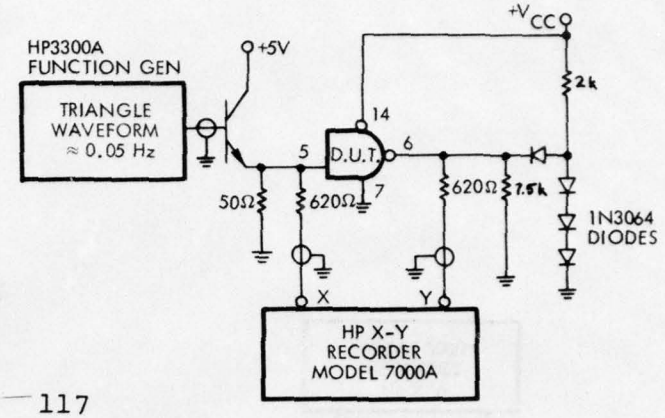
High to Low

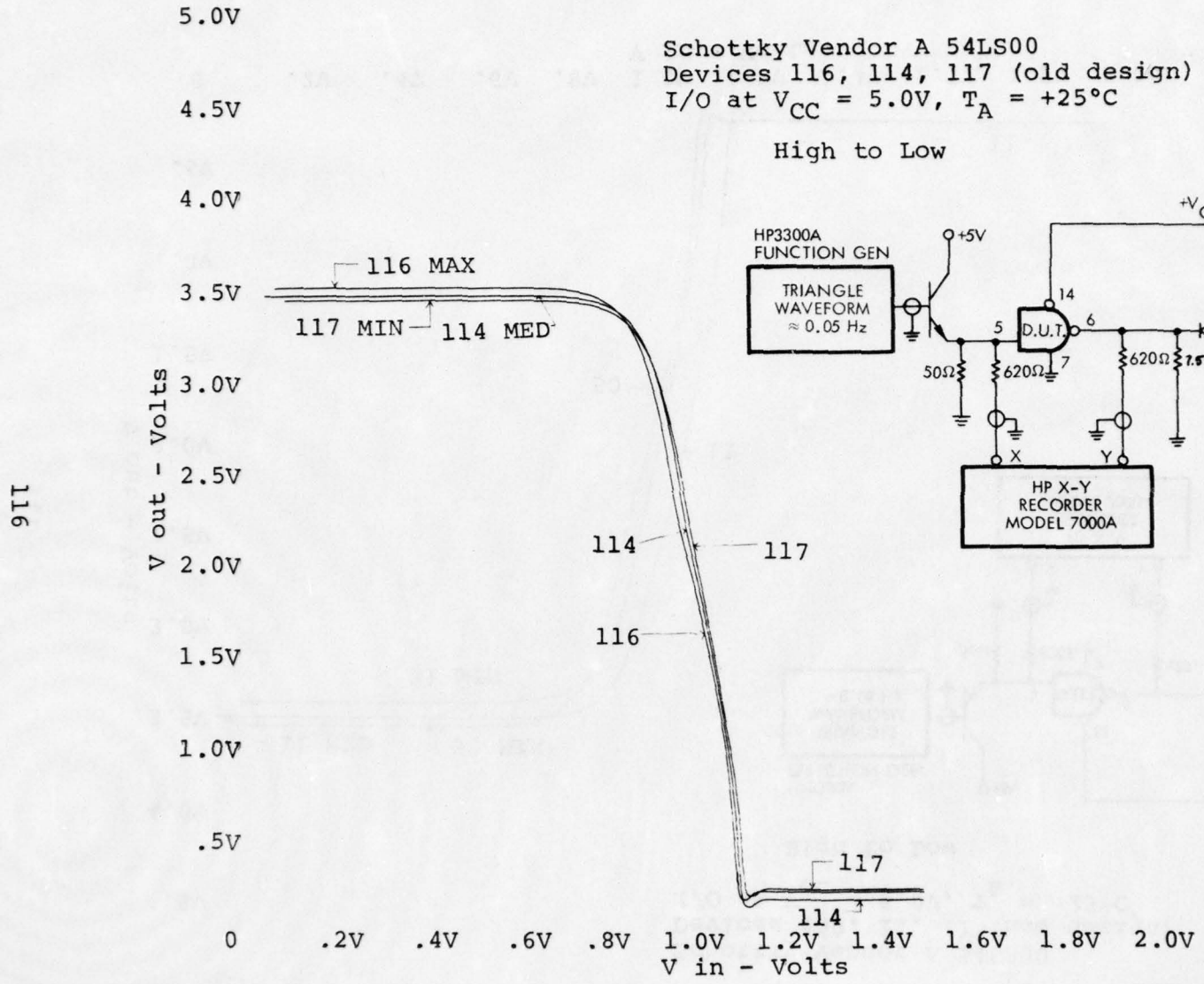




Schottky Vendor A 54LS00
Devices 116, 114, 117 (old design)
I/O at V_{CC} = 5.0V, T_A = +25°C

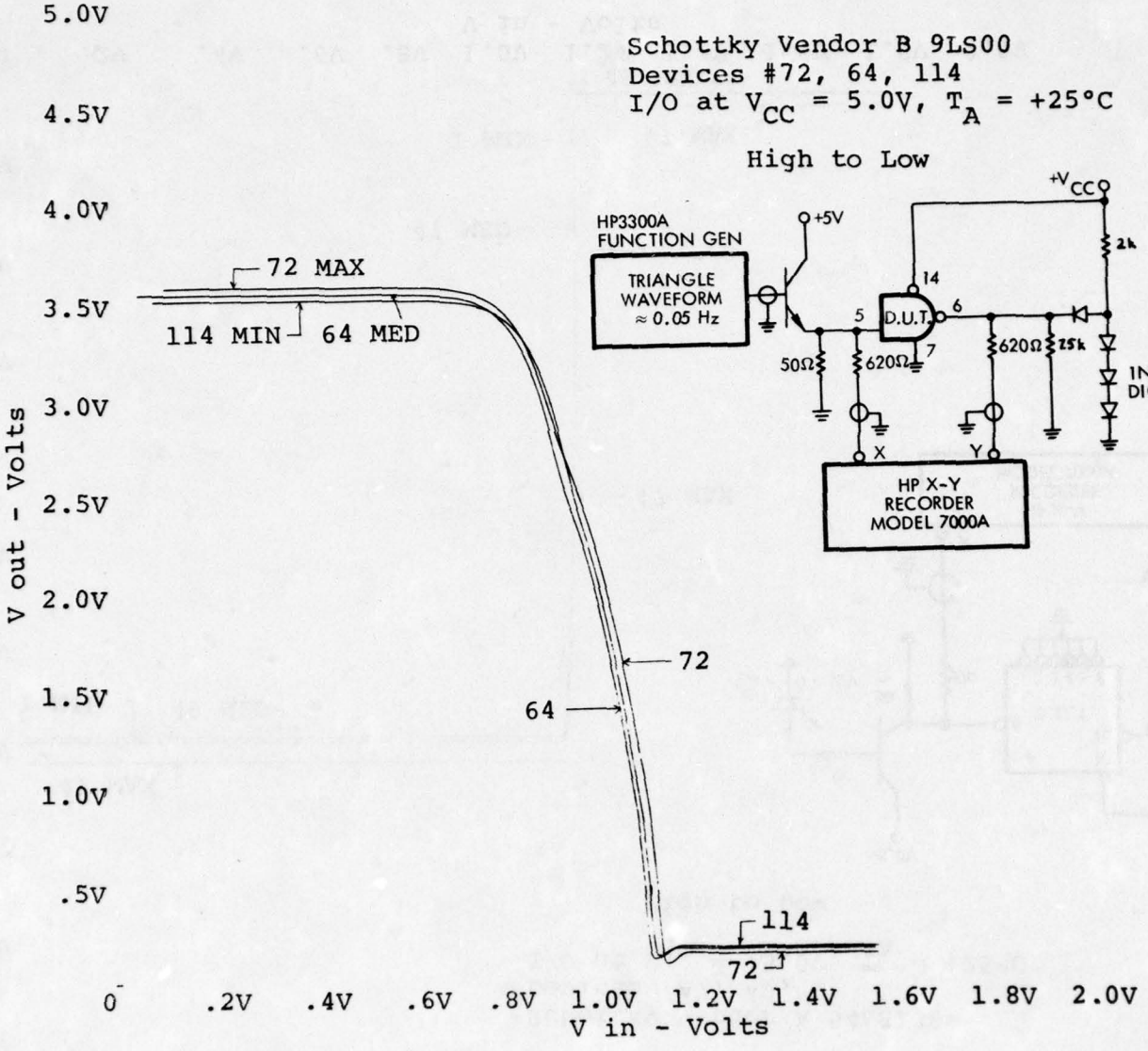
High to Low





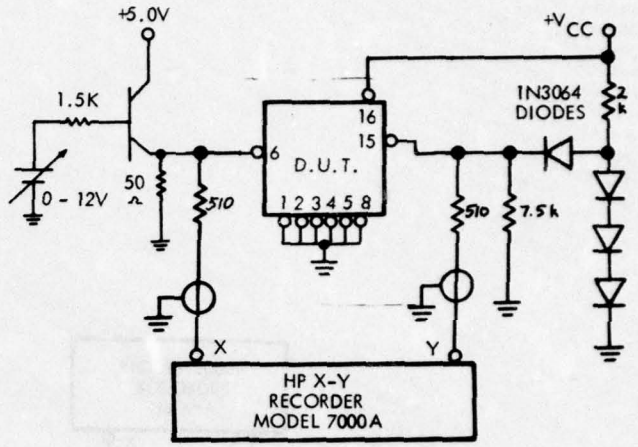
Schottky Vendor B 9LS00
Devices #72, 64, 114
I/O at V_{CC} = 5.0V, T_A = +25°C

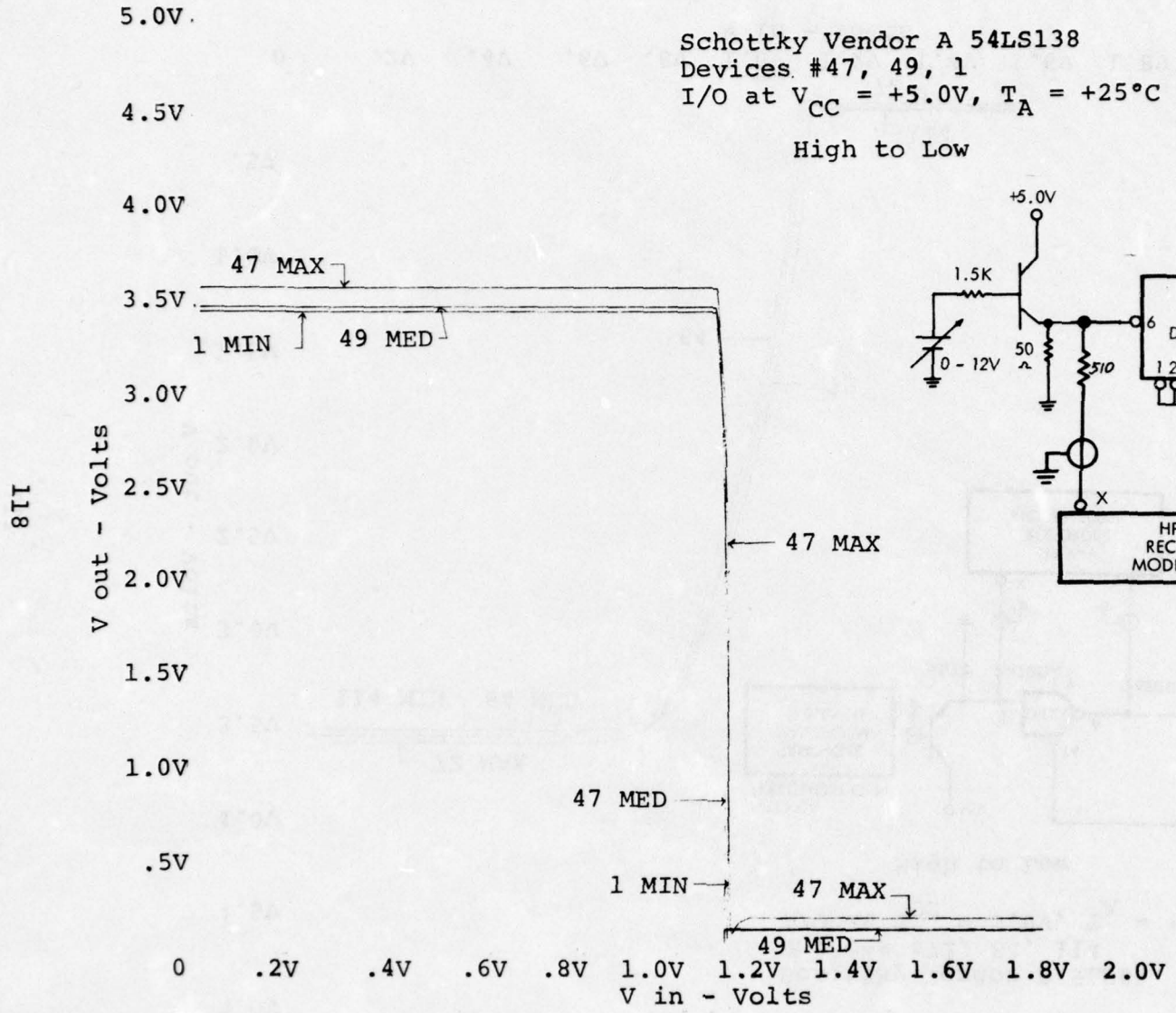
High to Low

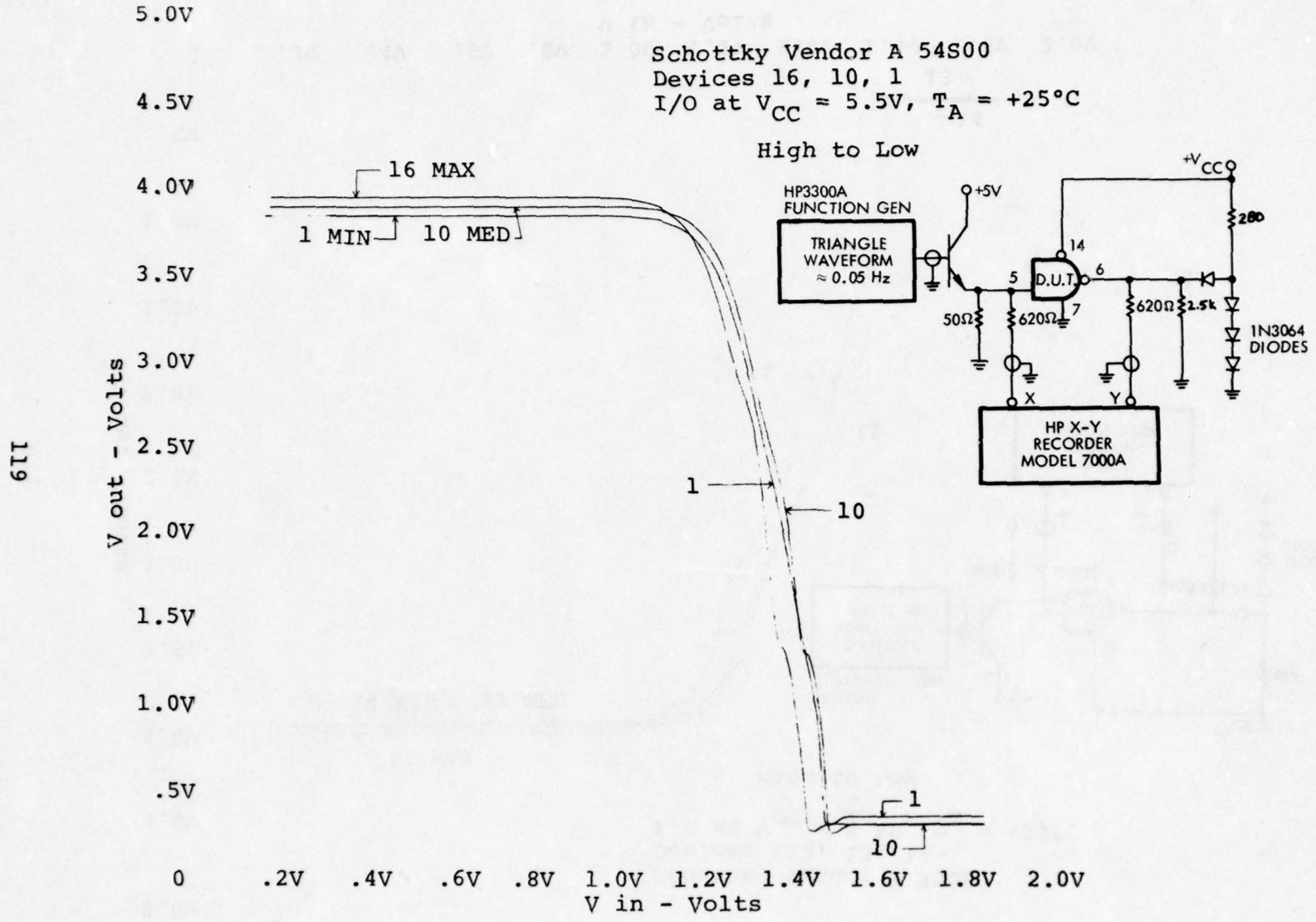


Schottky Vendor A 54LS138
Devices #47, 49, 1
I/O at V_{CC} = +5.0V, T_A = +25°C

High to Low

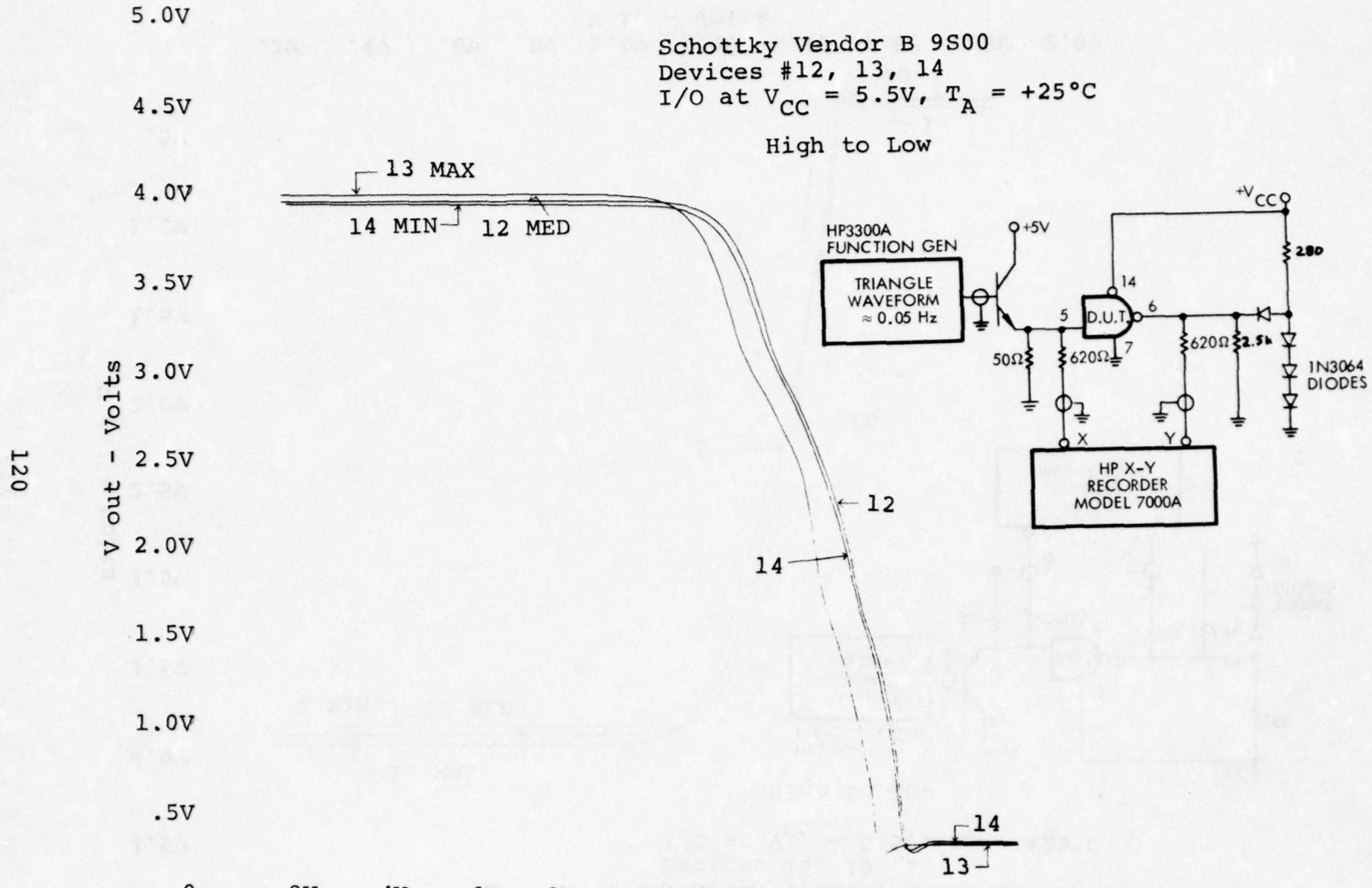





Schottky Vendor A 54S00
Devices 16, 10, 1
I/O at V_{CC} = 5.5V, T_A = +25°C
High to Low
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
.5V
0
.2V
.4V
.6V
.8V
1.0V
1.2V
1.4V
1.6V
1.8V
2.0V
V out - Volts
V in - Volts
16 MAX
1 MIN
10 MED
1
10
1
10
HP3300A
FUNCTION GEN
TRIANGLE
WAVEFORM
≈ 0.05 Hz
+5V
+VCC
280
14
5
D.U.T.
6
7
50Ω
620Ω
620Ω
2.5k
1N3064
DIODES
X
Y
HP X-Y
RECORDER
MODEL 7000A

Schottky Vendor B 9S00
Devices #12, 13, 14
I/O at V_{CC} = 5.5V, T_A = +25°C

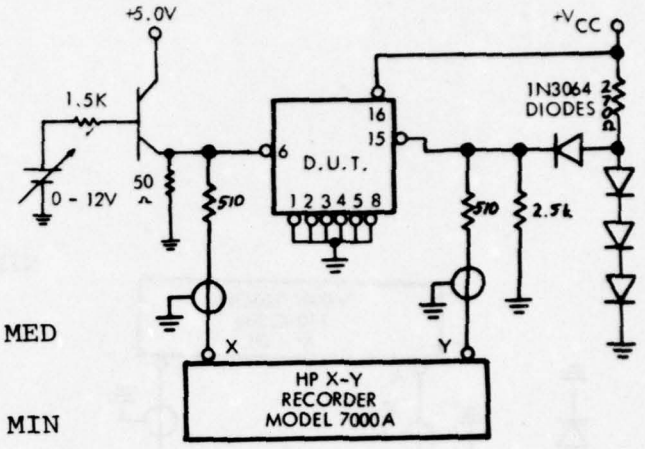
High to Low

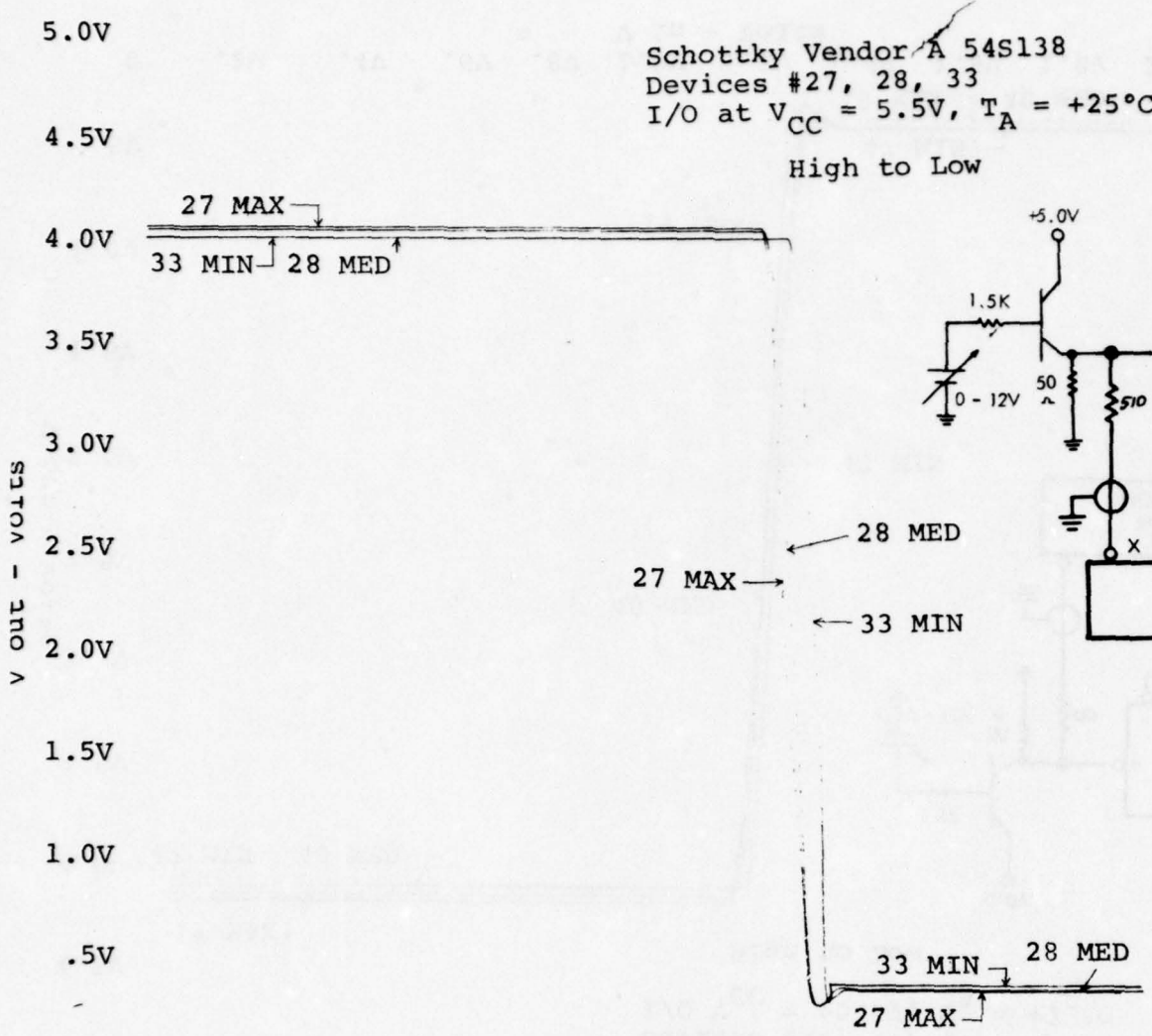


120

Schottky Vendor A 54S138
Devices #27, 28, 33
I/O at V_{CC} = 5.5V, T_A = +25°C

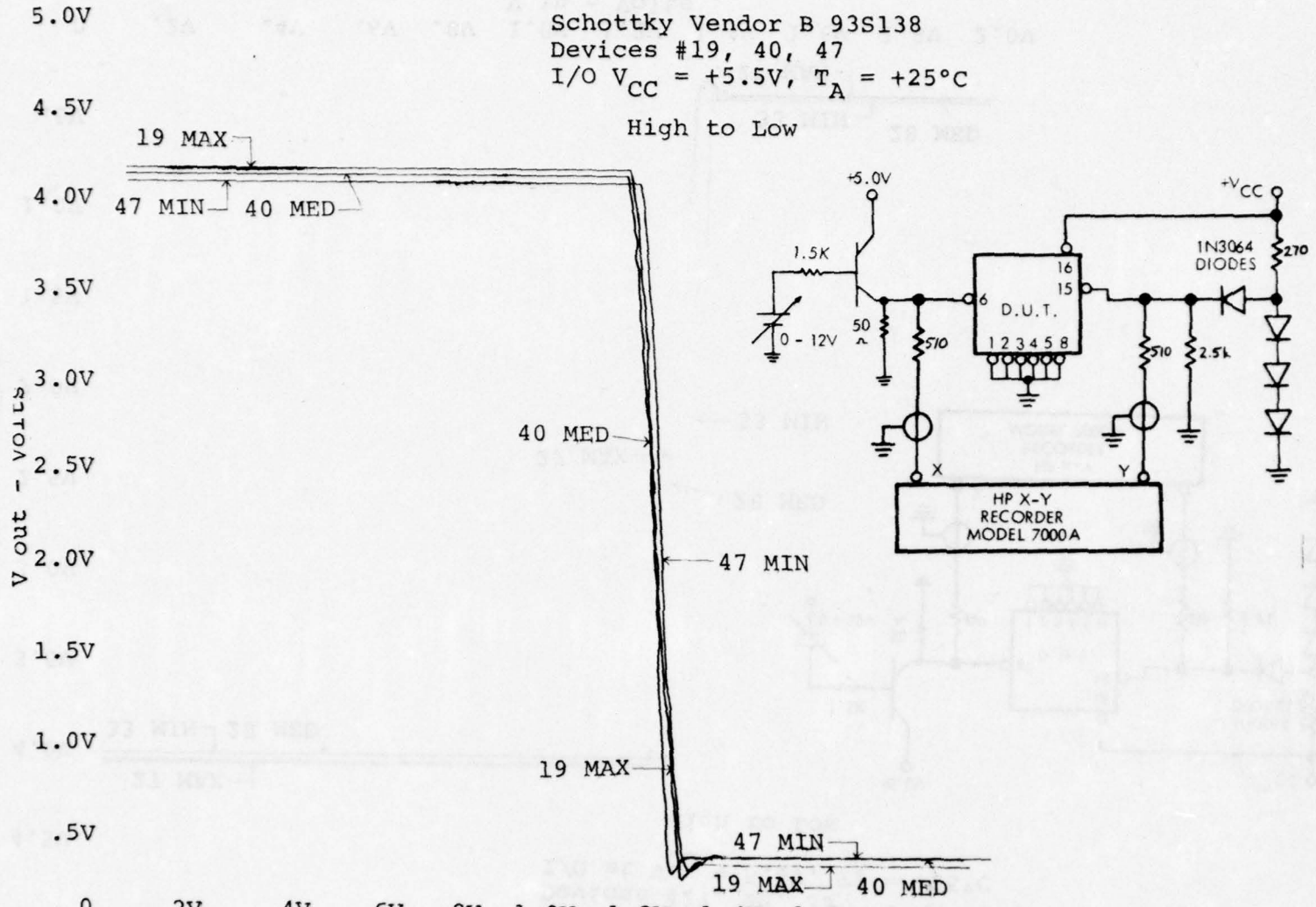
High to Low





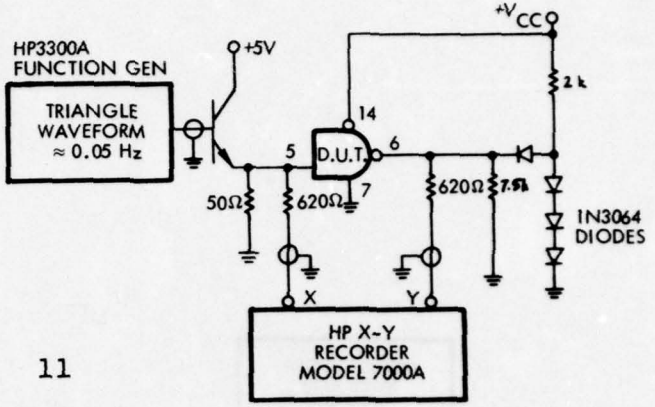
Schottky Vendor B 93S138
Devices #19, 40, 47
I/O V_{CC} = +5.5V, T_A = +25°C

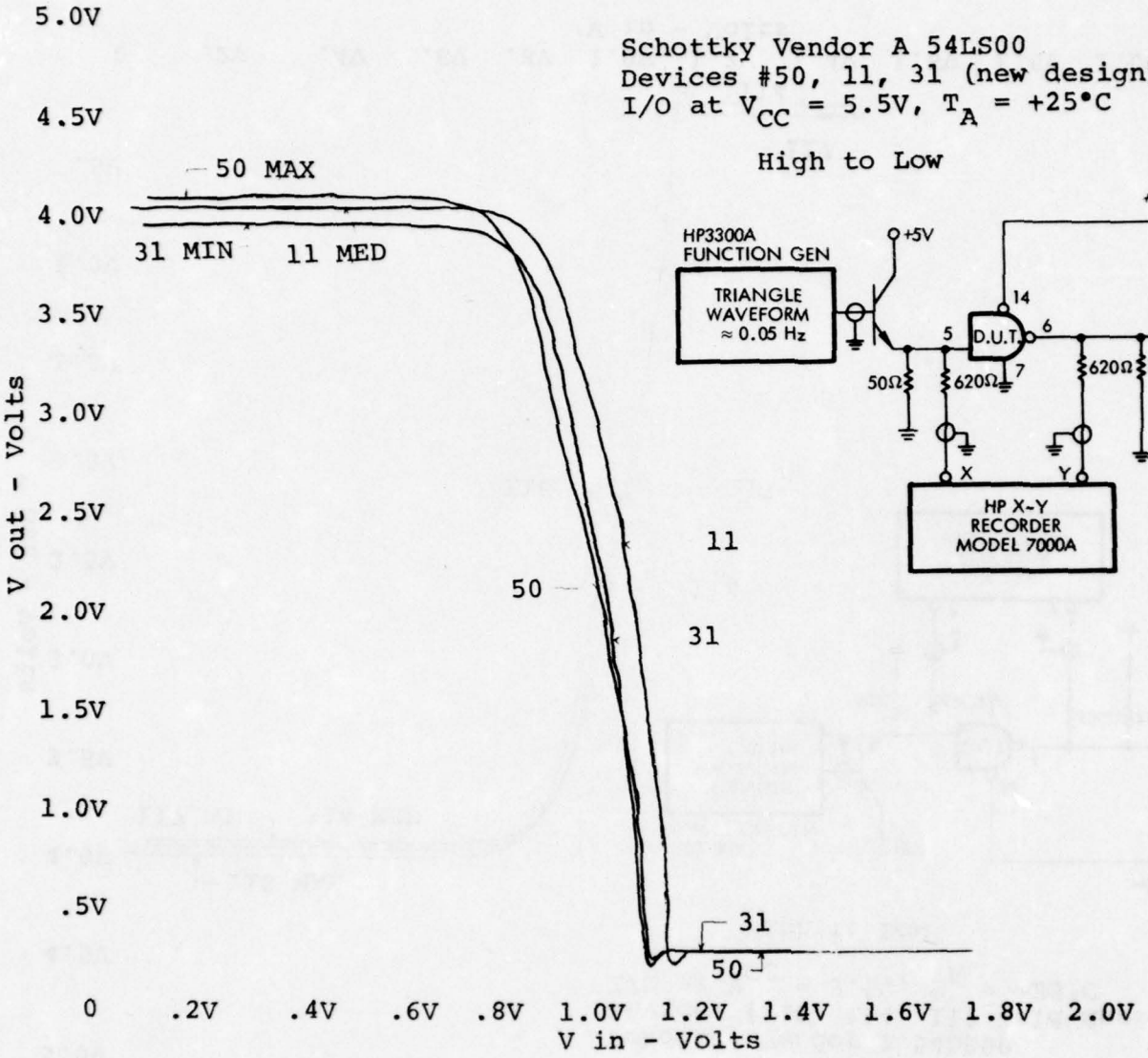
High to Low



Schottky Vendor A 54LS00
Devices #50, 11, 31 (new design)
I/O at V_{CC} = 5.5V, T_A = +25°C

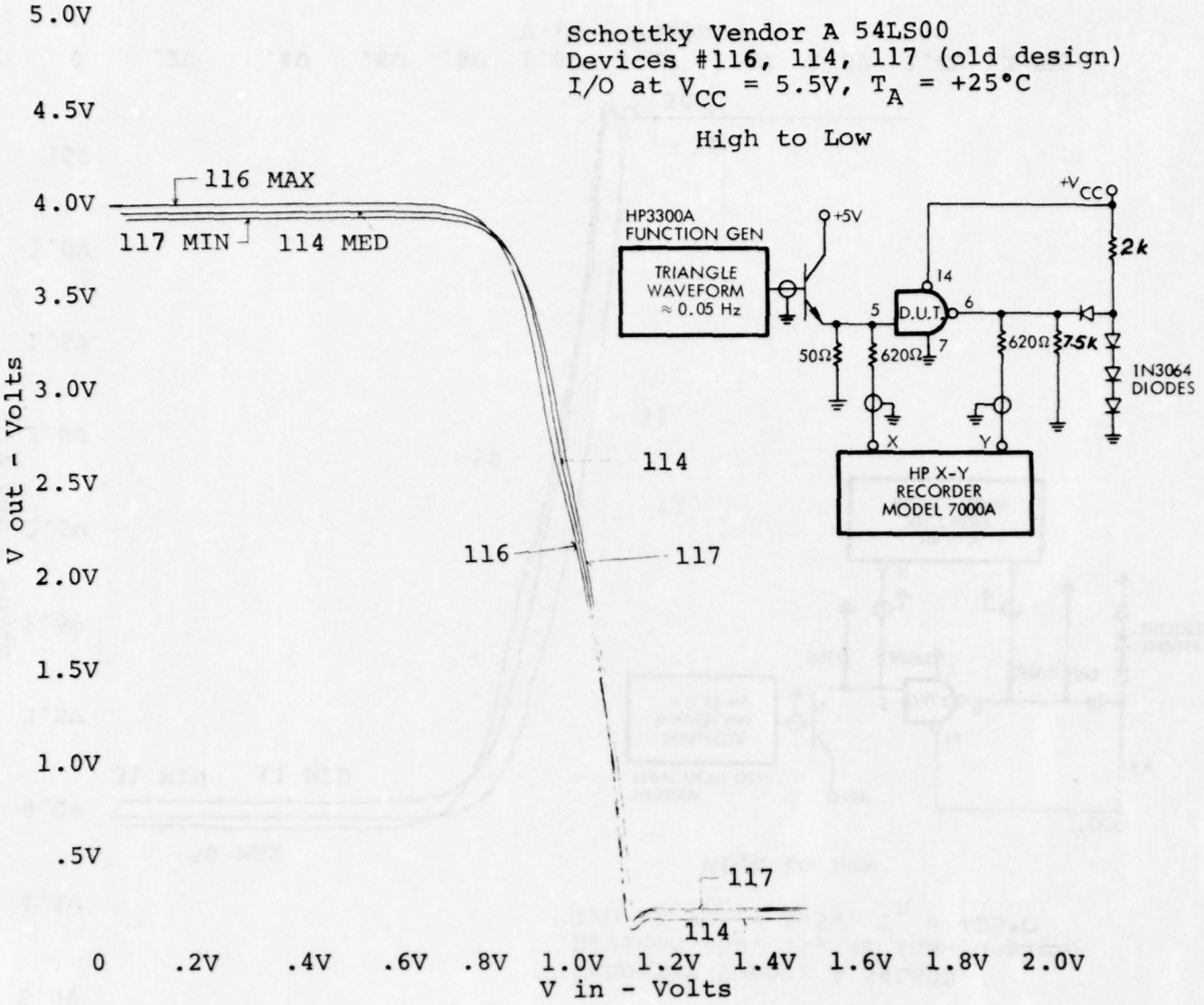
High to Low





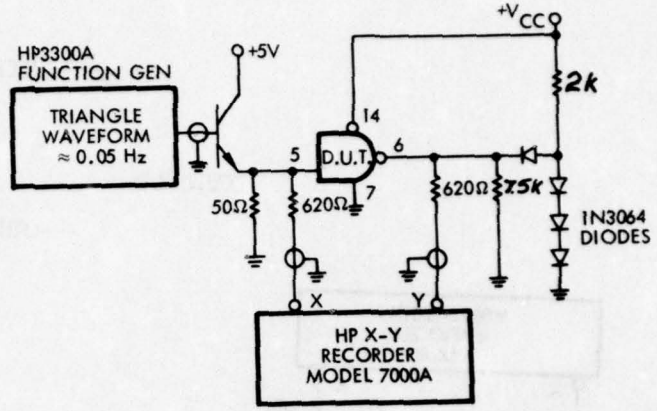
Schottky Vendor A 54LS00
Devices #116, 114, 117 (old design)
I/O at V_{CC} = 5.5V, T_A = +25°C

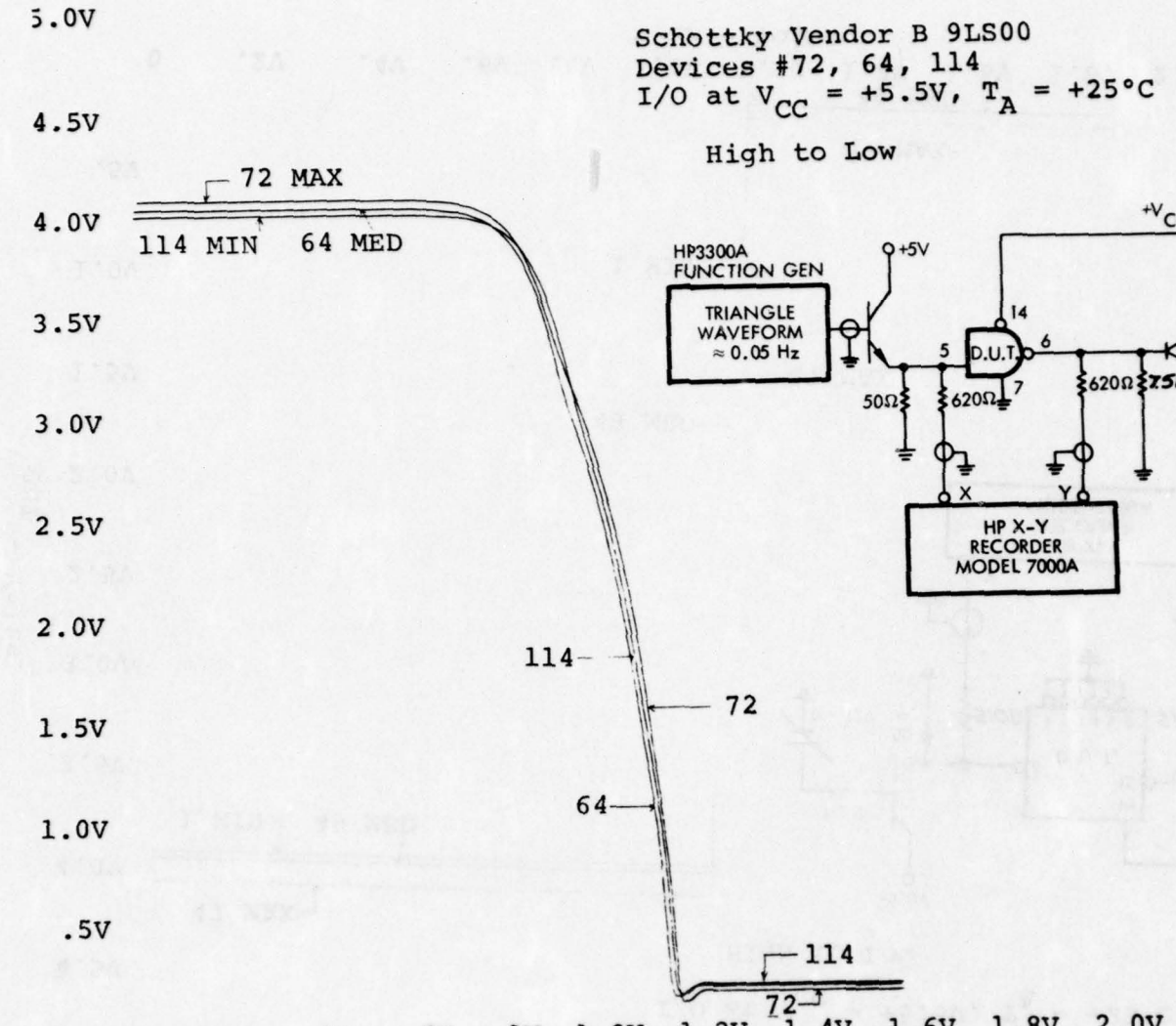
High to Low



Schottky Vendor B 9LS00
Devices #72, 64, 114
I/O at V_{CC} = +5.5V, T_A = +25°C

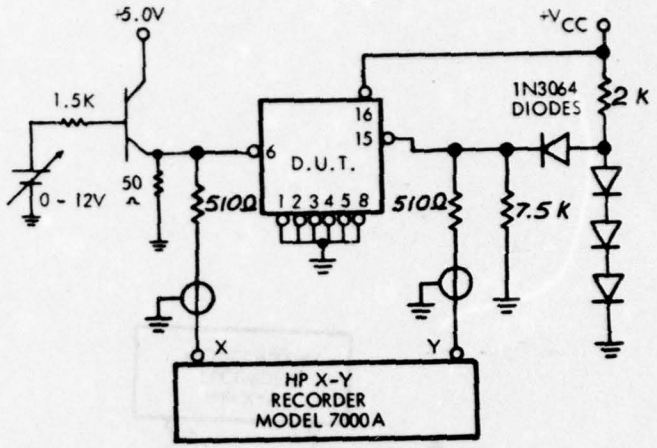
High to Low

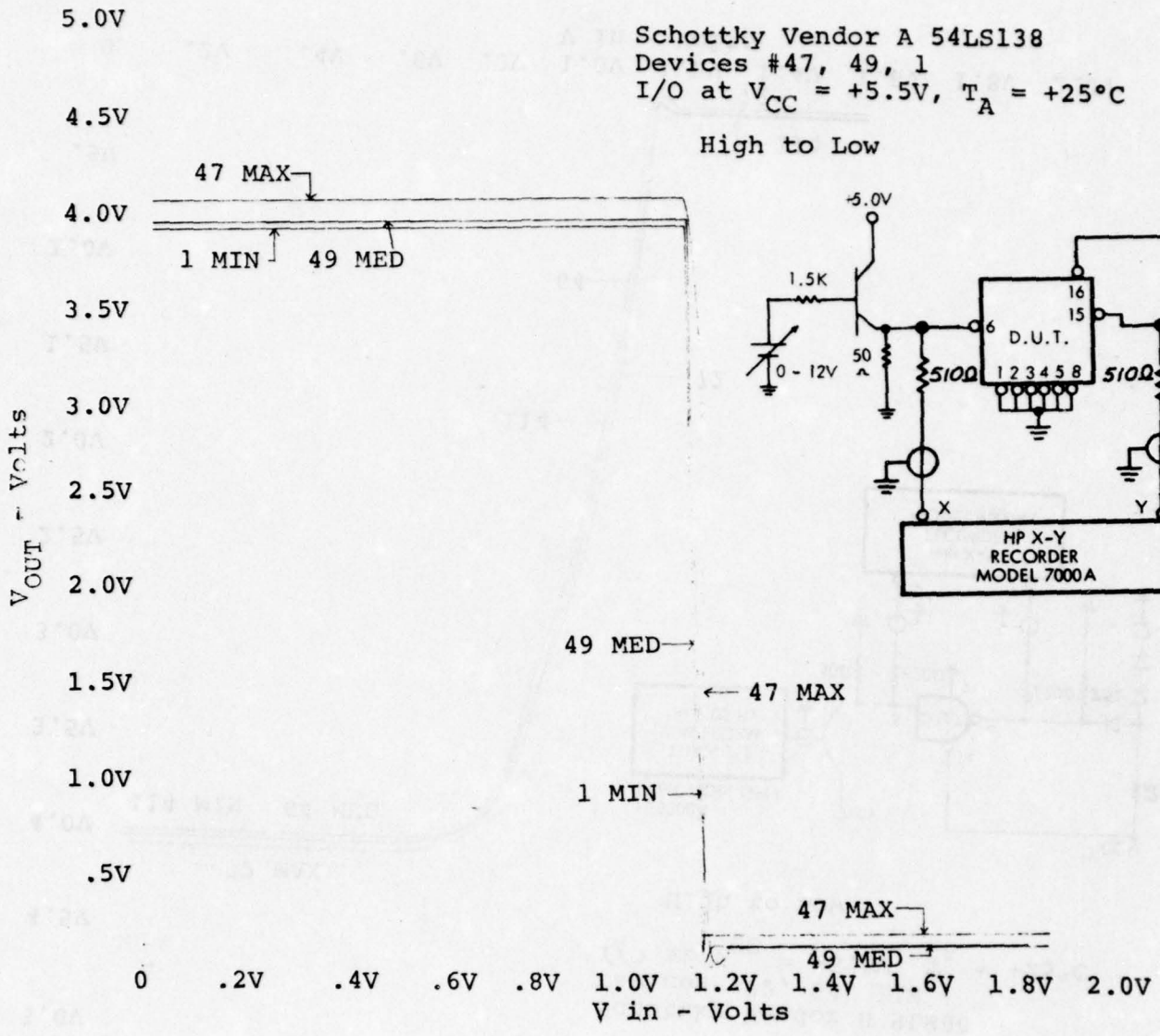




Schottky Vendor A 54LS138
Devices #47, 49, 1
I/O at V_{CC} = +5.5V, T_A = +25°C

High to Low

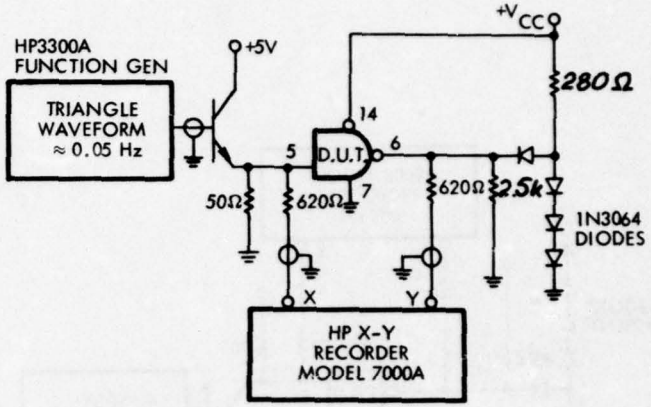


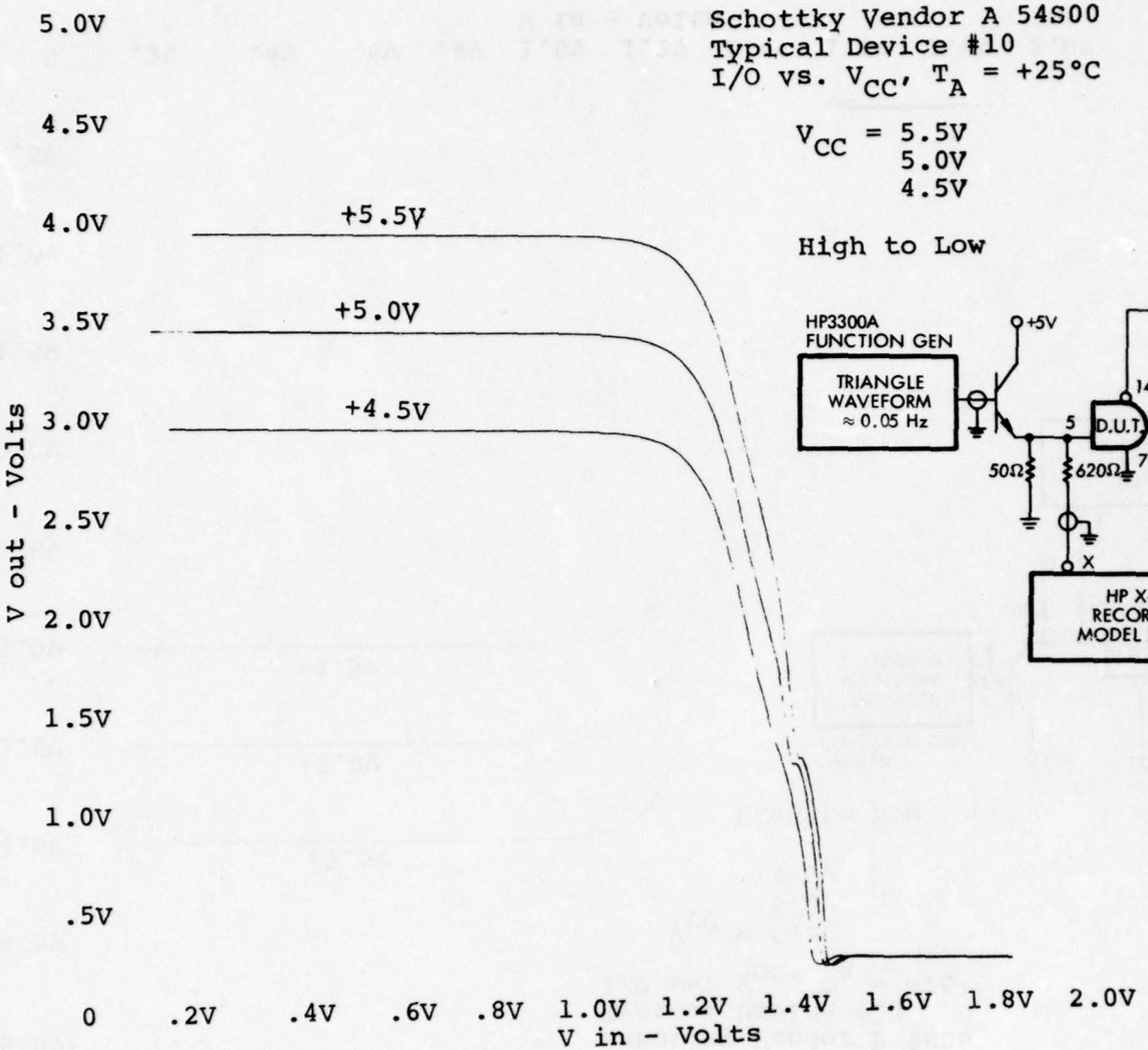


Schottky Vendor A 54S00
Typical Device #10
I/O vs. V_{CC}, T_A = +25°C

V_{CC} = 5.5V
5.0V
4.5V

High to Low

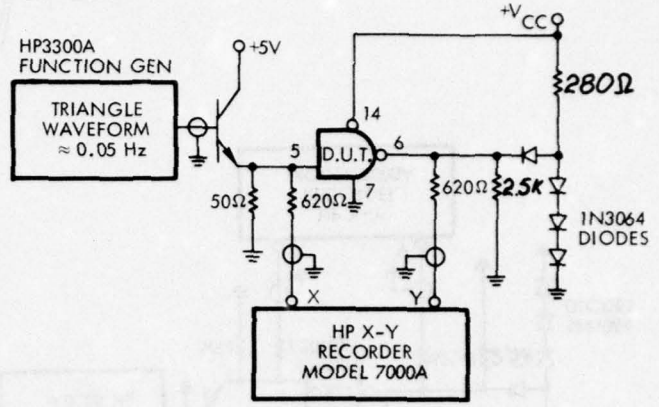


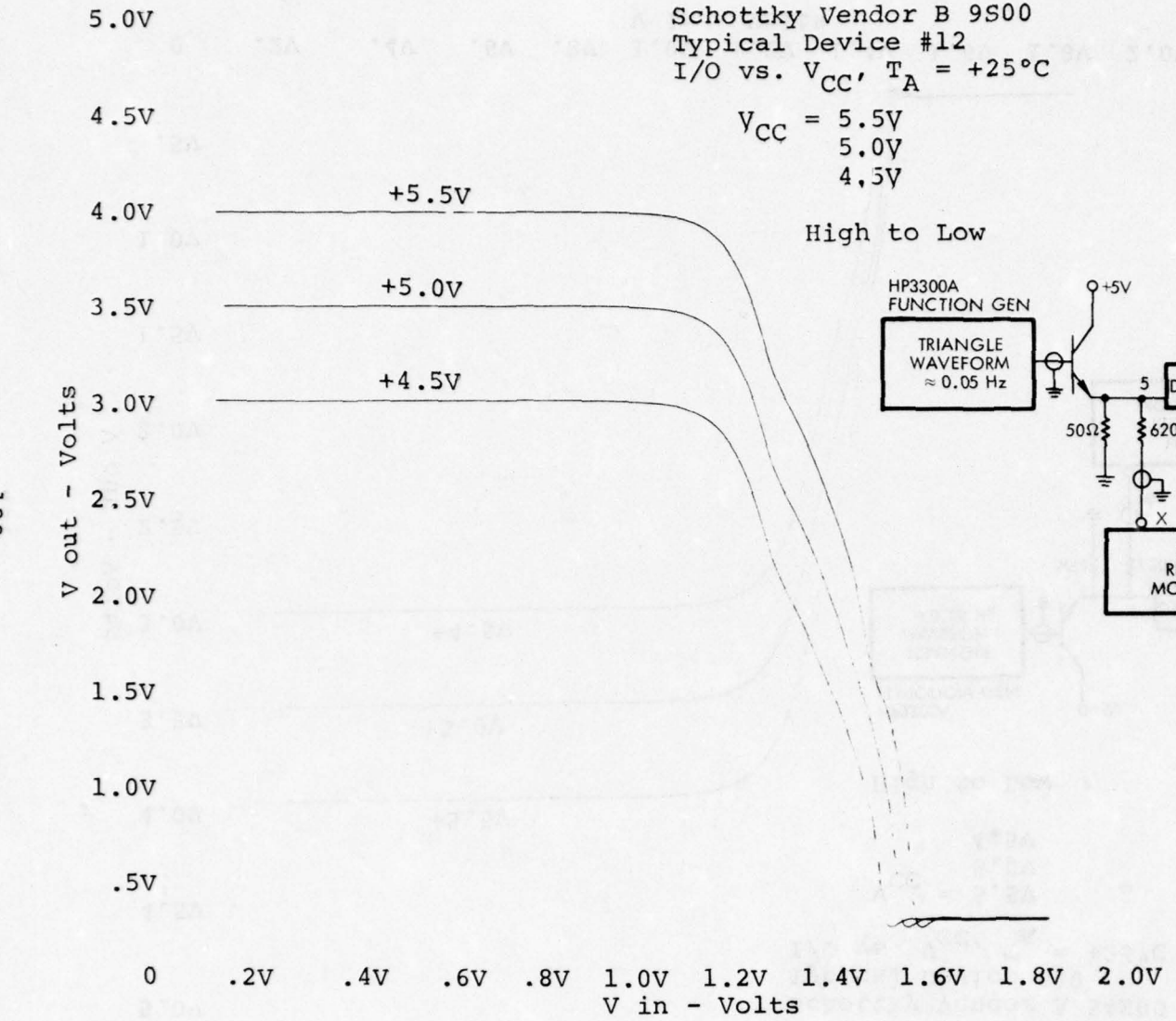


Schottky Vendor B 9S00
Typical Device #12
I/O vs. V_{CC}, T_A = +25°C

V_{CC} = 5.5V
5.0V
4.5V

High to Low

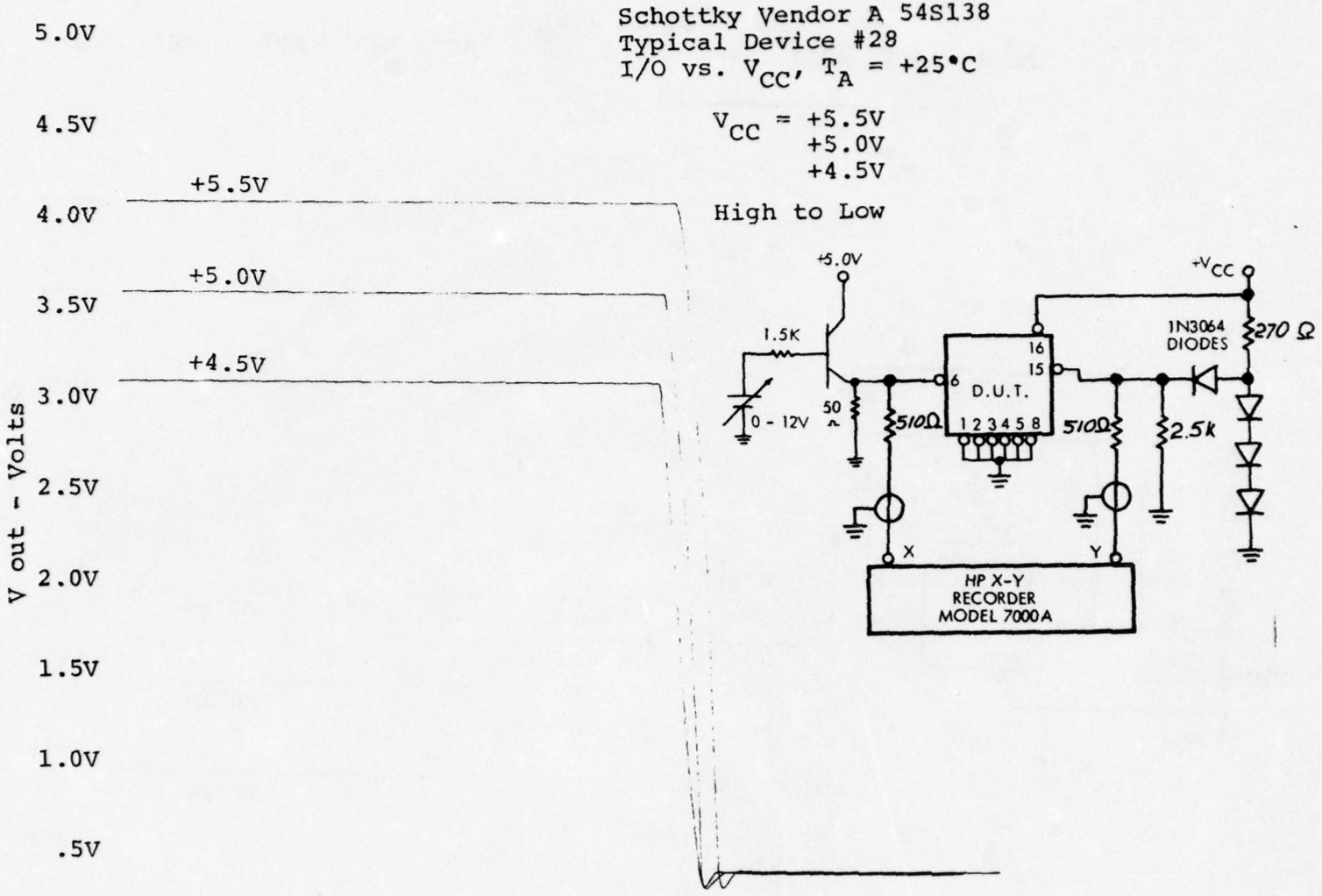




Schottky Vendor A 54S138
Typical Device #28
I/O vs. V_{CC}, T_A = +25°C

V_{CC} = +5.5V
+5.0V
+4.5V

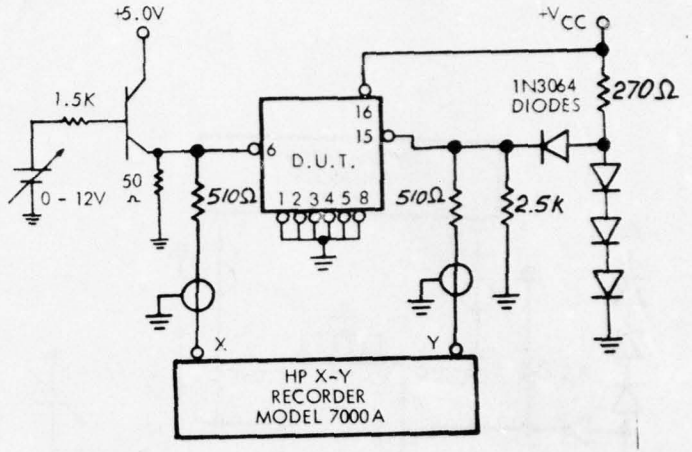
High to Low

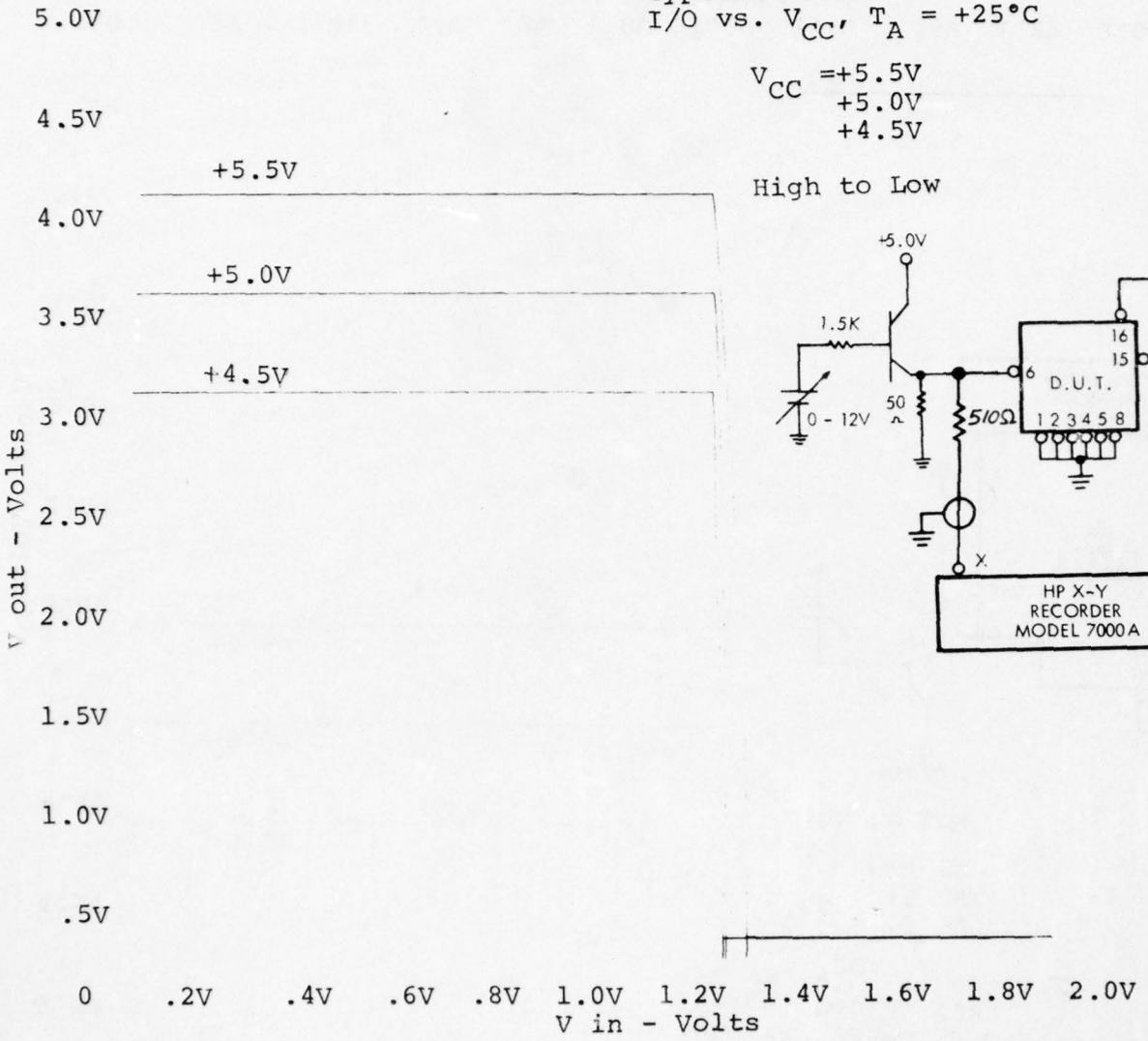


Schottky Vendor B 93S138
Typical Device #40
I/O vs. V_{CC}, T_A = +25°C

V_{CC} =+5.5V
+5.0V
+4.5V

High to Low

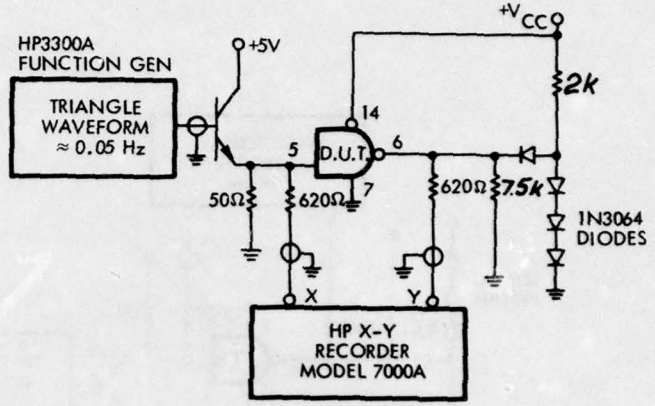


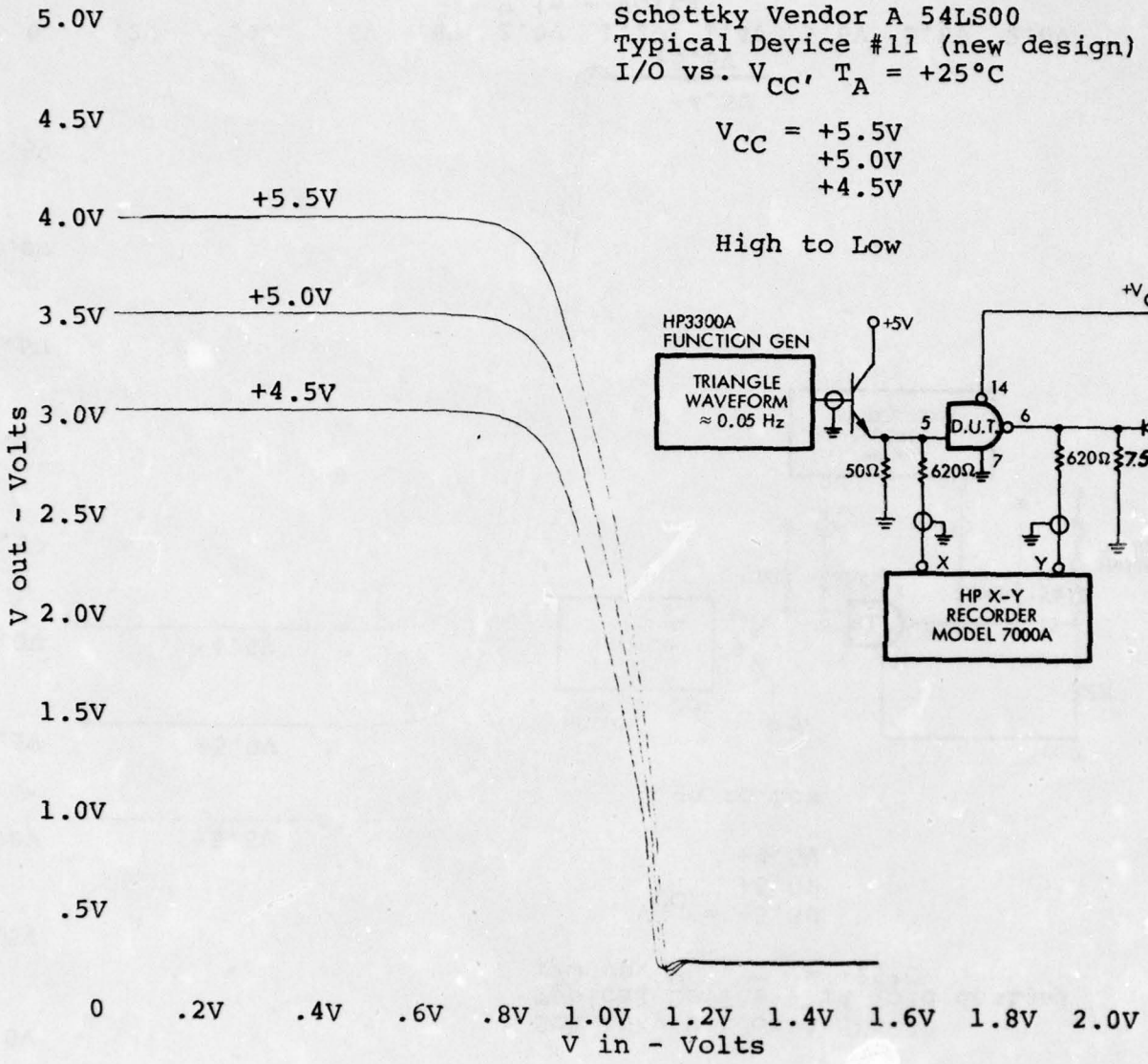


Schottky Vendor A 54LS00
Typical Device #11 (new design)
I/O vs. V_{CC}, T_A = +25°C

V_{CC} = +5.5V
+5.0V
+4.5V

High to Low

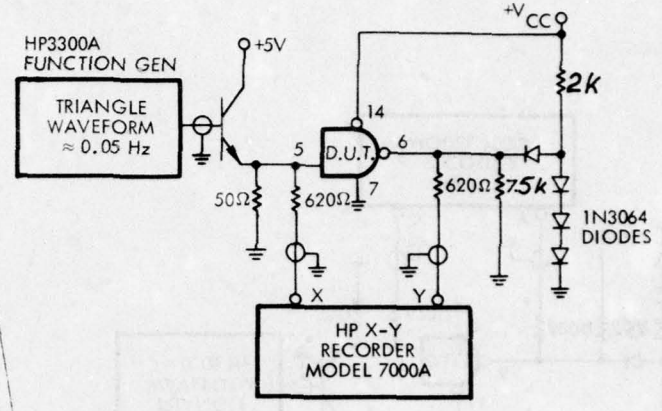


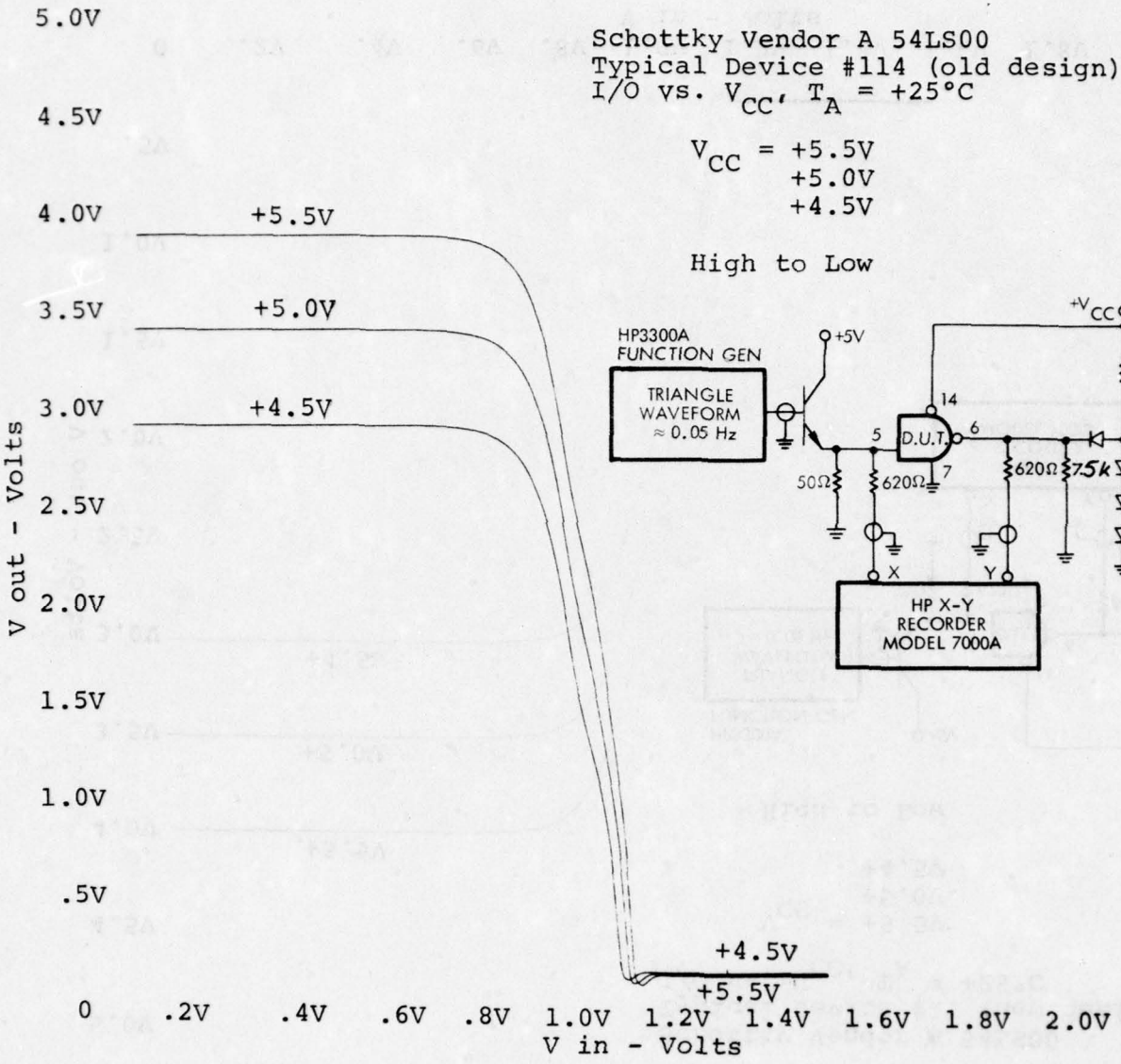


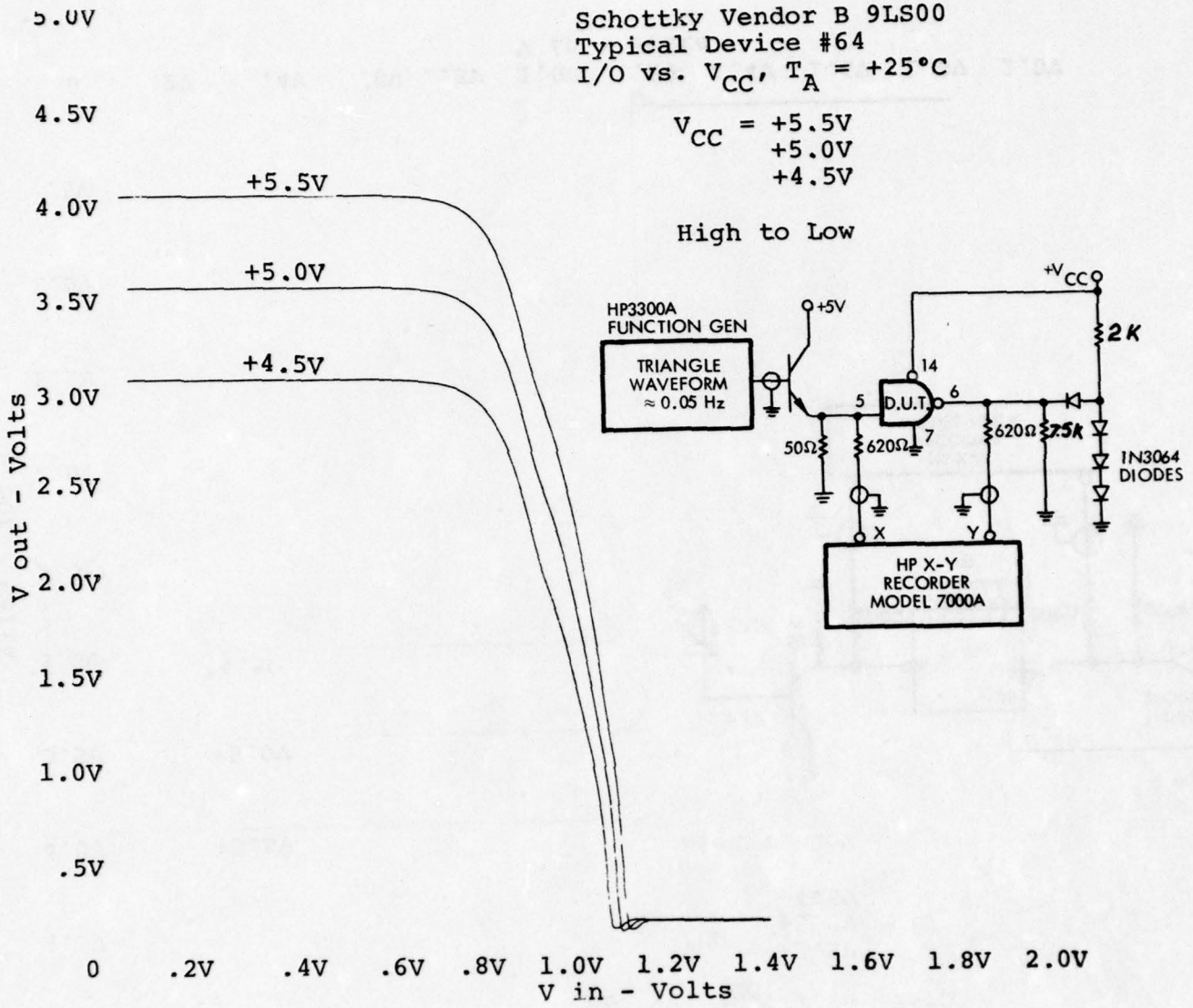
Schottky Vendor A 54LS00
Typical Device #114 (old design)
I/O vs. V_{CC}, T_A = +25°C

V_{CC} = +5.5V
+5.0V
+4.5V

High to Low



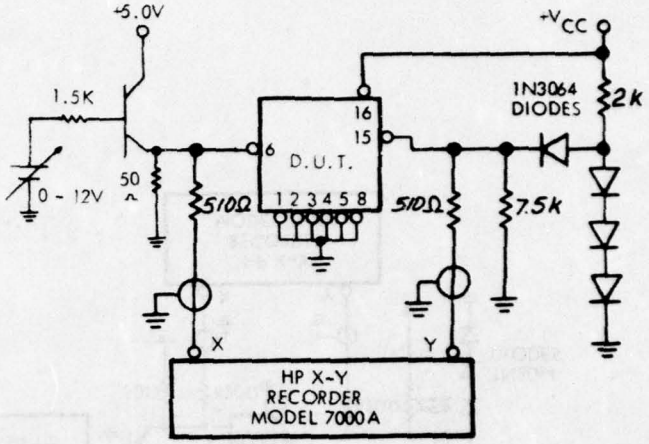


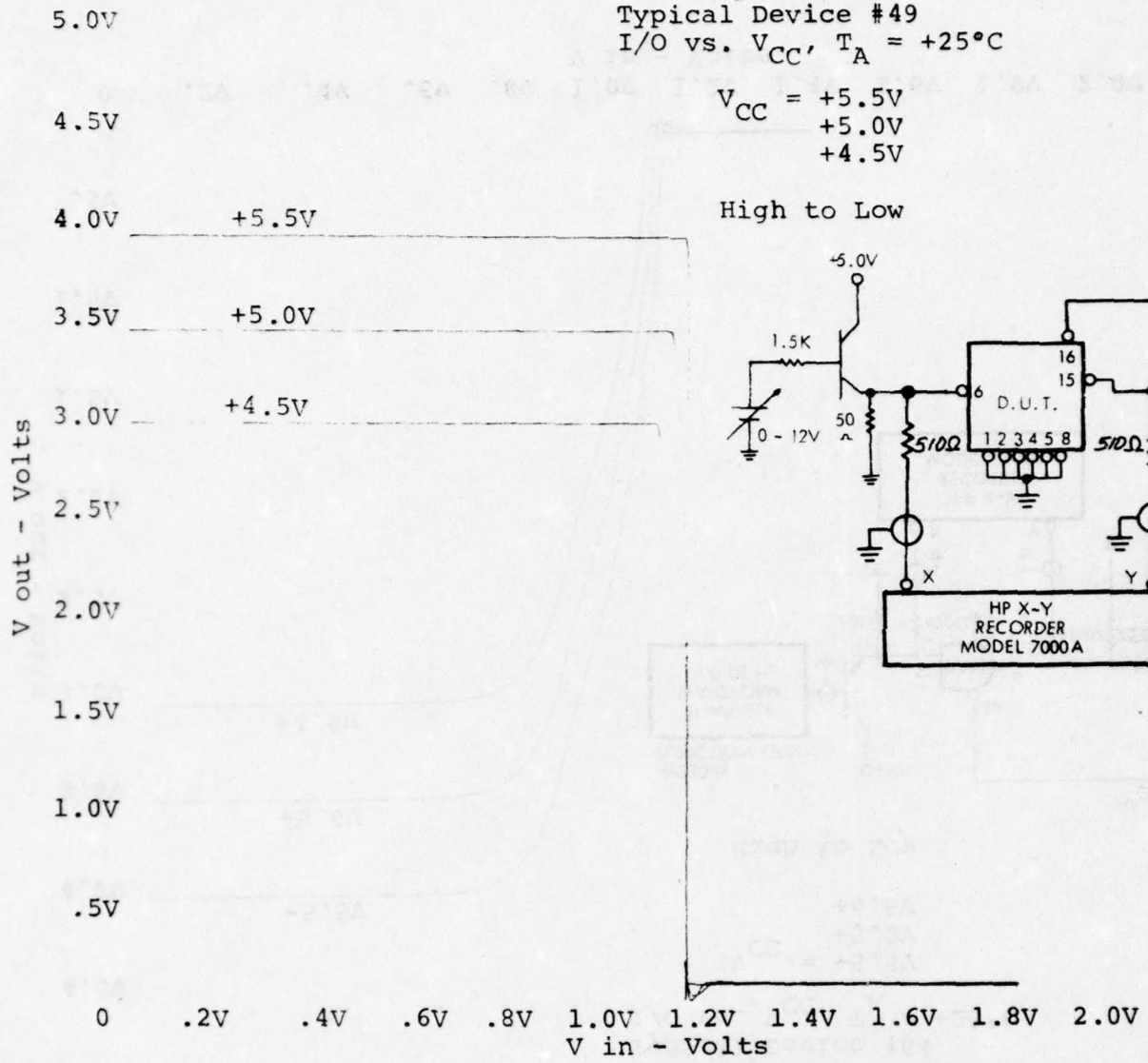

Schottky Vendor B 9LS00
Typical Device #64
I/O vs. V_{CC}, T_A = +25°C
V_{CC} = +5.5V
+5.0V
+4.5V
High to Low
+5.5V
+5.0V
+4.5V
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
.5V
V out - Volts
0
.2V
.4V
.6V
.8V
1.0V
1.2V
1.4V
1.6V
1.8V
2.0V
V in - Volts
HP3300A
FUNCTION GEN
TRIANGLE
WAVEFORM
≈ 0.05 Hz
+5V
+VCC
2K
14
5
D.U.T
6
7
50Ω
620Ω
620Ω
2.5K
1N3064
DIODES
X
Y
HP X-Y
RECORDER
MODEL 7000A

Schottky Vendor A 54LS138
Typical Device #49
I/O vs. V_{CC}, T_A = +25°C

V_{CC} = +5.5V
+5.0V
+4.5V

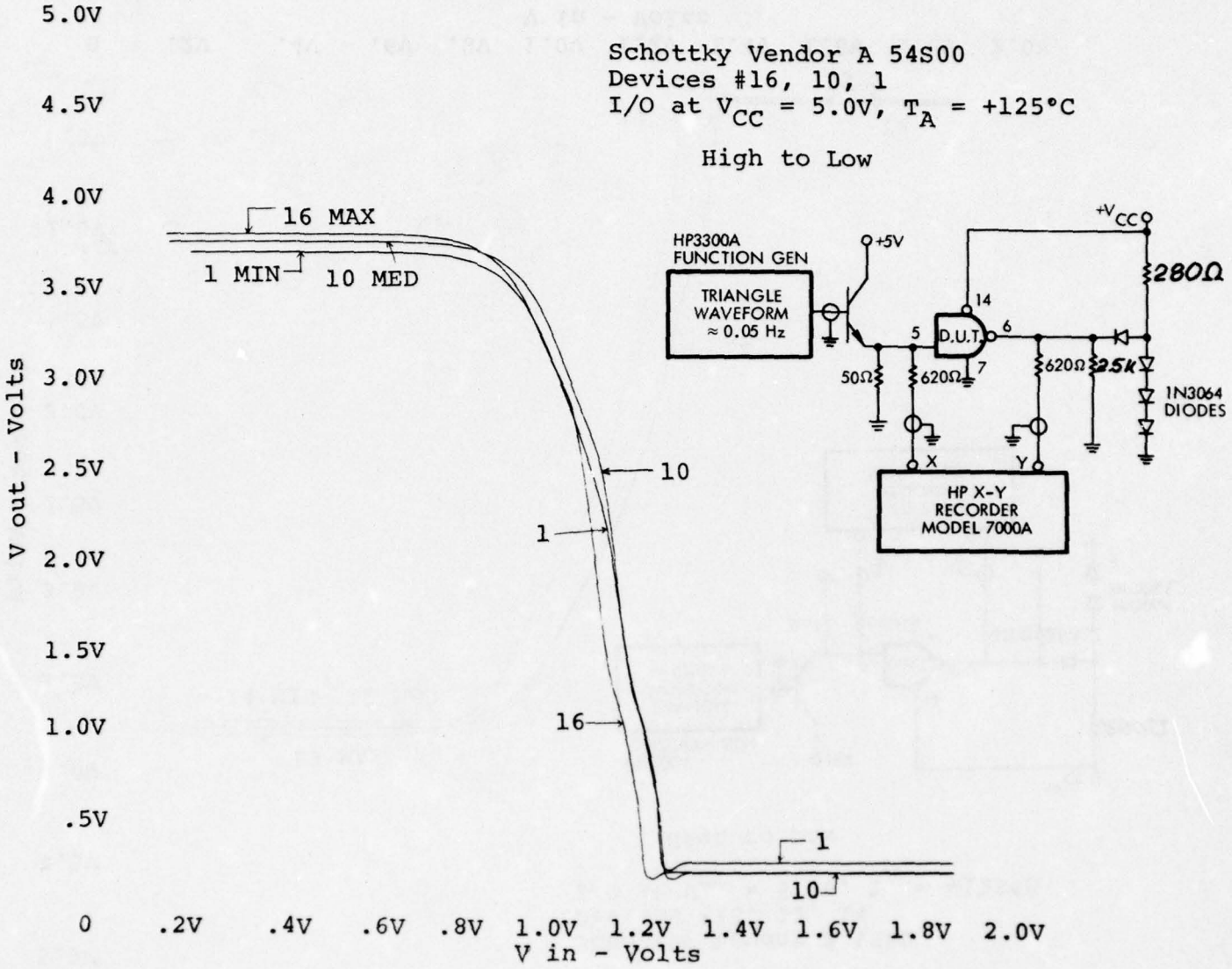
High to Low





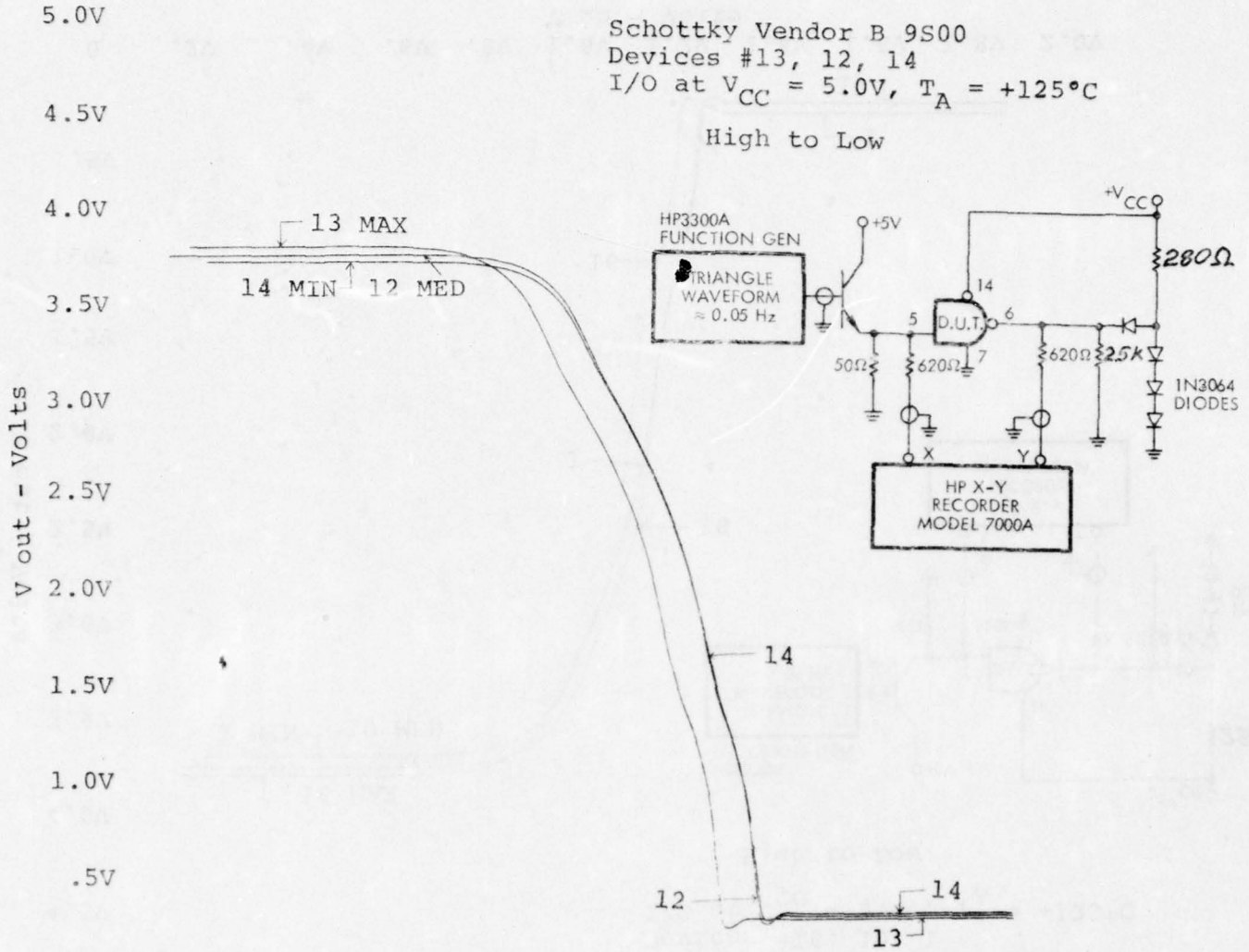
Schottky Vendor A 54S00
Devices #16, 10, 1
I/O at V_{CC} = 5.0V, T_A = +125°C

High to Low



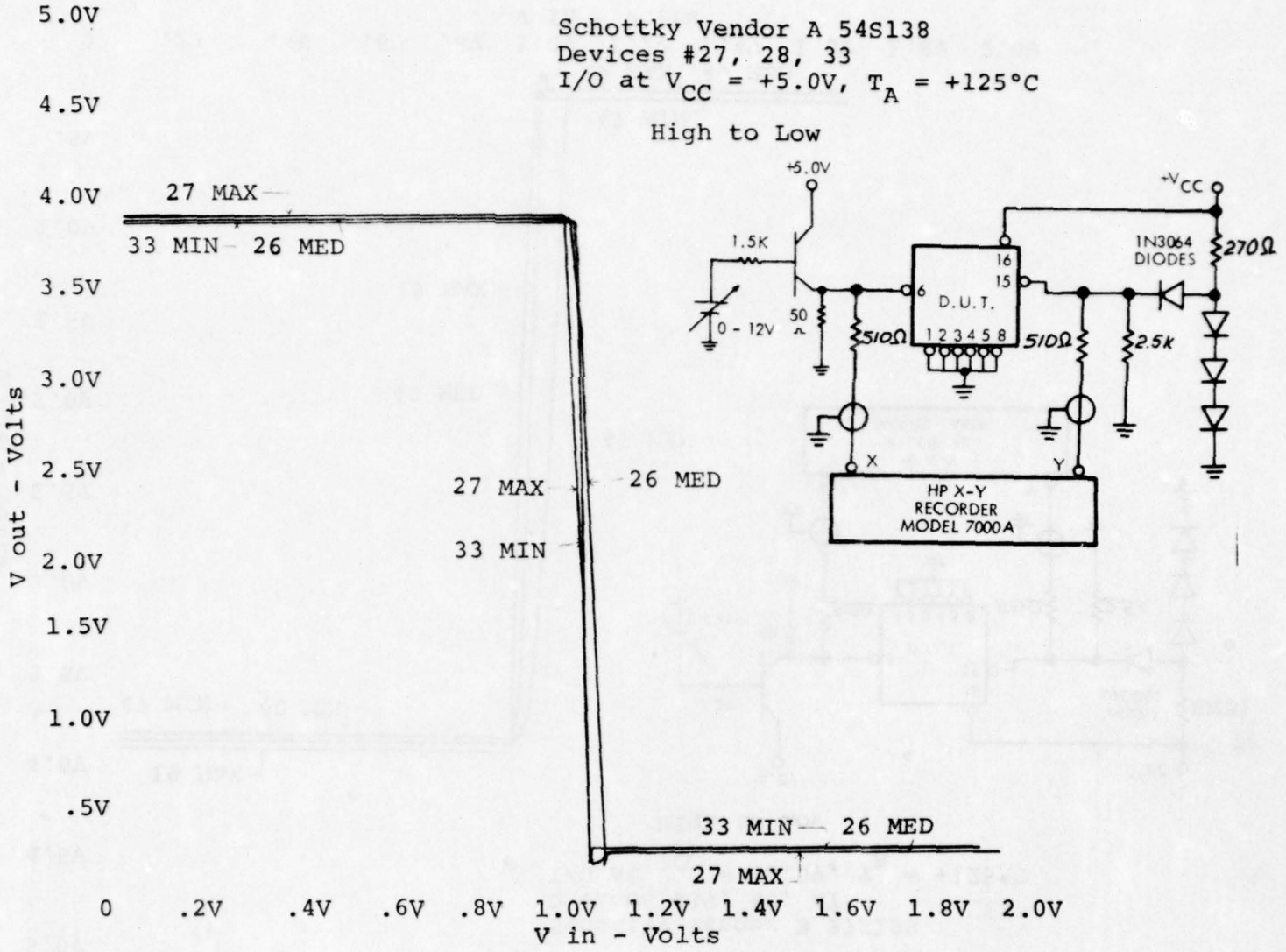
Schottky Vendor B 9S00
Devices #13, 12, 14
I/O at V_{CC} = 5.0V, T_A = +125°C

High to Low



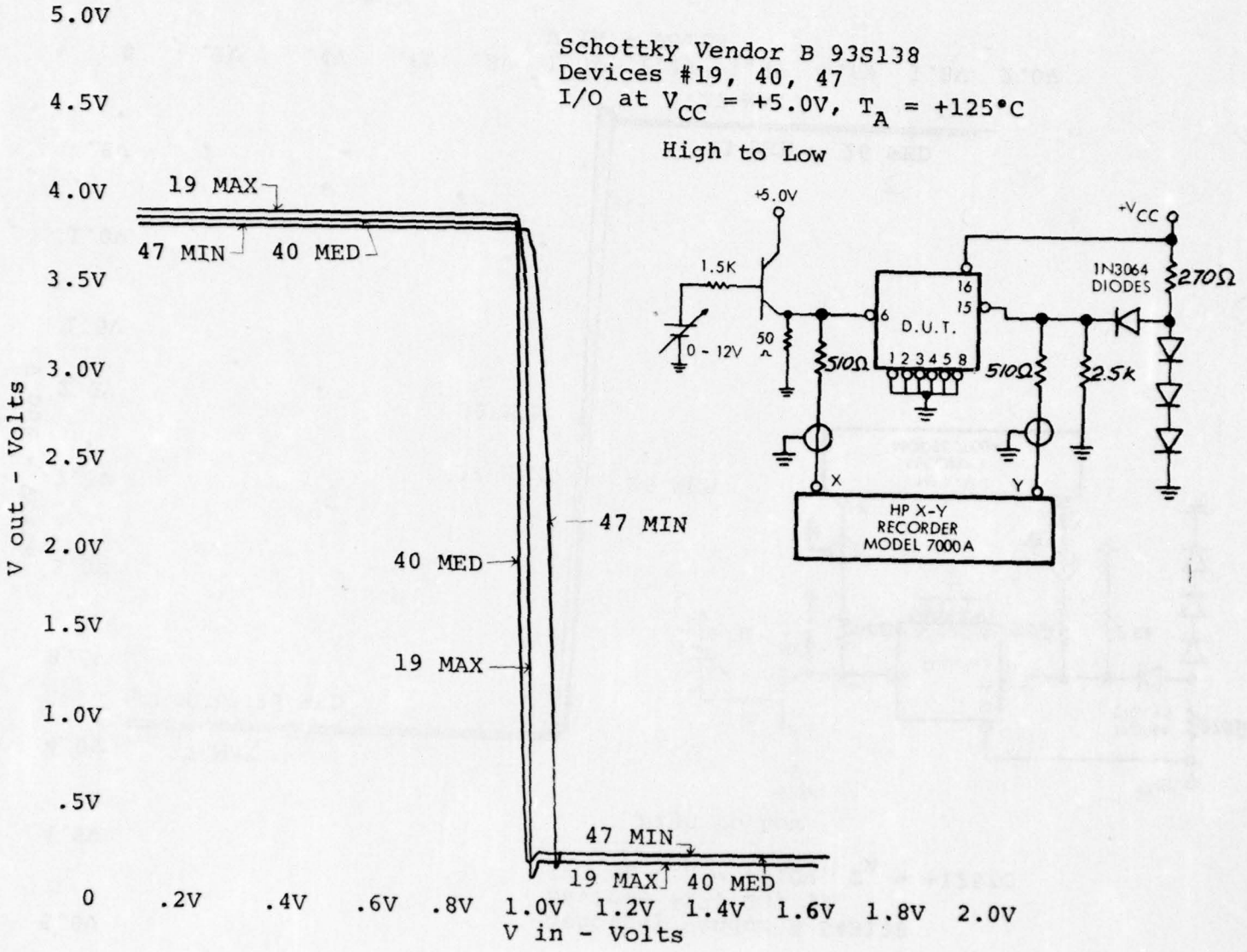
Schottky Vendor A 54S138
Devices #27, 28, 33
I/O at V_{CC} = +5.0V, T_A = +125°C

High to Low



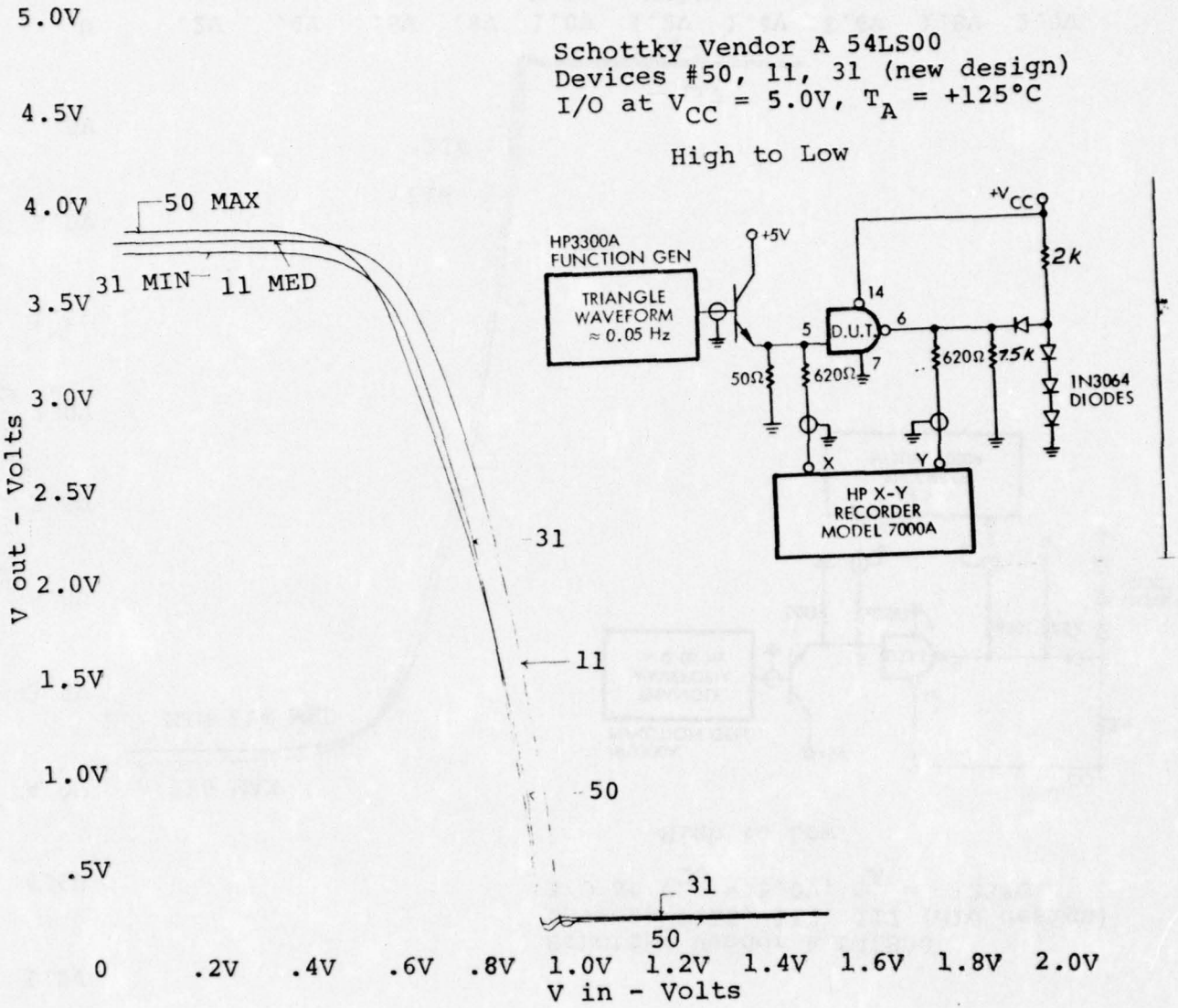
Schottky Vendor B 93S138
Devices #19, 40, 47
I/O at V_{CC} = +5.0V, T_A = +125°C

High to Low



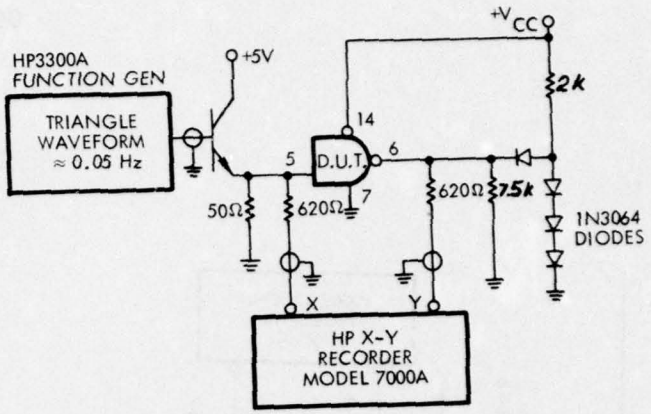
Schottky Vendor A 54LS00
Devices #50, 11, 31 (new design)
I/O at V_{CC} = 5.0V, T_A = +125°C

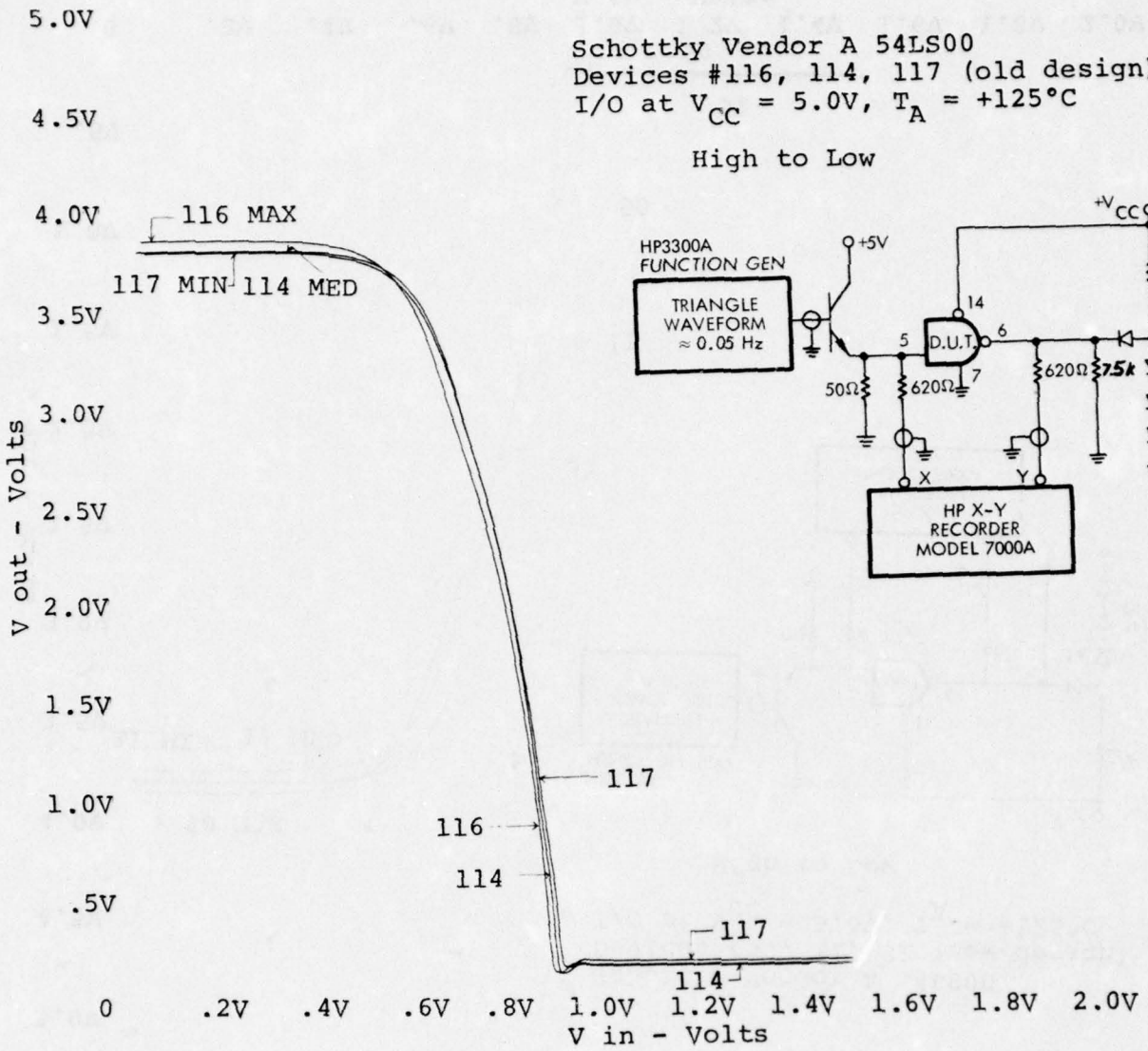
High to Low



Schottky Vendor A 54LS00
Devices #116, 114, 117 (old design)
I/O at V_{CC} = 5.0V, T_A = +125°C

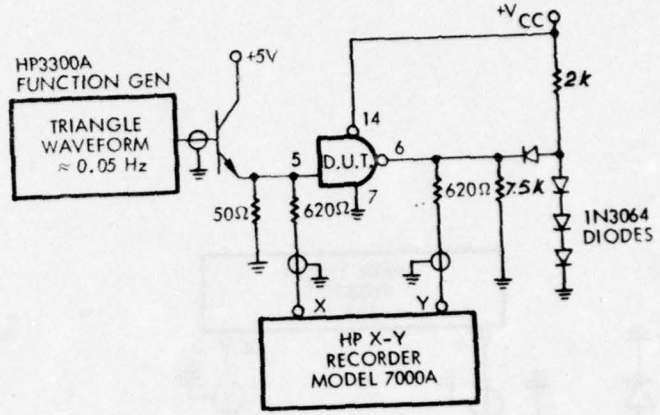
High to Low

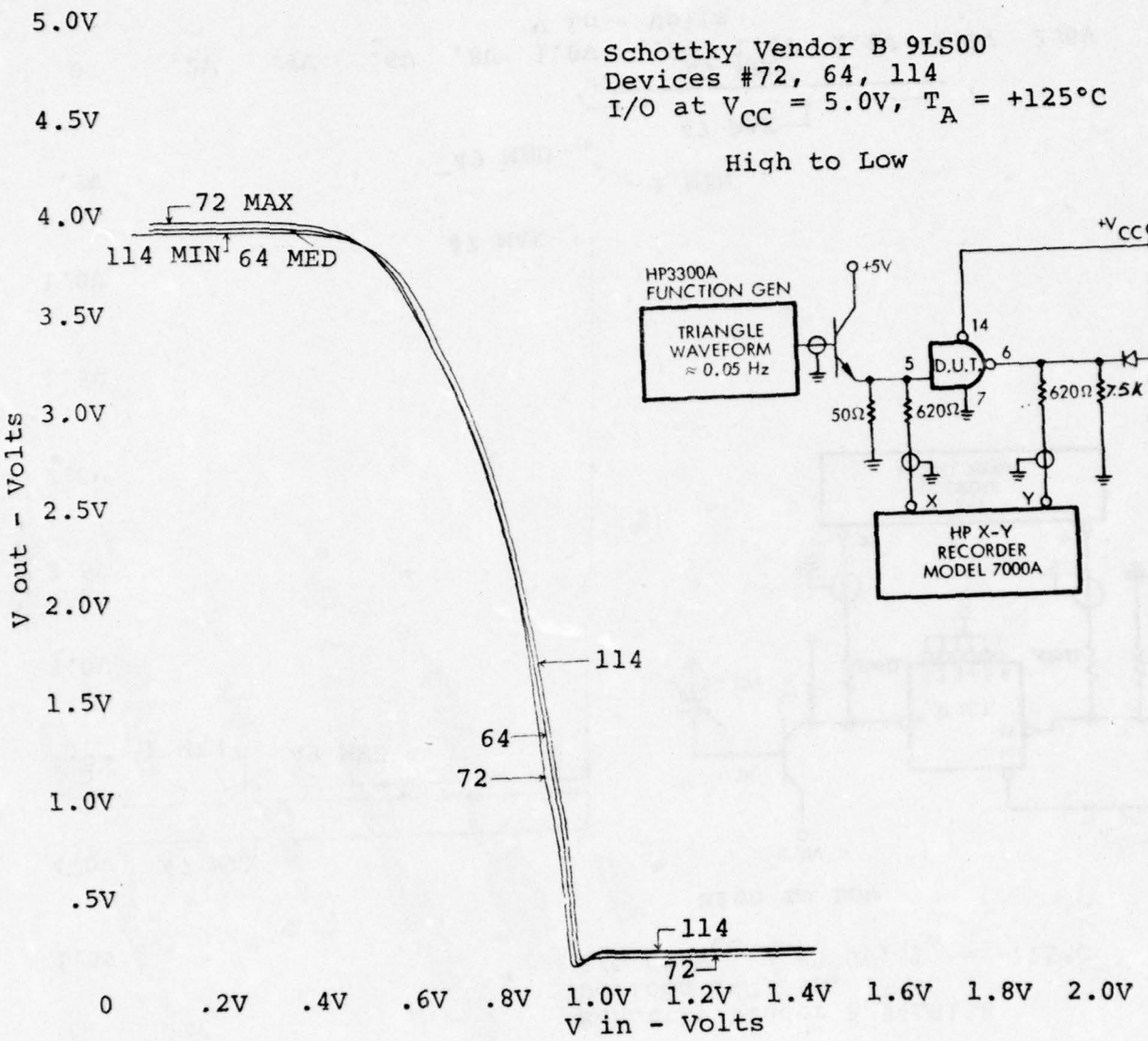




Schottky Vendor B 9LS00
Devices #72, 64, 114
I/O at V_{CC} = 5.0V, T_A = +125°C

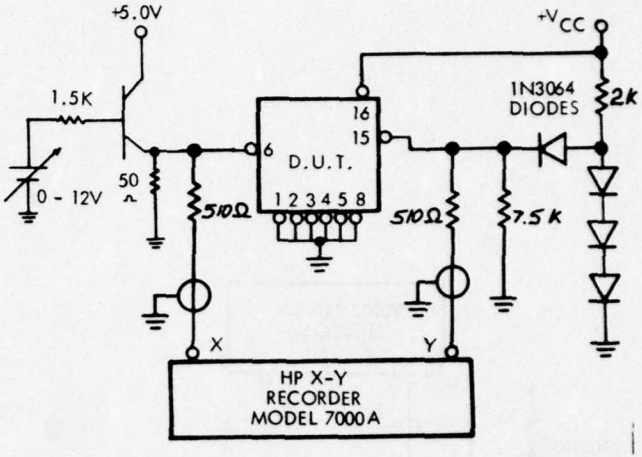
High to Low

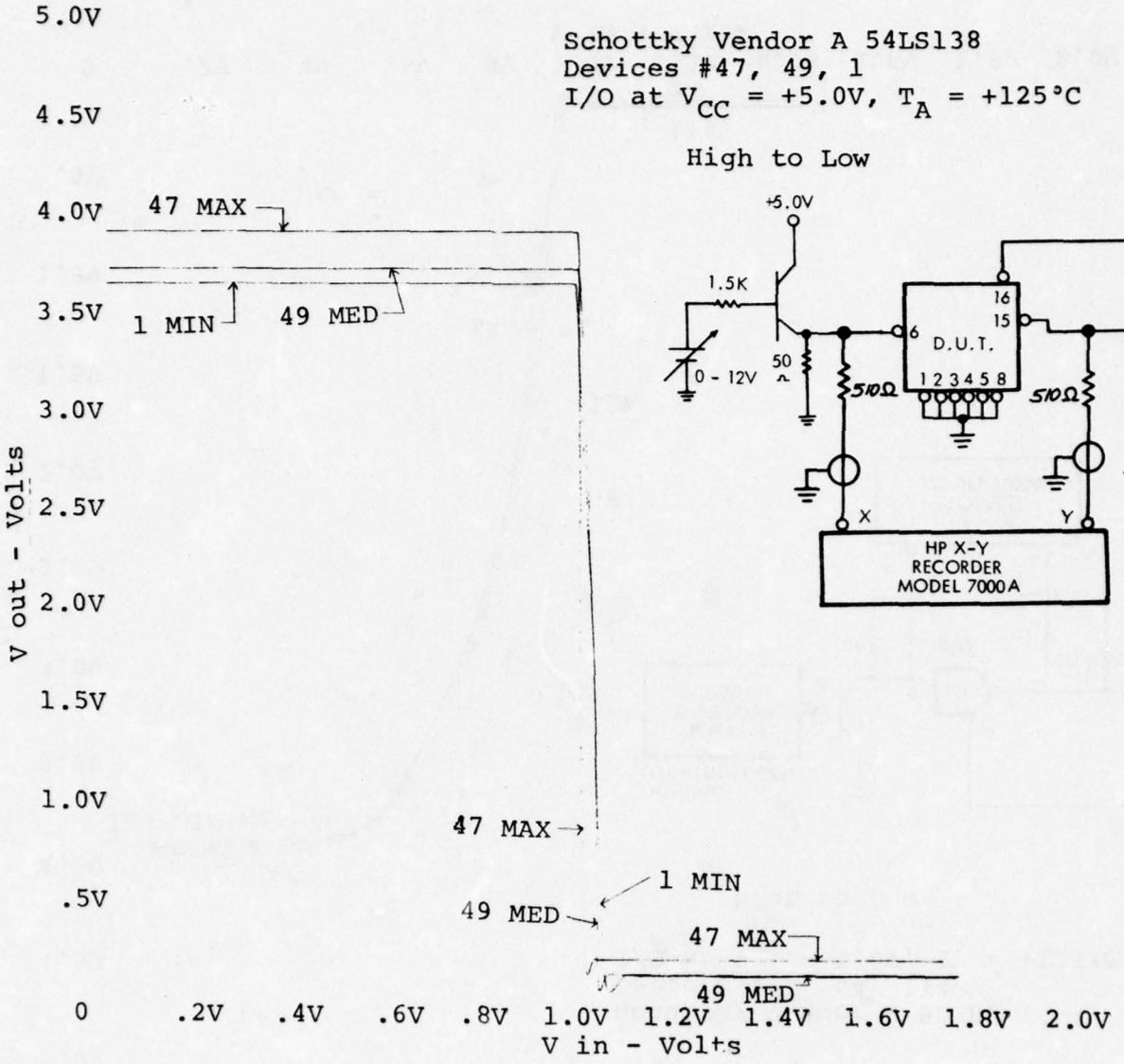




Schottky Vendor A 54LS138
Devices #47, 49, 1
I/O at V_{CC} = +5.0V, T_A = +125°C

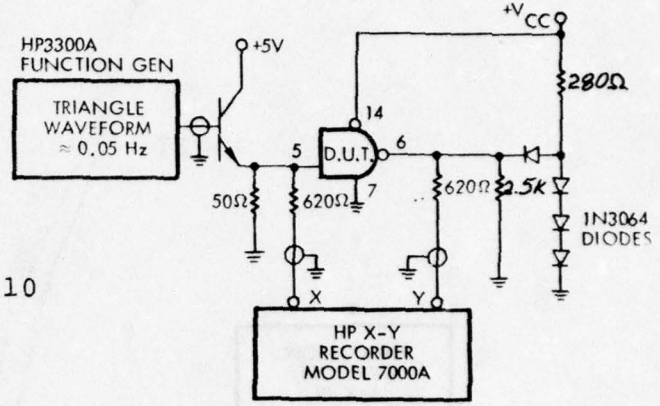
High to Low

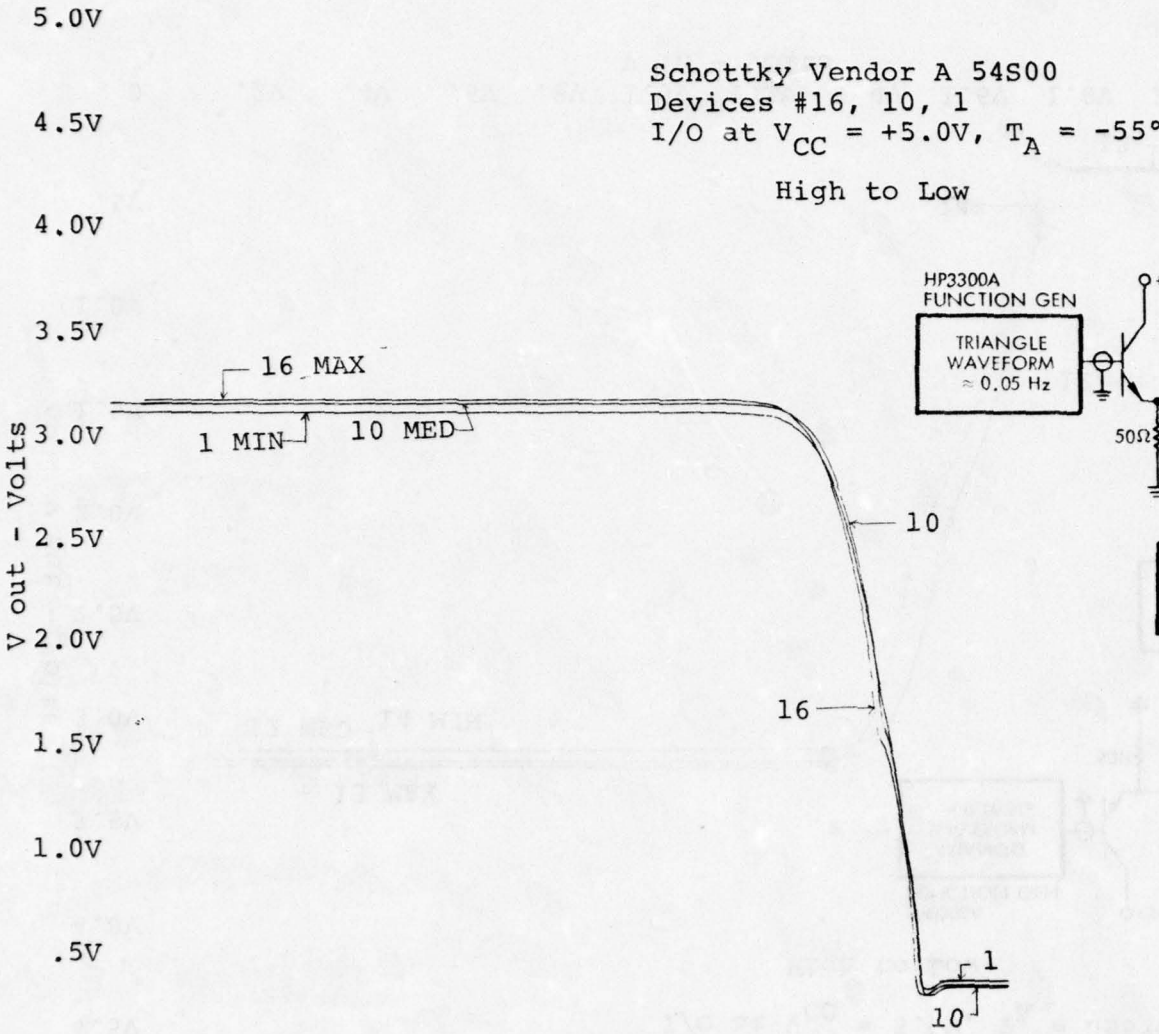




Schottky Vendor A 54S00
Devices #16, 10, 1
I/O at V_{CC} = +5.0V, T_A = -55°C

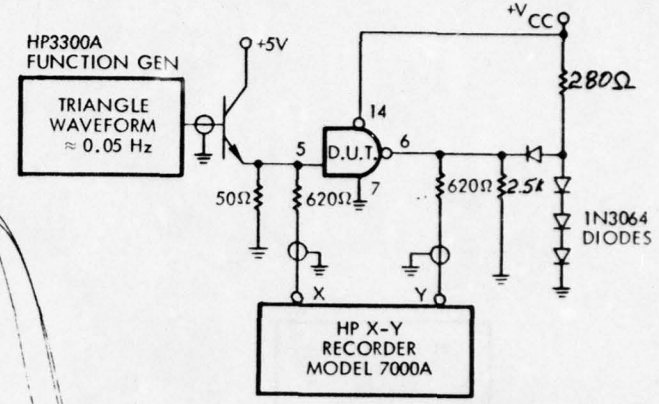
High to Low

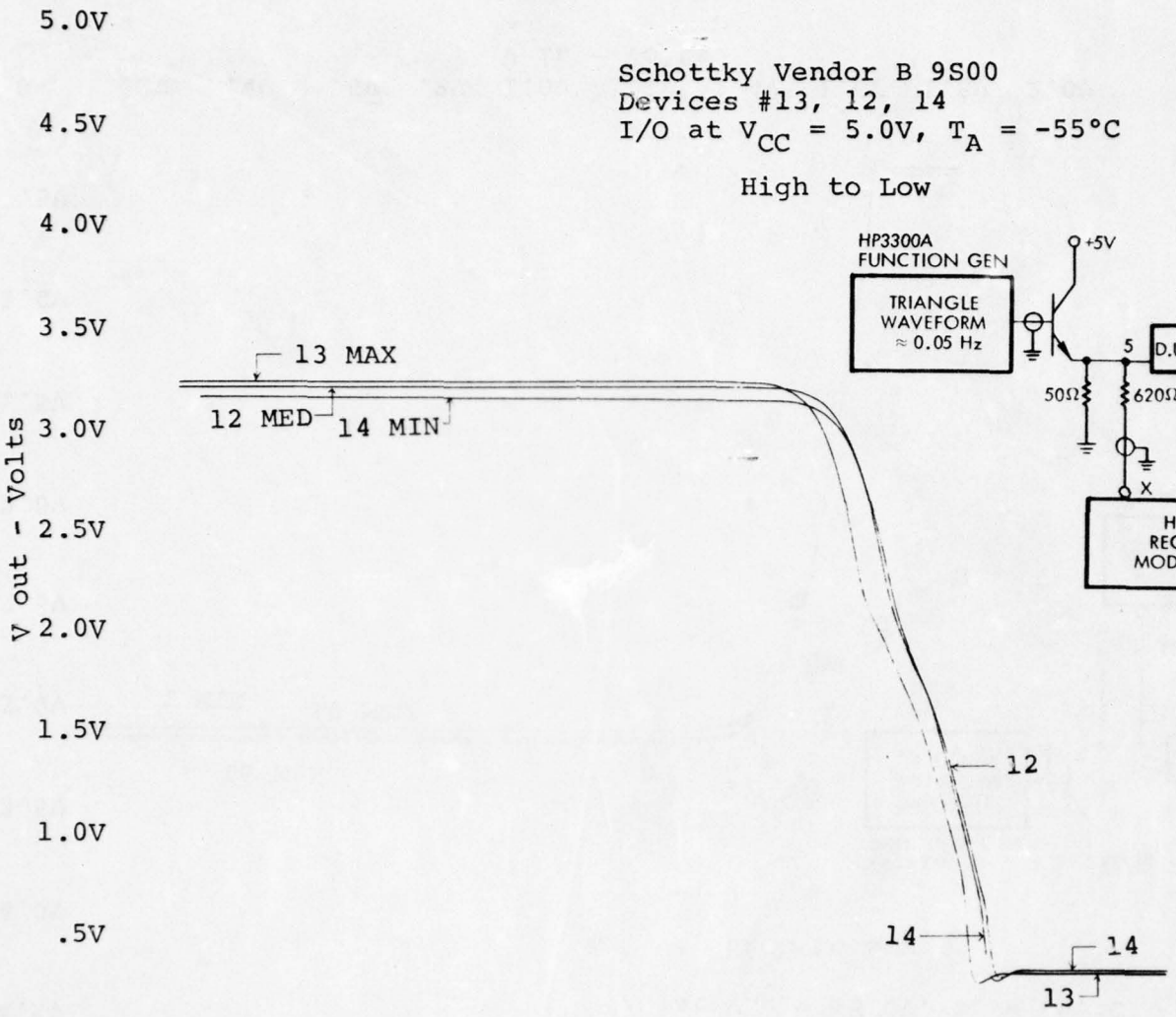




Schottky Vendor B 9S00
Devices #13, 12, 14
I/O at V_{CC} = 5.0V, T_A = -55°C

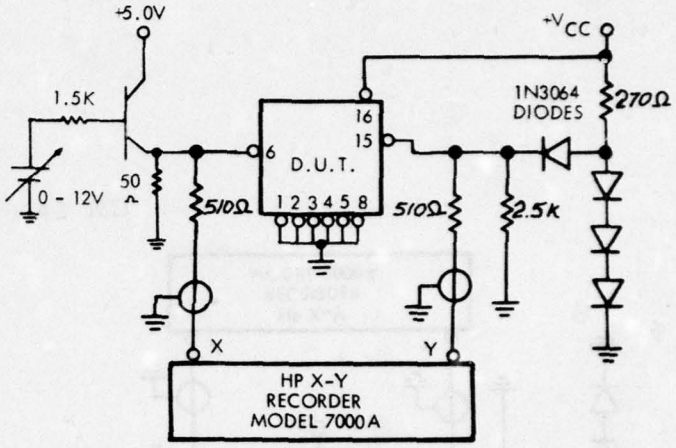
High to Low

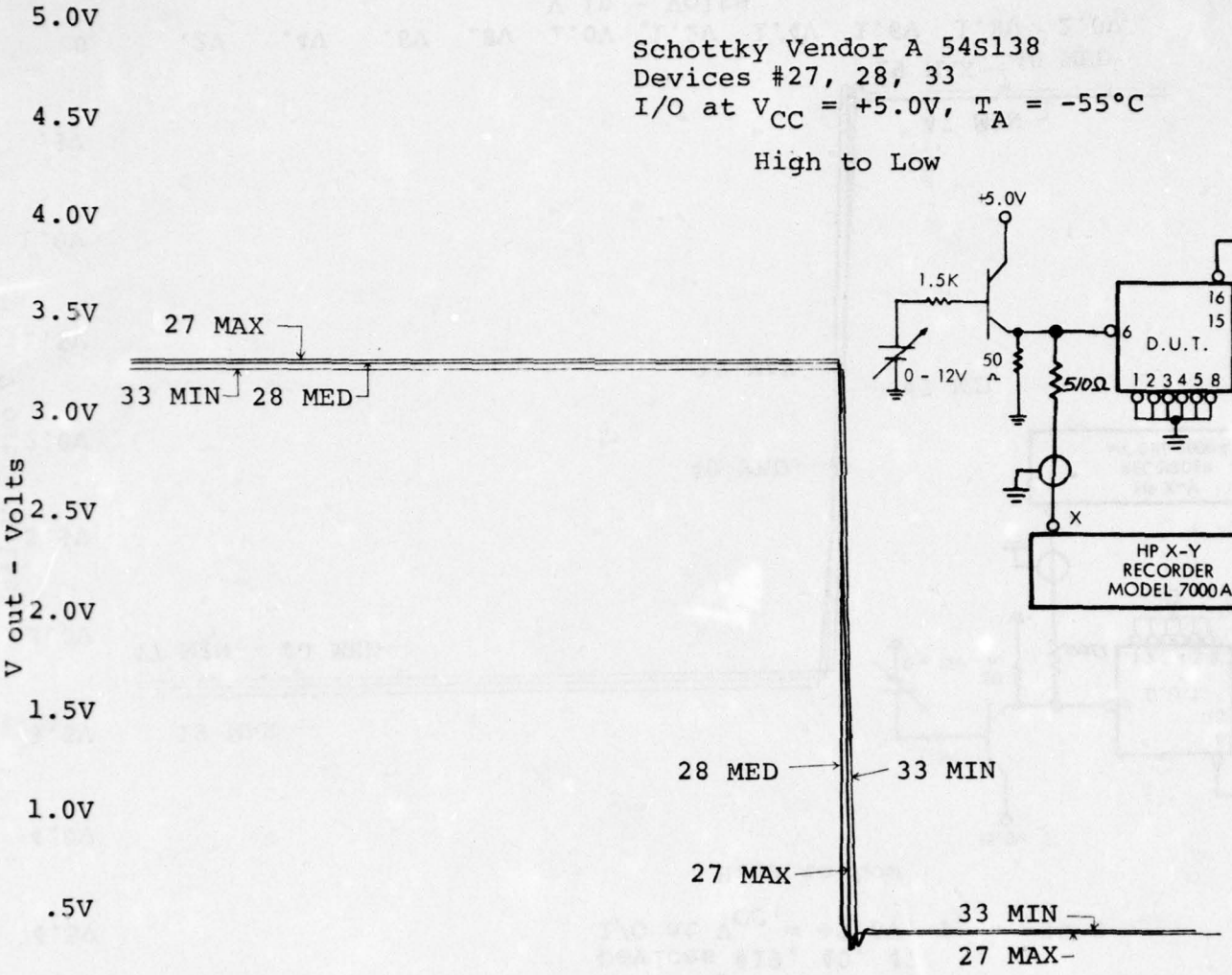




Schottky Vendor A 54S138
Devices #27, 28, 33
I/O at V_{CC} = +5.0V, T_A = -55°C

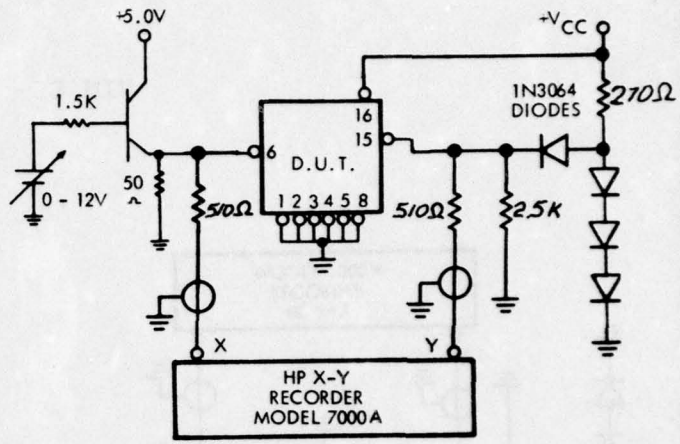
High to Low

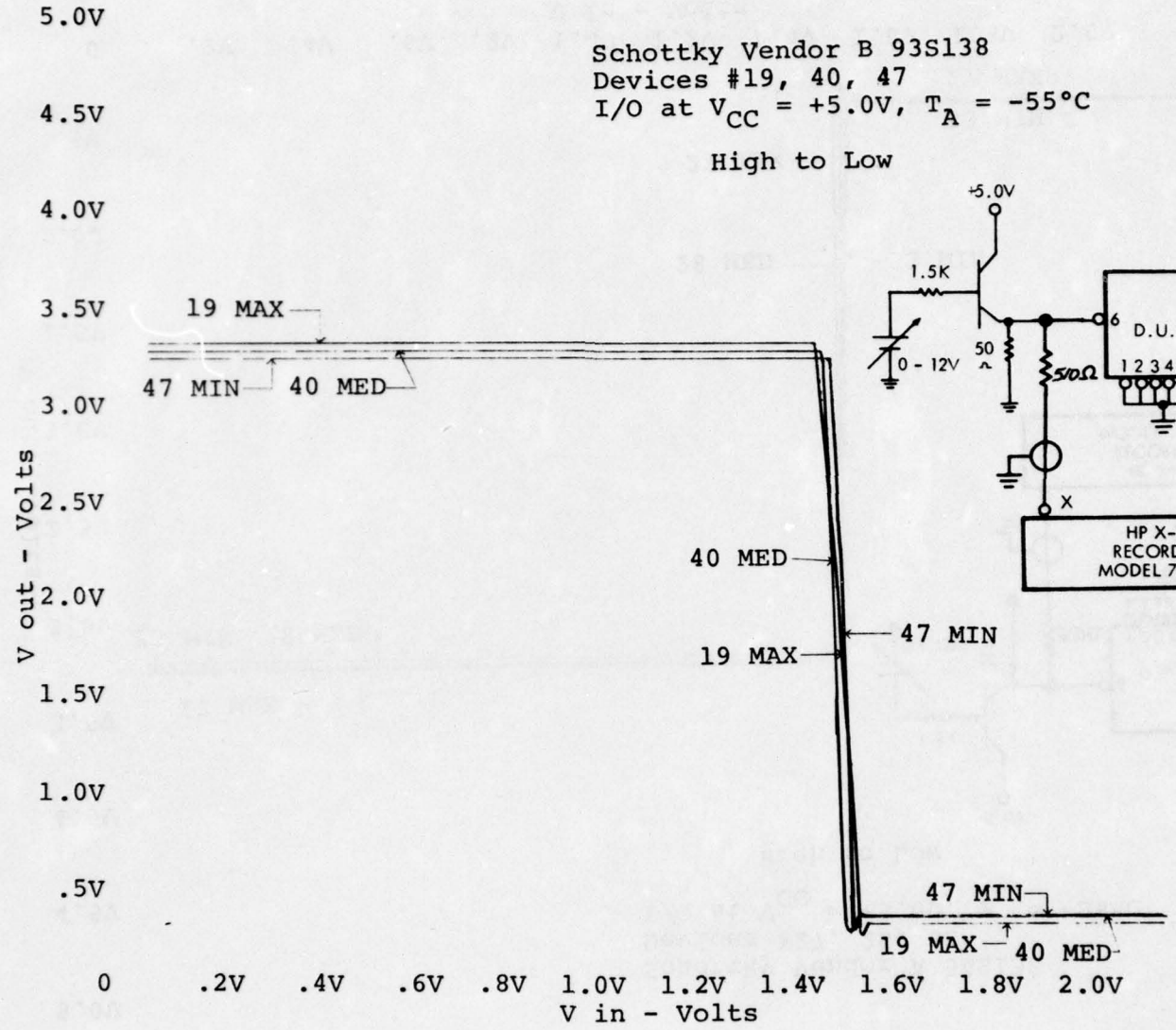




Schottky Vendor B 93S138
Devices #19, 40, 47
I/O at V_{CC} = +5.0V, T_A = -55°C

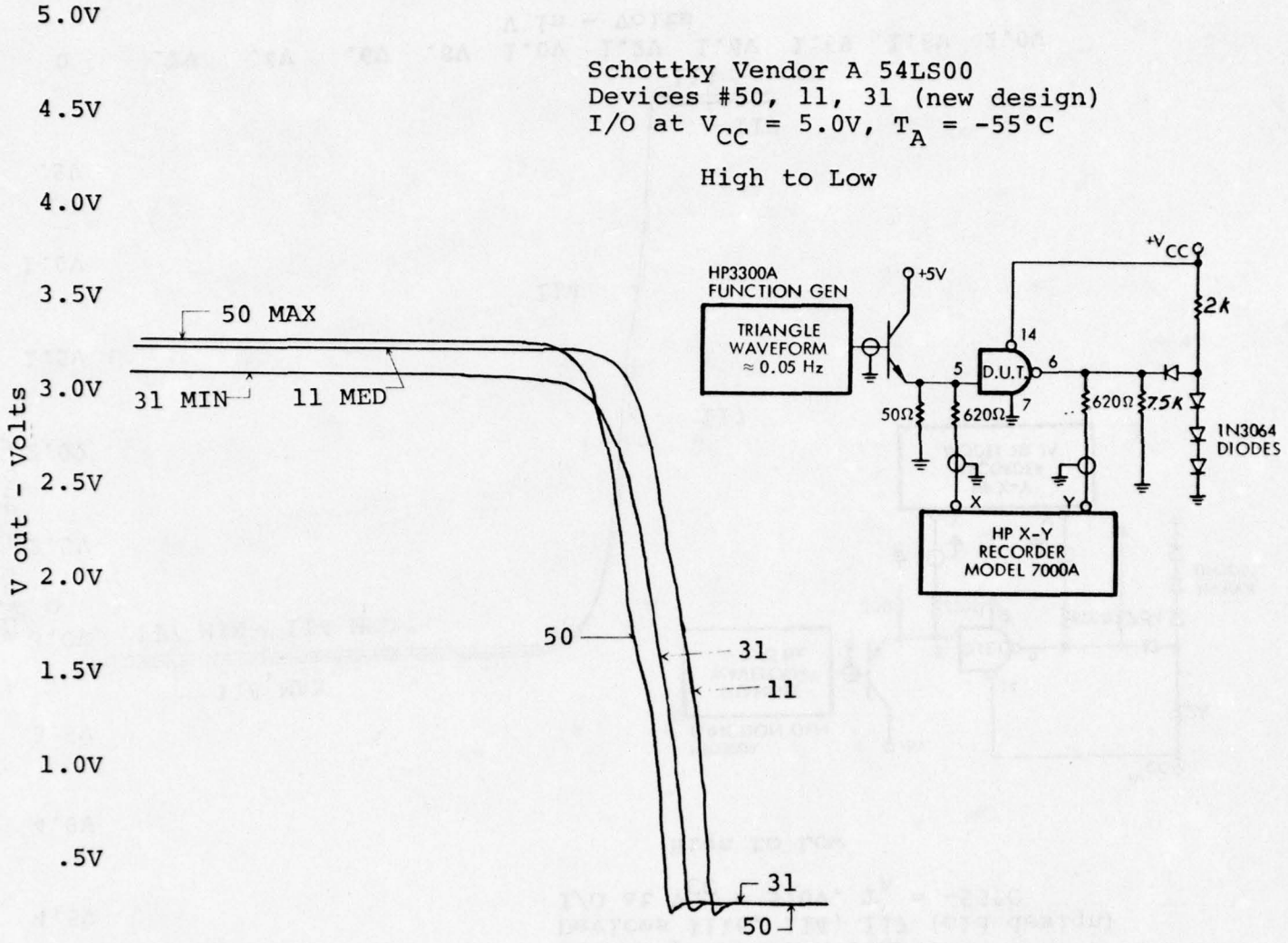
High to Low





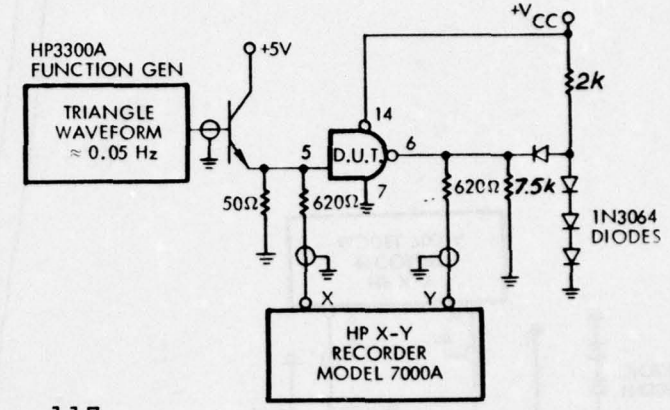
Schottky Vendor A 54LS00
Devices #50, 11, 31 (new design)
I/O at V_{CC} = 5.0V, T_A = -55°C

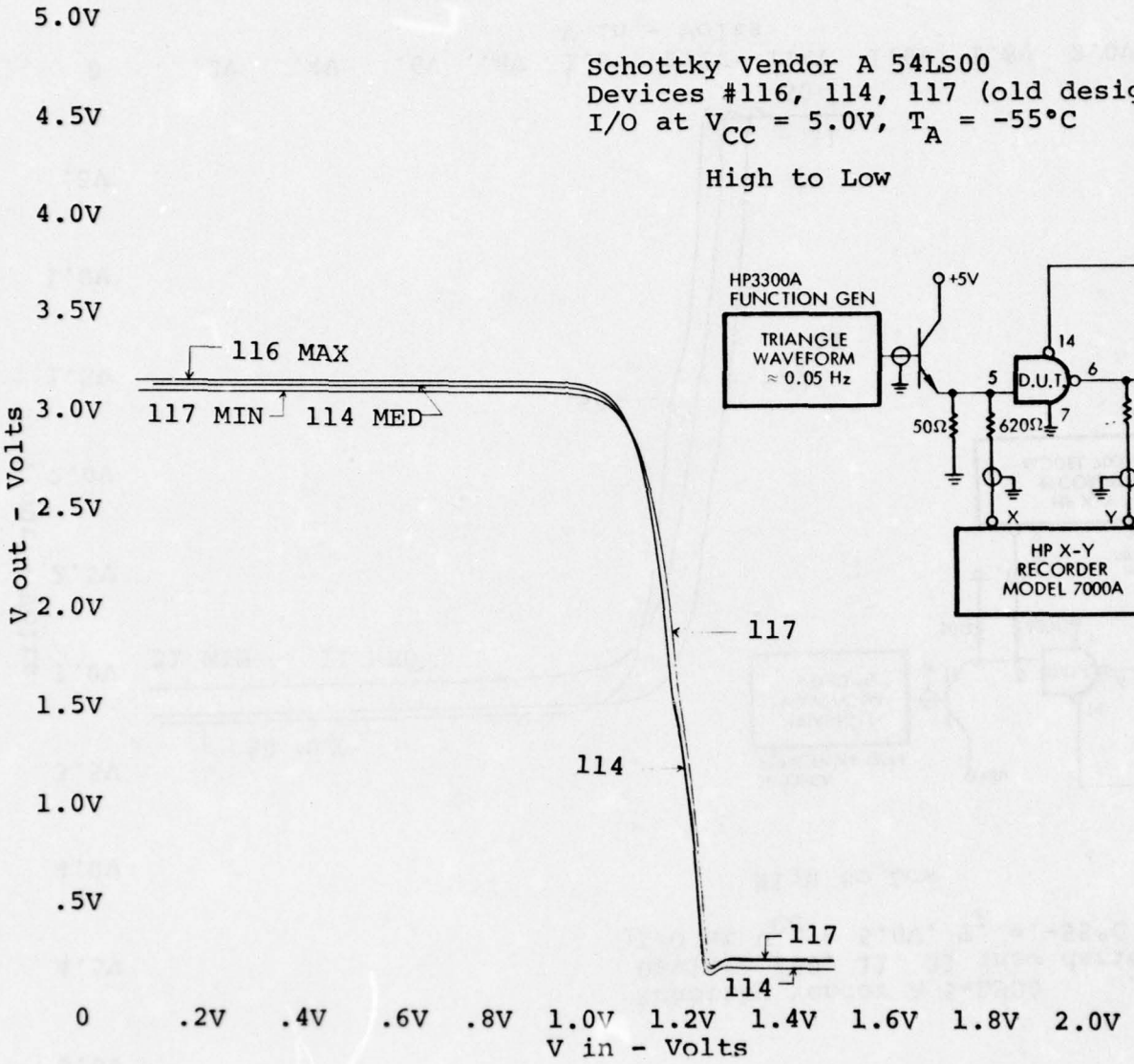
High to Low

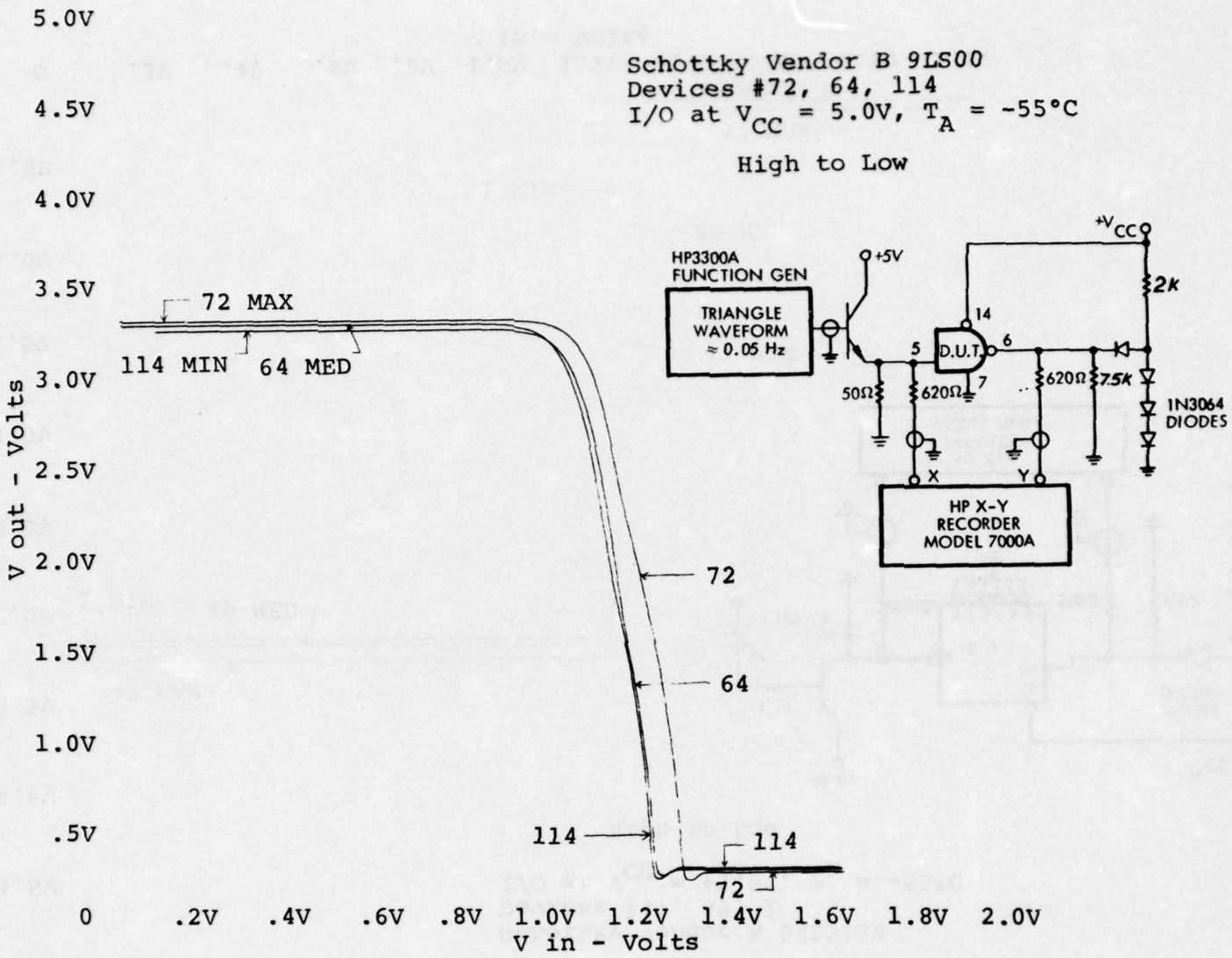


Schottky Vendor A 54LS00
Devices #116, 114, 117 (old design)
I/O at V_{CC} = 5.0V, T_A = -55°C

High to Low

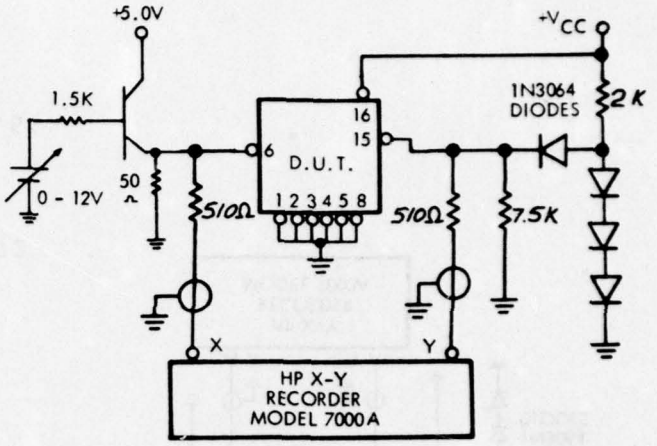


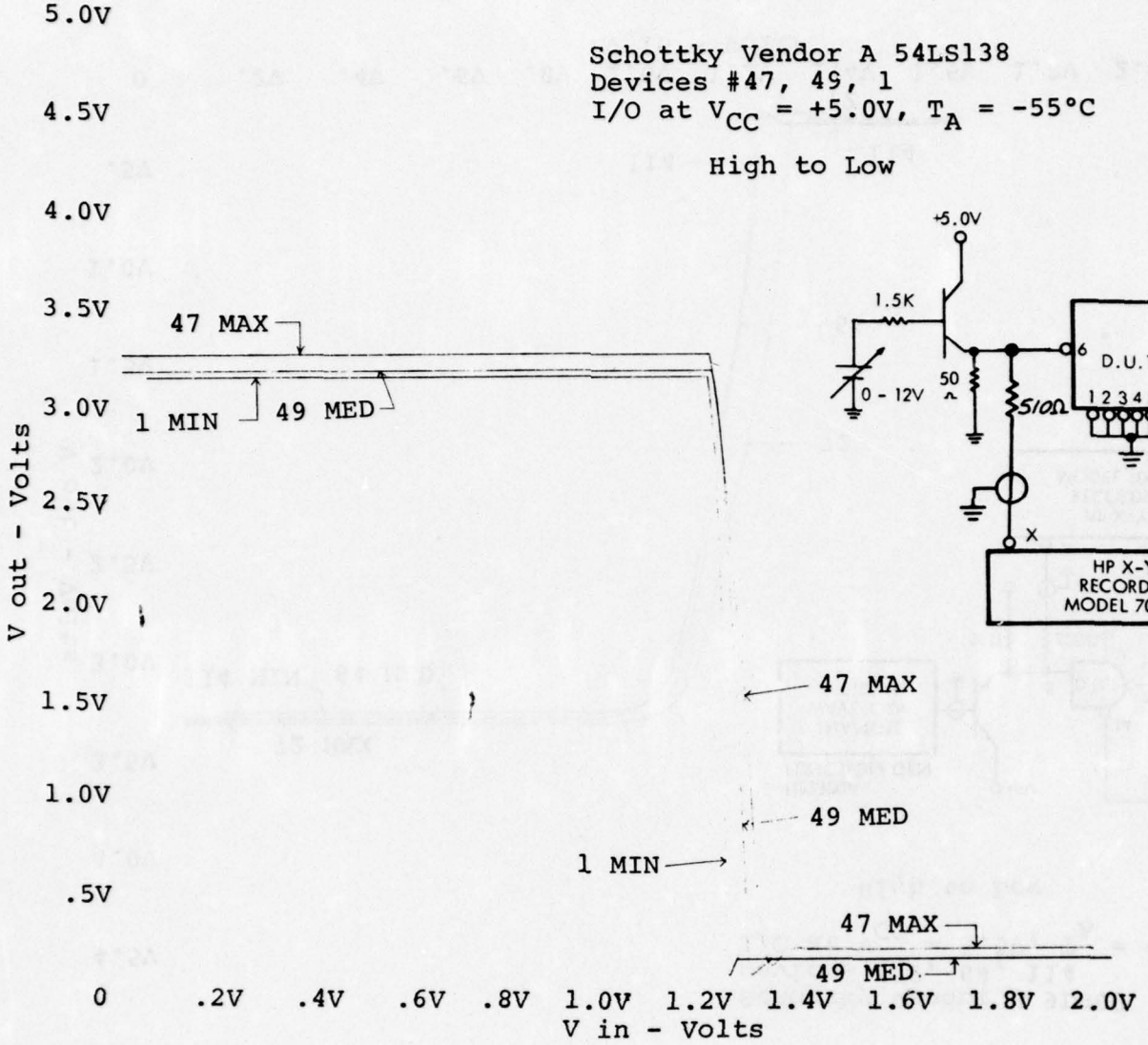



Schottky Vendor B 9LS00
Devices #72, 64, 114
I/O at V_{CC} = 5.0V, T_A = -55°C
High to Low
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
.5V
V out - Volts
72 MAX
114 MIN
64 MED
72
64
114
114
72
0
.2V
.4V
.6V
.8V
1.0V
1.2V
1.4V
1.6V
1.8V
2.0V
V in - Volts
HP3300A FUNCTION GEN
TRIANGLE WAVEFORM ≈ 0.05 Hz
+5V
+VCC
2k
14
5
D.U.T.
6
7
50Ω
620Ω
620Ω
7.5k
1N3064 DIODES
X
Y
HP X-Y RECORDER MODEL 7000A

Schottky Vendor A 54LS138
Devices #47, 49, 1
I/O at V_{CC} = +5.0V, T_A = -55°C

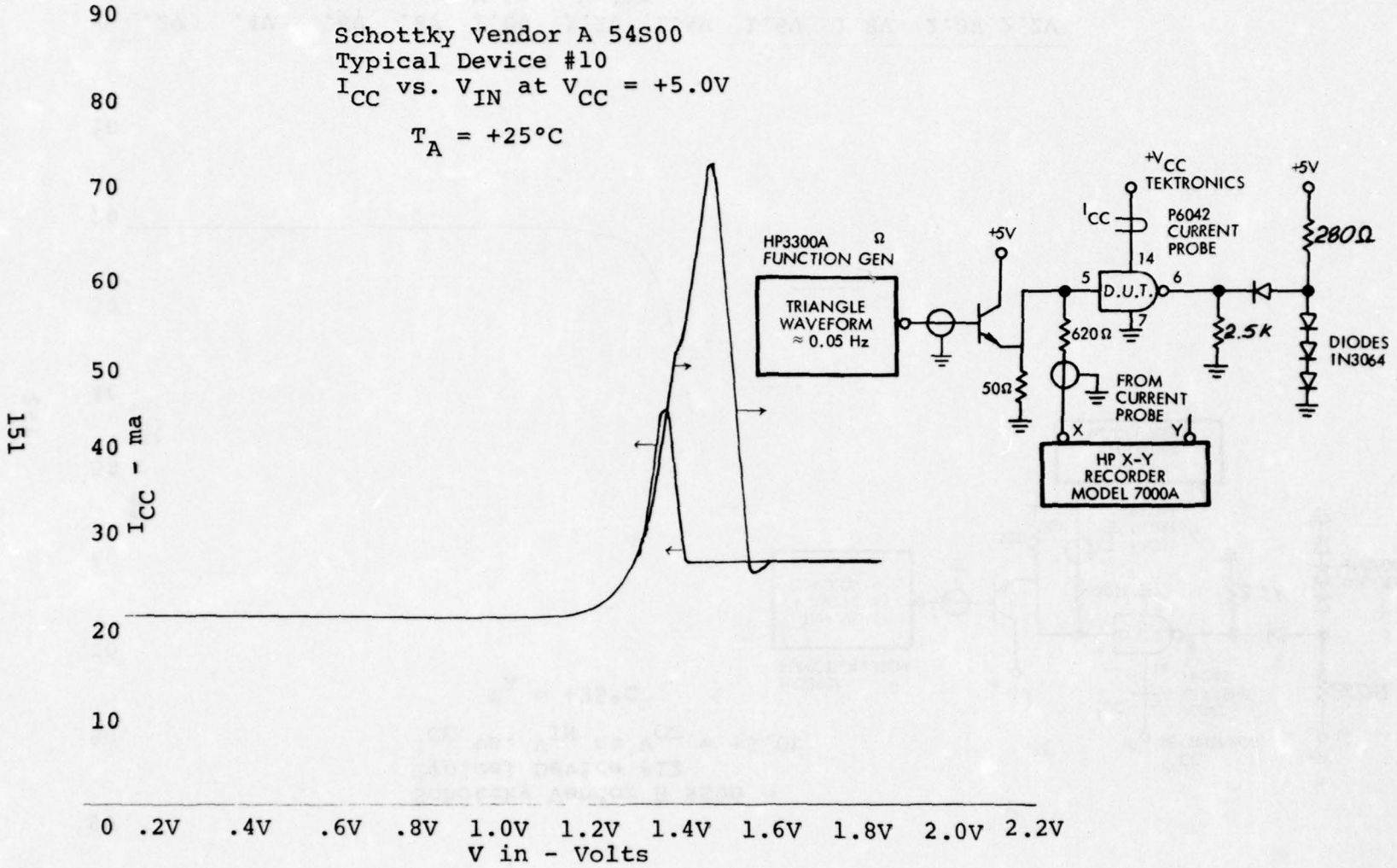
High to Low





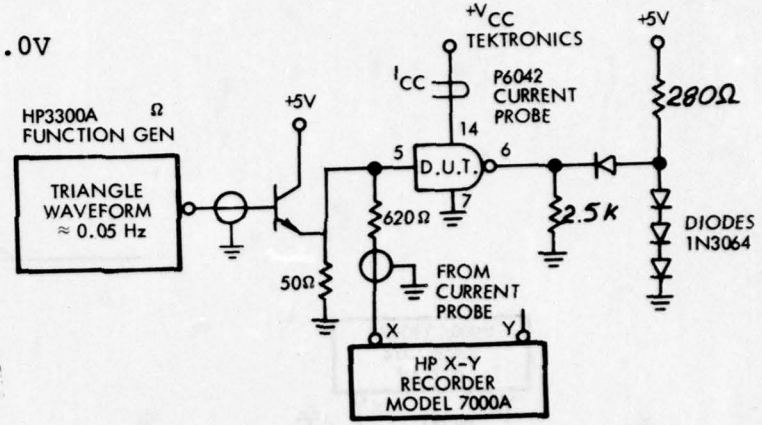
Schottky Vendor A 54S00
Typical Device #10
I_{CC} vs. V_{IN} at V_{CC} = +5.0V

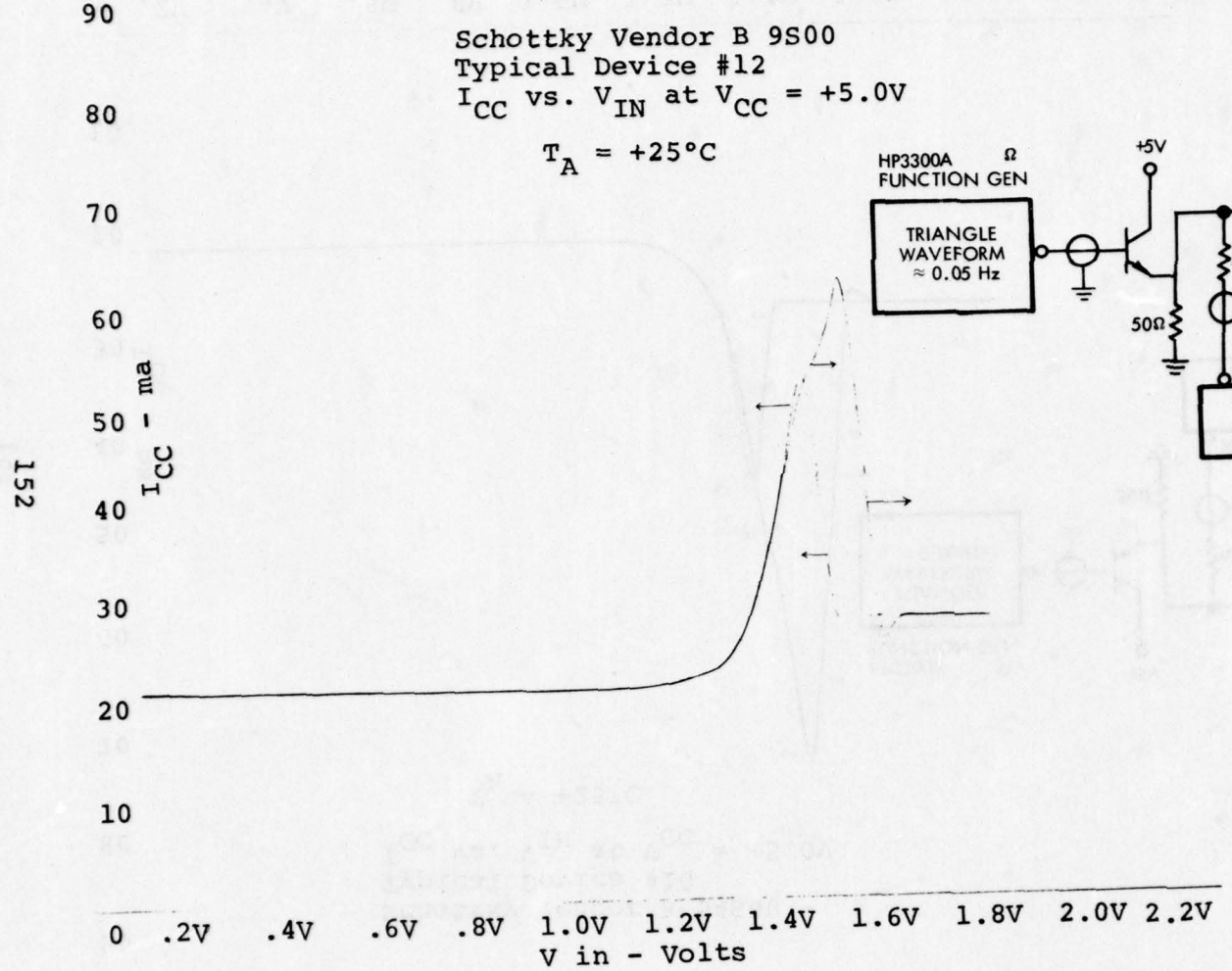
T_A = +25°C



Schottky Vendor B 9S00
Typical Device #12
I_{CC} vs. V_{IN} at V_{CC} = +5.0V

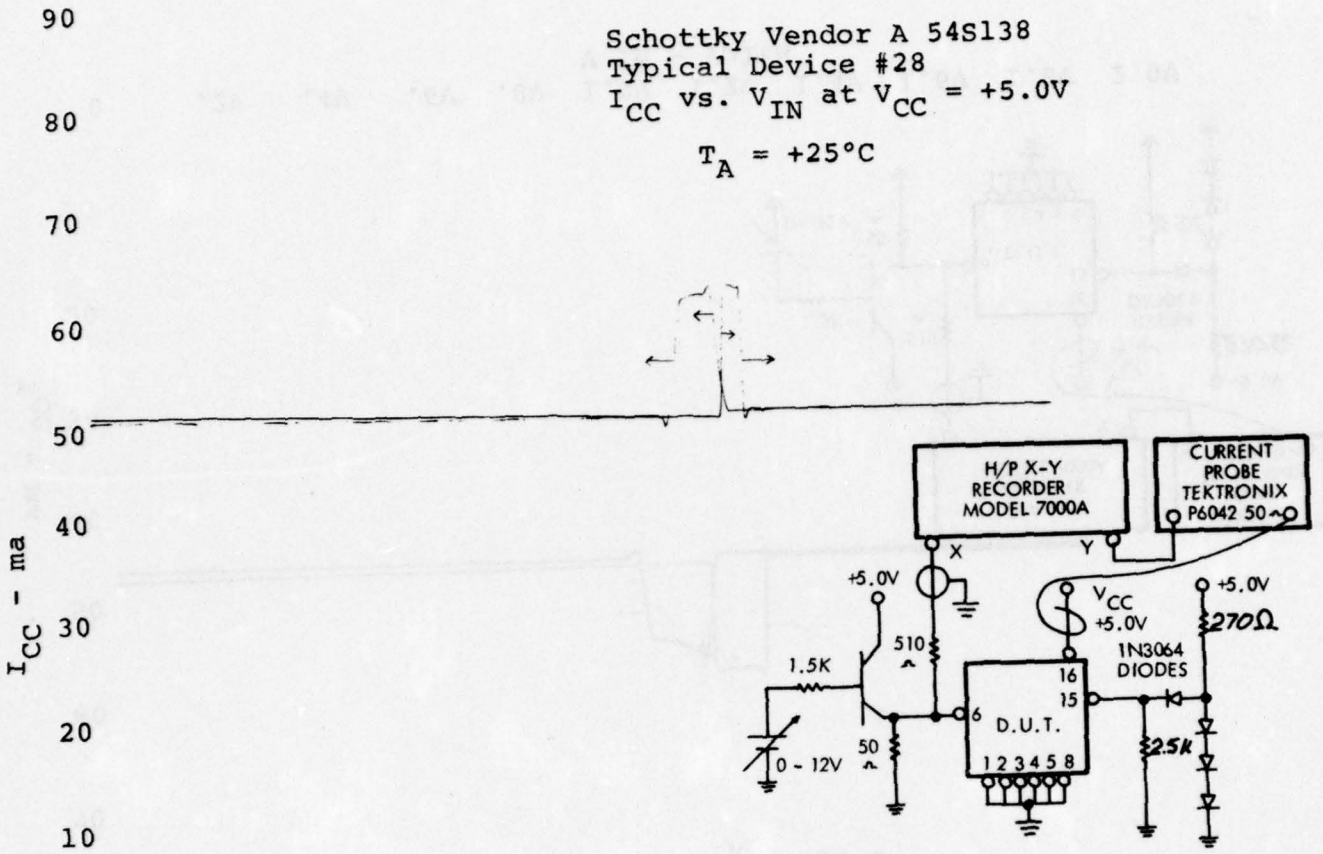
T_A = +25°C





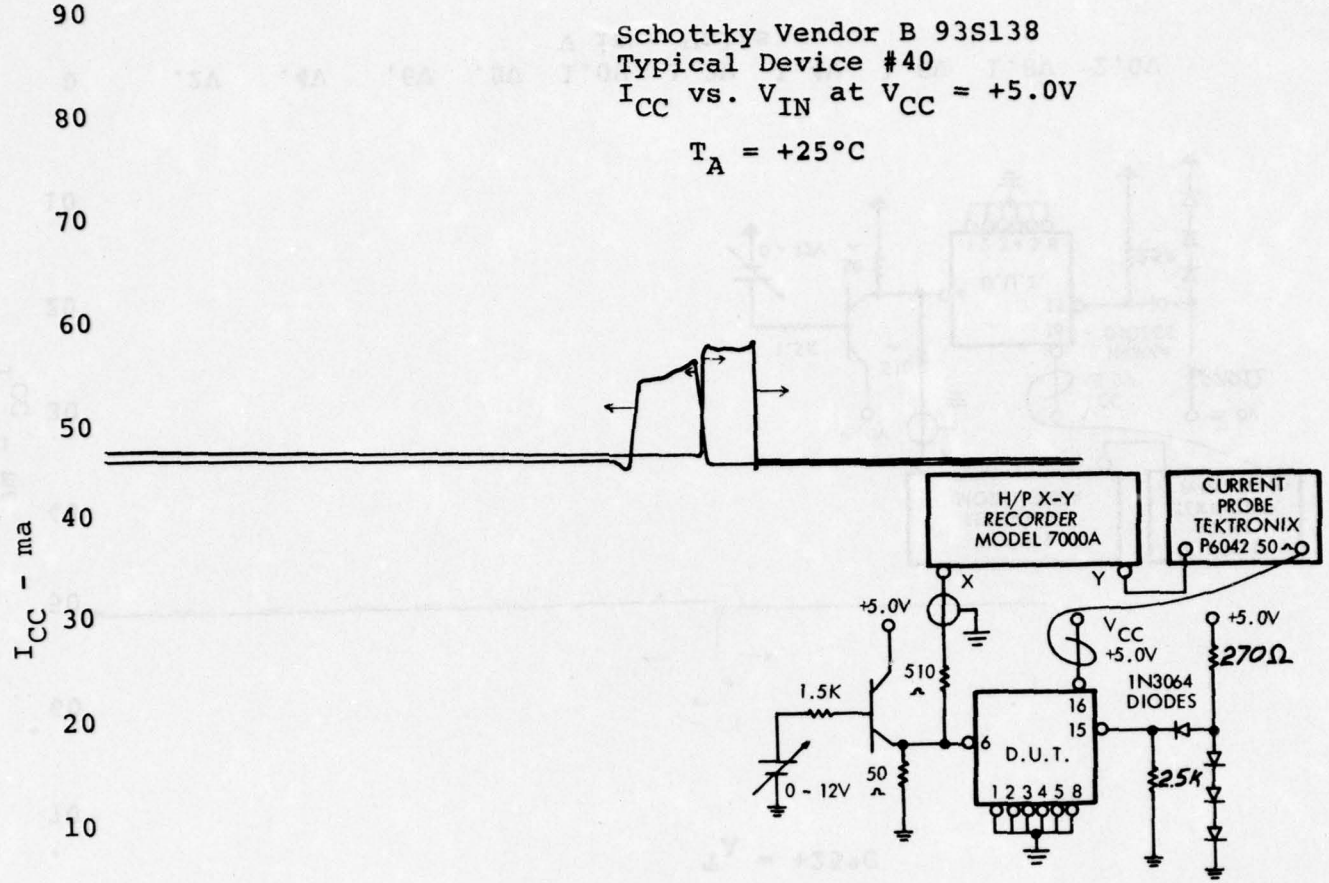
Schottky Vendor A 54S138
Typical Device #28
I_{CC} vs. V_{IN} at V_{CC} = +5.0V

T_A = +25°C

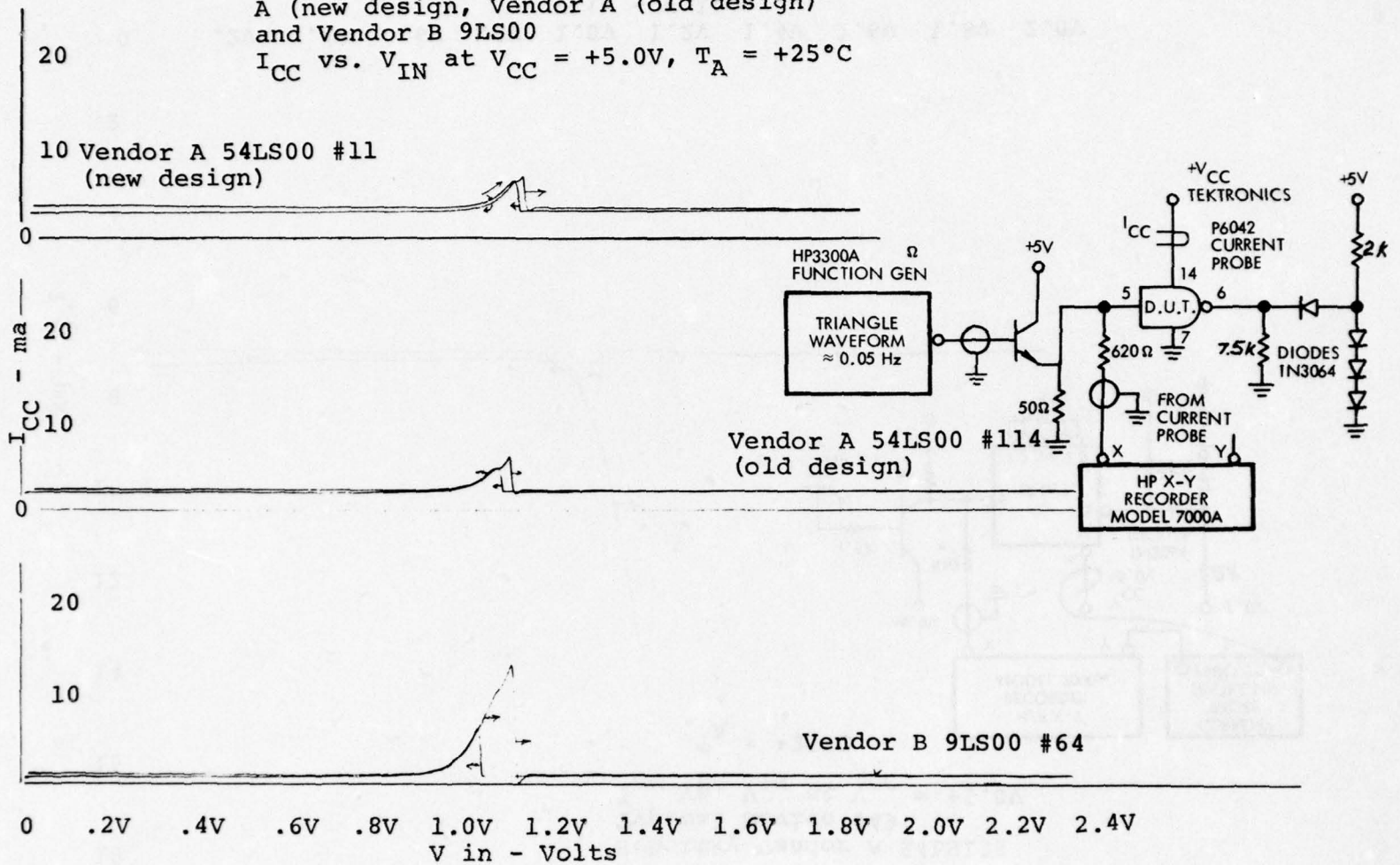


Schottky Vendor B 93S138
Typical Device #40
I_{CC} vs. V_{IN} at V_{CC} = +5.0V

T_A = +25°C

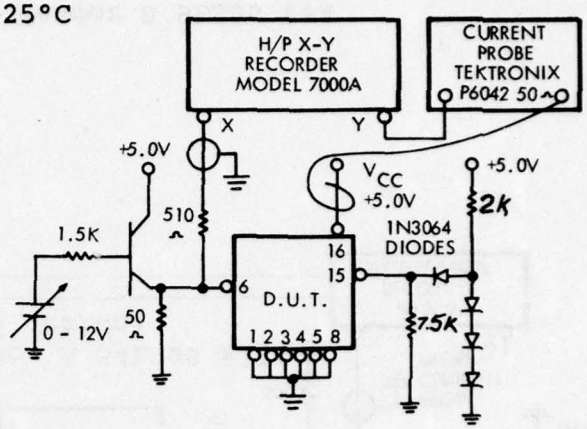


Comparisons of Schottky Vendor
A (new design, Vendor A (old design)
and Vendor B 9LS00
I_{CC} vs. V_{IN} at V_{CC} = +5.0V, T_A = +25°C



Schottky Vendor A 54LS138
Typical Device #49
I_{CC} vs. V_{IN} at V_{CC} = +5.0V

T_A = +25°C



APPENDIX B

APPENDIX B

CONSTRUCTION ANALYSIS OF VENDOR A 54S00

STANDARD SCHOTTKY TTL INTEGRATED CIRCUIT IN CERAMIC DIP

ABSTRACT

A Vendor A quadruple dual-input NAND gate, vendor part number 54S00, in a standard 14-pin ceramic dual-inline-package (CERDIP) was subjected to construction analysis. It is a standard Schottky device. Two units were received date coded 7330. The internal wires were found to be Al, while the single level chip metallization was as follows: Pt_xSi_y ohmic contacts, sputtered Ti-W, followed by vapor deposited Al (pure). The chip is entirely coated with vapor deposited SiO_2 for handling protection only. The emitter metallization of the output transistor, at the specified maximum output current of 20mA, carries the highest current density on the chip during normal operation of the device. At a thickness of 1.4μ and width of 6.3μ, this density is about $2.5 \times 10^5 A/cm^2$. At an oxide step, this metallization would be substantially thinner, the current density correspondingly higher. MIL-38510 specifies $2 \times 10^5 A/cm^2$ maximum. No other design deficiencies or workmanship defects were observed. The chip was mapped.

INTRODUCTION

This analysis was performed as part of an evaluation of this device for Rome Air Development Center. The analysis was designed to document the materials and construction details used in these units and to identify shortcomings in the design or defects in workmanship, if any.

RESULTS

This package is a ceramic dual-in-line (CERDIP), in accordance with JEDEC (TO-116), 14 lead SSI. Package dimensions are shown in Figure B-7.

The hermetic seal (tested during another part of the overall evaluation) is fritted glass. The pins, tin plated kovar, are embedded in the seal. An identification notch at

one end identifies pin 1. Package marking was as follows:

top:
7330
M 54S00
38510C

and bottom:
00H3
202

The packages are purchased from Kyoto Ceramic Company. No deficiencies or defects were noted.

The Chip

The lid was removed by applying mechanical stress to the lid and forcing a chisel edge into the seal in a controlled manner until the seal fractured. The chip measured 41 X 41 X 8.6 mils and used a gold-silicon eutectic die mount. The internal wires were ultrasonically bonded, 1 mil diameter aluminum (manufacturer specifies > 99.9% Al). No bond defects were noted. Microbond-pull testing of 4 of the 14 wires found a range in pull strength from 2.3 grams-force to 3.7 gm-f with 2.9 average. These wires should have a minimum of about 2 gm-f pull strength.

The chip metallization was a single layer interconnection scheme with a SiO_2 coating over the entire chip, primarily designed, not as passivation, but as scratch protection during chip handling. The metallization had the following structure: Al on top (> 99.9% pure, claimed by manufacturer), Ti-W below for good adhesion to Si and SiO_2 and as a diffusion barrier to Al, and finally Pt_xSi_y in the contact areas for good stable ohmic and Schottky barrier contact.

The top SiO_2 was measured to be about 2.0μ thick, somewhat thinner over the metallization. The Al layer of the metallization was about 1.4μ thick, and carries almost all the current. The Ti-W layer was measured in angle section to be about 3000Å thick. The Al layer was vapor deposited, the Ti-W was sputter deposited in an undisclosed ratio. The Pt_xSi_y is formed by sputtering on Pt in a very thin layer, a few hundred angstroms, and sintering to form Pt_xSi_y in the contact areas, followed by blanket etching to remove the Pt elsewhere.

The highest current density was found to exist in the output transistors' emitter metallization. Here the current is specified at 20mA maximum and the metallization is 6.3μ wide (X 1.4μ thick) resulting in a density of 2.5 X $10^5 A/cm^2$. Over

an oxide step, the density could reach 4 X 10^5 or higher. MIL-38510 specifies 2 X $10^5 A/cm^2$ as a maximum density for Al to avoid an unacceptable level of electromigration failures.

The chip microsection found an N-type epitaxial layer of 3μ thickness on a P-type substrate (grounded).

The Components

The chip was photographed and mapped to identify all the components. Figure B-1 shows the logic layout of the gates as relates to the external pins with Figure B-1a showing the electrical schematic of one gate. Figure B-2 shows the chip with all components marked.

The substrate is P-type. Prior to epitaxial layer growth, low resistivity N-type diffusions, subcollectors, are made in positions corresponding to transistors. These provide high conductivity paths from the vicinity of the base-collector junctions to the collector contact diffusions.

After the epitaxial growth, P-type isolation diffusions partition the epitaxial layer into individual collector regions and other components. This diffusion was measured to be about 3.7μ deep. The P-type base diffusion follows, also creating the resistors. This diffusion was measured to be about 1μ deep. This also creates the p-n junction guard rings for the input clamping diodes to be discussed later. Then the N+-type emitter diffusion, measured at a depth of 0.75μ, creates the emitters and the collector contact enhancement regions. This latter is necessary to achieve ohmic contact to the low-doped epitaxial layer.

The Transistors

Q1 is a two-emitter input transistor, top view shown in Figure B-3. The collector region is irregularly shaped with an area of 3750μ^2. The collector contact enhancement diffusion (c.c.e.d.) is 8μ X 30μ with a contact hole of 5.7μ X 25μ. The base regions of all those transistors with base to collector Schottky diodes are annular, i.e., a rectangular hole in a rectangular shaped diffusion. The hole allows the epitaxial region to "surface" within the base region. The contact hole in the base oxide exposes both part of the base region and all of this "surfacing" epitaxial area of the collector. When the metallization is deposited within the hole, it creates the ohmic contact to the base region and also creates the Schottky

diode from base to collector. This occurs because of the relative doping of the base region (high doping → ohmic contact) versus the epitaxial region (low doping → rectifying Schottky contact). Hosack[1] reports a barrier height of 0.82eV for Pt_xSi_y on n-type silicon. Also M. Kamoshida and T. Okada[2] report that the contact resistance of Pt_xSi_y on highly doped Si is essentially the same as that found for Al on Si.

For Q1, the overall base dimensions are 47μ X 47μ. The Schottky diode area is 26μ X 18.5μ. The contact hole, which completely exposes the Schottky diode, as well as some base area, is 32μ X 25μ. The two emitters are diffused into the base region away from the Schottky diode and are each 11μ X 8.5μ with contact holes of 6.2μ X 3.8μ.

Q2, the phase splitting transistor, is similar to Q1 in construction with only one emitter. The corresponding dimensions for Q2 are:

collector	67μ X 52.5μ
c.c.e.d.	35μ X 7.4μ
contact hole	33μ X 7.4μ
base (overall)	37μ X 34μ
Schottky diode	18.5μ X 7.9μ
contact hole	25μ X 15μ
emitter	27μ X 7.4μ
contact hole	22μ X 4.5μ

Q6 is also similar to Q1 in construction. It is the output transistor and has two emitters shorted together and two collector contacts shorted together:

collector	106μ X 84μ
c.c.e.d.'s (each of 2)	62μ X 9.5μ
contact holes (each of 2)	60μ X 9μ
base (overall)	60μ X 64μ
Schottky diode	49.5μ X 19μ
contact hole	55μ X 24μ
emitters (each of 2)	55μ X 6.8μ
contact holes (each of 2)	50μ X 5.5μ

Q4 and Q5 are combined within one isolated epitaxial region forming a Darlington pair with a common collector. This collector is 131μ X 59μ. It has a single c.c.e.d. (56μ X 9.3μ)

and a single collector contact hole (54μ X 8μ). The base of Q4 is similar in construction to that of Q1 with overall base dimensions of 35.8μ X 32.8μ, a Schottky diode of 19μ X 8.6μ and a contact hole of 25μ X 14.3μ. The emitter of Q4 is 24μ X 8μ with a contact hole of 19μ X 3.1μ.

Q5 is a transistor with no collector-base Schottky diode and thus has a normal rectangular diffusion of 45μ X 26μ. The base contact hole is 37μ X 4.3μ. The emitter is 37μ X 6μ with a contact hole 30μ X 4μ.

Q3 utilizes an extended base diffusion to create the two resistors associated with that transistor. See Figure B-4. The collector area is 5380μ^2.

The resistor to the collector seems to be about 1.7 squares, the resistor to the base region about 3.4 squares. These, with the resistance values shown in Figure B-1a, indicate a base diffusion sheet resistance of about 150 Ω/□

The base region measures 37μ X 31μ with a Schottky diode of 16μ X 9μ. Contact between base and the Schottky contact diode to the collector is accomplished, as shown in Figure B-3,

by simply extending the metal side of the contact diode out beyond the "surfaced" collector region so that it makes ohmic contact to the base. This is actually the same as in other Schottky transistors except that the metallization in this instance does not go anywhere else. The contact hole to accomplish this is 22μ X 14μ. The metallization is just large enough to ensure complete coverage of this hole. Similarly, good ohmic contact between R4 and the collector is made with a contact hole opening both R4 and the c.c.e.d. and metallization covering that contact hole.

The emitter diffusion is 22.8μ X 7.4μ with a contact hole 18.5μ X 3.8μ.

The Diodes

Each input has a Schottky barrier clamping diode to ground, to provide protection for the input against negative voltage spikes. The construction is quite similar to that in the transistors, forming what is actually a p-n junction - Schottky barrier hybrid diode. R.A. Zettler and A.M. Cowley[3] discuss the physics of the p-n junction "guard ring". Figure B-5 conceptuallizes the construction in this device. Figure B-6 shows a top view of an actual diode. Basically the p-n junction guard ring eliminates the unwanted edge effects present in passivated Schottky barrier diodes which cause susceptibility to noise and uncontrolled reduction in reverse breakdown voltage. This is also reason for completely enclosing in base regions the Schottky barrier diodes associated with the transistors. The dimensions of all input diodes, referring to Figure B-5, are as follows:

isolated N-type epitaxial region	104.5μ X 72.6μ
N+-type (emitter) diffusion	80μ X 11.6μ
contact hole in above	76μ X 8.1μ
P-type (base) diffusion (exterior)	114μ X 44.5μ
contact hole in above	104.5μ X 36.4μ
Schottky contact area ("surfaced" epitaxial within P-type region)	89μ X 24.4μ

The Resistors

As in Q3, all resistors are P-type base diffusion. Except for those in Q3, all are diffused into isolated epitaxial

regions separate from any transistor. These epitaxial areas are contacted (with N+ contact enhancement diffusions) by V_{CC} metallization. This holds the p (resistor) -n (epitaxial) junction in reverse bias.

CONCLUSIONS

The design found in this device appears to be sound with the one exception of current density in the output emitter metallization. The $2 \times 10^5 A/cm^2$ limit may be more severe than necessary in this particular chip since the literature indicates that large grained aluminum with a glass overcoat exhibits improved resistance to electromigration. For example, L. W. Danley[4] reports MTBF for aluminum at a density of $3 \times 10^5 A/cm^2$ at 150°C to be about 3.5×10^3 hours for small grained uncoated aluminum and about 3.5×10^5 hours for large grained glass coated aluminum (Au is on the order of 10^9 hours or 100,000 years!). These devices have the desirable glass overcoat. However, the low-stress grain boundaries which occur in vapor deposited aluminum are not easily delineated chemically, making it difficult to determine the grain size with any accuracy. The susceptibility of these devices to failure due to electromigration can best be determined through life testing.

Furthermore, it was noted that the deposited glass exhibited moderate to severe cracking.

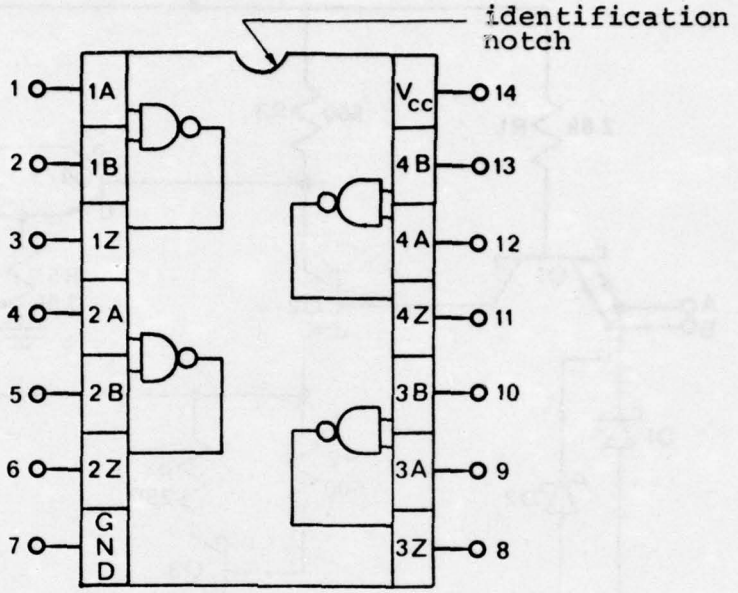


FIGURE B-1: Pin diagram of device showing logic layout. Not to scale.

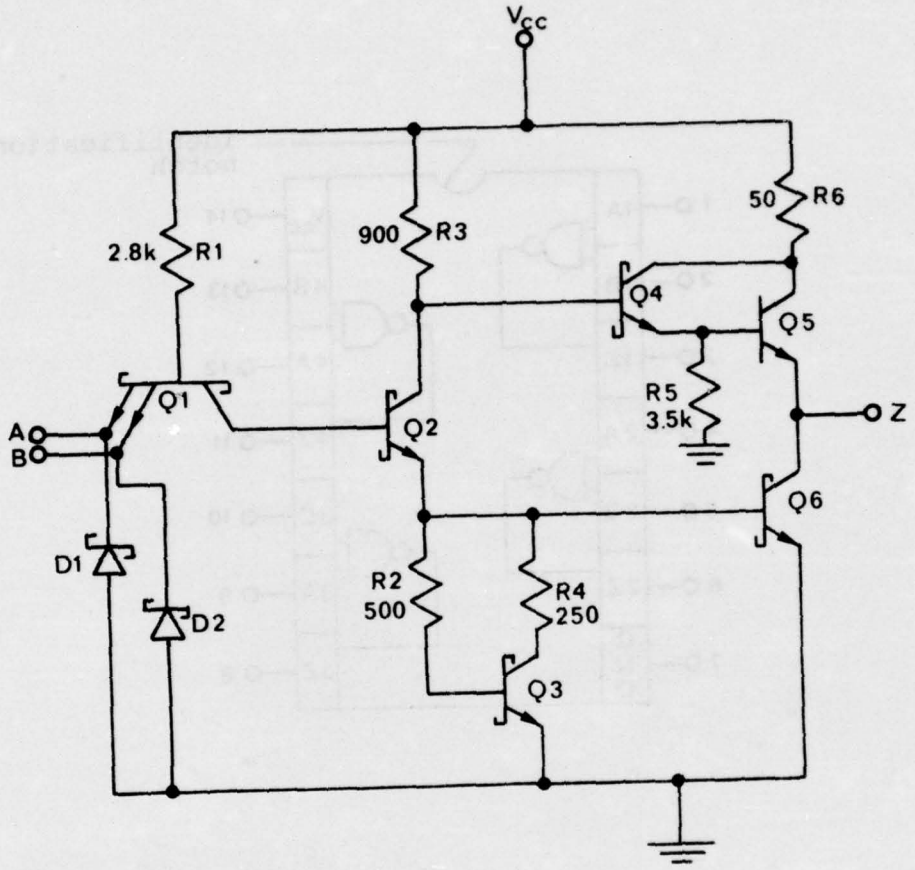


FIGURE B-1a: Electrical schematic of one of four NAND gates. Resistor values, provided by the manufacturer, are in Ω.

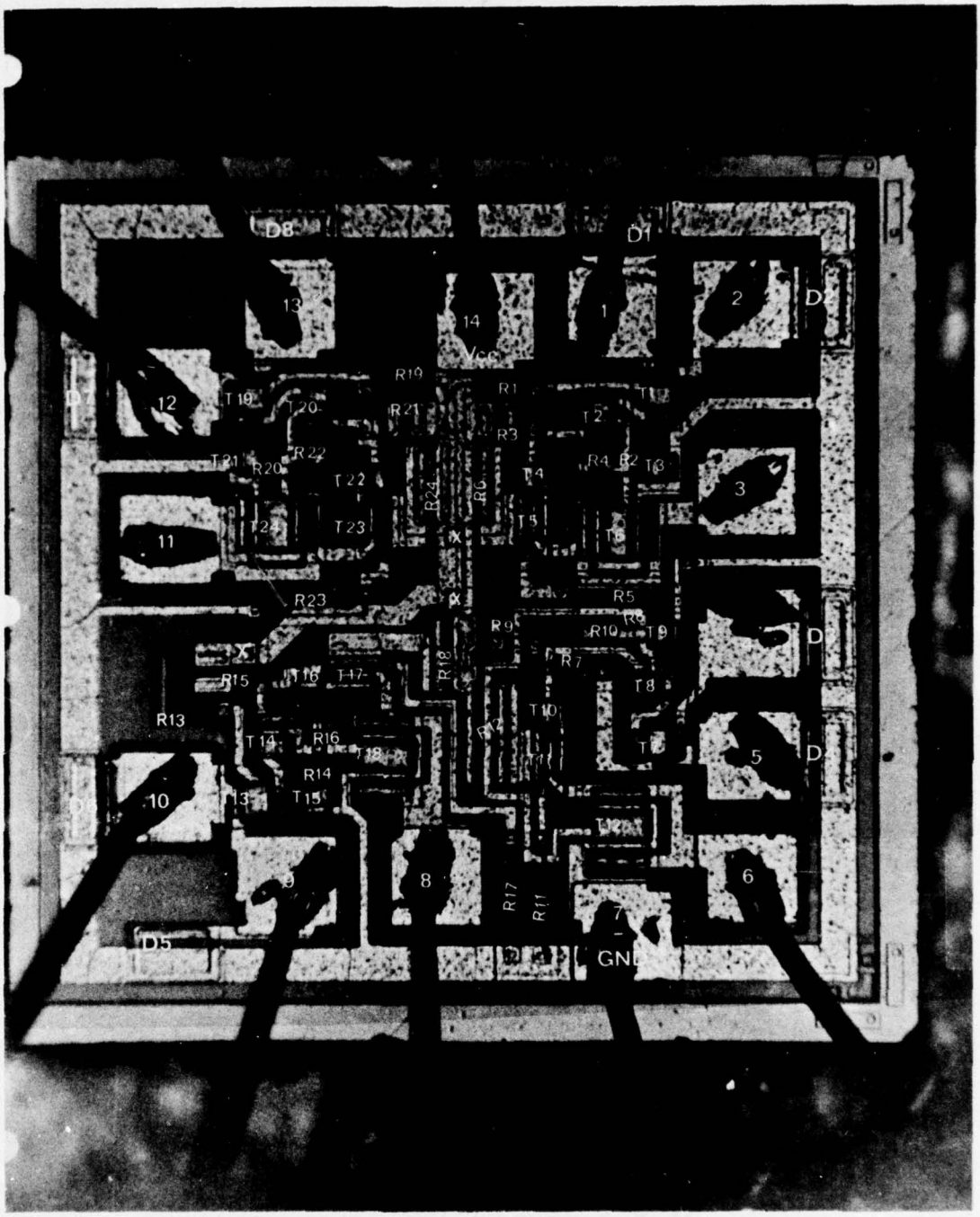


FIGURE B-2: Overall Photograph of Chip with Map Overlay

200 μm

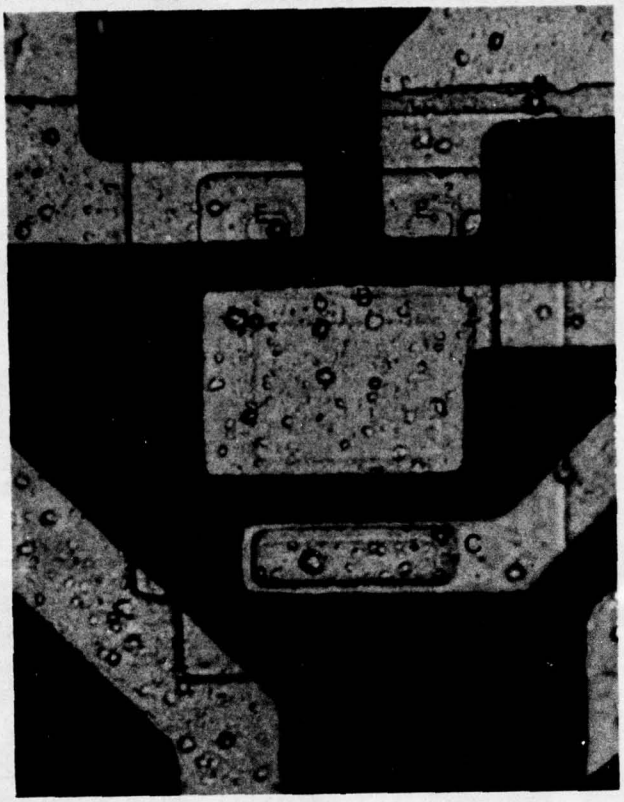


FIGURE B-3: Top view of input transistor Q1 (dual emitter). The large base contact (B) covers the "surfaced" epitaxial region to form the Schottky barrier contact diode between base and collector.

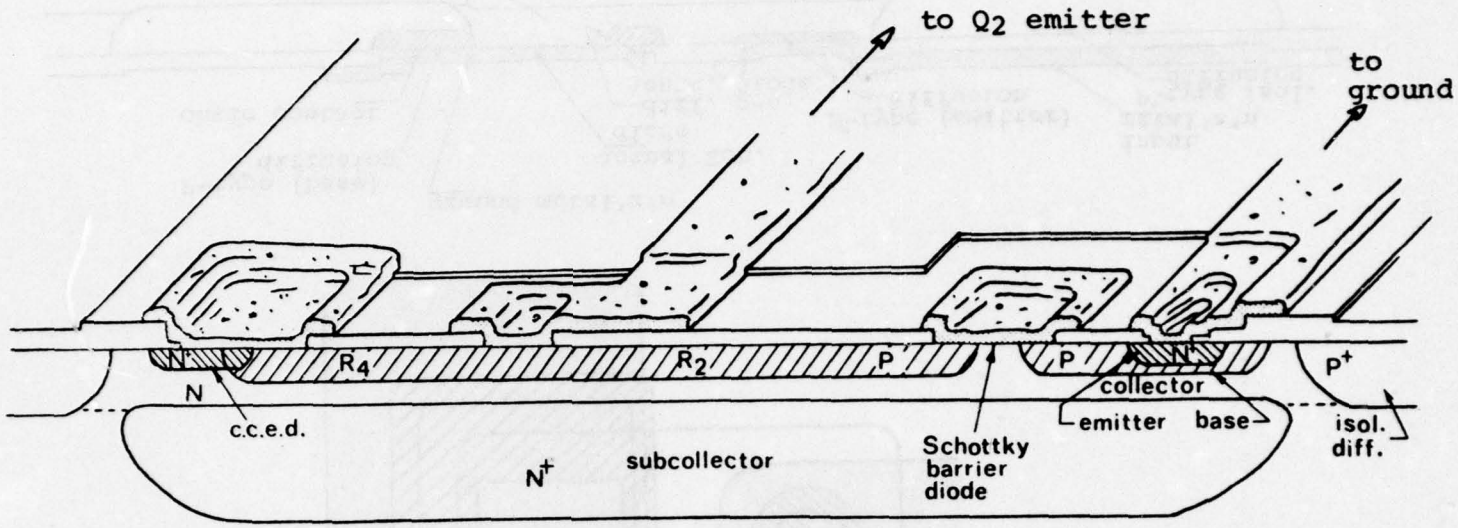


FIGURE B-4: Q3 in cross-section (not to scale).

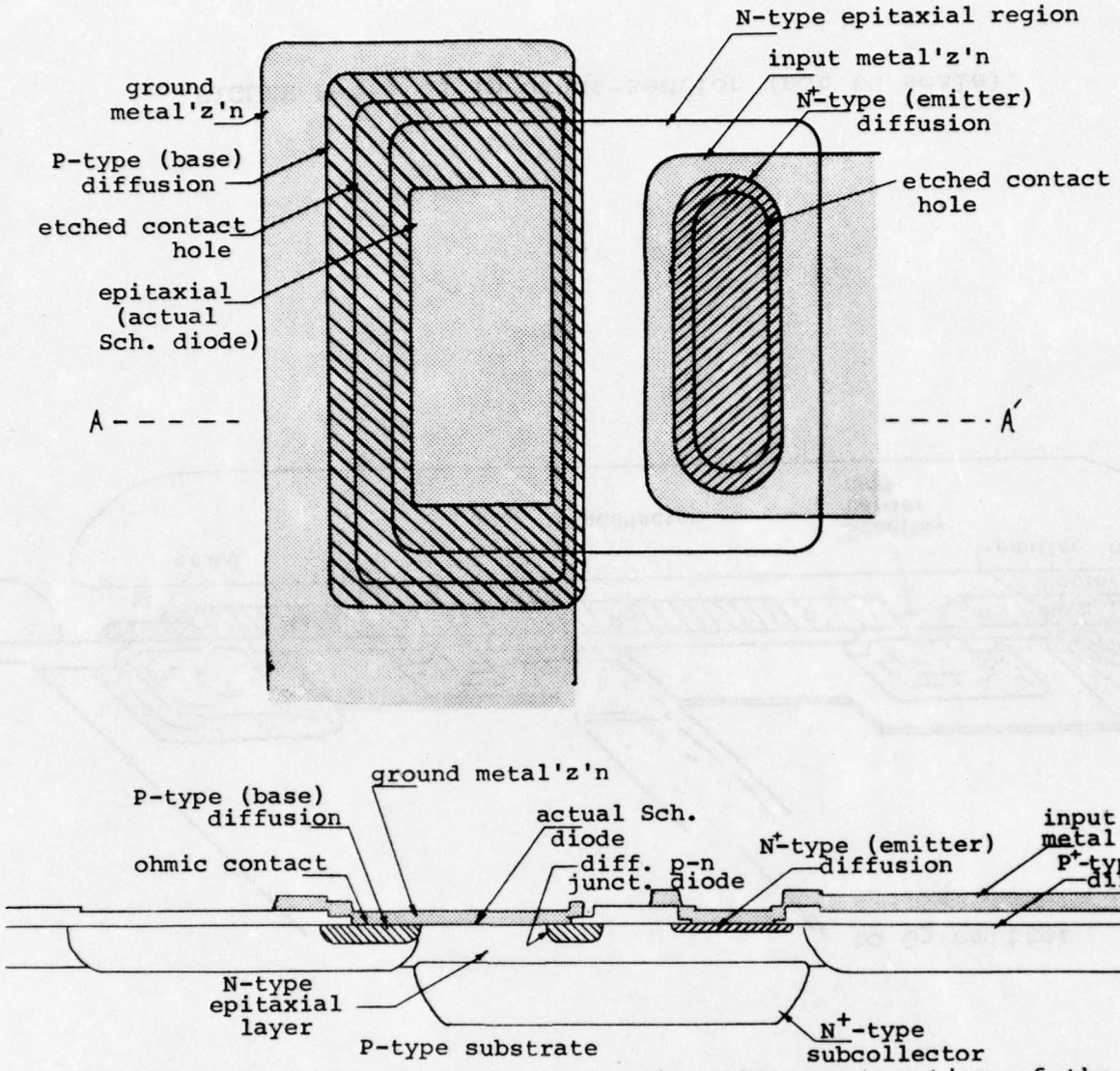


FIGURE B-5: Top and side views demonstrating the construction of the p-n junction-Schottky barrier hybrid input clamping diodes.

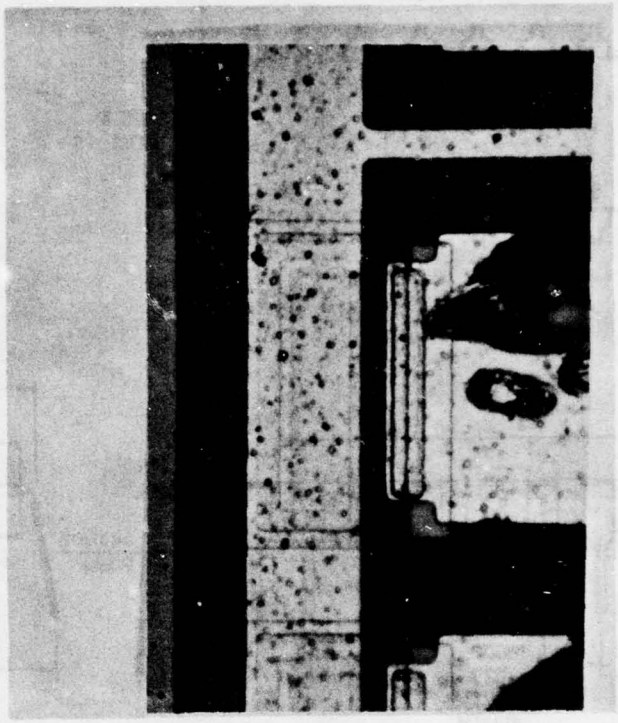
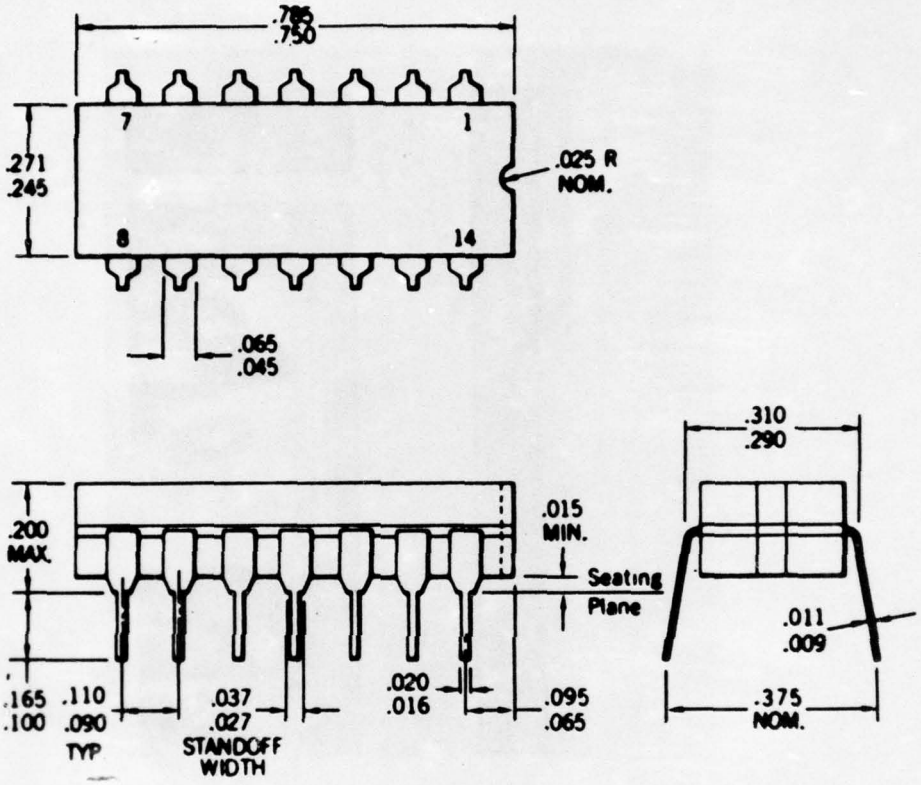


FIGURE B-6: Top view of actual input diode. (D3)

In accordance with
JEDEC (TO-116) outline
14-Lead SSI Dual In-line



NOTES
- All dimensions in inches
- Leads are intended for insertion in hole rows on .300" centers
- They are purposely shipped with "positive" misalignment to facilitate insertion
- Board-drilling dimensions should equal your practice for .020 inch diameter lead
- Leads are tin-plated kovar
- Package weight is 2.0 grams

FIGURE B-7: Package Outlines

APPENDIX C

APPENDIX C

CONSTRUCTION ANALYSIS OF VENDOR B 9S00

STANDARD SCHOTTKY TTL INTEGRATED CIRCUIT IN CERAMIC DIP

ABSTRACT

A quadruple dual-input NAND gate manufactured by Vendor B, p/n 9S00, in a standard 14-pin ceramic dual-inline-package (CERDIP) was subjected to construction analysis. It is a standard Schottky device. The two units analyzed were date coded 7422. The internal wires were found to be Al, while the single level chip metallization was as follows: Pt_xSi_y Schottky and ohmic contacts, sputtered Ti-W, followed by vapor deposited Al (pure). The chip is entirely coated with vapor deposited SiO_2. The emitter metallization of the output transistor, at the specified maximum output current of 20mA, carries the highest current density on the chip during normal operation of the device. At a thickness of 1.4μ and width of 7.6μ, this density is about 2.1 X $10^5 A/cm^2$. At an oxide step, this metallization would be substantially thinner, the current density correspondingly higher. MIL-38510 specifies 2 X $10^5 A/cm^2$ maximum. No design deficiencies or workmanship defects were observed. The chip was mapped.

INTRODUCTION

This analysis was performed as part of an evaluation of this device for Rome Air Development Center. The construction analysis was designed to document the materials and construction details used in these units and to identify shortcomings in the design or defects in workmanship, if any.

RESULTS

This package is a ceramic dual-in-line (CERDIP), in accordance with JEDEC (TO-116), 14 lead SSI. Package dimensions are shown in Figure C-1.

The hermetic seal (tested during another part of the overall evaluation) is fritted glass. The pins, tin plated kovar, are embedded in the seal. An identification notch at one end identifies pin 1. Package marking was as follows:

and the bottom was unmarked.

About 15% of the packages are purchased from Kyoto Ceramic Company, the balance are manufactured in house. No deficiencies or defects were noted.

The Chip

The lid was removed by applying mechanical stress to the lid and forcing a chisel edge into the seal in a controlled manner until the seal fractured. The chip measured 41 X 43.3 X 9.5 mils and used a gold-silicon eutectic die mount. The internal wires were ultrasonically bonded, 1 mil diameter aluminum (manufacturer specifies > 99.9% Al). No bond defects were noted. Microbond-pull testing of 4 of the 14 wires found a range in pull strength from 3.5 grams-force to 4.4 gm-f with 3.9 average. These wires should have a minimum of about 2 gm-f pull strength.

The chip metallization was a single stratum interconnection scheme with a P-doped SiO_2 coating over the entire chip. The metallization has the following structure: Al on top (> 99.9% pure, claimed by manufacturer), Ti-W below for good adhesion to Si and SiO_2 and as a diffusion barrier to Al, and finally Pt_xSi_y in the contact areas for good stable ohmic and Schottky contacts.

The top glass was measured to be about 2.3μ thick, somewhat thinner over the metallization. The Al layer of the metallization, measured to be about 1.4μ thick, carries almost all of the current. The Ti-W layer was measured in angle section to be about 3000Å thick. The Al layer is vapor deposited, the Ti-W sputter deposited in an undisclosed ratio. The Pt_xSi_y is formed by sputtering on Pt in a very thin layer, a few hundred angstroms, and sintering to form Pt_xSi_y in the contact areas, followed by blanket etching to remove the Pt elsewhere.

The highest current density was found to exist in the output transistors' emitter metallization. Here the current is specified at 20mA maximum and the metallization is 7.6μ wide (X 1.4μ thick) resulting in a density of 2.1 X $10^5 A/cm^2$. Over an oxide step, the density could reach 3.2 X 10^5 or higher. MIL-38510 specifies 2 X $10^5 A/cm^2$ as a maximum density for Al to avoid an unacceptable level of electromigration failures.

The chip microsection found an N-type epitaxial layer of 4.4μ thickness on a P-type substrate (grounded). Manufacturer specifies 4.5μ and a bulk resistivity of 0.5 Ω cm.

The Components

The chip was photographed and mapped to identify all the components. Figure C-2 shows the logic layout of the gates as relates to the external pins with Figure C-3 showing the electrical schematic of one gate. Figure C-4 shows the chip with all components marked.

The substrate is P-type. Prior to epitaxial layer growth, low resistivity N-type diffusions, subcollectors, are made in positions corresponding to transistors. These provide high conductivity paths from the vicinity of the base-collector junctions to the collector contact diffusions.

After the epitaxial growth, P-type isolation diffusions partition the epitaxial layer into individual collector regions and other components. This diffusion was measured to be about 4.7μ deep. The P-type base diffusion follows, also creating the resistors. This diffusion was measured to be about 2μ deep. This also creates the p-n junction guard rings for the input clamping diodes to be discussed later. Then the N+-type emitter diffusion, measured at a depth of 1.2μ, creates the emitters and the collector contact enhancement regions. This latter is necessary to achieve ohmic contact to the low-doped epitaxial layer. The manufacturer specifies the base diffusion at 2.5μ deep and 180-200 Ω/□, the emitter diffusion at 1.5μ deep and 9 Ω/□.

The Transistors

Q1 is a two-emitter input transistor, top view shown in Figure C-5. The collector region is 90μ X 70μ. The collector contact enhancement diffusion (c.c.e.d.) is 6.2μ X 42μ with a contact hole of 5.3μ X 35μ. The base regions of all those transistors with base to collector Schottky diodes are annular, i.e., a rectangular hole in a rectangular shaped diffusion. The hole allows the epitaxial region to "surface" within the base region. The contact hole in the base oxide exposes both part of the base region and all of this "surfacing" epitaxial area of the collector. When the metallization is deposited within the hole, it creates the ohmic contact to the base region and also creates the Schottky diode from base to collector. This occurs because of the relative doping of the base region (high doping → ohmic contact) versus the epitaxial

region (low doping → rectifying Schottky contact). Hosack[1] reports a barrier height of 0.82eV for Pt_xSi_y on n-type silicon. Also M. Kamoshida and T. Okada[2] report that the contact resistance of Pt_xSi_y on highly doped Si is essentially the same as that found for Al on Si.

For Q1, the overall base dimensions are 37μ X 50μ. The Schottky diode area is 26μ X 20μ. The contact hole, which completely exposes the Schottky diode, as well as some base area, is 31μ X 27μ. In fact the contact holes are not completely covered by the metal contact. See Figure C-5. Some of the bare silicon in the base region is covered only by the Phosphosilicate glassivation layer. The two emitters are diffused into the base region away from the Schottky diode and are each 14μ X 14μ with contact holes of 6μ X 6μ.

Q2, the phase splitting transistor, is similar to Q1 in construction with only one emitter. The corresponding dimensions for Q2 are:

collector	90μ X 63μ
c.c.e.d.	35μ X 12μ
contact hole	29μ X 13μ
base (overall)	40μ X 28μ
Schottky diode	24μ X 13.5μ
contact hole	25.5μ X 19.5μ
emitter	25μ X 10.5μ
contact hole	21μ X 4μ

Q6 is also similar to Q1 in construction. It is the output transistor and has two emitters shorted together and two collector contacts shorted together:

collector	143μ X 103μ
c.c.e.d.'s (each of 2)	76μ X 18.5μ
contact holes (each of 2)	62μ X 18μ
base (overall)	64μ X 69μ
Schottky diode	62μ X 16μ
contact hole	64μ X 29μ
emitters (each of 2)	63μ X 6.2μ
contact holes (each of 2)	60μ X 6.0μ

Q3 and Q5 are combined within one isolated epitaxial region forming a Darlington pair with a common collector. This collector is 106μ X 49μ. It has a single c.c.e.d. (32μ X 10.8μ) and a single collector contact hole (28μ X 8μ). The base of Q3 is similar in construction to that of Q1 with overall dimensions of 29μ X 16.5μ, a Schottky diode of 11.5μ X 9.5μ and a contact hole of 9μ X 4μ.

Q5 is a transistor with no collector-base Schottky diode and thus has a normal rectangular diffusion of 31μ X 17.5μ. The base contact hole is 28.5μ X 4.3μ. The emitter diffusion is 31μ X 14μ with a contact hole 25μ X 4μ.

Q4 utilizes an extended base diffusion to create the two resistors associated with that transistor. See Figure C-6. The collector area is 80μ X 127μ.

The resistor to the collector, R5, seems to be about 2 squares, the resistor to the base region, R3, about 2 squares. These, with the resistance values shown in Figure C-3, indicate a base diffusion sheet resistance of about 180 Ω/□ .

The base region measures 46μ X 36μ with a Schottky diode of 24μ X 11μ. Contact between base and the Schottky contact diode to the collector is accomplished, as shown in Figure C-6, by simply extending the metal side of the contact diode out beyond the "surfaced" collector region so that it makes ohmic contact to the base. This is actually the same as in other Schottky transistors except that the metallization in this instance does not go anywhere else. The contact hole to accomplish this is 28μ X 17μ. The metallization is just large enough to ensure complete coverage of this hole. Similarly, good ohmic contact between R5 and the collector is made with a contact hole opening both R5 and the c.c.e.d. and metallization covering that contact hole.

The emitter diffusion is 38μ X 16μ with a contact hole 22μ X 9μ.

The Diodes

Each input has a Schottky barrier clamping diode to ground, to provide protection for the input against negative voltage spikes. The construction is quite similar to that in the transistors, forming what is actually a p-n junction - Schottky barrier hybrid diode. R.A. Zettler and A.M. Cowley[3] discuss the physics of the p-n junction "guard ring". Figure B-5 of Appendix B conceptuallizes and summarizes the rationale for the construction of this device.

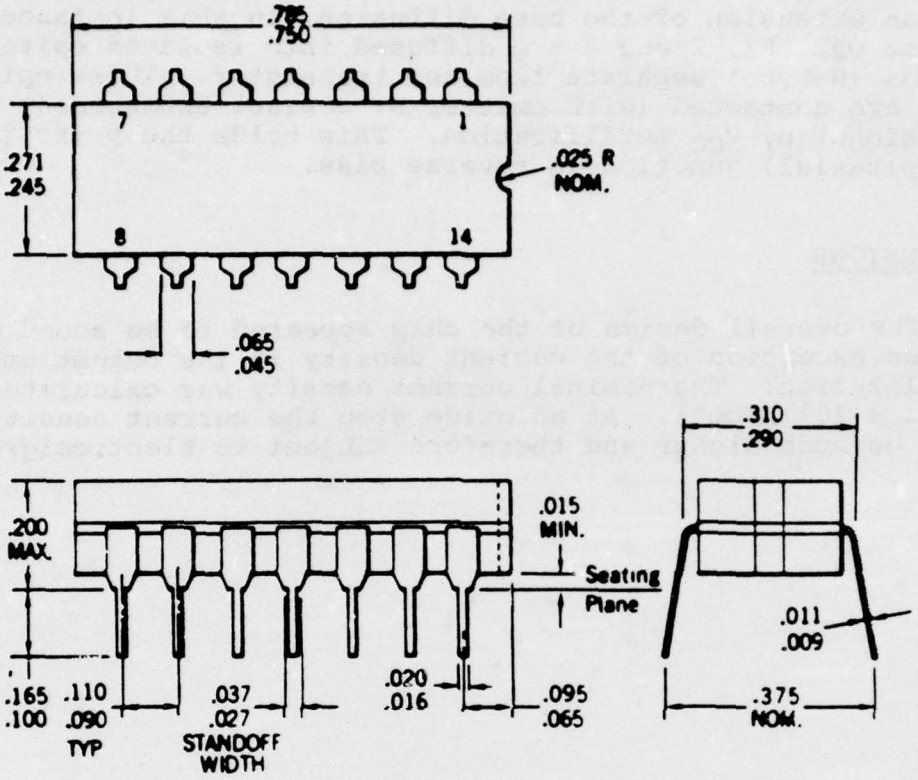
The Resistors

As in Q4, all resistors are P-type base diffusion. R4 is also an extension of the base diffusion, in this instance, the base of Q5. R1, 2 and 6 are diffused into isolated epitaxial regions (N-type) separate from any transistor. These epitaxial areas are contacted (with emitter N+ contact enhancement diffusions) by V_{CC} metallization. This holds the p (resistor) -n (epitaxial) junction in reverse bias.

CONCLUSIONS

The overall design of the chip appeared to be sound with the one exception of the current density in the output emitter metallization. The nominal current density was calculated to be 2.1×10^5 A/cm^{-2}. At an oxide step the current density would be much higher and therefore subject to electromigration.

In accordance with
JEDEC (TO-116) outline
14-Lead SSI Dual In-line



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with positive misalignment to facilitate insertion
Board drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.0 grams

FIGURE C-1: Package outlines.

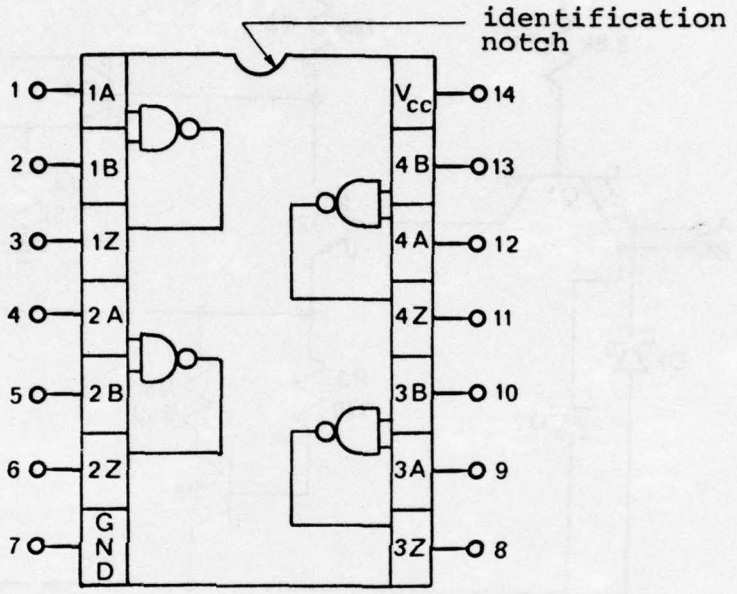


FIGURE C-2: Pin diagram of device showing logic layout. Not to scale.

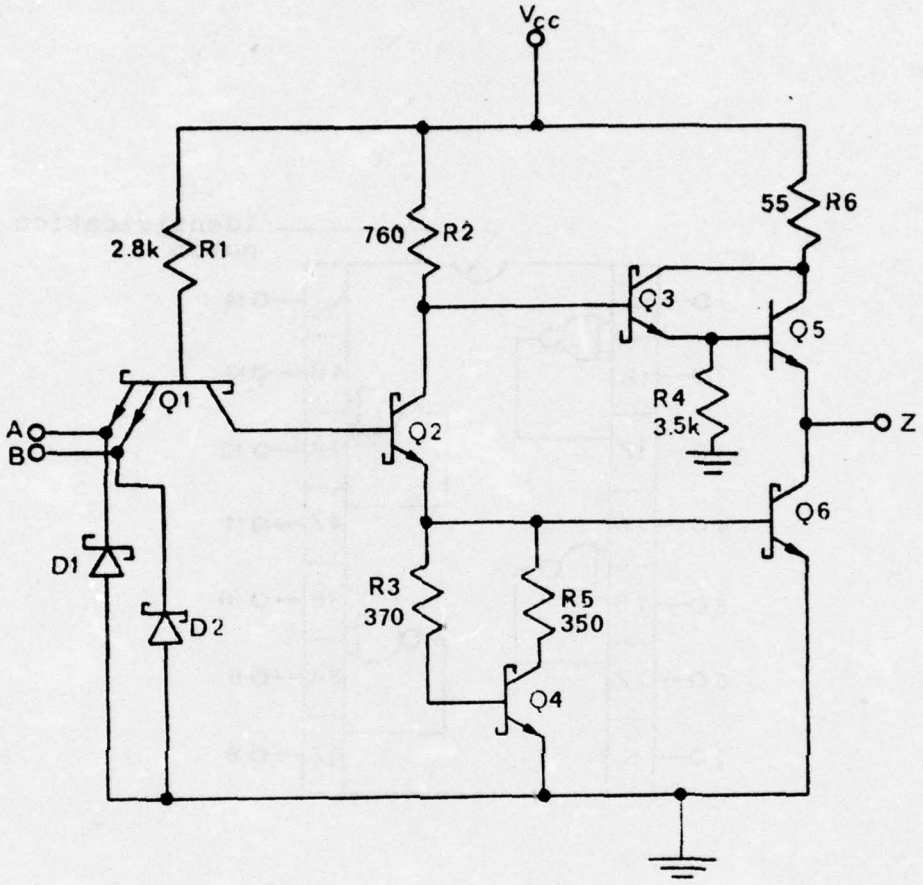


FIGURE C-3: Electrical schematic of one of four NAND gates. Resistor values, provided by the manufacturer, are in Ω.

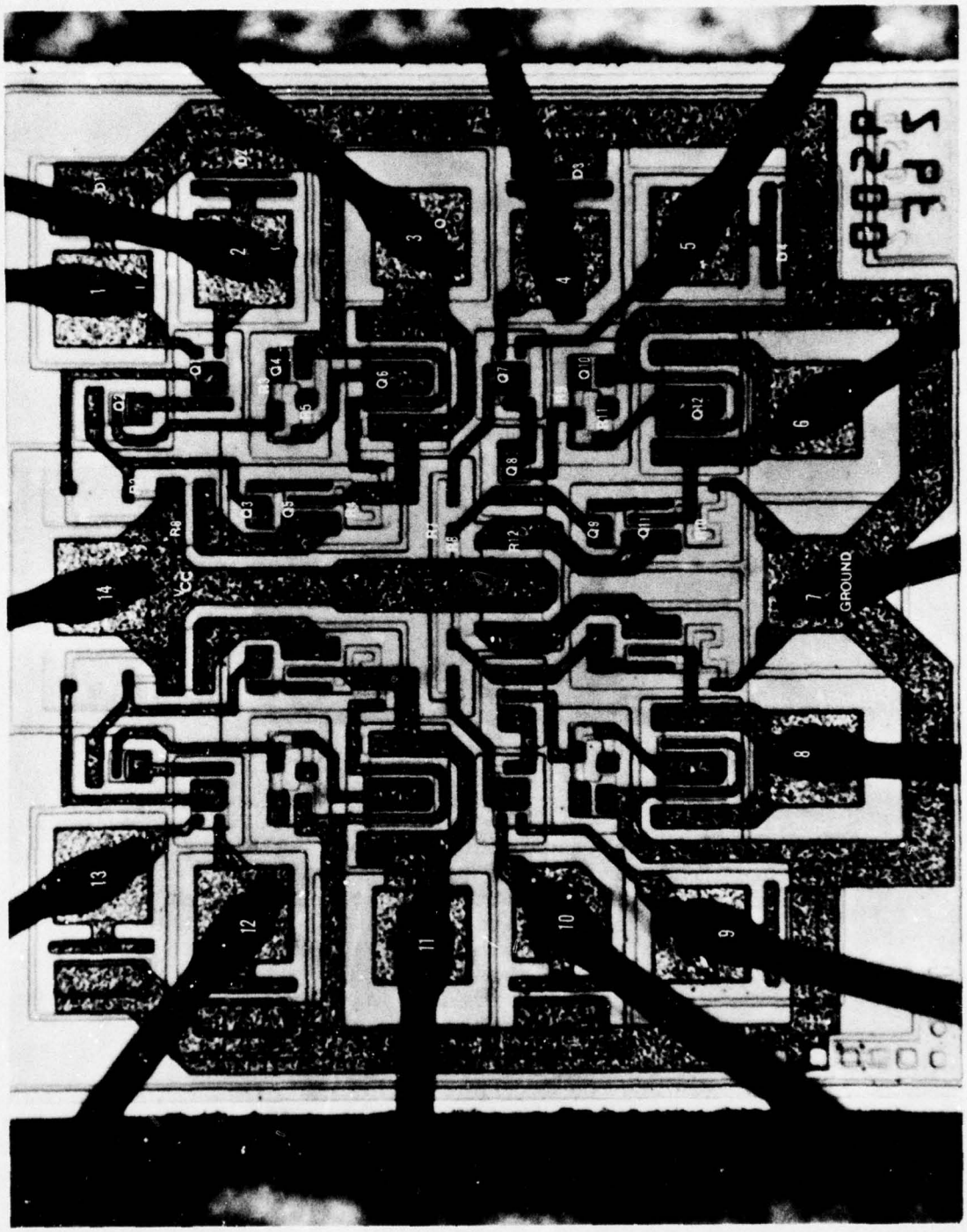


FIGURE C-2: Overall Photograph of Chip with Map Overlay

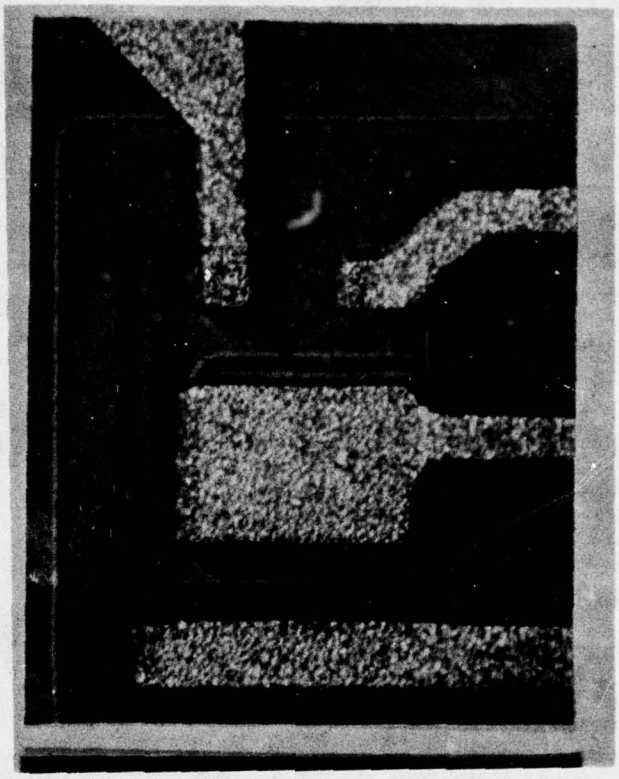


FIGURE C-5: Q1, the input transistor. The arrow indicates the contact window for the base and Schottky diode. Note that the metallization does not cover the hole, leaving base region exposed. The vapor deposited glass overcoat, however, provides passivation. The two emitter contacts are at the top of the base, the collector contact is at the bottom of the photo.

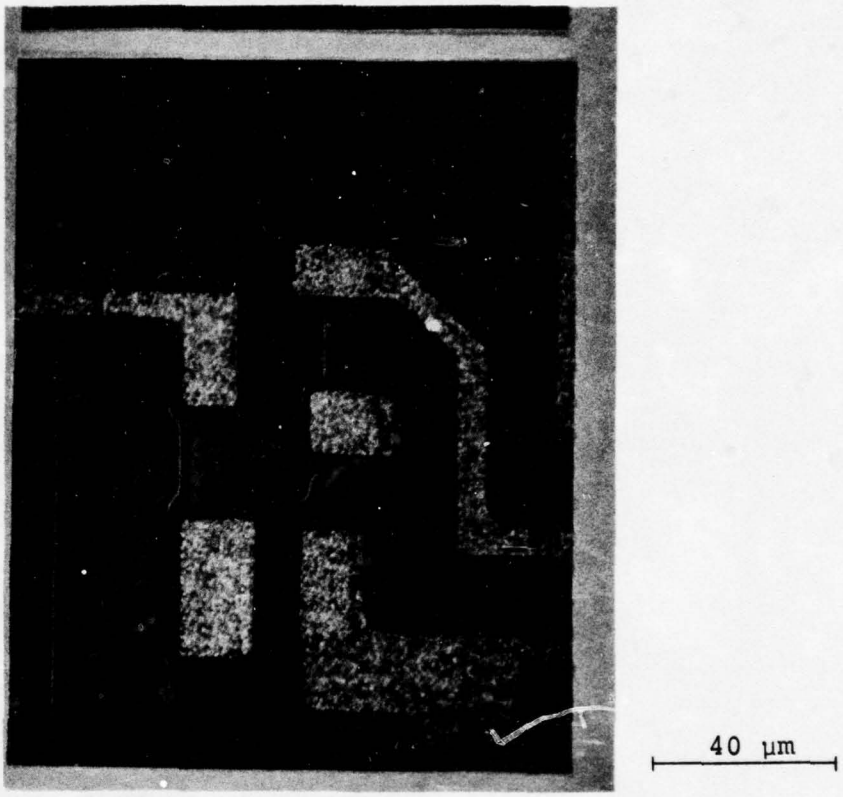


FIGURE C-6: Q4 is shown. The base diffusion is extended to create R3 and R5. The actual transistor base region is at the bottom of the photo with the Schottky diode at left and emitter at right.

APPENDIX D

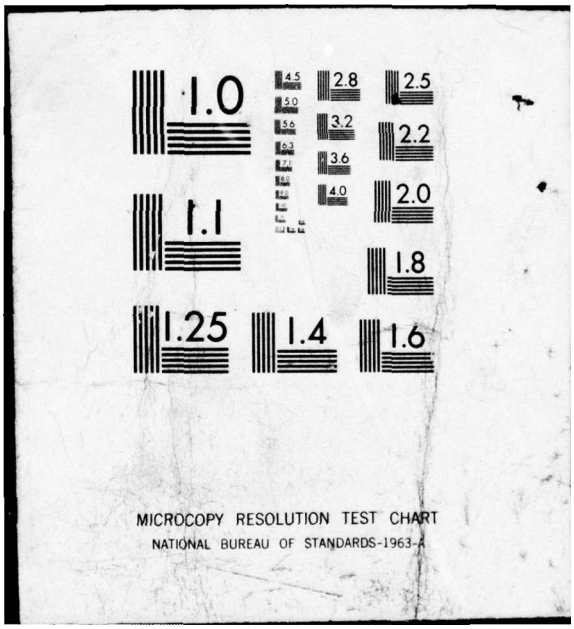
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APPENDIX D

CONSTRUCTION ANALYSIS OF VENDOR A 54S138

STANDARD SCHOTTKY TTL INTEGRATED CIRCUIT IN CERAMIC DIP

ABSTRACT

A Vendor A 1-of-8 decoder demultiplexer, standard Schottky TTL integrated circuit, part number 54S138 was the subject of a detailed construction analysis. The device is in a standard 16-pin ceramic dual-in-line package (CERDIP). Two units were received date coded 7444. The internal wires are aluminum while the single level chip metallization is Pt_xSi_y (ohmic contacts and Schottky barrier diodes)/Ti-W/Al (99.9% pure). The chip is entirely coated with vapor deposited SiO_2. No design weaknesses were noted. Poor wire bonding indicated workmanship problems. The chip was mapped.

INTRODUCTION

This analysis was performed as part of an evaluation of this device for Rome Air Development Center. The analysis was designed to document the materials and construction details used in these units and to identify shortcomings in the design or defects in workmanship, if any.

The 54S138 circuit is shown in Figure D-1. It can be broken down into three simpler circuits:

A. Input

The three input circuits designated A, B and C, each logically consist of two inverters in series. The first inverts the input, the second reinverts, reproducing the input.

B. Enable

This is an AND gate with one non-inverting input (designated CS3) and two inverting inputs (CS1, CS2).

C. Output

Each of eight output circuits (designated S through Z) is a NAND gate with four inputs. In each output gate, one

input is the output of the enable circuit. The remaining 3 inputs of each output gate are A or $\overline{A}$, B or $\overline{B}$ and C or $\overline{C}$. Of the eight possible combinations, one inputs each of the output gates.

Thus the logic is as follows: Unless CS3 is 1 and CS1 and CS2 are both 0, all outputs are 1, regardless of the inputs A, B and C. If CS3 is 1, CS1 and CS2 are both 0, then seven of the outputs are 1 and one of the outputs is 0. The following table shows which output will be 0:

TABLE D-1: Logic of 54S138

A	B	C	Output in 0 State (all others in 1 state)
0	0	0	Z
1	0	0	Y
0	1	0	X
1	1	0	W
0	0	1	V
1	0	1	U
0	1	1	T
1	1	1	S

Figure D-2 shows a logic schematic.

RESULTS

The Package

Figure D-3 shows package outline and dimensions. The hermetic seal (tested in another part of the overall evaluation) was fritted glass. The kovar pins, tin plated outside and aluminum clad inside the package, are embedded in the seal. The lids of the two units were marked as follows:

top: 7444
54S138

bottom: 138G 143T

Vendor A purchases its packages from Kyoto Ceramics Company. The packages are 16-lead, SS1, ceramic dual-in-line (CERDIP).

The Chip

The packages were opened by mechanically stressing the lid while forcing a chisel edge into the seal in a controlled manner until the seal fractured. The chip dimensions were 69 X 54.5 X 9.1 mils, and the chip was gold-silicon eutectic die mounted.

The internal wires were ultrasonically bonded, 1 mil diameter Al (manufacturer specifies > 99.9%Al). No bond defects were noted. Microbond pull tests of 6 of the 16 wires in one unit found pull strengths ranging from 0.4 grams-force to 2.9 gm-f with 1.86 average. All wires fractured at the heel of the chip bond. These results show poor wire bonding, probably due to non-optimum bonding parameters.

The chip metallization was a single stratum interconnection scheme with a SiO_2 coating over the entire chip, primarily designed, not as passivation, but for scratch protection during chip handling. The metallization had the following structure: Al on top (> 99.9% pure, claimed by manufacturer), Ti-W below for good adhesion to SiO2 and as a diffusion barrier to Al, and finally Pt_xSi_y in the contact areas for good stable ohmic and Schottky contact.

One unit was cross-sectioned. The top glass was measured to be about 0.6μ thick, somewhat thinner over the metallization. The Al layer of the metallization was about 2.0μ thick, and carries almost all of the current. The Ti-W layer was measured in angle section to be about 4000Å thick. The Al layer is vapor deposited, the Ti-W sputter deposited in an undisclosed ratio. The Pt_xSi_y is formed by sputtering on Pt in a very thin layer, a few hundred angstroms, and sintering to form Pt_xSi_y in the contact areas, followed by blanket etching to remove the Pt elsewhere.

The highest current density was found to exist in the output transistors' emitter metallizations. Here the current is specified at 20mA maximum and the metallization is 8.5μ wide (X 2.0μ thick) resulting in a density of $1.3 \times 10^5 A/cm^2$. Over an oxide step, the density could reach 2×10^5 or higher. MIL-38510 specifies $2 \times 10^5 A/cm^2$ as a maximum density for Al to avoid an unacceptable level of electromigration failures.

The microsection revealed an N-type epitaxial layer of 3.2μ thickness on a P-type substrate (grounded). The manufacturer specified epitaxial thickness is 3μ.

The Components

The chip was photographed and mapped to identify all the components. Figure D-4 shows the chip with all components marked.

The substrate is P-type. Prior to epitaxial layer growth, low resistivity N-type diffusions, subcollectors, are made in positions corresponding to transistors. These provide high conductivity paths from the vicinity of the base-collector junctions to the collector contact diffusions.

After the epitaxial growth, P-type isolation diffusions partition the epitaxial layer into individual collector regions and other components. This diffusion was measured to be about 3.3μ deep. The entire input circuit A is shown in Figure D-5.

The Resistors

P-type base diffusion is used for all of the resistors. This diffusion has a resistivity of about 180 Ω/□ . This sheet resistance was obtained by counting squares and comparing to schematic resistor values shown in Figure D-1.

Cross-sectioning found a depth of about 1.7μ for the base diffusion and 0.9μ for the emitter diffusion. The manufacturer specified depths were, respectively, 2.5μ and 1.5μ.

The Diodes

Clamping diodes in the input provide protection from negative voltage spikes. For each input a clamping diode to ground is provided. A contacted annular P-type base diffusion surrounding the Schottky barrier contact diode results in a p-n junction-Schottky barrier hybrid diode. References 3 and 5 describe the theory and advantages of such a structure.

D1, as seen in the electrical schematic, Figure D-1, is a Schottky barrier diode in series with Q3 collector,

with the current direction, in forward bias, toward Q3. To accomplish this, the isolated epitaxial region comprizing the Q3 collector is contacted without an N+ type contact enhancement diffusion, see Figure D-6. This results in a rectifying metal-semiconductor interface.

D2 and D3 are created in an adjacent isolated epitaxial region. D3 is, as D1, a Schottky barrier diode in series with Q3 collector but "pointing" the opposite direction. Metal contact without enhancement diffusion creates the diode, D3. That metallization also contacts an enhancement diffusion in the Q3 collector to provide ohmic contact to Q3. An N+-type diffusion within a P-type diffusion creates the p-n junction diode, D2. Contact to the semiconductor side of D3 is made using an N+-type enhancement diffusion and a metallization patch. A contact hole opens the N+ side of D2 and metallization makes ohmic contact and connects to Q3 base.

Transistors

Q1A, the input transistor for input circuit A is shown in Figure D-7. The isolated epitaxial region comprising the collector is rectangular 44.5μ X 79.8μ with a collector contact enhancement diffusion (c.c.e.d.) 16.5μ X 6.7μ and a contact hole 13.3μ X 9.4μ. In all those transistors with base to collector Schottky diodes, the contact hole in the base oxide exposes both part of the base region and part of the collector. When the metallization is deposited within the hole, it creates the ohmic contact to the base region and also creates the Schottky diode from base to collector. This occurs because of the relative doping of the base region (high doping → ohmic contact) versus the epitaxial region (low doping → rectifying Schottky contact). Hosack[1] reports a barrier height of 0.82eV for Pt_xSi_y on n-type silicon. Also M. Kamoshida and T. Okada[2] report that the contact resistance of Pt_xSi_y on highly doped Si is essentially the same as that found for Al on Si.

For Q1, the overall base dimensions are 23.2μ X 17.3μ. The Schottky diode area is 25μ X 18.5μ. The contact hole is 18.5μ X 30.5μ. The emitter is diffused into the base region away from the Schottky diode and is 6.2μ X 7.4μ with a contact hole of 5.7μ X 4.4μ.

Similar dimensions for other selected transistors are presented. Refer to Figure D-1 for component designations.

Q9E (includes D4E):

Collector	101μ X 54.5μ
cced	32.2μ X 19.8μ
first contact hole	8μ X 32μ
second contact hole (no cced, thus creating D4E)	33.5μ X 15.8μ
Base	24.2μ X 33μ
Schottky diode area	12.4μ X 33.5μ
contact hole	17.4μ X 33.5μ
Emitter	7.5μ X 24.8μ
contact hole	3.7μ X 20μ

Q1S

Collector	170μ X 44.6μ
cced	16.7μ X 6.8μ
contact hole	16.7μ X 9.9μ
Base	80.5μ X 18μ
Schottky diode area	29.2μ X 18.5μ
contact hole	31.5μ X 18.5μ
Emitter (1 of 4)	7.4μ X 9.3μ
contact hole (1 of 4)	3.7μ X 5μ

Q3S, Q4S (share common collector):

Collector	145μ X 68.8μ
cced	120μ X 11.2μ
contact hole	119μ X 8.7μ
Base, Q3S	24.2μ X 27.3μ
Schottky diode area	8.1μ X 28.5μ
contact hole	11.8μ X 28.5μ
Emitter, Q3S	6.8μ X 18.5μ
contact hole	14.8μ X 4.3μ
Base, Q4S (not Schottky)	32.2μ X 58.2μ
contact hole	8.4μ X 54μ
Emitter, Q4S	8.6μ X 49.6μ
contact hole	5.2μ X 46μ

Q5S:

Collector	81.8μ X 142.5μ
cced	120.3μ X 15.5μ
contact hole	118μ X 15μ
Base	43μ X 119μ
Schottky diode area	12μ X 105μ
contact hole	18μ X 112μ
Emitter	8.7μ X 111μ
contact hole	5.6μ X 107μ

CONCLUSIONS

No design weaknesses were found. However, the wire bond pull testing indicates poor workmanship in that area. Also, it was noted that the deposited glass exhibited moderate to severe cracking.

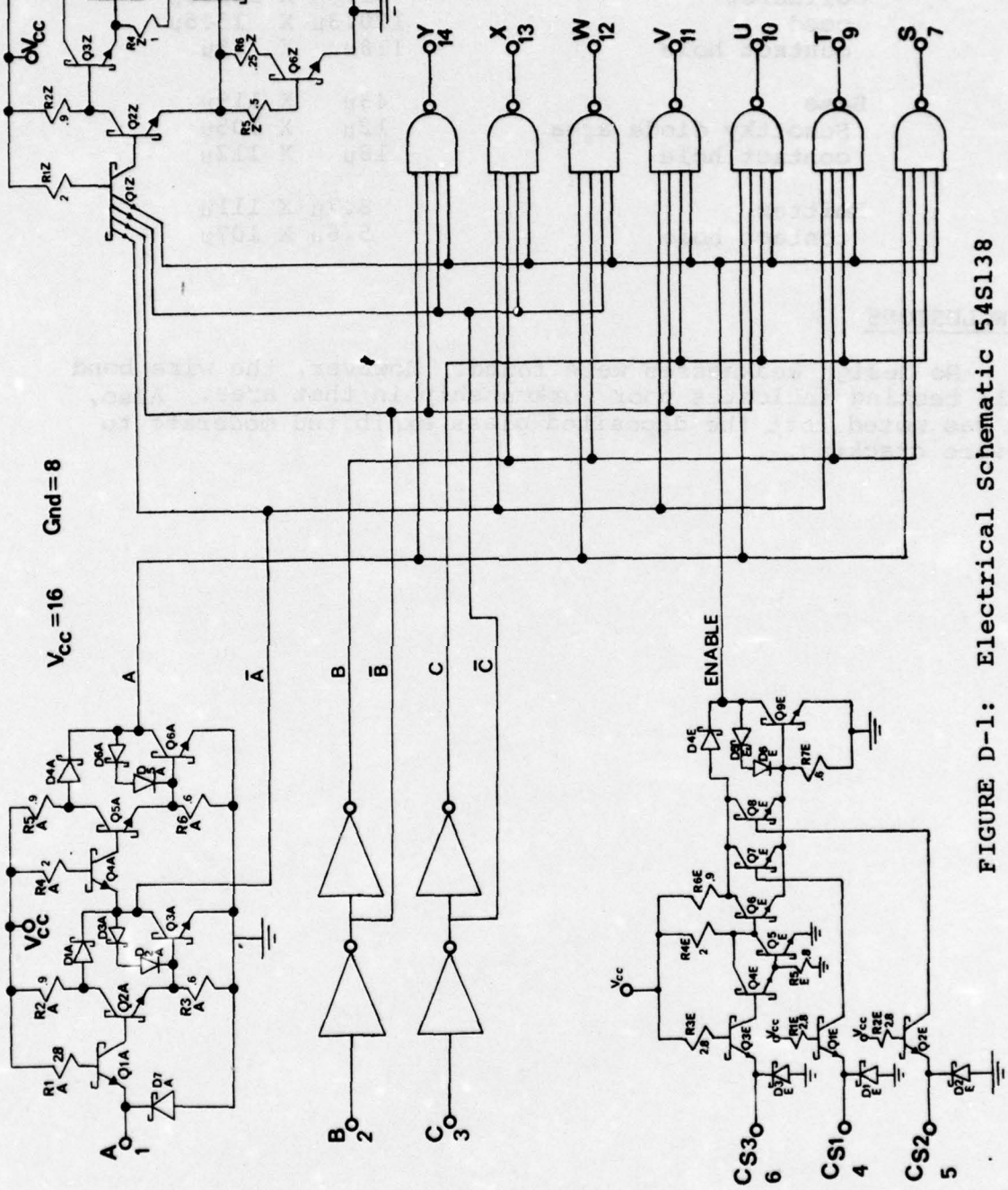


FIGURE D-1: Electrical Schematic 54S138

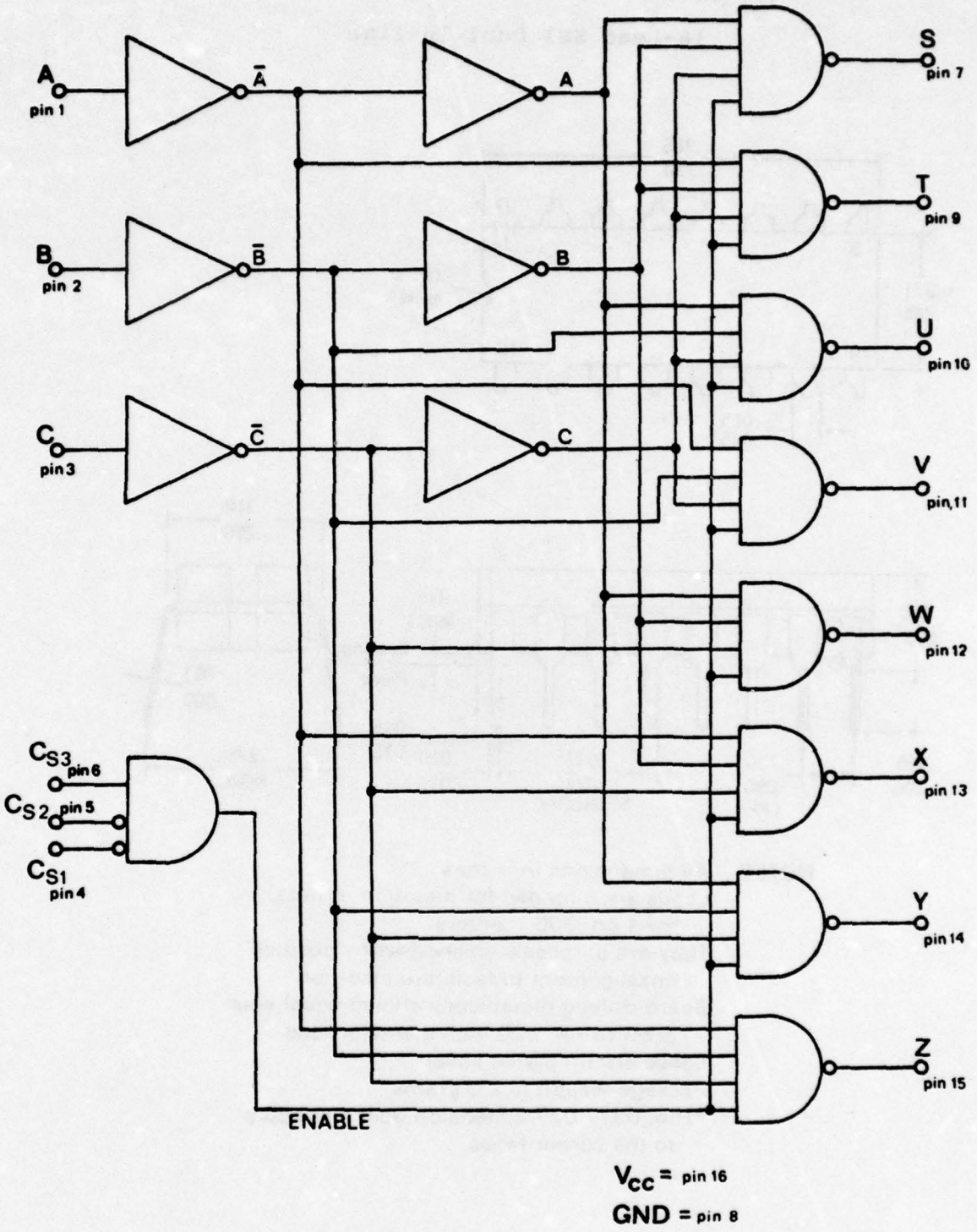
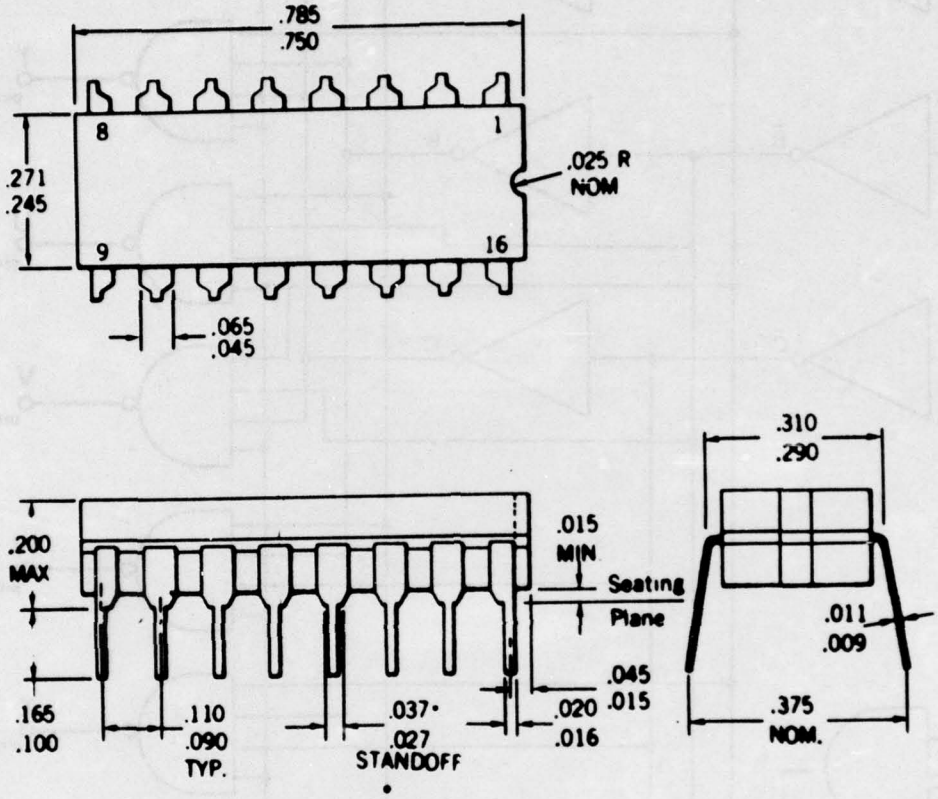


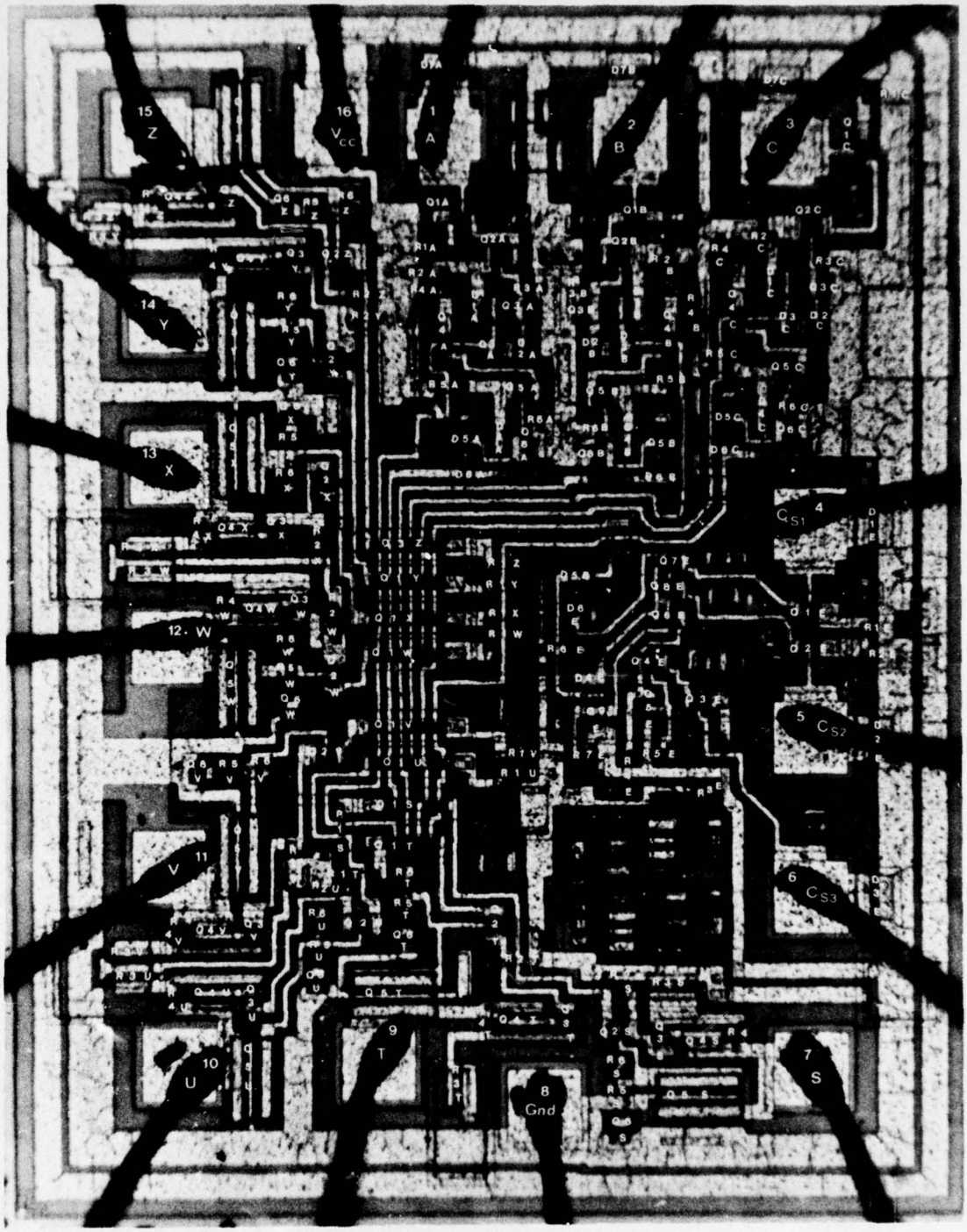
FIGURE D-2: Logic Layout

16-Lead SSI Dual In-line



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
*The .037/.027 dimension does not apply to the corner leads

FIGURE D-3: Package outlines.



200 μm

FIGURE D-4: Overall Photograph of Chip with Map Overlay

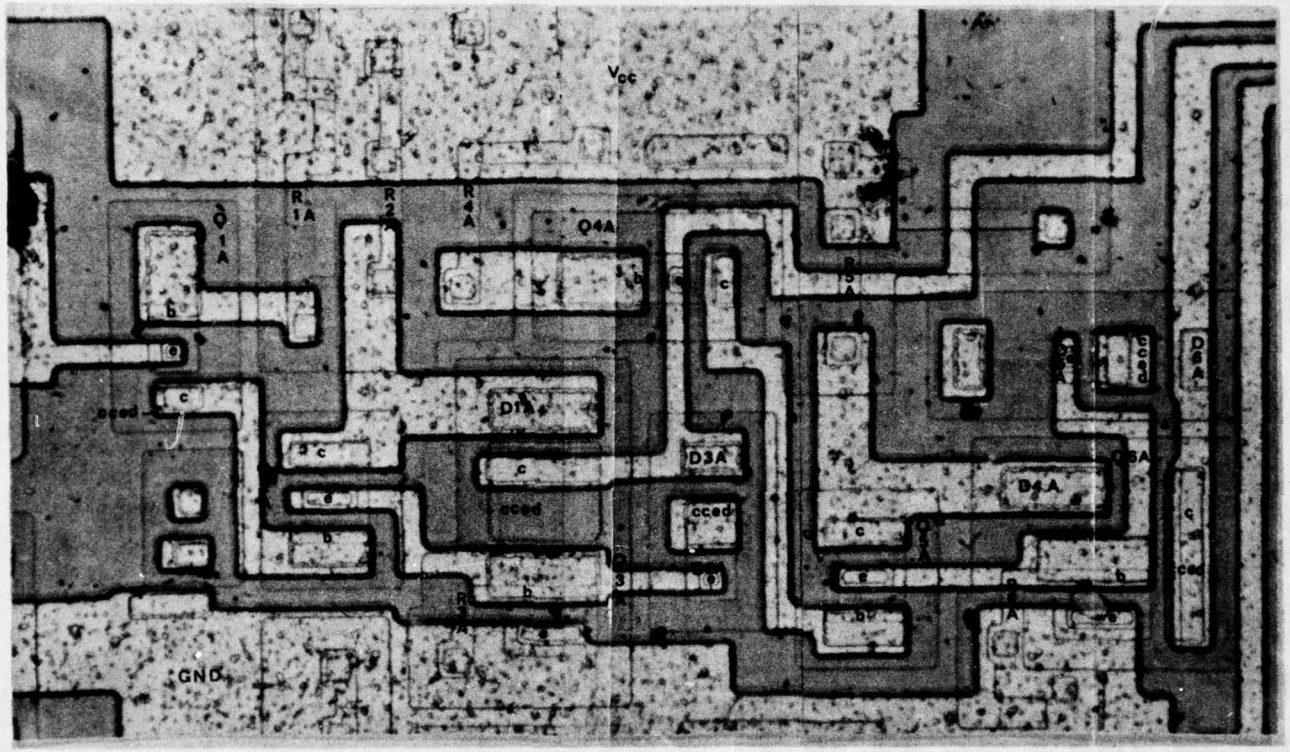


FIGURE D-5: Entire A input circuit.

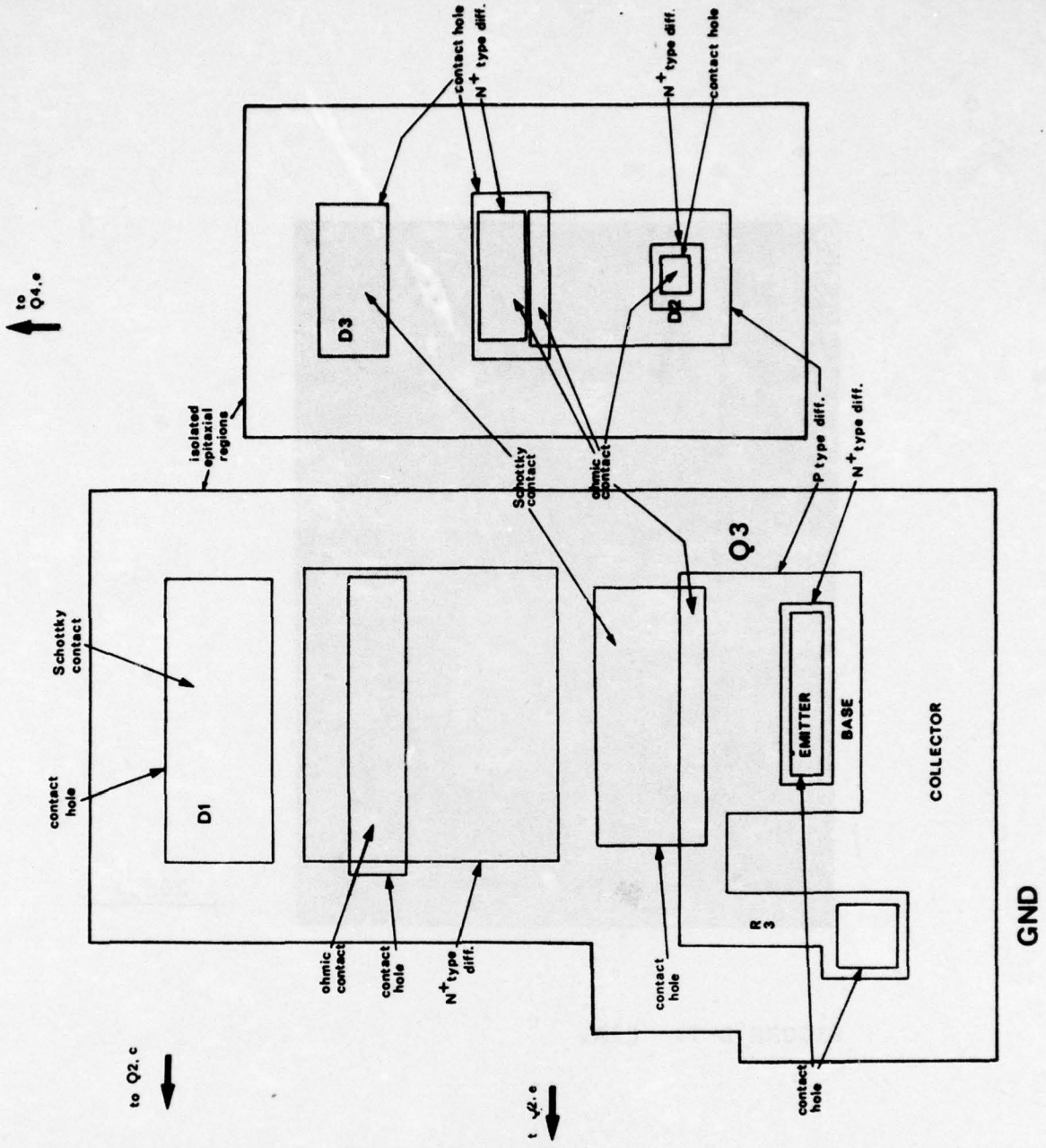


FIGURE D-6: Scale drawing of transistor Q3A and diodes D1, D2 and D3, showing construction. D1 is a metal-semiconductor Schottky barrier diode in series with the collector of Q3. D3 is also but the direction of forward current is away from Q3 collector (opposite of D1). D2 is a p(base diffusion)-n(emitter diffusion) junction diode. Also the base contact hole of Q3 exposes part of the collector region to permit the formation of the Schottky barrier collector-base Baker clamp diode. (Shaded areas represent chip metallization.)

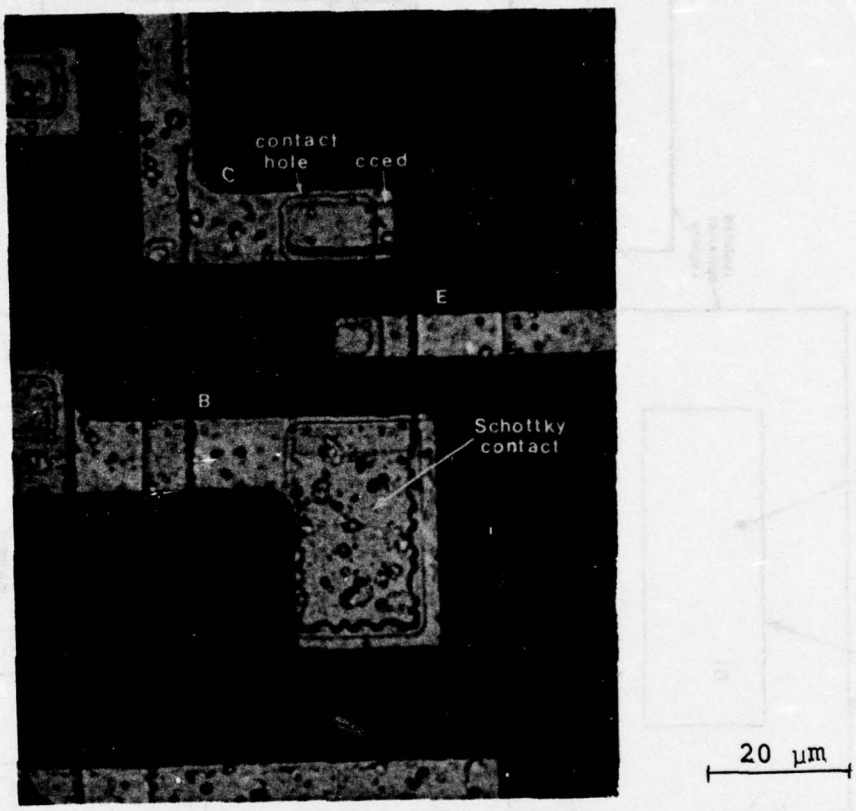


FIGURE D-7: Q1A.

APPENDIX E

APPENDIX E

CONSTRUCTION ANALYSIS OF VENDOR B 93S138

STANDARD SCHOTTKY TTL INTEGRATED CIRCUIT IN CERAMIC DIP

ABSTRACT

A Vendor B 1-of-8 decoder demultiplexer, standard Schottky part number 93S138 was the subject of a detailed construction analysis. The device is in a standard 16-pin ceramic dual-in-line package (CERDIP). Two units were received date coded 7441. The internal wires are aluminum while the single level chip metallization is Pt_xSi_y (ohmic contacts and Schottky barrier diodes)/Ti-W/Al (99.9% pure). The chip is entirely coated with vapor deposited SiO_2. No design weaknesses or workmanship defects were noted. The chip was mapped.

INTRODUCTION

This analysis was performed as part of an evaluation of this device for Rome Air Development Center. The analysis was designed to document the materials and construction details used in these units and to identify shortcomings in the design or defects in workmanship, if any.

The 93S138 circuit is shown in Figure E-1. It can be broken down into three simpler circuits:

A. Input

The three input circuits designated A, B and C, each logically consist of two inverters in series. The first inverts the input, the second reinverts, reproducing the input.

B. Enable

This is an AND gate with one non-inverting input (designated G1) and two inverting inputs (G2A, G2B).

C. Output

Each of eight output circuits (designated S through Z) is a NAND gate with four inputs. In each output gate, one input is the output of the enable circuit. The remaining 3

inputs of each output gate are A or $\overline{A}$, B or $\overline{B}$ and C or $\overline{C}$. Of the eight possible combinations, one inputs each of the output gates.

Thus the logic is as follows: Unless G1 is 1 and G2A and G2B are both 0, all outputs are 1, regardless of the inputs A, B and C. If G1 is 1, G2A and G2B are both 0, then seven of the outputs are 1 and one of the outputs is 0. The following table shows which output will be 0:

TABLE E-1: Logic of 93S138

A	B	C	Output in 0 State (all others in 1 state)
0	0	0	S
1	0	0	T
0	1	0	U
1	1	0	V
0	0	1	W
1	0	1	X
0	1	1	Y
1	1	1	Z

Figure E-2 shows a logic schematic.

RESULTS

The Package

Figure E-3 shows package outline and dimensions. The hermetic seal (tested in another part of the overall evaluation) was fritted glass. The kovar pins, tin plated outside and aluminum clad inside the package, are embedded in the seal. The lids of the two units were marked as follows:

top: 7441
93S138

and bottom: unmarked

Vendor B manufactures about 85% of its packages in-house, the balance being purchased from Kyoto Ceramics Company. The packages are 16-lead, SS1, ceramic dual-in-line (CERDIP).

The Chip

The packages were opened by mechanically stressing the lid while forcing a chisel edge into the seal in a controlled manner until the seal fractured. The chip dimensions were 78.3 X 66.7 X 9.8 mils, and the chip was gold-silicon eutectic die mounted.

The internal wires were ultrasonically bonded, 1 mil diameter Al (manufacturer specifies > 99.9% Al). No bond defects were noted. Microbond pull tests of 5 of the 16 wires in one unit found pull strengths ranging from 2.1 grams-force to 3.8 gm-f with 2.78 average. Two bonds fractured in the wires themselves, away from either bond. Three wires fractured at the heel of the chip bond.

The chip metallization was a single stratum interconnection scheme with a SiO_2 coating over the entire chip, primarily designed as passivation. The metallization had the following structure: Al on top (> 99.9% pure, claimed by manufacturer), Ti-W below for good adhesion to SiO_2 and as a diffusion barrier to Al, and finally Pt_xSi_y in the contact area for good stable ohmic and Schottky contact.

One unit was cross-sectioned. The top glass was measured to be about 1.5μ thick, somewhat thinner over the metallization. The Al layer of the metallization was about 1.6μ thick, and carries almost all of the current. The Ti-W layer was measured in angle section to be about 4000Å thick. The Al layer is vapor deposited, the Ti-W sputter deposited in an undisclosed ratio. The Pt_xSi_y is formed by sputtering on Pt in a very thin layer, a few hundred angstroms, and sintering to form Pt_xSi_y in the contact areas, followed by blanket etching to remove the Pt elsewhere.

The highest current density was found to exist in the output transistors emitter metallizations. Here the current is specified at 20mA maximum and the metallization is 9μ wide (X 1.6μ thick) resulting in a density of $1.5 \times 10^5 A/cm^2$. Over an oxide step, the density could reach 2×10^5 or higher. MIL-38510 specifies $2 \times 10^5 A/cm^2$ as a maximum density for Al to avoid an unacceptable level of electromigration failures.

The microsection revealed an N-type epitaxial layer of 3.2μ thickness on a P-type substrate (grounded). The manufacturer specified epitaxial thickness is 3μ.

The Components

The chip was photographed and mapped to identify all the components. Figure E-4 shows the chip with all components marked.

The substrate is P-type. Prior to epitaxial layer growth, low resistivity N-type diffusions, subcollectors, are made in positions corresponding to transistors. These provide high conductivity paths from the vicinity of the base-collector junctions to the collector contact diffusions.

After the epitaxial growth, P-type isolation diffusions partition the epitaxial layer into individual collector regions and other components. This diffusion was measured to be about 3.3μ deep.

The Resistors

P-type base diffusion is used for all of the resistors. This diffusion has a resistivity of about 230 Ω/□. This sheet resistance was obtained by counting squares and comparing to schematic resistor values shown in Figure E-1.

Cross-sectioning found a depth of about 1.7μ for the base diffusion and 0.9μ for the emitter diffusion. The manufacturer specified depths were, respectively, 2.5μ and 1.5μ.

The Diodes

Clamping diodes in the input provide protection from negative voltage spikes. For each input a clamping diode to ground is provided as shown in Figure E-5. The contacted annular P-type base diffusion surrounding the Schottky barrier contact diode results in a p-n junction-Schottky barrier hybrid diode. References 5 and 3 describe the theory and advantages of such a structure.

D2A is created by simply contacting the collector of Q4A, without the collector contact enhancement diffusion (c.c.e.d.) required for ohmic contact.

Transistors

Q1A, the input transistor for input circuit A is shown in Figure E-6. The isolated epitaxial region comprising the collector is rectangular, 72.6μ X 64.7μ with a collector contact enhancement diffusion (c.c.e.d.) 18μ X 16μ and a contact hole 8.7μ X 13.8μ. In all those transistors with base to collector Schottky diodes, the contact hole in the base oxide exposes both part of the base region and part of the collector. When the metallization is deposited within the hole, it creates the ohmic contact to the base region and also creates the Schottky diode from base to collector. This occurs because of the relative doping of the base region (high doping → ohmic contact) versus the epitaxial region (low doping → rectifying Schottky contact). Hosack[1] reports a barrier height of 0.82eV for Pt_xSi_y on n-type silicon. Also M. Kamoshida and T. Okada[2] report that the contact resistance of Pt_xSi_y on highly doped Si is essentially the same as that found for Al on Si.

For Q1, the overall base dimensions are 31μ X 18.4μ. The Schottky diode area is 21μ X 23μ. The contact hole is 23μ X 37μ. The emitter is diffused into the base region away from the Schottky diode and is 8.3μ X 7μ with a contact hole of 4μ X 3.5μ.

Similar dimensions for other selected transistors are presented. Refer to Figure E-1 for component designations.

Q4A (includes D2A):

Collector	261μ X 85.1μ
cced	none
contact hole (which creates D2A)	14.5μ X 10.6μ
Base	59.3μ X 32μ
Schottky diode area	10μ X 58.2μ
contact hole	17.4μ X 58.2μ
Emitter	8.7μ X 48.4μ
contact hole	3.5μ X 40.6μ

Q1S

Collector	96μ X 39μ
cced	8μ X 32μ
contact hole	11μ X 30μ

Base	33μ	X 36μ
Schottky diode area	16.5μ	X 33μ
contact hole	27μ	X 33μ
Emitter	6μ	X 28μ
contact hole	3μ	X 24μ

Q25, Q35 (share common collector):

Collector	139μ	X 83.2μ
cced	12μ	X 54μ
contact hole	$630\mu^2$	
Base, Q25	21.3μ	X 28.6μ
Schottky diode area	$555\mu^2$	
contact hole	$640\mu^2$	
Emitter, Q25	18μ	X 10μ
contact hole	16μ	X 4μ
Base, Q34 (not Schottky)	33.5μ	X 53.8μ
contact hole	40μ	X 7μ
Emitter, Q35	41μ	X 8μ
contact hole	37μ	X 4μ

Q4S:

Collector	155μ	X 97.6μ
first cced	73μ	X 22μ
contact hole	72μ	X 23μ
second cced	73μ	X 22μ
contact hole	52μ	X 23μ
Base	71.3μ	X 77μ
Schottky diode area	18μ	X 61μ
contact hole	31μ	X 64μ
Emitters (2)	6μ	X 64μ (each)
contact holes	2μ	X 60μ (each)

CONCLUSIONS

No design weaknesses were found nor any workmanship defects observed.

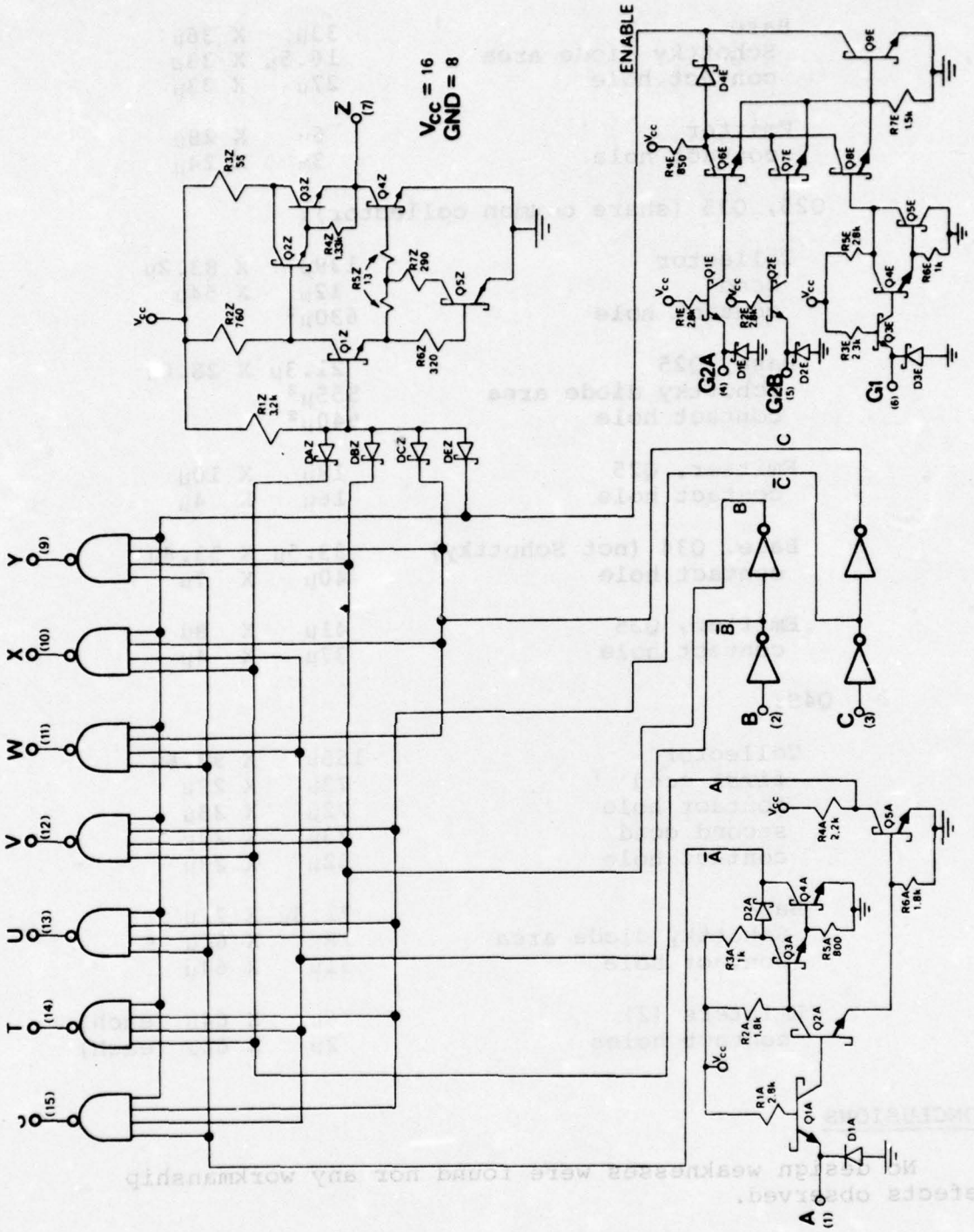


FIGURE E-1: Electrical Schematic

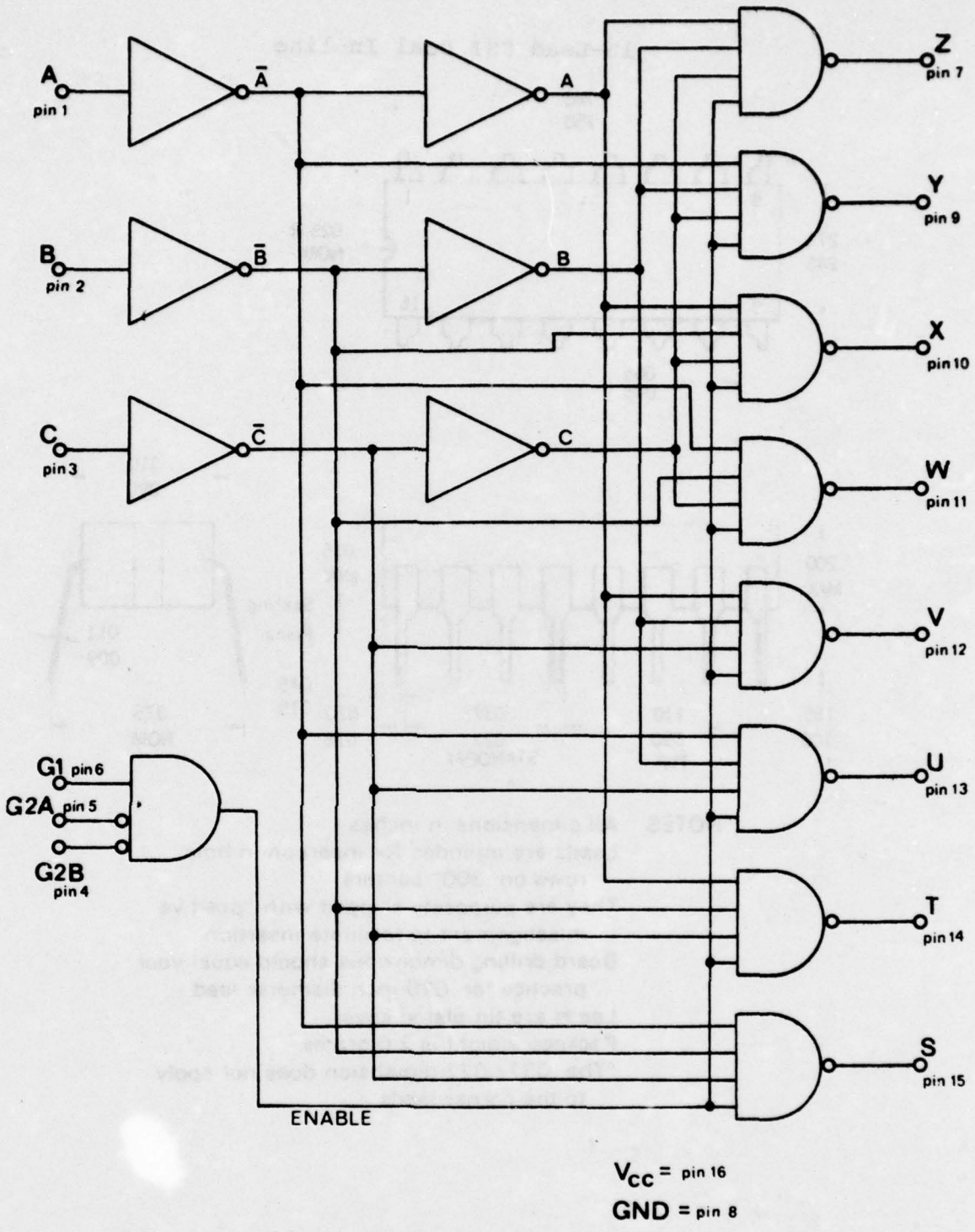
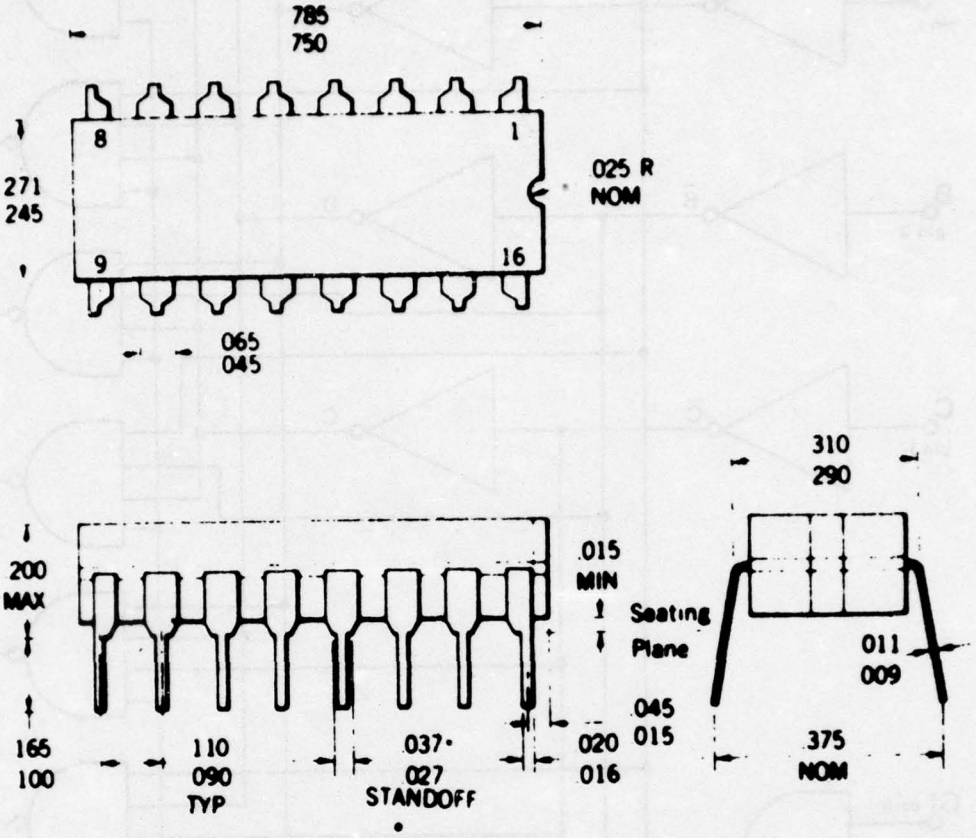


FIGURE E-2: Logic Layout

16-Lead SSI Dual In-line



NOTES
- All dimensions in inches
- Leads are intended for insertion in hole rows on .300" centers
- They are purposely shipped with "positive" misalignment to facilitate insertion
- Board-drilling dimensions should equal your practice for .020 inch diameter lead
- Leads are tin-plated kovar
- Package weight is 2.0 grams
- *The .037/.027 dimension does not apply to the corner leads

FIGURE E-3: Package outlines.

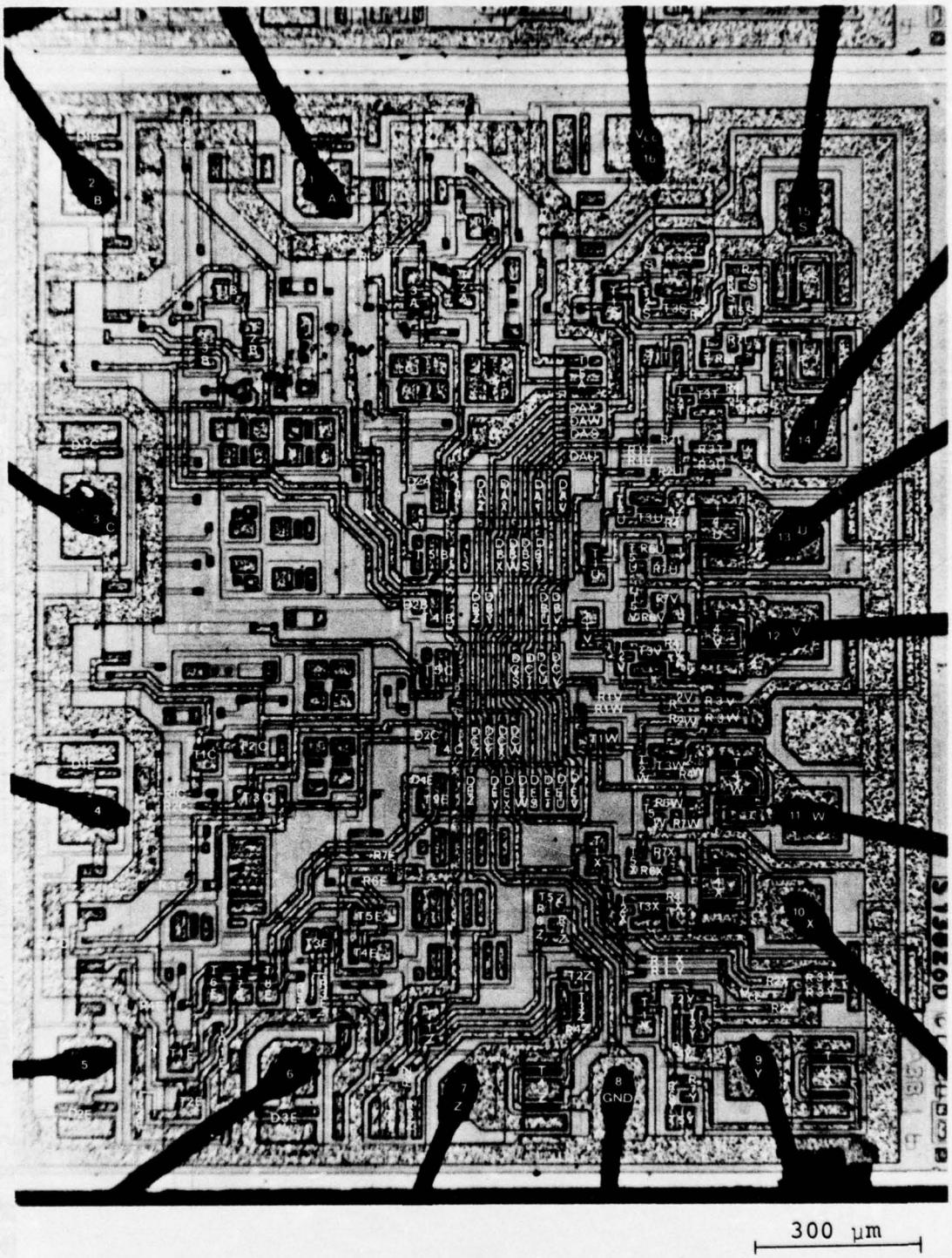


FIGURE E-4: Overall Photograph of Chip with Map Overlay

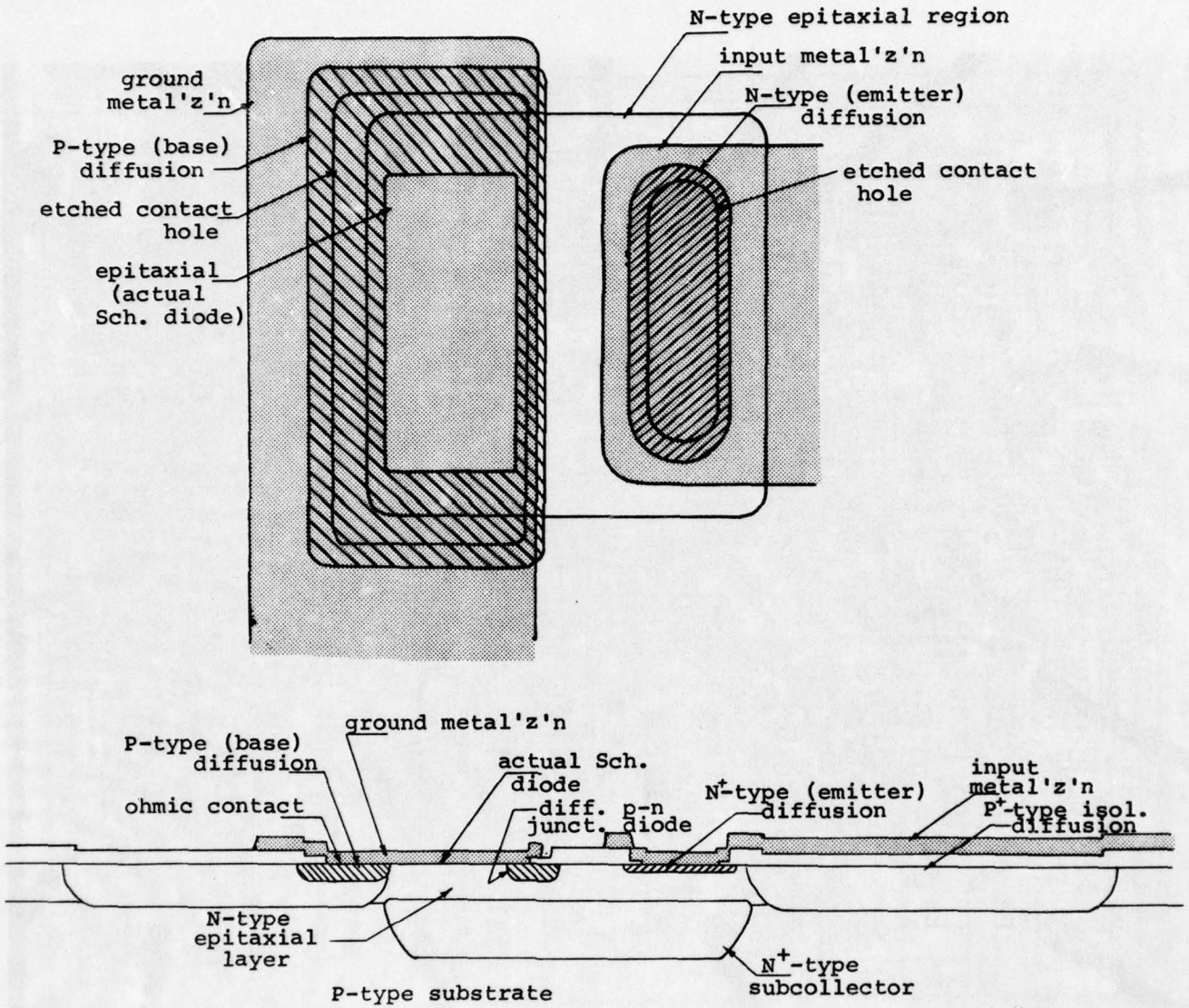


FIGURE E-5: Clamping diode structure viewed from above and in cross-section.

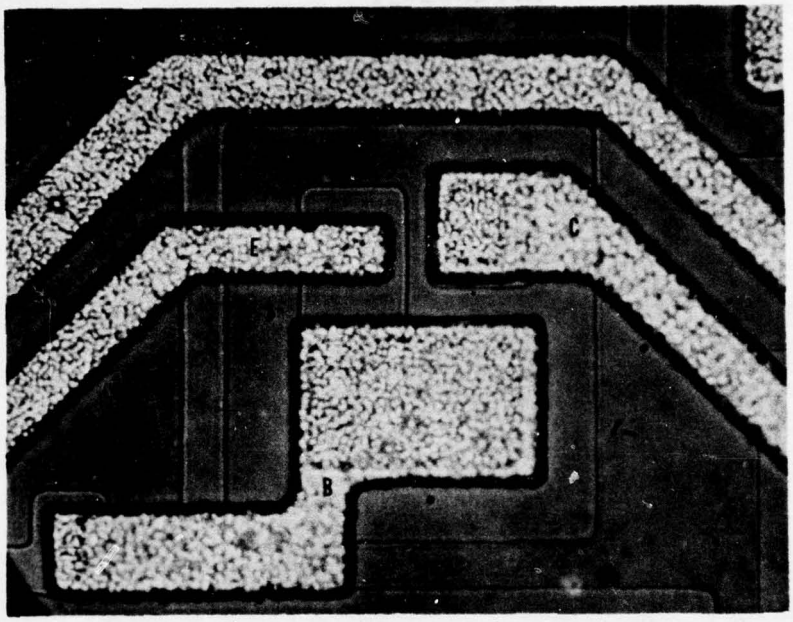


FIGURE E-6: Q1A, the input transistor of input circuit A.

APPENDIX F

APPENDIX F

CONSTRUCTION ANALYSIS OF VENDOR A 54LS00

LOW POWER SCHOTTKY TTL INTEGRATED CIRCUIT IN CERAMIC DIP

ABSTRACT

A Vendor A quadruple dual-input NAND gate, low power Schottky TTL part number 54LS00 was the subject of a detailed construction analysis. The device is in a standard 14-pin ceramic dual-in-line package (CERDIP). Two units were received date coded 7449 and 7407 with no other distinguishing marking. However, it was found that two different chips were used, the major difference being chip size (7407 was larger) and the limiting resistor in the output Darlington (7407 was larger). The internal wires are aluminum while the single level chip metallization is Pt_xSi_y (ohmic contacts and Schottky barrier diodes)/Ti-W/Al (99.9% pure). The chip is entirely coated with vapor deposited SiO_2 for handling purposes only. No design weaknesses or workmanship defects were noted. The chip was mapped.

INTRODUCTION

This analysis was performed as part of an evaluation of this device for Rome Air Development Center. The analysis was designed to document the materials and construction details used in these units and to identify shortcomings in the design or defects in workmanship, if any.

RESULTS

The Package

Both packages were identical except for date code marking. Figure F-1 shows package outline and dimensions. The hermetic seal (tested in another part of the overall evaluation) was fritted glass. The pins, tin plated kovar, are embedded in the seal. The lids of the two units were marked as follows:

#1, top:	7449 54LS00
and bottom:	S00A 49R

#2, top: 7407
54LS00

and bottom: S00 07T

The packages are purchased by Vendor A from Kyoto Ceramics Company, are 14-lead, manufactured in accordance with JEDEC (TO-116) SSI, ceramic dual-in-line (CERDIP).

The Chips

The packages were opened by mechanically stressing the lid while forcing a chisel edge into the seal in a controlled manner until the seal fractured. Upon opening, it was found that the two chips were different. The earlier date code (7407), unit no. 2, contained a larger chip than that in date code 7449, unit no. 1. The dimensions of each were as follows:

#1, d.c. 7449: 43.3 X 38.3 X 6.7 mils

#2, d.c. 7407: 52.2 X 52.2 X 8.6 mils

Each used a gold-silicon eutectic die mount.

The internal wires were, in both units, ultrasonically bonded, 1 mil diameter Al (manufacturer specified > 99.9% Al). No bond defects were noted. Microbond pull testing of 4 of the 14 wires in unit no. 1 found pull strengths ranging from 2.4 grams-force to 2.6 gm-f with 2.55 ave. All bonds fractured in the wires themselves, away from either bond. Microbond pull testing of 4 of the 14 wires in unit no. 2 found pull strengths ranging from 1.7 gm-f to 2.6 gm-f with 2.4 ave. Three of the four wires fractured at the heel of the chip bond, the fourth in the wire away from the bonds. The 1.7 gm-f wire is to be considered slightly weaker than should be consistently achievable with well controlled bonding parameters and a good standard of workmanship.

The chip metallization was a single stratum interconnection scheme with a SiO_2 coating over the entire chip, primarily designed, not as passivation, but as scratch protection during chip handling. The metallization had the following structure: Al on top (> 99.9% pure, claimed by manufacturer), Ti-W below for good adhesion to Si and SiO_2 and as a diffusion barrier to Al, and finally Pt_xSi_y in the contact areas for good stable ohmic and Schottky contact.

Unit no. 1, d/c 7449, only, was cross-sectioned since it was the more recent product. The top glass was measured to be about 2.0μ thick, somewhat thinner over the metallization. The Al layer of the metallization was about 2.0μ thick, and carries almost all of the current. The Ti-W layer was measured in angle section to be about 4000Å thick. The Al layer is vapor deposited, the Ti-W sputter deposited in an undisclosed ratio. The Pt_xSi_y is formed by sputtering on Pt a very thin layer, a few hundred angstroms, and sintering to form Pt_xSi_y in the contact areas, followed by blanket etching to remove the Pt elsewhere.

A Sloan DekTak Profiler was used to measure the pyrolytic oxide thickness on each chip. On chip no. 1 a thickness of 1.8μ was found, confirming the cross-section results to within 2000A or 10%. On chip no. 2, d/c 7407, a thickness of 1.2μ for the pyrolytic oxide was found.

The highest current density in both chips was found to exist in the output transistors' collector metallizations. Here the current is specified at 4mA maximum and in chip #1 the metallization is 21μ wide (X 2.0μ thick) resulting in a density of $\sim 10^4$ A/cm^2. Over an oxide step, the density could reach 1.5 X 10^4 or higher. In chip #2, the width of the metallization in the output collector is 18μ. Assuming the same metallization thickness (which is supported by profiler evidence) the current density is about 8.5 X 10^3 A/cm^2. Over an oxide step, the density could reach 1.2 X 10^4 or higher. MIL-38510 specifies 2 X 10^5 A/cm^2 as a maximum density for Al to avoid an unacceptable level of electromigration failures.

The #1 chip microsection revealed an N-type epitaxial layer of 4μ thickness on a P-type substrate (grounded). The manufacturer specified epitaxial thickness is 3μ.

The Components

Both chips were photographed and mapped to identify all the components. Figures F-2 and F-3 show the logic layout of the gates as relates to the external pins with Figure F-3 showing the electrical schematic of one gate. Figures F-4 and F-5 show the chips with all components marked.

The substrate is P-type. Prior to epitaxial layer growth, low resistivity N-type diffusions, subcollectors, are made in positions corresponding to transistors. These provide high conductivity paths from the vicinity of the base-collector junctions to the collector contact diffusions.

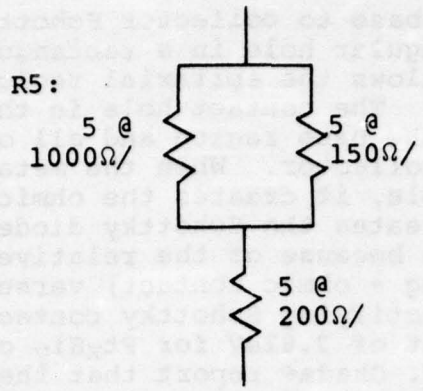
After the epitaxial growth, P-type isolation diffusions partition the epitaxial layer into individual collector regions and other components. This diffusion was measured to be about 4.8μ deep.

The Resistors

A separate P-type diffusion is used for some of the resistors, base diffusion for others. The "resistor" diffusion is higher resistivity, about 1000 Ω/ than the base diffusion, about 200 Ω/□. These are manufacturer specified sheet resistances and were confirmed by counting squares and comparing to schematic resistor values shown in Figure F-3. In chip #1, resistors R1, R2 and R3 (there are four of each) are diffused into two separate isolated regions of the epitaxial layer (high resistivity). R1 and R2 are 23 squares and 8 squares, respectively which, at 1000 Ω/□, agrees well with the values in Figure F-3. R3 was found by oxide color comparison and cross-sectioning to be an N^+-type low resistivity diffusion (emitter) within a P-type higher resistivity diffusion (base). Figure F-6 shows R3 in unit #1 in which the N^+-type diffusion is about 3 squares. Electrical measurements (specifically I_{OSC}) indicated that the resistor R3 in units with the later date code has a resistance value much lower than 200Ω which is indicated in Figure F-3. The resistance has been estimated at 50Ω. This would correspond to a sheet resistance of 15 to 20 Ω/□. The manufacturer claims the sheet resistance of their emitter diffusion to be proprietary information. R4 in chip no. 1 was measured to be about 6.5 squares and was found to be the high resistivity diffusion by oxide color comparison. Thus the true resistance value is 6000-7000Ω as stated in Figure F-3. R5 and R6 were found to be the high resistivity diffusion and were about 1 1/2 squares and 3 squares respectively.

Cross-sectioning found a depth of about 1.2μ for the high resistivity diffusion. The base diffusion was about 2.0μ and the emitters diffusion about 0.9μ. The manufacturer specified depths were, respectively, 1μ, 1.5μ and 1μ.

Chip no. 2 (date code 7407) was inspected and photographed in a top view. R1, R2, R4, and R6 use the high resistivity (1000 Ω/) P-type diffusion. R1 is about 27 squares, R2 about 8 1/2, R4 about 6 and R6 about 3 squares. These correspond well to the resistor values shown in Figure F-3. R3 is about 1 square and by oxide color comparison was found to be base diffusion. Thus the 200μ resistor value shown in Figure F-3 is achieved in chip no. 2. R5 is a combination of diffusions, high resistivity and moderate resistivity (base), which can be roughly represented as below:



This corresponds to about 1700Ω.

The Diodes

In contrast to the standard Schottky, 54S00, the low power Schottky NAND gates in this device, 54LS00, utilize a pair of input diodes rather than a multiple emitter input transistor. These are designated D1 and D3 in Figure F-3. The clamping diodes, D2 and D4, as in the standard power Schottky, provide protection from negative voltage spikes. For each input an input diode and a clamping diode to ground are combined in a single structure as illustrated in Figure F-7. The contacted annular P-type base results in a p-n junction-Schottky barrier hybrid diode. References 3 and 5 describe the theory and advantages of such a structure. A disadvantage in using such a structure in D1 would be increased propagation delay and accordingly the annular P-type diffusion is omitted here.

D5 is created by simply contacting the collector of Q1, without the collector contact enhancement diffusion (c.c.e.d.) required for ohmic contact. See Figure F-8.

Transistors

Q1, the phase splitting transistor, is shown in Figure F-8. The isolated epitaxial region comprising the collector is rectangular, 55μ X 59μ with a collector contact enhancement diffusion (c.c.e.d.) 11.4μ X 22.2μ and a contact hole 5.7μ X 10.6μ. The epitaxial oxide has a contact hole 9.8μ X 7.3μ to create the Schottky barrier diode D5. The base regions of all

those transistors with base to collector Schottky diodes are annular, i.e., a rectangular hole in a rectangular shaped diffusion. The hole allows the epitaxial region to "surface" within the base region. The contact hole in the base oxide exposes both part of the base region and all of this "surfacing" epitaxial area of the collector. When the metallization is deposited within the hole, it creates the ohmic contact to the base region and also creates the Schottky diode from base to collector. This occurs because of the relative doping of the base region (high doping → ohmic contact) versus the epitaxial region (low doping → rectifying Schottky contact). Hosack[1] reports a barrier height of 0.82eV for Pt_xSi_y on n-type silicon. Also M. Kamoshida and T. Okada[2] report that the contact resistance of Pt_xSi_y on highly doped Si is essentially the same as that found for Al on Si.

For Q1, the overall base dimensions are 40μ X 26.3μ. The Schottky diode area is 18μ X 11μ. The contact hole, which completely exposes the Schottky diode, as well as some base area, is 20μ X 11μ. The emitter is diffused into the base region away from the Schottky diode and is 13μ X 13μ with a contact hole of 6.2μ X 8.2μ.

Q4 is similar to Q1 in construction. It is the output transistor and has two collector contacts, one at either end of the transistor (Figure F-9).

collector	107μ X 86μ
1st c.c.e.d.	66μ X 19μ
contact hole	55μ X 6.6μ
2nd c.c.e.d.	66μ X 12.4μ
contact hole	61μ X 7.4μ
base (overall)	66μ X 45μ
Schottky diode	50μ X 7.2μ
contact hole	55μ X 14.2μ
emitter	55μ X 9.5μ
contact hole	50μ X 5.2μ

Q2 and Q3 are combined within one isolated epitaxial region forming a Darlington pair with a common collector. This collector is 133μ X 76μ. It has a single c.c.e.d. (56μ X 9.5μ) and a single collector contact hole (52μ X 4.5μ). The base of Q2 is irregularly shaped with an area of about $700\mu^2$. A contact hole in the thermal oxide opens part of this base region and extends out to contact the collector region as well, thus forming the collector-base Schottky barrier diode. This contact hole is 21μ X 7.5μ, about 60% of which is over the collector, 40% over the base. The Q2 emitter diffused into this base region is 10μ X 13μ with a contact hole 5.2μ X 8μ.

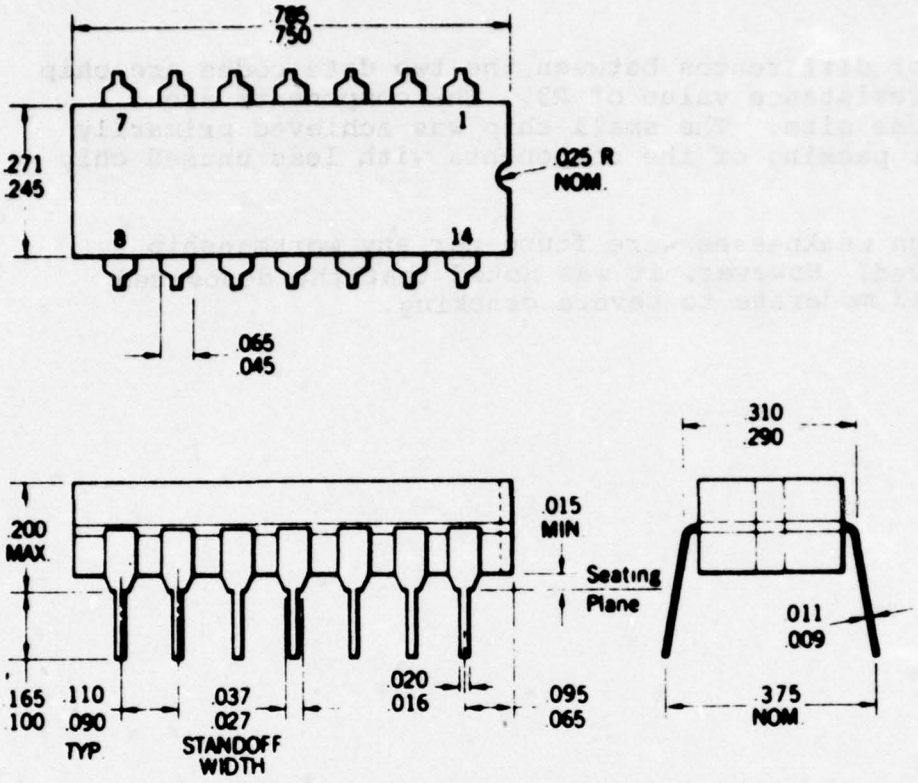
The transistor components have roughly the same dimensions in both units.

CONCLUSIONS

The major differences between the two date codes are chip size and the resistance value of R3. The components are roughly the same size. The small chip was achieved primarily through closer packing of the components with less unused chip space.

No design weaknesses were found nor any workmanship defects observed. However, it was noted that the deposited glass exhibited moderate to severe cracking.

In accordance with
JEDEC (TO-116) outline
14-Lead SSI Dual In-line



NOTES
- All dimensions in inches
- Leads are intended for insertion in hole rows on .300" centers
- They are purposely shipped with "positive" misalignment to facilitate insertion
- Board-drilling dimensions should equal your practice for .020 inch diameter lead
- Leads are tin-plated kovar
- Package weight is 2.0 grams

FIGURE F-1: Package Outlines

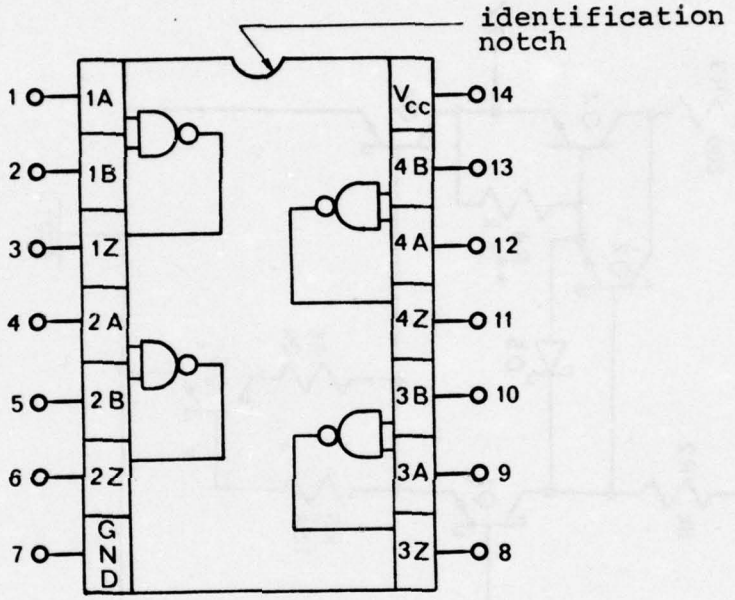
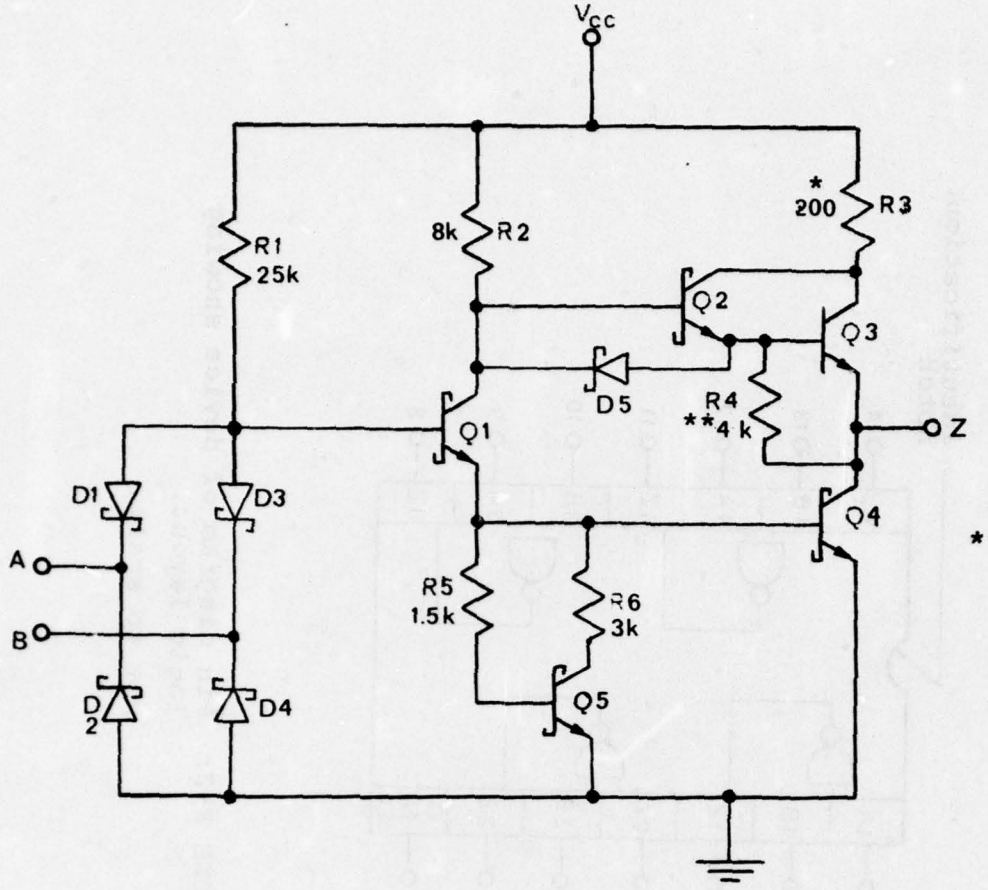


FIGURE F-2: Pin diagram of device showing logic layout.

Not to scale.



*∿50Ω in unit no. 1
**∿6500Ω in unit no. 1

FIGURE F-3: Electrical schematic of one of four NAND gates. Resistor values, provided by the manufacturer, are in Ω.

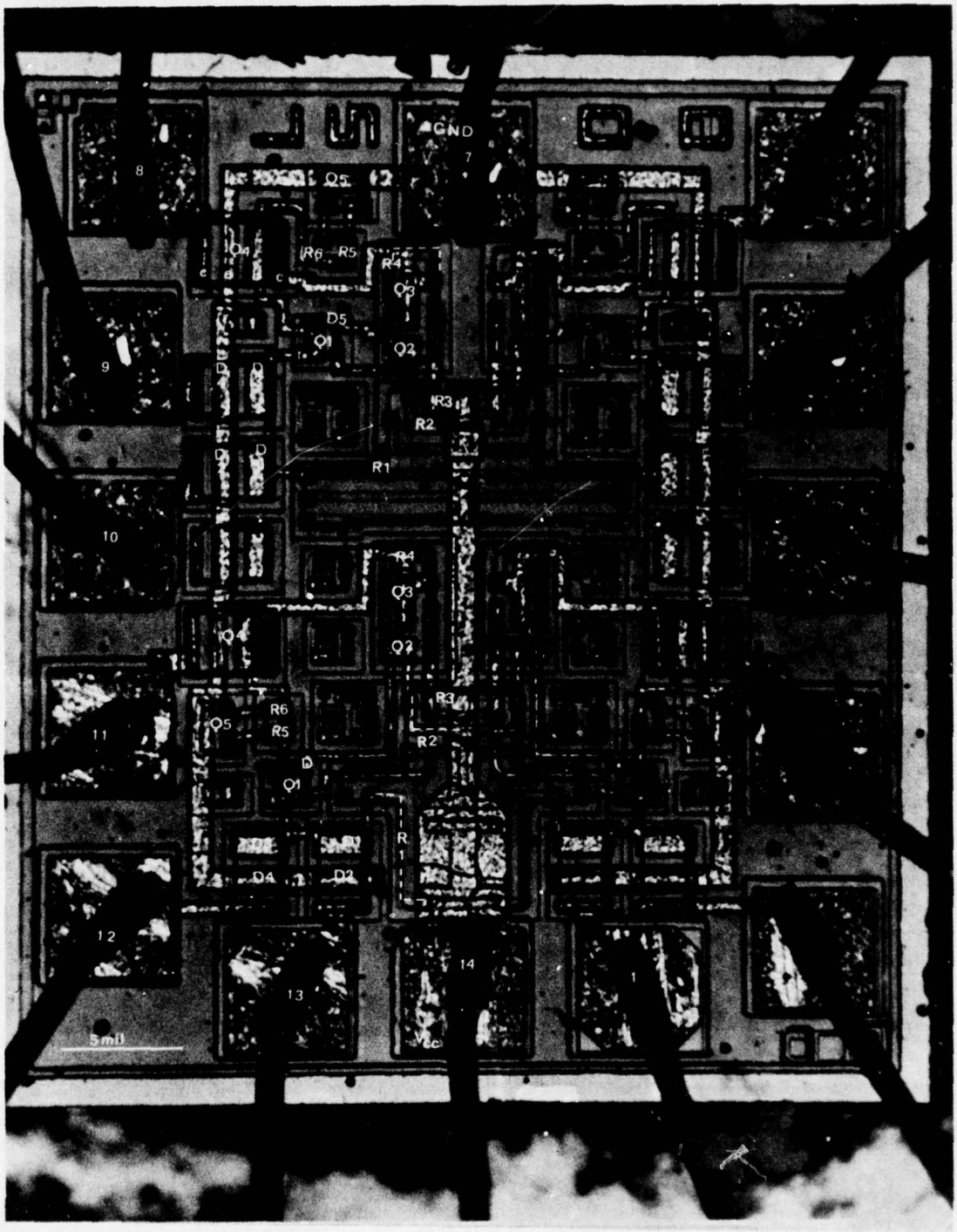


FIGURE F-4: Overall Photograph of Chip with Map Overlay

200 µm

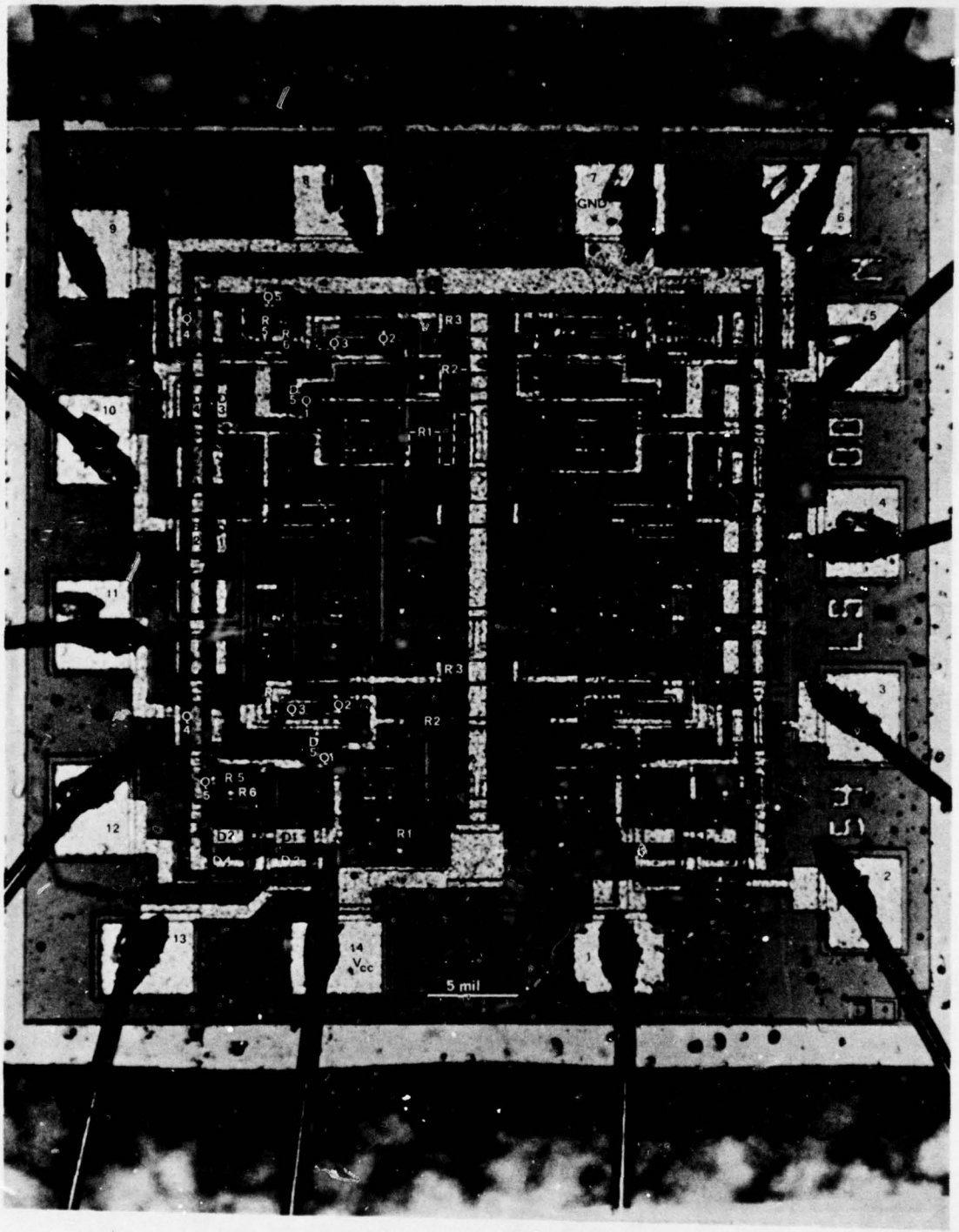


FIGURE F-5: Overall Photograph of Chip with Map Overlay

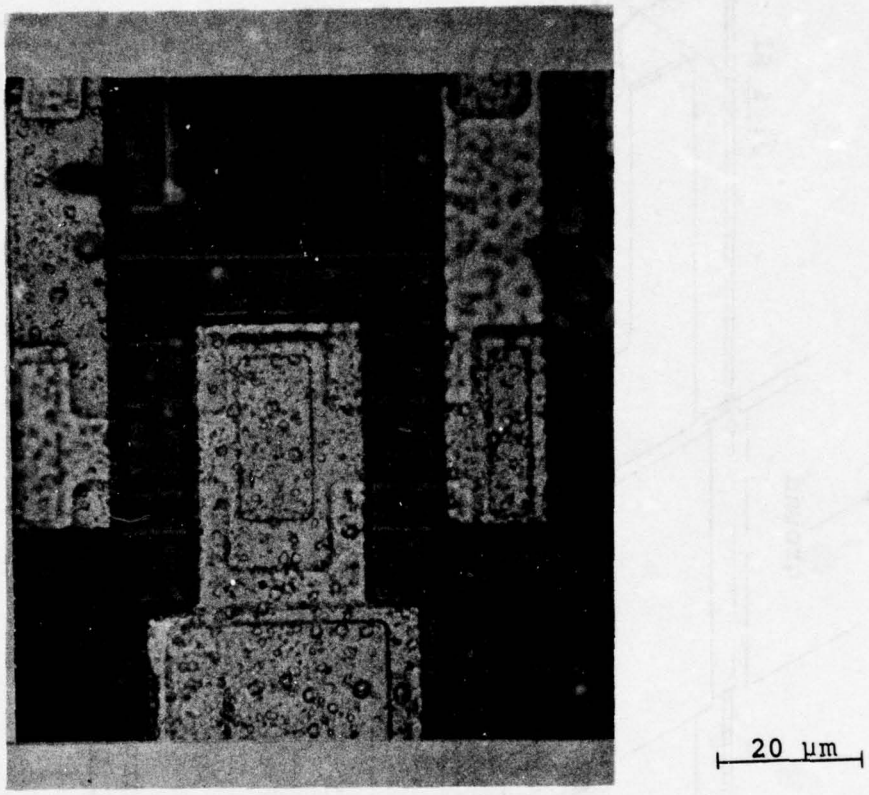


FIGURE F-6: R3 from chip in unit no. 1, date code 7449. In an isolated epitaxial region, base diffusion, P-type, 200 Ω/□ is diffused. Then R3 is formed by an emitter diffusion N^+-type, 15-20 Ω/□ to create a resistance of about 50Ω.

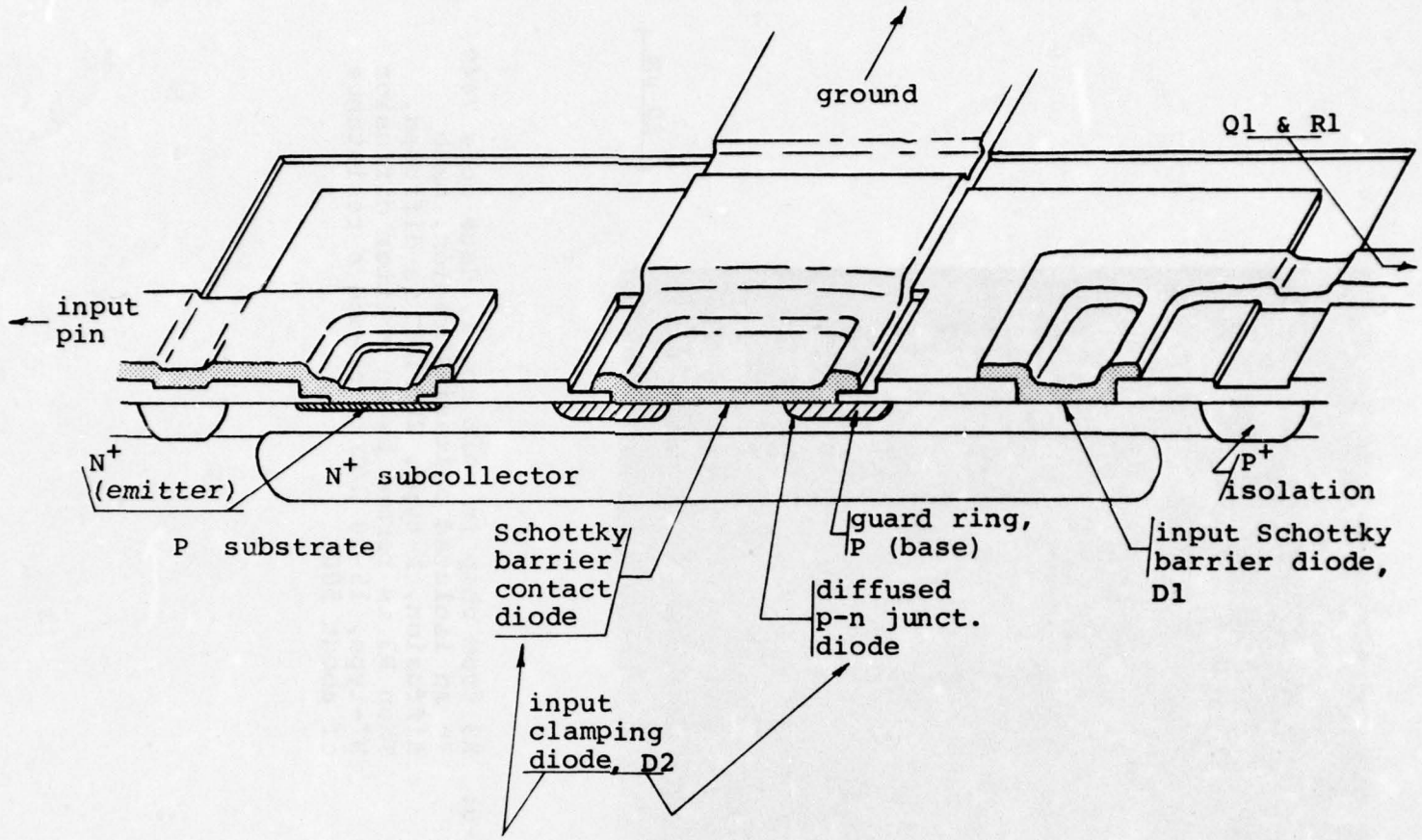


FIGURE F-7: Each of the eight inputs has an input diode (D1) and an input clamping diode (D2) utilizing the above structure. D1 is a pure Schottky barrier diode while D2 is a p-n junction-Schottky barrier hybrid diode.
Not to scale.

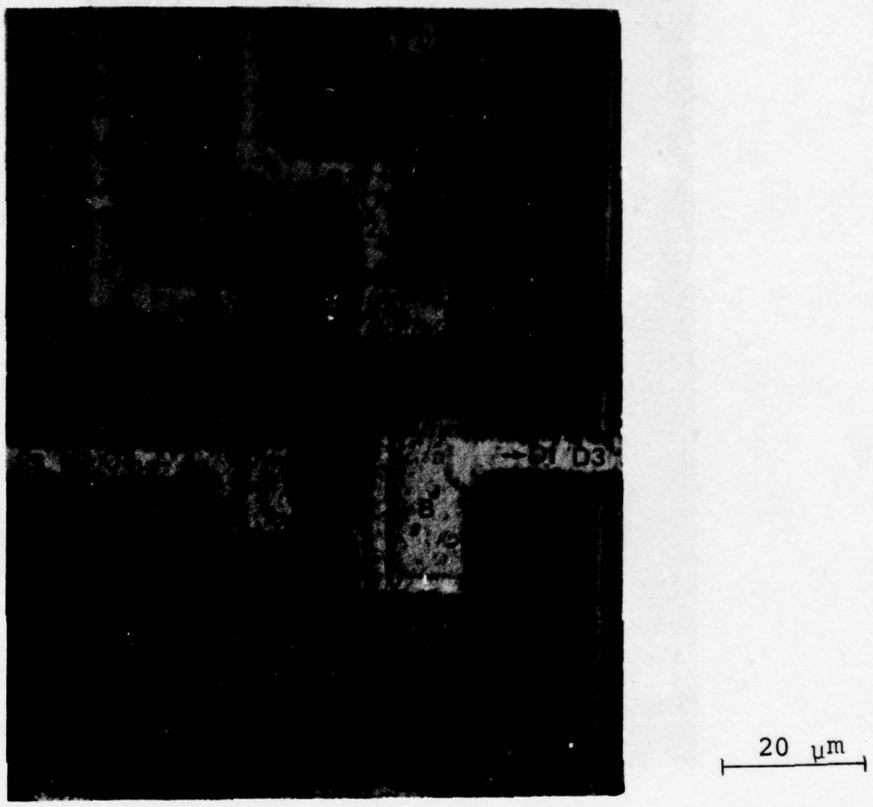


FIGURE F-8: Phase splitting transistor, Q2 of unit no. 1 chip. Base region is at bottom of collector with emitter on left and base contact with Schottky barrier contact diode at right. Collector contact with c.c.e.d. is in upper-right-hand corner of collector. D5 is in upper-left-hand corner.

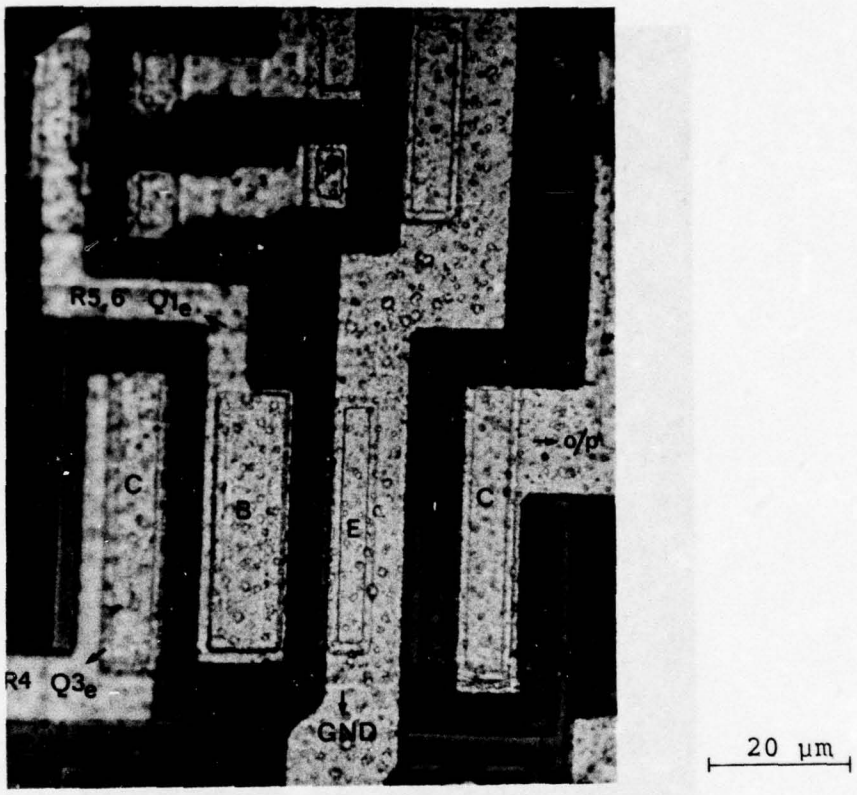


FIGURE F-9: Output transistor, Q4, of unit no. 1 chip. Base region, containing the emitter and the base-collector Schottky barrier diode, is centered between two collector contacts.

APPENDIX G

APPENDIX G

CONSTRUCTION ANALYSIS OF VENDOR B 9LS00

LOW POWER SCHOTTKY TTL INTEGRATED CIRCUIT IN CERAMIC DIP

ABSTRACT

A Vendor B quadruple dual-input NAND gate, a low power T^2L Schottky IC, part number 9LS00 was the subject of a detailed construction analysis. The device is in a standard 14-pin ceramic dual-in-line package (CERDIP). Two units were received date coded 7410. The internal wires are aluminum while the single level chip metallization is Pt_xSi_y (ohmic contacts and Schottky barrier diodes)/Ti-W/Al (99.9% pure). The chip is entirely coated with vapor deposited glass. No design weaknesses or workmanship defects were noted. The chip was mapped.

INTRODUCTION

This analysis was performed as part of an evaluation of this device for Rome Air Development Center. The analysis was designed to document the materials and shortcomings in the design or defects in workmanship, if any.

RESULTS

The Package

This package is a ceramic dual-in-line (CERDIP), in accordance with JEDEC (TO-116), 14 lead SSI. Package dimensions are shown in Figure G-1.

The hermetic seal, tested during another part of the overall evaluation, is fritted glass. The pins, embedded in the seal, are kovar, tin plated externally and aluminum clad internally.

An identification notch at one end identifies pin 1. Package marking was as follows:

Top: 9LS00
7410

Bottom: Unmarked

The manufacturer purchases about 15% of his packages from Kyoto Ceramic, and makes the other 85% in-house. No defects or design weaknesses were noted.

The Chip

The lid was removed by applying mechanical stress to the lid and forcing a chisel edge into the seal in a controlled manner until the seal fractured. The chip measured 27.2 X 47.2 X 9.5 mils and used a gold-silicon eutectic die mount. The internal wires are ultrasonically bonded, 1 mil diameter aluminum (manufacturer specifies > 99.9% Al). No bond defects were noted. Microbond-pull testing of 6 of the 14 wires found a range in pull strength from 2.8 grams-force to 5.4 grams-force with 4.15 average. These wires should have a minimum of about 2 grams-force pull strength.

The chip metallization was a single stratum interconnection scheme with a SiO_2 coating over the entire chip. The metallization had the following structure: Al on top (>99.9% pure, claimed by manufacturer), Ti-W below for good adhesion to Si and SiO_2 and as a diffusion barrier to Al, and finally Pt_xSi_y in the contact areas for good stable ohmic contact, and in the Schottky barrier contact diodes.

The top SiO_2 was measured to be about 1.1μ thick, somewhat thinner over the metallization. The Al layer of the metallization was about 2μ thick, and carries almost all of the current. The Ti-W layer was measured in angle section to be about 4000Å thick. The Al layer is vapor deposited, the Ti-W sputter deposited in an undisclosed ratio. The Pt_xSi_y is formed by sputtering on Pt in a very thin layer, a few hundred angstroms, and sintering to form Pt_xSi_y in the contact areas, followed by blanket etching to remove the Pt elsewhere.

The highest current density was found to exist in the output transistors emitter metallization. Here the current is specified at 4mA maximum and the metallization is 10.6μ wide (X 2.0μ thick) resulting in a density of $1.9 \times 10^4 A/cm$. Over an oxide step, the density could reach 3×10^4 or higher. MIL-38510 specifies $2 \times 10^5 A/cm^2$ as a maximum density for Al to avoid an unacceptable level of electromigration failures.

The chip microsection found an N-type epitaxial layer of 3μ thickness on a P-type substrate (grounded).

The Components

The chip was photographed and mapped to identify all the components. Figure G-2 shows the logic layout of the gates as relates to the external pins with Figure G-3 showing the electrical schematic of one gate. Figure G-4 shows the chip with all components marked.

The substrate is P-type. Prior to epitaxial layer growth, low resistivity N-type diffusions, subcollectors, are made in positions corresponding to transistors. These provide high conductivity paths from the vicinity of the base-collector junctions to the collector contact diffusions.

After the epitaxial growth, P-type isolation diffusions partition the epitaxial layer into individual collector regions and other components. This diffusion was measured to be about 3.2μ deep.

Resistors

A separate P-type diffusion is used for some of the resistors, base diffusion for others. The "resistor" diffusion is higher resistivity, about 700Ω/□, than the base diffusion, about 200Ω/□. These are calculated sheet resistances based on counting squares on the chip and using the manufacturer specified resistor values. Resistors R1, R2 and R4 (there are four of each) are diffused into two separate isolated regions of the epitaxial layer (high resistivity). R1 and R2 are 32 squares and 10 squares, respectively which, at 700Ω/□, agrees well with the values in Figure G-3. R4 was measured to be about .25 square and was found to be the high resistivity base diffusion by oxide comparison. R5 was found to be the base diffusion, about 13 squares. R6 is high resistivity diffusion, about 5 squares. R3 is about 7 squares and is also high resistivity diffusion.

Cross-sectioning found a depth of about 1μ for the high resistivity diffusion. The base diffusion was about 1μ and the emitter diffusion about 0.75μ. The manufacturer specified depths were, respectively, 0.8μ, 1μ and 0.6μ.

The Diodes

In contrast to the standard Schottky, 9S00, the low power Schottky NAND gates in this device, 9LS00, utilize a pair of input diodes rather than a multiple emitter input-transistor. These are designated D1 and D2 in Figure G-3.

The clamping diodes, D3 and D4, as in the standard power Schottky, provide protection from negative voltage spikes. For each input, an input diode and a clamping diode to ground are combined in a single structure as illustrated in Figure G-5. The contacted annular P-type base diffusion surrounding the D3 Schottky barrier contact diode results in a p-n junction-Schottky barrier hybrid diode. References 3 and 5 describe the theory and experimental advantages of such a structure. A disadvantage in using such a structure in D1 would be increased propagation delay and accordingly the annular P-type diffusion is omitted here. D5 is created by simply contacting the collector of Q1, without the collector contact enhancement diffusion (c.c.e.d.) required for ohmic contact. See Figure G-6.

Transistors

Q1, the phase splitting transistor, is shown in Figure G-6. The isolated epitaxial region comprising the collector is square, 59μ X 59μ with a contact hole 9.3μ X 14.0μ. The epitaxial oxide has a contact hole 6.2μ X 13μ to create the Schottky barrier diode D5. The base regions of transistors with base to collector Schottky diodes are annular, i.e., a rectangular hole in a rectangular shaped diffusion. The hole allows the epitaxial region to "surface" within the base region. The contact hole in the base oxide exposes both part of the base region and all of this "surfacing" epitaxial area of the collector. When the metallization is deposited within the hole, it creates the ohmic contact to the base region and also creates the Schottky diode from base to collector. This occurs because of the relative doping of the base region (high doping → ohmic contact) versus the epitaxial region (low doping → rectifying Schottky contact). Hosack[1] reports a barrier height of 0.82eV for Pt_xSi_y on n-type silicon. Also M. Kamoshida and T. Okada[2] report that the contact resistance of Pt_xSi_y on highly doped Si is essentially the same as that found for Al on Si.

For Q1, the overall base area is $560\mu^2$. The base contact extends out into the epitaxial region to create the collector-base Schottky diode. The contact hole is 19μ X 11μ. The emitter is diffused into the base region away from the Schottky diode and is 13μ X 15μ with a contact hole of 10μ X 10μ.

Q2 is similar to Q1 in construction. It is the output transistor and has two collector contacts, one at either end of the transistor (Figure G-7):

collector	110μ X 84μ
1st c.c.e.d.	62μ X 23μ
contact hole	56μ X 16μ
base (overall)	2400μ^2
Schottky diode	720μ^2
emitter	55μ X 13μ
contact hole	49μ X 5μ

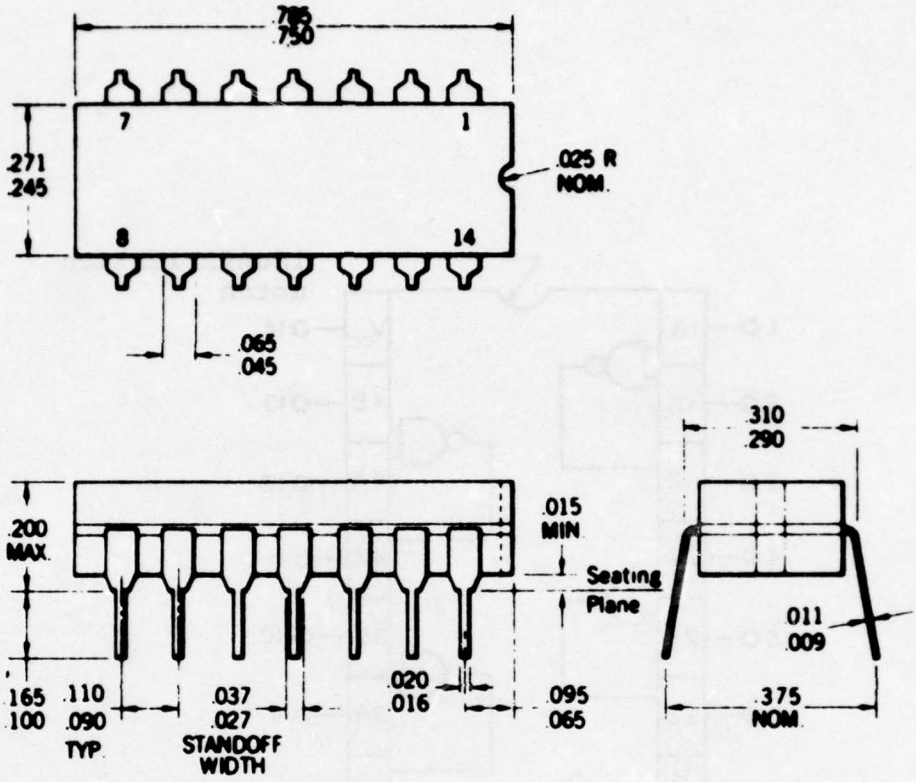
Q3 and Q4 are combined within one isolated epitaxial region forming a Darlington pair with a common collector. The collector has an area of 9000μ^2. It has a single c.c.e.d. (68μ X 12μ) and a single collector contact hole (59μ X 8μ). The base of Q3 is 20μ X 23μ. A contact hole in the thermal oxide opens part of this base region and extends out to contact the collector region as well, thus forming the collector-base Schottky barrier diode. This contact hole is 19μ X 5.7μ, about 60% of which is over the collector, 40% over the base. The Q3 emitter diffused into this base region is 11μ X 16μ.

Q4 is a transistor with no collector base Schottky diode and thus has a normal rectangular diffusion of 26μ X 51μ. The base contact hole is 4.7μ X 42μ. The Q4 emitter diffused into this base region is 11μ X 45μ with a contact hole 4.5μ X 38μ.

CONCLUSIONS

No design weaknesses were found nor any workmanship defects observed.

In accordance with
JEDEC (TO-116) outline
14-Lead SSI Dual In-line



NOTES
- All dimensions in inches
- Leads are intended for insertion in hole rows on .300" centers
- They are purposely shipped with "positive" misalignment to facilitate insertion
- Board-drilling dimensions should equal your practice for .020 inch diameter lead
- Leads are tin-plated kovar
- Package weight is 2.0 grams

FIGURE G-1: Package Outlines

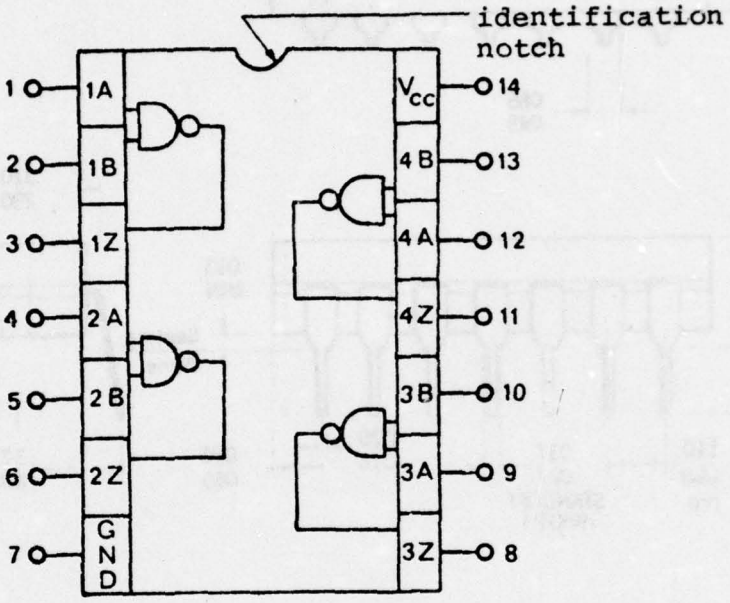


FIGURE G-2: Pin diagram of device showing logic layout.

Not to scale.

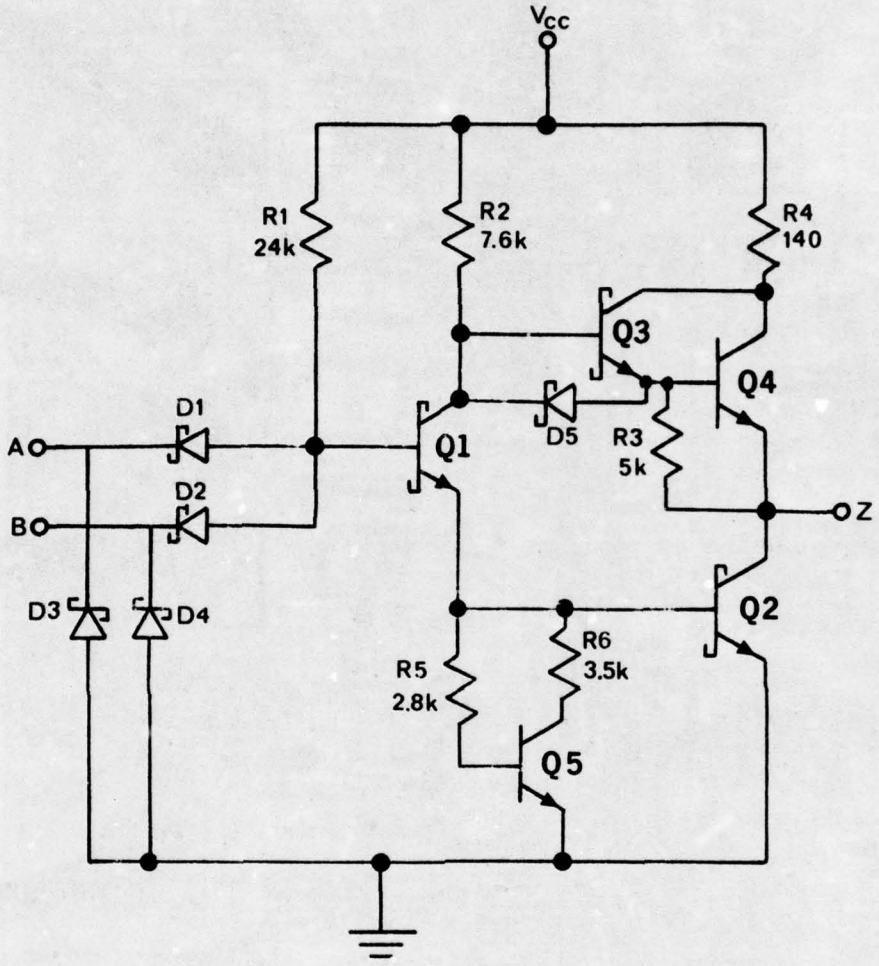


FIGURE G-3: Electrical schematic of one of four gates. Resistor values, provided by the manufacturer, are in Ω.

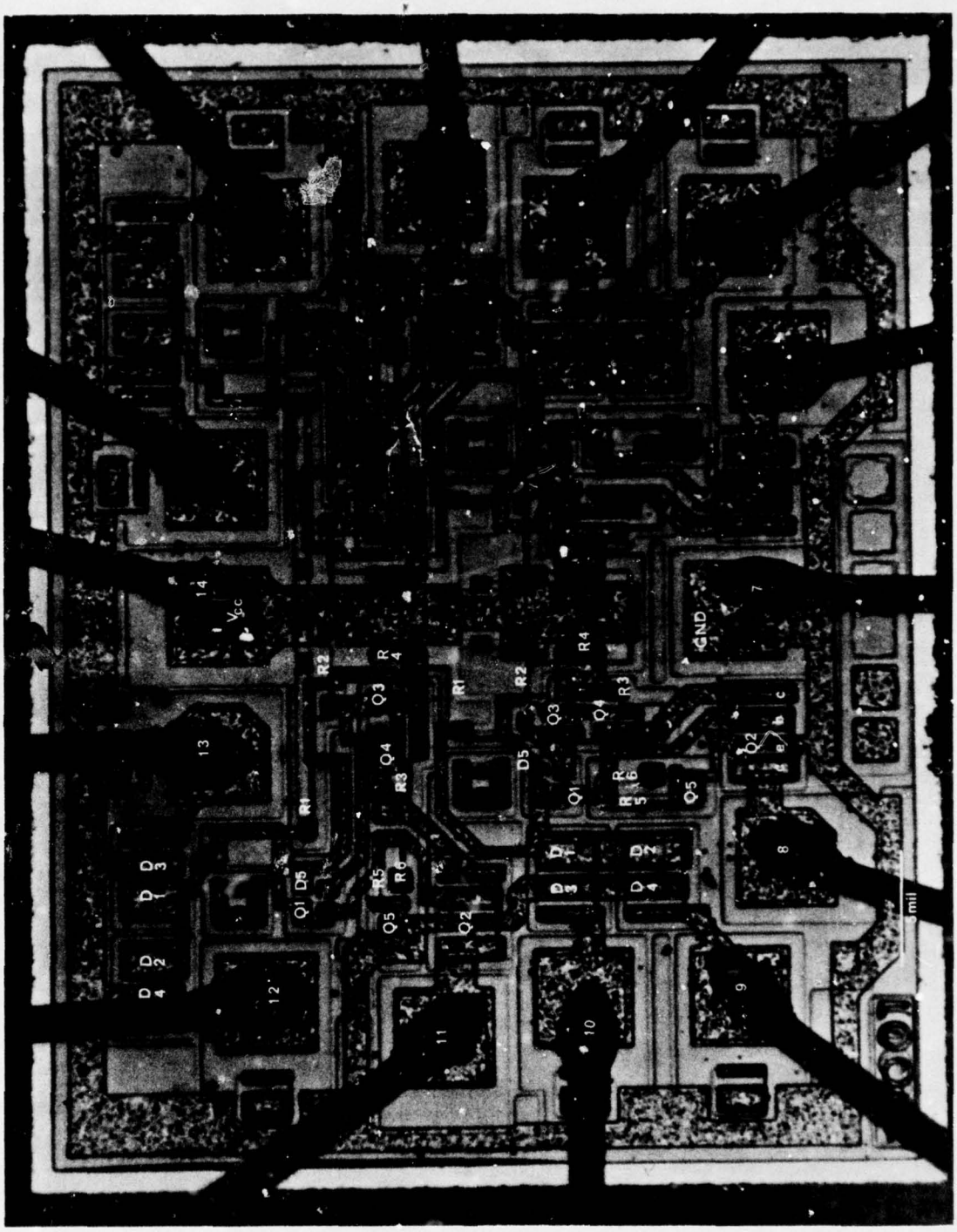


FIGURE G-4: Overall Photograph of Chip with Map Overlay

200 μm

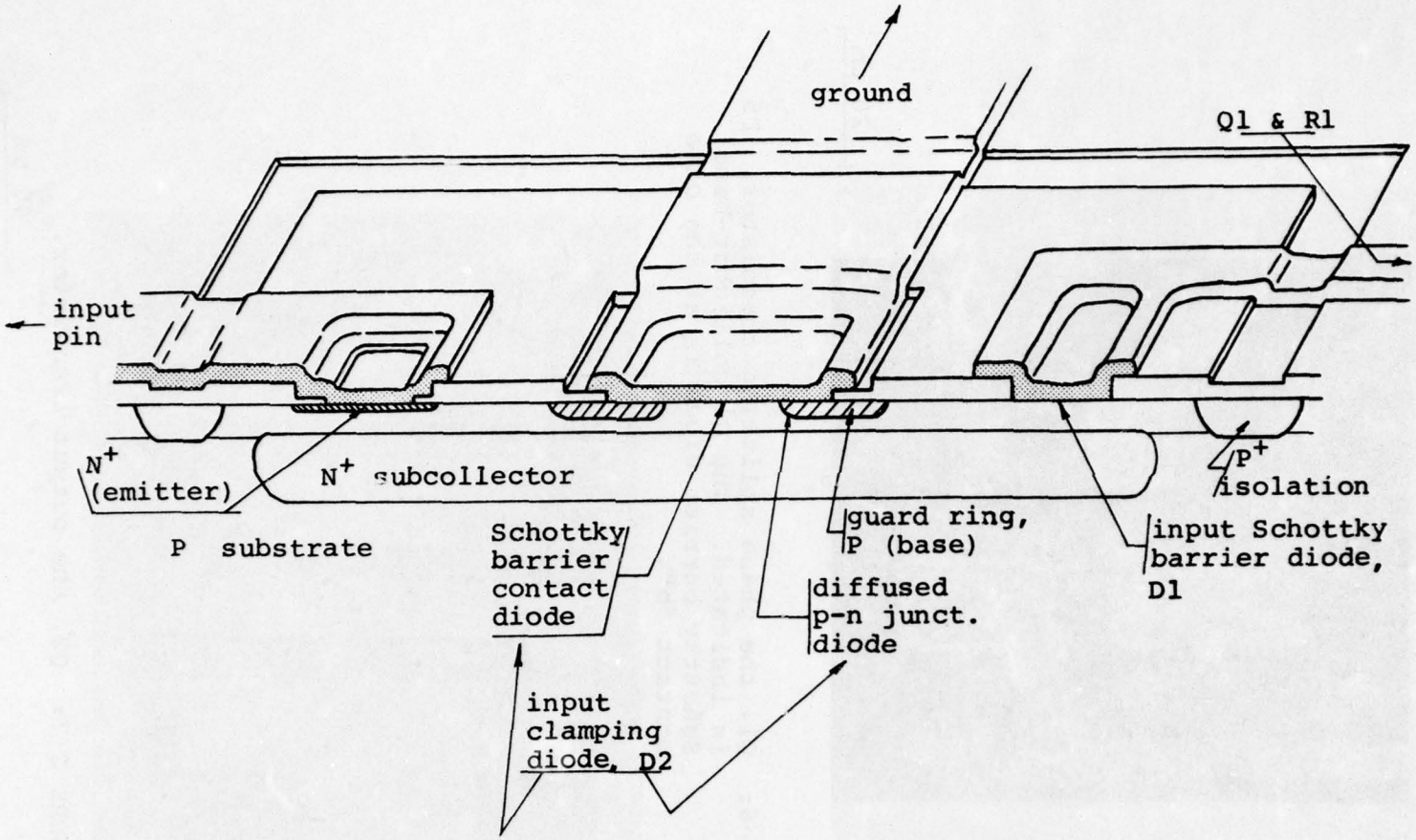


FIGURE G-5: Each of the eight inputs has an input diode (D1) and an input clamping diode (D3) utilizing the above structure. D1 is a pure Schottky barrier diode while D3 is a p-n junction-Schottky barrier hybrid diode.

Not to scale.

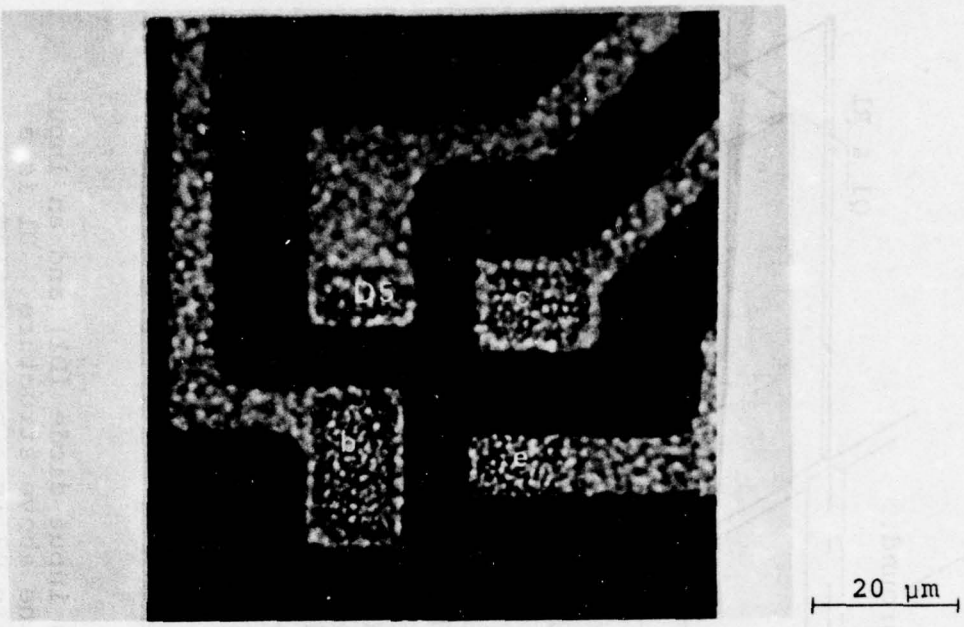


FIGURE G-6: Q1, the phase splitting transistor. D5 is indicated. The Q1 collector-base Schottky barrier diode is at the base contact "b".

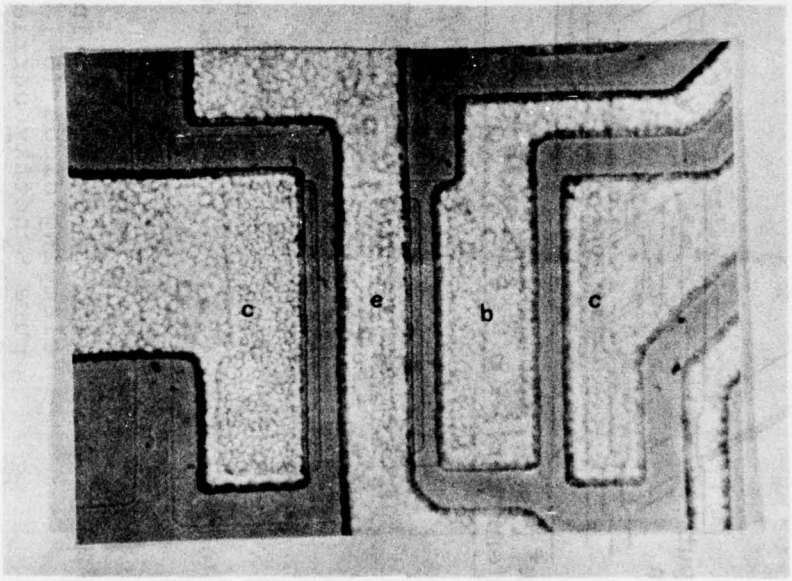


FIGURE G-7: Q2, the output transistor.

APPENDIX H

APPENDIX H

CONSTRUCTION ANALYSIS OF VENDOR A 54LS138

LOW POWER SCHOTTKY TTL INTEGRATED CIRCUIT IN CERAMIC DIP

ABSTRACT

A Vendor A 1-of-8 decoder demultiplexer, low power TTL Schottky IC, part number 54LS138 was the subject of a detailed construction analysis. The device is in a standard 16-pin ceramic dual-in-line package (CERDIP). Two units were received date coded 7351. The internal wires are aluminum while the single level chip metallization is Pt_xSi_y(ohmic contacts and Schottky barrier diodes)/Ti-W/Al (99.9% pure). The chip is entirely coated with vapor deposited SiO_2 for handling purposes only. No design weaknesses or workmanship defects were noted. The chip was mapped.

INTRODUCTION

This analysis was performed as part of an evaluation of this device for Rome Air Development Center. The analysis was designed to document the materials and construction details used in these units and to identify shortcomings in the design or defects in workmanship, if any.

The 138 circuit is shown in Figure H-1. It can be broken down into three simpler circuits:

A. Input

The three input circuits designated A, B and C, each logically consist of two inverters in series. The first inverts the input, the second reinverts, reproducing the input.

B. Enable

This is an AND gate with one non-inverting input (designated C_{SO} and two inverting inputs (C_{S1}, C_{S2}).

C. Output

Each of eight output circuits (designated S through Z) is a NAND gate with four inputs. In each output gate, one input is the output of the enable circuit. The remaining three inputs of each output gate are A or $\overline{A}$, B or $\overline{B}$ and C or $\overline{C}$. Of the eight possible combinations, one inputs each of the output gates.

Thus the logic is as follows: Unless C_{S0} is 1 and C_{S1} and C_{S2} are both 0, all outputs are 1, regardless of the inputs A, B and C. If C_{S0} is 1, C_{S1} and C_{S2} are both 0, then seven of the outputs are 1 and one of the outputs is 0. The following table shows which output will be 0:

Table H-1: Logic of 54LS138

A	B	C	Output in 0 State (all others in 1 state)
0	0	0	Z
1	0	0	Y
0	1	0	X
1	1	0	W
0	0	1	V
1	0	1	U
0	1	1	T
1	1	1	S

Figure H-2 shows a logic schematic.

RESULTS

The Package

Both packages were identical. Figure H-3 shows package outline and dimensions. The hermetic seal (tested in another part of the overall evaluation) was fritted glass. The kovar pins, tin plated outside the package and aluminum clad inside, are embedded in the seal. The lids of the two units were marked as follows:

top:	7351A 54LS138
bottom:	S138 T51

The packages are purchased by Vendor A from Kyoto Ceramics Company, are 16-lead SSI ceramic dual-in-line (CERDIP).

The Chip

The packages were opened by mechanically stressing the lid while forcing a chisel edge into the seal in a controlled manner until the seal fractured. The chip dimensions were 61.1 X 72.8 X 9.5 mils. A gold-silicon eutectic die mount was used.

The internal wires were ultrasonically bonded, 1 mil diameter Al (manufacturer specifies > 99.9% Al). No bond defects were noted. Microbond pull testing of 5 of the 16 wires found pull strengths ranging from 2.3 grams-force to 3.5 grams-force with 2.82 average. Two bonds fractured in the wires themselves, away from either bond, three fractured at the heel of the chip bond.

The chip metallization was a single stratum interconnection scheme with a SiO_2 coating over the entire chip, primarily designed, not as passivation, but as scratch protection during chip handling. The metallization had the following structure: Al on top (>99.9% pure, claimed by manufacturer), Ti-W below for good adhesion to SiO_2 and as a diffusion barrier to Al, and finally Pt_xSi_y in the contact areas for good stable ohmic and Schottky contact.

One unit was cross-sectioned. The top glass was measured to be about 1.2μ thick, somewhat thinner over the metallization. The Al layer of the metallization was about 1.6μ thick, and carries almost all of the current. The Al layer is vapor deposited, the Ti-W sputter deposited in an undisclosed ratio. The Pt_xSi_y is formed by sputtering on Pt in a very thin layer, a few hundred angstroms, and sintering to form Pt_xSi_y in the contact areas, followed by blanket etching to remove the Pt elsewhere.

The highest current density was found to exist in the output transistors' collector metallization. Here the current is specified at 4mA maximum and the metallization is 11.4μ wide (X 1.6μ thick) resulting in a density of $2.2 \times 10^4 A/cm^2$. Over an oxide step, the density could reach 2.8×10^4 or higher.

MIL-38510 specifies 2 X $10^5 A/cm^2$ as a maximum density for Al to avoid an unacceptable level of electromigration failures.

The #1 chip microsection revealed an N-type epitaxial layer of 3.2μ thickness on a P-type substrate (grounded). The manufacturer specified epitaxial thickness is 3μ.

The Components

The chip was photographed and mapped to identify all the components. Figure H-4 shows the chip with all components marked.

The substrate is P-type. Prior to epitaxial layer growth, low resistivity N-type diffusions, subcollectors, are made in positions corresponding to transistors and other components. These provide high conductivity paths from the vicinity of the base-collector junctions to the collector contact diffusions.

After the epitaxial growth, P-type isolation diffusions partition the epitaxial layer into individual collector regions and other components. This diffusion was measured to be about 3.2μ deep.

The Resistors

The P-type base diffusion was used for all of the resistors. The base diffusion has a sheet resistivity of about 160Ω/□. This was obtained by counting squares and comparing to schematic resistor values shown in Figure H-1. Cross-sectioning found a depth of about 1.5μ for the base diffusion and the emitter diffusion about 0.9μ. The manufacturer specified depths were, respectively, 1.5μ and 1μ.

The Diodes

In contrast to the standard Schottky, 54S138, the low power Schottky NAND gates in this device, 54LS138, utilize a pair of input diodes rather than multiple emitter input transistors. These are designated D2A, D2B, D2C, D3A, D3B, D3C, D1E, D2E, D3E, D7E and all other diodes assigned a triple letter designation (see Figure H-4). Clamping diodes, D1A, D1B, D1C, D4E, D5E, D6E, as in the standard power Schottky, provide protection from negative voltage spikes originating outside the device. For each input, pins 1-6, an input diode and a clamping diode to ground are combined in a single structure as illustrated in Figure H-5. The contacted annular P-type base diffusion surrounding the Schottky barrier contact

clamping diodes, D1A etc., results in p-n junction-Schottky barrier hybrid diodes. References 3 and 5 describe the theory and advantages of such a structure. A disadvantage in using such a structure in the input diodes, D2A etc., would be increased propagation delay and accordingly the annular P-type diffusion is omitted here.

Transistors

Q1A, the phase splitting transistor, is shown in Figure H-6. The isolated epitaxial region comprising the collector is rectangular, 69.1μ X 41.2μ with a collector contact enhancement diffusion (c.c.e.d.) 9.7μ X 22.6μ and a contact hole 17.4μ X 4.6μ. The base contact holes of all those transistors with base to collector Schottky diodes open onto the collector region as well as the base region. When the metallization is deposited within the hole, it creates the ohmic contact to the base region and also creates the Schottky diode from base to collector. This occurs because of the relative doping of the base region (high doping ohmic contact) versus the epitaxial region (low doping rectifying Schottky contact). Hosack[1] reports a barrier height of 0.82eV for Pt_xSi_y on n-type silicon. Also, M. Kamoshida and T. Okada[2] report that the contact resistance of Pt_xSi_y on highly doped Si is essentially the same as that found for Al on Si.

For Q1, the overall base dimensions are 29μ X 23.2μ. The Schottky diode area is 16.7μ X 2.9μ. The contact hole is 16.7μ X 5.8μ. The emitter is diffused into the base region away from the Schottky diode and is 12.6μ X 9.8μ with a contact hole of 6.4μ X 4.5μ.

The following are similar dimensions of other selected transistors.

Q4A:

Collector	250μ X 58μ
c.c.e.d.	39.8μ X 9.7μ
Contact hole	35μ X 5μ
Base	$985\mu^2$
Schottky diode area	7.7μ X 5.8μ
Contact hole	33μ X 4.9μ
Emitter	30.5μ X 9.7μ
Contact hole	25.2μ X 4.9μ

Q10E:

Collector	253μ X 59μ
c.c.e.d.	39.8μ X 9.7μ
Contact hole	35μ X 5μ
Base	$990\mu^2$
Schottky diode area	7.7μ X 5.8μ
Contact hole	32.9μ X 5μ
Emitter	30.4μ X 9.7μ
Contact hole	25.2μ X 5μ

Q2S and Q3S (share common collector):

Collector	136μ X 71.8μ
c.c.e.d.	81.4μ X 12μ
Contact hole	69.7μ X 7.7μ
Base Q2S	$520\mu^2$
Schottky diode area	$38.5\mu^2$
Contact hole	8μ X 3.5μ
Base Q3S (not Schottky)	58μ X 31μ
Contact hole	50.4μ X 3.9μ
Emitter Q2S	11μ X 9.7μ
Contact hole	4μ X 7μ
Emitter Q3S	50.4μ X 8.1μ
Contact hole	45μ X 4.4μ

Q4S:

Collector	134μ X 85μ
First c.c.e.d.	67μ X 12.6μ
Contact hole	62μ X 7.7μ
Second c.c.e.d.	46.5μ X 65.8μ
Contact hole	7.7μ X 61μ
Base	44.5μ X 65.8μ
Schottky diode area	$\sim 374\mu^2$
Contact hole	15.5μ X 44.5μ
Emitter	55.2μ X 9.7μ
Contact hole	49.4μ X 3.9μ

CONCLUSIONS

No design weaknesses were found nor any workmanship defects observed. However, it was noted that the deposited glass exhibited moderate to severe cracking.

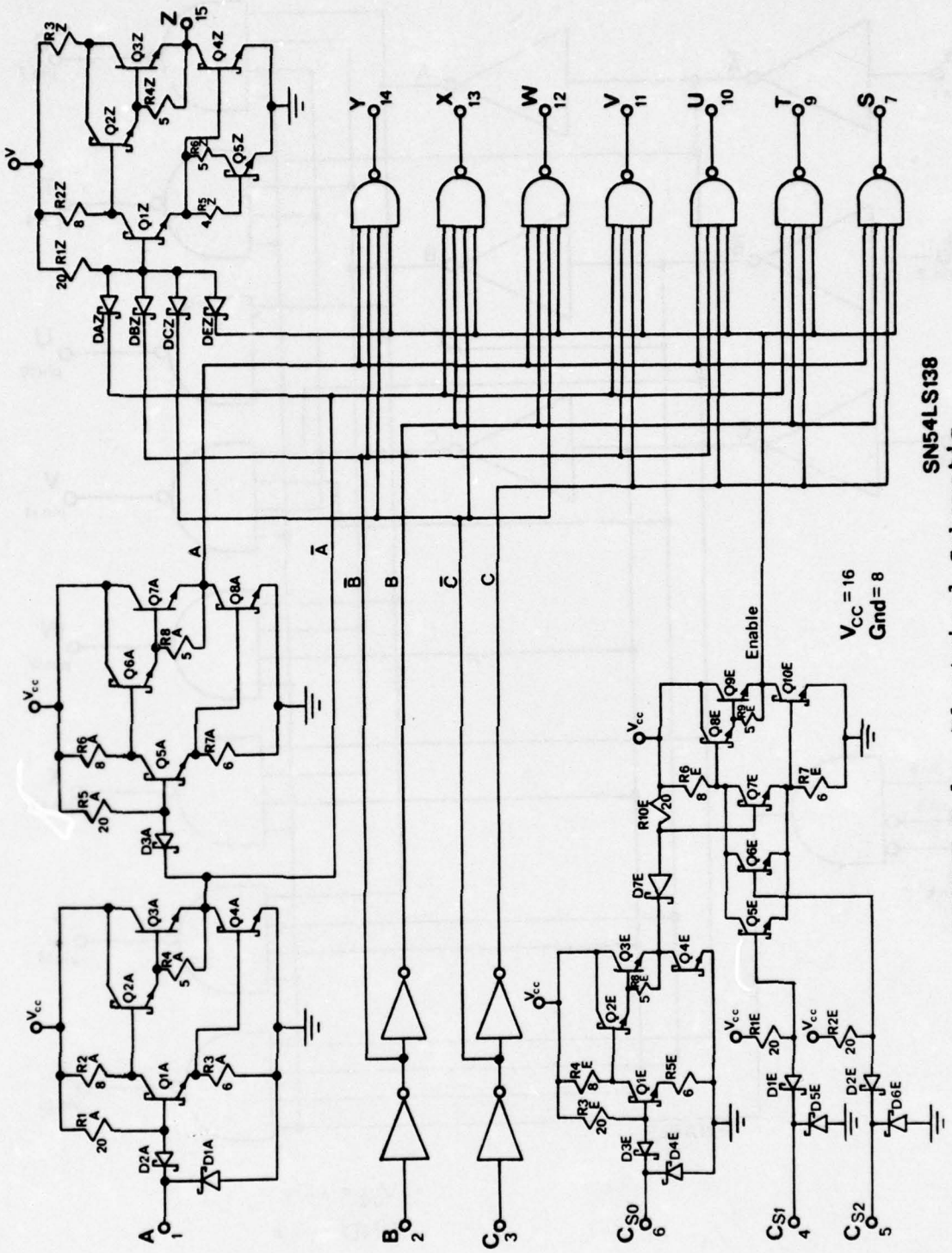


FIGURE H-1: Electrical Schematic

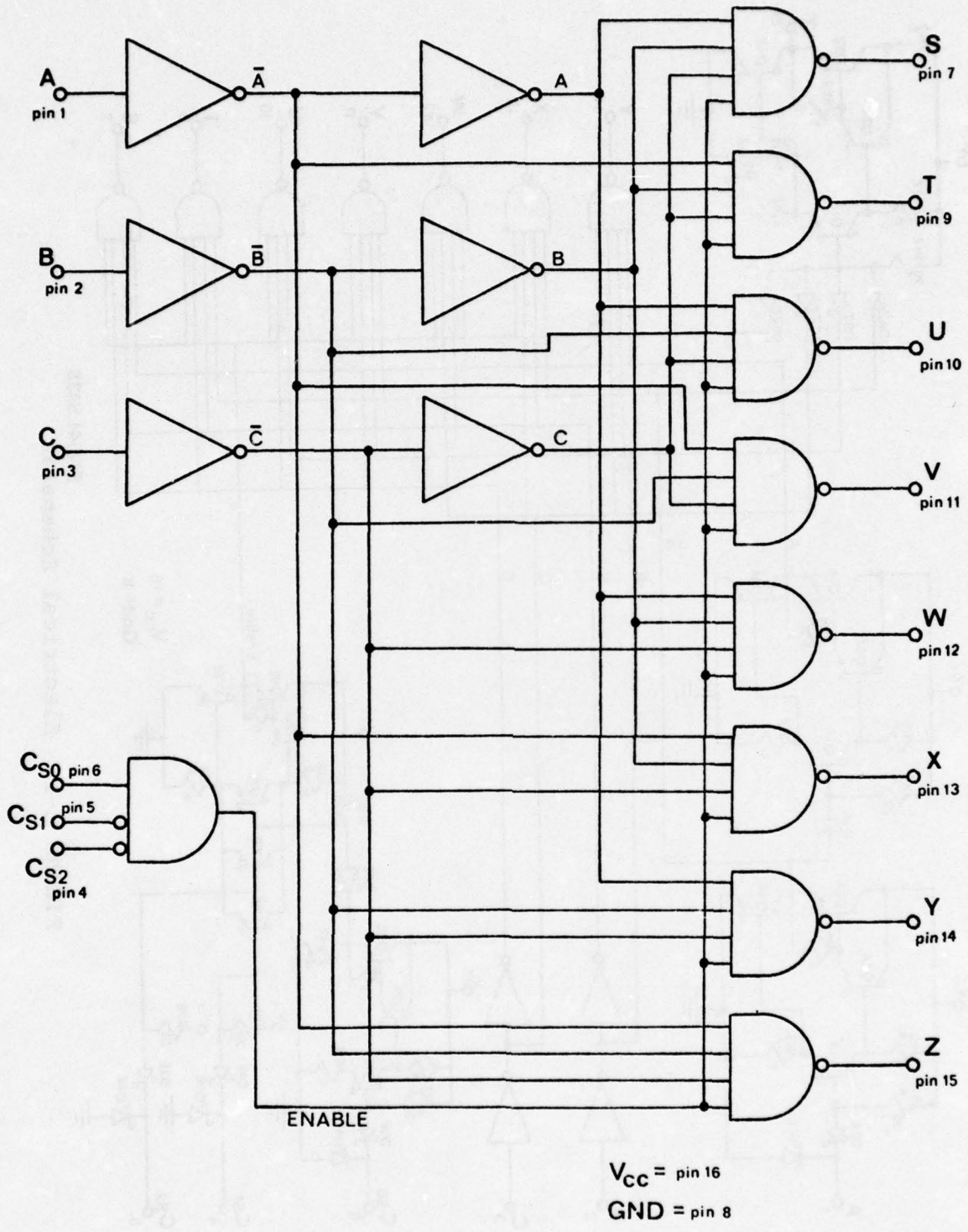
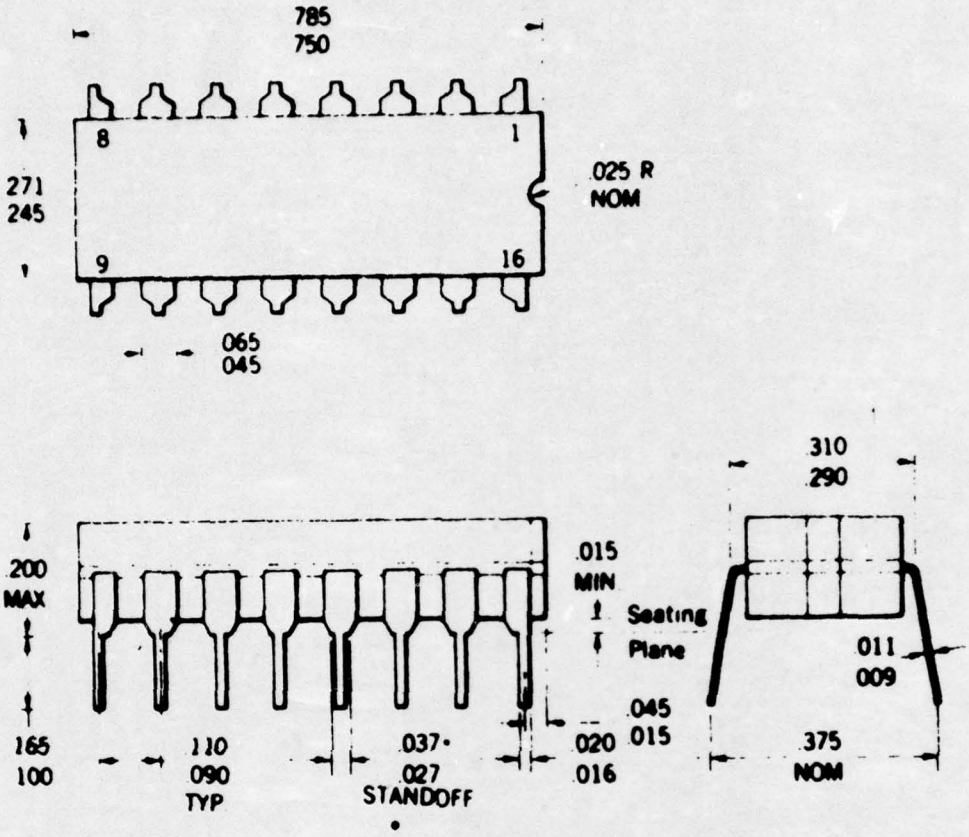


FIGURE H-2: Logic diagram of 54LS138

16-Lead SSI Dual In-line



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
*The .037/.027 dimension does not apply to the corner leads

FIGURE H-3: Package Outlines

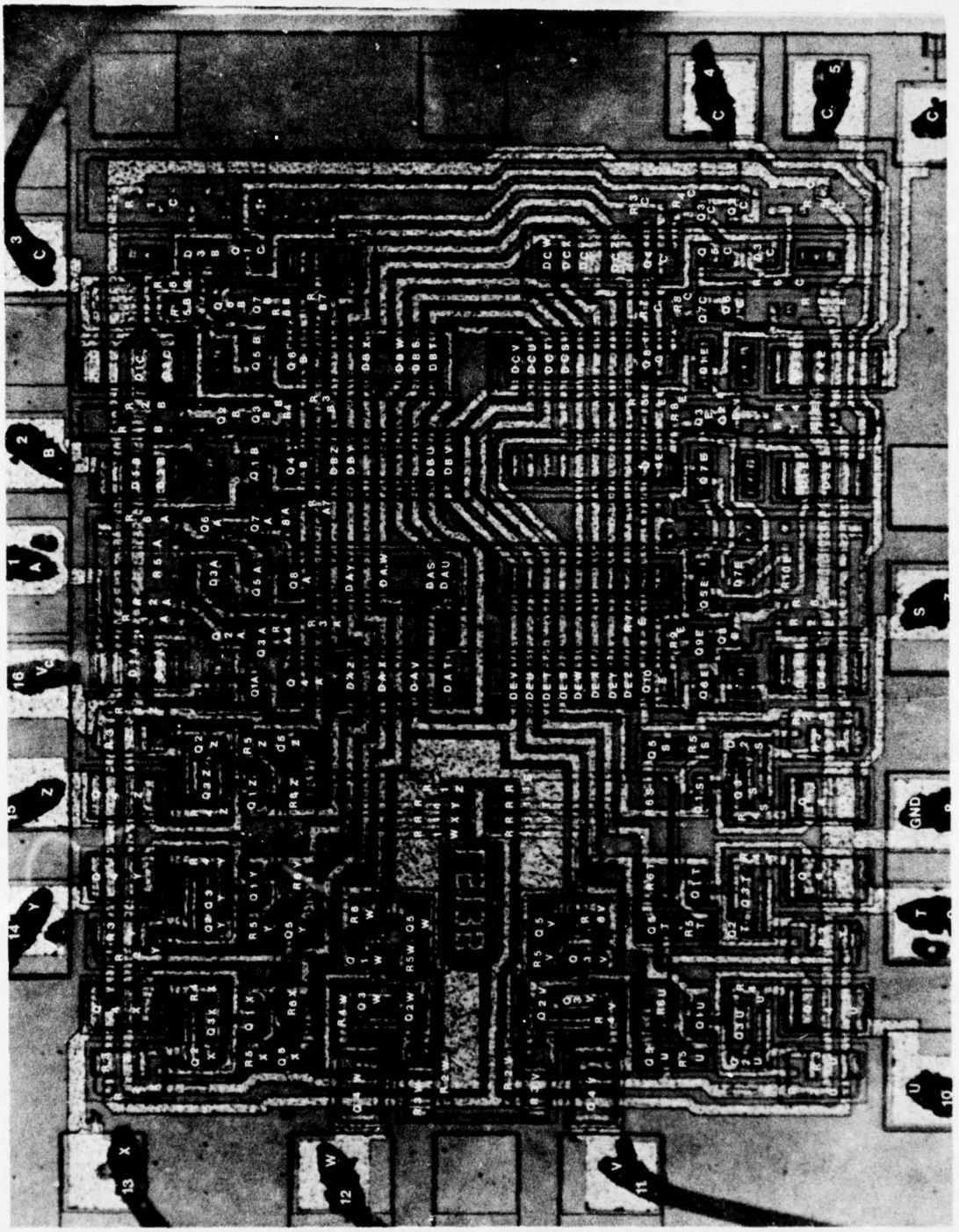


FIGURE H-4: Overall Photograph of Chip with Map Overlay

200 μm

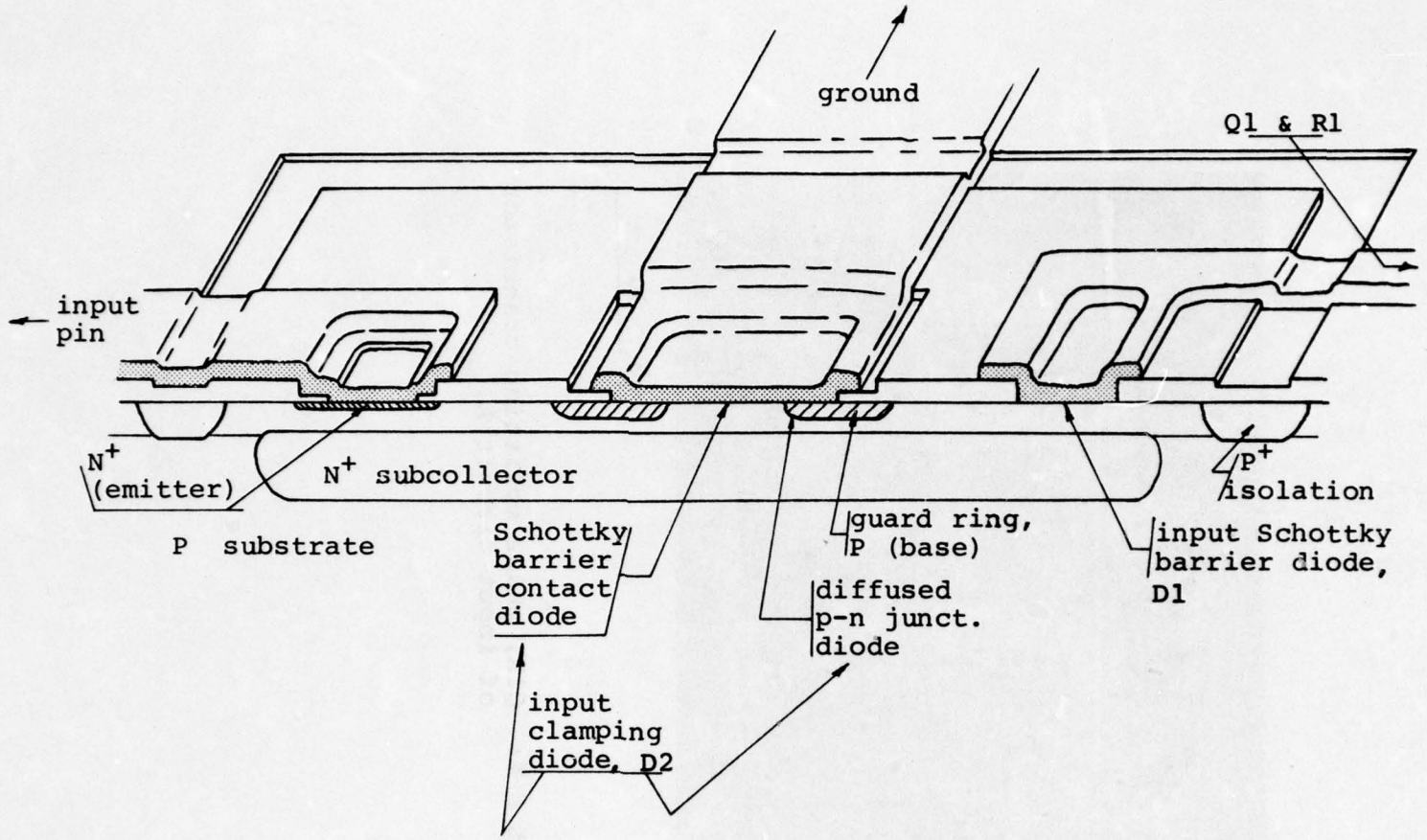


FIGURE H-5: Each of the eight inputs has an input diode (D2) and an input clamping diode (D1) utilizing the above structure. D2 is a pure Schottky barrier diode while D1 is a p-n junction-Schottky barrier hybrid diode.

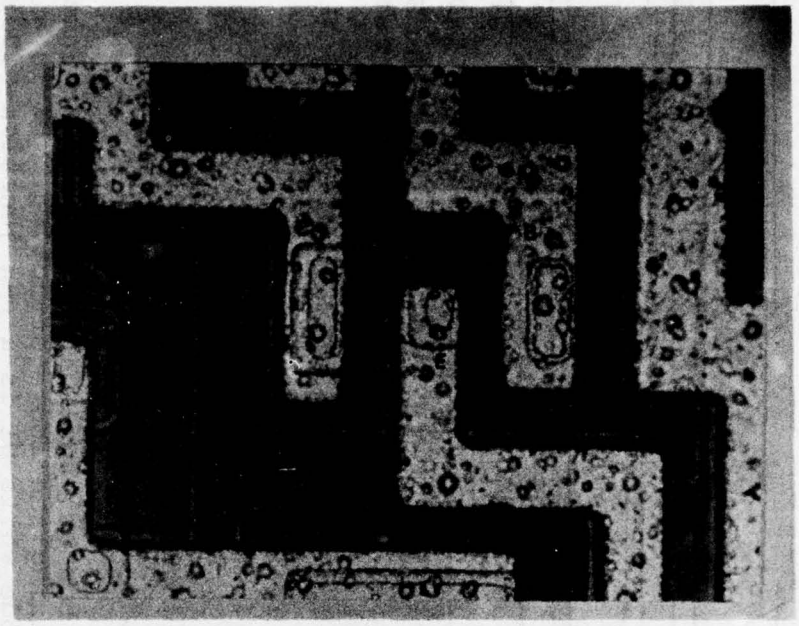


FIGURE H-6: Q1A, phase splitting transistor of input circuit A.

APPENDIX I

APPENDIX I

CHEMICAL ETCHING AND GOLD PLATING OF TIN PLATED CERDIP LEADS

1. OBJECTIVE

This procedure defines the masking, chemical etching and electroplating operations used to remove the tin plating on CERDIP leads and replace it with gold plating in order to permit high temperature exposure.

2. MATERIALS AND EQUIPMENT

2.1 Orange Stop-Off Lacquer (Reynolds and Markman, Inc.)

2.2 Tin Stripping Solution (1 Gal. conc. HCl acid, 2 oz. Sb_2O_3; 1/2 pint H_2O)

2.3 Nitric Acid Solution (1:1), Smut Remover

2.4 Alconox Solution (Acid neutralizer), 10 $\pm$ 1% by wt.

2.5 Distilled or deionized water.

2.6 Blue M oven, air circulating.

2.7 Scotch Tape, copper with adhesive backing (No. 1181) 5/8" wide

2.8 Plexiglass Rack supports with electrical connections 9 1/4" L by 2" W.

2.9 Nickel Sulfamate Plating (Ready-to-use) solution, 11 oz/gal., SEL-REX Corp.

2.10 C-1 Autronex Gold Plating Solution, 1 ox/gal, SEL-REX Corp.

2.11 Air Hose Jet Dryer

2.12 Methanol, Reagent Grade, Fisher Scientific

2.13 Acetone, Reagent Grade, Fisher Scientific

2.14 Q-tip Applicators, Fisher Scientific

2.15 Aluminum Weighing Pans, Fisher Scientific

2.16 Tinned Copper Wire #20 (0.030" diameter)

2.17 Tinned Copper Wire #30 (0.010" diameter)

2.18 Bristle brush, Fisher Scientific

2.19 Glass (Pyrex) trays, 12" L x 9" W x 2 1/2" D

3. MASKING OPERATION

3.1 Pour diluted (1:10 w/methanol) Orange Stop-Off Lacquer into an aluminum pan to a height one-half full.

3.2 Immerse the cerdip package in an inverted position to a depth to completely cover the glass frit seal of the package.

3.2.1 Remove package and position masked device on the surface of work bench in an inverted position (leads up).

3.2.2 Air dry masked devices for a minimum of 30 minutes.

3.3 Repeat immersion per above procedure.

3.3.1 Do not coat the lead areas where stripping and plating is desired. Any inadvertent coating on leads may be removed by rubbing with a Q-tip wet with acetone.

3.4 Visually inspect all masked areas.

3.4.1 Touch up frit areas that indicate voids, or any faulty masking.

4. TIN ETCHING OPERATION

4.1 Position the parts in an upright (leads down) position in a glass tray. It is suggested a minimum lot size of 30 be used.

4.2 Make up Tin Stripping solution in the concentration described in 2.2

4.2.1 Pour tin stripping solution into the tray to a height below the masking level of the leads.

4.2.2 Etch to remove the majority of the tin deposit. Total immersion time is 4 ± 1 minute. (30 piece lot)

4.3 Remove all devices from the etching tray and rinse in running (warm) tap water for 1 minute minimum.

4.3.1 Place all parts into a beaker filled with distilled water until total quantity of lot is etched.

5. SMUT REMOVAL FROM LEADS

5.1 Place parts in an upright (lead down) position in a glass tray. It is recommended that 15 devices per lot be used for this operation.

5.2 Pour nitric acid solution (1:1) into the tray to a height below the masking level of the leads.

5.2.1 Immersion time of 2.0 ± 0.5 minute is adequate to remove any oxide from the surface.

5.3 Rinse devices in running (warm) tap water for approximately one minute.

5.4 Immerse devices in ten percent aqueous solution of Alconox detergent for approximately five minutes to neutralize any residual acid.

5.5 Rinse devices in running (warm) tap water for approximately one minute.

5.6 Rinse devices with distilled water and oven dry in a Blue M air circulating oven for 60 ± 5 minutes at 75°C ± 2°C.

6. WIRE WRAPPING AND FIXTURING OF DEVICES

6.1 On a bench top, lay out strips of 5/8" wide conductive adhesive tap (adhesive side up) in rows of 12.

6.1.1 Invert and position the devices along the lengthwise centerline of the tape forming a series of devices positioned end-to-end.

6.1.2 Lift the remaining edges of the tape and press and rub with an orange stick to adhere tape against the leads and to make intimate contact with each lead.

6.1.3 Using #30 wire, wire wrap the device into three rows containing 12 per row on the plexiglass surface as shown in Figure I-1. Equally space four wire wraps per each row to support the devices.

6.1.4 Interconnect (wire) ends of rows 1, 2, and 3 with #30 wire to form electrical continuity with each other; attach ends of wire to the corner screws as shown in Figure I-1.

6.1.4.1 Wire the opposite ends of the same rows and again attach the opposite corner screws per Figure I-1.

6.2 Connect at each 2" width-end of the rack an 8-inch strand of #20 wire joining the ends to the corner screws of the fixture.

6.3 Dessicate the assembly if plating cannot be conducted within four hours. This is necessary to prevent any contamination that may form on cleaned leads.

7. NICKEL ELECTROPLATING

7.1 Nickel electroplate the leads of devices in a nickel sulfamate bath per the following conditions:

pH	3.5 ± 0.2
Temperature	150°F ± 5°F
Voltage	1.5V ± 0.1V
Amps	800 milliamps (20 amps/sq.ft.)

7.2 In order to achieve a nickel plating thickness of 70 µinch minimum, plating time must be 10 minutes minimum.

NOTE: Immerse only the leads in the plating solution.

7.3 Rinse the rack assembly in running (warm) tap water for one minute minimum.

7.4 Rinse the assembly in distilled water and immediately gold plate.

8. GOLD ELECTROPLATING

8.1 Gold electroplate the leads of devices in an Autronex C-I acid gold bath per the following conditions:

pH	4.0 + 0.2
Temperature	120°F-140°F
Voltage	2.8V + 0.1V
Amps	500 milliamps (12 amps/sq.ft.)

8.2 In order to achieve a gold plating thickness of 200 µinches, plating time must be 25 minutes minimum.

NOTE: Immerse only the leads in the plating solution.

8.3 Rinse the rack assembly containing the devices with running (warm) tap water for one minute minimum.

8.4 Rinse the rack in distilled water and air blast dry.

8.5 Remove the devices from the racks and remove the electrical tape.

8.6 Strip the masking compound and any adhesive residuals by soaking the devices in acetone and brushing with a bristle brush until all traces of masking compound and adhesive residue are removed. Rinse with clean acetone and dry.

9. DETERMINATION OF PLATING CURRENT (amps/sq.ft.)

9.1 Calculations applicable to this procedure, reference Figure I-2: The total surface area of one lead to be plated equals 0.0104 sq. in., derived by the lead dimensions being 0.17" long by 0.01" thick by 0.0184" wide. Note that this is based on only the total surface area to be plated on the lead.

(a) 0.0104 sq. in. per lead multiplied by 16 leads per device equals 0.1664 sq. in.

(b) 0.1664 sq. in. per device multiplied by 36 devices per rack equals 5.9904 sq. in., or 6.0 sq. in.

9.2 Calculations

$$\frac{6.0 \text{ sq. in.}}{144 \text{ sq. in/sq.ft.}} \times \text{Current Density (amps/sq.ft.)} = \text{Amperage/rack}$$

of the plating solution

Example: SEL-REX C-1 Gold Plating Solution

$$\frac{6.0 \text{ sq. in.}}{144 \text{ sq. in/sq.ft}} \times 12 \text{ amps/sq. ft.} = 0.500 \text{ amps}$$

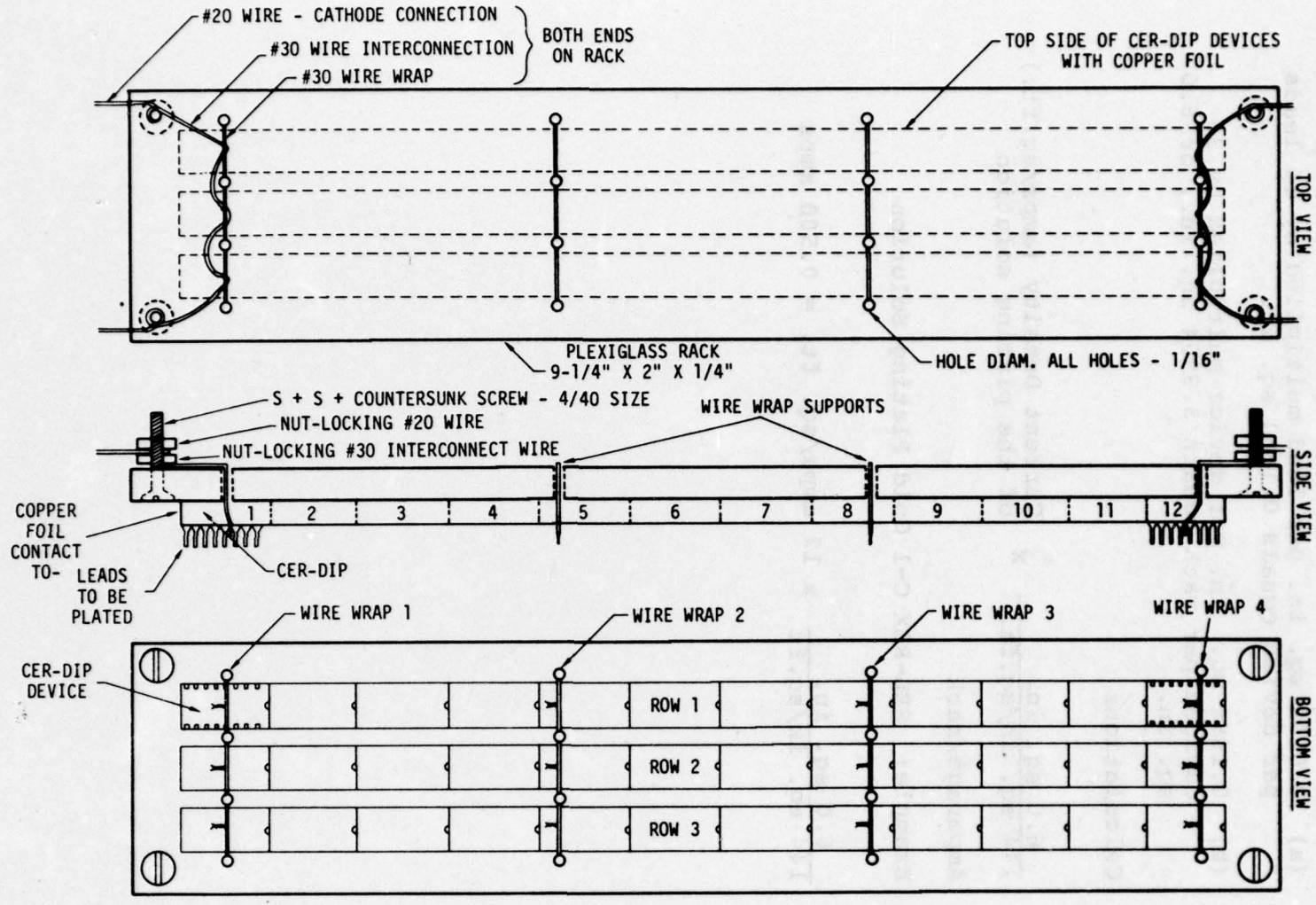


FIGURE I-1: Wire Wrapping and Fixturing Diagram

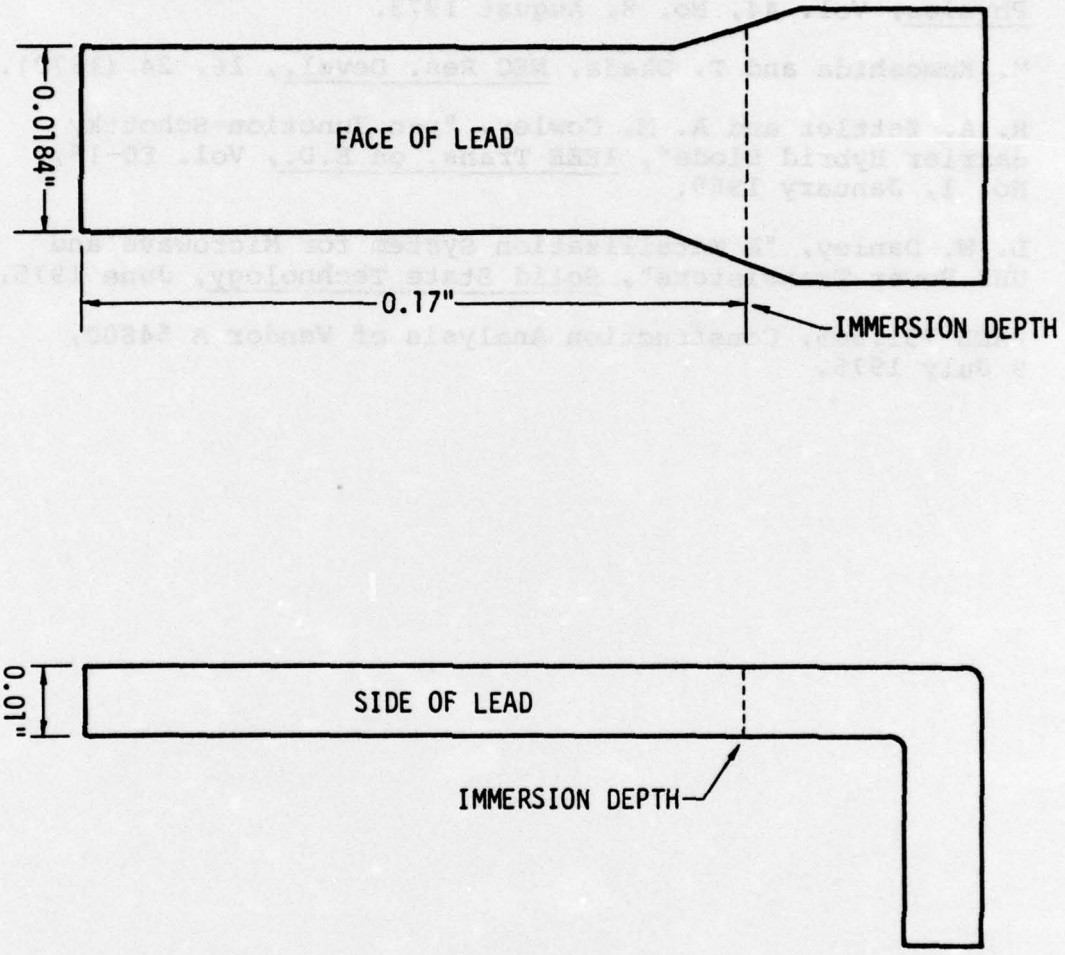


FIGURE I-2: Lead Configuration and Dimensions

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