AD-A032 822 SILICON TRANSISTOR CORP CHELMSFORD MASS F/G 9/1
PRODUCTION ENGINEERING MEASURE (PEM) FOR HIGH CURRENT, FAST-SWI--ETC(U)
JUN 75 F G ERNICK DAAB05-73-C-2032

UNCLASSIFIED NL

| OF |
AD
A032822

END

DATE
FILMED
1-77

NINTH QUARTERLY PROGRESS REPORT

19 January 1975 to 19 April 1975

PRODUCTION ENGINEERING MEASURE FOR HIGH CURRENT, FAST-SWITCHING TRANSISTORS

DAAB05-73-C-2032

Department of the Army
U.S. Army Electronics Command
Fort Monmouth, New Jersey 07703

SILICON TRANSISTOR CORPORATION
Katrina Road
Chelmsford, Massachusetts 01824

(6) Production Engineering Measure
(PEM) FOR HIGH CURRENT, FAST-SWITCHING
TRANSISTORS.

(11) 13 Jun 75

by

(10) Frederick G. Ernick

(12) 31p.

(9) NINTH QUARTERLY PROGRESS REPORT. no. 9,
19 Jan [redacted] -19 Apr [redacted] 75,

The object of this study is to conduct a production engineering measure (PEM) for a high current, fast-switching NPN transistor.

(15) CONTRACT NO DAAB05-73-C-2032

"The findings of this report are not to be construed as an official Department of the Army position unless so designated by other authorized documents."

Destroy this report when it is no longer needed. Do not return it. Do not return it to the originator.

This project has been accomplished as part of the U.S. Army Manufacturing and Technology Program which has as its objective the timely establishment of manufacturing processes, techniques or equipment to insure the efficient production of current or future defense programs.

PURPOSE

The purpose of this program is to conduct a production engineering measure (PEM) for a high current, fast-switching NPN transistor. The salient electrical characteristics are:

P_T	=	350 watts (T_C = 25°C)
θ_{JC}	=	0.5° C/W
V_{CBO}	=	240 Vdc
V_{CEO}	=	200 Vdc
V_{EBO}	=	10 Vdc
I_C	=	90 Adc
T_{stg}	=	-65° to +200°C

A pilot capability will be established to produce the subject transistors at a rate of 500 per month. This capability will be demonstrated by fabricating one hundred electrically good transistors.

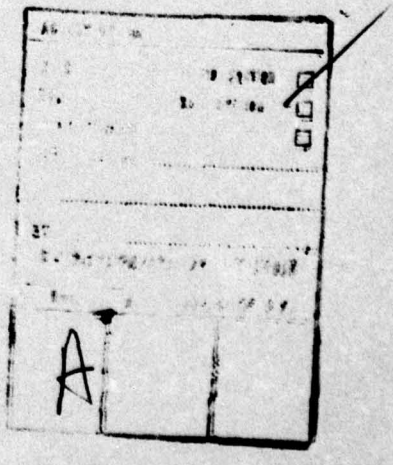

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

ABSTRACT

During this period, the First Article Test Report was approved. A plant survey was conducted to monitor production rates. Permission was obtained to start the pilot run. The pilot run was begun. Electrical and physical parameters of selected runs are shown. 400 chips were selected for encapsulation. A total of 232 devices were accepted at pre-cap visual inspection showing that the program is on schedule.

I. NARRATIVE

A. Background

During the previous period, First Article Testing was completed successfully. The results of the testing were shown in Quarterly Report Number Eight. The stability of the devices on the operating life tests indicate the suitability of the multiple epitaxial process for chip fabrication for this program. Similarly, the results of temperature cycling indicate the suitability of the hard solder construction technique employed for chip mounting. Possible failure mechanisms were discussed.

The First Article Test Report was submitted for approval and rejected because it did not provide all of the information required by SCS-13. The report was corrected and again submitted for approval.

B. Progress During the Present Period

During this period, the First Article Test Report was approved. A survey was conducted by Mr. D. Biser and Mr. R. Holevinski. Permission was obtained to proceed with the pilot run. It was decided that the pilot run would be made again utilizing both the JEDEC TO-36 and TO-115 package. Because of the relatively large quantities involved, it was agreed that the shipped devices could be in a 60/40 ratio by package type rather than the 50/50 ratio previously used. This was done at the request of Silicon Transistor Corporation because of the uncertainties in yields, i.e., it is possible one package would run at a lower yield than the other. The deviation from a 50/50 ratio means that less total pieces need to be started. Plans for the pilot runs were formulated.

Actual device fabrication was started on April 4, 1975. Table One summarizes the five runs that were started and deemed suitable for the pilot run. Each run contained 100 wafers and each wafer contained five potential transistors. From these

2,500 potential chips, 400 were accepted for encapsulation after wafer testing, sawing and breaking. 120 of the TO-36 and 112 of the TO-115 were accepted at pre-cap visual inspection after die bonding and lead bonding. Initial electrical evaluation indicates that the yield at Group A Testing will be more than adequate to insure the required number of devices.

The SCS-450-A form defining the transistor specifications is shown as Figure One.

During this period, the Eighth Quarterly Report was approved for distribution.

C. Progress During the Next Period

During the next period, the pilot phase and lot acceptance testing will be completed.

III. IDENTIFICATION OF PERSONNEL

During this period, P. Fitzgerald, F. Novotny, J. Plaisted and W. Stone devoted a total of eighty (80) hours to this program.

ELECTRICAL AND PHYSICAL PARAMETERS

TABLE ONE

Run #	EPI	Vendor	N-X_j Microns	N-P ohm cm	P X_j Microns	P P ohm cm	Oxide X_j Angstroms	BV_{CEO} Volts	BV_{EBO} Volts
4/4/1	1.2.28	Texas Inst.	44	16	7.5	.75	10,000	210-265	10.5
4/8/1	1.2.28	Texas Inst.	43	15	9.0	.75	15,000	215-265	11.8
4/10/1	1.2.28	Texas Inst.	45	17	8.0	.75	12,000	250-290	11
4/11/1	1.2.28	Texas Inst.	44	18	7.5	.75	10,000	290-300	10
4/14/1	1.2.28	Texas Inst.	48	18	8.0	.75	15,000	290-310	12

SEMICONDUCTOR DEVICE, TRANSISTOR, NPN, SILICON POWER

STA4900 and STA9901

1. SCOPE

1.1 Scope.- This specification covers the detail requirements for silicon, NPN, power transistors for particular use in power-switching, electronic-circuit applications. (See 3.3 and 6.2 herein.)

1.2 Maximum ratings.-

P_T 1/			θ_{J-C}	V_{CBO}	V_{CEO}	V_{EBO}	I_C 2/	$T_{(oper)}$ T_{stg}
at: T_C = +25°C	at: T_C +50°C	at: T_C = +100°C						
W	W	W	°C/W	Vdc	Vdc	Vdc	Adc	°C
350	300	200	0.5	240	200	10	90	3/

1/ Linear derating factor = 2.0 W/°C up to and including T_C = +200°C.

2/ Pulsed (see 4.3.1 herein) = 120A.

3/ Temperature range = -65° to +200°C.

1.3 Particular electrical characteristics.- (At T_C = +25°C:

	h_{FE} 1/								V_{BE} 1/			
	at: I_C= 120 Adc V_{CE}=4 Vdc		at: I_C= 90 Adc V_{CE}=5 Vdc		at: I_C= 40 Adc V_{CE}=2 Vdc		at: I_C= 20 Adc V_{CE}=2 Vdc		at: I_C= 120 Adc V_{CE}=4 Vdc		at: I_C= 90 Adc V_{CE}=5 Vdc	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
	---	---	---	----	---	---	---	---	---	---	---	---
	---	---	---	---	---	---	---	---	---	---	---	---
STA4900	5.0	---	10	40	15	50	30	120	---	3.0	---	1.5
STA9901	5.0	---	10	40	15	50	30	120	---	3.0	---	2.0

1/ Pulsed: see 4.3.1 herein.

	$V_{CE(sat)}$ 1/				t_{on}	t_s	t_f
	at: I_C= 120 Adc I_B= 24 Adc		at: I_C= 90 Adc I_B= 15 Adc		at: I_C= 90 Adc (see Page 7 herein)		
	Min	Max	Min	Max	Max	Max	Max
	Vdc	Vdc	Vdc	Vdc	usec	usec	usec
STA4900	---	2.0	---	0.75	7.0	4.0	1.0
STA9901	---	2.0	---	1.50	7.0	4.0	1.0

1/ Pulsed: see 4.3.1 herein.

2. APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein:

SPECIFICATIONS

MILITARY

MIL-S-19500 Semiconductor Devices, General Specification for.

STANDARDS

MILITARY

MIL-STD-202 Test Methods for Electronic and Electrical Component Parts.
MIL-STD-750 Test Methods for Semiconductor Devices.

DRAWINGS

ELECTRONICS COMMAND

SC-A-46600 Preproduction Sample Approval in Lieu of Qualification Requirement in Specifications for Semiconductor Devices and Electron Tubes.

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer. Both the title and number of symbol should be stipulated when requesting copies.)

2.2 Other publications.- The following document forms a part of the specification to the extent specified herein. Unless otherwise indicated, the issue in effect on date of invitation for bids or request for proposal shall apply.

NATIONAL BUREAU OF STANDARDS

Handbook H28 Screw-Thread Standards for Federal Services.

(Application for copies should be addressed to the Superintendent of Documents, Government Printing Office, Washington, D.C. 20402.)

3. REQUIREMENTS

3.1 Requirements.- Requirements for the transistors shall be in accordance with MIL-S-19500, and as otherwise specified herein.

3.2 Design and construction.- The transistor shall be of the design, construction, and physical dimensions as specified by the JEDEC TO-115 (STA4900) and TO-36 (STA9901) packages.

3.2.1 Terminal arrangement.- Terminal arrangement is determined by the package requirements.

3.2.2 Operating position.- The transistor shall be capable of proper operation in any position.

3.3 Performance characteristics.- The transistor performance characteristics shall be as specified in Tables I, II, and III.

3.4 Marking.- Except as otherwise specified herein, marking shall be in accordance with MIL-S-19500.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection.- Sampling and inspection shall be in accordance with MIL-S-19500, and as specified herein.

4.1.1 Inspection lot.- Applicable to the semiconductor device(s) covered herein, the term "inspection lot" shall be as defined in 4.3.2.1 of MIL-S-19500 except that the 6 week period time limitation therein shall be considered as not compulsory.

4.2 Qualification and acceptance inspection.- Qualification and quality conformance inspection shall be in accordance with MIL-S-19500, quality assurance provisions, and as otherwise specified herein. For qualification inspection, the requirement for tightened LTPD for each subgroup, as required in MIL-S-19500, Appendix C, paragraph 50.2 shall not apply: Groups A, B and C inspection shall consist of the examinations and tests specified in Tables I, II and III, respectively, herein. Quality conformance inspection shall include inspection of Preparation for Delivery (see 5.1 herein).

Table I.- Group A inspection

Test Method per MIL-STD-750	Examination or test	Conditions	LTPD	Symbol	Limits Min	Limits Max	Unit
	Subgroup 1		10				
2071	Visual and mechanical examination	—		—	—	—	—
	Subgroup 2		5				
3041	Collector-emitter cutoff current:	Bias Cond.C V_{BE}=0					
		V_{CE}=240 Vdc		I_{CES}	—	2.0	mAdc
3061	Emitter-base cutoff current	Bias Cond.D V_{EB}=10 Vdc		I_{EBO}	—	1.0	mAdc
3001	Collector-base breakdown voltage:	Bias Cond.D I_C=2.0 mAdc Pulsed: 1/					
				BV_{CBO}	240	—	Vdc
3011	Collector-emitter breakdown voltage:	Bias Cond.D I_C=3 Adc Pulsed: 1/					
				BV_{CEO}	200	—	Vdc
3026	Emitter-base breakdown voltage	Bias Cond.D I_E= 1 mAdc		BV_{EBO}	10	—	Vdc

Table I. - Group A Inspection (cont'd)

Test Method per MIL-STD-750	Examination or Test	Conditions	LTPD	Symbol	Limits Min	Max	Unit
	Subgroup 3		5				
3076	Forward-current transfer ratio	Pulsed: 1/ I_C=20 Adc V_C=2 Vdc		h_{FE}	30	120	---
3076	Forward-current transfer ratio	Pulsed: 1/ I_C=40 Adc V_{CE}=2 Vdc		h_{FE}	15	50	---
3076	Forward-current transfer ratio	Pulsed: 1/ I_C=90 Adc V_{CE}=5 Vdc		h_{FE}	10	40	---
3066	Base-emitter voltage	Test Cond. B I_C=90 Adc V_{CE}=5 Vdc Pulsed: 1/					
	STA4900			V_{BE}	---	1.5	Vdc
	STA9901			V_{BE}	---	2.0	Vdc
3066	Base-emitter voltage	Test Cond. B I_C=120 Adc V_{CE}=4 Vdc Pulsed: 1/		V_{BE}	---	3.0	Vdc
3071	Collector-emitter saturation voltage:	I_C=90 Adc I_B=15 Adc Pulsed: 1/					
	STA4900			$V_{CE(sat)}$	---	0.75	Vdc
	STA9901			$V_{CE(sat)}$	---	1.50	Vdc
3071	Collector-emitter saturation voltage	I_C=120 Adc I_B=24 Adc Pulsed: 1/		$V_{CE(sat)}$	---	2.0	Vdc

Table I.- Group A inspection (cont'd)

Test Method per MIL-STD-750	Examination or test	Conditions	LTPD	Symbol	Limits Min	Limits Max	Unit
	Subgroup 4		10				
3251	Pulse response:	Test Cond.B V_{CC}=90 Vdc R_C=1 Ohm R_B=1 Ohm V_{BE1}=10.5V V_{BE2}=11V					
	Turn-on time	—		t_{on}	—	7.0	usec
	Storage time	—		t_s	—	4.0	usec
	Fall time	—		t_f	—	1.0	usec
	Subgroup 5		10				
2/	High-temperature operation:	T_A= +150°C 3/					
3041	Collector-emitter cutoff current	Bias Cond.C V_{CE}=200 Vdc V_{BE}=0		I_{CES}	—	10	mAdc
—	Low-temperature operation:	T = -65°C 3/					
3076	Forward-current transfer ratio	Pulsed: 1/ I_C=90 Adc V_{CE}=5 Vdc		h_{FE}	10	—	—

1/ See 4.3.1 herein.

2/ In this subgroup, the sample units subjected to the High-Temperature Operation test shall be permitted to return to and be stabilized at room ambient temperature prior to their being subjected to the Low-Temperature Operation test.

3/ Measurement(s) shall be made after thermal equilibrium has been reached at the temperature specified.

Table II.- Group B inspection

Test Method per MIL-STD-750	Examination or test	Conditions	LTPD	Symbol	Limits Min	Limits Max	Unit
	Subgroup 1		20				
2066	Physical dimensions	1/					
	Subgroup 2		15				
2031	Soldering heat	One Cycle		—	—	—	—
1051	Temperature cycling	Test Cond.C except; 10 cycles, t=15 Min.at ea. temp. extreme		—	—	—	—
1056	Thermal shock (glass strain)	Test Cond.B		—	—	—	—
1021	Moisture resistance	No initial conditioning		—	—	—	—
	End-Point tests:						
3061	Emitter-base cutoff current	Bias Cond.D V_{EB}=10 Vdc		I_{EBO}	—	1.0	mAdc
3041	Collector-emitter cutoff current	Bias Cond.C V_{CE}=240 Vdc V_{BE}=0		I_{CES}	—	2.0	mAdc
3076	Forward-current current-transfer ratio	Pulsed: 2/ I_C=90 Adc V_{CE}=5 Vdc		h_{FE}	10	40	—

Table II.- Group B inspection (cont'd)

Test Method per MIL-STD-750	Examination or test	Conditions	LTPD	Symbol	Limits Min	Limits Max	Unit
	Subgroup 3		15				
2016	Shock	Non-operating; 1500 G; 3 blows of 0.5 msec ea. in orientations X1,Y1, Y2,Z1 (total=20 blows)		—	—	—	—
2056	Vibration, variable frequency	—		—	—	—	—
2046	Vibration fatigue	Non-operating		—	—	—	—
2006	Constant acceleration (centrifugal)	5,000G Orientations X1,Y1,Y2,Z1		—	—	—	—
	End-Point tests:						
	Same as for Subgroup 2 above						

Table II. - Group B inspection (cont'd)

Test Method per MIL-STD-750	Examination or Test	Conditions	LTPD	Symbol	Limits Min	Limits Max	Unit
	Subgroup 4		20				
2036	Terminal strength, terminal torque	Test cond. D1 Torque=24 oz-in; t=15 sec., base & emitter only		---	---	---	---
2036	Terminal strength, tension	Test cond. A t=10 sec., ea. term., weight=10 lbs (all terminals)		---	---	---	---
2036	Terminal strength, stud torque: STA4900	Test Cond. D2 Torque=120 lbs.-in. t=10±1 sec.		---	---	---	---
	STA9901	Test Cond. D2 Torque=12 lbs.-in., t=10±1 sec.		---	---	---	---
	Measurements during stud torque test 3/						
1071	Seal	Fine leak Test Cond. G or H Gross leak Test cond. A, C, D or F		---	---	5×10^{-7}	atm cc/sec
	Subgroup 5		20				
1041	Salt atmosphere (corrosion)	4/		---	---	---	---

Table II.- Group B inspection (cont'd)

Test Method per MIL-STD-750	Examination or test	Conditions	LTPD	Symbol	Limits Min	Limits Max	Unit
	Subgroup 6		10				
3051	Safe operating area (dc operation):			—	—	—	—
		5/ T_C= +100°C t=60 sec. $t_r \leq$ 6.0 sec. $t_f \leq$ 6.0 sec. 1 cycle					
	Test #1:	I_C=90 Adc V_{CE}=2.23 Vdc (P_T=200W)					
	Test #2:	(P_T=200W) I_C=4 Adc V_{CE}=50 Vdc					
	Test #3:	T_C= +100°C P_T=100W V_{CE}=200 Vdc					
	End-Point tests: Same as for Subgroup 2 above						

Table II.- Group B inspection (cont'd)

Test Method per MIL-STD-750	Examination or test	Conditions	LTPD	Symbol	Limits Min	Limits Max	Unit
	Subgroup 7		10				
3053	Unclamped inductive sweep	To be determined		—	—	—	—
	End-Point tests:						
	Same as for Subgroup 2 above						
	Subgroup 8		10				
3053	Clamped inductive sweep	Test Cond.B T_A=100°C t_r=1 usec t_f=1 usec I_B(on)=15A I_B(off)=15A I_C=90 Adc V_{CC}=200V R_L=0 L=1/ Clamping Diode f = 20 KHz		—	—	—	—
	End-Point tests:						
	Same as for Subgroup 2 above						

Table II.- Group B inspection (cont'd)

Test Method per MIL-STD-750	Examination or test	Conditions	LTPD	Symbol	Limits Min	Limits Max	Unit
	Subgroup 9		10				
1031;1032	High-temperature life (non-operating)	T_{stg}= +200°C t=340 hrs 8/		—	—	—	—
	End-Point tests:						
3061	Emitter-base cutoff current	Bias Cond.D V_{EB}=10 Vdc		I_{EBO}	—	2.0	mAdc
3041	Collector-emitter cutoff current	Bias Cond.C V_{CE}=240 Vdc V_{BE}=0		I_{CES}	—	9/ 10/	
3076	Forward-current transfer ratio	Pulsed: 2/ I_C=90 Adc V_{CE}=5 Vdc		h_{FE}	—	11/ 10/	
	Subgroup 10		10				
1026;1027	Steady state operation life:	T_C= +100°C t=340 hrs 8/ P_T=200W V_{CE}=30-40 Vdc		—	—	—	—
	End-Point tests:						
	Same as for Subgroup 9 above						

1/ See 4.3.3 herein.

2/ See 4.3.1 herein.

3/ With the transistor mounted in normal mounting position, the specified torque shall be maintained (torque-wrench removed) throughout each of the specified End-Point tests and measurements.

4/ Electrical rejects from the same lot under evaluation may be used for this test.

5/ See 4.3.4 herein.

6/ Filter choke (to be determined).

7/ Chokes (to be determined).

8/ See 4.2.3 herein.

9/ $^{+100\%}_{-50\%}$ or 200 uA, whichever is greater.

10/ Change from initial Group A reading.

11/ ±20%; however, h_{FE} - 10 shall be met.

Table III.- Group C inspection. 1/

Test Method per MIL-STD-750	Examination or test	Conditions	LTPD	Symbol	Limits Min	Limits Max	Unit
	Subgroup 1		20				
3151	Thermal resistance (junction-to-case)	—		θ_{J-C}	—	0.5	°C/W
1051	Temperature cycling	Test Cond.C1 except: t= 15 min.at ea. temp. extreme		—	—	—	—
	Subgroup 2		λ=10				
1031	High-Temperature life (non-operating):	T_{stg} = +200°C t=1000 hrs 2/		—	—	—	—

Table III.- Group C inspection 1/ (cont'd)

Test Method per MIL-STD-750	Examination or test	Conditions	LTPD	Symbol	Limits Min	Limits Max	Unit
	Subgroup 2(cont'd)						
	End-Point tests:						
3061	Emitter-base cutoff current	Bias Cond.D V_{EB}=10 Vdc		I_{EBO}	—	2.0	mAdc
3041	Collector-emitter cutoff current	Bias Cond.C V_{CE}=240 Vdc V_{BE}=0		I_{CES}	—	3/ 4/	
3076	Forward-current transfer ratio	Pulsed:(see 4.3.1) I_C=90 Adc V_{CE}=5 Vdc		h_{FE}	—	5/ 4/	
	Subgroup 3		λ=10				
1026	Steady state operation life:	T_C= +100°C t=1000 hrs V_{CE}=30-40 Vdc P_T=200W 2/		—	—	—	—
	End-Point tests:						
	Same as for Subgroup 2 above						
	Subgroup 4		15				
	Marking resistance to solvents	6/ (see 4.3.5 herein)		—	—	—	—

1/ See 4.2.4 herein. 2/ See 4.2.3 herein. 3/ +100% or 200 uA, whichever is greater. -50%

4/ Change from initial Group A reading. 5/ ± 20%; however, h_{FE} - 10 shall be met.

6/ Electrical rejects from the same lot under evaluation may be used.

4.2.2 Table 1 acceptance criteria for qualification inspection.- For qualification inspection, all units that are to be subjected to group B and group C inspection shall first be subjected to all tests of group A inspection using a combined LTPD of 5 for group A acceptance criteria.

4.2.3 Group B-Group C life test samples.- Samples of transistor types, that have been subjected to group B, 340-hour life test may be continued on test for 1000 hours in order to satisfy group C life test requirements. These samples shall be predesignated, and shall remain subjected to the group C 1000-hour evaluation after they have passed the group B, 340-hour acceptance criteria. The cumulative total of failures found during 340-hour test and during the subsequent interval up to 1000 hours shall be computed for 1000-hour acceptance criteria. (See 4.2.4 below).

4.2.4 Group C testing.- Group C tests shall be performed on a lot every 6 months. (See Table III herein.) The contractor shall, throughout the course of a contract or order, permit the Government representative to scrutinize all test data and findings covering manufacturer's test program on group C characteristics and parameters for the product concerned. Upon determination by the Government inspector (in advance of group C, 6-month, test results) that group C parameters are not being adequately met, the Government inspector may require lot-by-lot inspection, normally for a minimum of 3 consecutive lots, to be performed for required group C tests.

4.2.5 Disposition of sample units.- Sample units that have been subjected to group B, subgroup 2 and 5 tests shall not be delivered on the contract or order. Sample units that have been subjected to and have passed group B, subgroup 1,3,4, 6,7,8,9, and 10, and all group C tests (these tests to be considered non-destructive), may be delivered on the contract or order provided that, after group B and C inspection is terminated, those sample units are subjected to and pass group A inspection. Defective units from any sample group that may have passed group inspection shall not be delivered on the contract or order until the defect(s) has been remedied to the satisfaction of the Government.

4.2.6 Copies of lot-inspection data.- When specified in the contract or order, one copy of the Quality Conformance inspection data, including manufacturer's test data and findings, covering the device inspection lot being shipped shall accompany the device(s) concerned.

4.3 Particular examination and test requirements.-

4.3.1 "Pulsed"-conditions measurements.- Measurements required herein to be effected under pulsed conditions, shall be made in accordance with "Pulse Measurements" requirements in Section 4 of MIL-STD-750.

4.3.2 Mechanical damage resulting from tests.- Except for intentionally deforming, mutilating, or dismembering mechanical-stress tests to which samples are subjected, there shall be no evidence of mechanical damage to any sample unit as a result of any of the groups A, B, or C tests.

4.3.2.1 Durability of terminal lugs.- The lug ends of terminals shall remain intact on terminals throughout all physical, mechanical, and environmental tests herein.

4.3.3 Terminal strength (Stud Torque) test.- Acceptance criteria for external threaded parts shall be in accordance with Handbook H-28.

4.3.4 Safe operating area (DC Operation) test.- Each transistor under test shall sustain the applicable test conditions and the following acceptance criteria shall apply:

(a) I_C (for each transistor) shall not vary more than $\pm$ 10% during the dc operation; and

(b) All other specified End-Point test(s) limits shall not be exceeded, after the dc-operation test.

(c) Correlation note: Satisfactory endurance of the transistors throughout tests 1,2,3 respectively (per Table II, Subgroup 6 herein) is directly associable with ascertainment of the "safe operating area" for the transistors as illustrated in the nomograph of Figure 1.

4.3.5 Marking resistance to solvents test.- The device samples shall be subjected to test per Method 215 in MIL-STD-202, except that the following details shall apply:

(a) All surface areas on the body of the device where marking has been applied shall be brushed.

(b) All marking shall have remained legible, and there shall be no evidence of mechanical damage to the device, upon examination after test.

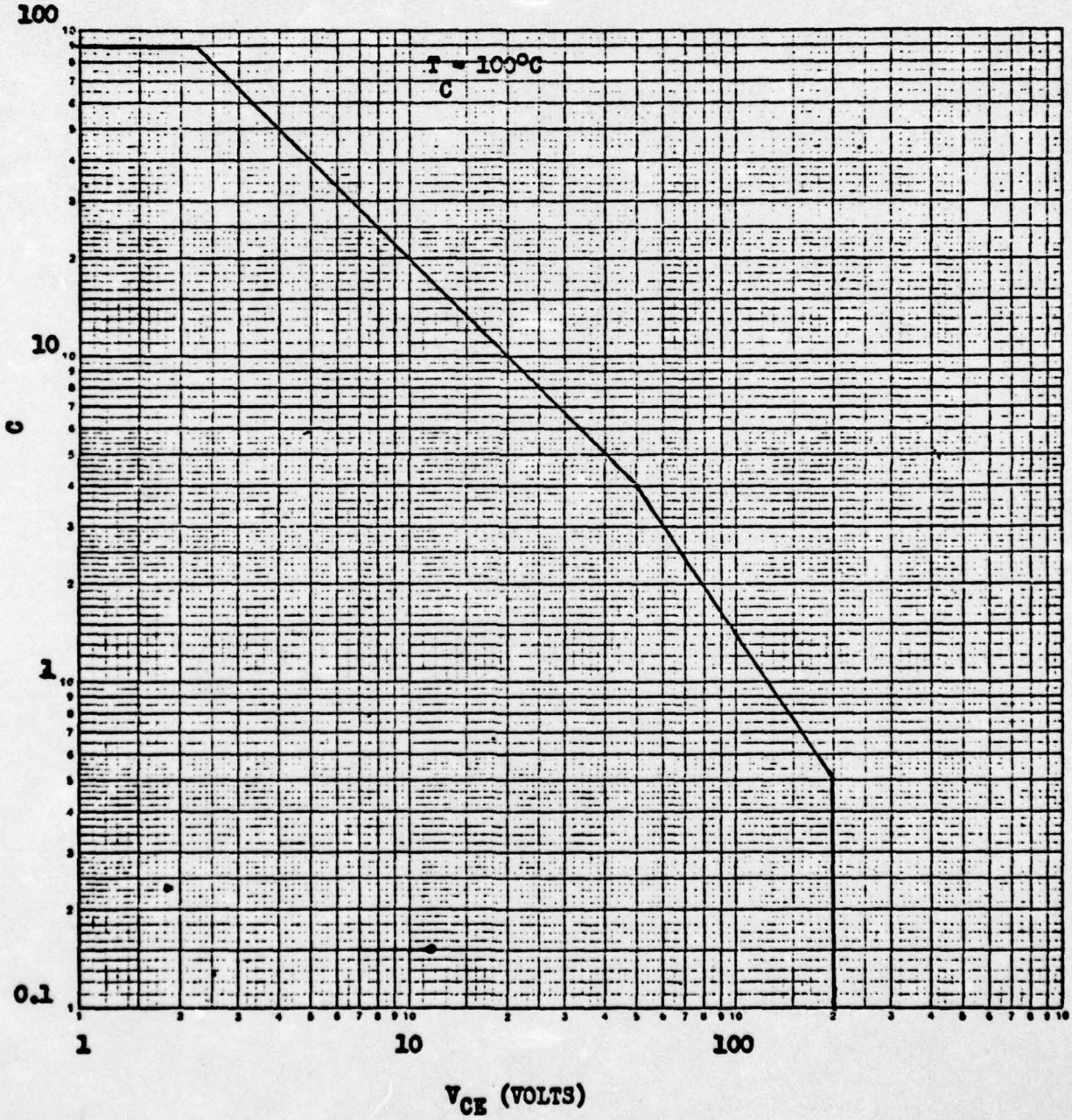

FIG. 1 DC SAFE OPERATING AREA NOMOGRAPH

4.4 Preproduction sample approval.- The preproduction sample approval requirements of SC-A-46600 replace any qualification requirements which can be referred to the product covered herein. The production testing requirements are as herein specified.

5. PREPARATION FOR DELIVERY

5.1 Preparation for delivery.- Preparation for delivery, and the inspection of preparation for delivery, shall be in accordance with MIL-S-19500.

6. NOTES

6.1 Notes.- The notes included in MIL-S-19500, with the following additions or exceptions, are applicable to this document.

6.2 Application guidance.- To insure proper circuit application, particular attention should be given to the differential voltage and gain characteristics, and rating, pertinent to the individual transistor types covered herein.

6.3 Ordering data.- Lot-inspection data: See 4.2.6 herein.

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER

2. GOVT ACCESSION NO.

3. RECIPIENT'S CATALOG NUMBER

4. TITLE (and Subtitle)
Production Engineering Measure for High Current, Fast-Switching Transistors

5. TYPE OF REPORT & PERIOD COVERED
Ninth Quarterly Progress Report-1/19/75-4/19/75

6. PERFORMING ORG. REPORT NUMBER

7. AUTHOR(s)
Silicon Transistor Corporation

8. CONTRACT OR GRANT NUMBER(s)
DAAB05-73-C-2032

9. PERFORMING ORGANIZATION NAME AND ADDRESS
Silicon Transistor Corporation
Katrina Road
Chelmsford, Massachusetts 01824

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS

11. CONTROLLING OFFICE NAME AND ADDRESS
Department of the Army
U.S. Army Electronics Command, Fort Monmouth NJ

12. REPORT DATE
13 June 1975

13. NUMBER OF PAGES
24

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)

15. SECURITY CLASS. (of this report)
Unclassified

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)
Approved for public release, distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)
High Current, Fast-Switching Transistors

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)
During this period, the First Article Test Report was approved. A plant survey was conducted to monitor production rates. Permission was obtained to start the pilot run. The pilot run was begun. Electrical and physical parameters of selected runs are shown. 400 chips were selected for encapsulation. A total of 232 devices were accepted at pre-cap visual inspection showing that the program is on schedule.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)