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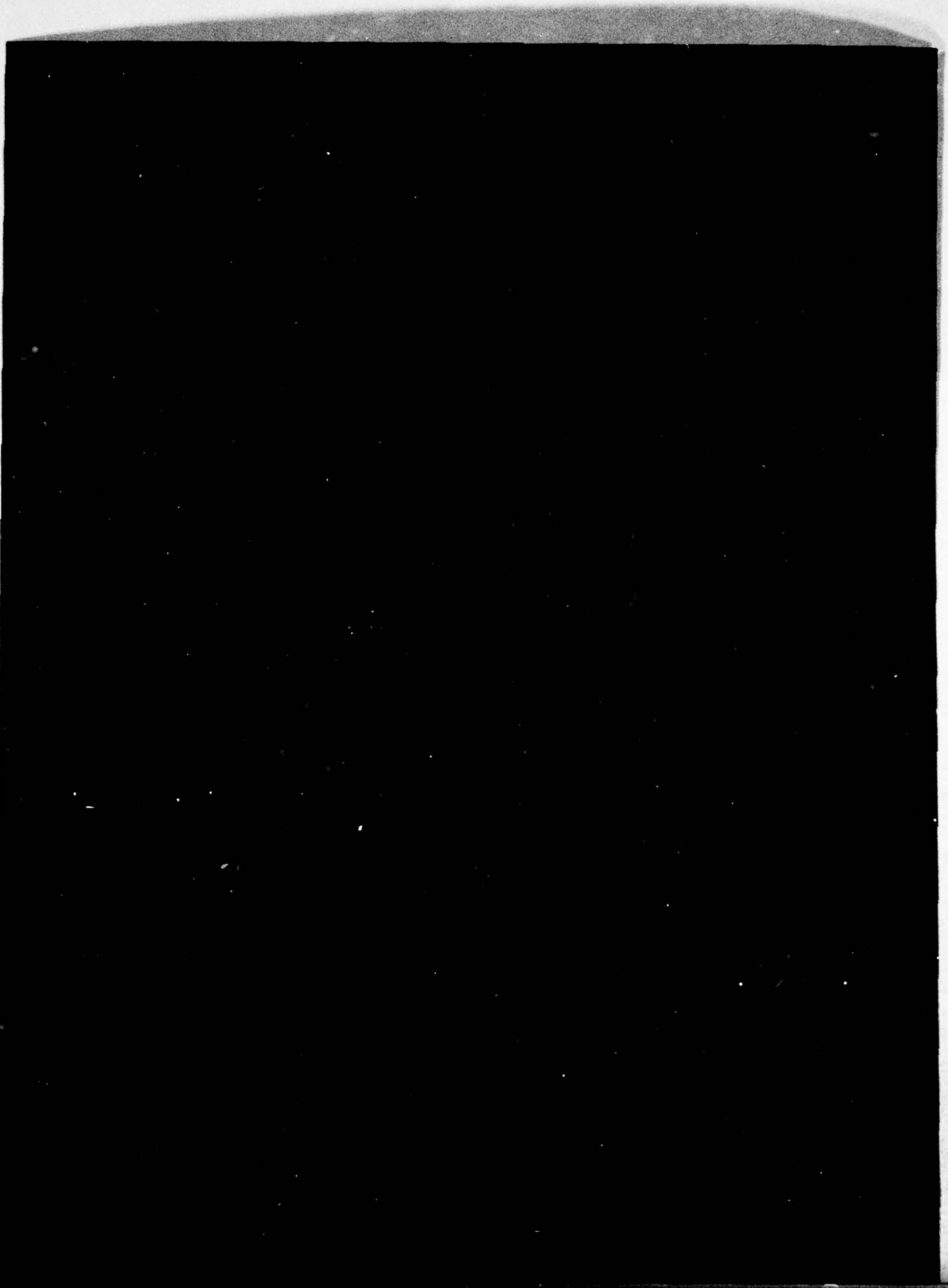

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This report contains well-known, but seldom assembled, information necessary for understanding and initiating the design of complementary metal-oxide semiconductor (CMOS) large-scale integrated circuit (LSI) digital logic using arrays of gates. A description is given of how CMOS field-effect transistors operate

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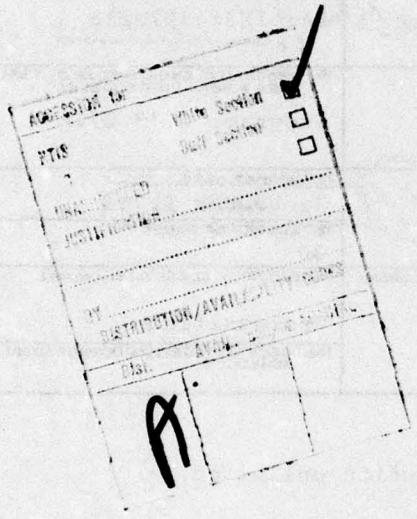
and how logic elements are made using them. The design of logic circuits is given, including brief descriptions of Boolean algebra and Karnaugh maps. Finally, custom LSI's and the CMOS gate array are briefly discussed.



CONTENTS

FIGURES

FIGURES (Cont'd)

1. INTRODUCTION

Advancing solid-state electronics has now brought to reality large-scale integrated circuits (LSI's). These integrated circuits are finding wide commercial use in hand-held calculators, wrist watches,[1] and automobile applications.[2] Most of these circuits are custom LSI's using metal-oxide semiconductor (MOS) field-effect transistors (FET's). A conventional handcrafted custom LSI is expensive to design in the first place and almost as expensive to modify later. An LSI has about seven levels of masking with associated etchings, dopings, and diffusions. Most changes in a conventional custom LSI necessitate a change in all seven masks, therefore causing the high expense for modifications. A recent advance that has significantly lowered initial costs and modification costs is the development of gate arrays.

One array consists of 1104 transistors (RCA TCC 051) on a 0.3-in. square silicon chip. It includes a number of crossover channels, input-output buffers, and protection circuits. The array is made with a fixed set of masks and, as a basic building block, comes with a metalized surface. The transistors are interconnected by removing the metal where conductors are not required. Only one mask for this metalization pattern is made up for each application, and only one mask has to be changed to modify the circuit. Furthermore, the specific layout of the chip can be done by the practicing circuit engineer using only a few guidelines.

This report summarizes the background information that a circuit engineer requires to proceed with the design of a custom digital LSI using a complementary MOS (CMOS) gate array.

2. DEVICE OPERATION

A cross-sectional view of a P-channel MOS FET is shown in figure 1(a). The metal is aluminum, the oxide SiO_2, and the semiconductor silicon. Source and drain are interchangeable. The device works as follows:[3] It is biased so that the junctions formed at

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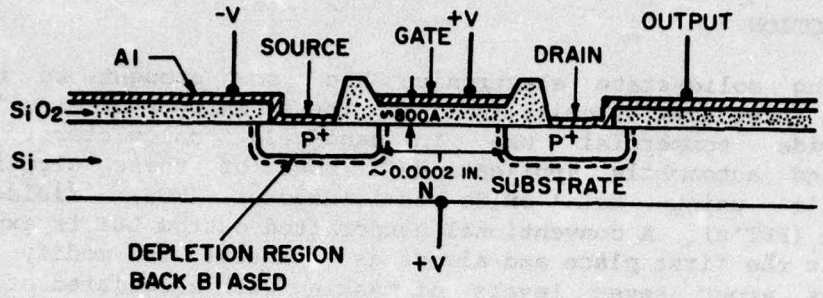
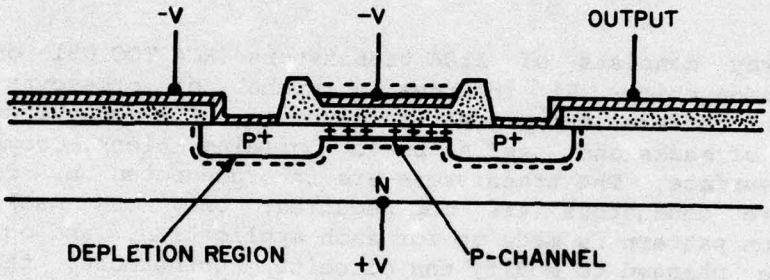
[1] *S. S. Eaton, Timekeeping Revolution through COS/MOS Technology, RCA COS/MOS Technology (1973), 33-41.*

[2] *D. K. Morgan, COS/MOS Integrated Circuits in the Automobile Environment, RCA COS/MOS Technology (1973), 45-51.*

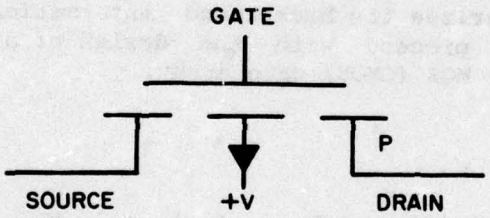
[3] *R. A. Bishop and D. R. Carley, Fundamentals of COS/MOS Integrated Circuits, RCA COS/MOS Technology (1973), 8-11.*



(a) GATED OFF



(b) GATED ON



(c) SYMBOL

Figure 1. P-channel MOS FET.

the P^+-N silicon interfaces are either back biased, at zero bias, or in between. They draw no current ($\sim 10^{-9}$ A). The normal minority carrier injection mechanism for transistor operation is not used. Instead, when a negative voltage is applied to the gate, as shown in figure 1(b), the high field effect through the thin oxide forces holes to be attracted to the surface of the N-type silicon under the gate. This field causes a thin channel, which is doped like P-type silicon, to exist and makes a

thin depletion region below it that now includes both junctions. Current is able to flow between source and drain. The resistance of the P-channel is typically 1000 ohms for a 0.001-in.-wide channel (× 0.002-in. long). The gate has a capacitance of about 0.4 pF, while the source and drain each have about 0.1 pF for P-channel and 0.2 pF for N-channel devices. Because the depletion region surrounds the conductive region, no current flows into the substrate, and the active region is well isolated from other active devices on the same substrate (very important in integrated circuits).

To keep the leakage current low when no gate voltage is applied, the silicon surface must be very pure, because the depletion region comes up to the surface edge. Any surface impurities increase the leakage current. The CMOS is specified at less than 10 nA (10^{-8} A) and typically has 0.1 to 1 nA (10^{-10} to 10^{-9} A). A value of about 10^{-4} is required for digital circuit operation where each gate is allowed to dissipate 1 mW. A chip with 1000 gates might rather be limited to 10^{-5} A to avoid heat-sinking problems.

The gate voltage required to attract enough holes to the surface to make a conductive P-channel is called the threshold voltage. This voltage is determined by the built-in potential of the silicon surface under the gate, by the thickness and dielectric constant of the oxide, and by the doping density of the N-type substrate. The thinner the oxide or the higher its dielectric constant, the lower the threshold voltage. It also takes a very strong field to attract enough holes to convert heavily doped N-type semiconductor to P-type with mobile carriers as required for the channel. Therefore, the lower the doping density of the N-type material, the lower the threshold voltage. These factors combine, forcing a compromise threshold voltage of 1 to 2 V.

The FET as described is an enhancement-mode transistor. It is nonconductive unless a gate voltage is applied. By arranging doping densities, a depletion-mode FET can be made, but it does not have the low-power-consumption properties of enhancement-mode transistors. Care must be exercized in fabricating FET's that impurities are not introduced on the surface. These impurities can move the threshold voltage and increase the leakage current. Moving the threshold voltage can change an enhancement-mode transistor to depletion mode and can change the gain characteristics, frequency response, and immunity to noise.

The symbol for the enhancement-mode, P-channel FET is shown in figure 1(c). The arrow points to the N-most material, which in this figure is the substrate. In an N-channel device, the arrow points to the channel. The bias voltage is applied in the polarity to back bias the diode if the symbol were to represent a diode. The P in the symbol

may be anywhere in the region of the source-channel-drain area and represents the polarity of the channel. Sometimes the arrow or letter is omitted. The source and drain are interchangeable. The line connecting source and drain should be shown as a broken line for enhancement-mode FET's and as a solid line for depletion-mode FET's. Very little use is made of depletion-mode FET's in digital circuits as active devices, so they are seldom seen, and frequently, authors show a solid line for enhancement-mode FET's. It is best to assume that an FET is an enhancement-mode device, unless there is some statement to the contrary.

In the CMOS, there are an equal number of P-channel and N-channel FET's. Figure 1(a) and (b) could be used to describe an N-channel device by switching P and N and + and -. The mobility of the carriers in an N-channel is about twice as high as for the P-channel; therefore, the P-channels are made about twice as wide to keep the output impedances of the two devices equal.

The dc characteristics of a typical N-channel MOS FET are shown in figure 2.

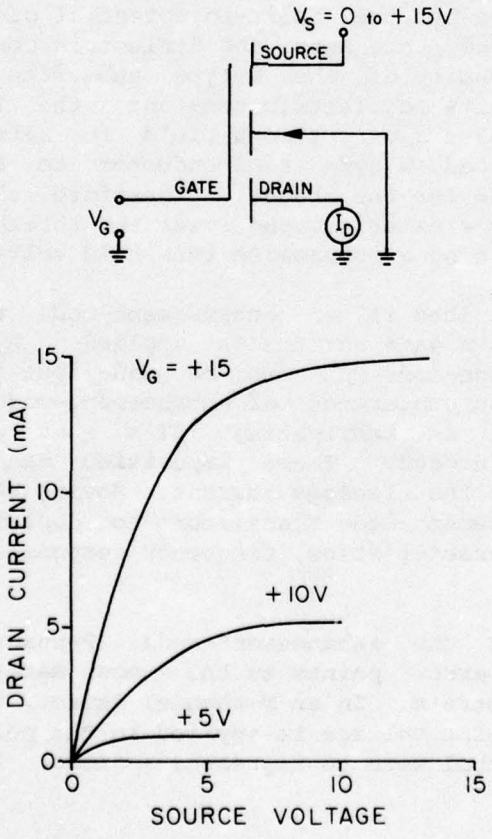
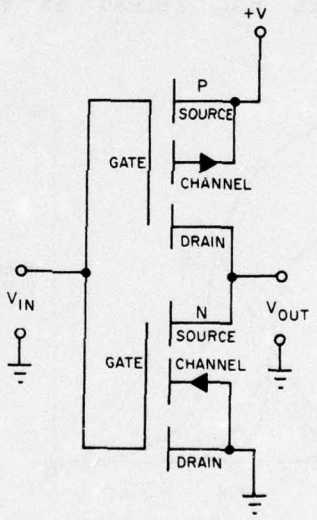


Figure 2. MOS FET voltage-current charteristics.

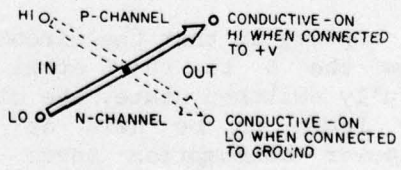
3. CIRCUIT OPERATION

3.1 Inverter

The most basic circuit using a CMOS FET pair is shown in figure 3(a). Conventionally, the P-channel FET is at the top with its substrate connected to +V, and the N-channel FET is at the bottom with its substrate connected to ground. Inputs and outputs are between 0 and +V. The +V is a "1" or HI and 0 (ground) is a "0" or LO. When V_{in} is 0 V, the N-channel FET (fig. 3(a), lower transistor) has no field induced by the gate, and it is OFF (nonconductive). The P-channel FET (fig. 3(a), upper transistor) has a relative -V applied to the gate (in the back bias polarity if it were a diode), and therefore it is forced into the conduction state. Since the source is connected to +V, the output is +V (HI).



(a) CMOS PAIR



(b) SWITCHING SENSE OF CMOS PAIR

Figure 3. CMOS pair operation.

When V_{in} is +V, then there is no high field on the P-channel FET, and it is OFF. The N-channel FET is (back) biased so that it is conductive. Since its drain is connected to ground, V_{out} is LO. The operation of this circuit can be visualized as shown in figure 3(b). Since the circuit changes LO to HI and HI to LO, it is an inverter or a logic NOT gate.

The voltage-current characteristics of the inverter are shown in figure 4. This inverter has several important properties when used in digital circuits. The voltage input-output is nonlinear so as to improve the squareness of input pulses. This nonlinearity helps 0's to stay 0's and 1's to stay 1's, makes the output more binary, and improves the immunity to noise of the logic circuit. The nonlinearity is well shaped for a wide range of power-supply voltages. A regulated power supply is not required to operate these circuits; a given circuit can be operated satisfactorily over the wide range of power-supply voltages. The sacrifice made for lower voltages is slower speed, because the conductivity of the channel is not raised as high by the lower gate voltage.

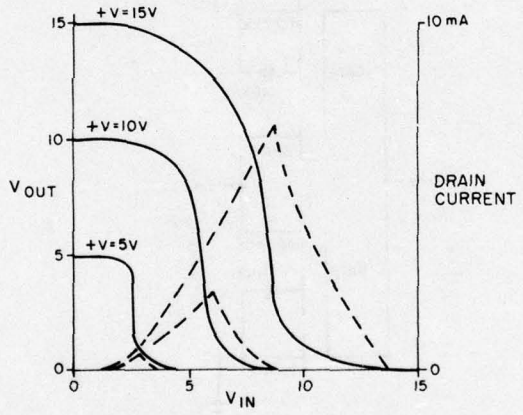


Figure 4. Inverter voltage-current characteristics.

The second property is that the circuit draws current only in the transition from the 0 to the 1 state and vice versa--during switching. In the fully switched state, the circuit draws only leakage current, permitting logic to be held at very low sustenance power levels. This low power consumption saves power-supply energy and permits the FET's to be densely packed, since they are not generating much heat.

Third, the CMOS FET's can be connected directly to each other, requiring no additional resistors, capacitors, or inductors. Therefore, they can be easily connected together to make an integrated circuit. Also, the output impedance is about 1000 ohms, while the input impedance is capacitive (the gate capacitance). Therefore, one FET can drive a large number of other FET's--fan outs up to about 50.

The limits on fan out and loading of FET's are set by the switching speed and power dissipation that can be tolerated. The capacitances of output lines and input gates are added up to determine the capacitive load. The 1000-ohm output impedance and this capacitance determine the RC time constant for propagation delay. A typical propagation delay is 25 ns. The power dissipation is given by CV^2f, in which C is the total capacitance, V is the supply voltage, and f is the data rate frequency. The power dissipation of a gate for several typical voltages and loads is shown in figure 5. A typical transistor-transistor logic (TTL) gate requires 7.5 mW with a speed of 12 ns. Thus, the CMOS consumes less power for average switching rates on an array of less than several megahertz.

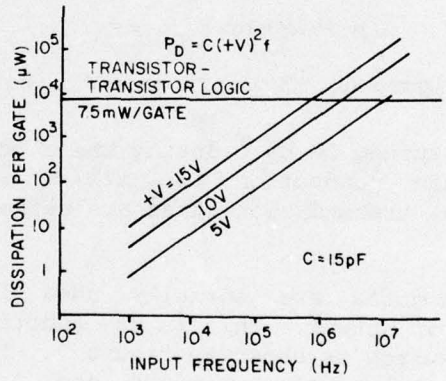


Figure 5. Power dissipation.

3.2 Transmission Gate

The second basic building block for digital logic using CMOS FET's is the transmission gate. The FET's are arranged as shown in figure 6(a). The gate works in either direction. It is turned on by the positive clock pulse C. $\overline{C}$ is the complement of the clock pulse ($\overline{C}$ is normally 1, 0 during the clock pulse). Normally, the N-channel FET has a 0 on the gate, and the source and drain are not conductively connected. The presence of a clock pulse puts a 1 on the N-channel FET gate, providing the high electric field that produces the conductive path between source and drain, turning ON the FET. In a similar manner,

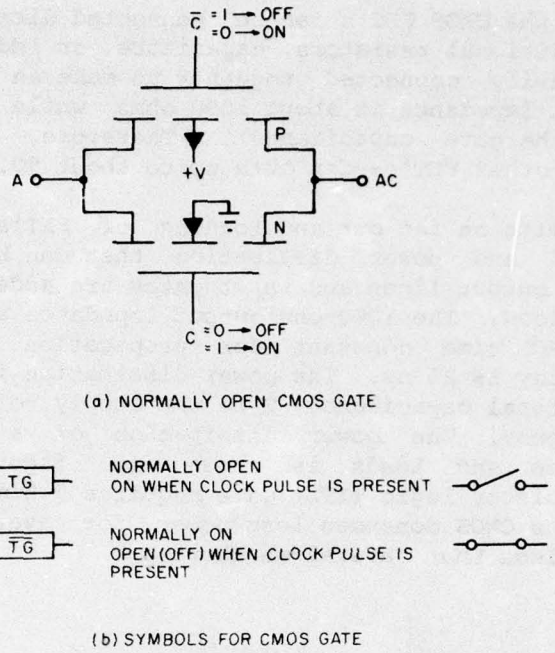


Figure 6. CMOS transmission gate.

the P-channel FET is turned ON by $\overline{C}$ during the clock pulse. Both FET's are necessary to obtain conduction for all V where $0 < V < +V$. For subsequent discussion, transmission gates are represented by the symbols shown in figure 6(b).

Transmission gates are normally used in complementary pairs with a common input or output. This is the function of the single-pole double-throw (SPDT) switch as shown in figure 7. This is also an analog switch, since the linearites of A and B are preserved under normal switching conditions.

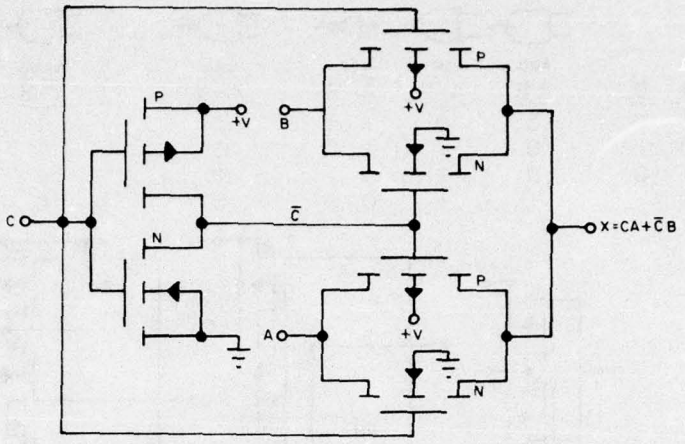


Figure 7. Single-pole double-throw or analog switch.

3.3 Logic Gates

The truth table and layouts using the CMOS for various logic gates are shown in figure 8.

An AND circuit produces a HI output only if all of the inputs are HI. Since one stage of CMOS produces a logic sense inversion, the NAND is the more basic circuit, and the unique output is LO. Since the N-channel FET's produce LO output when they are conductive, they are placed in series in the NAND circuit so that the output is LO only when all of the inputs are HI. (Recall from figure 3(b) that a HI input forces the N-channel FET's into conduction, whereas a LO input forces the P-channel FET's into conduction.) Since the NAND output should be HI for all other input conditions, the P-channel FET's are placed in parallel as shown in figure 8.

An OR circuit produces a HI output if any one of the inputs is HI. The NOR thus produces a LO output when any one of the inputs is HI. To get a LO output most of the time, the N-channel FET's must be placed in parallel as shown in figure 8. Since the NOR output should be HI only when all of the inputs are LO, the P-channel FET's are placed in series.

The operation of the NOT circuit was discussed with figure 3. When AND or OR logic functions are required with CMOS, a NOT is added to a NAND or NOR.

In figure 8, the little circles at the output or input of logic symbols indicate logic inversion (the NOT function). Logic inversion of a variable is indicated by a bar over the variable or by a prime on the variable. For example, $\bar{B}$ or B' is called "not B."

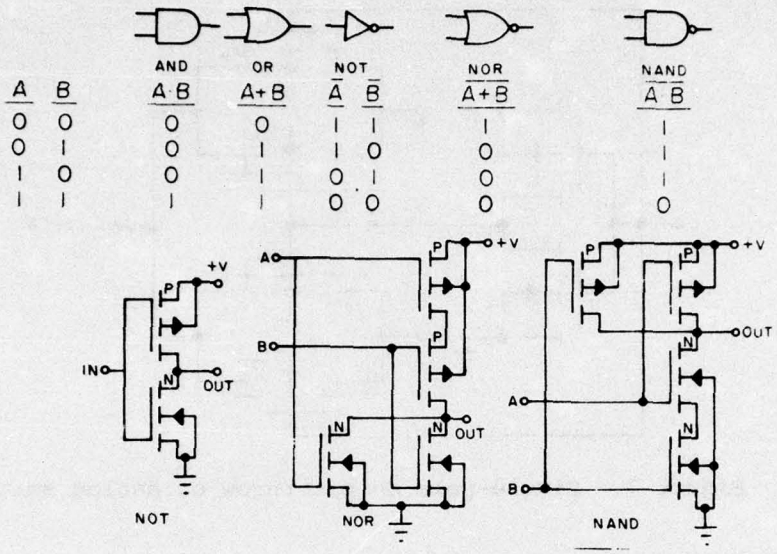


Figure 8. CMOS logic circuits.

4. LOGIC CIRCUITS

4.1 Memory Element/Shift Register

For a CMOS gate to stay latched in a state, its input must be tied to another CMOS in a way that provides regenerative feedback. The combination of NOT gates and transmission gates shown in figure 9 provides this condition. Since $\overline{TG}$ is normally closed, the master section tracks the data voltage (D) until a clock pulse comes along. At the leading edge of the clock pulse, TG closes, and the master loop is latched into the new D state existing during latching. Since the slave input TG is closed also by the leading edge of the clock pulse, $\overline{D}$ (the output of the master) is fed to the slave circuit. At the end of the clock pulse, the master is still in its latched state so that when the TG input to the slave opens, that state is retained by the slave circuit. Through the clock cycle, the input logic state D has been transferred from the input of the master loop to the output of the slave loop. The slave loop retains its logic state until another clock pulse comes along. The slave loop by itself is the smallest memory element. This positive clock shift register element (or basic D-type flip-flop) is leading-edge triggered logic. By interchanging TG and $\overline{TG}$, it is made into trailing-edge logic (negative clock).

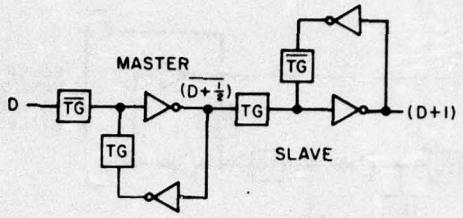


Figure 9. Shift register: basic D-type flip-flop (positive clock).

These shift registers can be added in series for providing logic delay or for decoding a serial bit word of any length. The serial bit word comes in on one line and is converted by the shift register to a parallel line output in a hold state to be used by the other logic. The clock is applied to the shift register only when the word is coming in. This is a serial-in, parallel-out decoder.

4.2 Presettable D-Type Flip-Flop

A parallel-in, serial-out decoder can be made by replacing the NOT gates by two-input NOR gates as shown in figure 10. Then the shift register element can be preset, and when the clock is applied, the serial word is shifted out to the right. In figure 10, buffer outputs are shown added to maintain fast switching when required.

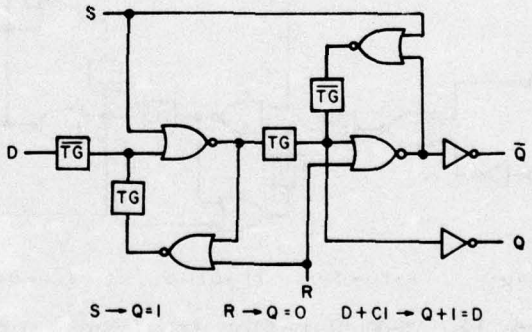


Figure 10. Presettable D-type flip-flop (positive clock).

4.3 Frequency Divider

A frequency divider (scale-of-two counter) is made by feeding the inverted slave output of a shift register circuit back into the master as shown in figure 11. The input to the divider is the clock, and the output provides the clock for the next divider stage. The counter can be made presettable by use of NOR gates in place of NOT gates, as is done for the D-type flip-flop.

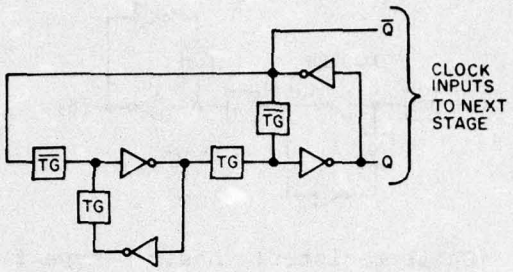


Figure 11. Frequency divider stage (clock pair).

4.4 J-K Flip-Flop

The J-K flip-flop (fig. 12) has two data inputs. When J or K is HI during a clock pulse, J sets the output HI, or K sets it LO (reset). When both J and K are LO during a clock pulse, the logic state of the output is not changed. When J and K are HI during a clock pulse, the logic state of the output is changed to the other state. It is basically a D-type flip-flop with additional logic to handle the two inputs and their relationship to the previous output.

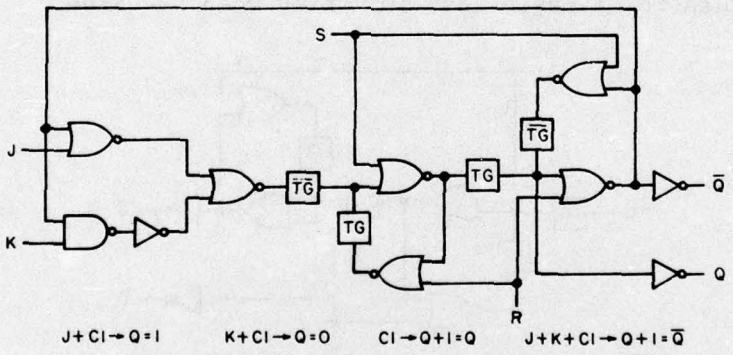


Figure 12. J-K flip-flop (positive clock).

5. DERIVING LOGIC CIRCUITS FROM TRUTH TABLES

5.1 Truth Table

A truth table[4] shows the output of a circuit for all possible combinations of the inputs. A D-type flip-flop is converted to a J-K flip-flop by the addition of some logic to the input. This input logic circuit serves as an example to show how a truth table leads to a logic circuit.

Based on the description of the operation of a J-K flip-flop just given, the truth table shown in figure 13 is derived. Q is the previous output of the D-type flip-flop as shown in figure 12. D is the new input to the D-type flip-flop.

J	K	Q	D
0	0	0	0
1	0	0	1
0	1	0	0
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

$D = J K'Q' + J KQ' + J'K'Q + JK'Q$

$D' = J'K'Q' + J'KQ' + J'KQ + JKQ$

Figure 13. J-K input truth table (to D-type flip flop).

The canonical logic expressions for the table also are shown in figure 13. Primed letters are in the inverse logic state of unprimed letters. Either equation gives the function. The D equation is derived by taking the rows for which D is 1. The first term produces a logic 1 when J = 1 AND K' = 1 (K = 0) AND Q' = 1(Q = 0). The other terms are similarly composed. When any one of the terms is one, then D = 1. Each term is thus a product and can be realized by using a three-input AND circuit (fig. 8). The sum of the terms is an OR function, which can be realized by connecting the output of the AND circuits to a four-input OR circuit. The output of the OR circuit provides the logic state D.

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[4] *A. B. Marcovitz and J. H. Pugsley, Introduction to Switching System Design, John Wiley and Sons, New York (1971).*

Sometimes it may be more convenient to use the second equation, instead. Each term is made up by using AND circuits as before, but to get D as an output, a NOR circuit instead of an OR circuit is used for combining them.

The equations of figure 13 do not use the minimum number of logic elements. These algebraic equations can be simplified by using Boolean algebra or some tabular constructs such as a Don't Care table or a Karnaugh map.

5.2 Boolean Algebra

The more useful basic relationships of Boolean algebra are shown in figure 14. Either primes or bars can be used to denote an opposite state. Normally, bars are used to denote it in logic diagrams. DeMorgan's Theorem can be stated as "The NOT of the sum is equal to the product of the NOT's" or "The NOT of the product is equal to the sum of the NOT's." This theorem is useful in converting logic circuits to NOR's and NAND's as required for CMOS LSI. The equations of figure 13

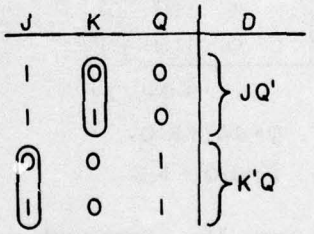
1. X = EITHER 1 OR 0
2. X' = OPPOSITE STATE OF X
3. $X+Y=0$ ONLY IF BOTH = 0 (OR)
   $XY=1$ ONLY IF BOTH = 1 (AND)
4. ASSOCIATIVE $(X+Y)+Z=X+(Y+Z)$
   $(XY)Z=X(YZ)$
5. ABSORPTION $X+X=X$
   $X\cdot X=X$
6. COMMUTIVITY $X+Y=Y+X$
   $XY=YX$
7. $X+0=X$ $\quad X\cdot 1=1$
8. $X\cdot 0=0$ $\quad X+1=1$
9. $X+X'=1$ $\quad X\cdot X'=0$
10. DISTRIBUTIVE $X(Y+Z)=XY+XZ$
    $X+YZ=(X+Y)(X+Z)$
11. $X+XY=X$
    $X(X+Y)=X$
12. $X+X'Y=X+Y$
    $X(X'+Y)=XY$
13. $(X')'=X$
14. $(X_1+X_2+\cdots+X_M)'=X_1'\,X_2'\cdots X_M'$
    $(X_1\,X_2\cdots X_M)'=X_1'+X_2'+\cdots+X_M'$
    } DE MORGAN'S THEOREM

Figure 14. Boolean algebra.

could be simplified by use of Boolean algebra, but unless a logic designer is familiar with the basic relationships and the standard tricks for manipulating them, the algebraic reduction is very tedious and subject to error. Fortunately, some tabular constructs (e.g., Don't Care tables and Karnaugh maps) permit direct reduction quite simply when the number of input variables is not too high. Computer programs are available to reduce the equations for digital logic and are almost a must for logic having five or more input variables.

5.3 Don't Care Table

Don't Care tables for the J-K input truth table are shown in figure 15. In the upper example, the "1" rows are arranged that provide D. The rows are paired up so that those that are different for only one input variable are together. Since the output is a "1" independent of the state of that input, the output is "don't care." It is only a function of the other input variables. In like manner, the lower table provides D' in a reduced algebraic form. These equations are equivalent to those given in figure 13 and could have been derived by using Boolean algebra as defined in figure 14. The shorter equations require fewer logic elements.



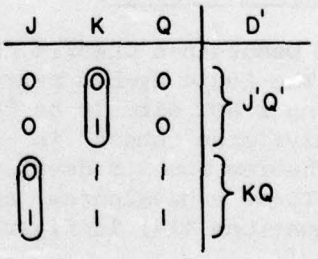


Figure 15. "Don't Care" tables.

5.4 Karnaugh Map

A systematic arrangement for putting input logic statements next to each other that are different in only one term is the Karnaugh map as shown in figure 16. It is easily constructed in two dimensions for up to four input variables. The J-K column is rolled through, in that each row is different from the other in only one digit. Also, the bottom can be rolled onto the top in the same manner. If there were four input variables, there would be four rows of possible outputs (instead of two), and the indexing of these rows would be rolled, as well. In finding reduced solutions, the 1's or 0's are grouped in one or two dimensions in groups of two or four on a side. The larger the group, the simpler the logic expression to provide the function. Any element can belong to more than one group, to include all elements in groups and provide the simplest logical expression. The Karnaugh map provides the same equations as the "Don't Care" tables of figure 15.

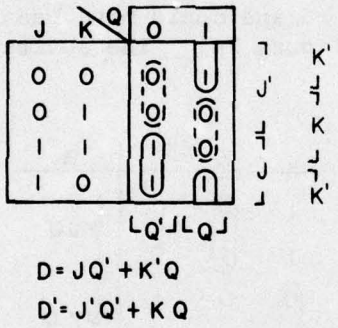


Figure 16. Karnaugh map.

5.5 Converting to NOR's and NAND's

The statement of DeMorgan's Theorem for two input variables is shown in figure 17(a). The logic symbol representation of it is shown below the equation. Adding a NOT circuit to the output of each circuit produces the symbol equivalence shown in figure 17(b). The other statement of DeMorgan's Theorem and its developed symbol equivalence are shown in figure 17(c). These equivalences apply for any number of inputs as indicated in equations (14) in figure 14.

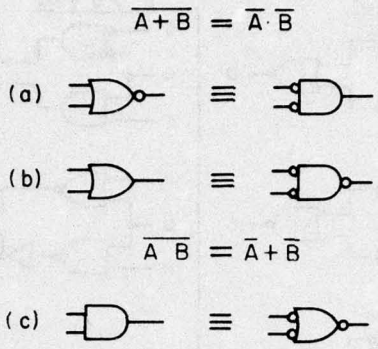


Figure 17. DeMorgan's Theorem.

With the identies shown in figure 17, all OR's and AND's in a logic diagram can be converted to NAND's and NOR's to minimize the number of inverters required in using CMOS LSI.

An easy way to visualize the identities is to consider the OR's and AND's as plump chickens. They can be converted respectively to NAND's and NOR's by having the appropriate tight girdle put on them. The girdle is so tight that it causes the chicken to lay an egg (at the output) and her eyes to bulge out (at the inputs). The input and output circles are NOT's that can be pushed to either end of a connecting line. Two NOT's cancel, or a NOT can be pushed through a logic symbol by being changed as shown in figure 17(a). To convert a logic diagram to NAND's and NOR's, every other logic element should thus be converted by using DeMorgan's Theorem. The NOT's are then moved around so that they are on the outputs of all of the logic symbols. If any are left over, they can be canceled out by having NOT logic elements (inverters) added as shown in figure 8.

When these transformations are applied to the equations for the J-K flip-flop input, the logic diagrams evolve as shown in figure 18. Either logic circuit provides the desired function. Both take J and K as inputs and require the same number of CMOS LSI transistors. The difference between them is the input Q. The choice of circuit should be based on which form of Q is most readily available, Q or Q'.

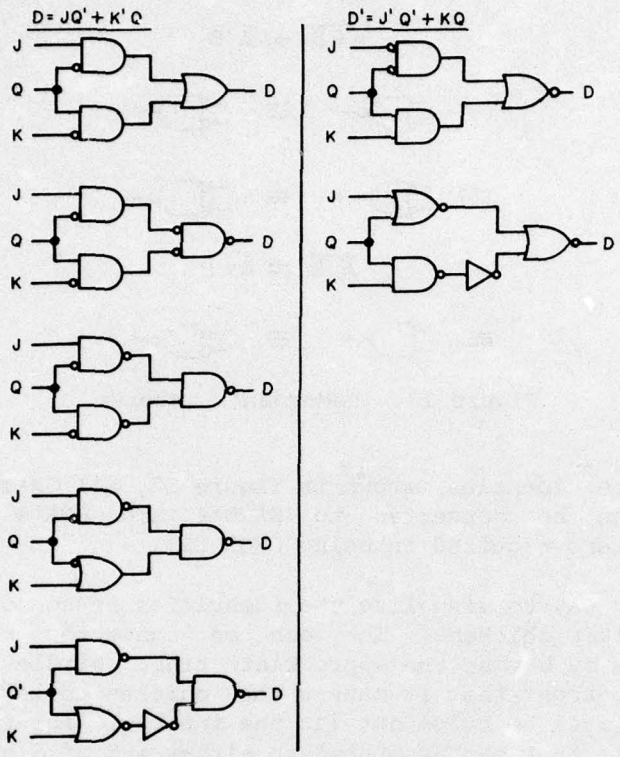


Figure 18. Evolution of J-K flip-flop input logic circuits.

6. CMOS LSI GATE ARRAY

Normally when a custom LSI is made, first the arrangement and interconnection of transistors is laid out. Provision is made for supply voltage, for input-output buffering, and for bonding pads. Then seven or more masks are generated for diffusing the dopants into the semiconductor, for creating insulating layers of oxide, and for metalizing the final surface. The layout of new masks produces problems in that the parasitic coupling between close elements can produce deleterious electrical effects, or heat production in a given area might be high, causing undesirable electrical performance and reduced useful life. When a circuit is changed, all seven or more masks must be changed, and many of the initial problems must be solved again. Only after a circuit has been produced in substantial quantities and has acquired a successful use history can it be considered as a reliable

integrated circuit. These attributes of "normal" integrated circuits lead to high initial cost, high cost of change, and a delayed and initially uncertain certification of reliability. Only when an integrated circuit is going to be used in large quantities or when space, weight, or reliability is at a premium is it practical to develop custom-integrated circuits.

Significant advances have been made in the technology reducing the initial cost and risk of custom-integrated circuits.[5,6] Computer programs have been developed to model parasitic and thermal effects. Other programs have been developed to do placing and routing. Once the placing and routing are in the computer memory, still other programs can automatically generate the masks. By using these programs, turnaround costs and risk are reduced significantly. To some extent, the product is lower in cost and initially more reliable, based on the substantial output and use history of the computer programs and associated fabrication processes (ongoing production). These advances in automation have reduced the quantities or premium required to justify customizing integrated circuits, but another technique of making custom-integrated circuits reduces them even more.

This technique uses an LSI array of transistors and required biasing and interconnecting parts. The semiconductor chip is up to 0.3 in. square and contains up to 1104 transistors. The TTL is available with up to 210 gates, CMOS with up to 276 gates (actually 1104 transistors to be connected any way), and transistor-resistor logic with up to 400 gates. The gate arrays are produced initially with metalization covering the surface. For a custom design, one mask is made that defines the metal to be etched away where it is not desired. The remaining metal forms the custom interconnecting pattern and bonding pads.

The same array chip can be used for many different circuits; therefore, only one set of diffusion masks needs to be developed, and it has to be proved out only once. The transistors are spread out uniformly, therefore reducing problems of electrical interaction and localized heating. When a circuit is designed, only one mask needs to be made, significantly reducing engineering cost and complexity. When a circuit is changed, only one mask needs to be changed. Bonding pads and packaging are also standardized for a given array chip, reducing the

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[5] *J. T. Doyle and C. A. Neugebauer, Approaches to Custom Large Scale Integration, General Electric Company, Schenectady, NY, AFAL-TR-73-66 (March 1973).*

[6] *R. O. Berg et al, Approaches to Custom LSI, Honeywell, Inc., AFAL-TR-73-16 (April 1973).*

reliability hazards normal in new fabrication processes. The advantages of array chips are that LSI's can be designed at the engineering level simply and inexpensively, leading to low initial cost, low change costs, and quick design turnaround, and that many of the failure mechanisms that lead to poor reliability in new circuits are reduced by the similarity in fabrication for all LSI's using the same basic array chip. The disadvantage of using array chips is that a truly handcrafted custom LSI could put twice the number of circuits on the same chip. This better use of space leads to lower unit costs and smaller volume. Therefore, when a large number of units is to be produced or where volume is at a high enough premium, the high initial cost of handcrafted custom LSI's is warranted. For fabrication of 10^3 units, the array is favored. For fabrication of 10^6 units, custom handcrafting is favored (J. Saultz, private communication).

The RCA TCC 051 CMOS array is shown in figure 19. The chip is 0.30 in. square and contains 1104 FET's, 48 input-output bonding pads, input-output protection circuits, buried interconnection and supply-voltage channels, and chip test devices. Nine-hundred-sixty FET's are considered internal to the chip, and the remainder are around the edge for input-output interfacing or for special impedance levels. For a given cross section of an FET as shown in figure 1, the "on" admittance level is proportional to the length of the source/drain gate. The internal FET's are about 1000 ohms when conducting, whereas the 96 FET's associated with the input-output pads are about 500 ohms. Also, 16 low-impedance FET's ($\sim$50 ohms) and 32 high-impedance FET's ($\sim$10,000 ohms) are around the periphery of the chip.

The basic internal cell of the array is shown in figure 20. It consists of two P-channel MOS FET's and two N-channel MOS FET's, each pair with a common source/drain. Supply voltages are made available near the points most likely to need them, and a few buried crossover channels are made available for crossing lines. Printed lines are made 0.0004 in. wide and are on 0.0008-in. centers as indicated by the overlay matrix of dots. This cell layout is easily used for making logic circuits as shown by the examples given in figure 21. Because the transistors come in pairs (with a common source/drain), a single transmission gate is not easily made by itself without rendering a complementary pair of transistors (one P-channel and one N-channel) useless. The basic cell in this array provides two transmission gates in an SPDT switch arrangement. Fortunately, transmission gates are used mostly in pairs as in figures 9 to 12.

When speed or large fan out is required, the resistance and capacitance of interconnecting lines and crossover channel must be taken into account.

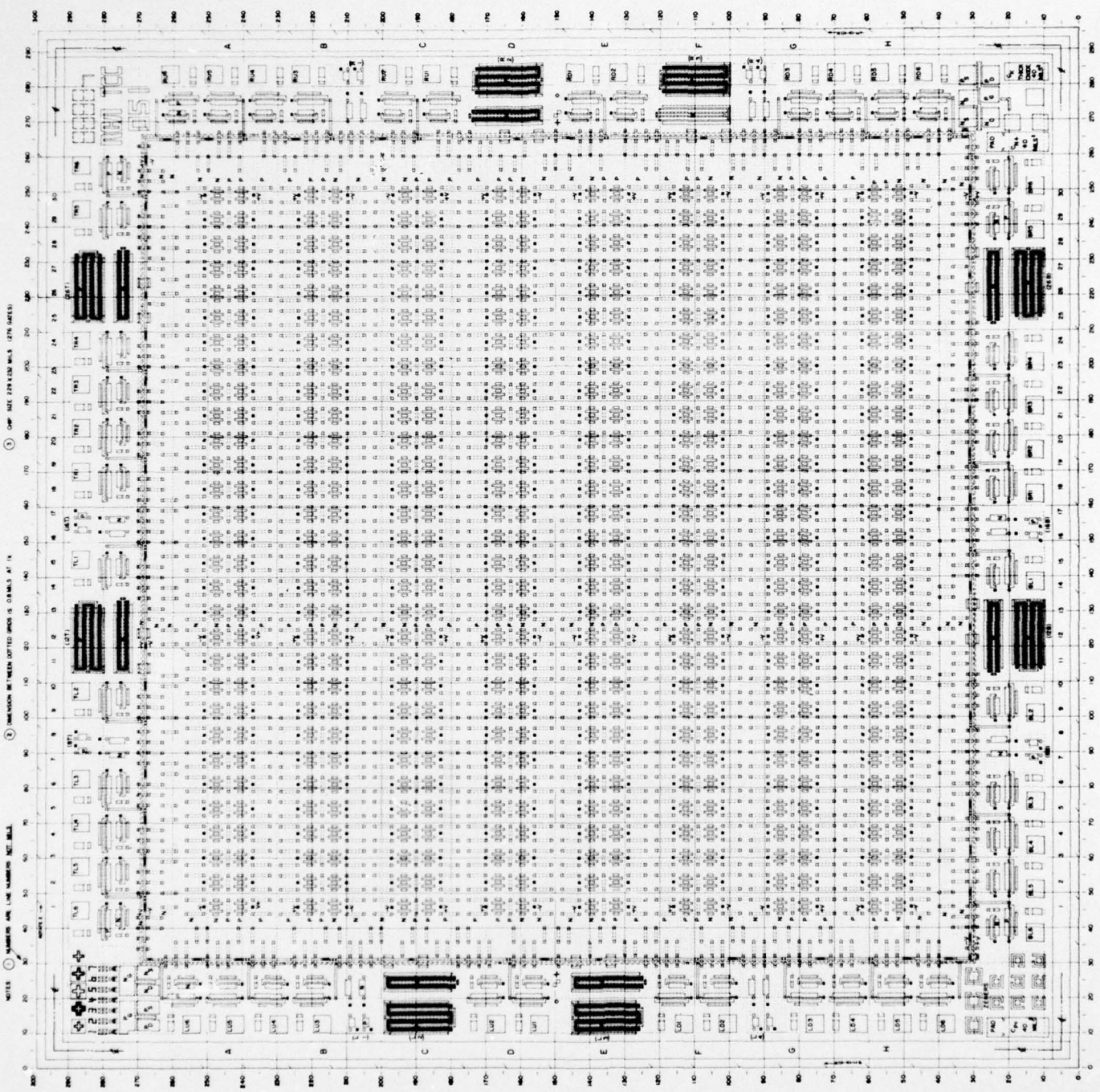

Figure 19. TCC 051 CMOS universal array chip layout.

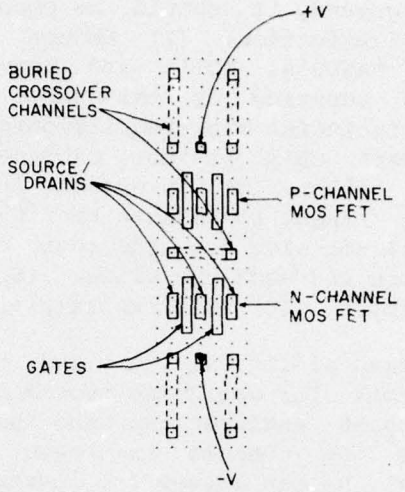

Figure 20. RCA CMOS cell.

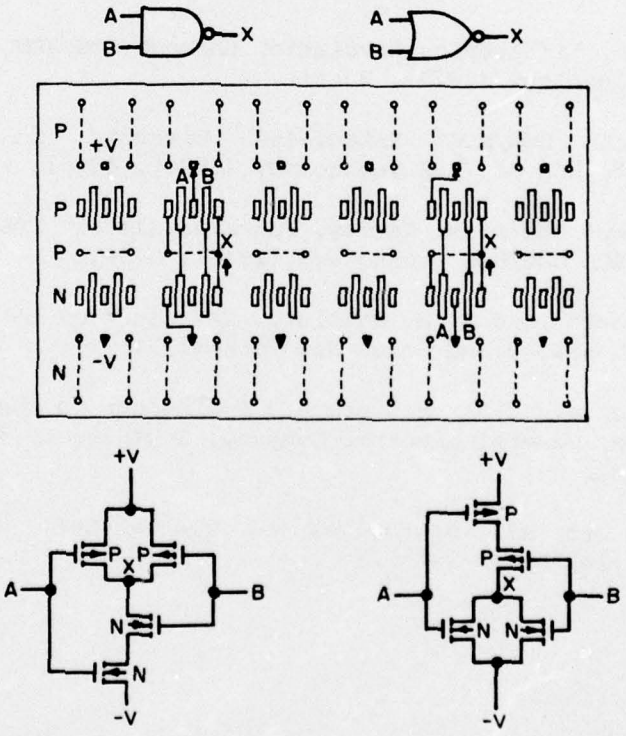

Figure 21. Two-input NAND and NOR gates.

With the above background, it should be possible to begin the CMOS LSI array design and fabrication: (1) Reduce the entire logic to diagram using NOR's, NANDS's, NOT's and transmission gates. (2) Partition the circuit counting up the number of input-output pads required for each chip including bias requirements, to be sure that the maximum number for each chip is not exceeded, and leaving about 20 percent of unused cells. (3) Lay out the chips, avoiding long or "heavy" interconnecting lines, to be sure that the series resistance or loading capacitance will not slow down the logic too much. (4) Have the mask made. (5) Expose and etch the slice. (6) Cut up the slice into chips. (7) Mount the chips. (8) Test the sample.

This basic description of digital logic and the CMOS array provide the basic building block for designing custom digital LSI's, using an array of gates. A design engineer can make the initial layout of the circuit. He can assess how changes in logic will affect the custom layout. And, in general, he can assess the degree of circuit complexity that can be accommodated by custom digital LSI's.

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(6) R. O. Berg et al, Approaches to Custom LSI, Honeywell, Inc., AFAL-TR-73-16 (April 1973).

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