

AD-A033 195

NETWORK ANALYSIS CORP GLEN COVE N Y
MODEL FOR CONCENTRATOR SIMULATION. (U)
FEB 75 P MCGREGOR
WM-FMSO-04

F/G 9/2

N00104-75-C-6588

NL

UNCLASSIFIED

1 of 1
ADA033195



END

DATE
FILMED
2 - 77

nac

NETWORK ANALYSIS CORPORATION

Beechwood, Old Tappan Road, Glen Cove, N. Y. 11542 / 516 671-9580

①

ADA 033195

⑫ 17p.

⑪ 26 February 26, 1975

⑨ 14 WM - WORKING MEMORANDUM FMSO-04

TO: George/Mountz, Paul Lujanac, FMSO

FROM: ⑩ Pat/McGregor, NAC

SUBJECT: Model for Concentrator Simulation, ⑥

DDC RECORDED
DEC 8 1976
A

ABSTRACT

This memorandum describes the basic model planned for use in the simulation experiments of the FMSO concentrator. As soon as this model is validated by FMSO personnel, final runs of the simulation program can be made.

⑮ 100104-75-C-6588

DISTRIBUTION STATEMENT A
Approved for public release;
Distribution Unlimited

389 161

mt

1. INTRODUCTION

The purpose of this memorandum is to describe the model planned for use in the simulation experiments of the FMSO concentrator. This description should be validated by FMSO personnel before the final runs of the simulation program in order to ensure the most useful and accurate results from the simulation experiments. The model is based on the functional description of the concentrator provided in the January 10, 1975 report of ADR to FMSO and numerous informal conversations with FMSO personnel.

ACCESSION NO.	
DATE	Write Section <input checked="" type="checkbox"/>
	Draft Section <input type="checkbox"/>
BY	<i>Little on Feb</i>
DISTRIBUTION/AVAILABILITY CODES	
Dist.	AVAIL. STATE/ SPECIAL
<i>A</i>	

2. CONFIGURATION

The main elements composing the concentrator configuration are shown in Figure 1. The concentrator has a planned initial capacity of interfacing 31 user terminals to three Host computers. Four user terminals will operate at 300 baud and twenty-seven at 110 baud. The hardware of the concentrator can be physically expanded to connect 128 terminal lines. However, it is not clear what the capacity of the system is in terms of satisfactorily supporting the activity of the terminal. To appraise this capacity, a simulation effort is currently underway. As part of this effort, it is first necessary to identify the timing characteristics of the system. This section briefly characterizes the major system components of the planned concentrator configuration.

2.1 CPU

The basic CPU is a Nova 800 Jumbo with 32K core with 800 ns basic cycle time. The system software is currently anticipated to be ROS (Real-Time Operating System). A console teletype is the primary means for operator control.

2.2 Low Speed Line Interface

The low speed lines will be interfaced through 4063 multiplexer units. This unit can be equipped to handle 64 asynchronous full duplex (or half duplex) facilities as a single I/O device (although occupying four I/O slots). The 4063 operates under program control in a character transfer, character buffered mode. Since both receiver and transmitter portions of a channel are character buffered, the program has an entire character time in which to retrieve a character before data can be lost or to send a character and keep the transmitter operating at maximum rate. The channels are anticipated to be connected to Bell 820E DAS through an EIA Standard RS-232B type interface for model 33 teletype access. Based on these

basic hardware facilities, the following timing and operating characteristics are estimated:

- Line servicing on an interrupt basis with a response time of less than 100 milliseconds required.
- Fielding of character interrupt requires 50 microseconds of processing time.

2.3 High Speed Line Interface

The Host processors will be connected to the concentrator over three synchronous 4800 bps channels, one to each Host. The channels will be formed of full duplex, four wire facilities using Bell modems (208 type most likely). Interface with the Nova will be through the 4015 (4021 if parity) synchronous communications controller. The controller is functionally divided into independent transmitter and receiver sections. Both sections operate with full word transfers, through hardware access of memory requiring less than one-half bit time delay for channel availability. Thus, software activity is required for initialization of a channel, but not for emptying (or filling) of a buffer being transferred. The transfer of a word using the standard data channel procedure takes a slightly extended instruction cycle of the machines capacity. Based on these hardware facilities, the following timing and operating characteristics are estimated:

- Line servicing requires 500 ns per character (1000 ns per word transfer).
- To initialize a line for buffer transfer takes 100 microseconds.

2.4 Disk

For protection against overload and for failure recovery reasons a disk is provided. The disk controller is a 4046 and the disk itself is a Wang moving head disk (F1221). The 4046 controller can handle up to four drives, although the initial configuration will have only one. The system stores data in blocks of 256 words, with transfers at the rate of one word every 11.1 microseconds. Transfers are on a sector basis (256 words), and the control can process up to sixteen consecutive sectors at a time within a single cylinder.

The maximum time required to move the heads from one cylinder to the next is 15 milliseconds, and at most 135 milliseconds are required for motion from one extremity to the other; average random positioning time is, therefore, at most 70 milliseconds. A command that moves the heads takes about 50 microseconds of control time and the program must wait at least this time before giving any other disk instruction.

Search time for a random data block, once the head positioning is complete, is 40.5 milliseconds maximum, 20.5 milliseconds average. Although the time to traverse one complete sector is 3.33 milliseconds, traversing the data block within a sector takes only 2.84 milliseconds.

The disk is not intended to play a role in the system operation except during emergency conditions, and consequently, will not be given further consideration in this discussion.

3. TRANSACTION LIFE CYCLE

The basic operation of the system is described below in terms of the life cycle of a transaction.

3.1 Life Cycle of Transactions

- Operator types ↑ to indicate transaction initiation.
- The Nova is interrupted, allocates input buffer space, initializes line control block, and sets date and time in output buffer for return to operator, e.g.,

73059/0900

- Operator inputs message,

PTBA/

- Input rate at approximate 1 CPS.
- The program type characters ("PTBA") are then examined to verify acceptability of the machine and program request. Upon verification, the Nova responds (CR) (LF)

- The operator inputs message,

MAP 96131 (CR) (LF)
002423407 ! n ! RFI (HERE IS)

- The HERE IS is a function key that signals the Nova "end of message." Acceptance of the message by the Nova is indicated by return of a CR LF to the operator. The message is then placed on the appropriate queue for output to a Host.
- If an output is available for the terminal, its transmission is initiated immediately after the CR LF response of the Nova. If not, output is available and the operator initiates another ↑, then a new output must wait until completion of the input with a HERE IS.
- A Host sends a general poll to the Nova. The "input" message queue (queue of messages that were input from a terminal) is examined, and if a message is present, its transmission is initiated. After receipt of the message from the Nova, the Host then places another general poll message in its output queue with non-preemptive priority over other output messages.
- The processing of the input message by the Host results in an output message of length averaging approximately 600 characters to be sent to the Nova.
- The Host segments the output message into blocks. Each block can be at most 160 characters in length. The Host will use as few blocks as possible for message segmentation.

- The Nova will use double buffering (each buffer is 160 characters) in returning output messages to the terminals. The Host will transmit a new block only when one or both of the buffers at the Nova are available.

- When the Nova receives an output block from the Host, the block is buffered until the line to the terminal is available for transmission. The line is considered available immediately after the end of transmission of another output block, the end of an input transmission from the terminal, or if the line is not engaged in any activity.

- The cycle is complete after the last output block is transmitted to the terminal.

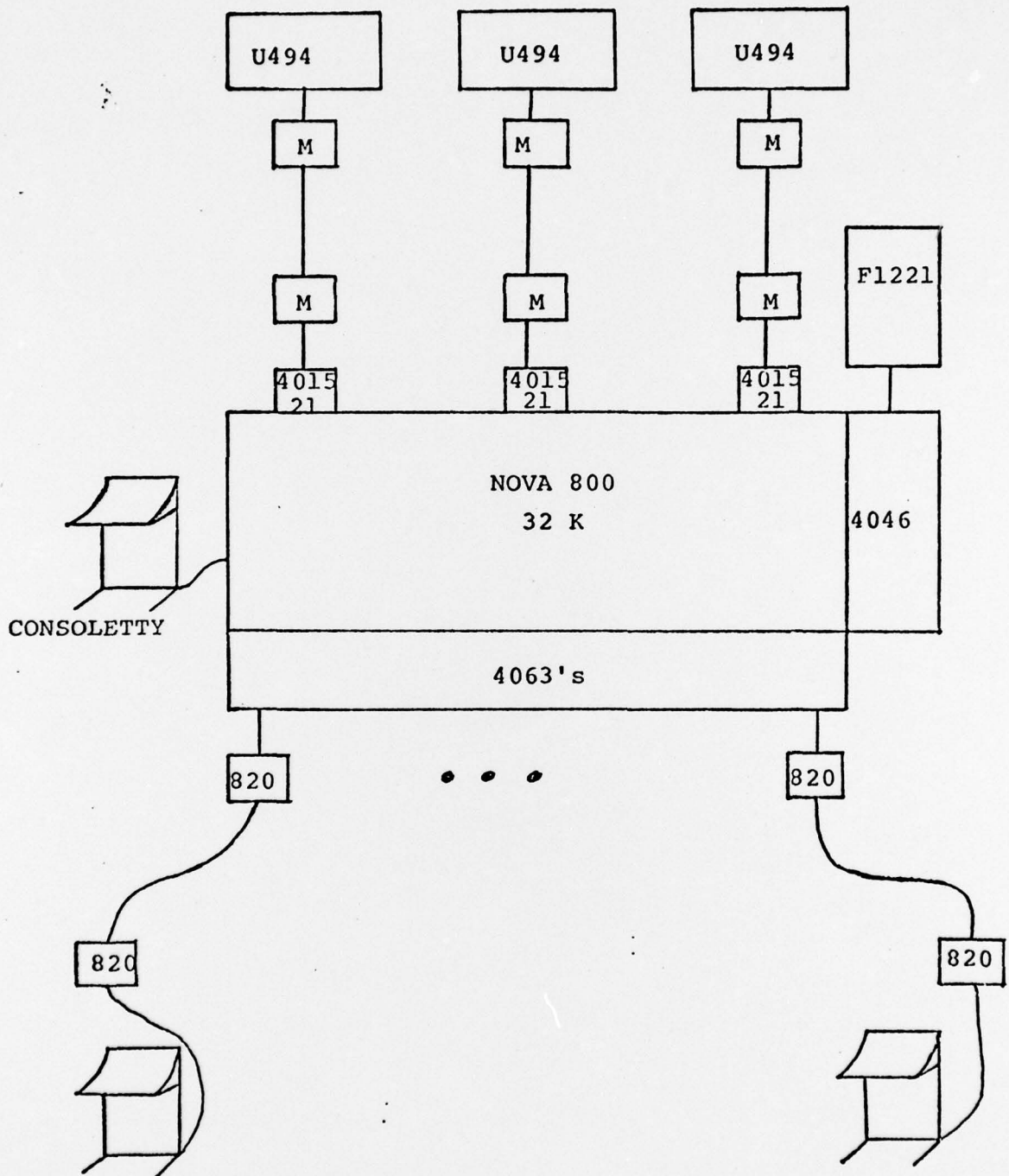


FIGURE 1: FMSO CONCENTRATOR CONFIGURATION

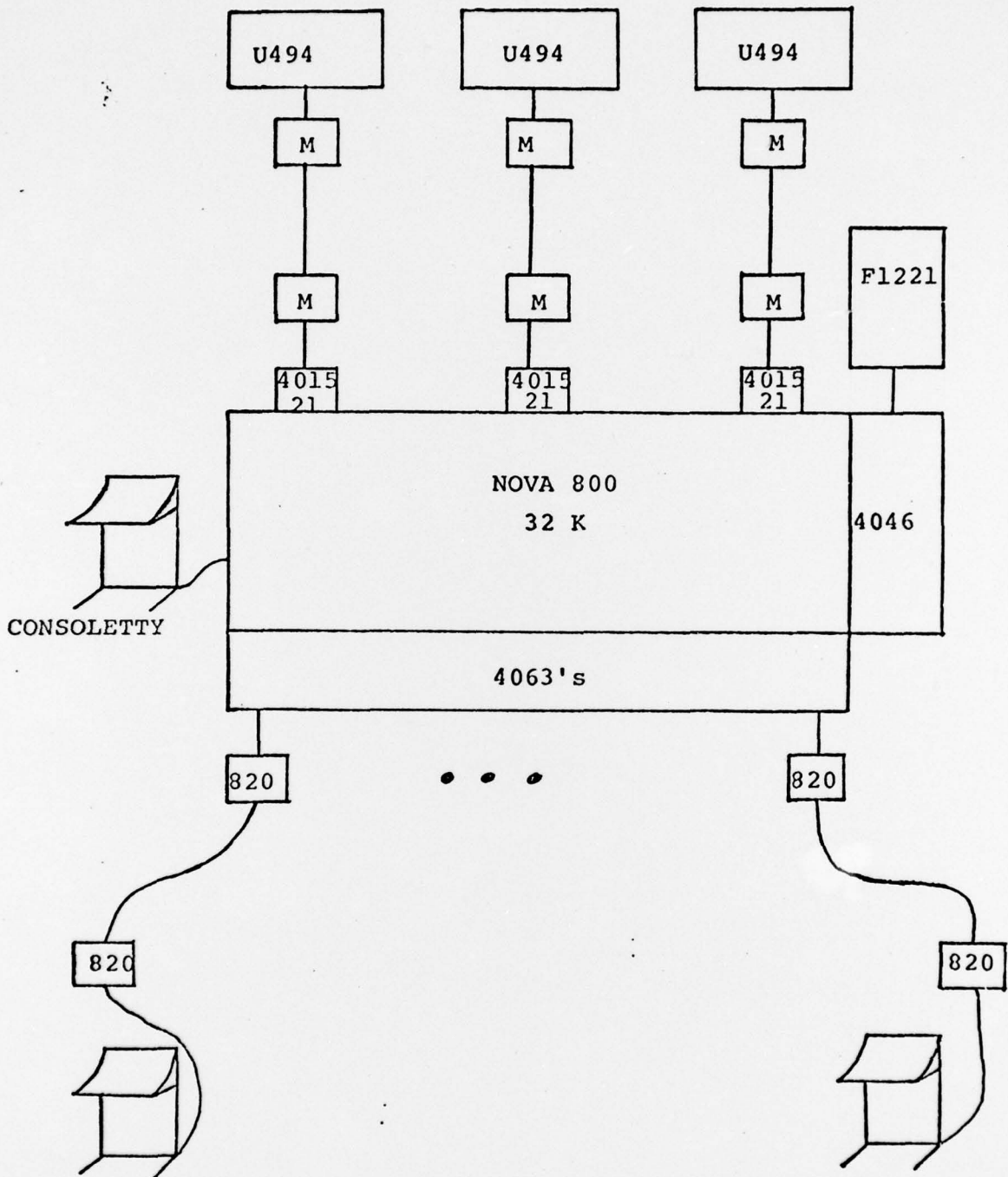


FIGURE 1: FMSO CONCENTRATOR CONFIGURATION

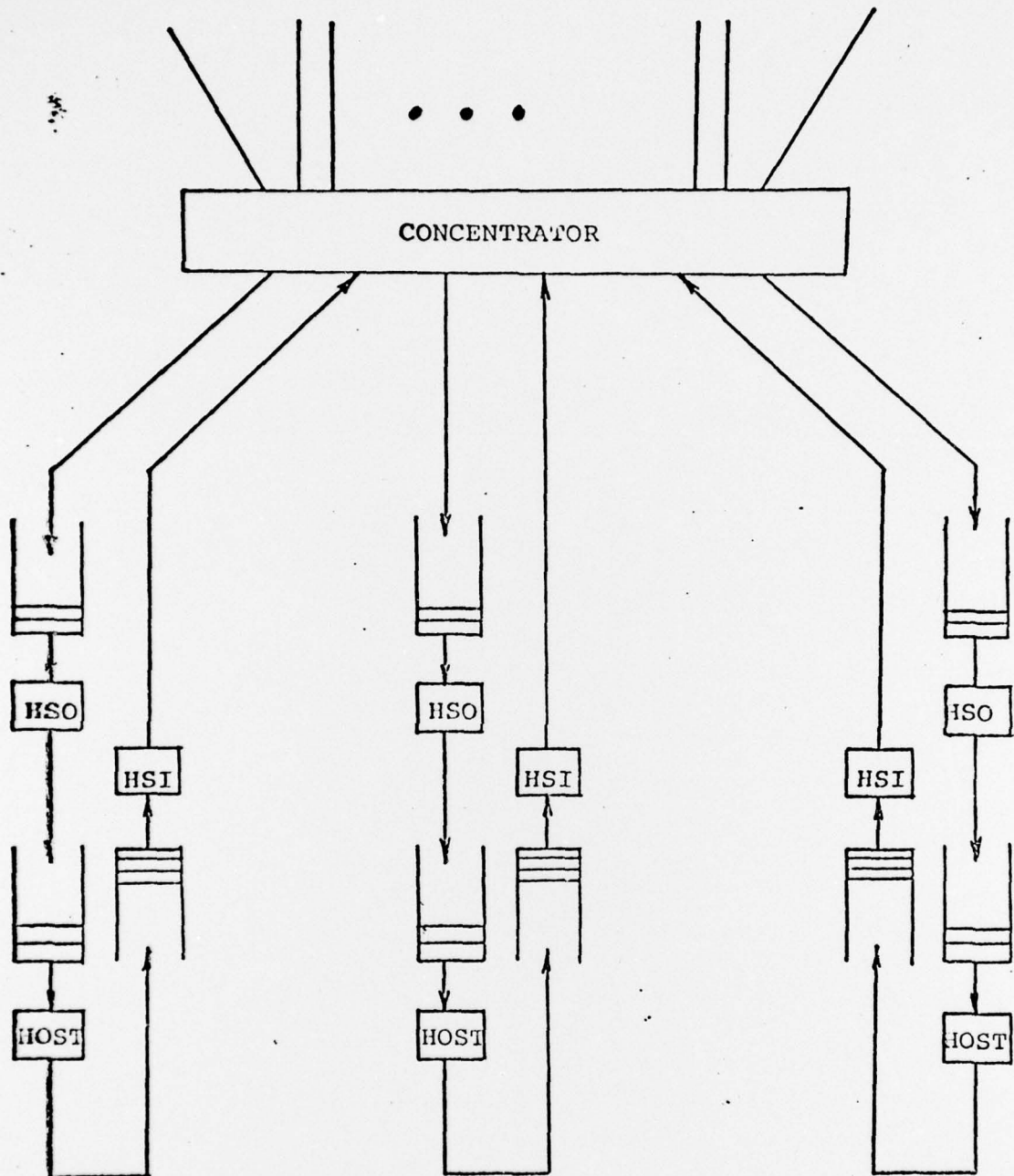


FIGURE 2: SIMPLIFIED QUEUEING MODEL FOR FMSO CONCENTRATOR

4. TRAFFIC

The system function is data base access and management, and consequently the traffic is of a transaction nature. Two fundamental types of transactions are identified: inquiries and upquiries. Both have short input messages averaging 22 characters in length, entered via model 33 teletype over an average period of 30 seconds. Inquiries result in an output averaging approximately 600 characters in length, with a maximum that may exceed 5000 characters (although infrequently). Upquiries result in the echoing of input information but no substantial output by the Host. The statistical division between inquiries and upquiries is not known, but estimated to be heavily weighted in favor of the inquiries. Outputs from the Hosts are delivered by the Nova as soon as the appropriate terminal line is available, that is, they cannot interrupt an input that is in progress.

Based on these considerations, the following traffic model will be used.

4.1 Transaction Types

Two transaction types are defined.

- Type 1 - inquiry
- Type 2 - upquiry

The traffic is modeled as consisting of 90% Type 1 transactions and 10% Type 2 transactions.

4.2 Input Messages

Input messages for both transaction types are assumed to have a biased exponential distribution with a mean of 22 characters and a constant factor of 19 characters. The input messages are assumed to be entered at a keying rate of one character per second.

4.3 Input Message Arrival Rate

The basic throughput of the system will be expressed in the number of transactions per peak hour. The interarrival time of messages at a terminal to be input to the system is assumed to be random with an exponential distribution having a mean determined by the throughput and the assumption of equal load at all terminals.

4.4 Output Messages

Output messages resulting from Type 1 transactions are modeled as having a random length characterized by uniform distribution over the range 210 to 1200 characters. Output messages resulting from Type 2 transactions are modeled as being the same length as the input message.

4.2 Input Messages

Input messages for both transaction types are assumed to have a biased exponential distribution with a mean of 22 characters and a constant factor of 19 characters. The input messages are assumed to be entered at a keying rate of one character per second.

4.3 Input Message Arrival Rate

The basic throughput of the system will be expressed in the number of transactions per peak hour. The interarrival time of messages at a terminal to be input to the system is assumed to be random with an exponential distribution having a mean determined by the throughput and the assumption of equal load at all terminals.

4.4 Output Messages

Output messages resulting from Type 1 transactions are modeled as having a random length characterized by uniform distribution over the range 210 to 1200 characters. Output messages resulting from Type 2 transactions are modeled as being the same length as the input message.

- Output messages are segmented into blocks. Each block can be at most 160 characters in length. The Host will use as few blocks as possible for message segmentation.

- Output message blocks can be sent to the Nova only when buffers are available. Within this constraint, they are sent according to a FIFO discipline.

- Output message blocks are addressed to a particular low speed line. (Each low speed line has a per- ^{? permanent} manent allocation of two buffers.) The absence of buffer space for a particular line does not affect the possible transmission of output blocks for other lines. *vs.*

- Output blocks can be transmitted at the same time messages are being sent on the input side to the Host, i.e., a full duplex mode of operation. This means an output block can commence transmission immediately after a polling inquiry has been transmitted.

5.3 Host Processing Time

The Host processing time, for both types of transactions, is modeled as random with a uniform distribution having a (mean of one second and a range of .5 seconds to 1.5 seconds.) *two low*

5.4 Nova Processing Time

The processing requirements for the Nova are described below.

- Fielding of character interrupts on a low speed line requires 50 microseconds.

- Processing of North-Arrow interrupts and Date and Time response requires 500 microseconds.
- Input message processing (buffer allocation, routing, validation, etc.) requires one millisecond per message.
- High speed line servicing requires 500 nanoseconds per character.
- Output message processing (buffer set up, control blocks, etc.) requires one millisecond per block.
- Processing of polling inquiry requires 500 microseconds.

6. CONCLUSION

In this memorandum, we have described the model planned for use in the simulation study of the FMSO contract. This model needs to be validated by FMSO personnel before final simulation experiments can be conducted.


NB