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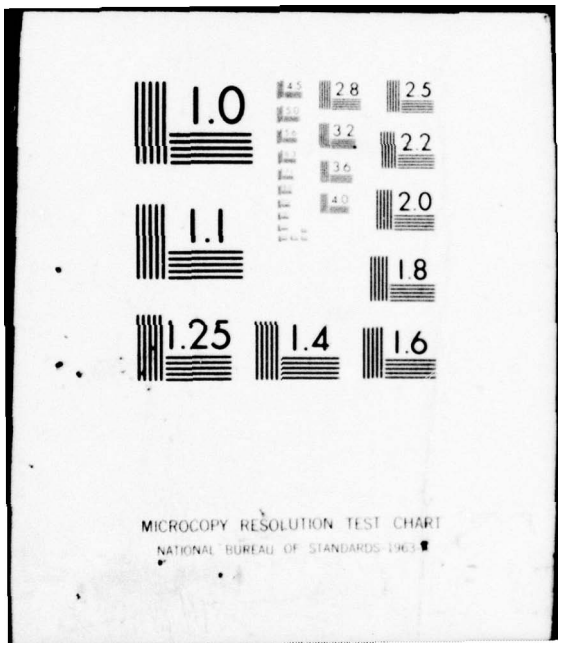
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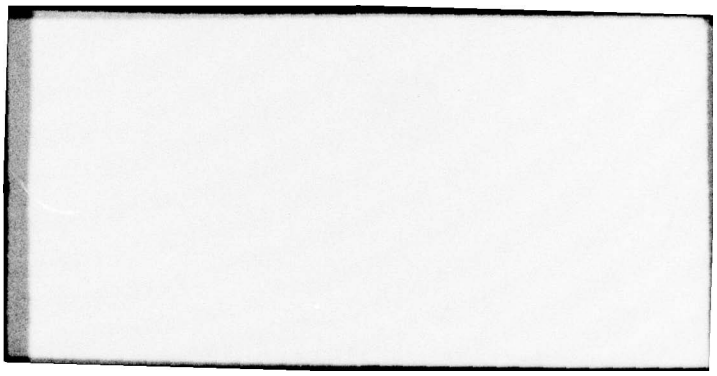

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PDP-11/05 TO ELECTRON BEAM INTENSITY MODULATION UNIT INTERFACE

THESIS

Presented to the Faculty of the School of Engineering

of the Air Force Institute of Technology

Air University

in Partial Fulfillment of the

Requirements for the Degree of

Master of Science

by

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Graduate Electrical Engineering

December 1976

Preface

This investigation is an attempt to provide the first part of a digital interface system which will ultimately provide real time intensity modulation of a scanning electron beam under computer program control. The interface will link a standard Digital Electronic Corporation (DEC) PDP-11/05 minicomputer with a two dimensional optical data modulator as described in Air Force Avionics Laboratory (AFAL) Technical Report AFAL-TR-75-165. Both pieces of AD25 450 equipment are located in the Electronics Technology Division of AFAL at Wright Patterson AFB, Ohio.

I wish to express my appreciation for the support of my thesis sponsor, Mr. Dave Flannery AFAL/DHO and the particular guidance that he offered in defining the interface requirements of the optical data modulator. I would also like to thank the members of my thesis committee: Dr. Gary B. Lamont, Capt Peter E. Miller, and Lt S. R. Robinson for their suggestions throughout the design development of this interface. The guidance and interest of my thesis advisor, Capt Miller, is especially appreciated by the author.

A special expression of appreciation goes to my wife, Marjorie, whose help and support have made this thesis possible.

Contents

List of Figures

List of Tables

Abstract

The result of this investigation is a design for an interface system which can be used to interface a Digital Electronic Corporation PDP-11/05 minicomputer with electron beam control electronics (EBCE). The EBCE is part of a deformable thermoplastic phase plate brassboard used for optical phase modulation in the Air Force Avionics Laboratory (AFAL/DHO).

The interface is a modular design made up of a unibus interface, buffer, input control, output control, master control, and a digital to analog (D/A) converter. The buffer module uses two first-in-first-out (FIFO) buffers to alternately accept data from the PDP-11 and send data to the EBCE via the D/A converter. The 16 bit word of the PDP-11 is multiplexed into 8 bit data words for interface manipulation, since 8 bits offer adequate resolution for the EBCE.

The interface is designed to allow writing of a 100 x 100 element matrix on the phase plate. This requires a 1.45 element/sec modulation rate of the analog signal sent to the EBCE. The use of a dual FIFO system, a multiplexed computer word, and a very fast D/A converter make this modulation rate possible.

I. Introduction

The purpose of this investigation is to develop an interface design that will provide the data and control link between a minicomputer and a specialized optical modulation device. The interface will provide the first stage in the development of a real time adaptive optic control system and will be used to demonstrate the feasibility of electron beam intensity modulation under computer control.

Background

Independent work has been accomplished by the Air Force Avionics Laboratory (AFAL/DHO) in developing a deformable thermoplastic phase plate and by Lt S. R. Robinson of the Air Force Institute of Technology (AFIT/EN) in an area which requires real time optical phase modulation. Further work which merges these separate efforts has led to a user requirement for a computer controller to direct phase modulation information to the deformable phase plate.

The user wishes to employ a small processing system to supply a modulation signal to electron beam control electronics (EBCE) which in turn will apply intensity modulation to an electron beam. The electron beam will scan the phase plate which will physically deform under the influence of the deposited charges. A laser beam passing through the phase plate will then become phase modulated. The overall system diagram is shown in figure 1.

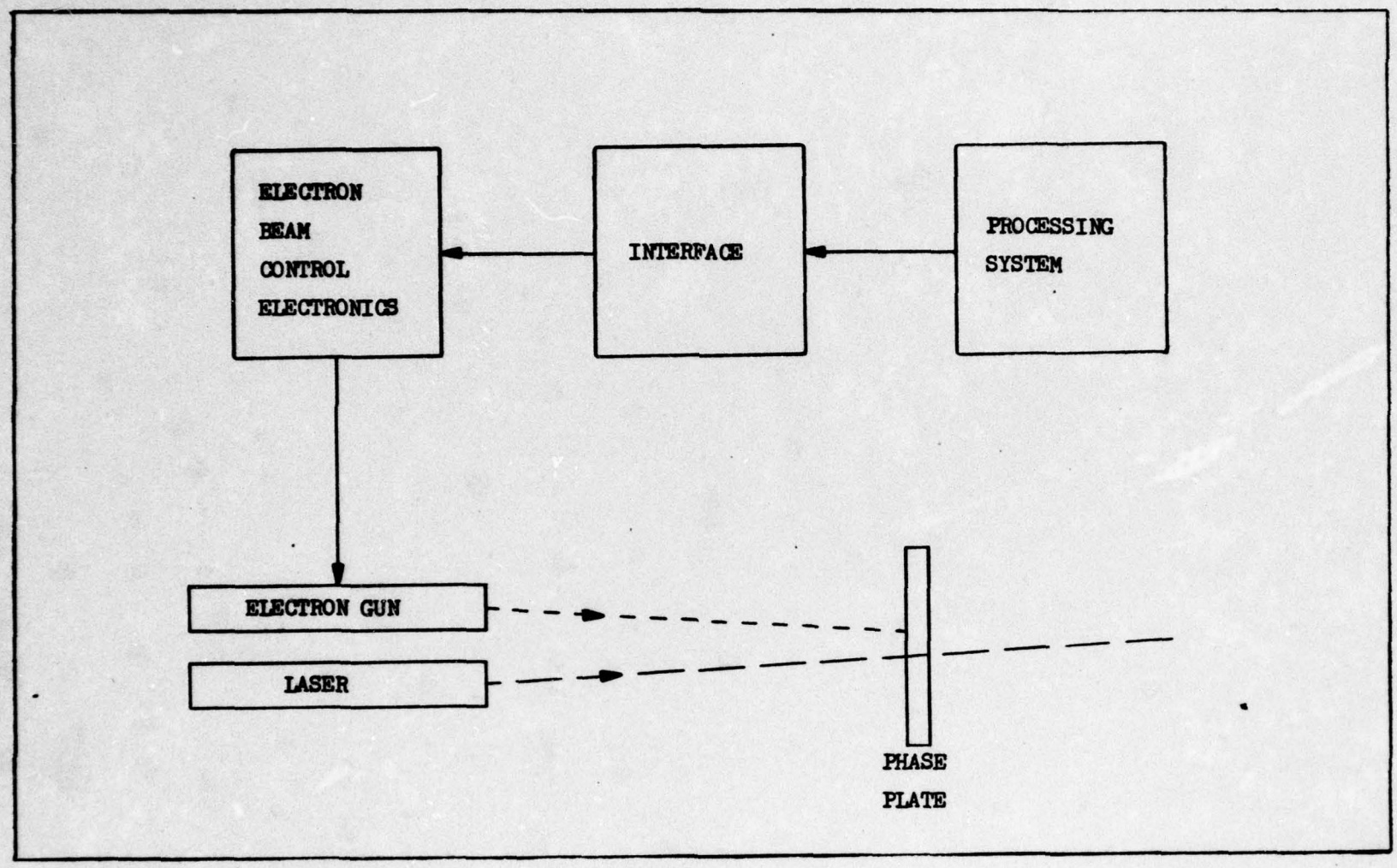

Figure 1. System Diagram

It is eventually desired for the electron beam to control a 10^6 element square array (1000 line scan x 1000 elements per line), which is the current maximum capability of the phase plate, with each array position receiving an amount of charge determined by program control. The fastest foreseeable operating speed desired is for the electron beam to scan the entire array once each millisecond. This would result in a beam modulation rate of 1×10^9 elements per second.

The EBCE package is available in AFAL/DHO. Also available for use in this project are a Digital Electronic Corporation (DEC) PDP-11/05 minicomputer with a floppy disk mass storage unit and a DEC A619 10-bit digital-to-analog (D/A) converter. In addition, software expertise is available and current AFAL personnel familiarity with PDP-11 software indicates that detailed PDP-11 programming can advantageously be accomplished by the user. Therefore, PDP-11 software should not be a major effort of this study.

Problem Statement

The desired beam modulation rate of 10^9 elements/sec provides a very formidable goal for this study, possibly surpassing state of the art computer speed technology. Fortunately, these are long range goals with an immediate design requirement being the fastest feasible rate of beam modulation. In order to benefit from the phase plate method of optical modulation over other current modulation methods, the control should operate on an array (one frame) of at least 100 elements within the frame write rate of the EBCE, which is one frame in .069 sec. Frame refresh is limited by the thermoplastic composition to "single shot" operation with repetition times measured in seconds. Due to

this slow repetition limit, for purposes of this study, frame refresh time will not be considered a factor.

These basic requirements can now be used to accurately define the design goals.

1. Unprocessed control information in digital form will be supplied to the PDP-11, processed through a user generated program, stored in memory if necessary, and presented to the EBCE through the interface and D/A converter. The interface must communicate with the PDP-11 and the EBCE and synchronize data transfer according to the timing requirements of each.

2. The interface should be designed to accept data at the maximum possible transfer rate from the PDP-11. The interface should be capable of applying this data to the electron beam at a rate which matches as nearly as possible the PDP-11 transfer rate. However, to provide a user option in modulation speed, slower rates should also be available.

3. The data must be presented to the EBCE in synchronization with the electron beam horizontal and vertical sweep positions. This will allow complete predictability of data position upon the phase plate for all data points.

4. The interface should allow user flexibility in choice of array configuration on the phase plate.

5. The interface must provide for a "single shot" writing of the phase plate. This will be the normal operating mode and will consist of the interface controlling the writing of one frame. The write sequence will be initiated by the user manually operating the single frame push button on the EBCE panel.

Specifications and Constraints

EBCE and Phase Plate Parameters. The following specific parameters have been provided as requirements which will provide sufficient data and machine flexibility to demonstrate the "computer control" concept of beam modulation:

Frame time - .069 sec

Sweeps per frame - 500 line sweeps for one frame sweep

Beam sweep speed - 11.5 to 254 μsec/inch

Aperture (frame) size - appx 1 inch square

Video (modulation) input - 1 to 700 mv

Line flyback time - 13 μsec

Line sweep unblank period - center 90% of sweep

Data Word Length. The data word length must be 5 bits minimum in order to provide the desired user accuracy after digital to analog conversion. This will provide the necessary resolution of laser modulation due to phase plate deformation.

Cost. The hardware cost target is $500 - $1000 (an AFAL/DHO constraint). The $500 should be used as the design to cost criteria in order to allow for reasonable cost and design growth.

Scope

Since the phase plate brassboard is a one of a kind system, the interface design of this study will have a use that is limited to the particular PDP-11/EBCE system located at AFAL/DHO. Therefore, there has been no attempt to design a general interface which would have application to other systems. This allows simplicity of design and optimization of the PDP-11/EBCE data transfer rate.

Software is addressed only as necessary to allow understanding of computer/interface communication and data flow. However, an applicable programming technique will be illustrated.

Approach

This design employs the top-down approach. Design decisions have been made at discrete levels of increasing detail. These levels correspond to Chapters II and III of this study, with the overall design based on the problem constraints and specifications set forth in this chapter.

Additionally, the design provides a structured system which is divided into functional modules. An attempt was made to generate these modules in such a manner that their function and interaction with the entire system are easily understandable. This is accomplished by designing a system in which the functional modules logically relate to a particular section of the overall block diagram.

Conventions

The interface is designed as a TTL system and standard TTl conventions are used throughout. This is in difference to the negative logic of the PDP-11 unibus which considers 0 VDC as a logical 1 and 5 VDC as a logical 0. In this interface system, 5 VDC is a logical 1 and 0 VDC is a logical 0 (positive logic).

All timing diagrams are depicted with "idealized" signals. The instantaneous rise times shown indicate the switching levels of finite rise time "real" signals.

Information paths are depicted with directional arrows in all block and module diagrams. Control and status paths are indicated

with single line arrows. Double line or triple line arrows are used for data words or computer words respectively, while cross hatched double line arrows indicate analog information.

Assumptions

In order to limit the scope of this study, it was necessary to make a number of basic assumptions. These assumptions are included here as an aid to the understanding of the overall design problem and as rational for many decisions made throughout this study.

1. The PDP-11 is a useful machine for data manipulation and interface mating in this study. It's use may dictate an overall system which is less than optimal for the control process required, but it can be used as a cost effective means of verifying the program controlled modulation concept.

2. PDP-11 programming expertise is available as a user resource.

3. Due to the unique nature of the optical modulator, the interface system of this study has a limited application and therefore warrants design as a special purpose item.

4. The fixed operating speed of the PDP-11 can be balanced through the interface such that the fixed timing requirements of the EBCE can be met.

5. The reader is familiar with general computer interfacing requirements and with basic logic design procedures.

Thesis Organization

Chapter II of this study presents the general system organization. The chapter states the requirements of the computer, the optical modulator, and the interface. The options for meeting these

requirements are discussed and the design approach detailed. In doing this, most functional block content decisions are made and certain operating signals and parameters are identified.

Chapter III presents the hardware design of the interface functional blocks discussed in Chapter II. All units which make up the blocks are discussed and the interconnecting signals analyzed. In addition, timing and synchronization are discussed in some detail to insure that this critical element of the design is adequately understood.

The conclusions and recommendations of this study are presented in Chapter IV. It includes application notes for building on this study in an expanded system, and specific possibilities for improving this design.

A software example, timing diagrams, and parts selections are contained in the appendices. The appendices also contain wiring diagrams for the functional modules.

II. Overall System Organization

Introduction

Before any hardware design can be properly implemented, there are many higher level decisions to be made. The purpose of this chapter is to relate the specifications and requirements set forth in Chapter I to the specific hardware design to follow in Chapter III. This is accomplished by showing how the requirements relate directly to functional blocks which are implemented through hardware modules. Since the interface will tie the PDP-11 to the EBCE (see figure 1), this chapter analyzes the modulation, processor, EBCE, and interface requirements to arrive at the overall system organization. The design problems addressed are: (1) data storage, (2) data retrieval under computer control, (3) digital to analog (D/A) conversion, and (4) synchronization of the modulating signals with user supplied line scan signals from the EBCE. The simplified interface block diagram is shown in figure 2.

Modulation Requirements

The phase plate is approximately one inch square and is constructed of a material which will physically deform under the influence of deposited electron charges as shown in the cross sectional view of figure 3.

The following discussion is in reference to figure 4. The EBCE controls the electron beam such that it scans across the phase

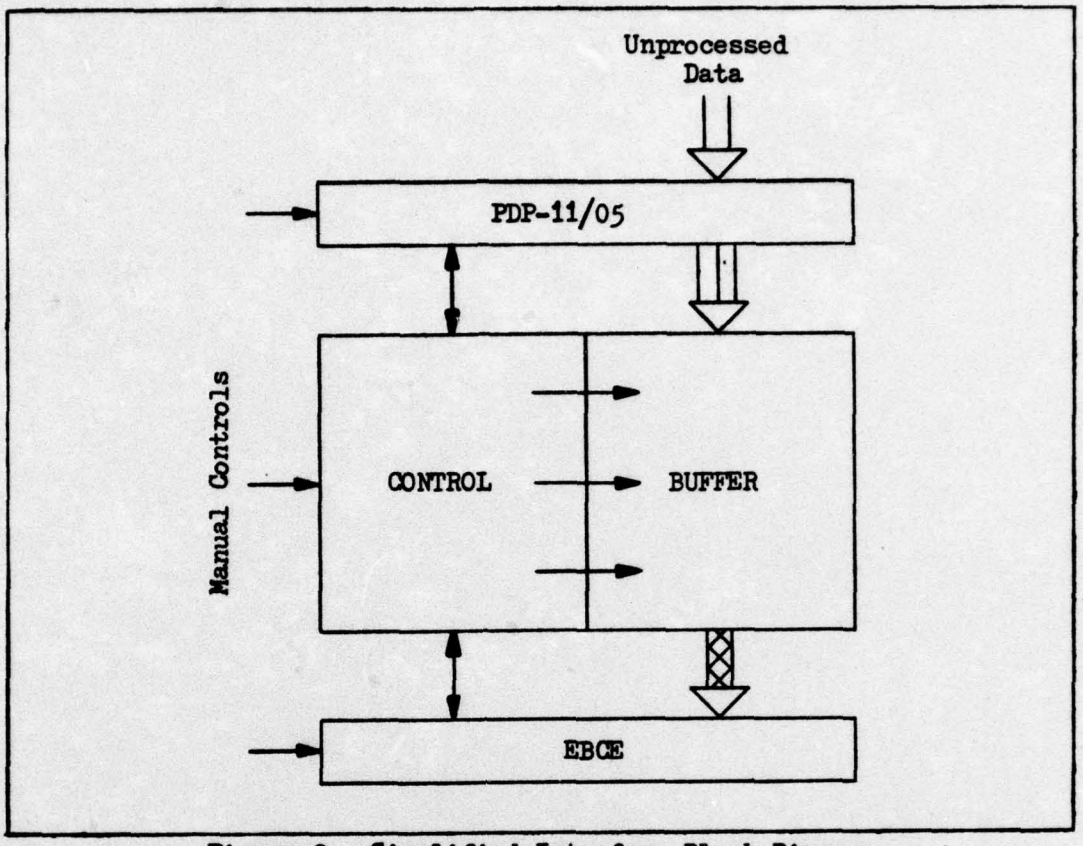

Figure 2. Simplified Interface Block Diagram

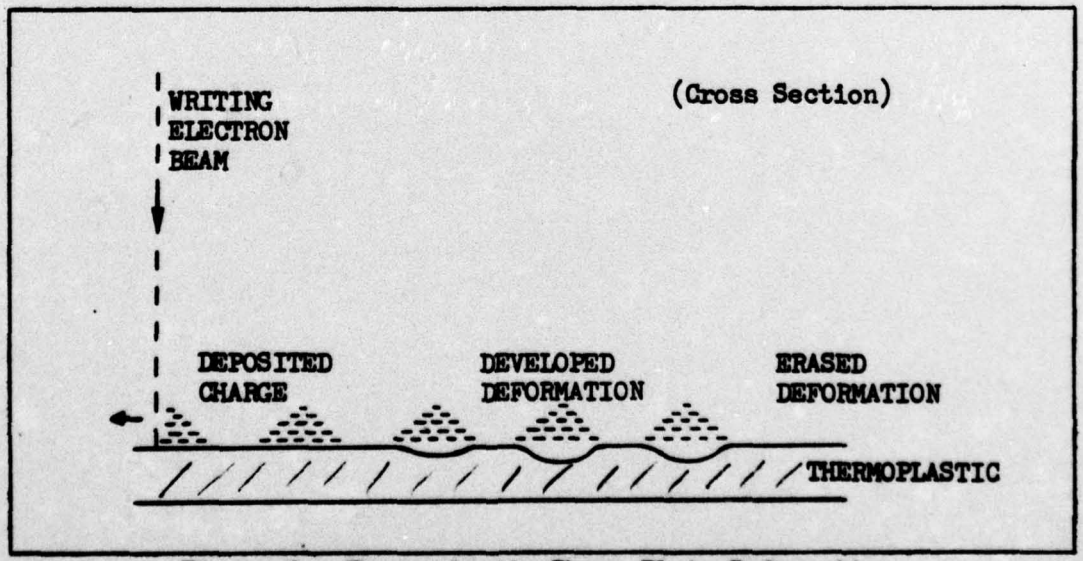

Figure 3. Thermoplastic Phase Plate Deformation

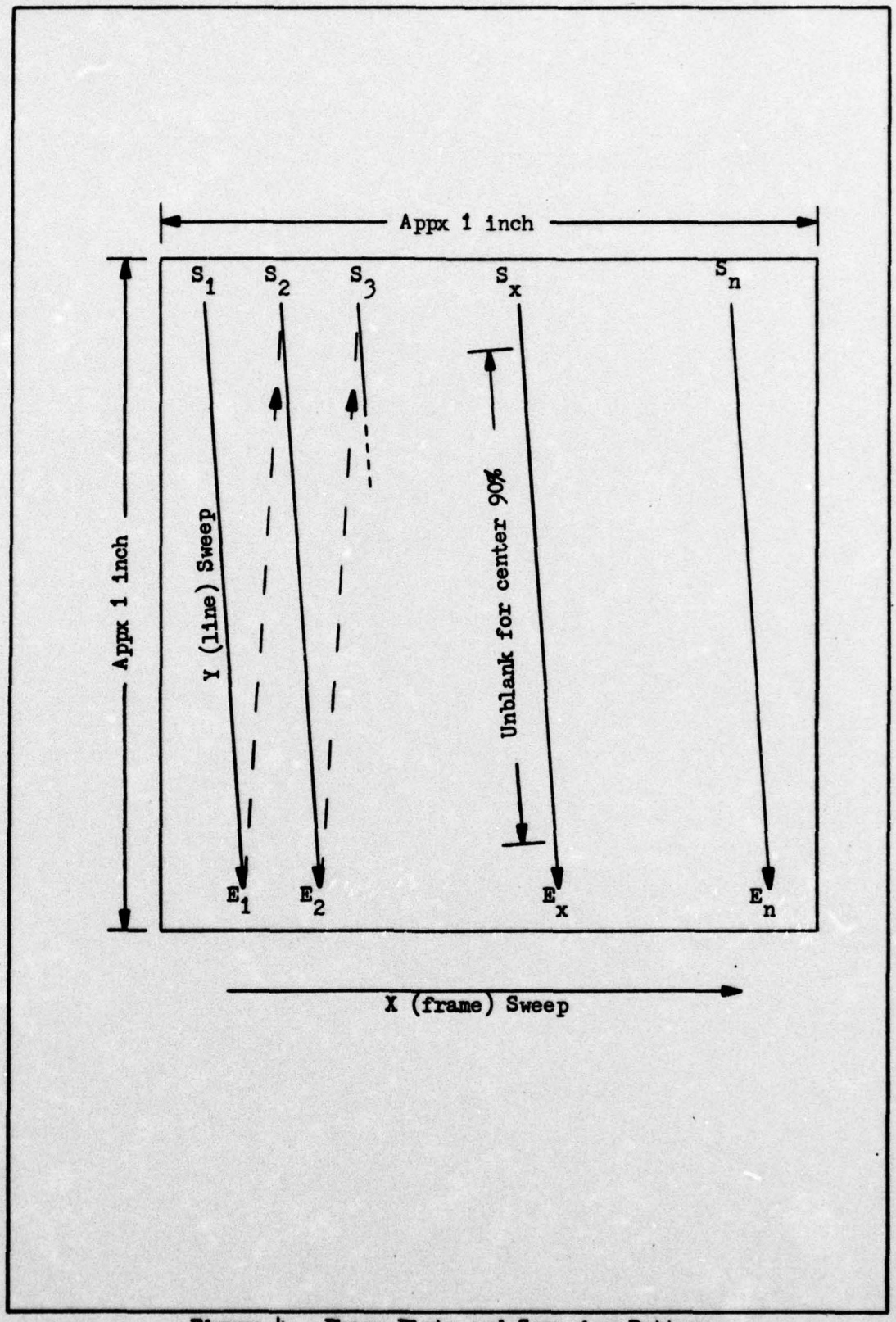

Figure 4. Phase Plate and Scanning Pattern

plate in the pattern shown, scanning from S_1 to E_1, S_2 to E_2,$\cdots S_x$ to E_x,$\cdots S_n$ to E_n where S_x are the start points and E_x are the end points of $n \leq 1000$ line scans. E_x to S_{x+1} represents the beam flyback to a new line start position and has a fixed time of 13 μsec. For this study, the long (X) sweep time (S_1 to E_n) is fixed at .069 sec and will be called the frame sweep. The short (Y) sweep time (S_x to E_x) is adjustable from 13 μsec to 254 μsec and will be called the line sweep. In order to facilitate the generation of different matrix sizes and still provide a valid feasibility study, the line sweep time is fixed at 138 μsec. This will provide 500 line sweeps during one frame sweep, i.e., 500 lines across the phase plate will be defined as one frame.

Only the center 90% of the sweep is unblanked (beam not biased "off"), therefore the unblank time is [(138 - 13) μsec] x .90 = 112.5 μsec. It is during this unblank time that the beam intensity modulation must be controlled. If the unblanked portion of each line could be divided into N discrete information elements, a N x 500 matrix would be generated. This is precisely the planned operating scheme of the phase plate, with each information element being controlled by the intensity of the modulated electron beam. The intensity information data, in analog form, is to be presented by the interface to the video input of the EBCE with the correct synchronization relationship to the sweep ramps so that a usable matrix is provided on the phase plate.

It should be noted here that if each analog data value were to be presented and held for 1.125 μsec during unblank and if each line of information were repeated five times, a square array of 100 x 100

distinct spots would be generated. A 10,000 spot matrix is two orders of magnitude better than the minimum desired; therefore, the 100 x 100 configuration will be the goal of this study. This concept of spot -- area made up of equally charged elements -- will be used for the remainder of this study.

Transfer Rate

The buffer module output speed must be great enough such that the electron beam does not proceed too far down the sweep prior to receiving a modulation signal. Making an arbitrary choice here, the beam should not cover more than 1% of its unblanked distance before receiving analog data. If half this time is to be allowed for the D/A conversion, the buffer output time should not exceed $\frac{112.5 \times .01}{2}$ μsec ≈ 550 nsec.

Processor Requirements

The PDP-11/05 to be used is a standard basic system with 16K of additional memory (24K total). The PDP-11 capabilities will of necessity impact the interface design. Since the requirements of this study can be accomplished by time dedicating the PDP-11 to this interface when it is in operation, the design will be implemented without an interrupt capability. For this study then, the PDP-11 will be fully dedicated to the interface with no concurrent software operation other than that presented in this section.

Software Algorithm Options. Prior to considering hardware or peripheral options, the available means of providing computer generated data to these items must be investigated. The two approaches considered in this study are: (1) compute and output data serially; and (2) compute and store serially, and then output data upon demand.

1. Compute and Output. The most economical and straight forward method of program beam control would be for the PDP-11 to perform each data point computation and output this information prior to proceeding to the next data point. This operation would set the overall system operating speed at the output speed of the PDP-11. However, there are two major problems with this approach.

a. The computational capability of the PDP-11/05 is slow compared to the speed desired from the overall system. For a simple algorithm (one add, one subtract, and one move) the PDP-11 would require nearly 30 μsec between outputs (assuming the move acted as an output instruction). This would only allow generation of a 3 x 500 matrix which is less than desired. It is possible that more complex algorithms could take computation times comparable to the total frame time.

b. Due to different computational algorithms and inherent instruction execution time variations in the PDP-11, the time differences between information outputs might vary from a few nanoseconds to a number of milliseconds. In order to stabilize output time variations, it would be necessary to key on the longest expected time and design the interface to pass data to the EBCE only after this time delay between each information point. This would require increased interface overhead and further extend the time between interface outputs.

For these two reasons, the compute and output approach is unacceptable.

2. Compute, Store, and Output. This approach involves performing the computational algorithms, storing the processed data in the

PDP-11 memory, and outputting the data at some later time. This approach will solve the problems of compute and output described in the previous section, but adds the additional restriction that all calculations must be performed prior to proceeding with the output portion of the program. In addition, more computer memory is required for storage. However, this is more practical than compute and store for this design, and was the method chosen for implementation. There are two different means of accomplishing the output of stored data that were considered important enough to warrant discussion here.

a. Direct memory access (DMA) is definitely the most straightforward way to move data from memory to an interface. However, the standard DEC DMA unit for the PDP-11 is not available for this study. There is a dedicated DMA module for using the existing floppy disc, but it is not available to transfer data directly from core and the retrieval speed from a floppy disk is much too slow for this application. The high purchase cost of DEC's DMA inferface kit ($850) and the design cost of a DMA module as part of the interface make the use of DMA undesirable for inclusion in this design.

b. Program controlled output (PCO) allows more flexibility in data output, but it is usually more expensive in terms of memory requirements and is definitely slower. User indications are that the 24K of memory is adequate for the computational algorithms to be used and still have at least 18K of memory remaining for data storage and data output algorithms. Analysis of the PDP-11/05 instructions and execution times indicate that a 16 bit word can be moved from core (using a MOV instruction) to a peripheral device in 9.4 μsec. There are also bit test and branching instructions which

can be used to check the status of a peripherial and, depending on the value of the status, continue in a testing loop or branch to the next program block.

Thus compute, store, and PCO does provide a software solution. In order to minimize PCO time, the data will be transferred with no parity or other error checking schemes. Since the processor to interface transmission distance is so short there is little possibility of error, lack of error checking is not seen as a problem area for this study. Note that overall output speed has been fixed at 9.4 μsec per computer word which will allow a maximum of 12 spots per line (assuming one spot per word). Means of increasing the number of spots per line will be discussed in subsequent sections.

Status Information. In order for the computer to know when to output data, the peripheral device must provide a status word for the computer to interrogate. As mentioned in the previous section, the PDP-11 has instructions which will allow it to perform this interrogation. The interface design then must provide a status word which can be set to request output data from the PDP-11.

Data Word Length. The PDP-11 has the capability of processing 8 bit bytes as well as 16 bit words. Using this byte capability would appear to be appropriate, as the EBCE only needs 5 bit accuracy. However, one 16 bit word will output faster than two 8 bit bytes, therefore an advantage can be gained by storing data words in computer memory byte locations in the order that it is desired to have them modulate the electron beam. Data transfer from the PDP-11 will be as 16 bit words. The interface will then split each 16 bit computer word into two 8 bit data words for interface manipulations. In effect,

one data word can be output each 4.7 μsec. Therefore, this design will compute and store 8 bit bytes and transfer 16 bit words to the interface. The interface will multiplex the 16 bit words into 8 bit data words for interface use.

Unibus Requirements. The PDP-11 unibus system must be properly buffered and terminated in order to drive peripherial devices without danger of data errors or equipment damage. Standard DEC units are available to perform this function at modest cost. This design will incorporate these units as a separate module described in Chapter III.

Electron Beam Control Electronics Operation and Requirements

The EBCE will be operated in the "single frame" mode for this study, that is, a manually operated push button on the EBCE console causes one frame to write on the phrase plate. In addition to the push button generated start, the EBCE requires a sweep sync signal to start the line sweeps and a video (beam modulation) signal. In return, the EBCE can supply an external unblank signal which is the signal that removes a bias voltage from a grid circuit and allows the electron beam to impinge on the phase plate.

Refer to figure 5 for the following discussion. The push button starts a long ramp deflection voltage which controls the frame sweep of the beam. The EBCE design is such that when the long ramp is present, sweep sync pulses are present prior to operating the "single frame" push button. Recall that the EBCE applies the unblank signal to the center 90% of the line sweep. A more detailed timing diagram for the EBCE operation is shown in Appendix A.

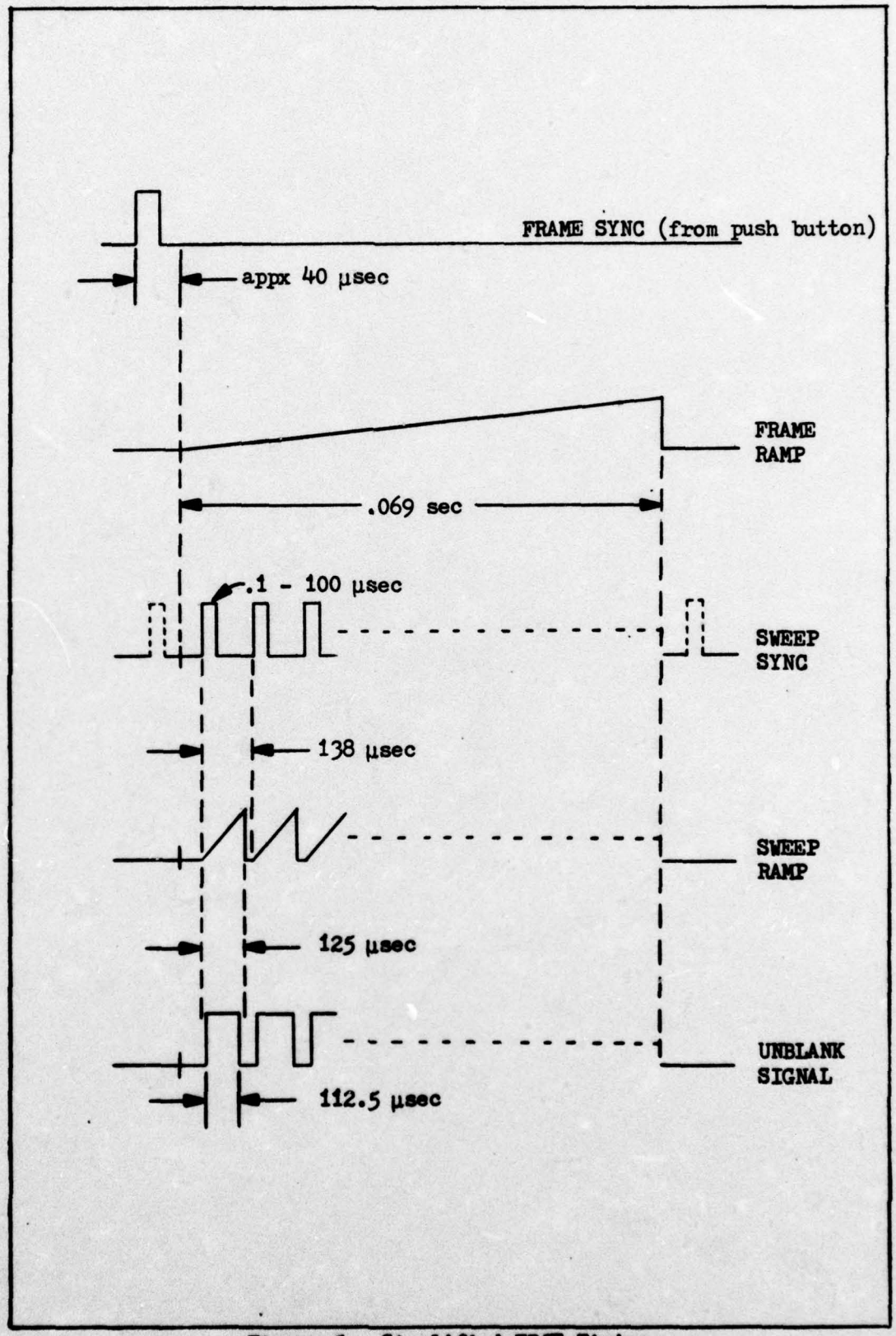

Figure 5. Simplified EBCE Timing

Sweep Sync Pulse. The sweep sync is normally provided by a simple variable frequency pulse generator. The pulse must drive one TTL load and the pulse length must not be longer than the sweep time. Since in this study the frame and line sweep times are both fixed, there is no requirement for varying the sweep sync rate. The sweep sync pulse will be fixed and, to simplify synchronization requirements, will be generated by the interface. The EBCE also has an output which can supply the unblank signal to the interface.

Video Input. The video signal is the actual modulation signal provided to the EBCE. This is an analog signal that will control the electron beam intensity, and thus must have the same degree of resolution as the desired phase modulation. In order to obtain this signal, the 8 bit data word must be processed by a D/A converter prior to being sent to the EBCE. This converter will be included as part of the interface and must have specifications which will yield the desired 5 bit resolution at a rate fast enough to prevent markedly degrading the phase plate spot deformation.

Interface Requirements

This section defines the functional blocks (modules) within the interface as shown in figure 6. These modules are the prime emphasis of the hardware design and thus provide the basis for the entirety of Chapter III, "Interface Design". It should be realized that the configuration derived by this author is merely one of many workable possibilities. However, the basic functional requirements are valid and the blocks presented provide what the author feels is a "good" approach.

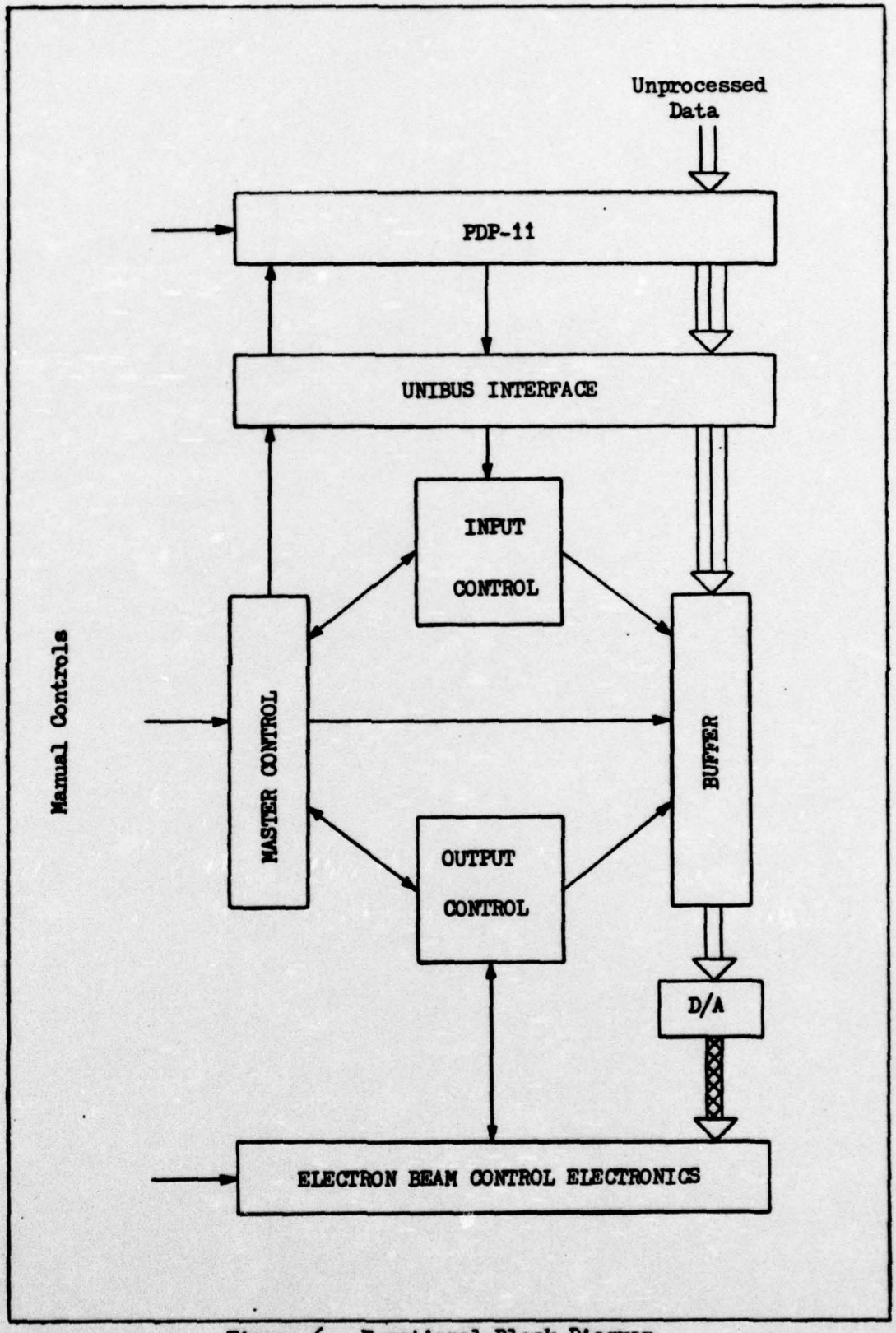

Figure 6. Functional Block Diagram

Buffer. The difference in operating speeds of the PDP-11 and the EBCE requires that some type of memory be available for temporary data storage. The buffer module must accept data from the unibus, temporarily store the data, and output the data at the correct time for EBCE usage. Therefore, the buffer module will incorporate a memory unit which will hold data transferred from the PDP-11 until the synchronization requirements with the EBCE are met and the data can be output. It appears that serial input of computer words to the interface and serial output of data words from the interface will provide a workable scheme. The buffer module must also contain logic which will select the proper byte from the computer word to guarantee that data output sequence and stored data sequence (in the PDP-11) are the same.

The buffer module also has special requirements, such as storage capability, transfer rate, and data repeat capability, that impact the type of storage system to be used for the memory unit. It is necessary to investigate these requirements in order to define the memory unit organization.

1. The sequential serial in/serial out scheme suggests the use of a first-in-first-out (FIFO) memory. Since read out of a FIFO usually results in data destruction, it will be necessary to take precautions to prevent loss of data if it will be needed again.

2. The amount of storage space (memory) available is a critical factor. In order to fix this value, it is necessary to define how the memory unit will be used.

a. The memory could be filled with all spot data stored in the computer, then the data output to the EBCE with correct synchronization. However, for a 10,000 spot matrix the large memory size

and associated expense is inconsistent with the constraints of this study.

b. If a memory the size of one line of data were used, the buffer could go through alternate fill/empty cycles and provide correct output synchronization. The problem here is that the line flyback time of the electron beam does not allow adequate time for refilling the buffer with more than two data points (13 μsec ÷ 4.7 μsec) prior to starting the next sweep. This would yield a maximum matrix of 2 x 500 spots, much too small to meet the user requirements.

c. The problems of the previous paragraphs are solved by choosing a dual buffer system as the memory unit configuration for this design. Each buffer section of the memory unit (hereafter called buffer #1 and buffer #2) will be capable of storing one line of data (100 words). With this configuration it is possible for buffer #1 to be outputting data while buffer #2 is being filled by the PDP-11, and vice versa. For a 10,000 spot (100 x 100) matrix, the time to fill each buffer is (4.7 x 100) μsec = 470 μsec. Since this matrix arrangement requires each line sweep (138 μsec) to be repeated at least 5 times, (5 x 138) μsec - 470 μsec = 220 μsec will be the minimum time allowed to perform any addressing, updating, or status checking necessary between data line outputs from the PDP-11. It is important to note that in order to have adequate time for this configuration to work, one of the buffers must be filled with valid data prior to starting an output to the EBCE. This memory unit configuration will also require some type of selection mechanism within the buffer module to allow choosing either buffer #1 or buffer #2 for input or output.

The memory configuration of (c.) meets the target matrix size (100 x 100) requirements and will also allow a smaller matrix choice simply by increasing the number of times a line is repeated and/or increasing the hold time for a particular spot data value. For the remainder of this study, N x M represents a variable size spot matrix where N and M are any integers less than 100. N is the previously defined number of spots per line and M is the number of different lines which have been repeated (500 lines ÷ number of times each line is repeated = M).

3. In order to write data from a buffer for successive line sweeps, a non-destructive read out memory should be used. However, since a FIFO has been chosen, the output must be rewritten back into the buffers so that data will be available for the next repeated line. This sets a requirement for data reentry logic.

The description of the buffer module as shown in figure 7 has generated a need for a number of control signals. Although not all these signals can be defined until some component selection is accomplished, many requirements are now apparent. These signal requirements will be presented where applicable in the remainder of the functional block description. The register transfer diagrams for input and output sequences are shown in figures 8 and 9.

Control. The overall control function can be broken into a number of smaller control blocks. This design logically lends itself into an input control block and an output control block for transferring data in and out of the buffer. The input control must cause data to be accepted any time the PDP-11 presents it, i.e., accept data asynchronously from the PDP-11. The output control must be

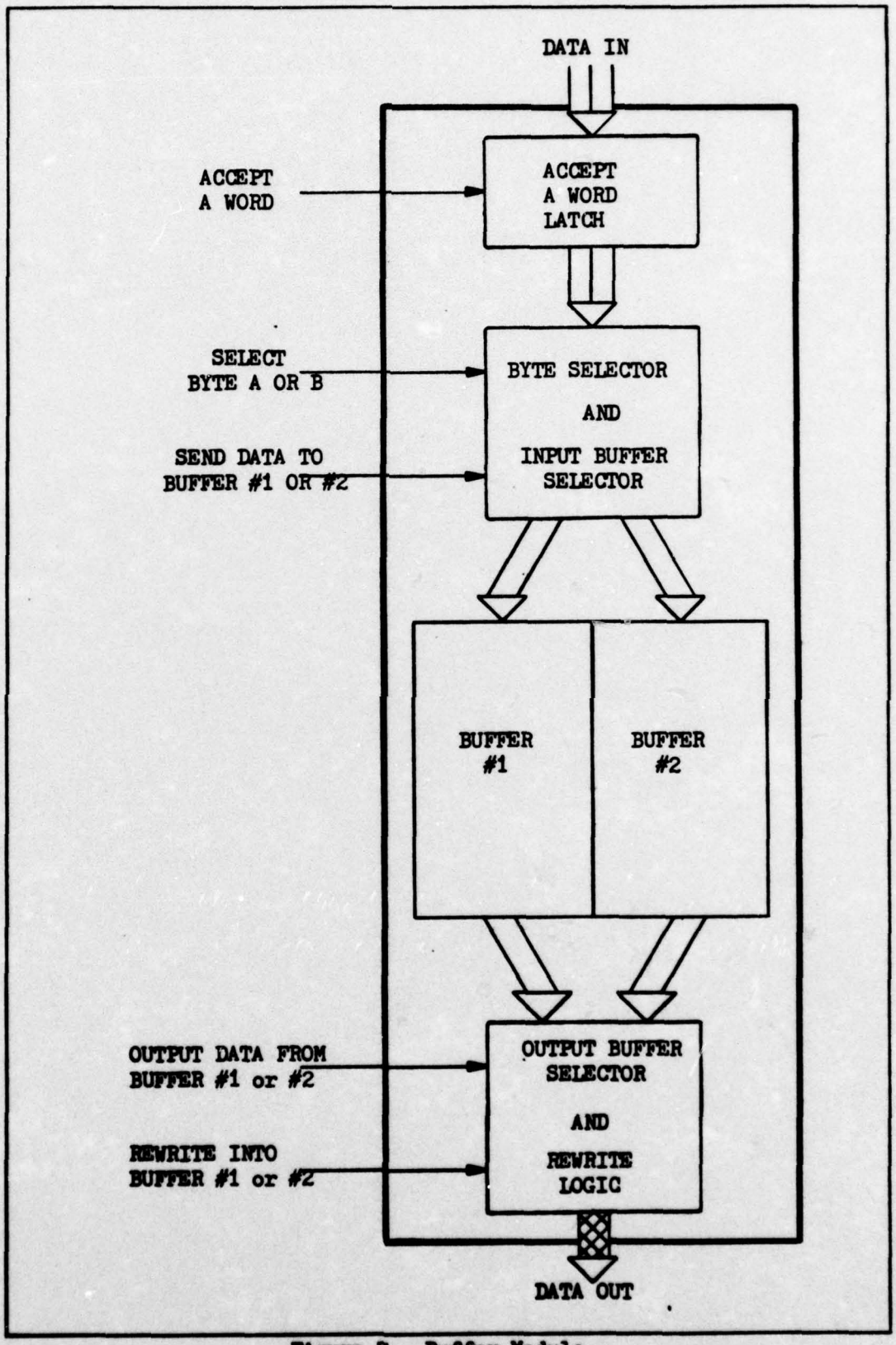

Figure 7. Buffer Module

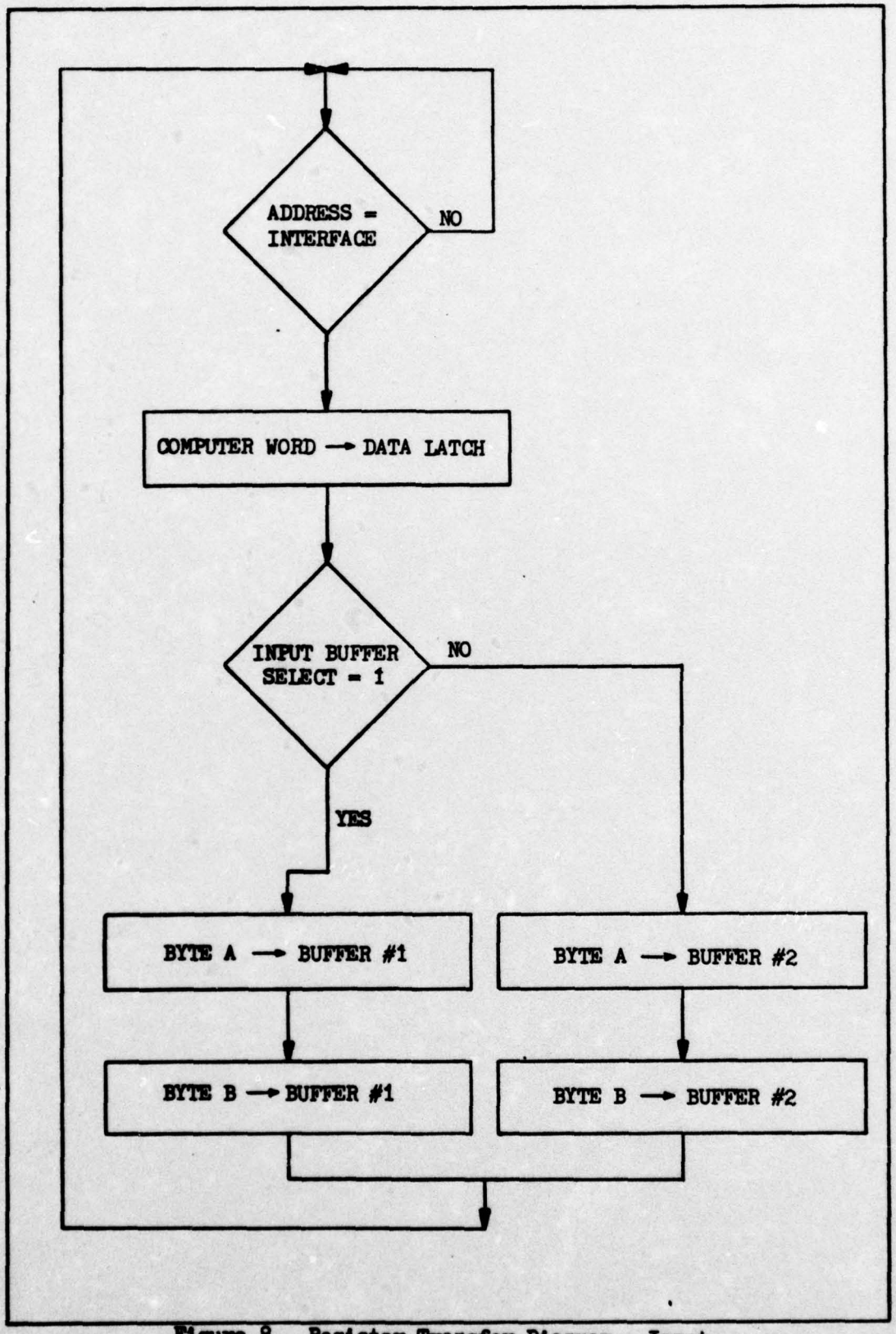

Figure 8. Register Transfer Diagram - Input

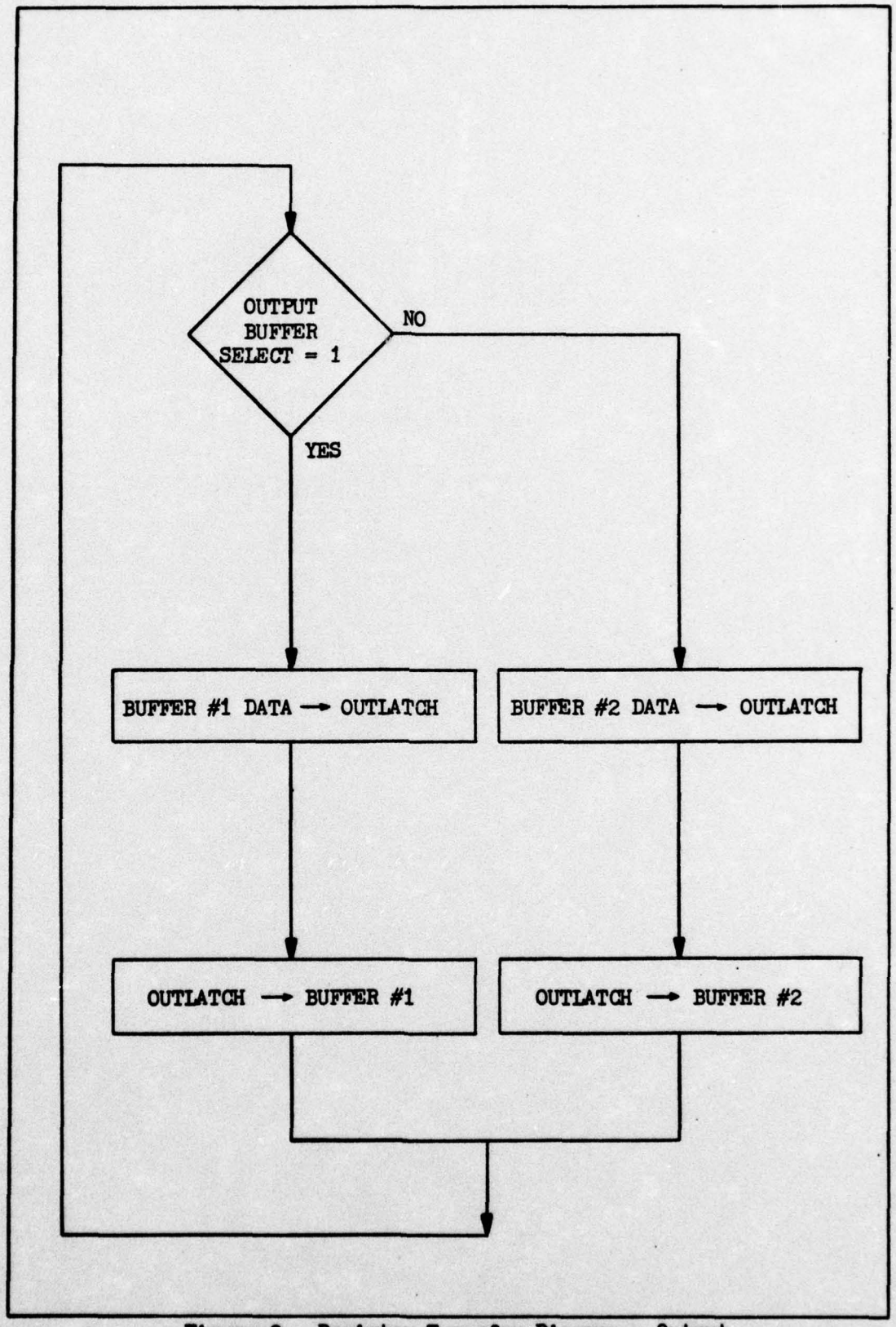

Figure 9. Register Transfer Diagram - Output

synchronized with and, as mentioned previously, provide a sweep sync signal to the EBCE. This can most efficiently be accomplished by using a clock signal, thus making output a synchronous operation on command by the unblank signal. Due to the asynchronous nature of the data transfer, a master control block will be incorporated to provide coordination within the interface. The master control module will accomplish this coordination through communication with the PDP-11 (status word), buffer (control signals), and EBCE (sweep sync and unblank signals).

The total interface design, then, will be considered an asychronous machine which segregates the input and output data flow between two synchronous machines. This will be accomplished through use of input, output, and master control modules as shown in figure 6. These modules will be further subdivided into individual task units. These units are described where applicable here, but their operation and design description are delayed until Chapter III.

1. Input Control. The primary purpose of the input control module is to transfer data words into buffer #1 and buffer #2. To accomplish this task, a number of requirements must be considered and hardware implemented where necessary. The control module diagram for the following discussion is shown in figure 10.

a. The interface must initiate action to accept a computer word from the PDP-11 unibus when that particular word is intended for the interface. To accomplish this, the control unit must receive a signal from the unibus interface module (incorporating standard DEC units) telling it to accept a word. The input control must generate a signal at that time to accept the computer word and then through a

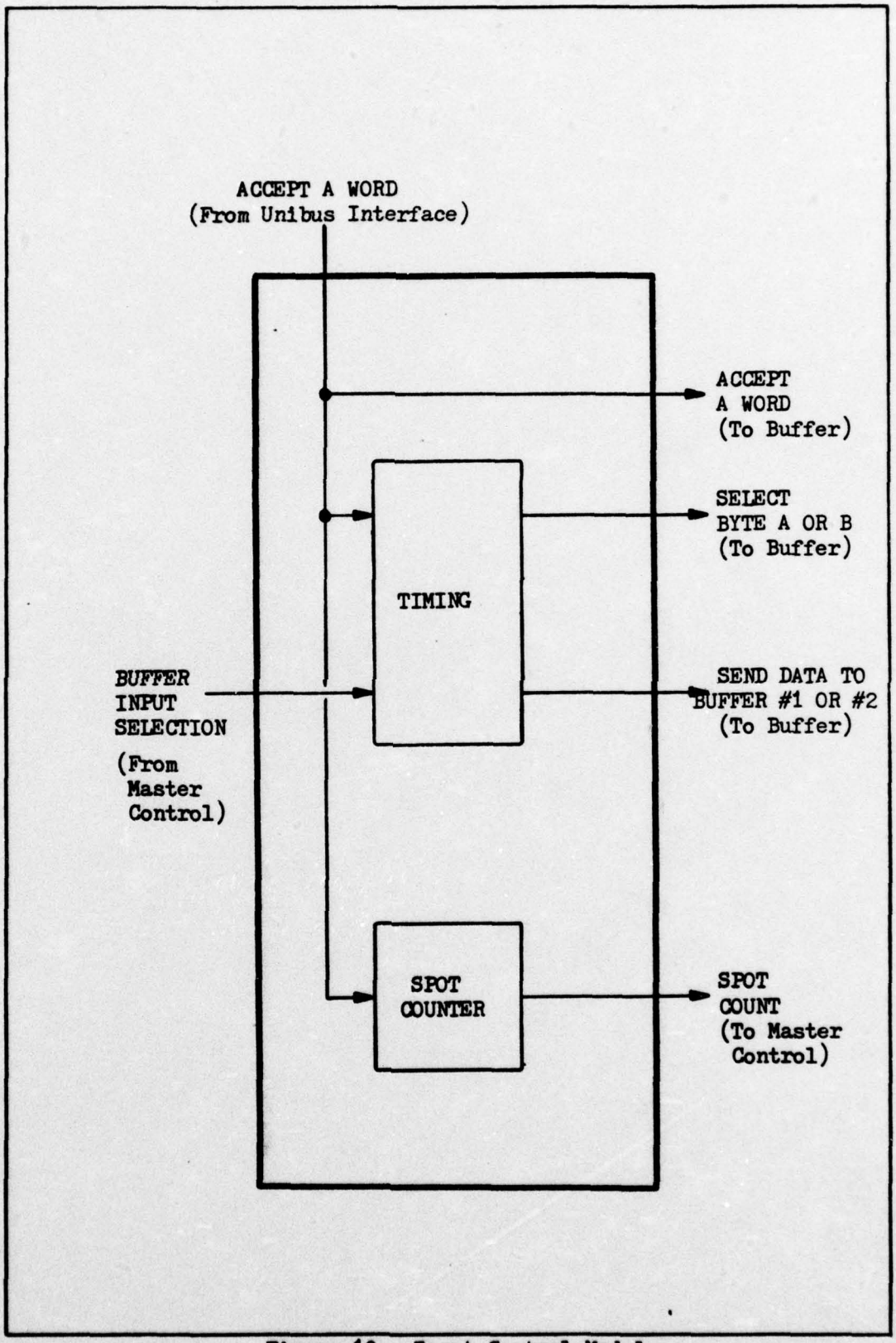

Figure 10. Input Control Module

timing unit generate signals which cause the buffer module to split the computer word into two data words and then to shift the data words sequentially into either buffer #1 or buffer #2.

b. In order to operate synchronously with the PDP-11, the control module will also contain a spot counter to determine how many computer words have been accepted. The counter will communicate the interface acceptance of the correct number of words by initiating a "do not transfer" signal to the PDP-11 through the status word. With this scheme, the computer software can be written to transfer a predetermined number of words (to agree with matrix size) from memory without incrementing slow software counters. At the end of the block transfer a software wait and check for status will occur until the interface asks for the next block of words to be transferred. Simply stated, the PDP-11 software is written to transfer N data points and the interface spot counter is manually preset to count down from N data points. After transfer of these N points, the PDP-11 and interface will communicate through a status word to determine when transfer of the next block of N points should begin. To accomplish this operation, it is necessary to pass the spot counter output to the master control module which will provide a status word to the PDP-11.

c. The input control operating speed is also an important consideration. The spot counter must provide the correct information to the master control module fast enough to allow for a status change and PDP-11 recognition of this change prior to outputting more data. Also, the input control timing unit must be designed so that all data transfers will occur prior to the next receive signal from the PDP-11.

2. Output Control. The primary purpose of the output control module is to transfer data words out of the buffer module. This requires that various synchronization and communication actions be considered. The diagram for this module is shown in figure 11.

a. In order to prevent long unblank times of the line sweep with no electron beam modulation, the data word output signal must be synchronized with the start of the line sweep unblank. This can be accomplished by sensing and using the unblank signal from the EBCE to allow the output control to start data transfers from memory. The control module must then generate pulses to remove data from buffer #1 or buffer #2. The unblank signal can be used to gate these output pulses in order to provide properly synchronized output.

b. It has been previously mentioned that the interface will generate the line sweep sync signal that the EBCE requires. The output control module will contain a clock to generate this line sweep sync signal. In order to simplify synchronization, the data output signals should be derived from the same clock that generates the sweep sync signals. This suggests that a higher frequency clock be used with frequency division to obtain the line sweep sync and the data output timing. The data output signals will be derived from a variable counter which will provide variable timing between data point outputs. The variation in spot time is a function of the N dimension of the matrix, and must therefore be consistent with the N spots transferred from the PDP-11 under input control.

Output Control should also insure that the number of data points output to the EBCE agrees with the number of points stored in the buffer module being read. This will prevent the buffer

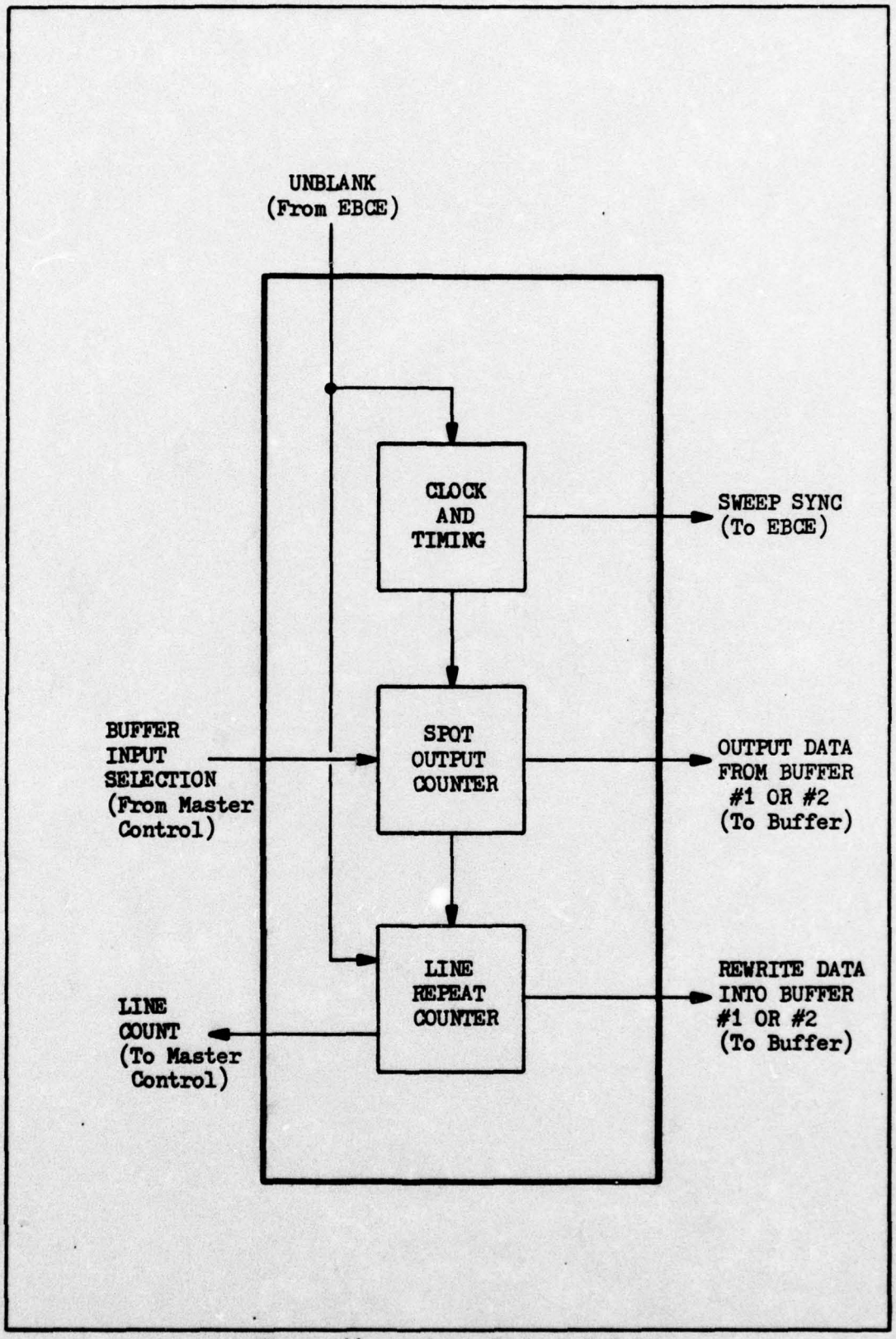

Figure 11. Output Control Module

from putting out erroneous value data points and will also be accomplished by using a counter.

c. Having made the N dimension of the matrix variable, the M dimension can also be made variable by providing the capability to change the number of times a particular line output is repeated. Since each line will always be repeated a minimum of five times (100 x 100 matrix), to provide for M to be less than 100 requires that each line be repeated more than five times. This will be accomplished by using a counter which can be preset to the number of times the user wishes to repeat any given data line; i.e., setting the counter to 100 will provide a N x 5 matrix.

d. As mentioned earlier, some type of rewrite logic for the FIFO buffers is required. This unit must cause the output data to be rewritten back into the buffer each time the line-repeat counter (identified in the previous paragraph) indicates the data line will be repeated. The unblank signal will be used to gate rewrite pulses to the buffer in a method similar to that discussed to remove data from the buffers. Also, the input to the buffers must be multiplexed between new data and data to be rewritten from the output. This multiplexing can be controlled by the master control module.

e. The output control module must also communicate with other functional modules. It must supply signals which will allow other modules to reset counters at the end of a frame, to clear a buffer when the data has been used, and to choose the correct buffer from which to read out data.

3. Master Control. The master control module will have the function of coordinating all input, output, and manual control actions

as well as providing status communication to the PDP-11. The master control module (see figure 12) must base its control operation on signals supplied by the input and the output control modules and on manually supplied signals. Master Control will act strictly in a coordination capacity to provide smooth interface operation that is in correct synchronization with both the PDP-11 and the EBCE. Master Control will provide the coordination without use of a clock. However, clock derived signals from the output control module are used, as mentioned in the previous section, to allow correct synchronization with Output Control information.

a. A primary task of the master control module will be to provide the status information through the unibus to the PDP-11. The status unit must provide a "transfer data" signal through a status word as a consequence of a manual run decision by the operator and the full or empty status of buffer #1 or #2. Since the PDP-11 is considered dedicated to this interface, there will be no peripheral contention for the unibus. Therefore, use of the status word will provide the only means of initiating data transfer; the interface will contain no interrupt capability.

b. The master control module will include the buffer (#1 or #2) selection units for both input and output. This signal will then be passed back to the appropriate (input or output) functional module for use as discussed in previous sections. The signals to be used for this selection are those discussed in the Input Control and Output Control sections.

c. A "clear" signal will be generated by a clear unit, also a part of Master Control. This signal will be used to clear all

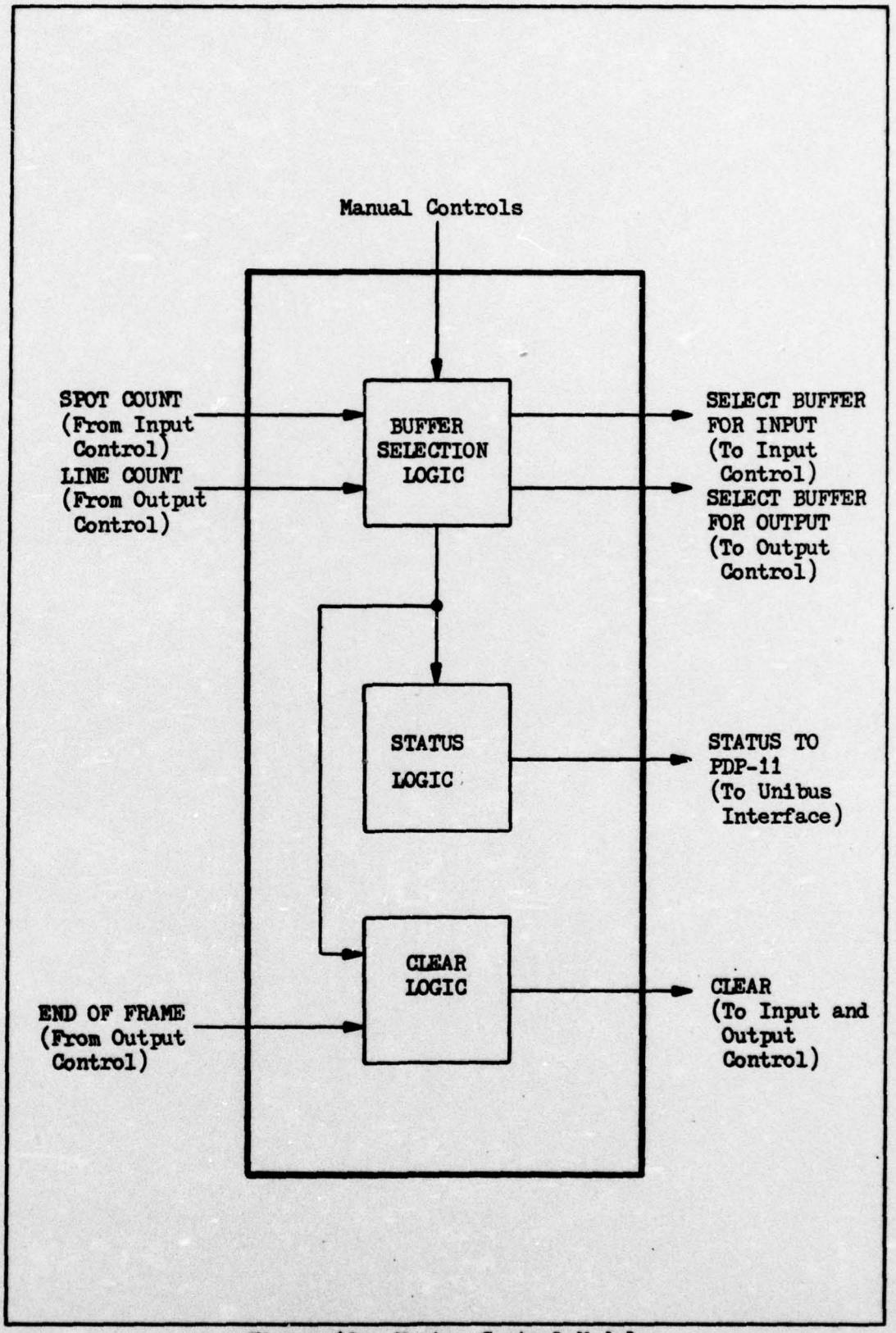

Figure 12. Master Control Module

counters to an initial start (ready to write a frame) condition and to reset the status unit. This clear signal will be the result of either a manual clear (operator push button) or the end of writing a frame as communicated by Output Control.

D/A Converter. The D/A converter will accept output data directly from buffer #1 or buffer #2 (output controlled by the output control module) and apply it in analog form to the video input of the EBCE. The D/A output will maintain the analog value as long as the input value is not changed. From previous discussion, the D/A converter should have a maximum conversion time of 550 nsec for 5 bits.

Unibus Interface. The unibus interface will require three units. Two of these will be a unibus driver and a unibus receiver, as recommended by DEC, to buffer transfer of data between the unibus and a peripheral device. The third unit must be a device which will address the interface and direct it to either receive data (data words) or to send data. In this design, the only data to be sent to the unibus will be the status word. This unit must have the capability of acknowledging PDP-11 address signals in accordance with guidelines set forth in the PDP-11 Peripherals Handbook. These guidelines will not be discussed since it is anticipated that standard DEC units will be used for all three devies.

Summary

The block diagram of figure 6 is an expanded view of the simplified diagram shown in figure 2. This expanded diagram shows the communication and data flow paths between all functional blocks discussed in this chapter. The individual units within the functional

blocks, which perform particular functions discussed in this chapter, are not shown. More detailed data and communication paths, both within the functional blocks and between different blocks, will be presented in Chapter III as the individual unit designs are presented.

III. Interface Design

This chapter completes the design description of this study. The PDP-11 software is considered first, then the interface design implementation is presented. This chapter references more detailed information in the appendices. The design implementation describes the individual units that make up the modules discussed in Chapter II, their interconnection, and any applicable sub-unit description. An expanded block diagram showing more detailed control signal paths between the modules (intermodule control signals) is shown in figure 13.

Both the modules and the module units are given symbolic names in all module diagrams to aid in text description. The module names represent the true names of the modules (BUF = Buffer, IC = Input Control, OC = Output Control, MC = Master Control, EBCE = EBCE, UB = Unibus Interface), while the unit names are derived by simply adding numbers to the host module name (BUF1, BUF2, BUF3, ····). The intermodule control signals as well as internal control signals for each module are explained. Intermodule control signals will be identified by signal name and with the symbolic names of their source and destination modules. For example, (IC) DATL (BUF) describing the signal DATL indicates that IC is the source module and BUF is the destination module. Signal names that are only used within a particular module will not contain source and destination information. Additionally, subscripts will be added to indicate application of the signal to either buffer #1 or buffer #2; for example, (MC) RWR_1 (BUF) is applicable to buffer #1.

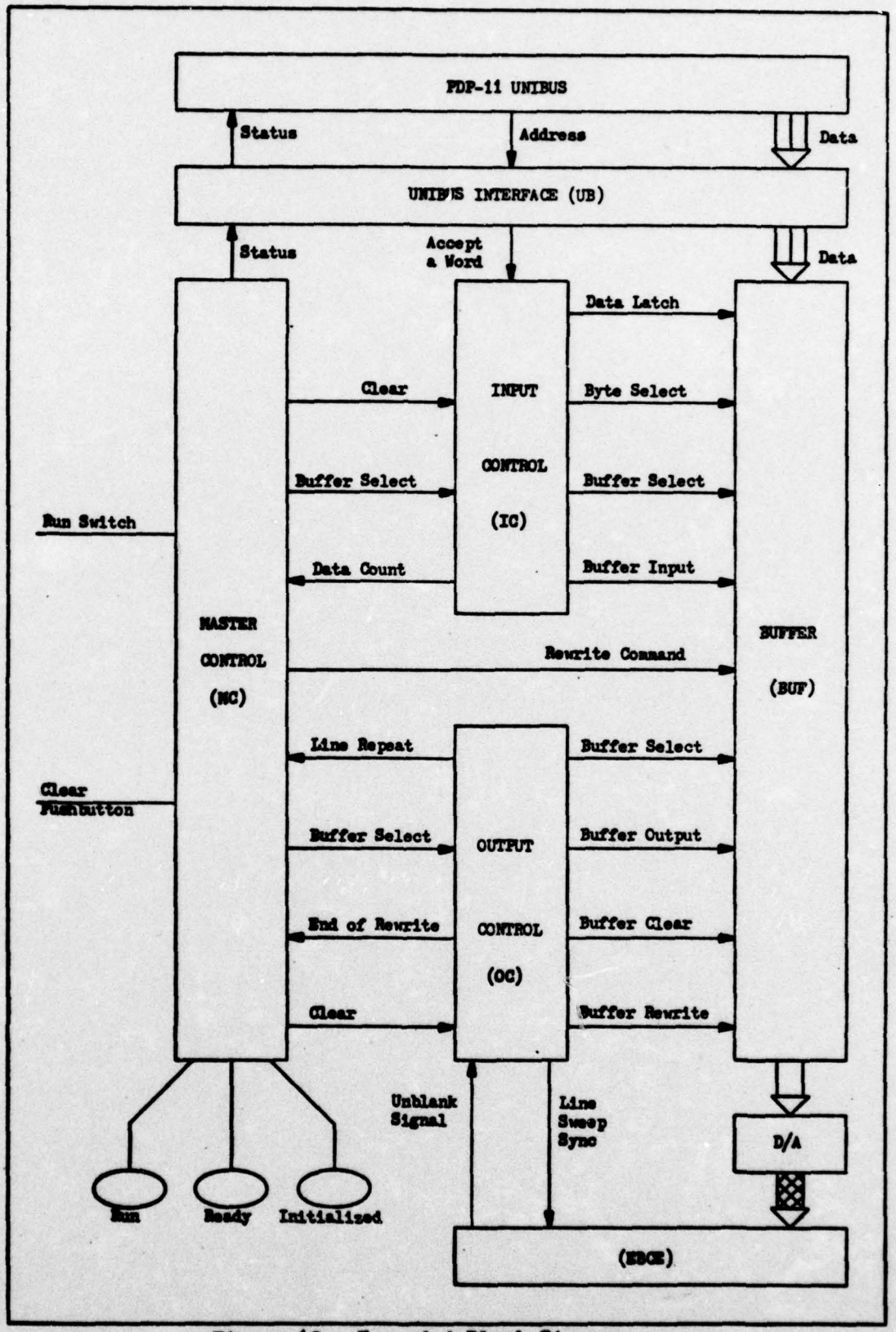

Figure 13. Expanded Block Diagram

Software Algorithm

As discussed in the computer requirements section of Chapter II, compute, store, and program controlled output (PCO) will be the method used by the PDP-11 for processing raw data and outputting modulated information to the EBCE. The computation will be accomplished and all modulation information stored prior to entering the output portion of the computer program. When data is requested by the interface, the correct number of words to write one line (having been a predetermined requirement of the program) will be output and a status check loop will be entered until a new line of data is needed by the interface. The flow diagram for the PDP-11 software is shown in figure 14, while a sample program of the output routine is shown in Appendix B.

Buffer (BUF)

Due to diverse operating procedures and signal requirements of different memory systems, it is necessary at this point to make a definitive selection of the FIFO. For this design the Fairchild 3351i 40 x 9 FIFO was chosen for buffer #1 and buffer #2. This FIFO is completely expandable in both word length and number of words; in this design it will be series expanded by three so that each buffer will be capable of storing 120 9-bit words. The signals required for the buffers are presented in the memory unit discussion in this section, while the signal generation is explained in the control module sections. The buffer module diagram, with signal names and their sources, is shown in figure 15. The component identification numbers for the buffer module are shown in Appendix C.

Data Latch (BUF1). When the PDP-11 addresses the interface with an output transfer data request (a MOV instruction), the first action

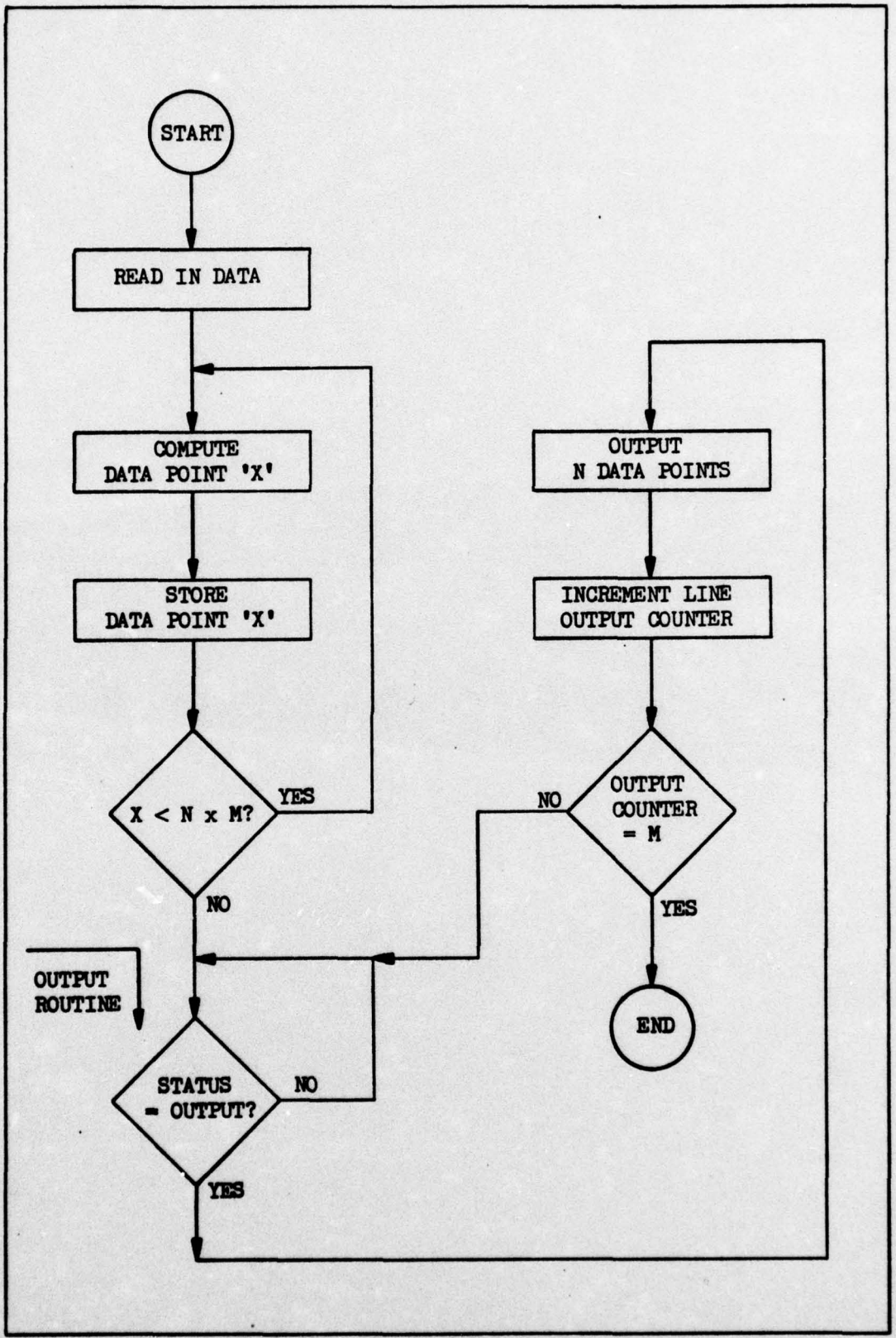

Figure 14. PDP-11 Software Flow Diagram

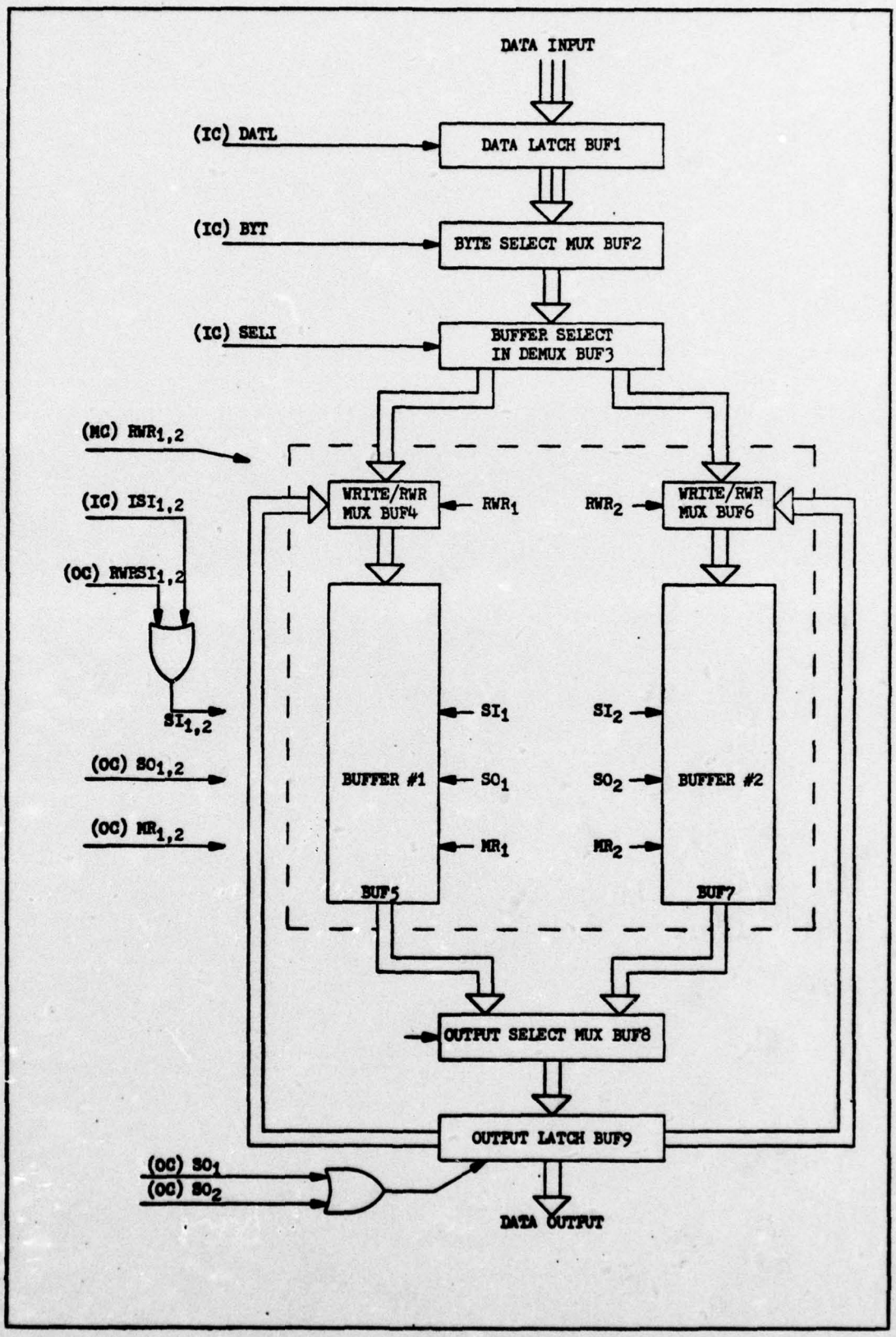

Figure 15. Buffer Module Diagram

of the interface is to strobe the computer word into a 16 bit latch (BUF1). This will serve to isolate the interface from the PDP-11 and will guarantee the availability of the data to the interface regardless of subsequent PDP-11 activity. The BUF1 latch signal (IC) DATL (BUF) is provided as the first in a timed sequence of control signals from Input Control.

Byte-Select Multiplexer (BUF2). Prior to the arrival of the next computer word at BUF1, the present word must be removed. This is accomplished with a multiplexer which first removes the lower order byte (BYTE A) of the latched computer word, then the higher order byte (BYTE B). In order to meet timing constraints of both the PDP-11 unibus and the FIFO, the multiplexing action requires a properly timed control signal from Input Control, (IC) BYT (BUF).

Buffer-Select-In Demultiplexer (BUF3). Since the decision has previously been made to use dual buffers, it is necessary to direct the data to the appropriate buffer. Master Control will generate the selection signal and pass it through Input Control so that the controlling signal will be (IC) SELI (BUF). The interface will always fill buffer #1 first, #2 second, then alternately fill #1 or #2 when each becomes empty as the selected number of lines are written from each buffer.

Write/Rewrite Multiplexer (BUF4 and BUF6). As part of the dual buffer system, BUF4 is identical in construction and operation to BUF6. The purpose of BUF4 is to allow either new data from the PDP-11 or previously stored data (to be used for a repeated line) from the buffer #1 output to be reinserted in buffer #1. The control signal

will coordinate both input and output activities and will therefore be generated directly by Master Control, (MC) RWR (BUF).

Buffer #1 and #2 (BUF5 and BUF7). BUF5 is identical in construction and operation to BUF7, both of which are the Fairchild 33511 FIFOs chosen earlier. The 33511s are connected in series as suggested by the manufacturer to provide 120 9-bit words of storage. This allows for slight future expansion on the 100 words required in this design.

The FIFOs require several signals which must be generated in order to provide input and output data movement. The timing constraints of these signals are critical in this design and to a large degree dictate control module designs. The FIFO timing requirements are contained in Reference 4.

1. A shift in (SI) strobe is required to move data into the FIFO. This strobe must be high for a minimum of 220 nsec, with 280 nsec minimum between strobes. A SI strobe will be required both to shift in new data (Input Control) and to rewrite data (Output Control), therefore the two signals (IC) ISI (BUF) and (OC) RWRSI (BUF) respectively will be OR gated to provide the SI when needed. As an example, to rewrite information into buffer #1, two signals will be needed, (MC) RWR_1 (BUF) and (OC) $RWRSI_1$ (BUF).

2. A shift out (SO) strobe is required to move data from the output position of the FIFO. This strobe must be present for a minimum of 200 nsec, with 300 nsec minimum between strobes. The FIFO can thus provide data for sequential output each 500 nsec (including the rewrite), well within the 1.125 μsec per output required for a 100 data point line. The shift out strobe (OC) SO (BUF)

will be generated by Output Control and must be sequenced with the unblank signal from the EBCE.

3. A master reset operation is available on the 33511 to set the buffer to all zeroes. In order to avoid any output confusion between old and new data, the clear operation will be exercised while the buffer is selected for output at the end of a repeated line output sequence. This will provide an empty buffer for new data being input from the computer. The control signal (OC) MR (BUF) will be generated as a consequence of the "line repeat counter" in Output Control. The signal must be 100 nsec minimum.

Buffer-Select-Out Multiplexer (BUF8). Since the data sequence will alternate between buffer #1 and buffer #2, starting with buffer #1, a multiplexer must be employed. The buffer selected will also depend on the number of times a line has been repeated. The control signal (OC) SELO (BUF) will be generated by the output control module.

Output Latch (BUF9). The output latch will hold the selected output data arriving from the output multiplexer. This will provide a stable bit pattern for the D/A converter. The latch control signal will be the OR gated shift out signals used for BUF5 and BUF7. Therefore, the data will remain stable between successive (OC) SO (BUF) signals.

The overall input and output timing sequences for the buffer module operation are shown in figures 16 and 17. Additional timing considerations are presented in the control module design selections and in Appendix D.

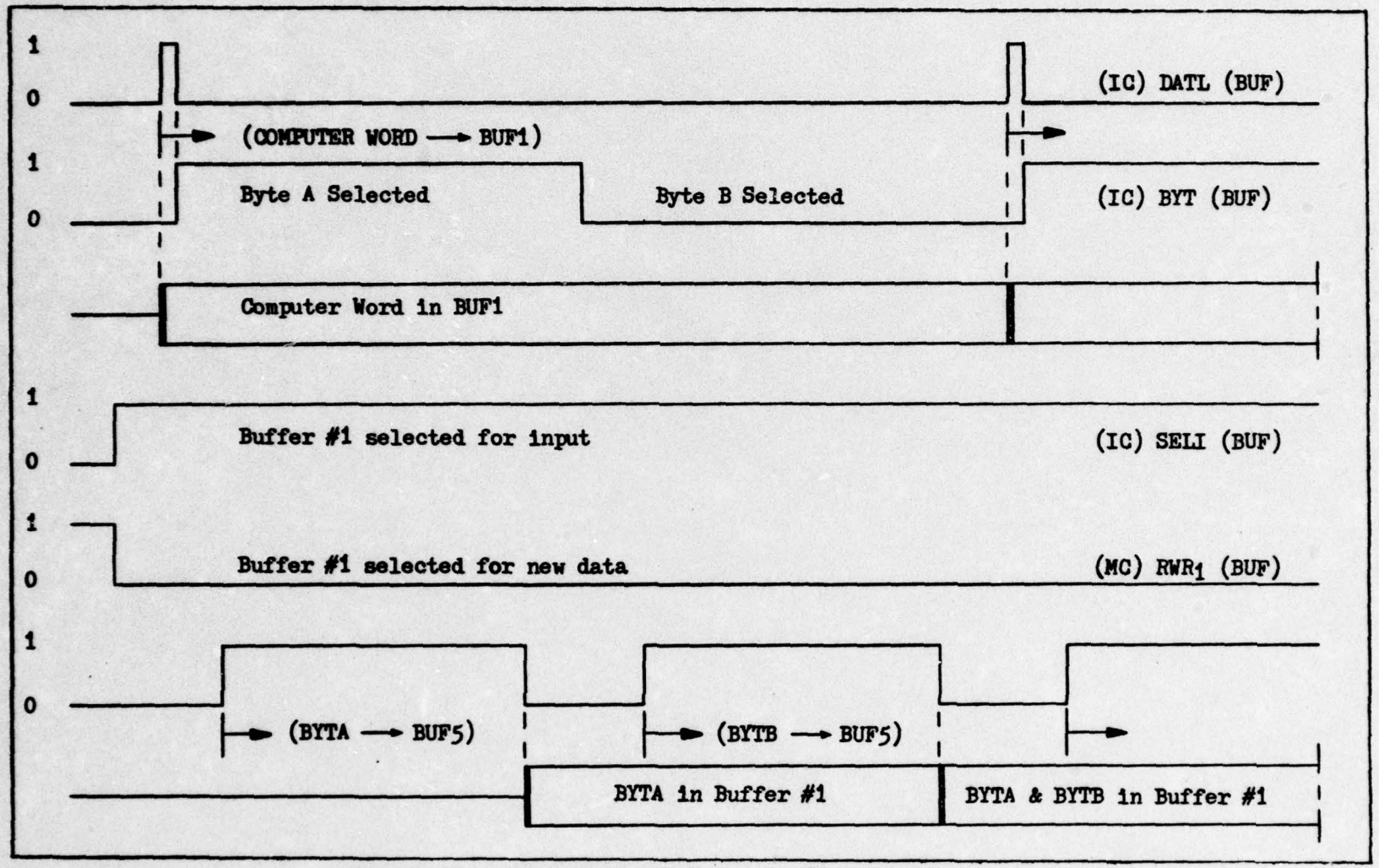

Figure 16. New Data Input Sequence (Buffer #1)

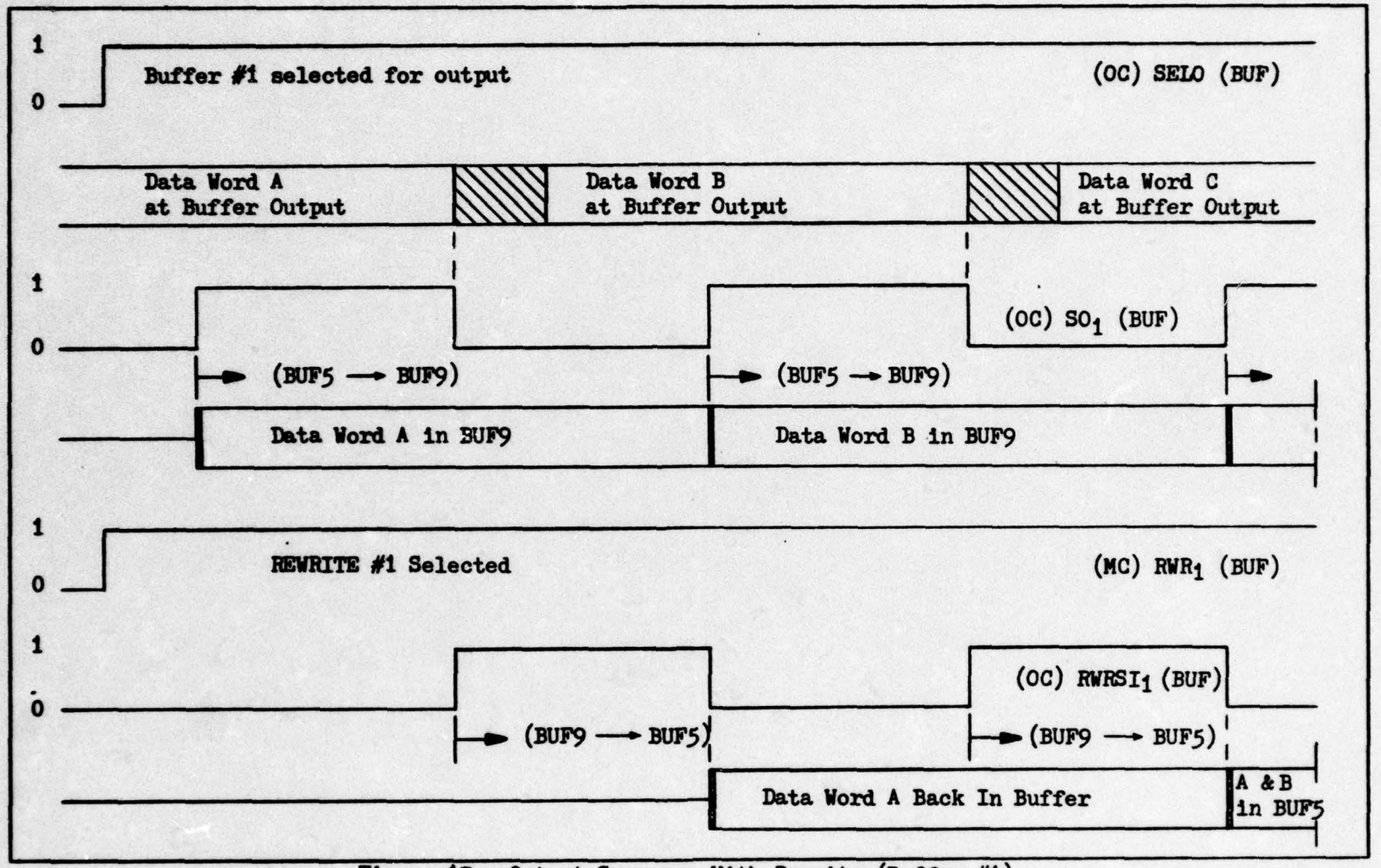

Figure 17. Output Sequence With Rewrite (Buffer #1)

Control

In accordance with the concept of structured design, the control portion of the interface design is divided into the previously discussed input, output, and master control modules. This division is not intended to imply that each is a separate and autonomous unit; indeed, the three modules are completely dependent on each other for proper control of data flow through the interface. The modules are intended to serve as logical division of control functions into hardware modules whose construction and operation are more easily understood.

Input Control (IC). Input Control generates all signals which are supplied to the buffer module in order to accept data from the PDP-11. To accomplish this, IC needs to receive only three signals, one from UB which acts as an accept data command, a clear command (CLEAR) from MC at the end of a frame, and the signal (MC) SELI (IC) telling which buffer is to receive the new data. IC will send the signal (IC) WDCT (MC) when the selected number of data words have been stored in memory. The input control module diagram is shown in figure 18 and the overall logic diagram is shown in Appendix C.

1. Accept a Word Logic (IC1). Previous discussion has indicated that a single signal from the unibus interface would supply the command to receive data. Actually, the receive signal is made up of four separate signals, three of which address the interface with control information and one which can be used as a correctly timed strobe to read a computer word from the unibus. The logic of IC1 will provide this strobe (ACPTWD) as an output to the timer and pulse generator which will then generate all signals necessary to move data into

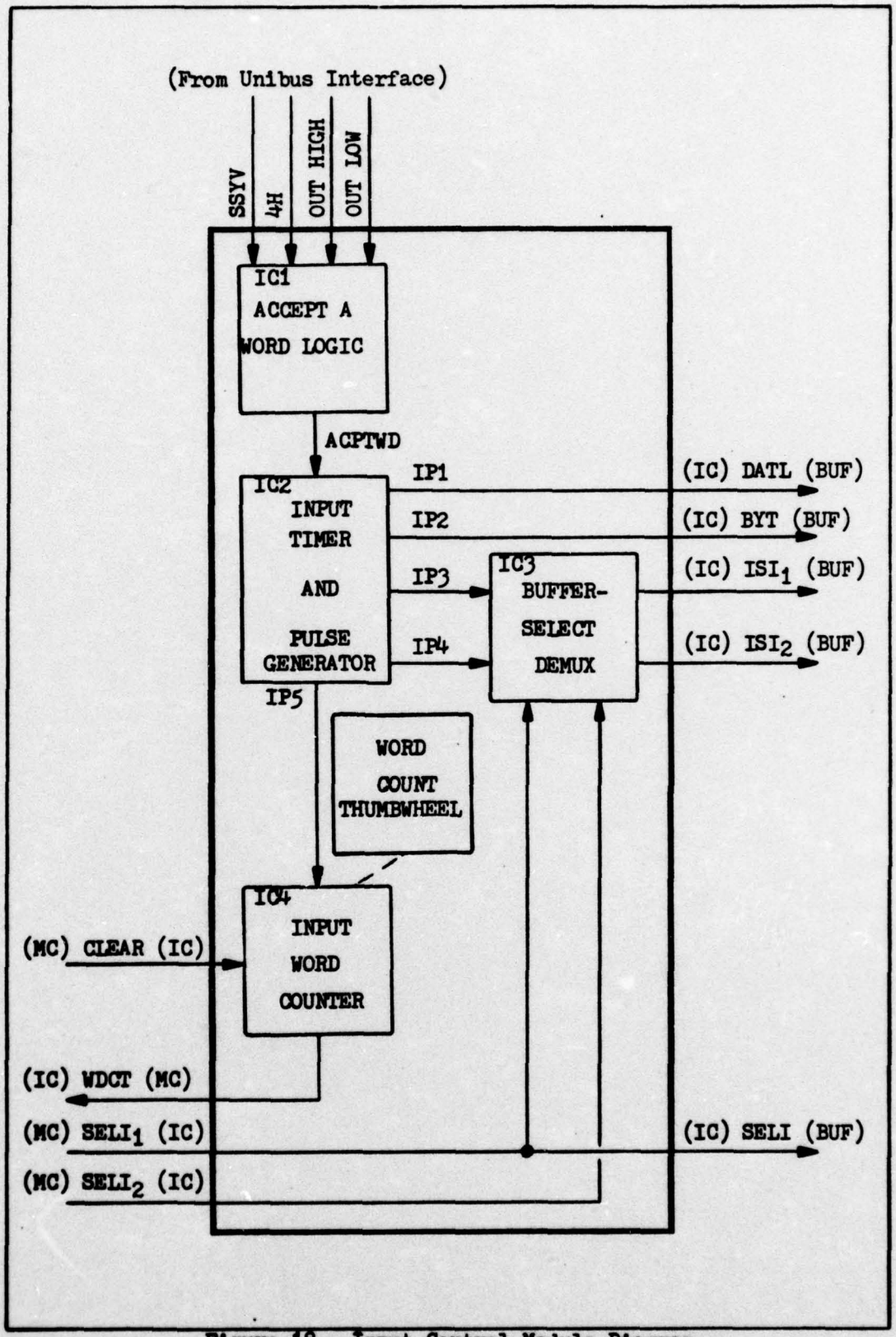

Figure 18. Input Control Module Diagram

the memory section of BUF. However, gating of part of these generated signals will be required by other units of Input Control.

2. Input Timer and Pulse Generator (IC2). IC2 is simply a multidelay and pulse generator unit as shown in figure 19 which will generate the required five signals, IP1 through IP5. The delay units 1-3 are monostable multivibrators which have their output pulse width adjusted to the appropriate delay from the input trigger IP1 (output of IC1). Pulse generators 1-4 are negative edge triggered monostable multivibrators which will supply the control signal pulses after the required delays.

The timing scheme of the pulses generated by IC2, which will move data as previously described from the unibus to buffer #1 or #2, is shown in figure 20. Table I identifies the IC2 output signals with their equivalent control signal name and the action caused by the signals. Since monostable multivibrators must be tuned to provide desired pulse lengths, this tuning must be an integral part of circuit construction. The exact monostable pulse lengths desired for this design are shown in the timing diagram in Appendix D. Note in figure 20 that four timing intervals are identified during which specific transfers occur.

3. Buffer-Select Demultiplexer (IC3). This unit will direct the signals that cause new data to shift into the memory to go either to buffer #1 or buffer #2. The direction is accomplished by gating (ANDing) IP3 or IP4 with the (MC) SELI (IC) signal to provide (IC) ISI_1 (BUF) or (IC) ISI_2 (BUF).

4. Input Word Counter (IC4). The word counter is a presettable down-counter which puts out a pulse every X counts of IP5.

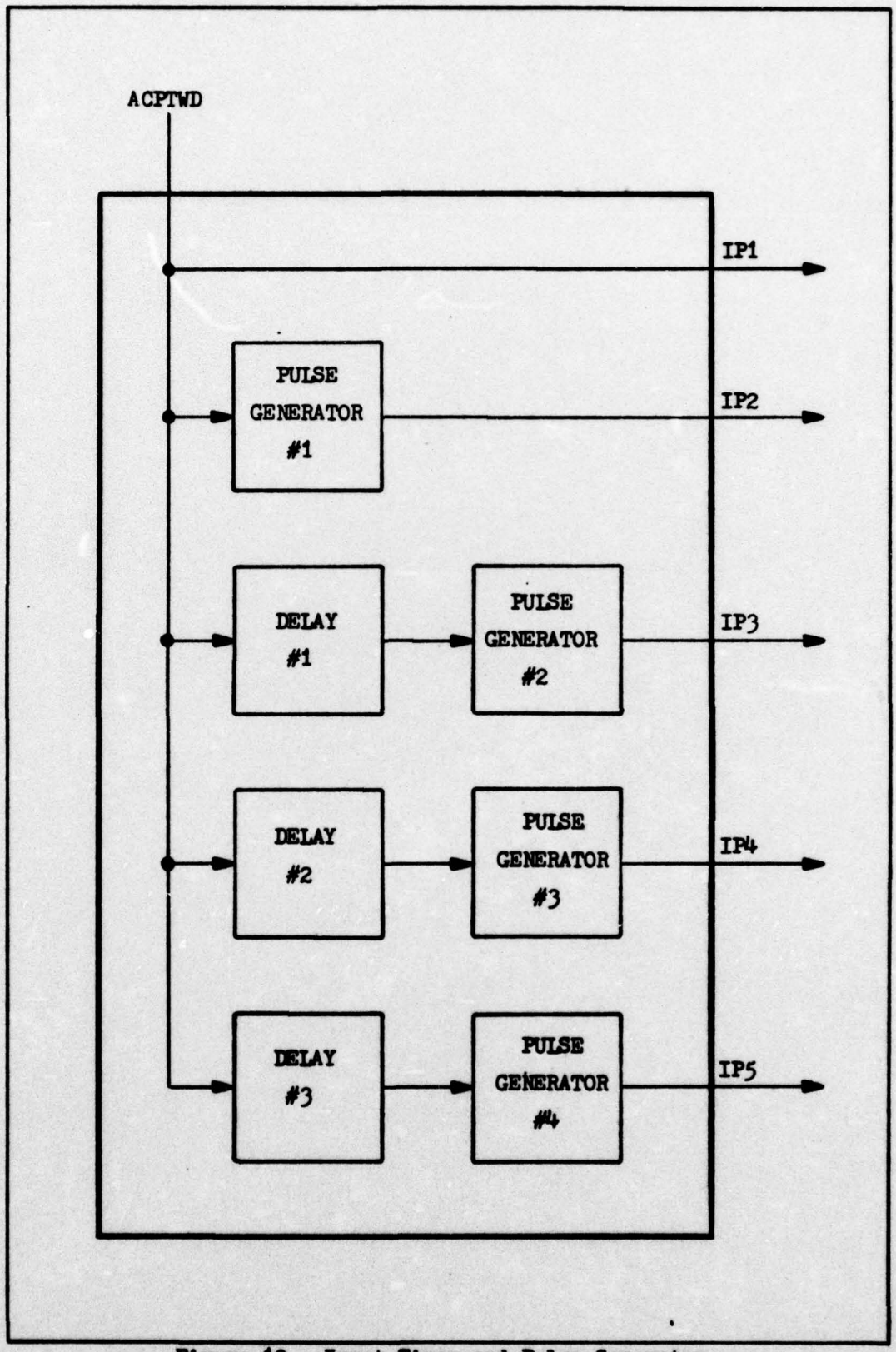

Figure 19. Input Timer and Pulse Generator

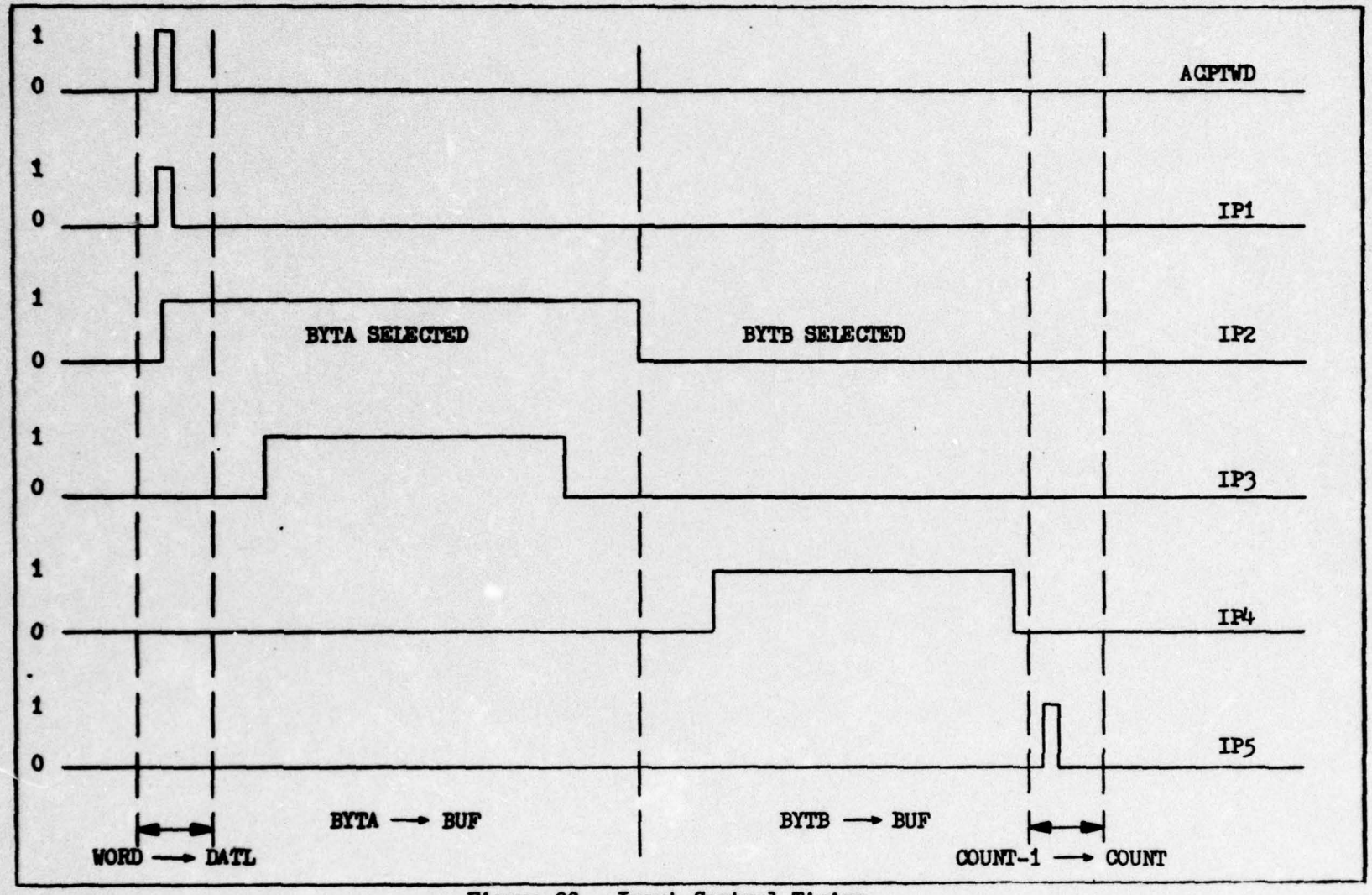

Figure 20. Input Control Timing

Table I. IC2 Signal & Pulse Usage

IC2 Output	Control Signal Name	Action
IP1	DATL	Causes a computer word to be strobed into BUF1 from the "D" line of the PDP-11 $D\langle 15{:}00\rangle \longrightarrow$ BUF1.
IP2	BYT	High signal selects low order byte through BUF2 for storage in memory. Low signal selects high order byte through BUF2 for storage in memory.
IP3	$ISI_{1,2}$ (following IC3)	Causes data selected by BUF2 (BYTA) to be shifted into buffer #1 or buffer #2, depending on (IC) SELI (BUF).
IP4	$ISI_{1,2}$ (following IC3)	Causes data selected by BUF2 (BYTB) to be shifted into buffer #1 or buffer #2, depending on (IC) SELI (BUF).
IP5	IP5	Decrements "Input Word Count" counter from preset value to count number of data words transferred.

From Table I we see that IP5 is a pulse generated at the end of every computer word (every two data words) transferred to the interface. A "Word Count Thumbwheel" will be used to set the counter to the correct down-count number for the desired matrix size. This number is found by dividing the matrix size (N dimension) by two and rounding the result up to the next full integer. For example, to obtain a 75 x 100 matrix, the thumbwheel would be set to $75 \div 2 = 37.5$ or $X = 38$. The counter generates (IC) WDCT (MC) and receives a (MC) CLEAR (IC) whenever it is present as determined by the master control module. (IC) WDCT (MC) will cause MC to change the status word to the PDP-11 and to select the other buffer (#1 or #2) for filling with the next block (line) of input data.

Output Control (OC). The output control module will generate or control all signals which are supplied to the buffer module to read data from memory, rewrite into memory, or clear memory (buffer #1 or #2). To accomplish these tasks, OC needs to receive three signals, (EBCE) UNBSIG (OC) which tells when the electron beam is unblanked and ready for modulation data, (MC) CLEAR (OC) at the end of the frame, and (MC) SELO (OC) telling which buffer is to output data. OC will supply the sweep sync trigger (OC) SWPTRG (EBCE) to initiate the line sweep. It will also send signals which tell: (1) when a line of data has rewritten into the selected buffer, (OC) RWREND (MC), and (2) when a line of data has been repeated the desired number of times, (OC) RPTEND (MC). It should be noted here that any time data is read from buffer #1 or buffer #2, the same data will also be rewritten back into the buffer so that it will be available to use as a repeated line. Thus, (OC) RWREND (MC) will indicate that data has been read from the selected

buffer, as well as a rewrite having been accomplished. If the data will not be used for a repeated line, the selected buffer will be set to all zeroes. The output control module diagram is shown in figure 21. Appendix C contains detailed diagrams of each module unit and the component identification numbers.

1. Output Timer and Pulse Generator (OC1). The purpose of OC1 is to provide the clock generated pulses which are used in the interface and, through combinational logic, to generate the signals which initiate properly timed gating of pulses for reading data from buffer #1 or #2. OC1 is made up of a number of sub-units to generate these signals as shown in figure 22, Output Timer and Pulse Generator diagram. To facilitate text description, the sub-units are referred to as OC1-1 through OC1-6.

a. CLOCK (OC1-1). The clock frequency must be such that it can be divided down to provide both the line sweep sync trigger (138 μsec period) and the read from memory signal. The ideal clock frequency would be one which could be divided evenly to provide the sweep sync trigger (7246.38 Hz) and the fastest beam modulation frequency desired (888,888.89 Hz). In order to accomplish this, it would be necessary for the clock to run at speeds exceeding TTL capabilities.

A compromise frequency of 869565.21 Hz was chosen which has a 1.15 μsec period. This clock frequency can then be divided by 120 to give the 138 μsec period required for the line sweeps. However, the 1.15 μsec period will only allow a maximum of (112.5 μsec per unblank) ÷ (1.15 μsec per spot time) ≈ 98 spots per line. The author considers this sufficiently close to the 100 spots per line target criteria to be satisfactory.

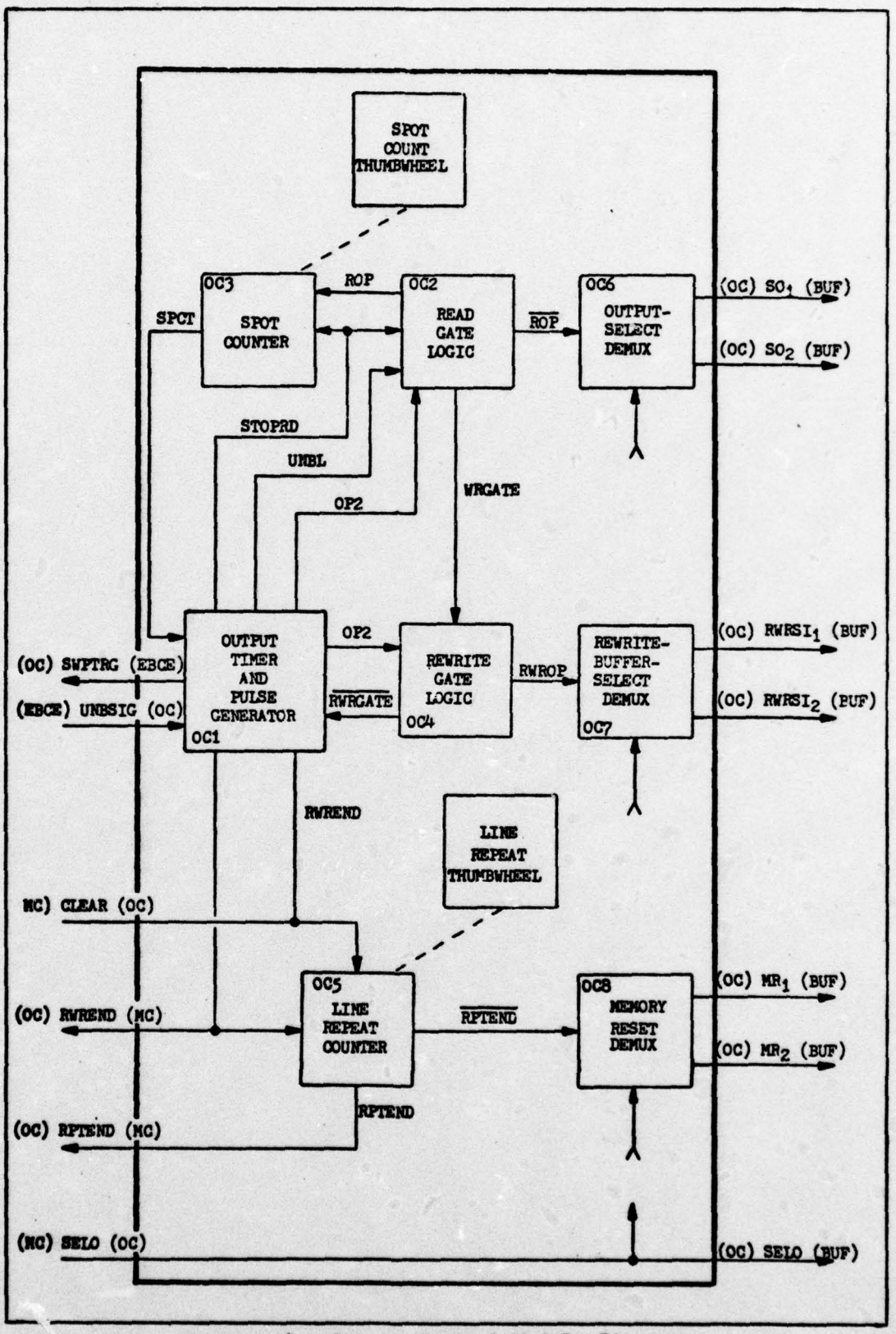

Figure 21. Output Control Module Diagram

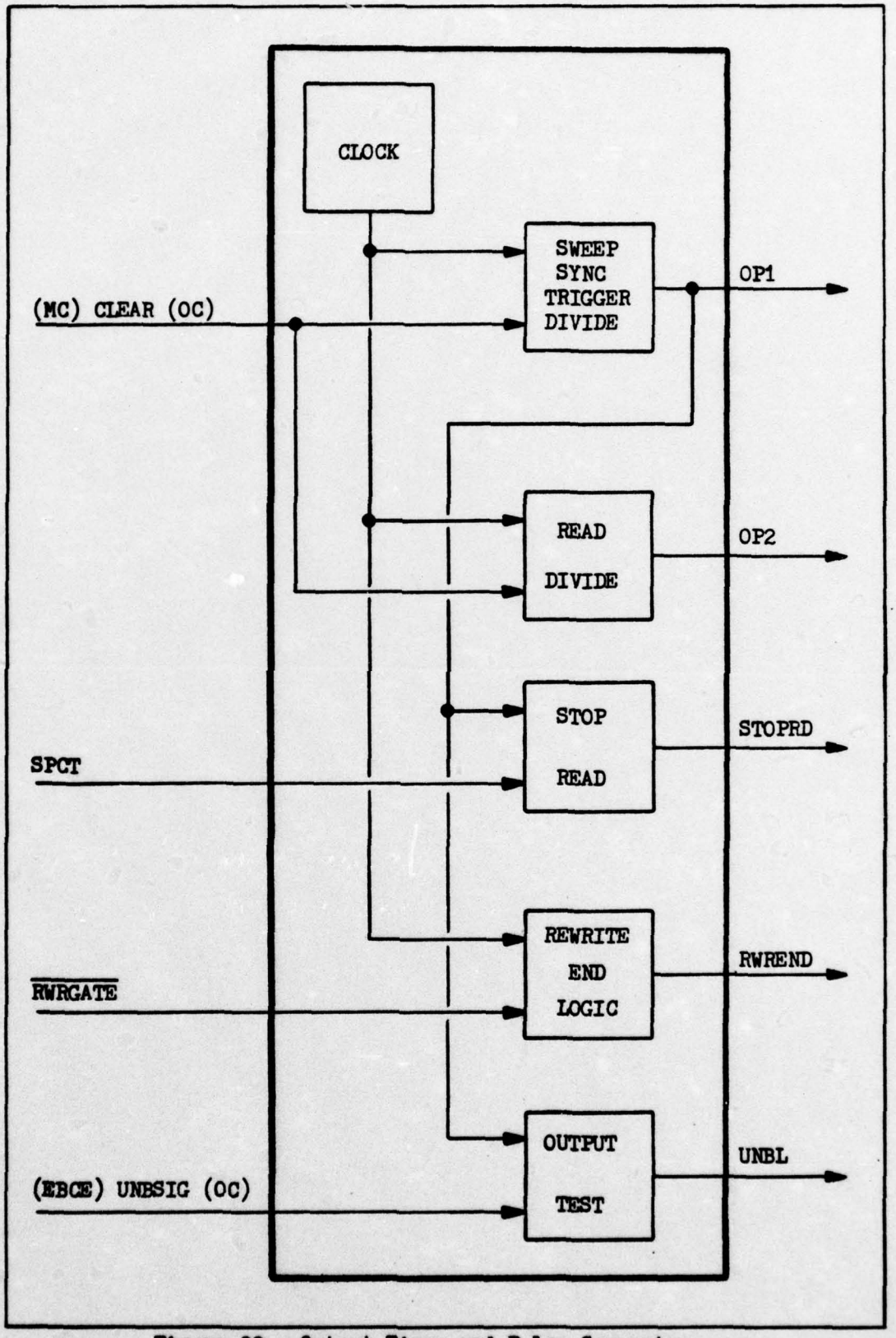

Figure 22. Output Timer and Pulse Generator

The clock will be realized through a simple tunable oscillator which should be adjusted to approximately 50% duty cycle. This duty cycle is important since the clock pulses are gated and divided down to obtain both SO and SI signals for buffer #1 and #2 operations.

b. Sweep Sync Trigger Divide (OC1-2). This sub-unit performs a division of the clock output by 120 to get OP1, the 7246.377 Hz signal for the sweep sync trigger. The divide function will be performed by a self resetting down-counter. OP1 is also used to reset other sub-units (to be described in this section) just prior to the next line sweep.

c. Read Divide (OC1-3). The read divide sub-unit is a settable divide by "Q" down-counter which will provide the OP2 pulses. The OP2 output pulses are gated by OC2 to provide the signal ROP which can be used to read data from memory. OP2 is also gated by OC4 to provide the signal RWROP which can be used to rewrite the memory output back into memory.

An important point in using OP2 is that the output pulses must be of sufficient length to meet the FIFO SO and SI pulse time requirements stated in the buffer module description. This constraint is met by using a settable down-counter which will output an OP2 pulse that is approximately the same length as the input pulse.

Another important point is the lack of OP1 and OP2 synchronization, other than being derived from a common clock source. Due to this lack of synchronization, the read divide number Q must always be an even divisor of 120 (sweep sync divide) in order to maintain the buffer module output in sequence with the beam unblank.

Table II. Matrix Size vs Q, N, & R

Q	N	Matrix Size	Spot Time (μsec)	R	Matrix Size
1	98	98 x M	1.150	1	N x 500
2	49	49 x M	2.300	2	N x 250
3	32	32 x M	3.450	4	N x 125
4	24	24 x M	4.600	5	N x 100
5	19	19 x M	5.750	10	N x 50
6	16	16 x M	6.900	20	N x 25
8	12	12 x M	9.200	25	N x 20
12	8	8 x M	13.800	50	N x 10
15	6	6 x M	18.400	100	N x 5
24	4	4 x M	27.600	125	N x 4
30	3	3 x M	34.450	250	N x 2
40	2	2 x M	46.000	500	N x 1

Q = "Read Divide" integer to provide the hold (or dwell) time for output data. This generates OP2 in OC1. The gating of OP2 by OC2 and OC4 provides both SI and SO signals.

N = "Spot Count" divide integer to provide the desired number of spots per line sweep (where spot size is determined by Q above). N must agree with the number of data points stored in the PDP-11 for each line. All lines must contain same number of data points. Refer to "Word Count" divider (IC4) of Input Control.

R = "Line Repeat" divide integer used in OC5 to provide that a specified number of data lines be repeated. This sets the M dimension of the matrix N x M.

Also, as no measures are taken to insure that OP2 arrives subsequent to UNBL, it will be possible to "loose" some portion of an OP2 pulse (due to the gating scheme of OC2). Values for the number Q which correspond to the N dimension of matrix size have been calculated and are shown in Table II.

d. Stop Read (OC1-4). This sub-unit uses the output from the spot counter (described later) to generate a signal (STOPRD) which will stop the gating of OP2 pulses to the memory. OC1-4 uses a JK positive-edge-triggered flip-flop with preset and clear which can be preset (turn on gating signal) by OP1 and cleared (turn off gating signal) by SPCT (signal from the spot counter).

e. Rewrite End Logic (OC1-5). This logic generates a pulse (RWREND) at the end of the rewrite sequence. The rewrite gating signal (described later) is used along with the clock to generate a RWREND two clock times long. RWREND can then be used as an input to counters which determine: (1) the number of data lines repeated (see OC5), and (2) when a complete frame (500 lines) has been written (see master control module). OC1-5 incorporates the use of two JK master-slave flip-flops with clear.

f. Output Test (OC1-6). The purpose of OC1-6 is to generate an unblank signal (UNBL) which will be used as the signal to initiate gating for OP2. UNBL will be either: (1) the inverted unblank signal (EBCE) UNBSIG (DC) or, depending on a selector switch, (2) a 120 μsec pulse generated by a monostable multivibrator which is triggered by OP1. The 120 μsec pulse will be used as a test function to simulate receiving (EBCE) UNBSIG (OC).

The timing scheme of the pulses generated by OC1, which will move data as previously described from buffer #1 or #2 to the D/A

converter, is shown in figure 23. Table III provides a summary of the OC1 output signals with their equivalent control signal names and the action caused by the signals. A more detailed timing diagram is contained in Appendix D.

2. Read Gate Logic (OC2). In order to guarantee that the SO and RWRSI signals persist for the required time duration, the decision was made to generate them by gating only complete OP2 cycles. This decision then prohibits simple ANDing of OP2 and UNBL to obtain SO and RWRSI. OC2 will generate SO, while OC4 will use OC2 information to generate RWRSI. A JK master-slave flip-flop in OC2 will generate a read gate signal (RDGATE) which will come high (open gate) the first time OP2 goes low after OC1-6 generates UNBL. The consequence of this action is the read out pulse (ROP) which will increment a spot counter and also generate (OC) SO (EUF) to read data from buffer #1 or #2. The flip-flop output will be cleared at the end of a line by the STOPRD signal from OC1. OC2 also contains an inverter to supply the necessary signal ($\overline{\text{ROP}}$) to OC6.

3. Spot Counter (OC3). OC3 is a programmable down-counter whose output (SPCT) will go high when the selected N pulses are counted. The spot counter is not wired to be self resetting as are all other counters in this design. Instead, it holds the output (SPCT) high until the STOPRD signal goes high (indicates new line of data to be output). This wiring configuration allows a simpler "stop read" logic sub-unit (OC1-4). It also guarantees that the read gate will only be open for OP2 pulses from slightly after UNBL until N spot counts have been reached. N is the same N used in describing the phase plate matrix size as N x M; the desired N dimension should

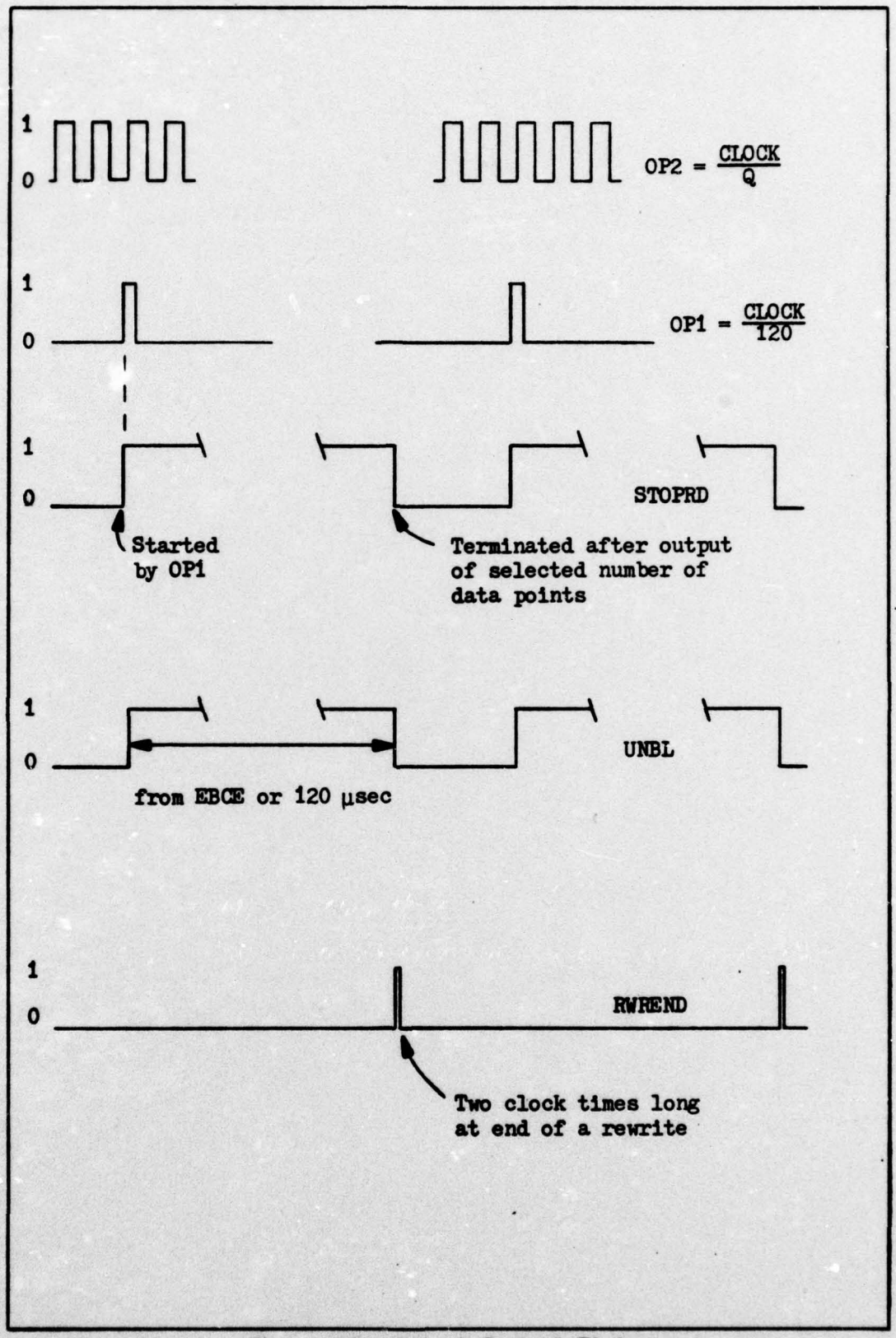

Figure 23. Output Control Timing

Table III. OC1 Signal & Pulse Usage

OC1 Output	Control Signal Name	Action
OP1	SWPTRG	Causes EBCE to start the phase plate write sequence. EBCE will then send (EBCE) UNBL (MC).
OP2	ROP (following OC2) $SO_{1,2}$ (following OC6)	Causes data to be shifted out of buffer #1 or buffer #2 depending on OC2, OC3, and (MC) SELO (OC).
OP2	RWROP (following OC4) $RWRSI_{1,2}$ (following OC7)	Causes data to be rewritten into buffer #1 or buffer #2 depending on OC2, OC4, and (MC) SELO (OC).
STOPRD	STOPRD	Turns off WRGATE in OC2 after selected number of data words have been read from a buffer. Allows WRGATE to be turned on by UNBL after SWPTRG.
RWREND	RWREND	Indicates end of the rewrite sequence to provide a count pulse for the "Line Repeat" Counter.
UNBL	UNBL	Turns on WRGATE in OC2 to let OP2 begin shift out sequence. Also turns on RWRGATE in OC4 to let OP2 begin rewrite sequence.

be set in the "Spot Count Thumbwheel." After the Nth count is reached, the SPCT signal is input to OC1. In addition to turning off the read gate, the STOPRD signal from OC1 resets the spot counter to N in readiness for counting the next string of read out pulses.

4. Rewrite Gate Logic (OC4). OC4 performs a function very similar to OC2, also using a JK master-slave flip-flop, but gating the OP2 signal to perform the rewrite function. Since there is a delay time for the data to be rewritten to appear at the FIFO input, the RWRSI signal must also be delayed. The rewrite gate logic accomplishes this by delaying RWRSI one half an OP2 cycle from the SO signal. OC4 thus generates a rewrite gate signal (RWGATE) which is ANDed with OP2 to form RWROP. Also $\overline{\text{RWRGATE}}$ is input to OC1 to initiate the RWREND signal described previously.

5. Line Repeat Counter (OC5). The line repeat counter is a presettable down-counter which puts out a pulse every R counts of RWREND. A "Line Repeat Thumbwheel" will be used to set the counter to the correct down-count number. It is this number which determines the repeat of a data line and thus the M dimension of the phase plate matrix. The number R is found by dividing the matrix size (M dimension) into 500 (number of line sweeps). For example, to obtain a 75 x 100 matrix, the thumbwheel would be set to 500 ÷ 100 = 5. The counter generates a repeat end signal (OC) RPTEND (MC) which goes to the master control module to aid in status determination and buffer #1 or #2 selection. OC5 also contains an inverter to supply the necessary signal (RPTEND) to OC8.

6. Output-Select Demultiplexer (OC6). This unit will direct the signals that cause the data read from memory to go either to

buffer #1 or buffer #2. The direction is accomplished by gating (ANDing) $\overline{\text{ROP}}$ with the (MC) SELO (OC) signal to provide (OC) SO_1 (BUF) or (OC) SO_2 (BUF).

7. Rewrite-Buffer-Select Demultiplexer (OC7). This unit will direct the signals that cause output data (data contained in the output latch, BUF9), which is to be rewritten into the memory, to go either to buffer #1 or buffer #2. The direction is accomplished by gating (ANDing) RWROP with the (MC) SELO (OC) signal to provide (OC) $RWRSI_1$ (BUF) or (OC) $RWRSI_2$ (BUF).

8. Memory-Reset Demultiplexer (OC8). This unit will direct the signals that cause buffer #1 or buffer #2 to reset to all zeroes just prior to reading in new data from the PDP-11. This is necessary to avoid mixing old and new data, since OC7 forces a rewrite at the end of each memory read cycle. The direction is accomplished by gating (ANDing) $\overline{\text{RPTEND}}$ with the (MC) SELO (OC) signal to provide (OC) $\overline{MR_1}$ (BUF) or (OC) $\overline{MR_2}$ (BUF).

Master Control (MC). The master control module will coordinate both the input and output control modules, provide status information to both the processor and the manual operator, make selections of buffer #1 or #2 input and output, and provide a means for manual control input to the interface unit. To accomplish these tasks, MC requires three previously defined signals, (IC) WDCT (MC) which tells when the proper number of data words have been stored in memory, (OC) RWREND (MC) which tells when data has been rewritten into the selected buffer, and (OC) RPTEND (MC) which tells when a line of data has been repeated the desired number of times. In addition, MC will incorporate

a manual run switch and a manual clear pushbutton to generate (MANUAL) RUN (MC) and (MANUAL) CLEAR (MC).

MC will also generate a number of control and status signals that have been described previously. These are (MC) SELI (IC) telling which buffer is to receive data from the PDP-11, (MC) SELO (OC) telling which buffer is to output data, and (MC) CLEAR (IC & OC) which resets counters in both IC and OC to an initialized state. CLEAR is also used within MC as described later. MC will also generate (MC) RWR (BUF) to control a selected write/rewrite multiplexer (BUF4 or 6), (MC) FILLBUF (UB) to act as the status word to the PDP-11, a RUN signal to power an indicator when the interface is in the run mode, a READY signal to power an indicator when the interface is ready for the EBCE to write a frame, and a INITIALIZED signal to power an indicator when the interface is ready to receive data from the PDP-11.

The master control module dictates the sequencing of all buffer operations. The initial starting state is such that buffer #1 is selected for input, write is selected for buffer #1, and buffer #1 is selected for output. This will be called the initial state as indicated by the initialized indicator. On power up, the RUN switch should be off and the initial state obtained by pushing the CLEAR button. When the RUN switch is turned on, the following sequence of operations will occur (assuming use of the sample program in Appendix B):

(1) Buffer #1 will be filled.

(2) Buffer #2 will be filled.

(3) The ready indicator will come on which, in conjunction with the initialized indicator, shows that the buffers are both full and waiting for output.

(4) A wait will occur until data in a buffer is used. Data will start being used when the single frame button is pushed on the EBCE unit.

(5) Buffer #1 will be read.

(6) Buffer #2 will be read while buffer #1 is being refilled.

(7) Buffer #1 will be read while buffer #2 is being refilled.

(8) Steps (6) and (7) will be repeated until the entire matrix has been written on the phase plate. At this time the computer will enter a hold status.

(9) The (MC) CLEAR (IC & OC) will automatically be generated in readiness for the next frame of information.

The master control module diagram is shown in figure 24. Appendix C contains detailed diagrams of each MC module unit and the component identification numbers.

1. Input Buffer Selector (MC1). This unit makes the selection of the buffer which will receive the next new data input from the PDP-11. MC1 uses a JK master-slave flip-flop with clear (wired as a toggle), which is in the initial state (buffer #1 selected) when cleared. The initial state is obtained as a result of the CLEAR signal. Subsequent to the initial state, each time MC1 receives (IC) WDCT (MC) the flip-flop will alternately set and clear to alternate input selections between buffer #1 or #2. Recall that

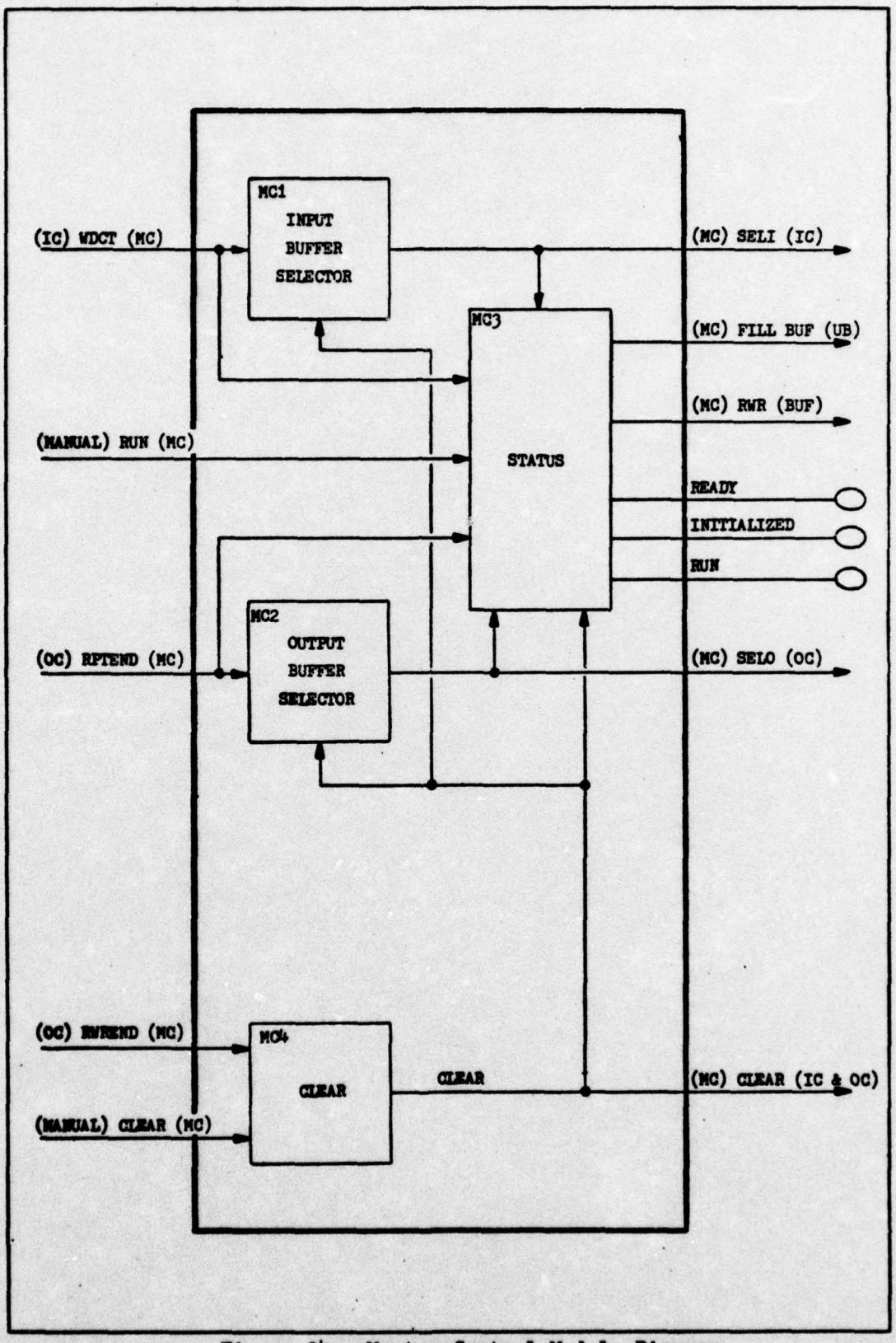

Figure 24. Master Control Module Diagram

(IC) WDCT (MC) indicates the buffer selected has been filled with the selected number of data words.

2. Output Buffer Selector (MC2). This unit makes the selection of which buffer will output data from BUF. MC2 is identical in construction and operation to MC1. The control signal is (OC) RPTEND (MC) which changes MC2 output at the end of repeated line sequence.

3. Status (MC3). MC3 is the prime unit of the master control module. This unit generates the status signal (MC) FILLBUF (UB), the READY signal, the INITIALIZED signal, the RUN signal, and the rewrite signal (MC) RWR (BUF). In order to generate these signals, MC3 uses CLEAR, SELI, SELO, (MANUAL) RUN (MC), (IC) WDCT (MC), and (OC) RPTEND (MC). MC3 incorporates two "buffer empty" flip-flops (JK negative-edge-triggered flip-flops with preset and clear) for keeping the status of each buffer. These flip-flops are manually cleared immediately after power up or automatically after writing a frame (to indicate that buffer #1 and buffer #2 are empty) which provides a FILLBUF status until both buffers #1 and #2 have been filled.

The OR of the flip-flop outputs (#1 FILL or #2 FILL) is ANDed with the RUN signal (output of a run switch debouncer) to provide the status signal (MC) FILLBUF (UB) -- a request for the PDP-11 to transfer out a block of data. The complements of #1 FILL and #2 FILL provide the (MC) $RWR_{1,2}$ (BUF) signals, i.e., a buffer is selected for a rewrite input when it is not selected for filling (receiving new data).

The "buffer empty" flip-flops are set (select buffer for rewrite) with a signal which is (IC) WDCT (MC) ANDed with the SELI

signal from MC1. After being set, the flip-flops are cleared (select buffer for fill) with a signal which is (OC) RPTEND (MC) ANDed with the SELO signal from MC2. This alternate setting and clearing of the "buffer empty" flip-flops corresponds to the steps described by the sequence of operations at the beginning of the master control module description.

The INITIALIZED signal is also output by MC3. It is generated simply by ANDing the (MC) $SELI_1$ (BUF) and (MC) $SELO_1$ (BUF) signals from MC1 and MC2. In addition, two JK master-slave flip-flops generate a signal which, when ANDed with INITIALIZED, provides the READY signal. These flip-flops are wired such that when (MC) $SELI_1$ (BUF) has gone high and back low one time (and one time only) after CLEAR, the READY signal will be high. INITIALIZED and READY indicators both on will indicate that the interface has properly accepted data into both buffers and is waiting for data to be read from memory.

4. Clear (MC4). MC4 incorporates a self resetting divide by 500 down-counter which will generate a pulse at the end of the frame, i.e., after 500 (OC) RWREND (MC) pulses. These frame end pulses are ORed with a manual generated clear pulse (MANUAL) CLEAR (MC) to provide CLEAR, which is used throughout the interface as previously described.

Digital to Analog Converter (D/A)

The D/A converter is a 6 bit very fast (24 nsec maximum settling time to $\frac{1}{2}$ LSB) resistor type converter which drives the EBCE directly. The EBCE has an adjustable gain for the analog input which negates any requirement for signal amplification as part of this design. The D/A power and connection requirements are contained in Appendix C. Note that this D/A converter is a part of the interface design. It

is not the DEC D/A unit which is part of the PDP-11 system and is not used in this design.

PDP-11 Unibus Interface (UB)

The unibus interface is made up of three separate standard DEC units. The module diagram is shown in figure 25, and the detailed wiring diagram is contained in Appendix C.

Unibus Receiver (M784). This unit consists of 16 inverting bus receivers on a plug in card which is compatible with the PDP-11 backplane. The output of these receivers is positive logic, and they may be connected directly to the interface data input lines.

Unibus Driver (M783). This unit consists of 12 bus drivers to be used as an input interface to the PDP-11 unibus. The input to these drivers is positive logic, and they may be connected directly to the interface. Information is gated through the drivers by a single enabling gate which must be high for transfer. For this design only one driver will be used to input the status information (one bit).

Address Selector (M105). The M105 is used to decode the UNIBUS Address and Control lines. In this design the M105 will respond to an address, which is jumper wire selectable, to either indicate a transfer of information (data) in or a transfer of information (status) out. The logic required to use the M105 control information for moving data to the interface is presented in the Input Control section of this study. To transfer status information from the interface, the decoded address line from the M105 must be NAND gated with the M105 "IN" line and the NAND gate output tied directly to the M783 enabling gate.

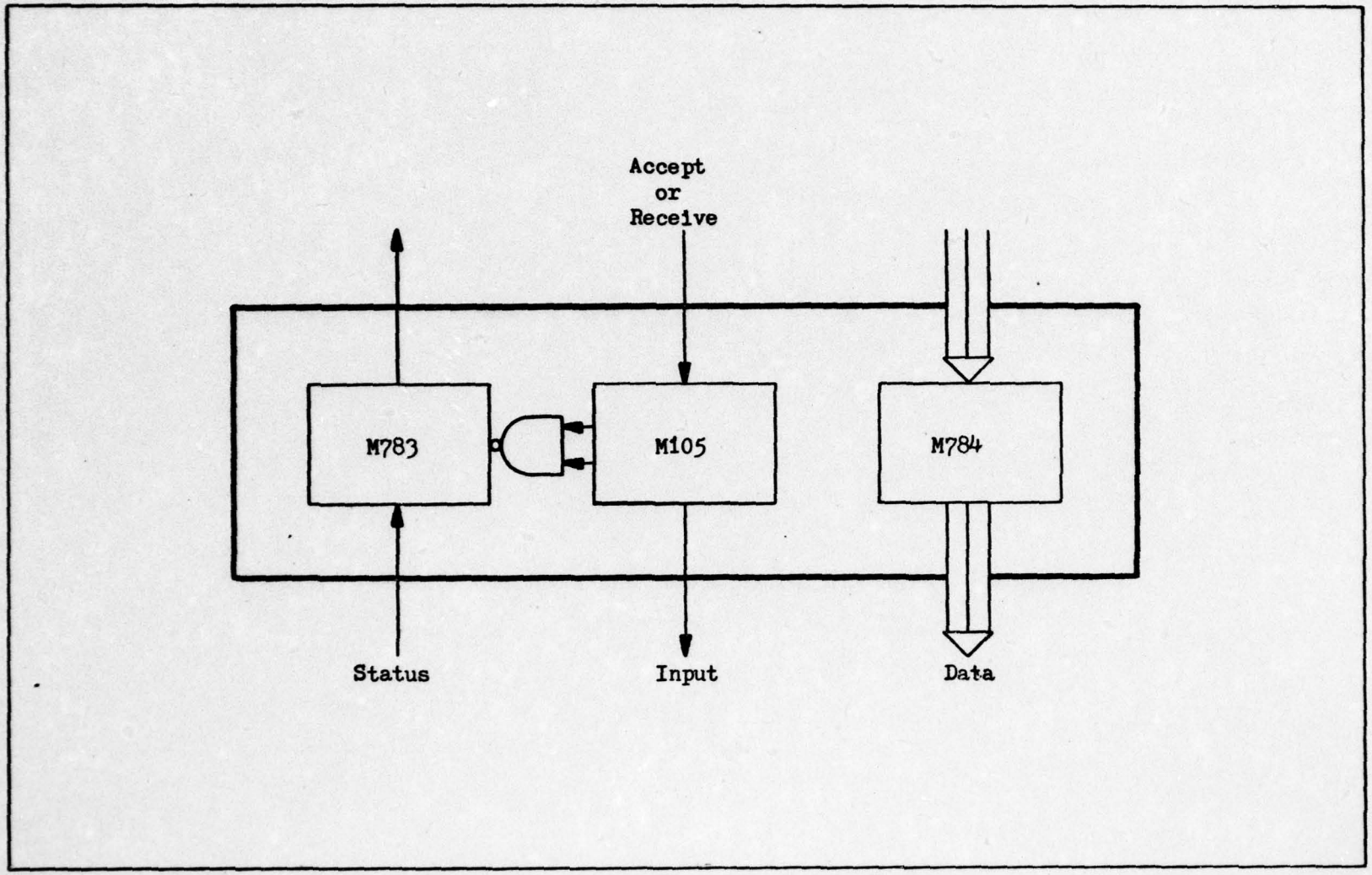

Figure 25. Unibus Interface Module Diagram

IV. Conclusions

The purpose of this chapter is to summarize the design process. It will also include recommendations concerning further expansion or improvement of the design.

Design Summary

The design process began with the definition of the problem and relevant background information. The specifications and constraints were presented, and the approach to be taken was then established. In the system organization chapter, additional design requirements and the software algorithm were established. This resulted in choosing the type of memory (FIFO) early in the design process. The FIFO choice then allowed definition of the required control system and its operation to obtain the desired phase plate matrix configuration. After defining the software algorithm, the overall design was presented in terms of block modules. The module designs were then presented at the next level of ovservation in terms of module units. These units were examined and implemented in terms of the unit tasks to be accomplished and all the information paths were expanded in detail.

The major problem that was addressed throughout the design was timing. This was manifest in terms of available time to accomplish the defined system tasks and in terms of signal synchronization. The long range desired modulation rate (10^9 elements/sec) is clearly beyond the output rate capability of the processor equipment available for this project. Although the maximum throughput rate of the designed

interface is slightly higher than the 1.45×10^6 elements/sec (100 x 100 matrix written in .069 sec) used in this study, no exact calculations were performed to define the absolute maximum. Rough calculations indicate that the system may provide (with minor changes) a "glitchless" performance approaching 2×10^6 elements/sec. The constraints which prevented use of DMA appear to degrade the PDP-11 transfer rate by a minimum factor of two to possibly as high as twenty, depending on design utilization.

The use of a dual buffer system in the buffer module memory provides a means of effectively doubling the interface throughput. The use of 8 bit bytes also provides the same advantage. Recent advances in economical D/A converters were an aid in minimizing the delay time between EBCE unblank and the analog signal output. The converter selected has the capability of 12-24 nsec conversion time, depending on the load. The use of a 6 bit D/A converter contributes some loss of generality to the 8 bit data word used up to this point, but this poses no problem as only 6 bits of the 8 bit word carry any information. If more accuracy is desired later, an 8 bit converter may be substituted with no other changes required.

In some cases it was necessary to use logic circuits which were more complex than anticipated. One such example is the read gating circuitry of OC2. It would have been desirable to start generating read pulses upon unblank instead of gating another pulse string. This would have eliminated any unblank to analog modulation timing uncertainty or delay. However, due to various design complexities a gating scheme was devised which only eliminated the uncertainty. The design introduced modulation information delays of up to one

complete cycle of OP2. For certain matrix size selections, this delay can be a major portion of the line sweep time.

Recommendations

1. The clock provided is not crystal controlled. Even though the design should be reasonably stable, it may be desirable to incorporate a crystal oscillator at some later time.

2. The design specifies for the D/A to drive the EBCE directly. It may be that interface to EBCE matching through an operational amplifier will prove necessary if D/A glitches are a factor or if D/A drive is inadequate. If so, care must be taken to use a high slew rate amplifier so as not to degrade discrete analog levels to a slowly varying voltage.

4. The gating configuration of OC2 can be modified to decrease the long read pulse delay following the unblank signal for small matrix sizes. This could be accomplished by counting a fast clock and generating pulses which correspond to counter outputs. This would require more logic and more counters than was considered appropriate for this study.

5. The master, output, and input control modules have a speed capability in excess of the buffer module due to the FIFO chosen. A random access memory (RAM) was an option early in the design process. For a faster system, the RAM would probably exhibit a speed advantage over the single package FIFO chosen for this design.

6. DMA would definitely help, but its use might require major changes of the input control module and the first three units of the buffer module.

7. A computer with faster I/O capability than the PDP-11 should be considered for any new interface system to be designed and used as a follow on to this study.

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Appendix A

ELECTRON BEAM CONTROL

ELECTRONICS TIMING DIAGRAM

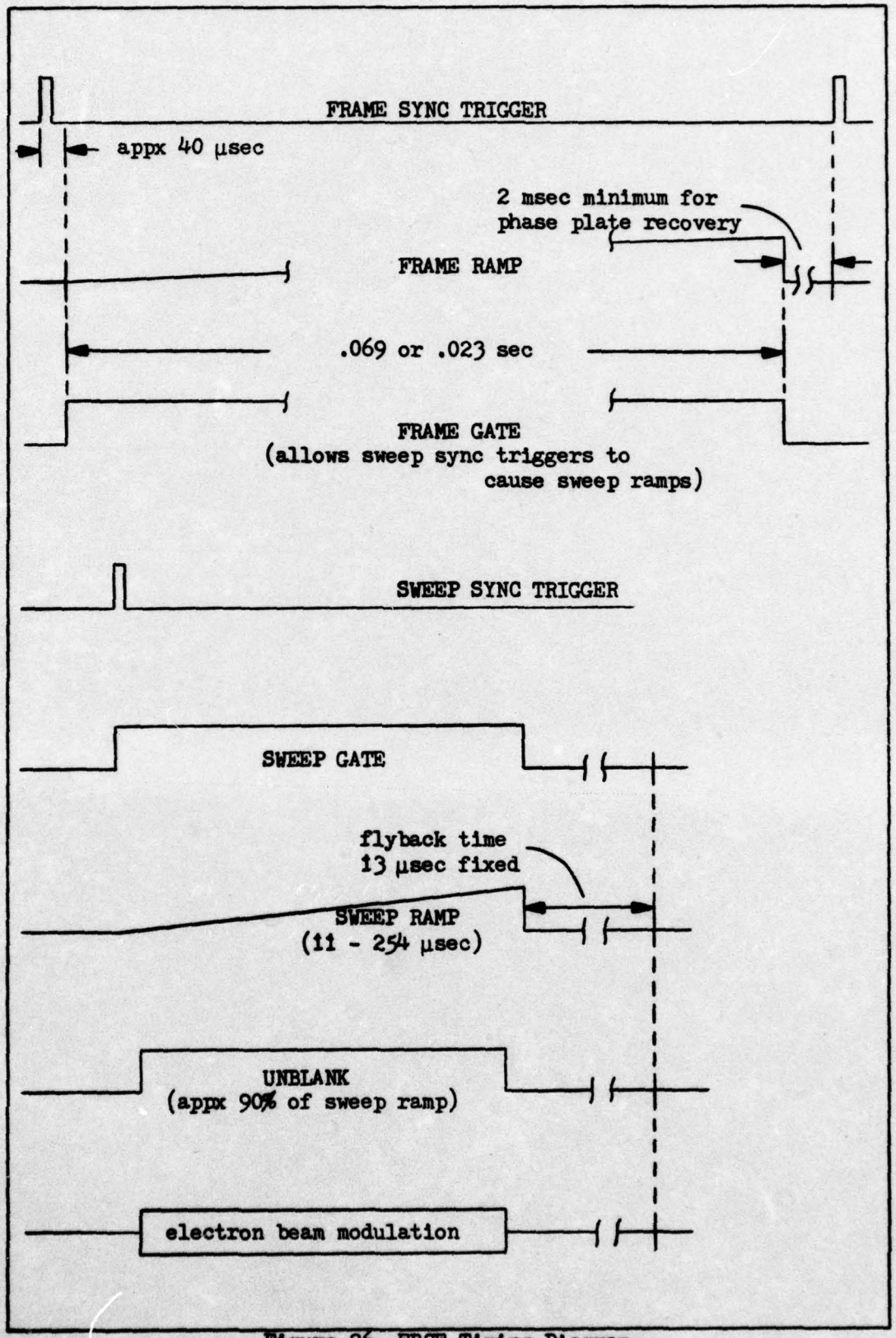


Figure 26. EBCE Timing Diagram

Appendix B

PDP-11 SAMPLE PROGRAM

PDP-11 Output Program

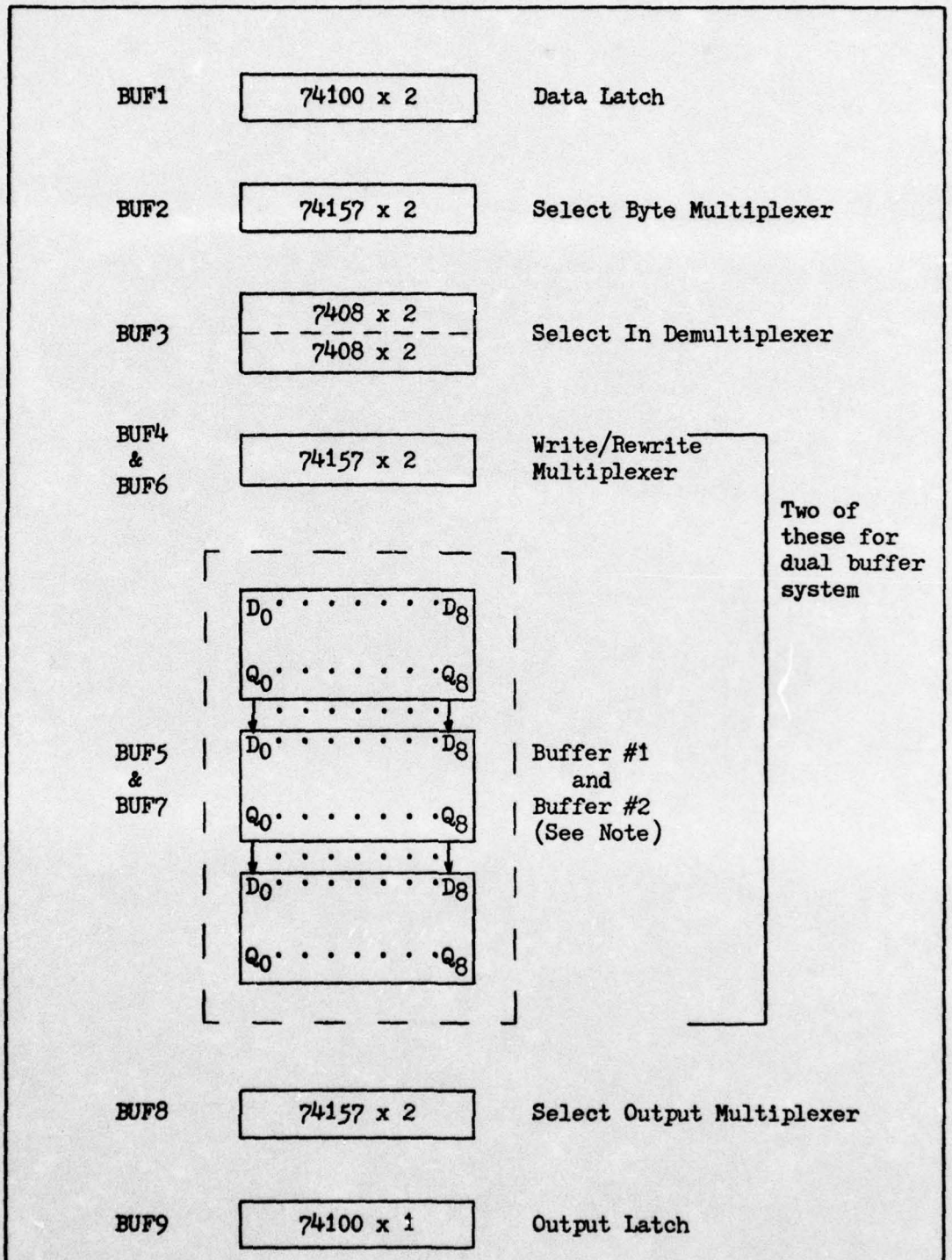
```
Load:   MOV #5000, RØ          ; LOAD ADDRESS OF FIRST
                                 16 BIT WORD (2 DATA POINTS)
                                 INTO RØ

        MOV (RØ)+, @#164000    ; MOVE FIRST WORD TO THE
                                 INTERFACE AND LOAD ADDRESS
                                 OF NEXT 16 BIT WORD INTO RØ
```

This instruction should appear in the program 'N' times

```
Check:  MOV @#176770, R1       ; MOVE CONTROL STATUS REGISTER
                                 INTO R1

        CMPB R1, #177          ; CHECK FOR DONE BIT (BIT 7
                                 OF STATUS WORD)

        BLE CHECK              ; IF DONE BIT NOT SET CHECK IT
                                 AGAIN

        BR LOAD                ; IF DONE BIT SET BRANCH TO
                                 BEGINNING OF OUTPUT PROGRAM
```

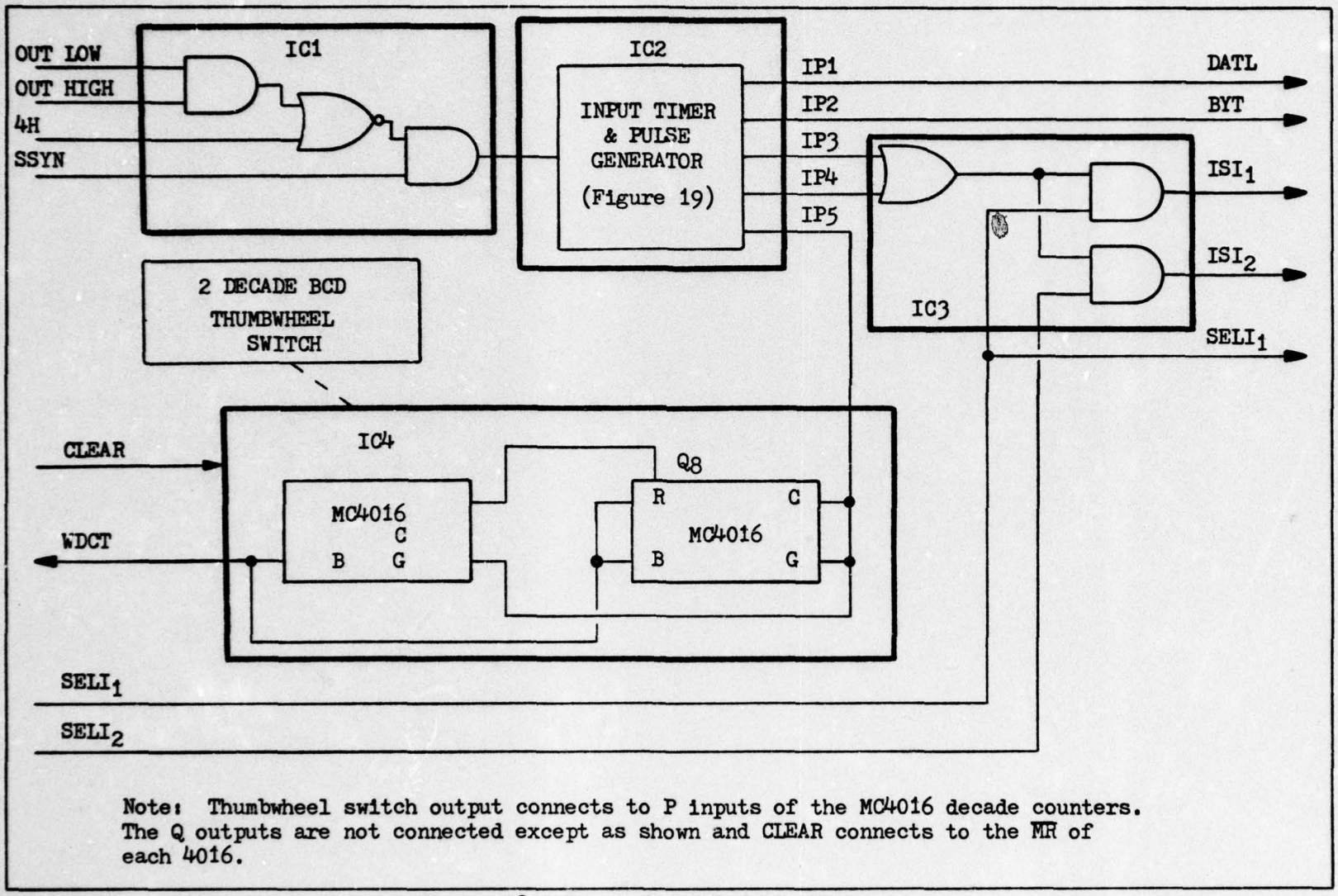
Appendix C

UNIT DIAGRAMS AND COMPONENTS



Note: Fairchild 33511 FIFO requires both +5 VDC and -12 VDC. All $\overline{OE}$ and $\overline{IE}$ inputs should be connected to ground (0 VDC) and IR output is not connected. FIFO expansion is as shown with outputs Q connected to inputs D. The 33511 is TTL compatible and can drive one TTL load.

Figure 27. Buffer Module Component Identification



Note: Thumbwheel switch output connects to P inputs of the MC4016 decade counters. The Q outputs are not connected except as shown and CLEAR connects to the $\overline{MR}$ of each 4016.

Figure 28. Input Control Logic Diagram

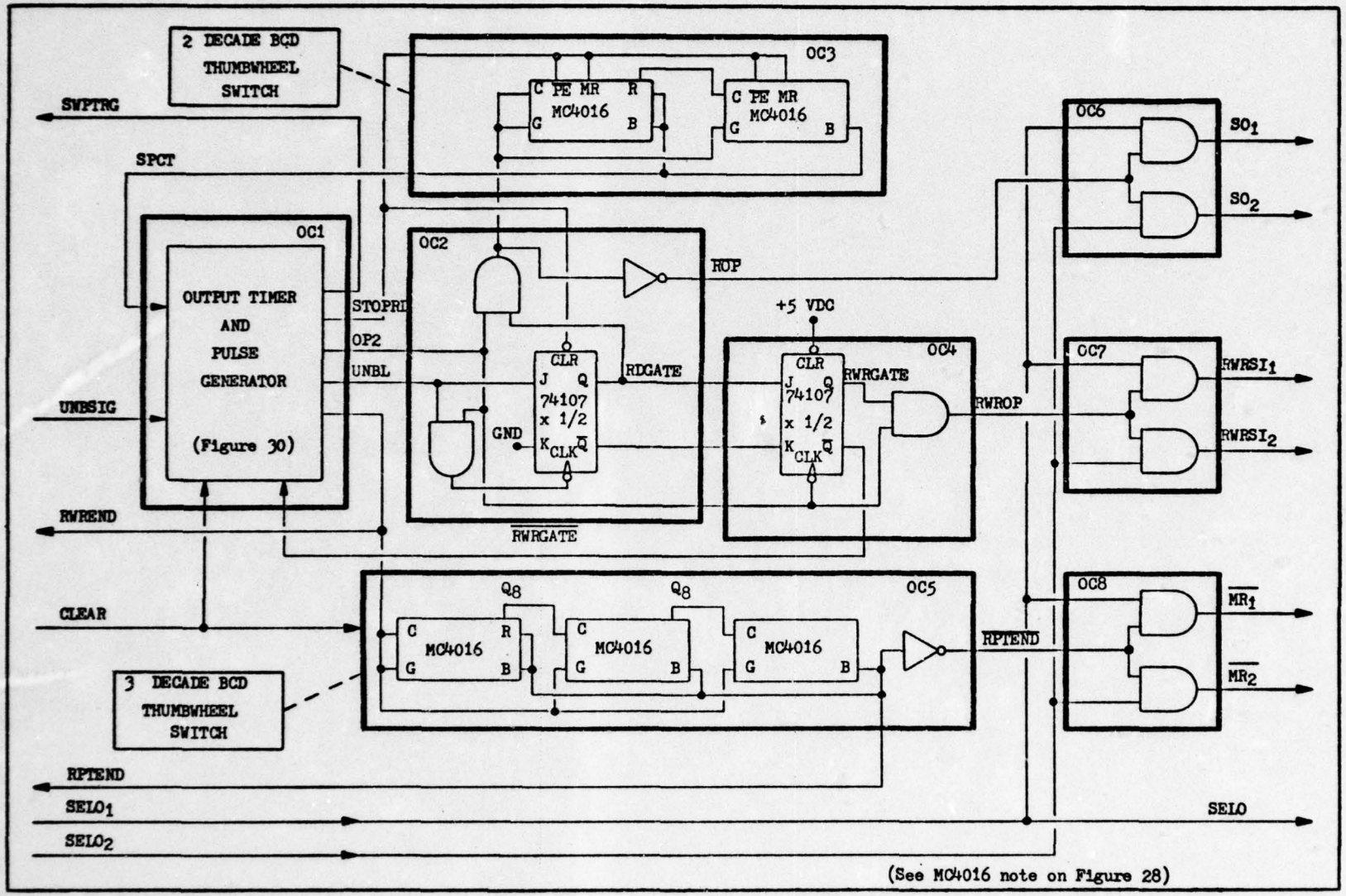


Figure 29. Output Control Logic Diagram

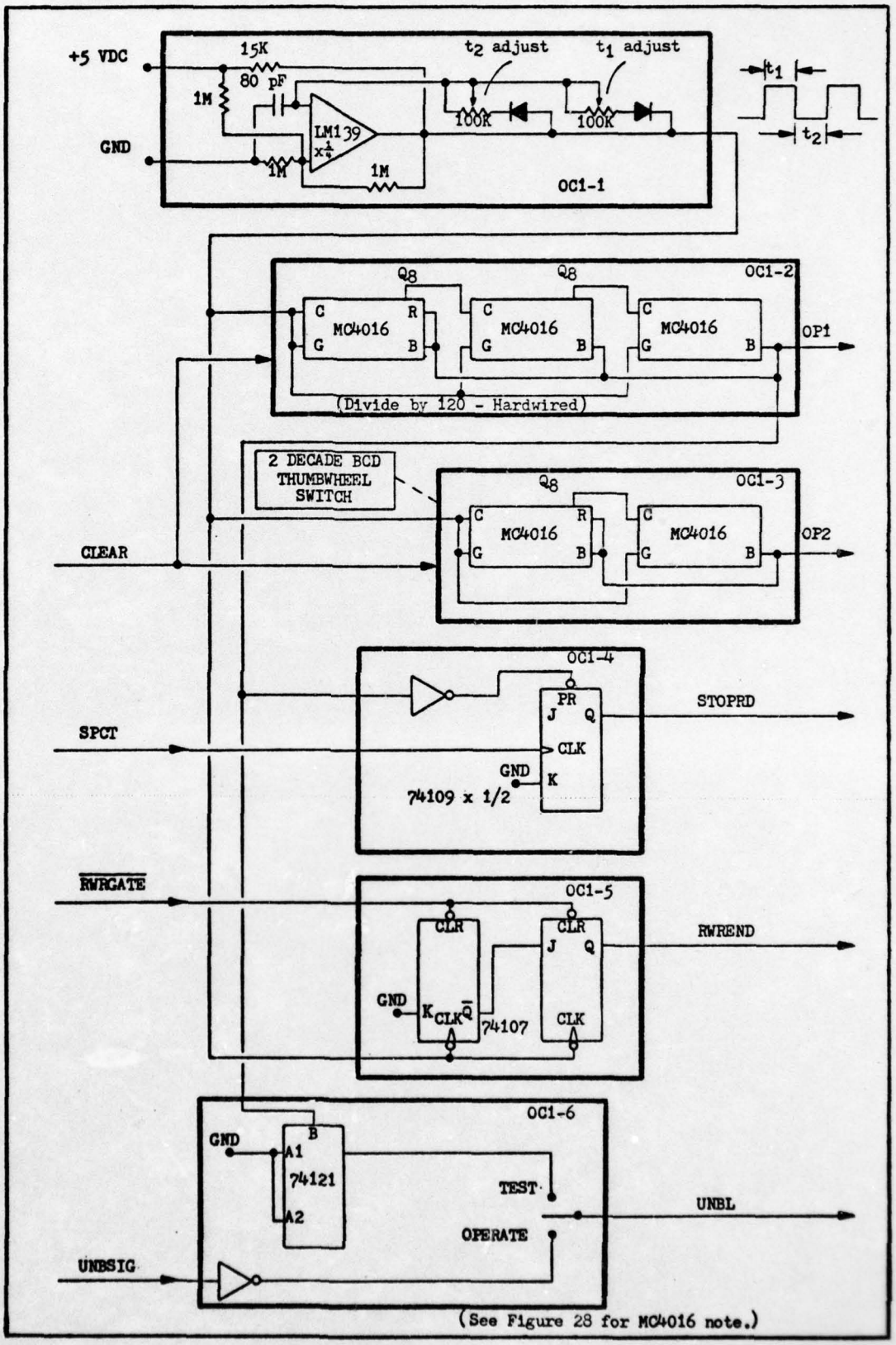


Figure 30. Output Timer and Pulse Generator Logic Diagram

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PDP-11/05 TO ELECTRON BEAM INTENSITY MODULATION UNIT INTERFACE.(U)
DEC 76 J R CROWDER

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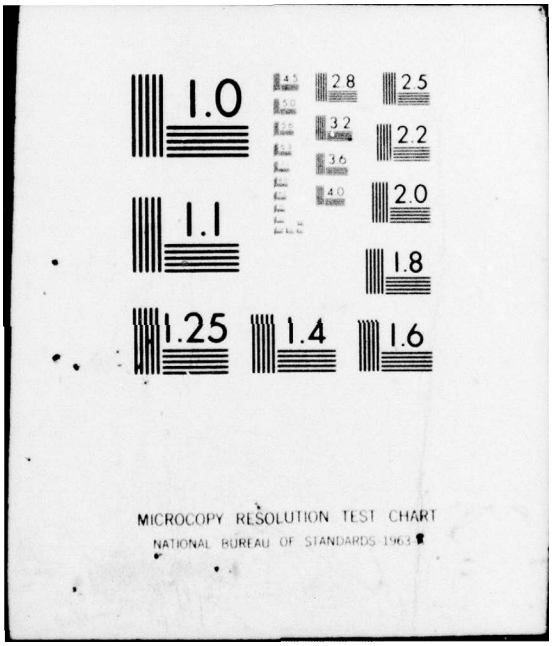
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MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963

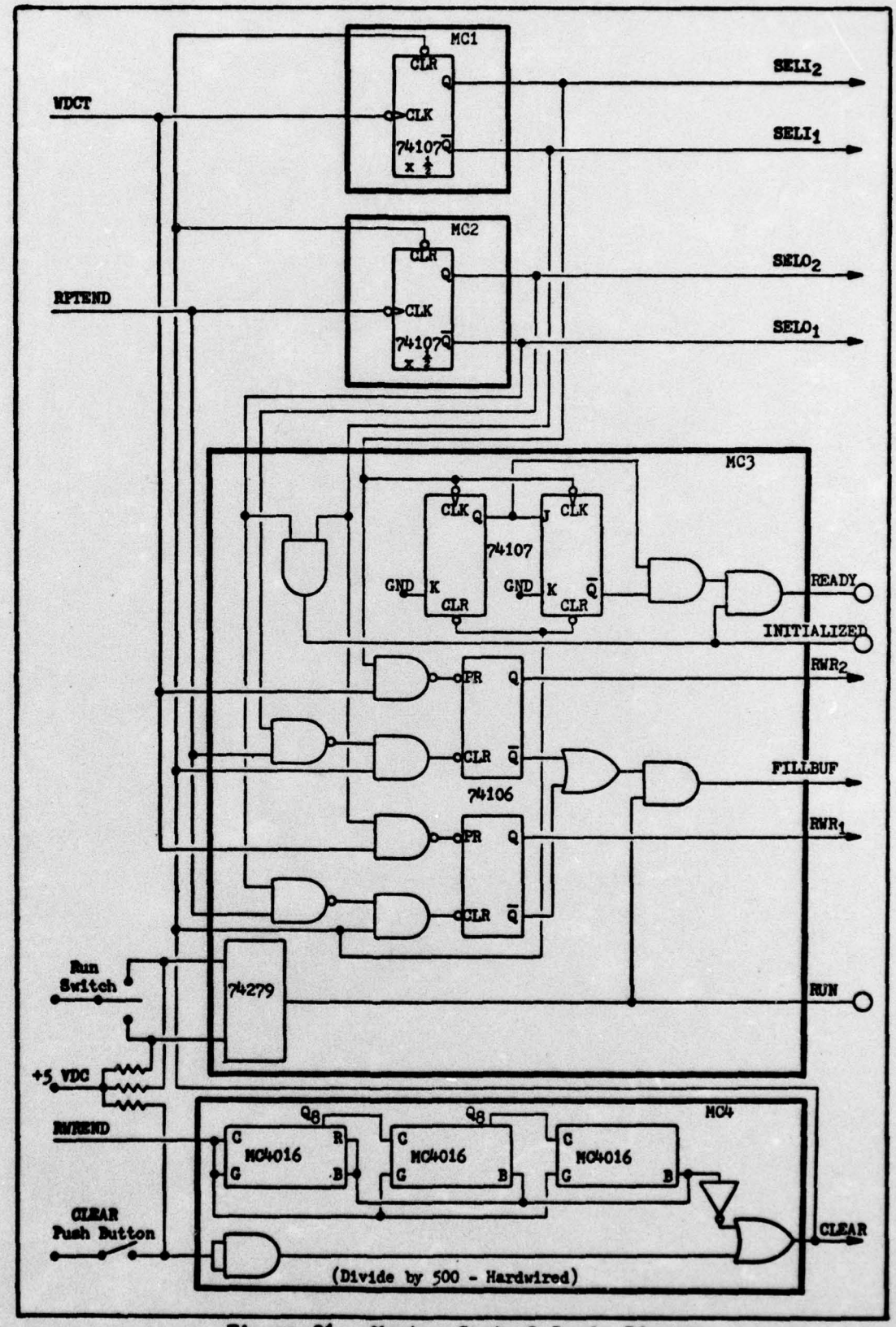
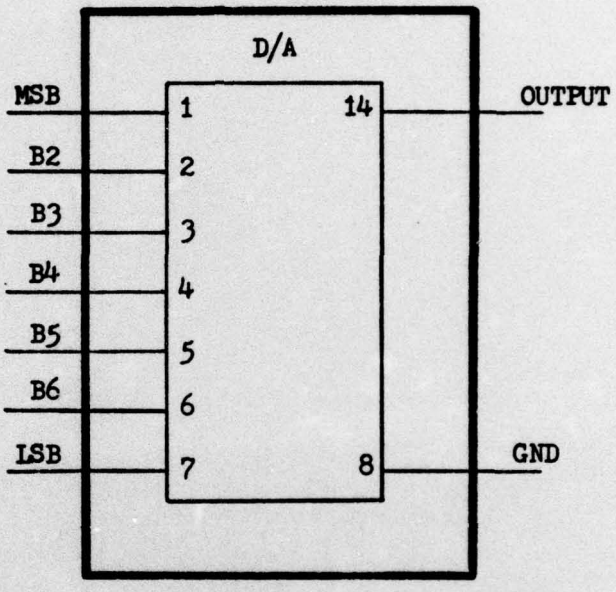


Figure 31. Master Control Logic Diagram



Note: The connections shown are for Optical Electronics Inc.'s Model 7461 D/A converter. There are no connections to pins 9-13. Notice that there are no external power requirements. The output may be connected to the input of an operational amplifier if desired.

Figure 32. D/A Power and Connection Requirements

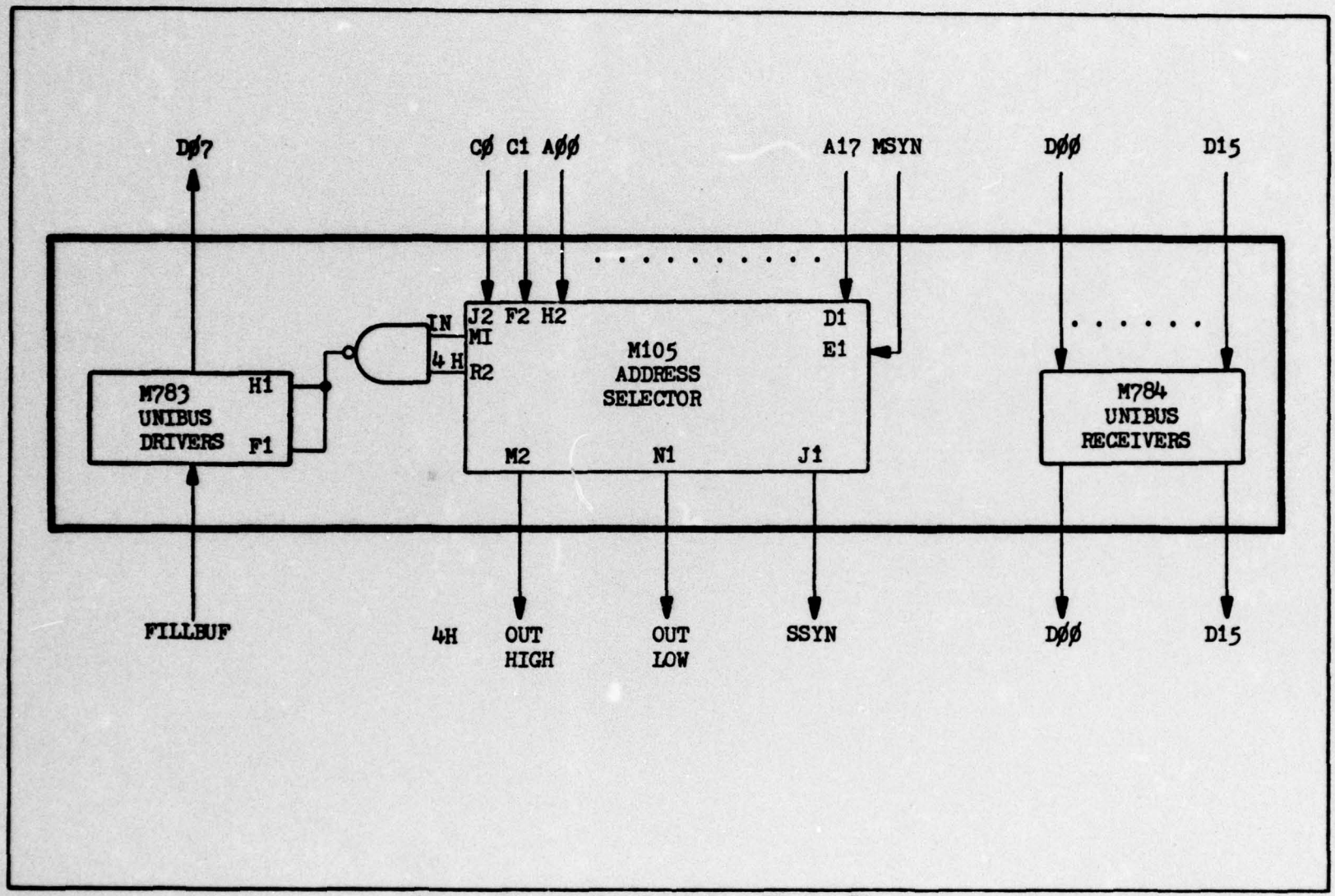
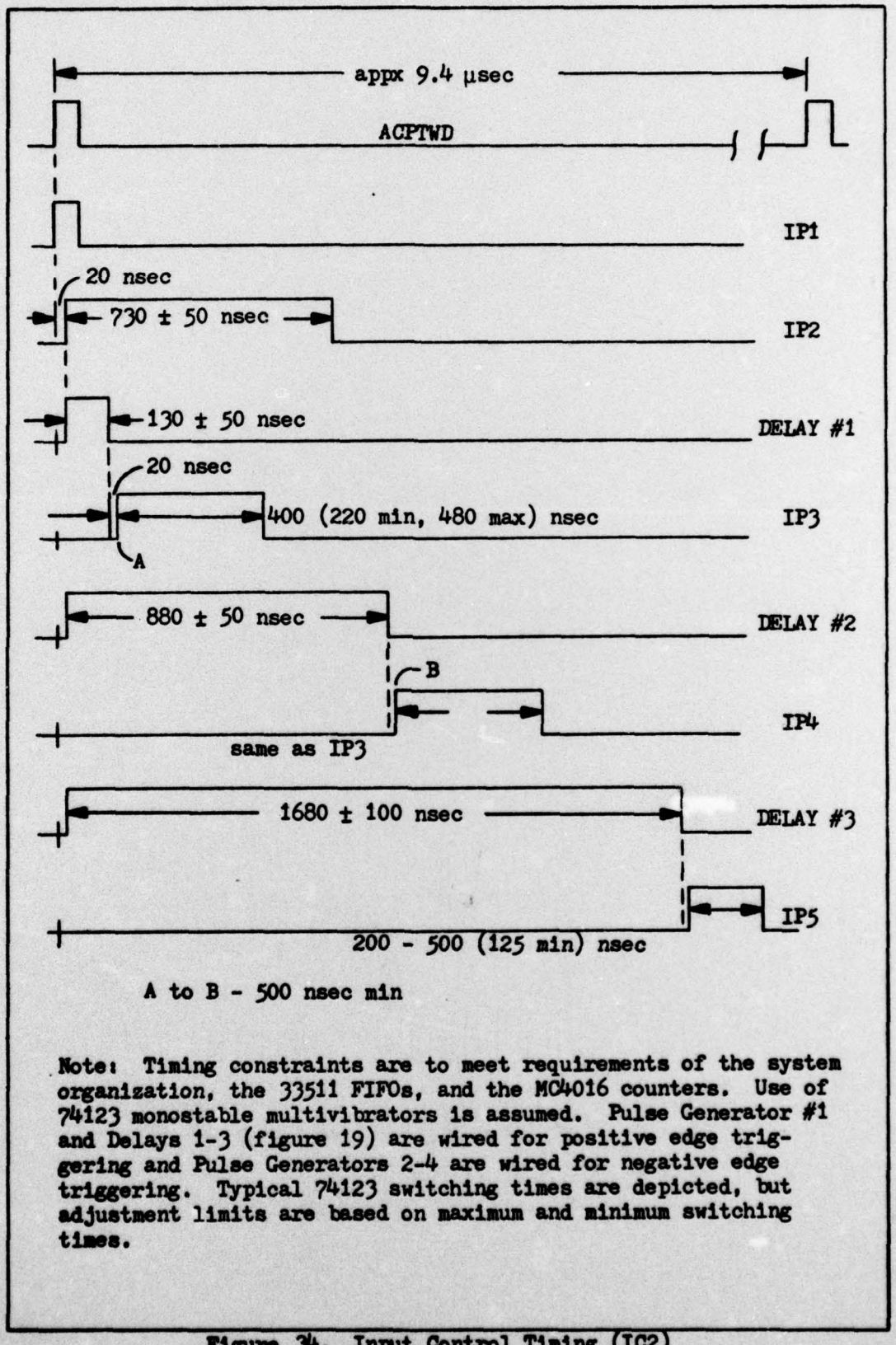


Figure 33. Unibus Interface Wiring Diagram

Appendix D

INTERFACE TIMING DIAGRAMS



Note: Timing constraints are to meet requirements of the system organization, the 33511 FIFOs, and the MC4016 counters. Use of 74123 monostable multivibrators is assumed. Pulse Generator #1 and Delays 1-3 (figure 19) are wired for positive edge triggering and Pulse Generators 2-4 are wired for negative edge triggering. Typical 74123 switching times are depicted, but adjustment limits are based on maximum and minimum switching times.

Figure 34. Input Control Timing (IC2)

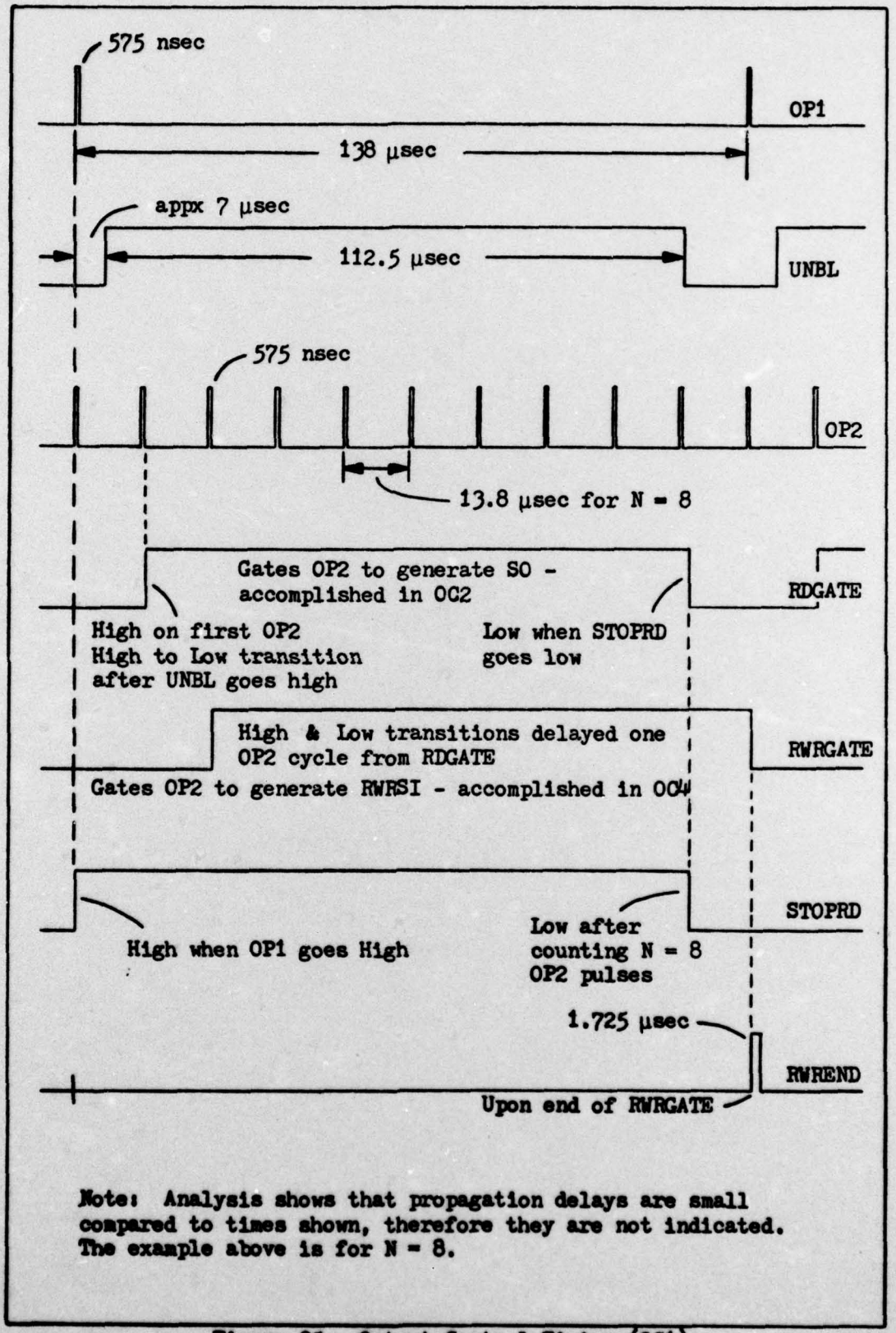


Figure 35. Output Control Timing (OC1)

VITA

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The result of this investigation is a design for an interface system which can be used to interface a Digital Electronic Corporation PDP-11/05 minicomputer with electron beam control electronics (EBCE). The EBCE is part of a deformable thermoplastic phase plate brassboard used for optical phase modulation in the Air Force Avionics Laboratory (AFAL/DHO).

The interface is a modular design made up of a unibus interface, buffer, input control, output control, master control, and a digital to analog (D/A)

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converter. The buffer module uses two first-in-first-out (FIFO) buffers to alternately accept data from the PDP-11 and send data to the EBCE via the D/A converter. The 16 bit word of the PDP-11 is multiplexed into 8 bit data words for interface manipulation, since 8 bits offer adequate resolution for the EBCE.

The interface is designed to allow writing of a 100 x 100 element matrix on the phase plate. This requires a 1.45 element/sec modulation rate of the analog signal sent to the EBCE. The use of a dual FIFO system, a multiplexed computer word, and a very fast D/A converter make this modulation rate possible.