CHARGE-COUPLED SCANNED IR IMAGING SENSORS

RCA Laboratories, Princeton, New Jersey

September 1976

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CHARGE-COUPLED SCANNED IR IMAGING SENSORS

RCA Laboratories

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The design of the 25 x 50 area array is nearly complete, and masks will soon be ordered. Arrays of this design will be made with both Pd_2Si and PtSi Schottky barriers. There will be optional masks for guard rings and for buried-channel operation. Processing has begun on a batch of wafers with Pt using the old masks, to give us some experience with Pt. Optical absorption measurements revealed a possible problem

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in the processing procedure, and an appropriate change was made. Infrared calculations were made demonstrating that thermal imaging with PtSi is possible, but that excess dark current at the detectors must be avoided.

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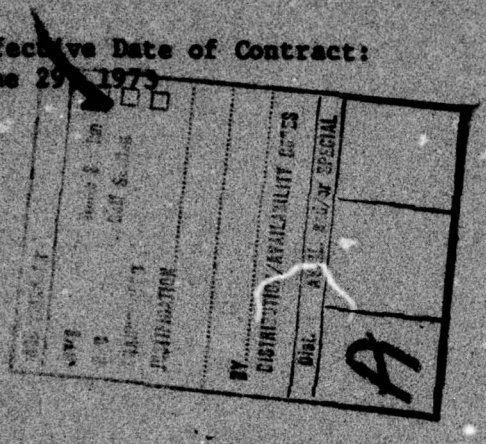

This report has been reviewed by the RADC Information Office (OI) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

This technical report has been reviewed and is approved.

SVEN A. ROOSILD
Contract Monitor

PREFACE

This Technical Report was prepared by RCA Laboratories, Princeton, New Jersey, under Contract No. F19628-73-C-0282 and ARPA Order No. 2444. It describes work performed from 1 November 1975 to 30 April 1976, in the Integrated Circuit Technology Center, J. H. Scott, Director. E. S. Kohn is the Principal Investigator and the Project Supervisor is K. H. Zaininger. Other members of the Technical Staff who participated in the research were: W. F. Kosonocky, P. A. Levine, J. Carnes, F. Shallcross, and G. Meray.

The manuscript of this report was submitted by the author on June 1976. Publication of the report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

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The vertical grid lines in Figs. 1,2, and 3 refer to a wave-number scale and should be ignored.

I. INTRODUCTION

A program is under way to fabricate infrared-sensitive, charge-coupled imagers with Schottky-barrier detectors. Our previous work has been with three-phase, single metallization line arrays using palladium-silicide, Schottky-barrier detectors. The present effort is directed at fabrication of a 25 x 50 area array. We will use platinum-silicide detectors which respond deeper into the infrared, and are therefore more sensitive to thermal images in the 300°K range. We have made calculations to predict the performance of these arrays, and they are presented in Section II. Because of the relatively small signals predicted, we have expanded the mask set to provide buried-channel and guard-ring options. Infrared transmission measures which are important to the selection of processing techniques are described. We conclude with a detailed discussion of the circuitry for operating the area array.

II. INFRARED PERFORMANCE ANTICIPATED FROM SCHOTTKY BARRIER ARRAYS

The response of Schottky-barrier detectors to thermal radiation has been reported by Shepherd et al. [1], and by Kohn et al. [2], and is therefore only summarized here. The spectral radiance emitted by a thermal radiator per frequency increment is [3]

$$L_\nu = \frac{2h}{c^2} \times \frac{\nu^3}{(e^{h\nu/kT}-1)} \quad \frac{W}{m^2\text{-Sr-Hz}} \tag{1}$$

The spectral *photon* radiance is then

$$L'_\nu = L_\nu/h\nu = \frac{2}{c^2} \times \frac{\nu^2}{e^{h\nu/kT}} \tag{2}$$

The spectral *incidence* of photons is given by the same expression with the *background* temperature T_B in place of T. Thus, the number of carriers generated in a detector of area A in time t_s is given by

$$N_b = \int_{\nu_{ms}}^{\infty} \text{Q.E.}(\nu) \quad L'_\nu\ (\nu, T_b)\ A\ t_s \left(\frac{\pi}{4F^2}\right) d\nu \tag{3}$$

where Q.E. (ν) is the spectral quantum efficiency of the detectors, and the expression in parenthesis converts from steradians to focal ratio F. For Schottky-barrier detectors, the integral is taken from the cutoff frequency ν_s

$$\psi ms = \frac{h\ \nu_{ms}}{kT} \tag{4}$$

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1. F. D. Shepherd et al., "Silicon Schottky-Barrier Monolithic IR TV Focal Planes, "*Advances in Electronics and Electron Physics*, to be published.
2. E. S. Kohn, "A Charge-Coupled Infrared Imaging Array with Schottky-Barrier Detectors," IEEE Journal of Solid-State Circuits, SC-11, 139 (1976).
3. RCA Electro-Optics Handbook, 1974, p. 36.

to the cutoff of silicon, but little accuracy is lost taking it to infinity because the exponential turn becomes negligible. With the approximation

$$e^{h\nu/kT_b} \gg 1 \tag{5}$$

and with the expression for the quantum efficiency of a Schottky-barrier detector

$$Q.E. = \frac{C_1}{q} \frac{(h\nu - q\,\psi_{ms})^2}{h\nu} \tag{6}$$

$$N_b = \frac{\pi A\, t_s\, C_1\, k^4\, T_b^4}{q\, C^2\, F^2\, h^3} \left(\frac{q\,\psi_{ms}}{k\,T_b} + 3\right) \exp-\left(\frac{q\,\psi_{ms}}{k\,T_b}\right) \tag{7}$$

or

$$N_b = 2.7 \times 10^{10}\, A\, t_s\, C_1\, T_b^4\, (\mu_o + 3)\, e^{-\mu_o} \tag{8}$$

where

$$\mu_o = \frac{q\,\psi_{ms}}{k\,T_b} = \frac{11{,}609\,\psi_{ms}}{T_b} \tag{9}$$

All quantities are in mks units except C_1, the detector efficiency factor, which is reported in the literature in reciprocal electron volts. The first q in Eq. (6) accounts for this. The quantities are defined in Table 1. The values in the table are for our line array with PtSi Schottky barrier. With these values,

$$N_b = 3.36 \times 10^5 \text{ carriers} \tag{10}$$

Thus, the stored charge is

$$Q_b = q\,N_b = 1.6 \times 10^{-19}\ C \times 3.36 \times 10^5 = 5.4 \times 10^{-14}\ C \tag{11}$$

Table 1.

k	Boltzmann's constant	1.38×10^{-23} J/°K
q	Electron charge	1.602×10^{-19} C
c	Speed of light	3×10^{8} m/s
h	Planck's constant	6.626×10^{-34} J·s
A	Area of detector	$(2.8 \times 10^{-9}$ m$^2)$
ts	Storage time	30×10^{-3} s
C_1	Detector Q.E. factor	$(0.1$ eV$^{-1})$
T_b	Background temperature	(288°K)
F	Focal ratio of optics	(1)
ψ_{ms}	Schottky-barrier height	(0.275 eV for PtSi:p-Si)
C_{fd}	Capacitance of floating diffusion	0.5×10^{-12} f
L_ν	Spectral radiance	W(m^2-Sr-Hz)$^{-1}$
L'_ν	Spectral *photon* radiance	(m^2-Sr-Hz)$^{-1}$
N_b	Number of carriers created in detector in time Ts	(-)

The numbers in parenthesis are the values used in the first example.

The output signal is

$$V_b = Q_b/C_{fd}$$

$$= \frac{5.4 \times 10^{-14}}{0.5 \times 10^{-12}} \approx 0.1 \text{ V} \qquad (12)$$

This is only 1% of the well capacity; furthermore, practical considerations can reduce the signal still further. Some of these are shown in Table 2. Our imaging experiments were done with a 3.8 cm, f/1, coated Ge lens, so that only the window reflection losses apply. In the following calculation, we shall ignore this loss.

Table 2. Miscellaneous Optical Losses

	Transmission
2 IRTRAN II windows R = 15% per surface	0.52
F-2 system	0.25
Ge Lens R = 36%/surface	0.41

(The reflection losses can be reduced by optical coating.)

A 288°K background detected by PtSi Schottky barriers has 4.7% per °K contrast [1]. Thus, a one degree difference produces a signal of about 8000 carriers. The shot noise is on the order of 580 carriers. Other noise sources [4] are shown in Table 3. Thus, good temperature resolution is possible, but only if the electrical noise sources are kept to the theoretical limit. The margin can be improved with a longer integration time. One noise source not easily calculated is noise on *excess* dark current. This is best controlled by keeping the total dark current negligible. Calculated dark currents are shown in Table 4. All combinations appear acceptable except PtSi above 90°K. Guard rings may be necessary to prevent excessive dark currents.

4. J. E. Carnes and W. F. Kosonocky, RCA Review 33, 607-21 (1972).

Table 3. IR-CCD Thermal Response, Noise Sources, and Noise Equivalent Temperatures[a].

λc (μm)	3.54 Pd_2Si	4.5 (PtSi)	5.5
N_b (T_b)	2.0×10^4	3.4×10^5	2.6×10^6
γN_b (T_b)	1.2×10^3	1.7×10^4	9.5×10^4
N_b (T_b + 10°)	3.6×10^4	5.5×10^5	3.3×10^6
N_b (T_b + 100)	2.0×10^6	1.6×10^7	saturated
Shot noise - $\sqrt{N_b}$	1.4×10^2	5.8×10^2	1.5×10^3
Incomplete transfer noise-[b] $\sqrt{2\varepsilon N_g N_1}$	1.6×10^3	1.7×10^3	2.1×10^3
Fast Interstate trapping noise-[c] $\sqrt{1.4 N_g (kT/q) N_{SS} Ag}$	1.6×10^3	1.6×10^3	1.6×10^3
Floating diffusion reset noise- 200 $\sqrt{C_{pf}}$	200	200	200
Combination of above noise sources - $\overline{N_t}$	2.3×10^3	2.4×10^3	3.0×10^3
NEΔT from above sources	1.9°K	0.15°K	0.04°K
NEΔT from above sources and 1% nonuniformity	1.9°K	0.20°K	0.23°K

(a) Terms defined in Ref. 4.
(b) εN_g (transfer loss per gate times number of gates) from Ref. 5.
(c) N_{SS} was taken as 4×10^{10} cm^{-2} eV^{-1}.

5. E. S. Kohn, "Charge-Coupled, Scanned IR Imaging Sensors," AFCRL-TR-74-0375, July 15, 1974.

Table 4. Schottky-barrier Dark Current at Three Temperatures.

	Current density A/cm^2 and number of carriers	
λ_c (μm)	3.54 Pd_2Si	4.5 PtSi
77°K	2.4×10^{-18} (<<1)	4×10^{-13} (2)
90°K	5.9×10^{-15} (<<1)	2.0×10^{-10} (1049)
100°K	7.5×10^{-13} (4)	8.0×10^{-9} (4.2×10^4)

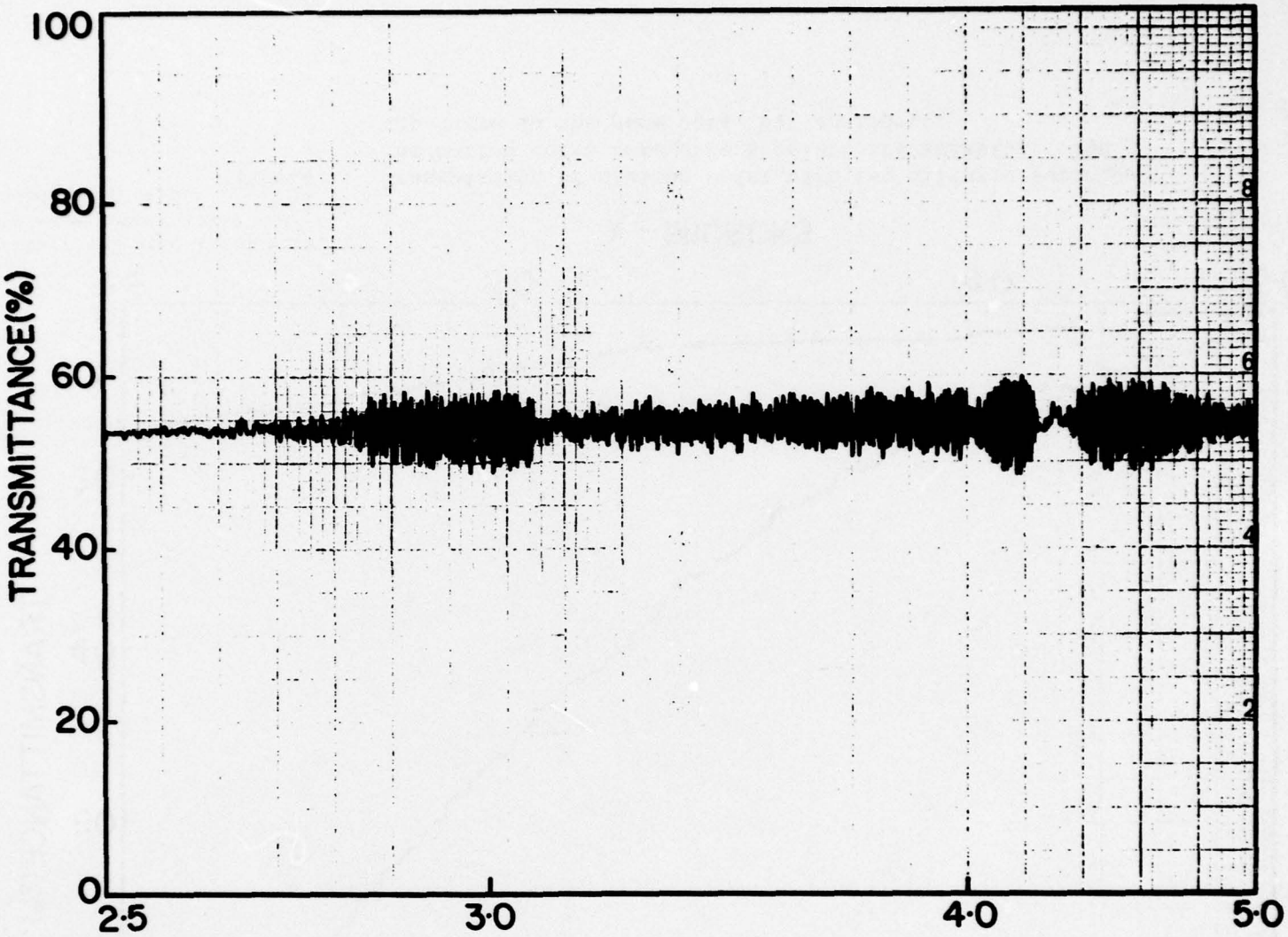
These values were calculated from the Richardson equation with $A^* = 32\ A/cm^2(°K)^2$ for holes in silicon [6]. The numbers in parenthesis represent the number of carriers accumulated in 30 ms in a detector of area $2.8 \times 10^{-5}\ cm^2$.

6. J. M. Andrews and M. P. Lepselter, Sol. St. Elec. 13, 1011-23 (1970).

III. OPTICAL TRANSMISSION OF SILICON WAFERS.

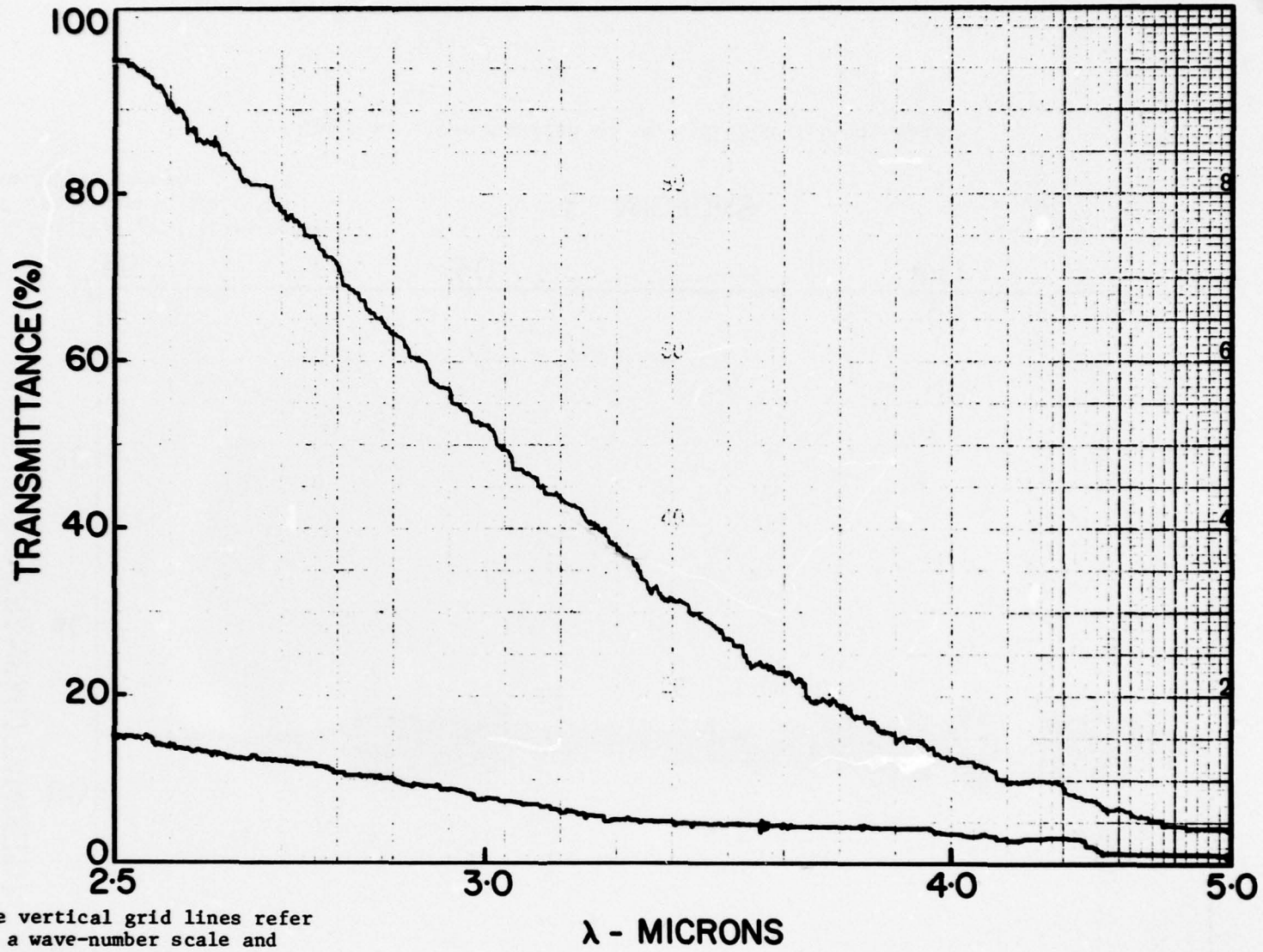
For our rear-illuminated infrared imagers the infrared transmission is critical. While pure silicon is transparent in the region of interest, free carrier absorption in doped regions can be significant, particularly at longer wavelengths. Our high resistivity p-wafers should not exhibit free-carrier absorption, but diffusions can. Certain diffusion processes used in our I.C. Center result in an n-type diffusion on the back of the wafer. In order to determine how harmful this is, we prepared samples with diffusions on both sides, and compared the spectral transmission on a spectrophotometer with that of an undoped wafer. The transmission of the undoped wafer is seen in Fig. 1 to be flat at 54%. This is accounted for by the two reflections (n = 3.45).

In Figs. 2 and 3, the lower trace is the absolute transmission. The upper trace is the same data scaled-up for clarity. Figure 2 shows the transmission for the diffused (both sides) wafer, beginning with 15% at 2.5 μm and dropping rapidly with wavelength. This is clearly not acceptable. Figure 3 shows the transmission of a wafer that was put through the "doped-glass" diffusion process. A protective oxide was prepared on the front side which would be patterned in a real device. The doped glass was deposited on this oxide, and the wafer was then subjected to the drive-in heating cycle. The transmission is shown in Fig. 3. No unusual absorption is seen. The fine structure is caused by the oxide which would not be in the transmission path in a real device.



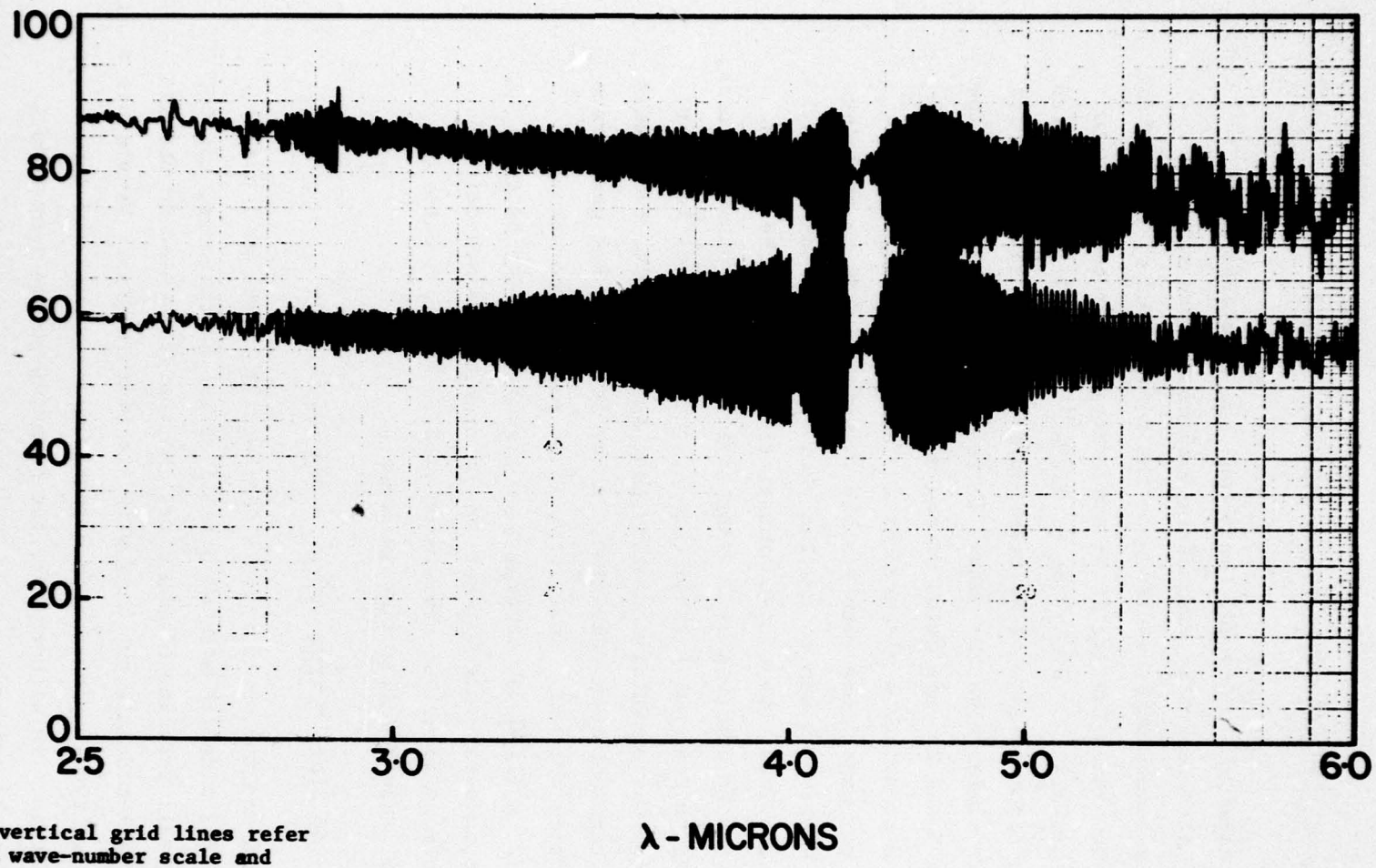
The vertical grid lines refer to a wave-number scale and should be ignored.

Figure 1. Transmission of μm-diffused silicon wafer.



The vertical grid lines refer to a wave-number scale and should be ignored.

Figure 2. Transmission of silicon wafer with two diffused surfaces. The bottom curve refers to absolute transmission. The top curve in the same data, but scaled-up.



The vertical grid lines refer to a wave-number scale and should be ignored.

Figure 3. Transmission of wafer diffused by doped-glass process. The bottom curve refers to absolute transmission.

IV. ELECTRICAL OPERATION OF THE AREA IMAGER

When the line imager was operated, the output was displayed as an oscilloscope trace. All electrical parameters including clock rate and integration time were continuously variable on the front panel of the control box. For the two-dimensional imager, it is not practical nor desirable to build in this much flexibility. Since the output will normally be displayed as a TV picture, the clock rates must be selected to suit the frame time for the number of picture elements on the chip. It is not practical to vary the clock rate since the X and Y sweep rates of the display would have to be simultaneously varied to maintain picture size. This is an unnecessary complication, since our experience with visible imagers permits us to select a suitable format. We have chosen to run the chip (and hence, the display) at a 60 Hz-frame rate. Thus, the *minimum* integration time will be 1/60 s. Longer integration time is achieved by leaving additional time between frames, but the time required to read out a frame (hence, the clock rate) is never changed. We determine the additional time by continuing to count the master clock even after a frame has been completed, and by beginning the next frame when the preset count is reached. Thus, it will be possible to set the integration time to 2^n x (1/60) s, ranging from (1/60) s to many seconds. At 1/60 s there will be no observable flicker in the display. A standard TV monitor has a 60-Hz frame rate, but scans each line in 64 μs, a value not easily changed. Our preferred line time is about

$$\frac{1}{60}\ \text{s} \div 50\ \text{lines} = \frac{1}{3000}\ \frac{\text{s}}{\text{line}} = 333\ \mu\text{s}.$$

The use of a standard monitor would require the C-clock to run at 1 MHz, a value somewhat fast for a device with an 0.8-mil gate. Furthermore, the CRT would be on only a small fraction of the time. We therefore plan to use an X-Y oscilloscope, and Z-modulate the beam with the video signal. We can use a Tektronix 536 with two type-T plug-ins or a standard scope with our own sweep generator for the Y axis. In either case, the blanking pulses generated in our circuitry provide the triggering.

A block diagram of the drive circuitry is shown in Fig. 4. The transfer scheme used by our interline 25 x 50 chip was discussed in the previous report,

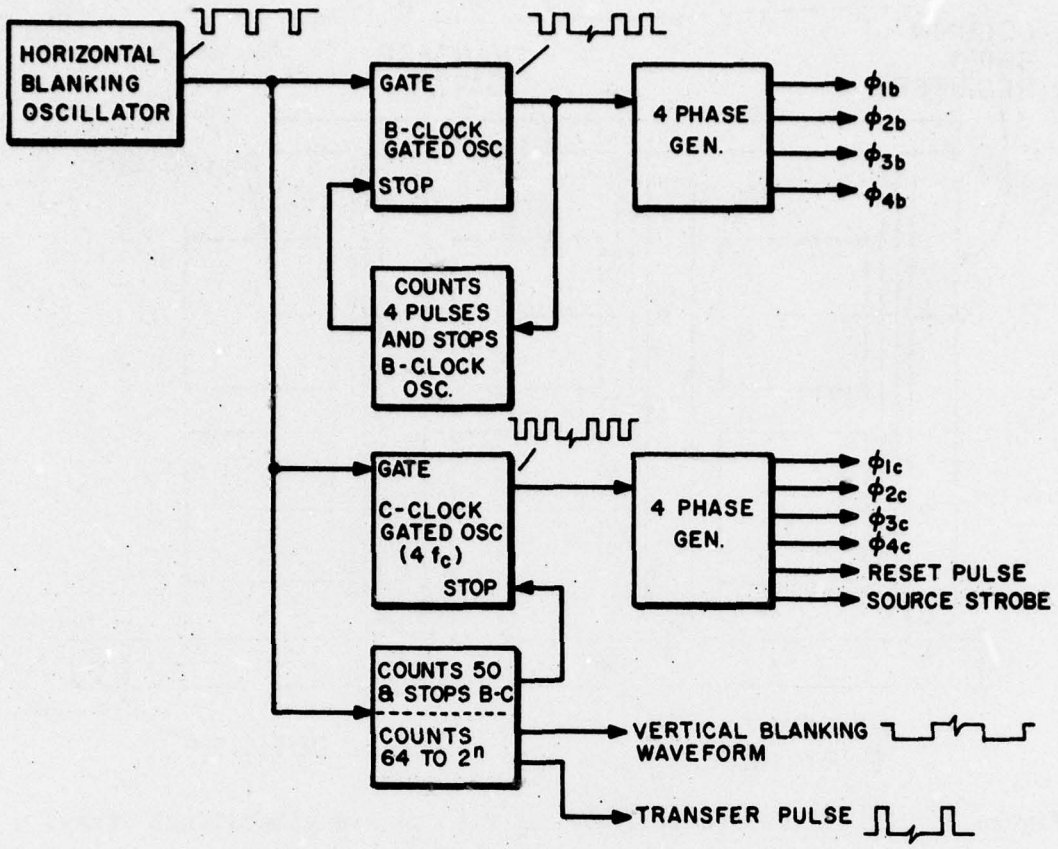


Figure 4. Block diagram of drive circuit.

and is repeated in Fig. 5. The detectors all load simultaneously into phase-1 gates of the B-registers upon application of a transfer pulse. (The phase-1B gates must be on at this time.) The B-register gates are then clocked down by 1 bit, loading the signals originating from the lowest row of detectors into the phase-1 gates of the C-register. (These phase 1-C gates must be on at this time.) The four B-register waveforms are shown in Fig. 6. This sequence is called "double-clocking" because two of the four gates are always on. In our case, phases-1 and-2 are normally on, except during the B-to-C transfer, as shown in Fig. 6. The C-register is also double-clocked, as shown in Fig. 7. Phases 1-C and 2-C are on when the C-register is stopped, to accept the B-to-C transfer. Also shown are the waveform S1, used to strobe the C-register input diffusion for charge presetting, and the waveform required by the reset gate.

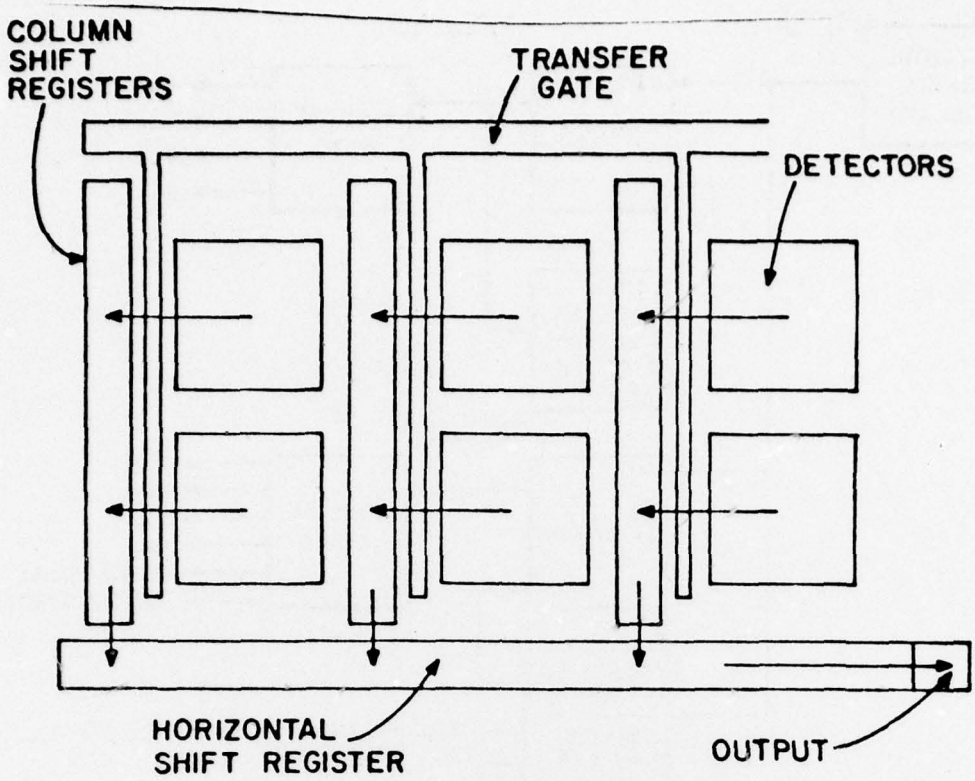


Figure 5. Interline transfer scheme for the two-dimensional array.

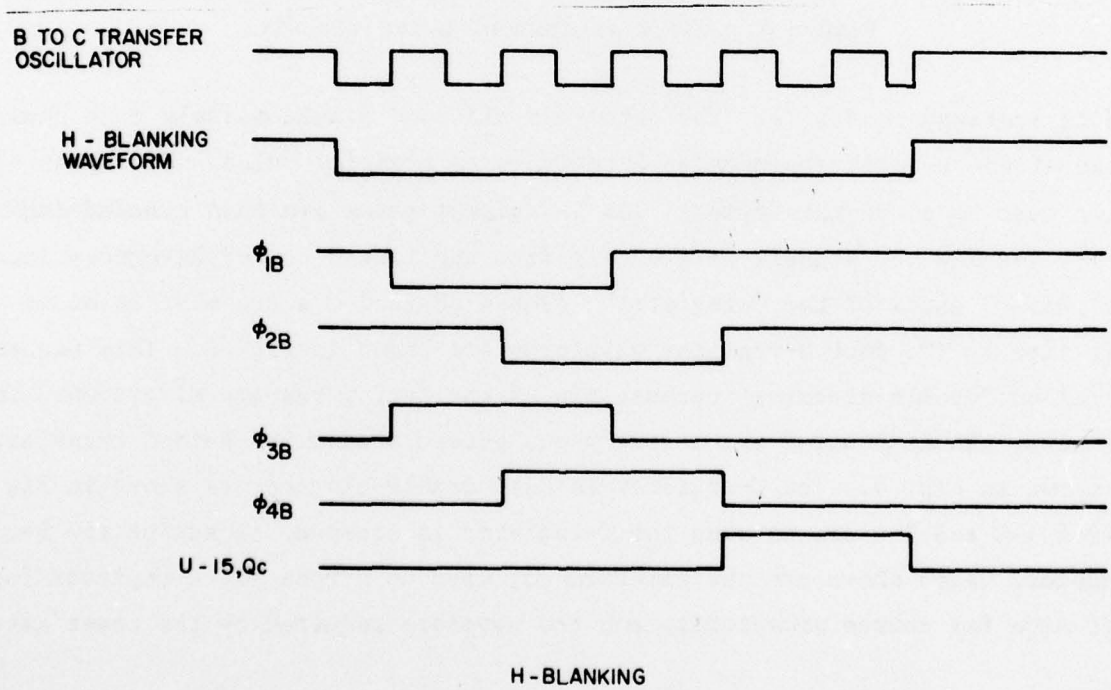


Figure 6. B-register waveforms during B-to-C transfer.

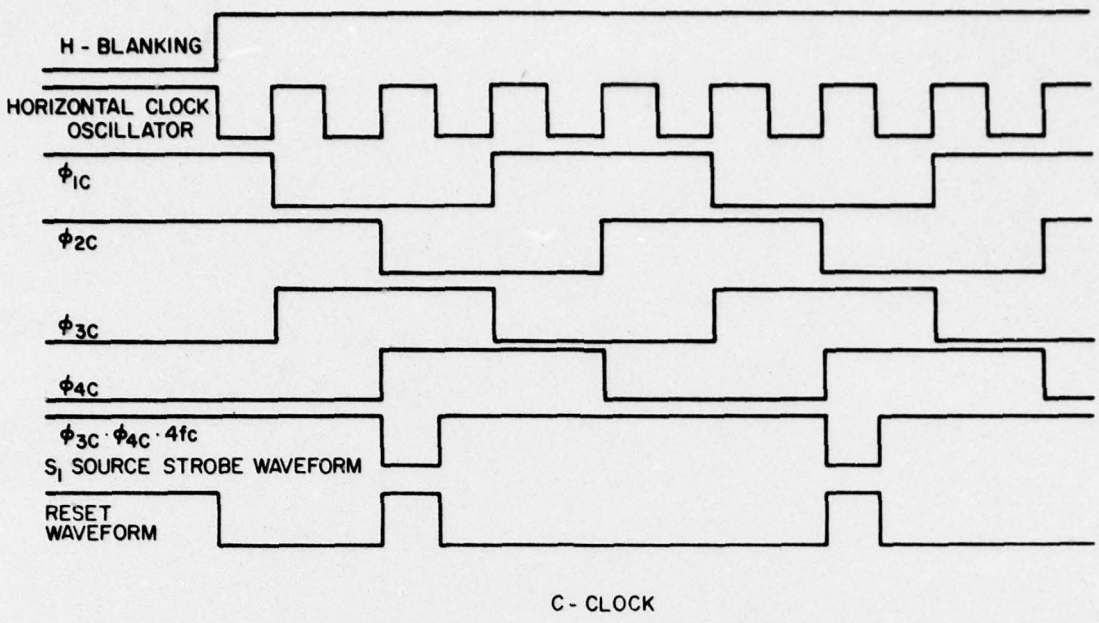


Figure 7. C-clock waveforms and auxiliary C-register pulses.

The master clock in our circuit is a 555 timer (U1 in Fig. 8), run as an asymmetric astable timer. It provides horizontal blanking pulses, shown in Figs. 6 and 7 as being low during blanking. The B-to-C transfer occurs during the short blanking time (Fig. 6). A 74124 start-stop oscillator (U-10) runs during the horizontal-blanking time, and drives flip-flops U-11 and U-12 which decode the four B-phases. A 7493 counter (U-15) counts the oscillator pulses, and blocks them after the first four. The C-register runs during the long "on" time of horizontal blanking pulse as in Fig. 7. Another 74124 start-stop oscillator (U2) runs during this "on" time, driving flip-flops U-3 and U-4 which decode the four "C" phases. A 16-bit binary counter (U-21, U-22, U-23, and U-24) counts the number of horizontal blanking pulses and stops the B-to-C transfers at a count of 50, with the help of NAND gate U-29. It continues to count to the selected value ranging from 64 to 32768. When this count is reached, counter U-25 counts four more horizontal lines, providing the vertical blanking pulse. The transfer pulse is triggered and completed during this time as shown in Fig. 9. It is worth noting that the C-clock is not counted; counting it is not necessary as any extra transfers of the C-register carry no detector signals and are dark on the display. Counting would, however, result in noise pickur on the display.

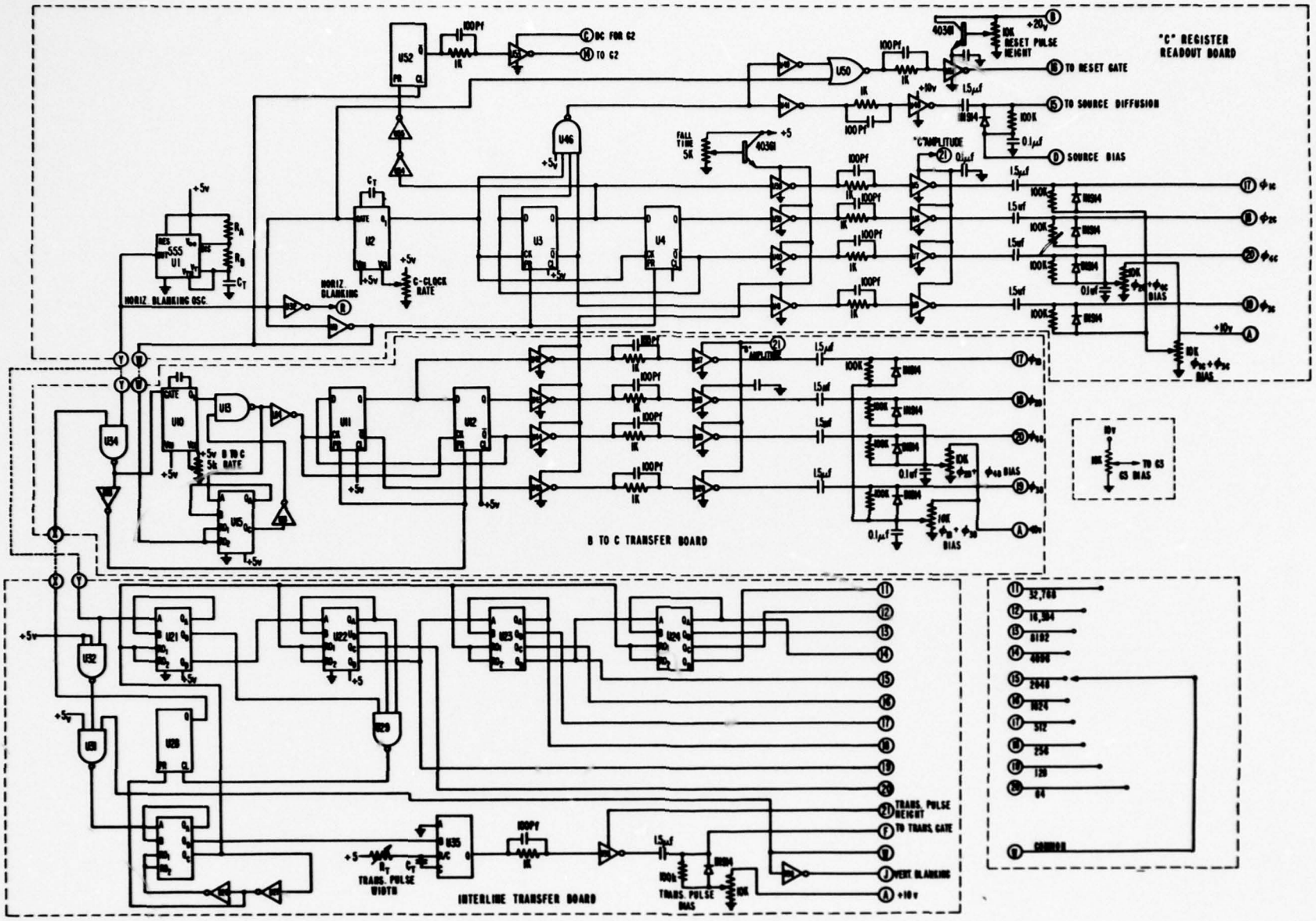


Figure 8. Detailed schematic of drive circuit

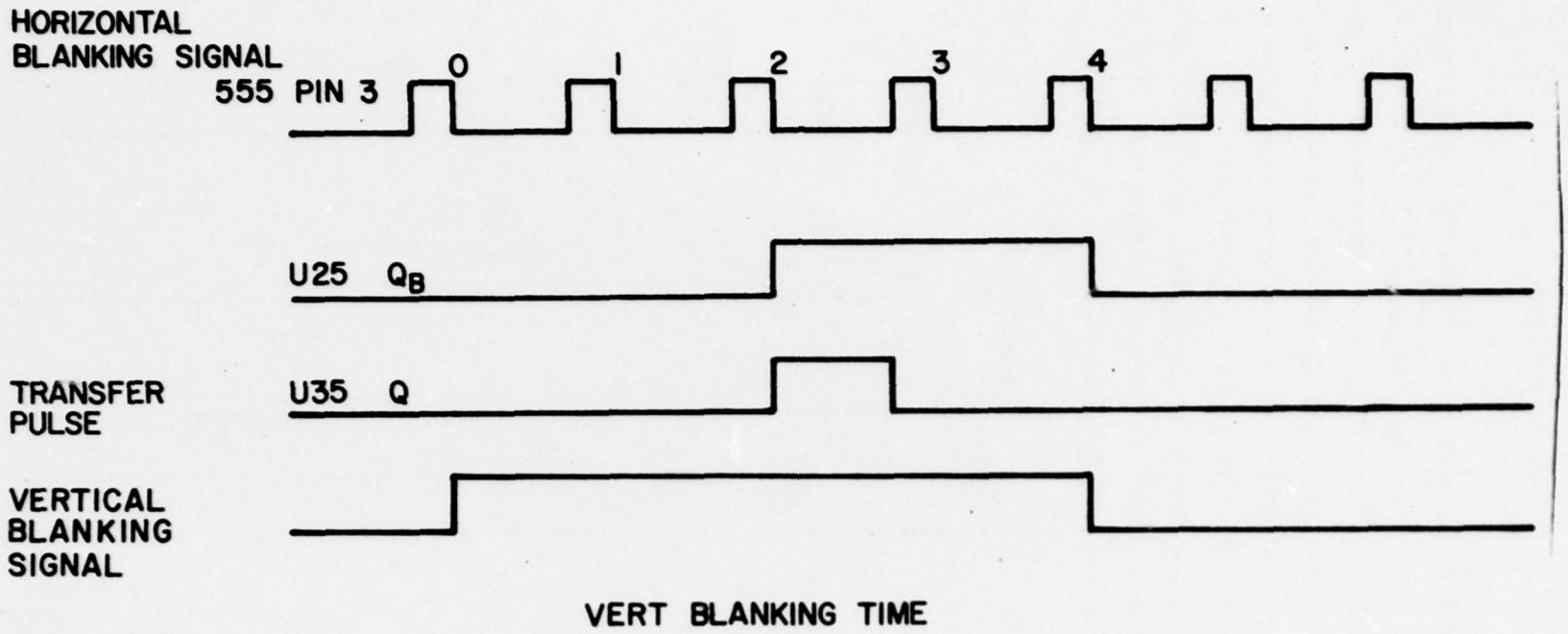


Figure 9. Position of the transfer pulse during the vertical blanking time.

V. CONCLUSIONS

The design of the 25 x 50 area array is nearly complete, and masks will soon be ordered. Arrays of this design will be made with both Pd_2Si and PtSi Schottky barriers. There will be optional masks for guard rings and for buried-channel operation. Processing has begun on a batch of wafers with Pt using the old masks, to give us some experience with Pt. Optical absorption measurements revealed a possible problem in the processing procedure, and an appropriate change was made. Infrared calculations were made demonstrating that thermal imaging with PtSi is possible, but that excess dark current at the detectors must be avoided.

REFERENCES

1. F. D. Shepherd et al., "Silicon Schottky-Barrier Monolithic IR TV Focal Planes," *Advances in Electronics and Electron Physics*, to be published.

2. E. S. Kohn, "A Charge-Coupled Infrared Imaging Array with Schottky-Barrier Detectors," IEEE Journal of Solid-State Circuits, SC-11, 139 (1976).

3. RCA Electro-Optics Handbook, 1974 p. 36.

4. J. E. Carnes and W. F. Kosonocky, RCA Review 33, 607-21 (1972).

5. E. S. Kohn, "Charge-Coupled, Scanned IR Imaging Sensors," AFCRL-TR-74-0375, July 15, 1974.

6. J. M. Andrews and M. P. Lepselter, Sol. St. Elec. 13, 1011-23 (1970).

APPENDIX

DETAILED DESCRIPTION OF CIRCUIT FUNCTIONS

U1 — 555 timer gives horizontal blanking period, runs as an asymmetric astable timer.

U2 — 74S124 start-stop oscillator 50% duty H→OFF, L→ON, f = 4fc

U3, U4 — Decodes four-phase, double-clocked waveform from U2.

U5, U6, U7, U8 — MMH0026 pulse drivers.

U9 — Inverts waveform from U1 to driver U3 and U4 into state so that during the horizontal blanking time $\emptyset_{1C}$→H, $\emptyset_{2C}$→H, $\emptyset_{3C}$→L, $\emptyset_{4C}$→L.

U10 — 74S124 gated on during the horizontal blanking time. The first four pulses are used to produce the double-clocked 4Ø waveform for the vertical transfer. The remaining pulses during the blanking time are not used.

U11, U12 — 7474 decodes U10 to make 4Ø double-clocked pulses.

U13 — 74S00 takes gating signal from U15 and after 4 pulses from U10 cuts off signal going to U11, U12.

U14 — Inverter needed because U11 and U12 trigger on positive going edge and U15 triggers on negative going edge.

U15 — 7493 counts four pulses from U10.

U16 — Inverter.

U17, U18, U19, U20 — MMH0026 drivers for B-register.

U21, U22, U23, U24 — 7493's count the number of horizontal lines for count of 50 to stop B-to-C transfers and the desired extra count for integration period added beyond the readout time.

U25 7493 counts four horizontal lines to make the vertical blanking time. Also provides output Q_B on count of 2, to trigger monostable U35 to provide transfer pulse for transfer from the imaged area to the B-register.

U26, U27 (Two inverters) Provide delay from U25 Q_C to U25 Ro1, Ro2. This widens the reset pulse to be sure it can reset the 5 TTL loads. U27 also inverts the reset pulse for PR on U28 because the 7474 requires a low level to preset.

U28 7474 used as a latch. At the beginning of the field after the transfer from detectors, U28 is preset to Q high. This allows the B-to-C transfer to be normally generated. After 50 lines U28 is cleared, and Q is low. This prevents the oscillator U10 from running to produce any more B→C transfers.

U29 7420 this provides the logic to decode the count of 50 to clear latch U28.

U30 Inverter provides vertical blanking signal.

U31 7400 gates on signal to U25 at start of vertical blanking time.

U32 Removes inversion of U31. This means U25 counts the trailing edge of the horizontal blanking pulse.

U33 Inverter, removes inversion of gate U34. This is so that U11 Pre and U12 Pre receive low levels during the horizontal line time.

U34 7400 stops U10 and presets U11, U12 after to B-to-C transfers have been made.

U35 74123 one shot is triggered on the count of 2 from U25. $\overline{Q}$ of U35 provides inverse of transfer pulse for detector to B-register transfer.

U36 MH0026 driver provides transfer pulse to transfer from detectors to B-register.

U37 Inverter provides horizontal blanking pulse.

U38, U39, U40, U41 Inverters for C-clock. All +5 V supplies are connected together to the fall time control. As the voltage is reduced, the drive to U5, U6, U7, U8 is reduced, causing the fall time to increase.

U42, U43, U44, U45 As above, but for B-clock.

U46 7420 logic to make S1 strobe. U46 output goes low when 4fc, $\emptyset_{3C}$ and $\emptyset_{4C}$ are all high.

U47 Inverter to compensate for inversion of driver U48.

U48 MMH0026 S-1 strobe driver.

U49 Inverter gives the reset gate an inverse of S1. It also buffers the reset logic from the input of U48.

U50 7402 output goes low at normal reset period or during H-blanking time.

U51 MMH0026 reset gate driver.

U52 7474 latch is cleared by H-D and then preset by the first low level on $\emptyset_{1C}$. This provides a signal to keep G_2 low during the time a signal is contained under $\emptyset_{1C}$ so that charge does not spill towards the source.

U53 MMH0026 G2 driver.

U54, U55 Form a delay so that G2 stays low until charge is transferred out of $\emptyset_{1C}$ stage 1.

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