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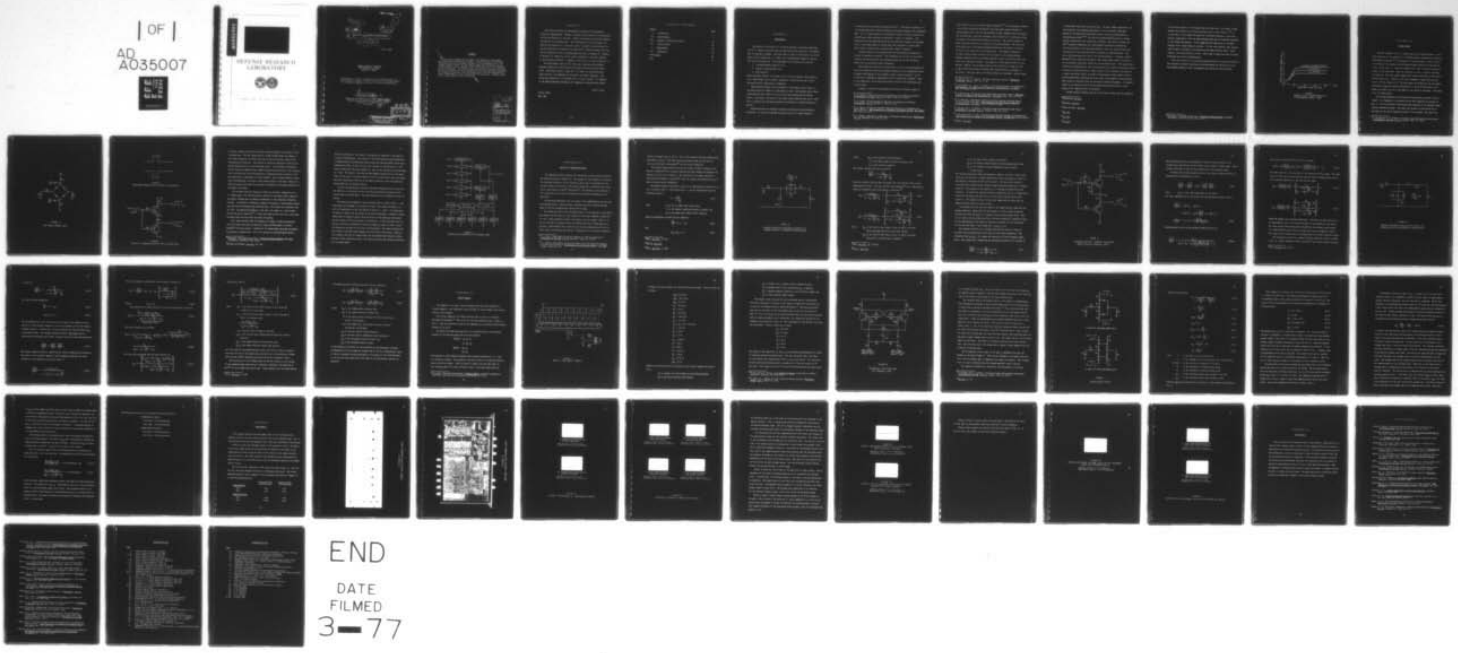

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6 DESIGN OF A SIX-CHANNEL ELECTRONIC GATE,

by

10 Jerry G. Cole

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DEFENSE RESEARCH LABORATORY
THE UNIVERSITY OF TEXAS
AUSTIN 12, TEXAS

(Presented as a thesis to the Faculty of the Graduate School of The University of Texas in Partial Fulfillment of the Requirements for the Degree of Master of Science in Electrical Engineering)

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ABSTRACT

This thesis presents the development and design of a six-channel electronic gate for sampling dc signals. Six-diode gates and transistor switching circuits are the basic elements of the six-channel gate. The primary design criteria are wide dynamic range, good linearity, and gain of approximately unity. Analysis of the switching times of the transistor switch is developed. The design values for the switch are also calculated. The other components of the six-channel gate have been adequately presented in literature; therefore, only the design values for these components are given. Measurements of the completed gate are presented. A dynamic range of 50 db and a gain of 0.965 is achieved.

P R E F A C E

This thesis presents the development and design of a multichannel electronic sampling gate. Chapter I presents the introduction to the problem and the requirements for the gate. Chapter II discusses the various elements required for a six-channel gate. The requirements for the switching voltages and the analysis of a transistor switch to generate these voltages for the six-diode gates are discussed in Chapter III. Design procedures for the various components of the six-channel gate are given in Chapter IV. Chapter V is devoted to a comparison of the actual performance of the gate compared to the predicted operation. A summary of the results is given in Chapter VI.

The experimental work for this thesis was conducted at the Defense Research Laboratory of The University of Texas under Navy Contract NObsr-72627. The author wishes to thank Dr. H. W. Smith for supervising this thesis and Dr. C. M. McKinney for serving on the thesis committee. The author also thanks Mr. R. H. Wallace, Mr. G. E. Ott, and Mr. L. D. Hampton of the Defense Research Laboratory for suggestions concerning this thesis.

Jerry G. Cole

Austin, Texas

May, 1961

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C H A P T E R I

INTRODUCTION

The purpose of this thesis is to present generally the design techniques for an "n" channel electronic gate and specifically the design of a six-channel gate for gating dc signals. The word "gate" as used in this thesis is a device which allows transmission of a signal for a predetermined length of time and then shuts the signal off. The requirements for the gate are as follows:

1. A minimum dynamic range of 40 db
2. A gain of approximately unity
3. Good linearity

Other desirable features of the gate are low cost per channel, small physical size, light weight, and low power consumption. These features may be best realized by use of semiconductor components.

The greatest problem to be encountered in the design of such a gate is the paralleling of a number of single gates to form a multichannel gate without increasing the noise level at the output and hence decreasing the dynamic range of the system. The noise in the output comes primarily from the dc unbalance or pedestal and switching transients encountered in turning the gates on and off.

Numerous methods of attacking the gating problem have been presented in literature. An article by Edwards discusses the use of a gated amplifier

in multiplexing and analog multiplying circuits.[1] One method of gating is to use pentode amplifiers keyed by applying a switching voltage to the suppressor grid. An "n" channel gate can be obtained by using a low plate resistor and paralleling as many pentodes as necessary to obtain "n" channels. This method was not considered practical for the particular system to be designed since a very large number of vacuum tubes and consequently a large power drain would be required for any appreciable number of channels.

Another solution to the problem that has been extensively employed is the use of mechanical switches.[2] The limitations of the life of the switch contacts and the relatively low switching speed rule out the mechanical switch for the application being considered.

The problem as presented is closely akin to that of the requirements for low-level commutation and multiplexing encountered in the telemetering field. A general bibliography of the telemetry field is given by Uglow.[3] A list of electronic commutators commercially built is presented by Kramer.[4] None of the commutators listed were particularly suited to the requirements previously stated.

A number of articles have appeared which describe systems similar to

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[1] C. M. Edwards, "Precision Electronic Switching with Feedback Amplifiers," Proceedings of the IRE, Vol. 44, November, 1956, pp. 1613-20.

[2] A. S. Kramer, "Electromechanical Switches for Telemetering Systems," Electronics, Vol. 32, October 2, 1959, pp. 54-5.

[3] K. M. Uglow, "A Survey of Progress Reported During 1955 in Telemetry and Remote Control," IRE Transactions on Telemetry and Remote Control, Vol. TRC-3, May, 1957, pp. 9-13.

[4] A. S. Kramer, "Electronic Commutators in Multiplex Telemetering," Electronics, Vol. 32, September 25, 1959, pp. 76-7.

that required for the previously stated problems.[5-10] Of considerable interest is an article by Dorsett and Searcy[11] which discusses various methods of gating signals for a low-level multiplexing system. Methods tried, discussed, and discarded were neon-tube switching, photo-conductive cell switching, diode switching, and second-harmonic magnetic switching. The article presents a gated transistor switch as a solution to the gating problem. The transistor switch was built at the Defense Research Laboratory and found to be unsatisfactory for the previously stated application. Two methods dismissed by the above article might be useful in the solution of the gating problem. Raytheon Corporation has a new photo-conductive switch in which the input and output are completely isolated. This might be a very simple solution to the problem. However, the switching times of the switch are too long, but such a light switch with faster switching times could possibly be developed in the future. The diode gate is the other possibility discarded. Several forms

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[5] E. Dorsett and J. H. Searcy, "Low Level Electronic Switch," IRE Record Convention, Part 5, 1957, pp. 57-60.

[6] J. M. Walther, Jr., and J. H. Searcy, "A Low-Level Electronic Subcommutator," Proceedings of the 1957 National Symposium on Telemetering, Vol. TRC-3, Sec. 3.2, April 1, 1957.

[7] E. D. Herberling, "System for Rapid Reduction of Telemetric Data," IRE Transactions on Telemetry and Remote Control, Vol. TRC-3, May, 1957, pp. 23-5.

[8] R. E. Marquand, "High-Speed, High-Accuracy Multiplexing of Analog Signals for Use in Digital Systems," Proceedings of the 1957 National Symposium on Telemetering, Vol. TRC-3, Sec. 3.4, April 1, 1957.

[9] J. Millman and T. H. Puckett, "Accurate Linear Bidirectional Diode Gates," Proceedings of the IRE, Vol. 43, January, 1955, pp. 27-37.

[10] J. M. Sacks and E. R. Hill, "Transistorized Time Multiplexer for Telmetering," IRE Transactions on Telemetering and Remote Control, Vol.TRC-3,May,1957,pp.26-30.

[11] Dorsett, op. cit.

of diode gates have been used extensively. The most common configuration of the diode gate for multiplex applications is the six-diode bridge gate. Several of the previously referenced articles utilize six-diode gates in multiplexing systems.[12-14] The article by Herberling[15] discusses a sixteen channel system which uses vacuum tube switching. The article by Sacks and Hill[16] presents essentially the same system as described by Herberling with the exception of the switching networks, which are transistorized, and the addition of two switching diodes to produce an eight-diode gate. The extra switching diodes are used in the switching matrix. A similar system by Marquand[17] uses transistor switching. This system seems closest to meeting the requirements previously stated for the six-channel gate. With proper modification and simplification, the six-diode gate and transistor switching circuits would give the desired results. Major factors to be considered are design of a simpler switching circuit, problems of paralleling a large number of gates without appreciably increasing the noise level, and designing a six-diode gate which would be consistent with all previously stated requirements. As specific values are not given in any of the previously mentioned articles, circuit design of all component units is necessary.

Another method of gating that was tried without success was the modulation

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[12] Herberling, op. cit.

[13] Marquand, op. cit.

[14] Sacks and Hill, op. cit.

[15] op. cit.

[16] op. cit.

[17] op. cit.

of the spade terminal of a Burroughs beam switching tube. The target voltage-current relationship for the beam switching tube is shown in Fig. 1.[18] It is seen that, if the target and spade are considered analogous to the plate and grid respectively, then the beam switching tube may be considered analogous to the vacuum tube pentode. It was suggested that modulation of the spade terminal with a signal might be possible. If this were possible, many channels could be gated by properly interconnecting the beam switching tubes. Unfortunately, the characteristics of Fig. 1 were found to apply only when all spade potentials were varied simultaneously.

With the possibility of using beam switching tubes for switching dismissed, the alternative method of gating with six-diode gates was chosen as the best and simplest method of those investigated for solving the stated problem.

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[18] Burroughs, "Burroughs Beam-X Tube," Technical Brochure BX-535, Burroughs Corporation, Plainfield, New Jersey, p. 6.

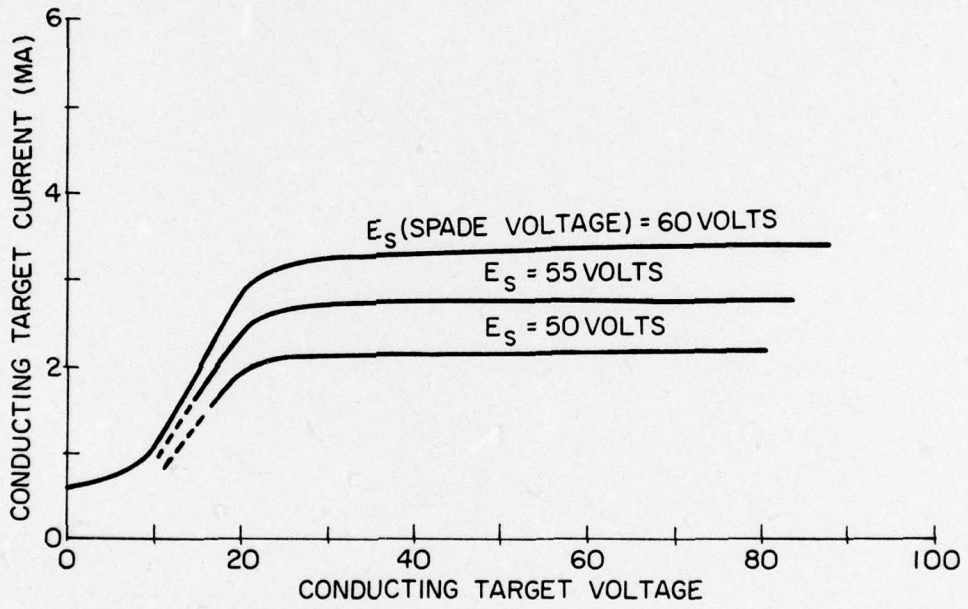

FIGURE 1
TARGET OUTPUT CHARACTERISTICS
OF BURROUGHS BEAM-X TUBE

C H A P T E R I I

SYSTEM DESIGN

The main component of an "n" channel gate is the six-diode gate. A very good discussion of the operation of six-diode gates is presented in an article by Millman and Puckett.[19] The diagram of a six-diode gate is shown in Fig. 2. As is shown on the diagram, the switching voltages required for the gate are + and - N and + and - C. When the condition of + and - N exists, the gate is cutoff or non-conducting. When the condition of + and - C exists, the gate is turned on. The input signal appears with slight attenuation at the output when the gate is on. There is very little leakage of signal when the gate is off. If the outputs of "n" six-diode gates are paralleled, and the proper switching voltages are applied sequentially to the switching diodes of the gates, the output will be a time sample of the inputs to the gates. The result is an "n" channel gate.

The voltage waveforms for switching six-diode gates are shown in Fig. 3. Figure 4 is a diagram of a transistor switch which supplies the waveform of Fig. 3. The first method of switching tried consisted of two cascaded common-emitter saturated switches. The delay time between the two pulses due to the delay of the second transistor proved to be too large. The sum of the

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[19] J. Millman and T. H. Puckett, "Accurate Linear Bidirectional Diode Gates," Proceedings of the IRE, Vol. 43, January, 1955, pp. 27-37.

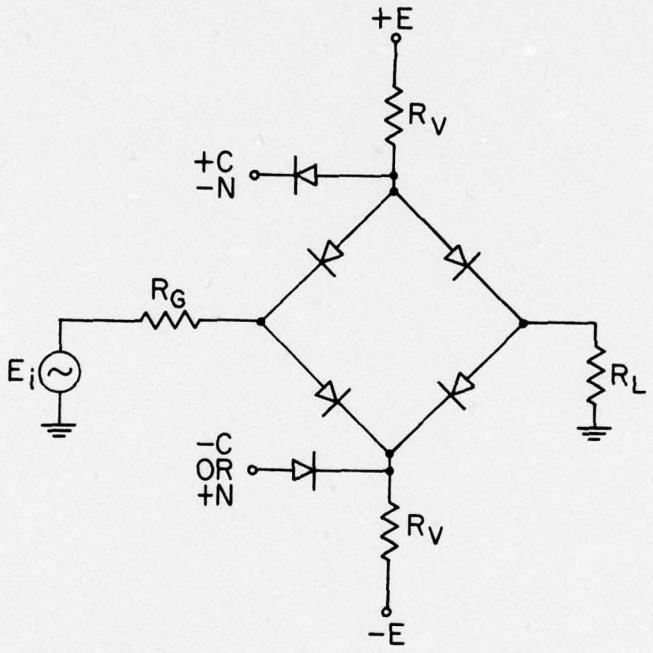

FIGURE 2

SIX-DIODE BRIDGE GATE

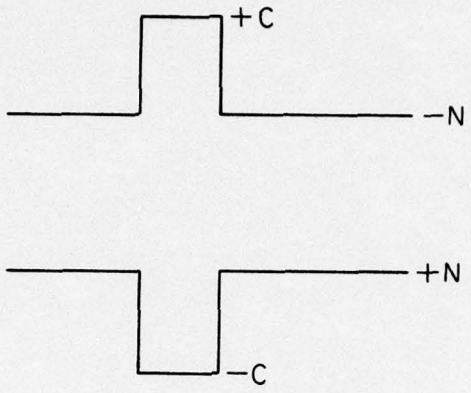

FIGURE 3
WAVEFORM REQUIRED FOR SWITCHING SIX-DIODE GATE

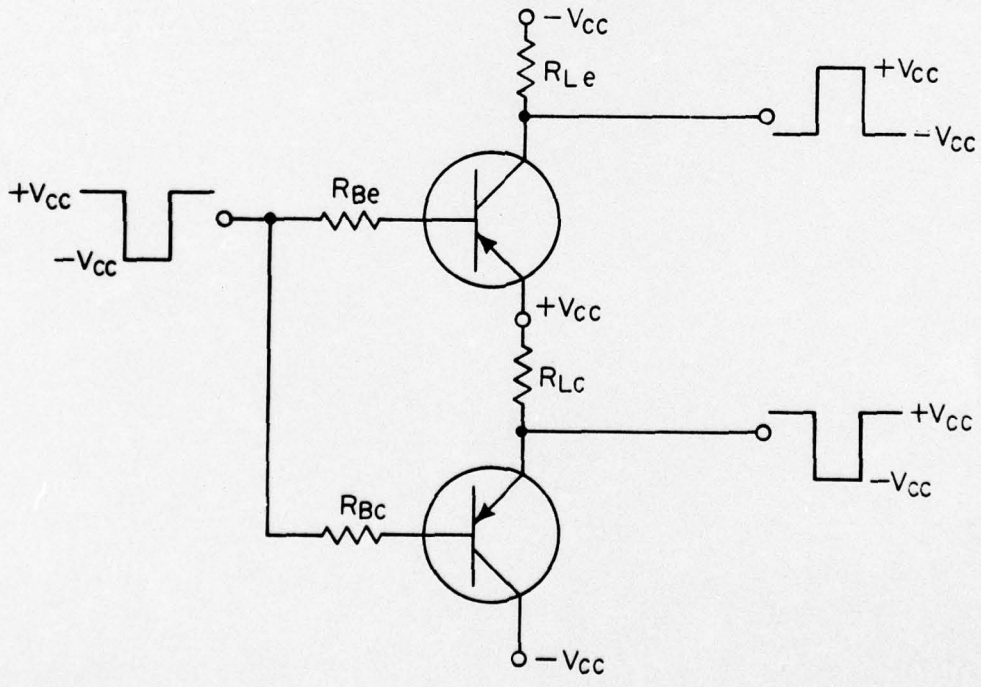

FIGURE 4
CIRCUIT OF TRANSISTOR SWITCH FOR SIX-DIODE GATE

switching voltages during the switching transient appears in the output of the six-diode gate. For the cascade switch a large voltage spike will appear in the output because of the delay time even if the rise and fall times of the transistors are identical. The problem of the delay time may be solved by employing parallel drive to the switching circuit. On this basis a switching circuit using the common-emitter, common-collector switch of Fig. 4 was conceived. Since the switch has not been presented in literature before, analysis of the switching times is developed in a later chapter. With a signal applied to both bases simultaneously, the delay to both output pulses is the same. Equal rise times and equal decay times are necessary to minimize the switching transient in the output of the gate.

The six-diode gate and transistor switch are the basic components of an "n" channel gate. To turn the gates on and off in the proper order, pulses of the proper voltages must be applied sequentially to the transistor switching circuits. One method of obtaining a sequence of pulses is a multielement switching tube such as Burroughs beam switching tube. Ten outputs are available from one tube. By paralleling elements of the tube, any number of pulses between one and ten may be obtained.[20] A diode matrix may be used with two or more beam switching tubes for more than ten sequential pulses.

For a gate with more than ten channels the number of parts required and the total output noise may be reduced by using six-diode gates in series-parallel[21] to form a matrix. Consider an "n" channel gate which may be grouped in m groups of p gates each. All of the outputs of six-diode gates within a

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[20] Burroughs, "Burroughs Beam-X Tube," Technical Brochure BX-535, Burroughs Corporation, Plainfield, New Jersey.

[21] Millman and Puckett, op. cit., pp. 36-7.

group are paralleled. The output of each group is connected to the input of a series six-diode gate. The outputs of the series gates are also paralleled. A scanning pulse of p sequential pulses scans the six-diode gates in the input grouping such that, at any one time, only one gate in each group is on. The series output gates are then scanned at a rate of 1/p turning on one series gate at a time. The output is the desired time sampled reproduction of the inputs. Since all but one of the series gates is off at any particular time, the switching noise contribution from all of the gates connected to the non-conducting series gates will be greatly reduced.

For the six-channel gate the above described components will be used with the addition of a flip-flop circuit for driving transistor switches for the series output six-diode gates. The beam switching tube is modified to have six outputs.

The system block diagram of the six-channel gate is shown in Fig. 5. Six input gates are arranged in two groups of three. The outputs of gates 1, 2, and 3 are paralleled, as are the outputs of gates 4, 5, and 6. An output gate is placed in series with the output of the first three gates. Likewise, another output gate is placed in series with the output of the remaining three gates, and the outputs of the series gates are paralleled. A beam switching tube connected to provide six switching lines with sequential pulses is used to drive the transistor switches for the input six-diode gates. The beam switching tube also drives a flip-flop which changes state with every third pulse. Actually, to be exactly like the "n" channel gate, the six-channel gate should be driven with only three sequential pulses. The flip-flop drives the transistor switches for the output gates.

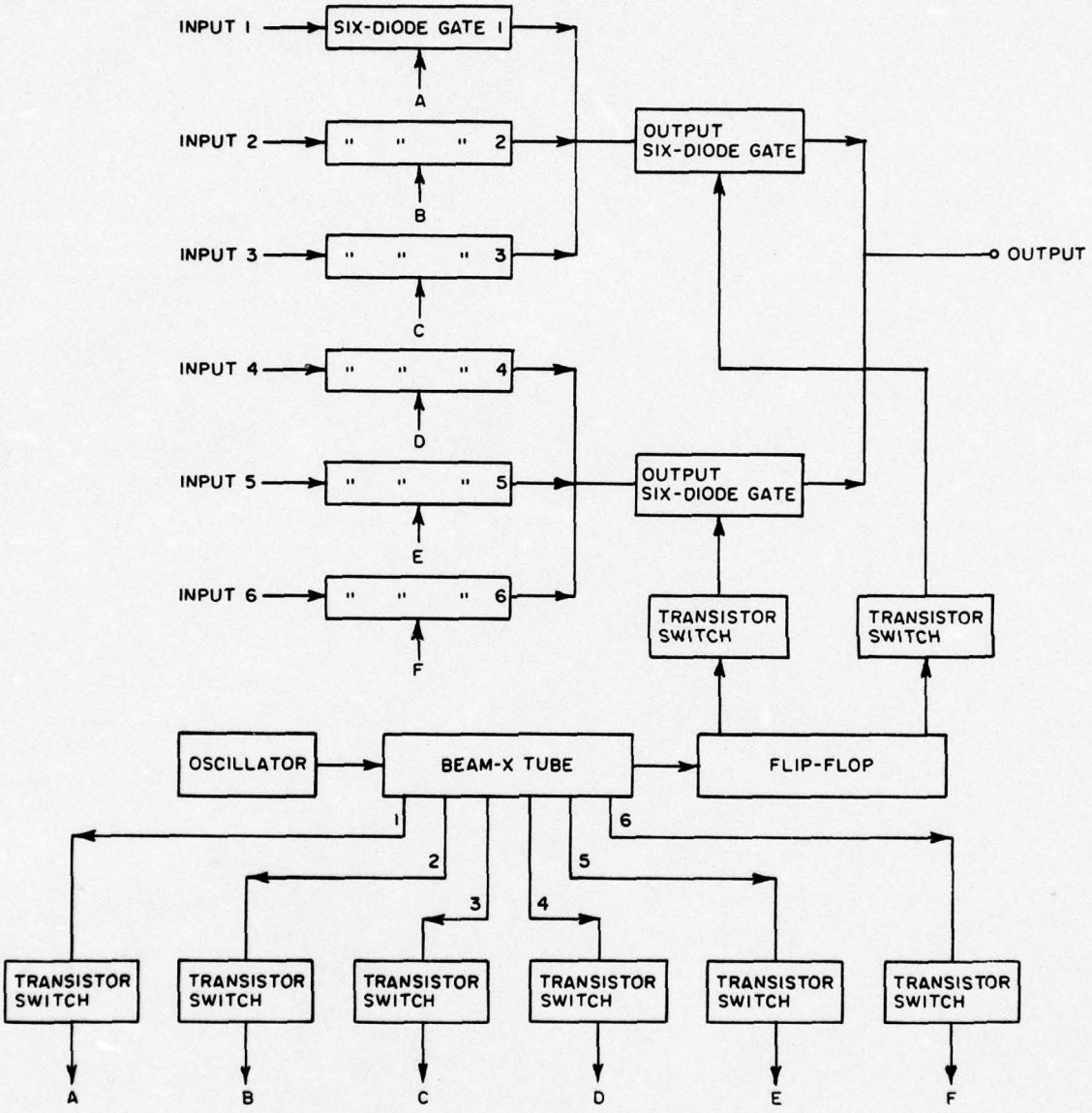

FIGURE 5
SYSTEM BLOCK DIAGRAM OF SIX-CHANNEL GATE

C H A P T E R I I I

ANALYSIS OF TRANSISTOR SWITCH

The transistor switch required for turning the six-diode gates on and off was described briefly in Chapter II. The purpose of this chapter is to analyze the switching transients of the transistor switch and to calculate the rise and fall times of the switch. The analysis presented is essentially an extension of the analysis of Moll[22] and Easley.[23] The analysis in this chapter is for a particular case, and the assumptions made by Moll and Easley are not applicable.

As previously mentioned, the rise times of the common-emitter and the common-collector switch should be equal; similarly the fall times and storage times of the two configurations should also be equal.

The transistor used in the switching circuit for the gate was a type 2N1371. The reasons for the choice of this transistor were high breakdown voltage and low cost. High breakdown voltage is desirable since the dynamic range of the gate is limited on the upper end by the maximum switching voltage applied to the gate. Unfortunately this transistor did not have characteristics particularly suited to switching applications. Measurement of the collector capacity

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[22] J. L. Moll, "Large Signal Transient Response of Junction Transistors," Proceedings of the IRE, Vol. 42, December, 1954, pp. 1773-84.

[23] J. W. Easley, "The Effect of Collector Capacity on the Transient Response of Junction Transistors," IRE Transactions on Electron Devices, Vol. ED-4, January, 1957, pp. 6-14.

showed an average value of 110 pf. The cutoff frequency from the manufacturers data sheet is two mc. The above values and other design criteria are not consistent with Moll's assumption[24] of short-circuit operation.

The analysis below presents briefly the results of Moll's analysis with Easley's correction[25] for collector capacity and then extends and modifies the analysis for the case in question. The calculation of storage time may be made directly from Moll's equations[26] since the storage time equations are not based on short-circuit assumptions.

The medium frequency equivalent circuit of a common-emitter transistor circuit is shown in Fig. 6. The current gain, α , may be approximated with the following equation:

$$\alpha = \frac{\alpha_N}{1 + \frac{s}{\omega_N}} \tag{3-1}$$

where α_N is the dc common base current gain,

s is the Laplace transform frequency variable, and

ω_N is the common base radian cutoff frequency.

Under the assumption of short-circuit operation:

$$\frac{R_{Le}}{r_c} \ll 1 - \alpha_N \tag{3-2}$$

and

$$\omega_N C_c R_{Le} \ll 1 \tag{3-3}$$

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[24] Moll, op. cit., p. 1775.

[25] Easley, loc. cit.

[26] Moll, op. cit., p. 1780.

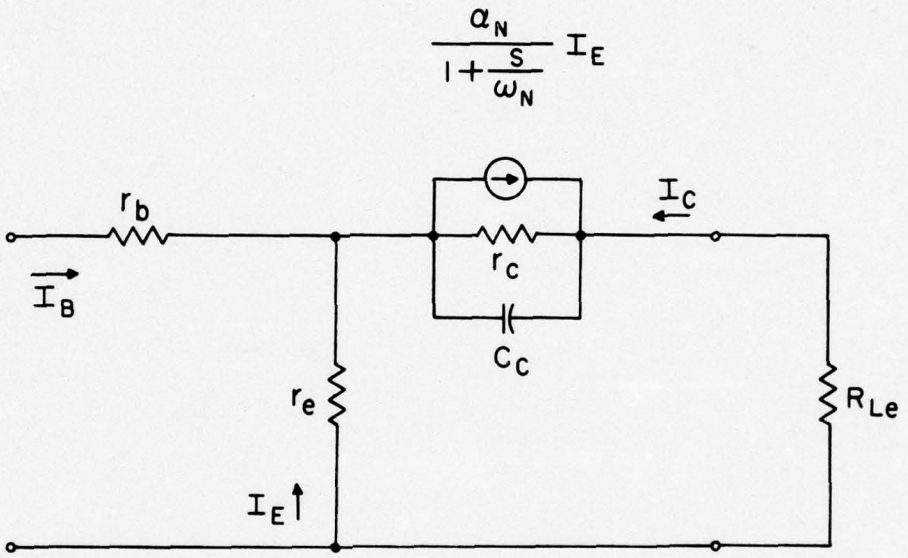

FIGURE 6

MEDIUM FREQUENCY EQUIVALENT CIRCUIT OF COMMON EMITTER TRANSISTOR CONFIGURATION

where R_{Le} is the collector load resistance,

r_c is the small signal collector resistance, and

C_c is the collector capacity.

The current transfer function is given by

$$\frac{I_C(s)}{I_B(s)} = \frac{\alpha_N}{1 - \alpha_N + \frac{R_{Le}}{r_c} + \frac{s}{\omega_N}} \quad . \tag{3-4}$$

From this transfer function Moll calculates the rise and fall times of the common-emitter switch. The rise and fall time equations[27] for a step current input are reproduced below with Easley's correction:[28]

$$T_{Re} = \frac{1 + \omega_N R_{Le} C_c}{(1 - \alpha_N + \frac{R_{Le}}{r_c})\omega_N} \ln \left[\frac{I_B}{I_B - 0.9 \frac{1 - \alpha_N + \frac{R_{Le}}{r_c}}{\alpha_N} I_c} \right], \tag{3-5}$$

$$T_{Fe} = \frac{1 + \omega_N R_{Le} C_c}{(1 - \alpha_N + \frac{R_{Le}}{r_c})\omega_N} \ln \left[\frac{I_{C1} - \frac{\alpha_N}{1 - \alpha_N + \frac{R_{Le}}{r_c}} I_{B2}}{0.1 I_{C1} - \frac{\alpha_N}{1 - \alpha_N + \frac{R_{Le}}{r_c}} I_{B2}} \right], \tag{3-6}$$

where T_{Re} is the time for the output to rise to 90% of its final value with application of a step base current,

T_{Fe} is the time for the output to fall to 10% of its final value after a turnoff pulse is applied,

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[27] Moll, op. cit., pp. 1779-80.

[28] Easley, loc. cit.

I_B is the step current applied to the base,

I_{B2} is the reverse current applied to base during turnoff, and

I_{C1} is the collector current immediately before turnoff current pulse.

For the particular case under consideration, however, the short circuit conditions are not satisfied. Another change which alters the analysis of Moll is the method of obtaining the base drive current. The base drive current is obtained from a voltage source through a high resistance shunted by a "speedup" capacitor. The purpose of the capacitor is to speedup switching during the transient. In effect the capacitor-resistor combination acts as a voltage drive during the switching transient and as a current drive during steady state condition. The complete circuit for both the common-emitter switch and the common-collector switch is shown in Fig. 7.

To calculate the rise and fall times of the common-emitter stage with the speedup capacitor, assume that the base signal is a step voltage during the transient and that the input is a constant current during steady state. This is, of course, not the actual case since the base voltage will change with time, but the approximation will result in sufficient accuracy for the calculation of rise and fall times. Also assume that $\omega_N R_{Le} C_c \gg 1$.

The transfer function for a voltage input must be derived in order to calculate the switching times on the basis of the stated assumptions. The assumption that $\omega_N R_{Le} C_c \gg 1$ makes the variation of α with frequency negligible. The current gain, neglecting the frequency variation of α, is given by

$$\frac{I_C(s)}{I_B(s)} = \frac{\alpha_N}{1 - \alpha_N + \frac{R_{Le}}{r_c} + R_{Le} C_c s} . \qquad (3\text{-}7)$$

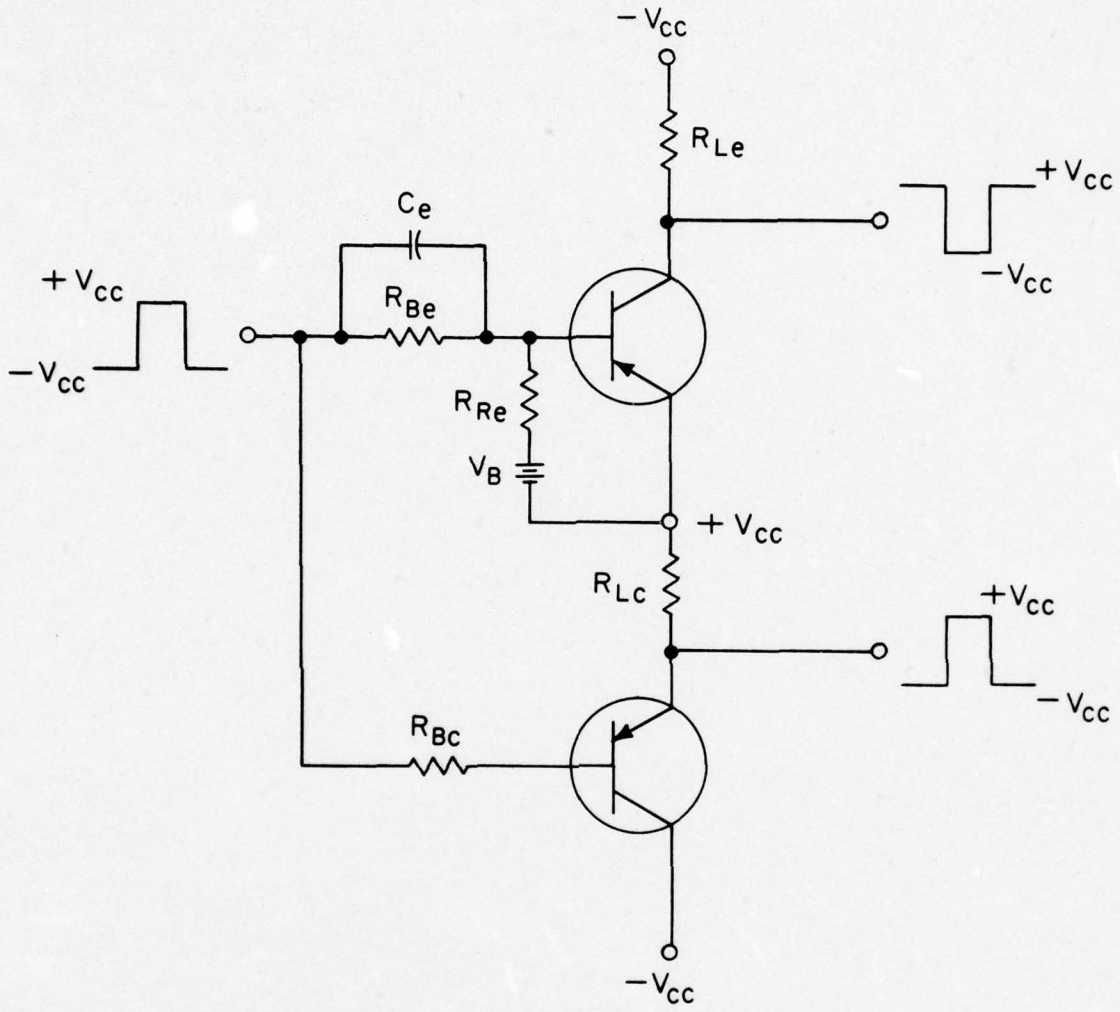

FIGURE 7

COMMON-EMITTER COMMON-COLLECTOR
SWITCH FOR SIX-CHANNEL GATE

The switching time can be approximated by using the time constant of the voltage step input and the current values of the constant current input. Moll's current values may be used for the calculation of the switching times.

To obtain the voltage transfer function, the current transfer function is multiplied by the admittance as below:

$$\frac{I_C(s)}{V_B(s)} = \frac{I_C(s)}{I_B(s)} \quad Y_{in}(s) = \frac{I_C(s)}{I_B(s)} \frac{I_B(s)}{V_B(s)} , \tag{3-8}$$

where $Y_{in}(s)$ is the input admittance of the switch.

The input impedance may be calculated from the equivalent circuit in Fig. 6.

$$\frac{I_B(s)}{Y_{in}(s)} = I_B(s)\, r_b - I_E(s)\, r_e$$

$$= I_B(s)\, r_b + I_B(s) \frac{I_C(s)}{I_B(s)}\, r_e + I_B(s)\, r_e$$

$$\frac{1}{Y_{in}(s)} = r_b + r_e + \frac{\alpha_N\, r_e}{1 - \alpha_N + R_{Le}\, C_c s} . \tag{3-9}$$

From Equations 3-8 and 3-9 the voltage transfer function is

$$\frac{I_C(s)}{I_B(s)} = \frac{\alpha_N}{R_{Le}\, C_c\, (r_b + r_e)\left[\frac{(1 - \alpha_N)\, r_b + r_e}{R_{Le}\, C_c\, (r_b + r_e)} + s \right]} . \tag{3-10}$$

The inverse transform of the above is as follows:

$$I_C(t) = \frac{-\alpha_N V_B}{(1 - \alpha_N) r_b + r_e} \left[\exp \left(- \frac{(1-\alpha_N) r_b + r_e}{R_{Le} C_c (r_b + r_e)} t \right) - 1 \right] . \qquad (3\text{-}11)$$

The time constant is the only part of the transfer function needed. The combination of this time constant and the constant current charging values yields the following equations for the rise and fall times:

$$T_{Re} = \frac{R_{Le} C_c (r_b + r_e)}{(1-\alpha_N) r_b + r_e} \ln \left[\frac{I_B}{I_B - \frac{1-\alpha_N + \frac{R_{Le}}{r_c}}{\alpha_N} 0.9 I_C} \right] , \qquad (3\text{-}12)$$

$$T_{Fe} = \frac{R_{Le} C_c (r_b + r_e)}{(1-\alpha_N) r_b + r_e} \ln \left[\frac{I_{C1} - \frac{\alpha_N}{1-\alpha_N + \frac{R_{Le}}{r_c}} I_{B2}}{0.1 I_{C1} - \frac{\alpha_N}{1-\alpha_N + \frac{R_{Le}}{r_c}} I_{B2}} \right] , \qquad (3\text{-}13)$$

where the symbols are as defined previously. Obviously the above solution is an approximation, but it is accurate enough for the purposes of this thesis. The value of the time constant may be found from the measured time constant of a common-emitter circuit with a voltage step input as suggested by Moll. The values of the currents may be calculated from the circuit component values.

The equivalent circuit of a common-collector transistor circuit is shown in Fig. 8. Again referring to Moll's article,[29] the current transfer function

[29] Moll, op. cit., pp. 1775-6.

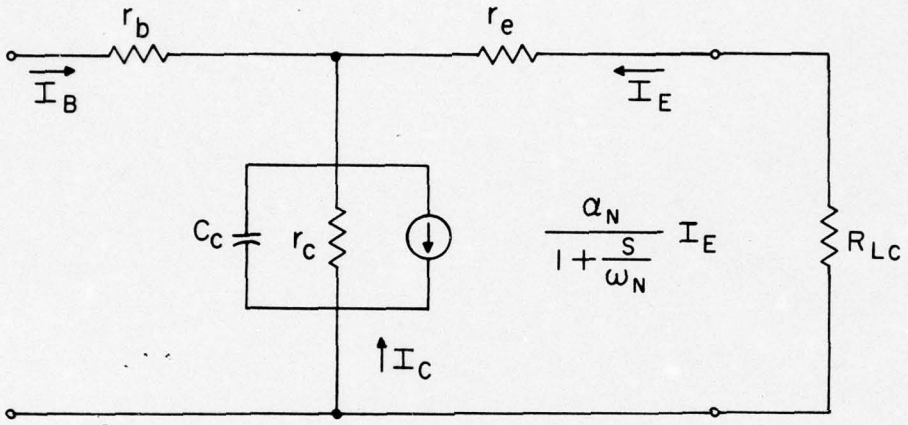

FIGURE 8

MEDIUM FREQUENCY EQUIVALENT CIRCUIT OF COMMON COLLECTOR TRANSISTOR CONFIGURATION

is given by

$$\frac{I_E(s)}{I_B(s)} = - \frac{1 + \frac{s}{\omega_N}}{1 - \alpha_N + \frac{R_{Lc}}{r_c} + \frac{s}{\omega_N}} \tag{3-14}$$

for the following assumptions:

$$\frac{R_{Lc}}{r_c} \ll 1 - \alpha_N \, , \tag{3-15}$$

$$\omega_N \, R_{Lc} \, C_c \ll 1 \, . \tag{3-16}$$

For the application in the six-diode gate the input to the common-collector switch is a step voltage; therefore, it will be necessary to find the voltage transfer function. Consider Fig. 8 with the addition of input resistor, R_{Bc}, in the base circuit. The voltage transfer function $I_E(s)/I_B(s)$ may be calculated by multiplying the current transfer function by the input admittance:

$$\frac{I_E(s)}{V_B(s)} = \frac{I_E(s)}{I_B(s)} \; \frac{I_B(s)}{V_B(s)} \, . \tag{3-17}$$

The current transfer function, neglecting the cutoff frequency and considering the effect of the collector capacity, which completely dominates the time constant for the transistor and circuit used, is

$$\frac{I_E(s)}{I_B(s)} = - \frac{(1 + R_{Lc} \, C_c \, s)}{(1 + R_L \, C_c \, s) - \alpha_N + \frac{R_{Lc}}{r_c}} \, . \tag{3-18}$$

The input impedance including the series external resistor is

$$Z_{in}(s) = \frac{V_B(s)}{I_B(s)} = R_{Bc} + r_b + R_{Lc} \left[\frac{s + \frac{1}{R_{Lc}C_c}}{s + \frac{1 - \alpha_N + \frac{R_{Lc}}{r_c}}{R_{Lc}C_c}} \right] . \tag{3-19}$$

Assume $$R_{Bc} \gg r_b . \tag{3-20}$$

The expression for output current for a step voltage input is given by

$$I_E(s) = - \frac{\frac{V_B}{s}\left(s + \frac{1}{R_{Lc}C_c}\right)\frac{1}{R_{Bc} + R_{Lc}}}{s + \frac{R_{Bc}\left(1 - \alpha_N + \frac{R_{Lc}}{r_c}\right) + R_{Lc}}{R_{Lc}C_c\left(R_{Bc} + R_{Lc}\right)}} . \tag{3-21}$$

The output current is as follows:

$$I_E(t) = V_B \left[\frac{1}{R_{Bc}\left(1 - \alpha_N + \frac{R_{Lc}}{r_c}\right) + R_{Lc}} - \frac{1}{R_{Bc} + R_{Lc}} \right] \exp\left[- \frac{R_{Bc}\left(1 - \alpha_N + \frac{R_{Lc}}{r_c}\right) + R_{Lc}}{R_{Lc}C_c\left(R_{Bc} + R_{Lc}\right)} \right] -$$

$$- \frac{V_B}{R_{Bc}\left(1 - \alpha_N + \frac{R_{Lc}}{r_c}\right) + R_{Lc}} . \tag{3-22}$$

The rise time calculated from the above analysis is

$$T_{Rc} = K \ln \left[\frac{V_B \left[\frac{1}{R_{Bc}\left(1 - \alpha_N + \frac{R_{Lc}}{r_c}\right)} - \frac{1}{R_{Bc} + R_{Lc}} \right]}{-0.9\, I_E + \frac{V_B}{R_{Bc}\left(1 - \alpha_N + \frac{R_{Lc}}{r_c}\right) + R_{Lc}}} \right] \tag{3-23}$$

and the fall time is

$$T_{Fc} = K \ln \left[\frac{\dfrac{\alpha_N R_{Bc}(V_B - V_{B2})}{(R_{Bc} + R_{Lc})\left[R_{Bc}(1 - \alpha_N + \dfrac{R_{Lc}}{r_c}) + R_{Lc}\right]}}{0.1\, I_{E1} - \dfrac{V_{B2}}{R_{Bc}(1 - \alpha_N + \dfrac{R_{Lc}}{r_c}) + R_{Lc}}} \right] \tag{3-24}$$

where T_{Rc} is the time for the output current to rise from 10% to 90% of its final value,

T_{Fc} is the time for the output current to fall from 90% to 10% of its maximum value,

$$K = \frac{R_{Lc}\, C_c (R_{Bc} + R_{Lc})}{R_{Bc}(1 - \alpha_N + \dfrac{R_{Lc}}{r_c}) + R_{Lc}} ,$$

V_B is the step input voltage to the base,

V_{B2} is the reverse input voltage applied during the turnoff transient,

R_{Lc} is the common-collector load resistor, and

R_{Bc} is the common-collector series base resistor.

As in the case for the common-emitter switch, the value of K may be obtained from the rise time of the common-collector switch to a non-saturating voltage pulse and the current charging values from the circuit component values.

The calculation of the storage times for the two circuits is not altered by not operating under short-circuit conditions; therefore, the equations of Moll[30] for the storage time may be used. These equations for the common-emitter

[30] Moll, op. cit., p. 1780.

and common-collector switches are given here for reference:

$$T_{Se} = \frac{\omega_N + \omega_I}{\omega_N \omega_I (1 - \alpha_N \alpha_I)} \ln \frac{I_{B1} - I_{B2}}{\frac{I_{C1}(1 - \alpha_N)}{\alpha_N} - I_{B2}} \tag{3-25}$$

$$T_{Sc} = \frac{\omega_N + \omega_I}{\omega_N \omega_I (1 - \alpha_N \alpha_I)} \ln \frac{I_{B2} - I_{B1}}{I_{B2} + I_{E1}(1 - \alpha_N)} , \tag{3-26}$$

where T_{Se} is the common-emitter storage time,

T_{Sc} is the common-collector storage time,

ω_I is the radian cutoff frequency with the collector and emitter interchanged,

α_I is the common base current gain with the collector and emitter interchanged,

I_{B1} is the base current during saturation,

I_{B2} is the base current immediately after saturation,

I_{C1} is the saturated collector current, and

I_{E1} is the saturated emitter current.

In the design of the switch for the switching of six-diode gates, the main consideration will be to make the storage time of the two configurations equal in order to minimize the switching spike in the output of the six-diode gates. If the rise and fall times are on the order of one microsecond, they may be neglected.

C H A P T E R I V

CIRCUIT DESIGN

The elements to be used in the six-channel gate have been presented in earlier chapters. The individual circuit designs of these elements will be presented in this chapter.

The circuit design for the beam switching tube is given in a brochure published by Burroughs.[31] The circuit for the beam switching tube is shown in Fig. 9. Only the resultant values of the components as calculated from Burrough's design will be given.

To convert the beam switching tube to a six-state device, the following elements of the beam switching tube are tied together:

Targets: T_2, T_3, T_4

T_7, T_8, T_9

Spades: S_2, S_3

S_7, S_8

This pattern of tying elements together will eliminate positions 2, 3, 7, and 8, leaving six outputs. The purpose of the start switch is to form the electron beam on the first target. After the beam is formed, the sine wave input to the switching grids will cause the beam to move to the next target when the

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[31] Burroughs, "Burroughs Beam-X Tube," Brouchure BX535, Burroughs Corporation, Electronic Tube Division, Plainfield, New Jersey, pp. 4-12.

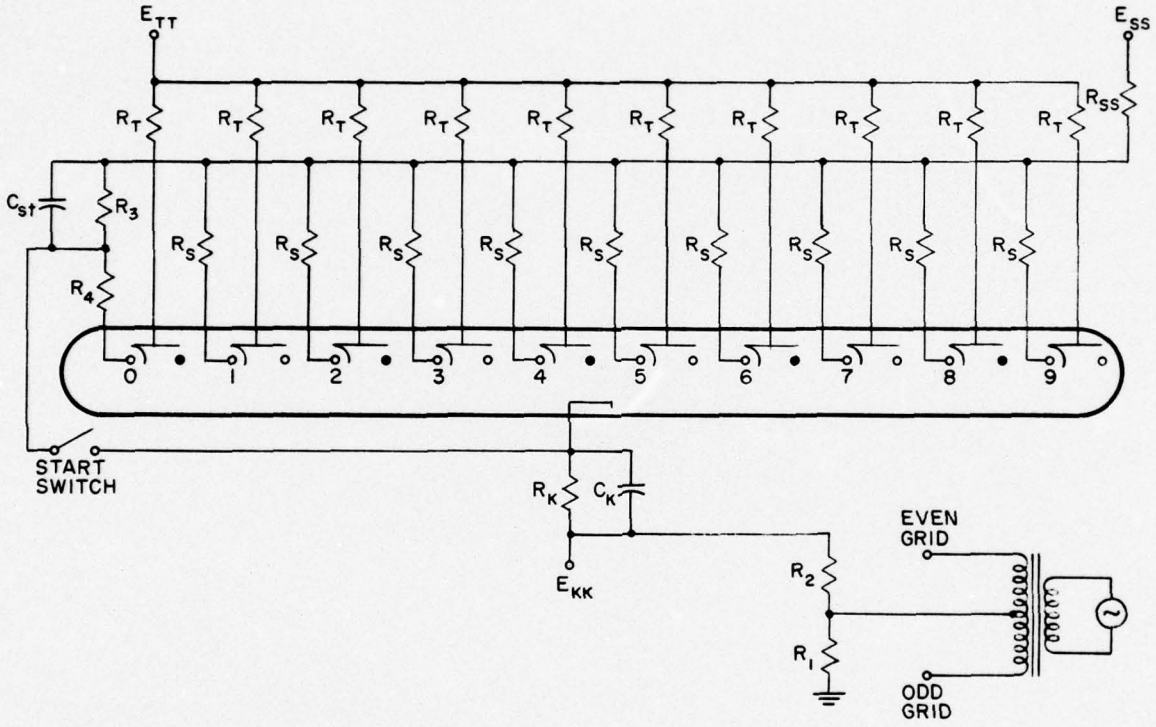

FIGURE 9
BEAM-X TUBE CIRCUIT DIAGRAM

voltage on the grid exceeds the required switching voltage. Circuit values are as shown:

E_{TT} = 20 volts

E_{KK} = -105 volts

E_{SS} = 0 volts

E_S = 60 volts

R_S = 150 K

E_C = 40 volts

E_K = -60 volts

E_g = -8 volts

$E_{in} = E_g - E_C$ = -48 volts

I_S = 0.42 ma

R_T = 6.8 K

R_K = 12 K

C_K = 1500 pf

R_1 = 30 K

R_2 = 68 K

R_3 = 13.5 K

R_4 = 130 K

C_{st} = 0.01 μf

R_{SS} = 9.1 K

Symbols used above which are not defined on the circuit diagram are defined below:

E_S is voltage rise from cathode to non-conducting spade,

E_C is grid bias potential from cathode,

E_K is voltage rise to cathode through cathode resistor,

E_g is maximum value of grid voltage when E_{in} is applied,

E_{in} is maximum negative amplitude of grid driving voltage, and

I_S is total quiescent spade current.

The design of the flip-flop for the six-channel gate is conventional. There are a multitude of sources on the design of transistor flip-flops, one of which is the General Electric Transistor Manual.[32] The design procedure used for the flip-flop for the six-channel gate is given in an article by Emile.[33] As in the design of the beam switching tube, only the values obtained from the design procedure will be presented. All symbols are defined by the diagram of the flip-flop in Fig. 10. The transistors are type 2N1371; the diodes are type 1N34-A. Circuit values are as shown:

$$V_{CC} = 20 \text{ volts}$$

$$E_{bb} = 6 \text{ volts}$$

$$R_c = 4.7 \text{ K}$$

$$R_b = 56 \text{ K}$$

$$R_p = 330 \text{ K}$$

$$R_d = 47 \text{ K}.$$

The values of the capacitors, C_c and C_d, were determined experimentally in order to yield the shortest switching times. The best switching times, less than 0.5 microsecond, were obtained when both C_c and C_d were 200 pf. The transistor switches previously described must be assumed not to load the output of the flip-flop. The trigger circuit of the flip-flop differentiates the output pulse

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[32] General Electric Company, G. E. Transistor Manual, Semiconductor Products Department, Syracuse, New York, 1958.

[33] P. Emile, Jr., "Design of a Two Transistor Binary Counter," Electronic Design, Vol. 7, March 18, 1959.

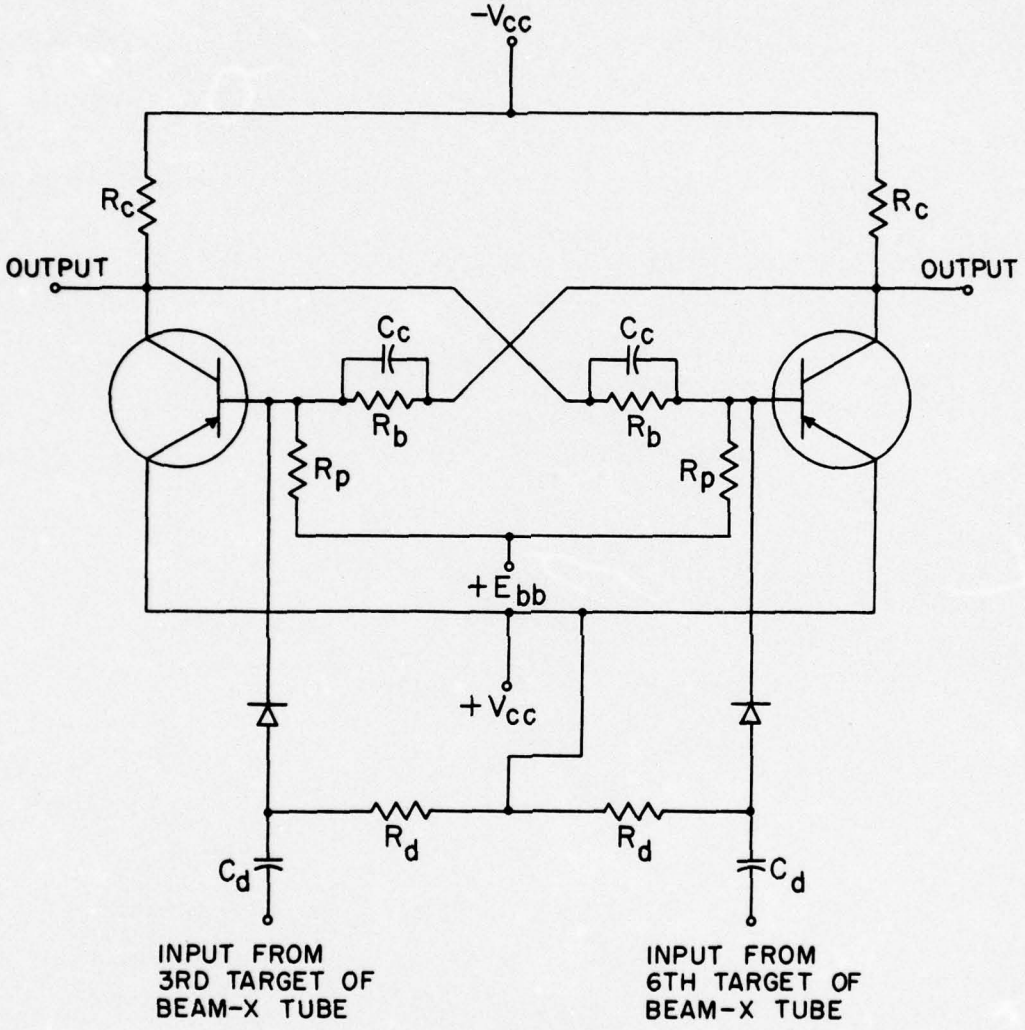

FIGURE 10

TRANSISTOR FLIP-FLOP FOR
SIX-CHANNEL GATE

of the beam switching tube. The diodes prevent the flip-flop from triggering on negative pulses; therefore, the flip-flop changes state only on the trailing edge of the third or sixth pulse of the beam switching tube.

The six-diode gate is discussed briefly in the chapter on system design. The information for design of the six-diode gates used in the six-channel gate is taken from an article by Millman and Puckett.[34] The six-diode bridge gate was chosen in preference to the less complicated two and four-diode versions (see Fig. 11) because the six-diode gate has inherently lower noise output and higher gain. A gain of approximately unity becomes important when two or more gates are to be operated in series. The circuit of the six-diode gate is shown in Fig. 2. All of the equations needed for design and other calculations are taken from Millman and Puckett's article[35] mentioned above. Other reasons for using the six-diode gate are small driving currents, fast switching speed and negligible signal leakage when the gate is off. The diodes used in the six-diode gates are type 1N627. The 1N627 is a computer diode with very fast recovery time. The switching time of the diodes may be neglected when compared with the transistor switching times.

The dc unbalance in the output of the gate is dependent only upon the balance of the bias voltage, E. Since the dc unbalance is the major noise factor in the six-channel gate, a regulated bias supply is required. The voltages, + and - E, may be obtained from two voltage regulator tubes in series.

The equations necessary for determining the performance of six-diode

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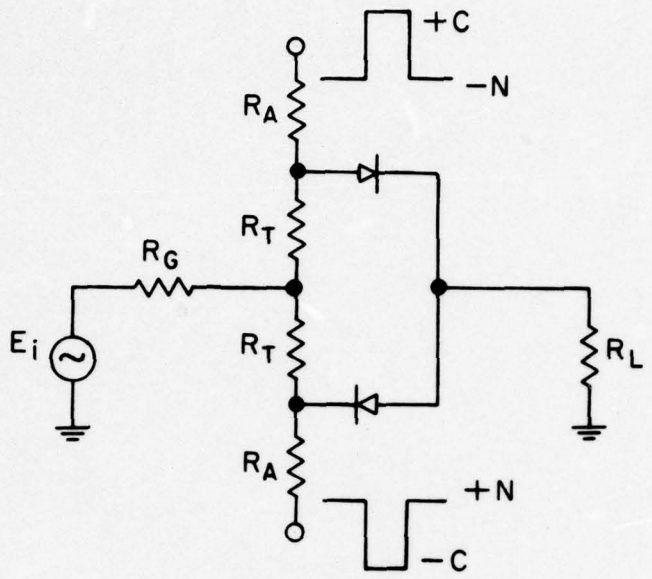
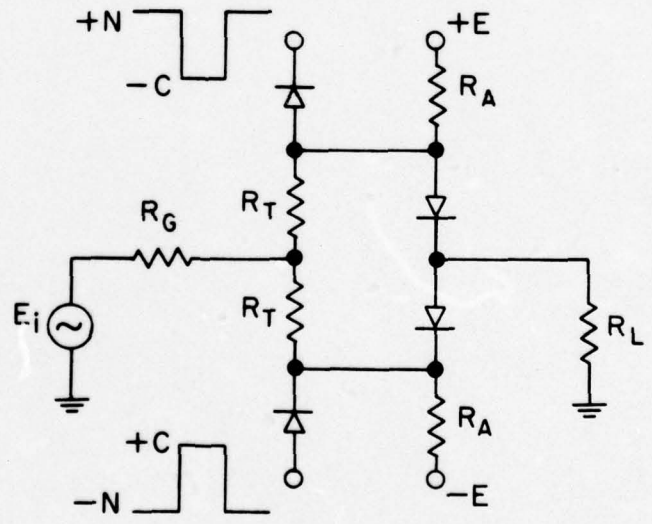
[34] J. Millman and T. H. Puckett, "Accurate Linear Bidirectional Diode Gates," Proceedings of the IRE, Vol. 43, January, 1955, pp. 27-37.

[35] op. cit., p. 33.



a. CIRCUIT OF TWO-DIODE BRIDGE GATE



b. CIRCUIT OF FOUR-DIODE BRIDGE GATE

FIGURE 11

DIODE BRIDGE GATES

gates are given below:

$$G = \frac{1}{1 + \frac{R_g + R_f}{R_L} + \frac{2R_g + R_f}{R_V}} , \tag{4-1}$$

$$L = \frac{2R_L R_f}{R_r^2} , \tag{4-2}$$

$$U(E) = \frac{R_g + \frac{R_f}{2}}{R_V} , \tag{4-3}$$

$$C_{min} = E_i , \tag{4-4}$$

$$N_{min} = E_i + \frac{ER_f}{R_V} , \tag{4-5}$$

$$E_{min} = E_i\left(2 + \frac{R_V}{R_L}\right) , \tag{4-6}$$

$$I_{Cs} = \frac{E_i + C}{R_r} , \text{ and} \tag{4-7}$$

$$I_{Ns} = \frac{N + E}{R_V} , \tag{4-8}$$

where G is the gain of the six-diode gate,

L is the leakage of the six-diode gate when nonconducting,

$100\,U(E)$ is the per cent dc unbalance of the gate,

R_f is the resistance of forward biased diode,

R_r is the resistance of reverse biased diode,

I_{Cs} is the switching current when the gate is on, and

I_{Ns} is the switching current when the gate is off.

Subscript min means minimum value of quantity. Other symbols are defined in Fig. 2.

The voltage, E, is chosen to be 105 volts, and the value of both C and N is chosen to be 20 volts. The output load resistor is chosen to be 10 K. A reasonable value of bias current results for a value of 110 K for R_V. The values of the above parameters as calculated from Equations 4-9 through 4-13 are given below:

$$E_i = 8.1 \text{ volts}, \tag{4-9}$$

$$G = 0.96, \tag{4-10}$$

$$(E) = 1.82 \times 10^{-3}, \tag{4-11}$$

$$I_{Cs} = 28 \text{ } \mu\text{amps}, \text{ and} \tag{4-12}$$

$$I_{Ns} = 1.13 \text{ ma}. \tag{4-13}$$

The maximum value of E_i is controlled by Equation 4-6. The attenuation of the gate is negligible. Of particular interest in determining an approximate dynamic range is the value of dc unbalance which sets the lower limit and the maximum signal voltage as determined in this case by 4-6. From this maximum signal level and the dc unbalance the dynamic range may be predicted. If the unbalance in E is two volts, the dc pedestal is about 3.6 mv. A dynamic range of approximately 66 db may be expected. The current which must be supplied by the transistor switch is calculated from Equations 4-7 and 4-8. This current is small enough to neglect in the analysis of the transistor switch.

The amplitudes of the various potentials and pulses used in the transistor switch have been set in other sections of the design. The following design uses the potentials previously specified, viz. V_{cc} = 20 volts and the switching pulses have levels of + 20 and - 20 volts. The negative switching level is actually 21.5 volts in order to drive the common-collector switch into saturation. The circuit diagram of the switch is shown in Fig. 6.

To simplify, choose R_{Le} equal to R_{Lc}. A value of 4.7 K for the load resistors results in a saturation current of 8.5 ma, which is high enough to prevent serious loading when the six-diode gate is connected. The RC time constant is 0.52 microseconds using a value of 110 pf for the collector capacity. A base current which will drive the common-emitter transistor into saturation must be used. Using a minimum current gain of 40 and an overdrive factor of 2, the value of base current required is 0.4 ma. The base resistor R_{Be} may be calculated from the maximum switching voltage and the base current:

$$R_{Be} = \frac{2V_{CC}}{I_B} = \frac{40}{0.4} = 100 \text{ K}. \qquad (4\text{-}14)$$

As long as the rise and fall times of the common-emitter and common-collector switch are less than about one microsecond, the switching transient in the output of the six-diode gate may be neglected. Such short transients may be filtered to reduce the amplitude. The main factor to be considered is the storage time since it may last several microseconds. The transient resulting from the differences in storage times of the two configurations may be eliminated by setting the storage times equal. By setting the logarithm terms of Equations 3-25 and 3-26 equal, the storage times for the two configurations are made equal. The storage time for the common-collector will be shorter than that of the common-emitter for the voltages given. Reduction of the common-emitter storage time is accomplished by the addition of a reverse bias during the turn-off transient. The reverse bias is supplied from the series combination of V_R and R_{Re} shown in Fig. 6. The value of V_R is 6 volts and R_{Re} is 220 K, which gives a reverse bias current of 0.0272 ma. This is the value of I_{B2} to be used in the calculation of the fall time and the storage time. The above values are used to calculate the storage time of the common-emitter switch. The value

of R_{Bc} for the common-collector switch is then chosen to make the storage times of the two configurations equal. After all circuit values are specified, the rise and fall times may be calculated from Equations 3-12, 3-13, 3-23, and 3-24. If the values are sufficiently short, the design is complete. If they are too long, a revision in the circuit design is necessary. A reasonable amount of judgment will allow a choice of circuit values which are mutually compatible to the requirements stated previously.

The storage time for the common-emitter switch calculated from Equation 3-25 is 1.82 microseconds. The value of R_{Bc} may be calculated by setting the logarithm terms of Equations 3-25 and 3-26 equal. The value of R_{Bc} for equal storage times is 4.66 K. A value of 4 K is used in the circuit.

The rise and fall times of the two configurations are calculated from Equations 3-12, 3-13, 3-23, and 3-24. The measured value of the time constants are as follows:

$$\frac{R_{Le}\, C_c (r_b + r_e)}{(1 - \alpha_N) r_b + r_e} = 0.5 \text{ microsecond, and} \qquad (4\text{-}15)$$

$$\frac{R_{Lc}\, C_c (R_{Bc} + R_{Lc})}{R_{Bc}\left(1 - \alpha_N + \frac{R_{Lc}}{r_c}\right) + R_{Lc}} = 0.6 \text{ microsecond.} \qquad (4\text{-}16)$$

Since the small signal base resistance becomes very small for high frequencies, Fquation 4-16 simplifies to $R_{Le}\, C_c$. The measured value of 0.5 and calculated value of 0.52 microseconds agree very closely. The calculated value of the common-collector time constant is 0.94 microsecond, which is in error with the measured value. The error can easily be attributed to variation from the mean value of current gain.

The calculated value of the switching times are given below:

Common-Emitter Switch

Rise Time: 0.43 microseconds

Fall Time: 0.80 microseconds

Common-Collector Switch

Rise Time: 0.92 microseconds

Fall Time: 0.92 microseconds.

C H A P T E R V

MEASUREMENTS

This chapter presents the measurements made on the six-channel gate. Figures 12 and 13 show the front and bottom view of the completed gate. All of the waveforms shown were photographed from a Tektronix Type RM-31-A oscilloscope.

Figure 14 shows the switching output of the transistor switch. The amplitude of the output pulses of the switch are as predicted, the output of the common-emitter section being 40 volts and the output of the common-collector section 38 volts. The lower voltage of the common-collector configuration is expected since it is not driven as far into the saturation region as the common-emitter switch.

The rise and fall transients of the switch are shown in Fig. 15. The rise and fall times are measured from the 10 to 90% amplitude points. The values measured from Fig. 15 are compared to the calculated times given in Chapter IV in the following tabulation:

	Calculated Times (microseconds)	Measured Times (microseconds)
Common-Emitter		
Rise	0.43	0.54
Fall	0.80	0.96
Common-Collector		
Rise	0.92	1.04
Fall	0.92	0.56

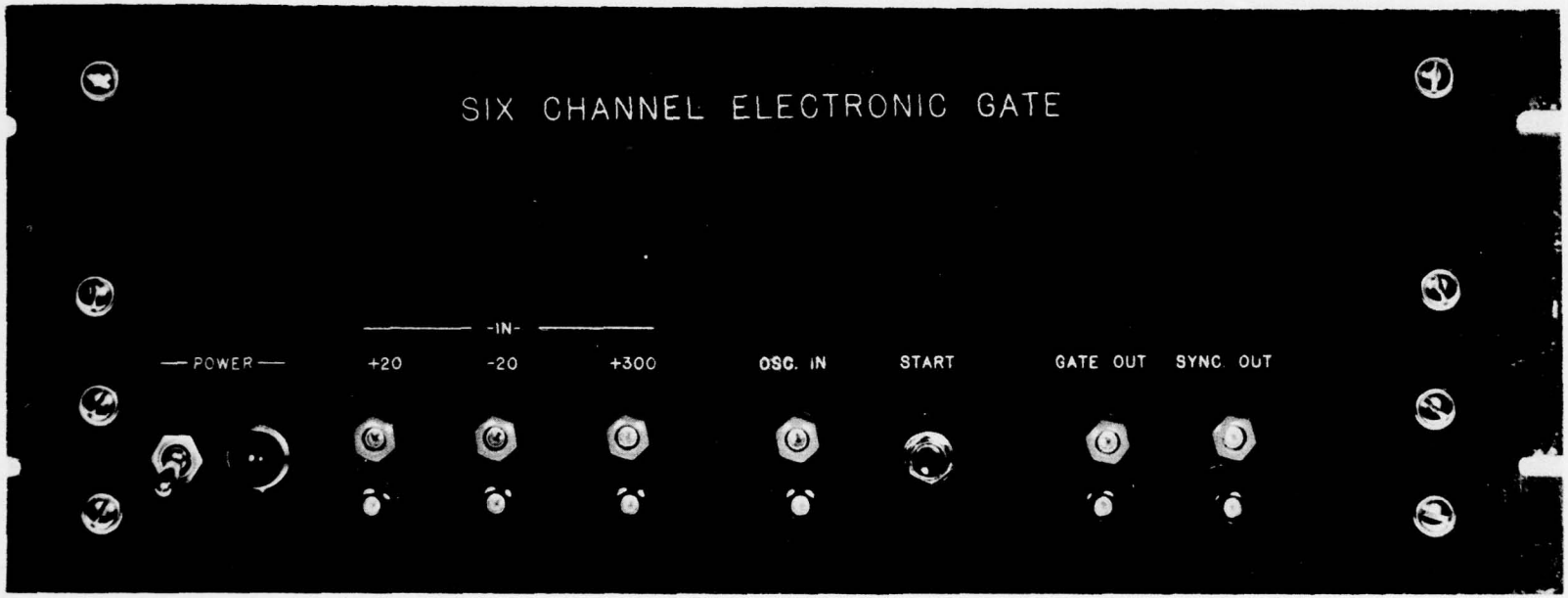


FIGURE 12
FRONT VIEW OF SIX-CHANNEL GATE

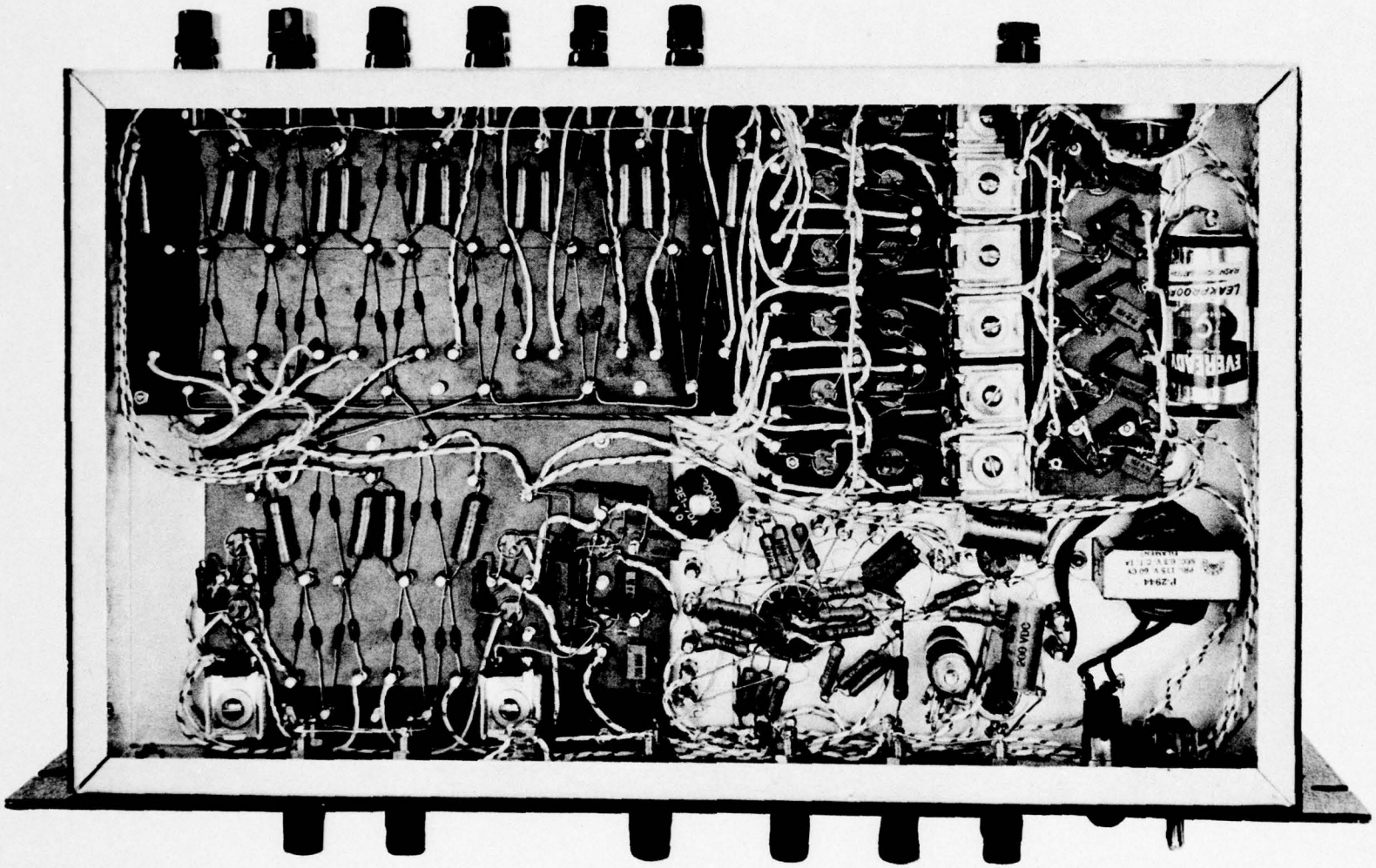
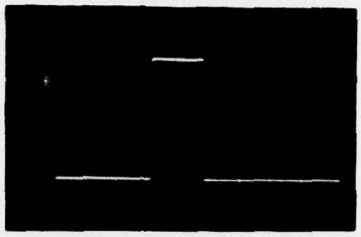
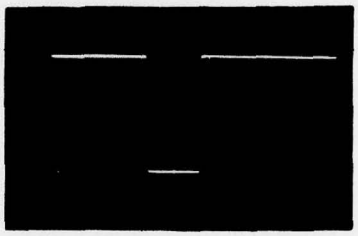


FIGURE 13
BOTTOM VIEW OF SIX-CHANNEL GATE



a. COMMON EMITTER SWITCH
OUTPUT WAVEFORM.

VERTICAL SCALE: 10V/DIV.
HORIZONTAL SCALE: 50μSEC/DIV.



b. COMMON COLLECTOR SWITCH
OUTPUT WAVEFORM.

VERTICAL SCALE: 10V/DIV.
HORIZONTAL SCALE: 50μSEC/DIV.

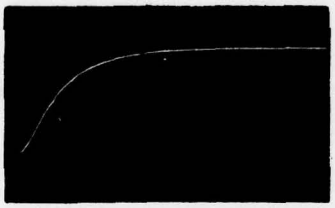
FIGURE 14
OUTPUT WAVEFORMS OF TRANSISTOR SWITCH

a. RISE TIME OF COMMON EMITTER SWITCH.

VERTICAL SCALE: 10V/DIV.
HORIZONTAL SCALE: 0.1μSEC/DIV.

b. FALL TIME OF COMMON EMITTER SWITCH.

VERTICAL SCALE: 10V/DIV.
HORIZONTAL SCALE: 0.2μSEC/DIV.



c. RISE TIME OF COMMON COLLECTOR SWITCH.

VERTICAL SCALE: 10V/DIV.
HORIZONTAL SCALE: 0.5μSEC/DIV.

d. FALL TIME OF COMMON COLLECTOR SWITCH.

VERTICAL SCALE: 10V/DIV.
HORIZONTAL SCALE: 0.2μSEC/DIV.

FIGURE 15
SWITCHING TIMES OF TRANSISTOR SWITCH

All switching times are of the order of one microsecond as was required in the design procedure. This is accomplished with very inexpensive transistors in the medium frequency range. The use of higher frequency transistors and non-saturated switching would result in considerable decrease in the switching times.

The switching times for the common-emitter are well within the accuracy of the approximations made and the variation between transistors. The values used in the calculations were average for the transistors used. The value of the rise time of the common-collector configuration is also within the allowable error due to transistor parameter variation. The reason for the measured value of the fall time of the common-collector stage being smaller than the calculated value can possibly attributed to the effect of a reverse bias caused by the potential difference from the base to the switch input. The effect of this reverse bias will be less as the base voltage decays. For the previously stated purposes, however the calculated value is close enough.

Figure 16 shows the noise output of the gate with no signal inputs. The dc unbalance and the widest switching spikes are to be considered the switching noise. As previously, the switching spikes on the order of one microsecond may be neglected. The output noise is less than 25 mv considering the wider transients as noise. The maximum output voltage is 7.5 volts; therefore, the output dynamic range is about 50 db. The minimum noise predicted is not achieved, but the resultant dynamic range is still well within the acceptable range.

Figure 17 shows a single output dc pulse applied to the third channel of the gate. The dc value of the input was 5.7 volts compared to 5.5 volts at the output which corresponds to a gain of 0.965 for two six-diode gates in series. This compares favorably to the calculated value of gain, 0.96, as calculated from Equation 4-10.

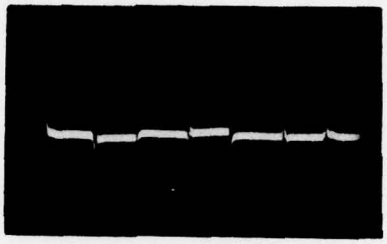


FIGURE 16
OUTPUT SWITCHING NOISE OF SIX-CHANNEL GATE
WITH NO INPUT SIGNALS

VERTICAL SCALE: 0.025V/DIV.
HORIZONTAL SCALE: 50μSEC/DIV.

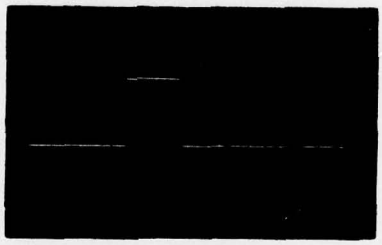


FIGURE 17
OUTPUT OF SIX-CHANNEL GATE WITH DC SIGNAL
APPLIED TO THIRD CHANNEL

VERTICAL SCALE: 2.5V/DIV.
HORIZONTAL SCALE: 50μSEC/DIV.

Figure 18 shows a typical output switching spike. The width of the spike is less than one microsecond, which was predicted in earlier chapters.

Typical output signals for high and low levels are shown in Fig. 19. In the low level case signals do not affect adjacent channels.

FIGURE 18
OUTPUT SWITCHING VOLTAGE SPIKE OF SIX-CHANNEL GATE ON EXPANDED SCALE

VERTICAL SCALE: 0.25V/DIV.
HORIZONTAL SCALE: 0.5μSEC/DIV.

a. HIGH LEVEL OUTPUT WITH NO INPUT ON FOURTH CHANNEL.

VERTICAL SCALE: 2.5 V/DIV.
HORIZONTAL SCALE: 50μSEC/DIV.

b. LOW LEVEL OUTPUT WITH NO INPUT ON FOURTH CHANNEL.

VERTICAL SCALE: 0.1 V/DIV.
HORIZONTAL SCALE: 50μSEC/DIV.

FIGURE 19
OUTPUT OF SIX-CHANNEL GATE WITH SEVERAL DC INPUTS

CHAPTER VI

CONCLUSIONS

From the results of the measured data, a multichannel, linear gate for dc signals with a dynamic range in excess of 40 db appears feasible by using six-diode gates and transistor switching circuits. The transistor switches may use medium-frequency, low-cost transistors if small switching spikes of less than one microsecond duration are tolerable. By using higher frequency switching transistors and non-saturated switching, the switching noise can probably be reduced by approximately a factor of ten in both amplitude and width. Many arrangements of the gates may be used to obtain the number of channels desired and also to reduce the noise output. The gates may also be used without modification for sampling ac signals of the proper frequency range.

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