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A LEVEL DENSITY ANALYZER FOR SHIPBOARD RFI MEASUREMENTS,(U)
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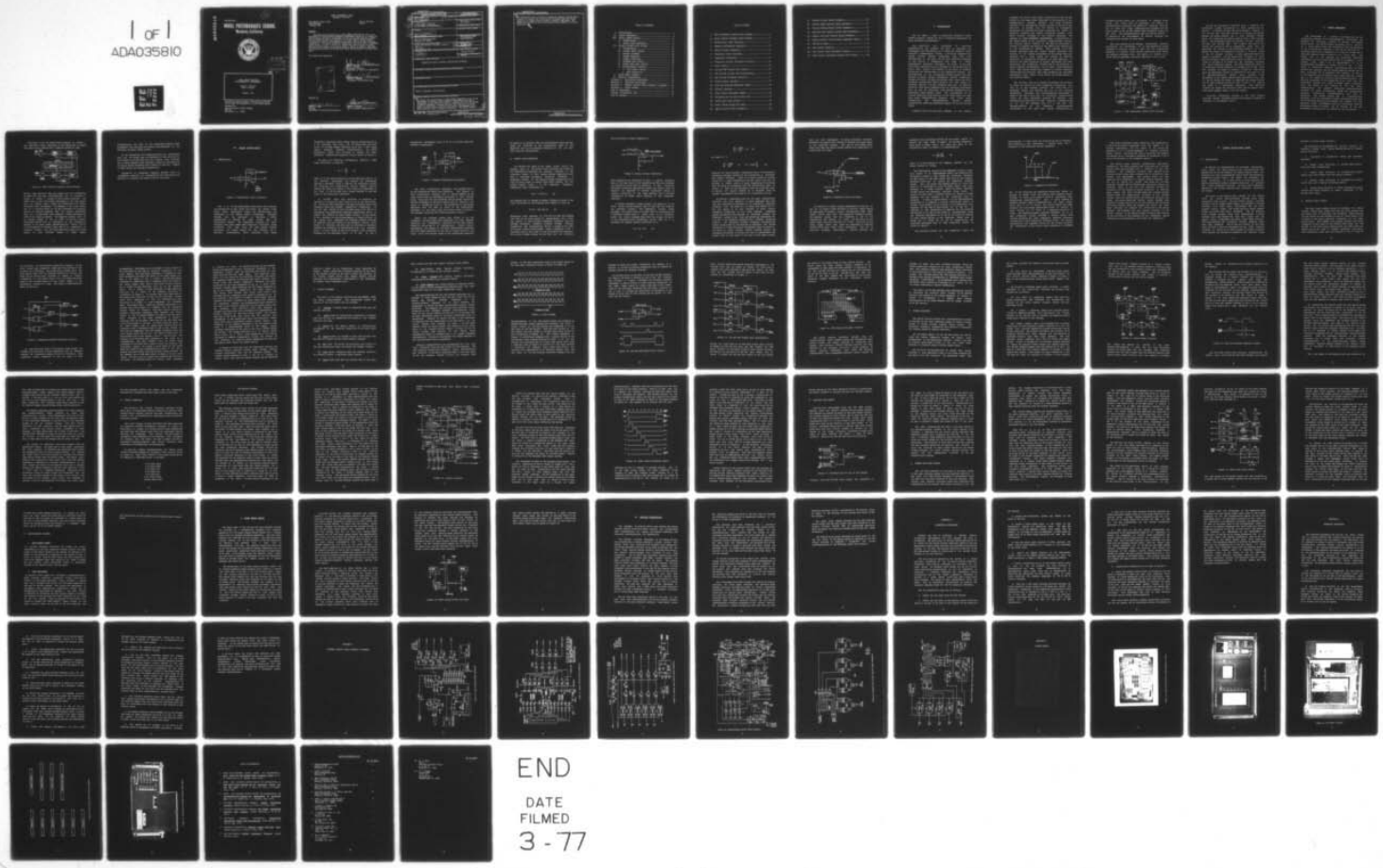

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Monterey, California

A LEVEL DENSITY ANALYZER FOR SHIPBOARD RFI MEASUREMENTS

Dennis C. Arneson
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October 1976

Approved for public release: Distribution unlimited
A task under the Shipboard RFI in UHF SATCOM Project

Prepared for:

Naval Electronic Systems Command
PME 106
Washington, D.C. 20302

NAVAL POSTGRADUATE SCHOOL
Monterey, California

Rear Admiral Isham Linder
Superintendent
1 October 1976

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ABSTRACT

The design and construction of a LEVEL DENSITY ANALYZER for use in the measurement of shipboard RADIO FREQUENCY INTERFERENCE consisted of integrating various analog and digital integrated circuits and related electronic components to enable accurate level analysis of a broad range of analog signals including noise and/or electromagnetic waves which constitute radio frequency interference. The overall design and system goals were to be able to adequately sample an analog signal, classify it, convert the classification to digital data and provide outputs to be logged either by manual or magnetic tape means. The design and construction efforts efficiently and economically achieved these goals.

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UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER: NPS-62DL76107	2. GOVT ACCESSION NO. / 3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle): A LEVEL DENSITY ANALYZER FOR SHIPBOARD RFI MEASUREMENTS	5. TYPE OF REPORT & PERIOD COVERED: Task report
	6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s): Dennis Calvin/Arneson John E./Ohlson	8. CONTRACT OR GRANT NUMBER(s)
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Naval Postgraduate School Monterey, CA 93940	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: N0003976WRT9053
11. CONTROLLING OFFICE NAME AND ADDRESS: Naval Electronic Systems Command PME 106 Washington, D.C.	12. REPORT DATE: October 1976 13. NUMBER OF PAGES: 83
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): 86p.	15. SECURITY CLASS. (of this report): Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Radio Frequency Interference

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The design and construction of a LEVEL DENSITY ANALYZER for use in the measurement of shipboard RADIO FREQUENCY INTERFERENCE consisted of integrating various analog and digital integrated circuits and related electronic components to enable accurate level analysis of a broad range of analog signals including noise and/or electromagnetic waves which constitute radio frequency interference. The overall design

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I. INTRODUCTION

Why is there a need to design and construct a Level Density Analyzer System for use in shipboard measurement of Radio Frequency Interference?

The relatively new technology of satellite communications has prompted the Navy to implement the development and installation of a viable and effective Fleet Satellite Communication System. A satellite communication system affords several advantages that have been unrealizable in the past, and the most important advantage is the ability to communicate long range to remote geographical positions throughout the world. In the past long range communications has depended on the HF spectrum in which radio signals are subject to the effect of numerous variations and disturbances in the propagation channel. The perturbations in the propagation channel result from such effects as sunspot cycles, ionospheric density variations, weather activity, man-made background noise levels and radio frequency interference (RFI) caused by the vast number of emitters sharing the high frequency spectrum. In addition effective long range communications was generally maintained only by use of relatively high powered transmitters and physically large antenna sites. The introduction of an orbital satellite relay station, on the other hand, has made long range communications possible with lower power transmitters and correspondingly smaller antenna installations radiating modulated signals in the UHF and SHF bands.

Communications via satellite, however, is not without

problems. The use of lower power tranmsitters at UHF and SHF results in very small power densities at the antennas of the communications receiver systems. The large distances involved in the propagation channel (ground to satellite and satellite to ground) plus the effects of atmospheric scattering and attenuation greatly challenge the design of sensitive receiver and signal processing systems. With these inherent problems at the receive terminals the presence of RADIO FREQUENCY INTERFERENCE is detrimental to the effectiveness of the satellite communications system. The sources and/or effects of RFI must be controlled or reduced to increase and maintain the quality and reliability of the communications system. This problem is of even greater importance when the ground receive terminals are located in the closed environment of Navy ships which are equipped with a large number and variety of emitters operating at frequencies throughout the radio spectrum. In addition the close proximity of motors, generators and other electrical and mechanical systems add to the potential of radio frequency interference. All of these electromagnetic field (EM) sources potentially combine to produce undesired intermodulation products, high order harmonics and increased background noise levels which reduce the effectiveness of the receiver system.

The problem then is to develop procedures and hardware to reduce the effects of radio frequency interference; and, just as in any problem solution, the first step is to carefully define the problem and all of the relating parameters. Therefore the electromagnetic environment of ships at sea and in port must be accurately characterized within the radio frequency spectrum of interest. The frequency band available for Navy satellite communications is in the UHF spectrum from 240 to 400 MHz. The characterization of the shipboard electromagnetic environment in this band must include determination of

background noise levels, the statistics of impulse noise levels and their rate of occurence, the effects of intermodulation products, the effects of spectrum splatter due to radar and other communications equipment and the power levels of HF and VHF higher order harmonics within the UHF band. The characterization must be further divided to include the EM environments of several selected and representative classes of Navy ships.

This work reports on the design, contruction, testing, application and maintenance of an instrumentation system designed to provide a source of data for the statistical analysis of impulse noise levels, background noise levels and impulse occurrence rate. The system is defined as a LEVEL DENSITY ANALYZER, hereafter referred to as an 'LDA'.

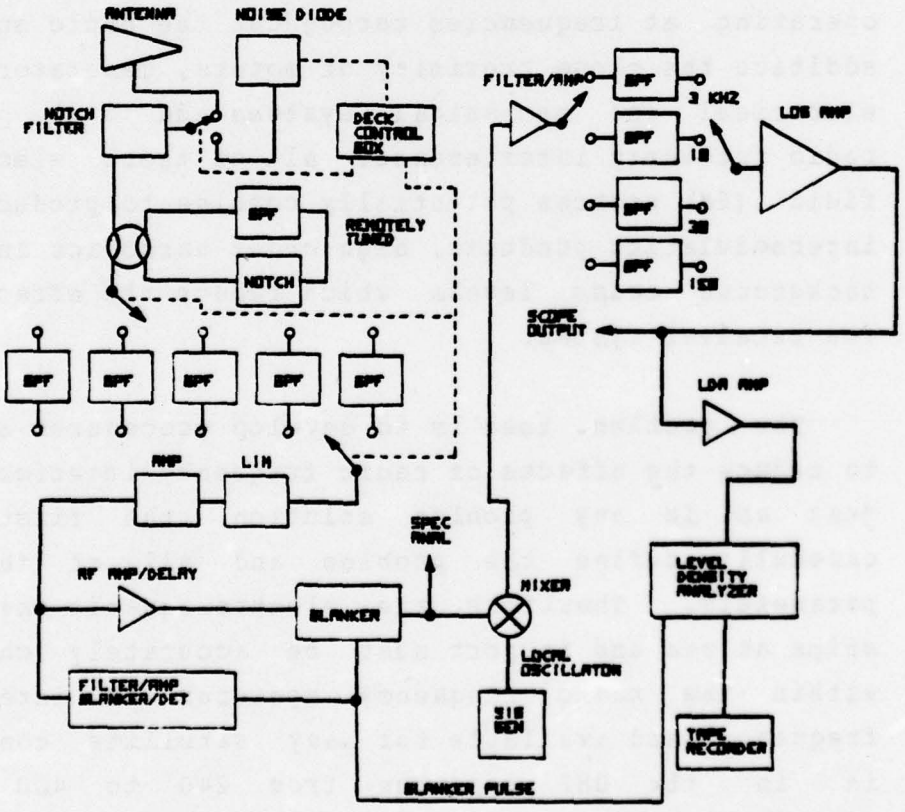


Figure 1. RFI Measurement System Block Diagram.

The LDA was designed to interface with a complete RFI Measurement System illustrated in block diagram form in Figure 1. Following through the block diagram, signals in the 240-400 MHz band are received by a conical log spiral antenna and passed through one of five bandpass filters which are selectable by remote control from a 'Deck Control Box'.[1] The selectable bands are 240-272, 272-304, 304-336, 336-368, and 368-400 MHz. The signals from one of the filters are coupled to the RF preamplifier where they are amplified and cabled to the RF/Blanker System.[2] In the RF system the signal is processed to provide a blanking pulse to the RF channel whenever a large amplitude pulse-like signal is received. The RF system also receives an input from an external local oscillator which is mixed with the RF signal to provide an IF signal for the blanking circuitry and the IF Amplifier System. The local oscillator which is a synthesized signal generator is normally set 30 MHz below the incoming RF signal to produce a 30 MHz IF. The signal from the RF/Blanker System is connected to the input of the IF Amplifier/Detector System[3] which provides final processing of the signal before being connected to the LDA. In the IF system the signal is amplified and passed through one of three bandpass filters--3 KHz, 10 KHz or 30 KHz--to the input of a logarithmic amplifier. This amplifier detects the signal and provides a band limited signal with a very broad dynamic range to the LDA System.

Pictorial information related to the Level Density Analyzer System including photos and schematic diagrams is contained in Appendixes C and D.

II. DESIGN PARAMETERS

The development of a system to provide data for the statistical analysis of an electromagnetic environment has mandated the following criteria to achieve the desired design goals. The system signal processing had to function on a video signal which was processed by the log amplifier of the IF system and connected to the LDA in the form of a baseband signal with a bandwidth of 1.5 KHz to 15 KHz and an amplitude dynamic range of from 0 to 7.5 volts peak. The signal had to be sampled and accurately amplitude classified, and the classification had to encompass a wide dynamic range from 0 up to approximately 50 dB in predetermined increments of either 3 dB or 10 dB. A wide range of selectable sampling time periods from 1 to 1000 seconds was required, and the system sampling process had to have provisions for an automatic 'run' feature. At the end of the sampling cycle resultant data output from the system had to be logged by a digital tape recording system. The physical parameters of the system had to be such that the instrument package was light in weight, small in physical size, and immune to the effects of RFI and power interruptions. The desired electrical characteristics included low power consumption, noise and interference immunity, reliability, maintainability and ease of operation. The system finally had to electronically interface with the IF/Detector Signal Processing System and the RF Blanking System which reduced the effects of high amplitude pulse interference such as a high power radar by developing pulses to 'blank' the RF channel of the RFI Measurement System and to be counted by the LDA System.

Referring to the LDA system block diagram in Figure 2 the specified basic operation of the system was to sample the input analog signals for a selected period of time.

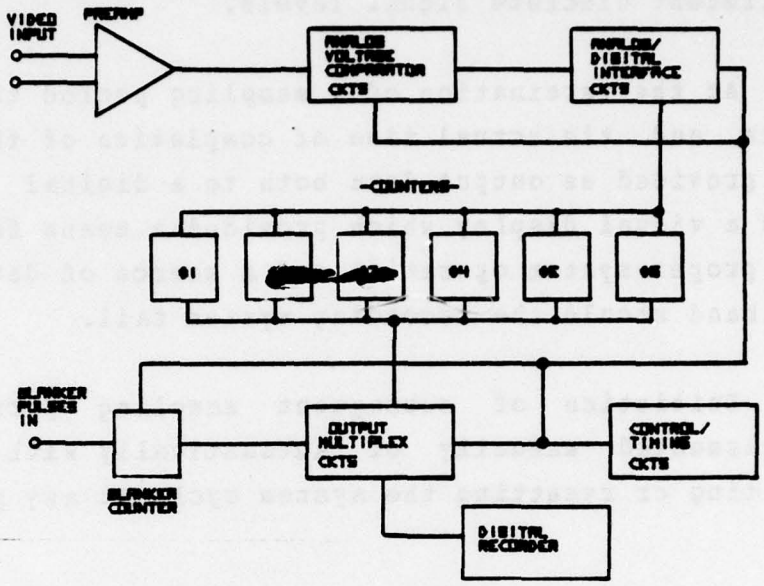


Figure 2. Level Density Analyzer Block Diagram.

During this period of time each sample was to be classified by amplitude, and each classification was to generate a signal to enable a series of fixed period counters. The effect was to count the actual percentage of the time period that the analog input signal was determined to be within specified level increments. For example if the input signal was at a constant level of -50 dBm throughout the sampling period, it would be expected that the counter associated with the -50 dBm level would display a number representing 100% of the sampling period. The sampling periods were to be integer powers of ten in order to provide a direct percentage readout and an indication of the probability density of the input signal characteristics. Either 3 dB or 10 dB increments of dynamic range were to be selectable by external control, and the dual selection capability would result in five discrete levels of input signal

discrimination for each of the selectable dynamic range increments thus providing an overall discrimination of ten different discrete signal levels.

At the termination of a sampling period the accumulated data and the actual time of completion of the cycle was to be provided as output data both to a digital tape recorder and a visual display which provided a means for verification of proper system operation and a source of data for logging by hand should the recording system fail.

Initiation of subsequent sampling periods could be implemented manually or automatically with provisions for halting or resetting the system cycle at any point.

III. ANALOG SYSTEM DESIGN

A. PREAMPLIFIER

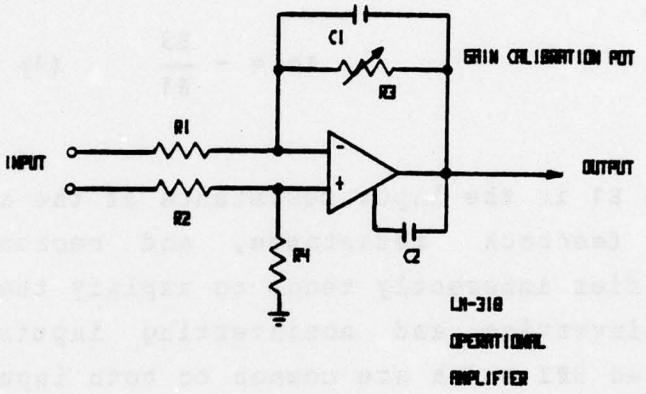


Figure 3. Differential Input Amplifier.

The 0 to 15 KHz logarithmic bandlimited input signals are susceptible to RFI, power line noise and ground loops which might drastically reduce the effectiveness and efficiency of the system signal processing; therefore extreme care was exercised in designing a buffer preamplifier to amplify the input signal from the IF/Detector System. The parameters required for input buffering were high common mode rejection, relatively large bandwidth, fast slew rate, and good supply voltage rejection. The device chosen for this function was a National Semiconductor LM318 precision high speed

operational amplifier which offers typical specifications of a 50 volt/usec slew rate, 100 dB common mode rejection ratio, 80 dB power supply rejection ratio and a 1 MHz large signal frequency response characteristic. The LM318 application notes[4] were utilized to develop the input buffering differential amplifier circuit shown in Figure 3.

The gain of an inverting differential amplifier under ideal conditions is given by:

$$Ao = - \frac{R3}{R1} \qquad (1)$$

where R1 is the input resistance of the amplifier and R3 is the feedback resistance, and because the operational amplifier inherently tends to amplify the difference between the inverting and noninverting inputs; signals such as induced RFI which are common to both inputs are amplified on the order of 100 dB less than a signal applied to only one input of the operational amplifier.

To achieve unity gain according to equation (1) resistors R1 through R4 were chosen to be of the same value. R1, R2 and R4 were available 7.68 Kohm precision metal film resistors which have minimal temperature coefficients. R2 and R4 were chosen to have the same value as R1 and R3 in accordance with operational amplifier application notes[4] to reduce the effects of input offset current. R3 was chosen to be a variable 20 turn potentiometer to enable setting in the system gain. Bypassing the feedback resistor provided an effective low pass filter in the feedback circuit which tended to decrease the gain with an increase in frequency reducing the potential of interference from high frequency noise. C1 had a value of 820 pf to provide a flat frequency response for the amplifier from 0 to 26 KHz. C2 was a

manufacturer recommended value of 10 pf to provide amplifier feedback compensation.

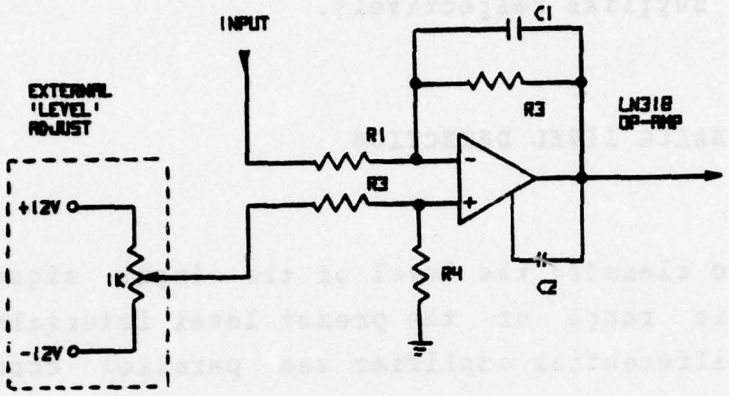


Figure 4. Summing Differential Amplifier.

The input differential amplifier was cascaded with a second differential unity gain amplifier. The purpose of this differential function was to enable summing of the input signal with an externally controlled DC bias voltage which controlled the LDA threshold during normal operation. Further reference to the Bias Control and its function are found in Appendices A and B. The parameters of the second amplifier were the same as those of the differential amplifier at the input, thus the circuit shown in Figure 4 was designed utilizing the LM318 application notes.[4]

Again all resistor values were chosen to be the available 7.68 Kohm metal film resistors, and the feedback capacitor and compensation capacitor had the same nominal values of 820 pf and 10 pf respectively. Actual circuit performance was similar to the input differential amplifier with the added capability to set the DC output level at any point within the dynamic range of the operational amplifier

by means of an external 1000 ohm potentiometer which had the wiper arm connected to the noninverting input of the amplifier and the end terminals connected to the ±12 volt power supplies respectively.

B. ANALOG LEVEL DETECTION

To classify the level of the input signal within the dynamic range of the preset level intervals the output of the differential amplifier was parallel connected to the inverting inputs of five analog voltage comparators each with a specified calibrated switching threshold. A necessary quality of the analog voltage comparators was a high switching speed to enable rapid state changes for any analog signals within a 15 KHz bandwidth. Assuming a sinusoidal input represented by:

$$V(t) = A \sin \omega t \qquad (2)$$

the maximum rate of change of signal voltage is given by the first derivative of the function with respect to time as:

$$V'(t) = \omega \cdot A \sin \omega t \qquad (3)$$

Evaluating this function at t=0 and f=15 KHz the maximum slew rate of the input signal is approximately 94.2 volts per second or .0942 mV/usec. Assuming, therefore, that the minimum comparator threshold interval between adjacent comparators was approximately 168 mV, a change of of .0942 mV is only .056% of each window. Thus a comparator with a switching time on the order of one microsecond was adequate. The circuit element chosen on this basis was the Fairchild

uA734 precision voltage comparator.[5]

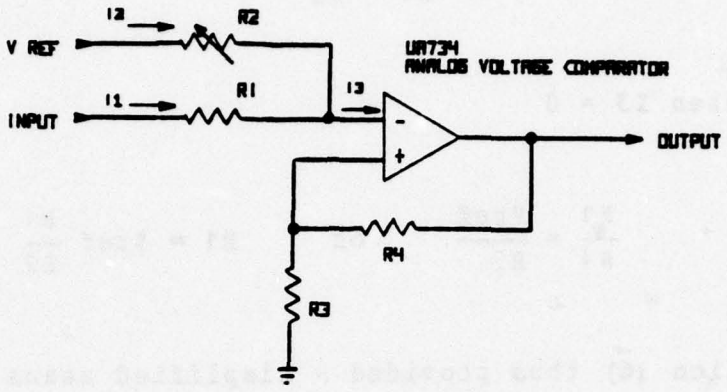


Figure 5. Analog Voltage Comparator.

This comparator was specified to have a typical switching time of 320 nsec with a 2 mV overdrive and was thus suitable for conversion rates well in excess of 15 KHz. Utilizing published comparator application notes[6] the circuit shown in Figure 5 was designed to provide calibrated analog to digital conversion of the input signals, and it included 'hysteresis' for added noise immunity in the comparator circuits.

A voltage comparator simply answers the question: Is the input signal current greater than or less than the value of the reference current? The comparator circuit shown produces one output level (0 volts) when I3 is positive and a different output level (7 volts) when I3 is negative. Since the circuit changes state with the change of sign of I3 the comparison point (threshold) occurs when I3 = 0. Assuming the summing junction potential is 0:

$$I1 = I2 + I3 \qquad (4)$$

$$\frac{E1}{R1} = \frac{Vref}{R2} + I3 \quad (5)$$

and when I3 = 0

$$\frac{E1}{R1} = \frac{Vref}{R2} \quad \text{or} \quad E1 = Vref \frac{R1}{R2} \quad (6)$$

Equation (6) thus provided a simplified means of determining necessary component values for any combination of reference and signal voltages. There is an error caused by voltage offset due to input differential current offset that may be reduced to almost zero at a given temperature by ensuring that the value of resistance from the noninverting input to ground is equal to the resistance from the inverting input to ground. For circuit design R1 in parallel with R2 closely approximated the value of R3 in parallel with R4.

To provide a reasonable load for the input differential amplifier and also maintain an input impedance much less than the differential impedance of the comparator, precision resistors with the value of 11.5 Kohms were chosen for R1, and the values of R2 were variable to allow circuit threshold calibration at any level desired. Increased system flexibility was realized by switching between two different values of R2. Thus the system was calibrated for 3 dB and 10 dB threshold intervals with external selection control. The switching between different intervals was easily accomplished by utilization of miniature DIP relays connected in a SPDT switching arrangement shown in Figure 6. The choice of using printed circuit mounted relays was extremely desireable to obviate the need to interconnect the signal lines by long wires to and from a front panel switch,

thus the only requirement to change comparator threshold intervals was wiring and a switch to connect the relay coils to the operating voltage. The use of long signal wires would have made the entire analog system very susceptible to induced RFI and noise.

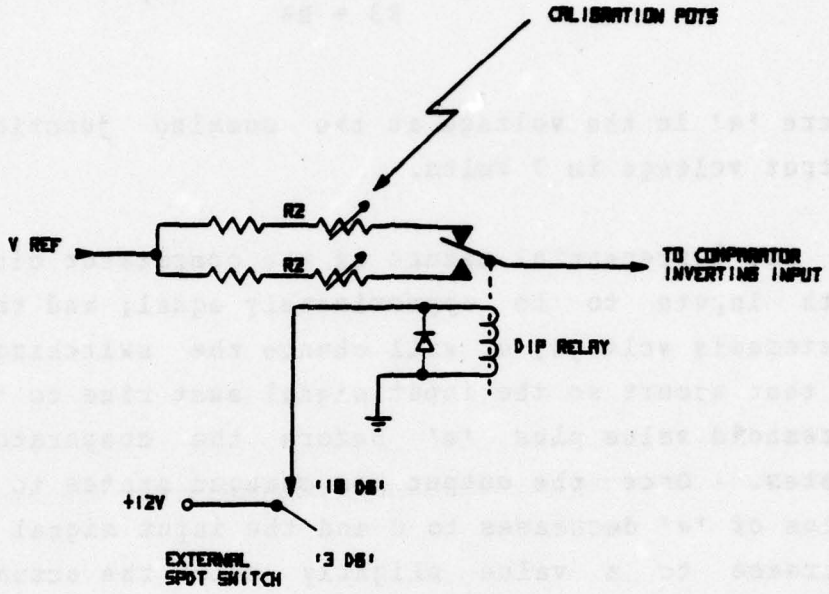


Figure 6. Comparison Point Switching.

In addition to offset voltage compensation resistors R3 and R4 in Figure 5 were utilized to provide a small degree of hysteresis to prevent circuit oscillations when input signal levels were near the comparator threshold points. For example, assume that the threshold of one of the comparators was exactly 2.0 volts, and the level of the input signal was also very near 2.0 volts. Any noise on the input signal would then cause the comparator to randomly switch states with noise level variations. The use of positive feedback (hysteresis), however prevents the

comparator from switching between the two output states at exactly the same level of input. If the high comparator ouput state is seven volts, the level fed back to the noninverting input in Figure 5 is determined by:

$$e = \frac{7 \cdot R3}{R3 + R4} \qquad (7)$$

where 'e' is the voltage at the summing junction and the output voltage is 7 volts.

The differential nature of the comparator circuit causes both inputs to be approximately equal; and therefore the hysteresis voltage, e, will change the switching threshold by that ascurt so the input signal must rise to the original threshold value plus 'e' before the comparator switches states. Once the output has changed states to 0 volts the value of 'e' decreases to 0 and the input signal must then decrease to a value slightly below the actual threshold voltage before the comparator switches states again. It should be noted that a tradeoff between the degree of noise immunity and the accuracy of the comparison point is required. A value of approximately 3 mV was experimentally determined to be adequate to prevent 'chattering' caused by system noise levels; and to realize a 3 mV hysteresis loop, equation (7) was used to find values for R3 and R4. In addition to the constraints of equation (7), the parallel combination of R3 and R4 was forced to approximately equal the parallel combination of R1 and R2 to reduce the effects of input offset current, so the resultant values were 22 Mohms and 9.1 Kohms for R4 and R3 respectively. The resultant hysteresis loop of each comparator circuit is shown in Figure 7.

The reference voltage for the comparator inputs was

approximately -9 volts which was obtained by use of standard size resistors, a PNP transistor, a signal diode and a Signetics LM 550 precision voltage regulator.

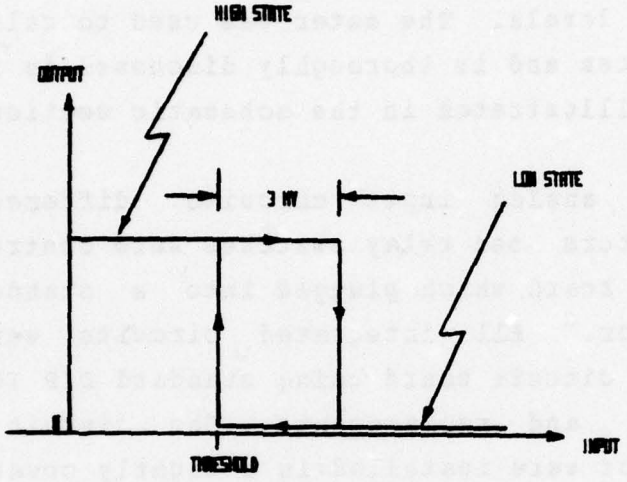


Figure 7. Comparator Hysteresis.

The -9 volt value for the reference voltage was chosen to provide an offset from the circuit input negative supply voltage, -12 volts, by at least 3 volts in accordance with manufacturer specifications.[7] Also -9 volts ensured an adequate dynamic range of comparison for the input signal level from 0 to 7.5 volts. The circuit design was taken directly from the device application notes[7] to convert an input voltage of -12 volts to a regualted output of -9 volts. The regulated output, parallel connected to R2 of each comparator circuit provided a stable ripple free voltage reference for each comparator enabling precision calibration of each comparator threshold point. The circuit configuration and component values for the voltage regualtor are illustrated in the circuit board schematics in Appendix C.

The analog comparator input signal was also connected to a low pass RC filter in parallel with the inputs to the voltage comparators, and the output of the filter was connected to a 0 to 100 microammeter to indicate relative signal levels. The meter was used to calibrate and operate the system and is thoroughly discussed in Appendices A and B and is illustrated in the schematic section.

The analog input circuits, differential amplifiers, comparators and relay switches were contructed on a printed circuit board which plugged into a standard 18 pin edge connector. All integrated circuits were mounted on the printed circuit board using standard DIP IC sockets for easy removal and replacement. The circuit board and edge connector were installed in a tightly covered aluminum box, and all DC inputs and outputs were wired into the edge connector through 1000 pf feedthrough capacitors through the aluminum walls of the box thus ensuring maximum RFI protection for the sensitive analog circuitry. In addition power supply and bias voltage leads were coupled through ferrite beads and capacitively filtered on the printed circuit board to further ensure the reduction of power line noise. The analog input and digital output signals were coaxially coupled into and out of the aluminum box utilizing semi-rigid coaxial cable and standard SMA cable and panel mount fittings for maximum RFI protection of the analog signals. The aluminum box was mounted directly on the bottom chassis of the system cabinet allowing easy removal of the top cover of the aluminum box and subsequent system calibration and maintenance (see Figure 28, Appendix D).

IV. DIGITAL SYSTEM LOGIC DESIGN

A. INTRODUCTION

To satisfy the requirements for low power dissipation, light weight and small physical size, maintainability and maximum RFI and noise immunity the system digital logic was designed with CMOS (Complimentary Metal Oxide Semiconductor) integrated circuit logic.[8] The result was extremely low power consumption, up to four volts of noise immunity and easily replaceable circuit elements consisting of socketed dual inline integrated circuits. The only other components required in the digital networks were resistors, capacitors and diodes.

The heart of the digital logic system was the MOSTEK 50395 Six Decade counter/display decoder Large Scale Integrated (LSI) circuit. The LSI counter circuit included features such as single power supply, six decades of up-down counting, lock ahead carry, multiplexed BCD and seven segment output, direct LED (light emitting diode) segment drive, and direct CMOS logic interface. Use of discrete logic counter devices would have necessitated a single counter, latch and decoder for each data digit, and the system output requirement was seven, eight digit counters. Thus approximately 168 integrated circuit elements would have been required. Use of the LSI circuit, on the other hand, provided a means of cascading two six digit counters together to obtain up to twelve digits of output requiring only fourteen LSI devices as opposed to 168 discrete logic

elements to obtain seven counters.

The selection of the MK50395 LSI circuit dictated the following general logic design specifications for planned system operation.

1. Establish an appropriate timing and frequency reference.

2. Design logic circuitry to provide count enable, latch and reset capabilities.

3. Design logic circuitry to interface the counter inputs with logic levels from the analog circuits.

4. Design logic circuitry to interface the counter output data with a digital recording system.

5. Design logic circuitry to select appropriate sample periods and enable automatic or manual operations at the system front panel.

B. DIGITAL INPUT CIRCUIT

The basic logic element chosen to interface the analog circuit output logic levels with the six digit counters was the CD4013 Dual 'D' Flip-Flop. The essential characteristic of this device is the transfer of the 'D' input state to the Q output at the time of positive transition of the input clock signal. This element thus enabled latching the analog comparator output state to the counter input gates for the period of one clock cycle ensuring that the logic state was stable during the time of counter operation (up-count). Each comparator output was tied directly to the 'D' input of

cne flip-flop. At the positive transition of phase 1 cf the clock signal each ccmparator output was then latched to the Q cutput cf a flip-flop. Each flip-flop Q output state was then logical CRed with the adjacent flip-flop Q' output, and these OR gate cuputs were utilized to enable or disable --depending cn the output state-- six, twc input NCR gates which in turn coupled phase 2 of the clock signal tc one appropriate ccunter at a time. The logic is illustrated as shcwn in Figure 8.

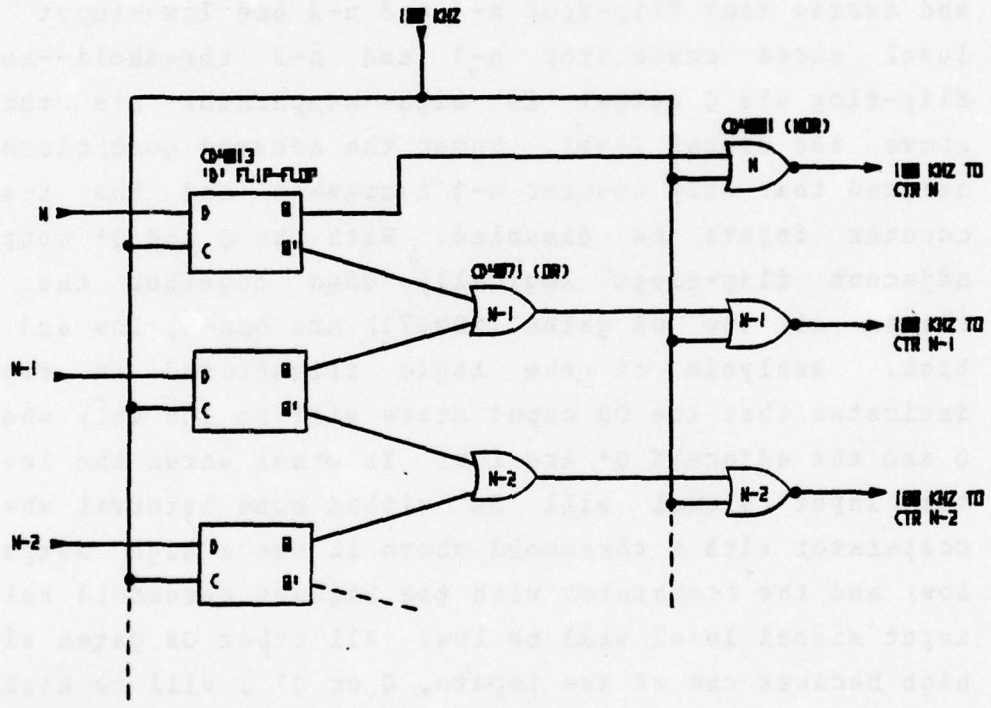


Figure 8. Ccmparator/Counter Interface Circuits.

At scme arbitrary level of the analog input signal, the threshcld of frcm zero to five ccmparators will be exceeded causing the ccmparator outputs to go to a low state. Each ccmparatcr cutput connected to the 'D' input of five

corresponding flip-flops will be latched to the Q output of the flip-flops at the time of positive transition of the clock signal. The flip-flops connected to comparators that have thresholds set below the level of the input signal will have a low state at the Q output, and the flip-flops connected to comparators with a threshold above the level of the input signal will have a high state at the Q output. The Q' output of each flip-flop will be in the opposite state. The Q output of each flip-flop is then logically ORed with the Q' output of the adjacent flip-flop as illustrated in Figure 8. To clarify this logic see Figure 8 and assume that flip-flop n-1 and n-2 are low--input signal level above comparator n-1 and n-2 threshold--and that flip-flop n's Q output is high--comparator n's threshold above the signal level. Under the assumed conditions it is desired that only counter n-1 increment and the remaining counter inputs be disabled. With the Q and Q' outputs of adjacent flip-flops logically ORed together the output states of the OR gates (CD4071) are ORn-1, low and ORn-2, high. Analysis of the logic illustrated in Figure 8 indicates that the OR ouput state will be low only when both Q and the adjacent Q' are low. In other words the level of the input signal will be within some interval where the comparator with a threshold above it has a high output (Q' low) and the comparator with the highest threshold below the input signal level will be low. All other OR gates will be high because one of the inputs, Q or Q' , will be high. The outputs of the OR gates each connected to one input of a corresponding NOR gate (CD4001) with the other input connected to the same clock signal as used for latching the flip-flops results in a phase 2 clock signal at the output when the output of the corresponding OR gate is low and a steady low state output when the OR gate output is high. In the example the n-1 NOR gate output is phase 2 of the clock signal and the n and n-2 outputs are disabled and held in a low state. The desired result is a stable count increment

in counter n-1 only. By similar analogy all six counter inputs corresponding to five flip-flops connected to the comparator outputs plus one flip-flop hard wired to a low state operated with the same logic. The flip-flop hard wired to a low state is the 'catchall' flip-flop and serves the important function of ensuring that input signals with levels below the lowest comparator threshold are still accounted for and thus classified to be in a large level interval between minus infinity and the lowest threshold of any of the comparators. Sampling of the input signal in this manner also ensured that every clock pulse that occurred during a sampling cycle would be counted by one of the counters. The choice of a phase 2 clock signal into the counters was made to prevent the input signal from changing the comparator outputs and corresponding latch outputs at the time of the positive transition of the clock signal into the counters. This condition would have resulted in multiple and erroneous count increments not representing the actual condition of the input analog signal. The latches were set on the first half cycle and the counters were incremented on the second half cycle thus ensuring a stable count cycle and a predictable counter system output. The summation of the numbers displayed in the six counter would total to a predetermined value of the sample period (seconds) multiplied by the rate of the clock (100000 pulses per second). For example selection of a 10 second period would result in a total count (summation of all counter contents) of 1000000. Consequently during the process of data reduction it would be easily determined if there was any system fault during the sample period.

It should be noted here that one additional counter, the blanker counter, received a signal input through external coaxial connections from the RF Blanking System. The blanker system operated in such a way as to produce an output pulse each time the system blanked the RF amplifier

chain as a result of an excessively large amplitude RF signal. These pulses were connected directly to the input of the blanker counter in the LDA to enable the counting of the blanker pulses during each sample period, and the resultant data represented a correlation to the statistics of impulse noise occurrence rate.

C. DIGITAL COUNTERS

The heart of the counter circuitry was the MOSTEK 50395 six digit counter/decoder. The significant inputs and outputs of the LSI circuit were as follows.

(a) Inhibit --counter input is inhibited when high and enabled when low.

(b) Store--Data is continuously transferred to display when low and data is transferred and stored in the display register when high.

(c) Count--the six decade counter is synchronously incremented on the positive transition of the count input signal.

(d) Clear--resets all decades to zero when brought high but does not affect the six digit display register.

(e) Set--when low forces the multiplex scan counter to the most significant digit and blanks the segment outputs.

(f) Scan--clock reference input for internal divide by six Johnson counter to multiplex digit outputs.

(g) Carry--goes high when the leading edge of the count

input occurs and when the counter contents equal 999999.

(h) BCI--binary coded decimal outputs internally multiplexed by a divide by six Johnson counter.

(i) Seven Segment--LED display outputs internally multiplexed by divide by six Johnson counter.

(j) Digit Enable--six strobe outputs of internal divide by six Johnson counter sequentially scanning from the most significant digit to the least significant digit.

The specifications set for the counter operation were a maximum of eight digits of data out and a scan rate of 500 digits per second. Because cascading of the counter/decoders resulted in 12 digit outputs, the requirement to extend the digit multiplexing process became mandatory. For example: the external scan reference signal connected to both cascaded counters simultaneously would cause the six decade outputs of both IC's to be scanned from the most significant digit to the least significant digit in synchronism. However to record the data it was desireable to resynchronize and sequentially scan from Digit 2 of the 'carry' counter (LSD counter) to Digit 1 of the input counter, where the input counter (LSD counter) is the first stage of the counter circuit (digit 6 to digit 1) and the 'carry' counter (MSD counter) is the second stage representing digits 12 through digit 7 in a normal cascading configuration. Figure 9a illustrates the timing sequence in the unsynchronized mode of operation.

External synchronization was accomplished by a two step 'SET' operation using the SET inputs of both counters. The scan reference signal was divided by eight, differentiated and inverted to provide a negative pulse to the scan input of the LSD counter, thereby driving the internal scan

divider to the most significant digit every eight pulses of the scan input reference signal as shown in Figure 9b.

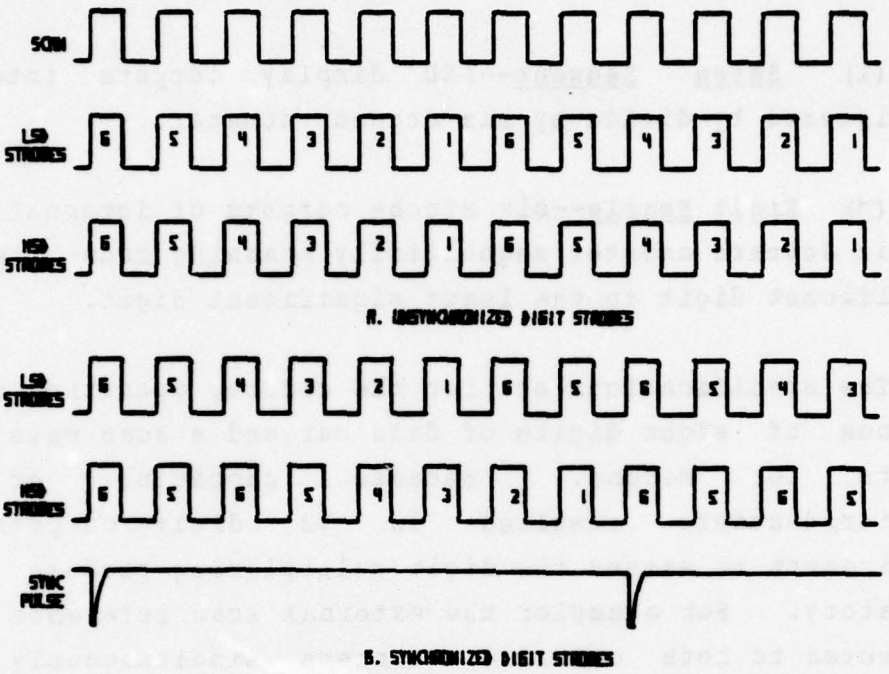


Figure 9. Digit Timing.

Synchronization of the MSD counter digits was realized by differentiating, diode clipping and inverting the digit 4 output strobe of the LSD counter and connecting it to the SET input of the MSD counter. Thus the scan divider of the MSD counter was also driven to the MSD every eight cycles as also illustrated in Figure 9b. The timing sequences in Figure 9b intuitively suggests that a logical gating of the multiplexed digit outputs starting at digit 2 of the MSD counter and continuing for an 8 cycle time period would give a resultant scan of digits 2-1-6-5-4-3-2-1 and would provide a continuous and complete eight digit data output. All counters were synchronized in an identical manner with the SET input of the LSD counters connected together with the

divided by eight scan output permitting the design of a circuit to provide an overall sequential scan of counter #6 through counter #0 (blanker counter).

To provide union of the data of the LSD and MSD counters the digit 6 and digit 2 strobes of one of the LSD counters was utilized to toggle a standard J-K flip-flop (CD4027) configured to switch states on every positive transition of the input signal (digit 6). Digit 2 was fed to the 'reset' input of the flip-flop ensuring that the phase relation of the Q and Q' outputs was maintained to correspond to two digits of data from the MSD counter and six digits of data from the LSD counter.

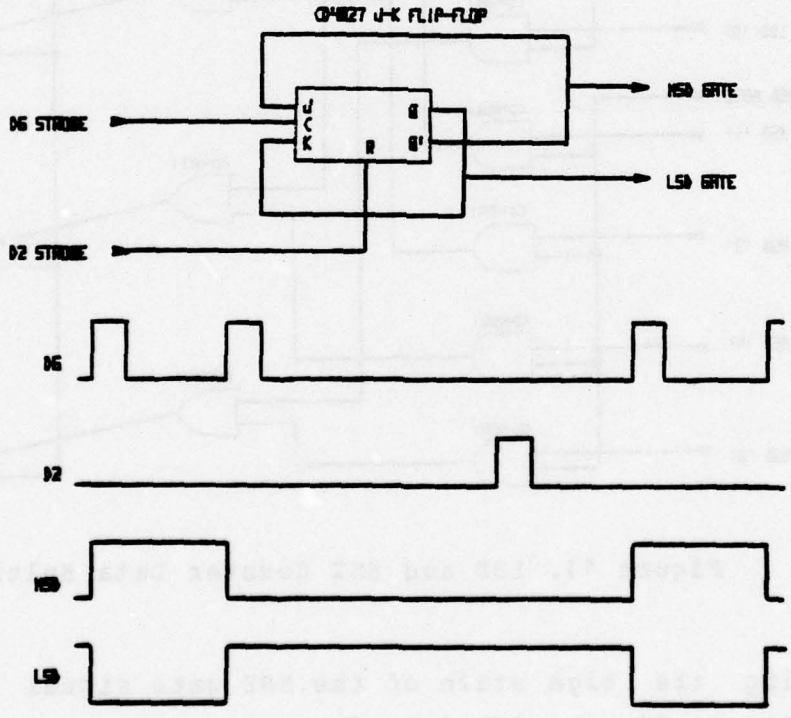


Figure 10. LSD and MSD Counter Gate Circuit.

This circuit formed the second multiplex prccessing of the ccunter data and is shown in Figure 10. The Q and Q' outputs were both utilized to AND gate two digits of data frcm the MSD counter and six digits of data from the LSD ccunter as illustrated in Figure 11.

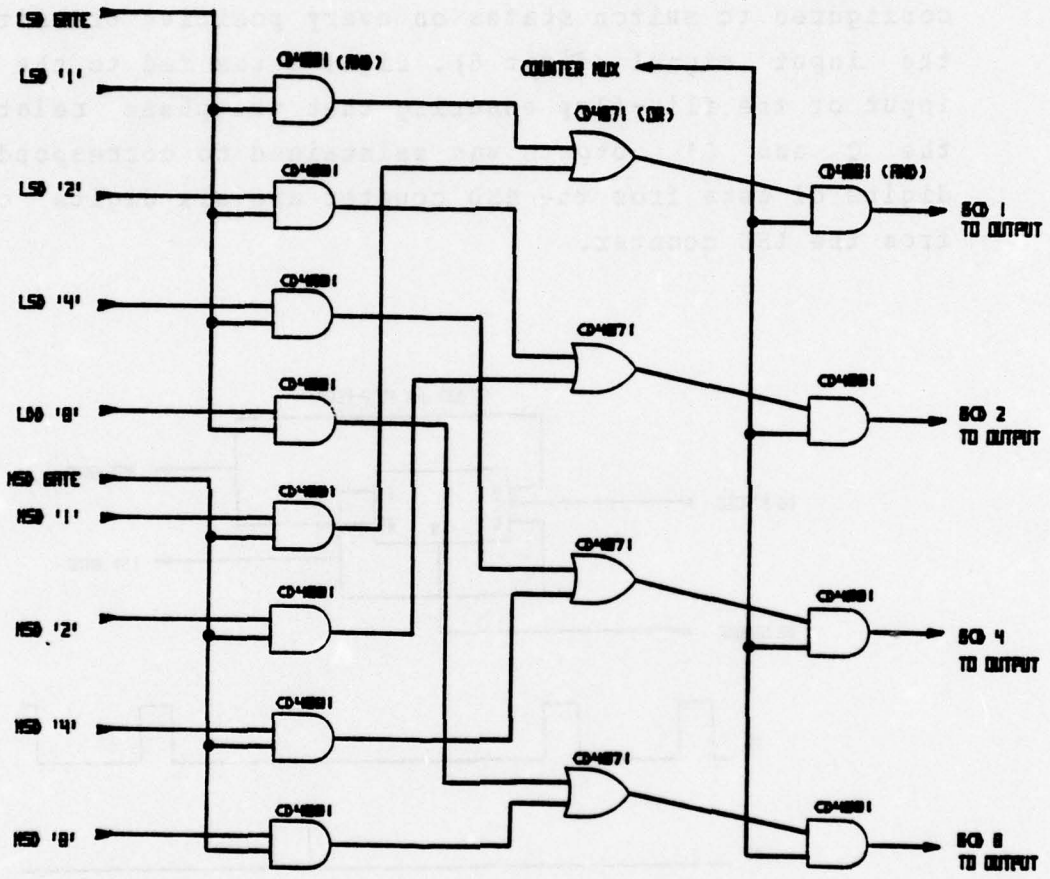


Figure 11. LSD and MSD Counter Data Multiplexing.

During the high state of the MSD gate signal (The Q cutput in Figure 10) the BCD data from the MSD ccunter was AND gated (CD4CB1) to the output stage of each counter circuit, and during the high state of the LSD gate cutput (the Q' output in Figure 10) the BCD data output cf the LSD ccunter

was gated to the output stage of each counter circuit. The output stage for each counter circuit consisted of an arrangement of dual input OR gates (CD4071) to logically OR the LSD and MSD BCD data to a single bus for each parallel bit of the BCD data (1,2,4,8). The BCD data was then AND gated to the main system BCD data buses by the counter multiplex signals described in the following control section.

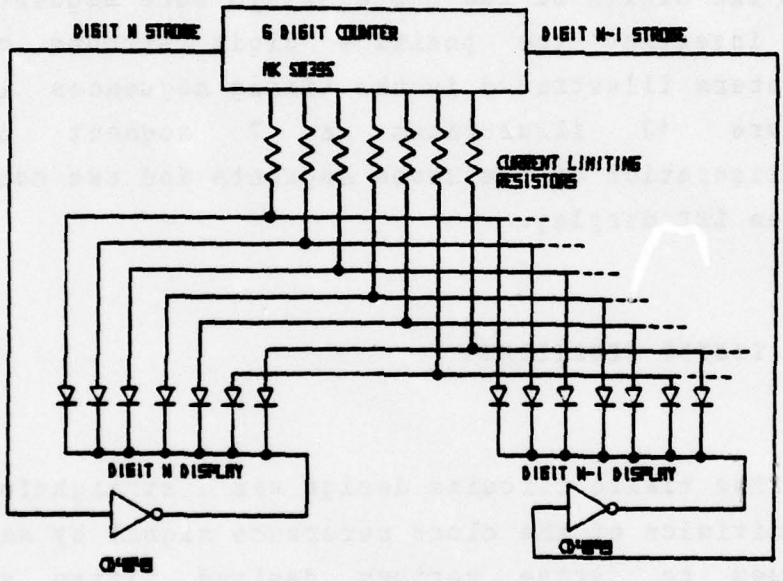


Figure 12. LED Display Multiplex Circuits.

The visual display circuitry derived from the counter/decoder seven segment ouputs and multiplexed digit enable outputs was simply realized by connecting each segment ouput through a current limiting resistor (150 ohm) directly to the matching a,b,c,d,e,f ancde elements of three, parallel connected, four digit LED displays (HP5082-7404). This arrangement provided twelve digits of

display of which ten were actually utilized. Using ten digits permitted a display of two more significant digits than were normally required thus enabling visual indication of any malfunction in the timing or counter circuitry. For example the maximum period was 1000 seconds resulting in a maximum total counter accumulation of 100000000 under normal operation (1000•100000). An accumulated count greater than 10000000 would visually be displayed in the extra one or two digits indicating a circuit malfunction.

The digits of the LED displays were sequentially enabled by inverting the positive digit strobes of the MM50395 counters illustrated in the timing sequences in Figure 9. Figure 12 illustrates a 7 segment digit display configuration of the seven segments and two common cathodes of an LED display.

D. TIMING FUNCTIONS

The timing circuits design was a straightforward process of division of the clock reference signal by several integer values to derive various desired timing signals. The following reference frequencies were desired to accomplish the overall timing of circuit functions.

(a) 100 KHz••• Phase 1 of the 100 KHz signal was used to latch the analog comparator outputs and enable count accumulation in the appropriate counters. Phase 2 was used as a direct gated input to each of the six, eight digit counters to represent analog voltage sample count..

(b) 500 Hz••• The balanced 500 Hz square wave signal provided a scan oscillator input to all seven counters and the system real time circuitry. The unbalanced 500Hz (10%

duty cycle) provided the timing to the digital tape recorder system.

(c) 62.5 Hz••• An unbalanced (10% duty cycle) pulse train provided digit synchronization to each LSD counter of each counter circuit board enabling a digit 8 to digit 1 scan of the decoded counter output data (seven segment and BCD).

(d) 50 Hz••• A balanced square wave provided a stable reference to the time-of-day circuitry for accurate time display and recording.

(e) 62.5 Hz••• An unbalanced square wave (25% duty cycle) provided the time reference for multiplexing the outputs of the seven counter circuits during the data recording cycle.

(f) 1 pps••• A balanced square wave provided master timing for sampling periods. The 1 pps signal was further divided by 10, 100,and 1000 to increase the sampling period range from 1 second to 1000 seconds.

The timing signals were all processed from a crystal stabilized 100 KHz oscillator module, accurate to ±.01% and stable over standard temperature ranges encountered during normal operation. The crystal oscillator was packaged in an oversize dual-in-line (DIP) package and was designed to interface directly with CMOS logic elements. The only external inputs required were Vdd (+12 volts) and signal ground. Figure 13 illustrates the division process designed to obtain the required timing signals for system operation. The 100 KHz balanced square wave was divided by 10 with one half of a dual BCD 'up' counter (CD4518) to produce a 10 KHz square wave output. This signal was again divided by 2 with one half of a dual 'D' flip-flop to produce a 5 KHz balanced

square wave cutput. Further division by a decade ccunter with one cf ten decoded outputs produced a 10% duty cycle 500 pps waveform fcr tape recorder timing and a balanced 500 Hz square wave for digit scanning. The two different outputs cf the decade counter were chosen to prcvide a timing offset between the two 500 Hz signals.

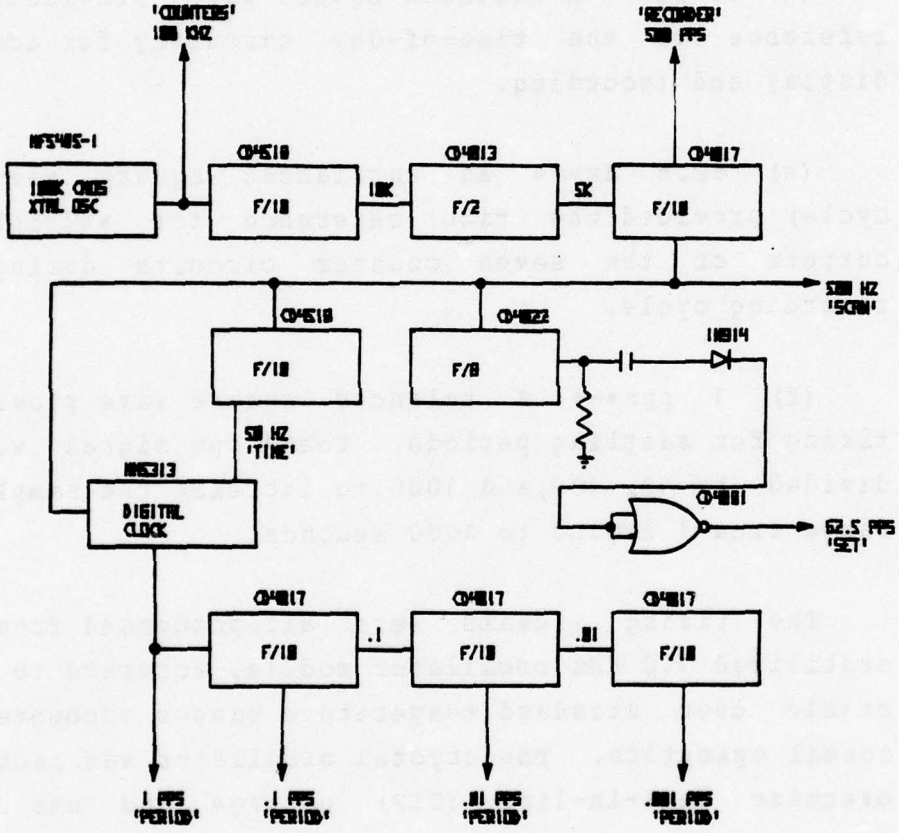


Figure 13. Timing Signal Circuits.

The offset was exactly two periods cf the input signal--apprcximately .4 msec, and the time difference between the cutput scan and the recorder time reference ensured that the data outputs from the MK50395 counters were stable before being 'written' into the magnetic reccrding

system. Figure 14 illustrates the relative timing of the two signals.

The balanced 500 Hz signal was divided by 8 to produce a 62.5 Hz signal for counter digit synchronization. A standard divide by 8 counter (CD4022) was utilized to produce a balanced 62.5 Hz square wave which was subsequently differentiated, diode clipped and inverted to provide a 62.5 Hz negative pulse train with pulse width equal to approximately 1 msec. The negative pulse train was connected to the SET input of the MK50395 counter/decoders (LSD counters) causing the internal digit scan divider of the counters to be driven to the MSD (digit 6) every 8 cycles of the scan oscillator reference signal (500 Hz). The 500 Hz scan input signal was also divided by the second half of a dual BCD counter (CD4518) to give a 50 Hz balanced square wave output for a time reference for the digital clock.

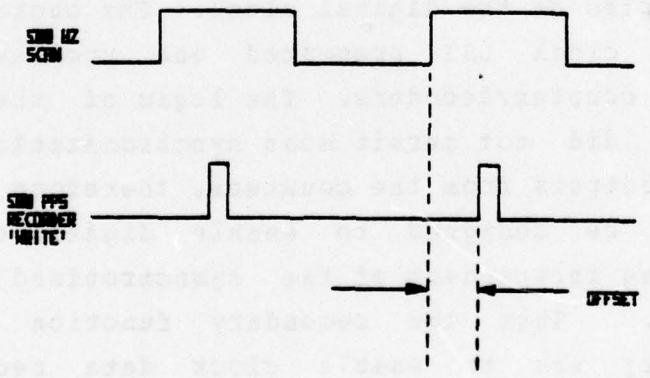


Figure 14. Scan and Recorder Reference Offset.

The real time circuit was a National Semiconductor LSI digital clock with both BCD and seven segment data outputs

and six digit strobe outputs similar to the MK50395 counter/decoder outputs. The features of the MM5313 digital clock circuit were 50 or 60 Hz reference operation, 4 or 6 digit display modes, 12 or 24 hour time display format, internal multiplex divider, single power supply, CMOS compatibility, fast and slow 'set' controls, hold count control and a 1 pps square wave output for use with peripheral logic circuitry. The 50 Hz reference signal into the digital clock was internally divided to produce an accurate hour, minute and second display, an equivalent BCD data output, and a 1 pps square wave output. The 500 Hz scan input signal was also internally divided by six to provide digit enable scanning from unit seconds (digit 6) to tens of hours (digit 1). Note that the scan is backwards from the time display as normally read (left to right).

To incorporate the digital clock into the system design the circuit was configured to operate in the 50 Hz mode by leaving the 50/60 Hz select pin of the integrated circuit unconnected, and the clock was also configured to the 24 hour and 6 digit display format by grounding the appropriate select pins on the digital clock. The choice of the MM5313 digital clock LSI presented one problem relative to the MK50395 counter/decoders. The logic of the digital clock circuit did not permit scan synchronization with the digit strobe outputs from the counters, therefore logic circuitry had to be designed to enable digital clock output data recording independent of the sysnchronized counter/decoder outputs. Thus the secondary function of the control circuitry was to enable clock data recording without synchronization to the counter/decoder circuit timing references. Specific signals related to the digital clock will be discussed in more detail in the following contol section.

The 1 pps output of the digital clock was divided by 10,

10C, 100C respectively to provide the timing for the MK50395 counter/decoder 'count enable' and 'count inhibit' inputs. Standard CMOS divide by ten counters (CD4017) were used to provide a 10% duty cycle 0.1, 0.01 or 0.001 pps signals and each of the four timing signals (1 pps to .001 pps) was made selectable with external front panel controls to set the desired sample period during normal system operation.

The digital recording system selected for 'data logging' had characteristics which included an input data buffer/storage circuit which accumulated 1024 bits of data prior to actual transfer of the data onto the magnetic tape. It was convenient therefore to provide data to the recording system in 256 bit (1024/4) blocks. BCD data outputs consisted of four parallel bits for each serial digit of data. Therefore the system output consisted of seven counters of eight digits each for a total of 224 bits. The digital clock provided 6 digits of four bit data for a total of 24 bits. At this point the total data bit count was 248 bits, 8 bits short of the desired 256 bit block of data.

Two digits of additional data were designed into the system data output. One digit was a front panel selectable BCD CODE utilized to represent any arbitrary digit wanted for integration into the data logging process. For example the 'CODE' digit (0-9) was utilized to represent the elapsed days during actual data collection tasks. The second digit added to the system was a hard wired '1010' BCD code (binary equivalent of decimal 10) to permit synchronization of the data during the replay of the magnetic tape into a computer system (the HP9830 calculator used for data reduction reads a '1010' code as a special character). Recording of two additional digits of output signal was integrated into the real time recording format of the digital clock output, thus the format of the digital clock output was modified to provide a scan of the hardwired 1010 digit, the 'code' digit

and then seccnds, sinutes and hours; and the resultanat modificaticn increased the total data count to 256 bits.

E. CONTECI FUNCTICNS

The design of the control circuitry centered around three dual J-K flip-flops (CD4027) utilized to provide ccunt inhibit/erable ccntrol, digital time data multiplexing and ccunter data multiplexing for interfacing with the digital recording system.

The J and K inputs of each flip-flop were each ccnnected in a specific feedback arrangement designed to allcw the flip-flops tc toggle to a single output state combination and then hold that output state until the prescribed circuit function was completed. Each circuit was then reset in sequential crder depending on its function. This procedure of allowing cnly one state for each 'tcggle' and then a subsequent resetting enabled easy circuit isolation when performing trcubleshooting and maintenance.

To stcw the ccunter enable/disable and record cycle ccntrol functicns assume the following 'idle' circuit states in Figure 15. Here 'idle' refers to the system condition of no sampling cr recording events in process.

Q of IC5a--high
Q of IC5b--high
Q of IC6a--low
Q of IC6b--low
Q of IC7a--low
Q of IC19b--high
Manual Reset--Off

Auto/Manual--Manual

Under these conditions three, three input AND gates, IC9a, b, and c (CD4073) are all gated off and have a zero output state, and the recorder time reference output and the BCD data from the digital clock are gated off.

The external 'Manual Start' switch is now held depressed applying +12 volts to one input of the three input AND gate, IC9a. A second input coming from IC19b is high; therefore the AND gate assumes a 'ready' condition. The 1 pps output of the digital clock is differentiated by R1 and C1 and the negative portion of the differentiated wave is clipped by dicde D1. The resultant positive pulse provides the third input to the AND gate, IC9a. When the positive spike occurs the output of IC9a follows and resets IC5a causing its Q output to go low. This Q output is connected to the count enable inputs of all of the counters and to the reset pins of the 'period' dividers. At this point the counters can increment and the 1 pps output of the digital clock also connected to the clock input of the 'period' divider chain can be divided by 10, 100, or 1000 depending on which period has been externally selected. The divider outputs are connected though an external SP4T PERIOD switch to the clock input of IC5a, and the J-K feedback arrangement of IC5a will permit a positive transition of the clock signal to toggle the flip-flop to the original state--Q high. When the period divider chain has appropriately divided the 1 pps input, and the divide by 10 output of the selected period divider transitions to a high state IC5a will toggle causing the Q output to go high. This positive transition of Q of IC5a will in turn toggle IC5b to cause its Q' output to go low, which in turn removes the reset condition from IC6a putting it into a ' ready' condition. The clock input of IC6a is connected to the digit 4 strobe (tens of minutes) of the

digital clock. The digit strobe signals of the digital clock are logical zero pulses with a width equal to one period of the 500 Hz scan signal and have a period of 500 divided by 6. Therefore at some unsynchronized time the digit 4 strobe output will transition to a logic one after the completion of the digit 4 logical zero pulse, and this postive transition will toggle IC6a causing the Q' output of IC6a to go low. This Q' output is connected to one input of a dual input NOR gate (CD4001), IC12a, enabling the output to follow the inversion of the other gate input which is the digit 5 strobe from the digital clock. The digit 5 strobe in a low state causes the output of the NOR gate to go high for one period of the scan reference signal. The digit 5 pulse output is connected (hard wired) to the appropriate data bus OR gates (CD4071), IC13b and IC13d, to provide a 1010 BCD code during digit 5 time to the output BCD data bus. Q' of IC6a is also connected to one input of a second dual input NOR gate, IC12b, with the other input connected to the digit 6 strobe of the digital clock; again the result is a single positive pulse with a period of one cycle of the scan reference signal. This output is connected to an external BCD CODE switch which provides a 0-9 BCD output for the previously mentioned code data. When Q' of IC6a goes to the low state, by being connected to the K input of IC6b, it set IC6b in the 'ready' condition. Then on the positive transition of the digit 6 strobe IC6b is toggled causing its Q' output to go low just at the start of the seconds through hours digit scan. This output enables the BCD data output gates from the digital clock, IC10a,b,c and d, and during this low state time data is coupled to the BCD data output bus. The next positive transition of the digit 4 strobe toggles IC6a to its original state, and the next positive transition of the digit 6 strobe toggles IC6b to its original state. The switching action ensures one and only one '1010' digit and code digit per recording cycle, and a single scan of the BCD seconds, minutes and hours data to

enable recording of that data once during each recording cycle.

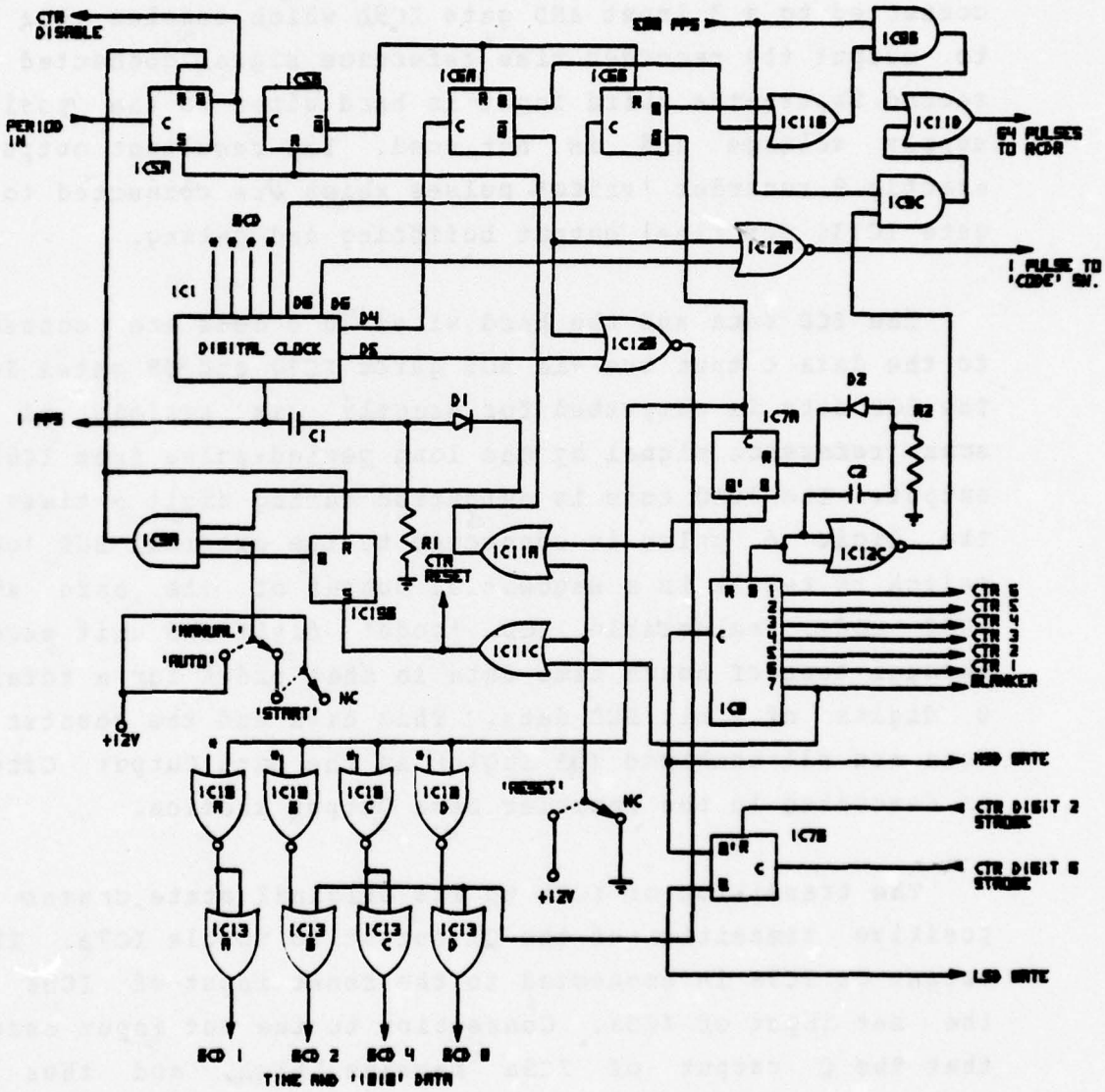


Figure 15. Control Circuits.

During the digital data scan the 'write' signal to the digital recorder is gated on for exactly 8 periods of the 500 pps recorder time reference signal. This is accomplished by connecting the Q outputs of IC6a and b to the inputs of the 2 input OR gate, IC11b. The output of the OR gate, a pulse with a period of 8 scan cycles, is connected to a 3 input AND gate IC9b which enables this gate to output the recorder time reference signal connected to a second input--the third input is hard wired to the positive supply voltage and is not used. The resultant output is exactly 8 recorder 'write' pulses which are connected to OR gate IC11d for final output buffering and gating.

The BCD data and the hard wired 1010 code are connected to the data output bus via NOR gates IC10 and OR gates IC13. The BCD data is outputted for exactly six periods of the scan reference signal by the long period pulse from IC6b Q' output. The 1010 code is outputted during digit 5 time and the digit 6 pulse is connected to the external BCD 'code' switch to result in a sequential output of the hard wired 1010 code, selectable BCD 'code' digit and unit seconds through tens of hours time data in that order for a total of 8 digits of 4 bit BCD data. This data and the counter BCD data are all combined (OR logic) in the Data Output Circuit as described in the Recorder Data Output section.

The transition of IC6b to its original state causes the positive transition of the Q' output to toggle IC7a. The Q output of IC7a is connected to the reset input of IC5b and the set input of IC5a. Connection to the set input ensures that the Q output of IC5a remains high, and thus the counters remain disabled, and the connection to the reset input of IC5b causes a logical one output from IC7a to reset IC5b and in turn IC6a. The Q' output of IC7a is also connected to the reset input of a divide by eight

decoder/counter (CD4022) used for multiplexing the BCD data from each of the seven counters. When Q' of IC7a goes low it enables the counter allowing the MSD gate signal from IC7b to increment the counter. The decoded outputs of the counter sequentially enable the BCD data gates at the output of each of the seven counters as shown in the timing diagram of Figure 16. The outputs of the counter used for this

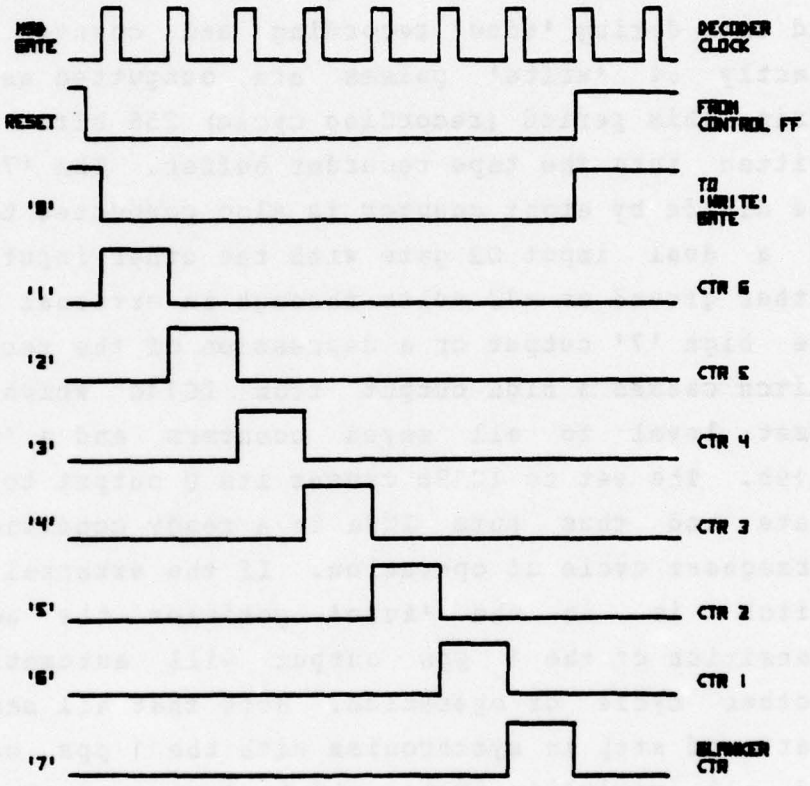


Figure 16. Final Output Multiplex Signal.

function are the '1' through '7' decoded outputs. The '0' is the high output during the reset condition of the counter, so when the counter output returns to a '0' condition after counting 8 MSD gate pulses the '0' output is differentiated by R2 and C2 and clipped by diode D2 to

provide a reset for IC7a, thus the Q' output of IC7a remains at a logical 0 for a period equivalent to a scan of 56 digits. During the scan of the 1 through 7 outputs the '0' output is low and is inverted by IC12c and connected to one input of IC9c a three input AND gate. One input of this gate is not used and is connected to +12 volts, and the other input is connected to the 10% duty cycle 500 Hz recorder time reference signal ('write' signal). The output of the AND gate is connected to the second input of IC11b, and thus during 'time' recording and counter multiplexing exactly 64 'write' pulses are outputted as desired, and during this period (recording cycle) 256 bits of data are written into the tape recorder buffer. The '7' output from the divide by eight counter is also connected to one input of a dual input OR gate with the other input connected to either ground or +12 volts through an external RESET switch. The high '7' output or a depression of the reset pushbutton switch causes a high output from IC11c which provides a reset level to all seven counters and a 'set' pulse to IC19b. The set to IC19b causes its Q output to go to a high state and thus puts IC9a in a ready condition for a next subsequent cycle of operation. If the external Auto/Manual switch is in the 'Auto' position the next positive transition of the 1 pps output will automatically start another cycle of operation. Note that all sampling cycles start and stop in synchronism with the 1 pps output pulse, and all recording cycles which start unsynchronously after the termination of a sample cycle occur between the 1 pps output pulses.

Visual display of the digital clock time was designed by connecting the seven segment outputs of the digital clock through current limiting resistors (150 ohms) directly to two HP5082-7404 four digit displays of which six digits were used to display hours, minutes and seconds. The cathode elements were enabled by the internally multiplexed digit

strcbe outputs of the clock connected through a noninverting BEX buffer (CI4050) to provide the sink for the LED current.

F. RECORDER DATA OUTPUT

The ECD data multiplexed from the ECD CODE switch, digital clock and control circuits and the seven counters was combined by logical OR gates in the data cutput circuit. The cverall purpcse of this circuit was to gate the 256 bits of data frcm separate outputs cnto four output data buses representing the 1, 2, 4, and 8 bits of the ECD code. These buses were then catled directly to the input buffer of the digital reccrding system and to a digital data test circuit bcard (see Data Test Circuit Design in section G). The stages cf the cutput circuitry consisted of eight, four input OR gates (CD4072) and eight, 2 input OR gates (CI4071). Each bit of the BCD data from the counters,

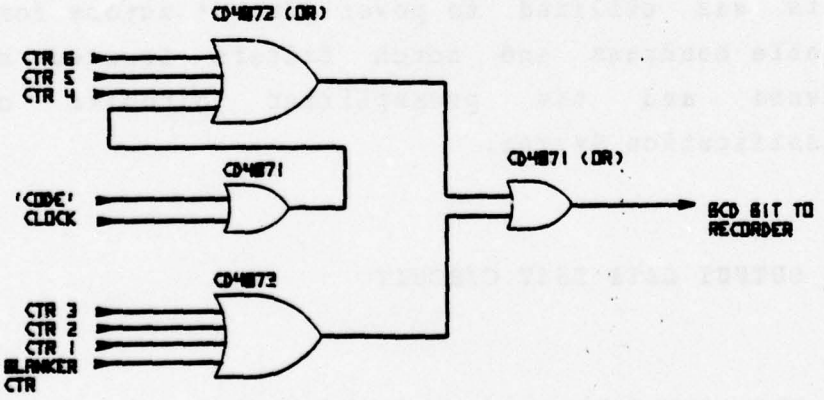


Figure 17. Circuitry for One Bit of Data Output.

digital clock and the BCD 'code' switch was connected to

one input of two, 4 input OR gates or the two inputs of a two input OR gate which is connected to the remaining input of one of the 4 input OR gates. Two of the 4 input OR gate outputs were combined with a second 2 input OR gate to provide a single bit of the data output. Illustration of a single bit output is shown in Figure 17 where the eight inputs to two, four input OR gates are the 1's bit of counters 1 through 6, the blanker counter, the ORed output of the digital clock, and hard wired 1010 code and the output of the BCD 'code' switch. The outputs of the two, 4 input OR gates are simply combined together with a 2 input OR gate to provide a single bus output of the '1' bit data.

The cable carrying the BCD data to the input buffer of the recording system located in the 'Deck Control Box' included a conductor for the 'write' pulses (recorder time reference signal) and a conductor for each bit of the BCD data. A separate three conductor cable provided +12 and -12 volts and signal ground for the recorder and deck control subsystems. The positive 12 volts was utilized for powering the tape recorder system and the positive and negative 12 volts was utilized to power 'drive' motors for the remote tunable bandpass and notch filters located between the antenna and the preamplifier circuits of the RFI Classification System.

G. OUTPUT DATA TEST CIRCUIT

The BCD data connected at the input to the input buffer of the tape recording system was also parallel connected to the input of a test circuit designed to periodically check the data that was being inputted to the tape recorder. This circuit thus enabled a periodic check and a provision for troubleshooting the overall data output circuits of the LDA

system. For example observation of erroneous data in this circuit would provide the observer with the logic information to enable circuit card and/or component replacement to repair any system malfunction prior to recording many hours of erroneous and unusable data onto magnetic tape. Inability to repair the system would also cue the operator to revert to a hand-recording method of data logging directly from the counter displays.

The circuit memory feature was designed around four, 64 bit shift registers (CD4031). The shift registers had a direct input and a recirculating mode of operation allowing input data to be stored permanently and circulated around the register or to be continuously updated by subsequent recording cycles of the LDA system.

Each bit (1, 2, 4, 8) of data was connected to a respective shift register,and an external (circuit card mounted) SPDT switch selected the circulate or direct serial input mode of operation of the shift registers. The recorder timing reference signal was utilized to clock the data into the registers just as the signal clocked the data into the tape recorder buffer. At the termination of the record cycle the shift registers then contained all 256 bits of data of the BCD data output of the LDA system. After the data was stored in the shift register, it was cycled digit by digit to the output connection by sequentially toggling a 'bounceless' switch. The shift register contents were displayed on a single digit seven segment display (MAN4) enabling visual observation of each digit of data stored in the four shift registers. The bounceless switch also toggled a programmable divide by 10 down counter (CD4029) which provided a second digit visual display to assist the operator keep track of the data location during the display cycling. The programmable counter was designed to count down from 8 to 1.

The bounceless switch was designed with a cross-coupled pair of dual input Schmidtt Trigger NAND gates as shown in Figure 16. The logic of the switch works in the following manner. With the pushbutton switch (circuit board mounted) undepressed the normally closed (NC) connection applies a ground to one input of one of the NAND gates. A logical 0 at the input of a NAND gate ensures a logical 1 at the output which is connected to one input of a second NAND gate. The other input to this NAND gate was connected to +12 volts through a resistor thus ensuring that the output of the gate was a logical 0. The 0 output connected to the second input of the first NAND gate thus ensured a stable 1 and 0 at the outputs of the gates. Depression of the pushbutton switch interchanged the +12 vols and the ground between the inputs of the NAND gates causing the outputs of each to switch states. This transition provided a mechanically operated clock to toggle or shift the data in the registers and to toggle the divide by eight and divide by ten counters.

As each four bit digit of data appears at the serial output of the four shift registers it is connected to the input of a BCD to seven segment converter/driver (CD4511). The corresponding seven segment data is directly connected through 2.2 Kohm resistors for current limiting to the anode elements of the MAN4 'Data' display. The common cathode element of the display is grounded thus each digit of data is displayed as the bounceless switch is toggled.

One output of the bounceless switch is also parallel connected to the clock inputs of a divide by 8 counter (CD4022) and a programmable divide by 10 counter (CD4029). The divide by 8 counter provides the programming input to the decade counter through a monostable multivibrator (CD4047). The '0' output of the octal counter is connected to the positive clock input of the multivibrator. On the

positive transition of the '0' output of the octal counter the ouput of the monostable goes high for a period of about 5 microseconds. This output is connected to the '8' Jam input of the decade counter which drives the counter output to a 1000 BCD code (decimal 8).

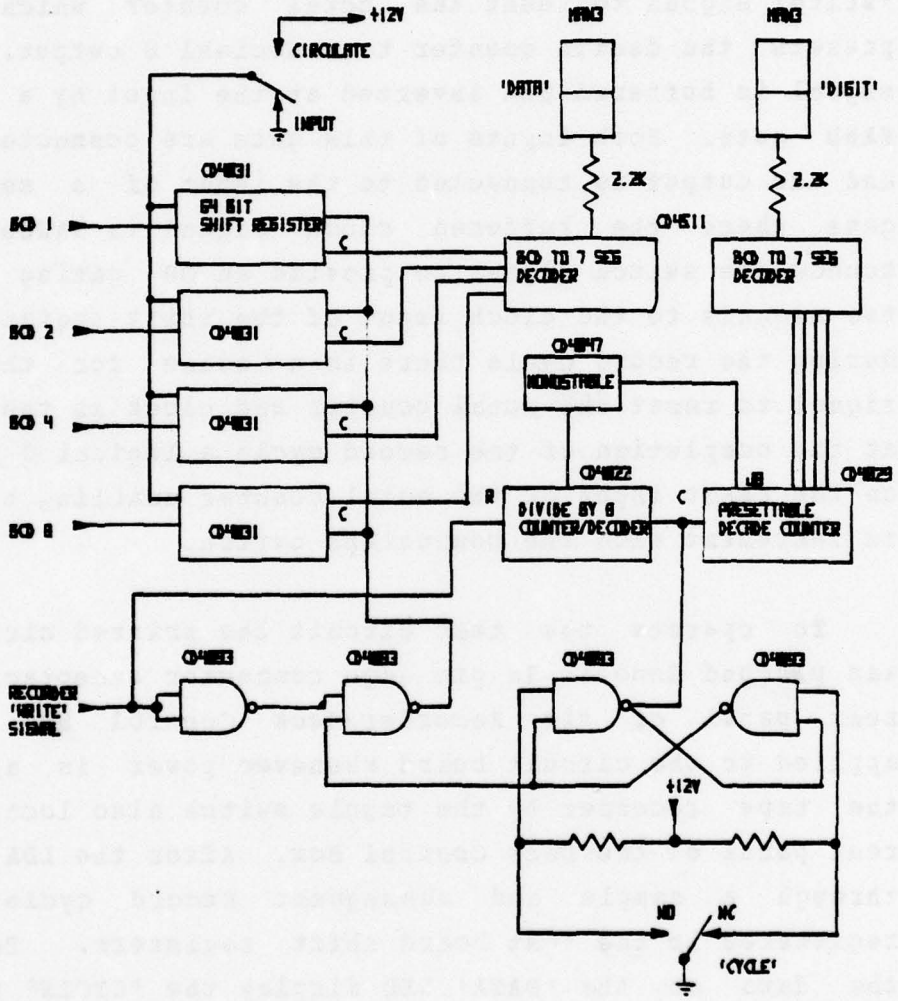


Figure 18. Output Data Test Circuit.

The BCD outputs of the decade counter are also connected to a second BCD to seven segment decoder and the outputs of the

decoder are connected directly to the anode segments of a second MAN4 digit display. The resulting display after a 'jam' input to the decade counter is a decimal '8'. As the cycle switch is toggled the decade counter counts down from 8 to 1 as the octal counter counts from 0 to 7.

Initializing the counters is accomplished by using the 'write' signal to reset the octal counter which in turn presets the decade counter to a decimal 8 output. The write signal is buffered and inverted at the input by a two input NAND gate. Both inputs of this gate are connected together and the output is connected to the input of a second NAND gate where the buffered clock signal is NANDed with the bounceless switch signal to provide an OR gating of these two signals to the clock input of the shift registers. Thus during the record cycle there is a means for the 'write' signal to reset the octal counter and clock in the data, but at the completion of the record cycle a logical 0 is placed on the reset input of the octal counter enabling the counter to increment with the bounceless switch.

To operate the test circuit the printed circuit board was plugged into an 18 pin edge connector receptacle on the rear panel of the Recorder/Deck Control Box. Power is applied to the circuit board whenever power is applied to the tape recorder by the toggle switch also located on the rear panel of the Deck Control Box. After the LDA has gone through a sample and subsequent record cycle data is registered in the test board shift registers. To display the data on the 'DATA' LED display the 'CYCLE' pushbutton switch must be pushed and released 64 times to sequentially display the stored digit data. At the same time that the CYCLE switch is pushed the DIGIT LED display indicates the relative location of the 'pushing' cycle by counting down from 8 to 1 a total of eight times. The displayed data is then correlated with the visually displayed data of the LDA

to check for proper system operation. It should be noted that the hard wired 1010 code which is the first digit of data out of the LDA system is converted to a blank output by the BCD to seven segment decoders, thus the initial displays after the recording cycle will always be a 'blanked' DATA digit and an '8' on the DIGIT display.

H. MISCELLANEOUS CIRCUITS

1. Scan Signal Buffer

To provide adequate buffering and reduce the fanout requirements of the scan frequency divider circuit, the scan output of the CD4017 divide by ten counter IC referred to in Figure 13 was connected in parallel to the inputs of four 2 input OR gates. Each OR gate output was then connected to two of the required eight scan inputs of the seven counter and one digital clock system.The buffer is physically located on the Digital Input circuit board.

2. Test Oscillator

To provide a test signal for 'in-system' troubleshooting, a LM566 function generator integrated circuit was used to design a 12 KHz signal generator which provided a square wave and a triangle wave output to a BNC panel connector on the rear of the LDA cabinet. The circuit was configured in accordance with manufacturer application notes[8] and is schematically illustrated in Appendix C. The test circuit is operated by connecting the test signal square or triangle wave output to the positive LDA input connector on the rear of the LDA cabinet. Power is applied to the circuit (+12 volts) by turning the 'TEST SIGNAL' toggle switch on the front control panel of the LDA to the 'ON' position. The

test oscillator is also located on the Digital Input circuit board.

V. POWER SUPPLY DESIGN

The basic power to the LDA and the tape recorder systems was provided by a manufacturer designed dual tracking regualted ±12 volt power supply module capable of a 5 ampere output with an overload shutdown capability. The only input required was 115V/60Hz AC line voltage. The positive supply voltage powered all of the circuits of the LDA system and the magnetic tape recorder with a total load of approximately 2.75 amps. The negative supply was only used in the LDA system for the analog voltage comparators and the input operational amplifiers which provided an approximate 50 ma load. As previously noted the negative power supply was also used in peripheral equipment of the RFI measurement system to provide power for remote tuning of a tunable bandpass and notch filter.

The second part of the power system (backup power) was 10 series-connected nickel-cadmium cells rated at a nominal 1.25 volts each to provide a +13.8 volt backup power source for the digital circuits of the LDA and the tape recorder. The backup power ensured that the time circuits and the tape recorder remained stable and operating in the event of loss of normal power. The battery package was capable of an approximate 2.0 amp-hour output which provided a relatively long time backup power source for the +12 volt load. The overall design of the power system is illustrated in Figure 19. Both the battery source and the +12 volt source were connected through series diodes to a main +12 volt DC bus which supplied +12 volts to the tape recorder and the LDA circuits.

A trickle current for battery charging was supplied directly to the battery terminals through a 680 ohm series dropping resistor and a series diode from a peripheral +36 volt power supply physically located in the Deck Control Box with the battery system. To ensure that the trickle charge actually charged the battery and did not provide current to the +12 volt load, three diodes were connected in series with the battery and the +12 volt bus. During normal operation the ±12 volt power supply output was approximately 12.5 volts, and the voltage was dropped to 11.8 volts by the amount of the 0.7 volt drop across the diode in series with the power supply, consequently with 11.8 volts on the cathode element and 13.8 volts on the anode element the three series diodes are not biased in the forward direction and battery current to the DC bus in minimal. In the event of an AC power failure or inadvertant system shut-off at the front panel the battery supplied approximately 11.7 volts to the DC bus, and the diode in series with the +12 volt power supply prevented excessive battery discharge through the power supply.

The final addition to the power system was a logic circuit to provide a signal to the LDA that there was an AC power interupt during a sampling cycle. The circuit was designed with a DIP relay to provide a reset pulse to the counter circuits during a power interupt. The reset signal was only connected to the counter circuits, and it did not in any way interupt or reset the remaining LDA timing and control functions. The reason for this procedure was to enable the determination that a power interupt had occurred by analysis of the recorded output data during data reduction. If a power interupt occurred at some point within a sample cycle the counters would be held reset during the time of the interupt, and subsequent totalization of the counter contents would then indicate that an incomplete sample period had been executed because the total

of the counters would not have been the predetermined total as previously indicated in the Counter Design section. The circuit to provide the reset voltage was designed by connecting the coil of the relay to the +12 volt output of the power supply. The normally open contact of the relay was left open and the normally closed contact was connected to the +12 volt DC bus. The pole connection of the relay switch was connected through a series resistor to the counter reset line. During normal operation the energized relay would be in the 'NO' position and no voltage would be applied to the reset line. If the power supply (+12 volt) decreased below the relay holding voltage (approximately 10 volts) the 'NC' contact would connect the 12 volt DC bus to the reset line, and the counters would be held reset until normal circuit functions were restored.

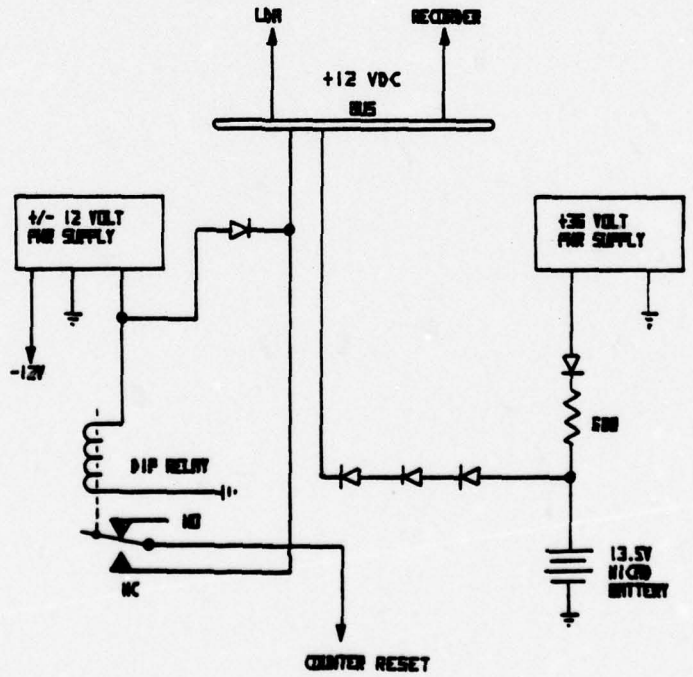


Figure 19. Power System Wiring and Logic.

The logic circuit (relay) was mounted on a small printed circuit board which was bolted to the back panel of the printed circuit board card cage. The required connections were then made by direct wiring into the +12 volt buses and the counter reset line as shown in Figure 19.

VI. PHYSICAL CONSTRUCTION

The assembly of printed circuit card holders and wiring between circuit boards and panel controls was accomplished with consideration for analog and digital isolation, RFI immunity, maintainability, and operability.

All digital circuits discussed in the Design section were constructed on easily removable printed circuit (PC) boards which plug directly into standard edge connectors. The seven counters plug into 18 pin edge connectors and the other three circuit boards--Control, Recorder Data Output, and Digital Input--plugged into standard 40 pin edge connectors. All PC board edge connector contacts were gold plated to reduce potential high ohmic contact between the edge connector sockets and the PC board. The printed circuit boards were installed in a single aluminum enclosed card cage with front access for easy removal or easy extension with constructed 18 pin and 40 pin printed circuit extender boards designed to enable access to the circuit board components from the outside of the card cage (see Figures 27 and 29, Appendix D). This allowed easy measurement of voltages and/or logic levels directly on the printed circuit board while the circuit was in normal operation. All that was required for test equipment to check each circuit was a CMOS logic clip which connected directly on each integrated circuit, a standard voltmeter and an oscilloscope when required.

The PC board edge connectors bolted on the rear of the card cage were interconnected with wiring bundles soldered directly to the edge connector contacts. Each bundle group

was securely wrapped and bound to the card cage to decrease the possibility of vibration or mechanical movement of the wires or solder connections.

The aluminum card cage container was a specially constructed box with removable top and front panel covers. The top was removable to provide access to the interconnecting wire bundles and the actual PC card retainers and edge connectors. The front panel was a hinged door providing access to the PC boards for removal or extension during troubleshooting and maintenance operations. The panel door was constructed and gasketed with an RFI webbing material to ensure a good RFI seal when closed and fastened with 13 screws that secured the front panel door directly to the card cage and the main frame front panel of the LDA cabinet.

To provide visibility of the counter and digital clock visual displays which were mounted on their corresponding PC boards with vertically mounted right angle DIP sockets the front panel door was constructed with two windows in it. The windows were covered with RFI screened red filter plexiglass that enhanced the visibility of the LED displays and provided good RFI filtering to protect the digital circuits from excess noise and/or RFI.

All interconnections made between the analog and digital circuits, the front panel switches, and external panel mounted connector fittings were made by either connecting individual wires to feedthrough capacitors or to SMA panel connectors for coaxial cable connections. Coaxial cables were used for connections between the analog and the digital circuits boxes and between the period divider chain, the external SP4T 'period' selector switch and the counter enable/disable circuitry discussed in the control section. Two additional coaxial connections were made from the test

function generator circuit constructed on the Digital Input PC board tc BNC fittings on the outside rear panel cf the LDA cabinet.

The input power supply voltages and the tape recorder timing signal and BCD data output jack were connected tc the digital circuits through 1000 pf feedthrough capacitors which deccupled the lines and ensured maximum RFI and noise protectien.

The labeled frcnt panel switches and panel meter of the LDA are shcwn in the system photos in Appendix D, and the wiring diagrams in Appendix C illustrate the wiring interconnecticns of the switches, meter and circuits.

APPENDIX A

CALIBRATION PROCEDURES

Because the LDA is primarily a digital system, calibration requirements are both minimal and easy to accomplish. The major goal of the LDA system calibration is to match the LDA analog circuit operating levels to the RFI Measurement System which provides the processed and detected signals to the LDA. The general relation of the LDA to the RFI Measurement System is illustrated in the system block diagram in the Introduction.

The first step in calibrating the system is a rather arbitrary presetting of the #2 analog voltage comparator threshold. This step is performed by utilizing the (1) Level Meter, (2) external Level Adjust and (3) the circuit board calibration potentiometer of the #2 comparator to establish a baseline reference for subsequent system calibration, that is the lowest comparator threshold is matched to a known signal level input and a fixed level meter reading. The result is that measurements which are taken will be accurately interpretted by knowing the baseline reference level for the #2 comparator threshold.

The LDA calibration steps are as follows.

A. Remove the top panel from the LDA cabinet.

B. Remove the top cover of the analog circuit board box which is located to the rear of the cabinet on the bottom of

the chassis.

C. Connect the IF/Detector system LDA OUTPUT to the input of the LDA.

D. Connect a known signal level to the input of the IF/Detector system log amplifier. Note: -60 dBm was determined to be the smallest signal that would ever be present at the input to the log amplifier, so this level of signal from an HP 8640b signal generator was used for LDA calibration.

E. With the meter input selected to LEVEL position the LEVEL ADJUST potentiometer for a reading of 19.5 microamps on the LEVEL meter.

F. Select the MANUAL position of the AUTO/MANUAL switch, '100C' on the PERIOD selector switch, and push the START pushbutton to begin a 1000 second sampling period.

G. Adjust calibration pot #1 on the analog circuit board so that #1 and #2 counters are both counting at approximately the same rate. Determination of an approximately equal count rate may be accomplished by resetting and restarting the count cycle a number of times while observing the numbers displayed in the #1 and #2 counter displays.

H. With the '3 dB' level interval selected increase the signal generator output level by 3 dB steps and adjust the comparator thresholds of the remaining comparators so each consecutive pair of counters--2 and 3, 3 and 4, 4 and 5, 5 and 6--are both counting at an equal rate. For each pair adjust calibration pots #2, #3, #4, and #5 at input signal levels of -57 dBm, -54 dBm, -51 dBm and -48 dBm respectively.

I. With the '10 dB' level interval selected increase the signal generator output level by 10 dB steps relative to the initial value, -60 dBm. Adjust calibration pots #2', #3', #4' and #5' at signal levels of -50 dBm, -40 dBm, -30 dBm and -20 dBm respectively for the counter indications described in step H.

J. The gain of the LDA analog preamplifier was preadjusted to be approximately equal to '1'. Therefore to ensure the capability of circuit board replacement, the second (spare) circuit board should be calibrated at the same time with the same reference level (-60 dBm) that was used with the primary circuit board. With the output from the signal generator set to -60 dBm and the LEVEL ADJUST control undisturbed from the position used during the calibration of the primary circuit board, change circuit boards and adjust the gain control potentiometer for a 19.5 microamp reading on the LEVEL meter. This ensures that both the primary and spare circuit boards have the same reference threshold.

K. Proceed with calibration as in steps F through I.

L. After the analog circuit board is calibrated the LDA meter is adjusted to shift the base line reference meter reading to a more convenient value of 20.0 microamps. This is accomplished by disconnecting the input from the LDA and shorting the input terminals together to 'zeroize' the input to the LDA. Then set the 'LEVEL ADJUST' control so both counters #1 and #2 are counting and adjust the 'METER ZERO' on the face of the meter to obtain a meter reading of 20.0 microamps. This adjustment may also be made whenever necessary during normal system operation.

The steps above provide a general calibration procedure for the LDA system, but to effectively deduce the meaning of

the output data the thresholds of the comparators must correlate with some actual signal power level at the antenna terminals of the RFI Classification System. If the LDA is calibrated with a -60 dBm signal connected to the input of the IF/Detector log amplifier circuitry, the question asked is: What is the power level of the corresponding signal or noise at the antenna terminals that would cause the baseline reference counters, #1 and #2, to both count? The answer to this question is determined by the measurement and calibration of the RF and IF system parameters, but in any case the final LDA system calibration must be the full utilization of the RF/IF system gain, noise figure, Y factor, and correction factors to provide an absolute power label for the thresholds set in the LDA system. It should be noted that different inputs such as Gaussian noise and unmodulated CW signals result in different levels of detected signal at the output of the log amplifier, therefore final baseline reference labeling must also include correction factors for different types of signals and their bandwidths as well as various system gain and frequency configurations.

APPENDIX B

OPERATING PROCEDURES

The operating procedures for the LDA are quite simple and in general require only limited experience and general LDA system knowledge from the operator. The LDA system may be operated in either a manual or automatic mode and either configuration requires minimal control manipulation and adjustment. The system configuration in general is at the discretion of the operator and where pertinent is governed by the characteristics of the signals to be analized by the LDA. The procedures outlined in this Appendix are applicable to the RFI Classification System for which the ODA has been designed, and thus follow guidelines established by experience gained during initial system test trials.

The following operating procedures are set forth to perform the analysis of a narrow band of signals within one of the sub-bands of the 240 MHz to 400 MHz spectrum. Refer to the Introduction for overall system hookup and the signal processing flow.

A. Tune all filters utilized in the RFI Measurement System configuration to the frequency band of interest. This includes centering the manual and remotely tuned bandpass filters (if used) at the center frequency and tuning the manual and remotely tuned notch filters (if used) away from the center frequency or on an interfering signal to be notched out of the RF system.

B. Turn the IF system attenuation to 0.0 dB and select the desired IF system filter bandwidth (30,10 or 3 KHz). Set the IF gain as required to obtain the desired signal level.

C. Select the appropriate bandwidth for the RF system (1 or 10 MHz) on the RF/Blanker box. Select the appropriate RF channel on the 'Deck Control' box.

D. Set the synthesized local oscillator frequency output to 30 MHz below the RF center frequency of interest. Note: The IF system bandwidth is 30 MHz at the input to the IF amplifier.

E. Terminate the input antenna terminals with a 50 ohm load by selecting NOISE DIODE ensuring that the noise diode power is OFF.

F. With the meter input selected to LEVEL set the LEVEL ADJUST control on the LDA to obtain a 20.0 microamp reading on the LEVEL METER.

G. Return the antenna terminals to the ANTENNA position on the Deck Control Box. At this point the reception of signal and/or noise should be indicated in the form of a greater needle deflection on the level meter.

H. Select an amount of attenuation on the IF box to reduce the LDA LEVEL meter reading to approximately 20.0 microamps. This step ensures maximum dynamic range (counter 2 through 6) for subsequent analysis of the input signals with the LDA. Note: Do not readjust the LEVEL ADJUST contol on the LDA after the original setting was established in step F.

I. Select the desired LDA PERIOD (1, 10, 100 or 1000

seccnds) for the desired sampling time. Select the 3dB or 10 dB level interval as desired cr as dictated by the dynamic rangc of the input signal.

J. Select the desired LDA CODE digit--this selection has no effect cn the analysis results.

K. Set up the tape recording system for lcgging operation as fcllows. Turn on the power to the tape reccrder, data Test Circuit and the battery charging circuit by flipping the small toggle switch located on the rear panel of the Deck Control Box to the ON pcsition. At this time the RED pcwer light will be illuminated on the front panel of the tape recorder. Access to the front panel is gained by lcwering the hinged door on the frcnt panel cf the Deck Ccntrcl Box. After access has been gained to the reccrder frcrt panel a cassette tape may be inserted into the cartridge slot in the recorder. Approximately 18 seccnds after the cartridge is inserted the READY light on the front panel of the recorder will illuminate. Lcgging operation may begin at this pcint and the reccrder will log several hcurs of data (approximately 2 million bits).

L. Fcr autcmatic operation select AUTC, and the system will sample and record automatically with a period equal to the selected PERIOD plus one second (all functions start and stop in ccincidence with the changes of unit seconds cn the digital clcck).

M. Fcr manual cperation select MANUAL and at the desired time push the START pushbutton and hold it in fcr at least one second. The system will sample fcr the selected period of time, reccrd and then halt in an idle state.

N. The system may be stopped at any point in the sampling cycle by depressing the RESET pushbutton. However,

if AUTO has been selected the system will start a subsequent count cycle within one second after the reset button is released. If the manual mode is being used the system will reset and remain in an idle state until the START button is pushed again.

O. At this point the actual LDA function has been performed, but it is mandatory to log all pertinent system configuration data. System gain (attenuation), center frequencies, filter bandwidths, local oscillator frequencies, LDA periods, LDA level intervals and the time of the event should be appropriately logged to ensure that the analysis data may by reduced to a meaningful signal density classification.

APPENDIX C

PRINTED CIRCUIT BOARD SCHEMATIC DIAGRAMS

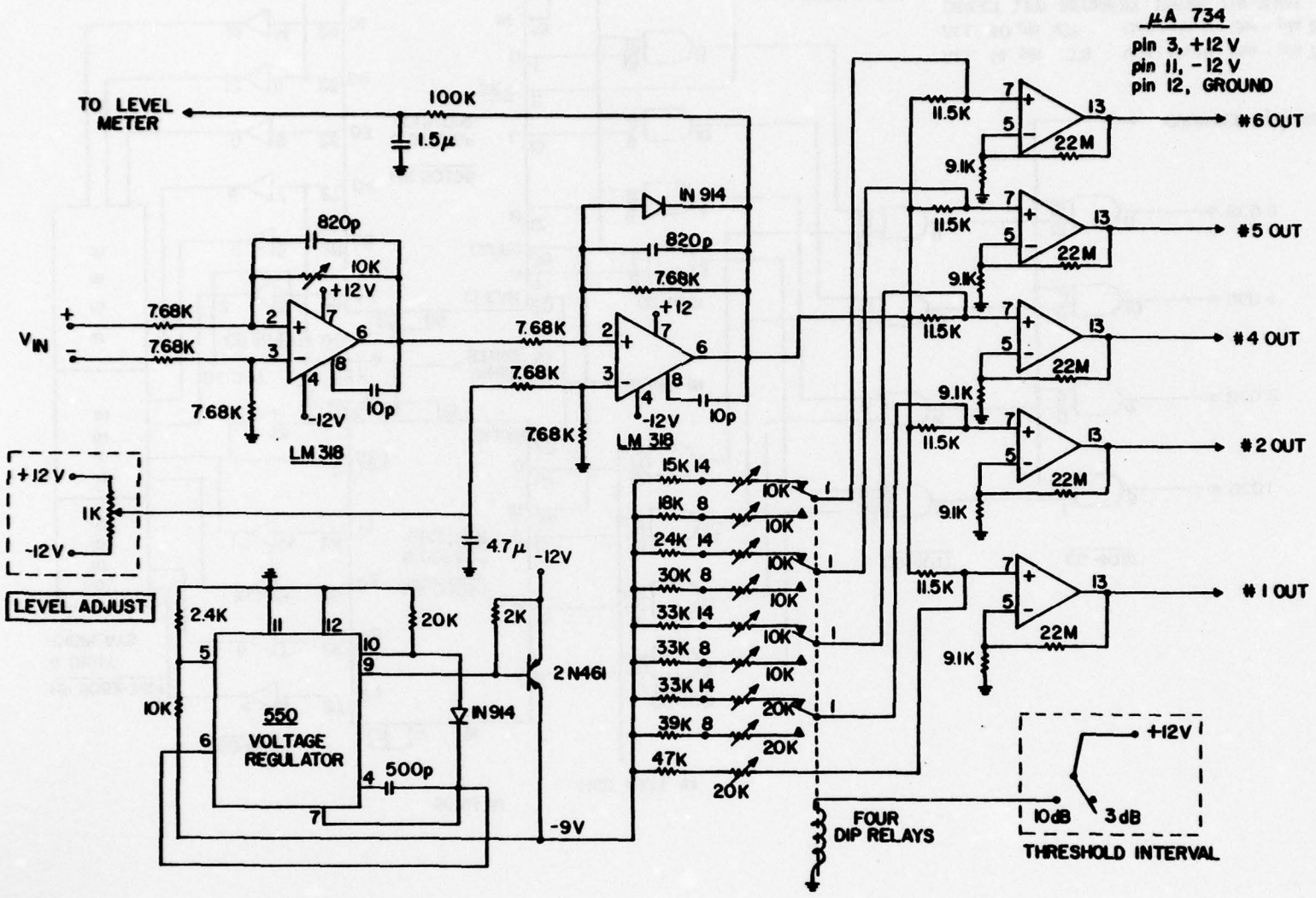
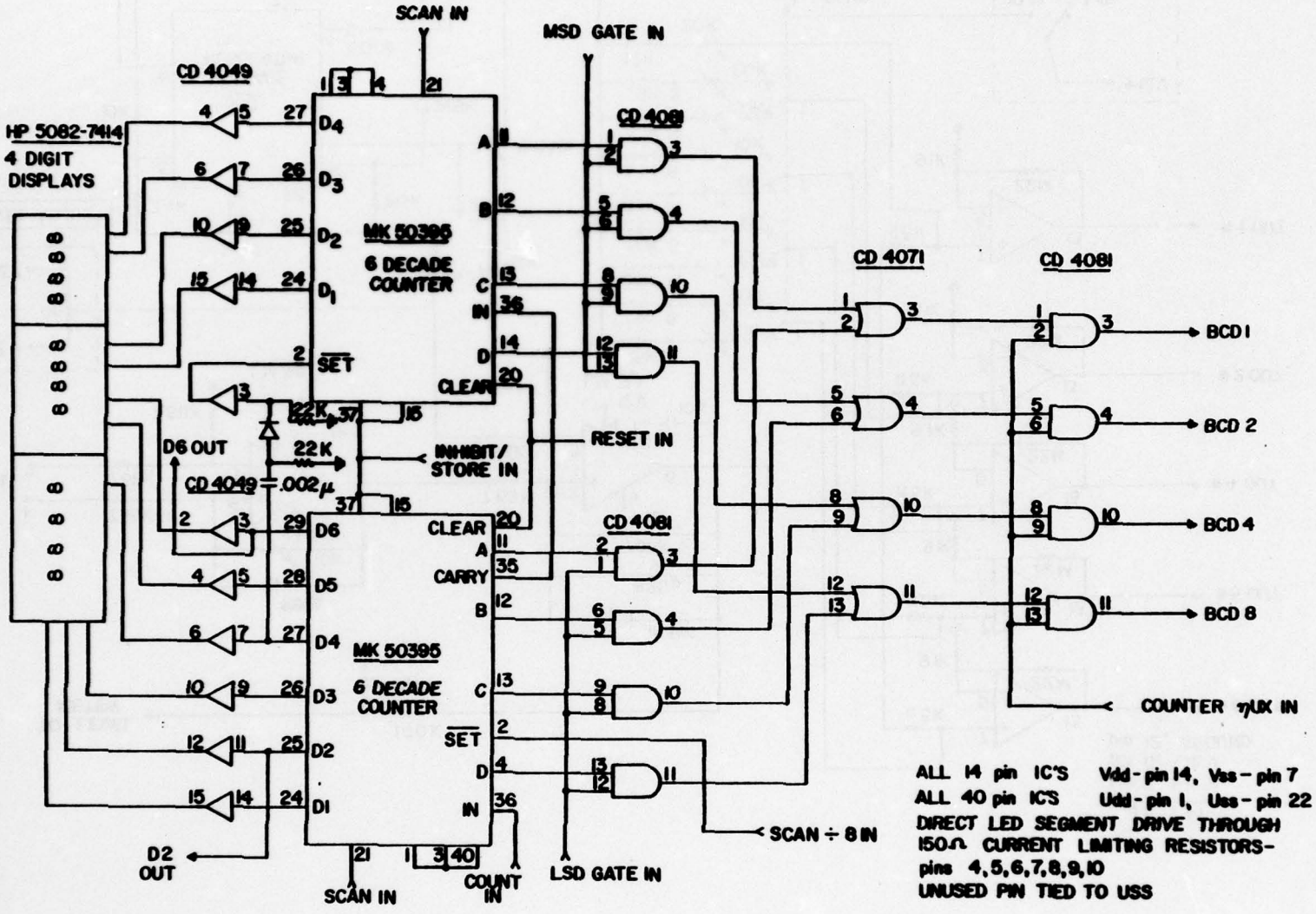


Figure 20. Analog Circuit Board Schematic.



Figur 21. Counter Circuit Board Schematic.

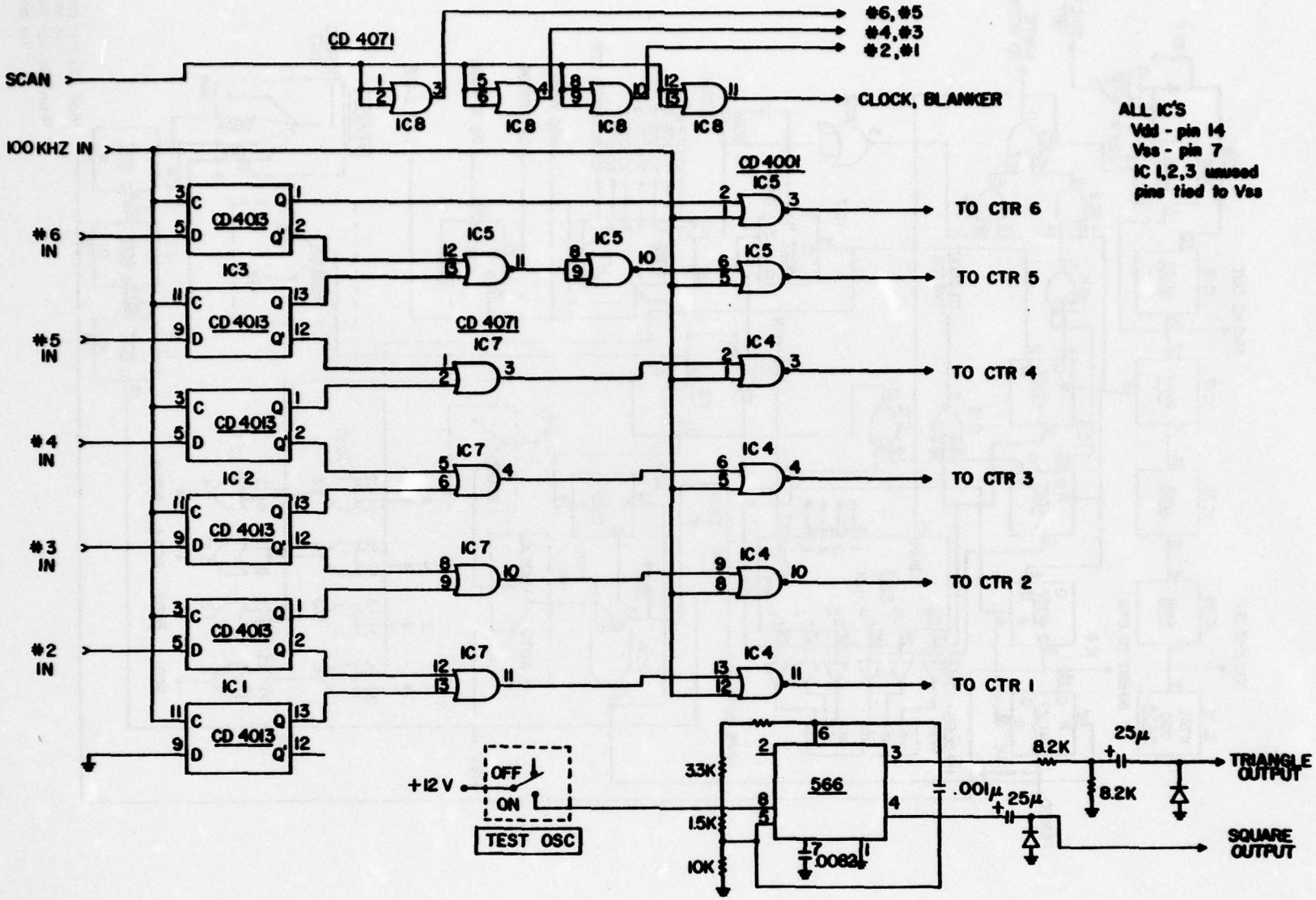


Figure 22. Digital Input Circuit Board Schematic.

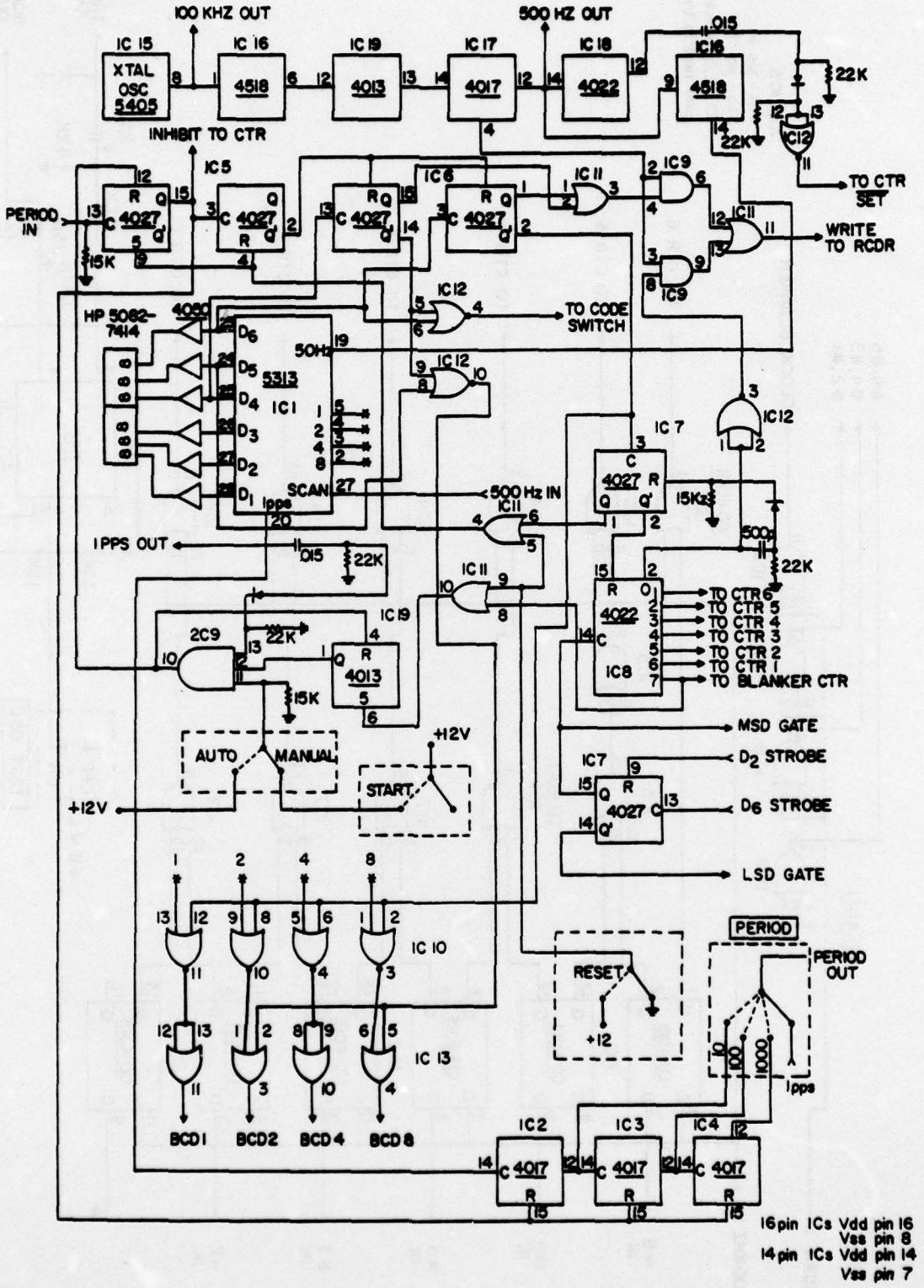


Figure 23. Control/Timing Circuit Board Schematic.

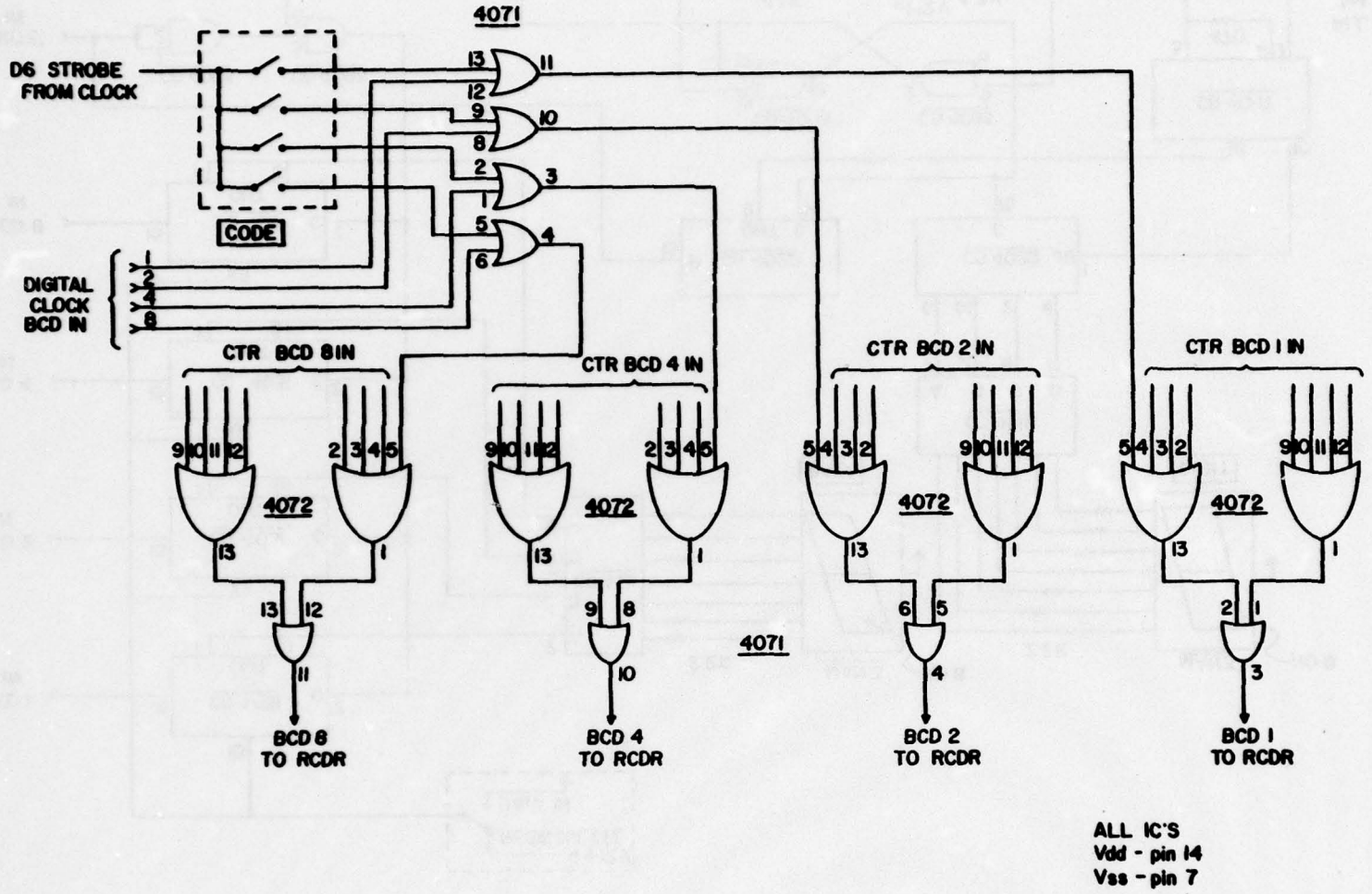


Figure 24. Recorder Data Output Circuit Board Schematic.

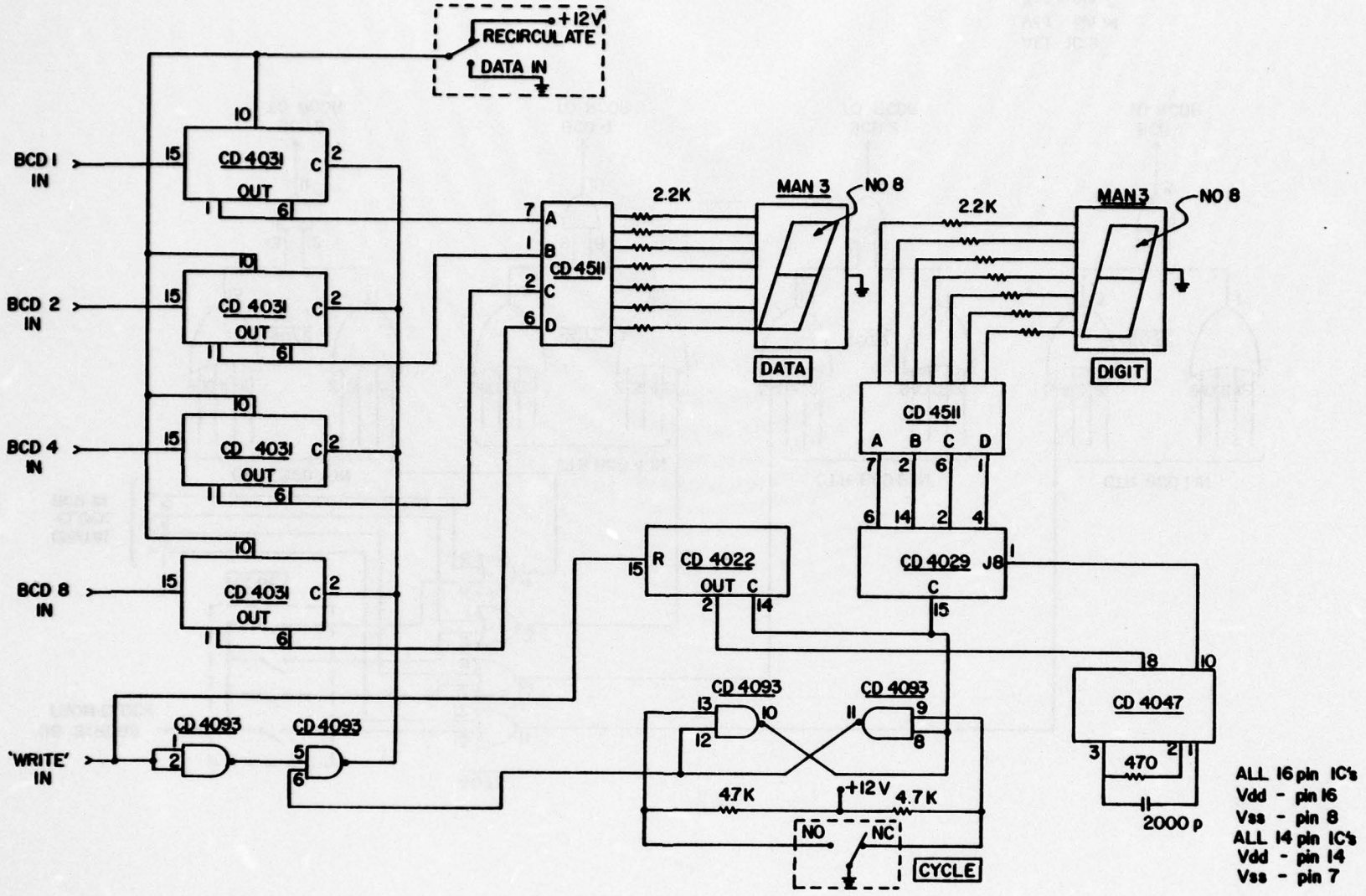


Figure 25. Output Data Test Circuit Board Schematic.

APPENDIX D

SYSTEM PHOTOS

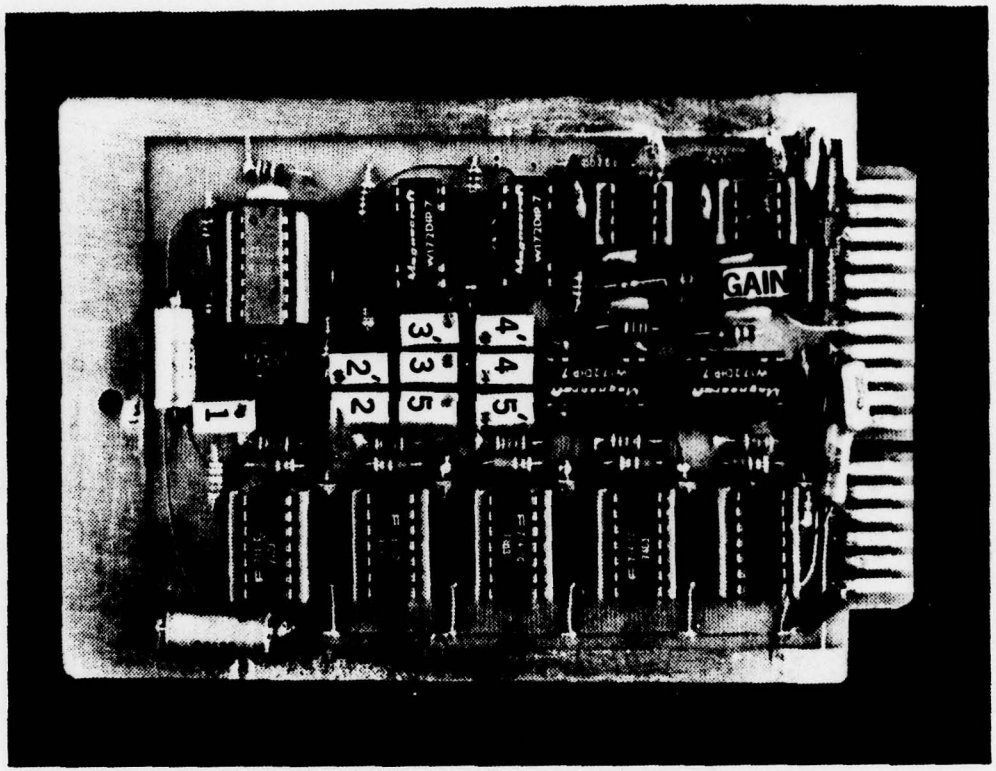


Figure 26. Analog Printed Circuit Board Component Layout.

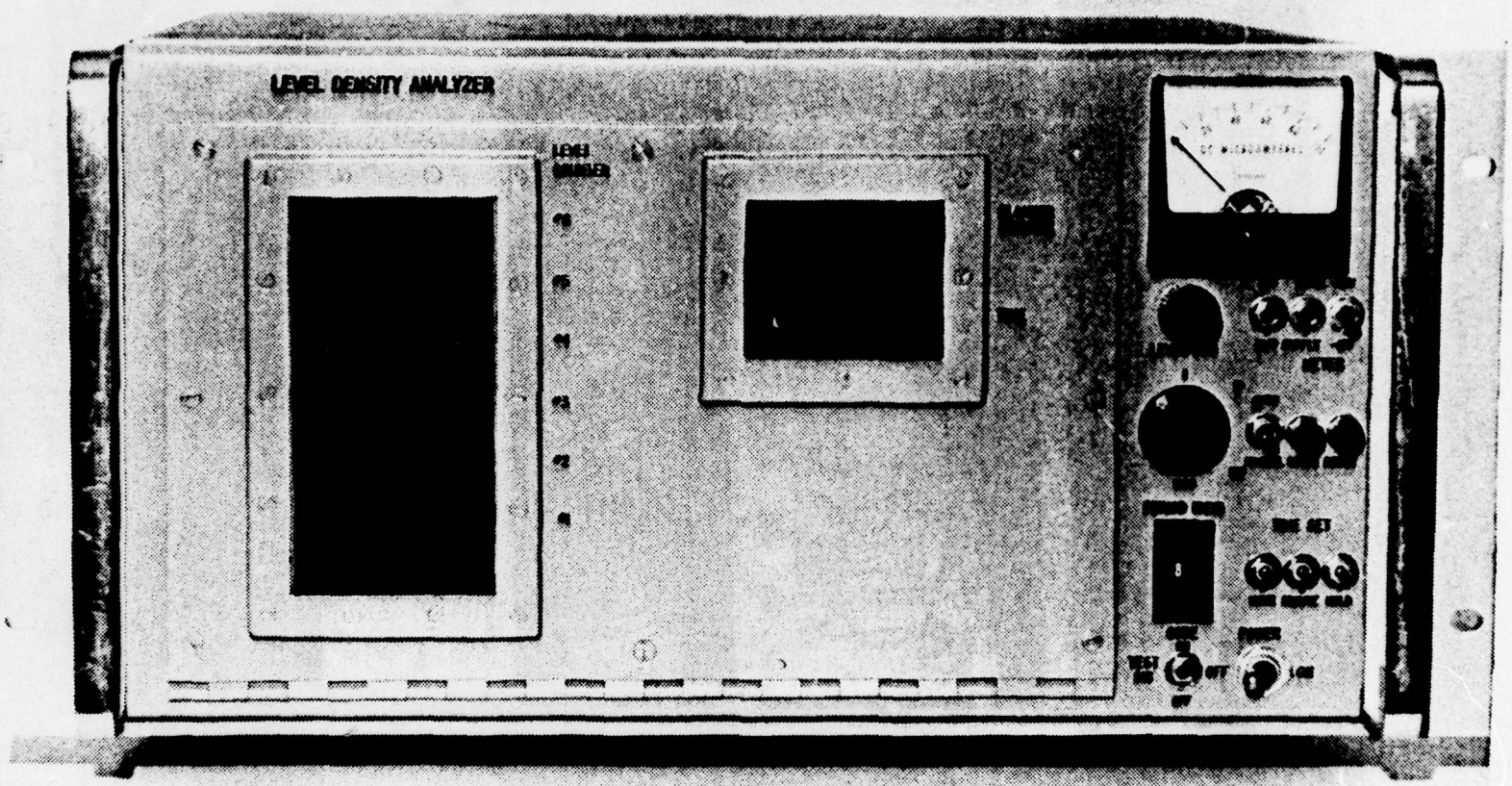


Figure 27. LDA Front Panel

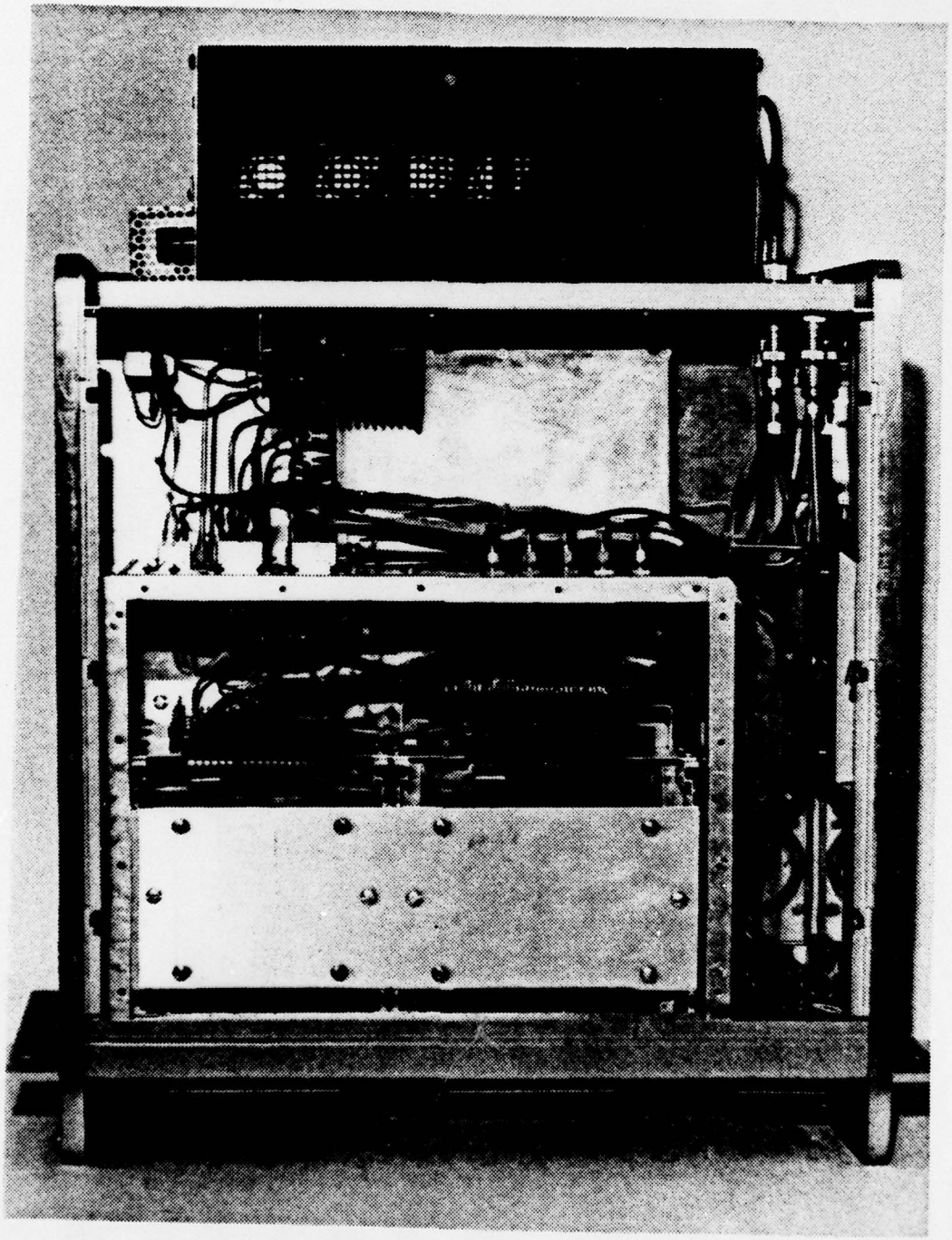


Figure 28. LDA Cabinet Interior.

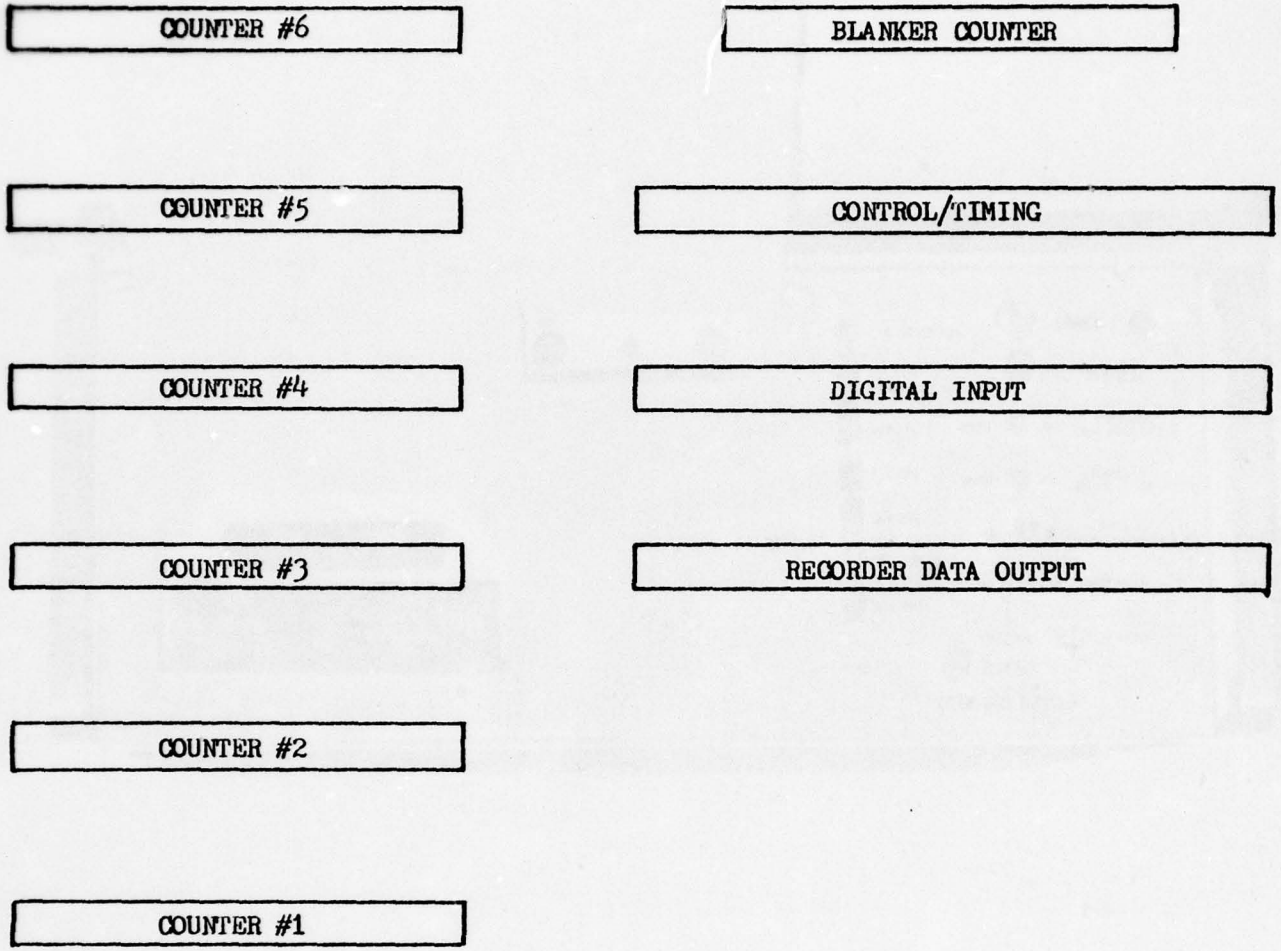


Figure 29. LDA Circuit Board Placement Diagram.

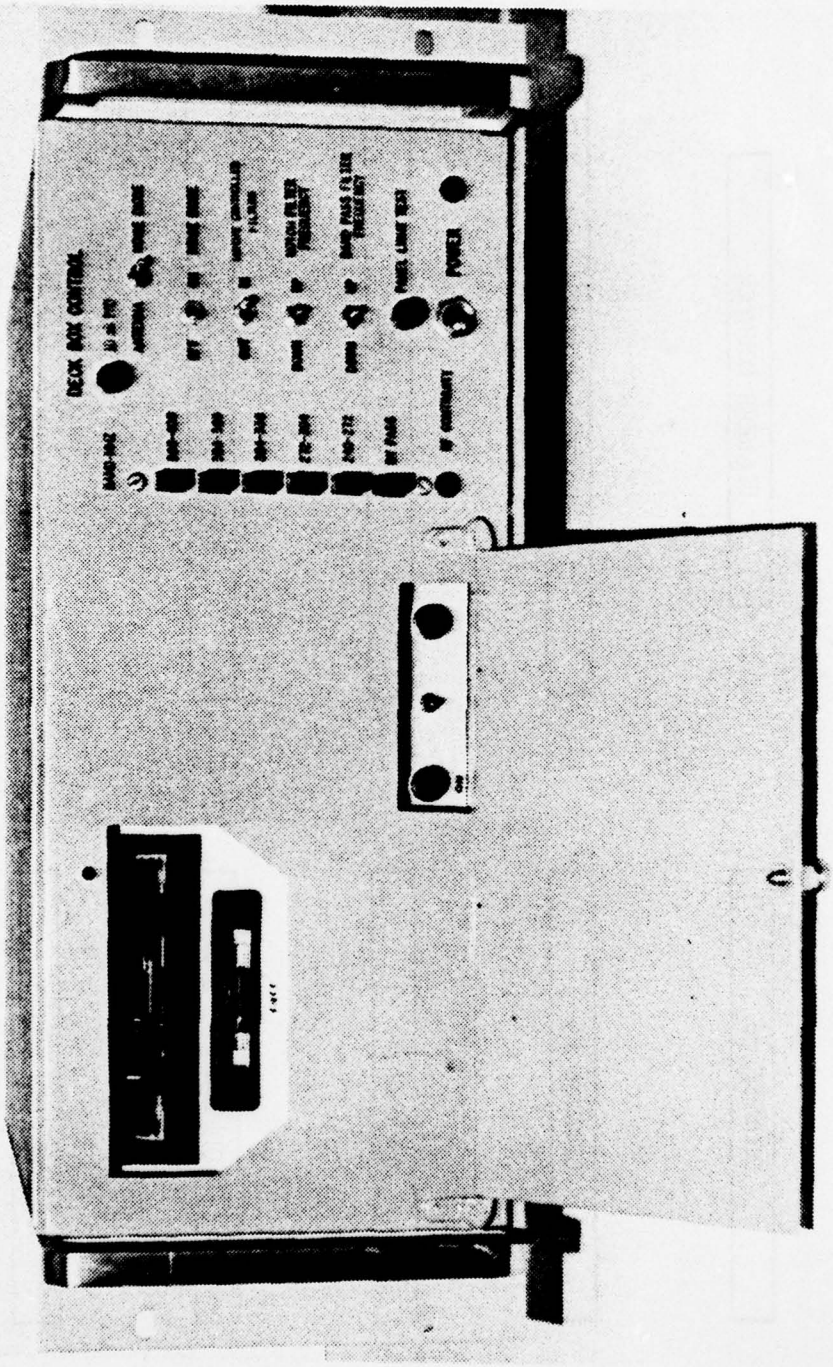


Figure 30. Deck Control Box/Tape Recorder Front Panel.

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