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THESIS

EMULATION OF THE AN/UYK-7
TACTICAL DATA COMPUTER ON THE
BURROUGH'S D-MACHINE

by

Jerry Michael Haggerty
and
John Michael Hartling

December 1976

Thesis Advisor:

S. Jauregui

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Emulation
of the
AN/UYK-7
Tactical Data Computer
on the
Burrough's D-Machine

by

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Submitted in partial fulfillment of the
requirements for the degree of

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ABSTRACT

A workable design is presented for emulating the AN/UYK-7 multiprocessing computer system on the Burrough's Interpreter Based System, the D-Machine. The program developed provides for exact execution of the AN/UYK-7 instruction repertoire with the exception of Floating Point, hardware interrupts and IOC Instructions. The design allows for future expansion to incorporate these functions. Input/Output is limited to a card reader, line printer and single disk. Various aspects of Emulation, the D-Machine, and the AN/UYK-7 are discussed and a detailed User's Manual is provided along with recommendations for modifying the design into a full emulation.

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I. INTRODUCTION

In its effort to provide the Fleet with officers well versed in all aspects of Computer Science, the Naval Postgraduate School strives to furnish each student in the Computer Science Curriculum with ample opportunities for hands-on operation and programming experience on a variety of computer systems. The systems presently available for this purpose include the IBM 360/67, PDP 11/45, XDS 9300, and several varieties of microcomputers and stand alone graphic systems. Unfortunately, this wide range of available systems and their incorporated programming languages does not include any of the numerous tactical computer systems in use in the Fleet today; moreover, because of budgetary and procurement lead time constraints, it is highly unlikely that the school will have such a system in the near future. To provide the desired systems, the Chief of Naval Education and Training and the Naval Postgraduate School, with the assistance of Burrough's Corporation, have provided a medium through which students may gain experience and perform research on, not one or two Tactical Data Systems but potentially on any particular computer in which the student may express an interest. This medium is the Burrough's Interpreter Based System, a microprogrammable computer, hereafter referred to as the Burrough's D-Machine.

Through microprogramming, the D-Machine can be made to operate exactly like any designated computer of interest.

Through the process of Emulation the authors sought to demonstrate that the D-Machine could be microprogrammed to imitate a selected computer. As the target computer, the authors selected the AN/UYK-7 which is used extensively in Tactical Data Systems and is one of the more complex systems in use today. It was felt that if a realistic emulation of the AN/UYK-7 could be demonstrated, then any lower level, less sophisticated computer could also be successfully emulated.

The goal of this thesis was not a complete AN/UYK-7 emulation, but rather development of the design for the Emulation, and adoption of a sufficient subset of the AN/UYK-7 instruction repertoire to demonstrate exact and efficient execution of AN/UYK-7 programs. The design allows for a complete emulation of all AN/UYK-7 functions and provides for future expansion to a complete emulation including all IOC Functions. Chapters II, III and IV are designed to provide the reader with a general knowledge of Emulation, the AN/UYK-7 and the Burrough's D-Machine. Chapter V describes the methods used for imitating the AN/UYK-7 instructions and its various modes of operation. Chapter V also defines the mapping of the AN/UYK-7 Control Memory Registers and status bits into the Burrough's D-Machine for the purpose of this Emulation. Chapter VI presents some of the problems encountered in the course of this thesis, and

the conclusions drawn by the authors as a result of this Emulation. Chapter VII provides recommendations for expanding this Emulation and suggests possible follow on thesis topics. Appendix A is included as a User's Manual, and contains information on how to use the D-Machine, how to run AN/UYK-7 programs on the Emulator, and how to use special features of the microprogramming language TRANSLANG which were not documented in the TRANSLANG Programmer's Manual. The program listings of the Loader and Emulator, written in association with this thesis and used to demonstrate the feasibility of the design by running AN/UYK-7 Programs, are included as Appendix B and C. A sort routine written in AN/UYK-7 machine language, and used to demonstrate the Emulator's capability is provided in Appendix D. The output of the sort program and the optional Loader functions of assembler and debugger are presented as Appendix E and F.

II. EMULATION

Modern computer systems are generally composed of five basic units: input, output, memory, arithmetic/logic, and control. The instruction execution and communications among these units are usually well understood with the exception of the control unit which is, typically, understood only by the system engineer. The control unit generates the signals necessary for the information flow and timing of the system. In conventional computers this is done through the use of flip-flops (e.g. registers and counters) and gates designed in a relatively ad hoc manner. Microprogramming the control unit has been proposed as an orderly alternative to this ad hoc design procedure where the hardware of the control section is replaced by a "microprogram control" unit.

Microprogramming is therefore a technique for implementing the control function of a digital computer using programmable control signals stored in a separate, word-organized memory, called control store. If the control store were a programmable memory, then the system architecture could be modified to optimize processing of each task to be performed; moreover, it could be altered completely to resemble the architecture of another, entirely different machine. The microprogramming of the control store of a computer system to alter the basic architecture enabling one

machine (the host machine) to execute machine language programs intended for another machine (the target machine) is defined as Emulation.

The remainder of this chapter is divided into three sections: general information on microprogramming, construction of an emulator and applications of emulation.

A. GENERAL CONCEPTS OF MICROPROGRAMMING

Since the cost of software has become a major portion of the overall cost of computer systems today, more and more manufacturers and users are turning to microprogramming the control section of their computer to tailor the machine to individual applications, thereby making computer programming more efficient.

The main function of the control section is to specify the conditions under which sets of gates are to be opened. In conventional machines this can lead to a very complex, hardwired system, especially if the instruction set is extensive. A relatively simple field change, addition or alteration, may require a major modification of this complex system. This is not true in a computer that uses a microprogrammable control store. The complex hardwired structure is replaced by microinstructions stored in the control store, one microinstruction per word, which tell the system which arithmetic and logic operations to perform by specifying which gates to enable/disable. In this way,

control of the computer is removed from the hardware and placed under the control of the microprogrammer. This places a heavy burden on the programmer since he must become intimately familiar with the innermost workings of the machine; however, it allows him to model the machine to his specific programming needs. This gives the microprogrammer extreme flexibility in his applications on the computer.

There are two types of microinstructions: vertical and horizontal. Vertical microinstructions usually control one operation; and the address of the successor microinstruction is implicitly the current address plus one, unless the current microoperation causes a branch. In horizontally microprogrammed machines each control bit of a microinstruction is assigned to a specific gate or set of gates. This means that one microinstruction can control multiple operations. On the other hand, vertical microinstructions are divided into separate fields, each of which are then decoded to enable/disable specific gates or sets of gates; therefore, horizontal microinstructions require less decoding and provide more flexibility. However, the advantage of vertical microinstructions is that they generally require shorter control words considerably reducing the overall cost of control micromemory. The length of control words vary from 20 bits (vertical) to in excess of 120 bits (horizontal); the average microinstruction is 50-80 bits. The D-Machine, the host machine for this thesis, utilizes a combination of

vertical (Type II) and horizontal (Type I) microinstructions in the form of a 56-bit word.

Since the execution time of one horizontal microinstruction is essentially the same as that of one vertical microinstruction, the multiple operations performed during one horizontal instruction is a desirable feature. This parallelism can drastically reduce the size of a microprogram, and dramatically decrease execution times. These reductions can only be realized, however, if the programmer can recognize concurrent actions and optimally group them into one instruction. A great deal of work has been done toward including the efficient use of available resources into a compiler for a high-level microprogramming language, but with little success. Either the probability of making the determination is low, or the cost of the optimization is too high. Much additional research is required in the area of recognizing and combining potentially concurrent actions.

Different microinstructions specify different microoperations to be performed, and depending on the nature of the microoperations, some phase of one instruction may overlap a phase of a subsequent instruction. Instruction timing is, therefore, an important factor in the overall efficiency of microprograms in which microoperations are not mutually exclusive. A brief description of the timing considerations that must be made in microprogramming the Burrough's D-Machine is given in Chapter IV.

Many main-frame manufacturers hesitate to allow the novice programmer access to the innermost workings of their computer (e.g. registers, data paths, and gates). One method of prohibiting this access is to use read-only micromemory with the microprograms being provided by the computer manufacturer. This helps preserve the designed identity of the computer but does not provide for its optimum use. The programmer who is given the capability of modifying the logical design of the machine to his specific programming needs will find his programming tasks greatly simplified. For example, he could implement new instructions, such as floating point, which were not designed into the original machine.

In summary, microprogramming is becoming more widely used for the following reasons: 1) the flexibility and growth potential of microprogrammable machines (especially in the area of emulation), 2) increasing software costs and current semi-conductor technology favor microprogram design, and 3) user-oriented instructions can be designed into machines through microprogramming.

B. BUILDING AN EMULATOR

Emulation describes a process through which the hardware components of one machine (host) are made to "appear" to assume the specific characteristics of the hardware of another machine (target). This provides the host machine with the capability of executing machine language instructions written for the target machine. Simulation is a software process that provides the same capability for program execution; however, simulation involves interpretive execution by a high-level language program. Emulation differs in that an emulator performs its interpretive execution through the hardware. Simulations usually perform within a factor of 100-200 times real-time. Emulation is generally within a factor of 10, but often can be tuned to approach real-time. For this reason emulations are usually more cost-effective than simulations. The following paragraphs describe the process involved in building an emulator.

There are two major approaches to emulating a target machine: 1) the hardware and firmware (the physical realization of a microprogram) can be used in conjunction with a software simulator (software alone would be pure simulation), or 2) the hardware and firmware can execute with no software support.

Depending on the percentage of software utilized, a software-assisted emulation may be somewhat slower than a

firmware emulation. Typically, the programmer mentally develops a software simulation of the target machine. He then decides which sequences of instructions are most frequently used, and which are the hardest to simulate. These become candidates for microprogramming. Frequently a single new instruction can be microprogrammed to replace repetitive sequences of the same high-level instructions, thus speeding up the emulation. With this software-firmware approach the user must decide the point at which he must stop substituting microcode for software routines. This is generally dependent on the amount of control storage available, or the cost-performance criteria with which he is working. An example of a software-hardware approach to emulation is the IBM 7000 series emulators used with the IBM System/360 Model 65.

The Burrough's D-Machine provides the capability of emulation using the software-hardware method. A simulation is written in the high-level language ALGOL. ALGOL on the D-Machine allows the user to define a new operator which, when called in the simulation program, branches to a preprogrammed series of microinstructions; executes the microinstructions; and returns to the ALGOL program. This gives the user the ability to execute frequently used routines (such as instruction fetch) from micromemory which has a faster cycle time than that of main memory where the ALGOL simulator resides. An advantage to this approach is that the system does not have to be regenerated after different emulators

are run since, in essence, only an ALGOL program has been executed. However, as previously discussed, this software emulator is slower than a firmware-controlled emulator.

The authors used the hardware-firmware approach in their emulation of the AN/UYK-7. This method will be developed in more detail along with suggested hardware additions which could enhance the emulation. Control of the system resides entirely in the firmware, which means that the emulator, once loaded, dedicates the machine to that emulation, and native mode programs can no longer execute until system regeneration. This unproductive overhead of loading and re-loading the emulator and the native mode machine is one drawback. An additional drawback is the larger micromemory required since the entire emulation is microprogrammed. However, the emulator executes exclusively through firmware making this approach to emulation significantly faster. An example of a firmware-controlled emulator is the IBM 1401 emulator on the System/360 Model 30.

Although systems such as the D-Machine use horizontal microinstructions to enable parallel or concurrent operations, the microprogram can only perform one function of the target machine at a time. That is, if the target machine performs parallel operations such as executing one instruction while simultaneously fetching the next instruction, the microprogram can only emulate one of these functions at a time. It must execute the current instruction and then fetch the next instruction. For this reason, emulation is

usually slower than the real time performance of the target machine even though it may have a faster memory cycle time.

In order to emulate a target machine, the microprogrammer must first understand three areas: 1) the host machine, 2) the target machine and 3) the microlanguage. Second, the registers, counters, and accumulators of the target machine must be mapped into the host machine. This is often done in two steps - depending on the number of available registers in the host machine. The registers of the target machine most frequently used should be mapped directly to registers in the host where possible. The remaining registers of the emulated machine are mapped into the host's main memory. As many of the target machine's registers as possible should be mapped directly, so that fewer memory references will be required by the emulator. For example, if the emulator were executing a Load Accumulator instruction and the specified accumulator had been mapped into one of the host's registers, then only one microinstruction is needed to emulate the load instruction. However, if the accumulator had been mapped to a memory location, then it would take several microinstructions to emulate the entire operation - i.e. setup the store address, store the value to be loaded into the write register, and perform a write to main memory. Not only does this require additional instructions, but it also includes a main memory access, whose cycle time is slower than micromemory's cycle time. Some instructions may require two main memory cycles, such as an ADD where the

mapped accumulator must be read, added to and then written out. This demonstrates the necessity of mapping as many registers as possible to the host machine's hardware. Seldom, however, can this mapping be accomplished without some use of main memory; therefore, the microprogrammer must select some portion of main memory as a privileged area for register mapping. The authors reserved the first 1024 words of main memory in the emulation of the AN/UYK-7, for register and buffer mapping.

The next step in the emulation is to assume that a user's object program is resident in main memory. The emulator must then fetch, decode and execute the program, instruction by instruction. The microprogrammer must decide which emulation functions should be written as subroutines, and which functions should be written in line. The most frequently referenced subroutine in any emulation is the fetch routine since it is executed for every instruction. The normal steps involved in this routine are:

1. Determine the address of the next instruction as indicated by the program address register.
2. Read the instruction from the main memory address calculated in step 1. This is the current instruction to be emulated.
3. Decode the instruction into its designator fields.
4. Calculate the operand address. (The AN/UYK-7 uses a displacement plus an index register plus a base register).
5. Read the operand from main memory.

6. Perform indirection if allowed and indicated.
7. Some instruction sets, AN/UYK-7 for example, allow whole or half-words. Check if current instruction is half-word.
8. Some instruction sets operate on partial word operands. If so determine if quarter, half or full-word operand is to be used.

These steps must be executed for each instruction fetched from the user's program. Depending on the particular instruction being emulated, some of these steps may be omitted (step 8 is only performed for Format I instructions) but the majority are generally applicable. This demonstrates the overhead involved in emulation prior to branching to the microroutine that does the actual instruction execution.

Some hardware additions that can facilitate emulation are a fast shifter and a field select unit (FSU). The shifter simplifies variable-length byte extraction, a common emulation process. For instance, in the D-Machine it takes the same amount of time to shift a word by 1 bit as it does for any shift up to 31 bits. The FSU allows the testing of selected fields without requiring a cycle to go through the adder (the D-Machine does not have this feature). This relieves the programmer of masking and shifting fields prior to testing them. These two features are the most common and cost-effective additions to the hardware.

One approach to emulation that has recently come into use, but which is not that widely used or understood, involves using a combination of hardware, software and operating system. IBM is experimenting in this area, and has established the following design characteristics for the System/370 emulators:

1. Emulators must be integrated with the operating system and run as a problem program. This eliminates the overhead of loading and reloading the emulator and the native mode machines.
2. Allow multiprogramming of emulators as well as a mix of emulators and native mode programs.
3. All programs including emulators must be interruptible.

With such a system IBM felt they could give the user an improved, more efficient environment from which to operate, either in the emulator or native mode. The authors feel this should be a primary field for future applications.

The final item to be discussed in the Section is emulation of Input/Output operations. Most sources agree that emulation of I/O is as difficult, if not more so, than the implementation of the central processor's instruction set. This is true primarily because once the basic routines needed for instruction and operand fetch are programmed, the actual instruction executions are fairly easy to microprogram. This is not necessarily true with I/O - buffers must be set up; data conversion possibly performed; and perhaps the hardest point, emulating circumstances in which results are

not yet known. For instance, if the I/O is to search for a specified record, then what happens if the key cannot be found? There are many such checks or error conditions that make I/O difficult to emulate. Another major problem is emulating interrupt handling during I/O. Since emulation of I/O is essentially a separate topic and since the authors did not implement emulation of the AN/UYK-7 Input/Output instruction set as part of the thesis, I/O emulation will not be described in any further detail. However, references 5, 12, 15, 21, and 22 provide excellent material on this topic.

C. APPLICATIONS

This section is designed to familiarize the reader with some of the applicable areas for emulation usage. It is by no means an exhaustive study of this topic, nor is it intended to be so.

Emulation was first used in, and is still the primary application for, converting from second generation computing systems to third generation systems. Normally, the process is costly and dangerous in the aspect of converting programs running on the existing system to programs capable of executing on the new machine. There are several methods other than emulation capable of performing this task, none of which are completely satisfactory: simulation is slow; automated translation is unproven; and instruction by instruction reprogramming is costly and cumbersome. The advantage of emulation is that if the old machine could be emulated on

the new machine allowing direct execution of all old programs, then the old programs could be converted at leisure, if desired and justified. For example, reprogramming might not be cost effective or justified for a program with an expected life span of six months. In such circumstances continued emulation of the program is the solution. However, the situation might be different if the program had an expected life span of three years.

Another major application for emulation is the design, development, and testing of a newly conceived system on an existing system. The target machine does not necessarily have to be an existing computer system, and the user could experiment with the design of any machine he desires. In this way a richer instruction set can be achieved; moreover, software and diagnostic routines could be developed for the new machine prior to the machine even being produced or marketed. IBM used this method to some extent by emulating System/370 on System/360 prior to building System/370. This application tends to decrease the time from initial construction to marketing because software, such as the operating system, can be tested and debugged concurrently.

A third application, and one seen as a major trend for the future, is the ability of the user to adapt the computer to his individual needs. Modern-day computers are built as powerful, general-purpose machines designed to operate effectively over a large field of problems. In doing so, however, the machine cannot optimize execution of any one

particular application. Emulation gives the user this ability. The user can either operate from an existing emulator, or he can tune the emulator to his individual application through microprogramming. One user may want a machine oriented toward string operations, while another user may be doing extensive scientific calculations. If each user could execute from a separate emulator tuned to his individual application, then each would be more efficient and productive. In addition the computer would probably be easier for the user to program. This is the area where multiprogramming of emulators is projected to be of the most use.

There are several other areas of emulation usage which were not discussed; such as the academic environment for research purposes (the reason for this thesis), and tuning of existing software. However, as previously stated, this section was designed only to give the reader a flavor of the possible uses of emulation and perhaps stimulate his own ideas for possible applications. For additional and more detailed material see references 2, 15 through 18, and 20 through 24.

III. THE AN/UYK-7

This chapter is intended to introduce the reader to those operational characteristics and capabilities of the AN/UYK-7 computer most pertinent to the Emulation. This will assist the reader in understanding the design and mappings used in this Emulation and presented in subsequent chapters. This chapter is not intended to be a technical manual and should not be used for that purpose. The reader should consult references 26 and 27 for more detailed information.

The AN/UYK-7 is a highly reliable, ruggedized, multiprocessor system designed and manufactured by the Univac Division of Sperry Rand Corporation. Built to military specifications (MIL-E-16400), it is utilized extensively throughout the United States Navy in Tactical Data Processing applications [26]. Rapid data transfer rates are provided during communications between external devices, internal random-access memory, and the central processor. The system is capable of average command execution times of 1.5 microseconds, and an input data transfer rate of over one million 32-bit words per second. The AN/UYK-7 maintains two completely separate sets of index, arithmetic and relative address (Base) registers, for use during Task and Executive states. In addition, a set of 18 privileged instructions

with special characteristics for executive control are reserved for the Interrupt State. These features along with the parallelism of AN/UYK-7 field and register references, make it an extremely difficult system to emulate in real-time.

The AN/UYK-7 was designed to operate as either a single or multiple processor system with up to 256K, 32-bit words of random access memory. This allows on-line access to 1024K bytes through an instruction feature which permits whole-word, half-word, or quarter-word memory references. This Emulation assumed an AN/UYK-7 configuration consisting of a single processor, monoprogramming, with one 64K, 32-bit word memory module. Partial word references were fully emulated providing random access to 256K bytes.

A. INTERRUPTS

The AN/UYK-7 processes data in real-time in response to a highly prioritized interrupt system with decision-making properties. This priority system allows the central processor to select that program routine which is necessary to respond to the interrupt requiring the most urgent attention. Since the Emulator was designed for a monoprogramming environment using asynchronous I/O, the interrupt features of the AN/UYK-7 were not fully implemented. Several types of interrupts, such as Program Faults (Illegal Instructions), were implemented and tested. All interrupt handling flags, lockouts and registers were mapped into the Emulator.

This will facilitate full implementation of interrupt features - should a decision be made to incorporate multiprogramming or synchronous I/O in the course of expansion to a full Emulation.

B. CENTRAL PROCESSOR

The AN/UYK-7 central processor contains all the control, arithmetic and timing circuitry required for processing alphanumeric data and for executive functions. The central processor operates in two different modes or states: the Interrupt State executes executive-type functions, and the Task State processes user programs. A group of 16 privileged instructions and a separate set of arithmetic, index and base registers are reserved for the exclusive use of the processor while in the Interrupt State. These features greatly enhance the AN/UYK-7's multiprocessing and multiprogramming capabilities. These special instructions and registers were mapped into the Emulator; however, they were not fully implemented because of the monoprogramming environment in which the Emulator was to be run.

The AN/UYK-7 maintains a central processor control memory (CMR) consisting of 82 integrated-circuit, random-access registers of varying sizes appropriate to their function (e.g. A-registers 32-bits, B-registers 20-bits). The various registers are grouped into stacks according to their use, addressing, and relative size. In the Emulator, these registers were mapped into the D-Machine's main memory

starting at address 0000, with address assignments corresponding exactly to that of the AN/UYK-7. The notable exception was that CMR addresses designated as "Unassigned" in the AN/UYK-7 were used as temporary storage registers in the Emulator. Register mapping is discussed in more detail in Chapter V and presented in tabular form in Figure V-2.

The AN/UYK-7 registers of particular interest to the user are: the Program Address Register (PAR); the Active Status Register (ASR); and the Base, Index and Arithmetic Register groups. These are the only registers which are either directly addressable or accessible to the programmer.

1. Program Address Register (PAR)

The PAR is a 20-bit register used for addressing the next instruction to be fetched from memory for execution. It consists of a 16-bit displacement value and a 3-bit Base Register reference. The effective instruction address is formed by the addition of the displacement and the contents of the selected Base register. The PAR displacement value is incremented by one word at the completion of each instruction cycle with the exception of JUMP instructions. These instructions cause replacement of the PAR by the "s" and "y" operand fields of the JUMP, thus providing for out-of-sequence instruction execution. The PAR mapping in the Emulator is not composed of two separate fields, but rather as the calculated effective address. This greatly simplifies and expedites instruction references; however, it

causes some difficulty with specific instructions which require access to the two separate fields of the PAR. When encountered, this problem was overcome by dividing the PAR value by 8K. Since the Base registers were preinitialized in 8K increments, starting at 1024, the results of the division yielded a quotient equivalent to the Base register assignment, and a remainder equal to the displacement.

2. Active Status Register (ASR)

The ASR is a 23-bit register used to indicate and control the status of various operations in the central processor. Individual bits of the register are assigned special functions, and when set indicate that a particular status exists and that the processor should be controlled accordingly. Individual bits are set/cleared as the result of either an instruction execution or direct processor intervention. The bits of particular interest to the programmer are the arithmetic bits (equal, greater than or equal, overflow, and limits) which are set as the result of arithmetic functions, and may be interrogated by specific instructions, such as conditional jumps. Based on the condition of the bit tested these conditional instructions may cause a change in the program sequence. In the Emulator the ASR bits most frequently referenced by the programmer are mapped into a D-Machine internal register together with the PAR. This considerably reduces main memory references, and reduces Emulator execution time. The ASR mapping is discussed in detail in Chapter V.

3. Base Register (S)

There are two sets (Interrupt, Task) of 18-bit S-Registers, numbered 0-7. These registers, used in final Y-Operand and instruction address calculations, are necessary in a multiprogramming and multiprocessing environment. In spite of the monoprogramming environment of the Emulator, the registers were mapped and used as designed; however, they were preinitialized by the Loader at 8K boundaries starting at address 1024. This provided the Emulator access to 64K of main memory in increments of 8K pages.

4. Arithmetic Register (A)

There are two sets (Interrupt, Task) of 32-bit A-Registers, numbered 0-7. They are used extensively throughout the instruction set to hold one or more of the operand - inputs to, or results of arithmetic functions. The A-Registers also serve as the main interface between the central processor and main memory. These registers are directly addressable by the programmer.

5. Index Register (B)

There are two sets (Interrupt, Task) of 20-bit B-Registers, numbered 1-7. These registers can be used as counters, or they can be employed in a special addressing technique called Indexing. During normal Y-Operand address calculations, the designated B-Register is added to the y-displacement and a specific S-Register to form an effective

address. This address is then considered to have been indexed by the B-Register value. Indexing provides the programmer with the option of sequentially referencing memory by merely incrementing the index during each pass through a loop. Reference to any B-Register other than B(0) implies that indexing is to take place during the Y-Operand address calculation. A reference to B(0) is treated as an index of zero since B(0) is not a valid register. In the Emulator, the contents of B(0) is always zero, and references to B(0) are conveniently treated the same as references to B(1) thru B(7). In the AN/UYK-7, the B-Registers have the same internal structure as the PAR; that is, they consist of two fields (a Base register, and a displacement). In the Emulator, B-Registers are treated as consisting of one field which can be separated into its two respective fields by division by 8K, as previously described in the PAR discussion.

In order to minimize access time and field decoding, all CMR registers were treated as 32-bit registers in the Emulator. This caused no problems with the exception of the PAR and Index Registers, which were resolved as previously discussed. The A, S, and B-Registers are directly addressable through the Load/Store CMR Instructions of the AN/UYK-7. They are incidentally addressable through references in specific fields of the different Format instructions reserved for that purpose.

C. INSTRUCTION FORMAT

Instructions of the central processor appear in five different formats according to their operational characteristics, as presented in Figure III-1. Formats I, II, and III occupy a full, 32-bit computer word; Formats IV-A and IV-B each occupy a half computer word. Two half-word instructions can be stored in one memory location. When a half-word instruction in the upper half of the computer word is executed, the processor sets bit 15 of the ASR; if a whole-word or lower half-word is executed the bit is cleared. In the Emulator, this bit determines whether the subroutine IFETCH or HALFFETCH is executed. IFETCH reads the next 32-bit instruction from memory. HALFFETCH shifts the lower half-word of the current instruction into the upper halfword position for execution.

Each of the five formats divide the instruction into different fields. Each field except "y" (the constant or address field) has a particular function in controlling the various internal enables and commands required for proper execution of the instruction. Some fields define the use, modification or application of the y-field to secure the desired operand; others select an accumulator, index, or base register; others select an IOC, define a sub-function code, or combine to form a special interpretation defined by the instruction. The AN/UYK-7 maintains a repertoire of 132 central processor instructions whose specific functions are defined in detail in reference 26.

Bit No.	31--26	25-23	22-20	19-17	16	15-13	12---0
FORMAT I	f	a	k	b	i	s	y
FORMAT II	f	a	f2	b	i	s	y
FORMAT III	f	a	f3/k	b	i	s	y

Bit No.	31--26	25-23	22-20	19-17	16
Bit No.	15--10	9-7	6-4	3-1	0
FORMAT IV A	f	a	f4	b	i
FORMAT IV B	f	a	m		

INDIRECT CONTROL WORD FORMATS (Indirect Addressing)

Bit No.	31-30	29-25	24-20	19-17	16	15-13	12---0
	c	w	p	b	i	s	y
	c	c1	unused	b	i	d	

Elements of the word are interpreted as follows:

FIELD	BASIC DEFINITION
f	6-bit function code
f2	3-bit subfunction code
f3	2-bit subfunction code
f4	3-bit subfunction code
a	3-bit accumulator register designator
k	3-bit operand interpretation designator
m	6-bit shift count designator
b	3-bit index register designator
i	1-bit indirect addressing designator
s	3-bit base designator
y	13-bit address displacement/operand designator
c	2-bit control designator
c1	1-bit indirect subfunction designator
w	6-bit character length designator
p	5-bit position indicator for character length
d	16-bit address displacement

INSTRUCTION AND INDIRECT ADDRESS WORD FORMATS [27]

FIGURE III-1

Of particular note to the reader is the K-Field of the Format I instructions. The value of K designates whether the operand to be fetched/stored is a whole, half, or quarter-word operand, as depicted in Figure III-2. If the value of K implies a partial-word operation, then it also determines which portion of the 32-bit word is to be accessed. That is, a K-value designating a quarter-word (byte) transfer can also specify that the byte is located in the upper, lower, or one of the intermediate two bytes of the 4-byte, 32-bit operand. It is this function that makes the AN/UYK-7 an extremely powerful word processing machine. This function was fully implemented and tested in the Emulator.

K	READ MEMORY to ARITHMETIC	STORE ARITHMETIC to MEMORY
0	sy(SE)+B(b) -> A15-0(SE)	NOT USED
1	Y15-0 -> A15-0 (SE)	A15-0 -> Y15-0; Y31-16 unchg
2	Y31-16 -> A15-0 (SE)	A15-0 -> Y31-16; Y15-0 unchg
3	Y31-0 -> A31-0	A31-0 -> Y31-0
4	Y7-0 -> A7-0 (ZE)	A7-0 -> Y7-0; Y31-8 unchg
5	Y15-8 -> A7-0 (ZE)	A7-0 -> Y15-8; Y31-16 unchg Y7-0 unchg
6	Y23-16 -> A7-0 (ZE)	A7-0 -> Y23-16; Y31-24 unchg Y15-0 unchg
7	Y31-24 -> A7-0 (ZE)	A7-0 -> Y31-24; Y23-0 unchg

SE--sign extended; ZE--zero extended
A is the ACCUMULATOR specified by the a-field

FORMAT I INSTRUCTION K-FIELD INTERPRETATION [27]

FIGURE III-2

D. MODES OF OPERATION

There are several different modes of operation of the AN/UYK-7; most of them are concerned with different addressing techniques. Specifically, they are: normal mode, index mode, repeat mode, and indirection. In the normal mode, the Y-Operand address is calculated as the sum of: the y-offset, a base register and an index register, or $Y=y+B(b)+S(s)$. There are two exceptions to this general formula. First, if the K-field of Format I instructions is a zero then $Y=sy+B(b)$, where "sy" is the concatenation of the s-field and y-field of the instruction. Second, for all instructions regardless of Format, if the B-field is zero then the B(b) value used in calculating the Y-Operand address is always zero. There are several additional addressing techniques employed during the repeat and indirect modes of operation. They are described in detail in Chapter V. These ad hoc addressing techniques employed by the AN/UYK-7 greatly enhance its capabilities but were extremely difficult functions to emulate.

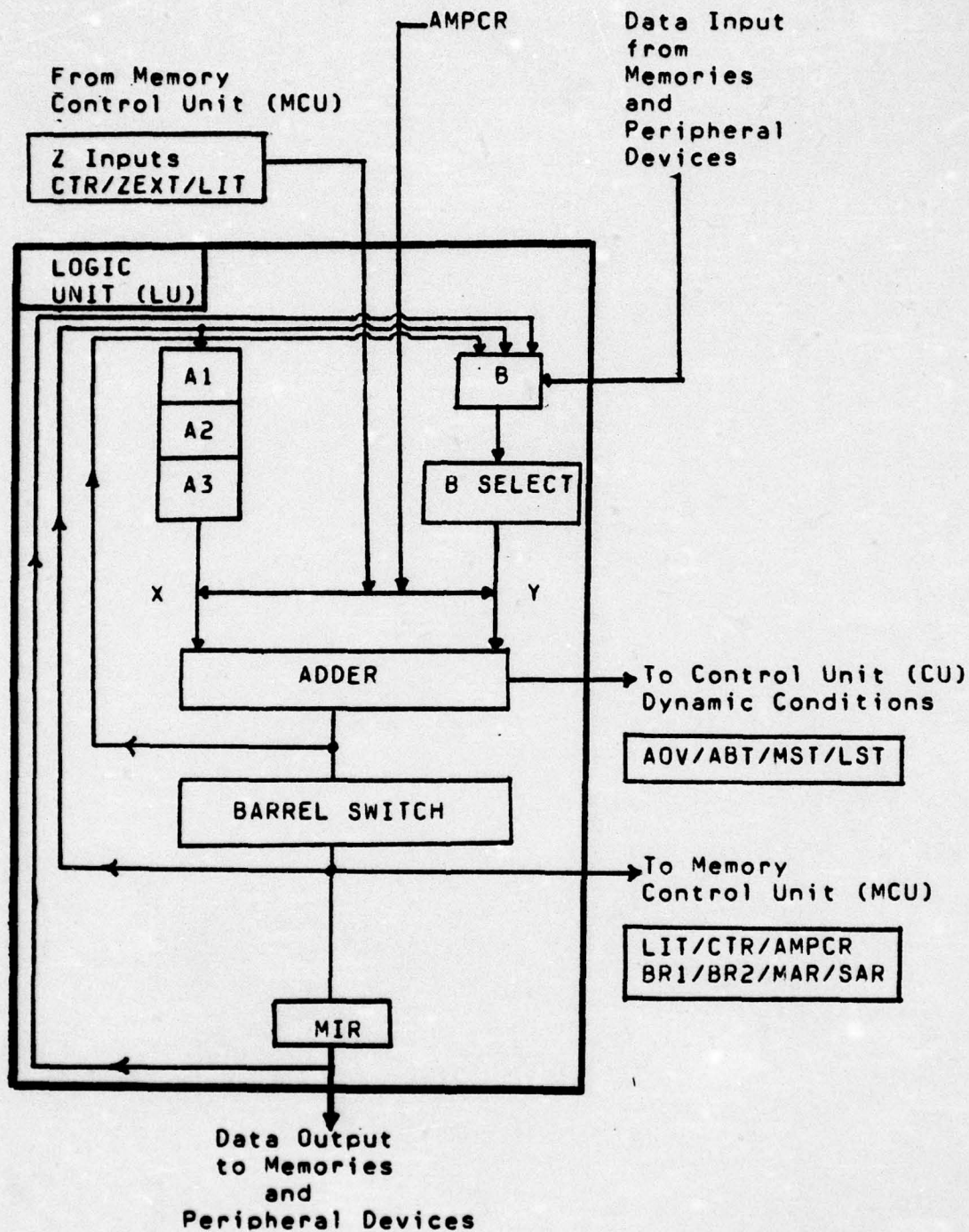
IV. BURROUGH'S D-MACHINE

A. GENERAL DESCRIPTION

An Interpreter Based System is a digital processing concept developed by Burrough's Corporation, that utilizes hardware building blocks which can be tailored through microprogramming to perform as a variety of general purpose or special purpose general processors [7, 8, 24]. The basic Interpreter, also referred to as the D-Machine, is the primary building block of this unique system. It is composed of five functional modules each of which can be modified to manipulate an 8 to 64-bit word format in increments of 8 bits. In the Naval Postgraduate School configuration, two of these modules, the Nanomemory and the Micromemory, are combined into one. The register sizes given in the following descriptions of the modules are specific to this configuration which is a 32-bit D-Machine.

1. Logic Unit (LU)

The Logic Unit (LU), presented in Figure IV-1, contains all the registers, the Barrel Switch and the Adder which are available to the microprogrammer for manipulating data fields during the process of emulating an instruction. A description of each of these registers and its functions follows [8,24].



LOGIC UNIT (LU) BLOCK DIAGRAM

FIGURE IV-1

The 32-bit registers A1, A2, and A3 are functionally identical. They temporarily store data within the Interpreter and serve as the primary (X) input to the adder. Any A-Register can be designated as a destination for the output from the Barrel Switch.

The 32-bit B-Register is the primary external input interface (from the Switch Interlock). It also serves as the secondary (Y) input to the Adder, and can receive the output of the Adder, in addition to the Barrel Switch which is the normal source for the results of arithmetic calculations. The B-Register can be the destination of any of the following during execution of any one microinstruction:

- a. The Barrel Switch output.
- b. The Adder output.
- c. The external data from the Switch Interlock.
- d. The Memory Information Register (MIR).
- e. The carry complements of four-bit or eight-bit groups.
- f. The Barrel Switch output ORed with b, c, or d above.

The output of the B-Register has true/complement selection gates which are controlled in three separate sections: the most significant bit (MSB), the least significant bit (LSB), and all the remaining internal bits. Each of these parts is controlled independently, and may be either all one's, all zero's, the true contents or the one's complement of the respective bits of the B-Register.

The 32-bit Memory Information Register (MIR) buffers the information which is to be written to main system S-Memory, or to a peripheral device. It is loaded from the Barrel Switch output and its output is directed either to the Switch Interlock or the B-Register.

The 32-bit Adder in the LU is a modified version of a straightforward carry look-ahead adder. Inputs to the Adder are from selection gates which allow various combinations of the A, B, and Z inputs. The A input is from the A-Register output selection gates and the B input is from the B-Register true/complement selection gates. The Z input is an external input to the LU and can be:

- a. The output of the counter in the Memory Control Unit (MCU) into the most significant eight bits with all other bits being zeros.
- b. The output of the literal register in the MCU into the least significant eight bits with all other bits being zeros.
- c. An optional input into the middle bits with the most and least significant bytes being zeros.
- d. All zeros.

There are always two inputs to the Adder referred to as the X-input and Y-input. An X-input may have A, Z, or zero as its source. A Y-input may have B, Z, or one as its source. An unspecified X-input is always assumed to be zero. Using various combinations of the possible inputs to the selection gates, any two of the three (A, B, or Z) inputs can be added together, or can be added together with an

additional one added to the least significant bit. In addition, all binary Boolean operations can be performed between any two inputs.

The 32-bit Barrel Switch is a matrix of gates that shifts a parallel input data word from the Adder, any number of places to the left or right, either end-off or end-around. The output of the Barrel Switch may be gated to one or more of the following simultaneously:

- a. The A-Registers (A1, A2, A3).
- b. The B-Register.
- c. Memory Information Register (MIR).
- d. Least significant 16 bits of MCU registers (BR1, BR2, MAR, AMPCR, CTR).
- e. Least significant 5 bits to the Control Unit (CU) for the shift amount register (SAR).

2. Memory Control Unit (MCU)

One MCU is required for an Interpreter to have access to 64K of main memory [8, 24]. The addition of a second MCU is possible, thus expanding on-line memory access to 128K. The MCU has three major sections:

- a. The microprogram address section contains a microprogram count register (MPCR), the 12-bit alternate microprogram count register (AMPCR), the incrementer, the microprogram address controls register, and their associated control logic. This section is used to address the Microprogram Memory (MPM) for the sequencing of microinstructions. The AMPCR contents may be used as a Y-input to the Adder.

- b. The memory/device address section contains the 8-bit memory address register (MAR), the two 16-bit base registers BR1 and BR2, the output selection gates, and their associated control logic.
- c. The Z register section contains registers which are the Z inputs to the LU Adder: a loadable counter (CTR), the literal register (LIT), selection gates for the loadable counter and their associated control logic.

3. Control Unit (CU)

The Control Unit (CU) has five major sections: the shift amount register (SAR), the condition register (COND), part of the control register (CR), the MPM content decoder and the clock control [8, 24].

The functions of the SAR and its associated logic are:

- a. To load shift amounts into the SAR for use in (0 to 32-bit) shifting operations.
- b. To generate the required controls for the Barrel Switch to perform the shift operation indicated by the current microinstruction.
- c. To generate the "word length complement" of the SAR contents, where the "complement" is defined as the amount that will restore the bits of a word to their original position after an end-around shift of N followed by an end-around shift by the "complement" of N.

The control register (CR) is a 56-bit register that stores all those control signals from the current microinstruction which are not used in phase I. The CR is divided into the phase III controls and the MPAD controls.

The condition register (COND) section of the CU performs four major functions:

- a. Stores 12 resettable condition bits in the condition register. The 12 bits of the condition register are used as interrupts, error indicators, status indicators, and lockout indicators.
- b. Selects 1 of 16 condition bits; 12 from the condition register and 4 dynamically generated during the present clock time in the Logic Unit for use in performing conditional operations.
- c. Decodes bits from memory for resetting, setting or requesting the setting of certain bits in the condition register.
- d. Resolves priority among Interpreters in the setting of global condition (GC) bits which provide a facility for inter-Interpreter lockout control.

4. Microprogram (M-Memory)

The Micromemory (M-Memory), also known as the Nanomemory (N-Memory) in the Naval Postgraduate School configuration, is a programmable control store memory which contains the user supplied microprograms in the form of microinstructions. Each microinstruction consists of a 56-bit nanoinstruction and provides the gating for functioning of the previously discussed LU, MCU, and CU modules. Micromemory consists of two 4K, 56-bit, modules allowing the

programmer access to approximately 8K of control store. The sequencing of microprogram instructions is controlled by the following procedure: the Nanomemory provides information to the condition testing logic indicating which condition is to be tested. The condition testing logic provides a TRUE/FALSE signal to the successor logic which selects between the three TRUE and three FALSE successor bits. These three successor bits provide eight possible successor command combinations which are listed below with their associated interpretations:

- | | |
|---------|--|
| a. WAIT | Repeat the current instruction |
| b. STEP | Step to the next Instruction |
| c. SKIP | Skip the next instruction |
| d. JUMP | Jump to address in AMPCR |
| e. RETN | Return from a micro subroutine |
| f. CALL | Call a micro subroutine |
| g. SAVE | Save the address of the head of a loop. |
| h. EXEC | Execute one instruction out of sequence. |

The particular successor command specified then provides the controls needed in the selection (MPCR/AMPCR) and incrementing logic to generate the next MPM address. Except for the EXEC command the MPCR is loaded with the MPM address.

For a more thorough description and discussion of these five modules, reference 10 provides an outstanding

diagrammatic breakdown of the Interpreter's internal hardware configuration and operation. Reference 7 discusses the interface of various Interpreter, peripheral, and memory configurations that have been tested by the Advance Development Organization of Burrough's Defense Space and Special Systems Group.

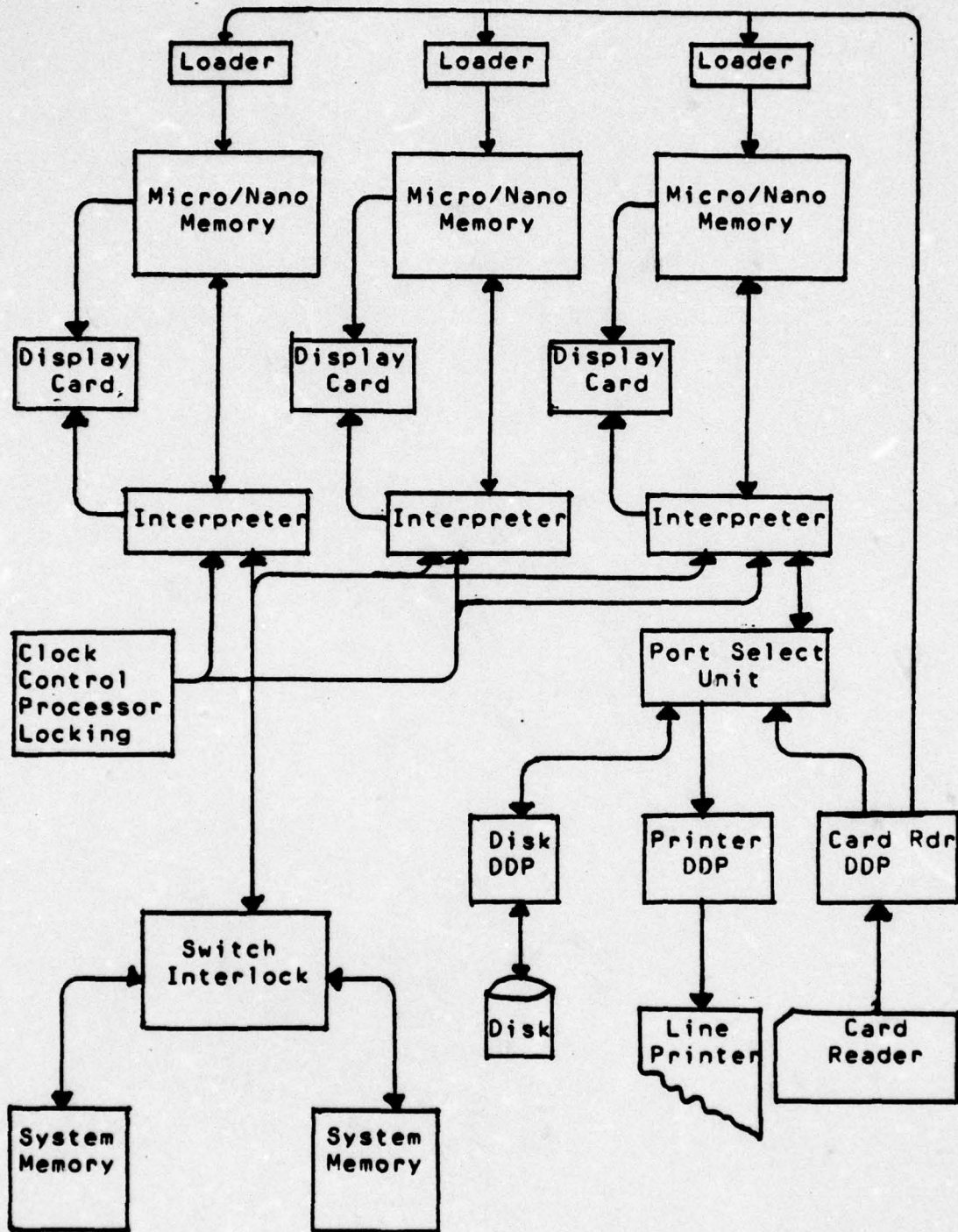
In general, there are three data processing functions to which the Interpreter may be applied: emulation of existing or hypothetical machines; direct execution of high level languages; and problem solution through microprogram "tuning" of the machine to the problem. The initial goal for the installation at the Naval Postgraduate School is emulation of existing machines such as the AN/UYK-7, with further expansion and development as a teaching tool in the areas of operating systems, file management, compiler writing, and emulation of hypothetical systems.

B. NAVAL POSTGRADUATE SCHOOL CONFIGURATION

1. Description

The system presently installed at the Naval Postgraduate School consists of three Interpreters, one 64K memory module, a card reader, line printer and dual cartridge disk. Only one of the three Interpreters is allowed to communicate directly with any peripheral and is discussed below under I/O Interface. Figure IV-2 represents the present configuration; however, future expansion calls for the addition of a supervisor's console and a cross-connection with the school's PDP-11/45. This will enhance the attached peripherals by three tape drives and greatly increase the amount of on-line storage to the point where implementation of a CMS-2 Compiler may be feasible.

When the system is energized and initialized daily, its basic microstructure is that of two B-6700 LIFO ALGOL Stack Machines - each with 32K of memory - attached to a single Input/Output Processor. The system is capable of pseudo-multiprocessing in this configuration. ALGOL programs submitted through the card reader are executed in a batch mode with the two processors competing to fetch the next job. All utility programs, the operating system and the file manager are executed with the machine in this configuration. In order to change the machine's configuration, the user must alter the microcode in order to execute the desired machine such as, the AN/UYK-7.



NAVAL POSTGRADUATE SCHOOL THREE INTERPRETER SYSTEM

FIGURE IV-2

2. I/O Interface

Since only one Interpreter (IOP) is allowed to exchange data directly with the peripherals, it is necessary for the remaining two processors to communicate their I/O requests to the IOP. This is done by the Interpreter placing a message in address 64K otherwise known as the "Mailbox", and then issuing an interrupt (INT) to the IOP. The IOP periodically tests for INT and when sensed, reads the Mailbox, decodes the message, and performs the predefined function. After completing its task, the IOP places a message in the Mailbox informing the requesting Interpreter whether or not the I/O was performed successfully. The IOP then issues an INT to the Interpreter which sent the request. When the requesting Interpreter receives the INT, it reads the Mailbox to determine whether its request was performed and continues accordingly. This method allows the two Interpreters to act completely independently, each referencing only its assigned segment of memory and the IOP performing all I/O asynchronously upon request.

3. Memory Interface

The memory module consists of a single ported, 64K, 32-bit word, core memory, which is the equivalent of 256K of on-line, 8-bit character storage. Access to this single memory is through a Switch Interlock Unit (SWI) which makes memory appear to be multiported to the user. The SWI acts on a priority basis with that Interpreter having the lowest

number (the IOP) given the highest priority. Once an Interpreter issues a memory read/write reference, it may continue execution and need not wait on a memory completion signal. However, the memory address register (MAR) on a Read/Write, and the Memory Information Register (MIR) on a write, should not be changed until a completion signal is received. Thus a microprogrammer who anticipates his memory accesses and intersperses these instructions among the other code, should never have a delay caused by memory referencing.

C. INSTRUCTION TIMING

The Interpreter uses a one megahertz clock and initiates a new microinstruction every microsecond. The Interpreter enhanced with Emitter Coupled Logic (ECL) and a higher speed memory can operate off an 8 Megahertz clock. A corresponding 8-fold improvement in execution times can be expected.

There are two basic instruction types in the Interpreter. Type I uses two phases (I and III) for execution; although, its phase III may be held in abeyance until completion of a subsequent Type II, which always uses only phase I to complete. Phase I of the following Type I instruction always overlaps Phase III of the previous Type I. Type I instructions involve condition testing, external functions and Adder/Logic operations. Type II instructions involve literal assignments to one of three registers (LIT, SAR and AMPCR). Appendix D of reference 9 contains an excellent discussion of instruction timing.

D. LANGUAGES

The D-Machine has two resident programming languages: the language of the operating system, ALGOL; and the microprogram assembly language, TRANSLANG.

1. ALGOL

The resident programming language of the Burrough's D-Machine is the ALGOL 60 Language enhanced with additional language constructs which permit manipulation of data in the form of character strings. ALGOL employs a vocabulary of reserved words and symbols. The structure of the language, syntax, reserved words and symbols, and additional features of the ALGOL implemented on the D-Machine are discussed in reference 10. The accepted character set for ALGOL varies depending on the machine used and the character set or sets available on the machine. The Naval Postgraduate School configuration requires that all characters be converted from EBCDIC into the 6-bit Burrough's Common Language (BCL) format for recognition by ALGOL. This conversion is performed by the IOP when it is used for interfacing communications from external devices to the other Interpreters. When information is directed to an external device the IOP performs a reverse conversion, from BCL to ASCII. Thus all inputs to the emulator from peripherals are 8-bit characters containing a 6-bit BCL code. The Interpreter's file management routines, operating system and utilities are written in ALGOL, for execution on the ALGOL Stack Machine

configuration. ALGOL source modules may be inputted to the ALGOL Compiler from disk or cards. Object modules are placed in user libraries on disk for future execution by the stack machine. The operating system (MCP) will load specific object modules for execution when it recognizes a "?RUN filename" control card, where filename is assumed to be a precompiled ALGOL program.

2. TRANSLANG

The microprogrammer is aided in producing microprograms by a Microtranslator/Assembler that translates symbolic instructions written in TRANSLANG into microinstructions. Reference 9 describes the structure of TRANSLANG by defining its syntax and semantics, and presenting a series of examples. The reference also includes descriptions of register state changes resulting from executing microinstructions. Interpreter controls and timing are explained. Coding techniques and conventions are discussed via sample programs. The reference analyzes external operations with main memory and peripheral devices, and the coordination and control of multiple Interpreters via the Switch Interlock and global condition bits.

The Microtranslator is written in ALGOL for the D-Machine. It is written modularly with each function setup as a procedure call. The language, TRANSLANG, used ALGOL as a model; however, almost the entire language is composed of reserved words. Reserved words have very specific meaning

to the translator and cause specific nanoinstructions to be developed. TRANSLANG is free form and each instruction may be written in almost any order; however, multiple instructions appearing on the same line or card must be separated by a period. Each TRANSLANG instruction corresponds to one microinstruction, which is the set of Interpreter functions performed in parallel at each machine clock. The constructs provided include iterative mechanisms, I/O, Boolean, logical and computational operations, control transfers, and assignment functions. In order to provide control points for transfer operations, each instruction may be labeled with a symbolic M-Address. The output module of the Microtranslator is placed on disk and when loaded into micromemory, alters the basic machine configuration. Reference 9 is used as the microprogrammer's programming manual; although, there have been several enhancements to the machine and language which are not included in the manual. These modifications are discussed in Appendix A of this thesis.

V. PROJECT DESCRIPTION

The AN/UYK-7 achieves its speed and versatility partially through concurrent field utilization and partially through the provision of special and general purpose registers. Its emulation is complicated by the various modes of instruction operation (repeat, indirection, indexing) and in particular by the use of ad hoc addressing techniques. The fact that the AN/UYK-7 performs many of its operations in parallel makes it difficult for an emulation which is imitating one facility at a time to run in AN/UYK-7 real-time. For the remainder of this discussion the acronyms A(a), B(b) and S(s) refer to the Accumulator, Index and Base registers, respectively. The subscripts (a, b, and s) correspond to the register specified in the cognizant field of the instruction, and may assume values of 0 to 7. Capital "Y" refers to the effective 18-bit, operand address; small "y" refers to the 13-bit, y-field of the instruction. The combination sy-field is formed by concatenation of the 3-bit, s-field and 13-bit, y-field of the instruction and forms an alternate operand address.

During the initial analysis of the Emulation it was decided to separate the project into the following phases:

First, the machine would be designed to accommodate a full emulation including multiprogramming and all IOC

functions. This required that all registers and condition bits of the actual AN/UYK-7 hardware be mapped into the model, even if they would not be used during this partial Emulation.

Second, it was decided to divide the Instruction Repertoire into the following groups:

- a. Those instructions that could be emulated immediately and tested completely; such as, all Format I's and II's except Multiply, Divide, Square Root and Double Register Operations.
- b. Those instructions that could be done prior to completion but for which there might be insufficient time for complete testing; such as, all Format III's, Shifts, Multiply, Divide, and Double Register Operations.
- c. Those special instructions and functional modes that would be incorporated if at all possible; such as, indirection and repeat.
- d. Those features for which there would definitely be insufficient time for incorporation; such as, Interrupts, IOC Instructions, and Floating Point Operations.

Third, a "Loader" program which could read AN/UYK-7 instructions from cards, decode them and place the results into memory for execution by the Emulator was mandatory.

Fourth, some facility for monitoring and debugging each instruction as it is executed by the Emulator would be required.

Fifth, some facility to output the results of each AN/UYK-7 program and to input test data was needed.

To accomplish these five tasks, two basic programs called the "Loader" and the "Emulator" were written. Each of these programs occupied its own Interpreter whenever the system was reconfigured as an AN/UYK-7.

A. LOADER

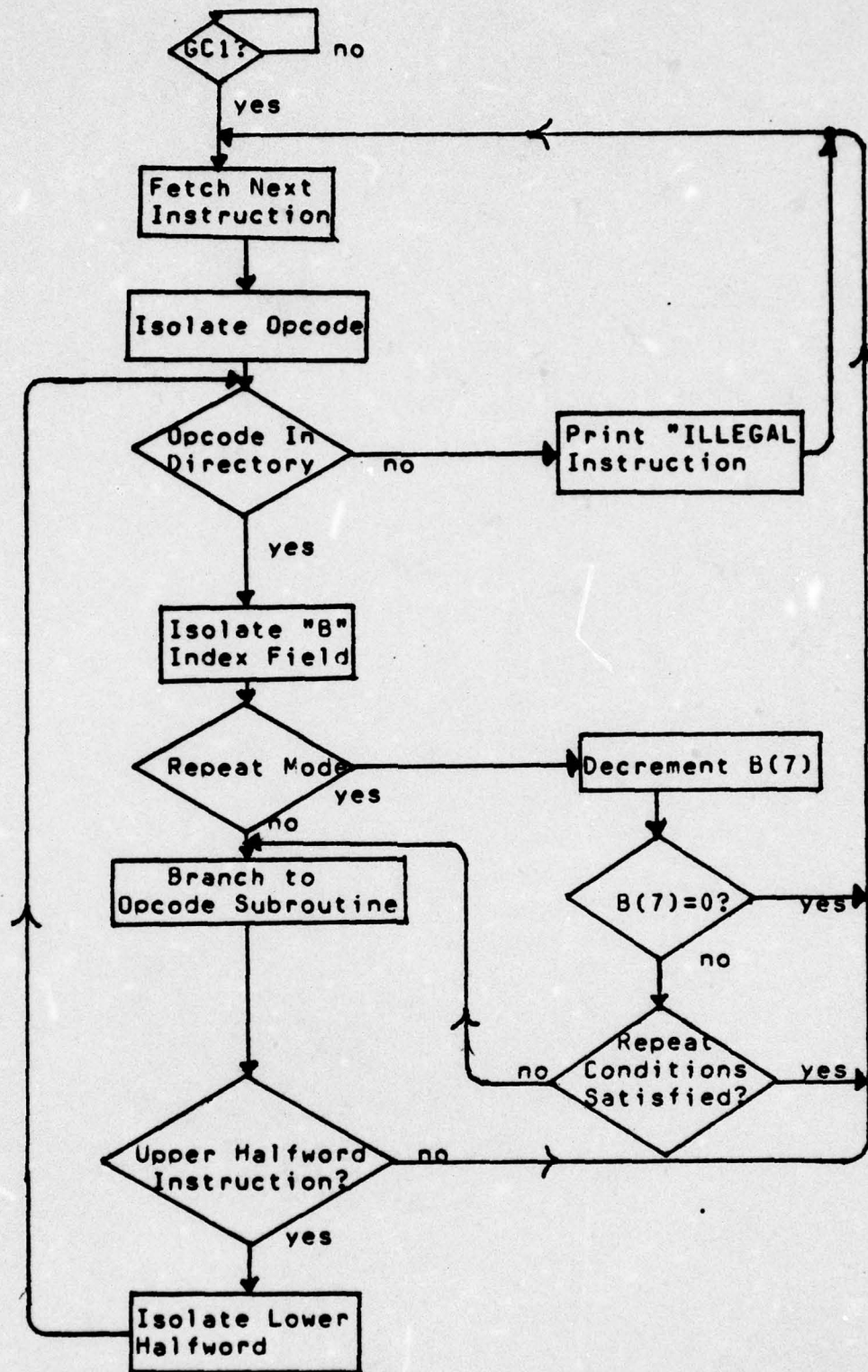
The Loader was written in TRANSLANG and fulfilled the third, fourth and fifth requirements; that is, it served as a combination loader, debugger and IOC monitor. Its use is described in Appendix A, the User's Manual section of this thesis. In general, the loader portion of the program acts like a pseudo-assembler. It has macros for defining a constant or character string, for saving space, for initializing registers and switches, and for inputting instructions. The loader will accept one instruction per card and determine whether it is a Format (I, II, III, IV-A, or IV-B) instruction. Based on this determination, the Loader will decode the specified fields from the card and generate a binary instruction which is placed in the next sequential location in the user's memory. Upon detecting an "N" card, the loader portion of the program signals the Emulator - which is resident in the alternate Interpreter - that instructions are available for execution.

At this point the loader function ceases and the program can be called upon by the Emulator to act as a debugger or as an IOC. As a debugger, the Loader can be used to generate a number of error messages to the operator, or to provide an actual dump of control memory registers 000 to 035, which includes all Task Registers, the PAR and the Active Status Bits. As an IOC, the Loader can be called upon to read a card, print a buffer, or read the disk.

It should be emphasized that the Loader was written strictly as a tool to assist in the development and testing of the Emulator. Presumably, once a full emulation is written and tested, the IOC functions will be incorporated into the Emulator, while the loader and debugger functions will be either written in AN/UYK-7 Machine Language, or absorbed by the Emulator. When this is done, the Interpreter previously utilized by the Loader will be free for loading as a second AN/UYK-7, and a true multiprocessing environment could be created. A copy of the Loader is provided in Appendix C.

B. EMULATION PROGRAM

The Emulator was written in TRANSLANG microcode, and is loaded directly into the Interpreter's micromemory from disk. A copy of the Emulator is provided in Appendix B. Overall program flow for the Emulator is presented in Figure V-1.



OVERALL PROGRAM FLOW

FIGURE V-1

Besides the necessary Control Memory Register mappings, it was necessary to minimize memory references by maintaining certain frequently used information in the D-Machine's internal registers. For this reason, the PAR is maintained in the lower 20 bits of the D-Machine's A2 register. The upper 12 bits of A2 are used to maintain some of the most frequently referenced bits of the AN/UYK-7's Active Status Register as listed in Table V-1.

ASR Bit	A2 Bit	Function
2	31	Equal/Unequal
1	30	Greater Than/Equal
0	29	Limits
3	28	Fixed PT Overflow
8	27	Task use of 05-4
9	26	Remove Interrupt Lockouts
10	25	Int/Task Accumulators
11	24	Int/Task Base Regs.
N/A	22-23	01 = Indirection 10 = Optional Indirection 11 = Character Addressing
N/A	21	Repeat Mode
15	20	Halfword Indicator
N/A	0-19	PAR

ACTIVE STATUS REGISTER

TABLE V-1

The remaining bits in the ASR are not used in this Emulation, but if needed could be mapped into any unused location in memory below address 1024.

The D-Machine's A1 register is used to maintain a copy of the instruction currently being executed. All other registers are free for computational use. The D-Machine's

General Condition Bit One (GC1) is reserved for communicating with the Loader. General Condition Bit Two (GC2) is used to indicate that an AN/UYK-7 instruction is being executed under a special condition; such as, repeat mode or in-direction.

The Emulator consists of an Opcode/Sub-opcode Directory, an instruction fetch routine (IFETCH), global subroutines and opcode execution subroutines. When the Emulator receives a signal from the Loader (GC1) to commence execution, it immediately passes control to IFETCH, which reads the PAR and places the first instruction in A1. The opcode portion of the instruction is isolated and used as a pointer into the Opcode Directory. Control is then passed to the opcode execution subroutine designed to handle that particular instruction. The opcode subroutines may stand alone and perform their functions independently; or they may call several global subroutines used to consolidate code for multiple opcodes. Upon completion of its execution, the opcode subroutine passes control back to IFETCH which then fetches the next instruction.

In the case of halfword instructions, control is passed to HALFFETCH which serves the same purpose as IFETCH, except for 16 bit instructions. Every attempt is made within the opcode subroutines to do in-line coding versus subroutine calls. This decreases execution time considerably; although, it greatly increases program size. During the initial programming phase the Interpreters were limited to a

4K micromemory due to the dynamic overlay routine (SMX) being positioned at 4k. As a result, excessive subroutine calls were necessary in order to keep the program size below 4K. This software deficiency has since been corrected by Burrough's and a full 8K micromemory is now available. These subroutine calls could now be removed and the subroutines moved back in-line.

Emulation of Central Processor instructions in the AN/UYK-7 repertoire was fairly straightforward. Most instructions were implemented with an average of 15 microinstructions. This generally included: isolating the various fields, forming the effective operand (Y) address, fetching the operands from main memory, performing the instruction function, and writing the result back to main memory, commonly referred to as S-Memory. Because of the parallelism of the D-Machine's nanoinstructions several of these functions were performed simultaneously. Many AN/UYK-7 instructions have sub-opcodes, each of which perform a different operation on the same operands. In such cases, the opcode subroutine centralized code by performing the field isolation and operand fetch functions prior to calling the subopcode subroutine. Either the operand itself or its address was passed in a register to the subroutine, which then performed its function and wrote the results back to S-Memory.

The difficulties arose in the AN/UYK-7 Emulation when the repeat and indirection modes of operation were implemented. The Repeat Instruction required that the next

sequential instruction be executed the number of times contained in the Index Register B(7), or until specified alternate conditions were met. This required that flags be set indicating that the repeat mode had been initiated and that special termination conditions were to be tested. Condition testing took place after each execution of the repeated instruction and prior to return to IFETCH for the next instruction. If the conditions were not satisfied IFETCH was bypassed and the same instruction was reexecuted after first decrementing B(7), and then indexing the operand address by the displacement value contained in the repeat instruction. If the conditions were met the normal IFETCH mode was executed and the repeat mode was terminated. Most instructions required checking the condition of a specified accumulator register to signal completion of the repeat mode; however, compare instructions used the results of their comparison to signal completion. Repeated replace instructions used a different Y-operand calculation for their store phase then for their fetch phase. Instructions that were not designated as being repeatable were executed once and the repeat mode was terminated. A copy of the Repeat Instruction was saved in S-Memory at address 0030; a copy of the instruction being repeated was saved at address 0031; and the Y-operand address used for storing during a repeated replace instruction was saved at 0033. These addresses are given in octal and are normally unused in the AN/UYK-7.

The indirect modes of operation possible in the AN/UYK-7 were extremely difficult to emulate. There are four modes of indirection possible: Normal Indirection, Character Addressing, Sequential Character Addressing, and Optional Indirection. Not all instructions are indirectable and some instructions are indirectable but not character addressable. To make this determination a table was created in the Emulator which would return a value based on the instruction opcode. This value indicates whether an instruction is repeatable, indirectable, or character addressable. All modes of indirection are initially signalled by the i-field of the instruction being a one. This indicates that the Y-operand points to an Indirect Control Word (ICW). The ICW, which is presented in Figure III-1, is then fetched and its bits 30-31 are examined to determine the indirection mode. In all cases, if the i-field of the ICW is set, the Y-operand again points to a new ICW. The Y-operand is calculated in accordance with the indirect mode. Operand fetching will continue in this manner, cascading through memory, until an ICW is found without its i-field set. At this point the lower 20 bits of the ICW replaces the lower 20 bits of the original instruction.

Normal indirection is indicated by a binary 10 in bits 31-30 of the ICW. Y-operand address calculation is performed as $Y=y+B(b)+S(s)$. Once the final ICW is determined then normal execution of the instruction resumes.

Single Character Addressing is indicated by a binary 01 in bits 31-30 of the ICW. Y-operand address calculation is performed as $Y=y+B(b)+S(s)$; however, in this mode two additional fields (P,W) of the ICW are meaningful. The P-field indicates the least significant bit position of the character to be fetched from the operand and the W-field indicates the number of bits in the character. When the character is fetched - it is right justified; operated on in accordance with the instruction; and then (depending on the instruction) ORed back into its original position in the Y-operand.

Sequential Character Addressing indicated by a binary 11 in bits 31-30 of the ICW, operates in exactly the same manner as Single Character Addressing except in the case where the store cycle is required. Before ORing the resulting character back into the Y-operand the P and W-fields are compared. If P minus W is positive then the difference replaces P and the character is stored accordingly. If the difference is negative then 32 minus W replaces P and the "sy" field of the ICW is incremented by 1 and replaced in memory for the next execution.

Optional Indirection is indicated by a binary 00 in bits 31-30 of the ICW. In this mode bit 29 of the ICW is also significant and modifies the Y-operand address calculation. If bit 29 is 0 then $Y=sy+S(b)$. If bit 29 is 1 then $Y=sy+B(b)+S$, where S is designated by bits 17-19 of B(b). Once the first operand is fetched then normal instruction execution occurs.

A large portion of the Emulation code was devoted to handling the four modes of indirection and its ad hoc address calculations. General Condition Bit 2 (GC2) was used to flag the indirect and repeat modes of operation. Address 0032, octal, in S-Memory was reserved for saving the current ICW being used during Character Addressing; address 0033, octal, was reserved for the Y-operand address in the case of optional indirection; address 0034, octal, was reserved for the address of the current ICW which could be updated during sequential character addressing. These addresses are part of the Control Memory Registers and are not normally used in the AN/UYK-7.

Although the IOC has not been emulated, Input/Output functions were implemented which make the systems' peripherals accessible to the user. The AN/UYK-7 Initiate I/O instruction was implemented in the Emulator with the exception that the a-field, which is normally used as a channel designator, actually designates the desired peripheral. Based on the contents of the a-field, a function code is formulated and passed to the IOC portion of the Loader. The Emulator then enters a neutral state awaiting an Interrupt from the Loader that the I/O has been performed. The Y-operand address of the I/O instruction fetched by the Emulator points to the address of the buffer, rather than to a buffer control word as in the AN/UYK-7. It was felt that

implementation of I/O in this manner would remain virtually transparent to the user, and would facilitate full emulation of IOC functions at a later date.

Of the 132 instructions in the AN/UYK-7 Repertoire, 111 have been fully implemented and tested. One instruction (Return Jump) has been implemented but not tested. Twenty instructions remain to be both written and tested. All unwritten instructions were assigned space in the Opcode Directory and, if used by the programmer, will cause an error message to be printed to the effect that the instruction has not been yet implemented. The implementation of these instructions involves developing the required microcode and inserting it into the space already allocated in the Opcode Subroutine Library. The unimplemented instructions include all Floating Point Operators, Scale Factor, and Interrupt Handlers.

The Repeat Instruction and its associated mode of operation have been implemented and tested with the exception of the repeat replace instructions, which have been written but not yet tested. Indirect addressing has been fully implemented but has not been tested. Input/Output functions of the IOC have been implemented and tested allowing the user to read a card, print a buffer, or read a disk sector. The disk write function has been designed into the Emulator but not implemented for fear of destroying resident disk material during execution. This function should not be fully employed until either a monitor system is developed which

would preclude write access to assigned disk sectors, or the assumption is made that the entire disk is available to the user as a scratch pad.

C. REGISTER MAPPING

Because the D-Machine has few registers available to the user, the authors chose to map all of the AN/UYK-7 registers into main memory. In addition, it was necessary to create several special locations to hold temporary results or conditions. In order to facilitate this mapping, all memory locations below 1024 decimal are reserved; thus, all user instructions and memory references were offset by this amount by the Loader. Since this Emulation will be in a monoprogramming environment, all Base Registers were initialized in increments of 8K with the first Base Register set to 1024. This allowed user access to approximately 63K of main memory, with each Base Register referencing an 8K page of memory. The Control Memory Register (CMR) allocations and additional temporary mappings (indicated by an *), are presented as part of Figure V-2. The registers marked "*" are not used in the AN/UYK-7, and were thus assigned special purposes in the Emulator. Additional unused register areas are available and labelled "unused" in Figure V-2. These register areas could be employed for the same purposes if needed in the course of expansion to a full emulation.

OCTAL ADDRESS	DECIMAL ADDRESS	DESCRIPTION
0-7	0-7	Task A-Reg. (0-7)
10	8	Unused
11-17	9-15	Task Index B-Reg. (1-7)
20-27	16-23	Task Base S-Reg. (0-7)
*30	24	Repeat Instruction Temp.
*31	25	Current Instruction being Repeated
*32	26	Current Indirect Control Word (ICW)
*33	27	Y-operand for Indirection
*34	28	ICW Address in Memory
*35	29	Program Address Register
36-57	30-47	Unused
60-67	48-55	Interrupt Breakpoint Registers (0-7)
70-77	56-63	Active Status Words (0-7)
100-107	64-71	Int. A-Registers (0-7)
110	72	CP Monitor Clock
111-117	73-79	Int. Index B-Reg. (1-7)
120-127	80-87	Int. Base S-Registers (0-7)
*130	88	Switch Values Temporary
131-137	89-95	Unused
140-157	96-103	Designator Storage Words (DSW)
160-167	104-111	Storage Protection Registers (SPR)
170-177	112-119	Segment Identification Registers (SIR)
*200	120	Location Counter
*201	121	Real Time Clock
*202-246	122-166	Disk Input Buffer
*247-323	167-211	Disk Output Buffer
*324-357	212-231	Card Input Buffer
360-365	232-237	Unused
*366-426	238-270	Printer I/O Buffer
427-437	271-279	Unused
*440-1777	280-1023	Error Routines
2000-77775	1024-65533	User Program Area
*77775-77776	65534-65535	Mailbox

*-Temporary Location Established By Programmers Convention

REGISTER - MEMORY MAPPING

Figure V-2

D. TIMING

Although no formal timing survey was conducted, an analysis of the Emulation itself provided an indicator which was used in developing a comparison to real-time. For this analysis it was assumed that each instruction was executed using direct addressing and not in repeat mode. The IFETCH routine used 16 microseconds which was an automatic overhead acquired by all instructions. The operand fetch and store routines (YFETCH, YSTORE and Y2FETCH) added an additional 33, 30, or 14 microseconds, respectively. Thus any instruction which referenced a Y-operand incurred an additional overhead of 14 microseconds at a minimum. Adding to this overhead, the execution time of the basic opcode itself yielded the time estimated for typical instructions given in Table V-2.

INSTRUCTION TIME	OPERANDS	EMULATION TIME	AN/UYK-7 TIME
Load	Register, Y	60	1.5
Add	Register, Y	63	1.5
Add	Register	36	1.0
Divide	Register, Y	600	15

TIME ESTIMATES

TABLE V-2

Using these figures it was estimated that this Emulation ran on the order of 40 times real-time. Two steps could be taken that would considerably improve this time. First, move all out-of-line subroutine calls in-line in the opcode subroutines. Second, enhance the Interpreter as discussed under Instruction Timing in Chapter III. It has been estimated that this same Emulation could run at approximately 5 times real-time on an enhanced D-Machine. This time compares favorably with a Simulation of the AN/UYK-7 written in PL-360 for the IBM 360, which runs on the order of 1000 times real-time. As discussed in Chapter II, it would be difficult to approach real-time in emulating the AN/UYK-7 because of the parallelism of its fetch and field isolation operations. The addition of a Field Select Unit (FSU) and additional internal temporary registers would be required before a real-time emulation could be realized.

VI. SUMMARY

The authors' conclusions and recommendations resulting from any research project are a fundamental part of the formal presentation and are therefore included in this thesis. In addition, the authors felt that the reader, who might be contemplating an emulation project, would be interested in the problem areas encountered during the pursuit of this thesis. Accordingly this chapter is divided into two sections - Problems and Conclusions.

A. PROBLEMS

During the course of this emulation numerous software and hardware problems were encountered which had a considerable effect on progress and the amount accomplished in the allocated time. Software problems stemmed principally from poor documentation of the D-Machine, the AN/UYK-7, their associated languages and internal configuration. The software problems with the D-Machine were generally resolved through experimentation on the machine or through phone calls to Burrough's Advanced Development Organization (ADO). The lack of thorough AN/UYK-7 documentation proved to be a more severe handicap since no test base for experimentation was accessible at the Naval Postgraduate School. Such a medium is absolutely mandatory when working in the emulation

environment. The programmer must be able to determine the machine reaction to unorthodox instruction configurations. Some degree of assistance was provided by the Fleet Combat Director Systems Support Activity (FCDSSA), San Diego; however, in some cases the result was a "best guess" as to what the AN/UYK-7 response would be.

Hardware problems are to be expected during the course of any major project and particularly when a new machine is involved. This Emulation was the first project to be undertaken on the Naval Postgraduate School's D-Machine since the machine was installed. The estimated mean-time-between-failures (MTBF) experienced by the authors was less than five hours. Problems ranged from loose circuit boards and dirty contacts, to disk read/write head misalignment. Unfortunately, the time to repair was aggravated by the fact that the school has no technicians trained on the D-Machine, and the authors were inexperienced in its maintenance and operating procedures. Without the assistance provided by Burrough's ADO the project could not have been seen through to fruition. The ADO provided the school with engineering assistance on three separate occasions, the last of which uncovered a major design problem. The machine has since been modified and the system is presently very reliable.

In addition to these two major problem areas progress was inhibited by the following:

1. Lack of Software Utilities - Since the D-Machine was a new installation the school has not had the opportunity to generate the numerous desirable software utilities. In an effort to eliminate the inherent slowness of a "Card Only" system, the authors have undertaken the implementation of the supervisor's console as an adjunct to this thesis. The authors are also implementing a Text Editor which will allow for on-line program modification, and will replace the present card input Line Editor.
2. Microprogramming is not a new concept at the Naval Postgraduate School; however, actual experience was lacking. The Computer Science Department has played a major role in implementation of the D-Machine and the required expertise is rapidly being developed.
3. The learning curve for undertaking an emulation is tremendous. The target machine, the host machine, their respective programming languages and internal configurations must be learned and understood in minute detail.
4. The target machine for this Emulation, the AN/UYK-7, is an extremely sophisticated and difficult to understand computer. The central processor instruction set is fairly straightforward and easy to implement; however, the numerous and differing modes of operation severely complicated the Emulation.

B. CONCLUSIONS

The authors feel that they have successfully achieved their goal of demonstrating the feasibility of emulating the AN/UYK-7 on the Burrough's D-Machine. The design presented in this thesis is a workable design as evidenced by execution of AN/UYK-7 programs successfully and by execution in

less than 40 times the actual execution time of the AN/UYK-7. Better than 90% of the AN/UYK-7 Instruction Repertoire has been implemented and tested, thus providing a sound foundation for a full emulation. The design allows for expansion to a full emulation which would include the IOC instruction repertoire and Floating Point without major modification. Further, the authors have concluded that by modification of the design to place out-of-line subroutine calls in-line and enhancement of the D-Machine, the Emulation would execute within 5 times the actual speed of the AN/UYK-7.

During the course of this project the authors had an opportunity to visit the Naval Surface Weapons Center (NSWC), Dahlgren, Virginia. Emulation in general was discussed with the programming staff, who had just completed emulation of the Trident Computer on the Nanodata QM-1, and who were contemplating emulating the AN/UYK-7 on the QM-2. Based on these discussions, the experience gained in the course of this thesis, and presupposing the present level of knowledge of the authors; it is estimated that a complete emulation of the AN/UYK-7, its IOC and all Interrupt functions would require an additional 2 man years of programming effort. This estimate includes a reasonably sophisticated degree of testing, and assumes full accessibility of the D-Machine and an AN/UYK-7 test base.

VII. RECOMMENDATIONS

The authors feel that this thesis has provided them with a learning experience previously unparalleled in either of their lives, since it has entailed detailed and independent learning of emulation, microprogramming (TRANSLANG), the Burrough's D-Machine and the AN/UYK-7. In addition, the authors became part time technicians in an effort to keep the D-Machine running. It is felt that the same educational horizons await any student considering a similar project; however, in an effort to keep others from having to "reinvent the wheel", the authors have included much of what was learned about these subjects in this thesis. Hopefully, by building on these experiences, others will be able to begin at a much higher level and consequently accomplish more. The following recommendations are submitted for consideration by anyone inclined to undertake a thesis involving emulation.

1. Do not try to emulate a machine that uses hardware interrupts on an Interpreter that does not have interrupts.
2. Pick a target machine that is well defined and documented. Computers are designed to perform a specific set of functions; the results of unorthodox use are not always known, but must be considered by the emulator. The availability of a target machine for testing to determine such results is mandatory.

3. Ensure that the host Interpreter is well documented and has a reasonable set of system utilities; such as, an editor, debugger, simulator, file manager, operating system and compiler.
4. Ensure the host Interpreter will receive hardware support if problems arise.
5. Ensure publications are available covering utilities, hardware, languages and target/host machine capabilities and operation.
6. Be prepared to work independently and have your questions answered through your own experimentation.

In addition to these recommendations, the authors would like to propose several thesis topics applicable to the D-Machine.

1. Several projects could be undertaken as a direct follow on to this thesis:
 - a. An Operating System, File Manager, and Assembler could be written in AN/UYK-7 machine language utilizing the existing Emulator.
 - b. The present Emulation could be enhanced to include Floating Point and any unimplemented instructions, including incorporation of the IOC functions and allowing for synchronous I/O.
 - c. A timing survey could be conducted comparing the existing Emulation with AN/UYK-7 benchmarks.
2. Several thesis projects are possible which entail enhancing the capabilities of the existing D-Machine Installation. These include writing the interface to the PDP-11/45, and a resident Text Editor.

The stand alone environment of the D-Machine lends itself to experimentation with the design of operating systems and file managers.

In summary, the authors would like to state that they found the D-Machine an outstanding learning device in spite of its many hardware problems. The authors found the ability to emulate existing computers exciting, and found the realization that they could build a working model of any computer they could design, exhilarating.

APPENDIX A. USER'S MANUAL

A. D-MACHINE

When the D-Machine was installed at the Naval Postgraduate School, it was not accompanied by any form of documentation for its operation, preventive maintenance, diagnostics or utility programs. For the most part this information has been derived through experimentation and frequent calls to Burrough's ADO. Some of the more pertinent information is included in this User's Manual to enable the user to load and run a program such as the AN/UYK-7 Emulation. Unless specified otherwise all addresses given in this discussion are in hexadecimal.

1. System Initializing

The machine is secured every night and must therefore, be reinitialized when powered up each morning.

- a. Ensure circuit breakers 2, 7 and 10 are on.
- b. Push the "ON" button on the disc and all three Interpreters.
- c. With desired discs in the drives, push the two "RUN" buttons on the disk unit.
- d. Turn on the card reader and printer.
- e. Place the IOP in normal vice single step mode via the switch inside the cabinet on the right.

- f. Push the "LOAD" button on the IOP; then push "CLEAR".
- g. Place the cards marked IOP-Loader into the card reader. Cards should be read and the IOP should stop at an MPAD of 00FA. If not, repeat steps e through g.
- h. Push the "LOAD" button on IOP to return the IOP to normal.
- i. Perform steps e to h for each of the other two Interpreters using the cards marked STK-loader. They should halt at a MPAD of 004A.
- k. Push "CLEAR" on each Interpreter. They should bootstrap themselves through the IOP and halt at either 0542 or 051A. (An Interpreter must be at 0542 to run a program and only one Interpreter can be at 0542 at a time.) Clear the IOP to force an Interpreter to switch from 051A to 0542.

The D-Machine now thinks it is a Burrough's B6700 single-stack machine. Any utility can be run using the proper control cards as documented in the computer lab. The more common utilities are Sunrise (updates the day, date and time; should be run first thing every morning), Dir-List (prints out the directory; system or user), Compile (compiles ALGOL programs) and TRANSLANG (assembles microprograms). By use of the proper control cards, the user can also obtain a source listing of his program as it is being compiled or assembled. Actually the default is a printout every time and the user must insert a "\$-list clist" control card to eliminate the listing.

To make the computer act as some machine other than the B6700, use the control card "?SMLOAD filename". The "?" must be in column one and the rest of the card is free-format. This loads the microprogram "filename" (which must be an assembled TRANSLANG program) into micro-memory overlaying the stack machine and then transfers control to that program starting at address 0000. Thus to load the AN/UYK-7, execute "?SMLOAD UYK7-LOADER" on one Interpreter and "?SMLOAD ANUYK7-EMULATOR" on the other. Refer to the appropriate sections of this chapter for further instructions on the execution of these programs.

2. Diagnostics

The programs used for diagnosing hardware problems are written in TRANSLANG and maintained as object modules on cards. The appropriate program is loaded in the same fashion as the bootstrap loader and terminates at a significant address. When "cleared", it should again terminate at an address which indicates success or failure. The operator must determine which from the program listing, as no messages are printed. There are no diagnostics written for the disk, printer or card reader. At the present time a CRT terminal is hooked up to the IOP; however, there is no software support for it. An interface is being written into the operating system and eventually all commands to and from the operator will be via the CRT. The card reader and line printer will then be strictly data I/O ports.

3. Debugging

While executing any TRANSLANG program, the user can monitor the program by use of the nixie light display panel and the function switch assigned to each processor. The lights indicate hex numbers. By selecting the appropriate function the user can observe the current nanoinstruction being executed; the address of the current microinstruction (MPAD); the memory address last written to or read from (BMAR); and the MIR register (MIR and EXT). The MIR function displays the lower 16 bits of the MIR register while the EXT function displays the upper 16 bits. These functions are presently the only means of debugging. For example, if the user were unsure of the information being read from S-memory, he could insert two additional instructions in the code: an instruction to place the data into the MIR register and a "WAIT" instruction. The CPU halts at the "WAIT" instruction and the user can then examine the information in MIR to ascertain its validity. The user may check the MPAD to determine if the address read was actually the address intended. To continue the program the user must press the force-step button inside the side panel. If the user wished to step through a series of instructions following the "WAIT", he could go to single-step, and while holding the force-step button, press the single-step button to override the "WAIT". After passing the "WAIT", single-step to execute one instruction at a time. In this manner the user can debug several instructions one at a time.

B. AN/UYK-7

This section of the User's Manual discusses how the user can reconfigure the D-Machine into an AN/UYK-7.

First, ensure that the disk packs which are mounted are the AN/UYK-7 System Packs and that both interpreters are loaded with an ALGOL Stack Machine.

Second, insert an "?SMLOAD UYK7-LOADER" card in the card reader. This will cause the Loader's microcode to overlay the stack machine's microcode and stop at address "0000".

Third, insert an "?SMLOAD UYK7-EMULATOR" card in the reader. This will cause the Emulator's microcode to overlay the alternate stack machine and stop at address "00A0". The AN/UYK-7 is now ready to accept and execute programs.

Fourth, place the AN/UYK-7 source programs in the reader and force step the Loader and the Emulator, respectively. The Loader will read one card at a time, decode it and place the 32-bit resulting instruction in memory for subsequent execution by the Emulator.

The last instruction of all user programs should be a "HALT", which will cause the Emulator to halt and the Loader to be reinitialized for the next job. Force stepping the Emulator after the halt will cause the next job to be read and executed. Use of this convention permits batch processing of programs by the AN/UYK-7. The program deck organization is discussed in the next section. Individual programs are separated by "N" cards.

1. Loader

a. Macros

This section describes how a program must be keypunched for input to the Loader. All Macro control characters and formats are listed in Figure A-1. Any character typed in column one, which is not listed, will cause an "Illegal Instruction" message and the card will be ignored. It is noteworthy that all functions are optional with the exception of the "N", which must terminate the program deck. All addresses are in octal and considered absolute as far as the user is concerned; however, they are offset by 1024 by the Loader. Macros and instructions may be interspersed as desired.

COL. 1	COL. 4-8	FUNCTION
"A"	Register 0-7	Cols. 9-19 contain the octal value to be inserted in the listed A-Reg.
"I"	Register 1-7	Cols. 9-19 contain the octal value to be inserted in the listed B-Reg.
"D"	Octal Address	Cols. 9-16 contain the decimal value to be inserted at the address listed or in-line if the address=0000.
"R"	Octal Address	Cols. 9-19 contain the decimal number of words to be saved at the address listed or in-line if the address=0000.
"W"	Octal Address	Cols. 9-80 contain the character string to be inserted at the address specified. The string terminates before col. 80 if a single quote (') is encountered.
"S"	Switch Value	Cols. 6-8 contain an octal number whose bit pattern selects which of eight AN/UYK-7 switches the user desires set.
"L"	Octal Address	Causes Base S-Registers to be set at 8K pages starting at 1024, and the program to be loaded at Address.
"O"	Octal Address	Causes change in the program counter in order that subsequent instructions may be loaded at Address.
"N"	Octal Address	Terminates loading of program and initializes PAR to Address for the Emulator.

LOADER MACRO DEFINITIONS

FIGURE A-1

b. Instruction Preparation

For inputting instructions to the Loader three basic formats are used which correspond roughly to the five formats used by the AN/UYK-7. The Loader formats are presented in Figure A-2 under their respective AN/UYK-7 Format Headings. All fields require a right justified octal representation. The "i" field should always be either a one or a zero since it represents a single bit. The combined "F3,K" field of Format III instructions requires that K always be zero; therefore, valid inputs are (0,2,4,6) which correspond to an F3 of (0,1,2,3). Columns 1-3 must always be left blank. Columns 15-80 may be used for programmer's comments. Each instruction is decoded into one 32-bit word and assigned to the next sequential address in memory. However, if the instruction is a half-word instruction then it will be stored in the lower half of the previous word if that word also contained a half-word instruction, else it will be stored in the upper half of the next sequential address. An instruction's sequential address assignment can only be changed via the "O" or "L" macros, which must precede the instruction. A sample program is presented in Appendix D.

FORMAT I

COL	COL	COL	COL	COL	COL	COL
1-3	4-5	6	7	8	9	10-14
BLANK	OPCODE	A-REG	K	B	I	Y-OPERAND

FORMAT II

COL	COL	COL	COL	COL	COL	COL
1-3	4-5	6	7	8	9	10-14
BLANK	OPCODE	A-REG	F2	B	I	Y-OPERAND

FORMAT III

COL	COL	COL	COL	COL	COL	COL
1-3	4-5	6	7	8	9	10-14
BLANK	OPCODE	A-REG	F3,K	B	I	Y-OPERAND

FORMAT IV-A

COL	COL	COL	COL	COL	COL
1-3	4-5	6	7	8	9
BLANK	OPCODE	A-REG	F4	B	i

FORMAT IV-B

COL	COL	COL	COL
1-3	4-5	6	7-9
BLANK	OPCODE	A-REG	SHIFT DESIGNATOR

INSTRUCTION FORMATTING

FIGURE A-2

c. TRANSLANG

Several modifications have been made to the D-Machine and the microprogramming language, TRANSLANG, since the publication of reference 9 in 1970. Unfortunately, an addendum to reference 9 has not been published and these powerful modifications remain undocumented. Because the authors took advantage of these capabilities in writing this Emulation the changes are documented here to provide the user a ready reference. They include: additional logical operators, program address modifiers, and an additional Y-select input register (BMAR).

(1) Logic Operators. The additional logic operators are listed in Table A-1 along with the code generated by the Microtranslator when they are encountered. In the Table, A1 and B are assumed as the X/Y input operands respectively. In addition, listed under the columns labelled TRUE/FALSE, are the tests generated by the Microtranslator when a TRUE/FALSE conditional test is encountered subsequent to the logical operation.

OP	MEANING	CODE GENERATED	TRUE TEST	FALSE TEST
LSS	Less Than	A1-B	NOT AOV	AOV
LEQ	Less Than or Equal	A1-B-1	NOT AOV	AOV
EQL	Equal	A1 EQV B	ABT	NOT ABT
NEQ	Not Equal	A1 EQV B	NOT ABT	ABT
GEO	Greater Than or Equal To	A1-B	AOV	NOT AOV
GTR	Greater Than	A1-B-1	AOV	NOT AOV

LOGICAL OPERATORS

TABLE A-1

The programmer is cautioned that when the Microtranslator encounters the keywords TRUE/FALSE it backtracks to the last logical operator to determine which test to generate. Thus a TRUE/FALSE conditional test which is arrived at through branching may not have generated the exact code the programmer anticipated. These operators were intended to be used in a sequential fashion as follows:

```
A1 GTR B
If TRUE Then (operation)
```

The Microtranslator generates:

```
A1-B-1
If AOV Then (operation)
```

The following illustrates circumstances in which the Microtranslator does not generate the code expected by the programmer:

```
A1 LSS B
If LC1 Then A1 GTR B;Step Else Skip
If TRUE Then (operation)
```

Generates the code:

```
A1-B  
If LC1 Then A1-B-1;Step Else Skip  
If AOV Then (operation)
```

In this situation "If AOV" is always generated when the TRUE is encountered; although, obviously if LC1 was not set then the programmer desired to test for "Less Than".

(2) Program Address Modifiers. Two powerful new instructions were added to the D-Machine which allow direct transfer of program control. These are the two Type II instructions: "Label-1=MPCR" and "Label-1=CPCR". The first causes a direct change in the program sequence by loading MPCR with the new Label. The second can be classified as a return jump since it causes a transfer of AMPCR to MPCR, and MPCR+1 to AMPCR; thereby setting up a program jump to a subroutine, and saving the return address. This code is identical to:

```
Label-1=AMPCR  
CALL
```

The only difference between them is that the CPCR requires only one instruction for execution, while the CALL requires two instructions.

(3) BMAR. The BMAR register is formed by the concatenation of BR1 or BR2 (16 bits) and MAR (8 bits). It can be used as a Y-Input of 24 bits to the Adder. The actual BR register selected is the one most recently referenced.

in an external operation. The user is cautioned in the use of BMAR because of its odd size of 24 bits. The unwary programmer could unintentionally allow extraneous bits in the most significant byte when BMAR is used for temporary storage of 16-bit addresses. That is, the assignment "A1=MAR" is considered to effect a transfer of 16 bits, while in fact 24 bits are transferred. A subsequent statement of "BMAR=A1" could permit extraneous bits to be introduced in the third least significant byte, if the programmer had made the assumption that only 16 bits were involved and automatic masking had taken place. The programmer can force selection of BR1 or BR2 by issuing an ASR or ASE, respectively, prior to a BMAR reference. These are considered external function NOOPS in the Naval Postgraduate School Configuration; however, they may not appear concurrently with a BEX statement.

The remainder of the TRANSLANG statements are reasonably straightforward once the programmer understands the instruction timing idiosyncracies. Reference 9 provides excellent guidance for the novice microprogrammer.

APPENDIX B. EMULATOR PROGRAM LISTING

This appendix provides a copy of the Microtranslator output listing of the Emulator. A copy of the source program is maintained on cards and also on the Burrough's D-Machine disk. The object module produced by the Microtranslator is maintained on disk. Each line of the program is divided into four sections. The leftmost grouping consists of the hexadecimal address to which the microinstruction was assigned by the Microtranslator during assembly. This is followed by the 56-bit microinstruction which was generated. The middle group consists of the programmers' source coding which was input to the Microtranslator. The rightmost group consists of the sequence numbers which were assigned to each input card as it was inserted into the source file on the disk by the Interpreter's resident line-editting program (CARD-LIST).

```

SHERGE ANUYK7-EMULATOR
PROGRAM ANUYK7-OBJECT
ABASE#0
PAR#29
BBASE#8
SBASE#16
S6#22
ZERO#0. ONE#1
CARDBUF#212
PRINTBUF#238
RINST#24
CINST#25
IAR#26
YADDR#27
IADDR#28
SWTCH#88
START-1 = MPCR
ILLEGAL-1=AMPCR
OPR01-1=AMPCR
OPR02-1=AMPCR
OPR03-1=AMPCR
ILLEGAL-1=AMPCR
OPR05-1=AMPCR
OPR06-1=AMPCR
OPR07-1=AMPCR
OPR10-1=AMPCR
OPR11-1=AMPCR
OPR12-1=AMPCR
OPR13-1=AMPCR
OPR14-1=AMPCR
OPR15-1=AMPCR
OPR16-1=AMPCR
OPR17-1=AMPCR
OPR20-1=AMPCR
OPR21-1=AMPCR
OPR22-1=AMPCR
OPR23-1=AMPCR
OPR24-1=AMPCR
OPR25-1=AMPCR
OPR26-1=AMPCR
OPR27-1=AMPCR
ILLEGAL-1=AMPCR
ILLEGAL-1=AMPCR
OPR32-1=AMPCR
OPR33-1=AMPCR
OPR34-1=AMPCR
OPR35-1=AMPCR
OPR36-1=AMPCR
OPR37-1=AMPCR
OPR40-1=AMPCR
OPR41-1=AMPCR
OPR42-1=AMPCR
OPR43-1=AMPCR
OPR44-1=AMPCR
OPR45-1=AMPCR
OPR46-1=AMPCR
OPR47-1=AMPCR
OPR50-1=AMPCR

```

```

00010000 D
0020000 D
0030000 D
0040000 D
0050000 D
0060000 C
0070000 D
0080000 D
0090000 D
0100000 D
0110000 D
0120000 D
0130000 C
0140000 D
0150000 D
0160000 D
0170000 D
0180000 C
0190000 D
0200000 D
0210000 D
0220000 D
0230000 D
0240000 D
0250000 D
0260000 D
0270000 D
0280000 D
0290000 D
0300000 D
0310000 D
0320000 D
0330000 D
0340000 D
0350000 D
0360000 D
0370000 C
0380000 D
0390000 D
0400000 D
0410000 D
0420000 D
0430000 D
0440000 D
0450000 D
0460000 D
0470000 C
0480000 C
0490000 D
0500000 D
0510000 D
0520000 D
0530000 D
0540000 D
0550000 D
0560000 D
0570000 C

```

```

ADDRESS OF A-REG(O)
TEMP. STORAGE LOCATION OF PAR
ADDRESS OF B-REG(O)
ADDRESS OF S-REG(O)
ADDRESS OF BASE REG 6
ADDRESS OF PERMANENT CARD BUFFER
ADDRESS OF PERMANENT PRINT BUFFER
TEMP. LOCATION OF REPEAT INSTR.
TEMP. LOCATION OF INSTR. REPEATED
TEMP. LOCATION OF CURRENT IAR
SCONTAINS PRECALCULATED Y-ADDRESS
ADDRESS OF CURRENT IAR
ADDRESS OF SWITCH VALUES READ-IN
SINVALID OPR 00
SINCLUSIVE OR
SCOUNT ONES
REPLACE INCLUSIVE OR
SINVALID OPR 04
DOUBLE LOAD A
XFP ADD
SENDER EXEC STATE
LOAD A AND INDEX
LOAD A AND INDEX
LOAD DIFFERENCE
SUBTRACT A
LOAD A
LOAD SUM
LOAD NEGATIVE
LOAD MAGNITUDE
LOAD B
LOAD B
SUBTRACT B
STORE B
STORE A
STORE A AND INDEX B
STORE NEGATIVE
STORE MAGNITUDE
SINVALID OPR 3C
SINVALID OPR 3I
XCLEAR BIT
XSET BIT
XREALCE ACC
XREPLACE INCREMENT
XREPLACE SUBTRACT
XREPLACE DECREMENT
MULTIPLY A
DIVIDE A
COMPARE BIT TO ZERO
COMPARE INDEX INCREMENT
COMPARE LIMITS
COMPARE MASKED
COMPARE GATED
JUMP ON EVEN PARITY

```

00580000 D
 00590000 D
 00600000 C
 00610000 D
 00620000 D
 00630000 D
 00640000 D
 00650000 D
 00660000 C
 00670000 D
 00680000 D
 00690000 C
 00700000 D
 00710000 D
 00720000 D
 00730000 D
 00740000 D
 00750000 D
 00760000 D
 00770000 D
 00780000 D
 00790000 D
 00800000 D
 00810000 D
 00820000 D
 00830000 D
 00840000 D
 00850000 D
 00860000 D
 00870000 D
 00880000 C
 00890000 D
 00900000 D
 00910000 D
 00920000 D
 00930000 D
 00940000 D
 00950000 D
 00960000 D
 00970000 D
 00980000 D
 00990000 D
 01000000 D
 01010000 D
 01020000 D
 01030000 D
 01040000 D
 01050000 D
 01060000 D
 01070000 D
 01080000 D
 01090000 D
 01100000 C
 01110000 D
 01120000 D
 01130000 C
 01140000 D
 01150000 D
 01160000 C
 01170000 D

XJUMP A POSITIVE
 XLOAD B AND JUMP
 XJUMP ON NO OVERFLOW
 XLOAD CHR TASK
 XLOAD CHR INCREMENT
 XSTORE CHR TASK
 XSTORE CHR INTERRUPT
 XSTORE CHR IN A
 XLOAD CHR FROM A
 XSHIFT LEFT CIRCULARLY
 XSHIFT LEFT CIRCULARLY DOUBLE
 XSHIFT RIGHT FILL ZERO
 XSHIFT RIGHT DOUBLE FILL ZEROS
 XSHIFT RIGHT FILL SIGN
 XSHIFT RIGHT DOUBLE FILL SIGN
 XSCALE FACTOR
 XLOGICAL SUMM
 XPRINT MESSAGE & RETURN TO HALFFETCH
 XPRINT MESSAGE & RETURN TO HALFFETCH
 XMULTIPLY REGISTER
 XPRINT MESSAGE & RETURN TO HALFFETCH
 XPRINT MESSAGE & RETURN TO HALFFETCH
 XSTORE IOC MONITOR CLOCK IN A

OPR51-1=AMPCR
 OPR52-1=AMPCR
 OPR53-1=AMPCR
 OPR54-1=AMPCR
 OPR55-1=AMPCR
 OPR56-1=AMPCR
 OPR57-1=AMPCR
 OPR60-1=AMPCR
 OPR61-1=AMPCR
 OPR62-1=AMPCR
 OPR63-1=AMPCR
 OPR64-1=AMPCR
 OPR65-1=AMPCR
 OPR66-1=AMPCR
 OPR67-1=AMPCR
 OPR70-1=AMPCR
 OPR71-1=AMPCR
 ILLEGAL9-1=AMPCR
 ILLEGAL9-1=AMPCR
 OPR74-1=AMPCR
 ILLEGAL9-1=AMPCR
 ILLEGAL9-1=AMPCR
 OPR77-1=AMPCR
 OPRO1XX:
 OPRO1X0-1=AMPCR
 OPRO1X1-1=AMPCR
 OPRO1X2-1=AMPCR
 OPRO1X3-1=AMPCR
 OPRO1X4-1=AMPCR
 OPRO1X5-1=AMPCR
 OPRO1X6-1=AMPCR
 OPRO1X7-1=AMPCR
 OPRO2XX:
 OPRO2X0-1=AMPCR
 ILLEGAL-1=AMPCR
 OPRO2X2-1=AMPCR
 OPRO2X3-1=AMPCR
 OPRO2X4-1=AMPCR
 OPRO2X5-1=AMPCR
 OPRO2X6-1=AMPCR
 OPRO2X7-1=AMPCR
 OPRO3XX: RUSES OPRO1XX ROUTINES DUE TO DUPLICATION OF CODE
 OPRO5XX:
 OPRO5X0-1=AMPCR
 OPRO5X1-1=AMPCR
 OPRO5X2-1=AMPCR
 OPRO5X3-1=AMPCR
 OPRO5X4-1=AMPCR
 ILLEGAL-1=AMPCR
 ILLEGAL-1=AMPCR
 OPRO6XX:
 OPRO6X0-1=AMPCR
 OPRO6X1-1=AMPCR
 OPRO6X2-1=AMPCR
 OPRO6X3-1=AMPCR
 OPRO6X4-1=AMPCR
 OPRO6X5-1=AMPCR
 OPRO6X6-1=AMPCR
 OPRO6X7-1=AMPCR

002A 024C 0000 0000 0000 0000
 002B 0280 0000 0000 0000 0000
 002C 02C0 0000 0000 0000 0000
 002D 0300 0000 0000 0000 0000
 002E 02E0 0000 0000 0000 0000
 002F 02F0 0000 0000 0000 0000
 0030 0300 0000 0000 0000 0000
 0031 0310 0000 0000 0000 0000
 0032 0320 0000 0000 0000 0000
 0033 033C 0000 0000 0000 0000
 0034 0340 0000 0000 0000 0000
 0035 0350 0000 0000 0000 0000
 0036 036C 0000 0000 0000 0000
 0037 0370 0000 0000 0000 0000
 0038 038C 0000 0000 0000 0000
 0039 0390 0000 0000 0000 0000
 003A 03A0 0000 0000 0000 0000
 003B 03B0 0000 0000 0000 0000
 003C 03C0 0000 0000 0000 0000
 003D 03D0 0000 0000 0000 0000
 003E 03E0 0000 0000 0000 0000
 003F 03F0 0000 0000 0000 0000
 0040 0400 0000 0000 0000 0000
 0041 0410 0000 0000 0000 0000
 0042 042C 0000 0000 0000 0000
 0043 0430 0000 0000 0000 0000
 0044 044C 0000 0000 0000 0000
 0045 0450 0000 0000 0000 0000
 0046 0460 0000 0000 0000 0000
 0047 0470 0000 0000 0000 0000
 0048 0480 0000 0000 0000 0000
 0049 0490 0000 0000 0000 0000
 004A 04AC 0000 0000 0000 0000
 004B 04B0 0000 0000 0000 0000
 004C 04C0 0000 0000 0000 0000
 004D 04D0 0000 0000 0000 0000
 004E 04E0 0000 0000 0000 0000
 004F 04FC 0000 0000 0000 0000
 0050 0500 0000 0000 0000 0000
 0051 0510 0000 0000 0000 0000
 0052 0520 0000 0000 0000 0000
 0053 0530 0000 0000 0000 0000
 0054 0540 0000 0000 0000 0000
 0055 055C 0000 0000 0000 0000
 0056 0560 0000 0000 0000 0000
 0057 0570 0000 0000 0000 0000
 0058 0580 0000 0000 0000 0000
 0059 059C 0000 0000 0000 0000
 005A 05A0 0000 0000 0000 0000
 005B 05B0 0000 0000 0000 0000
 005C 05CC 0000 0000 0000 0000
 005D 05D0 0000 0000 0000 0000
 005E 05E0 0000 0000 0000 0000
 005F 05FC 0000 0000 0000 0000
 0060 0600 0000 0000 0000 0000

0061	0610	0003	0030	00C0	0PR07X0-1=AMPCR	01180000	D
0062	0620	0000	0030	00C0	0PR07X1-1=AMPCR	01190000	D
0063	0630	0000	0030	00C0	0PR07X2-1=AMPCR	01200000	D
0064	0640	0000	0030	00C0	0PR07X3-1=AMPCR	01210000	D
0065	0650	0000	0030	00C0	0PR07X4-1=AMPCR	01220000	D
0066	0660	0000	0030	00C0	0PR07X5-1=AMPCR	01230000	D
0067	0670	0000	0030	00C0	0PR07X6-1=AMPCR	01240000	D
0068	0680	0000	0030	00C0	ILLEGAL-1=AMPCR	01250000	D
0069	0690	0000	0030	00C0	0PR50X0-1=AMPCR	01260000	D
006A	06A0	0000	0030	00C0	0PR50X1-1=AMPCR	01270000	D
006B	06B0	0000	0030	00C0	0PR50X2-1=AMPCR	01280000	D
006C	06C0	0000	0030	00C0	0PR50X3-1=AMPCR	01290000	D
006D	06D0	0000	0030	00C0	ILLEGAL-1=AMPCR	01300000	D
006E	06E0	0000	0030	00C0	ILLEGAL-1=AMPCR	01310000	D
006F	06F0	0000	0030	00C0	ILLEGAL-1=AMPCR	01320000	D
0070	0700	0000	0030	00C0	ILLEGAL-1=AMPCR	01330000	D
0071	0710	0000	0030	00C0	0PR51X0-1=AMPCR	01340000	D
0072	0720	0000	0030	00C0	0PR51X1-1=AMPCR	01350000	D
0073	0730	0000	0030	00C0	0PR51X2-1=AMPCR	01360000	D
0074	0740	0000	0030	00C0	0PR51X3-1=AMPCR	01370000	D
0075	0750	0000	0030	00C0	ILLEGAL-1=AMPCR	01380000	D
0076	0760	0000	0030	00C0	ILLEGAL-1=AMPCR	01390000	D
0077	0770	0000	0030	00C0	ILLEGAL-1=AMPCR	01400000	D
0078	0780	0000	0030	00C0	ILLEGAL-1=AMPCR	01410000	D
0079	0790	0000	0030	00C0	0PR52X0-1=AMPCR	01420000	D
007A	07A0	0000	0030	00C0	0PR52X1-1=AMPCR	01430000	D
007B	07B0	0000	0030	00C0	0PR52X2-1=AMPCR	01440000	D
007C	07C0	0000	0030	00C0	0PR52X3-1=AMPCR	01450000	C
007D	07D0	0000	0030	00C0	ILLEGAL-1=AMPCR	01460000	D
007E	07E0	0000	0030	00C0	ILLEGAL-1=AMPCR	01470000	D
007F	07F0	0000	0030	00C0	ILLEGAL-1=AMPCR	01480000	D
0080	0800	0000	0030	00C0	ILLEGAL-1=AMPCR	01490000	D
0081	0810	0000	0030	00C0	0PR53X0-1=AMPCR	01500000	D
0082	0820	0000	0030	00C0	0PR53X1-1=AMPCR	01510000	D
0083	0830	0000	0030	00C0	0PR53X2-1=AMPCR	01520000	D
0084	0840	0000	0030	00C0	0PR53X3-1=AMPCR	01530000	D
0085	0850	0000	0030	00C0	ILLEGAL-1=AMPCR	01540000	D
0086	0860	0000	0030	00C0	ILLEGAL-1=AMPCR	01550000	D
0087	0870	0000	0030	00C0	ILLEGAL-1=AMPCR	01560000	D
0088	0880	0000	0030	00C0	0PR70X0-1=AMPCR	01570000	D
0089	0890	0000	0030	00C0	0PR70X1-1=AMPCR	01580000	D
008A	08A0	0000	0030	00C0	0PR70X2-1=AMPCR	01590000	D
008B	08B0	0000	0030	00C0	0PR70X3-1=AMPCR	01600000	D
008C	08C0	0000	0030	0040	ILLEGAL-1=AMPCR	01610000	D
008D	08D0	0000	0030	0040	ILLEGAL-1=AMPCR	01620000	D
008E	08E0	0000	0030	0040	ILLEGAL-1=AMPCR	01630000	D
008F	08F0	0000	0030	0040	ILLEGAL-1=AMPCR	01640000	D
0090	0900	0000	0030	00C0	0PR71X0-1=AMPCR	01650000	D
0091	0910	0000	0030	00C0	0PR71X1-1=AMPCR	01660000	D
0092	0920	0000	0030	00C0	0PR71X2-1=AMPCR	01670000	D
0093	0930	0000	0030	00C0	0PR71X3-1=AMPCR	01680000	D
0094	0940	0000	0030	00C0	0PR71X4-1=AMPCR	01690000	D
0095	0950	0000	0030	00C0	0PR71X5-1=AMPCR	01700000	D

SPRINT MESSAGE & RETURN TO HALFFETCH
 SPRINT MESSAGE & RETURN TO HALFFETCH
 SPRINT MESSAGE & RETURN TO HALFFETCH

```

0096 096C 0000 0000 00C0
0097 0970 0000 0000 00C0
0098 0980 0000 0000 00C0
0099 0990 0000 0000 00C0
009A 09A0 0000 0000 00C0
009B 09B0 0000 0000 00C0
009C 09C0 0000 0000 00C0
009D 09D0 0000 0000 00C0
009E 09E0 0000 0000 00C0
009F 09F0 0000 0000 00C0

00A0 0000 0000 0000 00C0
00A1 0000 0000 0000 00C0
00A2 0000 0000 0000 00C0
00A3 0000 0000 0000 00C0
00A4 0000 0000 0000 00C0
00A5 0000 0000 0000 00C0

00A6 0000 0000 0000 00C0
00A7 0000 0000 0000 00C0
00A8 0000 0000 0000 00C0
00A9 0000 0000 0000 00C0
00AA 0000 0000 0000 00C0

00AB 0000 0000 0000 00C0
00AC 0000 0000 0000 00C0
00AD 0000 0000 0000 00C0
00AE 0000 0000 0000 00C0
00AF 0000 0000 0000 00C0
00B0 0000 0000 0000 00C0
00B1 0000 0000 0000 00C0
00B2 0000 0000 0000 00C0
00B3 0000 0000 0000 00C0

00B4 0000 0000 0000 00C0
00B5 0000 0000 0000 00C0
00B6 0000 0000 0000 00C0
00B7 0000 0000 0000 00C0
00B8 0000 0000 0000 00C0
00B9 0000 0000 0000 00C0
00BA 0000 0000 0000 00C0
00BB 0000 0000 0000 00C0

00BC 0000 0000 0000 00C0
00BD 0000 0000 0000 00C0
00BE 0000 0000 0000 00C0
00BF 0000 0000 0000 00C0
00C0 0000 0000 0000 00C0
00C1 0000 0000 0000 00C0
00C2 0000 0000 0000 00C0

01780000 D
01790000 D
01800000 D
01810000 D
01820000 D
01830000 D
01840000 D
01850000 D
01860000 D
01870000 D
01880000 D
01890000 D
01900000 D
01910000 D
01920000 D
01930000 D
01940000 D
01950000 D
01960000 D
01970000 D
01980000 D
01990000 D
02000000 D
02010000 D
02020000 D
02030000 D
02040000 D
02050000 D
02060000 D
02070000 D
02080000 D
02090000 D
02100000 D
02110000 D
02120000 D
02130000 D
02140000 D
02150000 D
02160000 D
02170000 D
02180000 D
02190000 D
02200000 D
02210000 D
02220000 D
02230000 D
02240000 D
02250000 D
02260000 D
02270000 D
02280000 D
02290000 D
02300000 D
02310000 D
02320000 D
02330000 D
02340000 D
02350000 D
02360000 D
02370000 D

OPR77XX:
OPR74X6-1=AMPCR
OPR74X7-1=AMPCR
OPR77X0-1=AMPCR
OPR77X1-1=AMPCR
ILLEGAL4-1=MPCR
ILLEGAL4-1=MPCR
OPR77X4-1=AMPCR
OPR77X5-1=AMPCR
OPR77X6-1=AMPCR
ILLEGAL4-1=MPCR

$ $ START BY TRYING TO SET GC1 WHICH MEANS THE
$ $ LOADER HAS LOADED THE OBJECT CODE AND
$ $ PRESET THE REGISTERS
$ $ IN GENERAL A2 CONTAINS ASR/PAR, A1 CONTAINS CURRENT INSTRUCTION
START: 0 = BR1; WAIT
SET GC1; WHEN GC1 THEN STEP
GETPAR-1 = CPCR
1 L-BYRESET GC2
COMP 10=8AR
A2=8=A2

IFETCH:
PUTPAR-1 = CPCR
IF IRO THEN STEP ELSE SKIP
IOUNMPREG-1 = CPCR
IF GC2 THEN STEP ELSE SKIP
GC2CHECK-1 = CPCR

IFETCH1:
A2 = MAR2
MR2; IF ROC
WHEN ROC THEN A2 + 1 = A2,8EX $ INC PAR
IFETCHNOTE: ENTRY FROM EXECUTE REMOTE OPRO2X2
B = A1
B R = 0
16 = SAR
B
IF LST THEN STEP ELSE SKIP
INDIRECT-1 = CPCR $ INDIRECT-1

IFETCH2:
A1 R = 0
7 = LIT; 17 = SAR
LIT AND B = B
A1 R = AMPCR
BBASE = LIT; 26 = SAR
STEP
LIT + B = MAR,A3; EXEC; IF LC1 $ B(8) ADDR ->MAR,A3
JUMP; IF LC2

$ $
$ $ ***** SUBR FOR MEMORY FETCHES *****
HALFFETCH: FETCH THE NEXT HALFWORD INSTRUCTION *****
HW,IF SAI
$ $ SOME INSTRUCTIONS ENTER HERE AT HALFFETCH+1
A1 C=A1
16=8AR
A1 R=A3
26=8AR
A2 C=8,CCSAR
20=8AR

SPRINT MESSAGE & RETURN TO HALFFETCH
SPRINT MESSAGE & RETURN TO HALFFETCH
SPRINT MESSAGE & RETURN TO HALFFETCH
SPRINT MESSAGE & RETURN TO HALFFETCH

```

AD-A035 885

NAVAL POSTGRADUATE SCHOOL MONTEREY CALIF
EMULATION OF THE AN/UYK-7 TACTICAL DATA COMPUTER ON THE BURROUG--ETC(U)
DEC 76 J M HAGGERTY, J M HARTLING

F/G 9/2

UNCLASSIFIED

NL

2 of 2
AD A035885



END

DATE
FILMED
3-77

00C3	4897	0C40	00C0	00F0
00C4	5000	0C01	A000	00F0
00C5	0A30	0000	0000	00C0
00C6	3899	0CC1	A000	00F0
00C7	0019	0000	0000	00F0
00C8	0A5C	0000	0000	00C0
00C9	0019	0000	0000	00F0
00CA	0A60	0000	0000	00C0
00CB	4009	E000	0C00	00F0
00CC	4009	0000	0000	00F0
00CD	2824	E010	0000	00F0
00CE	6029	0000	0000	00F0
00CF	00C0	0000	0C00	00C0
00D0	4897	A000	9000	00F0
00D1	007C	0000	0000	00A0
00D2	4897	E156	1025	00F0
00D3	1019	0000	0000	00F0
00D4	0A70	00C0	0C00	00A0
00D5	AC00	00C0	0C00	00F0
00D6	4897	E002	0000	00F0
00D7	6C19	0C40	0000	00F0
00D8	0A8C	0000	0C00	00A0
00D9	4897	0018	8000	00F0
00DA	0000	0000	0000	0020
00DB	4897	A0C1	1000	00F0
00DC	4897	E0F0	0000	00F0
00DD	6C19	E053	9000	00F0
00DE	4897	E000	9000	00F0
00DF	4820	E040	1000	00F0
00E0	4897	A009	9000	00F0
00E1	9070	0000	0000	0090
00E2	4897	E156	1000	00F0
00E3	4897	E140	0C00	00F0
00E4	0100	00C0	0000	00E0
00E5	4897	A0C1	1000	00F0
00E6	4897	E0C0	9000	00F0
00E7	4C00	E040	1C00	00F0
00E8	4897	E043	001C	00F0
00E9	4897	0640	0000	24F0
00EA	4897	0002	9000	00F0
00EB	0000	0000	0000	0030
00EC	4897	E040	0000	00F0
00ED	0A50	0000	0000	00CC
00EE	4897	0000	0000	00CC
00EF	4824	0000	0000	00F0
00F0	0A36	00C0	0000	00F0
00F1	4897	0C40	0000	00FC
00F2	4897	0000	0000	00FC
00F3	4820	0000	0000	00FC
00F4	4897	0000	0000	00FC
00F5	0A4C	0000	0000	00C0
00F6	0A00	0000	0000	00C0
00F7	0A00	0000	0000	00C0
00F8	0A00	0000	0000	00C0
00F9	0A00	0000	0000	00C0
00FA	0A00	0000	0000	00C0
00FB	0000	0000	0000	00C0
0230	0C00	D		
0239	0C00	D		
0240	0000	D		
0241	0C00	D		
0242	0C00	D		
0243	0C00	D		
0244	0C00	D		
0245	0C00	D		
0246	0C00	D		
0247	0C00	D		
0248	0C00	D		
0249	0000	D		
0250	0000	D		
0251	0C00	D		
0252	0C00	D		
0253	0000	D		
0254	0C00	D		
0255	0C00	D		
0256	0C00	D		
0257	0C00	D		
0258	0C00	D		
0259	0C00	D		
0260	0C00	D		
0261	0C00	D		
0262	0C00	D		
0263	0C00	D		
0264	0C00	D		
0265	0C00	D		
0266	0C00	D		
0267	0C00	D		
0268	0C00	D		
0269	0000	D		
0270	0C00	D		
0271	0C00	D		
0272	0000	L		
0273	0C00	D		
0274	0C00	D		
0275	0C00	D		
0276	0C00	D		
0277	0C00	D		
0278	0C00	D		
0279	0C00	D		
0280	0C00	D		
0281	0C00	D		
0282	0C00	D		
0283	0C00	D		
0284	0C00	D		
0285	0C00	D		
0286	0C00	D		
0287	0C00	D		
0288	0C00	D		
0289	0C00	D		
0290	0C00	D		
0291	0C00	D		
0292	0C00	D		

```

IF LST THEN BIT0 C=A2/ STEP ELSE SKIP RSET BIT IF CLEARED
YFETCH=1=AMPCR
BIT1 C=A2/IF LC2
IF NOT IRO THEN SKIP
PUTPAR=1=CPCR
IF NOT IRO THEN SKIP
IDUMPREG=1=CPCR
A3=AMPCR
STEP
A3 EOL OEXEC/IF LC1
IF FALSE THEN JUMP
HALFFETCH=AMPCR

SMAR=B(0) ADDRESS/RETURN MAR2=Y-ADDR/MIR-Y(K)
A1 R=A3/IF ROC
7=LIT/20=5AR
A3 AND LIT=CTR/A3/MR1/IF ROC SAVE K IN CTR/READ P(0)
IF NOT GC2 THEN SKIP
YABNORMAL=1=AMPCR
WHEN ROC THEN BEX
YREFETCH: NOT A3
IF ABT THEN B=MIR/SKIP
KNOZRO=1=AMPCR
R11 R=R0
16=5AR
A3 L=A3
A3
IF RST THEN A3 OR B C=A3/0MIR/SKIP EXTEND NEGATIVE SIGN
A3 R = A3/BMI
A3+B=A3/MIR/JUMP
7=LIT/13=5AR
A3 AND LIT=A3
SBASE=LIT
A1 L=A3,CSAR/MR1/IF ROC
A3 R=A3
WHEN ROC THEN A3+B=A3,0EX
A3+B=MAR2

YFETCH1: BRETURN HERE FROM Y-ABNORMAL UNLESS K=0 OR CHAR ADDR.
AMPCR=MIR/ASE
NOT CTR R=A3
24=5AR
A3+AMPCR=AMPCR
KTABLE=1=AMPCR
MR2/IF ROC
EXEC
CALL
B = AMPCR
STEP
JUMP
KTABLE: WAIT
KRI=1=AMPCR. KR2=1=AMPCR. KR3=1=AMPCR. KR4=1=AMPCR
KR5=1=AMPCR. KR6=1=AMPCR. KR7=1=AMPCR

```

0293000 0
 0294000 0
 0295000 0
 0296000 0
 0297000 0
 0298000 0
 0299000 0
 0300000 0
 0301000 0
 0302000 0
 0303000 0
 0304000 0
 0305000 0
 0306000 0
 0307000 0
 0308000 0
 0309000 0
 0310000 0
 0311000 0
 0312000 0
 0313000 0
 0314000 0
 0315000 0
 0316000 0
 0317000 0
 0318000 0
 0319000 0
 0320000 0
 0321000 0
 0322000 0
 0323000 0
 0324000 0
 0325000 0
 0326000 0
 0327000 0
 0328000 0
 0329000 0
 0330000 0
 0331000 0
 0332000 0
 0333000 0
 0334000 0
 0335000 0
 0336000 0
 0337000 0
 0338000 0
 0339000 0
 0340000 0
 0341000 0
 0342000 0
 0343000 0
 0344000 0
 0345000 0
 0346000 0
 0347000 0
 0348000 0
 0349000 0
 0350000 0
 0351000 0
 0352000 0

16 = SAR
 WHEN RDC THEN BEX S READ (Y)
 B L = A3
 A3 R = A3,MIR,BMI S (Y) 0-15 = MIR
 IF NOT THEN B=MIR; STEP ELSE JUMP
 B111 L = B S 118 IN BITS 16-31
 A3 OR B = A3,MIR,BMI; JUMP S SIGN EXTENDED
 16 = SAR
 WHEN RDC THEN BEX S READ (Y)
 B R = A3,MIR,BMI S (Y) 31-16 = A3
 IF NOT THEN B=MIR; STEP ELSE JUMP
 B111 L = B
 A3 OR B = A3,MIR,BMI; JUMP SEXTEND SIGN
 B = A3,MIR,BMI; JUMP S READ (Y)
 255 = LIT
 WHEN RDC THEN BEX S READ (Y)
 LIT AND B = A3,MIR,BMI; JUMP
 255 = LIT; B = SAR
 WHEN RDC THEN BEX S READ (Y)
 B R = B
 LIT AND B = A3,MIR,BMI; JUMP S (Y) 15-8 = MIR
 255 = LIT; 16 = SAR
 WHEN RDC THEN BEX S READ (Y)
 B R = B
 LIT AND B = A3,MIR,BMI; JUMP S (Y) 23-16 = MIR
 255 = LIT; 24 = SAR
 WHEN RDC THEN BEX SREAD (Y)
 B R = B
 LIT AND B = A3,MIR,BMI; JUMP S (Y) 31-24 = MIR
 YABNORMAL: SCALLED FROM Y-FETCH WHEN GC2 SET MAR=B-FIELD;A3,BR2=K-FIELD
 WHEN RDC THEN A3=B,CTR
 A2 R=A3
 21-SAR;7-LIT
 A3 AND LIT R=A3 S A3=SPEC.COMD-BITS
 1-SAR;YADDR=LIT
 IF LST THEN B=A3;BEX;STEP ELSE SKIP
 YREFETCH-1=HPCR
 LMAR
 MR1 IF RDC
 WHEN RDC THEN A3 EOL LIT;BEX STEST=3->CHAR.ADDR;E=Y-ADDR
 3-LIT;24=SAR
 IF FALSE THEN B=MAR;SKIP SNOT CA S0 SETUP Y-ADDRESS
 CHARFETCH-1=HPCR
 YFETCH-1=HPCR
 YSFETCH: IF GC2 THEN STEP ELSE SKIP
 Y2ABNORMAL-1=HPCR
 Y2REPABN: A1 L=A3;CSAR
 COMP 19-SAR;7-LIT
 A3 R=A3;CSAR;MR1;IF RDC S ISOLATED THE Y-FIELD;READ B(B)
 WHEN RDC THEN BEX SB=B(B)
 A3=B=A3
 A1 R=B SY+B(B)=A3
 LIT AND B=B RISOLATE S-FIELD
 LIT+B=MAR
 SBASE=LIT
 MR1 IF RDC

0000 0000 0000 0020
 0001 0000 0000 0000
 0002 0000 0000 0000
 0003 0000 0000 0000
 0004 0000 0000 0000
 0005 0000 0000 0000
 0006 0000 0000 0000
 0007 0000 0000 0000
 0008 0000 0000 0000
 0009 0000 0000 0000
 0010 0000 0000 0000
 0011 0000 0000 0000
 0012 0000 0000 0000
 0013 0000 0000 0000
 0014 0000 0000 0000
 0015 0000 0000 0000
 0016 0000 0000 0000
 0017 0000 0000 0000
 0018 0000 0000 0000
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 0067 0000 0000 0000
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 0069 0000 0000 0000
 0070 0000 0000 0000
 0071 0000 0000 0000
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 0075 0000 0000 0000
 0076 0000 0000 0000
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 0078 0000 0000 0000
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 0080 0000 0000 0000
 0081 0000 0000 0000
 0082 0000 0000 0000
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 0086 0000 0000 0000
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 0099 0000 0000 0000
 0100 0000 0000 0000
 0101 0000 0000 0000
 0102 0000 0000 0000
 0103 0000 0000 0000
 0104 0000 0000 0000
 0105 0000 0000 0000
 0106 0000 0000 0000
 0107 0000 0000 0000
 0108 0000 0000 0000
 0109 0000 0000 0000
 0110 0000 0000 0000
 0111 0000 0000 0000
 0112 0000 0000 0000
 0113 0000 0000 0000
 0114 0000 0000 0000
 0115 0000 0000 0000
 0116 0000 0000 0000
 0117 0000 0000 0000
 0118 0000 0000 0000
 0119 0000 0000 0000
 0120 0000 0000 0000
 0121 0000 0000 0000
 0122 0000 0000 0000
 0123 0000 0000 0000
 0124 0000 0000 0000
 0125 0000 0000 0000
 0126 0000 0000 0000
 0127 0000 0000 0000
 0128 0000 0000 0000
 0129 0000 0000 0000
 0130 0000 0000 0000
 0131 0000 0000 0000
 0132 0000 0000 0000
 0133 0000 0000 0000

```

0134 AC08 0000 0C00 00F0
0135 0009 EC03 0C1C 00F0
0136 AB09 0000 0000 0C00
0137 AC20 0000 0C50 00F0
0138 0009 C000 7050 00F0
0139 9000 0000 0000 0020
013A 0009 E156 7050 00F0
013B 1070 0000 0C50 00F0
013C 5419 0000 0000 00F0
013D 1290 0000 0000 0040
013E 0100 0000 0000 00E0
013F AB09 0000 0050 00F0
0140 AC08 E152 0C0C 00F0
0141 0030 0000 0000 00E0
0142 6408 0C43 0C1C 00F0
0143 1350 0000 0050 0040
0144 0030 0000 0C50 0040

0145 0009 0C40 003C 00F0
0146 AB09 0000 0C50 0C00
0147 AC08 2000 0C3C 00F0
0148 01AC 0000 0050 00E0
0149 AB09 0C40 1000 00F0
014A AC08 0C0C 0C50 00F0
014B 0009 0C40 0000 00F0
014C 025C 0000 0000 00A0
014D 0009 2056 0000 00F0
014E 0009 E0E0 7C50 00F0
014F 0009 0C40 0000 00F0
0150 9000 0000 0C50 0000
0151 0009 2056 0000 00F0
0152 0009 0C0C 0050 40F0
0153 0009 0010 0000 00F0
0154 0009 EC56 1050 00F0
0155 0020 0C43 0C1C 00F0

0156 0009 A000 7000 00F0
0157 1070 0000 0000 00A0
0158 0009 E156 1050 00F0
0159 0009 E100 003C 00F0
015A 000C 0000 0050 00E0
015B AB09 A000 0000 00F0
015C 0070 0000 0000 00A0
015D 0009 2C56 1050 00F0
015E 0000 0000 0000 00C0
015F AC08 E640 0C40 00F0
0160 1419 A001 1000 40F0
0161 0050 0000 0000 0040
0162 7070 0000 0000 0050

0163 0009 E000 7050 00F0
0164 0009 EC00 1050 40F0

WHEN R0C THEN BEX
A3=B-MAR2
Y2FETCH1: SNORMAL RETURN FROM Z2ABNORMAL
MR2;IF R0C
WHEN R0C THEN BEX;JUMP S(Y) NOW IN B REGISTER
Y2ABNORMAL: S CALLED FROM Y2 WHEN 0C2 SET; MAR=B-REG
A2 R=A3
21-SAR
A3 AND LIT R=A3
7=LIT;1-SAR
IF NOT LST THEN LMARISKIP
Y2REPABM-1=MPCR
YADDR=LIT
MR1;IF R0C
WHEN R0C THEN A3 EOL LIT;BEX TEST FOR CAR.ADDR.;Z=B(B)
3=LIT
S CHECK FOR CHARACTER ADDR.
IF FALSE THEN B=MAR2;STEP ELSE SKIP SIF NOT CA THEN SETUP. Y-ADDR03690C00 D
Y2FETCH1-1=MPCR
SNOT AMAR ADDRESSING
CHARFETCH-1=MPCR.
S
CHARFETCH: SFETCH CHARACTER ADDRESSED BY Y=(B)
B=MAR2;MIR
MR2;IF R0C
WHEN R0C THEN LIT=MAR;BEX SB=(Y);MAR=ICW ADDRESS TEMP.
IAR=LIT
B=A3;MR1;IF R0C
WHEN R0C THEN BEX
B R=B
20-SAR;37=LIT
LIT AND B-SAR
A3 R=A3
B R=B
5-SAR
LIT AND B-SAR
CSAR
0111 R=B
S MASK FOR V BITS
A3 AND B=A3;MIR;0M1
B=MAR2;JUMP
SRETURN TO CALLING OP YFETCH OR Y2FETCH;MIR=CHAR IN LSB
S
S ***** SUBR. FOR MEMORY STORES *****
YSTORE: S CALLED FROM OPCODES VALUE TO STORE IS IN MIR
SMAR1 IS SETUP TO READ 0(B)
A1 R=A3
17-SAR;7=LIT
A3 AND LIT=A3
A3;LIT=MAR
0BASE=LIT
A1 R=B;MR1;IF R0C
7=LIT;20-SAR
LIT AND B=A3
KSTABLE-1=MPCR
WHEN R0C THEN A3;AMPCB=AMPCB;DEX
IF NOT 0C2 THEN A1 L=A3;CSAR;SKIP
Y2ABNORMAL-1=MPCR
COMP 19-SAR;7=LIT
YSTORE2: S RETURN HERE FROM ABNORMAL IF NOT REPLACE ABNORMAL
A3 R=A3
SISOLATE Y-FIELD
A3;B(A3);CSAR
SY;B(B);A3

```

```

0165 0009 A0C0 0020 00F0
0166 0009 2C56 0030 00F0
0167 0009 2C80 0C3C 00F0
0168 0100 0000 0C00 00A0

0169 0009 0003 0030 00FC
016A AC20 0000 0C00 00FC
016B 0009 EC43 0C1C 00F0
016C 0020 0000 0C0C 00F0

016D 0009 C000 7C00 00F0
016E 9070 0000 0000 00A0
016F 0009 E156 9090 00F0
0170 1000 0000 0030 0000
0171 5019 E152 0000 00F0
0172 006C 0000 0000 00A0
0173 0030 0000 0000 00E0
0174 6019 00C0 00C0 00F0
0175 0070 0000 0000 00A0
0176 000C 0000 0000 0060
0177 00A0 0000 0030 00A0

0178 0009 0000 1000 00F0
0179 0100 0000 0000 00E0
017A 1000 0000 0030 00A0
017B 3019 A0C1 1000 00F0
017C 1770 0000 0000 00A0
017D 9070 00C0 0000 0050
017E 1020 0000 0000 00A0

017F 0009 0000 0000 00F0
0180 0100 0000 0000 00E0
0181 0009 0000 0030 00F0
0182 AC00 0000 0C00 00F0
0183 0009 0C40 9030 00F0
0184 A030 0000 0000 0000
0185 0009 E152 0000 00F0
0186 6019 0C40 9030 00F0
0187 0070 0000 0C00 00A0
0188 51FC 0000 0030 00A0
0189 0009 E156 4030 00F0
018A 0009 E0C0 0000 00F0
018B 2100 0000 0000 0000
018C 0009 2C56 0000 00F0
018D 01FC 0000 0030 00E0
018E AC00 0000 0C30 00F0
018F 0009 0010 9000 00F0
0190 0009 0C43 001C 00F0
0191 0009 EC56 0030 00F0
0192 AC00 A0F0 0C00 00F0
0193 0009 0C41 0030 00F0
0194 0009 EC44 0000 00F0
0195 0009 0C41 0000 00F0
0196 9009 0C00 0000 10F0
0197 9020 0000 0000 00FC

```

```

04130000 D
04140000 D
04150000 D
04160000 D
04170000 D
04180000 D
04190000 D
04200000 D
04210000 D
04220000 D
04230000 D
04240000 D
04250000 D
04260000 D
04270000 D
04280000 D
04290000 D
04300000 D
04310000 D
04320000 D
04330000 D
04340000 D
04350000 D
04360000 D
04370000 D
04380000 D
04390000 D
04400000 D
04410000 D
04420000 D
04430000 D
04440000 D
04450000 D
04460000 D
04470000 D
04480000 D
04490000 D
04500000 D
04510000 D
04520000 D
04530000 D
04540000 D
04550000 D
04560000 D
04570000 D
04580000 D
04590000 D
04600000 D
04610000 C
04620000 D
04630000 D
04640000 D
04650000 D
04660000 D
04670000 D
04680000 D
04690000 D
04700000 D
04710000 D
04720000 D

```

```

ISOLATES S-FIELD
SSAR SETUP FOR USE BY KS ROUTINES
FROM ALL INDIR EXCEPT CA AND REPLACE REPEAT
SAR2=Y*B(0)+S(0)
AMPCR=K-HANDLER;B(0)
ISOLATE SPEC COND BITE
MUST BE REPEAT STORE
XCODE FOR CHAR ADDR.
TEST FOR CA
XNOT CHAR ADDRESSING
XCA STORE CHAR AND RETURN
NOT CHAR ADDR.
XREAD PRECALCULATED ADDRESS OF Y
XADDRESS OF PRECALC. Y-ADDR.
XLET YSTORE READ/WRITE USING K
XREPLACE THEN USE PRECALC ADDR OF Y
XNOT REPLACE REPEAT CALC ADDRESS
XMASK WORD IN MIR BY W BITS;X0X000 D
IF SINGLE CA TO Y ADDR.;X0X000 D
DEPENDING ON LC1=P-V LT 0 = P
XSTORE AT ADDRESS (2C).
XREAD ICN
ISOLATE BITS 31 & 30
XSEQUENTIAL CA CHECK
XICV;X3=0C/W/P
XMASK FOR P&W FIELDS OF IAV
XAI NOV = P VALUE
XLIIT=ADDRESS OF Y-ADDRESS;X3=0C/W
XGET Y-ADDRESS;SAR=W VALUE
XNOT W/B=Y ADDRESS
XMAK W BITS LONG
XREAD (Y);B=DATA WORD
XMR = MASKED DATA LSB
X(Y);SAR = P VALUE
X(Y) SHIFTED BY P
X(Y) MASKED OR DATA
XMR-(Y) OR DATA BACK TO POSITION
XWRITE NEW (Y)
XICV;X3=0C/W/P

```



```

0100 AC08 0000 0C50 00F0
0101 0000 0000 0090 0010
0102 4009 0C40 0000 40F0
0103 4009 0C41 1090 40F0
0104 4009 0C41 0000 40F0
0105 4009 0C40 0000 00F0
0106 4009 0C5C 1090 00F0
0107 0C4E 0000 0090 0040

0108 0000 2001 1C90 00F0
0109 00F0 0000 0000 0000
010A 4009 0C40 1090 00F0
010B 4009 0C41 0000 00F0
010C 4009 0C40 0000 00F0
010D 0000 0000 0090 0020
010E 4009 0C5C 1090 00F0
010F 0C50 0000 0090 0040

01E0 AC08 0000 1C90 00F0
01E1 00F0 0000 0000 00A0
01E2 4009 0C40 1090 00F0
01E3 4009 0C41 0000 00F0
01E4 0000 0000 0000 0010
01E5 4009 0C40 0000 00F0
01E6 4009 0C5C 1C90 00F0
01E7 0C6C 0000 0000 0040

01E8 AC08 0000 0C0C 00F0
01E9 4009 0C41 0090 40F0
01EA 0000 0000 0C30 0030
01EB 4009 0C40 9000 00F0
01EC 4009 0C41 0090 00F0
01ED 4009 0C5C 1C90 00F0
01EE 0C70 0000 0000 0040

01EF 4009 0000 0C50 00F0
01F0 0C0C 0000 0000 0040

01F1 4009 09C1 1090 00F0
01F2 0000 0000 0090 0020
01F3 4009 0C5C 0C50 00F0
01F4 0C90 0000 0000 0040

01F5 4009 2001 1C90 00F0
01F6 0020 0000 0000 00A0
01F7 4009 0C5C 0000 00F0
01F8 0CA0 0000 0090 0040

01F9 4009 2301 1090 00F0
01FA 0070 0000 0000 00A0
01FB 4009 0C5C 0C90 00F0
01FC 0C0C 0000 0090 0040

WHEN RDC THEN BEX
B-SAR
B R=0,CSAR
B L=A3,0MI,CSAR
B L=B,CSAR
B R=0
A3 OR B=A3,MIR
OUTPUT2MORET-1=MPCR
S(A7-0)>>Y15-0
WHEN RDC THEN LIT L = A3,CSAR,BEX
255 = LIT; COMP 0 = SAR
A3 MIR B=A3,0MI
B L=B
B R=0
16=SAR
A3 OR B=A3,MIR
OUTPUT2MORET-1=MPCR
S(A7-0)>>Y23-16
WHEN RDC THEN LIT L=A3,BEX
255=LIT;16=SAR
A3 MIR B=A3,0MI
B L = 0
COMP 24 = SAR
B R=0
A3 OR B=A3,MIR
OUTPUT2MORET-1=MPCR
S(A7-0)>>Y31-24
WHEN RDC THEN BEX
B L=B,CSAR
COMP 0 = SAR
B R=A3,0MI
B L = 0
A3 OR B=A3,MIR
OUTPUT2MORET-1=MPCR

K55:
K56:
K57:

S ***** SUBR. FOR I/O FUNCTIONS *****
TOUNPREG:
O = MIR
SIGLOADER-1=MPCR
1 L = A3
COMP 16 = SAR
A3 OR 0MAR=MIR
SIGLOADER-1=MPCR
CARDREAD: SREAD A CARD INTO ADDRESS IN B
LIT L=A3
2=LIT/COMP 16=SAR
A3 OR B=MIR
SIGLOADER1-1=MPCR
PRINTLINE: SPRINT AN OUTPUT BUFFER ADDRESSED IN B
LIT L=A3
7=LIT/COMP 16=SAR
A3 OR B=MIR
SIGLOADER1-1=MPCR
DISKREAD: SREAD/WRITE DISK USING INFO AT Y<(B)>.(S)
SB=NUMBER OF WORDS
SB+1=DISK SECTOR TO BE ACCESSED
SB+2 = 3->READ; 4->WRITE
SB+3=ADDRESS OF BUFFER

*****05640C00 D
05200C00 D
05250C00 D
05300C00 D
05310C00 D
05320C00 D
05330C00 D
05340C00 D
05350C00 D
05360C00 D
05370000 D
05380C00 D
05390C00 D
05400C00 D
05410C00 D
05420C00 D
05430C00 D
05440000 D
05450000 D
05460C00 D
05470C00 D
05480C00 D
05490C00 D
05500C00 D
05510C00 D
05520C00 D
05530C00 D
05540C00 D
05550C00 D
05560C00 D
05570C00 D
05580C00 D
05590C00 D
05600C00 D
05610C00 D
05620C00 D
05630C00 D
05640C00 D
05650C00 D
05660C00 D
05670C00 D
05680C00 D
05690C00 D
05700C00 C
05710C00 D
05720C00 D
05730C00 D
05740C00 D
05750C00 D
05760C00 D
05770C00 D
05780C00 D
05790C00 D
05800C00 C
05810C00 D
05820C00 D
05830C00 D
05840C00 D
05850C00 D
05860C00 D
05870C00 D

```

```

01FD 0009 0C43 001C 00F0
01FE 0000 0000 0000 00F0
01FF AC00 0F46 0C1C 00F0
0200 0009 0C91 1000 00F0
0201 0000 0000 0000 0020
0202 AC00 0F46 0C1C 00F0
0203 0009 0C5C 1000 00F0
0204 AC00 0F46 0C1C 00F0
0205 0009 0C91 4000 00F0
0206 AC00 0000 001C 00F0
0207 0009 E000 0000 00F0
0208 0009 AC5C 4000 10F0
0209 9C00 AC5C 0000 00F0
020A 0A5C 0000 0000 00C0

020B 0009 0010 001D 00F0
020C 0009 0000 0000 10F0
020D 1ACB 0000 0000 00F0
020E 49C9 0000 0000 00F0
020F 9090 0000 0000 00F0
0210 0AC0 0000 0002 00F0
0211 0900 0000 0000 00F0
0212 200D 0000 0000 00F0
0213 10A0 0000 0000 00F0

0214 0009 0C41 0000 00F0
0215 0000 0000 0000 00A0
0216 0009 2C5D 0000 00F0
0217 20A0 0000 0000 0060
0218 0009 0C01 0000 00F0
0219 0000 0000 0000 00E0
021A 3019 2C5D 0000 00F0
021B 2090 0000 0000 0000
021C 0000 0000 0000 00C0
021D 20A0 0000 0000 00A0
021E 4010 0000 0000 00F0
021F 0009 0000 0000 00F0
0220 2130 0000 0000 00A0
0221 4009 2000 0000 00F0
0222 0009 2000 0000 00F0
0223 0000 0000 0000 00E0
0224 2130 0000 0000 00A0
0225 4010 0000 0000 00F0
0226 4009 0000 0000 00F0
0227 2130 0000 0000 00A0

0228 0009 0000 0000 00F0
0229 010C 0000 0000 00E0
022A 00CC 0000 0000 00A0

022B 0009 0000 0000 00F0
022C 010C 0000 0000 00E0
022D 0009 0000 0000 00F0
022E AC00 0000 0000 00F0

```

```

0500CC00 0
0500F000 0
05000000 0
05010000 0
05020000 0
05030000 0
05040000 0
05050000 0
05060000 0
05070000 0
05080000 0
05090000 0
05100000 0
05110000 0
05120000 0
05130000 0
05140000 0
05150000 0
05160000 0
05170000 0
05180000 0
05190000 0
05200000 0
05210000 0
05220000 0
05230000 0
05240000 0
05250000 0
05260000 0
05270000 0
05280000 0
05290000 0
05300000 0
05310000 0
05320000 0
05330000 0
05340000 0
05350000 0
05360000 0
05370000 0
05380000 0
05390000 0
05400000 0
05410000 0
05420000 0
05430000 0
05440000 0
05450000 0
05460000 0
05470000 0

```

```

B=MAR2
MR2; IF RDC
WHEN RDC THEN BMR+1=MAR2,BEX
B L=A3;MR2;IF RDC SA3=NUM WORDS/0
COMP 16=SA3
WHEN RDC THEN BMR+1=MAR2,BEX
A3 OR B=A3;MR2;IF RDC SA3=NUM WORDS/SECTOR
WHEN RDC THEN BMR+1=MAR2,BEX
B L=A1;MR2;IF RDC SA1=3 OR 4/0
WHEN RDC THEN B110=MAR2
A3=MIR
A1 OR B=A1;MR2;IF SA1 SA1=3-4/ADDRESS
WHEN SA1 THEN A1=MIR
SIGLOADER1; IFETCH-1=AMPCR
SIGLOADER;
B111=MAR2,CTR
MR2; IF SA1
IF GC2 THEN RESET GC2; STEP ELSE SKIP
SET LC1
WHEN SA1 THEN RESET GC1
INC;WHEN COV THEN RESET GC2;STEP
SET GC1;WHEN GC1 THEN STEP
IF LC1 THEN STEP ELSE JUMP
SET GC2; WHEN GC2 THEN JUMP

ERRMSG0; 3D-NUMBER OF ERROR MESSAGE TO BE PRINTED
B0=ILLEGAL INSTRUCTION
B1=INSTRUCTION NOT IMPLEMENTED
B2=SQUARE ROOT OF NEGATIVE NUMBER
B L=B
16=SA3;P5=LIT
LIT OR B C=MIR
SIGLOADER-1=CPCR
A2 L=B
6=LIT
LIT OR B C=MIR;IF LC2 THEN SKIP
SIGLOADER-1=MPCR
HALFFETCH=AMPCR
ILLEGAL; 0=0;SKIP
ILLEGAL; 0=0;SET LC2
ILLEGALCNR1; LIT=0;SET LC2;SKIP
ILLEGALCNR; LIT=0
3=LIT
ERRMSG0-1=MPCR
UNWRITTEM; 1=0;SKIP
UNWRITTEM; 1=0;SET LC2
ERRMSG0-1=MPCR
ERRMSG0-1=MPCR
SUBR; FOR REGISTER STORES *****
PUTPAR; *****
PAR=LIT
OUTPUT1-1=MPCR
*****
GETPAR; LVAR
PAR=LIT
MR1;IF RDC
WHEN RDC THEN BEX

```

022F	402D	0C4D	2050	00F0	06480000	D
0230	0A50	0000	0000	00C0	06490000	D
0231	9009	0000	0000	10F0	06500000	D
0232	9C20	0000	0000	00F0	06510000	D
0233	0A50	0000	0050	00C0	06520000	D
0234	9009	0000	0000	10F0	06530000	D
0235	9C00	0000	0000	00F0	06540000	C
0236	0000	0000	0050	00F0	06550000	C
0237	1F00	0000	0050	0040	06560000	D
0238	1C19	C060	9090	00F0	06570000	D
0239	2320	0000	0050	0040	06580000	D
023A	0100	0000	0050	00A0	06590000	D
023B	9009	E000	0050	00F0	06600000	D
023C	5C19	0000	0000	00F0	06610000	D
023D	2320	0000	0050	0040	06620000	D
023E	A009	0000	0050	00F0	06630000	D
023F	AC00	0000	0050	00F0	06640000	D
0240	3C09	0C4D	001C	00F0	06650000	D
0241	2320	0000	0050	0040	06660000	D
0242	2A59	0000	0030	00F0	06670000	D
0243	22F0	0000	0000	0040	06680000	D
0244	2300	0000	0000	0060	06690000	D
0245	4009	A000	001C	00F0	06700000	D
0246	2370	0000	0000	0040	06710000	D
0247	4009	A000	9000	00F0	06720000	D
0248	0070	0000	0030	00A0	06730000	D
0249	402D	E156	1000	00F0	06740000	D
024A	4009	A000	0030	00F0	06750000	D
024B	0070	0000	0050	00A0	06760000	D
024C	402D	2C5E	009C	00F0	06770000	D
024D	4009	A000	9050	00F0	06780000	D
024E	0070	0000	0000	00A0	06790000	D
024F	402D	E156	109C	00F0	06800000	D
0250	4009	A000	9050	00F0	06810000	D
0251	4030	0000	0000	00A0	06820000	D
0252	402D	E156	1000	00F0	06830000	D
0253	4009	E15E	0000	00F0	06840000	D
0254	0100	0000	0000	00EC	06850000	D
0255	73E9	0000	0050	00F0	06860000	D
0256	4009	E15E	0000	00F0	06870000	D
0257	0100	0000	0000	00E0	06880000	D
0258	7C19	E15E	0000	00F0	06890000	D
0259	20E0	0000	0050	00F0	06900000	D
025A	0300	0000	0000	00E0	06910000	D
025B	7C19	E15E	0000	00F0	06920000	D
025C	2020	0000	0050	00F0	06930000	D
025D	0500	0000	0000	00E0	06940000	D
025E	7C19	E15E	0000	00F0	06950000	D
025F	20E0	0000	0050	00F0	06960000	D
0260	0000	0000	0000	00E0	06970000	D
0261	7C19	E15E	009C	00F0	06980000	D
0262	2020	0000	0050	00F0	06990000	D
0263	2000	0000	0050	C090	07000000	D
0264	7019	0000	0050	00F0	07010000	D
					07020000	D
					07030000	D
					07040000	D
					07050000	D
					07060000	D
					07070000	D

```

OUTPUT: B=42;JUMP
          SMO RETURN
          IFETCH-1=AMPCR
OUTPUT1: MV1IF SAI
          WHEN SAI THEN 0;JUMP
OUTPUT2M0RET: IFETCH-1=AMPCR
OUTPUT2: MV2IF SAI
          WHEN SAI THEN 0;STEP
          IF JRO THEN STEP ELSE JUMP
          100MPADR-1=MPCR
          SY-ADDRESS IN MAR2 CAME FROM PRECALCULATED EXCEPT REP
          IF GC2 THEN A2 B=A3;SKIP SREPLACE REPEAT IS SPECIAL
          OUTPUT2M0RET-1=MPCR
          20-SARI;ADDR=LIT
          A3
          IF LST THEN LVAR;SKIP
          OUTPUT2M0RET-1=MPCR
          MHI;IF RDC
          WHEN RDC THEN BEX
          IF LC2 THEN B=MAR2
          OUTPUT2M0RET-1=MPCR
          S *****
          OUTLOGIC: LOGICAL SUBROUTINES *****
                   SY ADDRESS IN 0,A ADDR IN MAR1
                   S0PCODE01-> M0 RETURN
                   S0PCODE 02 -> RETURN
                   SSAVE Y-ADDRESS IN A1
                   SOUTPUT TO Y ADDRESS
                   SISOLATE AND RETURN F FIELD
                   S1SOLATE AND RETURN IN B & MAR A-FLD
                   SISOLATE AND RETURN IN A3&MAR A-FIELD
                   SRETURNS F1 FIELD FOR TYPE 3 IN A3
                   21-SAR;J=LIT
                   A3 AND LIT=A3;JUMP
                   CHECKMR: SCHR ADDRESS IN A3;LC1 SET IF PRIVILEGED;RETURN LC1 IF LEGAL
                   A3 LSS LIT
                   SCHECK ADDR LT 20 OCTAL
                   16-LIT
                   IF TRUE THEN SET LC1; JUMP
                   A3 LSS LIT
                   SCHECK ADDRESS LT 30 OCTAL
                   24-LIT
                   IF FALSE THEN A3 LSS LIT; SKIP
                   SCHECK A:DR LT 30 OCTAL
                   JUMP; IF LC1 THEN SET LC1
                   48-LIT
                   IF FALSE THEN A3 LSS LIT;SKIP
                   SCHECK ADDR LT 60 OCTAL
                   JUMP; IF LC1
                   88-LIT
                   IF FALSE THEN A3 LSS LIT;SKIP
                   JUMP; IF LC1 THEN SET LC1
                   96-LIT
                   IF FALSE THEN A3 LSS LIT;SKIP
                   JUMP; IF LC1
                   120-LIT;10-SAR
                   IF TRUE THEN SKIP

```

```

0265 202D 0000 0000 0000
0266 20ED 0000 0000 0000

0267 2619 0000 0000 0000
0268 0A50 0000 0000 0000
0269 0000 0000 0000 0000
0270 3009 0001 0000 0000
0271 4009 EC5C 2000 0000
0272 2270 0000 0000 0000
0273 0A50 0000 0000 0000

0274 4009 A0C1 1000 0000
0275 2000 0000 0000 0000
0276 4009 E000 9000 0000
0277 4000 0000 0000 0000
0278 10E0 0000 0000 0000
0279 4009 E156 0000 0000
0280 4009 E156 0000 0000
0281 9600 0000 0000 0000
0282 4009 2C52 0C00 2000
0283 0020 0000 0000 0000
0284 6509 2F40 0000 0000
0285 0000 0000 0000 0000
0286 4009 2C52 0000 0000
0287 0030 0000 0000 0000
0288 6009 0000 0000 0000
0289 2A00 0000 0000 0000
0290 AC10 0000 0000 0000
0291 4009 E156 0000 0000
0292 93F0 0000 0000 0000
0293 4009 E000 0000 0000
0294 4009 2C56 1000 0000
0295 4009 E15E 0000 0000
0296 0200 0000 0000 0000
0297 7FC9 E15E 0000 0000
0298 AC20 0000 0000 0000

0299 08CC 0000 0000 0000
0300 2000 0000 0000 0000
0301 0A50 0000 0000 0000

0302 4009 EC52 0000 0000
0303 6C19 0010 A000 0000
0304 4009 080F AC00 0000

0305 0000 0000 0000 0000
0306 4009 EC4C 0000 0000
0307 4000 EC5E 0000 0000
0308 7C20 080F AC00 0000
0309 7429 080F A000 0000
0310 4020 0010 A000 0000

```

```

JUMP IF LC1
JUMP IF LC1 THEN SET LC1
***** JUMP SUBROUTINES *****
PUTJUMP: 8A3-JUMP ADDRESS/STORE IN A3/JAR
IF LC1 THEN A2 R=A2/SKIP
IFETCH-1=MPCR
16=8AR
A2 L=8;IF LC2
A3 OR B=A2
PUTPAR-1=CPCR
IFETCH-1=MPCR

***** SHIFT SUBROUTINES *****
SHIFTAMOUNT: SRETURNS B=(A-REG);MAR=A-ADDR;SAR=SHIFAMOUNT
A1 L=A3
A3 R=A3
22=8AR
A3 AND LIT R=MAR
14=LIT;SAR
A3 AND LIT R=8
96=LIT;SAR
LIT EOL B/JAR
2=LIT
IF TRUE THEN LIT;B/MAR;MARISET LC1
BBASE=LIT
LIT EOL B;IF RDC
3=LIT
IF TRUE THEN SET LC1
IF LC1 THEN MARISET ELSE SKIP
WHEN RDC THEN BEX/SKIP
A3 AND LIT=8
63=LIT;SAR
A3 R=MAR;CTR
LIT AND B=SAR;A3/MR1;IF RDC
A3 6EO LIT
32=LIT
IF TRUE THEN A3-LIT=8ARISET LC1
WHEN RDC THEN BEX/JUMP
S8=(A-REG);MAR=A-ADDR;SAR=SHIF AMT.

***** COMPARE SUBROUTINES *****
SETCOMPARE: SCOMPARE A(B) WITH A(CA) AND SET CD BITS
HALFETCH=AMPCR
IF LC1 THEN STEP ELSE SKIP
IFETCH-1=MPCR
***** CALLED BY OPR 44,46,47
***** SELSE OPR 74X4,6,7 *****
SETCDRET: SENTER HERE AND RETURN WHERE CALLED FROM
A3 EOL B/SET LC2
IF TRUE THEN A2 OR 9100 C=A2;CSAR/SKIP
A2 AND 8011 C=A2;CSAR SCLEAR EQUAL BIT
S GREATER THEN EQUAL TO BIT NOV IN M8B
31=8AR
A3 XOR B
A3 LSS B; IF M8T THEN STEP ELSE SKIP
IF FALSE THEN A2 AND 8011 C=A2;JUMP ELSE SKIP
IF TRUE THEN A2 AND 8011 C=A2;JUMP
A2 OR 8100 C=A2;JUMP
S A2 RESTORED TO NORMAL BEFORE EXIT TO WHERE CALLED FROM

```

```

S ***** BIT COUNT SUBROUTINE *****
COUNTONES:  SCOUNT NUMBER OF ONES IN B AND RETURN COUNT IN A3,MIR
0-A3,LCIR
31=LIT,1-SAR
CHECKLSB:  B C=0,INC
IF LST THEN A3+1=A3,MIR
IF COV THEN JUMP
CHECKLSB-1=MPCR
S
S ***** MULTIPLY SUBROUTINE *****
MULTIPLY:  SA2 AND B CONTAIN OPERATORS
0-A3,A3,LCIR
31=LIT,1-SAR
O EOL B,IF LC1
IF FALSE THEN A2 XOR B,STEP ELSE JUMP
A2,IF MST THEN SET LC1
IF MST THEN NOT A2=A2
B
IF MST THEN NOT B=B
MULT1:  A2 R=A2,INC
IF LST THEN A1+B R=A1,SKIP SA1=MOST SIGNIFICANT
A1 R=A1
IF LST THEN A3 OR B,00=A3 SA3=LEAST SIGNIFICANT
IF NOT COV THEN A3 R=A3,STEP ELSE SKIP
MULT1-1=MPCR
IF LC1 THEN NOT A3=A3,STEP ELSE JUMP
NOT A1=A1,JUMP
S
S ***** DIVIDE SUBROUTINE *****
DIVIDE:  SB=DIVISOR, A3=MOST DIVIDEND, MAR=LEAST DIVIDEND ADDRESS
0-A1,A2,LCIR,SET LC2
30=LIT,COMP 1-SAR
O EOL B
A3, IF TRUE THEN SET LC1,JUMP OVERFLOW->DIVISION BY ZERO
IF MST THEN NOT A3=A3,SET LC1
B,MRA,IF RDC
IF MST THEN DIFF=B
DIV1:  A3 L=A3
IF MST THEN A1 OR B,001=A1
A1 LSS B,011
IF FALSE THEN A2 OR B,001=A2,STEP ELSE SKIP
A1-B,011=A1
INC,IF NOT COV THEN SKIP
DIV2-1=MPCR
A1 L=A1
A2 L=A2
IF MST THEN SET LC1,JUMP
DIV1-1=MPCR
DIV2:  IF LC2 THEN A2 L=A2,LCIR,SKIP
DIV3-1=MPCR
B=A3
WHEN RDC THEN A1 L=A1,BEX SB=LEAST DIVIDEND
A3 XOR B=A3
A3 XOR B=B
A3 XOR B=A3
IF LC1 THEN NOT A3=A3,SET LC1
DIV1-1=MPCR
07680000 D
07700000 D
07710000 D
07720000 D
07730000 D
07740000 D
07750000 D
07760000 D
07770000 D
07780000 D
07790000 D
07800000 D
07810000 D
07820000 D
07830000 D
07840000 D
07850000 D
07860000 D
07870000 D
07880000 D
07890000 D
07900000 D
07910000 D
07920000 D
07930000 D
07940000 D
07950000 D
07960000 D
07970000 D
07980000 D
07990000 D
08000000 D
08010000 D
08020000 D
08030000 D
08040000 D
08050000 C
08060000 D
08070000 D
08080000 D
08090000 D
08100000 D
08110000 D
08120000 D
08130000 D
08140000 D
08150000 D
08160000 D
08170000 D
08180000 D
08190000 D
08200000 D
08210000 D
08220000 D
08230000 D
08240000 D
08250000 D
08260000 D
08270000 D

```

```

0293 4889 0808 1031 00F0
0294 11FC 0000 0000 0080
0295 4889 0C41 8002 00F0
0296 5089 08C0 1090 00F0
0297 8829 00C0 0020 00F0
0298 294C 0000 0030 0040

```

```

0299 4889 0008 5001 00F0
029A 11FC 0000 0000 0080
029B 2889 0C52 0000 00F0
029C 648D 0C4C 0C00 00F0
029D 48C9 0008 0C00 00F0
029E 4C09 0002 2000 00F0
029F 4889 0C40 0C00 00F0
02A0 4C09 0C42 0000 00F0
02A1 4889 0008 A032 00F0
02A2 5C19 AC40 C000 00F0
02A3 4889 A008 C000 00F0
02A4 5C09 F81C 1000 00F0
02A5 8406 6000 9000 00F0
02A6 2A00 0000 000C 0040
02A7 2C00 E002 1000 00F0
02A8 482D A002 4000 00F0

```

```

02A9 4889 0008 6001 00F0
02AA 51E0 0000 0020 0080
02AB 4889 0C52 0000 00F0
02AC 68E9 00C0 0030 00F0
02AD 4FC9 E002 1000 00F0
02AE A889 0C40 0030 00F0
02AF 4C09 1458 0000 00F0
02B0 4889 E001 1000 00F0
02B1 4C09 A0DC 4030 00F0
02B2 4889 A45E 0C00 00F0
02B3 7C08 C0DC 2030 00F0
02B4 4889 A45E 4030 00F0
02B5 8019 00C0 0002 00F0
02B6 0C0C 0000 0000 0040
02B7 4889 A001 4030 00F0
02B8 4889 C001 2030 00F0
02B9 48E9 0000 0030 00F0
02BA 24FC 0000 003C 0040
02BB 3C19 C0C1 2001 00F0
02BC 0C0C 0000 0000 004C
02BD 4889 0C40 1000 00F0
02BE AC08 A001 4C30 00F0
02BF 4889 EC4C 1000 00F0
02C0 4889 EC4C 1000 00F0
02C1 4889 EC4C 1030 00F0
02C2 2FC9 E002 1000 00F0
02C3 24FC 0000 0030 0040

```

```

02C4 4809 0000 0000 0000
02C5 4819 0000 0000 0000
02C6 0000 0000 0000 0000
02C7 2000 0002 2000 0000
02C8 4820 0002 4000 0000
02C9 2029 0002 4000 0000
02CA 4820 0002 2000 0000

02CB 4809 0001 1000 0000
02CC 4800 0000 0000 0000
02CD 4809 0000 0000 0000
02CE 4808 0000 0000 0000
02CF 0000 0000 0000 0000

02D0 3009 2001 0000 0000
02D1 3070 0000 0000 0000
02D2 4809 0000 2000 0000
02D3 0000 0000 0000 0000

02D4 4809 0000 0000 0000
02D5 0000 0000 0000 0000
02D6 4809 0000 0000 0000
02D7 4808 0000 0000 0000
02D8 4809 0000 0000 0000
02D9 4809 0000 1000 0000
02DA 4809 0000 0000 0000
02DB 2300 0000 0000 0000
02DC 4809 0000 0000 0000
02DD 0100 0000 0000 0000
02DE 4809 0000 0000 0000
02DF 4808 0000 0000 0000
02E0 4809 0000 0000 0000
02E1 0070 0000 0000 0000
02E2 4809 0156 0000 0000
02E3 0010 0000 0000 0000
02E4 3029 0000 0000 0000
02E5 0020 0000 0000 0000
02E6 4809 0000 0000 0000
02E7 0100 0000 0000 0000
02E8 4809 0000 0000 0000
02E9 4808 0000 0000 0000
02EA 4809 0000 0000 0000
02EB 4809 0000 0000 0000
02EC 4809 0000 0000 0000
02ED 4819 0018 0000 0000
02EE 4809 0000 0000 0000
02EF 4808 0000 0000 0000
02F0 4809 0000 0000 0000
02F1 4809 0000 0000 0000
02F2 1070 0000 0000 0000
02F3 4809 0156 1000 0000
02F4 4809 0140 0000 0000
02F5 0000 0000 0000 0000
02F6 4809 0000 0000 0000
02F7 4808 0000 1000 0000
02F8 4809 0000 0000 0000
02F9 2300 0000 0000 0000

      DIV3: 0
      IF NOT MST THEN SKIP
      DIVNEG-1=MPCR
      IF LC1 THEN NOT A2=A2;STEP ELSE JUMP
      NOT A1=A1;JUMP
      DIVNEG: IF LC1 THEN NOT A1=A1;JUMP
      NOT A2=A2;JUMP
      S
      S *****ROUTINES FOR REPEAT AND INDIRECTION CONTROL *****
      GC2CHECK:
      A2 L = A3
      A3
      IF MST THEN STEP ELSE SKIP
      RPTCHECK-1 = CPCR
      GC2CHECK1:
      LIT L = B; IF LC2
      7 = LIT; COMP 21 = SAR
      A2 NIM B = A2; RESET GC2
      IFETCH1-1 = MPCR
      RPTCHECK:
      LMAR
      15 = LIT
      MR1; IF RDC
      WHEN RDC THEN BEX
      NOT B
      IF NOT ABT THEN B=A3;STEP ELSE JUMP
      A3-1 = MIR
      OUTPUT1-1 = CPCR
      LMAR
      RINST=LIT
      MR1; IF RDC
      WHEN RDC THEN BEX
      B R=A1;MIR
      7 = LIT; 23 = SAR
      A1 AND LIT = A1
      ACP0-1 = AMPCR
      IF LC2 THEN JUMP
      ANCP0-1 = MPCR
      RPTCHECK1: LMAR
      RINST=LIT
      MR1; IF RDC
      WHEN RDC THEN BEX
      B L = BALMAR
      CINST=LIT;16=SAR
      B;MR1;IF RDC
      IF MST THEN B11 R=A1;SKIP
      0=A1
      WHEN RDC THEN A1 OR B C=MIR;BEX
      B = A1
      A1 R = A3
      7 = LIT; 17 = SAR
      A3 AND LIT = A3;BMI
      A3 + LIT = MAR
      BRASE = LIT
      MR1; IF RDC
      WHEN RDC THEN B = A3;BEX
      A3 + B = MIR
      OUTPUT1-1 = CPCR

      SQUOTIENT IN A2;REM IN A1
      S GC2 IS SET
      SCHECK BIT 21=REPEAT BIT
      S CHECK FOR REPEAT MODE
      S CLEAR A2(23-21)
      S B(7)
      S REPEAT INSTR.
      S REPEAT INSTR.
      S A-FIELD
      S CHECK A-FIELD
      S FOR TERMINATE
      S CONDITIONS
      S CURRENT INSTR.
      S RESTORE C.I.
      S RESTORE C.I.
      S 6-FIELD
      S 6(B)+SY=>B(8)

```

```

02FA 4809 0000 0000 00F0
02FB 0180 0000 0000 00E0
02FC 4809 0000 0C00 00F0
02FD AC08 0000 0C00 00F0
02FE 4809 EC40 0030 00F0
02FF 2300 0000 0030 0060
0300 0830 0000 0000 0040

0301 4809 0640 0030 00F0
0302 4809 A000 9000 00F0
0303 1070 0000 0000 00A0
0304 4809 E156 1000 00F0
0305 4809 E140 000C 00F0
0306 0080 0000 0030 00E0
0307 4809 A0C1 0800 48F0
0308 9160 0000 0030 0090
0309 AC08 0C40 9C00 00F0
030A 4809 EC40 1008 00F0
030B 4809 0000 0020 00F0
030C 0180 0000 0030 00E0
030D AC08 0000 0C0C 00F0
030E 4809 EC40 0D38 00F0
030F 2300 0000 0020 0060
0310 4809 0C40 0040 00F0
0311 4809 9000 0030 00F0
0312 4820 0000 0030 00F0

0313 4809 A000 9000 00F0
0314 1070 0000 0000 00A0
0315 4809 E156 1000 00F0
0316 4809 E140 000C 00F0
0317 0080 0000 0000 00E0
0318 4809 A0C1 0800 48F0
0319 9160 0000 0030 0090
031A AC08 0C40 9C00 00F0
031B 4809 EC40 1008 00F0
031C 4809 A000 9000 00F0
031D 9070 0000 0030 0090
031E 4809 2C56 0800 00F0
031F 4809 2C40 000C 00F0
0320 0100 0000 0000 00E0
0321 4809 0000 0C00 00F0
0322 AC08 0000 0C00 00F0
0323 4820 EC40 101C 00F0

0324 4809 A000 9000 00F0
0325 1070 0000 0000 00A0
0326 4809 E156 1000 00F0
0327 4809 E140 000C 00F0
0328 0100 0000 0030 00A0
0329 4809 A0C1 0800 48F0
032A AC08 E000 9C00 00F0
032B 4820 EC40 101C 00F0

032C 4809 A000 9000 00F0
032D 1070 0000 0000 00A0
032E 4809 E156 1000 00F0
032F 4809 E140 000C 00F0
0330 0080 0000 0000 00A0
0331 4809 A001 0800 48F0

```

```

LMAR
YADDR=LIT
MR1 IF RDC
WHEN RDC THEN BEX
A3 + B = MIR
IFETCH2 -1 = MPCR

S6YFETCH:
AMPCR = MIR
A1 R = A3
7 = LIT; 17 = SAR
A3 AND LIT = A3
A3 + LIT = MAR
BBASE = LIT
A1 L = B;CSAR; MR1; IF RDC
S6=LIT;COMP 19=SAR
WHEN RDC THEN B R = A3;BEX
A3 + B = A3;LMAR
MR1; IF RDC
YADDR=LIT
WHEN RDC THEN BEX
A3+B=MIR;BMI;LMAR
OUTPUT1-1 = CPCR
B = AMPCR
STEP
JUMP

FETNORM:
A1 R = A3
7 = LIT; 17 = SAR
A3 AND LIT = A3
A3 + LIT = MAR
BBASE = LIT
A1 L = B;CSAR; MR1; IF RDC
31 = LIT; COMP 19 = SAR
WHEN RDC THEN B R = A3;BEX
A3 + B = A3
A1 R = B
7 = LIT; 13 = SAR
LIT AND B = B
LIT + B = MAR
SBASE = LIT
MR1; IF RDC
WHEN RDC THEN BEX
A3 + B = A3;MAR2;JUMP

FETCHOPT0:
A1 R = A3
7 = LIT; 17 = SAR
A3 AND LIT = A3
A3 + LIT = MAR
SBASE = LIT; 16 = SAR
A1 L = A3; MR1; IF RDC
WHEN RDC THEN A3 R = A3;BEX
A3 + B = A3;MAR2; JUMP

FETCHOPT1:
A1 R = A3
7 = LIT; 17 = SAR
A3 AND LIT = A3
A3 + LIT = MAR
BBASE = LIT; 16 = SAR
A1 L = B; MR1; IF RDC

```

```

08880000 D
08890000 D
08900000 D
08910000 D
08920000 D
08930000 D
08940000 D
08950000 D
08960000 D
08970000 D
08980000 D
08990000 D
09000000 D
09010000 D
09020000 D
09030000 D
09040000 D
09050000 D
09060000 D
09070000 D
09080000 D
09090000 D
09100000 D
09110000 D
09120000 D
09130000 D
09140000 D
09150000 D
09160000 D
09170000 D
09180000 D
09190000 D
09200000 D
09210000 D
09220000 D
09230000 D
09240000 D
09250000 D
09260000 D
09270000 D
09280000 D
09290000 D
09300000 D
09310000 D
09320000 D
09330000 D
09340000 D
09350000 D
09360000 D
09370000 D
09380000 D
09390000 D
09400000 D
09410000 D
09420000 D
09430000 D
09440000 D
09450000 D
09460000 D
09470000 D

```

0332	AC08	0C40	0C80	00F0	WHEN RDC THEN B R = MIR,BEX	% SY => MIR	09480000	D
0333	4009	E140	003C	00F0	A3 + LIT = MAR	% S(B)	09490000	D
0334	0100	0000	0000	00E0	SPACE = LIT		09500000	D
0335	4009	0C40	1000	00F0	B = A3,BMI; MR1; IF RDC	% B(B)=>A3,SY=>B	09510000	D
0336	AC08	EC40	1C00	00F0	WHEN RDC THEN A3 + B = A3,BEX		09520000	D
0337	4020	EC43	101C	00F0	A3 + B = A3,MAR2; JUMP	% SY,B(B)+S(B)	09530000	D
0338	4009	A000	9C00	00F0	INDIRECT:		09540000	D
0339	2300	0000	0030	00B0	A1 R = A3	% OPCODE	09550000	D
033A	4009	E15E	0000	00F0	40-LIT;26-SAR		09560000	D
033B	7019	0000	0030	00F0	A3 LSS LIT		09570000	D
033C	003C	0000	0000	0040	IF TRUE THEN SKIP		09580000	D
033D	3120	0000	0000	0060	IFETCH-1 = MPCR	% HALF-WORD INST	09590000	D
033E	A009	A000	C000	0CF0	FETWORM-1 = CPCR	% Y=Y+B(B)+S(S)	09600000	D
033F	0000	C000	0030	0020	INDIRECT1:		09610000	D
0340	AC08	A001	4C30	00F0	INDIRECT2:		09620000	D
0341	4009	0C40	0030	00F0	A1 R = A1,CSAR; MR2; IF RDC	% Y => MAR2	09630000	D
0342	4009	0C41	0030	00F0	20 = SAR		09640000	D
0343	4009	0C40	0030	00F0	WHEN RDC THEN A1 L = A1,BEX		09650000	D
0344	4009	AC5C	4C30	00F0	B = MIR, CSAR	% (Y) = MIR	09660000	D
0345	4009	A000	9000	00F0	B L = B,CSAR		09670000	D
0346	0000	0000	0000	0020	B R = B		09680000	D
0347	4009	E000	0030	00F0	A1 OR B = A1	% REPLACE A1(19-0)	09690000	D
0348	5019	0000	0000	00F0	A1 R = A3,BMI	% (Y)=B	09700000	D
0349	003C	0000	0030	0040	16 = SAR		09710000	D
034A	4039	0C40	9030	00F0	A3		09720000	D
034B	0010	0000	0030	00B0	IF LST THEN SKIP	% A1(16)=17	09730000	D
034C	4009	E158	0030	00F0	INDIRECT3-1 = MPCR	% A1(16)=0	09740000	D
034D	7019	0000	0000	00F0	B R = A3	% A1(16)=1	09750000	D
034E	33C0	0000	0030	0040	ONE = LIT; 29 = SAR		09760000	D
034F	3200	0000	0000	00C0	A3 GTR LIT		09770000	D
0350	4009	E000	0030	00F0	IF FALSE THEN SKIP		09780000	D
0351	5033	00C0	0C00	00F0	INDIRECT1-1 = MPCR		09790000	D
0352	4018	0000	0000	00F0	FETCHOPI-1 = AMPCR		09800000	D
0353	3230	0007	000C	0060	A3		09810000	D
0354	3300	0000	0000	0040	IF LST THEN CALL ELSE SKIP	% Y =>MAR2,(Y)=>B,MTR	09820000	D
0355	4009	00C0	0006	00F0	SKIP		09830000	D
0356	01A0	0000	0000	00E0	FETCHOPI0-1 = CPCR		09840000	D
0357	2300	0000	0030	0060	INDIRECT2-1 = MPCR	% SAVE (Y) = ICM	09850000	D
0358	4009	00C0	0000	00F0	LVAR		09860000	D
0359	01C0	0000	0000	00E0	LVAR		09870000	D
035A	2300	0000	0030	0060	LVARADR=LIT		09880000	D
035B	1019	0000	0000	00F0	OUTPUT1-1 = CPCR	% SAVE Y = ADDR ICM	09890000	D
035C	0040	0000	003C	0040	IF 0C2 THEN SKIP	% REPEAT	09900000	D
035D	3000	0000	0030	0060	INDIRECT4-1 = MPCR		09910000	D
035E	4009	A000	0030	00F0	56FETCH-1 = CPCR	% Y = Y+B(B)+S(6)	09920000	D
035F	0170	0000	0000	00E0	A1 = MIR,LVAR		09930000	D
0360	2300	0000	0000	0060	CINST=LIT		09940000	D
0361	003C	0000	0030	0040	OUTPUT1-1 = CPCR	% SAVE C-1	09950000	D
0362	4009	0C40	9030	00F0	IFETCH2-1 = MPCR		09960000	D
0363	9010	0000	0000	00B0	INDIRECT4:		09970000	D
0364	4009	E158	000C	00F0	B R = A3	% (Y)31-29	09980000	D
0365	7019	0000	0000	00F0	A3 GTR LIT		09990000	D
0366	003C	0000	0030	0040	IF FALSE THEN SKIP	% SKIP FOR OPTIONAL INDIRECTON	10000000	D
0367	4009	1000	0000	00F0	INDIRECT6-1 = MPCR	% NORMAL OR CA	10010000	D
0368	0000	00C0	0000	0030	B100 R = B		10020000	D
					ZERO-LIT; 0-SAR		10030000	D
							10040000	D
							10050000	D
							10060000	D
							10070000	D

```

0369 4809 CC5C 2080 00F0
036A 3230 0000 0000 00C0
036B 4809 E152 0C00 00F0
036C 6833 0000 0000 00F0
036D 4818 0000 0000 00F0
036E 3200 0000 0000 0060

036F 4809 E0C0 0000 00F0
0370 0100 0000 0000 00E0
0371 2300 0000 0000 0060
0372 0030 0000 0000 0040

0373 4809 E000 0000 00F0
0374 1000 0000 0000 0000
0375 4809 E000 0000 00F0
0376 5000 0000 0000 00F0
0377 0060 0000 0000 0040
0378 4809 1000 0000 00F0
0379 1000 0000 0000 0010
037A 4809 CC5C 2080 00F0

037B 3120 0060 0000 0060
037C 4809 E000 0000 00F0
037D 36E0 0000 0000 0040

037E 4809 A000 0000 00F0
037F 2000 0000 0000 003C
0380 0070 0000 0000 0060
0381 3019 0000 0000 00F0
0382 0450 0000 0000 0040
0383 4809 2001 0000 00F0
0384 2030 0000 0000 0000
0385 4809 CC5C 2080 00F0
0386 3740 0000 0000 0040

0387 2920 0000 0000 0060
0388 4809 A640 0000 00F0
0389 0080 0000 0000 00C0
038A 4809 A0C0 0000 00F0
038B A024 0000 0000 00F0
038C AC00 0000 0000 00F0
038D 4836 0C40 0000 00F0
038E 2CFC 0000 0000 0040
038F 2E50 0000 0000 0040

0390 4809 0C52 0000 00F0
0391 602F 0000 0000 00F0
0392 4809 0C52 0000 00F0
0393 602F 0C52 0000 00F0
0394 602F 0000 0000 00F0
0395 602F 0C52 0000 00F0
0396 702F 0000 0000 00F0
0397 483F 0000 0000 00F0
0398 4809 E000 0000 00F0
0399 502F 0000 0000 00F0

```

```

SSET A2(23)
A2 0R 0=A2
FETCHOPT0-1 = AMPCR
A3 EOL LIT
IF TRUE THEN CALL ELSE SKIP
SKIP
FETCHOPT1-1 = CPCR
INDIRECT5:
A3 = MIR,LMAR; SET GC2
YADDR=LIT
OUTPUT1-1 = CPCR
IFETCH2-1 = MPCR
INDIRECT6:
A3 R = A3
1 = SAR
A3
IF LST THEN STEP ELSE SKIP
INDIRECT8-1 = MPCR
B100 R = B
9=SAR
A2 0R 0=A2
INDIRECT7:
FEYNORM-1 = CPCR
A3 = MIR
INDIRECT5-1 = MPCR
INDIRECT8:
A1 R = A3
26 = SAR
CONDHECK-1 = CPCR
IF LC2 THEN SKIP
IFETCH-1 = MPCR
LIT L=B
3=LIT; COMP 22=SAR
A2 0R 0=A2
INDIRECT7-1 = MPCR
ANCHP0:
COUNTONES-1=CPCR
A1=AMPCR=AMPCR
AOP-1=AMPCR
A1=WAR
MRJEXEC/JIF ROC
WHEN ROC THEN BEX
B/CALL
GCSCHECK1-1=MPCR
RPTCHECK1-1=MPCR
S
S-CODE
AOP1: AOP0-1=AMPCR. AOP1-1=AMPCR. AOP2-1=AMPCR. AOP3-1=AMPCR
AOP4: AOP4-1=AMPCR. AOP5-1=AMPCR. AOP6-1=AMPCR. AOP7-1=AMPCR
SPBP CODE
AOP0: 0 EOL 0
IF FALSE THEN JUMP ELSE RETN
AOP1: 0 EOL 0
IF TRUE THEN JUMP ELSE RETN
AOP2: 0 EOL 0;IF NST THEN RETN
IF TRUE THEN JUMP ELSE RETN
AOP3: 0 0TR 0;IF NST THEN JUMP
IF TRUE THEN JUMP ELSE RETN
AOP4: RETN
AOP5: A3. IF NOT LST THEN JUMP ELSE RETN

```

```

1008CC00 0
10090000 0
10100C00 0
10110C00 0
10120C00 0
10130C00 0
10140C00 0
10150C00 0
10160C00 0
10170C00 0
10180C00 0
10190000 0
10200C00 0
10210C00 0
10220C00 0
10230000 0
10240C00 0
10250C00 0
10260C00 0
10270C00 0
10280C00 0
10290C00 0
10300C00 0
10310C00 0
10320C00 0
10330000 0
10340000 0
10350C00 0
10360C00 0
10370000 0
10380000 0
10390C00 0
10400C00 0
10410C00 0
10420C00 0
10430C00 0
10440C00 0
10450C00 0
10460C00 0
10470C00 0
10480C00 0
10490C00 0
10500C00 0
10510C00 0
10520C00 0
10530000 0
10540C00 0
10550C00 0
10560000 0
10570C00 0
10580C00 0
10590C00 0
10600C00 0
10610C00 0
10620C00 0
10630C00 0
10640C00 0
10650C00 0
10660C00 0

```

03A3	4009	6000	0000	00F0	A0P6:	A3.	IF LST THEN JUMP ELSE RETN	10670000	D
03A4	502F	0000	0000	00F0	A0P7:	RETN		10680000	D
03A5	403F	0000	0000	00F0	S			10690000	D
03A6	4009	6000	0000	00F0	ACMP0:	S	CHECK CONDITION BITS FOR TERMINATING REPEAT	10700000	D
03A7	0E10	0000	0000	00C0		A1+AMPCR=AMPCR	SA1=A-REG REFERENCED	10710000	D
03A8	0000	0000	0000	00C0		ACD-1=AMPCR		10720000	D
03A9	4009	6001	0000	00F0		COMP 1=8AR	SEOL IS LSB/0EO IS MSB/LIMITS 2ND MSB	10730000	D
03AA	4024	0000	0000	00F0		A2 C-A3		10750000	D
03AB	4036	0000	0000	00F0	EXEC	A3/CALL	SCALL CONDITION HANDLER	10760000	C
03AC	20F0	0000	0000	0040	0C2CHECK1-1=MPCR		STERMIMATE	10770000	C
03AD	2E50	0000	0000	0040	RPTCHECK1-1=MPCR			10780000	D
03AE					S-CODE			10790000	D
03B2					ACD:	ACD0-1=AMPCR, ACD1-1=AMPCR, ACD2-1=AMPCR, ACD3-1=AMPCR		10800000	D
						ACD4-1=AMPCR, ACD5-1=AMPCR, ACD6-1=AMPCR, ACD7-1=AMPCR		10810000	D
03B6	502F	0000	0000	00F0	SPOP CODE			10820000	D
03B7	502F	0000	0000	00F0	ACD0:	IF NOT LST THEN JUMP ELSE RETN		10830000	D
03B8	540F	0000	0000	00F0	ACD1:	IF LST THEN JUMP ELSE RETN		10840000	D
03B9	402F	0000	0000	00F0	ACD2:	IF NOT LST THEN A3/STEP ELSE RETN		10850000	D
03BA	402F	0000	0000	00F0	ACD3:	IF NOT LST THEN JUMP ELSE RETN		10860000	D
03BB	402F	0000	0000	00F0	ACD4:	IF NOT LST THEN JUMP ELSE RETN		10870000	D
03BC	540F	0000	0000	00F0	ACD5:	IF NOT LST THEN A3/STEP ELSE RETN		10880000	D
03BD	402F	0000	0000	00F0	ACD6:	IF NOT LST THEN JUMP ELSE RETN		10890000	D
03BE	4009	600A	0000	00F0	ACD7:	A3 0AD 0	STEST LIMITS BIT 2ND MSB	10900000	D
03BF	402F	0000	0000	00F0		IF NOT LST THEN JUMP ELSE RETN		10910000	D
03C0	4009	600A	0000	00F0		A3 0AD 0	STEST LIMITS BIT 2ND MSB	10920000	D
03C1	402F	0000	0000	00F0		IF NOT LST THEN JUMP ELSE RETN		10930000	D
03C2	4009	6041	0010	24F0	S	CONDCHK:		10940000	D
03C3	0000	0000	0000	00C0		AMPCR L=0R2/8AE	RETURN LC1->REPEATABLE	10950000	D
03C4	0009	E400	0000	00F0		COMP 0=8AR	SLC2 -> CHAR-ADDRESSABLE	10960000	D
03C5	0E10	0000	0000	00C0		A3+AMPCR=AMPCR	SSAVE RETURN ADDRESS IN BR2	10970000	D
03C6	2009	0C41	0000	00F0		CONDTABLE-1=AMPCR	SRETURN SAVED IN BR2;	10980000	D
03C7	0000	0000	0000	00C0		B C=0/IF LC1	SSET CONDITION CODE	11000000	D
03C8	3024	0000	0000	00F0	SETUPCD:	EXEC/IF LC2		11010000	D
03C9	4009	2640	0000	00F0		LIT+AMPCR=AMPCR	SSETUP TO EXECUTE CONDITIONS	11020000	D
03CA	0000	0000	0000	00C0		SETCOND-1=AMPCR	SSAVE SUBOPCODE IN CTR	11030000	D
03CB	0009	2C00	0000	00F0		LIT MAN 0=CTR		11040000	D
03CC	0020	0000	0000	0000		7=LIT/0=8AR		11050000	D
03CD	4020	0000	0000	00F0		JUMP	SEXECUTE SETCOND + VALUE IN TABLE	11060000	D
03CE	0000	0000	0000	00C0	SETCOND:	SPECCOND-1=AMPCR	S0=LIT-> 02 OR 03 CPCODE	11070000	D
03CF	09C9	0000	0000	00F0		SET LC1	S1=LIT R OR CA.	11080000	D
03D0	4030	0000	0000	00F0		SET LC2/SKIP	S2=LIT NOR P BUT CA	11090000	D
03D1	49C9	0000	0000	00F0		SET LC1	S3=LIT NOT CA BUT R	11100000	D
03D2	4009	0F00	0000	00F0	CONDEXIT:	0MAR R=AMPCR	S4=LIT NOT CA & NOT R	11110000	D
03D3	4009	0000	0000	00F0		0NI	SRESET B	11120000	D
03D4	4020	0000	0000	00F0		JUMP	SRETURN TO CALLING ROUTINE	11130000	D
03D5	4009	6640	0000	00F0	SPECCOND:		S MUST BE 02/03	11140000	D
03D6	0000	0000	0000	00C0		CTR+AMPCR=AMPCR		11150000	D
03D7	4009	E152	0000	00F0		SUBTABLE-1=AMPCR	SCHECK FOR 03	11160000	D
03D8	0000	0000	0000	00C0		A3 EOL LIT		11170000	D
03D9	6C00	2640	0000	00F0		3=LIT	IF TRUE THEN LIT+AMPCR=AMPCR/STEP ELSE SKIP	11180000	D
03DA	0000	0000	0000	00C0		0=LIT	S OFFSET PAST 02 CODES	11190000	D
03DB	4009	0000	0000	00F0		STEP		11200000	D
03DC	3C70	0000	0000	0040		SETUPCD-1=MPCR	S USE CODE FOR REGULAR OPCODES	11210000	D
					S-CODE			11220000	D
								11230000	D
								11240000	D
								11250000	D

```

0300 CONDTABLE: S9=NOT CA OR R23=NOT CA/R2=CA/NOT R21=CA/R20=C2 OR 03
0301 4=LIT, 3=LIT, 0=LIT, 0=LIT, 4=LIT, 4=LIT, 4=LIT, 4=LIT, 4=LIT, 1=LIT
0302 2=LIT, 1=LIT, 1=LIT, 1=LIT, 1=LIT, 1=LIT, 1=LIT, 1=LIT, 1=LIT, 1=LIT
0303 1=LIT, 1=LIT, 1=LIT, 2=LIT, 1=LIT, 1=LIT, 1=LIT, 4=LIT, 4=LIT, 3=LIT
0304 3=LIT, 1=LIT, 1=LIT, 1=LIT, 1=LIT, 1=LIT, 1=LIT, 3=LIT, 1=LIT, 1=LIT
0305 1=LIT, 1=LIT, 1=LIT, 1=LIT, 4=LIT, 4=LIT, 4=LIT, 4=LIT, 3=LIT, 1=LIT
0306 3=LIT, 3=LIT, 3=LIT, 4=LIT, 4=LIT, 4=LIT, 4=LIT, 4=LIT, 4=LIT, 4=LIT
0307 4=LIT, 4=LIT, 4=LIT, 4=LIT, 4=LIT, 4=LIT, 4=LIT, 4=LIT, 4=LIT, 4=LIT
0308 4=LIT
0309 SUBTABLE: SUSED FOR OPCODES C2 & 03
0310 1=LIT, 4=LIT, 4=LIT, 4=LIT, 1=LIT, 1=LIT, 1=LIT, 4=LIT, 4=LIT, 4=LIT
0311 3=LIT, 3=LIT, 1=LIT, 3=LIT, 1=LIT, 1=LIT, 1=LIT, 1=LIT, 3=LIT, 3=LIT
0312 SPOB CODE
0313 S *****
0314 S ***** LOGIC OPERATORS *****
0315 OPR01: Y2FETCH-1=CPCR
0316 GETF-1=CPCR
0317 A3+AMPCR=AMPCR
0318 OPR01XX-1=AMPCR
0319 A1 R=A3
0320 23=SAR7=LIT
0321 BMAR=A1
0322 A3 AND LIT=MAR
0323 B=A3/EXEC/MR1/IF RDC
0324 WHEN RDC THEN BEX/JUMP
0325 S ***** OPCODE 02 *****
0326 OPR02: Y2FETCH-1 = CPCR
0327 BMAR = MIR
0328 GETF-1=CPCR
0329 A3 + AMPCR = AMPCR
0330 OPR02XX-1 = AMPCR
0331 A1 R = A3
0332 23=SAR7=LIT
0333 A3 AND LIT = MAR; EXEC
0334 MR1/ IF RDC
0335 WHEN RDC THEN B=A3;BEX;JUMP S A(A3)>B;Y> A3
0336 S ***** REPLACE LOGICALS *****
0337 OPR03: GETF-1=CPCR
0338 7=LIT
0339 A3 EOL LIT; SET LC2
0340 OPR01-1=AMPCR
0341 IF FALSE THEN A3 EOL LIT;SET SF2=S=>SAME AS JCR01X7
0342 S=LIT
0343 IF TRUE THEN LIT L=0;STEP ELSE JUMP
0344 7=LIT;COMP 20=BAR
0345 A1 OR B=A1;JUMP
0346 S ***** DOUBLE WORD OPERATIONS *****
0347 OPR05: Y2FETCH-1=CPCR
0348 GETF-1=CPCR
0349 A3+AMPCR=AMPCR
0350 OPR05XX-1=AMPCR
0351 A1 R=A3
0352 7=LIT/23=BAR
0353 A3 AND LIT=A3;EXEC
0354 11260000 D
0355 11270000 D
0356 11280000 D
0357 11290000 D
0358 11300000 D
0359 11310000 D
0360 11320000 D
0361 11330000 D
0362 11340000 D
0363 11350000 D
0364 11360000 D
0365 11370000 D
0366 11380000 D
0367 11390000 D
0368 11400000 D
0369 11410000 D
0370 11420000 D
0371 11430000 D
0372 11440000 D
0373 11450000 D
0374 11460000 D
0375 11470000 D
0376 11480000 D
0377 11490000 D
0378 11500000 D
0379 11510000 D
0380 11520000 D
0381 11530000 D
0382 11540000 D
0383 11550000 D
0384 11560000 D
0385 11570000 D
0386 11580000 D
0387 11590000 C
0388 11600000 D
0389 11610000 D
0390 11620000 D
0391 11630000 D
0392 11640000 D
0393 11650000 D
0394 11660000 D
0395 11670000 D
0396 11680000 D
0397 11690000 D
0398 11700000 D
0399 11710000 D
0400 11720000 D
0401 11730000 D
0402 11740000 D
0403 11750000 D
0404 11760000 D
0405 11770000 D
0406 11780000 D
0407 11790000 D
0408 11800000 D
0409 11810000 D
0410 11820000 D
0411 11830000 D
0412 11840000 D
0413 11850000 D

```

```

0452 002D 0C4D 0030 00F0          0=MIR;JUMP          SMAR2=Y-ADDRMIR=(Y)
S ***** FLOATING POINT SUBROUTINES ***** 11060000 D
OPR06: UMNRITEN-1=MPCR          SPRINT ERROR AND RETURN TO IFETCH 11070000 D
S ***** EXTERNAL FUNCTION ***** 11080000 D
OPR07: Y2FETCH-1=CPCR          SB=ADDRESS OF Y+(B)+(LS) 11090000 D
SMAR=0          SRETURNS F2-FIELD IN A3 11900000 D
GETF-1=CPCR          SSETUPT FOR JUM 11910000 D
A3+AMPGR=AMPGR          SISLATE A FIELD 11920000 D
OPR07XX-1=AMPGR          11930000 C
A3 R=A3          11940000 D
7=LIT/23=SAR          11950000 D
A3 AND LIT=A3;EXEC          11960000 D
JUMP          11970000 D
S ***** LOAD A ***** 11980000 C
OPR10: YFETCH-1 = CPCR          S L A          12000000 D
GETAA3-1=CPCR          SPUTS PROPER INFO INTO MIR 12010000 D
OUTPUT-1=MPCR          SRETURNS A-FIELD IN A3&MAR 12020000 D
S ***** LOAD A AND INDEX 0 ***** 12030000 D
OPR11: YFETCH-1 = CPCR          S LXB          12040000 D
GETAA3-1=CPCR          S PUTS INFO INTO MIR 12050000 D
A1 R = A3;MIR;IF SAI          SRETURNS A-FIELD IN A3&MAR 12060000 D
I7 = SAR; 7 = LIT          S WRITE A-REG 12070000 D
A3 AND LIT = A3          S P-FIELD = A3 12080000 D
WHEN SAI THEN A3+LIT=MAR          12090000 D
BASE = LIT; 16 = SAR          12100000 C
MIR; IF RDC          12110000 D
WHEN RDC THEN BEX          12120000 D
YADDR=LIT          12130000 D
O + B + 1 = MIR          12140000 D
OUTPUT-1=MPCR          12150000 D
S ***** LOAD DIFFERENCE ***** 12160000 D
OPR12: YFETCH-1 = CPCR          SLDIF          12170000 D
GETAA3-1=CPCR          SRETURNS A-FIELD IN A3&MAR 12180000 D
MIR; IF RDC          12190000 D
WHEN RDC THEN A3 +1 = MAR,BEX S MAR = A+1 REG 12200000 D
B = A3;BHI          12210000 D
A3 = MIR          12220000 D
B = A3;BHI          12230000 D
A3 - B = A3;MIR          12240000 D
IF NOT ADV THEN A3-1=A3;MIR 12250000 D
IF NOT LC1 THEN SKIP          12260000 D
OPR36X1 -1 = MPCR          12270000 D
OUTPUT-1=MPCR          12280000 D
S ***** SUBTRACT A ***** 12290000 D
OPR13: YFETCH-1 = CPCR          S ANA          12300000 D
GETAA3-1=CPCR          SRETURNS A-FIELD IN A3&MAR 12310000 D
MIR; IF RDC          12320000 D
WHEN RDC THEN BEX          12330000 D
B = A3;BHI          12340000 D
A3 - B = A3;MIR          12350000 D
IF NOT ADV THEN A3-1=A3;MIR 12360000 D
OUTPUT-1=MPCR          12370000 D
S ***** ADD A ***** 12380000 D
OPR14:          ADD A S AA          12390000 D
          12400000 D
          12410000 D
          12420000 D
          12430000 D
          12440000 D
          12450000 D

```



```

0401 0C50 0000 0000 0000
0402 2400 0000 0000 0000
0403 0000 0000 0000 0000
0404 0A50 0000 0000 0000
0405 0000 0000 0000 0000
0406 0000 0000 0000 0000
0407 0000 0000 0000 0000
0408 0000 0000 0000 0000
0409 0000 0000 0000 0000
040A 0000 0000 0000 0000
040B 0000 0000 0000 0000
040C 0000 0000 0000 0000
040D 0000 0000 0000 0000
040E 0000 0000 0000 0000
040F 2400 0000 0000 0000
0410 0000 0000 0000 0000
0411 0000 0000 0000 0000
0412 0000 0000 0000 0000
0413 0000 0000 0000 0000
0414 0000 0000 0000 0000
0415 0000 0000 0000 0000
0416 0000 0000 0000 0000
0417 0000 0000 0000 0000
0418 0000 0000 0000 0000
0419 0000 0000 0000 0000
041A 0000 0000 0000 0000
041B 0000 0000 0000 0000
041C 0000 0000 0000 0000
041D 0000 0000 0000 0000
041E 0000 0000 0000 0000
041F 0000 0000 0000 0000
0420 0000 0000 0000 0000
0421 0000 0000 0000 0000
0422 0000 0000 0000 0000
0423 0000 0000 0000 0000
0424 0000 0000 0000 0000
0425 0000 0000 0000 0000
0426 0000 0000 0000 0000
0427 0000 0000 0000 0000
0428 0000 0000 0000 0000
0429 0000 0000 0000 0000
042A 0000 0000 0000 0000
042B 0000 0000 0000 0000
042C 0000 0000 0000 0000
042D 0000 0000 0000 0000
042E 0000 0000 0000 0000
042F 0000 0000 0000 0000
0430 0000 0000 0000 0000
0431 0000 0000 0000 0000
0432 0000 0000 0000 0000
0433 0000 0000 0000 0000
0434 0000 0000 0000 0000
0435 0000 0000 0000 0000
0436 0000 0000 0000 0000
0437 0000 0000 0000 0000
0438 0000 0000 0000 0000
0439 0000 0000 0000 0000
043A 0000 0000 0000 0000
043B 0000 0000 0000 0000
043C 0000 0000 0000 0000
043D 0000 0000 0000 0000
043E 0000 0000 0000 0000
043F 0000 0000 0000 0000
0440 0000 0000 0000 0000
0441 0000 0000 0000 0000
0442 0000 0000 0000 0000
0443 0000 0000 0000 0000
0444 0000 0000 0000 0000
0445 0000 0000 0000 0000
0446 0000 0000 0000 0000
0447 0000 0000 0000 0000
0448 0000 0000 0000 0000
0449 0000 0000 0000 0000
044A 0000 0000 0000 0000
044B 0000 0000 0000 0000
044C 0000 0000 0000 0000
044D 0000 0000 0000 0000
044E 0000 0000 0000 0000
044F 0000 0000 0000 0000
0450 0000 0000 0000 0000
0451 0000 0000 0000 0000
0452 0000 0000 0000 0000
0453 0000 0000 0000 0000
0454 0000 0000 0000 0000
0455 0000 0000 0000 0000
0456 0000 0000 0000 0000
0457 0000 0000 0000 0000
0458 0000 0000 0000 0000
0459 0000 0000 0000 0000
045A 0000 0000 0000 0000
045B 0000 0000 0000 0000
045C 0000 0000 0000 0000
045D 0000 0000 0000 0000
045E 0000 0000 0000 0000
045F 0000 0000 0000 0000
0460 0000 0000 0000 0000
0461 0000 0000 0000 0000
0462 0000 0000 0000 0000
0463 0000 0000 0000 0000
0464 0000 0000 0000 0000
0465 0000 0000 0000 0000
0466 0000 0000 0000 0000
0467 0000 0000 0000 0000
0468 0000 0000 0000 0000
0469 0000 0000 0000 0000
046A 0000 0000 0000 0000
046B 0000 0000 0000 0000
046C 0000 0000 0000 0000
046D 0000 0000 0000 0000
046E 0000 0000 0000 0000
046F 0000 0000 0000 0000
0470 0000 0000 0000 0000
0471 0000 0000 0000 0000
0472 0000 0000 0000 0000
0473 0000 0000 0000 0000
0474 0000 0000 0000 0000
0475 0000 0000 0000 0000
0476 0000 0000 0000 0000
0477 0000 0000 0000 0000
0478 0000 0000 0000 0000
0479 0000 0000 0000 0000
047A 0000 0000 0000 0000
047B 0000 0000 0000 0000
047C 0000 0000 0000 0000
047D 0000 0000 0000 0000
047E 0000 0000 0000 0000
047F 0000 0000 0000 0000
0480 0000 0000 0000 0000
0481 0000 0000 0000 0000
0482 0000 0000 0000 0000
0483 0000 0000 0000 0000
0484 0000 0000 0000 0000
0485 0000 0000 0000 0000
0486 0000 0000 0000 0000
0487 0000 0000 0000 0000
0488 0000 0000 0000 0000
0489 0000 0000 0000 0000
048A 0000 0000 0000 0000
048B 0000 0000 0000 0000
048C 0000 0000 0000 0000
048D 0000 0000 0000 0000
048E 0000 0000 0000 0000
048F 0000 0000 0000 0000
0490 0000 0000 0000 0000
0491 0000 0000 0000 0000
0492 0000 0000 0000 0000
0493 0000 0000 0000 0000
0494 0000 0000 0000 0000
0495 0000 0000 0000 0000
0496 0000 0000 0000 0000
0497 0000 0000 0000 0000
0498 0000 0000 0000 0000
0499 0000 0000 0000 0000
049A 0000 0000 0000 0000
049B 0000 0000 0000 0000
049C 0000 0000 0000 0000
049D 0000 0000 0000 0000
049E 0000 0000 0000 0000
049F 0000 0000 0000 0000
0500 0000 0000 0000 0000

```

```

0PR22:
YFETCH-1 = CPCR
GETAB-1=CPCR
NOT A3
IF FETCH-1=AMPCR
IF ABT THEN JUMP
A3 + LIT = MAR
BRASE = LIT, 16 = SAR
MRL1 IF ROC
WHEN ROC THEN GEX
B=A3,DNI
A3-B=MIR
IF NOT ADV THEN A3-B-1=MIR
OUTPUT-1=MPCR
STORE B
$ SB
0PR23:
A3 = MIR
GETAB-1=CPCR
NOT B
IF ABT THEN B000 = MIR ELSE SKIP
AZERO-1 = MPCR
LIT + B = MAR
BRASE=LIT,16=SAR
MRL1 IF ROC
WHEN ROC THEN GEX
B L = B
B R = MIR
AZERO: A3 = MAR
YSTORE-1 = MPCR
STORE A
$ SA
0PR24:
GETAB-1=CPCR
MRL1 IF ROC
WHEN ROC THEN GEX
B = MIR
YSTORE - 1 = MPCR
STORE A AND INDEX B
$ SXB
0PR25:
MRL1 IF ROC
WHEN ROC THEN GEX
B=A3,MIR
FETFORM-1 = CPCR
A1 R = B
7 = LIT, 17 = SAR
LIT AND B = B
LIT + B = MAR
BRASE = LIT
A1 R = B, MRL1 IF SAI
23 = SAR, 7 = LIT
WHEN SAI THEN LIT AND B = MAR $ A-REG
A3 = MIR, MRL1 IF ROC $ Y ADDR=> MIR
WHEN ROC THEN A1 R = A3,GEX $ A(A)=>B
20 = SAR
A3 AND LIT = A3
B = MIR, DNI
A3 + AMPCR = AMPCR
KSTABLE-1 = AMPCR
B = MAR2
EXEC, MRL1 IF ROC
JUMP

```

```

13060000 D
13070000 D
13080000 D
13090000 D
13100000 D
13110000 D
13120000 D
13130000 D
13140000 D
13150000 D
13160000 D
13170000 D
13180000 D
13190000 D
13200000 D
13210000 C
13220000 D
13230000 D
13240000 D
13250000 D
13260000 D
13270000 D
13280000 D
13290000 D
13300000 D
13310000 D
13320000 D
13330000 D
13340000 D
13350000 D
13360000 C
13370000 D
13380000 D
13390000 D
13400000 D
13410000 D
13420000 D
13430000 D
13440000 D
13450000 D
13460000 D
13470000 D
13480000 D
13490000 D
13500000 C
13510000 D
13520000 D
13530000 D
13540000 D
13550000 D
13560000 D
13570000 D
13580000 D
13590000 D
13600000 D
13610000 D
13620000 D
13630000 D
13640000 D
13650000 D

```

```

0465 2490 0000 0000 0060
0466 4009 0000 0000 0060
0467 4009 0000 0000 0060
0468 4009 0000 0000 0060
0469 4009 0000 0000 0060
0470 4009 0000 0000 0060
0471 4009 0000 0000 0060

0472 2490 0000 0000 0060
0473 4009 0000 0000 0060
0474 4009 0000 0000 0060
0475 4009 0000 0000 0060
0476 4009 0000 0000 0060
0477 4009 0000 0000 0060
0478 4009 0000 0000 0060
0479 4009 0000 0000 0060
0480 4009 0000 0000 0060
0481 4009 0000 0000 0060

0482 4909 0000 0000 0060
0483 4909 0000 0000 0060
0484 4909 0000 0000 0060
0485 4909 0000 0000 0060
0486 4909 0000 0000 0060
0487 4909 0000 0000 0060
0488 4909 0000 0000 0060
0489 4909 0000 0000 0060
0490 4909 0000 0000 0060
0491 4909 0000 0000 0060

0492 4909 0000 0000 0060
0493 4909 0000 0000 0060
0494 4909 0000 0000 0060
0495 4909 0000 0000 0060
0496 4909 0000 0000 0060
0497 4909 0000 0000 0060
0498 4909 0000 0000 0060
0499 4909 0000 0000 0060
0500 4909 0000 0000 0060
0501 4909 0000 0000 0060
0502 4909 0000 0000 0060
0503 4909 0000 0000 0060
0504 4909 0000 0000 0060
0505 4909 0000 0000 0060
0506 4909 0000 0000 0060
0507 4909 0000 0000 0060

0508 4909 0000 0000 0060
0509 4909 0000 0000 0060
0510 4909 0000 0000 0060
0511 4909 0000 0000 0060

```

```

S ***** STORE NEGATIVE *****
OPR26: *****
      GETAB-1=CPCR
      MRI1 IF RDC
      WHEN RDC THEN BEX
      NOT B = MIR
      YSTORE-1 = MPCR
S ***** STORE MAGNITUDE *****
OPR27: *****
      GETAB-1=CPCR
      MRI1 IF RDC
      WHEN RDC THEN BEX
      B = MIR
      IF NOT THEN NOT B = MIR
      A3 = MAR
      YSTORE-1 = MPCR
S ***** CLEAR BIT *****
OPR32: *****
      TAKE THE NUMBER IN AK FIELD, CLEAR THAT BIT IN Y
      YZFETCH-1=CPCR
      A1 L-A3
      COMP 6-SAR
      A3 B-A3
      26-SAR
      A3-SAR
      B C-A3,CSAR
      IF LC1 THEN A3 OR B001 C-MIRSKIP
      A3 AND B110 C-MIR
      YOUT-1=MPCR
S ***** SET BIT *****
OPR33: *****
      SAME CODE AS OPCODE 32 SO WILL USE THAT EXCEPT SET THE BIT
      SET LC1
      OPR32-1 = MPCR
S ***** REPLACE ADD *****
OPR34: *****
      YFETCH-1 = CPCR
      GETA3-1=CPCR
      A3 + 1 = A3,MIR1 IF RDC
      WHEN RDC THEN A3 AND LIT=MAR,BEX
      B-A3,BMI,SET LC2
      A3 + B = A3,MIR
      IF NOT THEN A3+1=A3,MIR
      IF NOT THEN B-A3,MIR
      OUTPUT1-1 = CPCR
      YSTORE-1 = MPCR
S ***** REPLACE INCREMENT *****
OPR35: *****
      YFETCH-1 = CPCR
      A3+1=MIR,SET LC2
      IF NOT THEN A3+1=MIR
      IF NOT THEN B-MIR
      GETAB-1=CPCR
      OUTPUT1-1 = CPCR
      YSTORE-1=MPCR
S ***** REPLACE SUBTRACT *****
OPR36: *****
      SET LC1
      OPR12-1 = MPCR
OPR36X1: OUTPUT1-1 = CPCR

```

```

1360000 D
1367000 C
1368000 C
1369000 D
1370000 D
1371000 D
1372000 D
1373000 D
1374000 D
1375000 D
1376000 D
1377000 D
1378000 D
1379000 D
1380000 D
1381000 D
1382000 D
1383000 D
1384000 D
1385000 D
1386000 D
1387000 D
1388000 D
1389000 D
1390000 D
1391000 D
1392000 D
1393000 D
1394000 D
1395000 D
1396000 D
1397000 D
1398000 D
1399000 D
1400000 D
1401000 D
1402000 C
1403000 D
1404000 C
1405000 D
1406000 D
1407000 D
1408000 D
1409000 D
1410000 D
1411000 C
1412000 D
1413000 D
1414000 D
1415000 C
1416000 D
1417000 D
1418000 D
1419000 D
1420000 D
1421000 D
1422000 D
1423000 D
1424000 D
1425000 D

```

```

0512 0849 0000 0000 00F0
0513 1550 0000 0000 0040

0514 06F0 0000 0000 0060
0515 2490 0000 0000 0060
0516 9009 E0DE 0000 00F0
0517 7409 E000 0000 00F0
0518 2300 0000 0000 0060
0519 1550 0000 0000 0040

051A 06F0 0000 0000 0060
051B 2270 0000 0000 0060
051C 2490 0000 0000 0060
051D 9009 E0C0 2000 00F0
051E AC08 0000 0000 00F0
051F 2900 0000 0000 0060
0520 9009 E000 0000 00F0
0521 9009 0000 0000 10F0
0522 9008 0F46 0000 00F0
0523 9009 A000 0000 00F0
0524 9009 0000 0000 10F0
0525 9008 0000 0000 00F0
0526 0A50 0000 0000 0060
0527 22AC 0000 0000 0040

0528 06F0 0000 0000 0060
0529 2270 0000 0000 0060
052A 9009 E0C0 0000 00F0
052B 2400 0000 0000 0060
052C 9009 E0C0 0000 00F0
052D 9009 2F56 0000 00F0
052E 9009 0000 0000 00F0
052F AC08 E000 0000 00F0
0530 9009 0C48 1000 00F0
0531 2A00 0000 0000 0060
0532 9009 C0C0 0000 00F0
0533 C009 0000 0000 00F0
0534 9009 0000 0000 10F0
0535 9008 0F46 0000 00F0
0536 9009 2F56 0000 00F0
0537 0070 0000 0000 00E0
0538 9009 A000 0000 00F0
0539 C009 A002 0000 00F0
053A 9009 0000 0000 10F0
053B 9008 0000 0000 00F0
053C 22A0 0000 0000 0060
053D 9009 C001 A000 00F0
053E 9008 0000 0000 0030
053F 2C19 0010 AC00 00F0
0540 9009 000F A000 00F0
0541 0A50 0000 0000 0040

0542 1270 0000 0000 0060
0543 9009 0C48 1000 00F0
0544 9009 A000 0000 00F0
0545 03F0 0000 0000 0040

```

```

SIGNALS REPEAT
REPLACE DECREMENT
S RD
SRETURNS A-FIELD IN 06MAR
S A(A)-1 => A(A)
MULTIPLY A(A)Y = A(A+1),A(A)
SA3=(Y)
SSAVE A2
SB, MAR=A-FIELD
SA2=(Y)
SA1=H05T, SA3=LEAST
SOUTPUT LEAST
SOUTPUT MOST
SRESTORE A2, RETURN TO IFETCH
DIVIDE A(A+1) & A(A) / Y=>A(A+1) + A(A)
SHIR-DIVISOR
SSAVE A2
SMIT-DIVISOR=(Y)
SA3=A ADDRESS
SCONVERT A(0) TO A(0)
SREAD A+1
SBAR SETUP FOR LEAST DIVIDEND
SA3-DIVIDEND/9-DIVISOR
SRETURNS A2=QUOTIENT, A1=REMAINDER
SSETUP TO OUTPUT QUOTIENT
SOUTPUT QUOTIENT
SCONVERT A(0) TO A(0)
SOUTPUT REMAINDER
SRESTORE A2
COMP 3=BAR
IF LC1 THEN A2 OR B100 C-A2, SKIP
A2 AND 0011 C-A2
IFETCH-1=MPCR
COMPARE BIT TO ZERO
SBC
SGET (Y) INTO E
SCHECK BIT IN A3=(Y)
SOPR37:
SET LC2
YSTORE - 1 = MPCR
YFETCH-1=CPCR
GETAB-1=CPCR
A3-1=MIR
IF NOT ABY THEN A3-1-1=MIR
OUTPUT1 - 1 = CPCR
YSTORE - 1 = MPCR
MULTIPLY A(A)Y = A(A+1),A(A)
YFETCH-1=CPCR
PUTPAR-1=CPCR
GETAB-1=CPCR
A3=A2/MR2/IF RDC
WHEN RDC THEN BEX
MULTIPLY-1=CPCR
A3=MIR
MVI, IF SAI
WHEN SAI THEN SBAR+1=MAR
A1=MIR
MVI, IF SAI
WHEN SAI THEN 0/STEP
IFETCH-1=MPCR
GETPAR-1=MPCR
SOPR41:
SDIVIDE A1 & A3 / B -A1(QUOTIENT) + A3(REMAINDER)
YFETCH-1=CPCR
PUTPAR-1=CPCR
A3=MIR
GETA3-1=CPCR
A3+1=MAR
LIT AND SBAR=MAR
MVI, IF RDC
WHEN RDC THEN A3=MAR, BEX
B-A3, 26M1
DIVIDE-1=CPCR
A2=MIR
IF ABT THEN 0=MIR
MVI, IF SAI
WHEN SAI THEN SBAR+1=MAR
LIT AND SBAR=MAR
7=LIT
A1=MIR
IF ABT THEN NOT A1=MIR
MVI, IF SAI
WHEN SAI THEN 0/STEP
GETPAR-1=CPCR
A2 C-A2, C=BAR
COMP 3=BAR
IF LC1 THEN A2 OR B100 C-A2, SKIP
A2 AND 0011 C-A2
IFETCH-1=MPCR
COMPARE BIT TO ZERO
SBC
SGET (Y) INTO E
SCHECK BIT IN A3=(Y)
SOPR42:
Y2FETCH-1=CPCR
B=A3
A1 R=B
63=LIT, 20=BAR

```

```

14260000 D
14270000 D
14280000 D
14290000 D
14300000 D
14310000 D
14320000 D
14330000 D
14340000 D
14350000 D
14360000 D
14370000 D
14380000 D
14390000 D
14400000 D
14410000 D
14420000 D
14430000 D
14440000 D
14450000 D
14460000 D
14470000 D
14480000 D
14490000 D
14500000 D
14510000 D
14520000 D
14530000 D
14540000 D
14550000 D
14560000 D
14570000 D
14580000 D
14590000 D
14600000 D
14610000 D
14620000 D
14630000 D
14640000 D
14650000 D
14660000 D
14670000 D
14680000 D
14690000 D
14700000 D
14710000 D
14720000 D
14730000 D
14740000 D
14750000 D
14760000 D
14770000 D
14780000 D
14790000 D
14800000 D
14810000 D
14820000 D
14830000 D
14840000 D
14850000 D

```

```

0546 0007 2C56 0000 00F0
0547 0009 E0C0 9000 00F0
0548 0009 E000 0000 00F0
0549 5C19 D4CE 200C 00F0
054A 0009 D01C 2020 00F0
054B 0A50 0000 0C90 C040

054C 0CFC 0000 0020 0060
054D 2490 0000 0000 0060
054E 4009 0C52 0000 00F0
054F 6019 0000 0000 00FC
0550 0A50 0000 0020 0040
0551 4009 2C40 002C 00F0
0552 0000 0000 0000 00A0
0553 8009 C001 A600 00F0
0554 A000 0000 0020 0030
0555 AC00 0000 0000 00F0
0556 4009 0C40 1000 40F0
0557 4009 E0C0 0000 C0F0
0558 8049 EC4C 0000 00F0
0559 400B EC5E 0000 00F0
055A 770B 00C0 0030 00F0
055B 7FC9 00C0 0030 00F0
055C 2C19 001D A000 00F0
055D 4009 000F A000 00F0
055E 22F0 0000 0000 0040

055F 0CF0 0000 0000 0060
0560 2490 0000 0000 0060
0561 90C9 E000 0000 00F0
0562 A000 0000 0000 00F0
0563 AC00 0000 0000 00F0
0564 4009 0C40 103C C0F0
0565 206C 00C0 0000 0040

0566 0CF0 00C0 0000 0060
0567 2490 0000 0000 0060
0568 A009 0000 0030 00F0
0569 0A50 0000 002C 00C0
056A AC00 0F4C 0C3C 00F0
056B 4009 2F5C 000C 00F0
056C A009 0C40 4000 00F0
056D AFC0 0000 0020 00F0
056E 8049 0C40 1000 00F0
056F 4009 A000 0030 00F0
0570 0F10 0000 0020 0040

0571 0CF0 0000 0020 0060
0572 2490 0000 0000 0060
0573 A009 0000 0020 00F0
0574 AFC0 0F4C 0C3C 00F0
0575 4009 2F5C 000C 00F0
0576 A009 EC5E 1000 00F0
0577 AC00 0000 0000 00F0

```

```

LIT AND B=BAR
A3 R=A3
A3 SET LC2
IF LST THEN A2 AND B011 = A2/SKIP
A2 OR B100=A2
IFETCH-1=MPCR
S *****
OPR43:
YFETCH-1=CPCR
GETAB-1=CPCR
O EOL 0
IF FALSE THEN SKIP
IFETCH-1=MPCR
LIT=B=BAR
BASE=LIT/16=SAR
A2 C=A2/MR1; IF RDC
CMP 2=BAR
WHEN RDC THEN BEX
B=A3; BHI; C=BAR
A3+1=MIR
A3 XOR B/SET LC2
SKIP; IF FALSE THEN 0=MIR/SET LC1
A3 GE0 B; IF M57 THEN STEP ELSE SKIP
IF TRUE THEN 0=MIR/SET LC1
IF LC1 THEN A2 OR B100 C=A2/SKIP
A2 AND B011 C=A2
OUTPUT-1=MPCR
S *****
OPR44:
YFETCH-1=CPCR
GETAB-1=CPCR
A3=MIR/SET LC1
MIR; IF RDC
WHEN RDC THEN BEX
B=A3; BHI
SETCOMPARE-1=MPCR
S *****
OPR45:
IF Y BETWEEN (ACA) AND (ACA+1) OR = (ACA) THEN CD WITHIN LIMITS
ELSE OUTSIDE OF LIMITS
YFETCH-1 = CPCR
GETAB-1=CPCR
MIR; IF RDC
IFETCH-1=MPCR
WHEN RDC THEN B=BAR+1=MAR; BEX
LIT AND B=BAR=MAR
B=A1/MR1; IF RDC
WHEN RDC THEN BEX/SET LC1
B=A3/SET LC2
A1=MIR; BHI
OPR74X15-1=MPCR
S *****
OPR46:
YFETCH-1 = CPCR
GETAB-1=CPCR
MIR; IF RDC
WHEN RDC THEN B=BAR+1=MAR; BEX/SET LC1
LIT AND B=BAR=MAR
A3 AND B = A3; MIR/MR1; IF RDC
WHEN RDC THEN BEX
S *****
OPR47:
SAR FIELD IS SHIFT AMOUNT
SBIT TO COMPARE IS LS
CHECK LSB; SIGNAL REPEAT WITH LC2
A2/SKIP
SET EQUAL CONDITION BIT IN ASR
S *****
OPR48:
COMPARE INDEX INCREMENT
SCHI
BY VALUE =A3; MIR
RETURNS A-FIELD IN B=BAR
STEP FOR B(0) => MOOP IF TRUE
S *****
OPR49:
B(A) ADDRESS
SGET LIMITS BIT TO MSB
SREAD B(A)
S(A3;B(A)); B=(A)
INCREMENT B(A) THEN TEST B(A)>>A(A)
STEP FOR UNLIKE SIGNAL REPEAT
S *****
OPR50:
COMPARE
SC
BY VALUE = A3; MIR
RETURNS A-FIELD IN B=BAR
S *****
OPR51:
S(A)
S(A) =A3; Y=>B
S(A) =A(A); B=(Y)
COMPARE LIMITS
S CL
S *****
OPR52:
IF Y BETWEEN (ACA) AND (ACA+1) OR = (ACA) THEN CD WITHIN LIMITS
ELSE OUTSIDE OF LIMITS
Y VALUE => A3; MIR
RETURNS A-FIELD IN B=BAR
S *****
OPR53:
SUSE IDENTICAL CODE IN OPR74X5
WHEN RDC THEN B=BAR+1=MAR; BEX
CONVERT A(0) TO A(0)
S(A) =A(A)
S(A) =A(A+1); SIGNAL REPEAT
MIR=A(A); B=(Y)
S *****
OPR54:
COMPARE MASKED
S CH
BY VALUE => A3; MIR
RETURNS A-FIELD IN B=BAR
S *****
OPR55:
YFETCH-1 = CPCR
MIR; IF RDC
WHEN RDC THEN B=BAR+1=MAR; BEX/SET LC1
LIT AND B=BAR=MAR
A3 AND B = A3; MIR/MR1; IF RDC
WHEN RDC THEN BEX
S *****
OPR56:
S *****
OPR57:
S *****
OPR58:
S *****
OPR59:
S *****
OPR60:
S *****
OPR61:
S *****
OPR62:
S *****
OPR63:
S *****
OPR64:
S *****
OPR65:
S *****
OPR66:
S *****
OPR67:
S *****
OPR68:
S *****
OPR69:
S *****
OPR70:
S *****
OPR71:
S *****
OPR72:
S *****
OPR73:
S *****
OPR74:
S *****
OPR75:
S *****
OPR76:
S *****
OPR77:
S *****
OPR78:
S *****
OPR79:
S *****
OPR80:
S *****
OPR81:
S *****
OPR82:
S *****
OPR83:
S *****
OPR84:
S *****
OPR85:
S *****
OPR86:
S *****
OPR87:
S *****
OPR88:
S *****
OPR89:
S *****
OPR90:
S *****
OPR91:
S *****
OPR92:
S *****
OPR93:
S *****
OPR94:
S *****
OPR95:
S *****
OPR96:
S *****
OPR97:
S *****
OPR98:
S *****
OPR99:
S *****
OPR100:
S *****

```


05A7	24F0	0000	0000	0000	0060
05A8	4809	E640	0000	0000	00F0
05A9	0000	0000	0000	0000	00C0
05AA	4809	A000	9000	9000	00F0
05AB	3070	0000	0000	0000	00A0
05AC	4824	E156	0000	0000	00F0
05AD	4820	0F40	1000	0000	00F0
05AE	1270	0000	0000	0000	0060
05AF	4809	0C40	0000	0000	00F0
05B0	4809	A0C1	1000	0000	00F0
05B1	2000	0000	0000	0000	0030
05B2	A809	E800	9000	9000	00C0
05B3	2400	0000	0000	0000	00B0
05B4	3009	E140	1000	0000	00F0
05B5	2520	0000	0000	0000	0060
05B6	2019	0000	0000	0000	00F0
05B7	22F0	0000	0000	0000	00A0
05B8	2210	0000	0000	0000	00A0
05B9	1270	0000	0000	0000	0060
05BA	49C9	0000	0000	0000	00F0
05BB	4849	0000	0000	0000	00F0
05BC	5A00	0000	0000	0000	00A0
05BD	1270	0000	0000	0000	0060
05BE	4809	0F40	0000	0000	00F0
05BF	4809	A0C1	1000	0000	00F0
05C0	2000	0000	0000	0000	0030
05C1	A809	E800	9000	9000	00C0
05C2	2400	0000	0000	0000	00B0
05C3	3009	E140	1000	0000	00F0
05C4	2520	0000	0000	0000	0060
05C5	2E19	0000	0000	0000	00F0
05C6	2210	0000	0000	0000	00A0
05C7	AC00	0C40	0C10	0000	00F0
05C8	4809	0C40	0000	0000	00F0
05C9	2370	0000	0000	0000	00A0
05CA	1270	0000	0000	0000	0060
05CB	49C9	0000	0000	0000	00F0
05CC	4809	0000	0000	0000	00F0
05CD	5B00	0000	0000	0000	00A0
05CE	4809	A0C1	1000	0000	00F0
05CF	2000	0000	0000	0000	0030
05D0	4809	E800	9000	0000	00F0
05D1	A000	0000	0000	0000	0020
05D2	4809	E800	0000	0000	00F0
05D3	8400	0000	0000	0000	00B0
05D4	5F09	2F40	0000	0000	00F0
05D5	2520	0000	0000	0000	0060
05D6	A809	E156	9000	0000	00F0
05D7	10E0	0000	0000	0000	00B0
05D8	AC00	E000	0C00	0000	00F0
16060000	D				
16070000	D				
16080000	D				
16090000	D				
16100000	D				
16110000	D				
16120000	D				
16130000	D				
16140000	D				
16150000	D				
16160000	D				
16170000	D				
16180000	D				
16190000	D				
16200000	D				
16210000	D				
16220000	D				
16230000	D				
16240000	D				
16250000	D				
16260000	D				
16270000	D				
16280000	D				
16290000	D				
16300000	D				
16310000	D				
16320000	D				
16330000	D				
16340000	D				
16350000	D				
16360000	D				
16370000	D				
16380000	D				
16390000	D				
16400000	D				
16410000	D				
16420000	D				
16430000	D				
16440000	D				
16450000	D				
16460000	D				
16470000	D				
16480000	D				
16490000	D				
16500000	D				
16510000	D				
16520000	D				
16530000	D				
16540000	D				
16550000	D				
16560000	D				
16570000	D				
16580000	D				
16590000	D				
16600000	D				
16610000	D				
16620000	D				
16630000	D				
16640000	D				
16650000	D				

```

0587 4009 0C40 0000 00F0
0588 2019 0000 0C00 00F0
0589 0000 0000 003C 0040
0590 0000 0000 0000 0040

0591 4009 0001 1030 00F0
0592 2000 0000 0030 003C
0593 4009 0000 0000 00F0
0594 0000 0000 0000 0000
0595 4009 0000 0000 0000
0596 0000 0000 0000 0000
0597 0000 0000 0000 0000
0598 0000 0000 0000 0000
0599 0000 0000 0000 0000
0600 0000 0000 0000 0000
0601 0000 0000 0000 0000
0602 0000 0000 0000 0000
0603 0000 0000 0000 0000
0604 0000 0000 0000 0000
0605 0000 0000 0000 0000
0606 0000 0000 0000 0000
0607 0000 0000 0000 0000

0608 2600 0000 0000 0060
0609 4009 0000 0000 40F0
0610 0000 0000 0000 0040

0611 2600 0000 0000 0060
0612 4009 0C40 1000 00F0
0613 4009 0019 0000 40F0
0614 4009 0F46 0000 00F0
0615 4009 2F56 0000 00F0
0616 0070 0000 0000 00E0
0617 4009 0C56 8000 00F0
0618 4009 0001 1000 00F0
0619 4009 0C40 0C00 00F0
0620 2019 0000 0000 00F0
0621 0F20 0000 0000 0040
0622 9009 0C40 8000 10F0
0623 9C08 0B02 803C 00F0
0624 0000 0000 0000 003C
0625 4009 0C5C 0000 00F0
0626 0000 0000 0000 0040
0627 4009 0C40 8000 00F0
0628 0000 0000 0000 00F0
0629 0000 0000 0000 00F0
0630 0000 0000 0000 00F0
0631 0000 0000 0000 00F0
0632 0000 0000 0000 00F0
0633 0000 0000 0000 00F0
0634 0000 0000 0000 00F0
0635 0000 0000 0000 00F0
0636 0000 0000 0000 00F0
0637 0000 0000 0000 00F0

0638 2600 0000 0000 0060
0639 4009 0C40 8000 00F0
0640 0000 0000 0000 0040

```

```

B=MIR
IF LC1 THEN SKIP
ILLEGALCHR1-1=MPCR
HALFFETCH-1=MPCR
*****
OPR61: SIF 1-1 THEN OFFSET BY 100 OCTAL
*****
A1 L=A3
COMP 6=5AR
A3 R=A3
22=5AR14=LIT
A3 AND LIT R=MAR
1=5AR14=LIT
MIR IF RDC
WHEN RDC THEN A3 R=A3,MAR,BEX
9=5AR14=LIT
IF LST THEN A3+LIT=A3,MAR,SET LC1
B=MIR
CHECKCHR-1=CPCR
IF LC1 THEN SKIP
ILLEGALCHR1-1=MPCR
HALFFETCH-1=MPCR
*****
OPR62: SHIFT AMOUNT IN 5AR18=(A),MAR= ADDR OF A-REG
*****
CSAR
B C=MIR
HALFFETCH-1=MPCR
*****
OPR63:
*****
SSAMPLE INPUT A+1=ZZWU, A=XXYY; OUTPUT A+1=WXXX A=YYZZ
SHIFTAMOUNT-1=CPCR
B=A3
B11 L=B,CSAR
BMAR+1=MAR
LIT AND BMAR=MAR
7=LIT
A3 AND B R=MIR;MIR1 IF RDC
WHEN RDC THEN A3 L=A3,BEX
B L=801
B=MIR,BEX
IF NOT LC1 THEN SKIP
OPR63XX-1=MPCR
B R=B,MV1 IF SAI
WHEN SAI THEN NOT CTR R=MAR
24=5AR
A3 OR B=MIR
HALFFETCH-1=MPCR
B R=B
OPR63XX: A3 OR B=MIR,BMI
MIR IF SAI
WHEN SAI THEN B=MIR
NOT CTR R=MAR
24=5AR
HALFFETCH-1=MPCR
*****
OPR64: SSAR=SHIFT AMOUNT;B=(A),MAR=A ADDRESS
*****
SHIFTAMOUNT-1=CPCR
B R=MIR
HALFFETCH-1=MPCR
*****
SHIFT RIGHT OBL/FILL ZEROS
SHAR=A-REG ADDRESS
SHIFT RIGHT OBL/FILL ZEROS
*****

```

```

16660000 D
16670000 D
16680000 D
16690000 D
16700000 D
16710000 D
16720000 D
16730000 D
16740000 D
16750000 D
16760000 D
16770000 D
16780000 D
16790000 D
16800000 D
16810000 D
16820000 D
16830000 D
16840000 D
16850000 D
16860000 D
16870000 D
16880000 D
16890000 D
16900000 D
16910000 D
16920000 D
16930000 D
16940000 D
16950000 D
16960000 D
16970000 D
16980000 D
16990000 D
17000000 D
17010000 D
17020000 D
17030000 D
17040000 D
17050000 D
17060000 D
17070000 D
17080000 D
17090000 D
17100000 D
17110000 D
17120000 D
17130000 D
17140000 D
17150000 D
17160000 D
17170000 D
17180000 D
17190000 D
17200000 D
17210000 D
17220000 D
17230000 D
17240000 D
17250000 D

```

```

0600 2600 0000 0000 0000 0060
0601 4009 0F46 0C9C 00F0
0602 4009 2F56 00DC 00F0
0603 0070 0000 0000 00E0
0604 2019 0000 0000 00F0
0605 0F3C 0000 0000 0040
0606 4009 0C40 9000 00F0
0607 4008 0000 0000 00F0
0608 4009 0C40 8C9C 00F0
0609 4009 0C41 0830 18F0
0610 9E08 EC5C 0090 20F0
0611 4009 08C2 800C 00F0
0612 0000 0000 0000 0030
0613 080C 0000 0000 0040
0614 4009 0000 0090 00F0
0615 4008 0000 0030 00F0
0616 4009 0000 0090 18F0
0617 9C08 0C40 8090 00F0
0618 4009 0802 803C 00F0
0619 0000 0000 0070 0030
0620 0800 0000 0070 0030
0621 2600 0000 0000 0060
0622 4009 0C40 8080 40F0
0623 0800 0000 7090 00C0
0624 400D 0019 0F00 00F0
0625 402D 0C40 0090 00F0
0626 2600 0000 0000 0060
0627 4009 0F46 009C 00F0
0628 007C 0000 0000 00E0
0629 2019 0000 0000 00F0
0630 0F40 0000 0000 0040
0631 4009 0C40 9C00 00F0
0632 4008 0000 0000 00F0
0633 4009 0C40 8090 00F0
0634 4008 0000 0000 00F0
0635 4008 0000 0000 00F0
0636 4008 0000 1C00 00F0
0637 4009 0C40 8080 00F0
0638 4C08 0002 1000 00F0
0639 4018 0019 0F00 00F0
0640 4009 0000 0090 00F0
0641 4009 5000 0000 00F0
0642 4009 0000 0000 18F0
0643 9C08 0C40 809C 00F0
0644 0800 0000 0070 0030
0645 4008 0000 0000 0030
0646 4008 0000 0000 0030
0647 4008 0000 0000 0030
0648 4008 0000 0000 0030
0649 4008 0000 0000 0030
0650 4008 0000 0000 0030
0651 4008 0000 0000 0030
0652 4008 0000 0000 0030
0653 4008 0000 0000 0030
0654 4008 0000 0000 0030
0655 4008 0000 0000 0030
0656 4008 0000 0000 0030
0657 4008 0000 0000 0030
0658 4008 0000 0000 0030
0659 4008 0000 0000 0030
0660 4008 0000 0000 0030
0661 4008 0000 0000 0030
0662 4008 0000 0000 0030
0663 4008 0000 0000 0030
0664 4008 0000 0000 0030
0665 4008 0000 0000 0030
0666 4008 0000 0000 0030
0667 4008 0000 0000 0030
0668 4008 0000 0000 0030
0669 4008 0000 0000 0030
0670 4008 0000 0000 0030
0671 4008 0000 0000 0030
0672 4008 0000 0000 0030
0673 4008 0000 0000 0030
0674 4008 0000 0000 0030
0675 4008 0000 0000 0030
0676 4008 0000 0000 0030
0677 4008 0000 0000 0030
0678 4008 0000 0000 0030
0679 4008 0000 0000 0030
0680 4008 0000 0000 0030
0681 4008 0000 0000 0030
0682 4008 0000 0000 0030
0683 4008 0000 0000 0030
0684 4008 0000 0000 0030
0685 4008 0000 0000 0030
0686 4008 0000 0000 0030
0687 4008 0000 0000 0030
0688 4008 0000 0000 0030
0689 4008 0000 0000 0030
0690 4008 0000 0000 0030
0691 4008 0000 0000 0030
0692 4008 0000 0000 0030
0693 4008 0000 0000 0030
0694 4008 0000 0000 0030
0695 4008 0000 0000 0030
0696 4008 0000 0000 0030
0697 4008 0000 0000 0030
0698 4008 0000 0000 0030
0699 4008 0000 0000 0030
0700 4008 0000 0000 0030

```

```

SEEXAMPLE INPUT A+1=ZZNW, A=XXYY, DUPUT A+1=00ZZ, A=WWXX
SHIFTAMOUNT-1=CPCR
B MAR+1=MAR
LIT AND B MAR=MAR
7=LIT
IF NOT LC1 THEN SKIP
OPR65XX-1=MPCR
B R=A3/MR1/IF RDC
WHEN RDC THEN BEX
B R=MIR/BEX
B L=B/MR1/IF SAI
WHEN SAI THEN A3 OR B=MIR/ASR
NOT CTR R=MAR
24=SAR
HALFFETCH-1=MPCR
OPR65XX: 0=MIR/MR1/IF RDC
WHEN RDC THEN BEX
MVI/IF SAI
WHEN SAI THEN B R=MIR
NOT CTR R=MAR
24=SAR
HALFFETCH-1=MPCR
*****
OPR66: SSAR=SHIFT AMOUNT, MAR=AIREG ADDR, B=(A)
B R=MIR/CSAR
HALFFETCH-1=AMPCR
IF MST THEN B111 L=BBI/STEP ELSE JUMP
B=MIR/JUMP
*****
SHIFT RIGHT SIGN FILL *****
SSAR SET FOR SIGN 1 EXTENSION
*****
SHIFT RIGHT DBLE/FILL SIGN *****
SEEXAMPLE INPUT A+1=ZZNW, A=XXYY, OUTAUT=A+1=00ZZ, A=WWXX
SHIFTAMOUNT-1=CPCR
B MAR+1=MAR
LIT AND B MAR=MAR
7=LIT
IF NOT LC1 THEN SKIP
OPR67XX-1=MPCR
B R=A3/MR1/IF RDC
WHEN RDC THEN BEX
B R=MIR
IF MST THEN B111 L=BBI/STEP ELSE SKIP
B=MIR/BEX
B L=B/MR1/IF SAI
WHEN SAI THEN A3 OR B=MIR/ASR
NOT CTR R=MAR
24=SAR
HALFFETCH-1=MPCR
OPR67XX: SB=(A)/SAR=SHIFT-32
MVI/IF RDC
WHEN RDC THEN 0=A3/BEX
B R=MIR
IF MST THEN NOT 0=A3/STEP ELSE SKIP
B111 L=BBI/SKIP
B MI
MVI/IF SAI
WHEN SAI THEN NOT CTR R=MAR

```

```

17260000 D
17270000 D
17280000 D
17290000 D
17300000 C
17310000 D
17320000 D
17330000 D
17340000 D
17350000 D
17360000 D
17370000 D
17380000 D
17390000 D
17400000 D
17410000 D
17420000 D
17430000 D
17440000 D
17450000 D
17460000 D
17470000 D
17480000 D
17490000 C
17500000 D
17510000 D
17520000 D
17530000 D
17540000 D
17550000 D
17560000 D
17570000 D
17580000 D
17590000 D
17600000 D
17610000 D
17620000 D
17630000 D
17640000 D
17650000 D
17660000 D
17670000 D
17680000 D
17690000 D
17700000 D
17710000 D
17720000 D
17730000 D
17740000 D
17750000 D
17760000 D
17770000 D
17780000 D
17790000 C
17800000 D
17810000 D
17820000 D
17830000 D
17840000 D
17850000 D

```



```

0684 2410 0000 0000 0040          OUTLOGIC-1-MPCR          COUNT ONES          19060000 D
OPRO2X0: A3 = B          S Y->A3, A(A)>=>B          19070000 D
COUNTONES-1-CPCR          19080000 D
OUTPUT-1 = MPCR          19090000 D
OPRO2X1: A3=B          EXECUTE REMOTE          19100000 D
IFETCHREMOTE-1-MPCR          S Y VALUE => A3          19110000 D
LIT AND AMPCR=AMPCR          S REMOTE INSTR. SETUP FOR IFETCH          19120000 C
A3 L=A1          SLET IFETCH EXECUTE          19130000 D
16 = SAR          EXECUTE REMOTE LOWER          19140000 D
A2 C=0,C8AR1EXEC          S AS = Y VALUE          19150000 D
20=SAR          SSETUP OPCODE          19160000 D
BTI C=A2/JUMP          SSET LOWER HALF BIT ON          19170000 D
OPRO2X4: A(A+1) AND Y => Y          19180000 D
S(A(A))>B, Y ADDR => MIR          19190000 D
S(A(A+1))          19200000 D
S A(A+1)          19210000 D
S A(A+1)          19220000 D
S A(A+1)          19230000 D
S A(A+1)          19240000 D
S A(A+1)          19250000 C
S A(A+1)          19260000 D
S A(A+1)          19270000 D
S A(A+1)          19280000 D
S A(A+1)          19290000 D
S A(A+1)          19300000 D
S A(A+1)          19310000 D
S A(A+1)          19320000 D
S A(A+1)          19330000 D
S A(A+1)          19340000 D
S A(A+1)          19350000 D
S A(A+1)          19360000 D
S A(A+1)          19370000 D
S A(A+1)          19380000 D
S A(A+1)          19390000 D
S A(A+1)          19400000 D
S A(A+1)          19410000 D
S A(A+1)          19420000 D
S A(A+1)          19430000 D
S A(A+1)          19440000 D
S A(A+1)          19450000 D
S A(A+1)          19460000 D
S A(A+1)          19470000 D
S A(A+1)          19480000 D
S A(A+1)          19490000 D
S A(A+1)          19500000 D
S A(A+1)          19510000 D
S A(A+1)          19520000 D
S A(A+1)          19530000 D
S A(A+1)          19540000 D
S A(A+1)          19550000 D
S A(A+1)          19560000 D
S A(A+1)          19570000 D
S A(A+1)          19580000 D
S A(A+1)          19590000 D
S A(A+1)          19600000 D
S A(A+1)          19610000 D
S A(A+1)          19620000 D
S A(A+1)          19630000 D
S A(A+1)          19640000 D
S A(A+1)          19650000 D

```

66C2	8809	0C49	0038	0CFC	B=MR,MR1,IF RDC	SMIR=A(A);B=Y-ADDR	19660C00	D
66C3	AC08	0C43	0C1C	08F0	WHEN RDC THEN B=MR2,BEX	SB=(A(A+1));MR2=Y	19670C00	D
66C4	9809	08C8	0838	1CF0	MR2,IF SAI		19680C00	D
66C5	9C08	0F46	081C	08F0	WHEN EAT THEN BMR=1=MR2		19690C00	D
66C6	8809	0C48	0C38	08F0	B=MR	SSETUP A+1 FOR OUTPUT	19700C00	D
66C7	2328	0008	0008	0840	OUTPUT=RET-1=MPCR	TEST ANC SET FLAG *****	19710C00	C
66C8	127C	0808	0808	0860	Y2FETCH-1=CPCR	SOMAR=YADDRESS;B=(Y)	19720C00	D
66C9	8809	0C48	0838	08F0	B	STEST MOST SIGNIFICANT BIT	19730C00	C
66CA	9419	1C48	0838	08F0	IF NOT MST THEN B11T=MR1/SKIP		19740C00	D
66CB	0F6C	0808	0808	0840	OPRO3X7-1=MPCR		19750C00	D
66CC	9809	0808	0808	1CF0	MR2,IF SAI		19760C00	D
66CD	9C18	081C	2C08	08F0	WHEN SAI THEN A2 OR B100=A2;SKIP		19770C00	D
66CE	8809	080E	2C38	08F0	IFETCH-1=MPCR		19780C00	D
66CF	045C	0808	0808	0840	S *****	DOUBLE LOAD A *****	19790C00	D
66D0	8809	0F46	081C	08F0	OPRO5X0: SMIR=(Y);MR2=YADDR		19800C00	D
66D1	8809	0808	0808	0CFC	BMR=1=MR2	SREAD Y+1	19810C00	D
66D2	AC08	0808	0C3C	08F0	MR2,IF RDC		19820C00	D
66D3	8809	0808	0808	18F0	WHEN RDC THEN A3=MR,MR2,BEX	SAB=A-ADDRESS	19830C00	D
66D4	9C08	08C8	083C	08F0	MR1,IF RDC	SWRITE Y	19840C00	D
66D5	8809	2F56	083C	08F0	WHEN SAI THEN A3+1=MR	SCONVERT A(0) TO A(0)	19850C00	D
66D6	8809	0C48	0C38	08F0	LIT AND BMR=MR		19860C00	D
66D7	22F8	0808	0808	0840	B=MR		19870C00	D
66D8	8809	0F46	081C	08F0	OUTPUT-1=MPCR	SWRITE Y+1	19880C00	D
66D9	8809	0C48	4008	0CFC	S *****	DOUBLE ADD *****	19890C00	D
66DA	AC08	0808	0C3C	08F0	OPRO5X1: SA3=A-ADDRESS;MR2=Y-ADDRESS;MR=Y		19900C00	D
66DB	8809	0C48	4008	08F0	BMR=1=MR2,BMI	SA1=(Y)	19910C00	D
66DC	AC08	0808	0C3C	08F0	B=A1,MR2,IF RDC		19920C00	D
66DD	8809	0C48	1008	08F0	WHEN RDC THEN A3=MR,MR2,BEX	SA3=(Y+1)	19930C00	D
66DE	8809	0C48	4038	08F0	B=A3,MR1,IF RDC	SB=(A)	19940C00	D
66DF	8809	0F46	083C	08F0	WHEN RDC THEN BEX	SA3=A+Y	19950C00	D
66E0	8809	0F46	083C	08F0	A1+B=A1,MR	SA3=A+Y	19960C00	D
66E1	8809	0808	0808	08F0	BMR=0,IF A0Y THEN SET LCI TEST FOR CARRY		19970C00	D
66E2	AC08	0C48	0C3C	08F0	BMR=1=MR	SCONVERT A(0) TO A(0)	19980C00	D
66E3	2C19	EC48	1038	08F0	LIT AND BMR = MAR		19990C00	D
66E4	8809	EC48	1038	08F0	MR1,IF RDC		20000C00	D
66E5	7C09	ADC8	4038	08F0	WHEN RDC THEN B=MR,MR2,BEX		20010C00	D
66E6	8809	E8C2	0808	08F0	IF LCI THEN A3+B+1=A3;SKIP SADD CARRY		20020C00	D
66E7	6C08	A002	0808	08F0	A3+B=A3		20030C00	D
66E8	6C09	0808	5038	08F0	NOT A3		20040C00	D
66E9	9809	0808	0838	18F0	IF A0Y THEN A1+1=A1,MR	SADD CARRY	20050C00	D
66EA	9C08	0F46	083C	08F0	IF A0Y THEN NOT A1;STEP ELSE SKIP		20060C00	D
66EB	8809	E808	0838	08F0	IF A0Y THEN B=A1,A3,MR	SOUTPUT A+Y	20070C00	D
66EC	8809	2F56	083C	08F0	MR1,IF SAI		20080C00	D
66ED	8809	E808	0838	08F0	WHEN SAI THEN BMR=1=MR	SCONVERT A(0) TO A(0)	20090C00	D
66EE	8809	E808	0838	08F0	LIT AND BMR=MR		20100C00	D
66EF	8809	E808	0838	08F0	AS=MR		20110C00	D
66F0	22F8	08C8	083C	0840	OUTPUT-1=MPCR	SOUTPUT (A+1)+(Y+1)	20120C00	D
66F1	8809	0F46	081C	08F0	S *****	DOUBLE SUBTRACT (A+1,A)-(Y+1,Y)->A+1,A *****	20130C00	D
66F2	8809	0C48	4008	0CFC	OPRO5X2: SA3=A-ADDR;MR2=Y-ADDR;MR=(Y)		20140C00	D
66F3	AC08	E8C8	0C3C	08F0	BMR=1=MR2,BMI	SB=(Y)	20150C00	D
66F4	8809	0C48	4008	08F0	B=A1,MR2,IF RDC	SA1=(Y)	20160C00	C
66F5	8809	2F56	083C	08F0	WHEN RDC THEN A3+1=MR,MR2,BEX	SCONVERT A(0) TO A(0)	20170C00	D
66F6	8809	0C48	4008	08F0	LIT AND BMR=MR		20180C00	D
66F7	AC08	E8C8	0C3C	08F0	B=MR,MR1,IF RDC	SMIR=(Y+1);READ A+1	20190C00	D
66F8	8809	E808	0838	08F0	WHEN RDC THEN A3=MR,MR2,BEX	SB=(A+1)	20200C00	D
66F9	8809	0C48	1038	08F0	B=A3,BMI	SA3=(A+1)	20210C00	D
66FA	8809	EC5E	1038	08F0	A3=B=A3;MR1,IF RDC	SA3=(A+1)-(Y+1)	20220C00	D
66FB	8809	0C48	4008	08F0			20230C00	D
66FC	8809	0C48	4008	08F0			20240C00	D
66FD	8809	0C48	4008	08F0			20250C00	D
66FE	8809	0C48	4008	08F0			20260C00	D
66FF	8809	0C48	4008	08F0			20270C00	D

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06F6 73C9 0000 0000 00F0
06F7 4C08 A000 0C30 00F0
06F8 8009 0C40 4000 00F0
06F9 2C19 AC50 4030 00F0
06FA 8009 AC5E 4030 00F0
06FB 7408 E00E 1000 00F0
06FC 7409 A00E 4030 00F0
06FD 9009 0003 0C80 10F0
06FE 9C08 0F46 000C 00F0
06FF 8009 2F56 000C 00F0
0700 4009 E0C0 0030 00F0
0701 22FC 0000 0C00 0040

0702 8009 0F46 001C 00F0
0703 8009 C0C1 A000 0CFC
0704 000C 00C0 0000 0030
0705 8009 0C40 4000 00F0
0706 AC08 E0C0 0C0C 00F0
0707 8009 0C40 1000 00F0
0708 AC08 0F46 0C0C 00F0
0709 8009 2F56 000C 00F0
070A 8009 AC52 0000 00F0
070B 8009 AC4C 0000 00F0
070C 0A50 0000 0000 00C0
070D 8008 AC5E 0000 40F0
070E 7449 00C0 0000 00F0
070F 7249 0003 0030 00F0
0710 AC08 00C0 0C30 00F0
0711 8009 EC52 0000 00F0
0712 4A08 C0CE 2000 00F0
0713 0F70 0000 0030 0040
0714 2C08 C0DC 2030 00F0
0715 082D 081D A000 00F0
0716 3C19 081C 2030 00F0
0717 4009 000E 2030 00F0
0718 082D C0CF A000 00F0

0719 4009 EC4C 0000 00F0
071A 4019 EC5E 0000 00FC
071B 7429 081D A000 00F0
071C 7C29 081D A000 00F0
071D 082D 000F A000 00F0

071E 2240 0000 0030 0040

071F 8000 0000 0080 00F0
0720 0A50 0000 0030 0040

0721 800C 0000 0080 00F0
0722 0A50 0000 0080 0040

0723 8000 0000 0080 00F0
0724 0A50 0000 0080 0040

1456 2C26 0C00 0
2C27 0C00 0
2C28 0C00 0
2C29 0C00 0
2C30 0C00 0
2C31 0C00 0
2C32 0C00 0
2C33 0C00 0
2C34 0C00 0
2C35 0C00 0
2C36 0C00 0
2C37 0C00 0
2C38 0C00 0
2C39 0C00 0
2C40 0C00 0
2C41 0C00 0
2C42 0C00 0
2C43 0C00 0
2C44 0C00 0
2C45 0C00 0
2C46 0C00 0
2C47 0C00 0
2C48 0C00 0
2C49 0C00 0
2C50 0C00 0
2C51 0C00 0
2C52 0C00 0
2C53 0C00 0
2C54 0C00 0
2C55 0C00 0
2C56 0C00 0
2C57 0C00 0
2C58 0C00 0
2C59 0C00 0
2C60 0C00 0
2C61 0C00 0
2C62 0C00 0
2C63 0C00 0
2C64 0C00 0
2C65 0C00 0
2C66 0C00 0
2C67 0C00 0
2C68 0C00 0
2C69 0C00 0
2C70 0C00 0
2C71 0C00 0
2C72 0C00 0
2C73 0C00 0
2C74 0C00 0
2C75 0C00 0
2C76 0C00 0
2C77 0C00 0
2C78 0C00 0
2C79 0C00 0
2C80 0C00 0
2C81 0C00 0
2C82 0C00 0
2C83 0C00 0
2C84 0C00 0
2C85 0C00 0

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0725 4000 0000 0000 0000
0726 0A50 0000 0000 0000
0727 4000 0000 0000 0000
0728 0A50 0000 0000 0000
0729 4000 0000 0000 0000
072A 0A50 0000 0000 0000
072B 4000 0000 0000 0000
072C 0A50 0000 0000 0000
072D 4000 0000 0000 0000
072E 0A50 0000 0000 0000
072F 2240 0000 0000 0000
0730 2240 0000 0000 0000
0731 2240 0000 0000 0000
0732 2240 0000 0000 0000
0733 4009 0012 0000 0000
0734 6000 0000 0000 0000
0735 1F00 0000 0000 0000
0736 4009 0002 0000 0000
0737 6000 0000 0000 0000
0738 1F00 0000 0000 0000
0739 1F00 0000 0000 0000
073A 2240 0000 0000 0000
073B 4009 0000 0000 0000
073C 0000 0000 0000 0000
073D 4009 0000 0000 0000
073E AC00 0000 0000 0000
073F 4009 0042 0000 0000
0740 6000 0000 0000 0000
0741 0A50 0000 0000 0000
0742 4009 0040 1000 0000
0743 4009 0000 0000 0000
0744 2300 0000 0000 0000
0745 4009 0000 0000 0000
0746 4009 0000 0000 0000
0747 AC00 0000 0000 0000
0748 0100 0000 0000 0000
0749 2300 0000 0000 0000
074A 4009 0046 0000 0000

S *****
OPROG14: WAIT IFETCH-1-MPCR
S *****
OPROG15: WAIT IFETCH-1-MPCR
S *****
OPROG16: WAIT IFETCH-1-MPCR
S *****
OPROG17: WAIT IFETCH-1-MPCR
S *****
OPROG18: UNWRITTEN-1-MPCR
S *****
OPROG19: UNWRITTEN-1-MPCR
S *****
OPROG20: UNWRITTEN-1-MPCR
S *****
OPROG21: UNWRITTEN-1-MPCR
S *****
OPROG22: UNWRITTEN-1-MPCR
S *****
OPROG23: UNWRITTEN-1-MPCR
S *****
OPROG24: AS EOL 0
IF TRUE THEN STEP ELSE SKIP
CARDREAD-1-MPCR
AS EOL 1
IF TRUE THEN STEP ELSE SKIP
PRINTLINE-1-MPCR
DISKREAD-1-MPCR
S *****
OPROG25: UNWRITTEN-1-MPCR
S *****
OPROG26: LMAR/RESET GC2
15 = LIT
MR1; IF RDC
WHEN RDC THEN BEX
NOT 0
IF ABT THEN A2 + 1 = A2 ELSE SKIP
IFETCH-1 = MPCR
0 = A3
A3-1 = MIR
OUTPUT1-1 = CPCR
A2 = MAR2
MR2; IF RDC
WHEN RDC THEN A1=MIR,LMAR,BEX BREAD N.I.
RINST=LIT
OUTPUT1-1 = CPCR
SMAR + 1 = MAR

WAIT IFETCH-1-MPCR
FLOATING POINT ADD/ROUND
WAIT IFETCH-1-MPCR
FLOATING POINT SUBR/ROUND
WAIT IFETCH-1-MPCR
FLOATING POINT MULT/ROUND
WAIT IFETCH-1-MPCR
FLOATING POINT DIV/ROUND
S *****
OPROG27: WAIT IFETCH-1-MPCR
INTERPROCESSOR INTERRUPT
S *****
OPROG28: UNWRITTEN-1-MPCR
SPRINT ERROR AND RETURN TO IFETCH
ALLOW ENABLE INTERRUPT
S *****
OPROG29: UNWRITTEN-1-MPCR
SPRINT ERROR AND RETURN TO IFETCH
PREVENT ENABLE INTERRUPT
S *****
OPROG30: UNWRITTEN-1-MPCR
SPRINT ERROR AND RETURN TO IFETCH
LOAD IOC MONITOR CLOCK
S *****
OPROG31: UNWRITTEN-1-MPCR
SPRINT ERROR AND RETURN TO IFETCH
I/O ROUTINES
S *****
OPROG32: UNWRITTEN-1-MPCR
SPRINT ERROR AND RETURN TO IFETCH
REPEAT S RP
S *****
OPROG33: LMAR/RESET GC2
15 = LIT
MR1; IF RDC
WHEN RDC THEN BEX
NOT 0
IF ABT THEN A2 + 1 = A2 ELSE SKIP
IFETCH-1 = MPCR
0 = A3
A3-1 = MIR
OUTPUT1-1 = CPCR
A2 = MAR2
MR2; IF RDC
WHEN RDC THEN A1=MIR,LMAR,BEX BREAD N.I.
RINST=LIT
OUTPUT1-1 = CPCR
SMAR + 1 = MAR

20660000 0
20670000 0
20680000 0
20690000 0
20700000 0
20710000 0
20720000 0
20730000 0
20740000 0
20750000 0
20760000 0
20770000 0
20780000 0
20790000 0
20800000 0
20810000 0
20820000 0
20830000 0
20840000 0
20850000 0
20860000 0
20870000 0
20880000 0
20890000 0
20900000 0
20910000 0
20920000 0
20930000 0
20940000 0
20950000 0
20960000 0
20970000 0
20980000 0
20990000 0
21000000 0
21010000 0
21020000 0
21030000 0
21040000 0
21050000 0
21060000 0
21070000 0
21080000 0
21090000 0
21100000 0
21110000 0
21120000 0
21130000 0
21140000 0
21150000 0
21160000 0
21170000 0
21180000 0
21190000 0
21200000 0
21210000 0
21220000 0
21230000 0
21240000 0
21250000 0
21260000 0
21270000 0
21280000 0
21290000 0
21300000 0
21310000 0
21320000 0
21330000 0
21340000 0
21350000 0
21360000 0
21370000 0
21380000 0
21390000 0
21400000 0
21410000 0
21420000 0
21430000 0
21440000 0
21450000 0

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0740 4009 0C50 0000 00F0
074C 230C 0000 0000 0060
074D 4009 0C50 9000 00F0
074E 2000 0000 0000 0030
074F 3C1C 0000 0000 0060
0750 2E99 0001 A000 40F0
0751 0A0C 0000 0000 C040
0752 7000 0000 0000 0020
0753 1000 0000 0000 00F0
0754 4009 0000 A000 C0F0
0755 3000 0000 0030 0060
0756 01AC 0000 0030 0040

0757 4009 0C50 1000 00F0
0758 AC00 0000 0C20 00F0
0759 4009 EC56 0000 00F0
075A 292C 0000 0000 0060
075B 4009 E000 0000 00F0
075C 5019 0000 0000 C0F0
075D 230B 0000 0030 00F0
075E 2009 0000 0030 00F0
075F 0A50 0000 0000 C040
0760 4009 A000 1000 00F0
0761 2660 0000 0000 0040

0762 49C9 0000 0000 C0F0
0763 756C 0000 0000 0040

0764 4009 0C52 0000 00F0
0765 6019 0000 0000 C0F0
0766 AC00 0000 0C30 00F0
0767 4009 0C52 0000 00F0
0768 6A99 0000 0000 00F0
0769 3019 0000 0000 00F0
076A 200B 0000 0000 00F0
076B 2309 0000 0030 00F0
076C 0A50 0000 0030 C040
076D 4009 A000 1000 00F0
076E 2660 0000 0000 0040

076F 49C9 0000 0000 00F0
0770 7630 0000 0000 0040

0771 4009 0C50 0030 00F0
0772 43C9 0000 0000 00F0
0773 2660 0000 0030 0040

0774 4009 0C52 0000 00F0
0775 7700 0000 0030 0040

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```

0 - MR, A1
OUTPUT1-1 = CPCR
0 R = A3
26 = SAR
CNDCHECK-1 = CPCR
IF LC1 THEN A2 C = A2; C; SAR; SET GC2; SKIP
IFETCH1-1 = NPCR
21 = SAR
SET GC2; WHEN GC2 THEN STEP
A2 OR 0001 C = A2
S; YFETCH-1 = CPCR
IFETCH1-1 = NPCR
***** JUMP ON EVEN PARITY *****
OPR50X0: SA1-Y-ADDRESS; A3=A(A)
B=A3; MR1; IF RDC
WHEN RDC THEN BEX
A3 AND B=B
C; COUNTONES-1=CPCR
A3
IF LST THEN SKIP
IF NOT LC1 THEN SET LC1; STEP ELSE SKIP
IF LC1 THEN SET LC1; SKIP
IFETCH-1=MPCR
A1=A3
PUTJUMP-1=MPCR
SIF 000(LST) AND NOT LC1(OPR50X0) => NO JUMP
SIF 000(LST) AND LC1(OPR50X1) => JUMP; SET LC1 FOR PUTJUMP
***** JUMP ON ODD PARITY *****
OPR50X1: SET LC1
OPR50X0-1=MPCR
***** JUMP IF A(A) AND A(A+1) EQUAL ZERO *****
OPR50X2: SA1-JUMP ADDRESS; B=(A(A)); MAR=A+1 ADDRESS
S; TEST A(A) FOR 0
IF EOL 0; MR1; IF RDC
WHEN RDC THEN BEX
0 EOL B
IF TRUE THEN SET LC2
IF LC2 THEN SKIP
IF LC1 THEN STEP ELSE SKIP
IF NOT LC1 THEN SET LC1; SKIP
IFETCH-1=MPCR
A1=A3
PUTJUMP-1=MPCR
SIF A(A) AND A(A+1) = 0 AND OPR50X2 => JUMP
SIF A(A) AND A(A+1) = 0 AND OPR50X3 => NO JUMP
***** JUMP IF A(A) OR A(A+1) NOT EQUAL ZERO *****
OPR50X3: SUSES SAME ROUTINES AS OPR50X2 WITH LC1 SET
SET LC1
OPR50X2-1=MPCR
***** JUMP (A) POSITIVE *****
OPR51X0: SB=(A)
IF NOT MST THEN SET LC1
PUTJUMP-1=MPCR
***** JUMP (A) NEGATIVE *****
OPR51X1: NOT B=B
OPR51X0-1=MPCR
***** SSAME AS 51X0 EXCEPT COMPLEMENT B *****
***** JUMP (A) ZERO *****

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21460000 0
21470000 0
21480000 0
21490000 0
21500000 0
21510000 0
21520000 0
21530000 0
21540000 0
21550000 0
21560000 0
21570000 0
21580000 0
21590000 0
21600000 0
21610000 0
21620000 0
21630000 0
21640000 0
21650000 0
21660000 0
21670000 0
21680000 0
21690000 0
21700000 0
21710000 0
21720000 0
21730000 0
21740000 0
21750000 0
21760000 0
21770000 0
21780000 0
21790000 0
21800000 0
21810000 0
21820000 0
21830000 0
21840000 0
21850000 0
21860000 0
21870000 0
21880000 0
21890000 0
21900000 0
21910000 0
21920000 0
21930000 0
21940000 0
21950000 0
21960000 0
21970000 0
21980000 0
21990000 0
22000000 0
22010000 0
22020000 0
22030000 0
22040000 0
22050000 0

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0776 4009 0C42 0000 00F0
0777 60C9 0000 0000 00F0
0778 266C 0000 0C30 0040

0779 4009 0C42 0020 00F0
077A 63C9 0000 0C90 00F0
077B 2660 0000 0030 0040

077C 4009 4012 0000 00F0
077D 67D9 0000 0030 00F0
077E 0A50 0000 0000 0040
077F 2300 0000 0000 0060
0780 266C 0000 0000 0040

0781 4009 4012 0020 00F0
0782 6400 0C42 0000 00F0
0783 67D9 0C40 4030 00F0
0784 0A50 0000 0000 0040
0785 4009 400E 0000 00F0
0786 2300 0000 0030 00F0
0787 266C 0000 0000 0040

0788 4009 4001 1000 00F0
0789 0000 0000 0000 00A0
078A 4009 2C30 003C 00F0
078B 4009 0000 9000 00F0
078C 4000 0000 0C30 00F0
078D 49C9 EC40 1000 00F0
078E 2660 0000 0000 0040

078F 4009 0003 0C1C 00F0
0790 4009 0000 4000 4C00
0791 03F0 0000 0000 00A0
0792 4000 0000 2C00 00F0
0793 4009 0C41 0000 00F0
0794 2000 0000 0000 0010
0795 4009 4150 0040 00F0
0796 4009 0C41 0C30 00F0
0797 0000 0000 0000 0020
0798 4024 CF5C 2000 00F0
0799 402D C0C0 2000 00F0

079A 4009 0C32 0000 00F0
079B 63C9 C0C1 4000 40F0
079C 9000 0000 0000 0030
079D 266C 0000 0000 00C0
079E 4009 0000 0000 00F0
079F 4010 000F 4000 00F0
07A0 23ED 0000 0030 00F0
07A1 20ED 0000 0030 00F0

22060000 0
22070000 0
22080000 0
22090000 0
22100000 0
22110000 0
22120000 0
22130000 0
22140000 0
22150000 0
22160000 0
22170000 0
22180000 0
22190000 0
22200000 0
22210000 0
22220000 0
22230000 0
22240000 0
22250000 0
22260000 0
22270000 0
22280000 0
22290000 0
22300000 0
22310000 0
22320000 0
22330000 0
22340000 0
22350000 0
22360000 0
22370000 0
22380000 0
22390000 0
22400000 0
22410000 0
22420000 0
22430000 0
22440000 0
22450000 0
22460000 0
22470000 0
22480000 0
22490000 0
22500000 0
22510000 0
22520000 0
22530000 0
22540000 0
22550000 0
22560000 0
22570000 0
22580000 0
22590000 0
22600000 0
22610000 0
22620000 0
22630000 0
22640000 0
22650000 0

OPR51X2: NOT B
IF ABT THEN SET LC1
PUTJUMP-1=MPCR
S ***** JUMP (A) NOT ZERO *****
OPR51X3: NOT B
IF NOT ABT THEN SET LC1
PUTJUMP-1=MPCR
S ***** LOAD E AND JUMP *****
OPR52X0: A1 EOL 0
IF FALSE THEN A2=MIR;SET LC1;SKIP SMAR1=ADDR OF B(A)
IFETCH-1=MPCR
OUTPUT1-1=CPCR
PUTJUMP-1=MPCR
S ***** INDEX JUMP B *****
OPR52X1: A1 EOL 0
IF FALSE THEN NOT B;STEP ELSE SKIP
IFETCH-1=MPCR
A1-1=MIR
OUTPUT1-1=CPCR
PUTJUMP-1=MPCR
S ***** JUMP SY+B *****
OPR52X2: A1 L-A3,BMI
16=SA;B;BASE=LIT
LIT+B=MAR
A3 R-A3;MIR;IF RDC
WHEN RDC THEN BEX
A3+B=A3;SET LC1
PUTJUMP-1=MPCR
S ***** UNCONDITIONAL JUMP LOWER *****
OPR52X3: A3=MAR2
A2 R=A2;CSAR;MR2;IF RDC
20=SA;R;63=LIT
WHEN RDC THEN A2 OR 8001 L-A2;BEX
B C=A1
10=SA R
A1 AND LIT=AMP CR
B C=A1
16=SA R
A2 OR SMAR=A2;EXEC
A2+1=A2;JUMP
S ***** JUMP OVERFLOW AND A *****
OPR53X0: 0 EOL 0
A2 C = A2;CSAR; IF FALSE THEN SET LC1
COMP 3=SA R
PUTJUMP-1 = AMP CR
A2 AND 8011 C = A2; IF NOT THEN SKIP
IF NOT LC1 THEN SET LC1; JUMP ELSE JUMP
IF LC1 THEN SET LC1; JUMP ELSE JUMP
S JUMP IF A=0 AND NO OVERFLOW OR A=1 AND OVERFLOW
JUMP ON CD EQUAL/UNEQUAL/LIMITS
S ***** SB= A-FILED; A3=JUMP ADDRESS *****
OPR53X1:

```

```

0742 4009 0C40 4000 00F0
0743 4009 4C40 0040 00F0
0744 3A00 0000 0000 00C0
0745 4009 0000 0000 00F0
0746 4024 0001 0000 00F0
0747 3000 0000 0000 0030
0748 4036 0000 0000 00FC
0749 4908 0F40 1000 00F0
074A 0A50 0000 0030 0040
074B 2660 0000 0000 0040

074C 4009 0C40 4000 00F0
074D 0500 0000 0000 00E0
074E 4009 415E 0C00 00F0
074F 0040 0000 0000 00E0
0750 78C9 0000 0005 00F0
0751 4C08 4002 0C00 00F0
0752 68C9 0000 0000 00F0
0753 4009 0C40 0000 00F0
0754 4009 0C40 0030 00F0
0755 58C9 0000 0000 00F0
0756 2F09 415E 0000 00F0
0757 0A50 0000 0030 0040
0758 7001 0000 0000 00F0
0759 4009 0001 4000 00F0
075A 0100 0000 0000 0040
075B 4012 0000 0030 00F0
075C 4009 0000 0030 00F0
075D 4C08 0000 0000 00F0
075E 4009 4C50 0000 00F0
075F 4429 0F46 000E 00F0
0760 4009 0003 001C 00F0
0761 4009 6009 0000 00C0
0762 3000 0000 0000 0010
0763 4C08 4C50 4C00 00F0
0764 0000 0000 0030 0020
0765 4009 0C40 0000 00F0
0766 4009 4C50 0000 00F0
0767 4009 0000 1000 00F0
0768 2660 0000 0030 00C0
0769 4009 0000 000C 1C00
076A 9C20 0000 0000 00F0

076B 4009 0C40 4000 00FC
076C 0500 0000 0000 00E0
076D 4009 415E 0030 00F0
076E 0040 0000 0030 00E0
076F 78C1 4002 0000 00F0
0770 68C9 0000 0030 00F0
0771 4C08 0000 0030 00F0
0772 4009 0C40 0000 00F0
0773 4009 0C40 0030 00F0
0774 58C9 0000 0000 00F0
0775 0A50 0000 0000 0040
0776 2660 0000 0000 0040

```

```

B = A1
A1=AMPCR=AMPCR
ACD=1=AMPCR
STEP
A2 C=A3JEXEC
31 = SAR
A3CALL
BMR = A3; SET LC1; SKIP
IFETCH=1=AMPCR
PUTJUMP=1=AMPCR
S *****
OPR53X2: B=SAR,A1,LMAR
SWITCH -LIT
A1 GEO LIT/MR1,IF RDC
4=LIT
0=CTR; IF TRUE THEN SET LC1
WHEN RDC THEN NOT A1,DEX
IF NOT THEN SET LC1
B R=0
IF LST THEN SET LC1
IF LC1 THEN A1 GEO LIT/SET LC1/SKIP
IFETCH=1=AMPCR
IF TRUE THEN WAIT
A2 L=A3,LMAR,CSAR
SBASE=LIT/COMP 12=SAR
A1 R=A1,MR1/SAVE
MR1/IF RDC
WHEN RDC THEN DEX
A1 R=MR1,DMI
IF NOT MST THEN BMR+1=MAR,INCJUMP
A3=MR2
11=SAR
WHEN RDC THEN A1 OR B L=A1,DEX
COMP 16=SAR
B R=0
A1 OR B C=MR
A3 + 1=A3
PUTJUMP=1=AMPCR
MV2/IF SAI
WHEN SAI THEN 0/JUMP
S *****
OPR53X3: B=SAR,A1,LMAR
SWITCH -LIT
A1 GEO LIT/MR1,IF RDC
4=LIT
NOT A1; IF TRUE THEN WAIT/SET LC1
IF NOT THEN SET LC1
WHEN RDC THEN DEX
B R=0
IF LST THEN SET LC1
IF LC1 THEN SET LC1/SKIP
IFETCH=1=AMPCR
PUTJUMP=1=AMPCR
S *****
OPR70X0:

```

```

22660000 D
22670000 D
22680000 D
22690000 D
22700000 D
22710000 D
22720000 D
22730000 D
22740000 D
22750000 D
22760000 D
22770000 D
22780000 D
22790000 D
22800000 D
22810000 D
22820000 D
22830000 D
22840000 D
22850000 D
22860000 D
22870000 D
22880000 D
22890000 D
22900000 D
22910000 D
22920000 D
22930000 D
22940000 D
22950000 D
22960000 D
22970000 D
22980000 D
22990000 D
23000000 D
23010000 D
23020000 D
23030000 D
23040000 D
23050000 D
23060000 D
23070000 D
23080000 D
23090000 D
23100000 D
23110000 D
23120000 D
23130000 D
23140000 D
23150000 D
23160000 D
23170000 D
23180000 D
23190000 D
23200000 D
23210000 D
23220000 D
23230000 D
23240000 D
23250000 D

```

```

0700 2250 0000 0050 0040          UNWRITTEM4-1=MPCR          SPRINT ERROR & RETURN TO HALFFETCH 23260000 0
S ***** DOUBLE SCALE FACTOR ***** 23270000 0
0PR70X1:
0709 225C 0000 0050 0040          UNWRITTEM4-1=MPCR          SPRINT ERROR & RETURN TO HALFFETCH 23290000 0
S ***** COMPLEMENT A ***** 23300000 0
0PR70X2:
070A 4009 0C42 0050 00FC          NOT 0=MIR                  23310000 0
070B 000C 0000 0000 0040          HALFFETCH-1=MPCR          23320000 0
S ***** DOUBLE COMPLEMENT A ***** 23330000 0
0PR70X3:  SB=(A)MAR=A-ADDRESS  SCOMPLEMENT A          23340000 0
070C 4009 0C42 0050 00FC          NOT 0=MIR                  23360000 0
070D 9009 0000 0050 10F0          MW1 IF SAI                 23370000 0
070E 9C08 0F46 000C 00F0          WHEN SAI THEN BMAR+1=MAR  23380000 0
070F 4009 2F56 000C 00F0          LIT AND BMAR=MAR          23390000 0
07E0 4009 0000 0000 00F0          MR1 IF RDC                  23400000 0
07E1 AC08 0000 0C50 00F0          WHEN RDC THEN BEX         23410000 0
07E2 4009 0C42 0050 00F0          NOT 0=MIR                  23420000 0
07E3 0000 0000 0050 0040          HALFFETCH-1=MPCR          23430000 0
S ***** MULTIPLY REGISTERS A X A+1 ***** 23440000 0
0PR74X0:  SB=A-FIELD;A3=6-FIELD  SSAVE A2                  23450000 0
07E4 227C 0000 0050 0060          PUTPAR-1=CPCR             23470000 0
07E5 4009 E000 000C 00F0          A3=MAR                      23480000 0
07E6 4009 A000 0030 00F0          A1=MIR;MR1 IF RDC          23490000 0
07E7 AC08 0C40 0C0C 00F0          WHEN RDC THEN B=MAR,BEX   23500000 0
07E8 AC08 0C40 2000 00F0          B=A2;MR1 IF RDC           23510000 0
07E9 AC08 0000 0C00 00F0          WHEN RDC THEN BEX         23520000 0
07EA 2900 0000 0000 0060          MULTIPLY-1=CPCR           23530000 0
07EB 4009 E000 0050 00F0          A3=MIR;0M1                 23540000 0
07EC 9009 0000 0050 10F0          MW1 IF SAI                 23550000 0
07ED 9C08 A000 0050 00F0          WHEN SAI THEN A1=MIR      23560000 0
07EE 4009 0F46 000C 00F0          BMAR+1=MAR                 23570000 0
07EF 4009 2F56 000C 00F0          LIT AND BMAR=MAR          23580000 0
07F0 9009 0C40 4000 10F0          B=A3;MW1 IF SAI           23590000 0
07F1 00C0 0000 0000 00C0          HALFFETCH=AMPCCR          23600000 0
07F2 9C08 0000 0000 00F0          WHEN SAI THEN 0/STEP      23610000 0
07F3 2240 0000 0050 0040          GETPAR-1=MPCR              23620000 0
S ***** DIVIDE A(A+1),A(A) / A(B) => A(A) ***** 23630000 0
0PR74X1:  SB=A-FIELD;A3=B-FIELD  SSAVE A2                  23640000 0
07F4 2270 0000 0000 0060          PUTPAR-1=CPCR             23650000 0
07F5 4009 0C46 000C 00F0          B+1=MAR                     23660000 0
07F6 4009 2F56 000C 00F0          LIT AND BMAR=MAR          23670000 0
07F7 0070 0000 0000 00E0          7=LLT                        23680000 0
07F8 4009 A000 0050 00F0          A1=MIR;MR1 IF RDC          23690000 0
07F9 4009 0C40 2000 00F0          B=A2                          23700000 0
07FA AC08 E000 0C0C 00F0          WHEN RDC THEN A3=MAR,BEX  23710000 0
07FB A009 0C40 1000 00F0          B=A3;MR1 IF RDC           23720000 0
07FC AC08 C000 0C0C 00F0          WHEN RDC THEN A2=MAR,BEX  23730000 0
07FD 2A00 00C0 0000 0060          DIVIDE-1=CPCR             23740000 0
07FE 4009 C0C0 0030 00F0          A2=MIR;0M1                 23750000 0
07FF 6C09 00C0 003C 00F0          IF ABT THEN 0=MIR         23760000 0
0800 9009 0000 0000 10F0          MW1 IF SAI                 23770000 0
0801 9C08 0F46 000C 00F0          WHEN SAI THEN BMAR+1=MAR  23780000 0
0802 4009 2F56 000C 00F0          LIT AND BMAR=MAR          23790000 0
0803 0070 00C0 0000 00E0          7=LLT                        23800000 0
0804 4009 A0C0 0050 00F0          A1=MIR                      23810000 0
0805 6C09 0000 0050 00F0          IF ABT THEN 0=MIR         23820000 0
0806 9009 0C40 4000 10F0          B=A3; MW1 IF SAI           23830000 0
0807 9C08 0000 0000 00F0          WHEN SAI THEN 0/STEP      23840000 0
0808 2240 0000 0050 0060          GETPAR-1=CPCR             23850000 0
0809 4009 C0C1 A000 40F0          A2 C-A2;CSAR              23860000 0

```



```

0043 0007 5140 000C 00F0
0044 0000 0000 0000 00F0
0045 0009 0000 0000 00F0
0046 AC08 0000 0C00 00F0
0047 0009 0C40 0030 00F0
0048 0009 0C52 0000 00F0
0049 5408 2C40 000C 00F0
004A 0000 0000 0000 0040
004B 000C 0000 0030 0040

004C 0009 5000 000C 00F0
004D 0009 0000 0030 00F0
004E AC08 0000 0C00 00F0
004F 0009 0C40 1000 00F0
0050 0009 0C40 000C 00F0
0051 0009 0000 0000 00F0
0052 AC08 0000 0C00 00F0
0053 2060 0000 0030 0040

0054 0009 0C40 000C 20F0
0055 0000 0000 0C30 00F0
0056 0009 0000 0000 00F0
0057 AC08 0F46 0C0C 00F0
0058 0009 2F56 000C 00F0
0059 0009 0C40 0000 00F0
005A AC08 0000 0C0C 00F0
005B 0009 0C40 1000 00F0
005C AC08 0000 0C00 00F0

005D 0009 0001 A000 40F0
005E A000 0000 0000 0030
005F 0009 0C4C 0000 00F0
0060 0008 0C58 0000 00F0
0061 7C20 0010 A000 00F0
0062 7429 0010 AC00 00F0
0063 0009 0C40 1030 00F0
0064 0009 0C4C 0000 00F0
0065 0008 0C5E 0000 00F0
0066 7C20 0010 A000 00F0
0067 7429 0010 AC00 00F0
0068 0020 000F A000 00F0

0069 0009 0C40 000C 20F0
006A 0009 0000 0000 00F0
006B AC08 0F46 0C0C 00F0
006C 0009 2F56 000C 00F0
006D 0009 0C40 0000 00F0
006E AC08 0000 0C0C 00F0
006F 0009 0C40 1000 00F0
0070 AC08 0C56 1000 00F0
0071 2060 0000 0000 0040

0072 0009 2C00 000C 00F0
0073 0000 0000 0030 00F0
0074 0009 0000 0000 00F0

```

```

0PR74X3: SMIR=A-FIELD; A3=B-FIELD          SMAR=B(B)
A3=LIT=MAR
DBASE=LIT
MRI,IF RDC
WHEN RDC THEN BEX
B=MI,MI
O EOL B
IF FALSE THEN LIT + B=MAR;STEP ELSE SKIP
HALF FETCH-1=MPCR
HALF FETCH=MPCR
S ***** COMPARE REGISTERS *****
0PR74X4: SAS=A(B); B=A(A)
A3=MAR
MRI,IF RDC
WHEN RDC THEN BEX
B=MI,MI
MRI,IF RDC
WHEN RDC THEN BEX
SETCOMPARE-1=MPCR
S ***** COMPARE A(B) WITH A(A+1); A(A) SET COMPARE *****
0PR74X5: SB,MI=A-FIELD; A3=B-FIELD
B=MI,MI
HALF FETCH=MPCR
MRI,IF RDC
WHEN RDC THEN SMAR+1=MI,MI
LIT AND SMAR=MI
SMIR=MI,IF RDC
SMIR=C(A)
WHEN RDC THEN A3=MI,MI
B=A3;MI,IF RDC
SAS=C(A+1)
WHEN RDC THEN BEX
SMIR=A(A);A3=A(A+1);B=A(B)
A2 C=A2+CSAR
COMP 2=SBAR
A3 XOR B
A3 LE0 B; IF MST THEN STEP ELSE SKIP
IF FALSE THEN A2 OR B100 C=A2;JUMP ELSE SKIP
IF TRUE THEN A2 OR B100 C=A2;JUMP ISAME SIGNS
B=A3;MI
A3 XOR B
A3 LSS B; IF MST THEN STEP ELSE SKIP
IF FALSE THEN A2 OR B100 C=A2;JUMP ELSE SKIP
IF TRUE THEN A2 OR B100 C=A2;JUMP
A2 AND 0011 C=A2;JUMP
S ***** COMPARE A(A+1) AND A(A) WITH A(B) *****
0PR74X6: SB,MI=A-FIELD; A3=B-FIELD
B=MI,MI
MRI,IF RDC
WHEN RDC THEN SMAR+1=MI,MI
LIT AND SMAR=MI
SMIR=MI,IF RDC
WHEN RDC THEN A3=MI,MI
B=A3;MI;MI,IF RDC
WHEN RDC THEN A3 AND B=A3;BEX
SETCOMPARE-1=MPCR
S ***** COMPARE B(B) WITH B(A) *****
0PR74X7: SB,MI=A-FIELD; A3=B-FIELD
LIT=MI
DBASE=LIT
MRI,IF RDC

```

```

2486000C D
24870000 D
24880000 D
24890000 D
24900000 D
24910000 D
24920000 D
24930000 D
24940000 D
24950000 D
24960000 D
24970000 D
24980000 D
24990000 D
25000000 D
25010000 D
25020000 D
25030000 D
25040000 D
25050000 D

```


0293 3980 0000 0000 0000
0392 3980 0000 0000 0000
0391 3990 0000 0000 0000
0390 3970 0000 0000 0000
0389 3080 0000 0000 0000
0380 3010 0000 0000 0000
0377 3700 0000 0000 0000
0366 3720 0000 0000 0000
0350 3610 0000 0000 0000
0349 3540 0000 0000 0000
0285 3060 0000 0000 0000
0283 3450 0000 0000 0000
0267 2030 0000 0000 0000
0266 2080 0000 0000 0000
0280 2030 0000 0000 0000
0284 2040 0000 0000 0000
022A 2300 0000 0000 0000
01FC 2090 0000 0000 0000
01F0 2090 0000 0000 0000
01F4 20A0 0000 0000 0000
01F0 20A0 0000 0000 0000
01EE 2320 0000 0000 0000
01E7 2320 0000 0000 0000
01DF 2320 0000 0000 0000
0107 2320 0000 0000 0000
01CF 2320 0000 0000 0000
01CD 2320 0000 0000 0000
0106 2320 0000 0000 0000
018E 1E70 0000 0000 0000
018D 10F0 0000 0000 0000
018C 1070 0000 0000 0000
0180 10F0 0000 0000 0000
018A 1000 0000 0000 0000
0189 1000 0000 0000 0000
0180 10E0 0000 0000 0000
0187 1970 0000 0000 0000
0176 17E0 0000 0000 0000
0175 1770 0000 0000 0000
0172 17A0 0000 0000 0000
0161 1600 0000 0000 0000
015E 1860 0000 0000 0000
0144 1440 0000 0000 0000
0129 1370 0000 0000 0000
0126 1400 0000 0000 0000
012B 1150 0000 0000 0000
012A 1110 0000 0000 0000
00F9 1000 0000 0000 0000
00E0 10A0 0000 0000 0000
00F7 1000 0000 0000 0000
00F6 1020 0000 0000 0000
00F5 0F00 0000 0000 0000
00E0 0F30 0000 0000 0000
00D0 00F0 0000 0000 0000
00D4 1190 0000 0000 0000
00CA 1E00 0000 0000 0000
00C0 2270 0000 0000 0000
00B3 3370 0000 0000 0000
00AA 20A0 0000 0000 0000
00A0 1E00 0000 0000 0000
00A6 2270 0000 0000 0000

0CAZ 22A0 0000 0000 0000 0000
0C9F 21E0 0000 0000 0000 0000
0C9E 0700 0000 0000 0000 0000
009D 07C0 0000 0000 0000 0000
0C9C 0780 0000 0000 0000 0000
0C9B 21E0 0000 0000 0000 0000
0C9A 21E0 0000 0000 0000 0000
0099 07A0 0000 0000 0000 0000
0C98 0790 0000 0000 0000 0000
0C97 0710 0000 0000 0000 0000
0096 0680 0000 0000 0000 0000
0C95 0530 0000 0000 0000 0000
0C94 0480 0000 0000 0000 0000
0C93 0420 0000 0000 0000 0000
0C92 0000 0000 0000 0000 0000
0C91 7F30 0000 0000 0000 0000
0C90 7E30 0000 0000 0000 0000
0C8F 21E0 0000 0000 0000 0000
0C8E 21E0 0000 0000 0000 0000
0C8D 21E0 0000 0000 0000 0000
0C8C 21E0 0000 0000 0000 0000
008B 7000 0000 0000 0000 0000
008A 7090 0000 0000 0000 0000
0C89 7000 0000 0000 0000 0000
0C88 7070 0000 0000 0000 0000
0087 2100 0000 0000 0000 0000
0086 2100 0000 0000 0000 0000
0085 2100 0000 0000 0000 0000
0C84 7C80 0000 0000 0000 0000
0C83 7A80 0000 0000 0000 0000
0C82 7A10 0000 0000 0000 0000
0081 7990 0000 0000 0000 0000
0C80 2100 0000 0000 0000 0000
0C7F 2100 0000 0000 0000 0000
0C7E 2100 0000 0000 0000 0000
0C7D 2100 0000 0000 0000 0000
0C7C 78EC 0000 0000 0000 0000
0C7B 7870 0000 0000 0000 0000
0C7A 7800 0000 0000 0000 0000
0C79 7780 0000 0000 0000 0000
0C78 2100 0000 0000 0000 0000
0C77 2100 0000 0000 0000 0000
0C76 2100 0000 0000 0000 0000
0C75 2100 0000 0000 0000 0000
0C74 7780 0000 0000 0000 0000
0C73 7750 0000 0000 0000 0000
0C72 7730 0000 0000 0000 0000
0C71 7700 0000 0000 0000 0000
0C70 2100 0000 0000 0000 0000
0C6F 2100 0000 0000 0000 0000
0C6E 2100 0000 0000 0000 0000
0C6D 2100 0000 0000 0000 0000
0C6C 76E0 0000 0000 0000 0000
0C6B 7630 0000 0000 0000 0000
0C6A 7610 0000 0000 0000 0000
0C69 7560 0000 0000 0000 0000
0C68 2100 0000 0000 0000 0000
0C67 73AC 0000 0000 0000 0000
0C66 7390 0000 0000 0000 0000
0C65 7320 0000 0000 0000 0000

0C64 7310 0000 0030 00C0
0C63 730C 00C0 0030 00C0
0C62 72F0 00C0 0000 00C0
0061 72E0 0000 0030 00C0
0C60 72C0 0000 0000 00C0
0C5F 72A0 0000 0030 00C0
0C5E 7200 0000 0000 00C0
0C5D 7260 0000 0030 00C0
0C5C 7240 0000 0000 00C0
0C5B 7220 0000 0000 00C0
0C5A 7200 00C0 0000 00C0
0C59 71E0 0000 0000 00C0
0C58 2100 0000 0000 00C0
0C57 2100 00C0 0030 00C0
0C56 2100 0000 0030 00C0
0C55 7100 0000 0000 00C0
0C54 7010 0000 0030 00C0
0053 5E00 0000 0030 00C0
0C52 5D70 0000 0000 00C0
0051 6C50 00C0 0000 00C0
0C50 60F0 0000 0030 00C0
0C4F 6030 0000 0000 00C0
0C4E 6A00 0000 00C0 00C0
0C4D 6A10 00C0 0000 00C0
0C4C 6990 0000 0000 00C0
0C4B 6970 0000 0000 00C0
0C4A 2100 0000 0030 00C0
0C49 6940 0000 0000 00C0
0C48 6900 0000 0000 00C0
0C47 6800 00C0 0000 00C0
0C46 6860 00C0 0000 00C0
3045 67E0 0000 0000 00C0
0C44 67C0 0000 0030 00C0
0043 6740 0000 0000 00C0
0C42 6720 0000 0030 00C0
0C41 6700 0000 0030 00C0
0C40 66A0 0000 0000 00C0
0C3F 21E0 0000 0000 0040
0C3E 21E0 0000 0000 0040
0C3D 6610 0000 0000 00C0
0C3C 21E0 0000 0030 0040
0C3B 21E0 0000 0000 0040
0C3A 6470 0000 0000 00C0
0C39 6400 0000 0030 00C0
0C38 6240 0000 0000 00C0
0C37 61F0 00C0 0000 00C0
0036 60A0 0000 0000 00C0
0C35 6070 0000 0030 00C0
0C34 5EF0 0000 0000 00C0
0C33 5E00 00C0 0030 00C0
0C32 5DC0 0000 0000 00C0
0C31 5C00 0000 0000 00C0
0C30 5C90 0000 0030 00C0
0C2F 50C0 00C0 0030 00C0
0C2E 5000 00C0 0000 00C0
0C2D 5A00 0000 0000 00C0
0C2C 5A20 0000 0000 00C0
0C2B 5990 0000 0000 00C0
0C2A 50F0 0000 0030 00C0
0C29 5040 0000 0000 00C0

0020 5790 0000 0000 0000 0000
 0021 5700 0000 0000 0000 0000
 0022 5650 0000 0000 0000 0000
 0023 5550 0000 0000 0000 0000
 0024 5400 0000 0000 0000 0000
 0025 5210 0000 0000 0000 0000
 0026 5070 0000 0000 0000 0000
 0027 4930 0000 0000 0000 0000
 0028 4790 0000 0000 0000 0000
 0029 4650 0000 0000 0000 0000
 0030 4510 0000 0000 0000 0000
 0031 4370 0000 0000 0000 0000
 0032 4230 0000 0000 0000 0000
 0033 4090 0000 0000 0000 0000
 0034 3950 0000 0000 0000 0000
 0035 3810 0000 0000 0000 0000
 0036 3670 0000 0000 0000 0000
 0037 3530 0000 0000 0000 0000
 0038 3390 0000 0000 0000 0000
 0039 3250 0000 0000 0000 0000
 0040 3110 0000 0000 0000 0000
 0041 2970 0000 0000 0000 0000
 0042 2830 0000 0000 0000 0000
 0043 2690 0000 0000 0000 0000
 0044 2550 0000 0000 0000 0000
 0045 2410 0000 0000 0000 0000
 0046 2270 0000 0000 0000 0000
 0047 2130 0000 0000 0000 0000
 0048 2000 0000 0000 0000 0000
 0049 1860 0000 0000 0000 0000
 0050 1720 0000 0000 0000 0000
 0051 1580 0000 0000 0000 0000
 0052 1440 0000 0000 0000 0000
 0053 1300 0000 0000 0000 0000
 0054 1160 0000 0000 0000 0000
 0055 1020 0000 0000 0000 0000
 0056 880 0000 0000 0000 0000
 0057 740 0000 0000 0000 0000
 0058 600 0000 0000 0000 0000
 0059 460 0000 0000 0000 0000
 0060 320 0000 0000 0000 0000
 0061 180 0000 0000 0000 0000
 0062 40 0000 0000 0000 0000
 0063 0000 0000 0000 0000 0000
 0064 0000 0000 0000 0000 0000
 0065 0000 0000 0000 0000 0000
 0066 0000 0000 0000 0000 0000
 0067 0000 0000 0000 0000 0000
 0068 0000 0000 0000 0000 0000
 0069 0000 0000 0000 0000 0000
 0070 0000 0000 0000 0000 0000
 0071 0000 0000 0000 0000 0000
 0072 0000 0000 0000 0000 0000
 0073 0000 0000 0000 0000 0000
 0074 0000 0000 0000 0000 0000
 0075 0000 0000 0000 0000 0000
 0076 0000 0000 0000 0000 0000
 0077 0000 0000 0000 0000 0000
 0078 0000 0000 0000 0000 0000
 0079 0000 0000 0000 0000 0000
 0080 0000 0000 0000 0000 0000
 0081 0000 0000 0000 0000 0000
 0082 0000 0000 0000 0000 0000
 0083 0000 0000 0000 0000 0000
 0084 0000 0000 0000 0000 0000
 0085 0000 0000 0000 0000 0000
 0086 0000 0000 0000 0000 0000
 0087 0000 0000 0000 0000 0000
 0088 0000 0000 0000 0000 0000
 0089 0000 0000 0000 0000 0000
 0090 0000 0000 0000 0000 0000
 0091 0000 0000 0000 0000 0000
 0092 0000 0000 0000 0000 0000
 0093 0000 0000 0000 0000 0000
 0094 0000 0000 0000 0000 0000
 0095 0000 0000 0000 0000 0000
 0096 0000 0000 0000 0000 0000
 0097 0000 0000 0000 0000 0000
 0098 0000 0000 0000 0000 0000
 0099 0000 0000 0000 0000 0000
 0100 0000 0000 0000 0000 0000

1792 SECONDS.

26336 RULES.

14930 TOKENS.

2536 CARDS.

100 DISK SECTORS.

0 ERRORS.
C WARNINGS.

APPENDIX C. LOADER PROGRAM LISTING

This appendix provides a copy of the Microtranslator output listing of the Loader written in conjunction with the Emulator. Its source is maintained on disk and cards; and its object module is maintained on disk. The Loader actually consists of three separate programs which provide assembly, debugging and IOC functions to the Emulator. It is a by-product of the Emulation, and it was used for implementation and testing of the Emulator. Its functions should be incorporated in the Emulator Program in the course of expansion to a full emulation.

SERGE LOADER-SOURCE
PROGRAM UVK7-LOADER

```

ABASE=0
SBASE=8
SBASE=16
PAR=29
SWITCH=88
PLC=120
HEXADDR=210
CARDBUF=212
COLS=233
COL9X12=214
COL13X16=215
LASTCOL=232
PRINTADDR=237
BLANKLINE=500
ERRORLIST=280. PRINTAREA=238. DISKADDR=332
NUMLINES=36

```

```

XBEGIN PROGRAM HERE BY ZEROING MEMORY
WAIT
START: SET RETURN HERE ON SIGNAL FROM EPULATOR TO RESTART
      SET OC1 WHEN OC1 THEN 1 L=A1,MAR2
      COMP 16 -: SAR
      O=: MIR; SAVE
      MV2; A1-1 =: A1; IF SAI
      IF NOT THEN SKIP ELSE STEP
      WHEN SAI THEN A1=: MAR2; JUMP

```

```

      SREAD CARDS IN TO SETUP ERROR ROUTINES
ERRORSETUP:
      010=MAR2
      LIT L=A1
      MOST(DISKADDR)=LIT; COMP 8=SAR
      A1 OR LIT=A1
      LEAST(DISKADDR)=LIT
      LIT L=B
      COMP 16=SAR; 100=LIT
      A1 OR 0=MIR
      OUTPUT1-1=CPCR
      ANPCR=A1
      ERRORLIST=ANPCR
      LIT L=B
      3=LIT/COMP 16=SAR
      A1 OR 0 = MIR

```

```

ERRORSETUP1:
      ETOP-1=CPCR
      ERRORSETUP1-1=MPCR

```

```

      SSETUP BUFFER OF ALL SPACES FOR PRINTING BLANK LINES
      0=BC;LCTR
      32=LIT
      BLANKLINE=ANPCR
      0=MIR
      ANPCR=MAR2
      MV2;IF SAI

```

```

      SREAD FOUR SECTORS = 9 CARDS
      00300000 D
      00310000 D
      00320000 D
      00330000 D
      00340000 D
      00350000 D
      00360000 D
      00370000 D
      00380000 C
      00390000 D
      00400000 D
      00410000 D
      00420000 D
      00430000 D
      00440000 D
      00450000 D
      00460000 D
      00470000 D
      00480000 D
      00490000 D
      00500000 D
      00510000 D
      00520000 D
      00530000 D
      00540000 D
      00550000 D
      00560000 D
      00570000 D

```

```

      ADDRESS OF A-REG(O)
      ADDRESS OF B-REG(O)
      ADDRESS OF S-REG(C)
      ADDRESS OF P-REGISTER TEMP.
      SLOCATION TO STORE SWITCH CHOICES
      TEMPORARY ADDR. OF NEXT INSTRUCTION
      SADDRESS TO INSERT ADDRESSES TO PRINT
      SPERMAMENT ADDR. OF CARDBUFFER
      SADDRESS OF CARD COLS. K-8
      SADDRESS OF CARD COLS. 9-12
      SADDRESS OF CARD COLS. 13-16
      SADDRESS OF COL 00 OF CARD
      SPERMAMENT LOCATION OF PRINT BUFFER
      SLOCATION OF BUFFER OF SPACES
      PRINTAREA=238. DISKADDR=332
      NUMBER OF LINES PRINTED X SIX

```

```

      SBEGIN PROGRAM HERE BY ZEROING MEMORY
      WAIT
      START: SET RETURN HERE ON SIGNAL FROM EPULATOR TO RESTART
            SET OC1 WHEN OC1 THEN 1 L=A1,MAR2
            COMP 16 -: SAR
            O=: MIR; SAVE
            MV2; A1-1 =: A1; IF SAI
            IF NOT THEN SKIP ELSE STEP
            WHEN SAI THEN A1=: MAR2; JUMP

```

```

            SREAD CARDS IN TO SETUP ERROR ROUTINES
ERRORSETUP:
            010=MAR2
            LIT L=A1
            MOST(DISKADDR)=LIT; COMP 8=SAR
            A1 OR LIT=A1
            LEAST(DISKADDR)=LIT
            LIT L=B
            COMP 16=SAR; 100=LIT
            A1 OR 0=MIR
            OUTPUT1-1=CPCR
            ANPCR=A1
            ERRORLIST=ANPCR
            LIT L=B
            3=LIT/COMP 16=SAR
            A1 OR 0 = MIR

```

```

ERRORSETUP1:
            ETOP-1=CPCR
            ERRORSETUP1-1=MPCR

```

```

            SSETUP BUFFER OF ALL SPACES FOR PRINTING BLANK LINES
            0=BC;LCTR
            32=LIT
            BLANKLINE=ANPCR
            0=MIR
            ANPCR=MAR2
            MV2;IF SAI

```

```

0C00 480C 0000 0030 00F0
0C01 0000 00C1 401C 00F0
0C02 0000 00C0 3030 0020
0C03 4012 0005 0030 00F0
0C04 9009 80DE 4030 1CFO
0C05 6019 0000 0C30 00F0
0C06 9C28 AD03 001C 00F0

```

```

0C07 4809 0008 001C 00F0
0C08 4809 20C1 4030 00F0
0C09 00C0 0000 0030 00B0
0C0A 4809 A13C 4030 00F0
0C0B 03C0 0009 0000 00E0
0C0C 4809 2001 003C 00F0
0C0D 000C 00C2 0030 00A0
0C0E 4809 AC5C 0030 00F0
0C0F 000C 0000 0030 006C
0C10 4809 0490 4030 00F0
0C11 1100 0000 0000 00C0
0C12 4809 2001 0030 00F0
0C13 0030 0000 0000 00A0
0C14 4809 AC5C 0030 00F0

```

```

0C15 0010 0000 0000 0060
0C16 019C 0000 0000 0040

```

```

0C17 4809 0000 0001 00F0
0C18 0200 0000 0000 00E0
0C19 1F00 0000 0000 00C0
0C1A 4809 0490 0030 00F0
0C1B 4809 0443 001C 00F0
0C1C 4012 0000 0000 00F0
0C1D 9009 0000 0000 1CFO

```



```

0040 0000 0000 0000 0000
0041 0000 0000 0000 0000
0042 0000 0000 0000 0000
0043 0000 0000 0000 0000
0044 0000 0000 0000 0000
0045 0000 0000 0000 0000
0046 0000 0000 0000 0000
0047 0000 0000 0000 0000
0048 0000 0000 0000 0000
0049 0000 0000 0000 0000
0050 0000 0000 0000 0000
0051 0000 0000 0000 0000
0052 0000 0000 0000 0000
0053 0000 0000 0000 0000
0054 0000 0000 0000 0000
0055 0000 0000 0000 0000
0056 0000 0000 0000 0000
0057 0000 0000 0000 0000
0058 0000 0000 0000 0000
0059 0000 0000 0000 0000
0060 0000 0000 0000 0000
0061 0000 0000 0000 0000
0062 0000 0000 0000 0000
0063 0000 0000 0000 0000
0064 0000 0000 0000 0000
0065 0000 0000 0000 0000
0066 0000 0000 0000 0000
0067 0000 0000 0000 0000
0068 0000 0000 0000 0000
0069 0000 0000 0000 0000
0070 0000 0000 0000 0000
0071 0000 0000 0000 0000
0072 0000 0000 0000 0000
0073 0000 0000 0000 0000
0074 0000 0000 0000 0000
0075 0000 0000 0000 0000
0076 0000 0000 0000 0000
0077 0000 0000 0000 0000

```

```

CARDUF=LIT
READFIELD-1=:CPCR
LIT=IA1
7=LIT/COMP 16=8AR
8 L=J97 SAVE
LOOP BEGINS HERE
5
A3 L=:A3
COMP 3=:8AR
8 C=:B,MIR
COMP 8=:8AR
A1 AND B=:B
8 OR A3=:A3,BMI: CALL
SEND OF LOOP
5
SOPCODE IS NOW IN LSB OF B
SIF NOT ADV THEN OPC<60 =>TYPE 1
A3 L=6 LIT
4B=:LIT
SOPCODE = 60OCTAL
IF FALSE THEN A3 LEQ LIT:SKIP
TYPE1-1=:MPCR
SIF NOT ADV THEN OPC<=61 =>TYPE 4A
49=:LIT
IF FALSE THEN A3 GEQ LIT:SKIP
TYPE4A-1=:MPCR
SIF ADV THEN OPC<=70 =>TYPE 4A
ELSE TYPE 4B
56=:LIT
IF FALSE THEN SKIP
TYPE4A-1=:MPCR
SINSTRUCTION IS TYPE 4B - OPCODE STILL IN A3
TYPE4B:
COL5X6=LIT
READFIELD-1=:CPCR
A3 L=:A3
COMP 3=:8AR
8 C=:B,MIR
COMP 8=:8AR
A1 AND B=:B
A3 OR B=:A3,BMI
A3 L=:A3
COMP 1=:8AR
A3 OR BOOT=:A3,BMI:SAVE
SSETUP FOR TWO PASS LOOP FOR REST OF *M*
A3 L=:A3
COMP 3=:8AR
8 C=:B,MIR
COMP 8=:8AR
A1 AND B=:B
A3 OR B=:A3,BMI:CALL
SEND OF LOOP
OUTPUT-1=:MPCR
5
SOPCODE IS STILL IN A3
TYPE4A:
COL5X6=LIT
READFIELD-1=:CPCR
SET LC2:SAVE
SSTART 3 PASS LOOP HERE
A3 L=:A3

```

```

01100000 0
01190000 0
01200000 0
01210000 0
01220000 0
01230000 0
01240000 0
01250000 0
01260000 0
01270000 0
01280000 0
01290000 0
01300000 0
01310000 0
01320000 0
01330000 0
01340000 0
01350000 0
01360000 0
01370000 0
01380000 0
01390000 0
01400000 0
01410000 0
01420000 0
01430000 0
01440000 0
01450000 0
01460000 0
01470000 0
01480000 0
01490000 0
01500000 0
01510000 0
01520000 0
01530000 0
01540000 0
01550000 0
01560000 0
01570000 0
01580000 0
01590000 0
01600000 0
01610000 0
01620000 0
01630000 0
01640000 0
01650000 0
01660000 0
01670000 0
01680000 0
01690000 0
01700000 0
01710000 0
01720000 0
01730000 0
01740000 0
01750000 0
01760000 0
01770000 0

```

```

SSETUP FOR TWICE TRHU LOOP
SNAKE ROOM FOR MSB
SNAKE ROOM FOR MSB OF *M*
SGET NEXT DIGIT OF M TWICE
SWORD WAS PULIT INTO LOWER A3

```

01780000 D
 01790000 D
 01800000 D
 01810000 D
 01820000 D
 01830000 D
 01840000 D
 01850000 D
 01860000 D
 01870000 D
 01880000 D
 01890000 D
 01900000 D
 01910000 D
 01920000 D
 01930000 D
 01940000 D
 01950000 D
 01960000 D
 01970000 D
 01980000 D
 01990000 D
 02000000 D
 02010000 D
 02020000 D
 02030000 D
 02040000 D
 02050000 D
 02060000 D
 02070000 D
 02080000 D
 02090000 D
 02100000 D
 02110000 D
 02120000 D
 02130000 D
 02140000 D
 02150000 D
 02160000 D
 02170000 D
 02180000 D
 02190000 C
 02200000 D
 02210000 D
 02220000 D
 02230000 D
 02240000 D
 02250000 D
 02260000 D
 02270000 D
 02280000 D
 02290000 D
 02300000 D
 02310000 D
 02320000 D
 02330000 D
 02340000 D
 02350000 C
 02360000 D
 02370000 D

COMP 3=1:1SAR
 B C=10,MIR
 COMP 8=1:1SAR
 A1 AND B=10
 A3 OR B=1A3,BMI
 IF LC2 THEN JUMP ELSE CALL
 SEND LOOP
 S
 A3 L=1A3,DEX
 COMP 1=1:1SAR
 SIMSERT 1 FIELD
 A3 OR 0001=1A3
 OUTPUT-1=1:1MPCR
 SRESULTS IN A3
 S
 S0PCODE IS IN A3
 COLSX0=LIT
 READAFIELD-1=1:1CPCR
 SET LC21SAVE
 ISTART 3 PASS LOOP HERE
 A3 L=1A3
 COMP 3=1:1SAR
 B C=10,MIR
 COMP 8=1:1SAR
 A1 AND B=10
 A3 OR B=1A3,BMI
 IF LC2 THEN JUMP ELSE CALL
 SEND LOOP A,K,B FIELDS INSERTED NOW GET 1 FIELD
 A3 L=1A3,DEX
 COMP 1=1:1SAR
 A3 OR 0001=1A3
 C9L9X12=LIT
 READAFIELD-1=1:1CPCR
 A3 L=1A3
 COMP 3=1:1SAR
 B C=10,MIR
 COMP 8=1:1SAR
 A1 AND B=10
 A3 OR B L=1A3,BMI
 COMP 1=1:1SAR
 COMP 8=1:1SAR
 SEND OF Y HAS BEEN INSERTED
 A3 OR 0001=1A3,BMI,SET LC2
 ISTART TWO - TWO PASS LOOPS HERE FOR REMAINDER OF Y FIELD
 YFIELD: SAVE
 A3 L=1A3
 COMP 3=1:1SAR
 B C=10,MIR
 COMP 8=1:1SAR
 A1 AND B=10
 A3 OR B=1A3,BMI
 CALL 13X16=LIT
 READAFIELD-1=1:1CPCR
 IF NOT LC2 THEN A3=MIR, SKIP ELSE STEP
 YFIELD-1=1:1MPCR
 SCOMPLETED Y
 SCOMPLETED TYPE 1 NOW SAVE IN MIR AND OUTPUT

TYPE1:
 0050 0000 0000 0000
 0100 0000 0000 0000
 0052 0000 0000 0000
 0005 0005 0001 1000
 0006 0000 0000 0000
 0007 0005 0001 0000
 0008 0000 0000 0000
 0009 0005 0001 0000
 000A 0005 0001 0000
 000B 0005 0001 0000
 000C 0005 0001 0000
 000D 0005 0001 0000
 000E 0005 0001 0000
 000F 0005 0001 0000
 0010 0005 0001 0000
 0011 0005 0001 0000
 0012 0005 0001 0000
 0013 0005 0001 0000
 0014 0005 0001 0000
 0015 0005 0001 0000
 0016 0005 0001 0000
 0017 0005 0001 0000
 0018 0005 0001 0000
 0019 0005 0001 0000
 001A 0005 0001 0000
 001B 0005 0001 0000
 001C 0005 0001 0000
 001D 0005 0001 0000
 001E 0005 0001 0000
 001F 0005 0001 0000
 0020 0005 0001 0000
 0021 0005 0001 0000
 0022 0005 0001 0000
 0023 0005 0001 0000
 0024 0005 0001 0000
 0025 0005 0001 0000
 0026 0005 0001 0000
 0027 0005 0001 0000
 0028 0005 0001 0000
 0029 0005 0001 0000
 002A 0005 0001 0000
 002B 0005 0001 0000
 002C 0005 0001 0000
 002D 0005 0001 0000
 002E 0005 0001 0000
 002F 0005 0001 0000
 0030 0005 0001 0000
 0031 0005 0001 0000
 0032 0005 0001 0000
 0033 0005 0001 0000
 0034 0005 0001 0000
 0035 0005 0001 0000
 0036 0005 0001 0000
 0037 0005 0001 0000
 0038 0005 0001 0000
 0039 0005 0001 0000
 003A 0005 0001 0000
 003B 0005 0001 0000
 003C 0005 0001 0000
 003D 0005 0001 0000
 003E 0005 0001 0000
 003F 0005 0001 0000
 0040 0005 0001 0000
 0041 0005 0001 0000
 0042 0005 0001 0000
 0043 0005 0001 0000
 0044 0005 0001 0000
 0045 0005 0001 0000

```

02300000 D
02390000 D
02400000 D
02410000 D
02420000 D
02430000 C
02440000 D
02450000 D
02460000 D
02470000 D
02480000 D
02490000 D
02500000 D
02510000 C
02520000 D
02530000 G
02540000 D
02550000 D
02560000 D
02570000 D
02580000 D
02590000 D
02600000 D
02610000 D
02620000 D
02630000 D
02640000 D
02650000 D
02660000 C
02670000 D
02680000 D
02690000 D
02700000 D
02710000 D
02720000 D
02730000 D
02740000 C
02750000 D
02760000 D
02770000 C
02780000 D
02790000 D
02800000 D
02810000 D
02820000 D
02830000 D
02840000 C
02850000 D
02860000 D
02870000 D
02880000 D
02890000 D
02900000 D
02910000 D
02920000 D
02930000 D
02940000 D
02950000 D
02960000 D
02970000 D

```

MOPACK-1=MPCR
 S
 SIF TYPE 4 INSTRUCTION THEN IF LOWER HALF OF PREVIOUS INSTRUCTION WAS ZERO AND IN THIS INSTRUCTION AND SAND OUTPUT, ELSE SHIFT THIS INSTRUCTION TO UPPER HALF SAND OUTPUT AND ADVANCE PAR.
 S

OUTPUT:
 A2-1=MAR2
 MR2:IF RDC
 WHEN RDC THEN BEX
 B L=18
 COMP 16=SAR
 PACKLEFT-1=MPCR
 NOT B
 IF ABT THEN BEX:STEP ELSE JUMP
 A3 OR B=MIR
 SJOIN INSTRUCTION INTO LOWER HALF

WRITEOUT:
 A3 OR B=MIR
 OUT-1=MPCR
 PACKLEFT:

MOPACK: A2=MAR2
 A2+1=A2
 OUT-1=MPCR
 S

READFIELD: SRETURN CONTENTS OF BUFFER ADDRESSES BY LIT
 LIT=MAR2
 MR2:IF RDC
 WHEN RDC THEN BEX: JUMP
 SEND OF INSTRUCTION SETUP ROUTINES
 S

ORIGIN:
 GETADDR-1=CPCR
 GET NEW ADDRESS AND PUT INTO P-REG LOCATION COUNTER 106
 LIT=MAR2
 PLOC=LIT:16=SAR
 L=18
 COMP 10=SAR
 A3+B=MIR:A2
 OUT-1=MPCR
 S

SETINDEXREG: GET REG NUMBER FROM WORD IN COL 7-8, BUFFER 199
 SAVE IN A3.AFTER OFFSETTING BY 9. PASS CONTROL TO SETREG WHICH WILL DECIPHER VALUE AND STORE IN PROPER REGISTER.
 SMAR ASSUMED STILL SET AT 198
 S

SETAREG: GET REG NUMBER FROM COL 7-8 WORD 199 SAVE IN A3.
 PASS CONTROL TO SETREG WHICH WILL DECIPHER VALUE AND STORE IN REG.MAR STILL SET TO MEREAD 198
 S

SETADDR-1=CPCR
 A3 + LIT =A3
 BBASE=LIT
 SETADDR-1=MPCR
 S

SETAREG: GET REG NUMBER FROM COL 7-8 WORD 199 SAVE IN A3.
 PASS CONTROL TO SETREG WHICH WILL DECIPHER VALUE AND STORE IN REG.MAR STILL SET TO MEREAD 198
 S

GETADDR-1=CPCR
 SVALUE RETURNED IN A3


```

0066 0009 0000 0901 00F0
0067 0210 00C0 0030 00E0
0068 0009 20C3 001C 00F0
0069 0020 0000 0030 00A0
006A 0009 0C40 0030 00F0
006B 0020 0000 0000 00A0
006C 0000 0F40 001E 00F0
006D 00A0 00C0 0030 00A0
006E 0009 2000 0030 00F0
006F 0000 0000 0030 00E0
0070 0200 0000 0030 00A0
0071 0009 0000 0030 00F0
0072 0009 0000 0030 00F0
0073 0020 0000 0000 00A0
0074 0009 20C3 001C 00F0
0075 0012 0000 0031 00F0
0076 0030 0000 0000 00B0
0077 0009 0C41 0032 00F0
0078 0009 0000 0F30 00F0
0079 0000 0000 0030 0030
007A 0009 0001 0030 00F0
007B 0009 0C40 0030 00F0
007C 0000 0000 0000 1CF0
007D 0000 2000 0030 00F0
007E 0040 0000 0030 00B0
007F 0200 0000 0030 00F0
0100 0009 0C40 0030 00F0
0101 0009 2C52 0000 00F0
0102 0300 0000 0000 00A0
0103 6C00 2000 0030 00F0
0104 0020 0000 0000 00A0
0105 0C19 00C1 0F00 00F0
0106 0210 00C0 0030 00A0
0107 0009 0C40 0030 00F0

0108 0200 0000 0030 00A0
0109 1070 0000 0000 00A0
010A 0210 0000 0000 00A0

010B 1C40 0002 0C2C 00F0
010C 0009 00C0 0000 10F0
010D 0C00 0000 0000 00F0
010E 0009 0000 0000 00F0
010F 0000 0000 0000 00F0
0110 0009 0000 0030 00F0
0111 0000 0000 0030 00F0
0112 0009 0C42 0000 00F0
0113 0020 0000 0000 00F0

0114 0009 0000 0C00 00F0
0115 0009 0000 1011 00F0

```

```

THIS SHOULD READ 20 WORDS INTO ADDRESS 334(0)
0-009,LCTR
33-LIT
LIT=MAR2
HEXADDR=LIT;COMP 16=8AR
B=MIR
OUTPUT1-1=CPCR
IF NOT GOV THEN 0MAR+1=MAR2,INC;STEP ELSE SKIP
ZBUFF:
ZBUFF-1=MPCR
CARDFETCH:
CARDUF=LIT
EXTOP-1=:CPCR
CARDFETCH-1=:MPCR
A2 L=A1
HEXADDR=LIT;COMP 20=8AR
LIT=MAR2
O=MIR,LCTR;SAVE
COMP 0=8AR;3=LIT
B L=MIR,INC;IF SAI
A1 R=001
COMP 3=8AR
A1 L=A1
B=MIR
IF GOV THEN MV2;STEP ELSE JUMP
WHEN SAI THEN LIT=MIR,MAR2
CARDUF=LIT;24=8AR
INPUT-1=CPCR
B R=0
LIT EOL B
40=LIT;16=8AR
IF TRUE THEN LIT=MIR;STEP ELSE SKIP
HEXADDR=LIT;16=8AR
IF TRO THEN 1 L=001;SKIP
CHECKCOL1-1=MPCR
B=MIR
CARDPRINT:
EXTOP-1=:CPCR
CARDPRINT-1=MPCR
CHECKCOL1-1=MPCR
S
S
THIS ROUTINE PERFORMS REQUESTED EXTERNAL INTERFA
TO THE TOP MIR = FUNCTION/ADDRESS
RETURNS CONDITION OF OP IN B
SET GC2 WHEN GC2 THEN NOT 0=:MARI
MVI; IF SAI
WHEN SAI THEN 0; SET INT
IF INT
WHEN INT THEN STEP
MVI;IF RDC
WHEN RDC THEN BEX; RESET GC2
NOT B
IF ABT THEN JUMP ELSE RETN
SEND EXTERNAL FUNCTION
S
GETADDR:
ASSUME MAR2 IS SET UP TO REREAD SAME WORD VIA BEX. RESULT WILL
BEX RETURNED IN A3, 7MIR CONTAINS ADDRESS OF WORD
BEX
0=:A3,BR2,LCTR
FIRST DIGIT IS LAST BYTE OF B

```

```

03500000 D
03590000 D
03600000 D
03610000 D
03620000 D
03630000 D
03640000 D
03650000 D
03660000 D
03670000 D
03680000 D
03690000 D
03700000 D
03710000 D
03720000 D
03730000 D
03740000 D
03750000 D
03760000 D
03770000 D
03780000 D
03790000 D
03800000 D
03810000 D
03820000 D
03830000 D
03840000 D
03850000 D
03860000 D
03870000 D
03880000 D
03890000 D
03900000 D
03910000 D
03920000 D
03930000 D
03940000 D
03950000 D
03960000 D
03970000 D
03980000 D
03990000 D
04000000 D
04010000 D
04020000 D
04030000 D
04040000 D
04050000 D
04060000 D
04070000 D
04080000 D
04090000 D
04100000 D
04110000 D
04120000 D
04130000 D
04140000 D
04150000 D
04160000 D
04170000 D

```



```

0147 13C0 C000 0C00 0060
0148 4009 2001 2000 00F0
0149 0060 0000 0030 00E0
014A 4009 CC5C 2030 00F0
014B 4009 E0C1 1000 00F0
014C 0E0C 00C0 0C30 00A0
014D 4009 E15C 1000 00F0
014E 4009 0C00 0900 00F0
014F 4009 0C40 0031 00F0
0150 021C 0000 0C00 00E0
0151 4009 2003 001C 00F0
0152 0E0C 0000 0C00 00E0

0153 13C0 0000 0030 0060
0154 0000 0F46 001E 00F0
0155 1520 0000 0C30 00A0
0156 4009 E000 0C30 00F0
0157 0000 0000 0C30 0020
0158 4009 0000 0931 00F0
0159 2010 0000 0030 00E0
015A 4009 0C41 0030 00F0
015B 4009 0C41 0030 00F0
015C 4000 0000 0C00 0030
015D 4009 A0C0 0F00 00F0
015E 4009 A001 4030 00F0
015F 4052 0000 0000 00F0

0160 4009 0C41 0030 00F0
0161 3000 00C0 0030 0030
0162 4009 0C41 0030 00F0
0163 4000 0000 0030 0030
0164 4009 A0C0 0F00 00F0
0165 4009 A001 4002 00F0
0166 0C19 E0C3 001C 00F0
0167 15F0 0000 0030 00A0
0168 4009 E0C0 100C 00F0
0169 4009 0C40 0030 00F0
016A 4009 0000 0030 1CF0
016B 4C00 00C0 0931 00F0
016C 0030 00C0 0000 00E0
016D 302E 0000 0C00 00F0

016E 4009 0001 0030 00F0
016F 0060 0000 0030 00A0
0170 0300 0000 00FC 00C0
0171 4009 C0C0 A00C 00F0
0172 4009 C00E 2030 00F0
0173 4029 CC5D A030 00F0
0174 4009 2C41 A030 00F0
0175 0310 0000 0000 00A0
0176 4009 E0C0 1030 00F0
0177 4009 E0C1 901C 00F0
0178 13E0 0000 0000 0060
0179 4009 CODE 2035 00F0
017A 4009 0C40 4002 00F0
017B 4000 E0C1 9000 00F0
017C 1570 0000 0000 C340
017D 4009 2003 001C 00F0
017E 0700 0000 0030 00E0
017F 13EC 0000 000C 0060

OUTPUT1-1=:CPCR
LIT L=:A2
G=:LIT
A2 OR B=:A2
SETBUFF: A3 L=:A3
COMP 16=:SAR;PRINTAREA-1=LIT
A3 OR LIT=:A3
0=:0C0
B=:MIR;LCTR
33=:LIT
LIT=:MAR2
PRINTAREA=LIT
ZEROLoop:
OUTPUT1-1=:CPCR
IF NOT COV THEN BKAR+1=:MAR2;INC; STEP ELSE SKIP
ZEROLoop-1=:MPCR
A3 R=:A1
16=:SAR
CONVERT: 0=:BC0;LCTR
1=LIT;COMP 6=:SAR
B L=:B
B L=:MIR
COMP 2=:SAR
A1 R=:B01
A1 L=:A1
SET LC2:SAVE
CONVLoop: B L=:B
COMP 5=:SAR
B L=:MIR
COMP 3=:SAR
A1 R=:B01
A1 L=:A2;JNC
IF COV THEN A3=:MAR2;SKIP ELSE STEP
CONVLoop-1=:MPCR
A3+1=:A3
B=:MIR
MV2:IF SAJ
WHEN SAJ THEN 0=:BC0;LCTR
3=:LIT
IF LC2 THEN JUMP ELSE CALL
END OF LOOP ONE 32 BIT WORD WRITTEN IN 3 WORDS
A2 L=:B
COMP 16=:SAR;6=:LIT
FETCHWORD-1=:MPCR
A2 R=:A2
A2-1=:A2
IF NOT MST THEN A2 OR B C=:A2;JUMP
LIT + B C=:A2
PRINTBUFF-1=:MPCR
FETCHWORD: A3+1=:A3
A3+1 C=:A3;MAR2
INPUT-1=:CPCR
A2-1=:A2;CTR
B=:A1;JNC
IF NOT COV THEN A3+1 C=:A3;STEP ELSE SKIP
CONVERT-1=:MPCR
LIT=:MAR2
PL0C=LIT
INPUT-1=:CPCR

```

```

04770C00 D
04780C00 D
04790C0C D
04800C00 D
04810C00 D
04820000 D
04830C00 D
04840C00 D
04850C00 D
04860000 D
04870C00 D
04880C00 D
04890C00 D
04900C00 D
04910000 C
04920C00 D
04930000 D
04940C00 D
04950C00 D
04960C00 D
04970C00 D
04980C00 D
04990C00 D
05000C00 D
05010C00 C
05020C00 D
05030000 D
05040C00 D
05050C00 D
05060C00 D
05070C00 D
05080000 D
05090C00 D
05100C00 D
05110C00 D
05120000 C
05130000 D
05140C00 D
05150C00 D
05160C00 C
05170C00 D
05180000 D
05190000 D
05200C00 D
05210C00 D
05220C00 D
05230C00 D
05240C00 D
05250C00 D
05260C00 D
05270C00 D
05280000 D
05290C00 D
05300C00 D
05310C00 D
05320C00 D
05330C00 D
05340C00 D
05350C00 D
05360C00 D

```

```

WORDS PER LINE=6
RA2=6/65=WDS PER LINE/65 WORDS
RA3=READ ADDR/BUFFER ADDR
RA=30303030

```

```

RSTART BY PRINTING ADDRESS

```

```

RBEGIN LOOP HERE
RSHIFT A1 INTO B

```

```

RB CONTAINS CONVERTED WORD

```

```

RSEE IF DONE ONE LINE YET

```

```

RDONE ALL 65 WORDS

```

```

0100 4809 0C40 2030 C0F0
0101 0E50 00C0 00D0 C0C0
0102 2029 0000 00E0 00F0
0103 0320 0000 0030 C040

0104 4809 00C1 0830 C0F0
0105 0E50 00C0 00D0 00AC
0106 4809 205C 0030 C0F0
0107 10A0 0000 0030 006C
0108 1030 00C0 00D0 C040
0109 4809 00C0 0030 C0F0
010A 14AC 0000 0030 C040

010B 49C9 20C3 001C 00F0
010C 0D60 0000 00D0 00E0
010D 4809 0000 0031 00F0
010E 0030 0000 0030 00E0
010F 13E0 0000 0030 006C
0110 4812 0C40 4030 C0F0
0111 4809 00C1 4030 C0F0
0112 0000 0000 0000 0030
0113 4809 00C0 9000 C0FC
0114 4809 00C1 4030 00F0
0115 4809 0C41 1030 C0F0
0116 9000 00C0 0000 0030
0117 4809 0C41 0030 00F0
0118 0000 00C0 0000 0030
0119 4809 0C40 0032 00F0
011A 0C00 0F46 001C 00F0
011B 0020 0000 0030 00E0
011C 2000 0000 0031 00F0
011D 18E0 0000 0030 00F0
011E 4809 00C1 4000 00F0
011F 0000 0000 0000 0030
0120 4809 0000 9C70 00F0
0121 4809 0C40 0030 00F0
0122 3000 0000 0030 00F0
0123 0330 0000 0000 0040
0124 4809 20C3 001C 00F0
0125 0040 0000 0030 00E0
0126 13E0 0000 0000 0060
0127 113C 00C0 0000 0060
0128 4809 0000 0030 C0FC
0129 4809 00C2 0030 C0F0
012A 0000 0000 0030 C0F0
012B 002C 00C0 0030 C040
012C 4809 00C1 C800 00FC
012D 0000 0000 0000 002C
012E 4809 0C43 001C 00F0
012F 13C0 0000 0000 0060
0130 0E50 00D0 00D0 C040
0131 0000 0010 001C 00F0
0132 13E0 0000 0030 0060
0133 4809 0C40 C000 00F0
0134 0000 0000 0030 002C
0135 4809 0040 0040 00F0
0136 0340 00C0 0030 0060
0137 4809 0000 0000 00F0
0138 4824 0C43 101C C0FC

```

RESTORE A2 FROM SAVED LOCATION

B=1A2
 NEWRD-1=AMPCR
 IF NOT LC1 THEN JUMP
 IORETURN-1=MPCR

PRINTBUFF:

1 L=10
 COMP 16=5AR;PRINTAREA=LIT
 LIT OR B=MIR
 EXTOP-1=CPCR
 PRINTBUFF-1=MPCR
 A3 R=A3
 SETBUFF-1=MPCR

DATA:

LIT=MAR2; SET LC1
 COL9X12=LIT
 O=MIR,LC1R
 3=LIT
 INPUT-1=CPCR
 B=A1,BM1/SAVE
 A1 L=A1
 COMP 4=SAR
 A1 R=A3
 A1 L=A1
 A3 + B L=A3,BAD
 COMP 3=SAR
 B L=B
 COMP 1=SAR
 A3+B=MIR,INC
 IF COV THEN BMAR+1=MAR2; STEP ELSE JUMP
 2=LIT
 IF LC1 THEN LC1R; STEP ELSE SKIP
 DATA1-1=MPCR
 A1 L=A1
 COMP 4=SAR
 A1 R=A3
 A3+B=A1,B
 IF LC2 THEN STEP ELSE SKIP
 RESERVE1-1=MPCR
 LIT=MAR2
 CARBUF=LIT
 INPUT-1=CPCR
 GETADDR-1=CPCR
 A1=MIR
 NOT A3
 IF ABT THEN STEP ELSE SKIP
 MOPACK-1=MPCR
 1 L=B
 COMP 10=SAR
 A3+B=MAR2
 OUTPUT1-1=CPCR
 NEWRD-1=MPCR
 SET GC1; WHEN GC1 THEN B111=MAR2
 B R=A1
 COMP 16=SAR
 A1+AMPCR=AMPCR
 EXTIOREQ-1=AMPCR
 STEP
 B=MAR2;A3;EXEC

SINPUT DECIMAL DATA

1 GET RID OF BCL HEADER
 2 ISOLATE LOW ORDER 4 BITS
 3 MULT BY 8
 4 MULT BY 2

5 ADD IN LSP BYTE

6 SHOULD HAVE BEEN CALLED BY RESERVE

7 SRFREAD COLS 4-8 FOR ADDRESS

8 IF ADDR=0 PUT IN LINE

9 OTHERWISE PUT AT ADDRESS GIVEN

10 OFFSET ADDRESS BY 1074

11 NORMAL RETURN TO GET NEXT CARD

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```

0189 49F6 0000 0030 00F0          CALL:SET LC1
018A 4949 0019 00D5 00F0          RESET GC1; B111=CTR
018B 0000 0000 0002 00F0          INC; WHEN COV THEN STEP
018C 1000 0000 0030 0040          IOREG-1=MPCR
EXTIOREG:
018D 0350 00C0 0000 00CC          DUMPREG-1=AMPCR
018E 0360 0000 0000 00CC          DUMPADD-1=AMPCR
018F 0370 0000 0030 00CC          CARDIO-1=AMPCR
0190 0380 0000 0030 00CC          DISKIO-1=AMPCR
0191 0390 0000 0030 00CC          DISKWRITE-1=AMPCR
0192 03A0 0000 0030 00CC          PRINTERIO-1=AMPCR
0193 03B0 0000 0000 00CC          WORDIO-1=AMPCR
0194 03CC 0000 0030 00CC          PRINTLINE-1=AMPCR
0195 0000 0000 0000 00CC          START-1=AMPCR
DUMPREG:
0196 4009 0000 0030 00F0          STEP
0197 1F4C 0000 0030 00CC          BLANKLINE=AMPCR
0198 4009 0000 0030 00F0          STEP
0199 4009 0000 0030 00F0          AMPCR=MIR
019A 4009 2001 0F30 00F0          LIT L=881
019B 4009 0000 0030 00F0          16=8AR;1=LIT
019C 4009 0000 0030 00F0          8=MIR
019D 10AC 0000 0030 00F0          OUTBLANK: EXTOP-1=CPCR
019E 1CC0 0000 0030 0040          OUTBLANK-1=MPCR
019F 141C 0000 0030 0040          IODUMP-1=MPCR
DUMPADD:
0199 1410 0000 0030 00CC          IODUMP-1=MPCR
CARDIO:
019A 4009 0000 0030 00F0          SREAD ONE CARD INTO BUFFER ADDRESSED IN 0,MAR2
019B 0000 0000 0000 0020          A3 L=A3
019C 2009 0000 0030 00F0          COMP 16=8AR
019D 1000 0000 0000 006C          A3 R=MIR;IF LC1
019E 103C 0000 0030 0040          EXTOP-1=CPCR
019F 1090 0000 0030 0040          CARDIO1-1=MPCR
0199 4009 0000 0030 00F0          IORETURN-1=MPCR
DISKWRITE:
019A 4009 0000 0030 00F0          WAIT
019B 0210 00C0 0030 00E0          0=8CB;LCTR
019C 0000 0000 0000 0000          33=LIT
019D 0000 0000 0000 0000          LIT=MAR2. PRINTAREA=LIT
019E 9C08 0000 0030 00F0          8=MIR;SAVE
019F 0429 0F4E 001E 00F0          MW;IF SAI
0199 4009 0000 0030 00F0          WHEN SAI THEN 0;STEP
019A 0000 0000 0000 0000          IF NOT COV THEN 8MAR;1=MAR2;INC;JUMP
019B 0000 0000 0000 0000          A3 AND LIT L=A3,BAD
019C 0000 0000 0000 0000          COMP 3=8AR;7=LIT
019D 0000 0000 0000 0000          8 L=B;LCTR
019E 0000 0000 0000 0000          COMP 1=8AR;9=LIT
019F 0000 0000 0000 0000          A3+B=A3
0199 4009 0000 0030 00F0          A3+AMPCR=MAR2;A1
019A 0000 0000 0000 0000          ERRORLIST=AMPCR
019B 0000 0000 0000 0000          LIT=A3
019C 0000 0000 0000 0000          PRINTAREA-1=LIT
019D 0000 0000 0000 0000          INPUT-1=CPCR
019E 4009 0000 0030 00F0          8=MIR
019F 4009 0000 0030 00F0          A3+1=A3;MAR2;INC
05970000 D
05980000 D
05990000 C
06000000 C
06010000 D
06020000 D
06030000 D
06040000 D
06050000 D
06060000 D
06070000 D
06080000 D
06090000 D
06100000 D
06110000 C
06120000 D
06130000 D
06140000 D
06150000 D
06160000 D
06170000 D
06180000 D
06190000 D
06200000 D
06210000 D
06220000 D
06230000 C
06240000 D
06250000 D
06260000 D
06270000 D
06280000 D
06290000 D
06300000 D
06310000 D
06320000 C
06330000 D
06340000 C
06350000 D
06360000 C
06370000 D
06380000 D
06390000 D
06400000 C
06410000 D
06420000 D
06430000 D
06440000 D
06450000 D
06460000 D
06470000 C
06480000 C
06490000 D
06500000 D
06510000 D
06520000 D
06530000 D
06540000 D
06550000 C
RSETUP ADDRESS OF BLANKLINE BUFFER
SALLOW FOR TINKING FOR AMPCR
$OUTPUT BLANKS = 30303C30
$ASSUME ERROR NUMBER IN A3
$MULTIPLY ERROR NUMBER BY 10

```


07160000 D
 07170000 D
 07180000 D
 07190000 D
 07200000 D
 07210000 D
 07220000 D
 07230000 D
 07240000 D
 07250000 C
 07260000 D

IF CV THEN A3+1=MAR2,A3J STEP ELSE JUMP
 IF LC2 THEN A3=A2,SET LC2 RUSE NEXT ADDRESS FROM A2
 OUTPUT1-1=CPCR
 A1+1=A1,MAR2
 WORD1-1=ANPCR
 A1 EOL LIT
 LASTCOL=LIT
 IF FALSE THEN JUMP 1218 = LAST COLUMN OF CARD
 IF LC2 THEN A3+1=A2 SRESET PROGRAM COUNTER
 WORD2: MEMRD-1=NPCR
 END

1END

0221 0C00 E0C3 1C1C 00F0
 0222 3E99 E0C8 2000 00F0
 0223 13C0 0000 0090 0060
 0224 9009 A0C3 901C 00F0
 0225 2176 0000 0C00 00CC
 0226 9009 A152 0C0C 00F0
 0227 0E00 0000 0070 00E0
 0228 6029 0000 0030 00F0
 0229 3009 E0C0 2000 00F0
 022A 0E50 0000 0000 0040
 022B 000C 00C0 0C00 0040
 022C 2200 00C0 0070 0040
 C1C4 2000 0000 0C90 00C0
 01C3 1F50 0003 0000 00C0
 01C2 1070 0C00 0070 00C0
 01C1 106C 0000 000E 00CC
 01C0 2060 0000 0090 00CC
 01BF 1000 0000 0090 00C0
 01BE 1CF0 0003 0000 00CC
 01B0 1C50 0000 0090 00CC
 01B6 10C0 0000 0090 00C0
 01A3 20C0 00C0 0090 0040
 0163 1090 0000 0000 0040
 0175 1030 0000 0000 0040
 0170 1750 0000 0000 00C0
 0126 13E0 0000 0090 0060
 0100 104C 0000 0000 0060
 00FF 13EC 0000 0000 0060
 00F0 10A0 0000 0000 0060
 00EB 13C0 00C0 0C90 0060
 00D2 1130 00C0 0090 0060
 00D1 1000 0000 0030 0040
 00CF 13C0 0000 000C 0060
 00CB 1130 0003 0000 0060
 00CA 0E30 0000 0090 0040
 00C6 1130 0000 0C70 0060
 00C5 1230 00C0 0C00 0040
 00C4 1130 0000 0090 0060
 00C3 1230 00C0 0000 0000
 00C0 1130 0000 0000 0060
 00BF 0E30 0000 0090 0040
 00B9 1130 0000 000C 0060
 00B5 0E30 0000 0000 0040
 00B0 0E30 0000 0C90 0040
 0CAC 000C 00C0 0090 00C0
 00A6 0020 0000 0000 0040
 6CA3 0090 0000 0000 0060
 0C90 0090 0000 0000 0060
 0003 0090 0000 0000 0060
 0001 0A6C 00C0 0000 0040
 0075 0090 0000 0030 0060
 0073 0A60 0000 0030 0040
 0062 0090 0000 0090 0060
 0060 0730 0000 0000 0040
 0050 0730 0000 0090 0040
 005A 0010 0000 0C90 0040
 0040 107C 0000 0000 0060
 0049 210C 0000 0000 0040
 0046 20A0 0000 0000 0040

0F93 1400 0000 0C3C 0040
0C40 0010 0000 0050 0040
0C3D 0C40 0000 0000 004C
0C3A 0C5C 0000 0C3F 004C
0C37 0C3F 0000 0080 0040
0C34 0000 0000 0C50 0040
0C31 00F0 0000 0C0C 0040
002E 04A0 0000 0080 0040
0C2B 10A0 0000 0050 0040
0024 13E0 00C0 0C00 00C0
0021 0020 0000 0C3C 0040
0015 10A0 00C0 0C3C 00C0
000F 13C0 00C0 0050 00C0

C ERRORS: 728 CARDS. 3969 TOKENS.

6700 RULES. 507 SECONDS.

DUP FILE ON DISK:UYK7-LOADER

INVALID ARGUMENT: FILE10 4

0 1:1209.1

#####

APPENDIX D. SAMPLE AN/UYK-7 SORT PROGRAM

This appendix provides a copy of a sample program which was used to demonstrate the capability of the D-Machine to function as an AN/UYK-7. The program, written in AN/UYK-7 Machine Language, will read twelve numbers per card, print the numbers, sort the input and print the sorted results. Any number of cards could be read and sorted until the "END" card is encountered. At this point the program would reinitialize memory and be ready to accept the next program. Several of the Loader's macro functions, including the L, W, D and N options, were utilized along with the appropriate formats for the five instruction types. It must be emphasized that when this program was run the ALGOL Machine had been removed and the D-Machine reconfigured through microprogramming to be an AN/UYK-7. The entire output format and program execution were produced by the Loader/Emulator combination with the IOP being used strictly as an Input/Output Channel. Examples of the Loader and Debugger output optional listings for this sample program are presented in Appendix E and F.

```

L 00002      ORIGIN SORT ROUTINE AT LOCATION 0002
D 01001      10
203320001001
110310001002
440310001002
532220000014
523220000003
102320001000
512420000021
320020001000
201320000777
514020000002
101310001002
241310001001
240310001002
330020001000
514020000006
201320001000
530000004040      JUMP TO TITLE ENDING ROUTINE
O 04000      BEGIN TITLE PRINTING ROUTINE AT 04000
071400005000
071400005352
071400005352
070400001022
071400005044
071400005352
071400005110
071400005352
071400005154
070410001002
106320001002
446320005416
531220004060      JUMP TO COMPLETION ROUTINE IF END CARD
071400005352
071400005220
071400005352
071400005352
071410001002
510000000002      JUMP TO BEGINNING OF SORT ROUTINE
O 04040      RETURN HERE FROM SORT ROUTINE AND FINISH TITLES
071400005352
071400005352
071400005264
071400005352
071400005330
071400005352
071400005352
071420001002
071400005352
071400005352
510000004011
O 04060      START COMPLETION ROUTINES HERE
071400005352
071400001002      PRINT END
7706000      TERMINATE PROGRAM AND RESTART EMULATOR

```

W 05000 AN/UYK-7 EMULATION DEMONSTRATION PROGRAM
W 05022
W 05044 THIS IS A TEST OF THE AN/UYK-7 EMULATION
W 05066 USING A MACHINE LANGUAGE PROGRAM
W 05110
W 05132 FOR A DEMONSTRATION SORT ROUTINE USING
W 05154
W 05176 THE FOLLOWING INPUT NUMBERS:
W 05220
W 05242 THE RESULTS OF THIS SORT
W 05264
W 05306 ARE AS FOLLOWS:
W 05330
W 05352
W 05374
W 05416END
N 04000

123 456 789 987 654 321 023 456 875 888 555 213
357 652 389 123 583 742 928 654 987 248 965 281
321 654 987 123 456 789 369 258 147 963 852 741
END TERMINATE SORT ROUTINE, READY FOR NEXT PROGRAM

APPENDIX E. SAMPLE LOADER OUTPUT LISTING

This appendix provides a copy of the output received from the Loader when the sample program discussed in Appendix D is run. This output is obtained by turning on the IRQ switch on the Loader's Interpreter. The output serves as a hard copy program listing for the programmer and can be utilized for debugging. The address to the left of each instruction is the octal assignment for that instruction, derived from the last "O" or "L" card, and was offset by 1024. The Loader input is terminated by an "N" card which initializes the PAR and signals the Emulator to commence execution.

L 0002	ORIGIN SORT ROUTINE AT LOCATION 0002
0 01001	TO
2C02	20320001001
2C03	180310001002
2C04	440310001002
2C05	532220000014
2C06	523220000003
2C07	102220001000
2C10	512420000021
2C11	320820001000
2C12	201320000777
2C13	514020000002
2C14	101310001002
2C15	241310001001
2C16	240310001002
2C17	330020001000
2C20	514020000006
2C21	201320001000
2C22	530000000040
0 04000	BEGIN TITLE PRINTING ROUTINE AT 04000
6C00	071400003000
6C01	071400003352
6C02	071400003352
6C03	070430001022
6C04	071400003044
6C05	071400003352
6C06	071400003110
6C07	071400003352
6C10	071400003154
6C11	070410001002
6C12	106320001002
6C13	446320003416
6C14	531220000060
6C15	071400003352
6C16	071400003220
6C17	071400003352
6C20	071400003352
6C21	071400001002
6C22	510000000002
0 04040	RETURN HERE FROM SORT ROUTINE AND FINISH TITLES
6C40	071400003352
6C41	071400003352
6C42	071400002664
6C43	071400003352
6C44	071400003330
6C45	071400003352
6C46	071400003352
6C47	071400001002
6C50	071400003352
6C51	071400003352
6C52	510000000011

JUMP TO TITLE ENDING ROUTINE
 JUMP TO TITLE PRINTING ROUTINE AT 04000

JUMP TO COMPLETION ROUTINE IF END CARD

JUMP TO BEGINNING OF SORT ROUTINE
 FROM SORT ROUTINE AND FINISH TITLES

```

0 04060 START COMPLETION ROUTINES HERE
0460 07140003352
0461 071430001002 PRINT END
0462 7704000 AM/UYK-7 EMULATION DEMONSTRATION PROGRAM
05000 AM/UYK-7 EMULATION DEMONSTRATION PROGRAM
05022 T-110 IS A TEST OF THE AM/UYK-7 EMULATION
05044 USING A MACHINE LANGUAGE PROGRAM
05066 FOR A DEMONSTRATION SORT ROUTINE USING
05110 THE FOLLOWING INPUT NUMBERS?
05132 THE RESULTS OF THIS SORT
05134 ARE AS FOLLOWS?
05176
05220
05242
05264
05306
05330
05352
05374
05416END

```

N 00000 AN/UYK-7 EMULATION DEMONSTRATION PROGRAM

THIS IS A TEST OF THE AN/UYK-7 EMULATION
USING A MACHINE LANGUAGE PROGRAM
FOR A DEMONSTRATION SORT ROUTINE USING
THE FOLLOWING INPUT NUMBERS:

123 456 789 907 654 321 023 456 875 000 555 213

THE RESULTS OF THIS SORT
ARE AS FOLLOWS:

023 123 213 321 456 456 555 654 789 875 880 907

THE FOLLOWING INPUT NUMBERS:

357 652 389 123 593 742 920 654 907 240 965 201

THE RESULTS OF THIS SORT
ARE AS FOLLOWS:

123 240 201 337 359 503 652 654 742 920 965 907

THE FOLLOWING INPUT NUMBERS:

321 654 907 123 456 789 359 250 147 963 852 741

THE RESULTS OF THIS SORT
ARE AS FOLLOWS:

123 147 250 321 359 456 654 741 789 852 963 907

END TERMINATE SORT ROUTINE, READY FOR NEXT PROGRAM

APPENDIX F. SAMPLE DEBUGGER OUTPUT LISTING

This appendix provides a sample of the output received from the Loader when it was used as a debugger for the sample program discussed in Appendix D. This output is obtained by turning on the IRQ switch on the Emulator's Interpreter. The switch was not left set for the entire program's execution because the output requires approximately thirty pages. The IRQ switch causes all CMR registers from address 0000 to 0035 to be printed as each instruction is executed. Each time an instruction does a Y-Operand write that address is also dumped. The addresses are printed in the leftmost column and include the following information which can be used during program debugging:

OCTAL ADDRESS	DESCRIPTION
0-7	Task A-Register contents
10	Unused (always = 0)
11-17	Task Index B-Register contents
20-27	Task Base S-Register contents
30	Repeat Instruction (if applicable)
31	Current Instruction being Repeated (if applicable)
32	Current Indirect Control Word (if applicable)
33	Y-Operand for Indirection (if applicable)
34	ICW address in memory (if applicable)
35	Program Address Register

Those addresses marked "if applicable" would normally be zero, but could contain data if either the Repeat mode or

Indirection mode had been used previously in the program. The lower 20 bits of address 0035 (PAR) point to the octal address of the next instruction. The upper 12 bits of the PAR are those ASR bits which were implemented as discussed in Section C of Chapter V. It is noteworthy that the output is an eleven bit octal representation of a 32-bit binary word, thus the leftmost octal digit represents only two bits.

By utilizing this optional listing in combination with the Loader listing, the programmer should be capable of proceeding through his program step by step. This facility proved an invaluable aid in troubleshooting the Emulator as each new instruction was written and tested.


```

0C000C06 05000201003 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
00000014 03000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
00000022 07000002000 0000002000 0000002000 0000002000 0000002000 0000002000 0000002000
0F000C30 09000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000

0C000000 06001600011 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
00000006 05000201003 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
00000014 00000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000
0C000022 07000002000 0000002000 0000002000 0000002000 0000002000 0000002000 0000002000
0C000C30 09000000000 0000000000 0000000000 0000000000 0000000000 0000000000 0000000000

```

THE RESULTS OF THIS SORT
ARE AS FOLLOWS:

223 123 213 321 436 456 555 654 709 875 890 907

THE FOLLOWING INPUT NUMBERS:

357 652 309 123 593 742 920 654 907 240 965 201

THE RESULTS OF THIS SORT
ARE AS FOLLOWS:

123 240 201 357 399 503 652 654 742 920 965 907

THE FOLLOWING INPUT NUMBERS:

321 654 907 123 456 709 369 258 147 963 852 741

THE RESULTS OF THIS SORT
ARE AS FOLLOWS:

123 147 258 321 369 456 654 741 709 852 963 907

END TERMINATE SORT ROUTINE, READY FOR NEXT PROGRAM

GLOSSARY

Active Status Register (ASR): A special word in the AN/UYK-7 used to indicate the status of special conditions or modes of operation. Each bit of the word has a separate meaning to the central processor.

ADO: The Burrough's Advanced Design Organization, Paoli, Pennsylvania, which designed the Naval Postgraduate School's D-Machine.

A Registers (A1, A2, A3): Each of the three A registers is functionally identical. The A registers are used for temporary data storage within the Logic Unit of the Interpreter and serve as a primary input to the adder.

Adder: The adder in the Logic Unit of the Interpreter, is a modified version of a straightforward carry lookahead adder. It is also used for executing logic operations.

Alternate Microprogram Count Register (AMPCR): The AMPCR is a 12-bit register in the Memory Control Unit of the Interpreter, which contains the jump or return address for program jumps and subroutine returns within a microprogram.

AMPCR: Alternate Microprogram Count Register.

Arithmetic (A) Registers: There are two sets of eight Arithmetic Registers in the AN/UYK-7. They are used extensively in arithmetic calculations and are directly addressable by the programmer.

ASR: The Active Status Word in the AN/UYK-7.

B Register: The B register is the primary interface between the Logic Unit of the Interpreter and the Data/Program Memory or Devices through the Switch Interlock. It also serves as a secondary input to the adder.

Barrel Switch: The barrel switch is a matrix of gates in the Logic Unit of the Interpreter, used to shift a parallel data word any number of places to the left or right in a single clock time.

Base Registers 1 and 2 (BR1, BR2): The Base Registers are two 8-bit registers in the Memory Control Unit of the Interpreter, which usually contain the base address of a 256-word block of Data/Program Memory.

Base (S) Registers: There are two sets of eight Base Registers in the AN/UYK-7 used extensively in multi-programming and multi-processing. Base registers are used for operand address calculations.

BR1 and BR2: Base Registers 1 and 2 in the Interpreter.

Building Block: The term used to describe the primary functional units of the Interpreter Based System and includes: Interpreter, Data/Program Memory and Switch Interlock.

Control Memory Registers (CMR): A block of 89 registers in the AN/UYK-7 used for special fast memory operations.

Condition Register (COND): The COND is a 12-bit register in the Control Unit of the Interpreter and is used to store various condition bits for use during program execution.

Central Processing Unit (CPU): The primary arithmetic and control unit in a conventional computer system.

Condition Select: The condition select is a matrix of gates in the Control Unit of the Interpreter that computes the results of a computation or logic operation in the Logic Unit with a preselected result. The results of the comparison may be used to determine the sequence of execution of microprogram instructions.

Control Unit (CU): The CU, one of the five functional units of the Interpreter, is used for condition testing and the storage and distribution of enable signals received from the nanoinstructions.

Counter (CTR): The CTR is an 8-bit counter in the Z register section of the Memory Control Unit of the Interpreter, used for loop control and other counting functions.

CTR: Counter in the Interpreter.

Data/Program Memory: The Data/Program Memory of the Interpreter, also called S-Memory, provides storage for data and program, and functions similarly to the main memory modules of a conventional computer system.

Emulation: Describes a process through which the hardware components of one machine (Host) are made to "appear" to assume the specific characteristics of the hardware of another machine (target).

End-Around-Shift: A shift operation in either the left or right direction, in which the bit or bits which would be shifted out of the register are reinserted in the more significant end.

End-Off-Shift: A shift operation in either the left or right direction, in which the bit or bits shifted out of the register are lost. Vacated bit positions are automatically replaced by zeros.

Firmware: In the Interpreter Based System, firmware is the combination of stored logic in the micro-memory and the hardware logic of the Interpreter.

GC Bits: A set of two (GC1, GC2) global condition bits in the Interpreter. They are used as lockouts during communications to the I/O processor.

HALFFETCH: A subroutine written for the Emulator, which is executed when a halfword instruction has been decoded.

Horizontal: A type of microprogramming instruction which controls multiple gates simultaneously allowing parallel functions to execute.

Host: A term used in Emulation to define the machine on which another machine is to be emulated (imitated). In this thesis the Burrough's D-Machine.

ICW: Indirect Control Word in the AN/UYK-7.

IFE1CH: A subroutine written for the Emulator, which reads the next instruction from main memory, deciphers the Op-code and passes control to the appropriate Op-code execution subroutine.

Incrementer (INCR): The INCR is in the Memory Control Unit of the Interpreter and increments the address of the next microinstruction to be executed by the Interpreter by zero, one or two, depending on the successor instruction which is either implied or specified. A WAIT causes an increment by zero, a STEP causes an increment by one, and a RETN causes an increment by two.

Indirection: An addressing technique or mode of operation of the AN/UYK-7 in which Y-Operand address calculation points to an Indirect Control Word (ICW) which in turn points to the operand or another ICW. Indirection is determined by the i-field of an instruction.

Indirect Control Word (ICW): The ICW is a 32-bit word in the AN/UYK-7 used in Indirection which can be broken down into several fields. The fields determine the mode of indirect address calculation to be used in pointing to the next ICW or the Y-Operand.

Indexing: An addressing technique wherein the normal address calculated is incremented/decremented (indexed) by the value in the specified index register.

Index (B) Register: There are two sets of seven Index Registers in the AN/UYK-7. They provide the ability to perform Indexing during memory referencing, and may also be used as counters.

INT: An Interrupt signal issued by an Interpreter.

Interpreter: The Interpreter is the basic building block of the Interpreter-Based System. Functionally, it is characterized by the combination of microprogram instructions stored in its M memory and the combination of bits in its nanoinstruction which enable signals to implement the hardware logic.

Interpreter-Based System: A computer design concept that provides, in the form of basic building blocks, the throughput and flexibility for a variety of data processing requirements.

Interrupt: In the AN/UYK-7, the Interrupt signals the central processor to cease its normal instruction flow and respond to a request for services. In the D-Machine, Interrupt (INT) is a flag which may be set between processors signalling that a message has been placed in the Mailbox.

Least Significant Bit (LSB): For a number or value represented in binary notation, that bit position which represents the least significant portion of the number.

LIT: Literal Register in the Interpreter.

Literal Register (LIT): An 8-bit register in the Z section of the Memory Control Unit of the Interpreter, which is used for temporary storage of literals from microinstructions.

Logic Unit (LU): The LU is one of the five major functional units of the Interpreter. It performs all of the arithmetic, Boolean logic, and shifting operations of the Interpreter.

Mailbox: An address (64K) in the Interpreter's S-Memory which is used for passing messages between Interpreters and the IOP.

MAR: Memory Address Register in the Interpreter.

Memory Address Register (MAR): The MAR is an 8-bit register in the Memory Control Unit of the Interpreter, which contains the least significant 8 bits of a memory or device address.

Memory Control Unit (MCU): The MCU is one of the five major functional units of the Interpreter. It controls the sequence of execution for microinstructions; the addressing of Data/Program Memory; and the selection of devices.

Memory Information Register (MIR): The MIR is a register in the Logic Unit of the Interpreter which serves as the output interface register between the Interpreter and the Switch Interlock.

Microprogram Address Control Register (MPAD CNTL): The MPAD CNTL, a register in the Memory Control Unit of the Interpreter - controls the loading of the MPCR and the AMPCR, and determines the value of the increment.

Microprogram Count Register (MPCR): The MPCR, located in the Memory Control Unit of the Interpreter, is a 12-bit register that usually contains the address, in M-memory, of the microinstruction presently being executed by the Interpreter.

Microprogram Memory (M-Memory): The M-Memory is one of the five major functional units of the Interpreter. It stores microinstructions which characterize the Interpreter for a given application, and may be implemented as a read/write semiconductor memory.

Microprogramming: A technique for implementing the control functions of a digital computer using programmable control signals in a separate memory called a control store, which is organized on a word basis.

MIR: Memory Information Register in the Interpreter.

Monoprogramming: A general computer operating environment in which one program at a time is executed.

Most Significant Bit (MSB): For a number or value represented in binary notation, that bit position which represents the most significant portion of the number, or the sign of the number.

MPCR: The Microprogram Count Register in the Interpreter.

Multiprogramming: A general computer operating environment in which more than one program at a time is executed with each given a fixed time slice.

Multiprocessing: A general computer operating environment in which two or more central processors execute simultaneously, and share resources; such as, memory and I/O devices.

Multiprocessor: A network of computers capable of simultaneously executing two or more programs or sequences of instructions by means of multiprogramming, parallel processing or both.

Nanoinstruction: A single instruction stored in N-Memory of the Interpreter, the contents of which constitute 56 unique signals for controlling hardware logic of the Interpreter.

Nanomemory (N-Memory): The N-Memory, one of the five functional units of the Interpreter, stores 56 specific enable signals for the hardware logic within the Logic Unit, Control Unit, and Memory Control Unit.

Page: A grouping of addresses of fixed length. In the Emulator the AN/UYK-7 memory was treated as eight pages of 8K each.

PAR: Program Address Register in the AN/UYK-7.

Program Address Register (PAR): A register in the AN/UYK-7 which holds the address of the next instruction to be accessed.

Port Select Unit (PSU): The PSU provides control and the electrical interface between a single Interpreter and its Devices and Data/Program Memory.

Shift Amount Register (SAR): The SAR is a 6-bit register in the Control Unit of the Interpreter and is used to store the number of positions a word or literal is to be shifted by the barrel switch.

Switch Interlock (SWI): The SWI provides the interconnection between Interpreters, Data/Program Memory, and Devices of an Interpreter Based System. Its function is to permit any one of a multiplicity of Interpreters to access all modules of an array of Data/Program Memory and/or all Devices.

Target: A term used in Emulation to define a machine to be emulated (imitated). In this thesis, the AN/UYK-7.

TRANSLANG: A computer programming language designed to convert pseudo-English language statements defining the action of the Interpreter for each machine cycle into binary patterns for the M-Memories.

Vertical: A microprogramming instruction which controls those gates needed for a single function execution.

Z Register Section: A collection of registers and selection gates in the Memory Control Unit of the Interpreter, which includes the CTR, LIT, and Input Selection gates used to control the execution sequence of microinstructions.

BIBLIOGRAPHY

1. Agrawala, A. K. and Rausher, T. G., "Microprogramming: Perspective and Status," IEEE Trans, C23, p. 817-37, August 1974.
2. Allred, G. R., "System/370 Integrated Emulation Under OS and DOS," Proceedings SJCC, 38, p. 163-67, 1971.
3. Almes, G. T., Drongowski, P. J., and Fuller, S. H., "Emulating the Nova on the PDP 11/40: A Case Study," Computer Conference, p. 53-6, Fall 1975.
4. Bagley, J. D., "Microprogrammable Virtual Machines," Computer, p. 38-42, February 1976.
5. Boulaye, G. and Mermet, J., Microprogramming, Herman, Paris, 1972.
6. Bricker, G. B., "Taking the Risk Out of System Upgrading," Data Processing Magazine, 12, p. 27-9, September 1970.
7. Burrough's Corporation Report 64116, Emulation Facility, by Advanced Design Organization, Paoli, Pa., 28 June 1971.
8. Burrough's Corporation Report TR70-2, The Interpreter, by R. L. Davis, 16 February 1970.
9. Burrough's Corporation Report TR70-8, Microprogramming Manual for Interpreter Based Systems, by Advanced Design Organization, Paoli, Pa., November 1970.
10. Burrough's Corporation Report 66143, Algol Reference Manual for the Interpreter Based System, by Advanced Design Organization, Paoli, Pa., 15 June 1975.

11. Dolhoff, T. L., "The Negative Aspects of Microprogramming," *Datamation*, 20, p. 64-6, July 1974.
12. Ellenby, J., "Emulation and Competition in I/O System Design," *Computer Conference*, p. 303-6, 1974.
13. Flynn, M. J., Neuhauser, C., and McClure, R. M., "EMMY- An Emulation System for User Microprogramming," *Proceedings NCC*, 44, p. 85-9, 1975.
14. Galey, J. M., "Microprogramming: The Bridge Between Hardware and Software," *Computer*, p. 23, August 1975.
15. Husson, S. S., *Microprogramming Principles and Practices*, Prentice-Hall, Inc., 1970.
16. Jaeger, R., "Microprogramming: A General Design Tool," *Computer Design*, 13, p. 150-7, August 1974.
17. Jones, L. H., "Instruction Sequencing in Microprogrammed Computers," *Proceedings NCC*, 44, p. 91-8, 1975.
18. Jones, L., "A Survey of Current Work in Microprogramming," *Computer*, p. 33-8, August 1975.
19. Jones, L. H. and Merwin, R. E., "Trends in Microprogramming. A Second Reading," *IEEE Trans*, C23, p. 754-9, August 1974.
20. Kahn, P. G. and Fuller, M. E., "Program Conversion: A Discussion of Techniques," *Data Processing Magazine*, 11, p. 28-31, November 1969.
21. Mallach, E. G., "Emulator Architecture," *Computer*, p. 24-32, August 1975.

22. Mandell, R. L., "Hardware/Software Trade-Offs--Reasons and Directions," Proceedings FJCC, 41, p. 453-9, 1972.
23. Rauscher, T. G., "On the Feasibility of Emulating the AN/UYK-7 Computer on the AADC Signal Processing Element," NTIS, November 1972.
24. Reigel, E. W. V. and Fisher D. A., "The Interpreter--A Microprogrammable Building Block System," Proceedings SJCC, 40, p. 705-23, 1972.
25. Rosin, R. F., "Contemporary Concepts of Microprogramming and Emulation," Computer Survey, 1, p. 197-212, December 1969.
26. Sperry Rand, UNIVAC, Computer Set AN/UYK-7 (V) Technical Manual Volume 1, Navships 0967-319-4010, January 1971.
27. Sperry Rand, UNIVAC, AN/UYK-7, Technical Description.
28. Tucker, A. B. and Flynn, M. J., "Dynamic Microprogramming: Processor Organization and Programming," Communications of the ACM, 14, p. 240-50, April 1971.
29. Wilkes, M. B. "The Growth of Interest in Microprogramming: A Literature Survey," Computer Survey, 1, p. 139-45, September 1969.

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