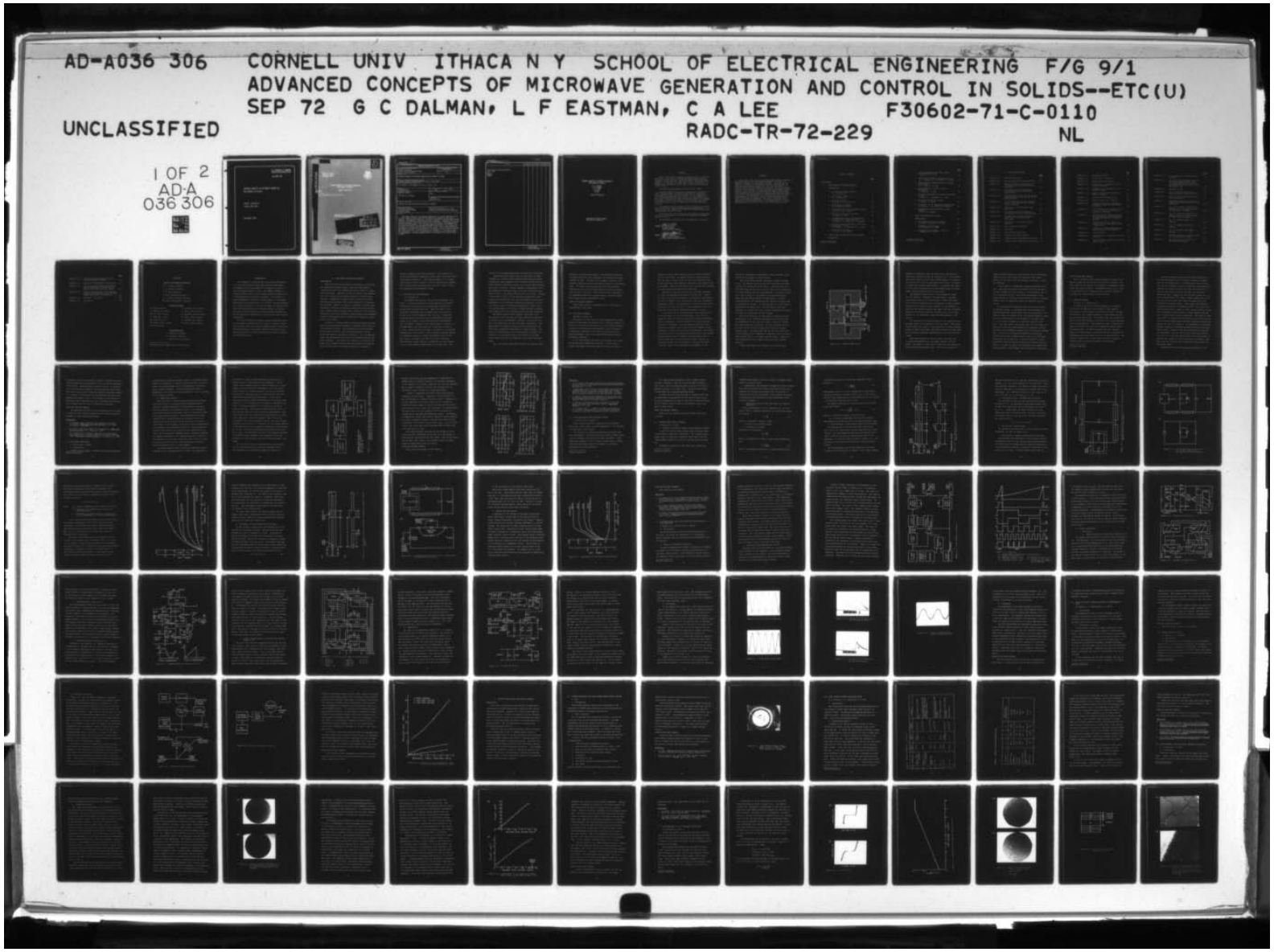
AD-A036 306 CORNELL UNIV ITHACA N Y SCHOOL OF ELECTRICAL ENGINEERING F/G 9/1
ADVANCED CONCEPTS OF MICROWAVE GENERATION AND CONTROL IN SOLIDS--ETC(U)
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AD-A036 306

ADVANCED CONCEPTS OF MICROWAVE GENERATION AND CONTROL IN SOLIDS

CORNELL UNIVERSITY
ITHACA, NEW YORK

SEPTEMBER 1972

AD A036306

RADC-TR-72-229
Technical Report
September 1972

ADVANCED CONCEPTS OF MICROWAVE GENERATION AND CONTROL IN SOLIDS

Cornell University

AF30602-71-C-0110

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SPRINGFIELD, VA. 22161

UNCLASSIFIED

Security Classification

DOCUMENT CONTROL DATA - R & D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY (Corporate author)	2a. REPORT SECURITY CLASSIFICATION
Cornell University School of Electrical Engineering Ithaca, New York 14850	UNCLASSIFIED
	2b. GROUP N/A

3. REPORT TITLE

ADVANCED CONCEPTS OF MICROWAVE GENERATION AND CONTROL IN SOLIDS

4. DESCRIPTIVE NOTES (Type of report and inclusive dates)

Technical Report (Seventh Quarterly 1 Apr - 30 Jun 1972)

5. AUTHOR(S) (First name, middle initial, last name)

G.C. Dalman, L.F. Eastman, C.A. Lee, J. Frey, et al

6. REPORT DATE	7a. TOTAL NO. OF PAGES	7b. NO. OF REFS
September 1972	128	50

8a. CONTRACT OR GRANT NO.	9a. ORIGINATOR'S REPORT NUMBER(S)
F30602-71-C-0110 Job Order No. 55730369	None
	9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report) RADC-TR-72-229

10. DISTRIBUTION STATEMENT

Approved for public release; distribution unlimited.

11. SUPPLEMENTARY NOTES	12. SPONSORING MILITARY ACTIVITY
RADC Project Engineer: R. Hunter Chilton (OCTE) AC 315 330-4251	Rome Air Development Center (OCTE) Griffiss Air Force Base, New York 13440

13. ABSTRACT

This report deals with the progress made during the seventh quarterly period of a solid state microwave oscillator and amplifier research and development program. Included are the results of studies of transferred electron punch-through injection, and avalanche diodes and solid state materials. Discussed first are LSA diodes and circuits, Gunn effect amplifiers and oscillators, a PCM Gunn oscillator, and GaAs materials studies. Next discussed are high average power TRAPATT diode structures and research on high frequency TRAPATT oscillators. Also reported are two studies of punch-through injection (Baritt) diodes, one for high frequency cw operation and the other for low frequency cw operation. Work on relaxing avalanche mode (RAM) oscillators is reported along with a summary of a new study on microwave transistors. The report concludes with a discussion of the progress made on ion implantation, on vacuum epitaxial growth in silicon and on ionization rates in GaAs.

DD FORM 1 NOV 65 1473

UNCLASSIFIED

Security Classification

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Solid State Microwave Generation						
Gunn Effect						
LSA						
TRAPATT						
IMPATT						

ADVANCED CONCEPTS OF MICROWAVE GENERATION AND CONTROL IN SOLIDS

G. C. Dalman
L. F. Eastman
C. A. Lee
J. Frey
et al

Cornell University

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FOREWORD

This is the seventh quarterly progress report on research conducted at the School of Electrical Engineering, Cornell University, under Contract F30602-71-C-0110, Job Order Number 55730369. The research is under the overall direction of G.C. Dalman, L.F. Eastman, C.A. Lee, and J. Frey. The results of research for the period 1 April 1972 to 30 June 1972 are discussed herein.

The RADC Project Engineer is R.H. Chilton (OCTE).

The major objectives of this contract are to perform reseach and development in advanced techniques of microwave power generation and control in solids. It is intended that the devices resulting from this effort will be competitive with or replace microwave tubes at low and medium power levels. New areas of application whose feasibility cannot be evaluated in advance will also be studied. It is expected that these solid state sources will be widely used in future microwave systems.

This report presents progress in the research and development of microwave solid state generators and amplifiers, including Gunn, LSA, IMPATT, high efficiency IMPATT devices, and punch-through injection diodes.

This report has been reviewed by the Office of Information (OI) and is releasable to the National Technical Information Services (NTIS).

This technical report has been reviewed and is approved.

Approved: R. HUNTER CHILTON
Project Engineer
Electron Devices Section

Approved: ARTHUR J. FROHLICH
Chief, Techniques Branch
Surveillance & Control Division

ABSTRACT

This report deals with the progress made during the seventh quarterly period of a solid state microwave oscillator and amplifier research and development program. Included are the results of studies of transferred electron, punch-through injection, and avalanche diodes and solid state materials. Discussed first are LSA diodes and circuits, Gunn effect amplifiers and oscillators, a PCM Gunn oscillator, and GaAs materials studies. Next discussed are high average power TRAPATT diode structures and research on high frequency TRAPATT oscillators. Also reported are two studies of punch-through injection (Baritt) diodes, one for high frequency CW operation and the other for low frequency CW operation. Work on relaxing avalanche mode (RAM) oscillators is reported along with a summary of a new study on microwave transistors. The report concludes with a discussion of the progress made on ion implantation, on vacuum epitaxial growth in silicon and on ionization rates in GaAs.

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INTRODUCTION

This program is concerned with research and development of solid state microwave signal generators and amplifiers. The emphasis of the investigation is centered on studies of active microwave effects in Gunn, LSA, IMPATT, TRAPATT, relaxing avalanche mode and punch-through injection devices, and on related physical electronic techniques. The program is being undertaken to further the understanding of the physical mechanisms and processes which are involved. The main objective is to obtain information of use in the design of improved solid state microwave devices and is directed toward the eventual inclusion of these devices in advanced microwave systems such as are required for communication, detection and other related applications.

The work accomplished during the seventh quarterly period of the program is discussed in this report. Section A deals with the Gunn effect and related research; Section B deals with transit-time devices and related research; and Section C describes the results of solid state materials studies conducted this quarterly period.

A. GUNN EFFECT AND RELATED RESEARCH

INTRODUCTION

This task involves new methods of generating, controlling and amplifying microwave signals using the bulk negative conductivity due to the transferred electron effect in n-type gallium arsenide. Operation at both the transit time frequency and in the limited space charge accumulation (LSA) mode are included. Fundamental concepts as well as materials growth and processing techniques and circuit studies are included in this program. Emphasis is placed on obtaining a better understanding of operation and obtaining better electronic performance. Higher peak and average power, better dc to RF conversion efficiency, more exact frequency control, greater gain-bandwidth products, and improved device reliability are among the objectives of this study.

In Section 1, efforts towards achieving multiple LSA diode operation are described and Section 2 describes some studies of LSA oscillator circuits. The performance of thin LSA diodes is discussed in Section 3 and the continuing work on Gunn effect amplifiers is contained in Section 4. Two new amplifier diodes are characterized and studied for maximum bandwidth and power saturation. The results of a project to develop a wide-range, swept microwave source using Gunn diodes is reviewed in Section 5 and Section 6 discusses progress on a program to

develop a varactor tuned Gunn oscillator. A new project on a pulsed code modulated communication link using a Gunn oscillator is discussed in Section 7. The final sections, 8 and 9, deal, respectively, with the control of silicon impurities in graphite boat solutions grown epitaxial GaAs, and with a study of solution epitaxial and performance of GaAs.

A.1 MULTIPLE LSA DIODE OPERATION

W. L. Wilson, Jr.

As reported last quarter, this work is essentially complete. It has been found that for the sequential combination of several LSA oscillators, the quarter-wave multiple-line junction circuit works very well. Power from each of the individual oscillators may be combined with very little insertion loss, and the effective duty cycle of a transmitter utilizing several LSA devices may be conveniently increased simply as the number of oscillators which are incorporated into the system. Loading of the complete array of devices is straightforward, and the entire lot of them may be tuned up at once. Because the bias voltage to each device is controlled independently, one is able to obtain frequency matching between the individual diodes by a simple adjustment of each of the bias levels. One might also wish to utilize a frequency "multiplexing" scheme, whereby a transmitter would be working at two or more different frequencies at the same time. This

would be very straightforward with this particular LSA system.

The multiple-line circuit does not work well for power combination of several diodes working simultaneously, however. Problems with anti-symmetric modes, unstable locking and poor phase coherence, make this circuit a poor choice when increased peak power is desired. Further attempts at suppression of the anti-symmetric oscillation mode, by the use of resistive elements in each of the radial lines met with no success. Although a wide range of values for the resistive elements was tried, isolation was either such that the anti-symmetric mode was not suppressed, or if sufficient isolation was achieved, then the oscillators would not operate simultaneously in phase, and a poor quality signal would result. Further attempts at making this scheme work in the simultaneous mode have been abandoned.

The hybrid junction power combiner, described in the last quarter, does work very well when simultaneous operation is desired, and is recommended. Tuning is a bit touchy, but not to the degree that it makes the scheme impractical. Good improvements in transmitter peak power can be obtained, and often with a significant improvement in signal quality. The amount of energy stored in the tuning elements increases the effective Q of the diode circuit, and yields a much purer output signal than from the individual oscillators operating alone.

Thus, two circuits have been developed for multiple diode

operation of LSA microwave diodes. For sequential operation of several devices in one transmitter, the quarter-wave power combiner is used. It allows for any number of devices to be connected together, and run one after the other on a time-share basis. To connect two simultaneously oscillating devices together, one may use the hybrid junction, with an adjustable short at one of the ports. This circuit allows combination of the individual powers in a coherent manner, and often brings about signal quality improvement as well.

PLANS FOR THE NEXT INTERVAL

This project has been completed, and no further work is contemplated at this time.

A.2 LSA CIRCUIT STUDIES

William L. Wilson, Jr.

The purpose of this work is to make experimental investigations of multi-port LSA circuits and to evaluate schemes for control of the device performance at its oscillating frequency as well as at multiples and sub-multiples of that frequency. In particular, behavior of the device at the bias port is being investigated, with an eye towards developing a pulsed subharmonic amplifier.

In the last quarter, work with the LSA device in a Multi-Axis Radial Cavity (MARC) was discussed. At that time, a coaxial slug-tuned circuit had been built into the cavity to

function as both a bias insertion port, as well as an active entry to the circuit. By proper choices of tuning slugs in both the usual rf output line, as well as the new bias line, it was hoped that multi-frequency operation of the device could be obtained. Work with this circuit has continued this quarter, and the following conclusions have been made.

Operation of the LSA oscillator is critically dependent on a very low impedance wave-trap at the bias port. Without a strong rf short at the frequency of operation of the device, too much rf energy is lost out the bias line, and rf waveform degradation results. The degradation of the rf voltage across the device can cause the diode to cease operation in the LSA mode, and serious device breakdown phenomena can occur.

It was found in our experiments that this characteristic of LSA operation can be very troublesome. Only very low impedance slugs very carefully tuned would prevent the devices from not operating. The positioning of the slugs was quite sensitive to frequency, and thus, whenever the device bias voltage was changed, or the load circuit was changed, it was necessary to re-tune the bias-line slug positions. The tuning was quite critical, and because the devices were usually undergoing breakdown until the proper tuning positions could be found, a high rate of device failure occured. Because of this high failure rate, and because of the basically oversensitive nature of the experimental arrangement, it was

decided to re-design the experimental cavity to create a more stable LSA environment in which to work.

The circuit which was next developed is shown in Figure A.2.1. The original LSA wave-trap, which had been most satisfactory, was reinstalled in the cavity. This meant that for the time being, the bias port would be left as it was and would not enter directly into the investigations. To create a second port, and to allow for the maximum in tuning flexibility, a third axis was created within the MARC cavity. A second center-conductor rod (somewhat smaller than the rf output rod) was inserted in the MARC. It was connected to an OSM connector mounted into the cavity wall. The OSM connector was then attached to a slotted line, and a second, independently tunable rf output (or input) port was thus created.

The circuit then gave us the option of loading the diode individually at two different frequencies, and of evaluating the performance of the oscillator under a variety of loading and signal insertion situations. The work conducted thus far has involved the use of the added second port as a signal insertion port. Suitable slugs were used in the second line so that signals at the frequency of operation of the LSA device were blocked, and did not escape from the cavity. Signals at other frequencies could, however, enter the cavity through this port.

Studies were made of the behavior of the device when

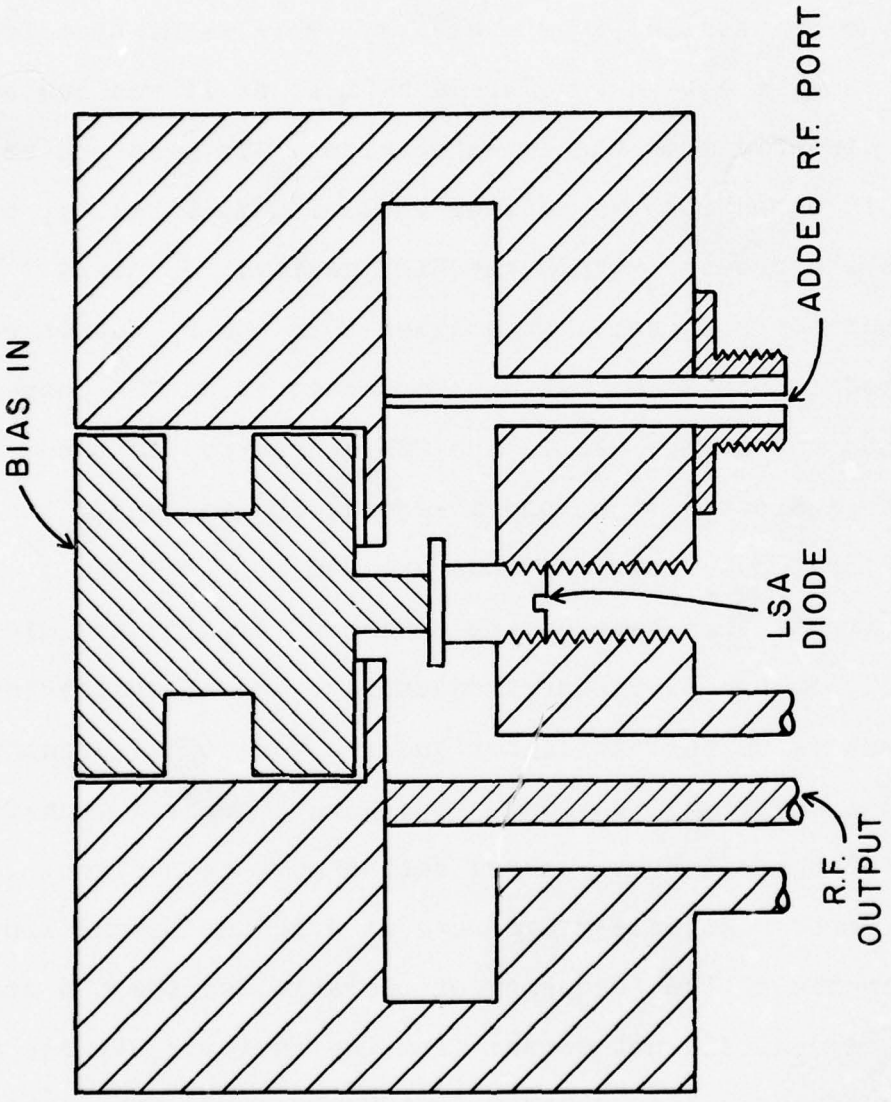


Figure A.2.1 Modified MARC Cavity.

signals at frequencies less than that of the oscillator frequency were injected through the alternate port. It was hoped that either amplification of the incoming signal, or locking of the LSA device to the injected signal would result. In order to observe any possible amplification, a circulator was placed in front of the tuning section of the insertion port, and the signal reflected from the cavity was studied.

The hoped-for amplification of the subharmonic signal was not observed. A variety of tuning schemes, including double-slug tuners in the slotted line, a double stub tuner, and a stub-line stretcher, were all employed at various times. Through careful tuning of these elements, it was possible to arrive at the situation whereby the signal from the oscillating diode did not escape through the insertion line, but a large fraction of the subharmonic signal was being matched to the cavity.

The settings of the tuning elements in the insertion line had some effect on the operation of the LSA diode. This effect could be tuned out, however, by manipulation of tuning elements in the rf output line proper, and device operation at the fundamental frequency optimized independently of the insertion port tuning.

When everything was set up just right, there was still no apparent amplification of the signal inserted into the cavity. The amount of power reflected was the same whether the LSA diode was being pulsed or not. Even when the injected

signal was tuned exactly to a sub-multiple of the oscillating frequency, and a beat signal was observed on the crystal detector at the output from the injection circulator, no gain was obtained.

A small amount of subharmonic locking was observed, however. The range over which the locking took place was small, and the locking gain close to unity, so the phenomenon was of little practical utility. Noticeable improvements of the output spectrum at the oscillating frequency could be observed, however, when the subharmonic signal was injected into the cavity.

The main source of difficulty with this system, as with the previous design, is achieving good coupling between the injected signal and the LSA diode, while not disturbing to too great an extent the loading at the oscillating frequency. Even when the injected signal is well-matched to the MARC cavity itself, it does not appear to be very well coupled to the diode. The next stage in the project will be to re-design the cavity such that the coupling between the insertion line and the diode are considerably stronger than in the present arrangement. This will be accomplished primarily by moving the insertion coax center conductor much closer to the LSA device. Because the line is OSM size, it will be possible to obtain significantly better coupling than exists at present with the circuit. It does not appear that much more can be gained from trying different tuning shcemes for the insertion line itself.

PLANS FOR THE NEXT INTERVAL

Work on achieving good coupling between the inserted subharmonic signal and the LSA device itself will continue. The MARC cavity will be rebuilt to accomodate a considerably closer insert line than at present. Investigations will also be made of the possibility of utilizing one of the later versions of the MARC, the connical MARC, in these studies.

A.3 THIN LSA DEVICES

B. Lind, W. L. Wilson, Jr.*

In order to get a better understanding of the behavior of the thin LSA devices, it was decided to make computer simulations of their behavior in realistic cavities. During this period a fast computer program for these simulations has been developed and tested. The program takes into account the effect of the space charge in the device, the carrier diffusion, and the doping profile. The program can easily be modified to take into account the effect of a temperature gradient across the diode as well. As was discussed in the last Quarterly Report, the space charge in these thin devices is important in determining oscillator behavior, as is the doping profile. The computer program works in time domain since the voltage and current of an LSA device are usually non-sinusoidal.

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*Project Supervisor

The space charge in these devices can be described by the Poisson equation and the continuity equation, together with the v-E characteristic. These equations can be solved directly by a computer by means of difference approximations.[1] However, the computer time will be long, since the steps in time and space have to be much less than the dielectric relaxation time $\tau = \frac{\varepsilon}{qn_o\mu} \approx$ lps and the Debye length $L_d = D \cdot \tau \approx$ 0.14 μm respectively. To obtain a faster program, we use the fact that in the active layer there are regions which are almost free from space charge. These regions are separated by moving accumulation or depletion layers. The field in the regions without space charge is slowly varying in space as long as the background doping density is slowly varying, and thus has to be calculated at just a few points. This idea has often been used[2-3] to simplify the calculations, but in this work we treat the space charge layers with more accuracy by taking into account the effect of diffusion. We approximate our equations somewhat, however, by assuming rectangular shapes of the space charge layers. Because of the method we use for solving the time dependence, we do not need to use a time step, which is less than 1 ps. The time step has only to be short enough to describe the voltage and current wave forms accurately. This means that the time step can be larger and thus increase the calculation speed.

Experimental studies have also been carried out. The

efficiency of 25 μm long diodes in S-band at low duty cycle has been increased from the preliminary 12% to 15-16% by optimizing the circuits. The pulse power was about 8 watts. At 10% duty cycle the efficiency dropped to 9% and because the diode would not take as high a bias voltage, the maximum pulse power dropped to 3.5 watts. At 90% duty cycle the efficiency was 6% and the maximum pulse power 2 watts. The decreases in efficiency and pulse power with increased duty cycle are larger than expected, and the reason for this will be studied more carefully.

PLANS FOR THE NEXT INTERVAL

The computer calculations and the experiment will continue in order to find out how the devices and the circuits shall be designed to obtain optimum performance.

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A.4 GUNN EFFECT AMPLIFIERS

D. Lochhead and J. Frey*

a. Introduction

A method for the design of wideband Gunn Effect Amplifiers

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*Project Supervisor

in microstrip utilizing the dynamic output of a wideband network analyzer is presented. A coaxial multi-slug circuit is used to obtain a prototype design, which is transferred to microstrip using standard techniques. A microstrip amplifier with a maximum gain of 6 dB and 3 dB down bandwidth of 2 GHz is compared to its coaxial prototype.

b. Experimental Results

While the design of reflection-type amplifiers utilizing Gunn effect devices can be pursued with sophisticated and expensive automatic techniques[1] a simpler method, involving prototype modeling of the amplifier circuit in an adjustable coaxial-line system and subsequent transfer to microstrip form, can be used with good results. With "supercritical" devices ($nl>5x10^{11}/cm^2$), thermal effects, in conjunction with non-uniform field profiles within the active device, can lead to stabilization of oscillations if the bias field for amplification is considerably above threshold field[2,3] so that the amplifier circuit's main function is to tune out the capacitance of the device over the amplifier bandwidth desired, optimally matching the negative resistance of the stabilized device to the load. The relatively low Q of the active Gunn effect device can thus be used in conjunction with a low-Q tuning slug to achieve stable amplification over a broad bandwidth.

Our design method utilizes the dynamic wide-band display available from a network analyzer in order to see immediately

the effect of various tuning slugs and slug positions in a coaxial circuit on amplifier gain and bandwidth. A block diagram of the design circuit is shown in Figure A.4.1; originally a 50 ohm coaxial line (N-dimension) with the active device mounted in a coaxial cavity at one end, is connected at plane "A". Matching slugs are moved along the line until optimum prototype amplifier performance -- which may be measured by maximum bandwidth, maximum gain over a small bandwidth, etc. -- is obtained, and the design is transferred, by means of standard procedures,[4] to a microstrip circuit on alumina substrate. Optimum gain-bandwidth product results to date have been obtained using relatively high-impedance slugs (34-45 ohms), that are a quarter-wavelength long at the center of the pass band. Since the maximum rf power that can be tolerated by the network analyzer is about 5 mW, the technique described can be used only to optimize the small-signal behavior of the amplifier, but the amplifier's saturation characteristics will in any case be more dependent upon the device than upon the circuit. The dielectric constant of each alumina substrate is measured[5] before linewidths are calculated but, as yet, dispersion in the microstrip line has not been included in the design.

The "circulator" used in optimizing the circuit design with the network analyzer is within the analyzer itself. A real amplifier once completely designed must include an

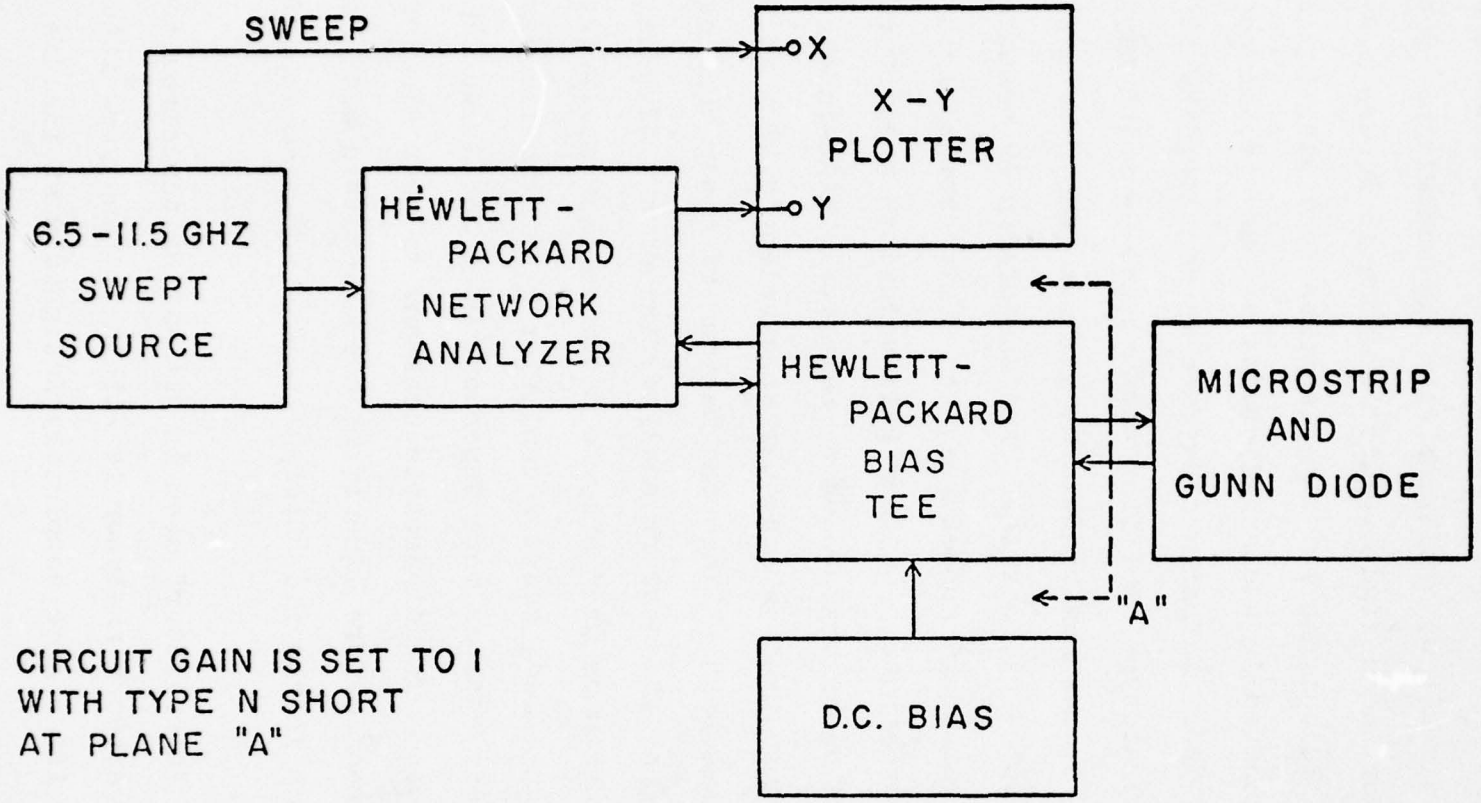


Figure A.4.1 Broadband Amplifier Design Facility. Coaxial Prototype is Connected at Plane "A", for Designing; Microstrip Realization Connected at "A" for Verification.

external circulator, and some degradation of amplifier performance when a non-ideal circulator is used must be expected. If the circulator to be used is measured over the band, however--and its VSWR is reasonably constant over the band--its imperfections can be included in the amplifier design.

A number of amplifiers have been constructed using the techniques outlined above. Comparison of the performance of one of them with its coaxial prototype is shown in Figure A.4.2. For this amplifier, the active device had an nl product of $7 \times 10^{11}/cm^2$, active length 15 microns, and was operated at bias levels between two and three times threshold, for amplification. The device was not of the sandwich n^+-n-n^+ structure; its cathode was an evaporated gold-germanium contact. Performance at higher power levels than possible using the network analyzer, but using a wideband circulator, verified these results, with a saturated (3 dB down) net power output ($P_{out} - P_{in}$) of 24 mW, within 5 mW of the power output available from the diode used as an oscillator at 8 GHz.

The simple technique described for the design of microstrip Gunn effect amplifiers can be used for rapid design of these devices, particularly when the nature of the active device and the bias level at which it is operated remove the major burden of stabilization from the circuit.

PLANS FOR THE NEXT INTERVAL

This is the final report on this subject.

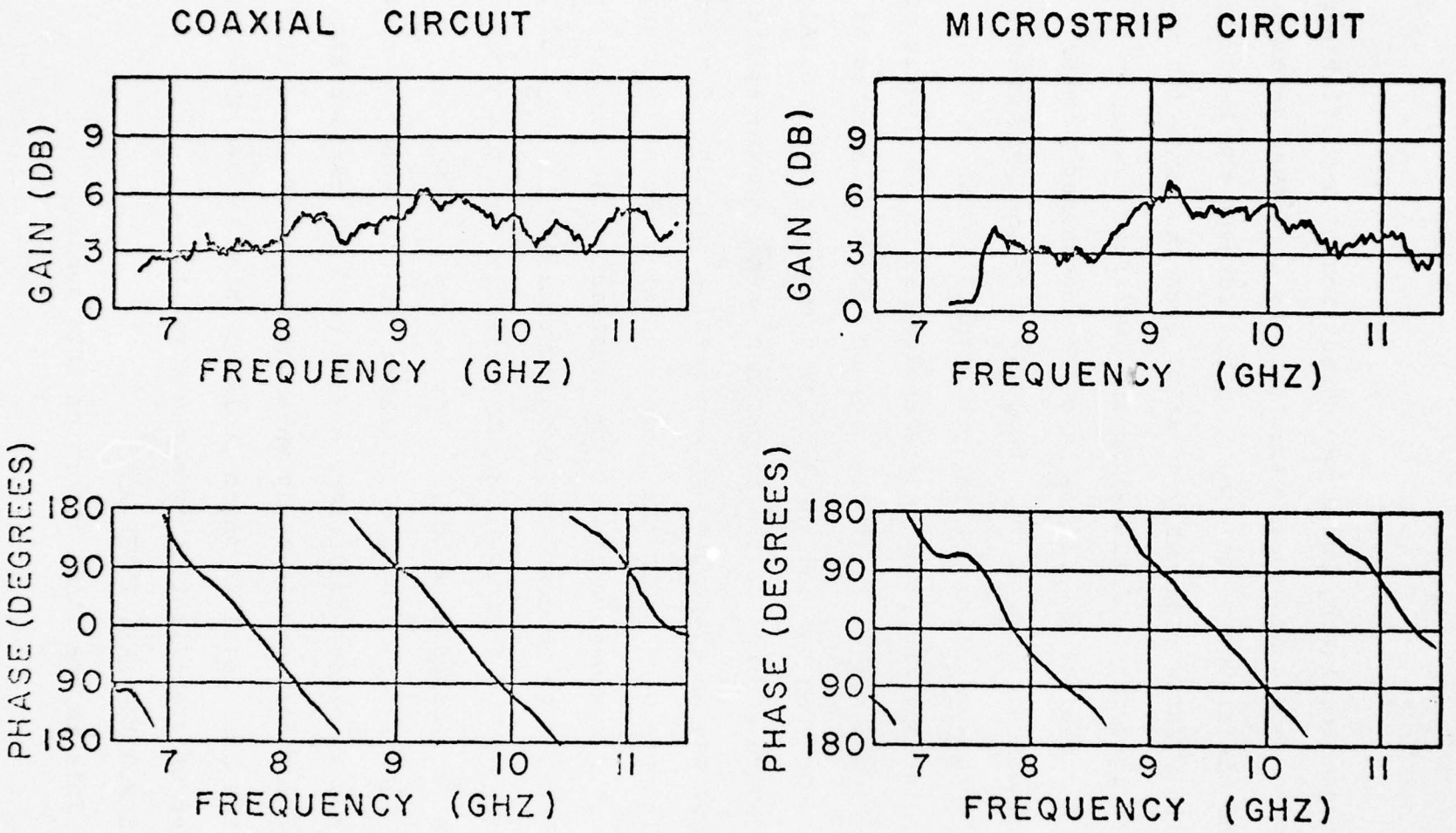


Figure A.4.2 Amplifier phase and gain plots for a coaxial prototype and microstrip realization. $V_b \approx 2V_{th}$.

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A.5 WIDE RANGE SWEPT GUNN MICROWAVE SOURCES

V. Wrick and W.L. Wilson*

Work on this project was completed in this quarterly period and a final report is under preparation. The following is an abstract of this report.

Two circuits for varactor tuning Gunn oscillators have been investigated. The Multi-Axis Radial Cavity (MARC) yields 1 GHz of tuning at 8 GHz with 11 dB power variation. Power output was limited to 18 mw to achieve broad tuning. Tuning discontinuities exist within this range due to spurious resonances in the bias wavetrap.

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*Project Supervisor

The ridge-connected waveguide circuit (RCWC) produces 400 MHz of tuning at 9 GHz with 3.8 dB of power variation. This circuit has also exhibited power in excess of 60 mW for optimum coupling to the output line. Tuning discontinuities are minimized due to improved wavetrap design.

The RCWC oscillator has been used in a phase-locked loop to demonstrate an application for the varactor tuned source. FM noise measurements are made for the free running oscillator, and for several values of gain in the feedback loop of the phase locking circuit.

PLANS FOR THE NEXT INTERVAL

During the next quarterly period, a final report will be issued.

A.6 VARACTOR TUNED GUNN OSCILLATOR

G. Dennis and J. Frey*

a. Summary of Oscillator Design and Performance Criteria

A trade off exists between tuning range and output power in electrically tuned Gunn oscillators.[1] For a large tuning range, tight rf coupling is essential, which means that the tuning element should be as close to the Gunn diode as possible.

Although the objective of this work was to obtain the

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*Project Supervisor

maximum tuning range, it was also desired to maximize output power for a given circuit.

A transmission line analysis of sample oscillator circuits, both with and without the varactor, was made so that an expression for frequency and variation Δf as a function of varactor bias could be calculated. Both parallel and series configurations were analyzed and their performance characteristics compared.

b. Calculation of Gunn Diode Capacitance and Negative Resistance

Using a measurement of the dc resistance R_0, the Gunn diode "cold" or unbiased capacitance can be calculated using the formula:

$$C = \frac{\varepsilon A}{d} \qquad (1)$$

where ε = dielectric constant of GaAs

A = area of the junction region

d = length of the diode.

Using the d.c. resistance,

$$R_0 = \frac{\rho d}{A}$$

where ρ = resistivity of GaAs at a given donor density, N_d, and

$$\rho = \frac{1}{q\mu_n N_d} \qquad (2)$$

where q = electronic charge and μ_m = electron mobility for

a given donor density, the Gunn diode capacitance can be written as

$$C = \frac{\varepsilon}{R_0 N_d q \mu_n} \tag{3}$$

Substituting values for ε and μ appropriate for GaAs below velocity saturation, a measured value of $R_0 = 1.6\Omega$, and $N_d = 10^{15}/cm^3$; the capacitance of the Gunn diode used in the circuits to be described below was about 0.6 pf.

The negative resistance of the Gunn diode was calculated using the formula[2]

$$-R = 10\ R_0\left(\frac{V_b}{V_t} - 1/2\right) \tag{4}$$

where V_t = threshold voltage of the Gunn diode

V_b = the bias voltage where the diode is operated.

The negative resistance was -9Ω at the operating point used.

c. Transformation of the Coaxial Circuit into Microstrip

Prototype design of the Gunn oscillator circuits was done using a 50Ω coaxial line with two adjustable slug transformers. The slug impedances which gave the maximum output power, 60 mW for the diode considered above, were of 10Ω impedance, $\lambda/4$ long at 10 GHz, as shown in Figure A.6.1. The positions of the slugs and the diode were measured and recorded.

The slug impedances can be transformed into stripline dimensions using the theory of Wheeler.[3] The lengths between

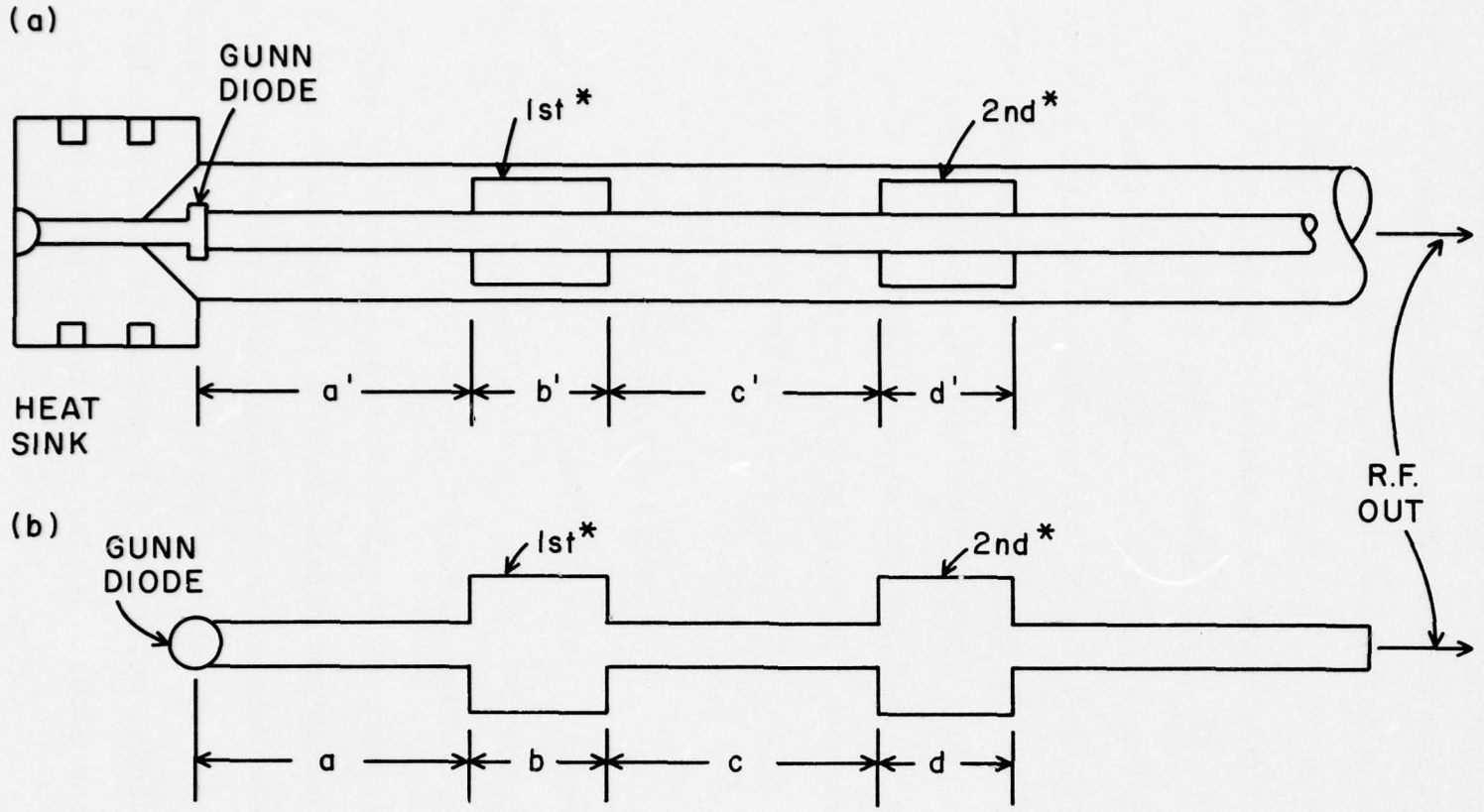


Figure A.6.1 (a) Coaxial, and (b) Microstrip configurations used for parallel tuned circuit.

the Gunn diode and the two slugs were calculated in air wavelengths, λ_0 at the center frequency of the tuned band. Since the dielectric constant of the ceramic is higher than that of air, the wavelength λ_m in microstrip is shorter than the air wavelength. For a dielectric constant of ten, $d_o/d_m = 2.7$. At f = 9.4 GHz, $\lambda_0 = 3.2$ cm and $\lambda_m = 1.2$ cm.

d. Microstrip Circuit - Untuned Gunn Oscillator

The equivalent circuit for the microstrip line appears in Figure A.6.2. C_p represents the parasitic package capacitance of the Gunn diode, which was measured and found to be .27 pf. A Smith Chart was used to reflect the slug admittances back to the diode plane. Using the calculated and measured values of C_D, C_p and -G, the diode admittance was calculated to be

$$Y_d = -5.5 + j\ 2.25 \text{ mho.}$$

e. The Parallel Tuning Circuit

The equivalent microwave and d.c. bias circuits for this arrangement are shown in Figure A.6.3.

f. Performance of Parallel Varactor-Tuned Oscillator

The inductance and capacitance of the microwave circuit, including the effect of the varactor, when reflected back to the diode plane and combined with the parasitic capacitance of the Gunn diode, determine a frequency of resonance in the vicinity of the diode. A simple analysis can be done to

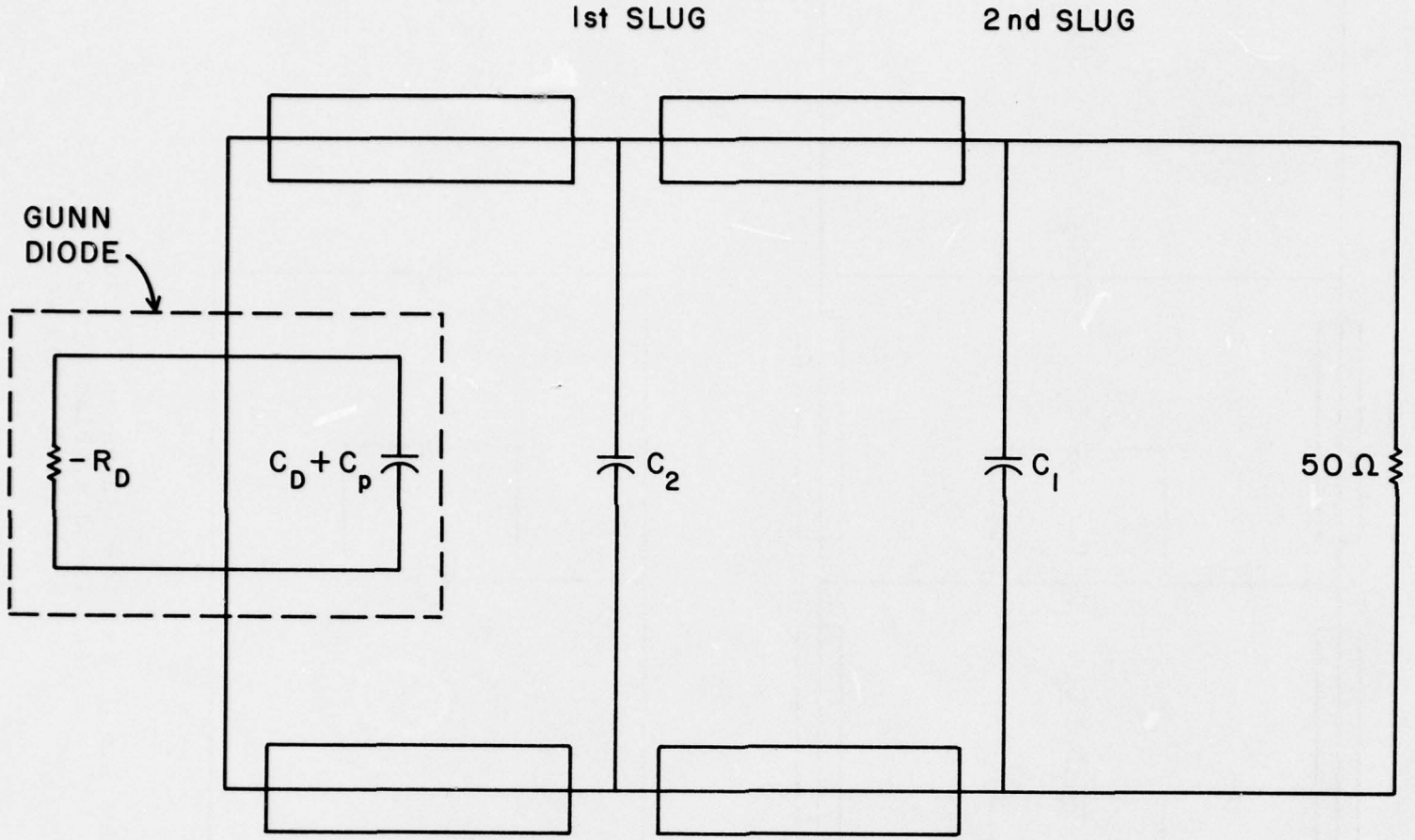


Figure A.6.2 The equivalent circuit for the microstrip line before the addition of the tuning element.

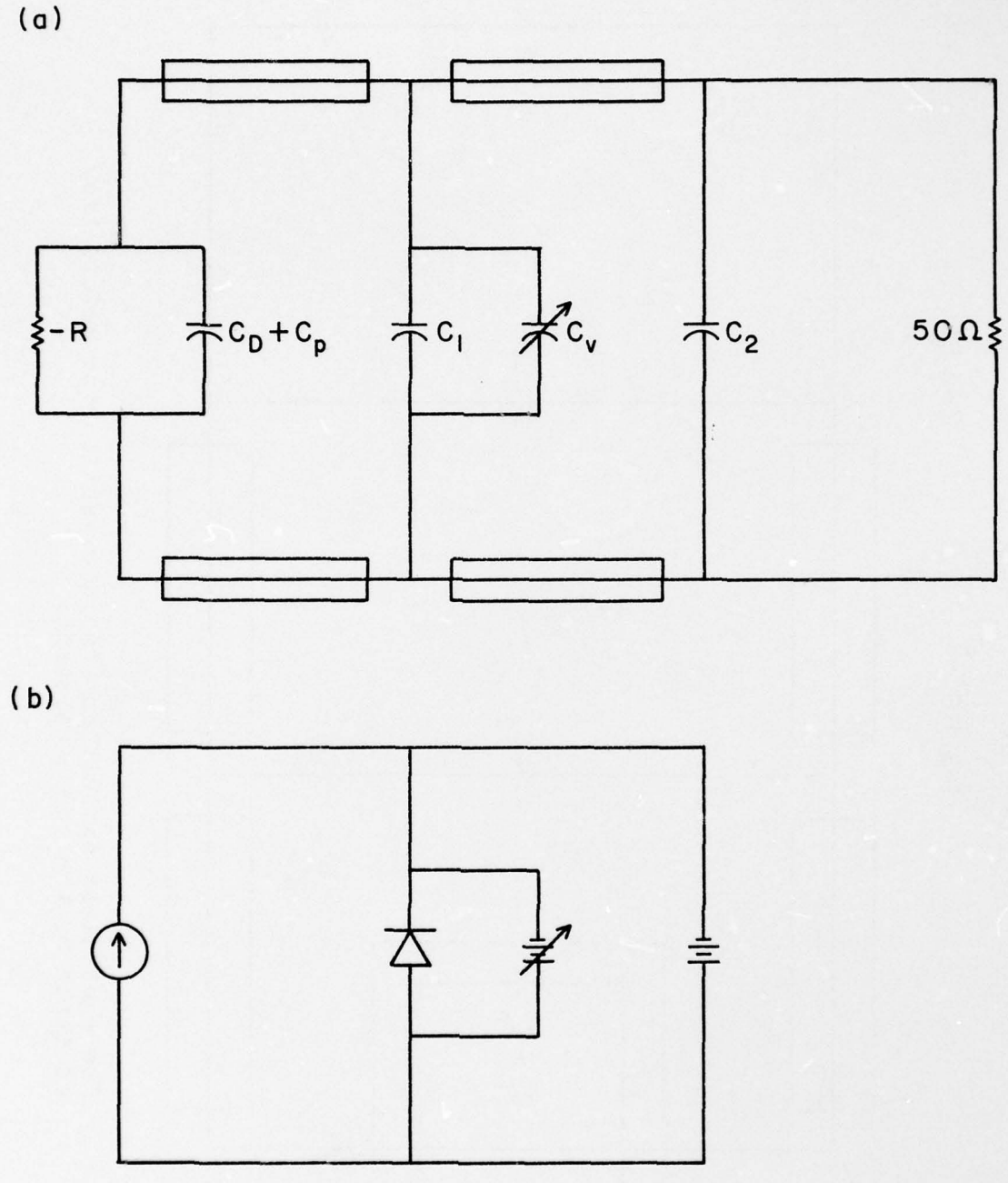


Figure A.6.3 (a) The Equivalent Circuit, and
(b) The d.c. Bias Circuit
for a parallel tuned oscillator.

determine the approximate effect of changes in the varactor bias-level capacitance on this resonant frequency. This approximate analysis shows that the change in resonant frequency that occurs, when the varactor capacitance is added to the circuit, is given by

$$\Delta f = -1/2 \; L/L' \; f_o \qquad (5)$$

where f_o = resonant frequency without varactor in circuit

L = inductance of resonance circuit as seen at Gunn diode plane

L' = inductance of varactor as seen at Gunn diode plane (transformation of varactor capacitance).

L' was calculated for each varactor bias point by adding the varactor capacitance to that of the first slug in the transmission line analysis done before, and reflecting the new admittance back to the diode plane. Since the change in $\frac{\Delta f}{f_o} << 1$, $f_o = 9.4$ GHz was used as the resonant frequency throughout the calculations.

The actual tuning range was from 9.36 GHz with no bias voltage on the varactor to 9.34 GHz with a bias of -40 volts on the varactor. Tuning and power variation of this circuit are shown in Figure A.6.4; theoretical tuning for 100% varactor "efficiency" (coupling) is shown as the "100%" curve. To quantify this coupling efficiency, a simple algorithm was applied by means of which, for 100% coupling the total

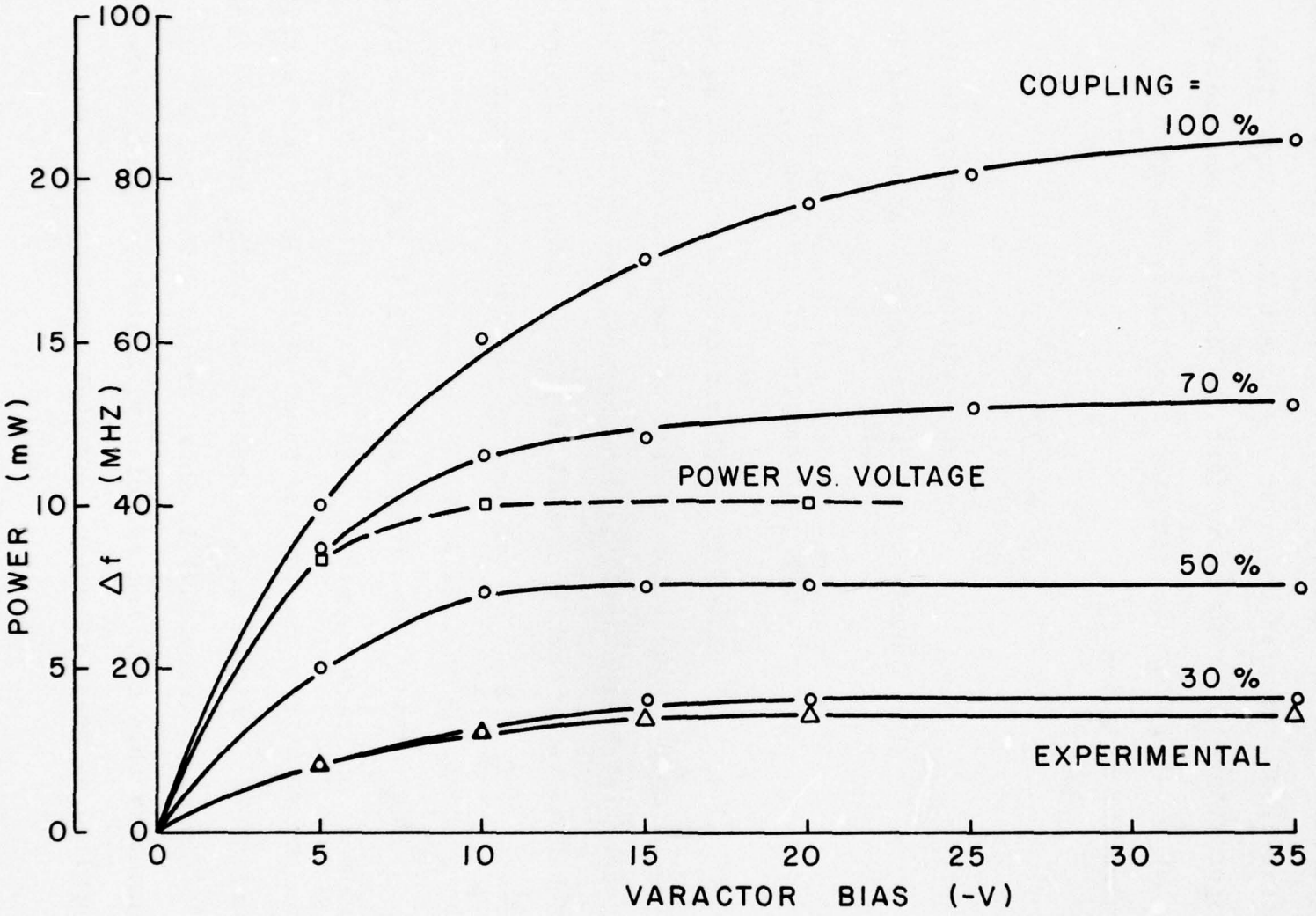


Figure A.6.4 Performance of the Parallel Tuned Oscillator.

varactor impedance was reflected to the diode plane; for 50% coupling, only one-half of the varactor impedance was reflected to the diode plane; for 40% only two-fifths of the varactor impedance was reflected, etc. The varactor was obviously, then, not in a good position for tight r.f. coupling. Since most field lines pass from the stripline through the substrate to the ground plane the efficiency of coupling with the varactor was poor. Only approximately 30% coupling is achieved with the varactor in the position used.

The output power remained relatively constant over the entire tuning range, ranging from 8.5 mW to 10 mW. This uniformity was also a function of weak coupling, since varactor losses did not affect the circuit much.

g. Performance of Series-Tuned Gunn Oscillator

The basic series tuning circuit was realized much in the same way as the parallel circuit. The Gunn diode was first mechanically tuned for maximum r.f. power. The distances between the slug and the diode were calculated in the same manner as before. The circuit used and its equivalent circuit are shown in Figures A.6.5 and A.6.6. The varactor chip was, for this experiment, placed in series with the microstrip line and gold wire was used to connect the diode to the microstrip line. For this circuit, the equation analogous to (5) is

$$\Delta f = 1/2\ f_0\ C'/C. \qquad (6)$$

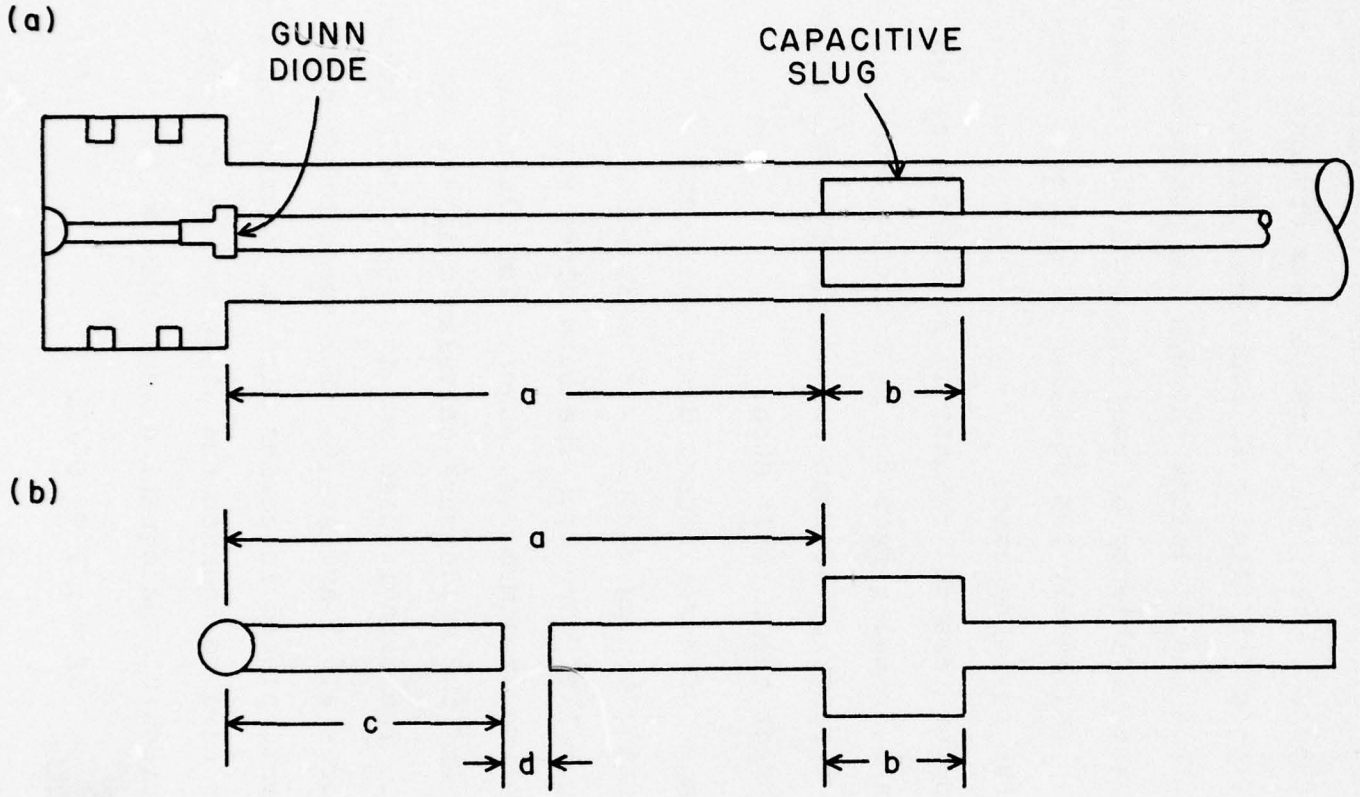


Figure A.6.5 (a) Coaxial, and (b) Microstrip Configuration used for series tuning.

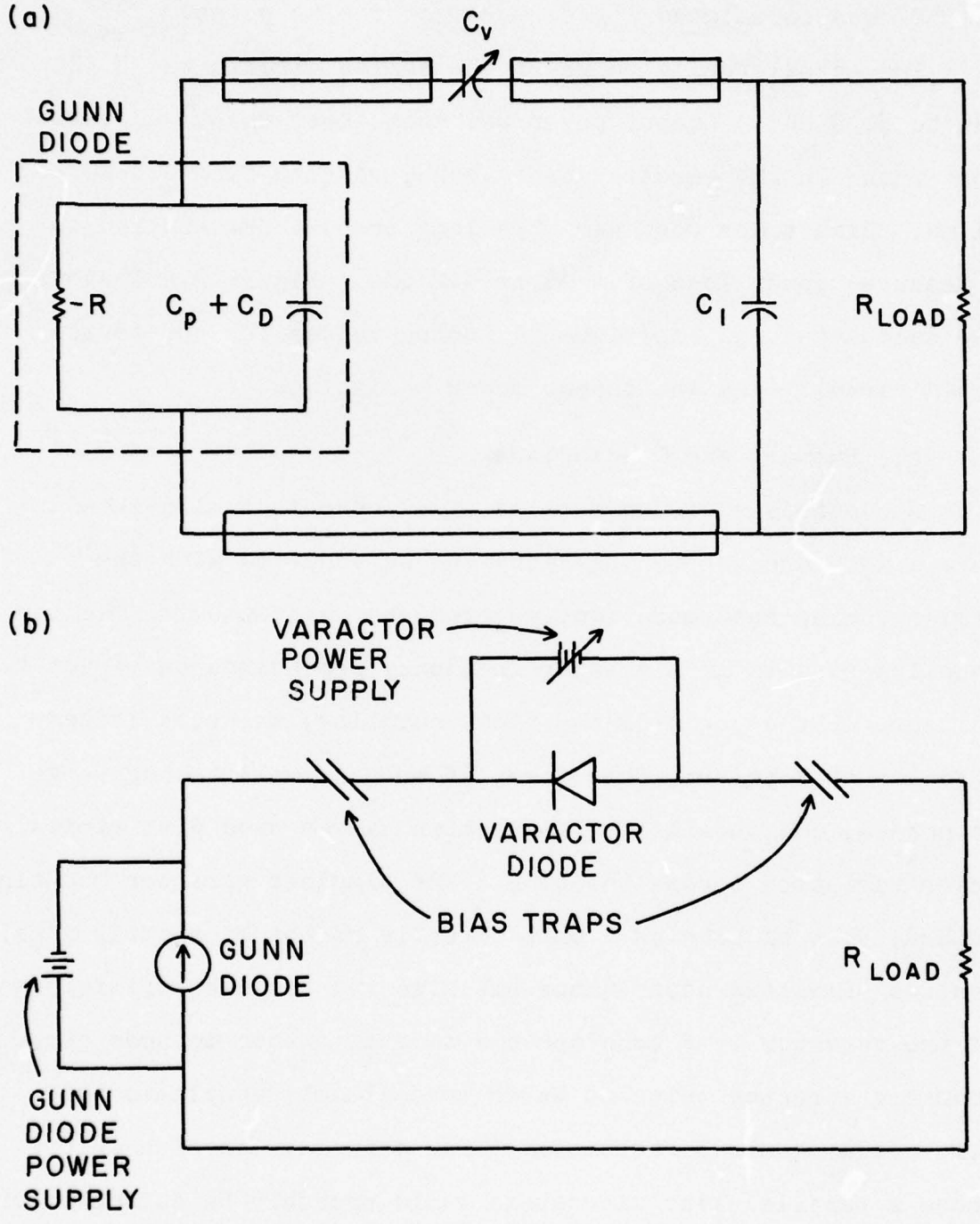


Figure A.6.6 (a) Equivalent Circuit and (b) d.c. Bias Circuit for Series Tuned Oscillator.

C′ was calculated for each varactor bias point.

The actual tuning range of the series circuit was 8.32 GHz to 8.20 GHz. Output power was much lower than, and varied more than in the parallel tuned case, ranging from 0.6 mW to .1 mW. Bias traps used were $\lambda/4$ long at 6.25 GHz and led to a measured power loss of 4 dB at 8.2 GHz. Figure A.6.7 shows the calculated and experimental tuning values for the series tuned circuit, and the output power variations.

h. Summary and Conclusions

A comparison of two methods of electronic tuning shows that a much broader tuning range can be achieved with the series tuning configuration, as predicted by Cawsey.[3] Tighter coupling results in a greater frequency dependence on varactor voltage. But along with the tight coupling, varactor losses affect output power. Therefore, if only a small tuning range is needed, the parallel configuration can be used with minimal power variation across the band. The simplest varactor mounting method, that of placing a chip directly on the microstrip line, reduces parasitic capacitance but also reduces the efficiencies of the varactor by a considerable amount. Other methods of mounting varactor chips so as to more closely couple to the r.f. field should be attempted. For example, use of a chip above a parallel-line microstrip would probably be suitable for varactor-tuned circuits.

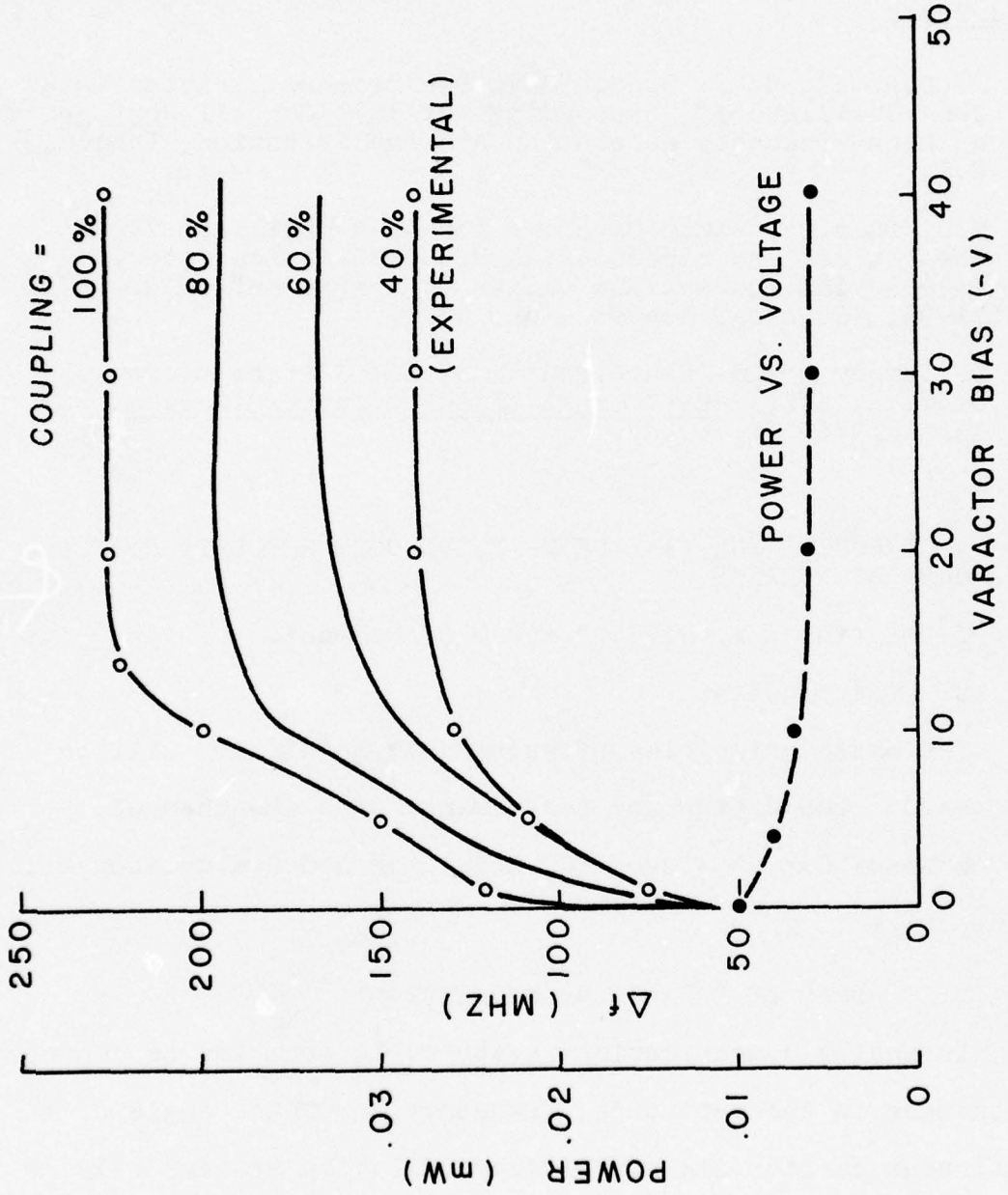


Figure A.6.7 Performance of the Series Tuning Varactor.

PLANS FOR THE NEXT INTERVAL

This project is now complete.

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A.7 A COMMUNICATION LINK USING PULSE-CODE MODULATION OF A GUNN OSCILLATOR

T. Martin, W.L. Wilson* and G.C. Dalman*

a. Introduction

The basic principles of pulse-code modulation will be discussed. The design and performance of a one-channel, narrow bandwidth, 16-level PCM modulator and demodulator will be described.

b. Theory of Pulse-Code Modulation

In analog communications systems, information is conveyed by changes in the amplitude, frequency, or phase angle of a continuous carrier signal. Pulse modulation systems rely on the sampling theorem, which states that if an analog signal is

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*Project Supervisor

sampled at periodic intervals, then the instantaneous amplitude of the waveform at each sample time carries enough information to accurately reproduce the analog signal (providing the sampling rate is greater than 2 f_{max}, where f_{max} is the highest-frequency component of the analog signal). Pulse modulation schemes may be divided into two classes - those in which some parameter of the pulse varies continuously (i.e., pulse amplitude modulation, pulse width modulation, pulse position modulation); and those in which the pulses carry information in digital form. The latter scheme is pulse-code modulation.

Binary PCM (henceforth referred to as simply PCM) has several advantages over conventional modulation and over the non-coded pulse schemes. The biggest advantage is that PCM information is conveyed only by the presence or absence of a pulse at a particular, known time. The receiver need not be concerned with the amplitude, width, or precise position of the pulse. This characteristic makes PCM the obvious choice for transmitting information through a noisy channel. PCM is also ideally suited to multiplexing, because the pulses (or lack of pulses) occur at a precise, known rate.

c. Outline of Circuitry Required for PCM

The basic units of a PCM system are an analog-to-digital (A/D) converter at the transmitter, and a digital-to-analog (D/A) converter at the receiver. The other requirement is some form of synchronization to separate the pulses corresponding to one sample time from the others.

Analog to digital conversion is accomplished in this system as follows (refer to Figure A.7.1). The sampling period is 100 μ sec (sample rate is 10 kHz). The start of a sample period triggers a linear ramp generator. This ramp is compared with the analog voltage, and when the ramp equals the analog voltage, the comparator output changes states. The ramp continues until it is cut off, a precise interval of time after it started. The output of the comparator then changes back to its original state. The comparator output is thus a pulse whose width is inversely proportional to the amplitude of the analog signal. The ramp is kept as short as possible to minimize distortion due to variation in the sample rate.

This variable-width pulse gates clock pulses into a 4-bit binary counter, and is set up so that a maximum of 15 clock pulses enter the counter for a given sample. The output of the counter is connected to the parallel inputs of a shift register, which transforms the 4-bit number into serial form. These serial pulses control a monostable, which is adjusted to give the desired width of pulse. Another monostable is triggered by the beginning of each sample period, which provides synchronization at the receiver. Figure A.7.2 shows the relationship between the various pulses used in this scheme. Waveform I shows the analog signal and the timing ramp to the comparator. Waveform II is the variable-width pulse from the comparator. Waveforms III to VI are the clock pulses divided

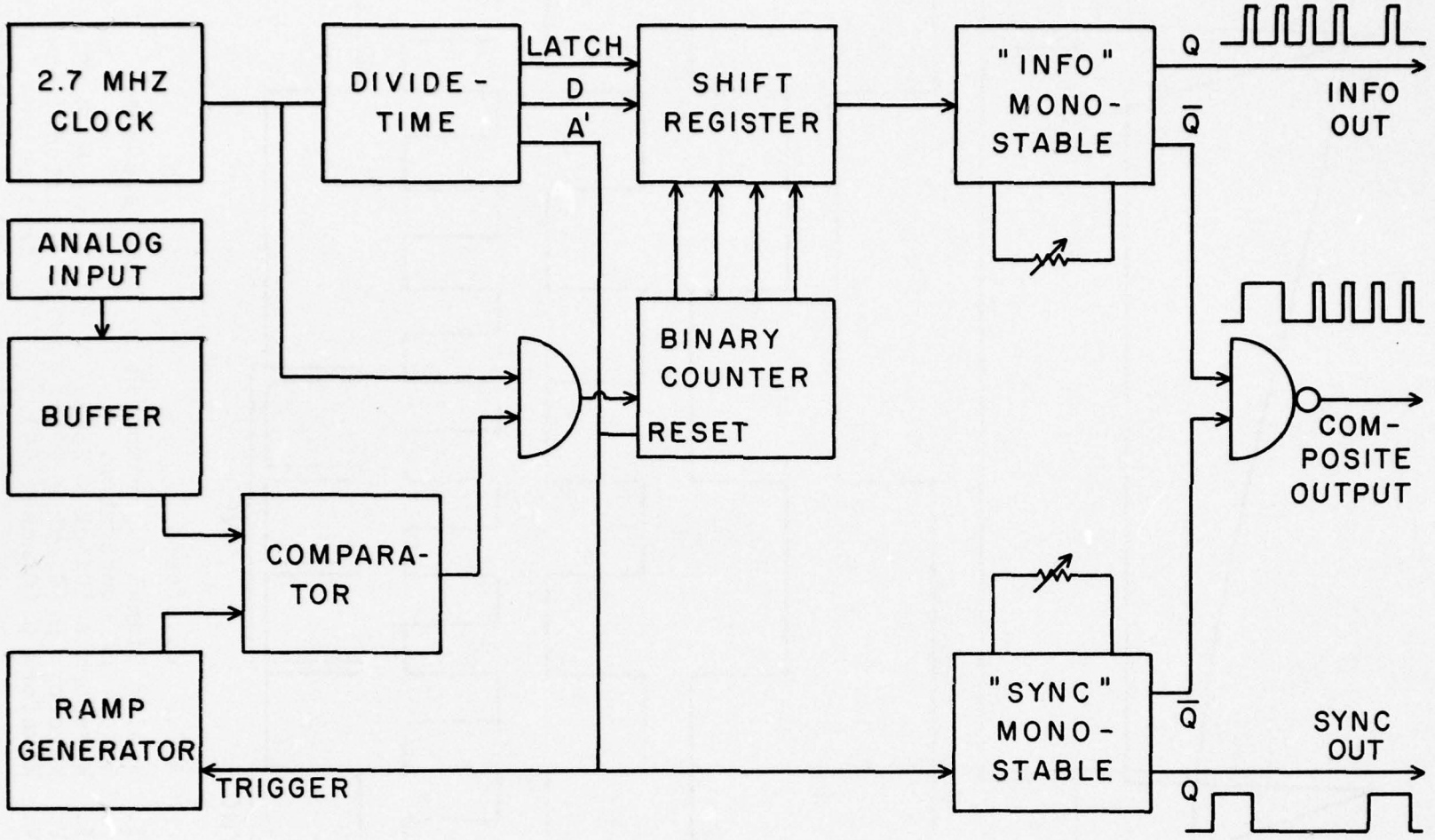


Figure A.7.1 Block Diagram of Modulator.

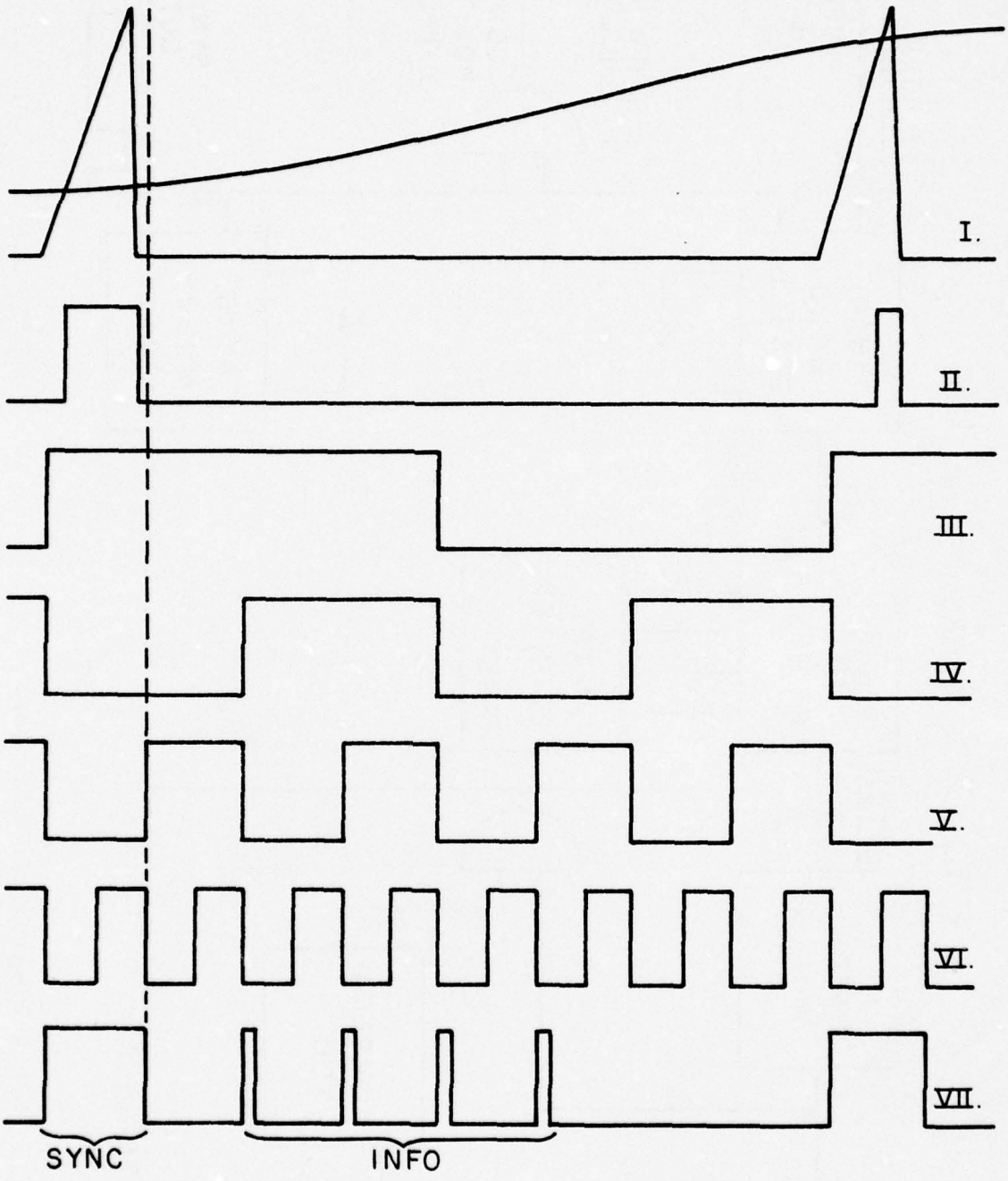


Figure A.7.2 Waveforms

I. Analog Signal Superimposed on Ramp Waveform.
II. Output of Comparator.
III. Waveform A (Clock ÷ 256).
IV. Waveform B (Clock ÷ 128).
V. Waveform C (Clock ÷ 64).
VI. Waveform D (Clock ÷ 32)
VII. Position of sync and info pulses in composite output waveform.

by successful factors of two. The last waveform (VII) shows the composite output waveform which contains the sync pulse, and the BCD pulses delivered in a chain.

The demodulator makes use of a simple but effective method of D/A conversion. If the four pulses in each group are transmitted back-to-front (i.e., so that the pulse corresponding to 2° is transmitted first) then the pulse group may be demodulated by applying it to an RC network, as described fully in the circuit description. Synchronization is provided by making the sync pulse longer than the information pulses, so that the receiver can differentiate between the pulses. The recovered sync pulse in the receiver is used to dump the charge remaining on the RC demodulating network, so as to ready it for the next 4-bit "word".

d. Circuit Description

1. Modulation

a. Crystal-Controlled Clock Source (Figure A.7.3)

The digital system requires an accurate clock pulse generator. The frequency of the clock pulses is such that 15 pulses occur in the time the sampling ramp is on. The circuit shown is a crystal-controlled oscillator (Q_1 and associated quartz crystal) working at 10.8 MHz. Transistor Q_2 is an emitter follower to prevent loading of the oscillator. The output of the emitter follower does not go to zero volts however, so the next stage, Q_3, merely acts as a buffer to drive the 4-bit

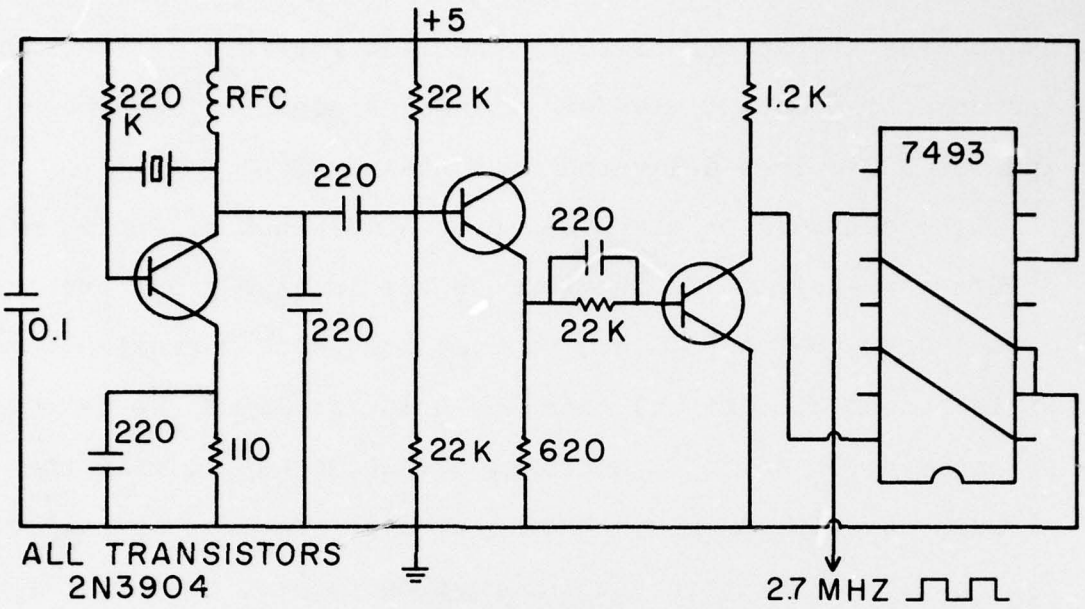


Figure A.7.3 Crystal Controlled Clock.

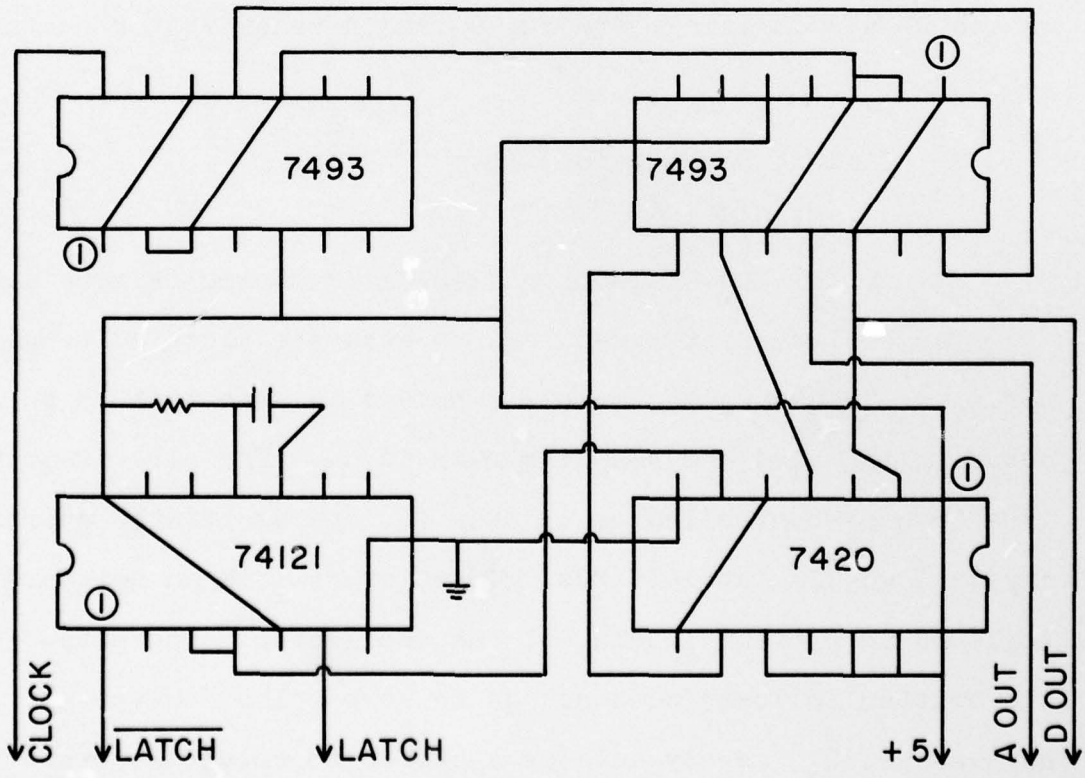


Figure A.7.4 Dividing and Timing Circuit.

binary counter (used here as a divider). The output of the binary counter is a square wave of frequency f/2, f/4, f/8, or f/16, where f is the frequency of the crystal oscillator. The frequency chosen for this system is f/4, or 2.7 MHz.

b. Timing Generator (Figure A.7.4)

The timing generator takes the clock output (2.7 MHz) and further divides it to give waveforms to be used for triggering each sample period, triggering the synchronization, "latching" the shift register, and clocking the shift register. The operation of this unit is seen best by referring to the block diagram (Figure A.7.1), and the waveforms shown in Figure A.7.2. The dividing chain yields waveform A, used to initiate each sample period; waveform D, which is used to clock the shift register; and waveforms B and C, which, when properly combined with A, give a pulse which occurs at a precise position during the sample period. The trailing edge of this pulse triggers a monostable, which puts out a latch pulse for the shift register.

c. Comparator Operation (Figure A.7.5)

Referring to the schematic, the comparator operation is straightforward. Transistor Q_4 is a current source, charging C_1 or feeding Q_5, depending on the voltage at the base of Q_5. The monostable is triggered by A' (a short pulse marking the beginning of each sample period). After being triggered, the output at pin 1 goes from +4 volts to zero, causing Q_5 to shut off for a time governed by R_1 and C_2. When the monostable

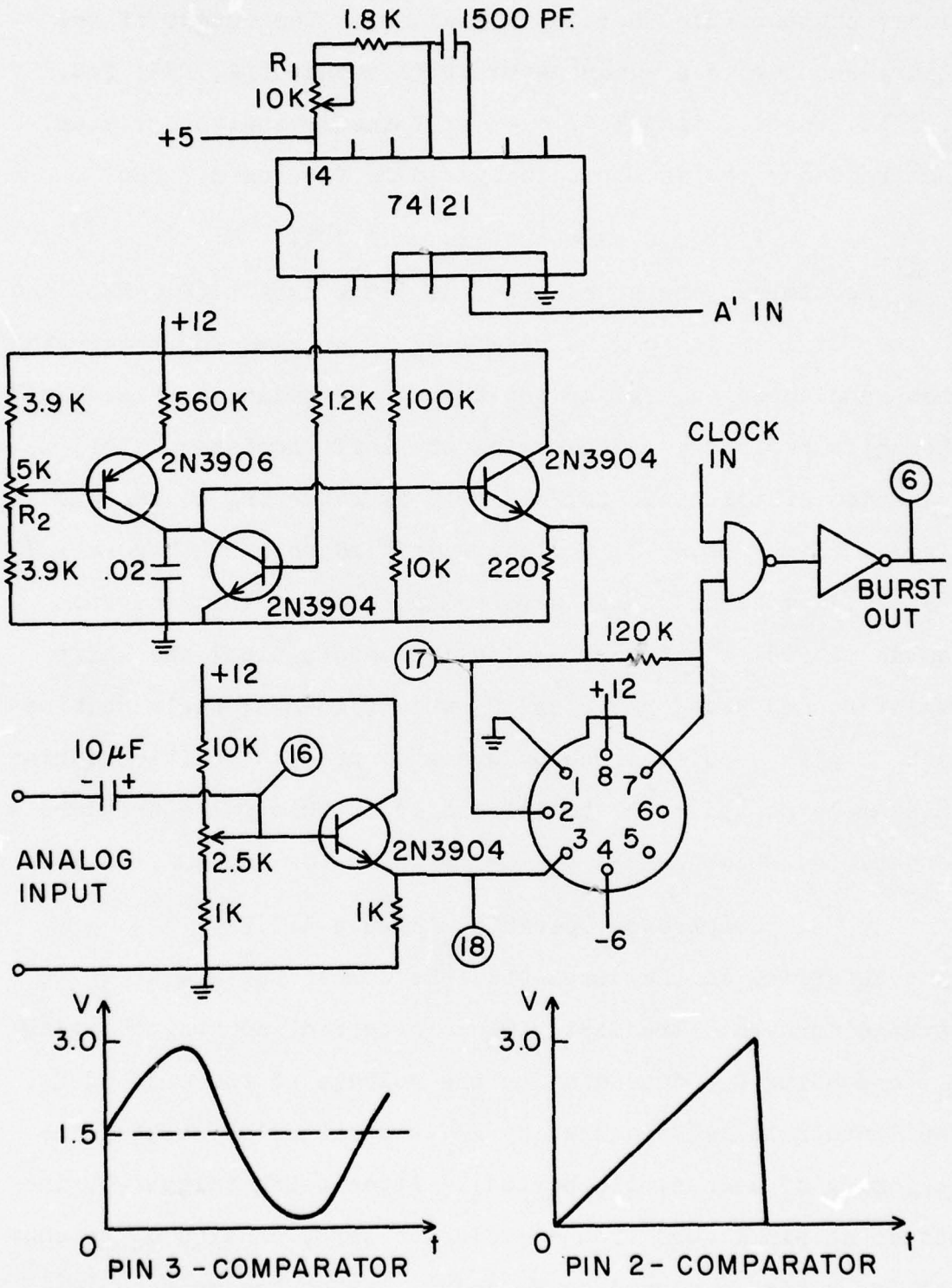


Figure A.7.5 Triggered Ramp and Comparator Circuit.

returns to its normal state (+4 volts at pin 1), Q_5 again conducts, holding the collector of Q_4 at ground. Transistor Q_6 is an emitter follower to buffer the voltage on C_1 from the comparator loading. The voltage at the emitter of Q_6 is normally zero, until A' triggers a ramp, whose duration is controlled by R_1. Potentiometer R_2 controls the current from the source Q_4, hence the slope of the ramp. The analog input voltage is capacitively coupled to the base of Q_7, which is biased to give a quiescent emitter voltage of one-half the maximum ramp voltage. This quiescent point is controlled by R_3. The two voltages (emitters of Q_6 and Q_7) are compared by IC_1; the output of this comparator is TTL compatible ("on" = ∿5 volts, "off" = ∿0 volts) and is applied, along with the clock signal, to a 2-input NAND gate. The output of this gate is a burst of from 0 to 15 clock pulses. This output is inverted to provide the burst, which is the input signal for the counter.

d. Counter, Shift Register, and Output Monostables (Figure A.7.6)

The clock burst from the comparator board is fed into the 4-bit counter. This counter is reset at the beginning of each sample period by A', readying it for the counting. The clock burst occurs during the first 6 μ sec of the sample period; after the ramp returns to zero, counting stops and the number is held. This number is transferred to the shift register during the "latch" pulse, which comes from the timing board. The contents of the shift register are then clocked out serially

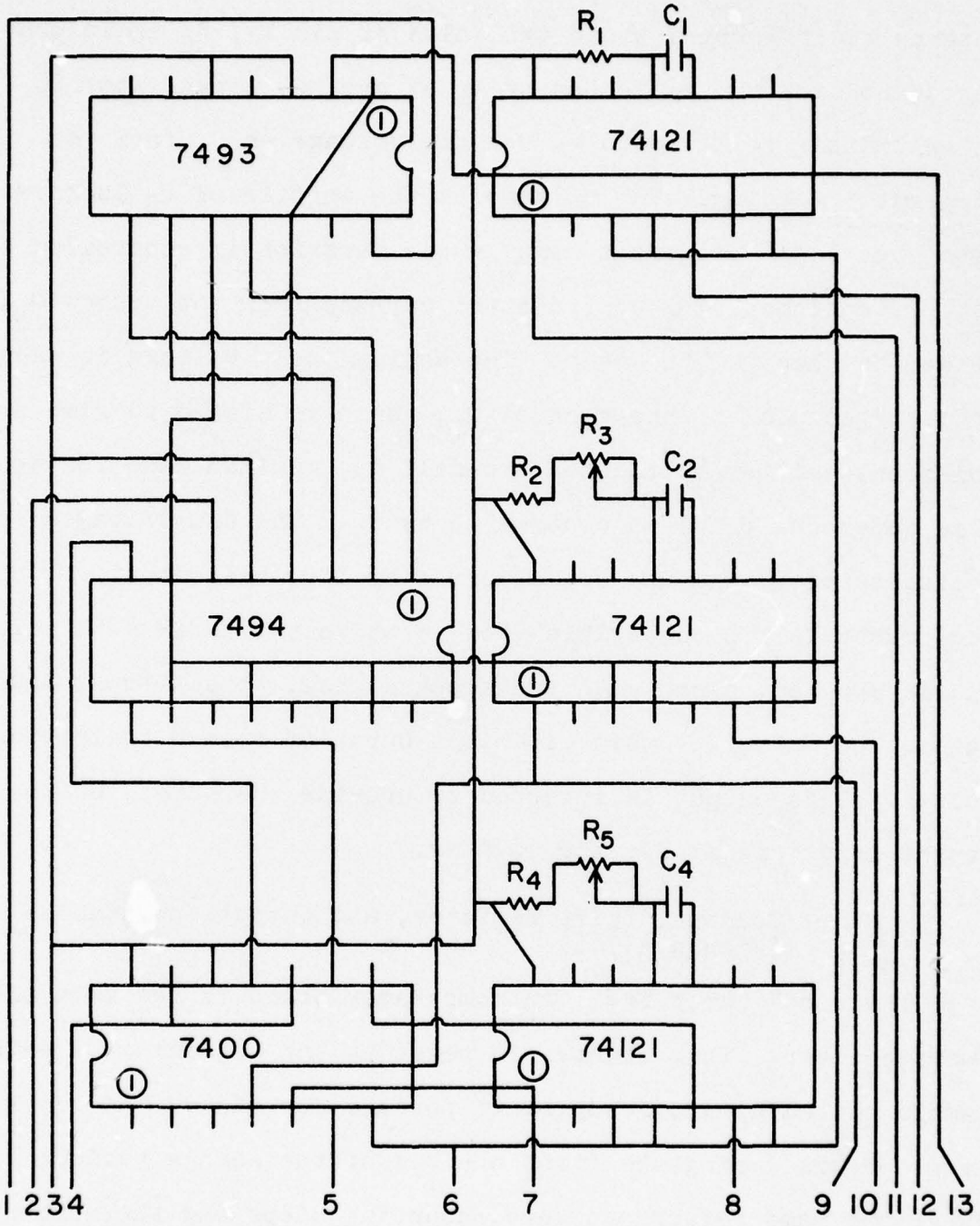


Figure A.7.6 Counter, Shift Register and Monostables.

1. Burst in
2. Latch in
3. +5 Volts
4. D in
5. Compos. out
6. Ground
7. $\overline{\text{Info}}$ out
8. Info out
9. $\overline{\text{Sync}}$ out
10. Sync out
11. $\overline{A}'$ out
12. A in
13. A′ out

by clock waveform D. The output of the shift register, "AND"ed with D, is fed to the input of the "info" monostable, which triggers on the positive-going edge. The "sync" monostable has as its input A', and puts out a pulse indicating the beginning of the sampling period. Two monostables are used (one for "info", one for "sync") so that the duration of the sync pulse may be made longer or shorter than the information pulses. The pulse widths are controlled by the variable resistors associated with each monostable. The inverted outputs (normally high) of both monostables are fed to a NAND gate, whose output is the composite waveform shown in Figure A.7.2. It is this waveform which will control the pulse transmitter.

2. Demodulation

The input to the demodulator (Figure A.7.7) is a reconstructed pulse train ("info") and sync pulses. The arrival of a sync pulse causes Q_3 to conduct, dumping the charge on C_1. The sync pulse is "off" before the first info pulse arrives. The info pulses control the current flow through Q_2, which is normally zero because the base is clamped high. When a pulse lowers the base voltage, current flows to put a charge on C_1. Because the info pulses are reconstructed, they all have the same amplitude and duration. Thus, each pulse raises the voltage on C_1 by a constant amount Δv. Resistor R_1 drains off the charge on C_1, and is adjusted so that the voltage on C_1 due to pulse 1 (Δv) decays to 1/2 Δv at the instant pulse 2

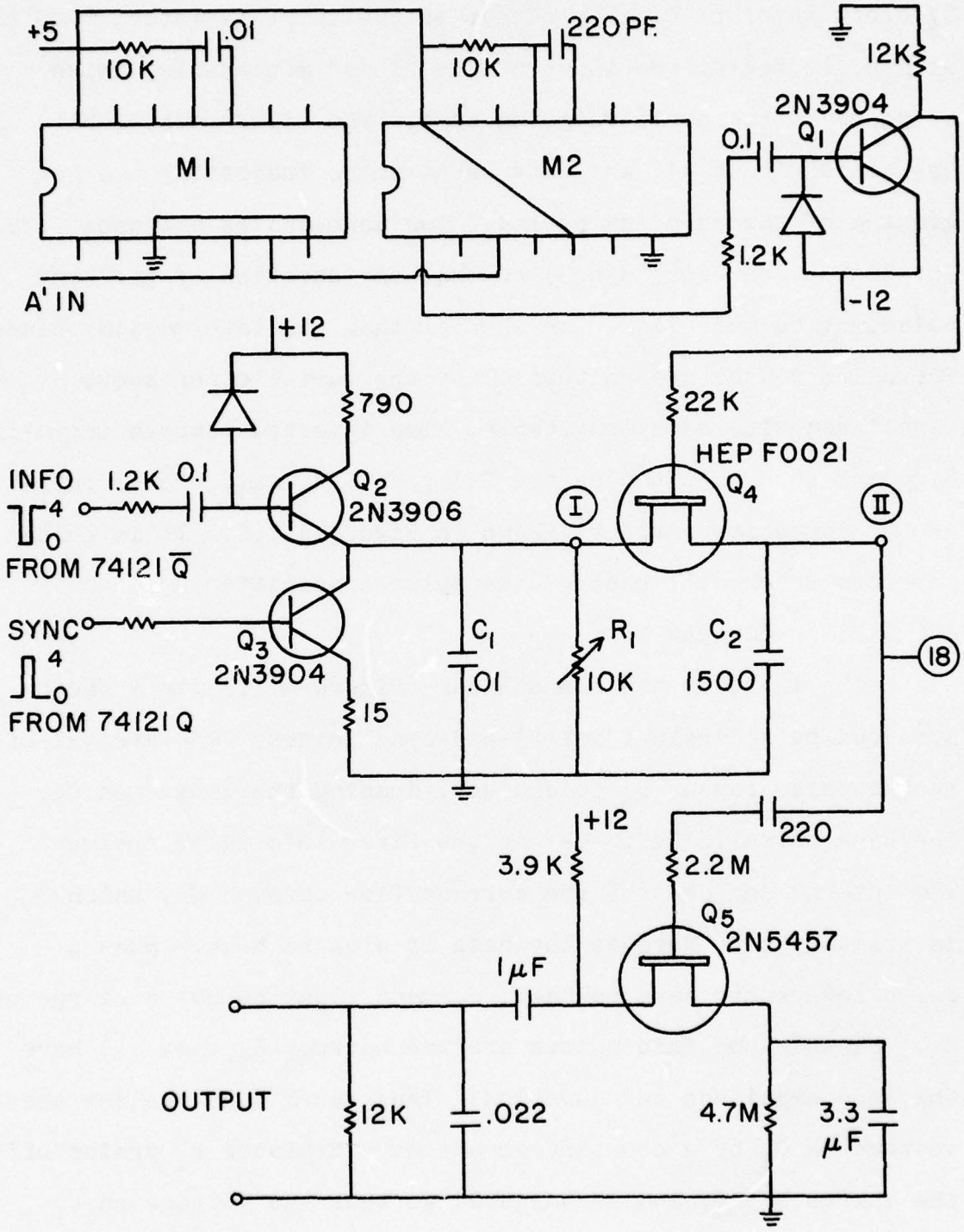


Figure A.7.7 Demodulator Circuit.

arrives. (This is of course assuming both pulses 1 and 2 were present.) By referring to Figure A.7.10, it is seen that the voltage on C_1 anytime after the 4th pulse is directly proportional to the value of the binary number. As stated before, this scheme works because the binary number is transmitted back-to-front.

The combination of JFET Q_4 and C_2 is a sample-and-hold circuit, which samples the voltage on C_1 at some time after the arrival of the fourth pulse. The time at which C_1 is sampled depends on the width of the monostable pulse (M1); the length of the sample is controlled by M2. The normally-high ($\bar{Q}$) output of M2 is fed to the base of Q_1. The output at the collector is normally -12 volts, because the transistor is conducting (saturated); the arrival of the pulse (from 4 to 0 volts) turns off the transistor, causing the collector voltage to go to zero. Thus the gate of the JFET (Q_4) is normally held at -12 volts, hence cutting off conduction from source to drain (this is the "hold" state). When the gate goes to zero volts, the FET conducts, equalizing the voltages on C_1 and C_2. (This is the "sample" period).

The output of the sample-and-hold is a step function which approximates the analog signal at the transmitter (Figure A.7.12). The JFET stage (Q_5) is simply a high-input-impedance, low-gain amplifier, to avoid loading the capacitor C_2. The RC network in parallel with the output of this stage is a low-pass filter

which begins rolloff at about 2 kHz. This eliminates much of the high-frequency noise associated with the step-function input. The output level is approximately one volt, compatible with most audio amplifier inputs.

3. Photographs

All photographs were taken with a 500 Hz sine wave as the input to the modulator. The photographs are intended to give a clearer understanding of the circuit operation, and give an idea of performance of the overall modulation-demodulation system. Neither time scales nor voltage scales are given, since it is only the appearance of the waveforms that is important.

Figure A.7.8 is the 500 Hz sine wave at the input to the modulator. Figure A.7.9 shows the 500 Hz output of the demodulator. The difference in waveforms is slight; there is no detectable difference in the signals when listened to.

Figures A.7.10 and A.7.11 show the voltage on capacitor C_1 of the demodulator. Figure A.7.10 shows the result with the input signal level adjusted so as to utilize 14 levels of the 16 available. Figure A.7.11 is the result with the input signal (at the modulator) attenuated - only 3 of 16 levels are utilized. The arrow on each photo shows the position in time of the sampling of the voltage on C_1.

Figure A.7.12 is the voltage on C_2 with the modulator input level adjusted for the full 16 levels (maximum input level before distortion). It is this signal which is amplified

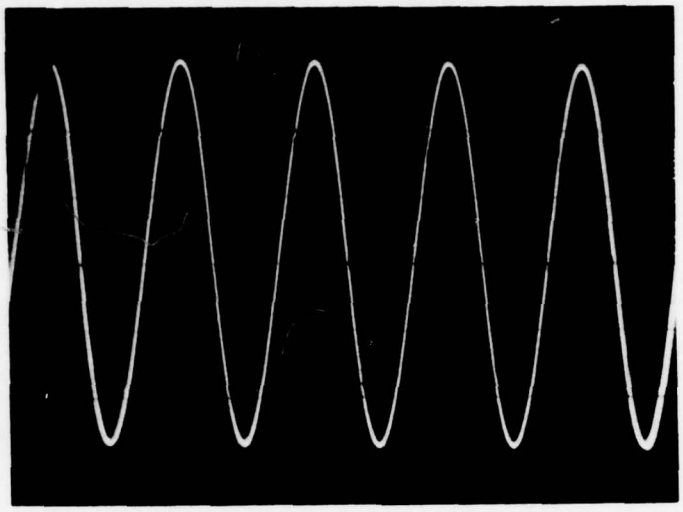


Figure A.7.8 500 Hz Input to Modulator.

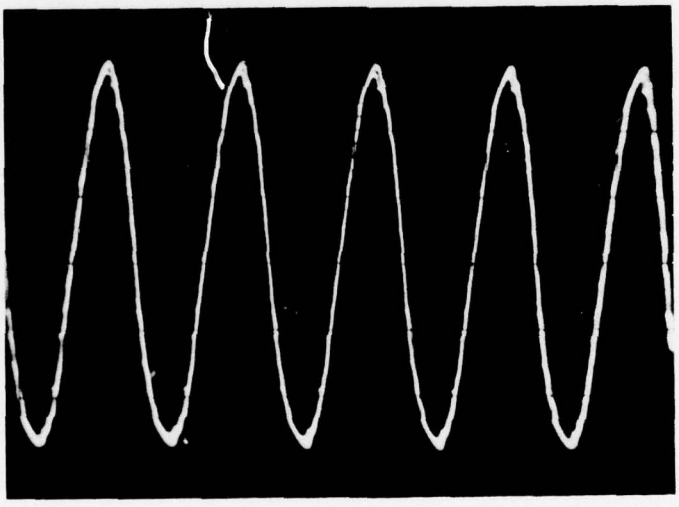


Figure A.7.9 Demodulated Output Signal.

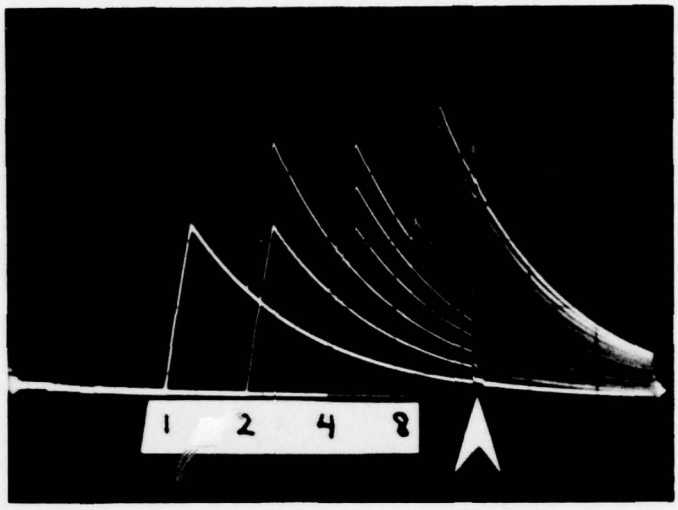


Figure A.7.10 Voltage on C_1 of Demodulator with 14-level Encoding.

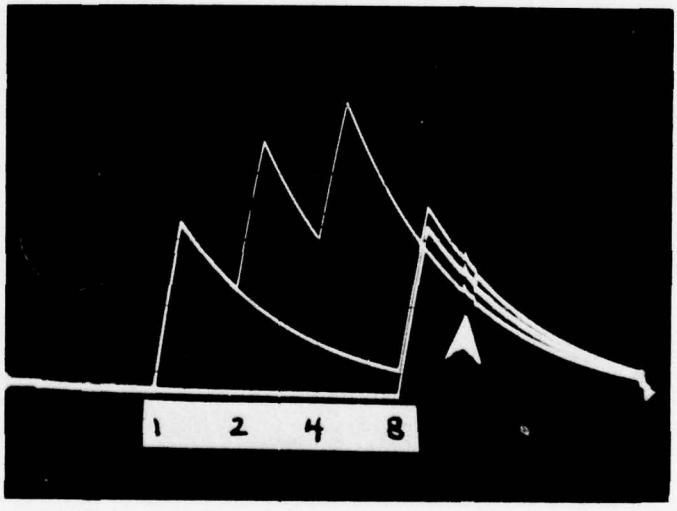


Figure A.7.11 Voltage on C_1 of Demodulator with 3-level Encoding.

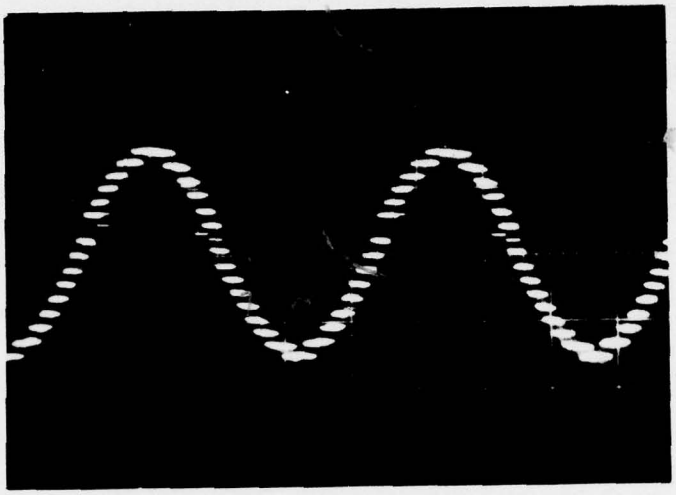


Figure A.7.12 Output of Sample-and-hold Circuit before Filtering.

and filtered to give the waveform shown in Figure A.7.9. Note in Figure A.7.12 the even spacing between levels - this is an indication of the quality of the demodulator, as well as the accuracy of adjustment of the set-up controls.

4. Performance

The performance of the overall system was evaluated objectively and subjectively. The -3 dB bandwidth extends from 110 Hz to 2.8 kHz. This is a nearly ideal response curve for voice communication. The frequency response was measured with a sine wave input to the modulator: the amplitude of the input signal was adjusted to utilize all 16 levels (100% modulation).

Subjective performance was evaluated by listening to both voice and music played through the system, using a cassette recorder as a signal source. Voice was completely intelligible under normal circumstances - however, as the input signal level dropped ("speaking softly"), distortion increased because fewer of the quantum levels were utilized. This characteristic is to be expected with a 16-level system; compression of the audio signal will be used in the final application, to overcome this problem. Performance with music as a signal was quite good, especially when the dynamic range of the signal was relatively narrow.

PLANS FOR THE NEXT INTERVAL

The Gunn diode oscillator circuit will be designed and constructed. A suitable pulser for the Gunn oscillator will

be designed and tested. Experimentation with both transistor and delay-line pulse networks will be done to maximize pulse-repetition frequency.

A.8 STUDY OF SOLUTION EPITAXIAL GROWTH AND PERFORMANCE OF GaAs

M. Randles, L. F. Eastman* and C. A. Lee*

a. Introduction

The Berg-Barrett method of x-ray topography using the equipment available was deemed insufficient for the task of revealing fine details of the interfaces of a GaAs multiple epitaxial layer diode structure.

b. Discussion of Results

In the previous report, the sample alignment procedure for obtaining Berg-Barrett x-ray topographs of GaAs was detailed. The photographic exposure of the reflected x-ray beam is essentially a one-to-one image of the crystal surface. This means that any magnification of the surface detail has to be accomplished by standard photographic enlarging techniques. This sets a practical upper limit of about 100 times magnification for a good negative. Therefore, the quality of the x-ray negative determines the amount of surface detail that can be resolved.

It was determined that the x-ray equipment used here is insufficient for cleavage face x-ray topography. To observe

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*Project Supervisor

typical detail on a cleaved edge would require resolution of 5-10 microns. Many attempts were made to achieve this type of resolution but with no success. It is felt that the resolution could be improved by using a microfocus x-ray source but none was available.

The Berg-Barrett method, however, retains its position as a valuable analytic tool for larger surfaces (greater than a couple millimeters on a side, for example). The description of the Berg-Barrett method given in previous quarterly reports will provide a handy step-by-step guide for anyone wishing to use this technique.

PLANS FOR THE NEXT INTERVAL

This is the final report on this subject.

A.9 STABLE GUNN OSCILLATOR

V. Wrick and G. C. Dalman*

a. Introduction

A frequency-stable C.W. microwave source has potential applications in ultra-sensitive receivers, lab equipment, or as a locking source for high power transmitters. By using a varactor-tuned Gunn oscillator, a reaction cavity, and a phase detector, a phase-locked loop has been realized which provides a highly stable X-band source.

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*Project Supervisor

b. Discussion of Results

Figure A.9.1 shows the circuit diagram for the phase-locked loop. The reaction cavity shown in the figure is tuned to the normal free-running frequency of operation, f_o. The reaction-cavity is placed in the line at a distance $L/\lambda g$ from the source such that it is a parallel resonant circuit at the plane of the oscillator. Power from the reaction cavity is fed to one port of the balanced-mixer phase detector, and an equal amount of power is fed to the other port of the phase detector from the output of a coupler connected to the main transmission line. The location of the coupler and length of the connecting transmission line is adjusted so that the output of the phase detector is zero. If a phase shift occurs as the result of a frequency change of the oscillator, the output of the phase detector becomes finite. This error signal is amplified and fed back to the varactor with the proper polarity to retune the oscillator for the minimum error signal.

The reaction cavity is a significant element in short-term FM noise reduction as well as providing the phase discriminator. The feedback loop is necessary to provide long-term stabilization of the oscillator frequency over Δf values in excess of those possible with the reaction cavity stabilizer alone. This loop can also provide some short-term stabilization. Figure A.9.2 shows a block diagram of the test facility used to measure the bandwidth of the cavity. The cavity provides an

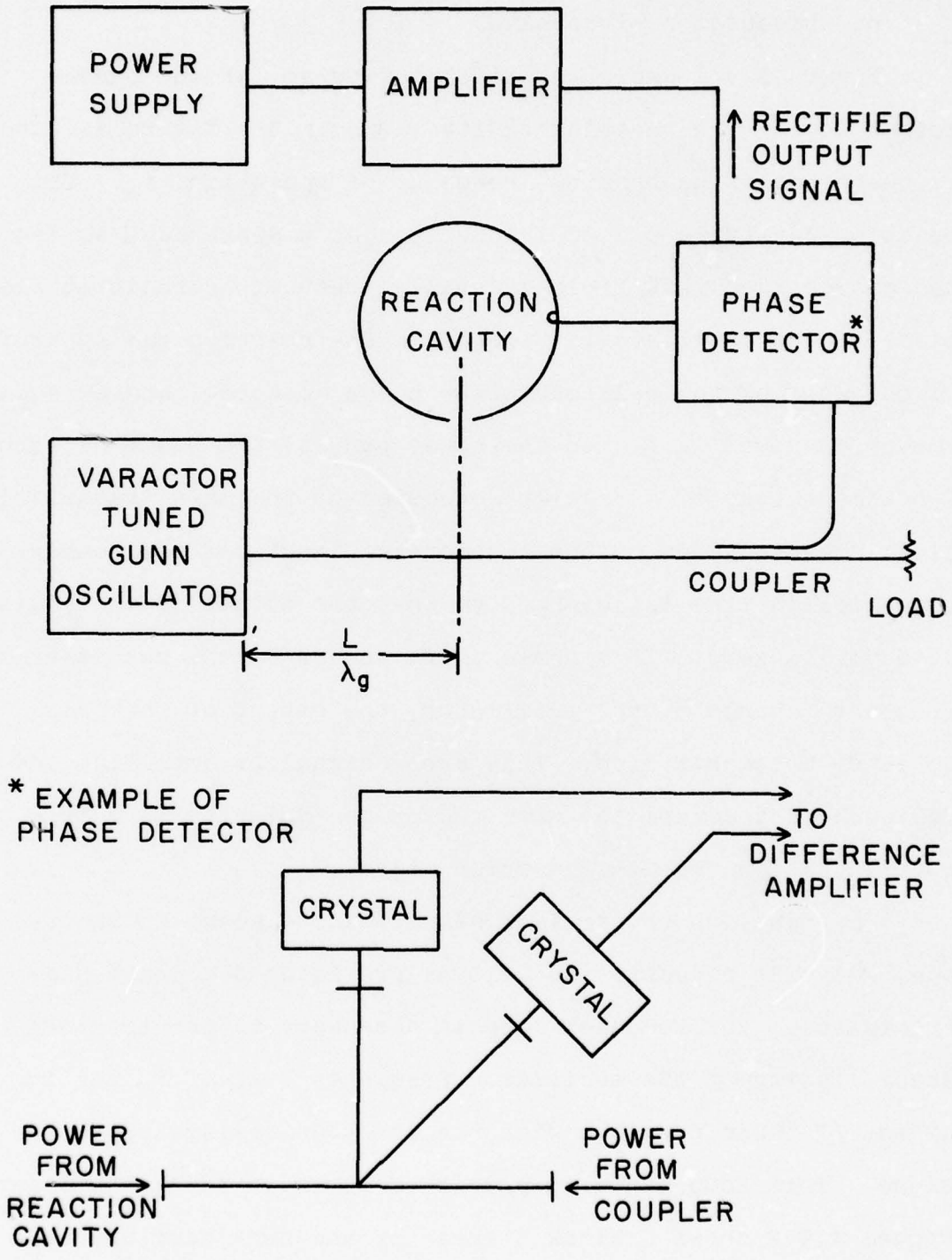


Figure A.9.1 Frequency Stabilizing Circuit.

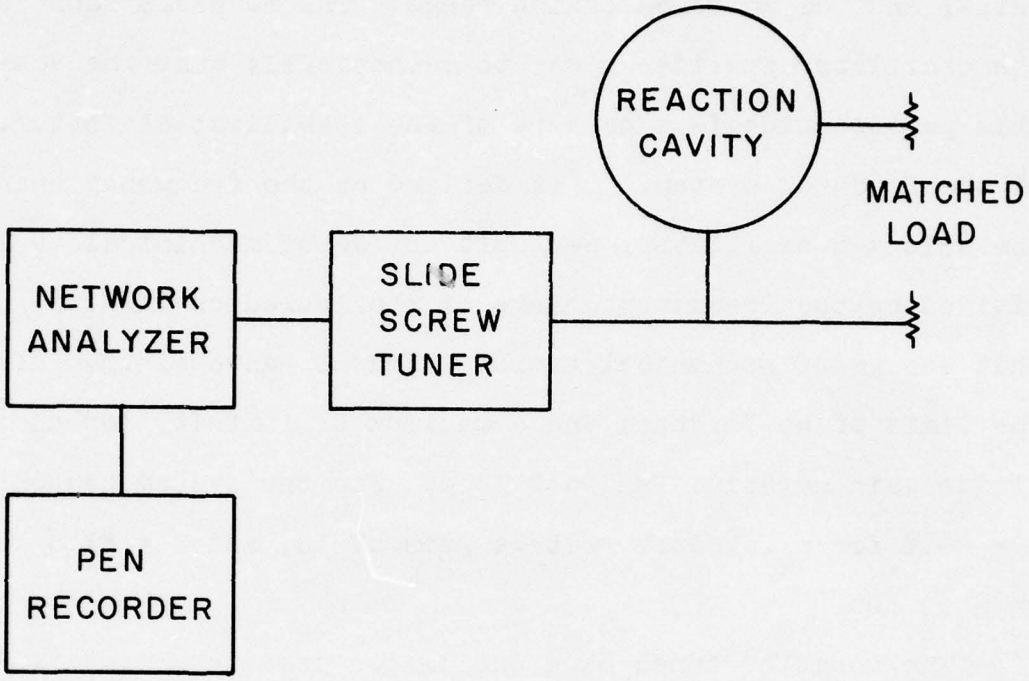


Figure A.9.2 Reaction Cavity Test Facility.

effective stabilizing range of around 2 MHz. Figure A.9.3 shows a graph of the locking range of the oscillator for two feedback gains, and the unlocked tuning range. The moveable short behind the oscillator provides a way to mechanically tune the source. This perturbation is a measure of the stabilization factor, S, of the feedback system. S is defined as the frequency change of the unlocked oscillator, per unit change of mechanical tuning, divided by the frequency change of the locked oscillator, per unit change of mechanical tuning. Thus S has a minimum of 1 in the limit of no feedback and a maximum of infinity for an infinite gain negative feedback loop. For the system tested, S = 40.8 for a feedback voltage gain of 10, and S = 81.6 for a gain of 100.

The varactor tuned Gunn oscillator used in conjunction with the phase locked loop is a good low noise source. By improving the discriminator and utilizing a high gain low noise DC amplifier in the feedback loop, it is conceivable that S could be raised to 1000. For low gain in the feedback loop, the circuit has the potential for use as a phase locked loop FM detector.

PLANS FOR THE NEXT INTERVAL

Near carrier FM noise measurements will be made to determine the amount of noise reduction brought about by this frequency stabilization method.

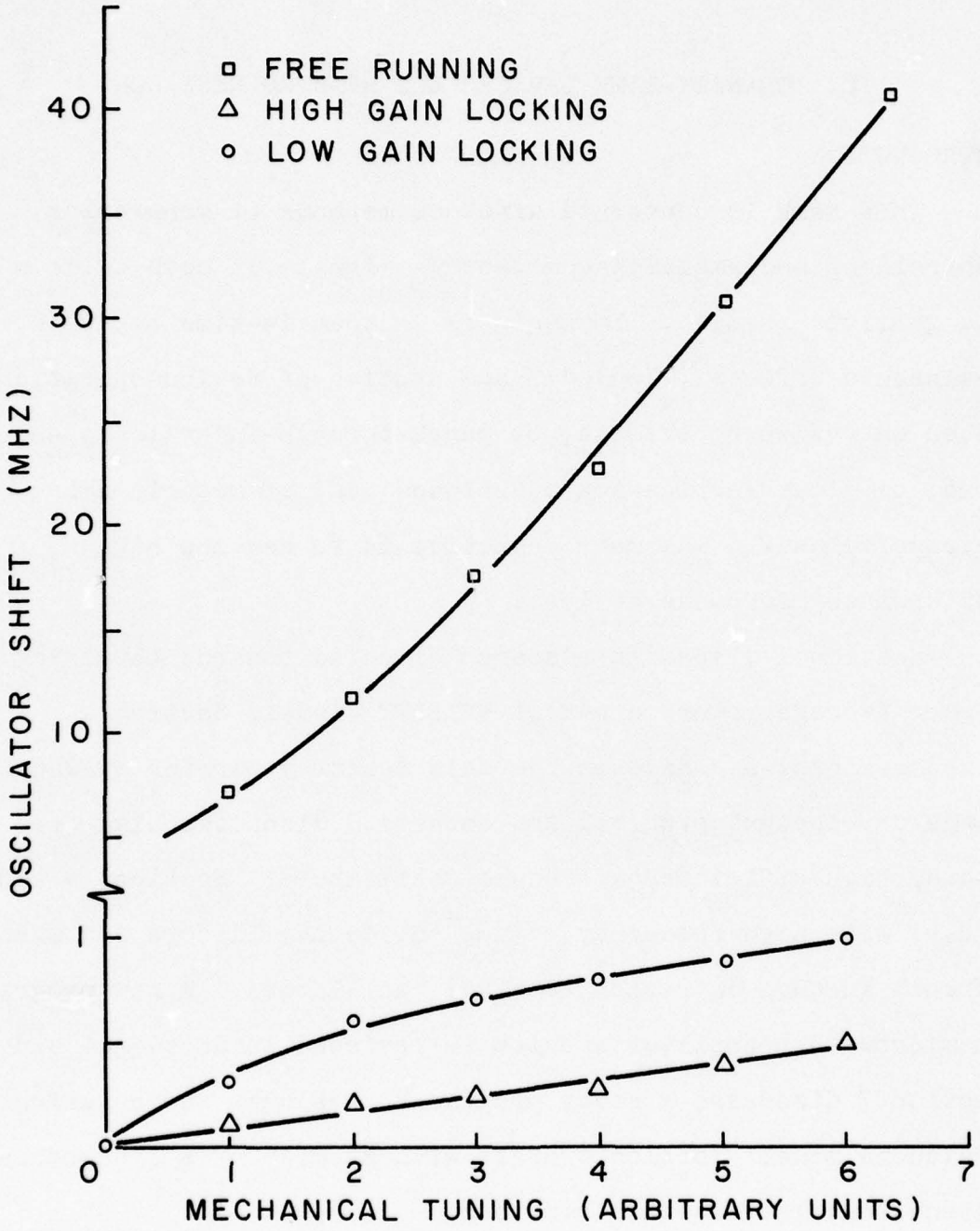


Figure A.9.3 Frequency Pulling vs. Mechanical Tuning for Locked and Free Running Oscillator.

B. TRANSIT-TIME DEVICES AND RELATED RESEARCH

INTRODUCTION

This task is concerned with new methods of generating, controlling and amplifying microwave signals in both silicon and gallium arsenide. Emphasis is on transit-time negative resistance effects. Included are studies of device operation based on avalanche effects; on punch-through-injection phenomena; of diode fabrication techniques; and of materials processing methods. The main objective is to develop high performance microwave devices.

Section 1 discusses research directed towards obtaining higher average power output of TRAPATT diodes, Section 2 discusses progress made on the GaAs Schottky barrier avalanche diode development program, and Section 3 discusses high frequency high-efficiency avalanche oscillators. Sections 4 and 5 deal with high frequency pt-n-p^+ diode oscillators and with punched through injection (Baritt) oscillators. A new program on microwave transistor studies is reviewed in Section 6 and Section 7 discusses a study program to evaluate the relaxing avalanche mode. Section 8 deals with studies of a synchronous detuned oscillator power combiner.

B.1 OPTIMUM STRUCTURES FOR HIGH AVERAGE POWER TRAPATT DEVICES

J. Frey

a. Introduction

During this interval efforts were concentrated on the technology of TRAPATT diode fabrication, including etching and thinning procedures for multiple mesa devices.

b. Etch Procedures

Use of evaporated and alloyed gold as both a contact and a mesa etch mask has been described previously.[1] Although considerable success was achieved using the gold mask, an attempt was made during this interval to use a thermally grown (steam) oxide as an alternative mask. In addition, a plated heat sink process was attempted. While the plated heat sink was a success, the oxide mask failed to withstand the mesa etch.

In brief, the total multi-mesa process consisted of the following steps:

1. Sheet diffusion, using spin-on dopants
2. Etch thin wafer in bubble etcher[2] to .0015" - .002"
3. Grow 1μ steam oxide on substrate side of wafer
4. Evaporate gold on junction side of wafer
5. Alloy gold
6. Plate gold to .002"
7. Photoresist and etch multi-mesa pattern on oxide
8. Etch mesas.

This process was successful until step 8, at which point the

oxide failed to mask successfully against the CP4 etch for a sufficiently long etch time.

Thermocompression wire bonding of planar IMPATT diodes was perfected during this interval. The diodes, which are .006" in diameter, with oxide-masked junction edges, are contained in .015" square chips. Die bonding is performed using 88/12 Au/Si preforms at 300°C. Thermocompression wedge bonding is accomplished using .001" Au wire at a temperature of 320°C. A bonded planar diode, on a .015" x .015" x .008" chip, is shown in an S4 package in Figure B.1.1. The diode shown produced 200 mW peak-pulsed power in C band, in a coaxial two-slug circuit.

PLANS FOR THE NEXT INTERVAL

During the next interval the plated gold heat sink process, which permits handling wafers etch-thinned to .002" or less, will be combined with the gold etch mask in a continuation of the study of multiple mesa fabrication procedures.

References

1. J. Frey, "Optimum Structures for High Average Power TRAPATT Devices", RADC-TR-72-45 Technical Report, March, 1972.

2. A.I. Stoller, et al, "A New Technique for Etch Thinning Silicon Wafers", RCA Rev. 31, p. 265, 1970.

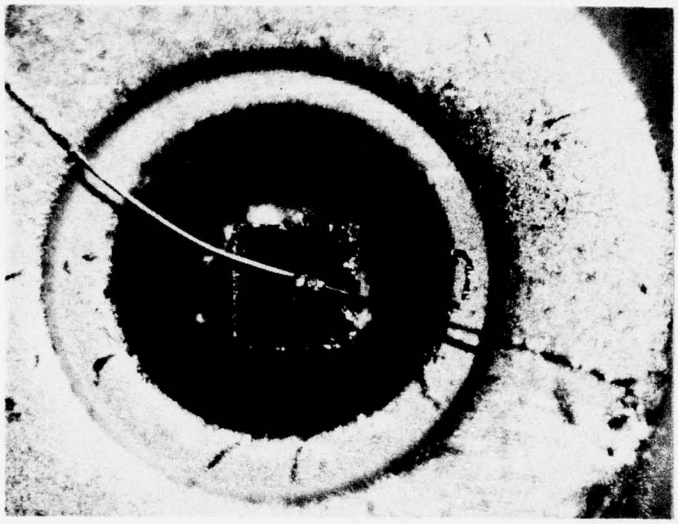


Figure B.1.1 .006" Diameter Planar IMPATT Diode on .015" x .015" x .008" chip, bonded in S4 package.

B.2 GaAs SCHOTTKY BARRIER AVALANCHE DIODES

N. O. Johnson, G. C. Dalman* and C. A. Lee*

a. Introduction

Work during this period has been concerned primarily with the growing of liquid phase epitaxial layers suitable for avalanche diodes. The method of growing was described in a previous report.[1] During this quarter seven new runs were made. The results are discussed below.

b. Experimental Results

A summary of the results obtained is shown in Table 1. Run #10 was the first run with two epitaxial layers on the same substrate. It showed that even without intentional doping of the gallium melt it was not possible to reach a doping less than $1x10^{16}$ cm^{-3}. In order to improve this situation, runs #11 and #12 were made. The bottom wafer was replaced by a wafer made from the source material. In run #11 both the buffer layer and the active layer were grown with a source material wafer present. In run #12 only the active layer was grown in this way. In both cases the doping was close to $3x10^{16}$ cm^{-3}, and no difference caused by the two ways of growing the buffer layers could be detected. The #11 wafer was smooth with many pits. Diodes were made which showed a flat doping profile with a slight increase close to the substrate. These diodes oscillated in an X-band cavity with typical values shown in Table 2.

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*Project Supervisor

TABLE 1. RESULTS OF RUNS No. 11 TO No. 17

No.	Substrate	Initial Temp.	Cooling Rate	Epilayer Doping	Comments
11	Upper: n^+Se Lower: source material	730°C	Max. allowable	$3 \cdot 10^{16}$ cm^{-3}	Smooth layer with many pits.
12	Upper: 9L Lower: source material	730°C	- " -	$2.9 \cdot 10^{16}$ cm^{-3}	Flat doping profile with slight increase close to substrate. Soft breakdown, 10mA at 23V.
13	Upper: 9U Lower: 12U	730°C	- " -	$.5\text{-}1.0 \cdot 10^{16}$ cm^{-3}	
14	n^+ Se	715°C	- " -	$1.5 \cdot 10^{16}$ cm^{-3}	Both layers polished, high backward saturation current.
15	n^+ Se	715°C	5°C/h		Very uneven coating.
16	n^+ Se	760°C	Max. allowable	$2 \cdot 10^{17}$ cm^{-3}	Less pits. Active layer polished.
17	n^+ Se	715°C	- " -	$1 \cdot 10^{16}$ cm^{-3}	Thick spacer.

TABLE 2. RESULTS FROM OSCILLATING DIODES

Wafer No.	11	14	17	Vapor Phase Epitaxial Layer
Output Power	80mW	18mW	150mW	500 mW
Frequency	X-band	8.2 GHz	9.42 GHz	X-band
Voltage	30V	40V	70V	60V
Current	420mA	200mA	400mA	420mA
Pulse Length	1μs	1μs	1μs	1μs
Pulse Repetition Rate	500 Hz	100 Hz	500 Hz	500 Hz
Efficiency	.7%	.25%	.6%	2%

In run #15 a slow cooling rate was used. This enhanced the problem of obtaining an even coating. When earlier epitaxial layers were polished, it was evident that because of a temperature gradient along the surface of the wafer the epitaxial layer was slightly thicker close to the edges than in the center. With the slow cooling rate there was no epitaxial layer at all in the center. A careful examination of this wafer under a microscope revealed the formation process of the pits in many earlier layers. The epitaxial growth started at a limited number of nucleation centers and from those points growth took place in only one direction at a certain angle to the surface. Just before the growth front from one nucleation center reaches the one in front of it, a small pit is formed. Therefore there is a correlation between the number of nucleation centers, the thickness of the epitaxial layer and the number of pits. Thus a higher temperature or a thicker spacer between the wafers may reduce the number of pits.

In run #16 the temperature was increased to 760°C, which should give an average epitaxial layer thickness of 6 μm instead of 4 μm at 730°C. The number of pits was lowered considerably. The doping was, however, unusually high, 2×10^{17} cm^{-3}.

In run #17 the 0.25 mm thick spacer was replaced by the 0.40 mm thick spacer. The temperature was lowered to 715°C to give a 6 μm thick epitaxial layer. There was an increase in

pits as compared to run #16. The doping was $1x10^{16}$ cm^{-3}, and diode parameters are shown in Table 2.

Diodes have also been made from vapor phase grown material purchased from Monsanto[2] in a way described by Berenz.[3] The best result as yet is shown in Table 2.

PLANS FOR THE NEXT INTERVAL

The growth process of epitaxial layers will be refined and the testing of diodes in circuits will be started.

References

1. N.O. Johnson, G.C. Dalman and C.A. Lee, "GaAs Schottky Barrier Avalanche Diodes", Advanced Concepts of Microwave Generation and Control in Solids, Technical Report RADC-TR-72-45, March 1972, pp. 81-85.

2. N.O. Johnson, G.C. Dalman and C.A. Lee, "GaAs Schottky Barrier Avalanche Diodes", Advanced Concepts of Microwave Generation and Control in Solids, Technical Report RADC-TR-71-307, January 1972, pp.49-50.

3. J.J. Berenz, A Gallium Arsenide Schottky Barrier Avalanche Diode Oscillator, RADC-TR-71-19, January 1971.

B.3 HIGH-FREQUENCY HIGH-EFFICIENCY AVALANCHE OSCILLATIONS

H. A. Hung and C. A. Lee*

a. Introduction

Work done during this quarter may be divided into three parts: further investigations on the diode chips made in previous periods were performed; new diodes were obtained with

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*Project Supervisor

diffusion runs from new substrates; and, a ridged waveguide cavity for high-efficiency operation was completed.

b. Experimental Results

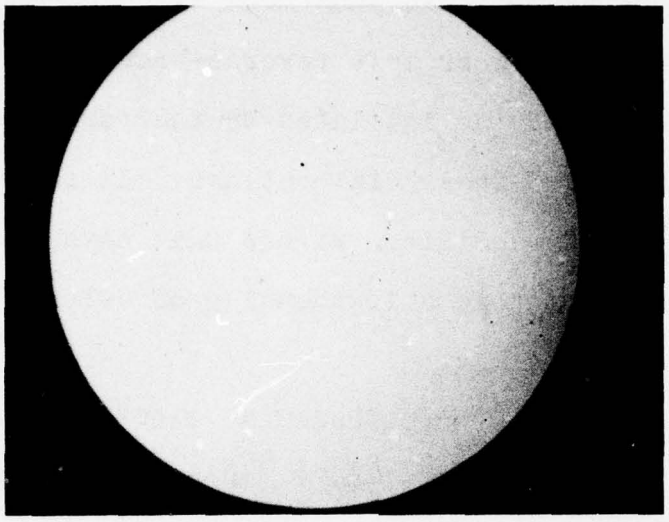
More chips from the diffusion run, DR 2/24 with 3 Ω-cm epi-resistivity, were bonded in order to investigate the diode performance. The yield of diodes with good dc I-V characteristics, especially in the reverse direction, was very low. The problem could be a result of the fact that the density of defects in the epi-wafer was high. The yield was further reduced because the chips were made fairly thin, less than a mil in total thickness, and the sample was poorly scribed, making the process of thermocompression bonding with the existing large size bonding tip difficult. An alternative is to use a stitch bonder. Nevertheless, a few diodes were made with reasonable dc reverse-bias characteristics. They had a breakdown voltage of 76 volts, a value higher than one would expect for high frequency operation. On testing these diodes in a coaxial cavity, tuned with three non-conducting slugs, clean TRAPATT signals as observed through a tunnel diode detector were obtained. The typical result, so far, was 7.5 watts with 23% efficiency operating at 1.45 GHz. The diodes were pulsed at 500 cps with pulse width of 600 ns.

Another diffusion run was performed on two samples simultaneously, hoping that higher frequency diodes would be made. These samples were from the same batch of wafers as the 3 Ω-cm

ones used in all previous diffusion runs, except that they had epi-resistivity values of 2.7 and 4.2 Ω-cm as indicated by their manufacturer, Semimetal. However, no successful diodes with expected parameters were fabricated. Better quality epitaxial material would be sought.

New wafers of Si NN^+ epi-substrate were purchased from the manufacturer, KEV Inc. The resistivity of the epi-region ranges from 2.5 to 3 Ω-cm. A value of around 4 μm for the epi-thickness was observed after a sample was scribed, lapped, and stained. Defects in material, in particular, dislocations, were investigated with Sirtl etch: equal volumes of solutions, A: one part by weight of Cr_2O_3 and two parts by weight of H_2O, and B: HF. Figure B.3.1(a) shows the result of the epi-surface of the new material after it was treated with the Sirtl etch for 4 minutes at room temperature. The diameter of the exposed sample was 2.2 mm. The density of the etch pits was found to be fairly low, roughly $900/cm^2$, and was not increased much with the etching time doubled. For comparison, a similarly treated sample by Semimetal, used in previous diode fabrications, is shown in Figure B.3.1(b). It is obvious that the etch-pit density is higher in the old material than in the new one. These dislocation defects, while originating from the substrate or at the interface with the epitaxial layer, taken by themselves, do not change the electronic properties of the epitaxial layer. They give rise, however, to inhomogeneities in the diffusion of impurities and act as nucleation centers for metal

(a)



(b)

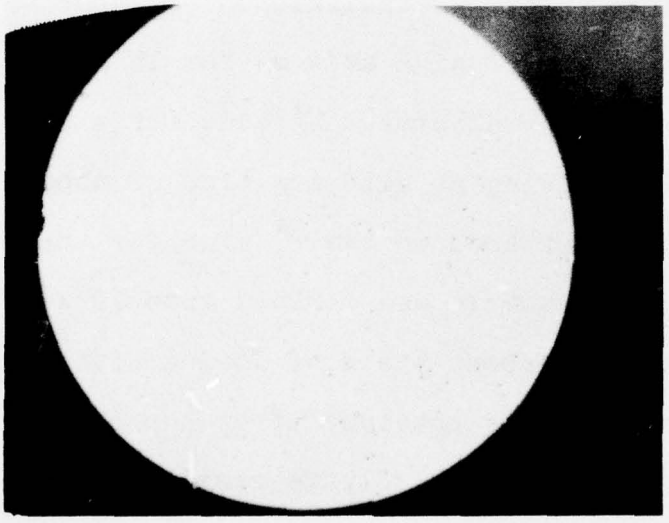


Figure B.3.1 (a) Epi-surface by KEV showing the Etch-pit Density. (b) Epi-surface by Semimetal showing the Etch-pit Density.

precipitates. Possibly, p-n junctions with these defects exhibit short-circuited or soft reverse-breakdown characteristics. Breakdown may be initiated by the formation of microplasma at the edge of these dislocations. It is believed that the yield of processed Silicon wafers that have been properly characterized and contain a low density of defects would be much increased.

The new wafer was outdiffused at 1200°C for one hour, followed by Ga-diffusion at 1150°C (measured at the surface of the diffusion bucket) for a period of 6 minutes plus 4 minutes to bring the temperature up. The substrate side of the sample was then lapped and chemically polished down to less than 2 mils thick. Metallization was done by first sputtering Pt on the P^+ side at 4 ma for 15 minutes. Au was then sputtered on the substrate N^+ side for a prolonged period of 25 minutes including an alloying time of about 10 minutes. Finally, Au was sputtered on the P^+ side for the purpose of easy bonding. The sample was scribed into 10 x 10 $mils^2$ chips. A hundred percent yield of diodes with excellent dc I-V characteristics was obtained after the chips were bonded and etched. The breakdown voltage ranges from 22 volts to 29.5 volts for varying chips. Capacitance-voltage measurements were made on several of the bonded diodes. Plots of $1/C^2$ and $1/C^3$ versus reverse-bias voltage were made. A straight line was obtained near the junction only in the

plots of $1/C^3$ versus voltage, as shown in Figure B.3.2, indicating that a cube-root junction had resulted. The reason is due to the fact that the epitaxial width was fairly narrow to start, the outdiffusion and diffusion consequently causing a non-uniform impurity doping density across the depleted region. This is also illustrated by the gradual decrease in capacitance value as the reverse-bias voltage approaches the breakdown value. There is no obvious indication of punch-through or capacitance value leveling off for higher reverse-bias. More characterization of these diodes including the investigation of the mechanism and the temperature effects of the saturation current is in progress.

Work has also been completed in the design of a ridged waveguide[1,2] cavity. In order to operate a diode in the high-efficiency mode, a circuit capable of operating over a 3:1 frequency range is preferred. It also should have low loss at harmonics of the fundamental output frequency. For an X-band operation, a coaxial cavity will have very small dimensions (a few millimeters diameter) in order to push the cut-off frequency of the higher-order mode up to the 30 GHz region. A ridged waveguide would be the probable alternative. With a ridge inside and portion of the internal dimensions reduced, the structure provides two advantages. One, the cut-off frequency of the dominant mode is lowered while that of the higher-order mode is raised, providing a wide operating bandwidth. It has the added advantage of lowering the wave

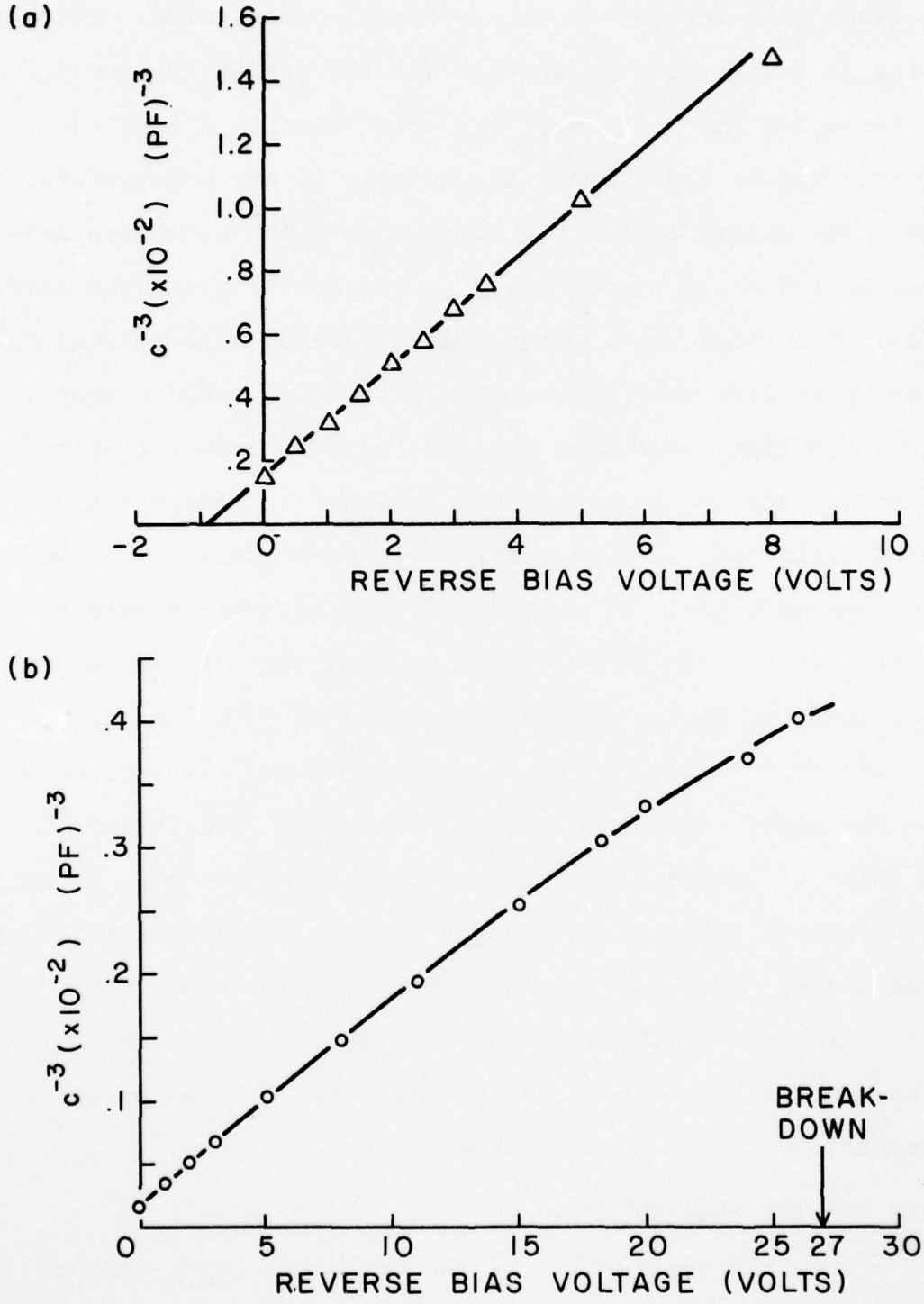


Figure B.3.2 (Capacitance)$^{-3}$ as a Function of Reverse Bias Voltage (Low and High Voltage Plots)

impedance with respect to the rectangular waveguide. However, tuning in a waveguide to provide all the proper impedance for the harmonics may be more of a problem than in a coaxial cavity. Figure B.3.3 shows a schematic of the waveguide cavity made. The cavity itself had dimensions which were less than those of a Ku-band with a ridge in the center along the waveguide. The ridge and the side walls tapered into a regular X-band waveguide with minimum discontinuity at the transition. A low-pass filter was used for feeding bias into the diode. The screws and the sliding short provided the major tuning. During experiment another slide screw tuner can be used to give more matching. With this arrangement, the calculated cut-off for the TE_{20} mode was 23 GHz and that of the dominant TE_{10}, 7.5 GHz, giving a bandwidth close to 3 to 1 ratio.

Initial testing of the ridged waveguide circuit, together with the newly fabricated diodes, has shown oscillation in the X-band. The circuit and the diodes have not been optimized for operation yet. At present, the tested diodes have fairly large areas. Two modifications will be made. One is to reduce the size of the chips by etching; the other is to try "bare mounting" the chips, eliminating some of the parasitic elements due to the package itself.

PLANS FOR THE NEXT INTERVAL

Further investigation of the new diodes from the new material will be performed, particularly in the ridged

waveguide cavity. Some improvements on the cavity may be necessary.

References

1. S. Hopfer, "The Design of Ridged Waveguides", IRE Trans., MTT-3, pp. 20-29, October 1955.

2. J.R. Pyle, "The Cutoff Wavelength of the TE_{10} Mode in Ridged Rectangular Waveguide of Any Aspect Ratio", IEEE Trans., MTT-14, April 1966, pp. 175-183.

B.4 HIGH FREQUENCY Pt-n-p^+ MICROWAVE OSCILLATORS

J. Oakes and C.A. Lee*

During this quarter, diodes were fabricated from the silicon slice previously described and these were characterized by observing some of their DC and AC properties. Construction of an M band (50-75 GHz) circuit for operating the devices was also begun.

Previous Quarterly Reports have described a silicon Pt-n-p^+ structure of total thickness 3.5 mils and n-epi layer thickness near 1 μm. This silicon wafer was scribed and broken using a diamond tipped scriber .0055" square chips. These chips, some threaded A packages and some pieces of .004" x .0005" gold ribbon, were thoroughly cleaned and the chips bonded into the packages at 20,000 psi and 300°C.

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*Project Supervisor

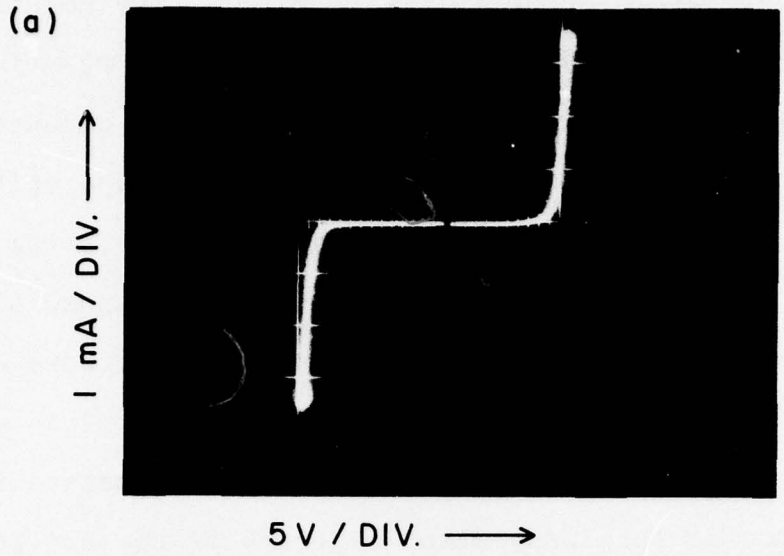
Photographs of the DC characteristics of two of the resulting diodes are shown in Figure B.4.1. The negative voltage axis corresponds to forward bias of the Pt-n junction resulting in the higher potentials observed for conduction in that direction. The diode of B.4.1 (a) requires a voltage of -14V for a current of 1mA while the diode of B.4.1 (b) requires only -2.6V for the same current. Some of the bonded diodes looked purely resistive no matter how often they were etched. These differences in DC characteristics are believed to result from large variations in n-type epi-layer thickness across the wafer due to the inadvertent exposure of the epi-layer to a strong etch while the substrate of the wafer was being thinned.

C-V measurements were performed on the diode of Figure B.4.1 (a) using a GR 250A RX meter at 100 MHz. Figure B.4.2 shows the resulting data. Using

$$\text{Area} = 1.4 \times 10^{-4} \text{cm}^2$$
$$\epsilon_{\text{Silicon}} = 1.05 \times 10^{-2} \text{F/M}$$
$$\mu_{\text{Silicon}} = 1500 \text{ cm}^2/_{\text{v-sec}}$$

we can calculate the doping density of the n-epi layer to be 1.8×10^{15} cm^{-3} or 2.3 Ω-cm resistivity since

$$C^{-2} = \left(\frac{2}{\epsilon e N_d A^2} \right) V.$$



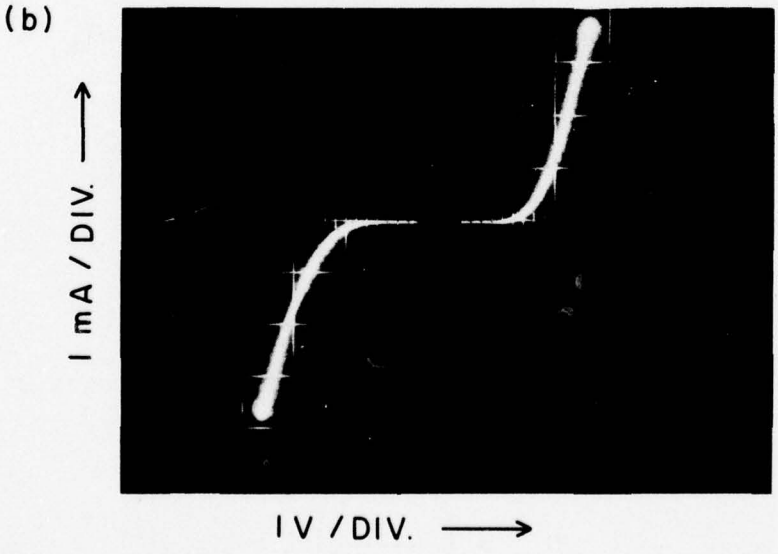


Figure B.4.1 Pt-n-p^+ Diodes

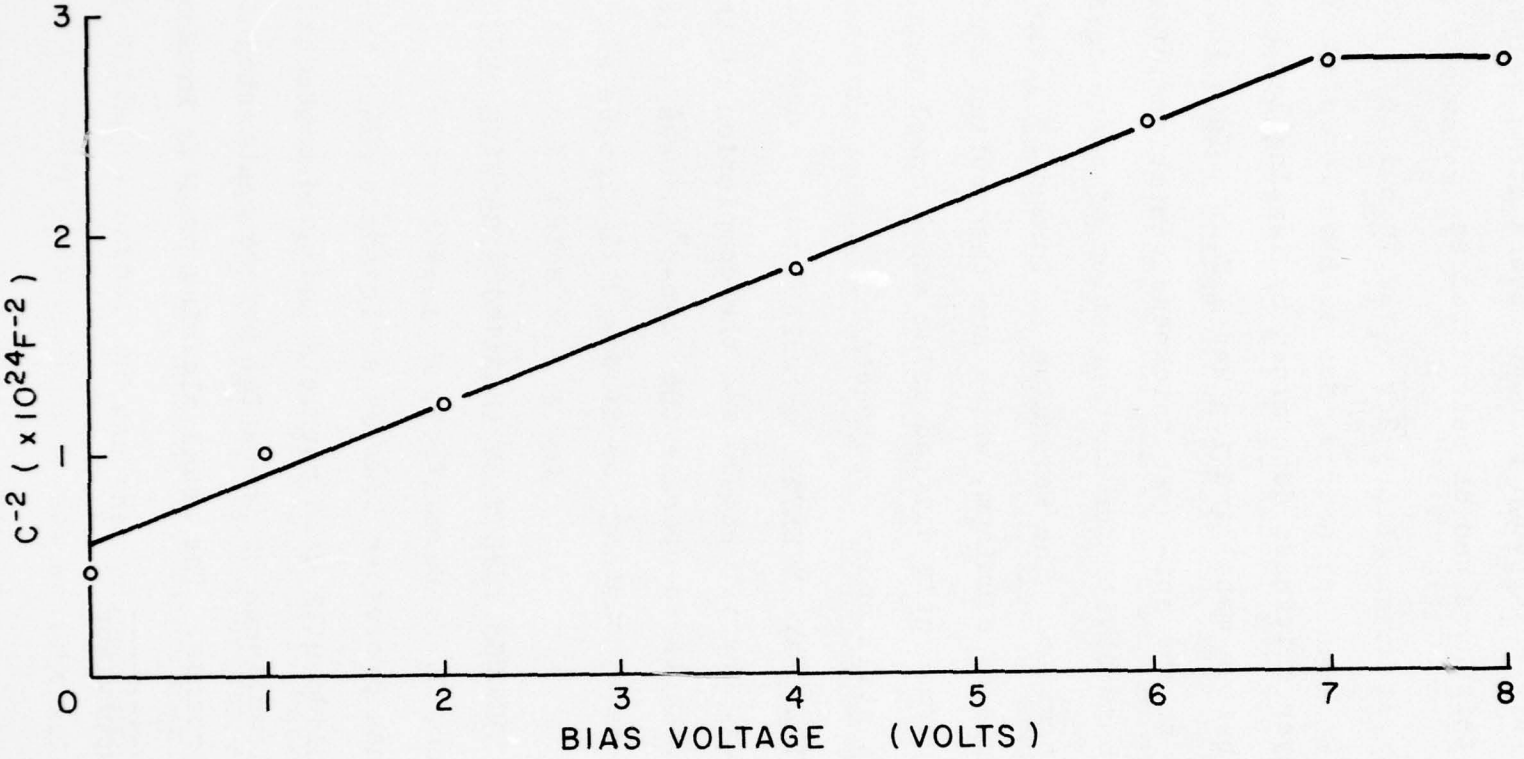
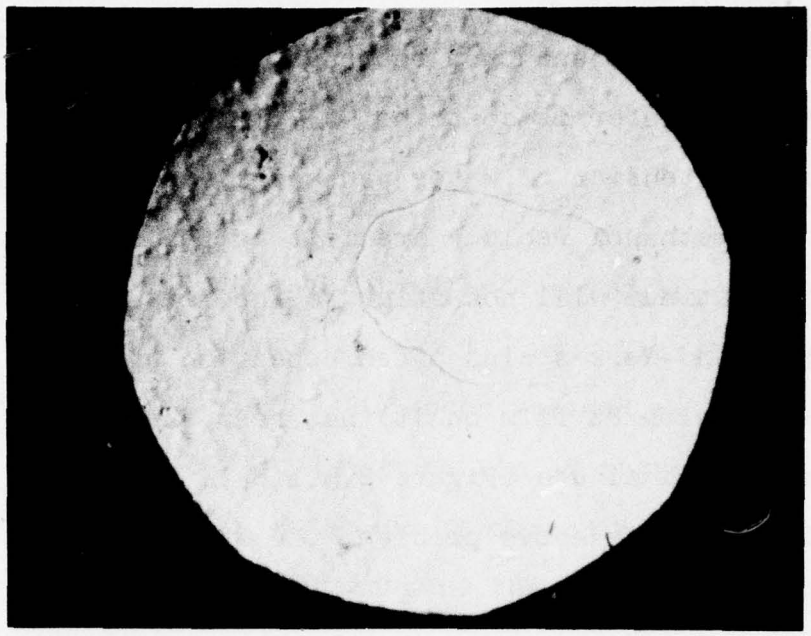


Figure B.4.2 Capacitance vs. Voltage for Diode of B.4.1(a).

(a)



(b)

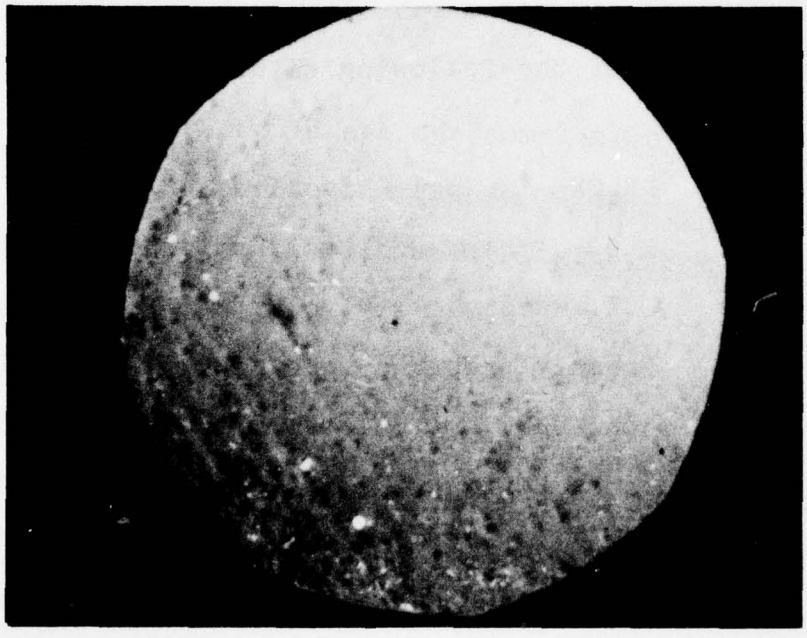


Figure B.5.1 Bad PT film resulted from a dirty Si surface. (33X)

(a) Loose Pt film

(b) Dark stain

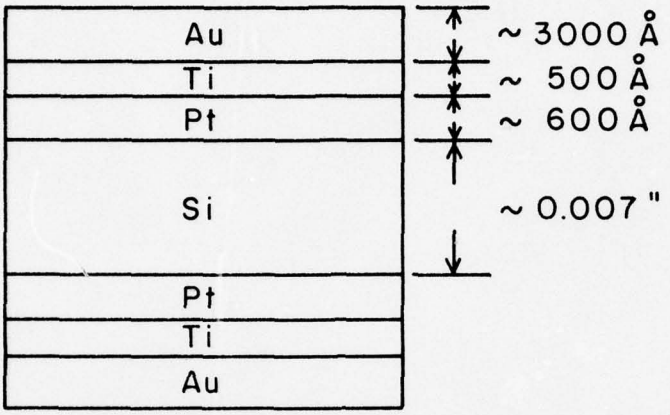
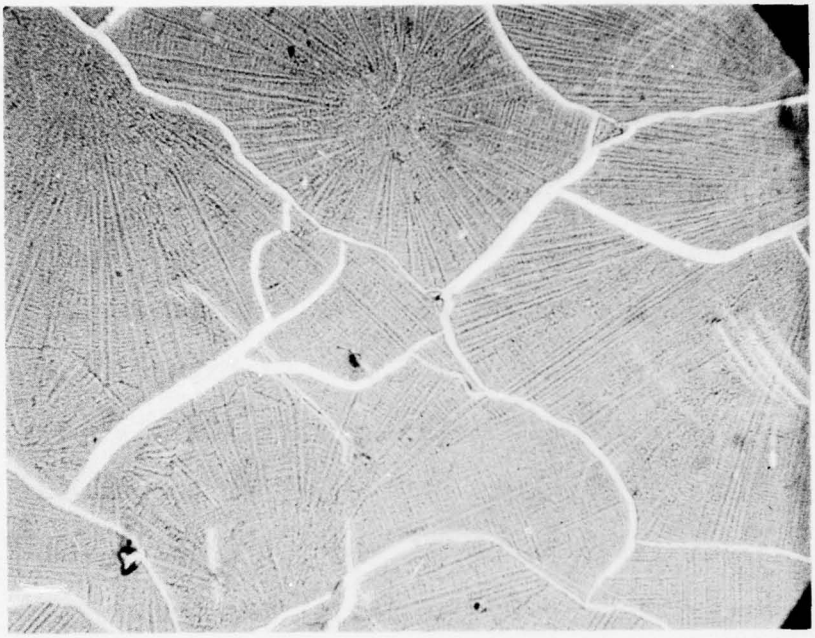


Figure B 5.2 Cross section of a diode chip (not to scale)

(a)



(b)

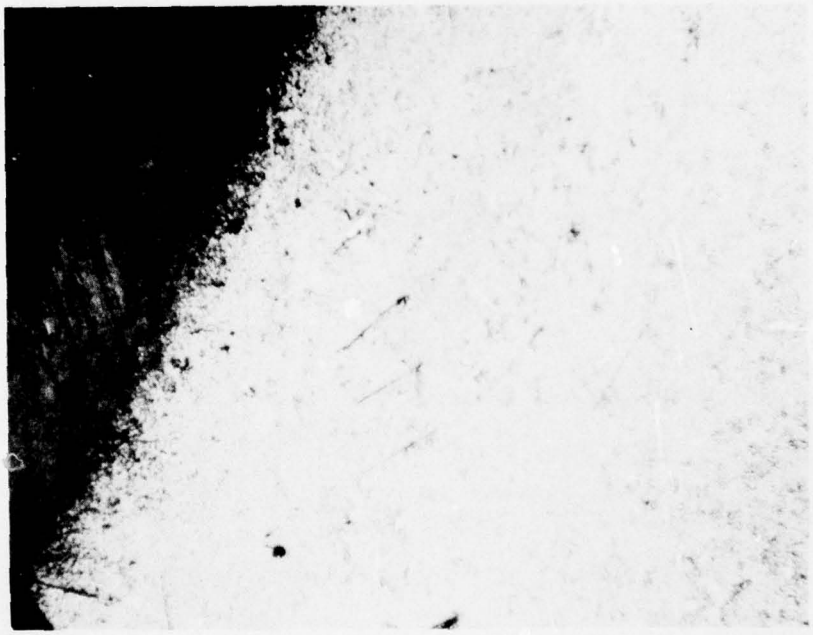


Figure B.5.3 (a) Au Pt alloyed surface resulted from high current density (60X)

(b) Non-uniform Au film resulted from sudden current increase during sputtering. (42X)

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it was easily removed with some filter paper from beneath the wafer which could then be taken out of the beaker and directly put into the sputtering system.

Three layers of thin films were sputtered on top of the silicon substrate as shown in Figure B.5.2. Low current density ($\sim$ 1.25 mA/sq. in.) was used. At higher current density, the gold would either alloy with the platinum (Figure B.5.3(a)) or the gold film will not be uniform (Fig. B.5.3(b)). Also, lower current density decreases the possibility of sparking in the sputtering system.

PLANS FOR THE NEXT INTERVAL

A technique will be developed to bond the diode chips which are so thin and fragile that the usual thermal bonding often cracks them.

Devices will then be tested.

B.6 MICROWAVE TRANSISTOR STUDIES

R. Dawson and J. Frey*

a. Introduction

GaAs FET structures, with one-micron gates, exhibit an f_{max} (frequency for unity unilateralized power gain) of around 35 GHz.[1,2] This frequency is about two times that reported for Si structures[3,4] of "equivalent" geometry and construction.

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*Project Supervisor

This difference has been attributed to the two-times higher peak electron velocity in GaAs. Previous workers have generally assumed that the velocities saturate at their peak values in both Si and GaAs,[3,4,5] but they do not account for the fact that good quality GaAs exhibits (a) a negative mobility region and (b) a saturated velocity almost equal to that of Si, at nearly the same field strength at which electron velocity saturates in Si.[6] These factors warrant a more detailed consideration than they have previously been given.

A similar observation has been made by Ruch,[6] who did a Monte Carlo computation under the assumptions of a uniform field and "cold" electron injection. He showed that at high fields, electron velocities over-shoot saturation values within a very short distance from the injection plane. The over-shoot in velocity was assumed to be determined by the product of low-field mobility and high field, $\mu_o E$.

According to Ruch, the excess energy associated with this velocity over-shoot can equilibrate by means of various scattering processes. In Si, the electron velocities equilibrate in a very short time, or distance, due to the relatively short scattering lengths associated with strong acoustic and equivalent intervally scattering between (100) minima. In GaAs, however, the equilibration time and distance are much longer due to the higher over-shoot velocity (since μ_o in GaAs is much greater than that in Si) and the relatively long scattering lengths associated with polar optical and nonequivalent

intervally scattering between (000) and (100) minima. The electron velocity equilibrates to the saturation values in a distance of about 0.5μ in a constant field above the saturation value. Under these conditions, the average velocity at high fields over a micron distance is thereby much higher in GaAs than in Si in spite of the nearly identical saturated velocity values.

While Ruch's computation yields considerable insight into relevant physical processes, it is doubtful that fields are actually spatially uniform in FET structures. This factor would invalidate the "cold" electron assumption and give rise to considerably less, if any, velocity over-shoot in the high-field regions of the FET.[7] Detailed consideration should be given to a nonuniform field distribution in the channel.

In the analysis presented here, the effects of negative mobility and saturated velocity are considered under highly idealized conditions; namely, (1) the low field velocities are determined by $\mu_o E$[8] (2) the velocity-field curves appropriate to GaAs doped to $10^{17}/cc$[9] are linearized (The linear curve fit is in fact quite good.) (3) velocity over-shoot effects are not included, and (4) only a static solution is considered. This analysis indicates features related to the analog performance of FETs, and identifies regions through which electrons probably travel with identifiable velocities, thereby allowing transient times to be inferred.

b. General Discussion

The fundamental physical concepts of Field Effect Transistors are easily understood on an intuitive basis. Yet the simplicity of these physical concepts belies the analytic difficulties involved in obtaining quantitative descriptions. The principal difficulty stems from the need to solve the continuity equation subject to the two-dimensional Poisson equation. The difficult nature of this problem, in spite of the rather simple geometries involved, was recognized by Shockley[11] who wrote the first definitive paper on the subject. His analysis coined the phrase "gradual channel" assumption. Over a region closest to the source where

$$\left|\frac{d^2V}{dy^2}\right| >> \left|\frac{d^2V}{dx^2}\right| ,$$

the channel width is essentially determined by the transverse field (y direction) while the current is determined by a one-dimensional longitudinal problem (x direction). A schematic of the FET is shown in Figure B.6.1. Using this approach, it is found that the channel width at some distance, ℓ, from the source, is reduced to zero, resulting in the current-saturation phenomenon known as "pinch off". An important analytical problem thus arises: current continuity must be maintained in spite of a conduction width that is theoretically nil. To satisfy current continuity, a filamentary current can be

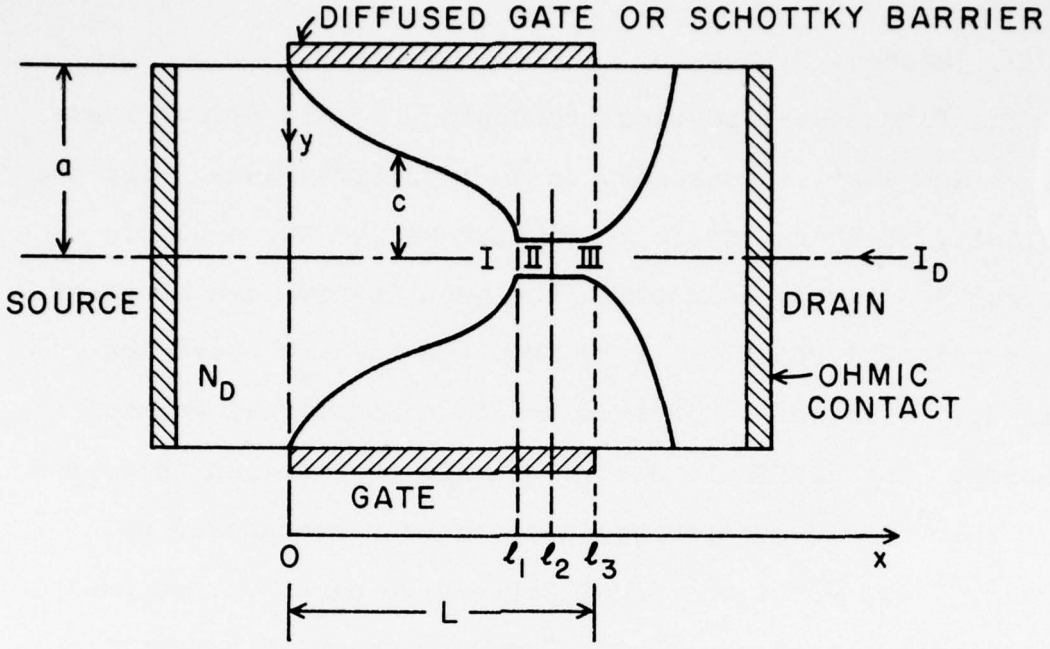


Figure B.6.1 Schematic of FET

Region I - Gradual Channel Region
Region II - Negative Mobility Region
Region III- Saturated Velocity Region

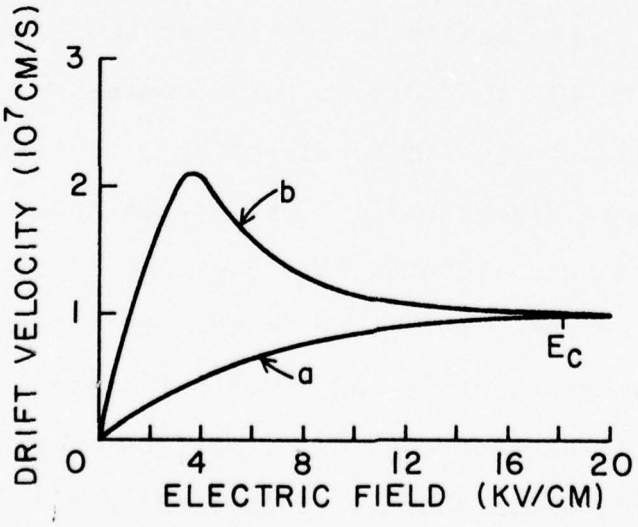


Figure B.6.2 Velocity-field characteristics in GaAs and Silicon. (After Ruch (6))

imagined; but rather good arguments also support the maintenance of a finite channel width through the "pinched off" region. Recognizing this problem, Shockley divided the FET into two regions: a "gradual channel" region near the source, and a pinched-off region near the drain. A number of techniques have been used to join these solutions, (Shockley,[11] Prim and Shockley,[13] Wu and Sah[14]) but their techniques give very little physical information with regard to the conduction mechanisms in the "pinched" region.

In many devices, particularly narrow channel structures, field strengths near the drain become very high. At fields greater than 10^3 V/cm mobilities become field dependent, and at fields greater than 1.5×10^4 V/cm, carrier velocities saturate. In such structures it can be shown that the velocity saturates before the "gradual channel" assumptions are violated.[12] One very successful multiple-region approach developed by Grebene and Ghandi[12] has used the "gradual channel" solution for the region near the source where carrier velocities are below saturation, and a solution of the two dimensional problem near the drain, using the constraint of saturated velocity. This constraint determines a well defined channel width through the "pinch off" region. Solutions for the two regions can be joined at the point where the carrier velocity saturates. Very good agreement between theoretical predictions and measured characteristics (Drain current and output resistance) was

obtained for Si devices both in trend and in absolute values. Recently Zuleeg and Lehovec[15] extended this approach to account for field-dependent mobilities before the onset of velocity saturation. While they claim that the analysis describes GaAs devices, the velocity-field characteristics used, which exhibit no differential negative mobility, are more appropriate to Si.

A rigorous solution of the two-dimensional problem has been carried out by Kennedy and O'Brien[16] for Si structures. Potential, field and charge density profiles were generated which clearly indicate that:

1. Channel widths in the pinch-off region do not become infinitesimal.
2. Excess charge densities accumulate, above the extrinsic doping levels, in the region of the channel where carrier velocities saturate.
3. Channel conduction widths increase as ratio of gate length to epilayer thickness decreases.
4. The "pinch-off" point moves toward the drain as drain voltage increases, and there is a corresponding restriction in channel conductive width.

The first three conclusions agree with those of Grebene and Ghandi,[12] while the last does not. This difference is probably related to the fact that the analytical model of Grebene and Ghandi does not include a diffusion component of current in the "pinch-off" region, nor does it allow for relaxation of the

depletion boundaries as charge is accumulated in the "pinch-off" region due to saturated velocity effects.

To date, several people have combined various aspects of the models discussed above to specifically describe GaAs devices: Zuleeg and Lehovec,[4] Turner and Wilson,[5] Drangeid and Sommerholder,[3] Baechtold,[17] and others. These analyses predict a number of features exhibited by GaAs FETs reportedly related to saturated velocity effects. Several of these features are (1) f_{max} in inversely proportional to channel length*, (2) the transconductance is nearly constant over a significant range of gate voltage (3) device parameters agree reasonably well when various physical properties are adjusted for best fit (4) premature saturation of drain current is directly related to the occurrence of saturated velocity. These analyses must be described as relatively successful in terms of theoretical and experimental agreement, yet the common assumption that electron velocity saturates at the peak velocity value may, at the very least, be misleading. For example, negative mobility effects may be responsible for Baechtold's observation of anomalous noise behavior in GaAs FETs.

c. Velocity-Field Characteristics

For comparative purposes, the velocity-field characteristics of intrinsic GaAs and Si are shown in Figure B.6.2. These characteristics indicate the nearly equivalent values of saturated velocity, $v_s \tilde{=} 10^7$ cm/sec., at fields of about

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*For constant mobility devices, f_{max} is inversely proportional to channel length squared.

2×10^4 volts/cm. At low fields, the characteristics are influenced by impurity scattering which results in lower mobilities for higher doped materials. In Figure B.6.3 characteristic velocities and fields for GaAs are identified, corresponding to a linearization of the data of Ruch and Fawcett[9] for a doping density of $10^{17}/cm^3$.

d. Analysis

Three regions are considered in the FET of Figure B.6.1: gradual channel, negative mobility region and saturated velocity region. A complete solution of the potential, voltage and current characteristics requires a time development of the continuity equation, including drift, diffusion, and displacement components of current. While one must be alert to the possibility of time varying, or unstable solutions indicative of oscillations due to bulk negative resistance or due to nucleation and movement of domains,[18,19,20] experimentally, stable static operation is usually observed. We therefore look for a static solution of the continuity equation:

$$I_D = I_{Drift} + I_{Diffusion}.$$

Minority carrier components will be neglected due to the predominance of majority carriers and the absence of junctions in the assumed direction of current flow.

Region I. Gradual Channel: $0 \leq x \leq \ell_1$. In this region the diffusion component is neglected.

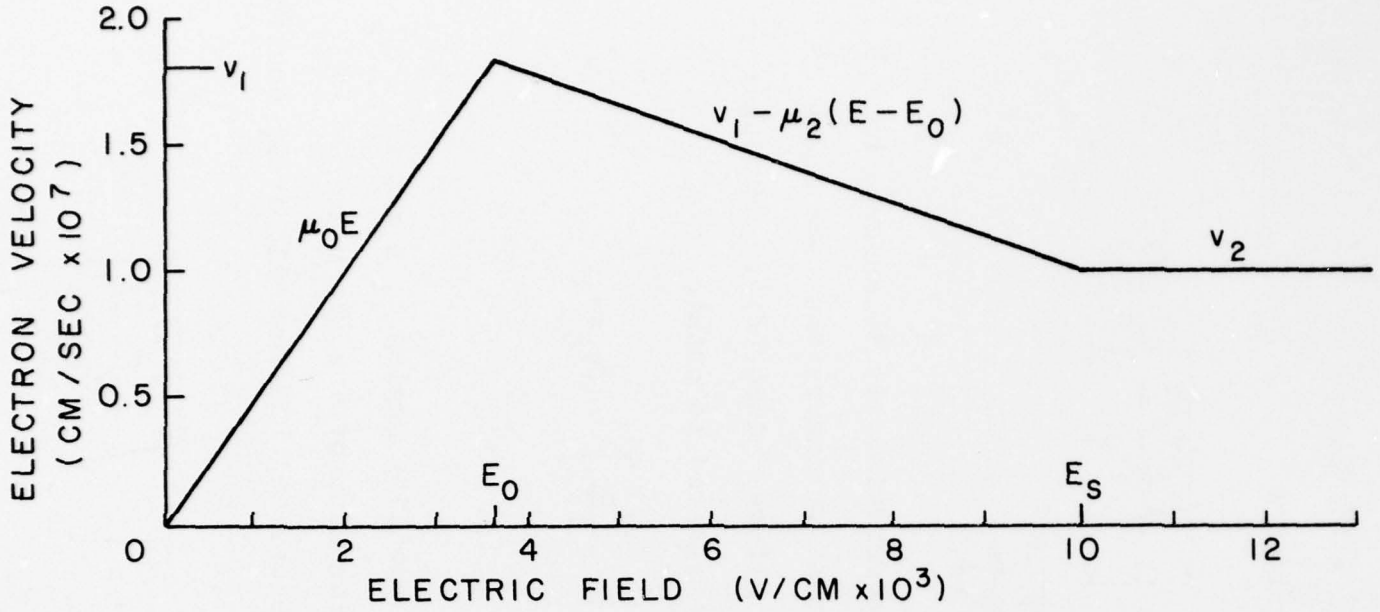


Figure B.6.3 Velocity field Characteristics for GaAs (Linearized), $N_I = 10^{17}$ atm/cc

$\mu_o = 5{,}000 \frac{cm^2}{volt\text{-}sec}$ $\quad E_o = 3.6 \times 10^3$ v/cm

$\mu_2 = 1{,}080 \frac{cm^2}{volt\text{-}sec}$ $\quad E_s = 10 \times 10^3$ v/cm

$$(1)\quad \vec{I}_D = -qN_d\, c(x)\, b\, \vec{v}$$

where $\vec{v} = -\mu_o \vec{E}$ and $\vec{E} = -\vec{\nabla} V(x)$

b = channel perimeter

$$(2)\quad \vec{I}_D = -qN_d\, 2\, b\, a \left[1 - \sqrt{\frac{V_g+V_B+V}{|V_p|}}\right] \mu_o \frac{dV}{dx}\, \hat{x}$$

where $c(x) = a\left[1 - \sqrt{\frac{V_g+V_B+V}{|V_p|}}\right]$.

For the devices under consideration, it is assumed that, $V_{\ell 1} < V_p - (V_g + V_B)$ in order to insure that the onset of field dependent mobility occurs before "pinch off". Letting $-\left.\frac{dV}{dx}\right|_{\ell_1} = E_o$, equation (2) can be integrated to obtain

$$V_{\ell_1} = V_p \left[1 - \frac{I_d}{KE_o}\right]^2 - (V_g+V_B)$$

where $K = 2q\mu_o baN_d$

Region II. Negative Mobility Region $\ell_1 \leq x \leq \ell$

In this region the following assumptions are made:

(1) The width of the channel remains relatively constant as determined by V_{ℓ_1}, i.e.,:

$$c(x) = c'_\ell = a\left[1 - \sqrt{\frac{V_g+V_p+V_{\ell_1}}{V_p}}\right]$$

and $$c_\ell = c'_\ell/a \quad .$$

Self consistency will be examined later for this particular solution.

(2) Excess charge density is expected to accumulate as governed by Poisson's equation:

$$\frac{\partial^2 V}{\partial x^2} = q \frac{n(x)}{\varepsilon}$$

(3) In spite of the expectation that excess carriers accumulate in Region II, diffusion current is at first neglected, and then examined for self consistency.

(4) The field magnitude is assumed to be a monotonically increasing function of x.

Starting with equation (1) where in Region II the velocity is given by:

$$\vec{v} = -[\mu_o \vec{E}_o - \mu_2 (\vec{E} - \vec{E}_o)]$$

$$= [\mu_o |E_o| + \mu_2 \frac{\partial v}{\partial x} + \mu_2 |E_o|] \hat{x}$$

and assuming that c_ℓ remains relatively constant over Region II, the following equation for V(x) can be obtained:

$$\frac{dV}{dx} = -|E_o| \left(1 + \frac{\mu_o}{\mu_2}\right) + \sqrt{|E_o|^2 \left(\frac{\mu_o}{\mu_2}\right)^2 - \alpha\left[(x-\ell_1) + \frac{V(x)-V_{\ell_1}}{|E_o|}\right]} \quad (8)$$

where $$\alpha = \frac{2qN_d}{\varepsilon} |E_o| .$$

Equation (8) can be integrated numerically. At this stage

we can examine two plausible solutions:

(1) Average field through Region II given by

$$\frac{|E_o| + |E_s|}{2} \text{(linear increase)}.$$

Then, $$V(x) \cong (x-\ell_1)\left[\frac{|E_o| + |E_s|}{2}\right] + V_{\ell_1}, \text{ and}$$

$$\alpha(x-\ell_1) + \frac{\alpha\left[V(x)-V_{\ell_1}\right]}{|E_o|} \text{ is of the order of } 10^{14}$$

for reasonable parameter values.

In this case

$$x - \ell_1 \leq 0.01_{\mu}$$

in order for a static solution with negligible diffusion to be meaningful. Distances of this order are extraordinarily small. Since the field drops from E_s to E_o over this region, a significantly high density of charge must be accumulated in Region II.

(2) Average field in Region II is zero, i.e.,

$$V(x) - V_{\ell_1} \cong 0.$$

Then, in order for the quantity within the square root of (8) to be positive,

$$x_{max} - \ell_1 \leq \frac{|E_o|^2}{\alpha}\left(\frac{\mu_o}{\mu_2}\right)^2$$

$$\leq \sim 0.03\mu \quad .$$

Situation 1 corresponds to a linear increase in field and a constant excess charge density through Region II. But this clearly implies a non-physical solution because diffusion current would be infinite at the boundary of regions I and II but zero through regions I and II. Situation 2 is not much more physical, but at least these approximations allow a rough estimate for the extent of Region II, without obtaining an explicit solution. Since the distances indicated are extraordinarily small, and charge accumulation is significant, it is doubtful that the original approximation of negligible diffusion current is valid.

e. Conclusion

A cross-check on the assumption that drift dominates in Region II indicates that diffusion is not negligible. A distance of about 0.03μ is predicted for the extent of Region II by the drift analysis. It is possible that inclusion of the diffusion component of current will not significantly alter the prediction of a small Region II. A solution to the combined drift-diffusion equation will be required to establish the physical dimensions and behavior of the negative mobility region. The solution to Region III for the saturated velocity region has been carried out by Grebene and Ghandi.[12] Their analysis can be readily adopted. It may be desirable, however, to extend their analysis to include diffusion, since significant charge accumulation is expected in Region III as well as

in Region II. The solution for the three regions can be joined for a composite description. Should Region II be extremely small, the joining procedure can be simplified by the idealization of a thin sheet of charge across which the field drops from E_s to E_o. The details of this procedure await a more definitive description of the negative mobility region.

The conjectured conclusions set out below require further investigation. Should the result of a very small physical size of the negative mobility region be substantiated by further analysis, more definitive observations can be made. In the light of the preceding analysis, then:

1. In GaAs FETs operated above saturation fields, $|E| > 10^4$ V/cm, the carrier velocity drops to a saturated value of 1×10^7 cm/sec rather than 2×10^7 cm/sec, the value usually taken.

2. The distance indicated by a static field solution over which this drop in velocity occurs is extremely small.

3. The actual distance required for carriers to drop in velocity from their peak values is probably determined by a characteristic scattering time for intervally scattering, $\tau \cong 10^{-13}$ sec, leading to a distance of about 0.03 μ. This distance may be comparable to the extent of Region II.

4. The majority of features that have been attributed to GaAs structures due to saturated velocity are probably appropriate to analogue operation with the exception of the

major and general conclusion that "GaAs FETs are better than Si FETs because of a higher saturated velocity". The experimental superiority of GaAs structures is probably related to other factors: (a) velocity relaxation effects[6] (b) higher velocity in low field regions of the device than in Si devices (c) less source degenerative resistance (d) lower parasitic substrate losses.[6,21,22]

5. Under very high field operation, i.e., in high-power structures, the frequency response of GaAs devices is expected to be degraded, because a longer portion of the channel would experience a saturated velocity which appears to be lower than previously assumed.

PLANS FOR THE NEXT INTERVAL

During the next interval, the difficulties in finding either an analytical closed-form solution, or a numerical solution, of the equations for the GaAs FET will be explored. Mask designs for scaled oversize FETs, which will be fabricated in order to verify the conclusions reached here, will be designed.

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B.7 EVALUATION OF THE RELAXING AVALANCHE MODE

M. Randles, C.A. Lee* and G.C. Dalman*

An experimental investigation of the relaxing avalanche mode of a silicon avalanche diode has been started.

This study proposes to supply some experimental data for the relaxing avalanche mode of operation of a silicon P+-n-n+ avalanche diode as outlined by F.G. Zappert.[1] For example, some experimental criterion needs to be developed for differentiating the relaxing avalanche mode from the avalanche resonance pumped or IMPATT modes. In addition, noise measurements will be made and circuit tuning effects will be investigated. The relaxing avalanche mode has been shown to have interesting amplifier properties[2] which merit further study.

Work has begun on the construction of a coaxial FM noise measuring system that will operate between 4 and 8 GHz. This

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*Project Supervisor

system will complement the X-Band FM noise test-set already in use here.

PLANS FOR THE NEXT INTERVAL

The 4-8 GHz FM noise system will be completed and used to test a CW relaxing avalanche mode oscillator. In exploring the topics mentioned herein, experimental effort will focus upon those of most immediate importance.

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B.8 SYNCHRONOUS DETUNED OSCILLATOR POWER COMBINER

B. Ho and G.C. Dalman*

a. Introduction

In comparison with vacuum tube devices, present-day single diode microwave solid-state oscillators put out very small amounts of power so that, in many applications, solid-state diode oscillators cannot compete with vacuum devices. Two methods of increasing the power levels of solid-state devices have been tried, viz., increase the power of a single diode, and combine the outputs of a number of low power diodes. This report

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*Project Supervisor

will focus on the power combining method.

Recently, several power combining methods have been shown to be feasible. Fukui[1] has successfully combined the power of a number of separate solid-state oscillators in a Hybrid circuit, and Rucker and Kurokawa[2,3,4] have described methods of combining powers of a number of oscillator diodes in a single cavity and in a symmetrical design. However, there are certain disadvantages and restrictions related to the above methods; for example, nearly identical diodes are required and the suppression of all unwanted modes is necessary for optimal performances. Dalman and Lee[5] have been able to overcome these restrictions in their "synchronous detuned microwave oscillator power combiners". The synchronous detuning method of combining oscillators' power is simply a method of combining detuned oscillators' power when they are frequently locked. The task of this report is to broaden this synchronous detuning idea experimentally and theoretically. Emphasis is placed on obtaining a better understanding of the operation and obtaining better performance.

This quarter's work involves combining the powers of two nearly ideal oscillators by the synchronous detuning method. The purpose of this test is to record the performance of nearly ideal oscillators and to use them in the future as controls to explain the less ideal solid-state diode oscillators. For the near ideal oscillators, reflex klystrons are used. In these control experiments, the input power level is the main variable.

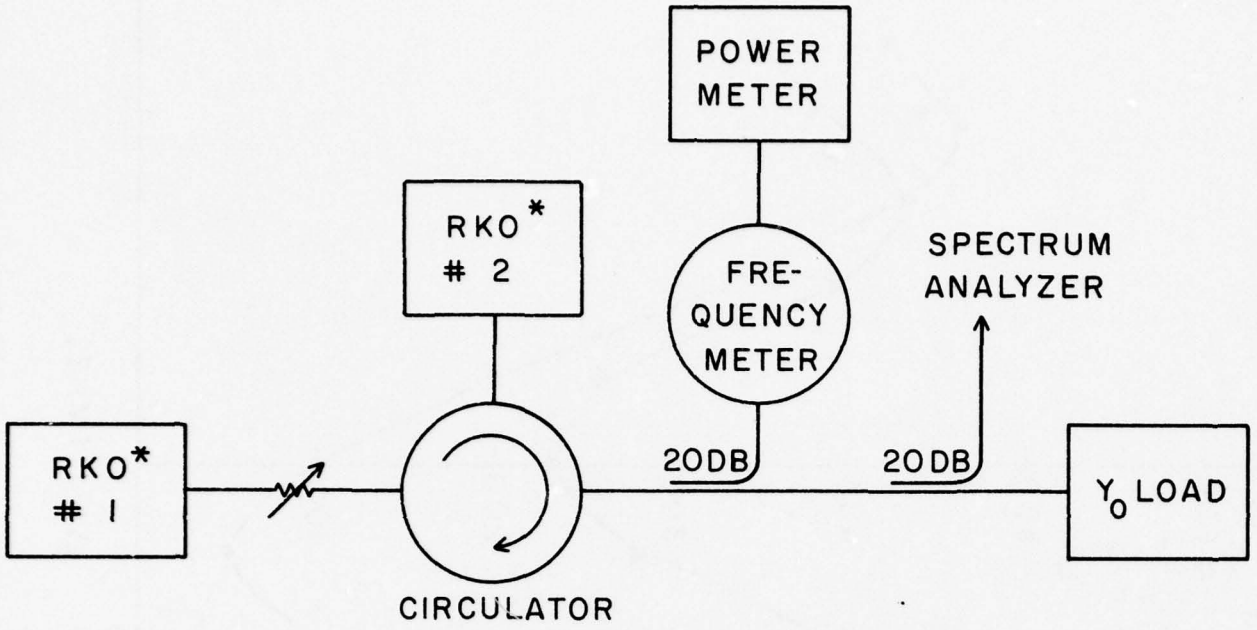
b. Experiment

The experimental set-up used for the measurements is shown in Figure B.8.1. The power combining characteristics of two reflex klystrons with the same power level but operating at different repeller modes were tested. It was found that the output power characteristic is more symmetrical with the higher voltage repeller mode on the second reflex klystron. The result of these tests are shown in Figure B.8.2 for 200 mW operation and Figure B.8.3 for 300 mW operation. It is seen from Figures B.8.2 and B.8.3 that the output powers at certain frequencies are greater than the sum of the two input powers. This phenomena will be investigated further in the future.

Figures B.8.4, B.8.5 and B.8.6 illustrate how the output power varies with different input powers as a parameter. In Figure B.8.4, the locking power (P_1) was held constant while the oscillator power (P_2) was varied; in Figure B.8.5 the locking power was varied as the oscillator power was held constant; and in Figure B.8.6, both of these power levels were changed, but $\frac{P_o}{P_2}$ was held constant to maintain a constant locking range. From all three graphs, we can make the following conclusions:

1. The graphs all exhibit the same kind of symmetrical curves, centered approximately at f_o (only a slight shift in f_o was observed).

2. The output powers at certain frequencies within the locking range are greater than the sum of input powers. This



*REFLEX KLYSTRON OSCILLATOR

Figure B.8.1 Experimental Set-up for Studying Synchronous Detuning Method of Power Combining.

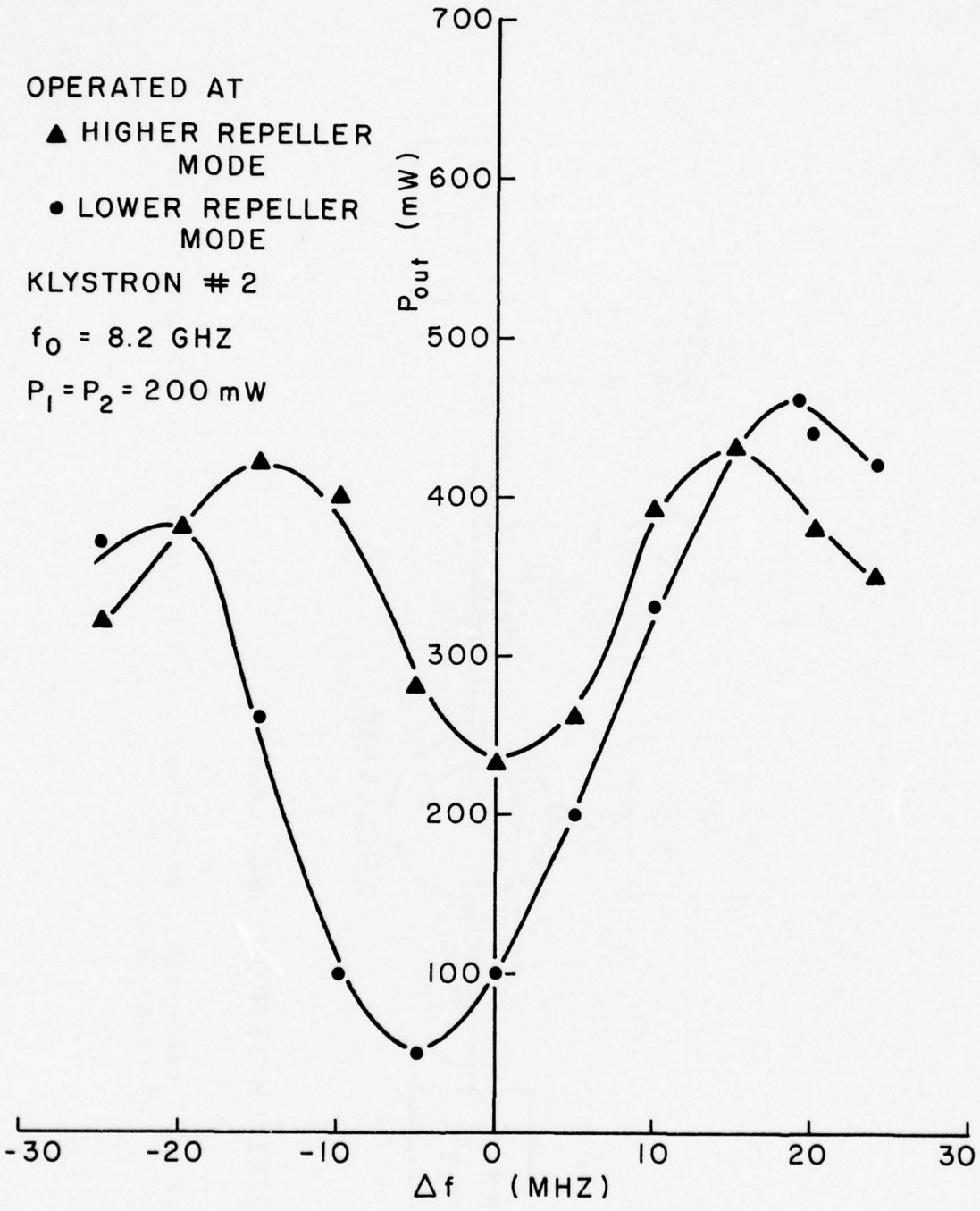


Figure B.8.2 P_{out} as a function of klystron #2 repeller modes (the repeller mode of klystron #1 is fixed)

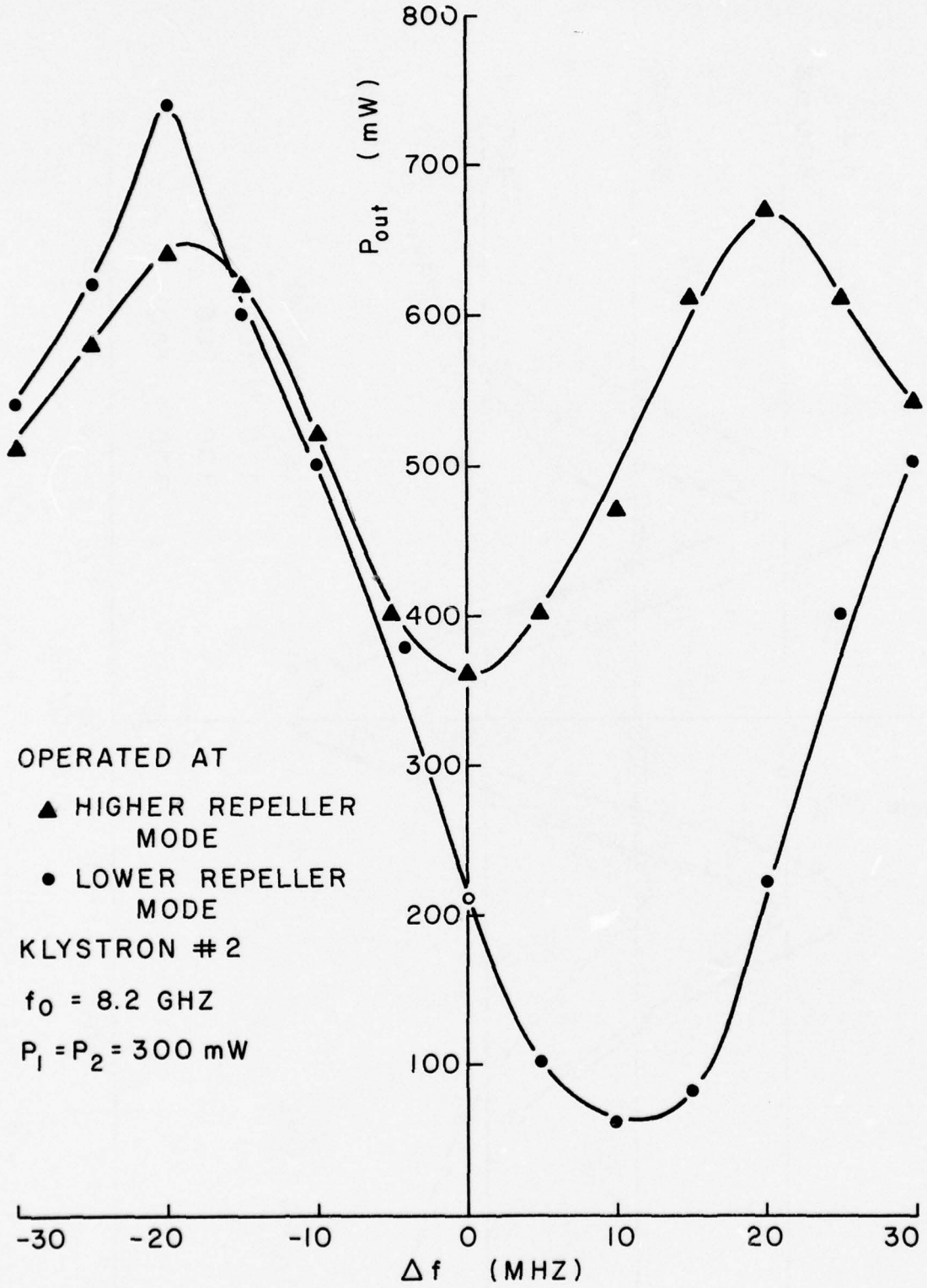


Figure B.8.3 P_{out} as a function of klystron #2 repeller modes (the repeller mode of klystron #1 is fixed).

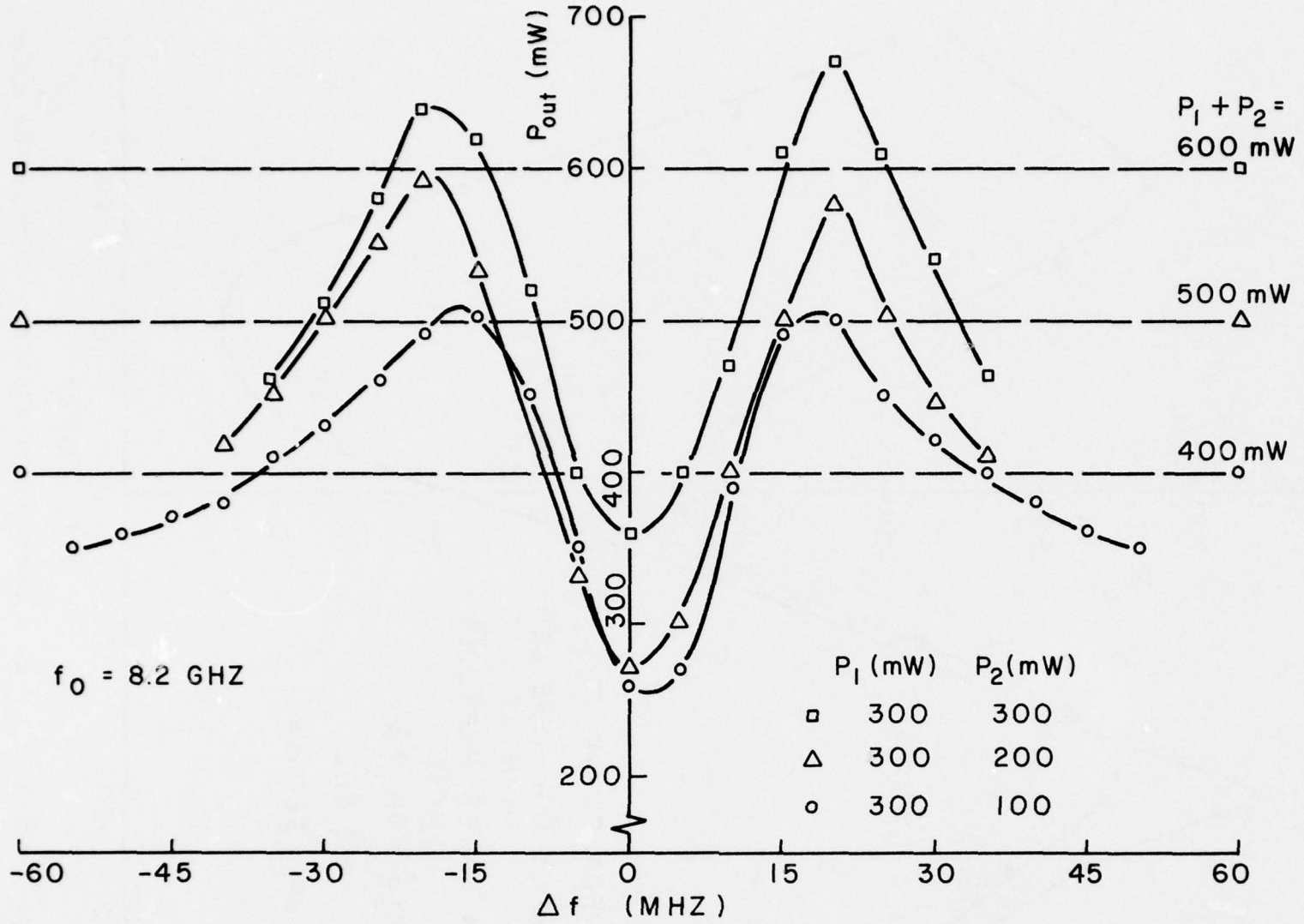


Figure B.8.4 P_{out} vs. frequency when P_1 is constant.

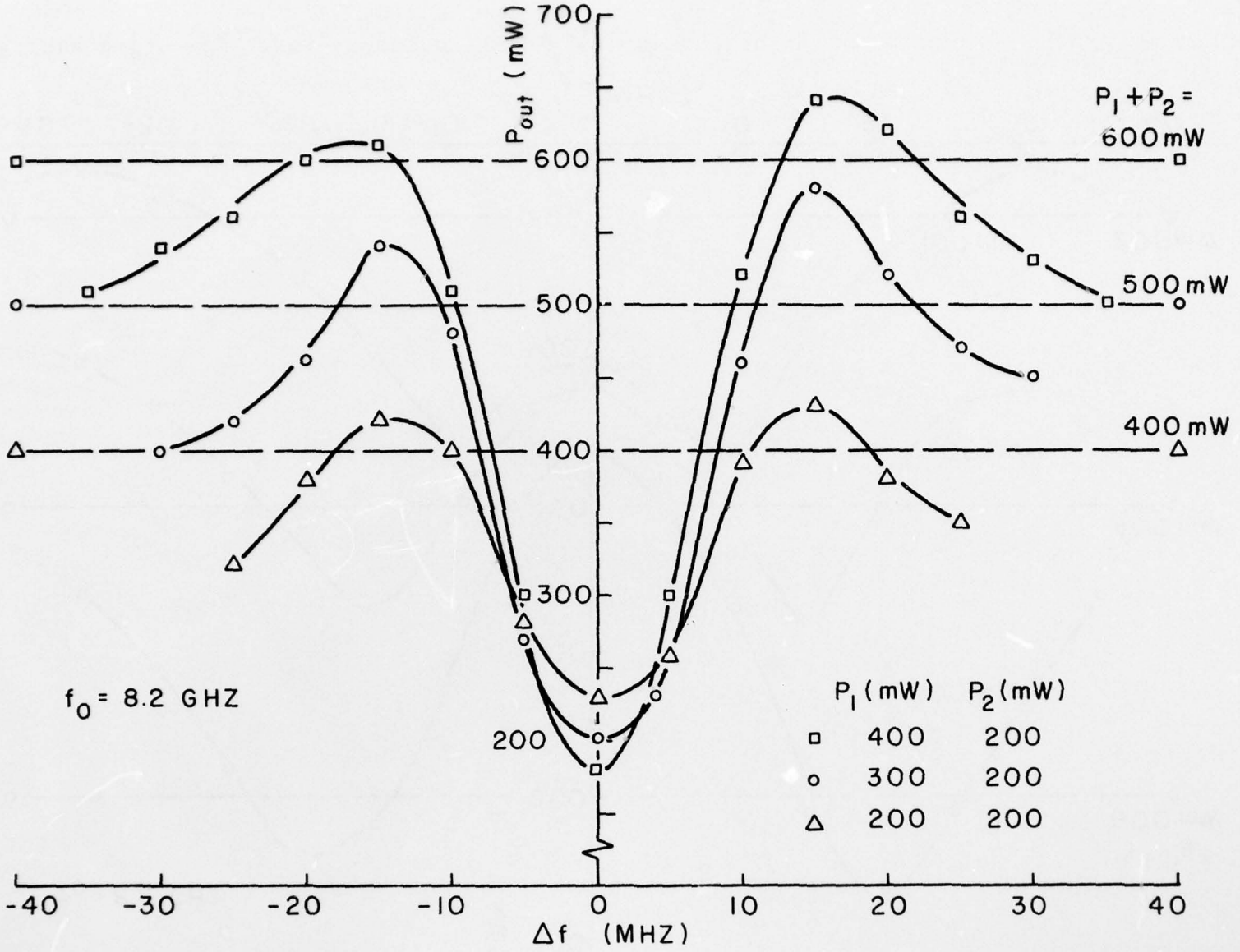


Figure B.8.5 P_{out} vs. frequency when P_2 is constant.

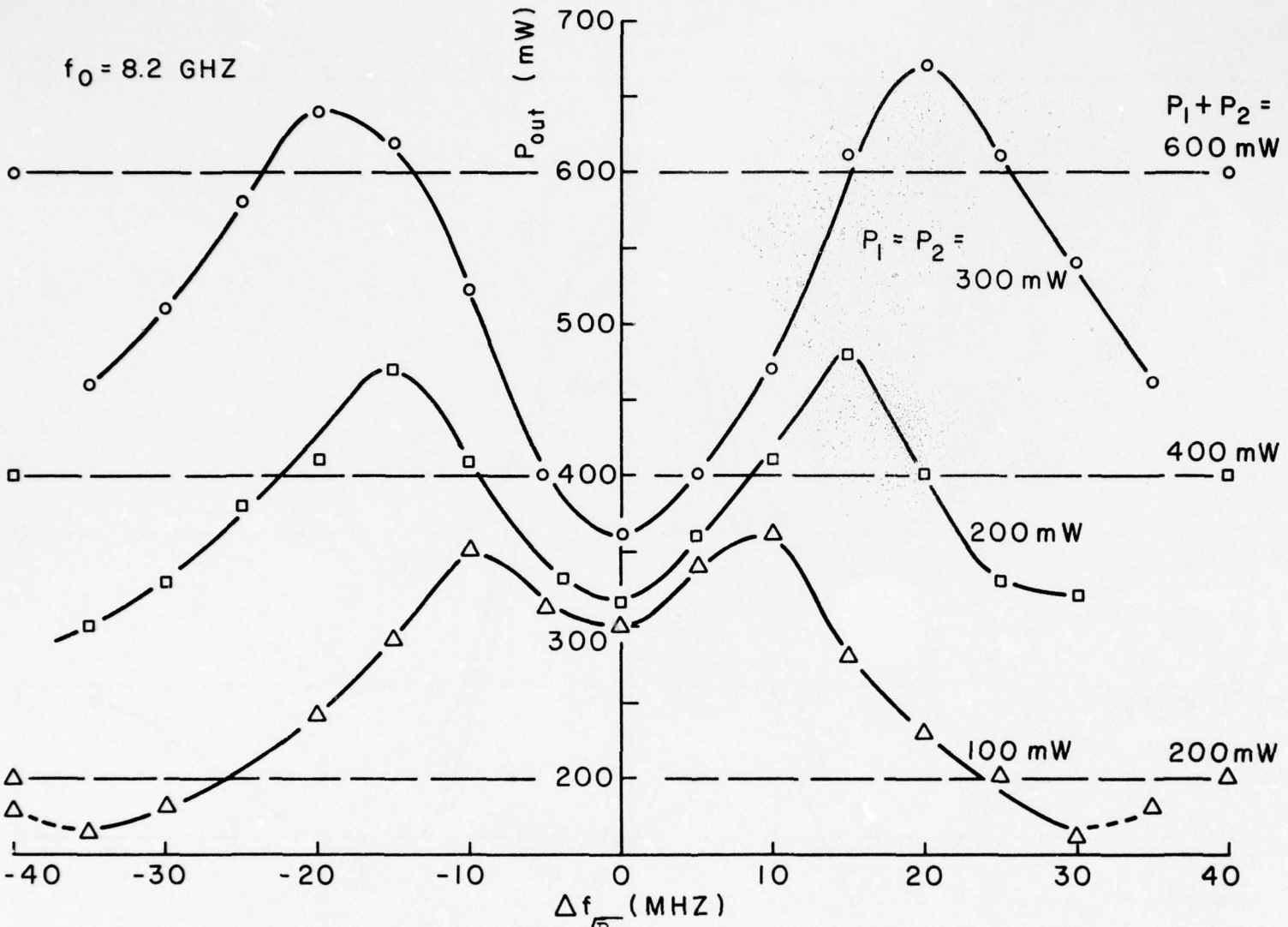


Figure B.8.6 P_{out} vs. frequency when $\sqrt{\frac{P_1}{P_2}}$ is constant.

phenomena was observed in every case.

3. If the oscillator power (P_2) is held constant, the peak to valley output power difference increases with increasing locking power (P_1) and the output power at f_o (the minimum power) decreases with increasing locking power.

4. If the locking power is held constant, the peak to valley output power difference does not vary much with different oscillator power, however the output power at f_o is increased with increasing oscillator power.

5. For the same locking range, all of the curves seem to have nearly the same shape except that high input powers will increase the frequency difference between maximum output powers.

PLANS FOR THE NEXT INTERVAL

Work on the synchronous detuning method of power combining will be continued. The emphasis will be on solid-state diode IMPATT oscillators. Theoretical work will also be included.

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C. SOLID STATE MATERIALS STUDIES

INTRODUCTION

An important part of the research and development program on solid state microwave oscillators and amplifiers has been directed towards a better understanding of the materials used for the solid state devices being studied. This program is of considerable importance since the ultimate performance of the device is directly related to materials quality. Progress made on an ion implantation program is reviewed in Section 1, the results of a study program on ionization rates in GaAs are described in Section 2, and work underway on vacuum epitaxial growth of silicon is discussed in Section 3.

C.1 Ion Implantation and Diffusion

D. Edwall, J. Frey* and C.A. Lee*

During this period, the 200 Kev ion implantation machine was completed. All components of the machine (vacuum systems, high voltage power supply, and ion source) have now been tested separately, although some difficulty has arisen in properly aligning the beam in the separator magnet.

A final report on the construction of the machine is in progress.

PLANS FOR THE NEXT INTERVAL

The beam alignment problem should be resolved during this interval, and test implants performed.

C.2 IONIZATION RATES IN GaAs

D. McCarthy and C.A. Lee*

During the previous quarter multiplication measurements were made on metal-gallium arsenide Schottky barrier structures. The measured multiplication factors will be used to calculate the ionization rates for electrons and holes. The method that is used to measure the multiplication factors is of great importance in determining the reliability of the calculated ionization rates. The experimental apparatus used to make the multiplication measurements will be described here.

As the reverse bias is increased across a junction, the

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electric field within the depletion will also increase. At sufficiently high electric fields there will be an increase in the primary reverse current due to avalanche multiplication. The multiplication factor is defined as the ratio of the multiplied current to the primary reverse current. In measuring the multiplication factor it would be misleading to take the ratio of the direct currents involved because of leakage currents and generation within the space charge region. To get around this problem signals produced by carriers specifically injected into the high field region should be studied. One of the most convenient methods of generating carriers in a semiconductor is to generate electron-hole pairs by irradiating the semiconductor with light. Light is used to generate carriers in the present investigation.

A schematic representation of the apparatus used in the multiplication studies is shown in Figure C.2.1. This method of measurement is similar to that used by Lee et al.[1,2] In this experimental arrangement, the light is chopped and focused onto the junction through the objective of a microscope. This scheme makes it possible to illuminate a very small part of the junction thus making it easier to control the scattered radiation striking the junction. The uniformity of the multiplication over the junction can also be investigated by scanning the junction with the small diameter spot of light. Electrical contact is made to the top of the mesa means of a tungsten pointer mounted on

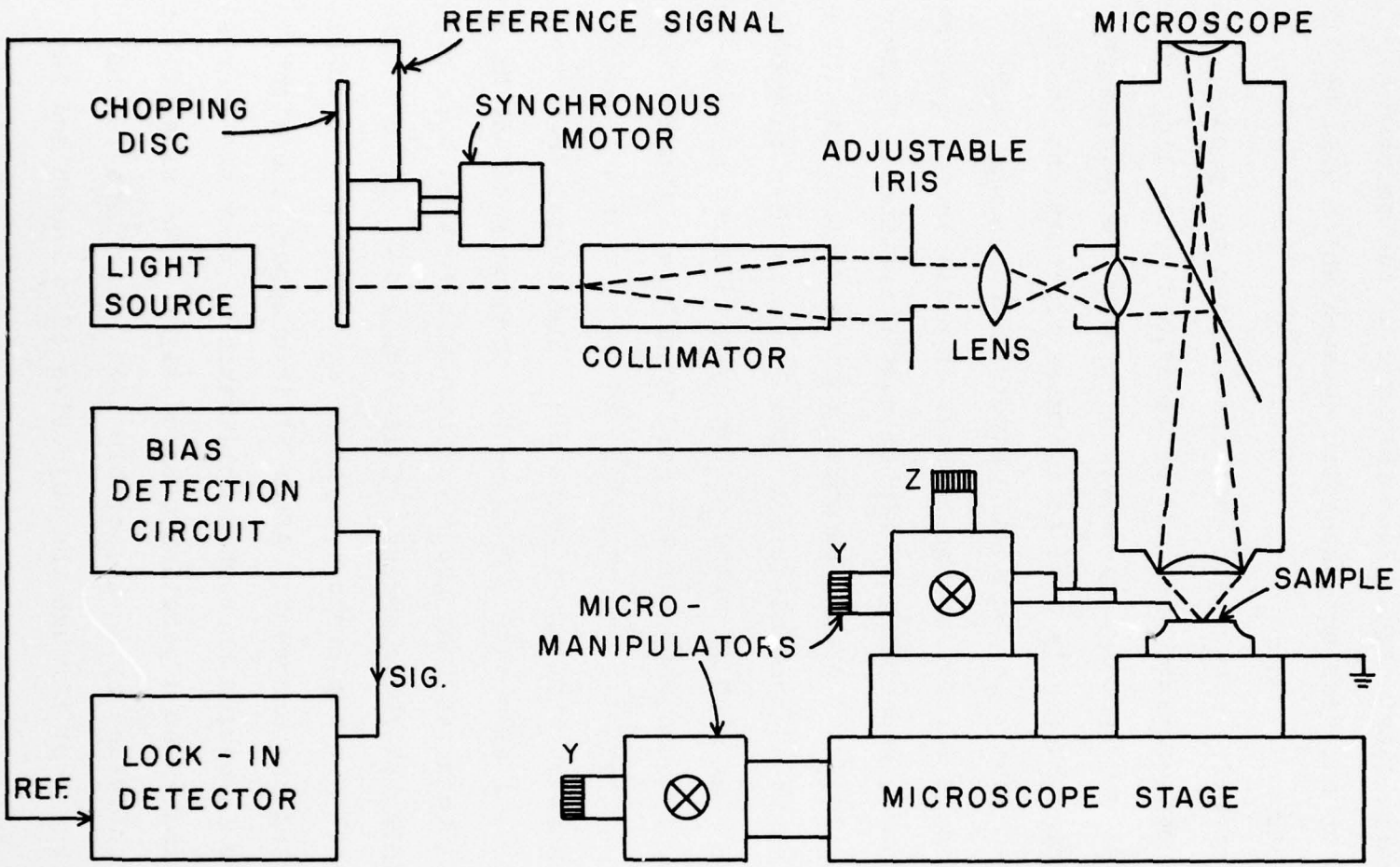


Figure C.2.1 Schematic diagram of apparatus used for multiplication studies.

a micromanipulator stage. The other end of the pointer is connected to the bias and detection network which will be discussed later.

The specific components that are used in the present multiplication measurements will now be described. The light source consists of a tungsten lamp driven by a regulated d.c. supply. The regulated supply is used to minimize fluctuations in the intensity of the tungsten lamp. Fluctuations in the light intensity will introduce a great deal of noise in the measured photoresponse, especially at higher multiplications. Filters are placed in front of the tungsten lamp to control the intensity and wavelength of the radiation. The light is then chopped by a chopping disc with 15 slits driven by a 1800 rpm synchronous motor; the induced photocurrent will then have a fundamental frequency of 450 Hz. The chopping disc also passes between another tungsten lamp and a photocell. The signal from the photocell will also have a fundamental frequency of 450 Hz and there will be a constant phase relationship between this signal and the injected photocurrent. This signal is used as a reference signal for the purpose of phase sensitive detection of the injected photocurrent. After it is chopped, the light from the source is passed through a collimator so that the source can be approximated as a parallel beam of light. The size of the beam is controlled by an adjustable iris and a lens is then used to focus the beam through the objective of a Bausch and Lomb

model DMETR microscope. Spot sizes of less than ten microns can be achieved with the present system.

The bias and detection circuit used in obtaining the multiplication characteristics of the junctions investigated will now be described. The simplest type of bias and detection circuit is shown in Figure C.2.2. Although this circuit has been used successfully by earlier investigators[3] it has several advantages. The major difficulty arises from the fact that for the junction to behave as a current source producing the induced photocurrent the impedance of detection circuit must be much less than the dynamic impedance of the junction. This condition requires that the capacitor by-passing the potentiometer be quite large and the series sampling resistor be quite small. The large value of capacitance could be impractical for junctions with large breakdown voltages, and the low value of sampling resistor will, of course, limit the sensitivity of the circuit. Another disadvantage of this circuit is that grounding problems may become important. One advantage of this circuit is that it allows for the direct observation of the induced photocurrent as well as the noise in the junction.

A greatly improved bias and detection circuit similar to that used by Lee *et al*[2] is shown in Figure C.2.3. This circuit makes use of two series resonant circuits each with a resonant frequency equal to the fundamental frequency of the injected photocurrent. One of the resonant circuits is directly across

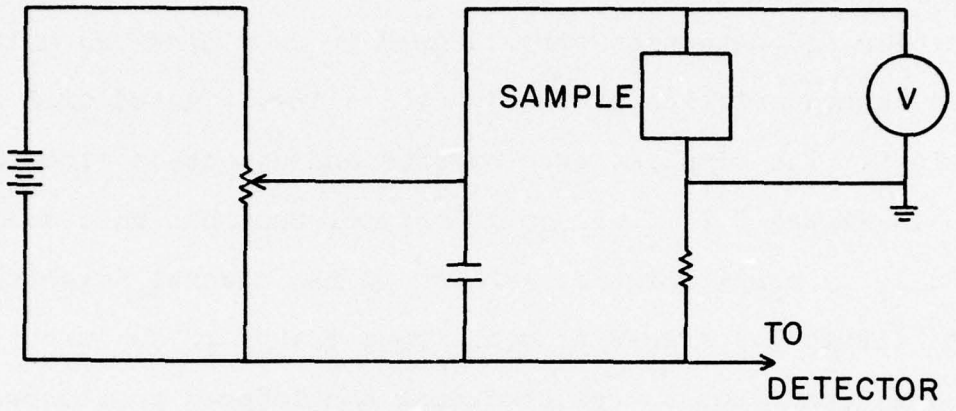


Figure C.2.2 Bias and detection circuit for multiplication studies.

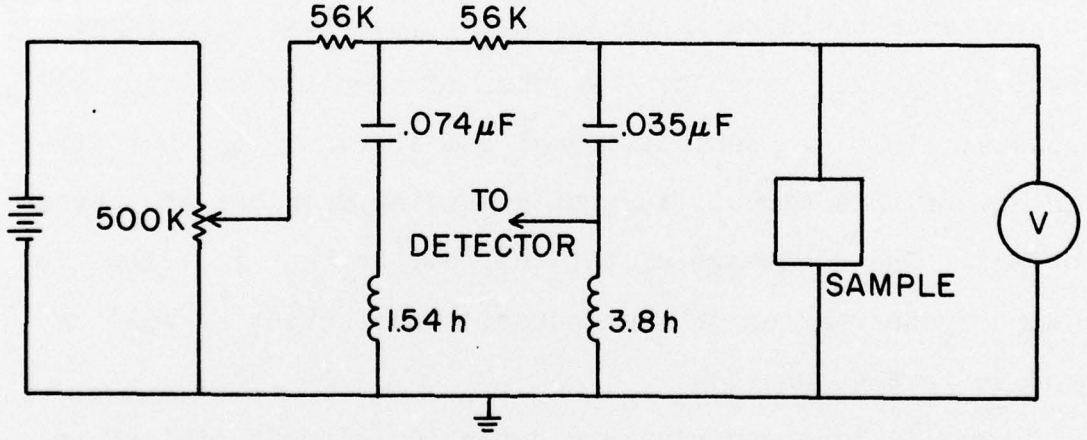


Figure C.2.3 Improved bias and detection circuit for multiplication studies.

the junction thus serving as a low impedance path for the fundamental component of the photocurrent. In addition to forming a low impedance path for the photocurrent, this resonant circuit is used to detect the photocurrent. Assuming that a phase sensitive detection scheme is used the signal appearing at the detector input will equal $2 \pi f_o L I_{PH}$, where f_o is the fundamental frequency of the photocurrent, I_{PH} is the fundamental Fourier component of the photocurrent, and L is the inductance in the resonant circuit. This represents a signal significantly greater than the signal that would be detected by the circuit shown in Figure C.2.2 thus the sensitivity of the detection circuit is greatly increased by this type circuit. The second series resonant circuit shown in Figure C.2.3 serves as a low impedance path for any extraneous signals at the fundamental frequency introduced by the bias circuit. The two series resonant circuits are decoupled by the large resistance shown in the circuit diagram. In addition to providing a low impedance path for the photocurrent and greatly increasing the sensitivity of detection circuit the circuit shown in Figure C.2.3 has a common ground connection, which is desirable. The only advantage of the circuit shown in Figure C.2.2 over the circuit shown in Figure C.2.3 is that photocurrent cannot be viewed directly by the latter circuit. This, however, is a minor disadvantage of the latter circuit compared to its advantages. Because of the reasons mentioned above, the circuit

shown in Figure C.2.3 is used in the present multiplication studies. The outputs of the voltmeter shown in Figure C.2.3, as well as the lock-in detector shown in Figure C.2.3, are applied to the inputs of an X-Y recorder. Thus as the bias is slowly changed a curve of the photocurrent versus applied bias is directly traced out.

PLANS FOR THE NEXT INTERVAL

In the next interval multiplication measurements will be continued. Ionization rates for electrons and holes will be calculated from the measured multiplication factors.

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C.3 VACUUM EPITAXIAL GROWTH IN SILICON

A. Kimura and C.A. Lee*

During the last quarter, epitaxial growth of NN^+ junction by sublimation in high vacuum system has been continued. Some improvements were made on the procedures of sublimation which resulted in a large reduction of etch pit density at the NN^+

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*Project Supervisor

interface. Si Schottky barrier diodes with hard breakdown characteristics were fabricated from the low etch pit density wafer.

As was reported in the last Quarterly Progress Report, a relatively high etch pit density was observed at the interface of L-H junction grown by sublimation. A sudden increase in the background pressure at the beginning of sublimation was considered to be the cause of some unwanted deposits of material on the substrate surface. In order to avoid the problem, both the substrate and the source wafer was heated at the same temperature up to 1340°C until the background pressure came down to 1×10^{-8} torr. Then the RF coil was shifted upwards to keep the source temperature at 1340°C, while lowering the substrate temperature. It is believed that this procedure minimizes deposition of unwanted materials on the substrate surface as a result of high background pressure. Figure C.3.1 shows the variation of temperature and background pressure during sublimation.

Figure C.3.2 shows an appreciable reduction in etch pit density after sublimation compared to the pictures shown in the previous report.[1]

Si Schottky barrier diodes were fabricated from the NN^+ epitaxial wafer to determine the quality. Figure C.3.3 shows a static characteristic of Si Schottky barrier diode fabricated from NN^+ epitaxial wafer grown by sublimation. It represents

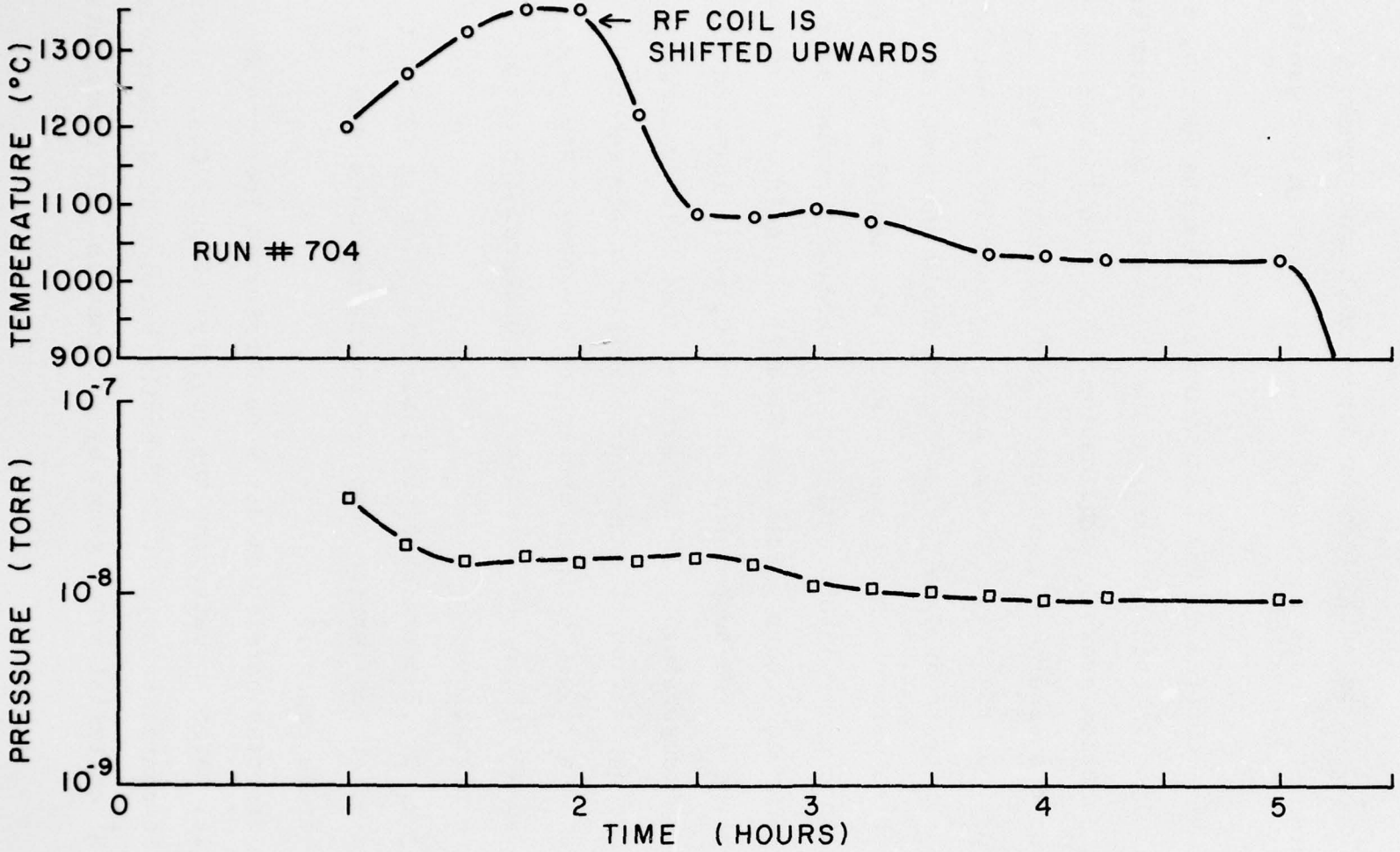


Figure C.3.1 Variation of Temperature and Pressure.

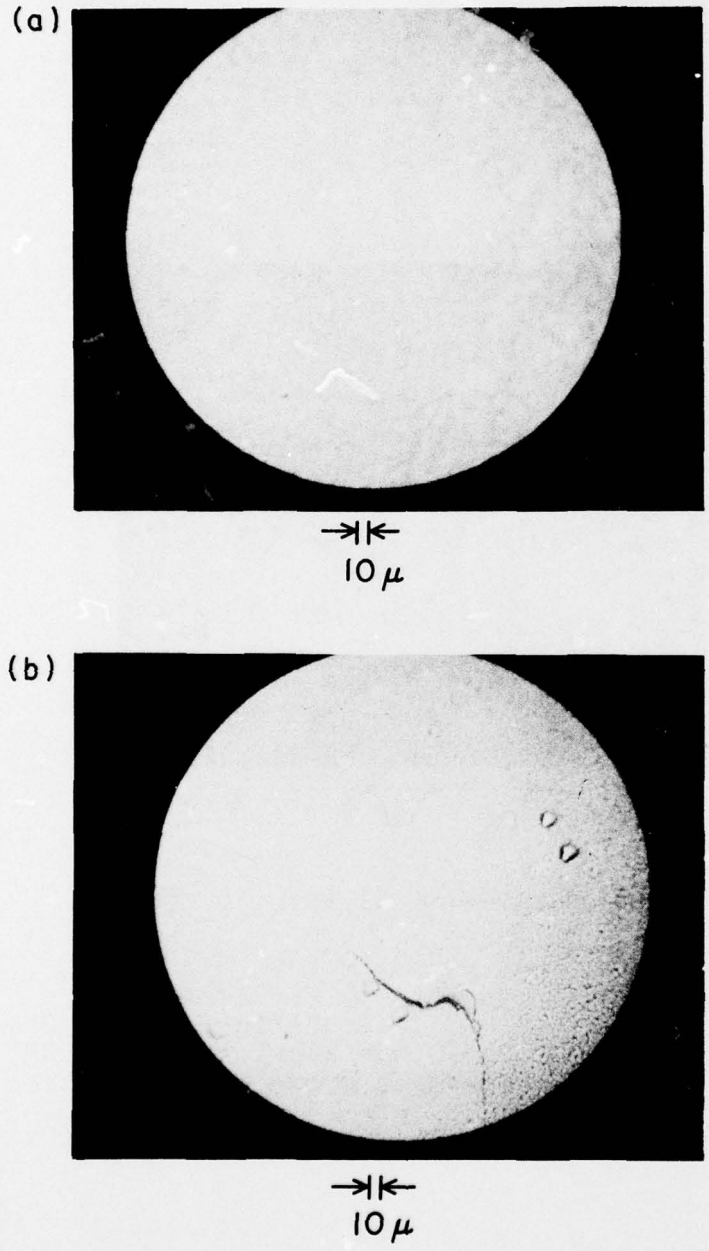


Figure C.3.2 (a) Sirtl Etched Surface of Substrate before sublimation.

(b) Interface of NN^+ junction after epitaxial growth.

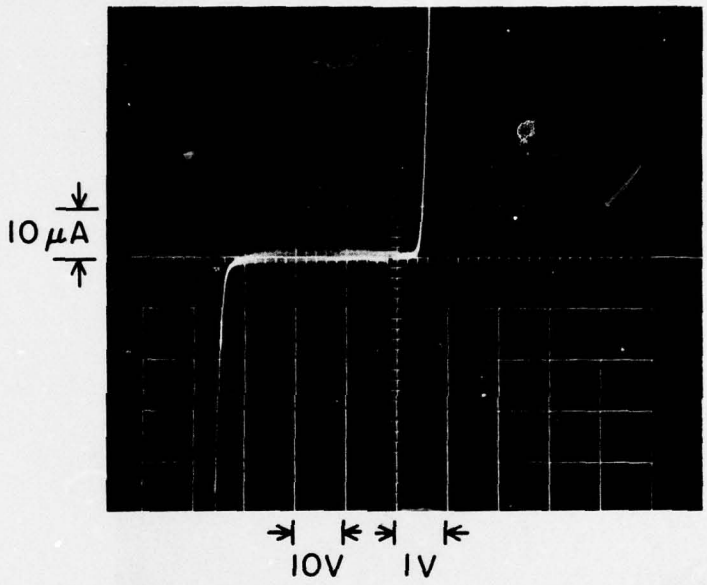


Figure C.3.3 A static characteristic of Si Shottky Barrier Diode Fabricated from NN^+ Epitaxial Wafer grown by sublimation.

a hard breakdown characteristic in the reverse direction indicating a good quality of the grown epitaxial layer. Figure C.3.4 shows the C-V plots of the diode. It is seen the punch through voltage is about 20V and the breakdown voltage is 34V. Slope of -1/2 and -1/3 represents abrupt junction and linearly graded junction respectively.

We use the approximation for one-sided linearly graded junction, since the device has a Au-N-N^+ structure with a slope close to (-1/3) which is shown in Figure C.3.4.

The following equations give the relation among measurable quantities:

$$C = \left[\frac{q\varepsilon_s{}^2 a}{3(V_{bi} + V)}\right]^{1/3} \quad pf/cm^2 \tag{1}$$

and

$$a = \frac{\varepsilon_s}{qV_B{}^2} \frac{8}{9} E_{mB}{}^3 \tag{2}$$

where C = capacitance per unit area

q = 1.6×10^{-19} coulomb

ε_s = $11.8 \times 8.85 \times 10^{-14}$ Farad

V_{bi} = built-in potential

V = reverse bias voltage

a = impurity gradient in the epitaxial wafer

E_{mb} = maximum electric field at avalanche breakdown

V_B = avalanche breakdown voltage.

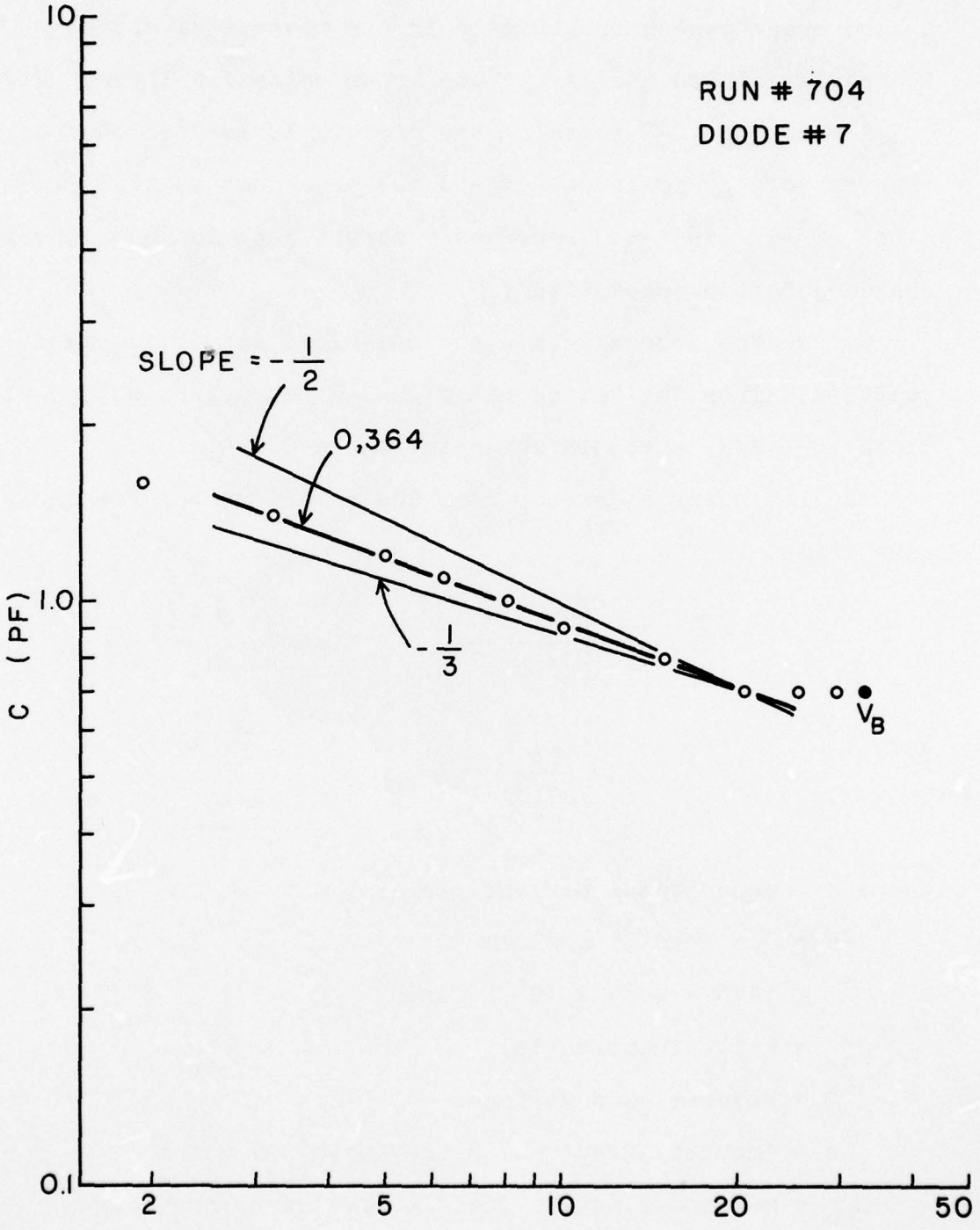


Figure C.3.4 C-V Plots of the Diode.

Figure C.3.5 shows the measured values of $\frac{1}{C^3}$ vs. V. from which the impurity gradient is obtained. Using equation (2) with measured values of $a = 9.85 \times 10^{20}/cm^4$ and $V_B = 34$ volts, the maximum electric field at avalanche breakdown is given to be

$$E_{mB} = 5.77 \times 10^5 \text{ V/cm} \quad .$$

For a symmetrical linearly-graded junction with the same doping gradient, the maximum electric field at avalanche breakdown is given by[2]

$$E_{mB} = 4 \times 10^5 \text{ V/cm}$$

which can be expected to be lower than the value for the one-sided linearly graded junction.

Good quality Si Schottky barrier diodes were fabricated from NN^+ epitaxial wafer grown by sublimation in high vacuum system.

PLANS FOR THE NEXT INTERVAL

Si epitaxial growth of NN^+ junction by vacuum sublimation will be continued to attain further improvements in the quality.

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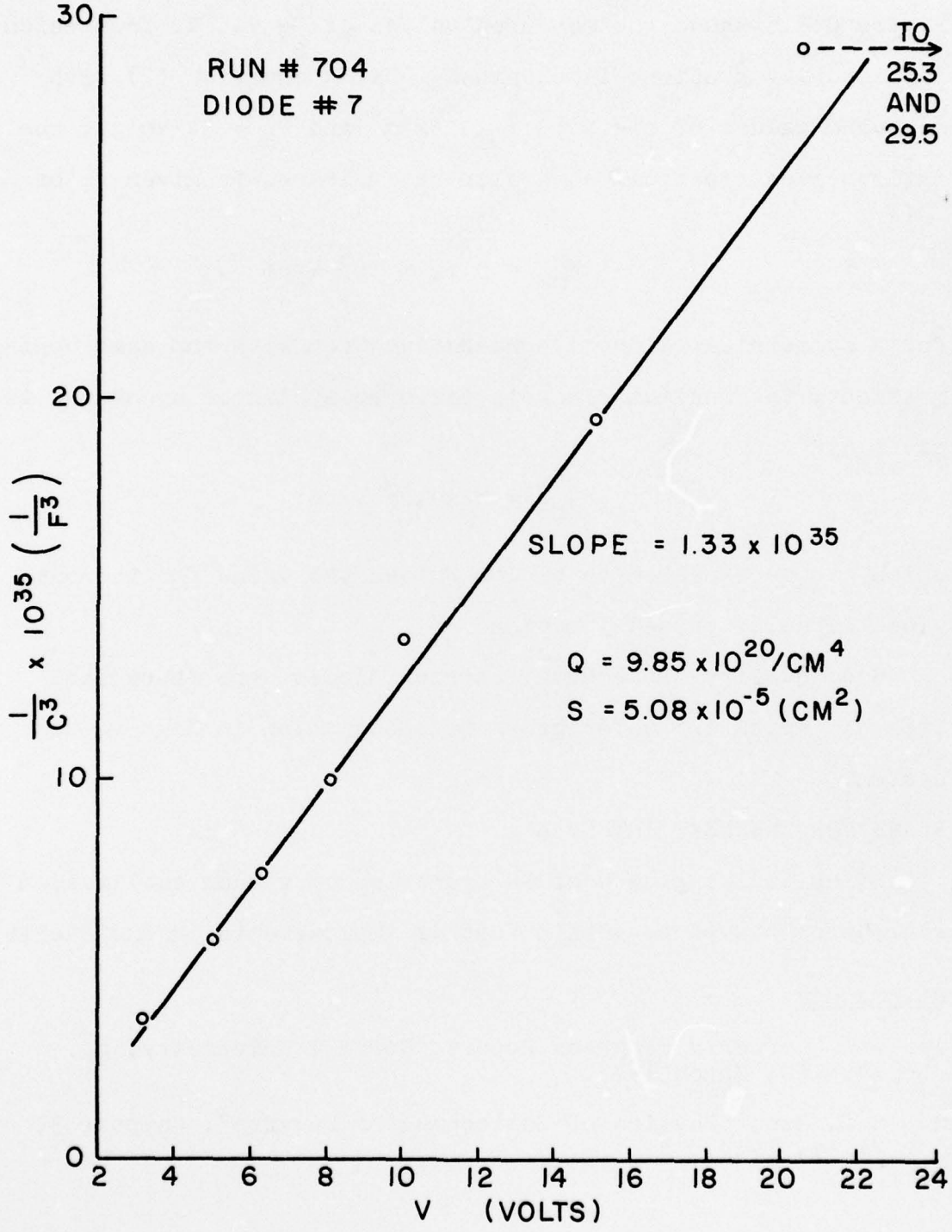


Figure C.3.5 $\frac{1}{C^3}$ Versus V.