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DEVELOPMENT OF AN INTEGRATED MODULE REGULATED VOLTAGE SUPPLY.(U)
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U.S. ARMY MERADCOM

FORT BELVOIR, VIRGINIA 22060

PREPARED BY

YUCCA INTERNATIONAL INCORPORATED

14415 N. SCOTTSDALE ROAD

SUITE 700

SCOTTSDALE, ARIZONA 85260

S/N 392 729

TABLE OF CONTENTS

1.0 INTRODUCTION

The principal performance requirements for solid state power conditioners are generally derived from inherent performance capabilities of mobile electric power engine-generator sets. They are embodied in MIL STD 1332 and in specifications for uninterruptable power supplies. In these specifications the criteria for frequency stability was originally linked to engine speed control assuming a directly coupled generator. Frequency stability for solid state power conditioners can easily be upgraded without significant design penalty. However, an equipment operating mode at high voltage and a short term current overload capacity of 200%, increases cost because of a greater equipment complexity and a higher component kVA requirements.

Many output voltage ratings for solid state power conditioners are not necessarily based on a mandatory performance requirement of mobile power stations, but apply mainly to the inherent means for reconnecting the generator's armature windings either in parallel or in series, and apply also to the manipulation of the magnetic flux of the machine to obtain either a 120-160 V RMS, 208-277 V RMS or a 416-480 V RMS rating. This is also true for the typical 200% over-current capacity over a 10 second period. To maintain this performance level with solid state power conditioners, necessitates an increase of the rating of all solid state switching components including filter networks, circuit breakers, and other power components, to two times the equipment kVA capacity in order to meet high current, low voltage; or low current, high voltage requirements.

The task performed on this contract DAAG 53-76-C-0035 is for an Integrated Module Regulated Voltage Supply which is a specific component of the solid state power conditioner.

This report provides a system overview of the solid state power conditioner, a detail discussion of the integrated module regulated voltage supply, and a section on conclusions and recommendations.

2.0 SYSTEM DESCRIPTION

By virtue of its dc link, the Solid State Power Conditioner (SSPC) is designed to operate from a nonregulated ac power source, nominally 120/308 or 240 V RMS, three phase, 4 wire, with amplitude variations from (-) 15% to (+) 10% and a nominal line frequency of 50 to 60 Hz ± 10 Hz. A three wire dc power supply with its common reference bus enables the IPMI to operate either from three wire utility systems, or from a battery, or from a fuel cell power source as a stand-alone dc to precise ac power inverter. The dc to ac inverter section contains one IPS per phase output when supplying three phase precise ac power, or three IPS in parallel when operating singly or two IPS per phase when supplying 240 V RMS. Independent of the operating mode, each IPS operates as line-to-line commutated inverter and is terminated by a low pass filter (L_o, C_o). The IPS inverter receives its dc power from a preregulated dc bus ± E_1. Pulse Duration Modulation (PDM) is utilized primarily for the generation of a precise sinusoidal ac voltage waveform (V_o) and to a much lesser extent for amplitude regulation. The pre-regulated dc bus (E_1) in turn is obtained from the nonregulated dc power source (V_d) by means of an integrated module regulated voltage supply.

PDM is used to maintain constant output voltages in the event of a temporary overvoltage (E_1) condition. PDM will also be utilized to reduce V_o to zero when subjected to an overcurrent condition. However, for the purpose of this discussion, PDM will be utilized solely for the generation of a sinusoidal output voltage (V_o), with separate amplitude control. In this way the input section as well as output section of the SSPC can be

considered as separate modules with assigned components as shown in Figure 1. Incorporation of the IPS into the SSPC requires observance of a preprogrammed sequence of operations of the peripheral control functions. Abrogration of this sequence can cause a catastrophic malfunction within the IPMI. Figure 2 shows the simplified circuit schematic for the preferred turn-on sequence to obtain nonregulated dc power as utilized in the IPMI. After closure of the manual circuit breaker CK_1, the auxiliary control voltage activates immediately all control functions for the IPS prior to activating contactor CK_2 and thusly the nonregulated dc power bus $\pm V_d$. The auxiliary power supply, schematically shown in Figure 2, presents a good example of the modular construction of the SSPC. Two synchronized and parallel commutated inverters provide redundant ac power to a transformer TR_2 containing two center tapped primary windings, designed for a 400 Hz switching rate. The secondary of TR_2 provides 400 Hz power for two high-speed fans, such as Rotron type Propimax 3B, whereby the total auxiliary power drain of the inverter is typically 160 W. Six identical IPS voltage supplies require a power drain of approximately 70 W, whereby each electrically insulated module provides (± 6 VCD @ constant 1.2 A) for each IPS section. Allowing for a power drain of 40 watt in the microprocessor controller and the pilot lights, and for 30 W switching losses in the primary circuit of TR_2, results in a typical power drain of 300 W which is equally provided by the two buses ($\pm V_d$ @ 150 W).

Nonregulated dc power (V_d), as supplied from a three phase full wave rectifier bridge assembly, ranges in voltage from typically V_d min = 238 VDC to V_d max = 356 VDC when operating either at 15% undervoltage

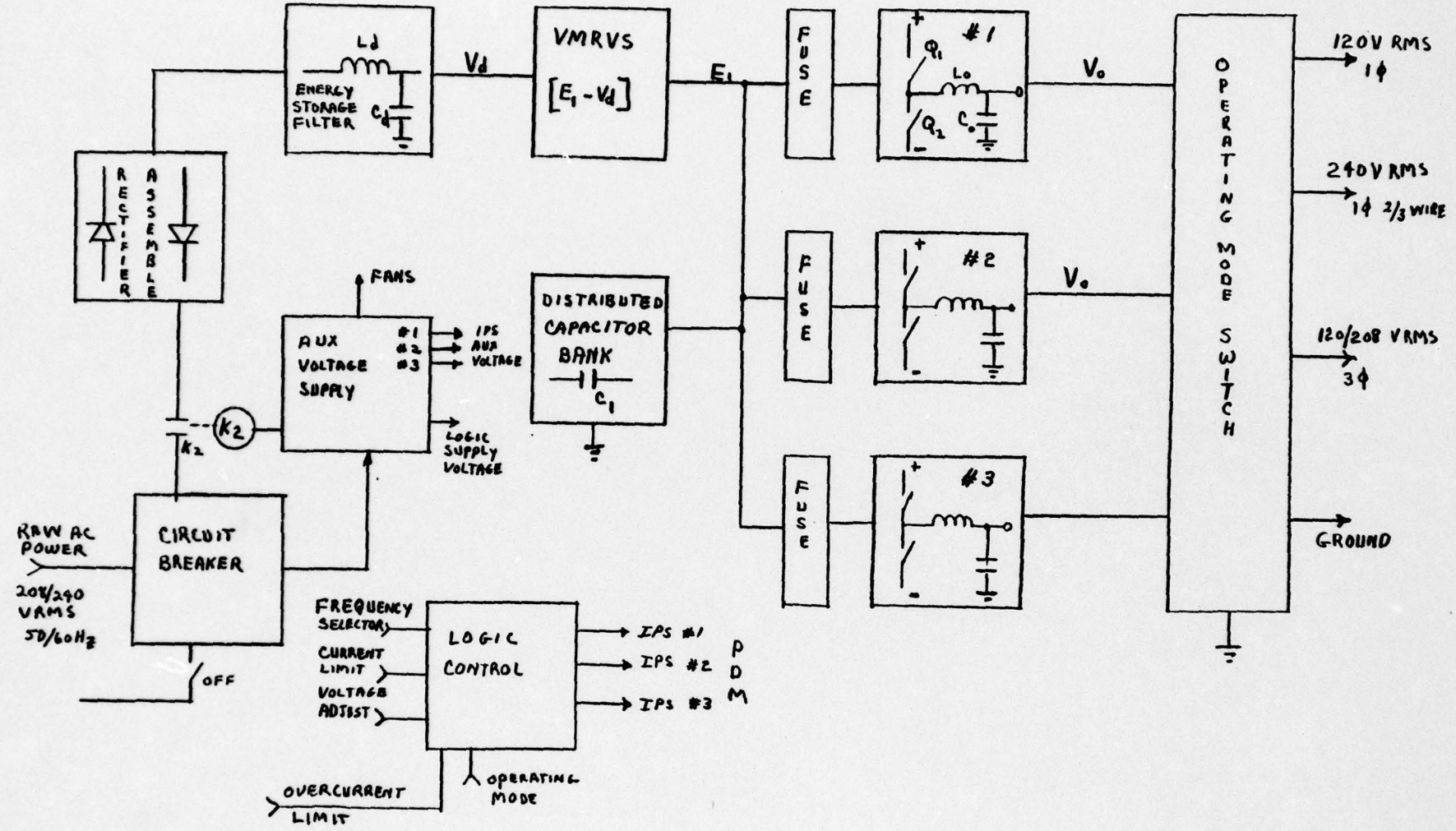


Figure 1: Major Building Blocks of the IPMI

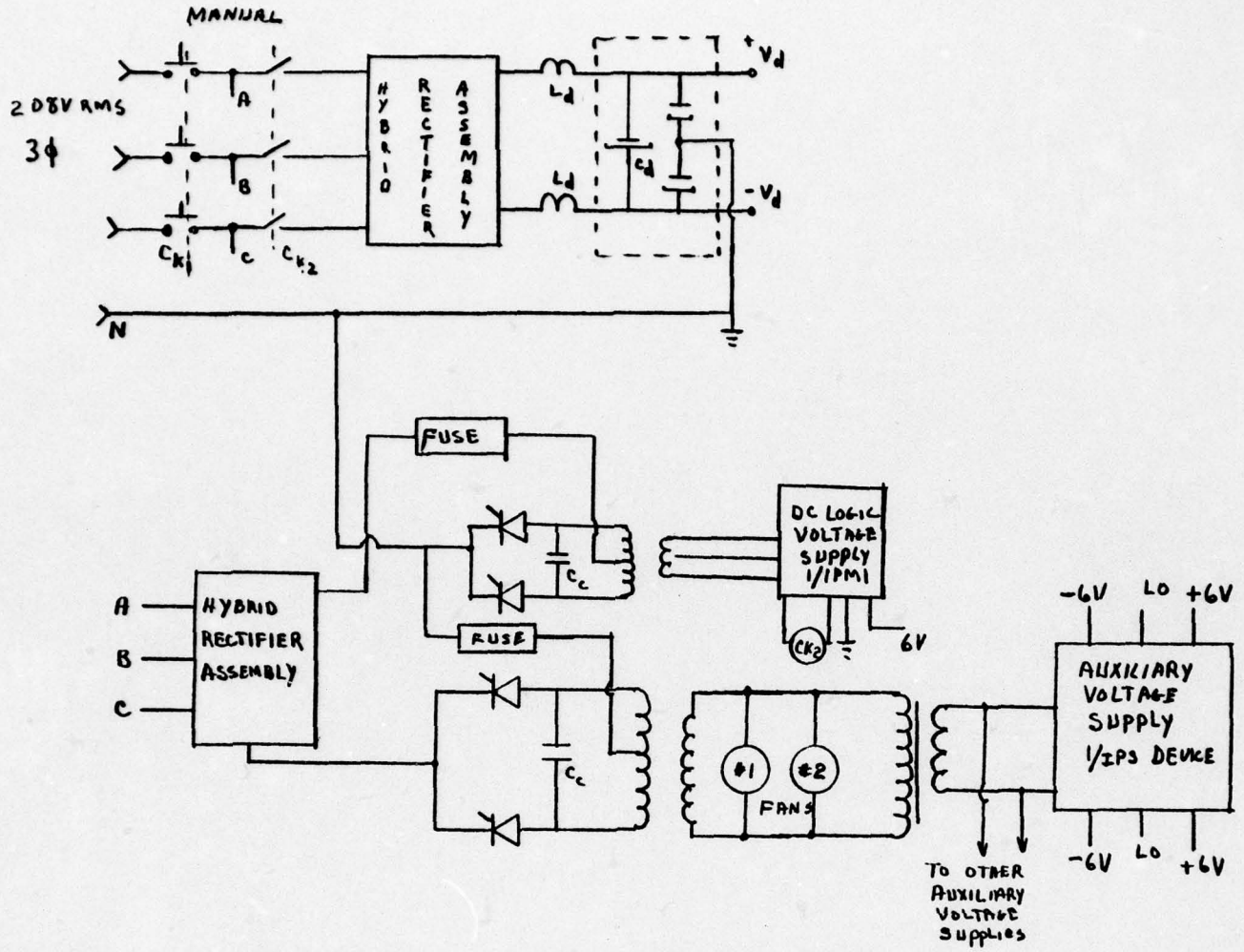


Figure 2: Turn-on Sequence to Obtain Non-regulated Power

from a 208 V RMS utility power source, or at 10% overvoltage from nominally 240 V RMS. Hence undervoltage operation requires a worst case output power switching capacity P_{VBo} of the VBM corresponding to equation (1):

$$P_{VBo} = P_o [(E_1 - V_{dmin})/V_{dmin}\, \eta_o] \quad W \qquad (1)$$

$$P_{VBo} \simeq 7500 \text{ W}$$

where: $\eta_o \simeq 0.97$ - efficiency of IPS inverter module

$P_o = 15$ kW = precise ac output power

The supply of $P_o = 15$ kW single phase precise ac power at $V_o = 120$ V RMS, $I_o = 156$ A RMS (load power factor $PF_o = 0.8$) and a supply frequency $f_o = 50$ Hz, represents the worst case operating mode for the SSPC since it requires maximum filtering of the dc bus in order to suppress ripple current. The regulated dc supply voltage (E_1) for this operating mode is typically

$$E_1 \simeq \pm (\sqrt{2}\, V_o)/\eta_o \simeq \pm 175 \text{ V dc.}$$

The peak current amplitude supplied by either dc bus to the single phase ac inverter mutually phase displaced by π radians, is $|I_1| = 77$ A peak, while its dc current component $I_1' = (I/\pi)I_o = 56$ A dc. The dc current supplied to the capacitor section C_1 is typically

$$I_{c1} = (1500/.97)/350 \simeq 44 \text{ A dc}$$

The average current in the distributed capacitor filter C_1 when discharging is $I_{c1} \simeq 35$ A dc. This represents typically a 50 A RMS amplitude for the entire discharge recharge cycle. Reduction of ripple voltage

and crosstalk between the IPS inverter sections, respectively decoupling the output from the input section, is accomplished by a distributed capacitor filter C_d and C_l, its size is in direct proportion to the ac content of its load as shown in equation (2).

$$C_{d,l} = 1/(2\pi f_o pq Z_l) \quad F \tag{2}$$

$$C_{d,l} < 1400 \quad F$$

$$C_{d,l} = C_d + D_l$$

$$Z_l \triangleq 0.2\ Z_{in} = 0.2\ E_o\ I_o \triangleq 0.96 \text{ ohm}$$

where:

Z_{in} → Equivalent input impedance of the IPMI, single phase operation

(pqf_o) → lowest ripple frequency as function of IPMI operating mode

f_o = *output* frequency (50 Hz)

p = Number of phases

q = Number of simultaneously conducting switches or rectifiers

Correspondingly, the critical operating inductance of the dc filter choke (L_d) is determined by the ripple voltage $(V_{do} - V_d) = 0.0606\ V_d$ (o.0571 V_{do} of the unfiltered and non-regulated power bus and the desired attenutation to 1% across $(C_d + C_l)$, whereby

$$L_d \simeq (2/\omega_d{}^2)(C_d + C_l) \text{ and}$$

$$\omega_d = 2\pi f_d = \text{ripple frequency of nonregulated dc bus } V_d$$

Either nonregulated dc power bus ($\pm V_d$) is filtered with a dc choke $L_d \simeq 20\ \mu H$ when supplied from a 3 phase, 50 Hertz utility power source utilizing a full wave rectifier bridge.

While the 240 V RMS three phase, or two or three wire single phase precise power operating mode requires a preregulated dc power supply E_1 = ± 175 V, it should be noted that the 3 phase operating mode V_o = 208 V RMS, requires only E_1 ≃ (±) 150 V dc. As a consequence the output power switching capacity of the voltage boost module VBM is reduced to P_{VBo} ≃ 4.25 kW. It is preferable for this operating mode to substitute an International Rectifier Company "pace pac" (IR #82-0045, 60 PIV, 100 A) rectifier hybrid assembly, with a complimentary set of similar thyristor hybrid half bridge assemblies as a control element against overvoltage. Either 3 phase operating mode reduces the demand for filtering of the dc bus to approximately C_d = 1650μF.

3.1 THE INTEGRATED MODULE REGULATED VOLTAGE SUPPLY (IMRVS)

The power switching capacity P_{VBo} = 7.5 kW is measured at the output of the IMRVS will remain the same for either the single phase or the three phase inverter inasmuch the precise ac voltage ranges from 120 to 140 or 208 to 240 V RMS, requiring typically a regulated dc bus voltage E_1 = 356 V dc. For this operating condition the maximum error voltage will be $(E_1 - V_d) \approx 112$ V dc, based on a three phase utility supply voltage, nominally 208 V RMS with either 15% undervoltage or 10% overvoltage capability. Thus:

$$0 < (E_1 - V_d) < 112 \text{ V dc maximum}$$

or 56 V dc maximum for a symmetrical regulated dc power bus.

The supply of 240 V/416 V RMS, precise ac power requires dc voltage isolation and, as such, incorporation of one IMRVS for each.

The VBM utilizes thyristors as basic switching elements, is constructed typically from a conventional series-shunt element, naturally commutated half bridge inverter circuit. The series filter capacitors C_1, can be reconnected across the nonregulated power bus ($\pm V_1$) in order to provide an equal burden to either supply. This is shown in Figure 3.

The series-shunt filter is essentially tuned to the fundamental output frequency when supplying maximum output voltage $e_p(\omega_{c1})$ to the primary winding N_1 of transformer TR_1. The voltage rating for the center-tapped secondary windings (N_2) when furnishing power through a bi-phase rectifier is (5):

$$E_s \text{ max} = 11.11\ (1/2(E_1 - V_d) + 1.5 \text{ V}) \text{ V RMS} \qquad (5)$$

$$\approx 64 \text{ V RMS max.}$$

Correspondingly, the sum of all current amplitudes (I_{N2}) in windings (N_2) of the transformer (TR_1) is shown in (6):

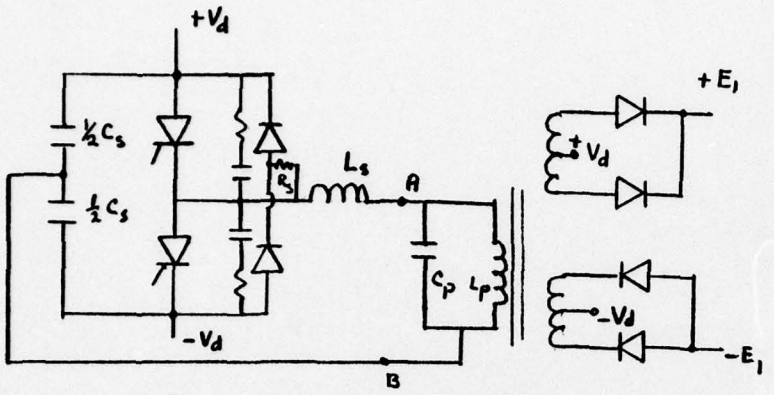


Figure 3A: VBM Circuit Schematic

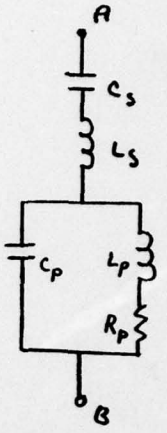


Fig. 3B: Equivalent Circuit

Figure 3: Circuit Schematic of VBM Using Thyristors

$$I_{N2}\ \text{max} = 2\sqrt{2}I_1 \qquad (6)$$

The volt-ampere capacity VA_{N1} of the primary winding N_1 is specified in terms of power rating P_{VB} for the IMRVS when terminated with a bi-phase rectifier (7):

$$VA_{N1} = 1.34\ P_{VB} \qquad (7)$$

where

$$P_{VB} = (E_s \cdot I_s)/\eta_1$$

$$\simeq 0.555\ P_o/\eta_1$$

$\eta_1 \simeq 0.87 \rightarrow \eta_{TR1} \cdot \eta_p$ estimated power transfer efficiency of VBM

$\eta_{TR1} \simeq 0.95 \rightarrow$ estimated efficiency of transformer TR_1

$\eta_p \simeq 0.92 \rightarrow$ estimated power transfer efficiency of series-shunt filter with consideration of switching watt losses in thyristors.

For a typical IPMI power rating of $P_o = 15$ kW the Voltage Booster Module must consequently be rated @ $P_{VB} = 8.75$ kW maximum, or VA_{VB} maximum $\simeq 11.75$ k VA.

This is based on the minimum nonregulated dc supply voltage $\pm V_{dmin} = 119$ V dc. The equivalent load resistor R_p for the shunt filter shown in Figure 3B is obtained from the following power relationship (8):

$$e_{dmax} = \frac{2V_d}{\pi}\ \text{V RMS @}\ \omega_{c1}\ \text{Radians/s}$$

$$e_{pmax} \simeq e_{dmax} \cdot Z_1 \simeq e_{dmax}\ @\ \omega_{c1} = \omega_{ps}\ \text{(assuming a lossiess series filter)}$$

where:

$$\omega_{ps} = (\omega_{cp} \cdot \omega_{cs})^2$$

$\omega_{cp} = 2\pi f_{clp}$ = natural resonance frequency of the shunt filter in Hz.

$\omega_{cs} = 2\pi f_{cls}$ = natural resonance frequency of the series filter in Hz.

Z_1 = transfer function of the series shunt filter as described in Appendix 1.

$$i_p \simeq \frac{VA_{VB}}{e_d} \triangleq \left(\frac{P_{VB}}{R_p}\right)^{1/2} \quad \text{A RMS}$$

$$R_p = \left(\frac{2V_d}{\pi}\right)^2 \cdot \frac{P_{VB}}{VA_{VB}^2} \quad \text{ohm} \qquad (8)$$

Similarly, the inductance L_p is:

$$L_p = \left(\frac{2V_d^2}{\pi}\right) \frac{(VA_{VB}^2 - P_{VB}^2)^{1/2}}{\omega_{CP}\, VA_{VB}^2} \quad \text{ohm-s}$$

Since the magnitude of $VA_{VB} = \sqrt{2}P_{VB}$ when the shunt filter is critically damped at a frequency ω_{cp} Radian/s, the inductance L_p is calculated from (9):

$$L_p \simeq \frac{2V_d^2}{\pi^2\, \omega_{cp}\, P_{VB}} \quad \text{ohm-s} \qquad (9)$$

At this point VA_{VB}, R_p, and e_d are specified and fixed quantities for maximum power output. It follows that the maximum operating frequency ω_{c1} for the shunt filter is solely determined by the winding configuration of transformer TR_1 and its apparent inductance L_p in primary winding N_1.

Utilizing Ferrite cores and multiple transformer windings which are connected in parallel, the minimum inductance which can be attained by reasonable means is:

$$L_p = 2.6\ \mu H\ @$$

$$\omega_{cp} = 20\ kHz$$

for:

$$V_d = 119\ V_{dc}$$

Substituting equations (8) and (9) into (I-9) shown in Appendix 1, yields equation (10):

$$C_p = \frac{2}{3} \cdot \frac{P_{VB}\ \pi^2}{V_d^2\ \omega_{cp}}\ F \qquad (10A)$$

$$C_p = 2C_s \qquad (10B)$$

$$L_s = 4.5\ L_p \qquad (10C)$$

Capacitor $C_p \approx 32\ \mu F$ for above operating conditions.

It is noteworthy at this point that the circuit is unconditionally stable and commutates both thyristors TH_1 and TH_2 under all load conditions, if

$$0 < \omega_{c1} < \omega_{ps}$$

When neglecting its leakage resistance, a short circuit in transformer TR_1 will cause a short circuit current I_{spk} which amplitude is (11):

$$I_{spk} = \frac{2\sqrt{2}}{\pi} V_d\ (C_s/L_s)^{1/2}\ \text{A peak}$$

$$I_{spk} = \frac{2\sqrt{2}}{3\pi} F_d\ (C_p/L_p)^{1/2}\ \text{A peak} \qquad (11)$$

$$\approx 0.3\ V_d\ (C_p/L_p)^{1/2}\ \text{A peak}$$

The circuit is underdamped for all but one load condition, at which the resonance circuit is never more than critically damped. Hence, after turn-on, commencing with the second half cycle of operation, capacitors C_s and C_p resonantly charge to a voltage level ‡ $2V_d$ if not clamped by the appropriate inverse by-pass diode D_1 or D_2 to the dc bus. In place of separate diodes, thyristors TH_1 and TH_2, can be chosen with a low reverse blocking voltage, approximately 50 V.

The input voltage $e_d\ (\omega_{c1})$ to the series-shunt filter is a continuous variable and a function of the active conduction period for each half cycle, where:

$$0 < e_d\ (\omega_{c1}) < \frac{2V_d}{\pi} \quad \text{V RMS}$$

and where the conduction period for each thyristor shown in Figure 9, is (12)

$$\phi = \frac{\pi}{\omega_{ps}} \quad \text{s} \qquad (12)$$

The amplitude of the input voltage to the filter $e_d\ (\omega_{c1})$ is similar as shown in equation (5), except that ω_{c1} ‡ constant. It varies typically 20% commensurately with the damping decrement β.

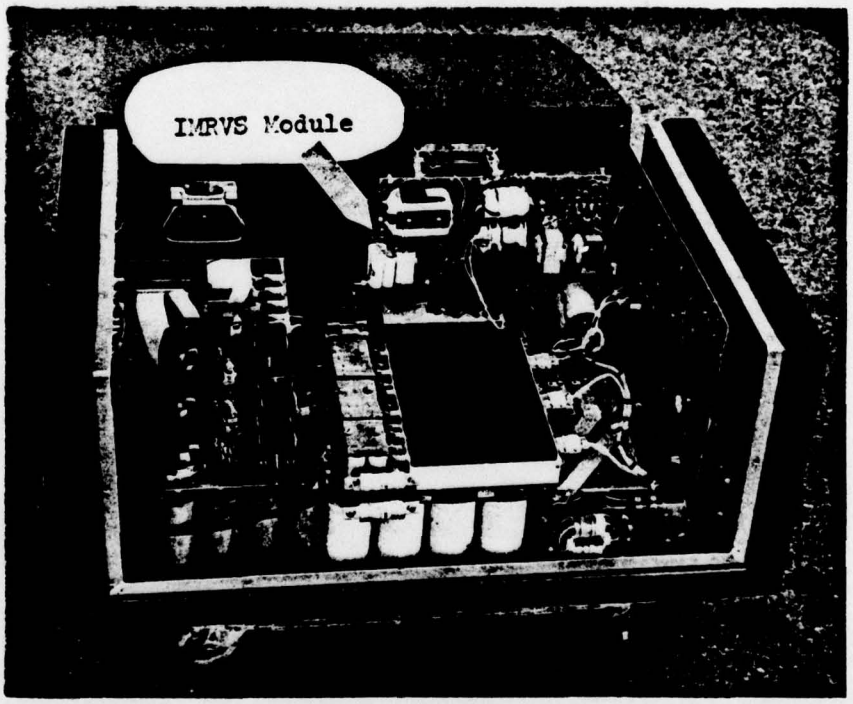
The transformer voltage $e_p\ (\omega_{c1})$ is (13)

$$e_p\ (\omega_{c1}) = Z_t\ e_d\ (\omega_{c1}) \quad \text{V} \qquad (13)$$

The approximate location of the poles for the fourth order transfer function Z_t is obtained by factoring the demoninator as shown in Appendix 1, yielding (14):

$$Z_t = \frac{s_1(sL_p + R_p)/L_sL_pC_p}{\left[s_1^2 + \frac{1}{L_sD_s}\ \frac{(C_s + C_p)}{C_p}\right]\left[s_1^2 + s_1\ \frac{R_p}{L_p} + \frac{1}{L_pC_p}\ \frac{C_p}{(C_s + C_p)}\right]} \qquad (14)$$

Prior to the availability of components suitable for the construction of modular building blocks, thyristors were considered the preferred switching devices when commutated by a series-shunt filter. However, the recent availability of the automotive ignition transistor makes it possible to assemble low cost, multiple chip transistor switch arrays similarly as used in the IPS. This has made it possible to construct high density and lightweight IMRVS previously not considered practical utilizing either conventional transistor power switches, or thyristors. A picture of the IMRVS is shown below.



4.0 CONCLUSIONS AND RECOMMENDATIONS

The primary emphasis of this effort was to develop an Integrated Module Regulated Voltage Supply (IMRVS) using high frequency SCR and resonant tuned circuits. This type of circuit will operate satisfactory over a limited frequency range. However, it was found that to operate over a ten to one frequency range, as required for regulated voltage boost, was very difficult. The difficulties encountered included:

- other resonant modes
- protection against shorted output at some resonants
- reliable triggering of the SCR at the frequencies

Because of these difficulties and the advent of high voltage high current transistor and transistor modules, it is recommended that the next generation IMRVS use PDM and transistor modules to achieve the desired voltage boost. An analysis of this new design is provided in Appendix II.

5.1 APPENDIX I

Series-Shunt Filter

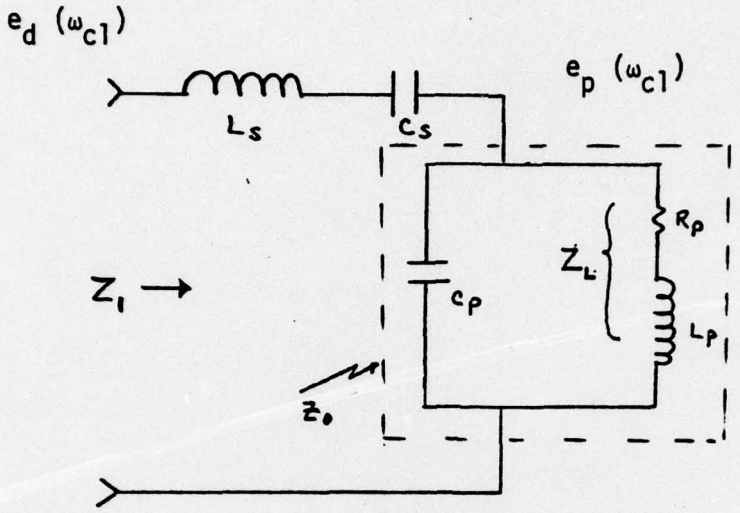


Figure 1-I: Series=Shunt Filter

The output voltage $e_p\ (\omega_{c1})$ for the series-shunt filter shown in Figure 1-I is obtained from the transfer function (I-1):

$$Z_t = Z_o/Z_{in} \qquad \text{(I-1)}$$

$$Z_t \equiv \frac{e_p\ (\omega_{c1})}{e_d\ (\omega_{c1})} = \frac{1 \cdot Z_o}{1Z_{in}}$$

and

$$e_p\ (\omega_{c1}) = e_d \cdot Z_1$$

The output function Z_o describes the impedance of the shunt-filter (I-2):

$$Z_o = \frac{R_p + sL_p}{s^2 L_p C_p + sC_p R_p + 1} \quad \text{ohm} \qquad \text{(I-2)}$$

poles: $s_{11-12} = -R_p/2L_p \pm j\,[1/L_pD_p - R_p{}^2/4L_p{}^2]^{1/2}$

Correspondingly the input function Z_{in} yields (I-3):

$$Z_{in} = \frac{s^2 L_s C_s + 1}{sC_s}$$

$$Z_{in} = \frac{(s^2 L_s C_s + 1)(s^2 L_p C_p + sD_p R_p + 1) + sL_p + R_p)\, sC_s}{C_s\,[s^2 L_p R_p + sC_p R_p + 1]} \quad \text{ohm} \qquad \text{(I-3)}$$

poles: $s_{13} = 0_1 s_{14\text{-}15} = s_{11} \cdot s_{12}/C_s$

whereby: the series filter L_s - C_s is assumed to be lossless, R_s R_p

R_s equivalent resistance in series with filter L_s and C_s

The transfer function for the series-shunt filter is (I-4):

$$Z_1 = \frac{1}{1 + \dfrac{(s^2 L_s C_s + 1)\,(s^2 L_p C_p + sC_p R_p + 1)}{sC_s\,(sL_p + R_p)}} \qquad \text{(I-4)}$$

The demonimator contains the biquadratic equation (I-5):

$$s^4 L_s L_p C_s C_p + s^3\,(L_s C_s D_p R_p) + s^2\,(L_s C_s + L_p C_p + L_p C_s) + sR_p(C_s + C_p) + 1 = 0 \qquad \text{(I-5)}$$

The general expression for (I-5) is shown in (I-6):

$$s^4 + s^3 \frac{a_1}{a_o} + s^2 \frac{a_2}{a_o} + s\frac{a_3}{a_o} + \frac{a_4}{a_o} = 0 \qquad \text{(I-6)}$$

where:

$a_o = L_s L_p C_s C_p$

$a_1 = L_s C_s C_p R_p$

$$a_2 = L_s C_s + L_p C_p + L_p C_s$$

$$a_3 = R_p (D_s + C_p)$$

$$a_4 = 1$$

The series filter $L_s - C_s$, Figure 9, is assumed lossless. For this special case, equation (I-6) can be factored into its quadratic component (I-7) and solved for its coefficients in accordance to (I-8):

$$(s^2 + K_1)(s^2 + sK_2 + K_3) = 0 \qquad \text{(I-7)}$$

$$s^4 + s^3 K_2 + s^2 (K_1 + K_3) + sK_1K_2 + K_1K_3 = 0 \qquad \text{(I-8)}$$

Solving for the coefficients:

$$K_2 = a_1/a_o = R_p/L_p$$

$$K_1 + K_3 = a_2/a_o \rightarrow K_{3(1)} = 1/L_pC_p$$

$$K_1K_2 = a_3/a_o \rightarrow K_1 = \frac{1}{L_sC_s} \frac{C_s + C_p}{C_p}$$

$$K_1K_3 = a_4/a_o \rightarrow K_{3(2)} = \frac{1}{L_pC_p} \frac{C_p}{C_s + C_p}$$

Since $K_{3(1)} = K_{3(2)}$ it follows that $C_p (C_s + C_p) \rightarrow 1$ and $C_p > C_s$

Substitution of the coefficients K_1, K_2 and K_3 into (I-7) yields (I-9):

$$\left[s^2 + \frac{1}{L_sC_s} \frac{C_s + C_p}{C_p}\right] \left[s^2 + s \frac{R_p}{L_p} + \frac{1}{L_pC_p} \frac{C_p}{C_s + C_p}\right] \qquad \text{(I-9)}$$

The poles of the transfer function shown in (I-4) are (I-10A) and (I-10B):

$s_{1.2} = j\omega_{cl} = 2\pi f$ Radians/s, whereby f_{cl} = control frequency in Hz for the VBM

$$\omega_{cs} = \pm j \, L_s C_s \left[\frac{C_s + C_p}{C_p}\right]^{1/2} \quad \text{Radians/s} \qquad \text{(I-10A)}$$

$$\omega_{cp} = -\frac{R_p}{2L_p} \pm j \left[\frac{1}{L_p C_p}\left(\frac{C_p}{C_s + C_p}\right) - \left(\frac{R_p}{2L_p}\right)^2\right]^{1/2} \qquad \text{(I-10B)}$$

Since $C_p/(C_s + C_p) \Delta 1$ it follows that $C_p = K_4 C_s$, whereby K_4 is an integer multiplier. Under these conditions (I-10A) and (I10B) can be solved to yield the inductance L_s for the non-damped case (I-11):

$$\omega_{cs} = \omega_{cp} \qquad C_p = K_4 C_s$$

$$\frac{K_4 C_s}{(K_4 + 1)\, C_s} \cdot \frac{}{L_p K_4 C_s} = \frac{1}{L_s C_s} \cdot \frac{(K_4 + 1) C_s}{K_4 C_s}$$

$K_4 = 2,3,4 \ldots . n$

For $K_4 = 2$:

$$L_s = \frac{(K_4 + 1)^2}{K_4} L_p \qquad \text{(I-12)}$$

$L_s = 4.5 L_p$

$C_p = 2C_s$

When critically damped, both the reactive and real parts of equation (I-10B) are equal when:

$\alpha = \beta$ for $\omega_{clp} = \alpha + \beta$

whereby $\alpha = R_p/2L_p$ Decrement Factor

$$\beta = \left[\frac{1}{L_p C_p} \cdot (C_s + C_p) - \left(\frac{R_p}{2L_p} \right)^2 \right]^{1/2} \quad \text{Radians/s}$$

Determination of capacitor C_p at $\alpha^2 - \beta^2$ at $(C_s + C_p)/C_p = 1.5$, yields (I-13):

$$C_p = \frac{4}{3} \cdot \frac{L_p}{3R_p^2} \quad F \qquad \text{(I-13)}$$

5.1 APPENDIX II

Transistorized IMRVS

The IMRVS using transistors is schematically shown in Figure II-1. The circuit consists of a half bridge inverter which is

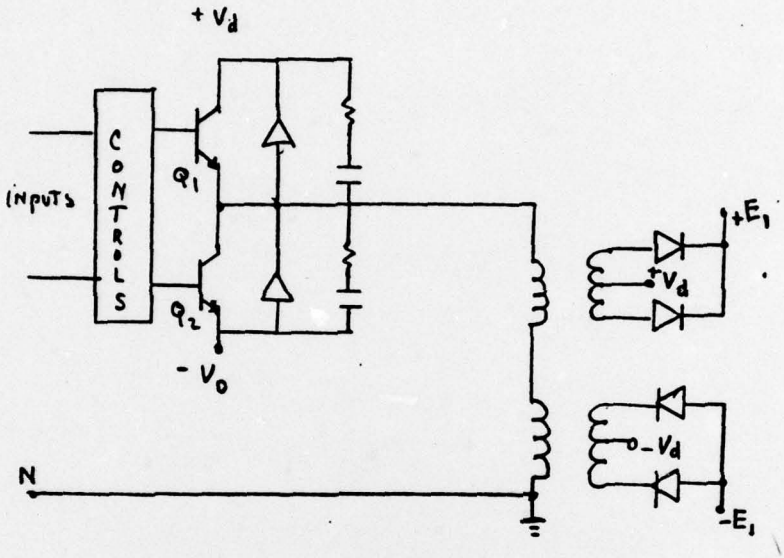


Figure II-1. Circuit Schematic of IMRVS Using Transistors

commutated between ($\pm$) V_d. The volt-ampere capacity VA_p and VA_s of the primary and secondary transformer winding is specified in Equation (II-1) for a power switching capacity $P_{VBol,2} = 1/2\ P_{VBo} = 3750$ W as supplied to either dc bus by a bi-phase rectifier:

$$VA_{s1,2} = D_s\ 2\ I_s \simeq 5450\ VA \qquad \text{(II-1A)}$$

where: $I_1 = 7500/112 \simeq 67$ Adc

$E_s = [1/2(E_1 - V_d) + 1.5\ V] = 57.5$ V RMS

$I_s \simeq I_1/\sqrt{2} \simeq 47.5$ A RMS

and

$$VA_p = 2\ VA_s/\eta_1 \simeq 12528\ VA \qquad \text{(II-1B)}$$

$E_{p1} \simeq (2V_d - 3) \simeq 235$ V RMS = ac output voltage

$I_p = 59$ ARMS - current amplitude in primary winding (N_1) of transformer TR_1

$\eta_1 = 0.87$ = power conversion efficiency of IMRVS

This requires typically a transistor average current switching capacity of $I_c \simeq 42\ A_1$ whereby $V_{CEosus} \simeq 400$ V. Each transistor is commutated at typically $I_c < 85$ A peak.

The control of the output power envelope of the transistor VBM is obtained through pulse duration modulation. When utilizing constant frequency and a variable pulse duration control method, the variable conduction interval of each transistor is (II-2A)

$$0 < \phi < \frac{\pi}{c1max}\ s \qquad \text{(II-2A)}$$

$$\omega_{c1} = \omega_{c1max} = \text{constant}$$

where: $\omega_{c1} = 2\pi f_1$ Radians/s

f_1 = switching frequency in Hz.

This is shown in Figure 8.

Similarly, a variable frequency, constant pulse width operating mode yields a conduction interval (II-2B)

$$\phi = \frac{\pi}{c1max}\ s \qquad \text{(II-2B)}$$

whereby: $0 < \omega_{c1}\ \ \omega_{c1max}$

This operating mode reduces the switching watt losses in the transistors, although it generally yields lower power transfer efficiency when operating at low duty cycle. Independently of the operating mode, the output voltage is the controlled variable, and is:

$$0 < e_d\ (\omega_{c1}) < \frac{2V_d}{\pi}\ \text{VRMS}$$

Fourier analysis yields the ac output voltage $e_d\ (\omega_{c1})$ as a function of conduction duty cycle, whereby the conduction period ϕ is measured in seconds (3):

$$e_d\ (\omega_{c1}) = \frac{V_d}{\pi} \sum_{n=1}^{n=\infty} \left[\left(\int_0^{\phi} \cos n\omega_{c1}\ td\ (\omega_{c1}\ t) \right) \cos n\omega_{c1}\ t + \left(\int_0^{\phi} \sin n\omega_{c1}\ td\ (\omega_{c1}\ t) \right) \sin n\omega_{c1}\ t \right] V_p$$

where: $\phi = \frac{\pi}{\omega_{c1}}$ (s); $V_d : 0 < t < \phi$; $\quad 0 : \phi < t < \pi$

$$-V_d : \pi < t < \phi; \quad 0 : \phi < t < 2\pi$$

$$e_d\ (\omega_{c1}) = \frac{V_d}{\pi} \sum_{n=1}^{n=\infty} \frac{1}{n} \left(\sin n\omega_{c1}\ \phi \cos n\omega_{c1}\ t + (1 - \cos n\omega_{c1}\phi) \right.$$

$$\left. \sin n\omega_{c1}\ t \right) \quad V_p$$

$$\frac{2V_d}{\pi} \sum_{n=1}^{n=\infty} \left(\frac{1}{n} \sin\left[\frac{n\omega_{c1}\,\phi}{2}\right] \cos n\omega_{c1}\left[t - \frac{\phi}{2}\right]\right) \quad V_p$$

$$= \frac{2V_d}{\pi} \left[\sum_{n=1}^{n=\infty} \left(\frac{1}{n} \sin\left[\frac{n\omega_{c1}\,\phi}{2}\right] \cos n\omega_{c1}\left[t - \frac{\phi}{2}\right]\right)^2\right]^{1/2} \quad \text{VRMS} \quad (3)$$

It should be noted that the impact of non-linear networks to limit di/dt and dv/dt slopes within each transistor switch is neglected, as well as its forward voltage drop during conduction.