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ADVANCED MONITORING TECHNIQUES FOR DIGITAL COMMUNICATION SYSTEM--ETC(U)
JAN 77 J L HAMMOND, D J SCHAEFER, S S LIU F30602-75-C-0118
RADC-TR-77-29 NL

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RADC-TR-77-29
Phase Report
January 1977

ADVANCED MONITORING TECHNIQUES FOR DIGITAL COMMUNICATION SYSTEMS

Georgia Institute of Technology

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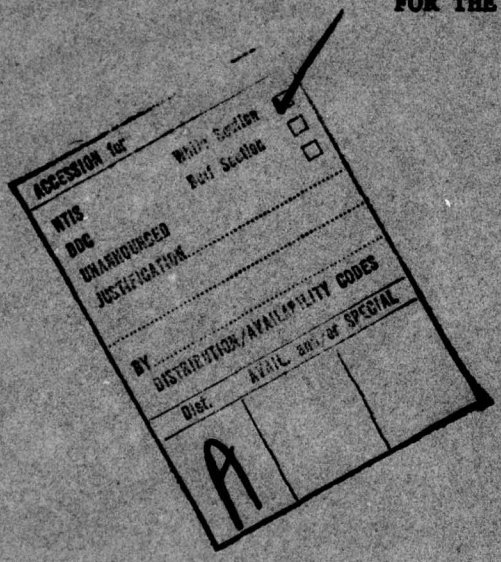
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3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle): ADVANCED MONITORING TECHNIQUES FOR DIGITAL COMMUNICATION SYSTEMS.	5. TYPE OF REPORT & PERIOD COVERED: Phase Report.
	6. PERFORMING ORG. REPORT NUMBER: N/A
7. AUTHOR(s): J. L. Hammond, D. J. Schaefer, S. S. Liu, B. J. Leon	8. CONTRACT OR GRANT NUMBER(s): F30602-75-C-0118
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Georgia Institute of Technology, School of Electrical Engineering, Atlanta GA 30332	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 95670018
11. CONTROLLING OFFICE NAME AND ADDRESS: Rome Air Development Center (RBC), Griffiss AFB NY 13441	12. REPORT DATE: January 1977
	13. NUMBER OF PAGES: 171 (12) 183 p.
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Same	15. SECURITY CLASS. (of this report): UNCLASSIFIED
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Same

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18. SUPPLEMENTARY NOTES

RADC Project Engineer: Jacob Scherer (RBC)

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Digital Communications
Electromagnetic Compatibility

408 631

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report considers the problem of monitoring digital communication systems. Possible monitoring techniques are reviewed and a group of different methods, which will completely define the system state, is chosen. A new format violation type indication is suggested and analyzed for the seven-level partial response/FM system.

Four-level FM, seven-level partial response/FM and quadrature partial response

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types of modulation are reviewed and a group of eleven generic faults are chosen as representative malfunctions for communication links using such modulation methods. The response of each of six monitors to each of the generic faults is determined theoretically.

Simulation studies are conducted for a seven-level partial response/FM system using three monitors and a selection of typical faults. The simulation results are found to be consistent with the theoretical results.

A method for processing error rate monitor outputs to obtain a fault alarm is worked out and the results are verified with simulation studies.

Recommendations are given for a group of five monitors for a seven-level partial response/FM system. It is demonstrated that these monitors will detect all of the group of eleven generic faults and that fault isolation can be accomplished between ten of the eleven faults.

Fault isolation cannot be accomplished as well for the four-level FM system because format violation monitors cannot be used. A similar result pertains to the QPR system, although some type of format violation monitor may be possible for this type system. Fault detection can be accomplished for FM and QPR in the same manner as for partial response systems.

ADVANCED MONITORING TECHNIQUES FOR DIGITAL COMMUNICATION SYSTEMS

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A study conducted under the Rome Air Development Center Post Doctoral Program, Contract F30602-75-C-0118, for the Defense Communications Agency.

PREFACE

The work reported herein is a continuation of a study of monitoring methods for digital communication systems conducted by the RADC Post Doctoral Program for the Defense Communications Agency.

The post doctoral program team for this task is under the direction of Professor B. J. Leon of Purdue University. Team members during the period of the present study are Professor J. L. Hammond (directing the work at Georgia Tech), Dr. D. J. Schaefer of Purdue and Mr. S. S. Liu of Georgia Tech. The project director for the Defense Communications Agency is Dr. F. J. Ricci. Mr. I. P. Plotkin, Dr. D. M. Schutzer and Mr. D. R. Smith of the Defense Communications Agency have contributed through frequent discussions of the subject task.

The hybrid computer simulation study, reported in Section II of the report, was carried out by Dr. Schaefer at Purdue University. The theoretical part of the study was done at Georgia Tech.

TABLE OF CONTENTS

	Page
Abstract	v
Forword	vii
List of Figures	xi
List of Tables	xiii
Introduction	1
Section I, Theoretical Studies	5
1.0 Background	5
1.1 Major Link Faults	9
1.1.1 Information Subsystems	9
1.1.2 Bit Synchronization Subsystem	10
1.1.3 Frame Synchronization Subsystem	10
1.2 General Types of Link Monitors	12
1.2.1 Received Signal Level Monitors	12
1.2.2 Eye Pattern Monitors	13
1.2.3 Out-of-Band Noise Monitors	13
1.2.4 Format Violation Monitors	14
1.2.5 Pseudo-Errors Monitors	15
1.2.6 Pseudo-Error for Trend Indications	16
1.3 Data Processing Techniques for Error Rate Monitors	17
1.4 Format Violation Monitors for Links using Partial Response Signaling	23
1.4.1 Three-level Partial Response	23
1.4.2 Seven-level Partial Response	26
1.5 Specific Systems	31
1.5.1 Four-Level FM	31
1.5.2 7-Level Partial Response	33
1.5.3 Quadrature Partial Response Systems (QPR)	33
1.6 Choice of Monitors and Methods for Fault Isolation	42
1.6.1 Preliminary Choice of Monitors	42
1.6.2 Analysis of Monitor Responses	43
1.6.3 Fault Isolation	51

	Page
Section II, Hybrid Simulation of Digital Systems Over Analog Links	55
2.0 Introduction	55
2.1 The 3-Level Partial Response System	56
2.1.1 Random Number Generator	56
2.1.2 Partial Response Filters	58
2.1.3 FM Modulator	59
2.1.4 Channel Simulation	61
2.1.5 IF Filter	61
2.1.6 Automatic Gain Control Stage	61
2.2 7-Level Partial Response Simulation	65
2.2.1 Input Timing and Binary to 4-Level Converter	69
2.2.2 Data Precoder	74
2.2.3 Link Simulation	76
2.2.4 7-Level to 4-Level Analog Converter	79
2.2.5 4-Level Analog to Digital Converter	79
2.2.6 4-Level Digital to Binary Decoder	84
2.2.7 Multilevel Timing Recovery PLL	84
2.2.8 System Performance Monitors	90
2.2.9 Input Data Delay Line	100
2.2.10 Test Circuitry	100
2.2.11 Data Comparator	102
2.2.12 Simulation Software	104
2.3 Four-Level FM Simulation	109
2.3.1 Frequency Discriminator	111
2.3.2 Frequency Discriminator L. P. Filter	114
Section III, Results of Simulation Studies, Conclusions and Recommendations	116
3.1 Description of Simulation Studies	116
3.2 Results of Simulation Studies	119
3.3 Conclusions	128
3.4 Recommendations	134
References	136
Appendix A, Monitor Responses for Simulated No Fault Conditions	139
Appendix B, Monitor Responses for Simulated Fault Conditions	141
Appendix C, Simulation Set Up Procedures	151
Appendix D, Software Listing for FDATA2	160

LIST OF FIGURES

		Page
Figure 1	Typical User-to-User Link	6
Figure 2	Typical Level 3 Radio Configuration	7
Figure 3	A Multiplexor/Demultiplexor and Microwave Radio using Bit Stuffing	8
Figure 4	Three-level Partial Response Encoder	24
Figure 5	An Error Monitor for 7-Level, Class 1 Partial Response Systems	28
Figure 6	Generic Block Diagram for a 4-Level FM System	32
Figure 7	A General Partial Response/FM System Diagram	34
Figure 8	Generation of a Modified Duobinary Signal and its Resulting Spectrum	35
Figure 9	Typical Duobinary Time Waveforms	37
Figure 10	Spectra of Modified Duobinary Waveforms	39
Figure 11	Phase Diagram of the Signal Set for QPR Modulation	40
Figure 12	A Possible Implementation of a QPR System	41
Figure 13	A Typical Multilevel Signal with Information Concerning Monitors and Faults	48
Figure 14	Block Diagram of a 3-Level Partial Response System	57
Figure 15	3-Level Partial Response Input D/A, Partial Response Filter and Link Simulations	60
Figure 16	IF Filter and AGC Simulations	62
Figure 17	Phase Lock Loop Demodulator and Partial Response Filter	64
Figure 18	Performance Monitor, Timing Recovery, and Data Decoder for 3-Level Partial Response System	66
Figure 19	Bit Error Indications and Timing Pseudo Error Monitor for 3-Level Partial Response System	67
Figure 20	Jitter Monitor and Error Comparator for 3-Level Partial Response System	68
Figure 21	Block Diagram of 7-Level Partial Response System	70
Figure 22	Input Timing Generator and Binary to 4-Level Encoder	72
Figure 23	Timing and Binary to 4-Level Converter Waveforms	73
Figure 24	Input Data Precoder for 7-Level Partial Response System	75
Figure 25	Data Precoder 2 Bit Processor	77
Figure 26	Level Adjustor Network	78
Figure 27	7-Level to 4-Level Analog Converter for 7-Level Partial Response System	81

		Page
Figure 28	7-Level Analog to Digital Converter	82
Figure 29	4-Level Analog to Digital Converter	85
Figure 30	4-Level Digital to Binary Decoder	86
Figure 31	4-Level to Binary Decoder Logic Levels	88
Figure 32	Multilevel Timing Recovery Circuit	89
Figure 33	Pseudo-Error Monitor	91
Figure 34	Block Diagram of Format Violation Monitor for 7-Level Partial Response System	93
Figure 35	Format Monitor Waveforms	94
Figure 36	7-Level Sample and Hold Network for Format Violation Monitor	95
Figure 37	Limiter and Bit Delay for Format Violation Monitor	97
Figure 38	Format Level Detectors for Format Violation Monitor	98
Figure 39	Alternate Realization of Format Violation Monitor	99
Figure 40	Input Data Delay Line	101
Figure 41	Peak Detector and Switch	101
Figure 42	Dual Trace Scope Generator	101
Figure 43	Data Comparator	103
Figure 44	7-Level Partial Response Waveforms for Test Signal Input	105
Figure 45	7-Level Partial Response Performance Monitor Outputs	107
Figure 47	Block Diagram of 4-Level FM System	110
Figure 48	Discriminator Characteristic	112
Figure 49	Frequency Discriminator	113
Figure 50	Frequency Discriminator Low Pass Filter	115
Figure 51	Pseudo-Error Monitor Performance for Varying Error Rates	120
Figure 52	Pseudo-Error Monitor Rate for Varying Band Spacing	121
Figure 52	Typical Transient Monitor Outputs	123

LIST OF TABLES

		Page
Table 1	Indication of Sensitivity of Various Monitors to Various Faults	18
Table 2	Values of K and T	22
Table 3	Possible Values of $\overline{B_i'}$	30
Table 4	Monitor Responses to Faults in the Signal Subsystem	44
Table 5	Monitor Responses to Faults in the Frame Synchronization Subsystem	45
Table 6	Monitor Responses to Faults in the Bit Synchronization Subsystem	46
Table 7	Fault Profiles for Eleven Faults with Six Monitors	52
Table 8	Faults Whose Profiles Differ by One Monitor Reading	53
Table 9	Encoding Format	71
Table 10	A_K Binary Coding	74
Table 11	7-Level to 4-Level Analog Converter Internal States	80
Table 12	Description of Simulated Faults	118
Table 13	Monitor Responses for No Fault Conditions	124
Table 14	Summary of Average Number of Frames for Threshold Exceedances for Various Faults	125
Table 15	Fault Profiles from Simulation Study	126
Table 16	Number of Frames for Fault Detection and Isolation for Simulated Conditions	127

INTRODUCTION

The problem of monitoring digital communication links has been under consideration for several years with a number of different groups contributing to results. The Defense Communications Agency, through the RADC Post Doctoral Program, has sponsored work at Purdue and Georgia Tech in this area over the past several years. This work has resulted in several papers [1] - [7] and two reports [8], [9].

Previous work, reported by a number of other authors [10] - [19], has resulted in methods for monitoring variables affecting performance and error rate for links using most of the common types of modulation. Fault isolation techniques seem to have received very limited attention in past work. Also, very little work has been reported on methods for processing the data produced by instantaneous bit error monitors.

The purpose of the present study is to review and unify the existing methods of link monitoring, as applied to state-of-the art digital systems, and extend these methods to provide for fault isolation. Attention will also be given to data processing techniques for the instantaneous monitor outputs.

More specifically the work is concerned with each of four tasks; namely:

(1) Review and bring together the monitoring methods applicable to state-of-the art digital radios; compare these monitoring techniques.

(2) Identify the major link faults common to all modulation types; identify specific types of failures associated with state-of-the

art modulation methods; and identify monitoring methods sensitive to each type of fault.

(3) Develop means for processing instantaneous error indications so as to produce alarms indicating that faults have occurred.

(4) Develop methods of fault isolation.

The approach to these tasks is two fold, namely: theoretical and through hybrid simulation. Because of the two pronged approach, it seems logical to discuss the work in two sections: Section I, a report on the theoretical studies and, Section II, a report on the simulation experiments. The conclusions and recommendations are presented in Section III. The work of Section I identifies a group of monitors and a collection of generic faults. The monitor responses to each fault are determined from theoretical considerations. Section II gives the results of simulation studies designed to verify and expand on the theoretical work.

The thrust of the present study is toward monitoring large portions of a communication link with centralized equipment located in the receiver. While it is desirable that the monitoring equipment be sensitive to catastrophic failures of elements and subsystems, the emphasis of the present study is on gradual degradations and on providing if possible an ability to detect small degradations before they are large enough to cause actual errors.

The monitors, which are the subject of the present study, are regarded as a complement to the alarms and specialized monitors which are tending to be designed into each piece of major digital equipment to indicate specific equipment failures. Since the monitors to be considered are located at a specific point in the communication link, many different

element failures or malfunctions will have an equivalent and indistinguishable effect on the monitor indications.

One of the stated objectives of the present study is fault isolation. As indicated above, the monitors being considered are generic in that they respond in an equivalent manner to failures or malfunctions of any element in a particular chain of elements performing a common function. Thus fault isolation will be viewed as determining from the monitor indications which of a number of generic system functions has been impaired. For example the monitors outputs will be used to determine if an outage or degradation is due to conditions in the signal or synchronization circuitry of the link. It is felt that if generic fault isolation to link subsystems can be provided by the overall monitors, then use of this information with data from equipment alarms will make it possible to work toward pinpointing specific element faults.

At least one application of fault isolation would seem to require only identification of malfunctioning subsystems. This application is that of appropriate control of procedures for regaining frame synchronization. The search procedures which are required in regaining frame synchronization are time consuming. Thus when a loss of frame synchronization is indicated by an appropriate monitor, it is desirable to know whether frame synchronization has really been lost or whether excessive noise in the signal path has effected the frame synchronization indication. Thus isolation of the fault to either the signal subsystem or the frame synchronization subsystem is all that is required.

The hybrid simulation studies, reported in Section II, deal of necessity with generic faults and typical base band system models. Although it is possible to simulate every element of a physical system, the broad scope of the present study makes this approach prohibitively time consuming.

SECTION I

THEORETICAL STUDIES

1.0 Background

Figure 1 shows one half of a typical link in a multilevel digital communication network. The digital radio transmitter and receiver is shown in more detail in Figure 2 along with the location of the monitoring equipment considered in the majority of this study.

A location for the monitoring equipment in the radio receiver is chosen because various signal parameters in the receiver are amenable to producing useful monitor outputs and because the receiver signals are sensitive to almost all faults in any part of the link.

Synchronization of bit intervals between transmitter and receiver is necessary in any digital system. In addition, if the signals from a number of different channels are time multiplexed, frame synchronization is required, as is relative synchronization of the multiplexed signals. In a nonsynchronous system, synchronization of the multiplexed signals from different channels can be accomplished through bit stuffing. Bit stuffing is a method whereby redundant signals are added in particular time slots as necessary to synchronize the inputs to a multiplexor. The redundant signals are removed at the demultiplexor.

A diagram showing the major features of a Multiplexor/Demultiplexor using bit stuffing is shown in Figure 3.

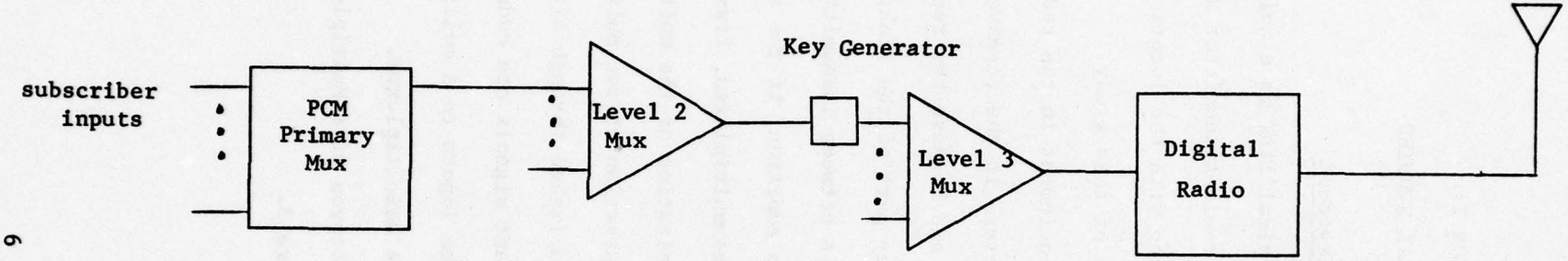


Figure 1 Typical User-to-User Link

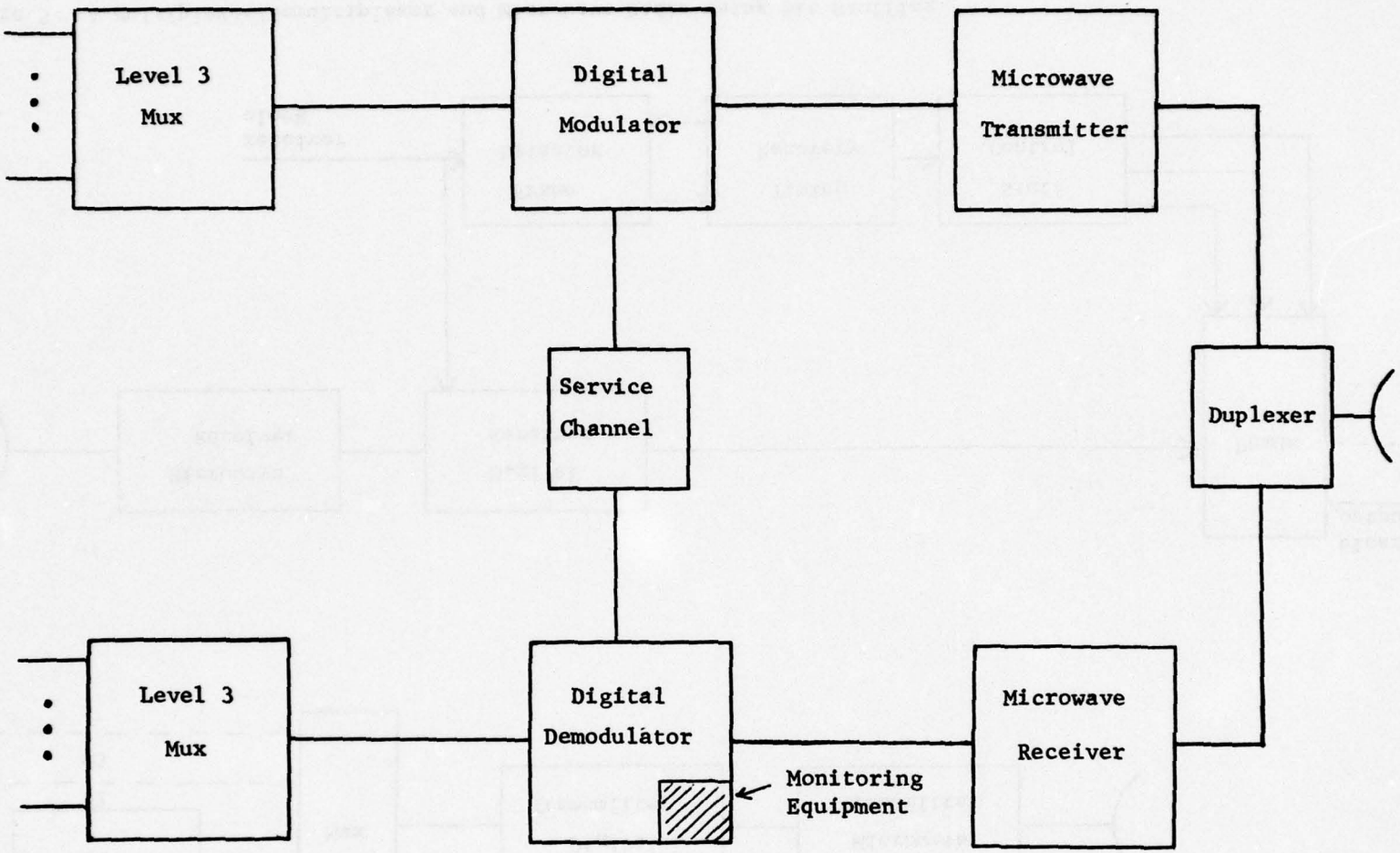


Figure 2 Typical Level 3 Radio Configuration

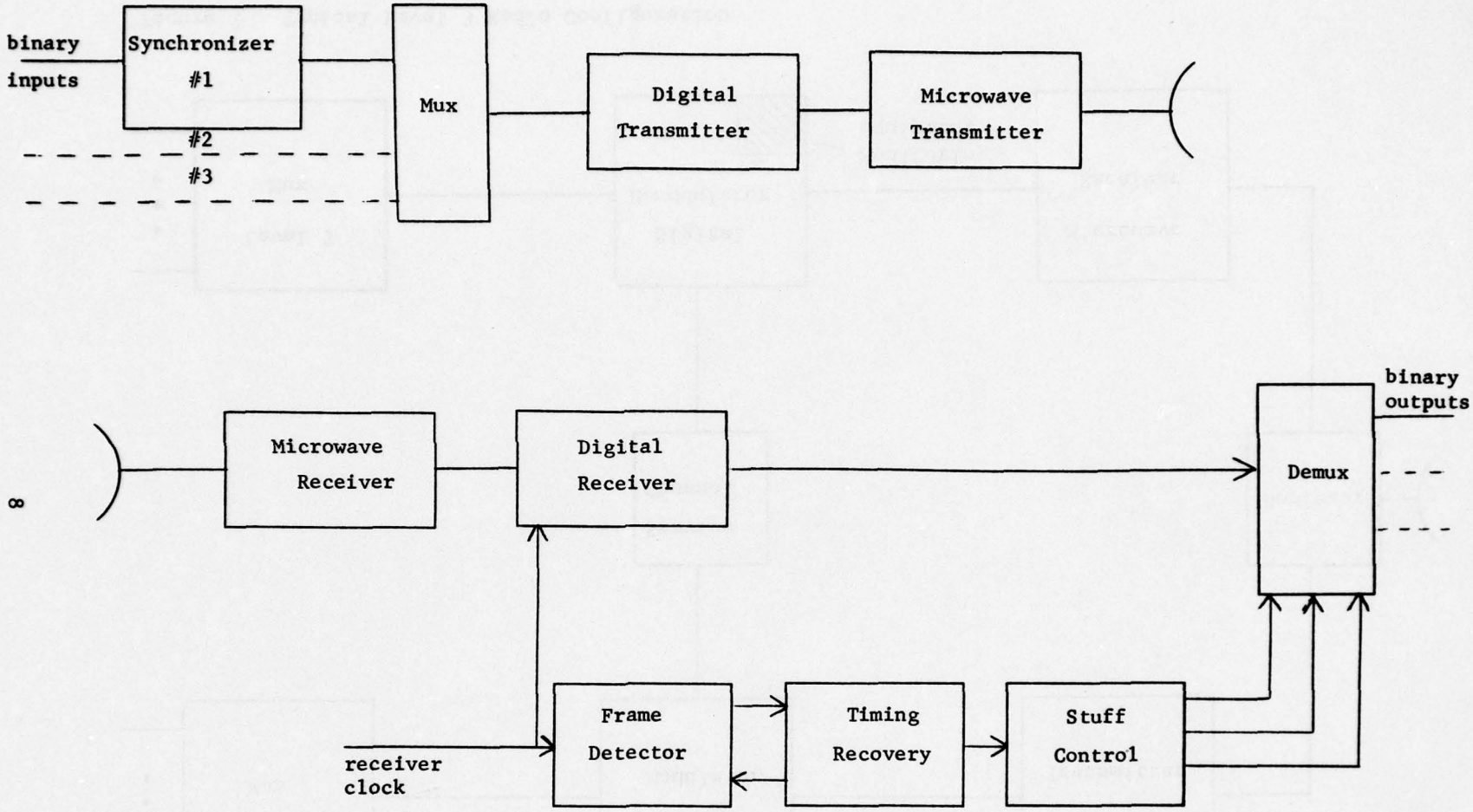


Figure 3 A Multiplexor/Demultiplexor and Microwave Radio using Bit Stuffing

1.1 Major Link Faults

A consideration of the general structure of any point-to-point digital communication link reveals a number of general types of faults which are common to the various specific systems.

In order to transmit digital information through a typical link in a hierarchical telecommunication system, means must be provided for transmitting and maintaining bit synchronization and frame synchronization as well as transmitting the information bits. Any complete monitoring strategy must, therefore, provide means for detecting malfunctions associated with these three subsystems which will be identified as: (a) the information subsystem (b) the bit synchronization subsystem and (c) the frame subsynchronization system.

1.1.1 Information Subsystems

The following types of faults directly affect the transmission of information in the information system:

(1) Open circuits in any element of the signal path.

(2) Noise added in any component.

(3) Fading of the signal due to effects in the channel.

(4) Adjacent channel interference.

(5) Distortions of the signal due to carrier drift.

(6) Changes in component gain.

All of the faults listed above have the effect of changing the signal-to-noise ratio or the signal-to-interference ratio as a function of time. Faults in the synchronization systems can have an indirect effect on signal-to-noise ratios.

1.1.2 Bit Synchronization Subsystem

Faults in the Bit Synchronization System result in either complete loss of synchronization or in jitter of the synchronization signal. Typical faults are:

(1) Excessive noise added to the synchronization signal.

(2) Loss or severe attenuation of the synchronization signal.

(3) Malfunctions of the phase locked loop used to produce the local clock signal.

The clock signal for bit synchronization is typically obtained at the receiver through a channel separate from the signal channel or from information derived from the signal channel through an averaging operation. In either case information and synchronization signals tend to be independent. The major effect of faults can thus be localized to one subsystem.

1.1.3 Frame Synchronization Subsystem

Faults in the Frame Synchronization System cause a loss of bit integrity with attendant errors resulting when parts of a message are lost or sent to the wrong destination. Faults in this system include:

(1) Failure of the circuitry for detecting the location of the framing bits.

(2) Failure of the "stuff" circuitry.

(3) Failure of the "destuff" circuitry.

(4) Abnormal differences in bit rates between two or more inputs to a multiplexor. (Differences in rates too large for the stuff circuitry to handle.)

(5) Errors in the rate of sampling multilevel analog signals to produce digital outputs.

Faults (2) - (5) produce the effect of adding or deleting bits at random in the bit stream.

The primary effect of each of the faults innumerated above is to produce one or more of the following conditions:

Affecting the Information Signal[1]

(1) Low signal-to-noise ratio due to low signal power with normal noise power.

(2) Low signal-to-noise ratio, due to high noise power with normal signal power.

(3) Complete loss of signal.

(4) Additive interference in band.

(5) Loss of one signal input to a multiplexor.

Affecting the Frame Synchronization Signals

(6) Loss of frame synchronization at any one of the three levels of the multiplex hierarchy with no degradation of the individual information signals.

(7) Loss of bit integrity caused by incorrect sampling of multilevel signal.

(8) Loss of bit integrity by extraneous insertions or deletion of one or more bits in the pulse stuffing operation.

---

[1]The signal-to-noise ratio for faults (1) and (2) or the signal-to-interference ratio for fault (5) will be taken as so small as to cause a large number of errors. For fault (3), complete loss of signal, the AGC will effectively increase the noise power to a large value.

Affecting the Bit Synchronization Signals[1]

(9) Complete loss of bit synchronization with no other signal degradation.

(10) Small bit synchronization jitter.

(11) Large bit synchronization jitter.

The eleven fault conditions listed above will be used in the remainder of the report in evaluating monitor methods. Although the list is not all inclusive, it is felt to include the primary generic effects of most faults.

1.2 General Types of Link Monitors

In recent years a number of types of link monitors have been investigated. Each method is sensitive to various classes of faults and each has its own particular characteristics, a fact which can be exploited in attempting to achieve a fault isolation capability. Many methods of testing require the use of test signals [22], [23] which disrupt or totally shut down the use of the link. Such methods are not of concern in this study, which is directed toward nondisruptive methods.

The important nondisruptive link monitor methods are now listed and discussed.

1.2.1 Received Signal Level Monitors

Received signal level monitors have been implemented in several ways, namely:

(i) by measuring received energy

---

[1] Fault (11), large bit synchronization jitter, will imply a maximum timing error on the order of one half of the signaling interval. Fault (10), small bit synchronization jitter, will imply a maximum timing error on the order of one tenth of the signaling interval.

(ii) by indicating the presence or absence of the carrier

(iii) by noting the AGC voltage.

Such a monitor variable is sensitive to all faults which remove or severely attenuate the transmitted or received signal. This monitor is applicable to any modulation type with or without partial response signaling.

1.2.2 Eye Pattern Monitors

The eye pattern type of monitor indication [17], [21] has been used extensively. This type of monitor simultaneously displays the received signals from a number of signaling intervals on an oscilloscope. By properly interpreting the resulting waveform an indication of the presence of almost all types of faults can be obtained. The method is applicable to all types of systems.

The major shortcoming of the method lies in the fact that it is essentially limited to manual operation since a careful and detailed analysis of many features of the displayed waveform is required. Many of the other, nonmanual, types of monitors can be regarded as automated implementations of certain features of the eye pattern waveforms.

1.2.3 Out-of-Band Noise Monitors

This type of monitor measures the noise power in a narrow frequency band just outside of the band occupied by the signal of the system being monitored. Use of the monitor is predicated on the fact that increases in noise power typically occur over a wide frequency band so that an increase in the out-of-band noise power usually accompanies an increase in the in-band noise power.

This type of monitor can be used with almost any type of modulation with or without partial response. It is sensitive almost exclusively to the level of noise power, although it would be sensitive to power in the bandwidth of the monitor regardless of its source.

1.2.4 Format Violation Monitors

This general type of monitor is designed to be senstive to deviations from a prescribed format for some feature of the transmitted signal. Several types of such monitors have been discussed in the literature [14], [15], [16], [18], and each will be considered separately.

Format Violation - Parity Check: This method requires the addition of a redundant bit in each block of data in a binary information stream. The redundant bit is chosen to produce either even or odd parity in the transmitted block so that single errors can be detected by observing the parity of the received signal.

The method is sensitive to all single errors in the information system regardless of the source of the error. It can be applied with any type of modulation with or without partial response.

Format Violation - Frame Bit: To maintain frame synchronization, some specified pattern of frame bits must be added to the information bit stream. The frame bit pattern is subsequently detected at the receiver to provide framing information.

The absence of single frame bits in their proper location can be detected and used as a frame bit error indication. In addition, data on the absence of single frame bits can be processed to provide an "out-of-frame" indication if frame bits are in error in all of a sequence of frames of specified length.

The single frame bit error indication can be caused by degradations in the information or bit synchronization systems which result in a single frame bit being in error as well as by malfunctions of the frame synchronization system which result in an incorrect frame bit pattern. The out of frame indication has a reduced sensitivity to errors in the information or bit synchronization subsystems while maintaining a strong sensitivity to an incorrect frame bit pattern caused by errors in the frame synchronization subsystem.

Both types of frame bit indications can be used with any type of modulation or with partial response.

Format Violation - Partial Response: For partial response signaling, a correlation between successive information bits is introduced at the transmitter. As a result of this correlation, not all transitions between levels in the partial response signal are permissible and a monitor, sensitive to forbidden transitions, can be devised. This type of monitor produces a count whenever the received signal on one signaling interval produces a format violation, although in some cases the count is not coincident with the error.

This type of monitor is sensitive to pertubations of the multilevel partial response signal caused by noise, interference, or large jitter in bit synchronization. The monitor is, of course, restricted to partial response signaling.

1.2.5 Pseudo-Error Monitors [1], [2], [17]: This general type of monitor is sensitive to received signal vectors which fall near the decision threshold used to produce a discrete output from a received analog signal.

The monitor is typically implemented by establishing a pseudo-error region about each decision threshold so that a pseudo-error count is recorded each time a signal vector falls in such a region. Choice of the width of the region determines the "gain" of such a monitor. A near error, rather than a true error, is indicated and thus this monitor can provide an indication of a trend toward error.

Pseudo-error monitors can be designed for any type of modulation with or without partial response. This type of monitor is sensitive to faults in the information subsystem or the bit synchronization subsystem.

1.2.6 Pseudo-Error for Trend Indications: Of the monitors discussed above, only the pseudo-error type will give an indication of a trend toward error before errors occur.

The use of "pseudo-errors" with other types of monitors for trend indications has been reported by Smith [18] and others. A typical use of pseudo-errors in this way is to offset the time of the samples of an analog partial response waveform and compare these delayed (or advanced) samples with the usual decision thresholds to obtain a modified discrete output. A format violation monitor can then be used to indicate the pseudo-errors in the modified discrete output signal. The amount of change in the sampling time determines the "gain" in producing pseudo-errors.

The combination of an artifice for producing pseudo-errors and an error monitor results in a composite monitor method with the possibility for a trend indication. The characteristics of the basic monitor method are not changed by using it to indicate pseudo-errors.

Table 1 summarizes the discussion of general types of monitors by indicating the sensitivity of various monitors to the general types of faults discussed in Section 1.1.

1.3 Data Processing Techniques for Error Rate Monitors

The monitor variables pseudo-error, parity violation and format violation - partial response, provide indications of a single event, related to bit error, on each signaling interval. These instantaneous "error" readings are less useful as a monitor indication than an average error rate, which can be related to error probability. To obtain average error rate, some processing of the basic data is required.

The remaining material in this section of the report analyzes an algorithm which computes a running average of the error indications produced by any of the three monitors listed above over K past bits. The output of this running average is then compared to a threshold level, T, so that values above the threshold indicate a fault and values below the threshold indicate satisfactory operation.

Numerical values for K and T can be obtained from the analysis given below if four additional numbers are specified, namely:

P_1 - the probability of indicating a fault with none present (probability of false alarm)

P_2 - the probability of indicating a fault if one is present (probability of correct detection)

P_F - the probability of an error indication from the monitor method being considered under the condition of a fault

Table 1 Indication of Sensitivity of Various Monitors to Various Faults

Faults	General Types of Monitors							
	RSL	Eye Pattern	Format Violation				Pseudo Error Amplitude	Out-of-Band Noise
			Parity Check	Single Frame Bit	Out-of-Frame	Partial Response		
Low S/N normal noise low signal	X	X	X	X	X	X	X	
Low S/N high noise normal signal		X	X	X	X	X	X	X
Complete loss of signal	X	X	X	X	X	X	X	
Additive interference		X	X	X	X	X	X	
Loss of one signal to multiplex	X	X	1	X	X	X	X	
Loss of frame sync			X	X	X			
Loss of bit integrity (sampling)			1	X	X	X		
Loss of bit integrity			1	X	X			
Loss of bit sync		X	X	X	X	X	X	
Small bit sync jitter		X				X	X	
Large bit sync jitter		X	X	X	X	X	X	

Notes: 1. Depends on where parity check is applied in relation to fault.
2. A timing-type pseudo-error can be used with any one of several monitors to provide an error margin.

P_0 - the probability of an error indication from the monitor method being considered under the condition of no fault.

Let the instantaneous error indication be denoted r_i, defined as

$$r_i = \begin{cases} 1, \text{ for error indication} \\ 0, \text{ otherwise.} \end{cases} \tag{1}$$

The probability that $r_i = 1$ is the probability of an error indication, which is denoted p_e. A straightforward calculation gives the mean and variance of r_i as

$$E\, r_i = p_e \tag{2}$$

$$\text{Var } r_i = p_e\,(1 - p_e). \tag{3}$$

The running sum, $R_K(n)$, given by

$$R_K(n) = \frac{1}{K} \sum_{i=n-K+1}^{n} r_i \tag{4}$$

is used as the basis for a monitor indication. Note that

$$P_e = P\{r_i=1\} \cong \lim_{K \to \infty} \frac{1}{K} \sum_{i=n-K+1}^{n} r_i = \underset{K \to \infty}{\text{limit}} \frac{\text{(no. of errors)}}{\text{(no. of bits)}}$$

and that $R_K(n)$, for finite K, is a noisy estimate of p_e.

A test for a fault is prescribed as follows:

If $R_K(n) \geq T$ indicate a fault

If $R_K(n) < T$ indicate no fault.

The parameters T and K are now specified in terms of the four variables, p_1, p_2, P_0, and P_F.

As a first step in the calculation, the mean and variance of $R_K(n)$ can be determined to be

$$E\, R_K(n) = p_e \tag{5}$$

$$\text{Var}\, R_K(n) = \frac{p_e\,(1-p_e)}{K} \,. \tag{6}$$

Since the random variables r_i are binary random variables, $R_K(n)$ is a discrete random variables and its probability function is given by

$$P\{R_K(n) = \frac{x}{K}\} = \binom{K}{x} (1-p_e)^{K-x}\, p_e^x \tag{7}$$

where $\binom{K}{x}$ are the binomial coefficients. Equation (7) specifies a binomial distribution.

Give the test defined above, p_1 and p_2 are specified by the following conditional probabilities

$$p_1 = P\{R_K(n) \geq T/p_e = P_0\} \tag{8}$$

$$p_2 = P\{R_K(n) \geq T/p_e = P_F\} \tag{9}$$

Using the probability function of (7), either of these probabilities can be expressed as

$$P_i = \sum_{x=KT}^{\infty} \binom{K}{x} (1-p_e)^{K-x}\, p_e^x \tag{10}$$

where KT is assumed to be an integer and $p_e = P_0$ for i = 1 or P_F for i = 2.

Equation (10) evaluated for i = 1 and 2 gives two equations in the unknowns T and K since the quantities p_1, p_2, P_0 and P_F are assumed to be known. Accuracy requirements would not typically require solution of the

two equations in the finite sum form of (10). Instead it is usually satisfactory to approximate (10) by the integral of the continuous function Gaussian function, (see for example Papoulis [24]), to obtain

$$P\{R_K(n) \geq T\} \cong \int_{TK}^{\infty} \frac{1}{\sigma\sqrt{2\pi}} e^{-(k-k_0)^2/2\sigma^2} dk \qquad (11)$$

where $k_0 = K\, p_e$ and $\sigma = \sqrt{K\, p_e(1-p_e)}$. The integral in (11) can be expressed in terms of the function Q(x), defined as

$$Q(x) = \int_{TK}^{\infty} \frac{1}{\sqrt{2\pi}} e^{-u^2/2}\, du \qquad (12)$$

which is tabulated.

Using Q(x) and the approximation of (11) the conditional probabilities of (8) and (9) can be expressed as

$$p_1 = P\{R_K(n) \geq T/p_e = P_0\} = Q\left[(T-P_0)\left(\frac{K}{P_0(1-P_0)}\right)^{\frac{1}{2}}\right] \qquad (13)$$

$$p_2 = P\{R_K(n) \geq T/p_e = P_F\} = Q\left[(T-P_F)\left(\frac{K}{P_F(1-P_F)}\right)^{\frac{1}{2}}\right] \qquad (14)$$

Solution of these equations for T and K then yields

$$\sqrt{K} \cong \frac{[P_0(1-P_0)]^{\frac{1}{2}}}{P_F - P_0}\, Q^{-1}(p_1) - \frac{[P_F(1-P_F)]^{\frac{1}{2}}}{P_F - P_0}\, Q^{-1}(p_2) \qquad (15)$$

$$T \cong \frac{P_F[P_0(1-P_0)]^{\frac{1}{2}} Q^{-1}(p_1) - P_0[P_F(1-P_F)]^{\frac{1}{2}} Q^{-1}(p_2)}{[P_0(1-P_0)]^{\frac{1}{2}} Q^{-1}(p_1) - [P_F(1-P_F)]^{\frac{1}{2}} Q^{-1}(p_2)} \qquad (16)$$

where Q^{-1} denotes the inverse of the Q function.

In many cases of interest the following restrictions apply:

$$p_1 = 1 - p_2$$

$$P_0 << P_F << 1.$$

In such cases (15) and (16) reduce to the more tractable expressions

$$K \cong \frac{[Q^{-1}(p_1)]^2}{P_F} \tag{17}$$

$$T \cong \sqrt{P_0 P_F}. \tag{18}$$

Table 2 below gives K and T for several values of P_0 for $p_1 = .05$, $p_2 = .95$ and $P_F = 10\ P_0$.

Table 2 Values of K and T ($p_1 = .05$, $p_2 = .95$, $P_F = 10\ P_0$)

P_0	K	T
10^{-5}	2.7×10^{4}	3.2×10^{-5}
10^{-4}	2.7×10^{3}	3.2×10^{-4}
10^{-3}	2.7×10^{2}	3.2×10^{-3}
10^{-2}	2.7×10	3.2×10^{-2}

Using the analysis above, values for K in the running sum of (4) and for the threshold T can be computed. The output of a specific monitor, such as a pseudo-error monitor, is then averaged by the running sum. If the running sum exceeds T a fault is indicated, while if the running sum is below T, operation can be assumed to be normal. The values of K and T depend on the following required information:

P_F - an estimate of the probability of an error indication from the monitor method being used under the condition of a fault

P_0 - an estimate of the probability of an error indication from the monitor method under the condition of no fault

p_1 - an assigned false alarm probability which can be tolerated

p_2 - an assigned probability which can be tolerated for indicating a fault if one is present.

1.4 Format Violation Monitors for Links using Partial Response Signaling

Partial Response signaling was developed in an effort to reduce intersymbol interference for a fixed rate of transmission or, conversely, to make it possible to increase the rate of transmission for a fixed error probability. The technique uses to advantage the correlation between message bits introduced by the known channel characteristics. Precoding, (a method for introducing correlation between message bits at the transmitter), is used in current systems to avoid error propagation.

Partial response signaling can be used with any modulation method. In this report 3-level and 7-level partial response signaling with an FM modulated carrier are studied both theoretically and through simulation. Quadrature partial response which involves amplitude modulation of PSK signals is given some theoretical attention in section 1.5.3.

1.4.1 Three-level Partial Response

Three-level partial response has been studied in detail in earlier work under the subject contract (see for example [5], [8] and [9]). It seems desirable, however, to review this work briefly as a background for 7-level partial response.

Three-level partial response has a binary input which is encoded into a 3-level partial response signal as shown in the diagram below.

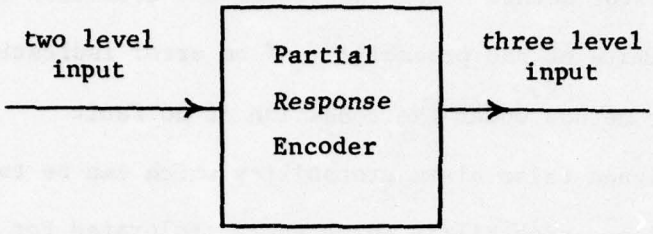


Figure 4 Three-level Partial Response Encoder

The equations describing the encoding operation for class 1 partial response, are as follows (see for example Craig [17] for a list of the 5 common classes),

$$b_k = a_k \oplus b_{k-1} \tag{19}$$

$$b_k' = \begin{cases} d, & b_k = 1 \\ -d, & b_k = 0 \end{cases} \tag{20}$$

$$y_k = b_k' + b_{k-1}' \tag{21}$$

where $\{a_k\}$ is the binary input sequence with a_k equal to 0 or 1, $\{b_k\}$ is the precoded input sequence with b_k equal to 0 or 1, $\{y_k\}$ is the partial response sequence with y_k equal to $\pm$ 2d or 0 and the symbol $\oplus$ indicates modulo-2 addition.

The decoding operation is described by

$$\hat{a}_k = 0 \text{ if } y_k = \pm 2d$$
$$\hat{a}_k = 1 \text{ if } y_k = 0 \,. \tag{22}$$

Equations (19), (20), and (21) place constraints on possible sequences of y_k values under noise free conditions. For example consider the sequence y_{k+1}, y_k. From (21) it is straightforward to obtain the equation

$$y_{k+1} - y_k = b'_{k+1} - b'_{k-1} \quad . \tag{23}$$

Since b'_k can take on only the values $\pm$ d, $b'_{k+1} - b'_{k-1}$, and hence $y_{k+1} - y_k$, can take only the values 0, $\pm$ 2d. Consideration of (23) and the fact that y_k can take on the values $\pm$ 2d, 0 leads to the conclusion that (23) cannot hold for the conditions

$$y_{k+1} = 2d \ , \ y_k = -2d$$

or

$$y_{k+1} = -2d, \ y_k = 2d \ .$$

Thus the sequences 2d, -2d and -2d, 2d are forbidden. A similar analysis using longer sequences of y_k establishes the following format rules:

(i) Equal extreme values of y_k must be separated by an even number of zero values for y_k. (i.e. 2d, 0, 0, 2d is allowable while -2d, 0, -2d is not).

(ii) Non-equal extreme values of y_k must be separated by an odd number of zero values. (i.e. 2d, 0, -2d is allowable while 2d, -2d and 2d, 0, 0, -2d are not.)

Note that the case discussed above violates rule (ii).

An obvious monitoring technique is to check for violations of the forbidden transitions. Since the forbidden transitions do not occur for ideal operation, every format violation indicates that an error has occurred.

1.4.2 Seven-level Partial Response

At least two authors have discussed format violation monitors for partial response signals with more than three levels. Gibson [16] discusses 7-level class 4 systems and Gunn and Lombardi [19] discuss a 15-level, apparently class 4, system. The monitors and conclusions from these papers can be adopted to 7-level class 1 operation. The monitors are designed in a manner similar to that used for three-level partial response. As in the three-level case, occurrences of forbidden transitions are noted and identified as errors.

For seven-level partial response the input, A_i, is a sequence of four-level signals. The A_i are precoded into a sequence B_i which are then encoded into a transmitted seven-level signal S_i. The values taken on by the A_i, the B_i and the S_i are given below:

$\{A_i\}$ - 4-level input sequence - values (0, 1, 2, 3)

$\{B_i\}$ - 4-level precoded sequence - values (0, 1, 2, 3)

$\{B_i'\}$ - analog values of 4-level precoded sequence - values (-3, -1, 1, 3)

$\{S_i\}$ - 7-level partial response sequence - values (-6, -4, -2, 0, 2, 4, 6)

The precoding, coding and decoding algorithms are respectively

$$B_i = A_i - B_{i-1} \text{ (Mod 4)}; \; B_0 = 0 \tag{24}$$

$$S_i = B_i' + B_{i-1}'; \; B_0 = -3 \tag{25}$$

Decoding Algorithm

S_i	A_i'
-6, 2	0
-4, 4	1
-2, 6	2
0	3

As in the case of three-level partial response, (24) and (25) place restraints on possible sequences of S_i. Unlike three-level partial response, however, the number of forbidden transitions in seven-level partial response seems to be too large and too dependent on past states to allow for easy identification of forbidden transitions. As an alternative, the authors cited above suggested a monitor based on the solution to (25). Under ideal no noise conditions, (25) can be expressed as

$$S_i - B'_{i-1} = B'_i \ . \tag{25a}$$

Since B'_i takes on only the values (-3, -1, 1, 3), it follows that

$$-3 < S_i - B'_{i-1} < 3 \ . \tag{26}$$

An implementation of a monitor based on (26) is diagramed in Figure 5, where the symbols $\overline{S_i}$ and $\overline{B'_i}$ indicate the values of S_i and B'_i at the receiver for the condition of noisy operation. Note that the monitor shown is a feedback type circuit which is initialized with $B'_0 = -3$. It solves in effect the equation

$$\overline{B'_i} = \overline{S_i} - \hat{B}_{i-1} \ . \tag{27}$$

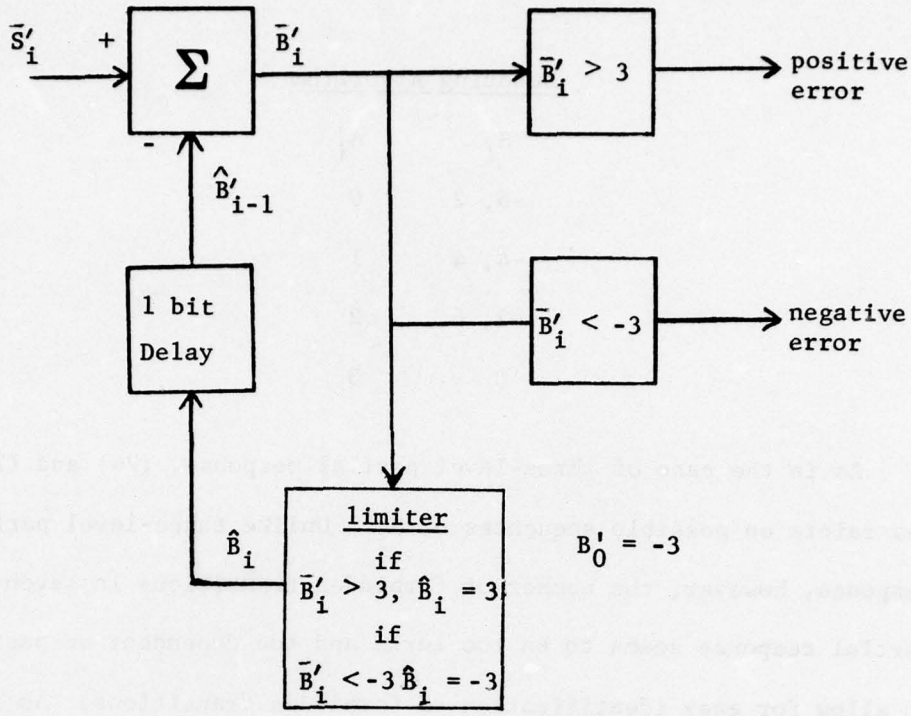


Figure 5 An Error Monitor for 7-level, Class 1 Partial Response Systems

If an error occurs for any state in $\overline{S_i}$, the error is propagated around the closed loop until $|\overline{B_i}| > 3_i$ for some i, not necessarily that coincident with the error. After an error has caused $|\overline{B_i}| > 3$ the limiter causes $\hat{B}_i$, the signal feedback, to be ± 3 so that the monitor "resets" to an error free condition until the arrival of another error in $\overline{S_i}$.

Gibson shows that the monitor has the following additional properties:

(i) The probability that the error occurred more than approximately 25 bits prior to an indication is small.

(ii) The monitor fails to detect an error when a second error of opposite sign occurs before the first error is detected.

An elementary analysis substantiates several of the properties stated above and suggests a new use of the monitor. Let the ith received signal be in error by ϵ so that

$$\overline{S_i} = S_i + \epsilon \tag{28}$$

Such a condition would occur if noise was added to S_i. The output, $\overline{B'_i}$, of the monitor is then

$$\overline{B'_i} = \overline{S_i} - \hat{B}_{i-1} = S_i - \hat{B}_{i-1} + \epsilon$$

If it is assumed that the system suffers only one error, located on the ith signaling interval, then

$$\hat{B}'_{i-1} = B'_{i-1}$$

and, using (25)

$$\overline{B'_i} = B'_i + \epsilon$$

Further calculation using (25a), and assuming that no error has been indicated, yields

$$\overline{B'_{i+1}} = S_{i+1} - \hat{B}_i = S_{i+1} - B'_i - \epsilon = B'_{i+1} - \epsilon$$

$$\overline{B}_{i+2} = S_{i+2} - \hat{B}_{i+1} = S_{i+2} - B'_{i+1} + \epsilon = B'_{i+2} + \epsilon$$

$$\overline{B'_{i+3}} = S_{i+3} - \hat{B}_{i+2} = S_{i+3} - B'_{i+2} - \epsilon = B'_{i+3} - \epsilon$$

Note that an error indication will not occur until $\overline{B'_i} = B'_i \pm \epsilon$ has a value such that

$$|B'_i \pm \epsilon| > 3 \ .$$

For arbitrarily small ϵ such an indication will always occur for $B_i' = \pm 3$. It would seem reasonable to conclude that typical noise perturbations will result in $|\epsilon|$ on the order of three or less.

Now consider another type of error, namely loss of bit integrity, through the deletion or insertion of a bit into the 7-level bit stream. This could occur for example through errors in the time of sampling the 7-level analog signal. For this condition, rather than being in error by a relatively small quantity ϵ, $\overline{S_i}$ is effectively a random choice of its possible values from the set (-6, -4, -2, 0, 2, 4, 6). Thus for this case there is a reasonable chance that the monitor output, $\overline{B_i'}$, is considerably greater than 3 in magnitude. Possible values of $\overline{B_i'} = \overline{S_i} - \overline{B_{i-1}'}$ are listed below in Table 3.

Table 3 Possible values of $\overline{B_i'}$

$\overline{S_i}$ \ $\overline{B_{i-1}'}$	3	1	-1	-3
6	3	5	7	9
4	1	3	5	7
2	-1	1	3	5
0	-3	-1	1	3
-2	-5	-3	-1	1
-4	-7	-5	-3	-1
-6	9	7	-5	-3

A study of the table shows that under the conditions of loss of bit integrity described, $|\overline{B_i'}|$ can be as large a 7 or 9. This suggests that $|\overline{B_i'}|$ values in the range 3-6 be associated with excessive random noise, while values of 7 or higher be identified with a loss of bit integrity in the 7-level signal.

1.5 Specific Systems

Three specific types of systems are considered in the present study, namely four-level FM, seven-level partial response on an FM carrier and quadrature partial response. For the first two systems, which are well documented in the literature, generic diagrams are given in this section of the report along with comments on specific faults and monitoring methods. For the quadrature partial response system a brief review of the basic operation is also included.

An effort has been made to treat as many effects in a general category as possible and thus minimize the system dependent considerations. For example, faults in digital-to-analog and analog-to-digital conversion devices are treated generically. Each system must have such devices, even though the nature of the analog signals is different for the different specific modulations.

In spite of efforts to minimize system dependence it is necessary to identify a few characteristics which are not common to all of the systems and this is done below. Most of the specific faults identified produce one or more of the generic effects listed in Section 1.1 on the signals of one of the three subsystems.

1.5.1 Four-Level FM

A basic block diagram of a four-level FM system is given in Figure 6. Faults unique to this system have to be characteristic of the four-level FM type modulation. Such faults include the following:

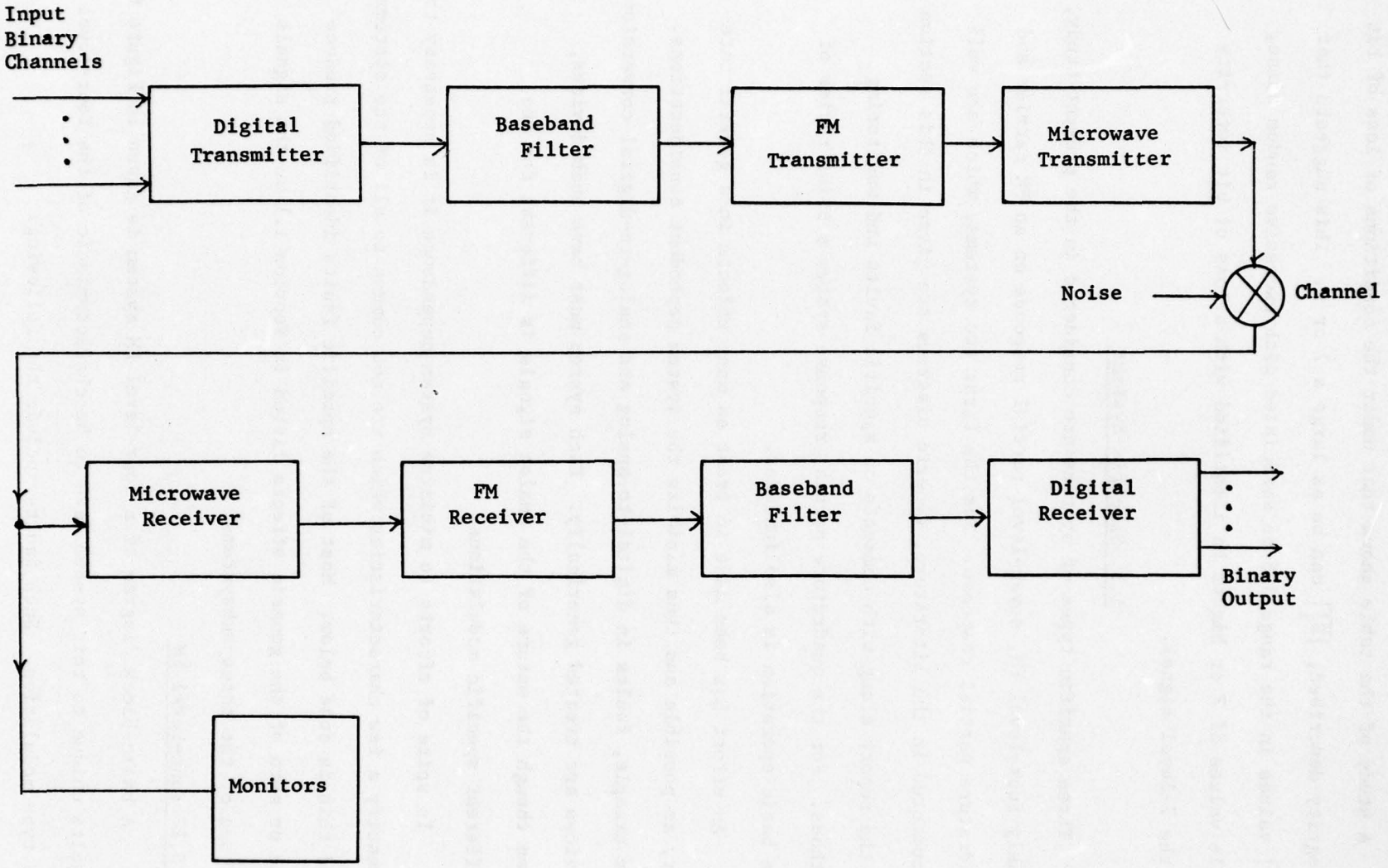


Figure 6 Generic Block Diagram for a 4-Level FM System

(1) carrier offsets from the center frequency of filters

(2) noise effects peculiar to frequency modulation

(3) specific faults in the FM transmitter or receiver which remove or distort the signal

Of the monitors described in Section 1.2, all but the format violation monitor designed for partial response signaling are applicable to FM.

1.5.2 7-Level Partial Response

The 7-level partial response system being considered is basically an FM system modulated by a partial response signal, as shown in Figure 7.

In order to provide partial response signaling, a Precoder, a Transmit and Receiver Filter, and a Decoder have been added to the basic FM system. Faults in these added components, all of which affect the 7-level signal, are thus characteristic of this system.

All of the monitors of Section 1.2 are applicable including the partial response format violation monitor. The latter monitor will detect any faults which disturb the prescribed correlation properties of the 7-level signal.

1.5.3 Quadrature Partial Response Systems (QPR)

The basic QPR system uses a modified duobinary base band signal described by Lender [25]. Such a signal can be generated in two ways as shown in the block diagrams of Figure 8 (a). For either system the two encoders are described by the equations

$$\text{Encoder 1:} \qquad B_i = A_i \oplus B_{i-1} \tag{29}$$

$$\text{Encoder 2:} \qquad C_i = B_i \oplus C_{i-1} \tag{30}$$

where A_i, B_i and C_i represent the amplitudes of "binary square waves." It is straightforward to show that the overall encoding of both encoders

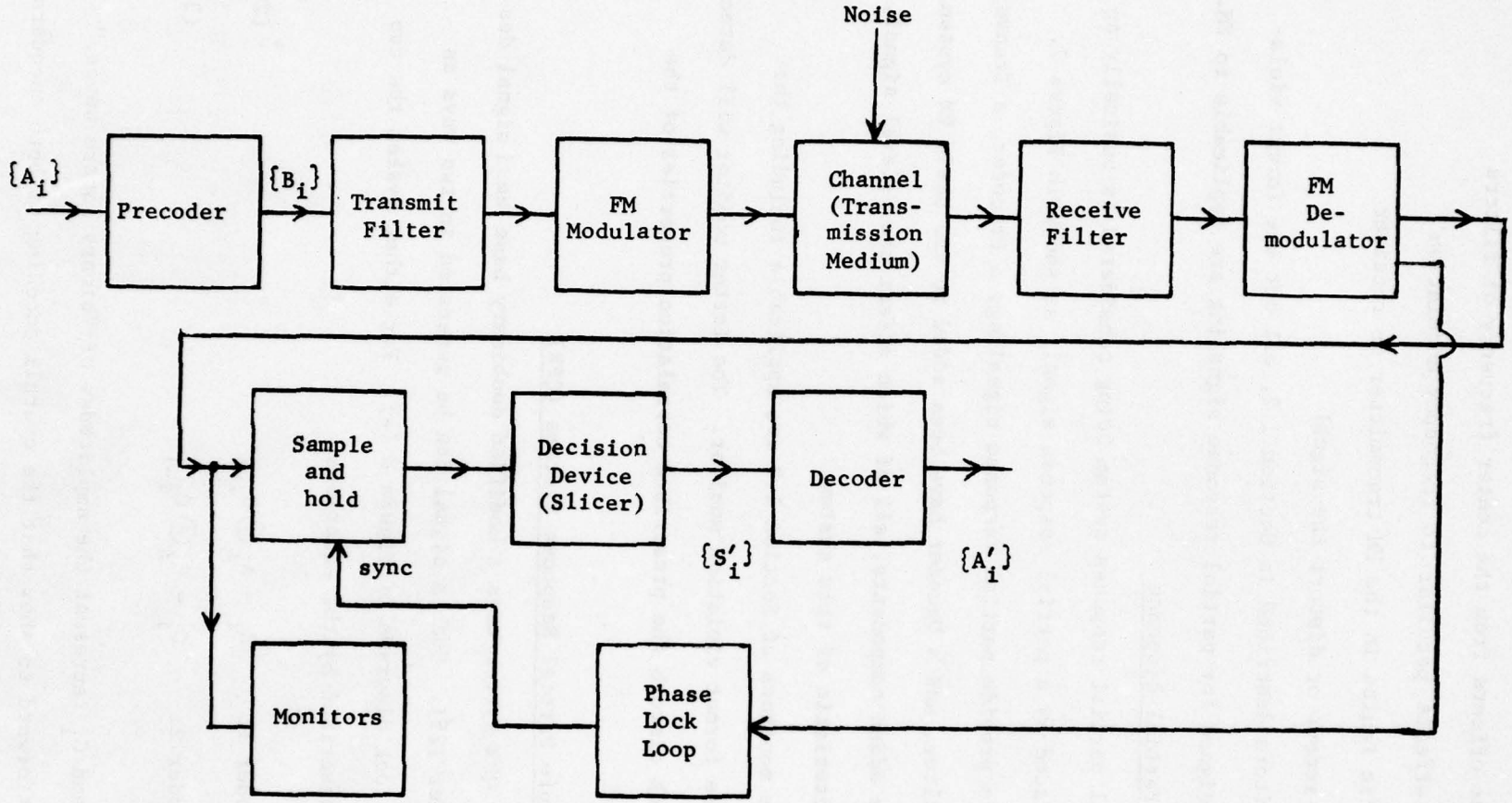


Figure 7 A General Partial Response/FM System Diagram

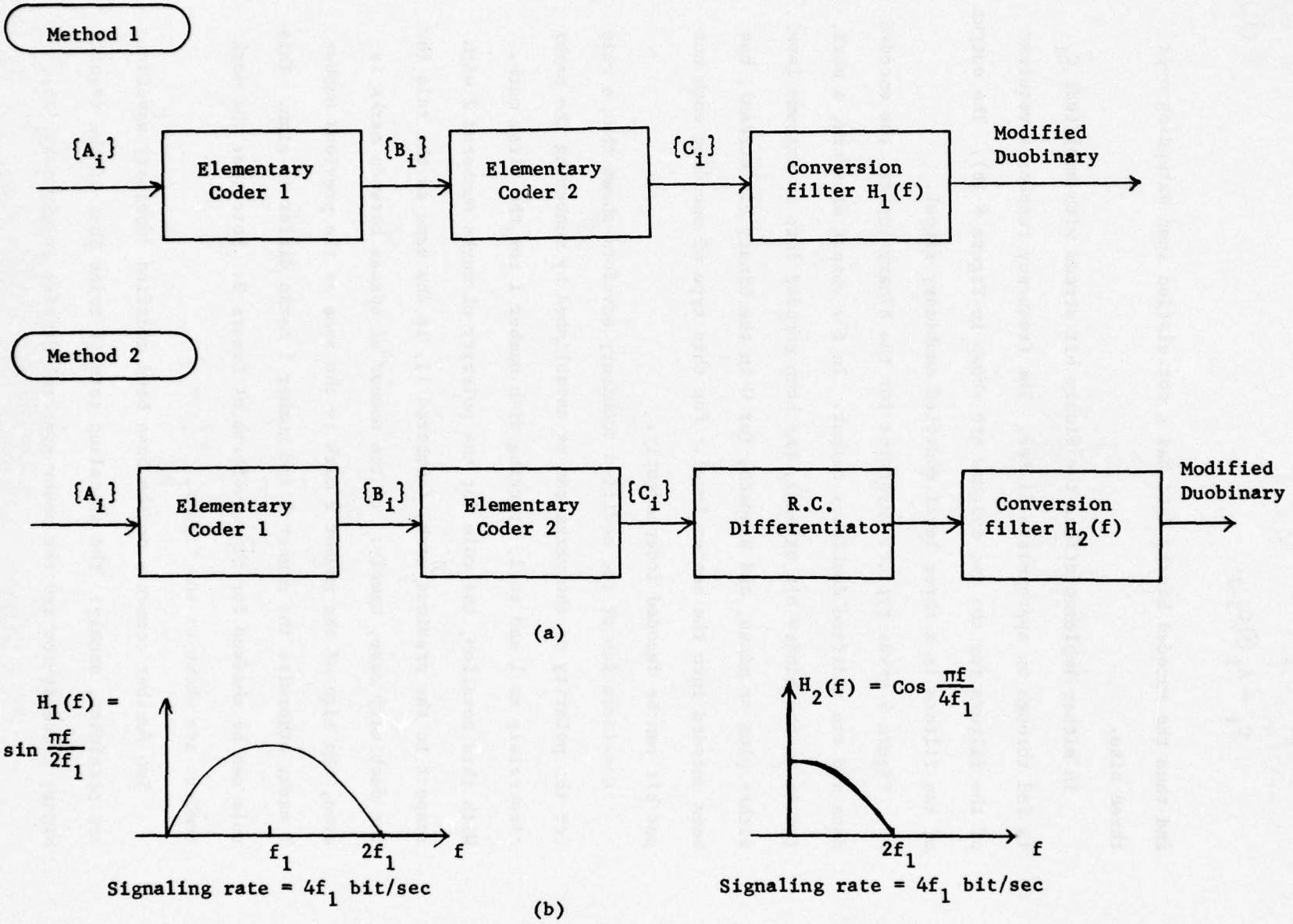


Figure 8 Generation of a Modified Duobinary Signal and its Resulting Spectrum

relates A_i and C_i by the equation

$$C_i = A_i \oplus C_{i-2}, \tag{31}$$

and thus the encoded binary data has a correlation span extending over three bits.

In either implementation, the binary bit stream with amplitude C_i is fed through an appropriate filter. The frequency responses required of the filters for the two systems are shown in Figure 8 (b). The output of the filters is a three level modified duobinary signal.

Figure 9 gives typical waveforms for the binary inputs, the encoded data and the modified duobinary output. In the output waveform, a mark, (or +1 in the binary bit stream), has been encoded into an extreme level, either plus or minus, and a space, (or 0 in the binary bit stream), has been encoded into the center level. For this type of encoding each output bit can be decoded independently.

Consideration of the modified duobinary waveform shows that a rule for the polarity of the marks can be established by numbering the marks alternately as 1 and to 2, starting with number 1 for the first mark. With this notation, the rule for the polarity of marks numbered 2 with respect to the previous mark, (numbered 1), is the same as the rule for the duobinary case, namely: if the number of spaces between marks is even, the sign of the number 2 mark is the same as the previous number 1 mark; otherwise the number 2 and number 1 marks differ in sign. This rule can be chedked for the waveforms of Figure 9. Note that the mark numbers are shown on the figure.

Two further comments on the base band modified duobinary waveform are pertinent, namely: the signaling rate is twice that of the regular binary transmission and the power spectral density is given by, [25],

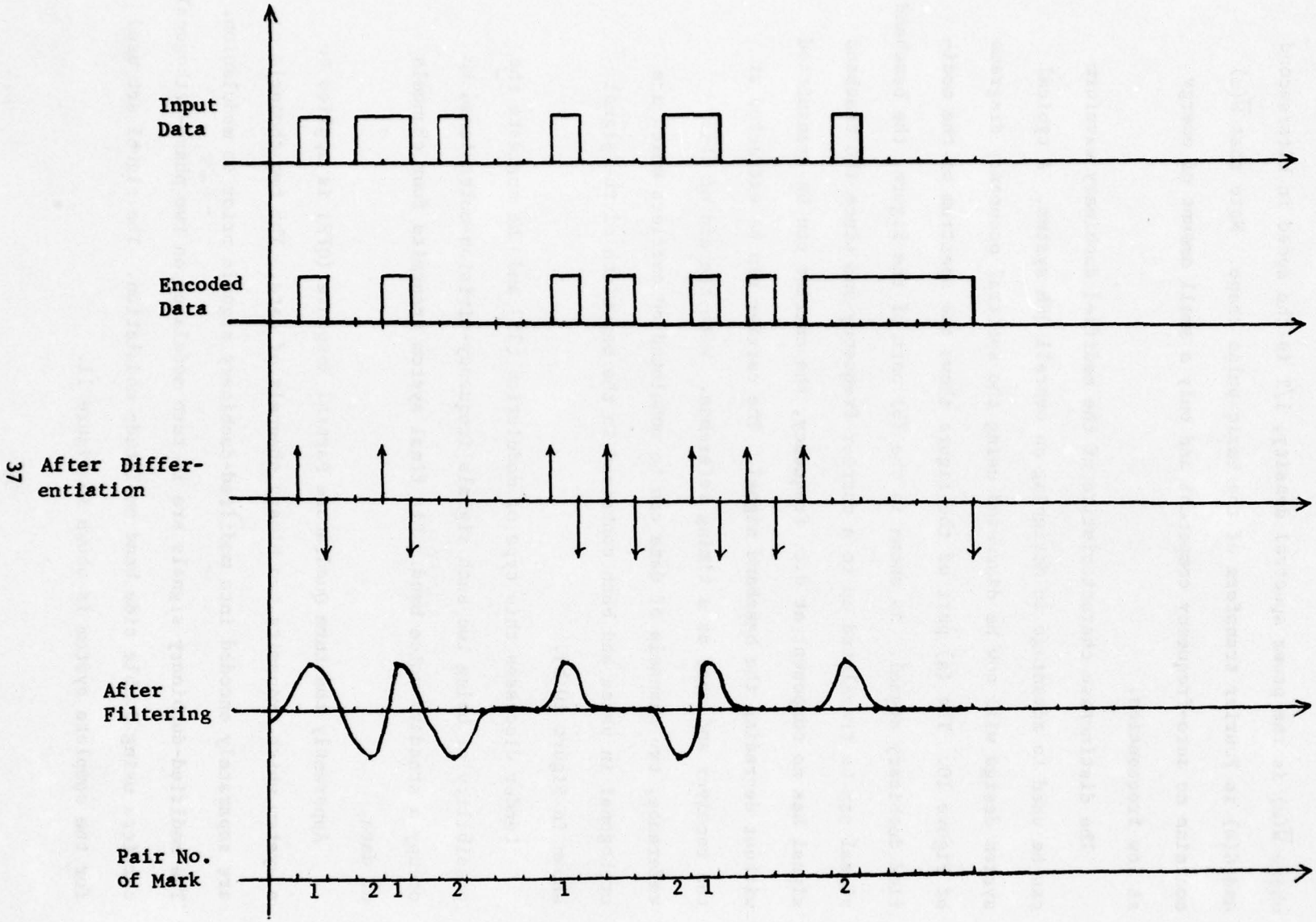


Figure 9 Typical Duobinary Time Waveforms

$$\overline{W}(\omega) = \frac{1}{4T} |G(\omega)|^2 \sin 2\omega T \qquad (32)$$

where $\overline{W}(\omega)$ is the power spectral density, 1/T is the speed in bits/second and $G(\omega)$ is Fourier transform of the basic pulse shape. Note that $\overline{W}(\omega)$ contains no zero-frequency component and only a small amount of energy at low frequencies.

The distinctive characteristics of the modified duobinary waveform can be used to advantage in designing an overall QPR system. A typical system design will now be discussed using the spectral occupancy diagrams of Figure 10. The (a) part of the figure shows the spectrum of the modified duobinary signal. As shown in the (b) part of the figure, the baseband signal can be translated up to a carrier frequency and since the baseband signal has no component at d.c. frequency, the carrier can be transmitted without degrading the baseband signal. The carrier can be extracted at the receiver and used as a timing reference. With the aid of this reference, two channels of data can be modulated on carriers which are orthogonal in phase and both contained in the bandwidth of the signal shown in Figure 10(b).

Lender discusses this type of modulation [25] and he suggests the possibility of using two such signals frequency-division-multiplexed to occupy a standard voice band. His final system transmits four channels of data.

Apparently the term Quadrature Partial Response (QPR) is applied to a system which transmits two binary channels of data. The two channels are separately encoded into modified-duobinary signals prior to modulation. The modified-duobinary signals are in turn modulated on two phase-orthogonal carriers using double side band amplitude modulation. The signal set used for the complete system is shown in Figure 11.

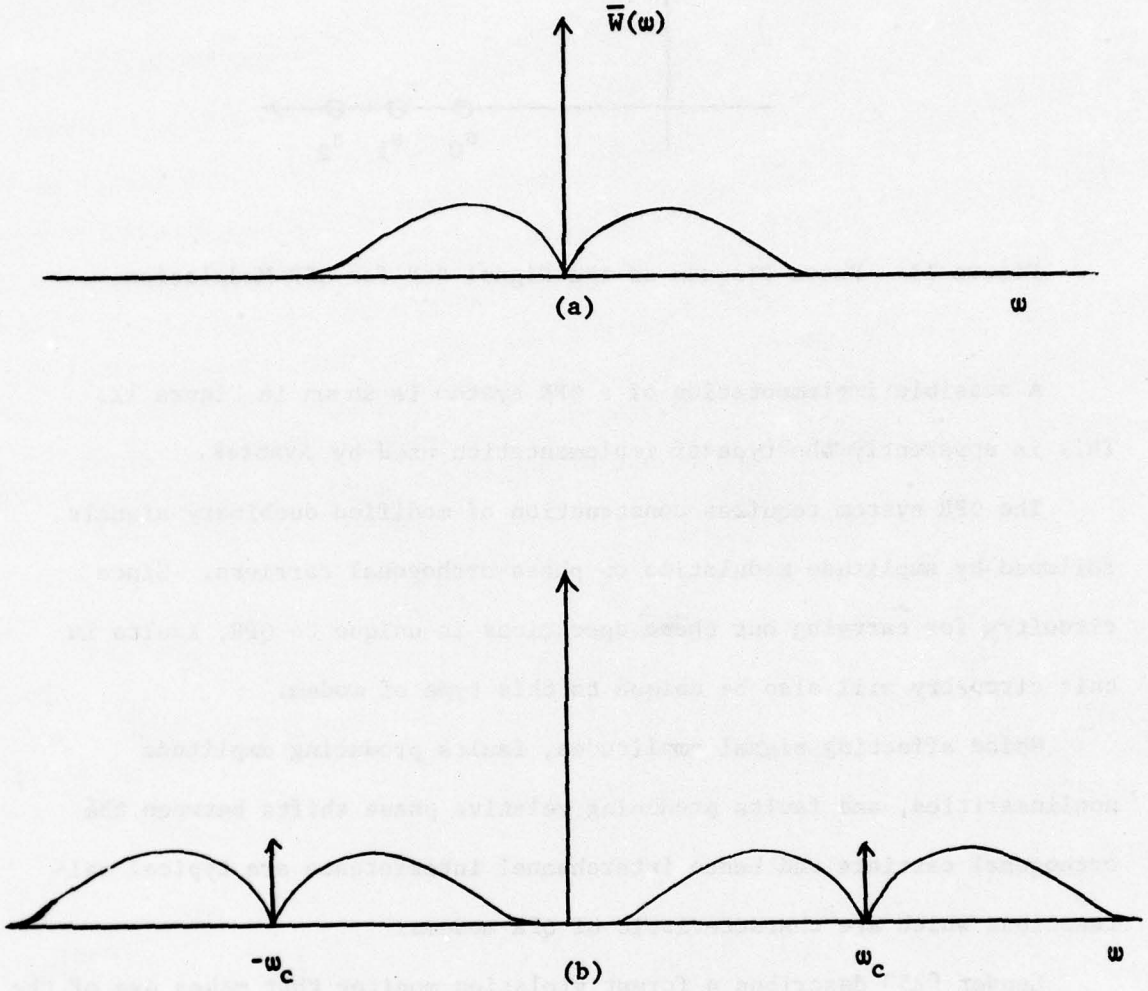


Figure 10 Spectra of Modified Duobinary Waveforms

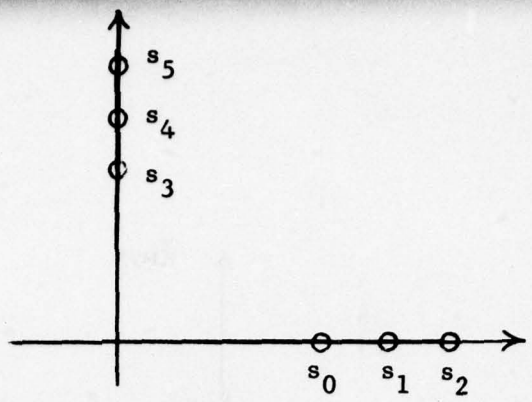


Figure 11 Phase Diagram of the Signal Set for QPR Modulation

A possible implementation of a QPR system is shown in Figure 12. This is apparently the type of implementation used by Avantek.

The QPR system requires construction of modified duobinary signals followed by amplitude modulation on phase-orthogonal carriers. Since circuitry for carrying out these operations is unique to QPR, faults in this circuitry will also be unique to this type of modem.

Noise affecting signal amplitudes, faults producing amplitude nonlinearities, and faults producing relative phase shifts between the orthogonal carriers and hence interchannel interference are typical malfunctions which are characteristic of QPR modems.

Lender [25] describes a format violation monitor that makes use of the particular type of correlation used with the modified duobinary signal. Apparently this type of monitor will function in much the same manner as the format violation monitors studied for 3 and 7-level partial response signals.

A pseudo-error type monitor, using amplitude bands about each of the three thresholds for each of the modified duobinary signals, seems to be a feasible possibility. There is no apparent reason why the Received Signal

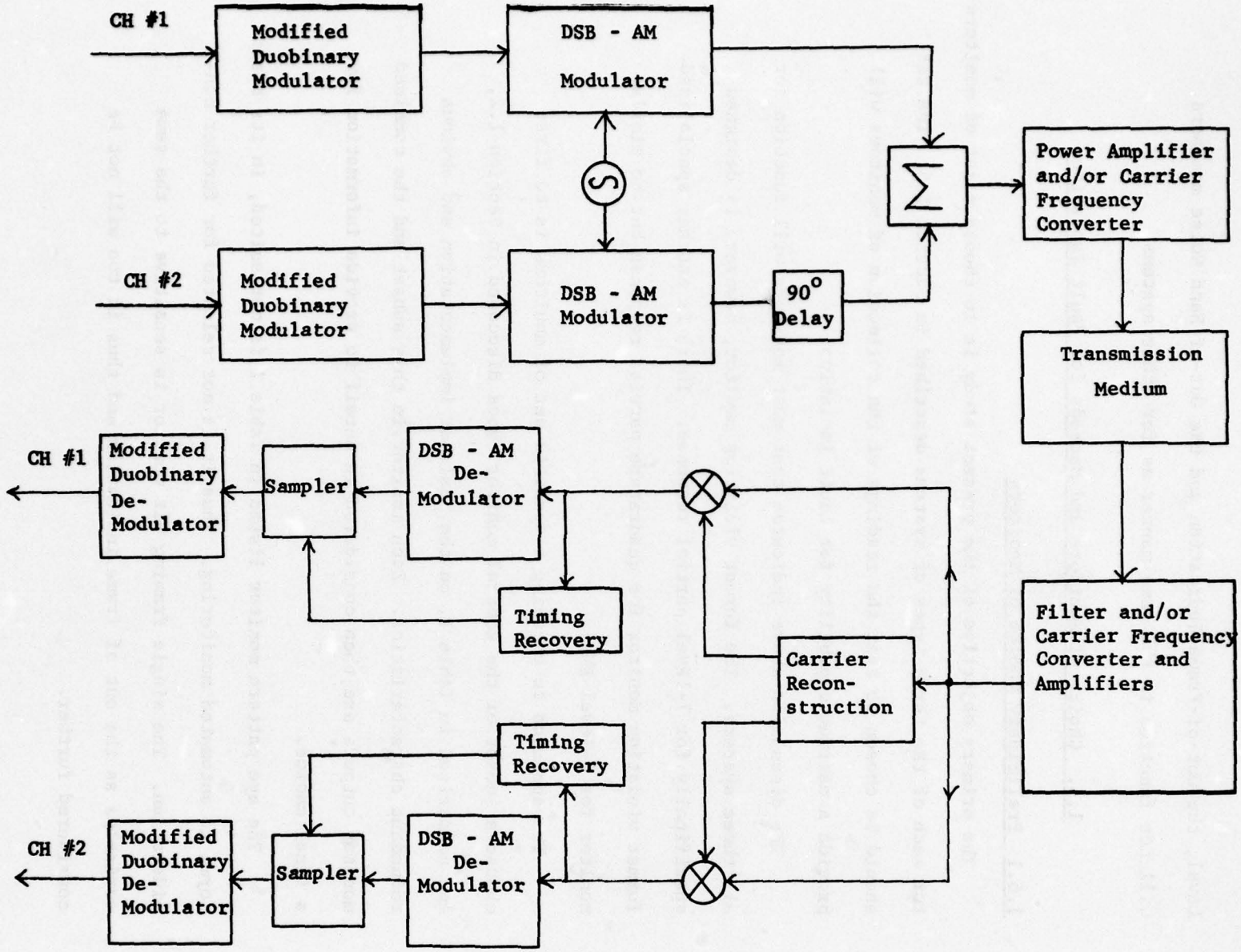


Figure 12 A Possible Implementation of a QPR System

Level, the Out-of-Frame Indication and the Out-of-Band Noise monitors will not function in the same manner as for other systems.

1.6. Choice of Monitors and Methods for Fault Isolation

1.6.1 Preliminary Choice of Monitors

The primary objective of the present study is to choose a set of monitors for each of the three types of systems described in Section 1.5. The set should be chosen so that the readings of the collection of monitors will provide a maximum capability for fault isolation.

The discussion above indicates that most monitors will function for all three systems. The format violation monitor, however, is designed specifically for 7-level partial response. There is another specialized format violation monitor for quadrature partial response but no similar monitor for 4-level FM.

The approach to choosing a specific set of monitors is to first choose a subset of the general monitor types discussed in Section 1.2, and summarized in Table 1, on the basis of implementation and obvious redundant characteristics. Each monitor in this subset and the combined monitor outputs are then considered in detail to provide information for a final choice.

The eye pattern monitor listed in Table 1 is not suited, in its basic form, to automated monitoring. Thus it is not selected for further consideration. The single framing bit monitor is sensitive to the same variables as the out of frame indication and thus it too will not be considered further.

A monitor based on the introduction of a parity bit requires the addition of overhead bits to the bit stream as well as circuitry for carrying out the parity check. Because of the need for the introduction of additional bits, this monitor is not directly comparable to others under consideration and it will not be considered further in this part of the study.

The monitor types which are studied in detail are identified as:

- out-of-band noise monitor
- out-of-frame indication
- received signal level
- pseudo-error
- partial response format violation with indications greater than 3 and greater than 7

1.6.2 Analysis of Monitor Responses

The response of each monitor to each of the faults listed on pages 11 and 12 can be determined and catalogued.

The out-of-band noise monitor responds only to noise or signal energy in the narrow bandwidth of the out-of-band noise filter. Thus an examination of the fault list shows that readings are low for all faults but fault (2) which is produced by high noise power. The readings of this monitor are listed in Tables 4, 5, and 6.

The out-of-frame monitor will indicate "yes" when there is an error in the frame bits in a specified number of successive frames. Consideration of the Signal Subsystem faults indicates that, since a signal-to-noise or signal-to-interference ratio low enough to cause a large number of errors is assumed for faults (1), (2), and (4), these will cause successive frame bit errors. Similarly, fault (3), loss of signal will cause an

Table 4 Monitor Responses to Faults in the Signal Subsystem

Fault	Monitor					
	Out-of-Band Noise	Pseudo-Error	Format Violation Greater Than 3	Format Violation Greater Than 7	Out-of-Frame	Signal Power
(1) Low S/N due to low signal power, normal noise power	L	H	H	L	Yes	L
(2) Low S/N due to normal signal power, high noise power	H	H	H	L	Yes	H
(3) Loss of signal	L	H	H	H	Yes	L
(4) Additive interference in band	L	H	H	L	Yes	H
(5) Loss of one signal at multiplex output	L	M	M	L	No	M
Legend: L - Low, M - Medium, H - High						

Table 5 Monitor Responses to Faults in the Frame Synchronization Subsystem

Fault	Monitor					
	Out-of-Band Noise	Pseudo-Error	Format Violation Greater Than 3	Format Violation Greater Than 7	Out-of-Frame	Signal Power
(6) Loss of frame sync	L	L	L	L	Yes	H
(7) Loss of bit integrity - multi-level analog signal	L	L	H	H	Yes	H
(8) Loss of bit integrity at multiplex output	L	L	L	L	Yes	H
Legend: L - Low, M - Medium, H - High						

Table 6 Monitor Responses to Faults in the Bit Synchronization Subsystem

Fault	Monitor					
	Out-of-Band Noise	Pseudo-Error	Format Violation Greater Than 3	Format Violation Greater Than 7	Out-of-Frame	Signal Power
(9) Loss of bit sync	L	H	H	H	Yes	H
(10) Small bit sync jitter	L	M	M	L	No	H
(11) Large bit sync jitter	L	H	H	M	Yes	H
Legend: L - Low, M - Medium, H - High						

out-of-frame indication. The loss of one signal to a multiplex, fault (5), will decrease the signal power and hence increase the AGC gain, which in turn amplifies the noise. It seems reasonable, however, that this increase in the noise will not cause an out-of-frame indication.

Each of the faults in the Frame Synchronization Subsystem result in a loss of bit integrity which interferes with the framing bits and causes an out-of-frame indication. Faults (9) and (11) in the bit synchronization subsystem produce a sufficiently large number of bit errors to cause an out-of-frame indication; while fault (10), which causes only a few errors, does not. These results are listed in the tables.

The implementation of a received signal level monitor chosen is a measure of signal power. Three faults, namely: (1), (3), and (5) cause lower than normal readings of this monitor. The reasoning seems obvious for this case and the results are listed in the tables.

The pseudo-error monitor functions by indicating a count any time a sample of the multilevel analog signal lies in a specified band about the slicer levels. A 7-level partial response signal, which is typical of multilevel signals, is shown in Figure 13. The normal sampling times, the slicer levels and the pseudo-error bands are shown in the figure.

Faults in the signal subsystem all have the effect of changing the signal-to-noise or signal-to-interference ratio. Faults (2) and (4) are caused by an increase of either noise or interference power. Faults (1), (3), and (5) are caused by a decrease in signal power which, through AGC action, indirectly increases noise power. Examination of Figure 13 shows that an increase in noise power, which adds a noise voltage to the noise-free signal shown, causes a reasonable probability that a sample of signal plus noise will be in a pseudo-error band. Thus for the signal

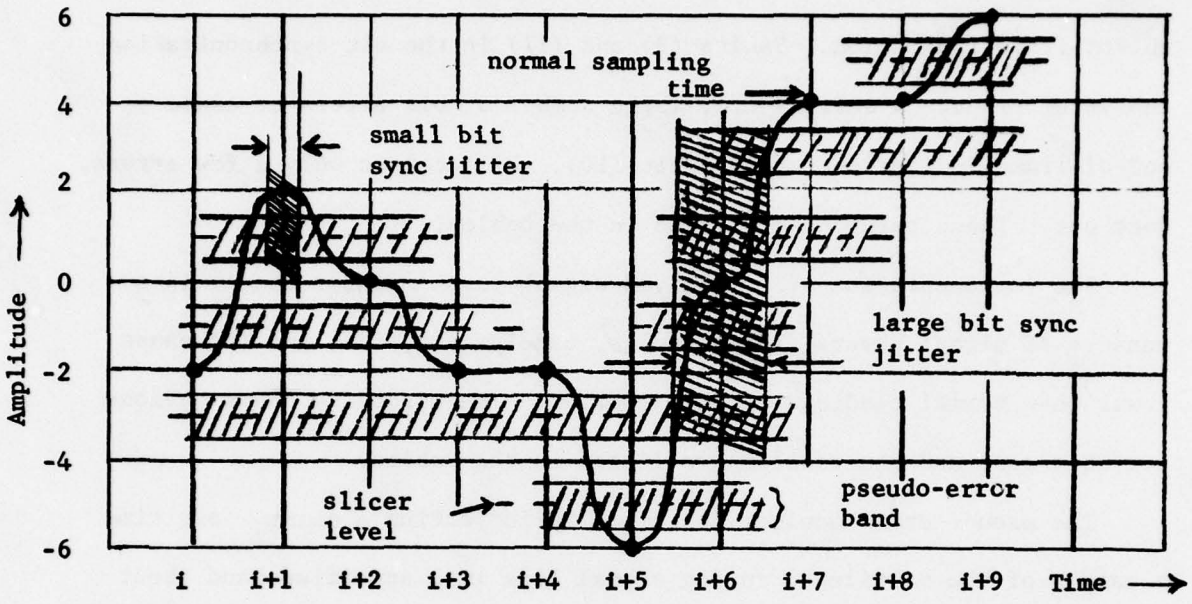


Figure 13 A Typical Multilevel Signal with Information Concerning Monitors and Faults

subsystem faults the pseudo-error monitor will read high. A loss of one signal to a multiplex, fault (5), causes less increase in AGC gain and hence less effective noise than complete loss of signal and thus the pseudo-error reading for fault (5) will be termed medium. These readings are indicated in the tables.

To consider the effect of faults in the bit synchronization subsystem, regions of shift in sampling time corresponding to large and small bit sync jitter are shown in Figure 13. Actual samples of the analog signal will occur at random positions within the shaded areas. Note that small bit sync jitter (with no other errors) will infrequently cause an amplitude sample within the pseudo-error band and hence a medium reading is assigned. On the other hand, a large bit sync jitter gives a substantial probability of an amplitude sample occuring in the pseudo-error band so that a high reading is assigned.

A complete loss of bit sync allows samples of the amplitude waveform to occur at completely random times. Thus the probability of a pseudo-error reading is essentially the ratio of the time during which the signal is within a pseudo-error band to the time of observation. This gives a high pseudo-error reading, as indicated with the other two cases in Table 6.

Faults in the frame synchronization subsystem do not produce pseudo-error and hence the readings for this case are low.

The final monitor of interest is the format violation monitor which is discussed in detail in Section 1.4 of the report. It is shown in Section 1.4 that errors between adjacent levels in the 7-level signal cause a format violation monitor reading greater than 3 but typically less than 7. On the other hand, perturbations causing errors larger than the difference between adjacent levels will typically cause a monitor reading greater than 7.

Consideration of faults in the signal subsystem thus leads to the conclusion that the effective noise produced by faults (1)-(4) will cause high readings of the greater than 3 monitor since the noise is sufficient to cause a number of adjacent level errors. A complete loss of signal, however, is the only fault that will cause a sufficient effective noise level (after action of the AGC) to produce errors between other than adjacent levels. Thus the greater than 7 monitor indicates low for faults (1), (2), and (4) and high for fault (3). Loss of one signal to a multiplex will cause some adjacent level errors but few if any errors of a larger magnitude. Thus a medium reading for fault (5) is indicated in Table 4 for violations greater than 3 and a low reading for faults greater than 7.

Faults in the frame synchronization subsystem due to loss of frame sync, fault (6) and loss of bit integrity due to pulse stuffing, fault (8), do not appreciably affect the 7-level signal and thus both format violation monitors read low for the faults. On the other hand, loss of bit integrity at the multilevel (7-level) signal, fault (7), for example a double sampling of the same level or failing to sample a level, can cause a sequence of samples which violate the required correlation properties and produce either adjacent level errors or larger errors. Thus for this case both monitors read high.

Faults in the bit synchronization subsystem due to loss of bit sync, fault (9), and large bit sync jitter, fault (11), both cause a reasonably large number of adjacent level errors and hence high readings of the greater than 3 monitor. Loss of bit sync can also cause a large number of errors greater than between adjacent levels while large bit sync jitter will likely cause a few such errors. Thus high and medium readings are assigned respectively to these faults in Table 6. Finally, small bit sync

jitter, fault (10), causes a few adjacent level violations but none larger, so that medium and low are the appropriate monitor responses.

1.6.3 Fault Isolation

The readings of the six monitors can be considered as a fault profile which provides for fault isolation. With this in mind, the monitor readings for the eleven generic faults treated above are collected in Table 7 so that each now is the profile for one fault condition. The faults are arranged so as to place in proximity the largest number of similar profiles.

A study of this table reveals that two faults, loss of frame synchronization (6) and loss of bit integrity at a mutliplex output (8), have identical profiles and hence cannot be distinguished with the collection of monitors under consideration. On the other hand, all other fault profiles differ in the reading of at least one monitor thus allowing for fault isolation between the ten generic faults.

It is useful to identify from the table those profiles which differ in only one monitor reading. The group of fault pairs which differ in this way are listed in Table 8 along with the monitor whose reading distinguishes the two. Note that any monitor not necessary to distinguish any pair of faults is not essential in the fault isolation process.

On this basis, the out-of-frame indication and the format violation greater than 3, might be eliminated leaving the following monitors:

out-of-band noise
signal power
pseudo-error
format violation greater than 7.

This group of four monitors will uniquely identify nine out of the eleven generic faults under consideration. The two faults which cannot be distinguished from each other are, however, discriminated from the other nine.

Table 7 Fault Profiles for Eleven Faults with Six Monitors

Legend: L - Low, M - Medium, H - High / FAULT	Monitor	Out-of-Band Noise	Out-of-Frame Indication	Signal Power	Pseudo-error	Format Violation Greater Than 3	Format Violation Greater Than 7
(2) Normal signal high noise		H	Yes	H	H	H	L
(3) Loss of signal normal noise		L	Yes	L	H	H	H
(1) Low signal normal noise		L	Yes	L	H	H	L
(4) High additive interference		L	Yes	H	H	H	L
(9) Loss of bit synchronization		L	Yes	H	H	H	H
(7) Loss of bit integrity at multilevel analog signal		L	Yes	H	L	H	H
(11) Large bit sync jitter		L	Yes	H	H	H	M
(6) Loss of frame synchronization		L	Yes	H	L	L	L
(8) Loss of bit integrity at multiplex output		L	Yes	H	L	L	L
(5) Loss of one signal at multiplex output		L	No	M	M	M	L
(10) Small bit sync jitter		L	No	H	M	M	L

Table 8 Faults Whose Profiles Differ by One Monitor Reading

Fault Pair	Monitor Distinguishing the Two Faults
High additive interference (4)/ loss of bit sync (9)	Format violation greater than 7
High additive interference (4)/ large bit sync. jitter (11)	Format violation greater than 7
Loss of bit sync (9)/ large bit sync. jitter (11)	Format violation greater than 7
Loss of bit sync (9)/ loss of bit integrity at multilevel analog signal (7)	Pseudo-error
Normal signal high noise (2)/ high additive interference (4)	Out-of-band noise
Loss of one signal at a multiplex output (5)/ small bit sync jitter (10)	Signal power
Loss of bit sync (9)/ loss of signal normal noise (3)	Signal power
Low signal normal noise (1)/ high additive interference (4)	Signal power
Low signal normal noise (1)/ loss of signal normal noise (3)	Format violation greater than 7

Unfortunately, the particular type of format violation monitor giving the greater than 7 reading can be used only with seven-level partial response. Without the use of this monitor, the remaining thee monitors distinguish four individual faults, two pairs of faults and one group of three faults. The fault groupings between which discrimination is possible are: faults 2, 5, 7, 10, 1/3, 6/8, 4/9/11.

SECTION II

HYBRID SIMULATION OF DIGITAL SYSTEMS OVER ANALOG LINKS

2.0 Introduction

The previous task on the subject contract, examining the monitoring of digital communication links, investigated the properties of several monitoring schemes for use in conjunction with a 3-level partial response type of signaling system. The primary purpose of the study was to investigate the steady state properties of several proposed monitoring schemes. This was done using Purdue University's hybrid computer laboratory to simulate a digital link consisting of VICOM's time division multiplex (TDM) baseband equipment which uses class 1 partial response signaling over Philco-Ford LC-4 and LC-8 microwave radios together with a Motorola MR-300 microwave radio. The results of this study are discussed in detail in an earlier report [9].

In order to use this work to maximum advantage, it was decided to expand the performance monitoring study to include a 7-level partial response system which could employ the basic link, transmitter and receiver simulations developed in the previous study of the 3-level partial response system. The implementation of the 7-level system required the addition of input and output processing circuitry to accept data at a data rate which was equal to twice the input data rate for the 3-level system. In achieving this performance, it was necessary to design a binary to quaternary converter to provide an input to the partial response filter. This also allows the simulation of a basic four-level FM data link by simply removing the partial response filters from the 7-level partial response simulation.

2.1 The 3-Level Partial Response System

In order to make this report self-contained, the descriptions of the portions of 3-level partial response simulation which are of use in the present study will be repeated. Figure 14 shows the block diagram of the 3-level partial response system. A CDC 1700 digital computer is used to provide a random data source together with a stable clock for the input and delay line circuitry. In addition, the CDC 1700 performs the task of accummulating and sorting all of the performance data provided by the performance monitors. The real time simulation of the processing circuitry allows much more rapid data acquisition than would be possible with a strictly digital simulation. The partial response filters, channel simulation and receiver subsystem of the 3-level simulation are used where appropriate in the 7-level partial response and the 4-level FM simulations. Before discussing their application in the multilevel system, these modules will be described in the context of the 3-level partial response simulation with appropriate comments as to how their use differs in the other simulations.

2.1.1 Random Number Generator

The multiplexed bit stream is simulated by calling a pseudo-random number generation routine which returns a random number uniformly distributed on [-32767, 32767]. A random bit sequence is obtained by extracting the low order bit of this integer. The measured statistics of this signal are:

$$P\{1\} = \frac{1.0642719 \times 10^6}{2.1299195 \times 10^6} = 0.49968$$

$$P\{0\} = \frac{1.0656476 \times 10^6}{2.1299195 \times 10^6} = 0.50032 \ .$$

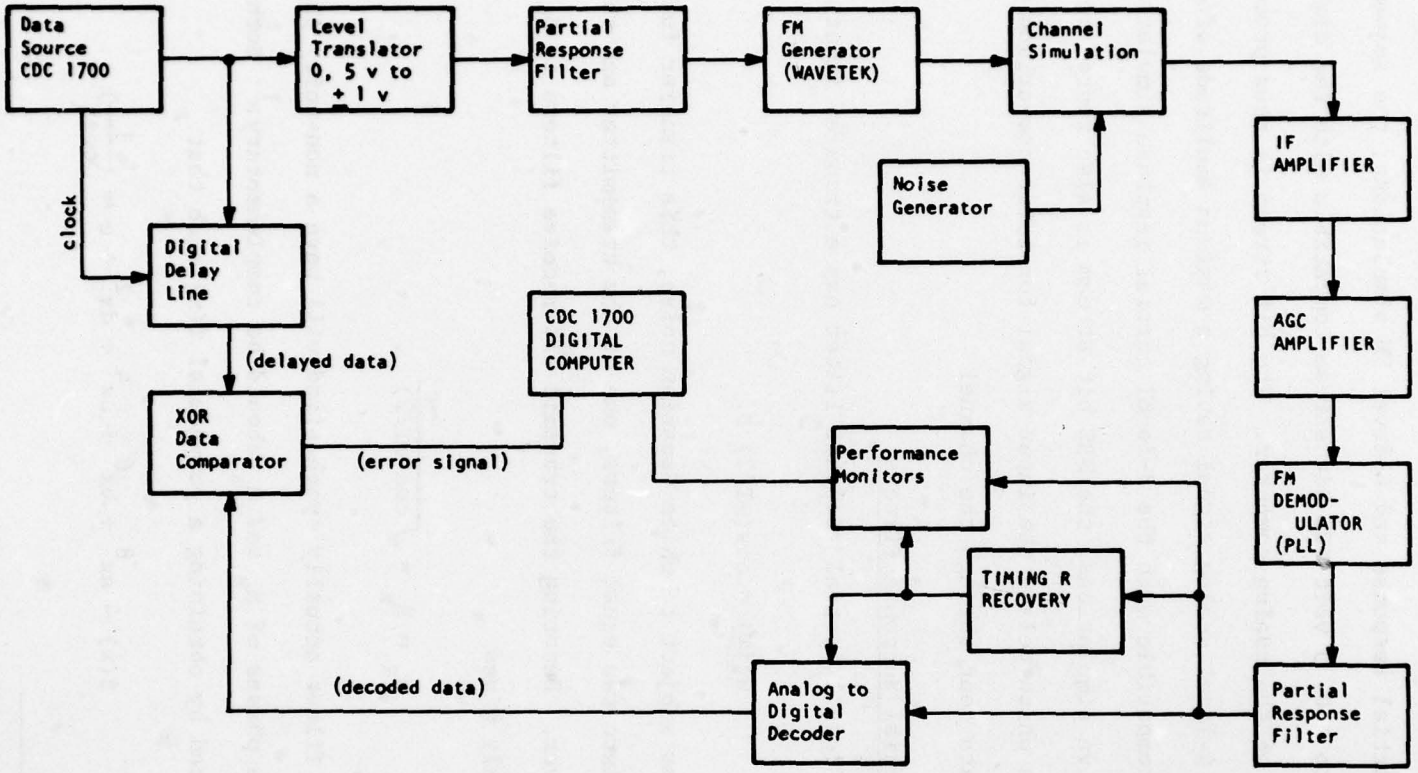


Figure 14 Block Diagram of 3-Level Partial Response System

A random bit from this sequence is transferred to the analog computer once every T seconds. In the 3-level partial response simulation, this sequence is converted to a NRZ polar bit stream with amplitude of ±1 volts. For the 7-level partial response and 4-level FM simulations, the sequence is converted into a 0, 5 volt NRZ bit stream compatible with the digital hardware available on the analog computer. The bit stream is then processed to provide a 4-level analog signal having a maximum amplitude of ±1 volt so as to be compatible with the 3-level partial response simulation. In each of the above simulations, the NRZ bit stream is also routed to a digital delay line which delays the input signal for later comparison with the decoded data sent through the channel.

2.1.2 Partial Response Filters

The Class 1 partial response filter has a transfer function given by

$$H(j\omega) = \cos(\omega T/2) \quad . \tag{33}$$

For systems subject to white Gaussian noise, this transfer function should be split into two equal filters, one at the transmitter and the other at the receiver. Denoting the transmit and receive filters by H_x and H_R respectively gives

$$H_R = H_x = \sqrt{\cos(\omega T/2)} \quad .$$

Since any filter actually synthesized will have a non-unity phase characteristic, the phases of H_R and H_x should be complementary.[1] Both filters were approximated by obtaining a polynomial f(x) such that

$$f(x) = ax^8 + bx^6 + cx^4 + dx^2 + e \approx \left(\frac{1}{\cos x}\right)$$

[1] Note that perfectly complementary filters would require one of the filters to be unstable. Hence, some compromise is required.

where x is a normalized variable such that $0 \leq x \leq \pi/2$. The coefficients are obtained by evaluating f(x) at x = 0, $\pi/8$, $\pi/4$, $3\pi/8$, and $\pi/2$. Since

$$|H_x(s)|^2 \Big|_{s = j\omega} = \frac{1}{f(\omega)}$$

the transfer function is easily shown to be

$$H_x(s) = \frac{3.25104}{s^4 + 4.3966s^3 + 9.2883s^2 + 8.1050s + 3.25104}$$

Noting that

$$|H_x(j\omega)|^2 \cdot |H_R(j\omega)|^2 = \cos^2(\omega T/2)$$

gives the receiver's partial response filter transfer function

$$H_R(s) = \frac{17.149}{s^4 + 16.8954s^3 + 33.5581s^2 + 35.8009s + 17.149}$$

The realizations of the filter transfer functions are given in Figures 15 and 17 for the transmit and receive filters respectively. For the simulation, these transfer functions must be scaled to 2/T = 900.00 for a 450 baud rate. For the 7-level partial response simulation, the filters may also be scaled to accommodate a 5-baud rate. This is accomplished by the selection of pushbutton number 5 on console 1. Reference [9] gives plots of the above transfer function together with a more complete analysis.

2.1.3 FM Modulator

The FM modulator consists of a Wavetek Model 136 voltage controlled oscillator with an input sensitivity of 4.0 kHz per volt. As shown in Figure 15, the modulation index is a function of the setting of 1P08. The oscillator output is set to have a peak amplitude of 0.75 volts.

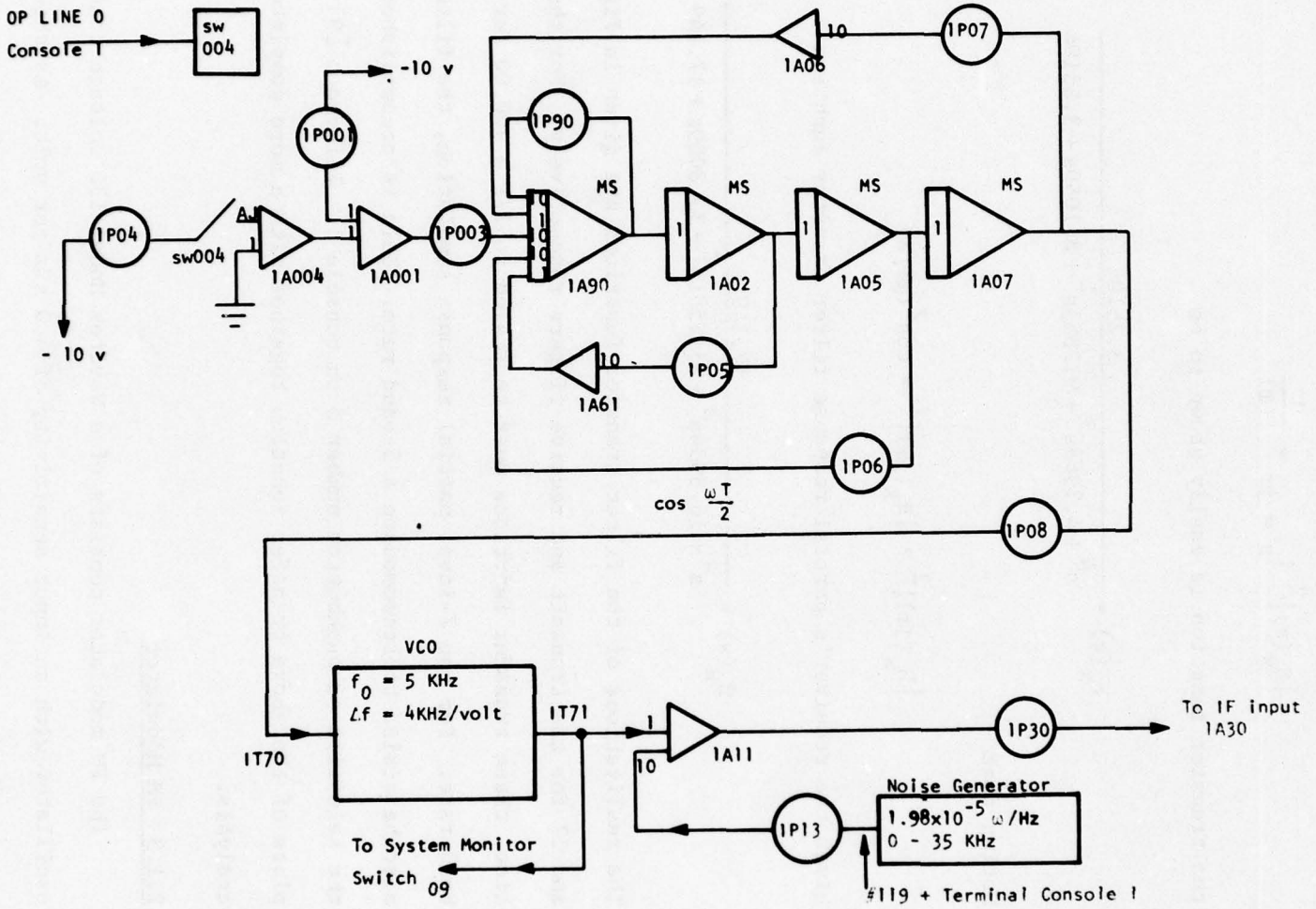


Figure 15 3-Level Partial Response Input D/A, Partial Response Filter and Link Simulations

2.1.4 Channel Simulation

The effects of a non-ideal channel are simulated by the addition of Gaussian noise or other phenomena to the modulated carrier at 1A11. The noise generator used for simulating a noisy channel is a true, zero mean Gaussian noise generator with an output of 1.17 v RMS and a power spectral density of 3.11×10^{-6} watts/rad. over a two-sided bandwidth of 70 kHz. The noise generator is attenuated by 1P13 to vary the actual signal to noise ratio in the channel. With 1P13 of Figure 15 set to 0.33, the carrier to noise ratio (C/N) at the output of the IF filter is 0 dB.

2.1.5 IF Filter

The carrier plus noise is transmitted from the channel (1A11) to the input of the IF amplifier given in Figure 16. The IF amplifier has a standard 6-pole Butterworth bandpass filter characteristic which is synthesized as three cascaded two-pole sections. The complete transfer function for the IF is given by

$$F(s) = \frac{s^3}{(s^2 + 0.0914s + 0.8410)(s^2 + 0.25s + 1.0)(s^2 + 0.10864s + 1.1891)} \tag{34}$$

The IF center frequency is 5 kHz with a 3 dB bandwidth of approximately 1 kHz. The equivalent noise bandwidth is $\frac{2\pi W}{3}$ rad/sec where W is the 3 dB bandwidth in radians.

2.1.6 Automatic Gain Control Stage

Since the phase-lock loop is sensitive to the amplitude of the incoming signal, an AGC stage is added between the IF amplifier and phase-lock loop demodulator. If Z(t) is the incoming signal, then the output from the AGC is given by

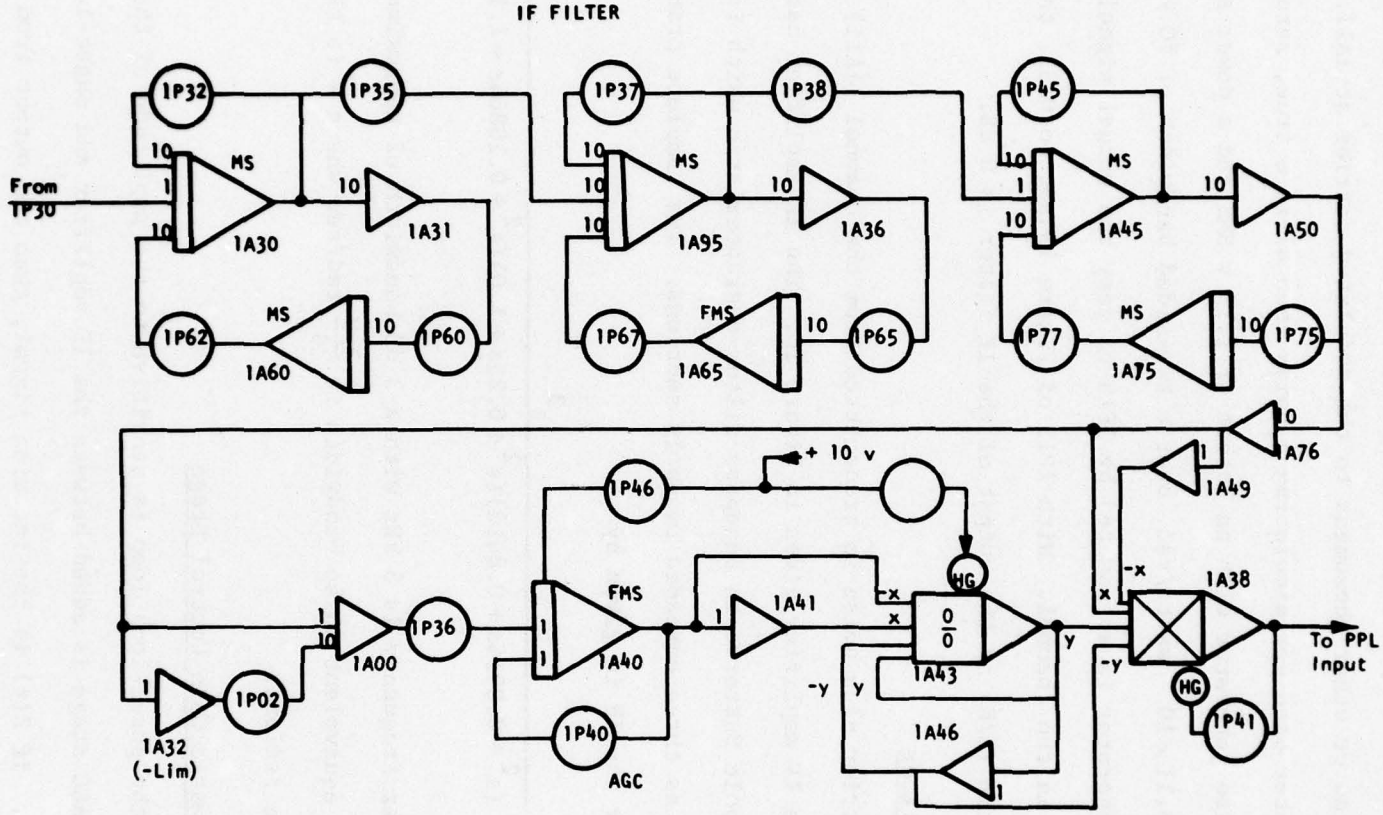


Figure 16 IF Filter and AGC Simulations

$$X(t) = 0.625 \frac{0.02\ Z(t)}{|Z(t)| * h(t)}$$

where h(t) is the impulse response of a first order lowpass filter with a time constant of 20 μsec. The AGC stage appearing in Figure 16 provides a gain of 1.26 with a nominal output voltage of 1.15 volts.

2.1.7 Phase-Locked Loop FM Demodulator

The FM signal from the AGC amplifier is demodulated by the phase-lock loop shown in Figure 17. As this circuitry has been discussed in the previous year's reports [8],[9], only a brief description will be given here.

The loop is a third order type-one loop in which the loop filter has a transfer function given by

$$G(s) = \frac{2.24 \times 10^8}{(s+2000.)(s+60000.)} .$$

The overall loop transfer function is

$$H(s) = \frac{3.29 \times 10^{12}}{s^3 + 5.2 \times 10^4 s^2 + 10^8 s + 3.29 \times 10^{12}} .$$

Next consider the noise properties of the phase-lock loop. If the input noise has a symmetrical bandpass spectral density much wider than the bandwidth of the received signal and the PLL is in its linear mode of operation, then the output signal power spectral density is

$$S_0(\omega) = \frac{12.74\ |H(j\omega)|^2}{K^2}\ S_i(\omega) \qquad (35)$$

where $S_i(\omega)$ is the baseband signal power spectral density and K is the VCO sensitivity [28]. Every simulation discussed in this report uses a fixed

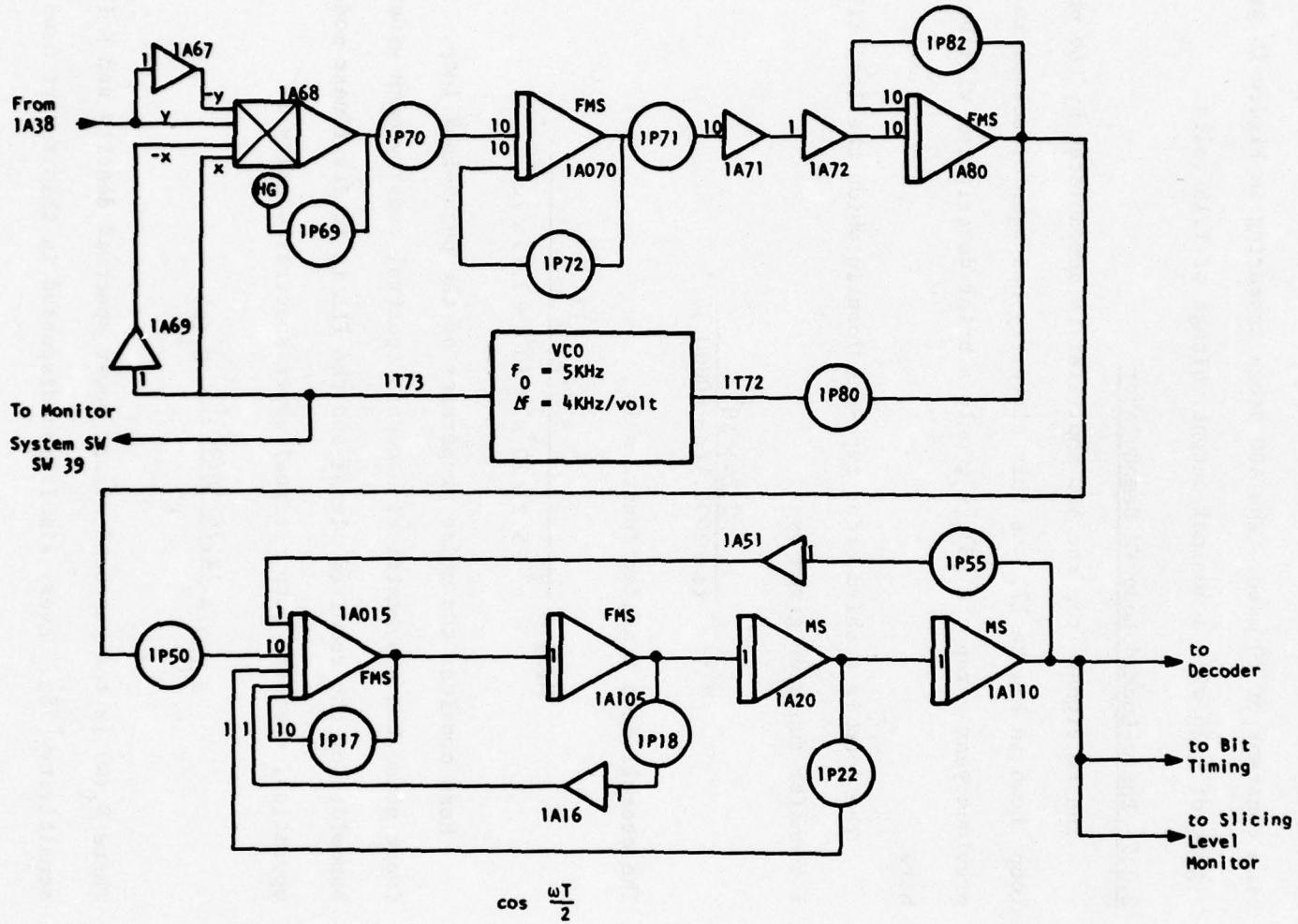


Figure 17 Phase Lock Loop Demodulator and Partial Response Filter

carrier power; hence, the signal output power is also fixed. The noise output spectral density is given by

$$N(\omega) = \frac{12.74\ |H(j\omega)|^2}{K^2}\ \eta \qquad (36)$$

where η is the power spectral density of the noise with a value

$$\eta = \frac{\eta_i A^2}{2}$$

with η_i being the power spectral density of the noise added to the carrier and A the VCO amplitude. Using the above equations, the C/N versus S/N for the PLL can be determined.

The demodulated signal is then routed to the receive partial response filter of Figure 17 before being decoded into digital a format. The remaining decoder and performance monitoring circuitry is given in Figures 18, 19, and 20. Since these modules are not used in the 7-level partial response and 4-level FM simulation, circuit descriptions are not given. Complete descriptions of the 3-level partial response simulation are available in [9].

2.2 7-Level Partial Response Simulation

The three level partial response system of Section 2.1 was designed to operate at a data rate of 1/T = 450 bps. By increasing the complexity of the input signal to the partial response filter from a binary to a quaternary signal, the overall link simulation is capable of handling a binary input data rate of 2/T bps while still transmitting a 450 baud signal over the data link. The processing of a four-level input signal by the partial response filters results in an analog signal which may have any one of seven possible states. If the maximum limits of the input signal are restrained to be that of the ±1 volt levels of the 3-level partial response

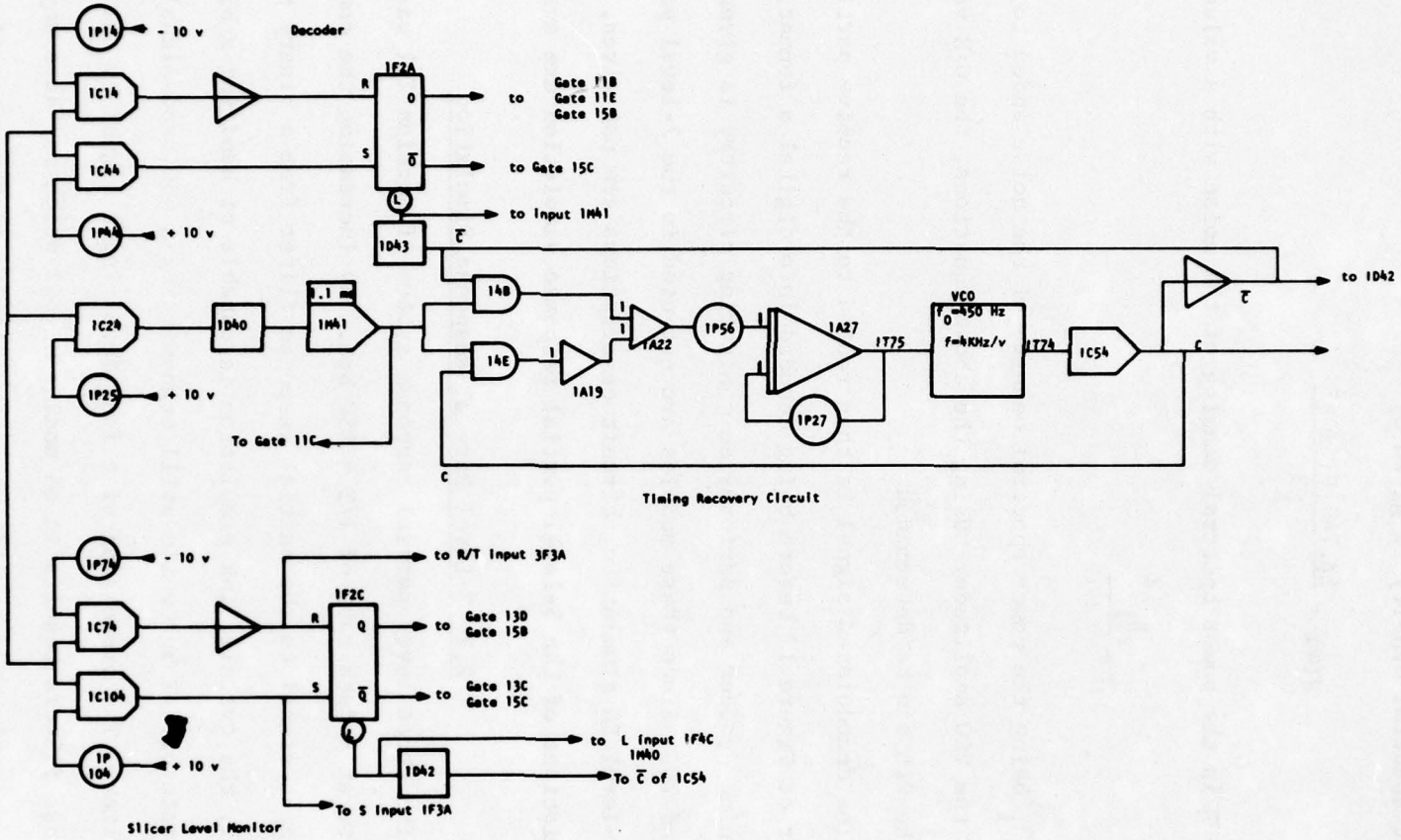


Figure 18 Performance Monitor, Timing Recovery, and Data Decoder for 3-Level Partial Response System

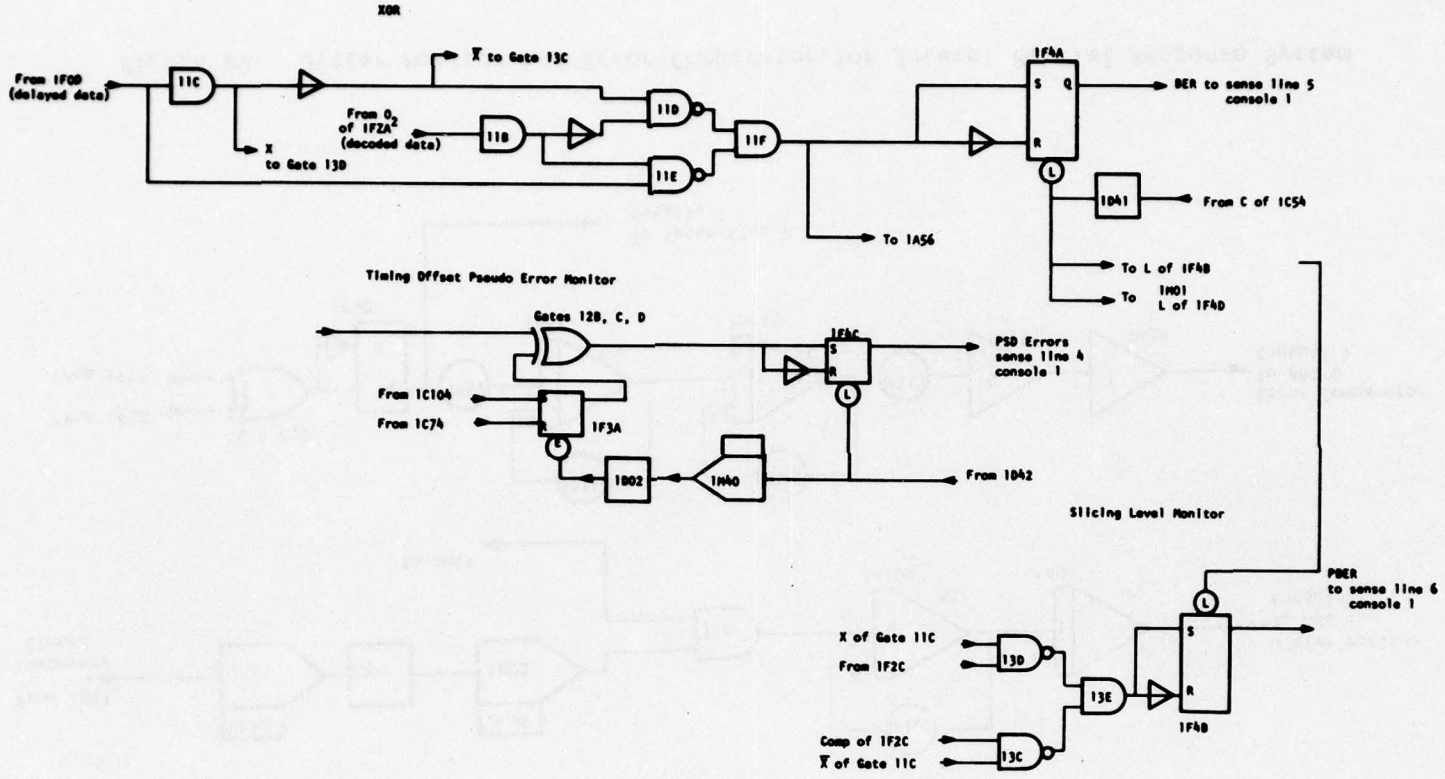


Figure 19 Bit Error Indicators and Timing Pseudo Error Monitor for 3-Level Partial Response System

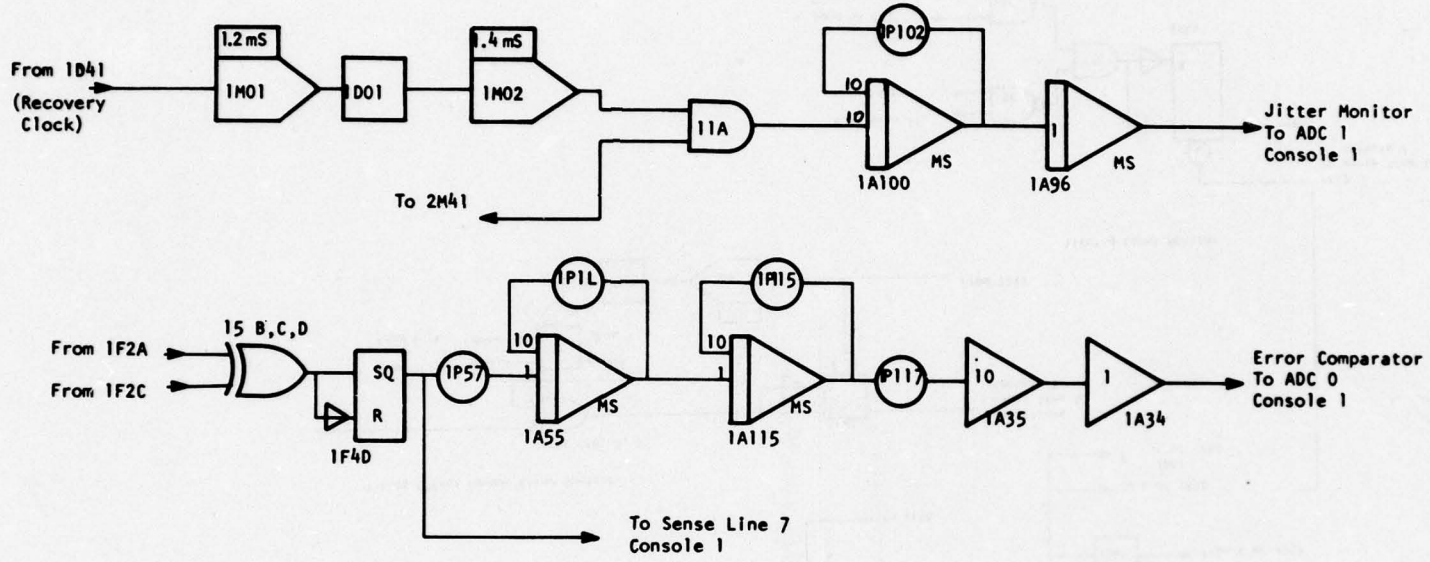


Figure 20 Jitter Monitor and Error Comparator for 3-Level Partial Response System

system, the signal to noise ratio at the receiver must be improved to compensate for the decreased level spacing. Hence, we are in effect trading system noise performance for an increase in the link data rate.

Since this study is concerned with evaluating both transient and steady state properties of performance monitors, an additional low data rate of 5 bps is included in the simulation to allow instaneous data to be displayed on a multichannel stripchart recorder.

A general block diagram of the 7-level partial response simulation is given in Figure 21. The basic link simulation consisting of the partial response filter, FM generator, channel simulation, IF and AGC amplifiers together with the PLL FM demodulator is identical to the three-level partial response simulation. In order to implement the higher data rate, however, the original linear sequences must be transformed into 2-bit codes to generate a 4-level signal for input to the partial response filters. Similarly, the system timing and final decoded binary signal must now be recovered from an analog signal having seven levels instead of three. The first group of circuitry described will discuss the programming necessary to generate the 7-level partial response signal which is sent to the FM modulator.

2.2.1 Input Timing and Binary to 4-Level Converter

In order to accept data at a rate of 2R bits per second and still transmit the data over the actual network channel at a rate of R bauds, the input information must be changed from simple binary to a more complex format. In the case of the seven-level partial response system, the binary signal is encoded into a 4-level digital signal based on the bit sequences and levels given in Table 9.

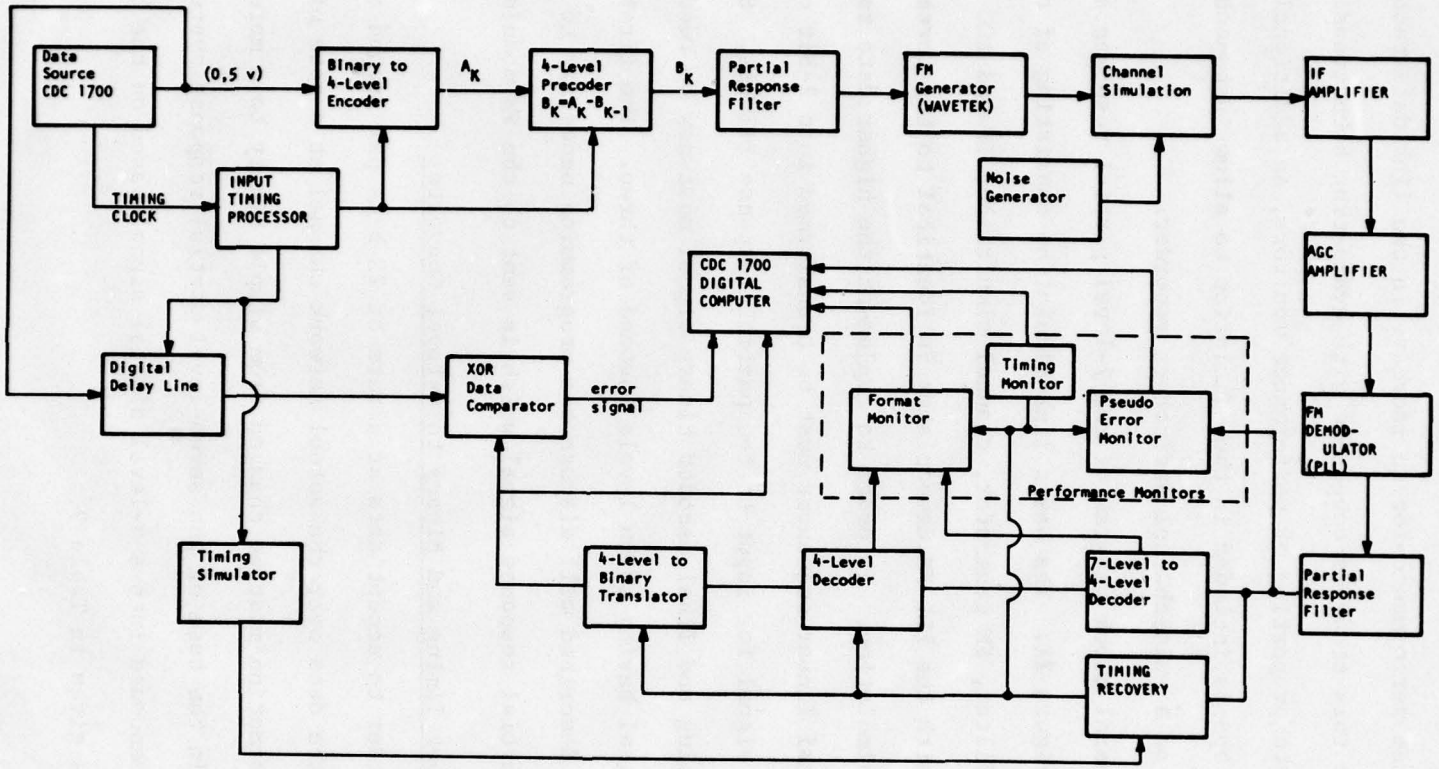


Figure 21 Block Diagram of 7-Level Partial Response System

Table 9 Encoding Format

Bit Sequence	4-Level Digital (Volts)
11	+1.0
10	+0.34
01	-0.34
00	-1.0

As shown in the above table, the limits of the 4-level signal are restrained to ±1 volt in order to be fully compatible with the simulation of the 3-level partial response system discussed earlier. In order to perform the binary to 4-level encoding operation the original input data at rate 2R must be converted into two-bit sequences, and then a 4-level signal generated at a rate of R bauds/sec.

The circuitry, as shown in Figure 22, performs three basic functions; the generation of timing signals, digital processing, and generation of the 4-level signal. Timing pulses are received from the CDC 1700 digital computer at a rate of 2R pulses per second. Comparator 2C04 provides an interface to compensate for differences in the internal clocks of the analog computers. The fast clock (2R pps) is delayed approximately 1/4 period by monostable 00 and then divided down to a slow clock rate of R pps. This provides the two timing clock rates necessary for generation of the 4-level signal, while also eliminating race problems in the digital logic. The input data from the digital computer is loaded serially at a rate of 2R bps into the shift register formed by 2F0C and 2F0D. The contents of this register are then loaded in parallel into the second register formed by 2F1C and 2F1D at the slow clock rate of R bits per second as shown in the waveforms of Figure 23. The states of flip-flops 2F1C and 2F1D then determine the status of the solid state switches 04, 34, 64, and 94 which determine the amplitude of the four-level signal at amplifier 2A01.

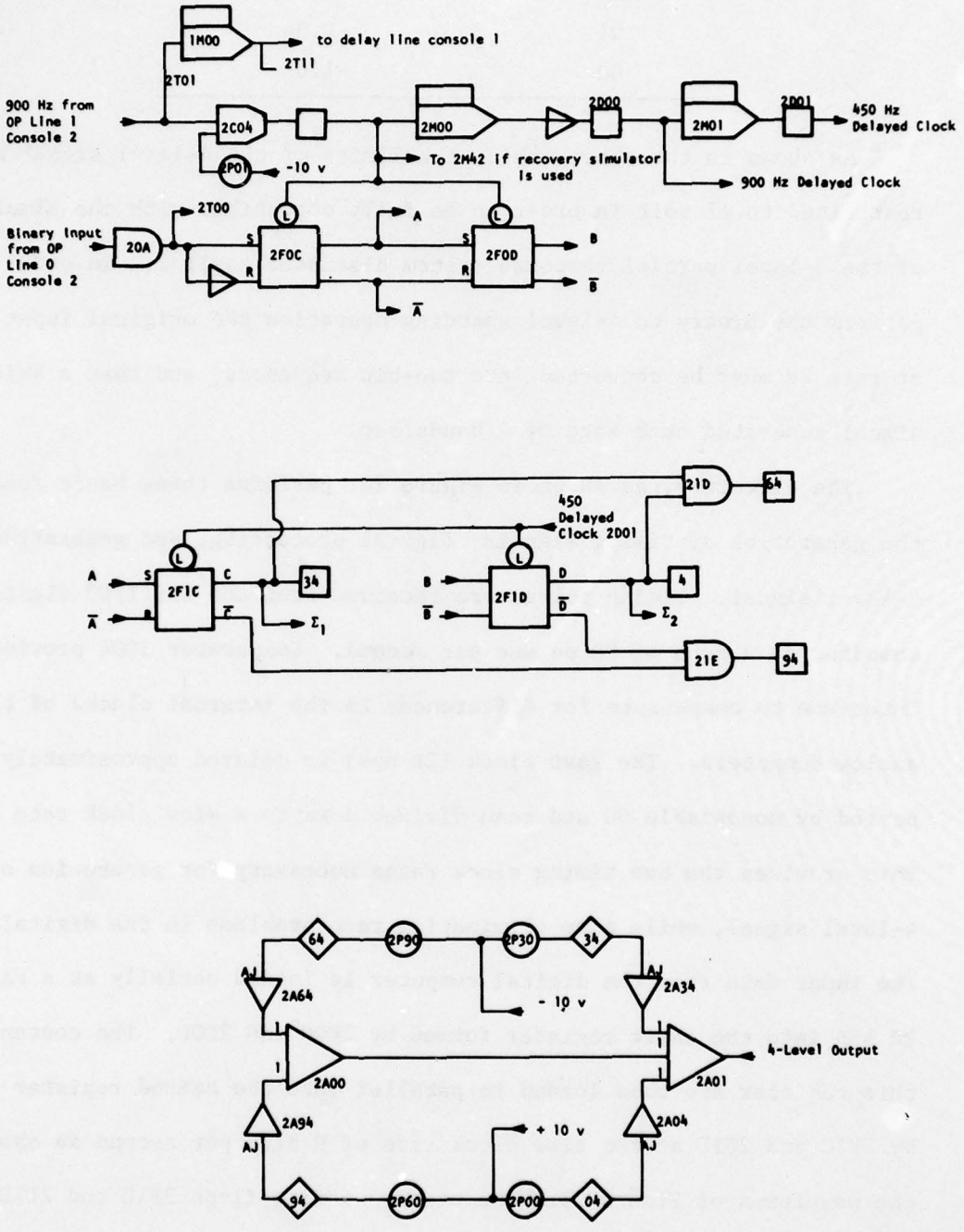


Figure 22 Input Timing Generator and Binary to 4-Level Encoder

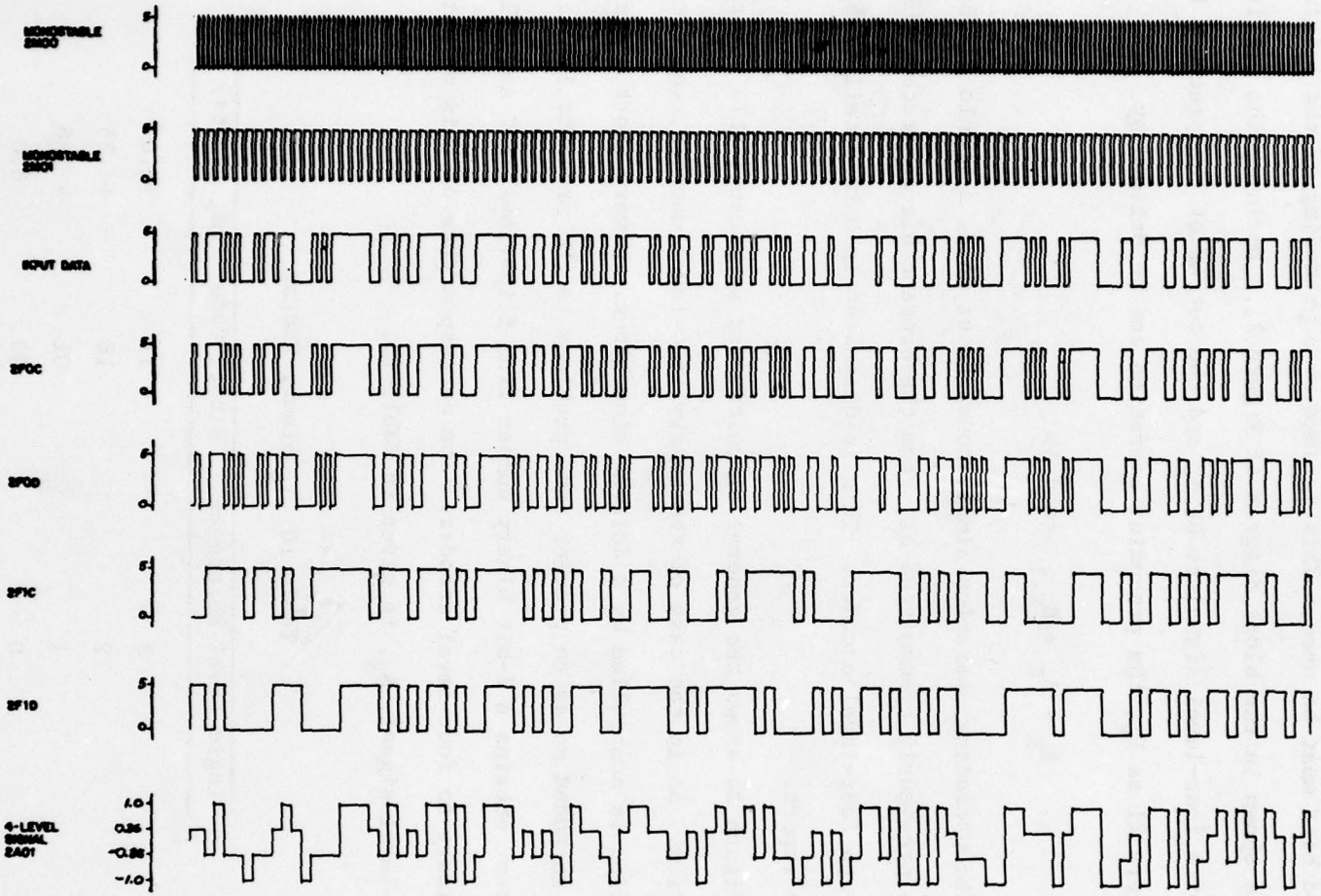


Figure 23 Timing and Binary to 4-Level Converter Waveforms

2.2.2 Data Precoder

In order to prevent the propagation of errors in a partial response system, some means of removing the system decoder's dependence on previously decoded bits must be used. This is done by a precoding of the original data as shown in the block diagram of Figure 21. Defining the original bits of a four-level signal to be A_K and the output of the precoder block of Figure 21 as B_K, the precoding operation can be defined by

$$B_K = A_K - B_{K-1} \pmod 4 \tag{37}$$

The precoding operation simply consists of doing a modulo 4 subtraction of the previously transmitted bit from the present bit generated by the binary to four-level encoder. This is discussed in more detail in Section I of the report.

Figure 24 shows the general circuitry for performing this subtraction operation. As in the case of the binary to 4-level encoder, the precoding operation is controlled by a delayed slow clock. A very short additional delay is added so as to prevent race problems in the precoder logic. The processor obtains a 2-bit binary number from flip-flops 2F1C and 2F1D of the binary to four-level encoder. The correspondence of this number to the 4-level signal, A_K, is given in Table 10.

Table 10 A_K Binary Coding

Logic Level Reference	Binary Code	A_K (Volts)
3	11	+1.0
2	10	+ .36
1	01	- .36
0	00	0.0

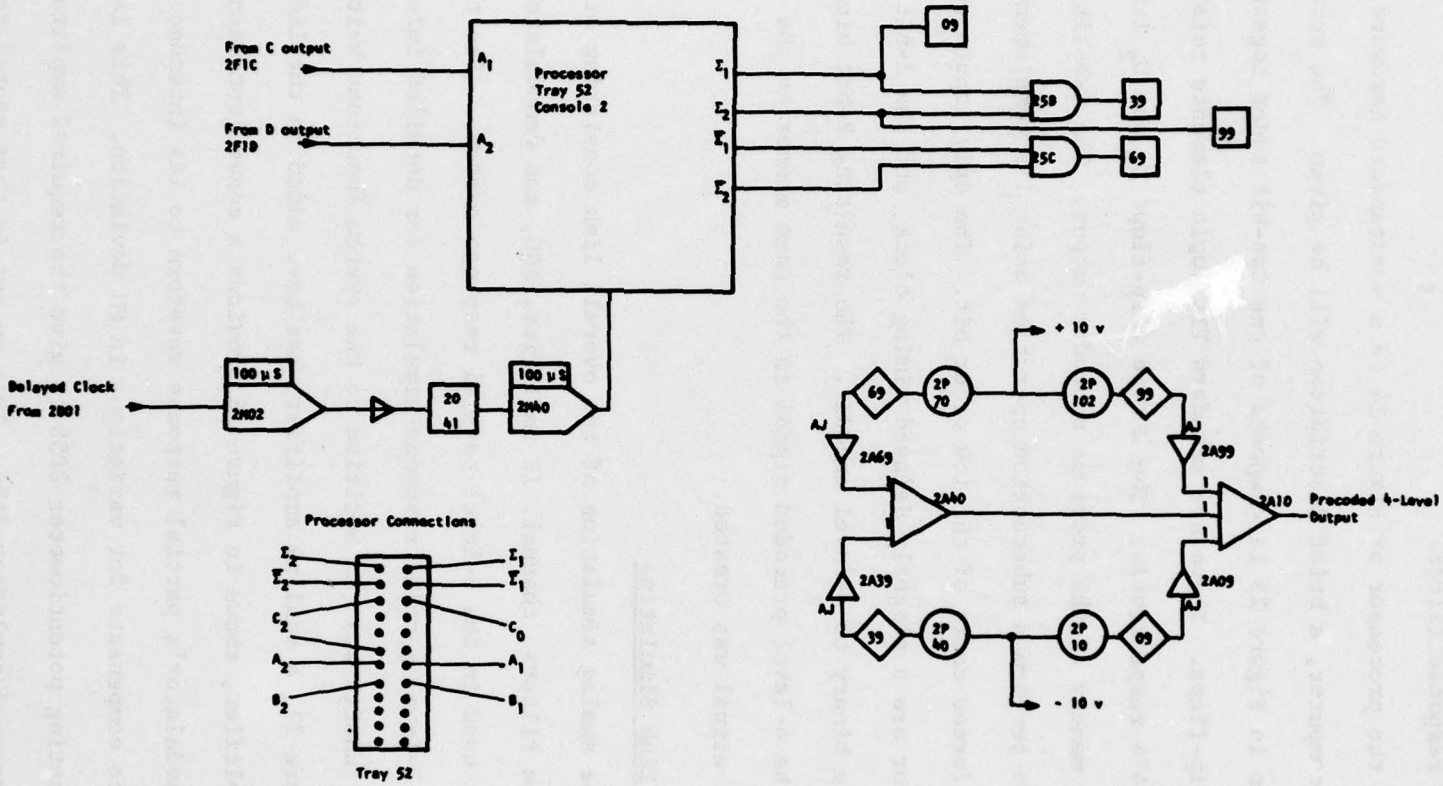


Figure 24 Input Data Precoder for 7-Level Partial Response System $[B_K = A_K - B_{K-1}]$

The processor block of Figure 24 performs the operation defined by equation (37) and generates the proper 4-level signal to be sent to the partial response filter.

As the processor of Figure 24 is a nonstandard hardware element in the analog computer, a brief description will be given. The processor circuitry as given in Figure 25 is composed of one two-bit adder together with two D type flip-flops. These are standard TTL logic elements referenced SN7482 and SN7474 respectively. The D type flip-flops D_1 and D_2 function as a one-bit memory of the previous precoder output. The two-bit adder is wired to perform a subtraction operation using 1's complement arithmetic with a forced carry of the low order bit. The only inputs required by the processor are a slightly delayed timing clock, and the 2-bit binary signal from the binary to 4-level encoder. The resulting 2-bit binary output forms the 4-level precoded signal in the same manner as the original 4-level signal was created.

2.2.3 Link Simulation

The analog simulation of the overall link consisting of the partial response filters, channel, IF amplifier, AGC, and demodulator is identical to that used in the 3-level partial response system. (See the description of the 3-level partial response simulation for detailed information on these system functions.) In addition to the system functions which are shown in Figure 21, a scaling amplifier, has been added to the link simulation. The amplifier, shown in Figure 26 provides a convenient means of adjusting the demodulator's partial response waveform to its intended maximums of ±2 volts to compensate for variations in FM deviation. This is accomplished by adjusting potentiometer 2P55 to give the required amplitude levels at the output of amplifier 2A55. This output is then routed to the performance monitors, decoder, and timing recover modules shown in Figure 21.

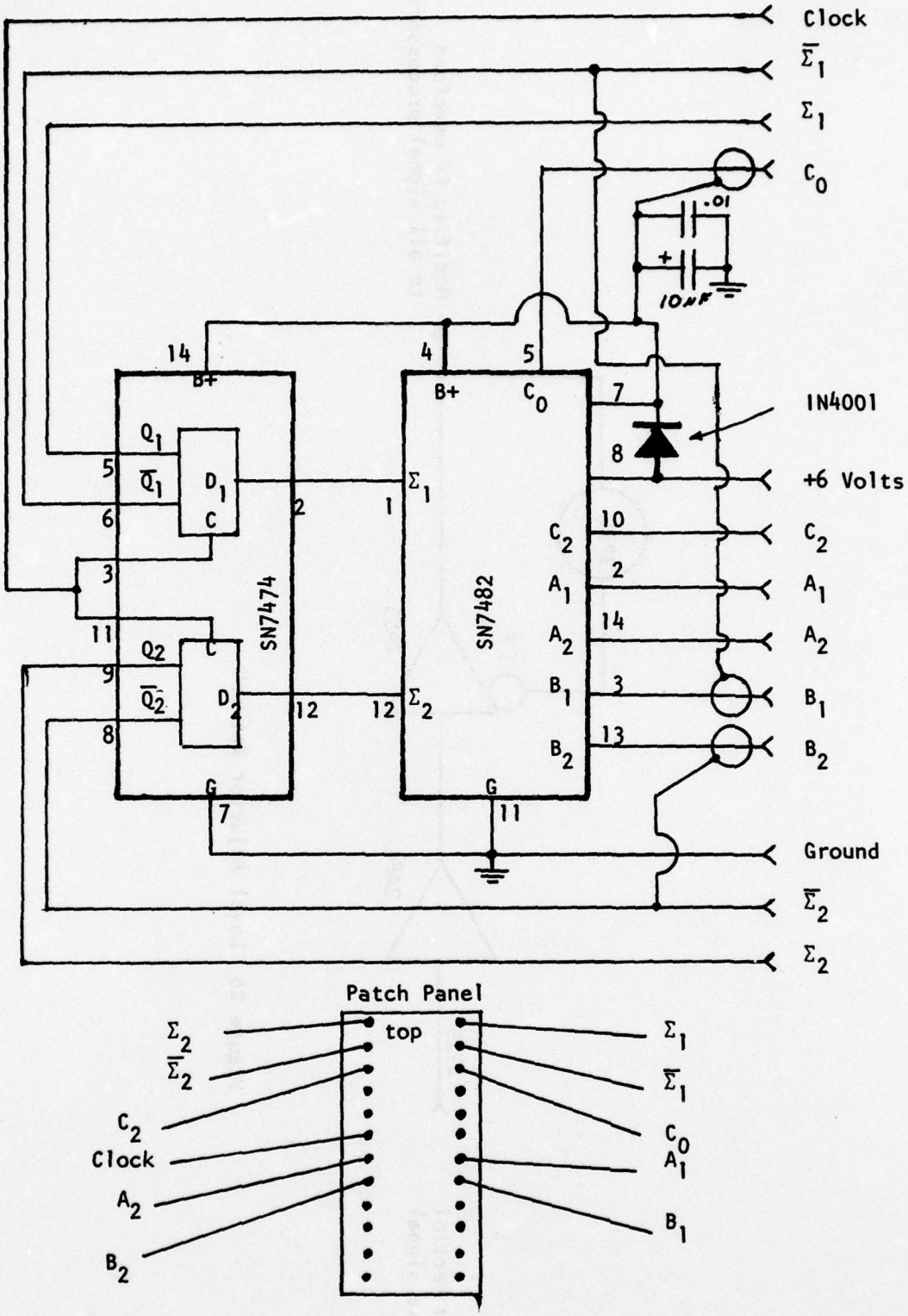


Figure 25 Data Precoder 2 Bit Processor

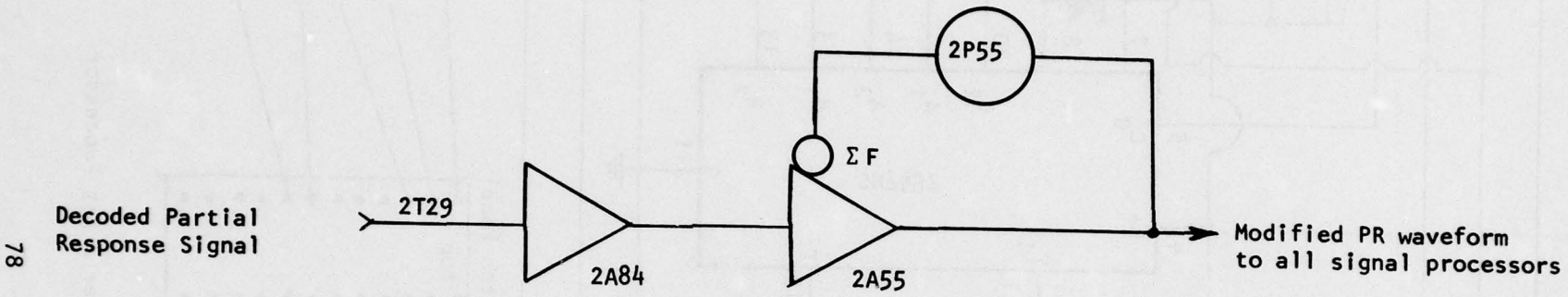


Figure 26 Level Adjustor Network

2.2.4 7-Level to 4-Level Analog Converter

Having demodulated and filtered the transmitted signal, the first step in the decoding process is to digitize the seven-level partial response signal. This is accomplished by the set of six comparators shown in Figure 27. For purposes of decoding the transmitted signal, the actual digital value of the partial response signal is not required. Hence, the output of the comparators are used to drive a set of gates which perform the modulo 4 conversion to drive the analog switches which generate the decoded 4-level signal. Table 11 lists the seven partial response levels together with the logic states of all comparators and gates of the 7- to 4-level analog converter. The circles in Table 11 indicate the particular logic element responsible for a specific 4-level output at amplifier 2A16. It should be noted that the 7- to 4-level converter performs conversions which are completely independent of the system timing clock. Hence, decoding the analog signal may result in many incorrect output levels in the 4-level signal. These are eliminated when the final decoding process is done by the 4-level A/D converter which will be discussed in the next section.

In addition to the above implementation, a digitized version of the partial response signal is created by driving a set of function relays from the 7-level to 4-level comparator outputs. These switches connect potentiometers to the input of 2A66 to form a digitized version of the instanteous partial response signal as indicated in Figure 28.

2.2.5 4-Level Analog to Digital Converter

The 4-level signal from 2A16 will contain many states which do not correspond to the actual transmitted signal. These states are a result of the transition of the partial response signal from one level to another and

Table 11 7-Level to 4-Level Analog Converter Internal States

Input Levels		Comparators						Gates								Output
Logic Level	Voltage (volts)	2C 44	2C 74	2C 104	2C 49	2C 79	2C 109	22B	22C	22D	22E	22F	23A	23F	24A	2A16 (volts)
6	+2.00	H	H	H	H	H	H	L	L	L	L	L	(L)	H	H	+0.36
5	+1.36	L	H	H	H	H	H	H	L	L	L	L	H	(L)	H	-0.36
4	+0.68	L	L	H	H	H	H	L	H	L	L	L	H	H	(L)	-1.00
3	0.00	L	L	L	H	H	H	L	L	(H)	L	L	H	H	H	+1.00
2	-0.68	L	L	L	L	H	H	L	L	L	H	L	(L)	H	H	+0.36
1	-1.36	L	L	L	L	L	H	L	L	L	L	H	H	(L)	H	-0.36
0	-2.00	L	L	L	L	L	L	L	L	L	L	L	H	H	(L)	-1.0

Note: L indicates a logic zero

H indicates a logic one

Circles indicate component responsible for analog output voltage at 2A16

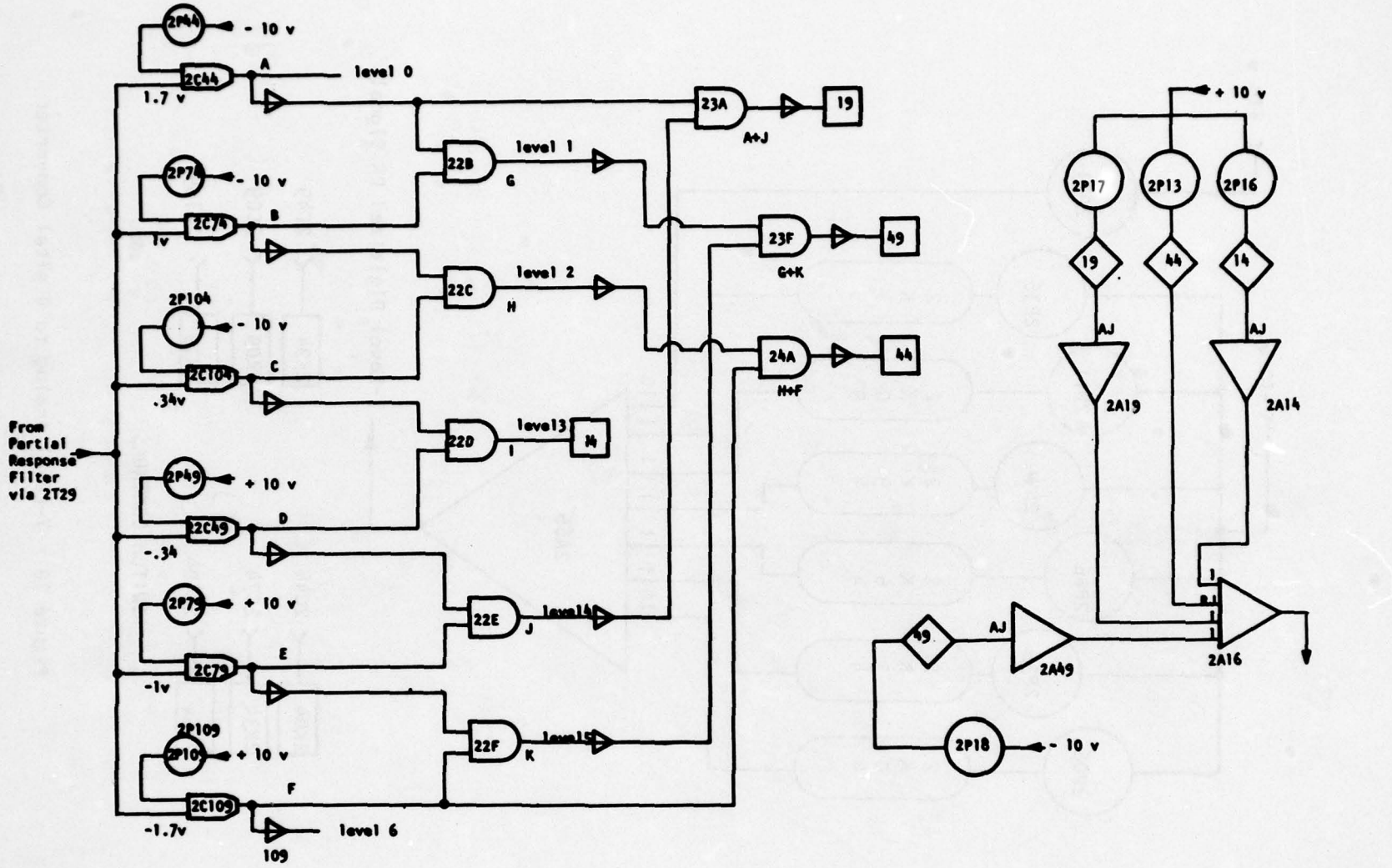


Figure 27 7-Level to 4-Level Analog Converter for 7-Level Partial Response System

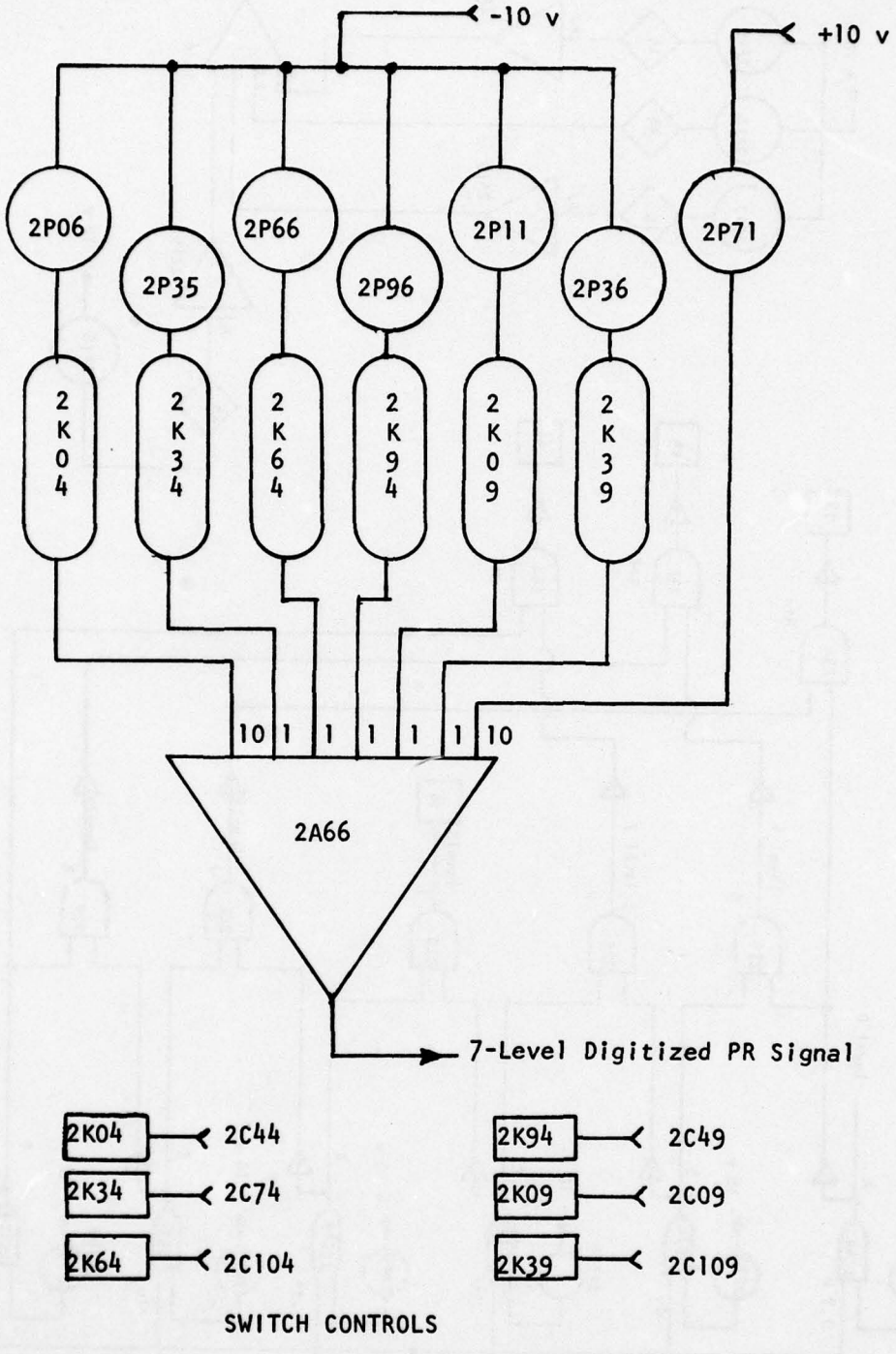


Figure 28 7-Level Analog to Digital Converter

are usually of very short duration compared to the desired 4-level signal. These transient levels are eliminated by redetecting the 4-level signal of 2A16 by a clocked detector. The detector, which is controlled by the system timing recovery clock, samples the 4-level signal of 2A16 and generates a binary code corresponding to the four possible decoded levels. This signal, consisting of x_1, x_2, x_3, x_4 as shown in Figure 29, drives a 4-level to binary converter whose internal states are defined in the table below.

4-Level A/D Internal States

4-Level Input	Converter			Logic					2A51 Output
	2C 24	2C 54	2C 84	2F 4B	2F 4C	2F 4D	24D	24E	
+1	H	H	H	H	H	L	L	L	+1
+ .34	L	H	H	L	H	L	H	L	+ .34
- .34	L	L	H	L	L	L	L	H	- .34
-1	L	L	L	L	L	H	L	L	-1

The two-step process of decoding the 7-level partial response signal could have been acomplished without first creating an intermediate 4-level signal. This would, however, have necessitated additional circuitry to be implemented in the 4-level FM simulation to be discussed later. Using the two-step decoding processes allows the demodulated 4-level FM signal to be decoded directly by the 4-level ADC. For display and illustration convenience, the final decoded 4-level signal appears at 2A51. In a real hardware implementation of this decoder, all processing would be done digitally after the initial level decision made by the six comparators of the 7-level to 4-level converter.

2.2.6 4-Level Digital to Binary Decoder

Most digital processing requires some type of binary bit stream. Consequently, the final step in the signal processing is to recover the binary signal which is encoded in the multilevel transmitted signal.

The quaternary level information, x_1 through x_4, obtained from the 4-level A/D of Figure 29 is used to set a pair of flip-flops 2F3A and 2F4A as shown in Figure 30. Each level of the quarternary signal corresponds to a two-bit binary sequence. If the first bit of this sequence is a logic 1, flip-flop 2F3A is set high for a full clock cycle of the low speed recovery clock. Similarly, if the quarternary level being decoded requires a logic 1 in the second bit of the two-bit sequence, flip-flop 2F4A is set high. The states of both flip-flops are read by gates 24B and 24C which are controlled by the complementary outputs of the slow speed system recovery clock. The output of these gates is added through 2A20 and a new binary sequence is formed, as shown in Figure 31, which has a rate equal to twice the slow clock frequency. Note that for this decoder implementation to work well, the timing recovery clock must be symmetrical. This is easily accomplished by deriving the clock waveform from a flip-flop output which functions as a divider from a higher clock rate. Hence, it presents no major difficulty in implementation.

2.2.7 Multilevel Timing Recovery PLL

The actual phase lock loop used for timing recovery is identical to that used in the three-level partial response simulation with the exception of the voltage controlled oscillator frequency. In order to ensure a symmetrical timing clock for use in the binary decoder, the VCO frequency

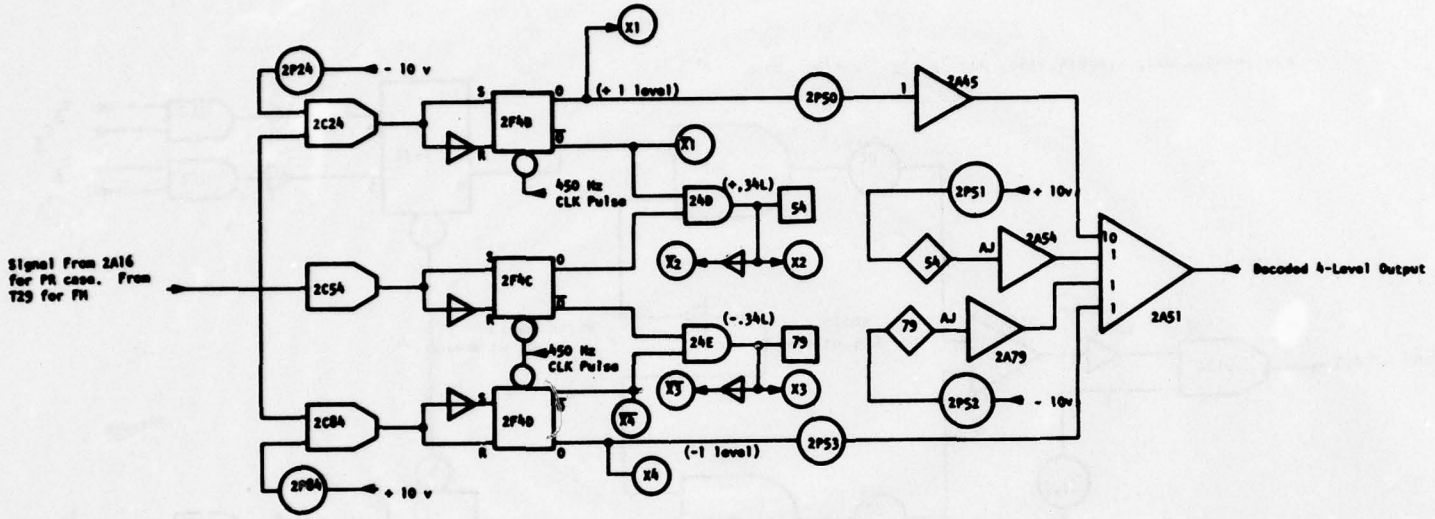
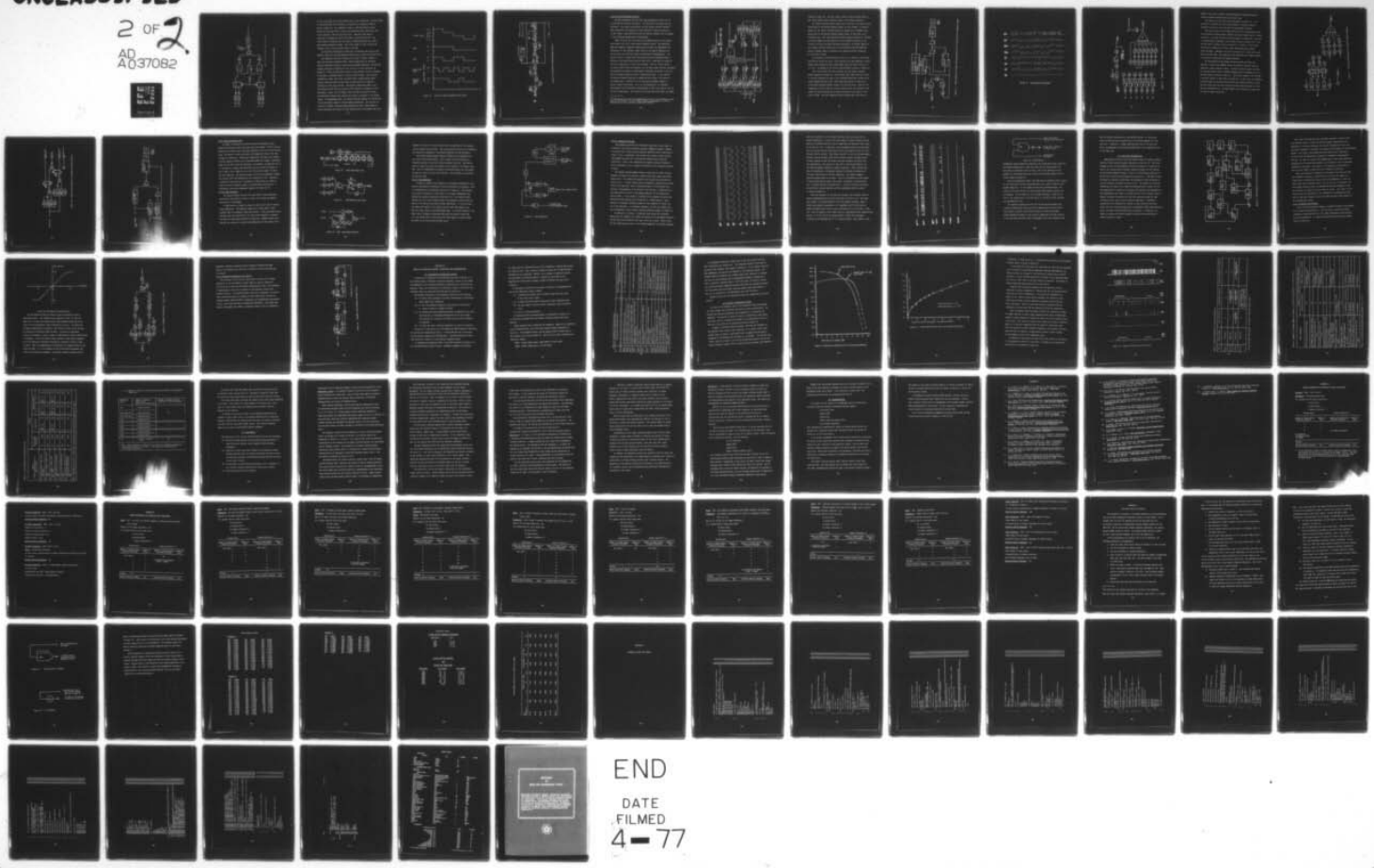


Figure 29 4-Level Analog to Digital Converter

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ADVANCED MONITORING TECHNIQUES FOR DIGITAL COMMUNICATION SYSTEM--ETC(U)
JAN 77 J L HAMMOND, D J SCHAEFER, S S LIU F30602-75-C-0118
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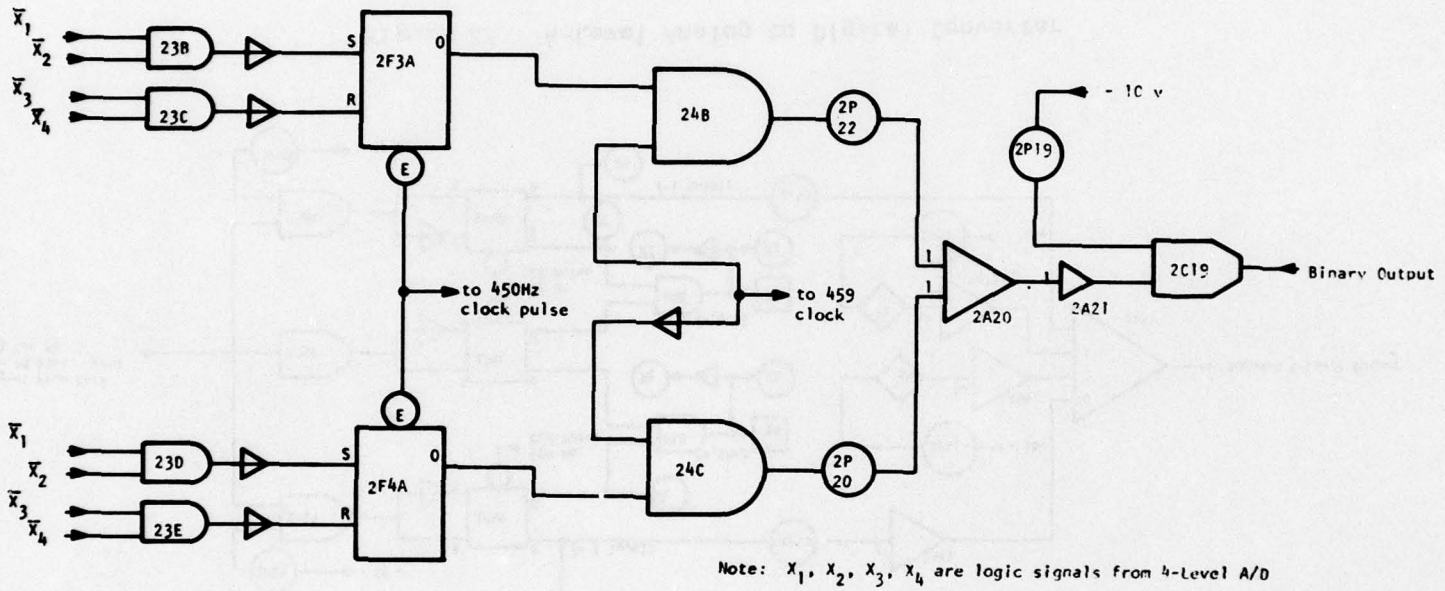


Figure 30 4-Level Digital to Binary Decoder

is set to the data rate of the binary input to the simulation. The VCO, which is a Wavetek Model 112 oscillator, is digitized by comparator 2C69 as shown in Figure 32. The comparator output is differentiated and then divided by flip-flop 2F5A to obtain the synthesized slow speed clock used in the receiver's data recovery circuitry. The phase lock loop is completed by feeding the clock output back to gates 21B and 21C. The clock signal is compared with the output of monostable 2M41 and a phase error signal generated by 2A05. This error signal is then filtered and returned to the voltage control input of the VCO.

An analytical description of this type of loop has been given in the previous report [9] and suplementary material can be found in [26] and [27].

The remaining circuitry of Figure 32 is used to obtain a pulse to drive the PLL input monostable 2M41. System timing must be recovered from the demodulated analog 7-level partial response waveform. The partial response waveform is digitized by the 7-level to 4-level converter of Figure 27. Since the four-level output of this network is still unclocked, it provides a convenient place to recover system timing. The circuitry consisting of 2A44, 2A37, 2A41, and 2C39 forms a differentiator which outputs a positive pulse for any type of rapid positive or negative transition in the ouput of 2A16. The period of monostable 2M41 is set long enough so that only one pulse per clock period is recognized by the monostable. Hence, on the average, after the PLL is initially locked, the monostable response will provide an accurate indication of the system timing. As implemented above, the timing circuitry employs all transitions of the quarternary signal to provide phase information. One question of interest is whether obtaining timing information from a fewer number of level transitions will result in less timing jitter in the phase lock loop.

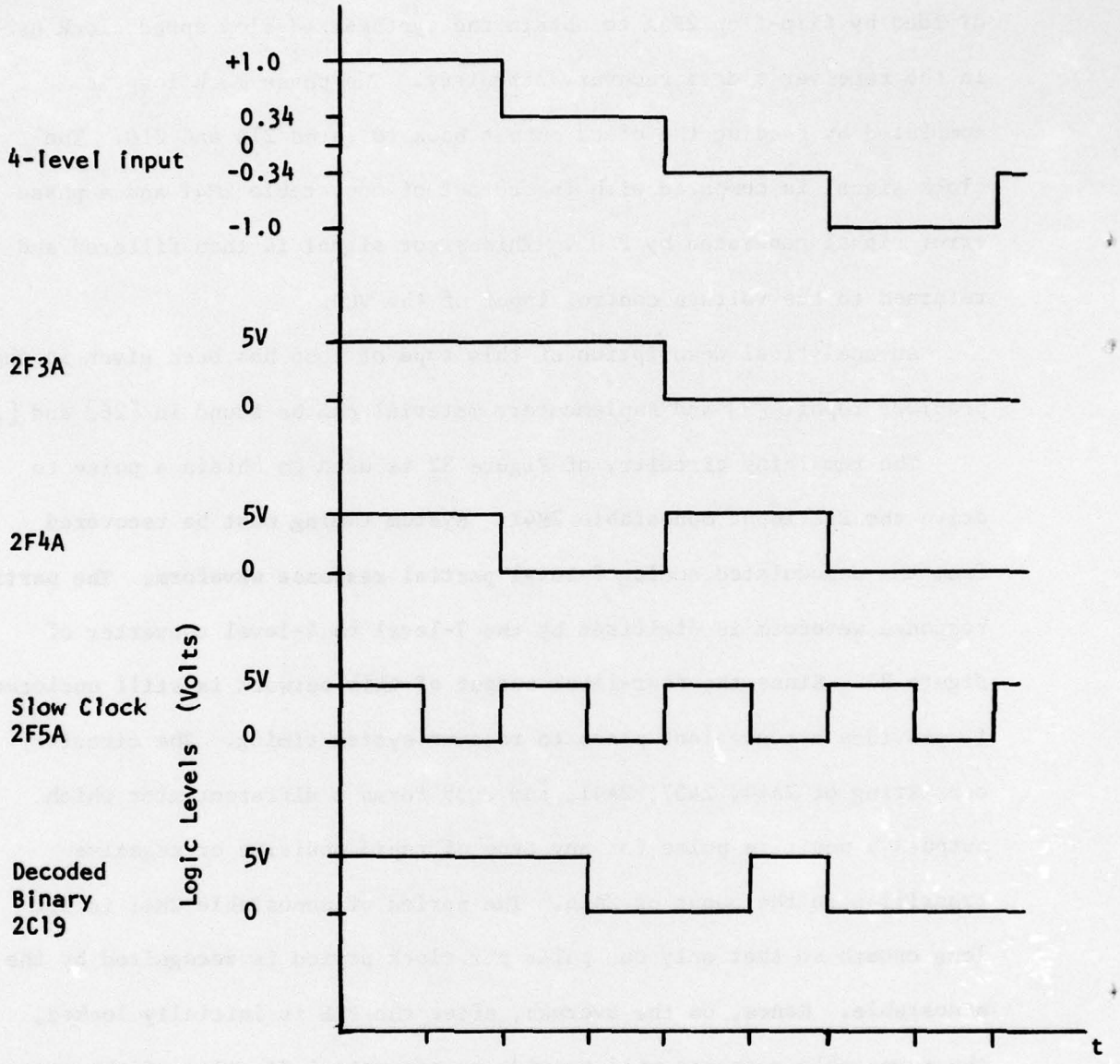


Figure 31 4-Level to Binary Decoder Logic Levels

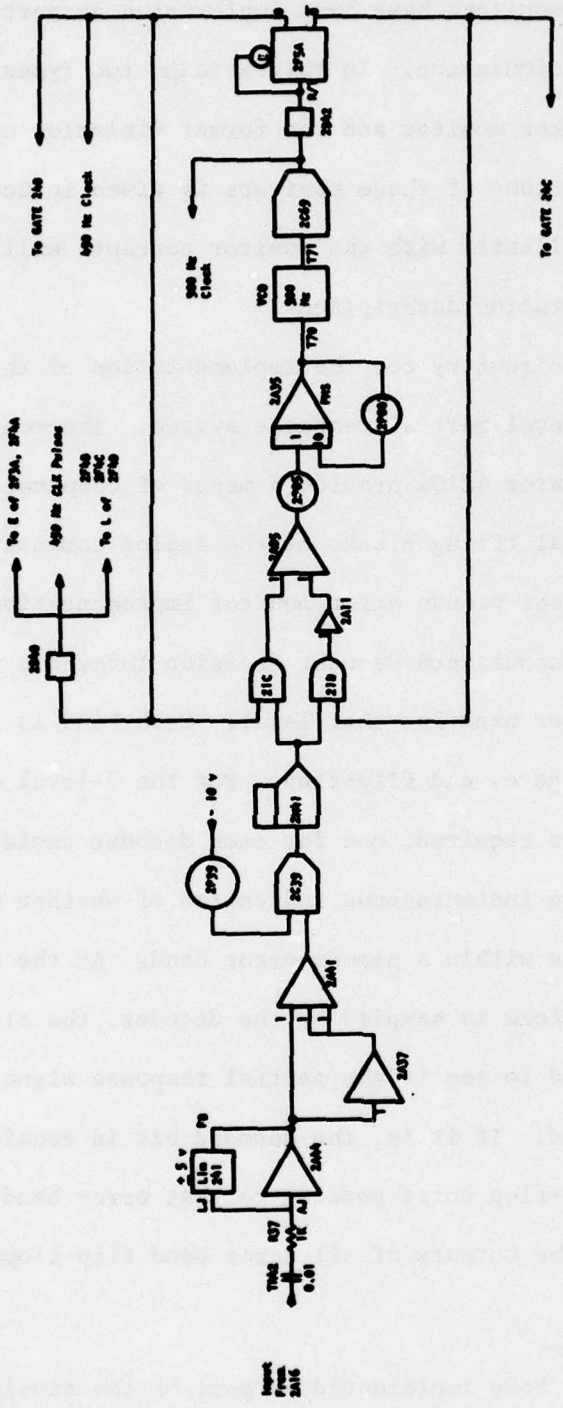


Figure 32 Multilevel Timing Recovery Circuit

2.2.8 System Performance Monitors

Several performance monitors have been implemented as part of the 7-level partial response simulation. In this section two types will be discussed: the pseudo error monitor and the format violation monitor[1]. Since theoretical descriptions of these monitors is given in Section I of this report, some familiarity with the monitor concepts will be assumed in the following implementation descriptions.

Figure 33 gives the circuitry for the implementation of the pseudo-error monitor for the 7-level partial response system. The monostable 4M00 and companion comparator 4C104 provide a means of compensating for differences in the internal timing clocks of the analog computers and do not enter into the actual pseudo error monitor implementation. The monitor creates a region about each decoder decision threshold which is defined as the pseudo-error band for that level. Each band is formed by a pair of comparators, a gate, and flip-flop. For the 7-level system, six pseudo error bands are required, one for each decoder decision threshold. The comparators provide an instantaneous indication of whether or not the partial response signal is within a pseudo-error band. At the instant the partial response waveform is sampled by the decoder, the status of the comparators is checked to see if the partial response signal is within a pseudo error band. If it is, the decoded bit is considered questionable and the flip-flop corresponding to that error band is set for one full clock period. The outputs of all error band flip-flops are summed

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[1] A frame monitor has also been implemented as part of the simulation. Since most of the monitor is in the digital computer programming, it will be discussed in a later section on simulation software.

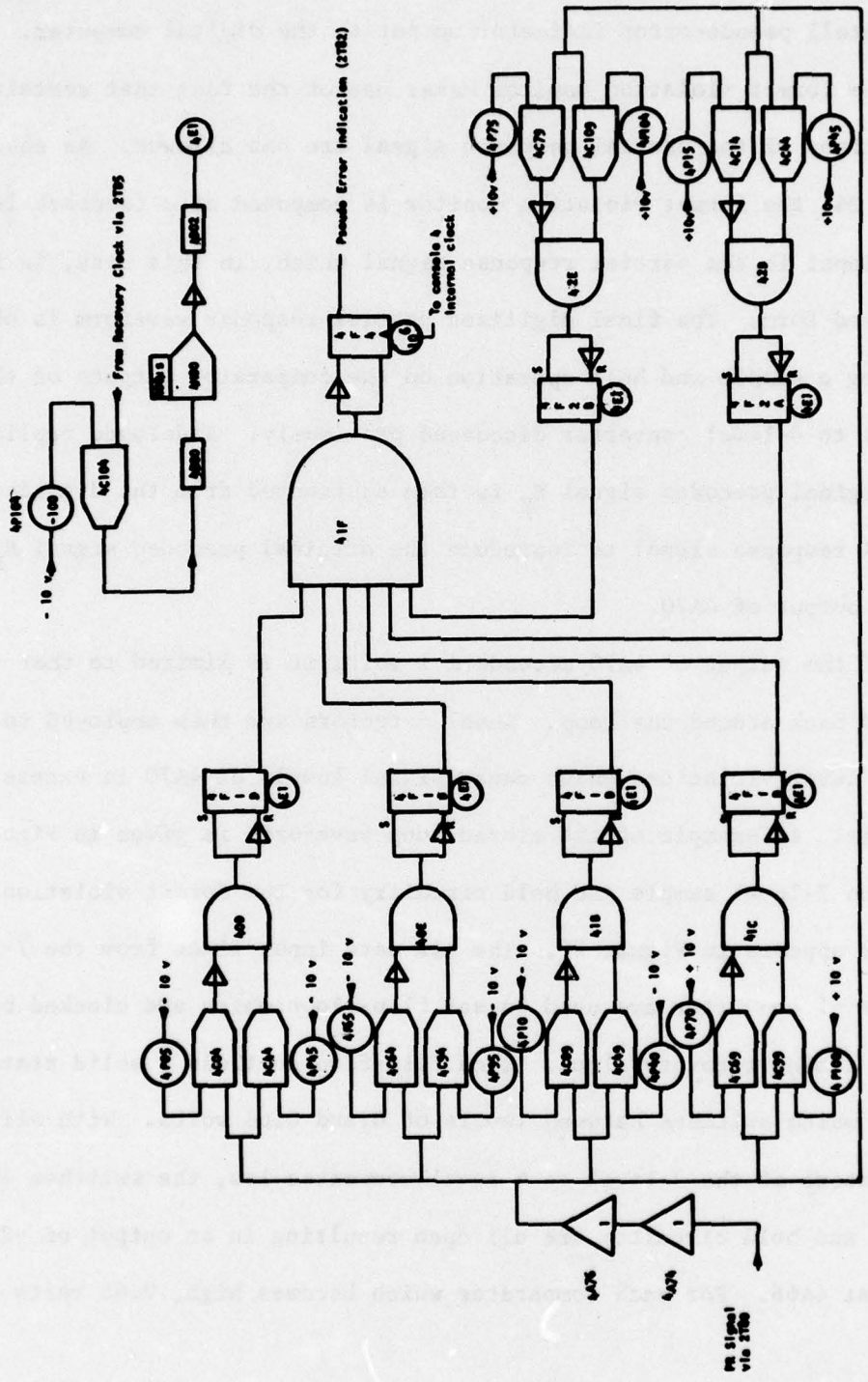


Figure 33 Pseudo Error Monitor

together by gate 41F. The gate output controls flip-flop 4F3A which is the overall pseudo-error indicator output to the digital computer.

The format violation monitor makes use of the fact that certain level transitions of the partial response signal are not allowed. As shown in Figure 34, the format violation monitor is composed of a feedback loop whose input is the partial response signal which, in this case, is in digitized form. The final digitized partial response waveform is obtained by doing a sample and hold operation on the comparator outputs of the 7-level to 4-level converter discussed previously. A delayed replica of the original precoded signal B_K is then subtracted from the digitized partial response signal to reproduce the original precoded signal B_K at the output of 4A70.

If the output of 4A70 exceeds ± 1 volt, it is limited to that value and fed back around the loop. Level detectors are then employed to sense format level violations which cause signal levels at 4A70 in excess of ± 1 volt. An example of the closed loop waveforms is given in Figure 35.

The 7-level sample and hold circuitry for the format violation monitor appears in Figure 36. The six data input lines from the 7-level to 4-level converter are used to set flip-flops which are clocked by the system timing recovery clock. Each flip-flop controls a solid state switch which switches between levels of 0 and 0.68 volts. With all the comparators of the 7-level to 4-level converter low, the switches of the sample and hold circuitry are all open resulting in an output of -2.0 volts at 4A66. For each comparator which becomes high, 0.68 volts is

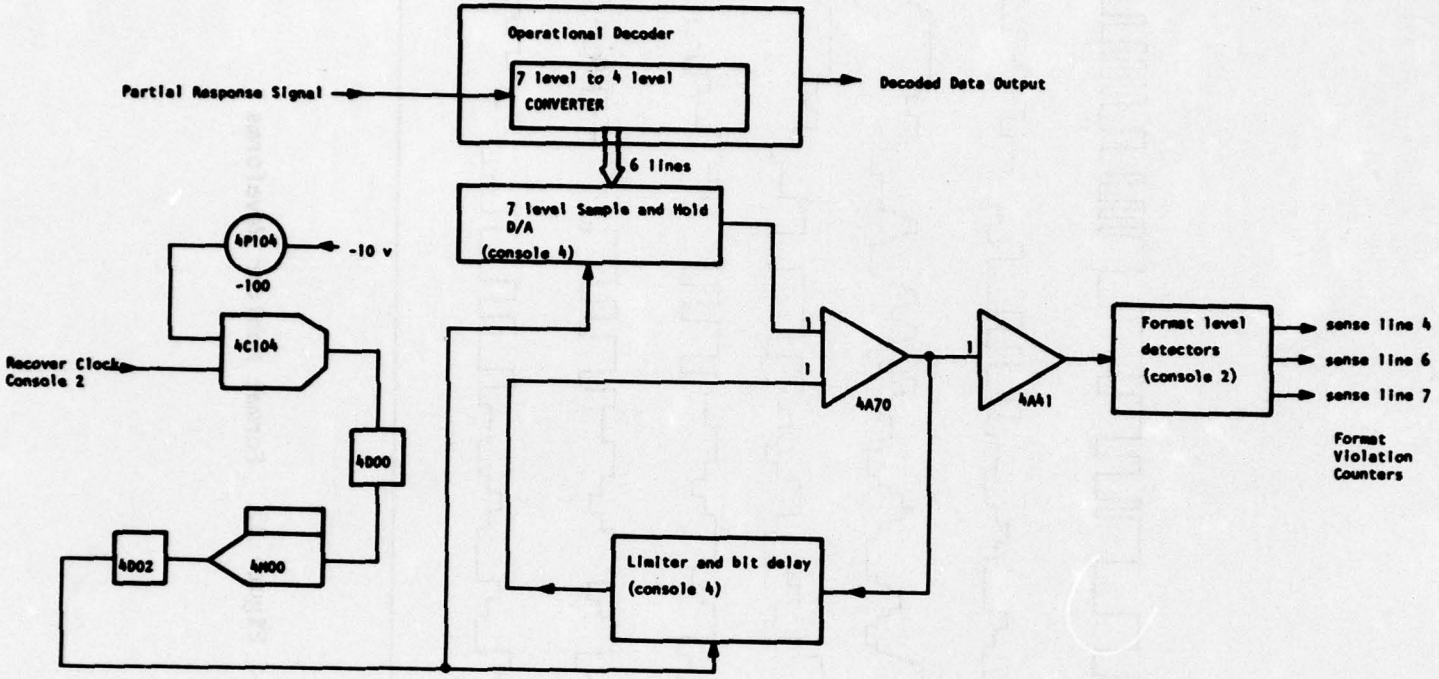


Figure 34 Block Diagram of Format Violation Monitor for 7-Level Partial Response System

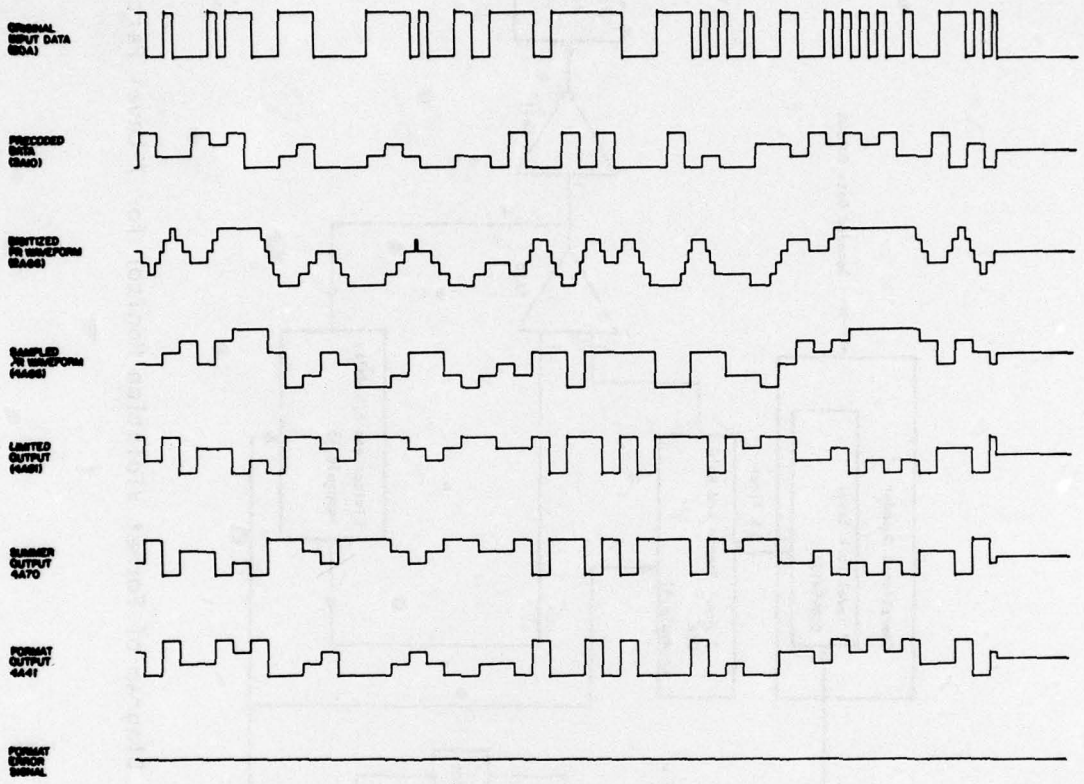


Figure 35 Format Monitor Waveforms

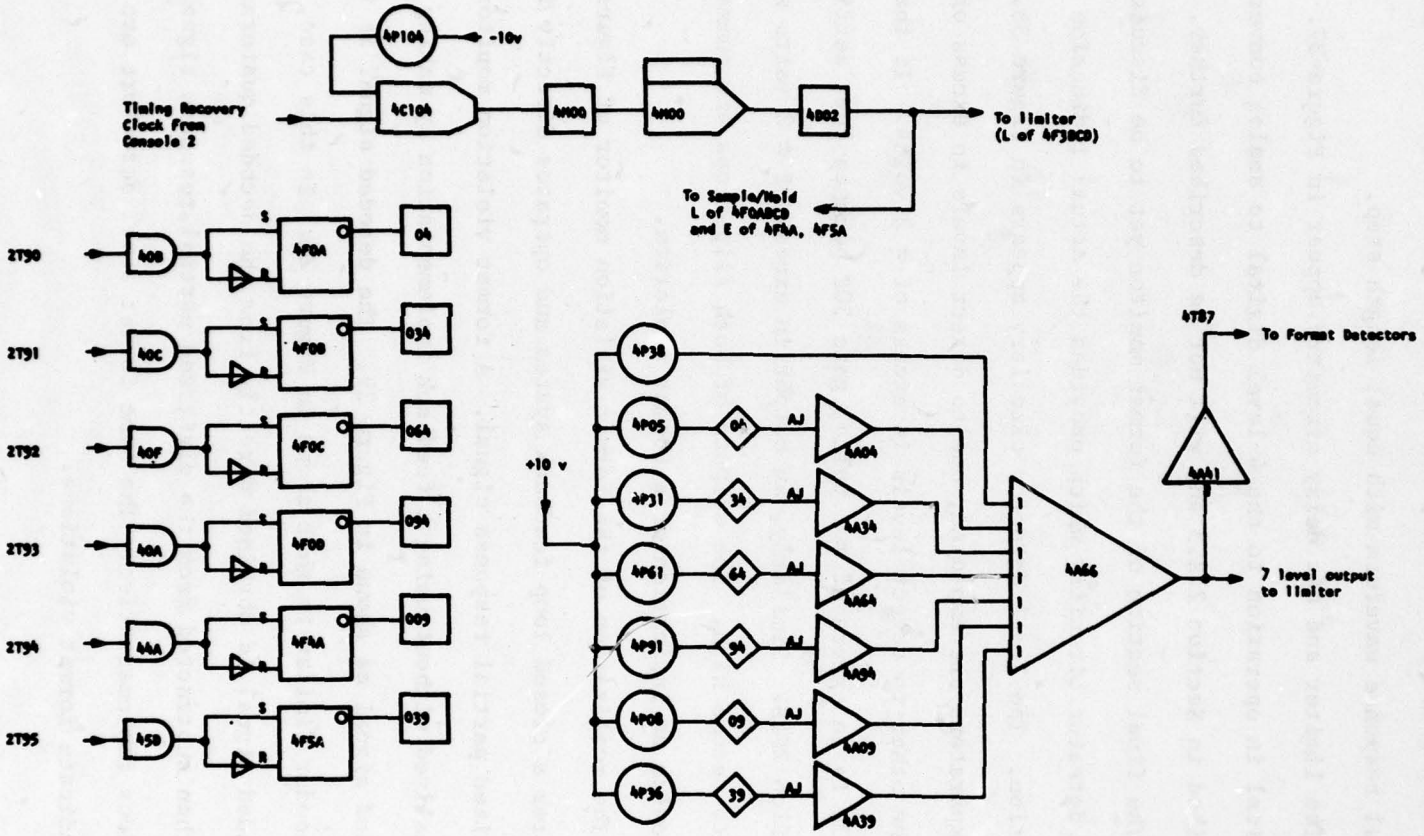


Figure 36 7-Level Sample and Hold Network for Format Violation Monitor

added to the output of 4A66, thereby forming the required digitized parcial response waveform with equal length step.

The limiter and bit delay circuitry appear in Figure 37. It is identical in operation to the 4-level digital to analog converter described in Section 2.2.5 and will not be described further.

The final section of the format monitor yet to be discussed is the level detector circuitry which provides the actual indication of a format violation. The level detector circuitry appears in Figure 38. Two sets of comparators are employed, one to detect levels in excess of ± 1 volt and the other to detect levels in excess of ± 2 volts. If the output of 4A70 is in excess of ± 1 volts, gate 30F becomes low, setting flip-flop 2F2B. Similarly, an output in excess of ± 2 volts will cause 2F2C to become high. The outputs of both flip-flops are summed together to provide an indication of a format violation.

The realization of the format violation monitor of Figure 34 requires a closed loop feedback system and operates directly from the digitized partial response signal. A format violation monitor may also be realized without using a feedback implementation by making use of the decoded signal as shown in Figure 39. The decoded signal is fed through a precoder similar to that shown in Figure 24. In this case, the delayed precoded signal is obtained directly from the decoded quaternary signal and then subtracted from the digitized partial response signal as in the previous implementation. The same format level detectors are then used to indicate format violations.

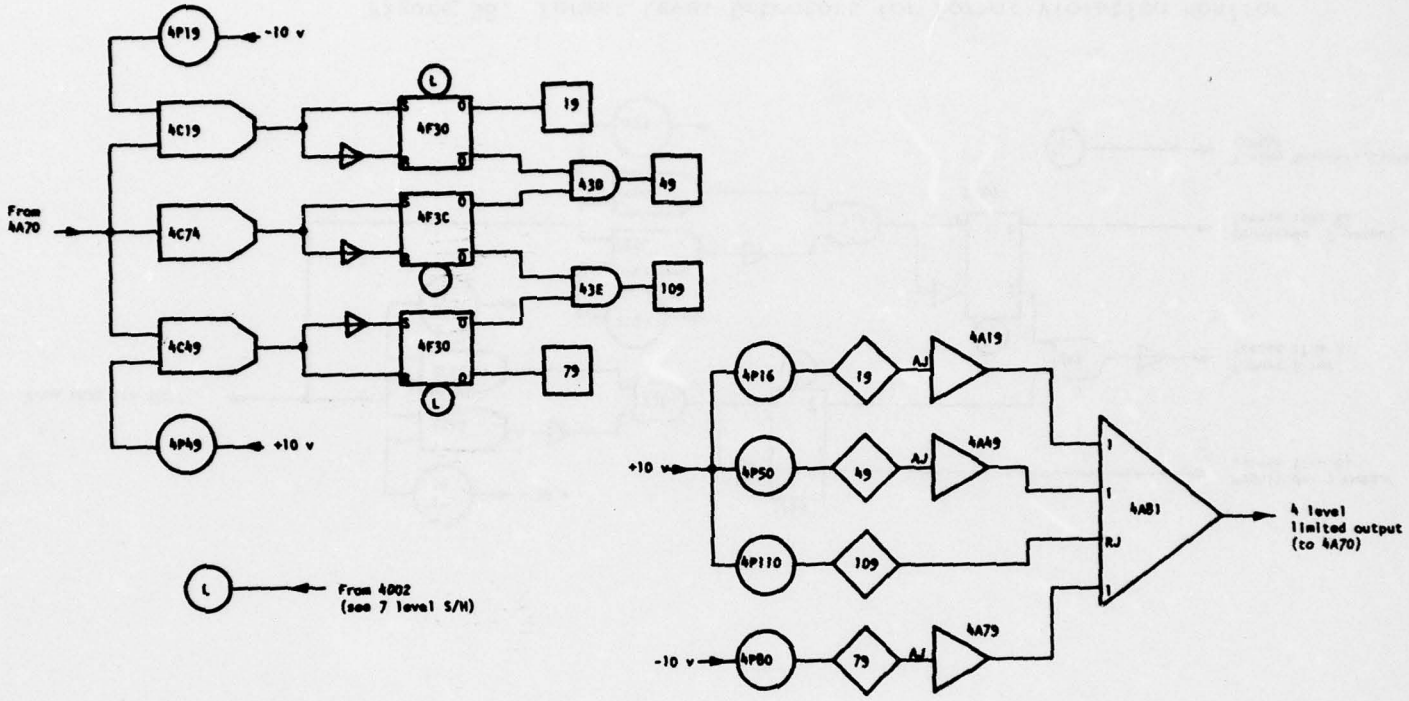


Figure 37 Limiter and Bit Delay for Format Violation Monitor

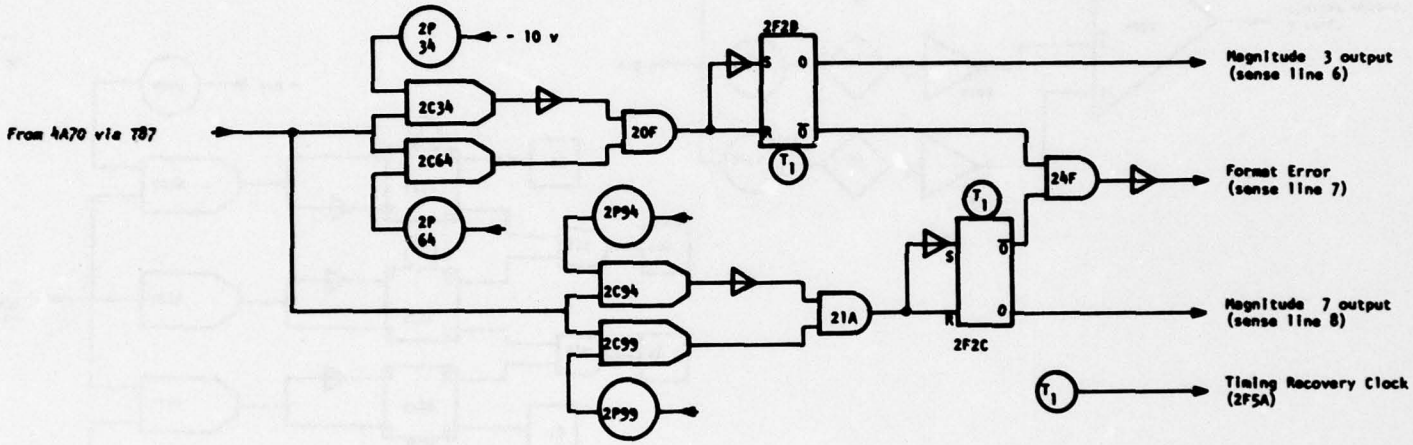


Figure 38. Format Level Detectors for Format Violation Monitor

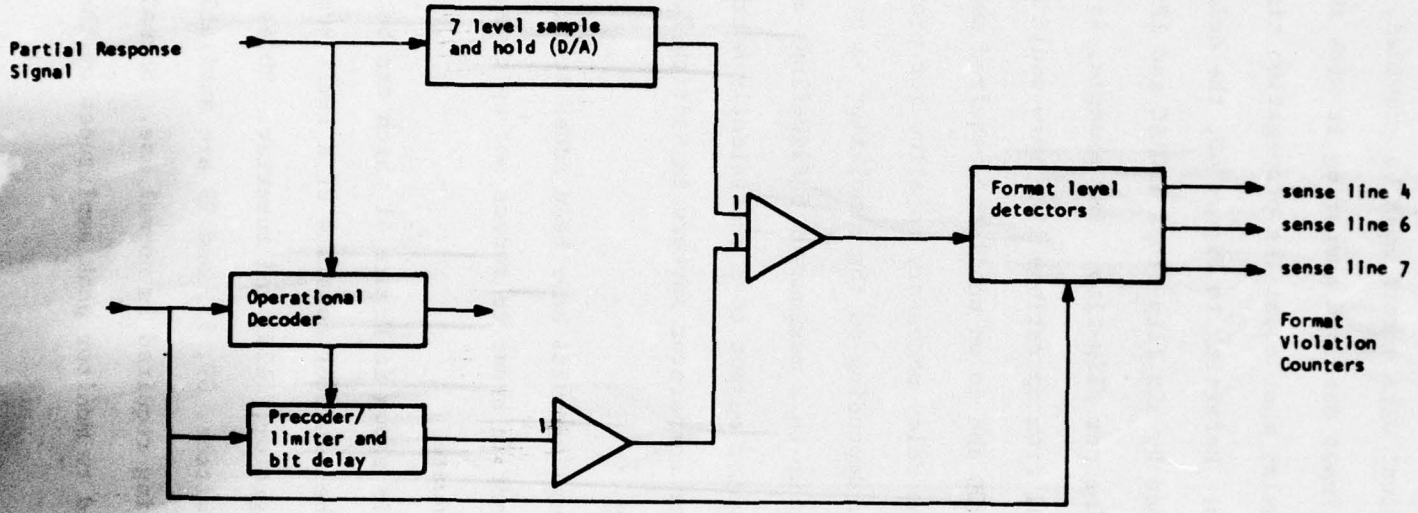


Figure 39 Alternate Realization of Format Violation Monitor

2.2.9 Input Data Delay Line

In order to ascertain the actual simulation performance, some method of detecting actual data errors must be provided. This is done by delaying the original input data and comparing it with the actual decoded data. The amount of delay must equal the propagation time of the data through the simulation. Referring to Figure 40, the delay line consists of shift register formed by six flip-flops 1F0ABC and 1F1ABC. Monostable 1M00 sets the delay time per flip-flop. For example, if 1M00 were set to a 1 ms period, a signal from operations line zero would be delayed at 1 ms at 1F0A, 2 ms at 1F0B and so on until the required amount of delay has been achieved. The delay necessary to allow for propagation through the circuits will vary depending on the simulation in use. Typically, a minimum of three and up to a maximum of 5 flip-flops are needed to reduce the error indicator output to a sufficiently narrow pulse. A discussion of the error comparator appears in Section 2.2.11.

2.2.10 Test Circuitry

Two special purpose circuits have been added to the simulations discussed in this report in order to reduce set-up time and simplify monitoring of the hardware.

A peak detector is shown in Figure 41 which can be used to monitor signal amplitudes. The detector consists of a limit summer, 1A26, together with an integrator, 1A25, and inverter. Three switchable inputs through solid state switches 09, 93, and 99 are available to decrease the amount of repatching required in normal use. Normally these three switches are connected to monitor peak amplitudes of the signal in the

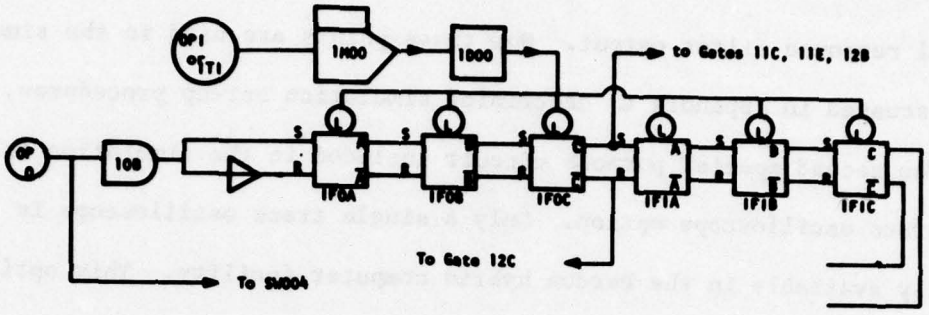


Figure 40 Input Data Delay Line

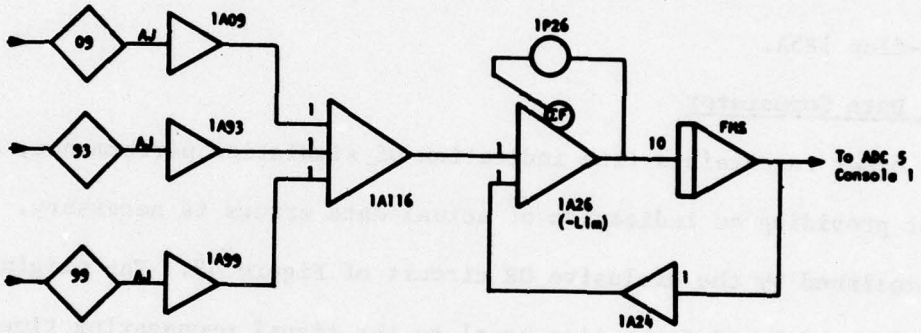


Figure 41 Peak Detector and Switch

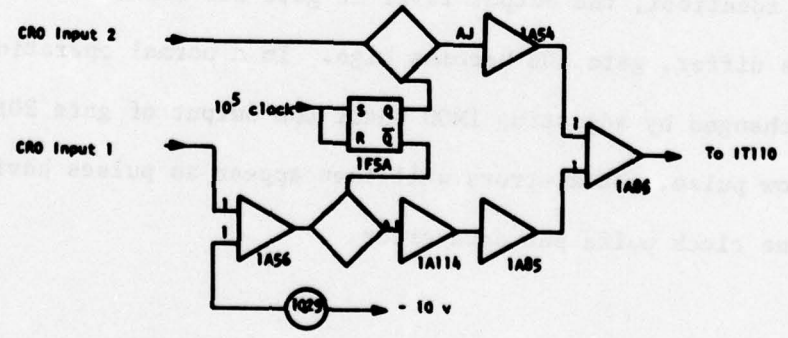


Figure 42 Dual Trace Scope Generator

channel, VCO level of the PLL detector and the amplitude of the receiver partial response filter output. How these points are used in the simulation are discussed in Appendix C describing simulation set-up procedures.

The second special purpose circuit included in the simulation is a dual trace oscilloscope option. Only a single trace oscilloscope is normally available in the Purdue hybrid computer facility. This option, shown in Figure 42, allows the display of two signals on the single trace CRO. This is accomplished by rapidly alternating between the two signals by means of a pair of solid state switches. The switching is controlled by flip-flop 1F5A.

2.2.11 Data Comparator

In order to obtain a true indication of simulation performance, some means of providing an indication of actual data errors is necessary. This is accomplished by the exclusive OR circuit of Figure 43. The original input data is delayed for a time equal to the signal propagating time through the system as discussed in Section 2.2.9. The delayed signal together with the actual decoded signal from comparator 2C19 provide the inputs to the XOR via gates 22A and 20E respectively. So long as these two inputs are identical, the output level at gate 20B remains zero. When the inputs differ, gate 20B becomes high. In a normal operation, the delay time is changed by adjusting 1M00 until the output of gate 20B is a very narrow pulse. Data errors will then appear as pulses having the width of one clock pulse per data error.

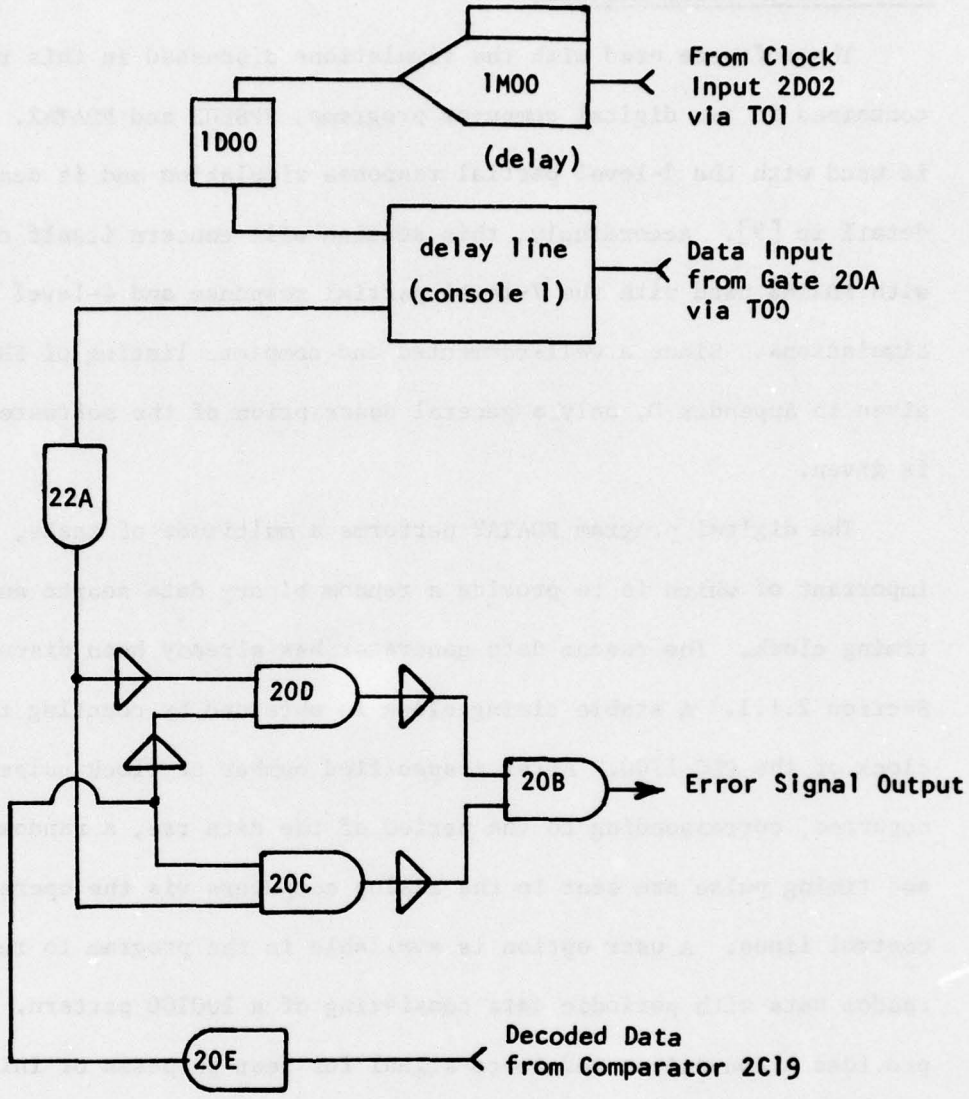


Figure 43 Data Comparator

2.2.12 Simulation Software

The software used with the simulations discussed in this report is contained in two digital computer programs, FPSEUD and FDATA2. FPSEUD is used with the 3-level partial response simulation and is described in detail in [9]. Accordingly, this section will concern itself entirely with FDATA2 used with the 7-level partial response and 4-level FM simulations. Since a well-commented and complete listing of FDATA2 is given in Appendix D, only a general description of the software functions is given.

The digital program FDATA2 performs a multitude of tasks, the most important of which is to provide a random binary data source and stable timing clock. The random data generator has already been discussed in Section 2.1.1. A stable timing clock is obtained by counting the internal clock of the CDC 1700. After a specified number of clock pulses have occurred, corresponding to the period of the data rae, a random data bit and timing pulse are sent to the analog computers via the operational control lines. A user option is available in the program to replace the random data with periodic data consisting of a 100100 pattern. This provides a convenient reference signal for test purposes or initial set up of the simulation. A stripchart recording of this test signal with the corresponding 7-level partial response waveforms appears in Figure 44.

In addition to acting as a timing and data source for the hybrid simulation, the computer also checks the status of all performance monitors and the data error indicator each time a data bit is sent. After a data bit and timing pulse are sent to the analog computers, the digital computer

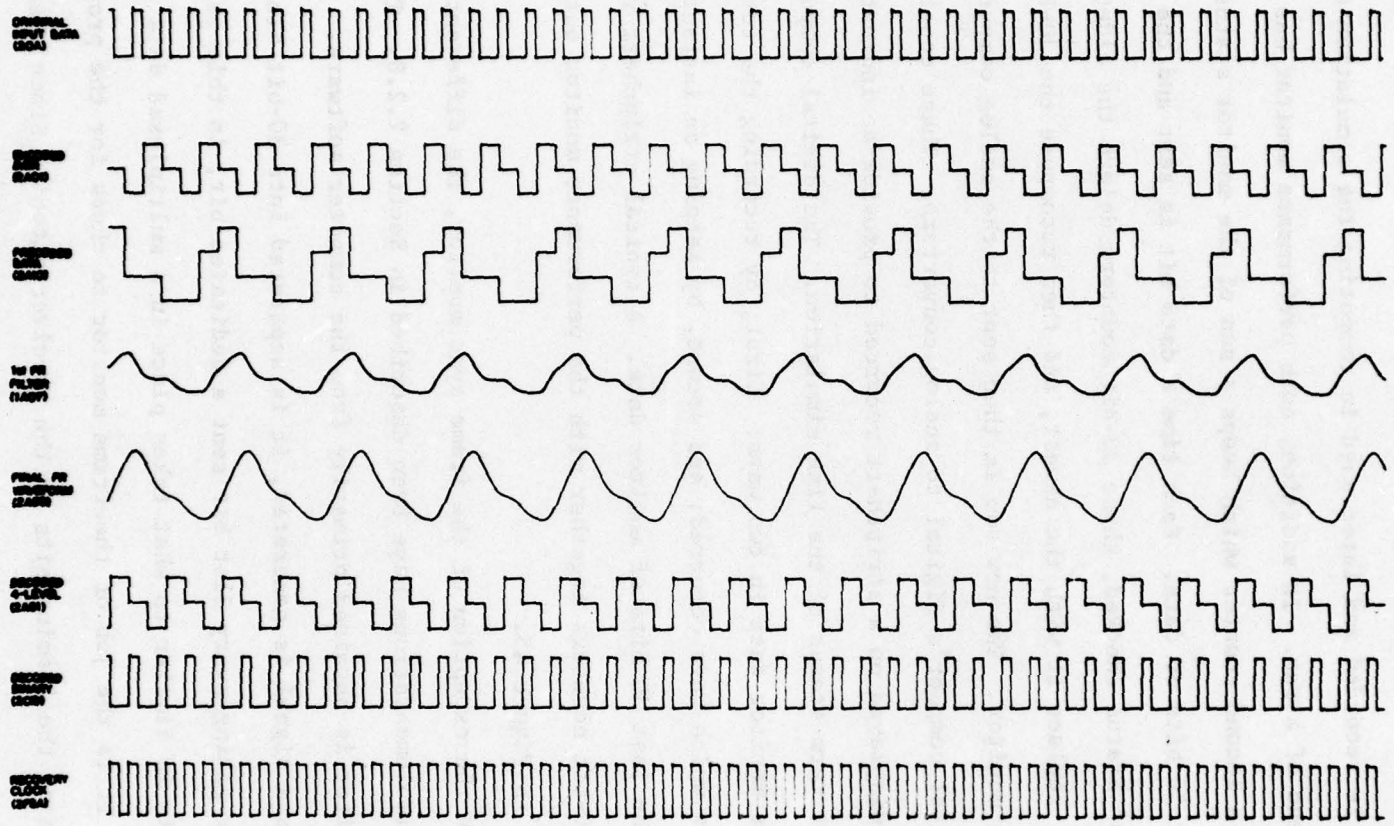


Figure 44 7-Level Partial Response Waveforms for Test Signal Input

will wait one-half of a clock period and then check the status of all monitor indicators. A sum of the total number of errors detected by each monitor is recorded and later used in computing the simulation error rates at the end of a run. In addition, each performance monitor has associated with it a second counter which keeps a sum of the monitor status for only the past 30 bits of data. Each time a data bit is sent and the performance monitors' status checked, these 30-bit counters delete the oldest piece of data, replace it with the newest, and then recompute the 30-bit sum for each monitor. The new sum is then sent to the analog computer via the digital compuer's digital to analog converters. These counters may then be displayed on a stripchart recorded to provide an indication of the short term status of the link simulation. The digital computer processes monitor data in two ways: first, by recording the total number of errors which have occurred; and second, by keeping an instantaneous sum of the last 30 bits of monitor data. A typical stripchart recording of the 30-bit counters together with the performance monitor outputs is given in Figure 45.

With the exception of the frame sync monitor, the different types of monitor implementations have been described in Section 2.2.8. The frame sync monitor is obtained primarily from the computer software. When a random data signal is generated, it is separated into 30-bit blocks or frames by making every 31st bit sent a dedicated bit, in this case a logic one. This is similar to what takes place in a multiplexed data communications system. It is the job of the frame monitor to check for the proper reception of the framing bits at the receiver output. Since there is some

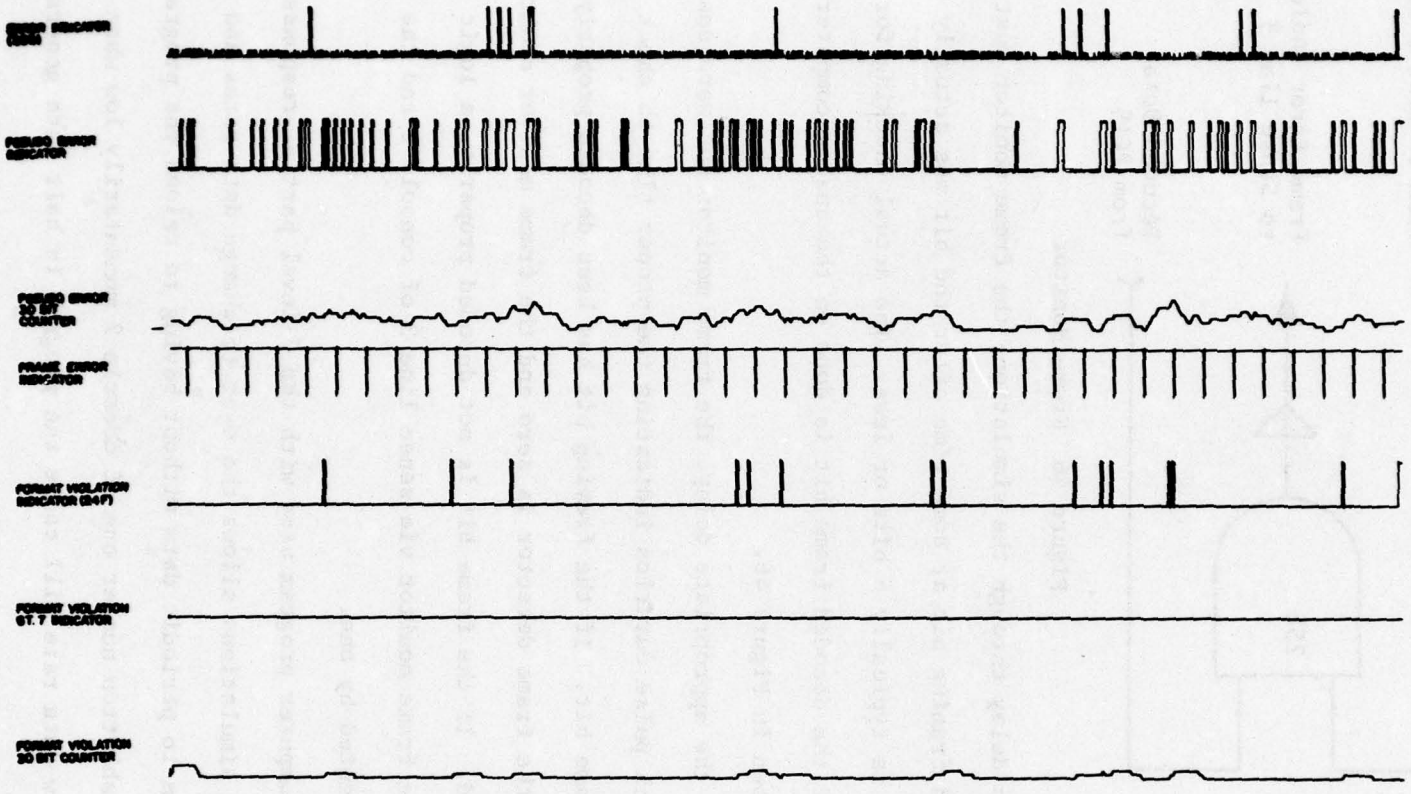


Figure 45 7-Level Partial Response Performance Monitor Outputs

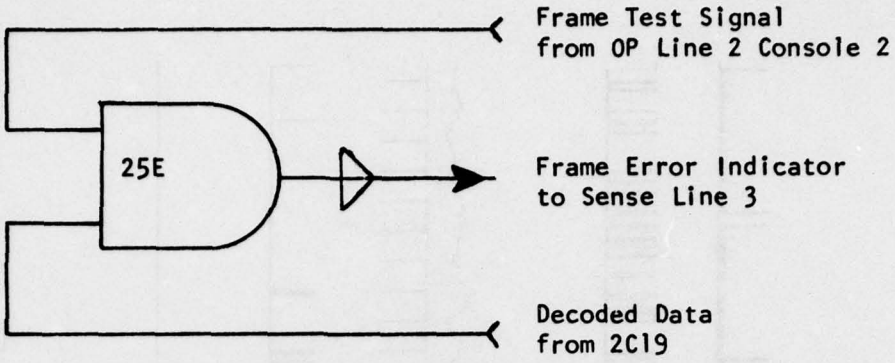


Figure 46 Frame Monitor

propagation delay through the simulation, the frame monitor must check for the decoded framing bit at some time after the bit was actually sent. This delay is typically 6 bits or less. The actual checking for the presence of the decoded frame bit is done on the analog computer by the circuit shown in Figure 46.

After the appropriate delay, the frame monitor software sends a signal of one clock pulse duration indicating the proper time to check for the decoded frame bit. If the framing bit has been decoded properly, the output of the frame detector is zero and the frame monitor counters are not changed. If the frame bit is not decoded properly, a logic one is sent to the frame monitor via sense line 3 of console 2 and the counters are incremented by one.

The computer program used with the 7-level partial response and 4-level FM simulations allows the user to change data rates and switch from random to periodic data without having to reload the program. Placing pushbutton number one of console 2 momentarily low when running at the slow data rate will cause the program to halt data generation and

ask for further instructions on the CDD1700 teltype. At this point, either stored data may be printed out or the system changed to a high data rate. Similarly, a change from high data rate to low data rate may be accomplished by placing both pushbuttons 1 and 2 momentarily low at the same time.

2.3 Four-Level FM Simulation

Simulation of a basic 4-level FM digital system is readily obtained from the 7-level partial response simulation of Section 2.2. The block diagram of the 4-level FM simulation given in Figure 47 is identical to that of the 7-level partial response simulation except for the absence of the partial response filters, 7-level to 4-level analog converter of Section 2.2.4, and the data precoder of Section 2.2.2. The basic 4-level FM signal is obtained by modulating the FM generator with the binary to 4-level converter described in Section 2.2.1. The channel and receiver simulations are identical to those discussed previously except that the PLL demodulator is replaced by a standard discriminator type demodulator. Once demodulated, the signal is decoded directly the by 4-level analog to digital converter of Section 2.2.5 and then processed using the same circuitry as the 7-level partial response simulation. Performance monitoring of the simulation is similar to that described previously except that the 4-level FM signal has no prescribed format characteristics. Hence, no format violation monitoring is possible. In addition, the number of pseudo-error bands required for pseudo error monitoring is reduced from six to three.

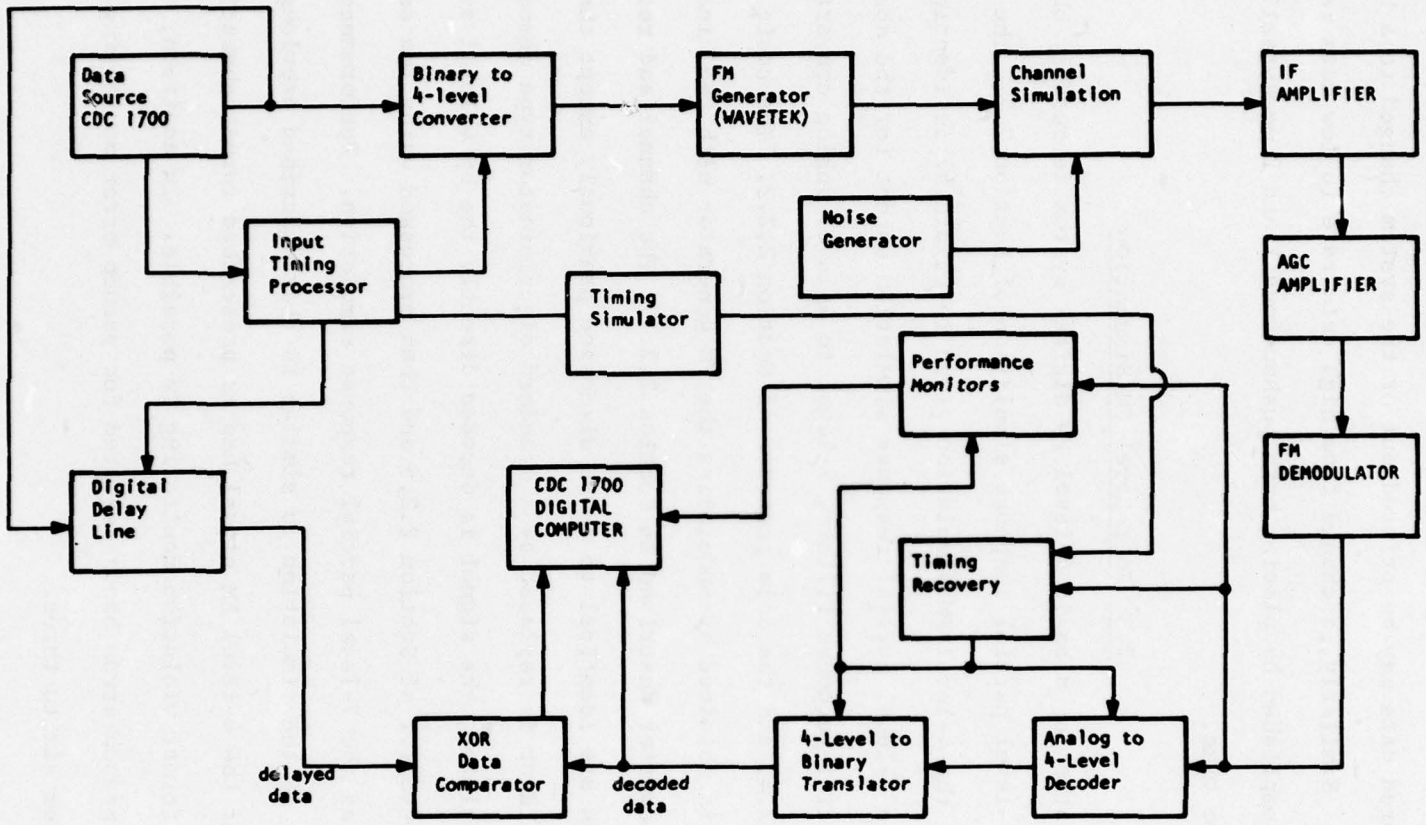


Figure 47 Block Diagram of 4-Level FM System

The 4-level FM simulation just described transmits a signal having four discrete states. Unlike the partial response simulations which demodulate a continuous waveform, the 4-level FM demodulator must have sufficient bandwidth to reproduce the discrete level changes in the modulating signal. As a result, the maximum data rate which may be transmitted by the 4-level FM simulation is limited to a maximum of approximately 100 bps. In order to increase this maximum rate, either some additional processing of the modulating waveform or an increase in the IF operating frequency is necessary. The change in IF frequency is undesirable in that it would require rescaling of the IF amplifier circuitry.

When the simulation is operated at the slower 5 bps rate used with the stripchart recorder, no difficulties arise since the length of a single baud is sufficiently long to allow the demodulator to reach its final value before sampling occurs. As the bit rate is increased, the baud length decreases until the demodulated waveform resembles a sine wave instead of a signal with four discrete states. This effect is the direct result of limitations in the bandwidth of the demodulator wich must be kept small enough to reject any 5KHz IF signal which appears at the discriminator output.

2.3.1 Frequency Discriminator

The 4-level FM simulation employs a standard frequency discriminator as the system's FM demodulator. This was done to provide increased demodulator bandwidth which was not readily obtainable using the phase lock loop demodulator. A typical discriminator characteristic appears below in Figure 48.

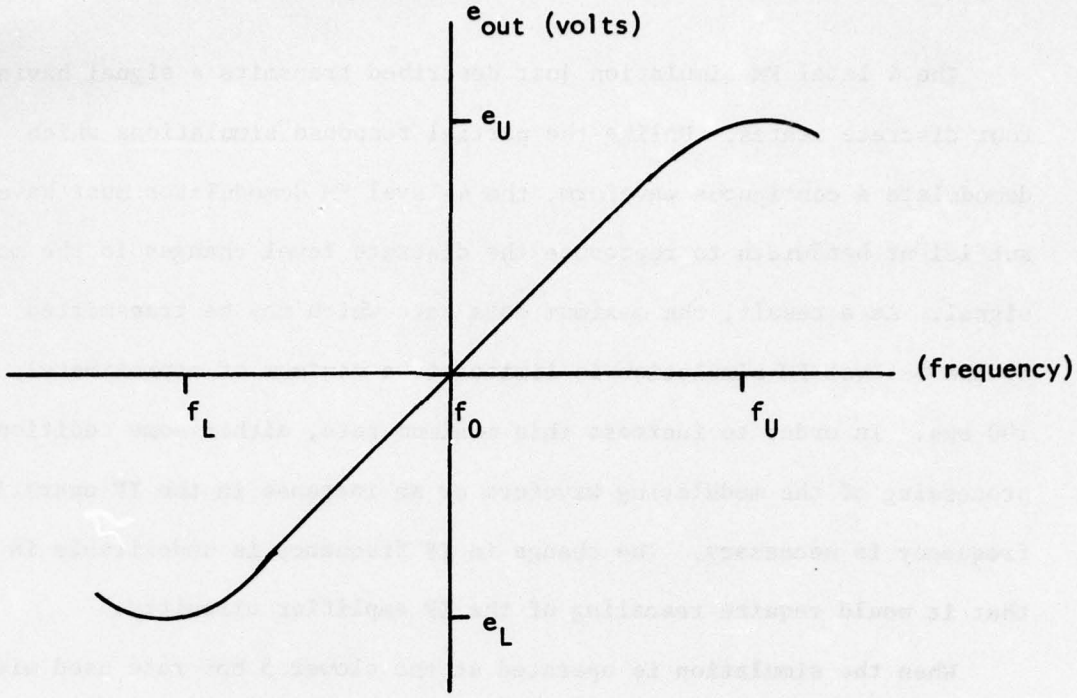


Figure 48 Discriminator Characteristic

The discriminator shown in Figure 49 may be discussed as three functional blocks. The feedback loops composed of 2A75, 76, 105, and 2A80, 101, 110 each form simple second order bandpass filters which are tuned to the discriminator corner frequencies f_U and f_L. To obtain the dc signal proportional to frequency, the outputs of these filter sections are squared by multipliers 2M83 and 2M113. The positive multiplier outputs are combined to give an output at 2A86 whose dc level is proportional to frequency. Since the output of 2A86 contains a large signal component at the IF frequency, additional filtering is required to obtain a clean dc level. This is accomplished by the addition of a lowpass filter at the output of 2A86. It is the bandpass of this filter which determines the overall discriministic bandwidth. The design trandeoffs between filter

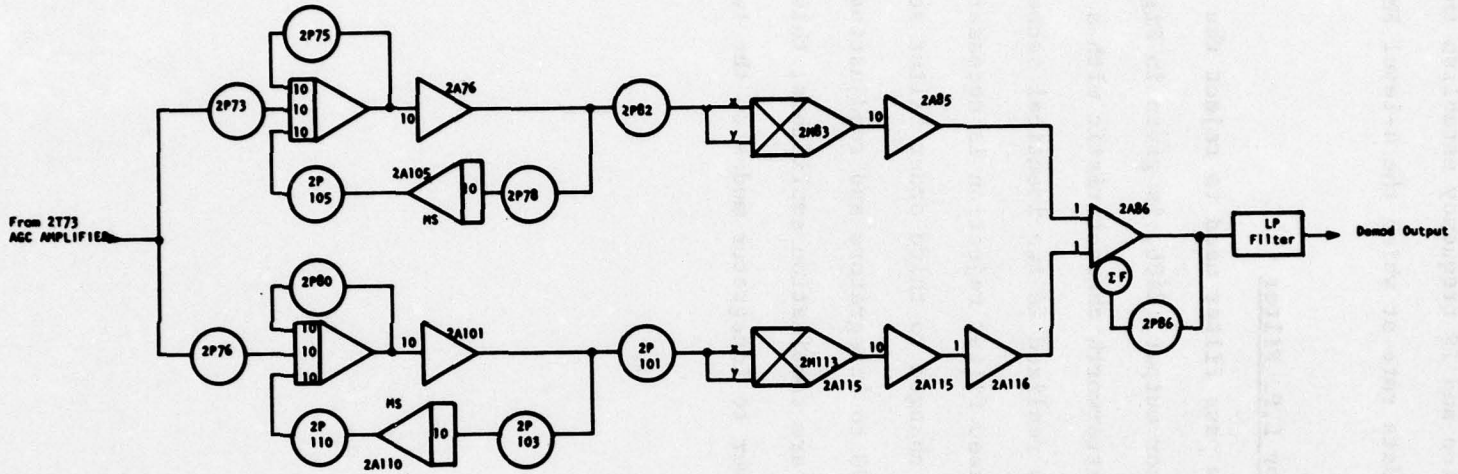


Figure 49 Frequency Discriminator (f_0 at 5 kHz)

bandwidth, stopband attenuation and IF frequency establish the upper limit on the maximum useful data rate at which the 4-level FM system may be operated.

2.3.2 Frequency Discriminator L.P. Filter

The circuitry of the low pass filter used to reject the IF signal components at the discriminator output, 2A86, is given in Figure 50. The filter has a four pole Butterworth characteristic with a 3 db bandwidth of approximately 1 KHz and is realized in two identical second order cascaded sections. If increased filter rejection is necessary, the second order sections may easily be changed to third order filter sections by changing summers 2A30 and 2A90 to integrators and readjusting potentiometer values. Since 2A30 and 2A90 are combination amplifiers, this change only requires replugging from summer to integrator modes on the two amplifiers.

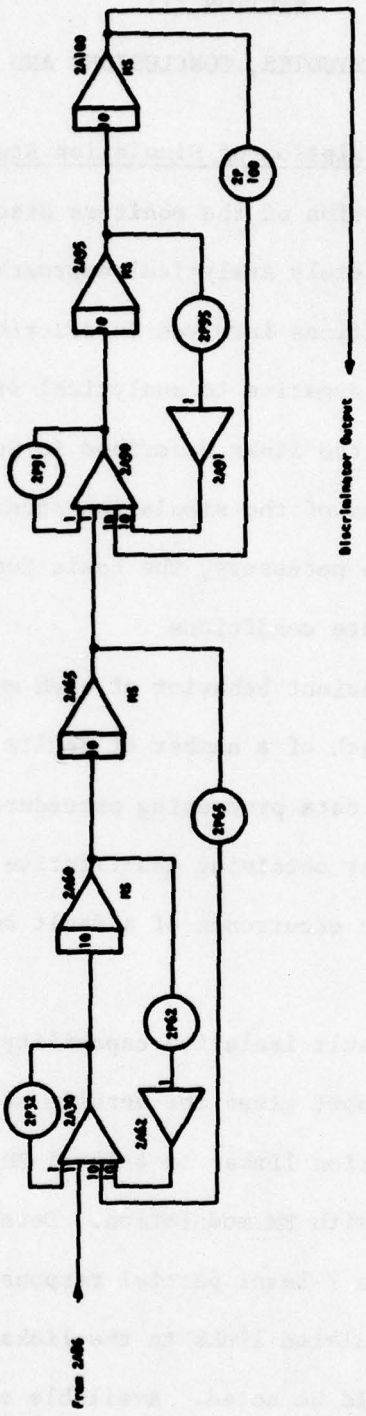


Figure 50 Frequency Discriminator Low Pass Filter

SECTION III

RESULTS OF SIMULATION STUDIES, CONCLUSIONS AND RECOMMENDATIONS

3.1 Description of Simulation Studies

A quantitative evaluation of the monitors discussed in Section I is not feasible using a completely analytical approach, because of the number and complexity of the equations involved in describing the system and the monitors. Thus, as an alternative to analytical studies, the monitors are evaluated using the simulated links described in Section II.

The general objectives of the simulation studies are the following:

(1) To verify, where necessary, the basic functioning of each monitor under steady state conditions

(2) To test the transient behavior of each monitor following the occurrence of each of a number of faults

(3) To evaluate the data processing procedure, proposed for the error rate monitors, by obtaining quantitative data on the average time between the occurrence of a fault and the time a threshold is exceeded

(4) To verify the fault isolation capability of a group of monitors.

Section II of the report gives the details of hybrid computer simulations of two types of communication links: a 4-level FM link and a link using 7-level partial response with FM modulation. Detailed simulation studies were carried out using the 7-level partial response system.

In comparing the simulated links to the links discussed in Section 1.0, the following points should be noted. Available equipment and feasible

run times limit the simulation study to one transmitter, channel and receiver of a typical link. Thus, multiple information inputs and the TDM multiplex hierarchy are not simulated. However, in an attempt to partially account for the effects of multiple channels, framing bits are added to the simulated bit stream and an attempt is made to simulate the loss of bit integrity.

As discussed in Section II four types of monitors are implemented and used in the simulation studies, namely:

(1) a pseudo-error monitor with a variable width band about each of the seven slicer levels

(2) a format violation monitor indicating outputs exceeding three

(3) the same format violation monitor indicating outputs exceeding seven

(4) an out of frame indication.

A running sum data processing method, as discussed in Section 1.3, is used with the pseudo-error and format violation greater than three monitors.

Twelve specific fault conditions are simulated. Eight of the conditions can be identified with six of the eleven generic faults identified in Section I. The simulated faults, and the generic fault to which each is most similar, are listed in Table 12. Two sets of no fault conditions are simulated, namely:

(SNF1) normal signal power, small amount of noise power

(SNF2) normal signal power, no noise power.

Table 12 Description of Simulated Faults

	Description of Simulated Fault	Number and Description of Most Similar Generic Fault
(SF1)	FM carrier frequency offset, no noise	(1) low signal power, normal noise power
(SF2)	FM carrier frequency offset, normal noise power	
(SF3)	Increase in noise power, constant signal power	(2) Normal signal power, high noise power
(SF4)	Periodic increases in noise power for short bursts, constant signal power	
(SF5)	Loss of IF signal	(3) Loss of signal, normal noise power
(SF6)	Off channel interference from single frequency tone plus noise	(4) High additive interference
(SF7)	Inversion of polarity of selected samples of the 7-level signal	(7) Loss of bit integrity at multiplexed analog signal
(SF8)	Sampling time offset	(9) Loss of bit synchronization
(SF9)	Off-channel interference, no noise power	No comparable generic fault
(SF10)	Loss of RF signal, no noise power	No comparable generic fault
(SF11)	Loss of FM demodulator VCO, no noise power	No comparable generic fault
(SF12)	Loss of receiver VCO, relatively high noise power	No comparable generic fault

In preliminary simulation studies each of the four monitors and the fault simulations were checked out. The principal portion of the work is concerned with transient type monitor evaluations. In the typical transient type experiment, all monitors are applied to the simulated system. The systems inputs are applied until normal steady state operation is reached and then at some reference time a predetermined change in conditions is made to simulate a specific fault. After the fault, all monitor outputs are recorded for each signaling interval along with the running sum output for the pseudo-error and format violation greater than three monitors. The run is continued for a predetermined time after the fault.

Specific results of the simulation studies are summarized in the next section.

3.2 Results of Simulation Studies

All four of the monitors used in the simulation study were checked out under steady state conditions and found to work satisfactorily. The pseudo-error monitor performance was determined as a function of its parameter. The results are given as curves of pseudo-error rate versus true error rate for varying C/N in Figure 51 and pseudo-error rate as a function of the width of the pseudo-error band in Figure 52.

A number of transient monitor studies, involving the responses of the monitors after a fault, were conducted. In a typical study, after steady state is reached, a particular fault is applied and the direct responses of the monitors are recorded on a stripchart. The running sums, using a value of K equal to 30, for the pseudo-error monitor and for the format violation, greater than 3, monitor are also recorded and compared to

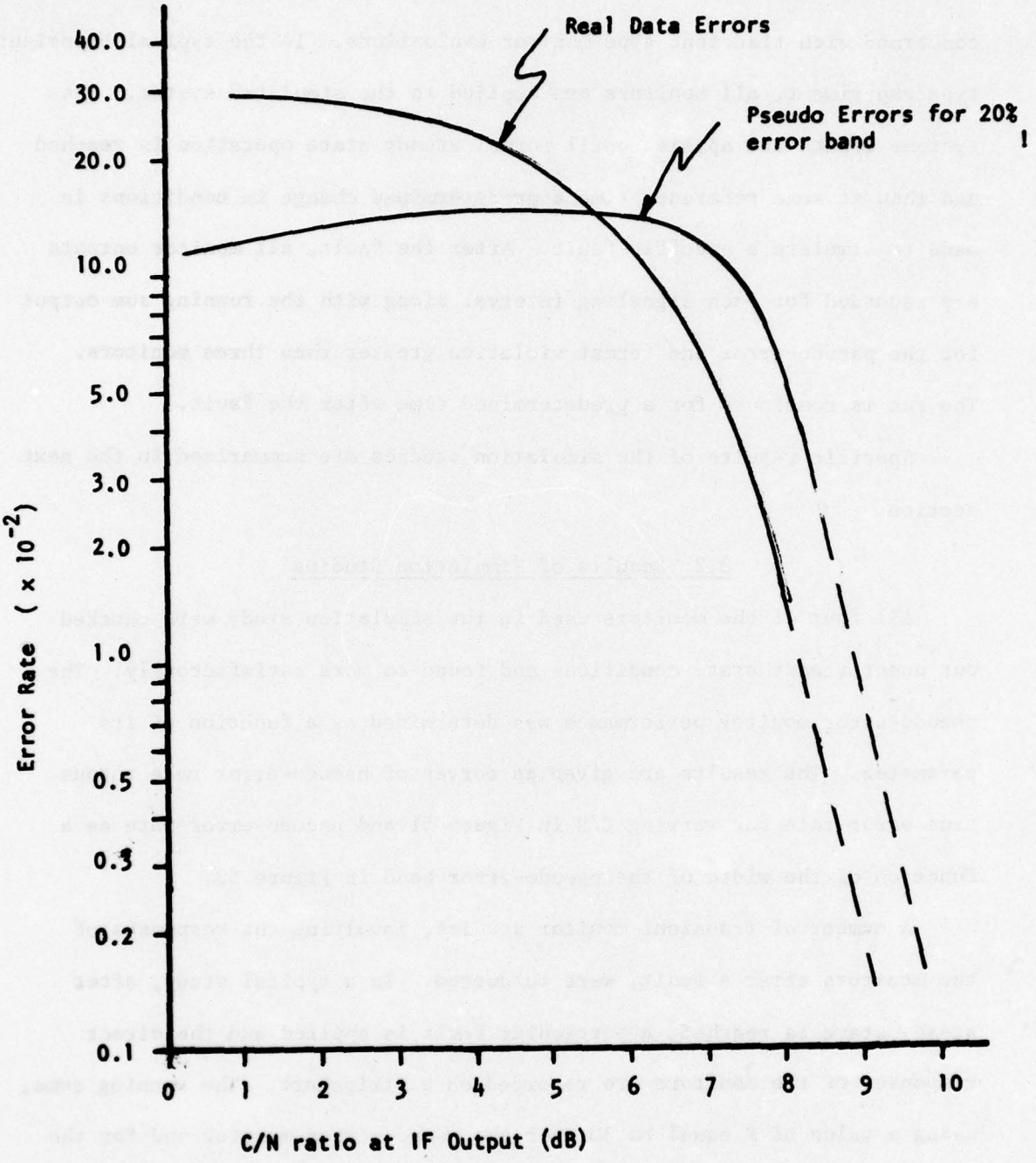


Figure 51 Pseudo-Error Monitor Rate For Varying Band Spacing

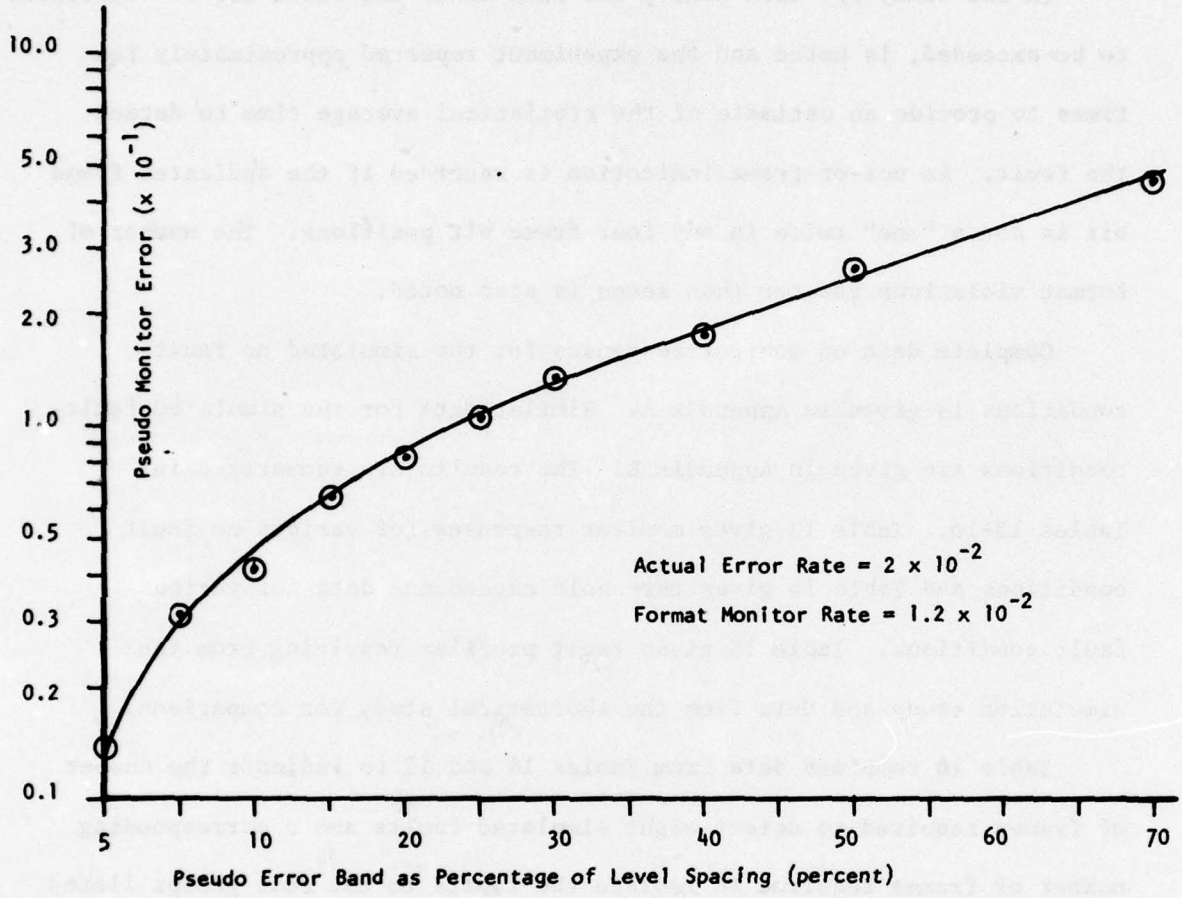


Figure 52. Pseudo Error Monitor Rate for Varying Band Spacing.

a threshold, T, taken to be 1.5. A representative section of the stripchart recorder output is given in Figure 53.

In the study for each fault, the time after the fault for the threshold to be exceeded, is noted and the experiment repeated approximately ten times to provide an estimate of the statistical average time to detect the fault. An out-of-frame indication is recorded if the dedicated frame bit is not a "one" twice in any four frame bit positions. The number of format violations greater than seven is also noted.

Complete data on monitor responses for the simulated no fault conditions is given in Appendix A. Similar data for the simulated fault conditions are given in Appendix B. The results are summarized in Tables 13-16. Table 13 gives monitor responses for various no fault conditions and Table 14 gives threshold exceedance data for various fault conditions. Table 15 gives fault profiles resulting from the simulation study and data from the theoretical study for comparison.

Table 16 combines data from Tables 14 and 15 to indicate the number of frames required to detect eight simulated faults and a corresponding number of frames required to isolate the faults to the four groups listed in the table. The results of Table 16 are indicative of what is possible. However, it should be emphasized that the table is constructed using only the monitors for which threshold exceedance, (or similar), data was taken and that the numbers, though possibly typical, depend strongly on the parameters used in the simulation study.

An analysis of the results is made in the next section of the report. It is appropriate, however, at this point to comment on the results for several faults as presented in Table 14.

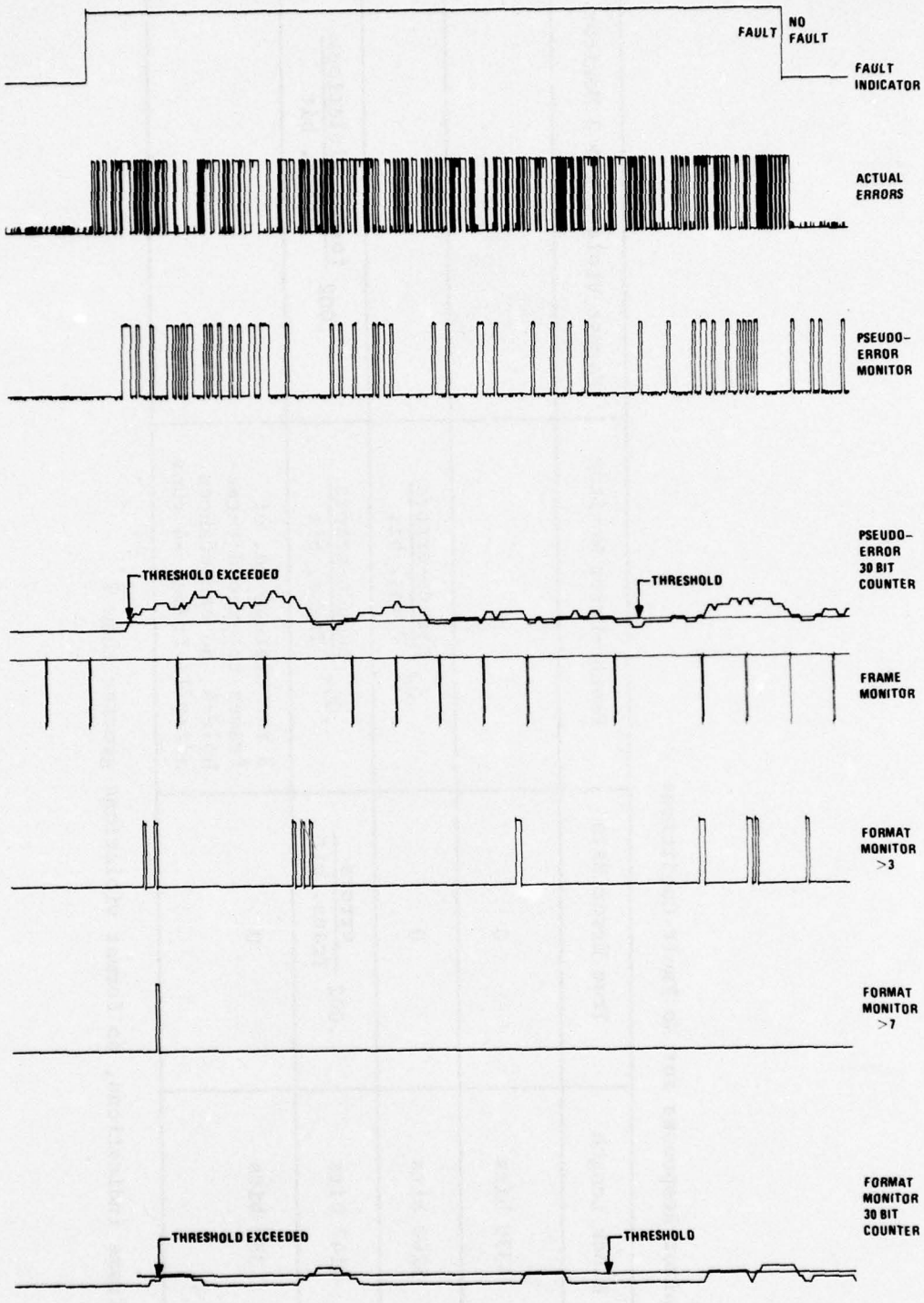


Figure 53. Typical Transient Monitor Outputs.

Table 13 Monitor Responses for No Fault Conditions

S/N	Block Length	True Error Rate	Pseudo-Error Monitor	Format Violation > 3 Monitor
12 db.	330 bits	0	0	0
10.7 db.	3200 bits	0	.03 $\frac{\text{pseudo-errors}}{\text{Trans. bit}}$	0
9.16 db.	4147 bits	.002 $\frac{\text{errors}}{\text{Trans. bit}}$	.004 $\frac{\text{pseudo-errors}}{\text{Trans. bit}}$	.002 $\frac{\text{format violations}}{\text{Trans. bit}}$
8.4 db.	330 bits	0	3 run average no. of frames to exceed threshold-4, no exceedances after 11 frames -4 runs	0

No out-of-frame indications, no format violations greater than 7

Table 14 Summary of Average Number of Frames for Threshold Exceedances for Various Faults

Fault Condition	Average no. of frames for Threshold Exceedance	
	Pseudo-error Monitor	Format Violation > 3 Monitor
SF1-no noise, FM carrier offset	2.5	No exceedance - 9 runs 1 run average-19
SF2-normal noise, FM carrier offset	2.0	4
SF3-increase in noise power 10.7 - 8 db.	2.1	No exceedance - 2 runs 6 run average-12
SF3-increase in noise power 12 - 7.4 db.	5.0	No exceedance - 1 run 8 run average-11.6
SF4-periodic increase in noise power	4.0	8
*SF5-loss of IF signal	1	2.2
*SF6-off channel interference single tone - plus noise	1.1	No exceedance - 1 run 8 run average-3.8
SF7-inversion of polarity 7-level signal	No exceedances - 9 runs 1 run average-10	1
*SF8-sampling time offset	1.1	1.1
SF9-off channel interference, no noise	No exceedances, no true errors	No exceedances - no true errors
*SF10-loss of RF signal, no noise	No exceedances	No exceedances
*SF11-loss of FM demod VCO, no noise	No exceedances	No exceedances
*SF12-loss of receiver VCO, with noise	No exceedances	No exceedances

*Note: true error rate extremely large (greater than 1 in 3)

Table 15 Fault Profiles from Simulation Study

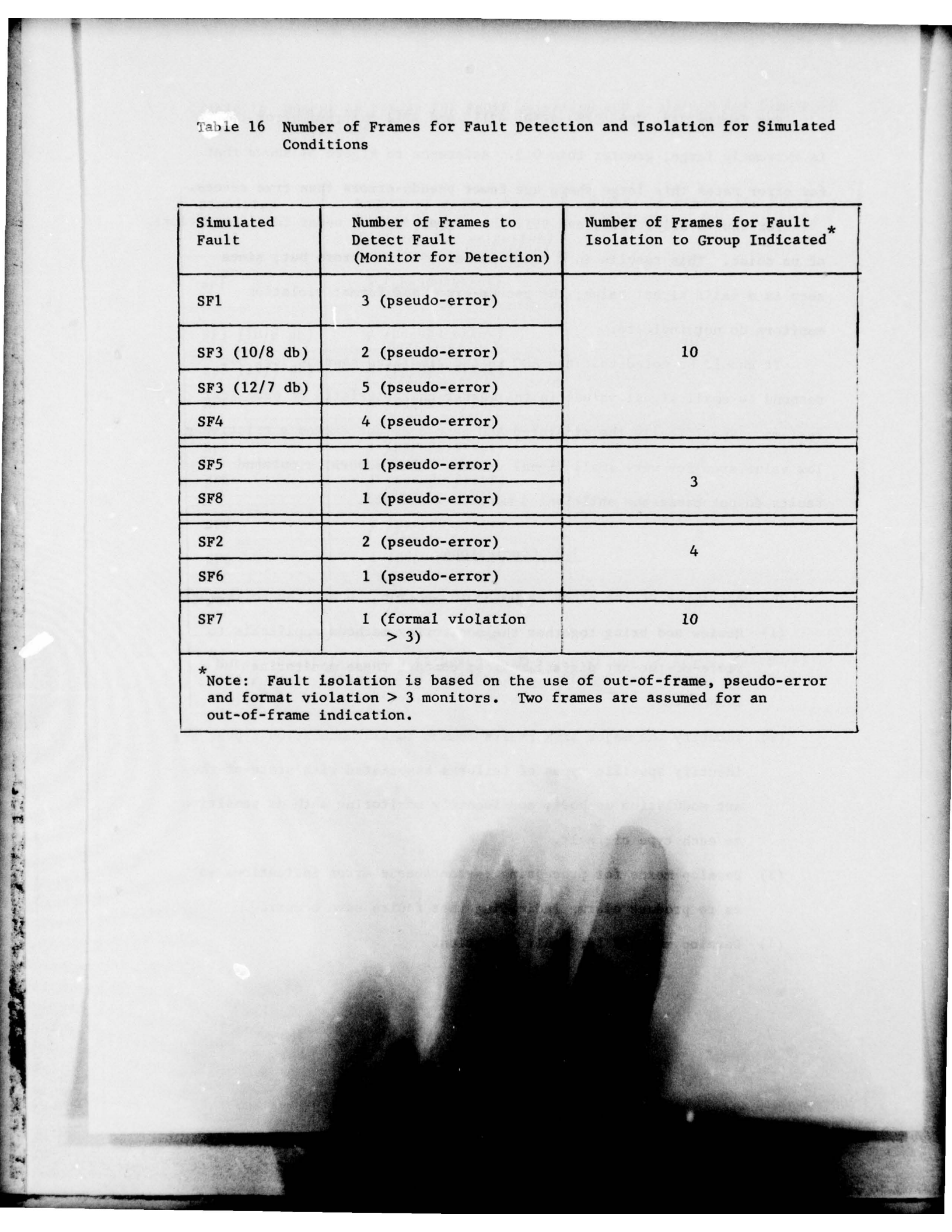
Fault (number and description of generic fault)	Monitor					
	Out-of-frame indication		Pseudo-error		Format Violation	
					> 3	> 7
(2) Normal signal, high noise SF3, SF4	No	(Yes)	SF3 - H SF4 - H	(H)	SF3 - L SF4 - L (H)	SF3 - L SF4 - L (L)
(3) Loss of signal, normal noise SF5	Yes	(Yes)	H	(H)	H (H)	L (H)
(1) Low signal, normal noise SF1 , SF2	No	(Yes)	SF1 - H SF2 - H	(H)	SF1 - L SF2 - H (H)	SF1 - L SF2 - L (L)
(4) High additive interference SF6	No	(Yes)	H	(H)	H (H)	L (L)
(9) Loss of bit synchronization SF8	Yes	(Yes)	H	(H)	H (H)	H (H)
(7) Loss of bit integrity at multilevel analog signal SF7	No	(Yes)	L	(L)	H (H)	H (H)

Note: Parenthetical entry in table gives reading from theoretical study summarized in Table 7.

Table 16 Number of Frames for Fault Detection and Isolation for Simulated Conditions

Simulated Fault	Number of Frames to Detect Fault (Monitor for Detection)	Number of Frames for Fault Isolation to Group Indicated*
SF1	3 (pseudo-error)	10
SF3 (10/8 db)	2 (pseudo-error)	
SF3 (12/7 db)	5 (pseudo-error)	
SF4	4 (pseudo-error)	
SF5	1 (pseudo-error)	3
SF8	1 (pseudo-error)	
SF2	2 (pseudo-error)	4
SF6	1 (pseudo-error)	
SF7	1 (formal violation > 3)	10

*Note: Fault isolation is based on the use of out-of-frame, pseudo-error and format violation > 3 monitors. Two frames are assumed for an out-of-frame indication.



For faults SF5, SF6, SF8, SF10, SF11, and SF12 the true error rate is extremely large, greater than 0.3. Reference to Figure 51 shows that for error rates this large there are fewer pseudo-errors than true errors.

For faults SF10, SF11, and SF12 the signal is lost under ideal conditions of no noise. This results in a large number of true errors but, since zero is a valid signal value, the pseudo-error and format violation monitors do not indicate.

It should be noted that the AGC in the simulated systems does not respond to small signal values in the manner characteristic of practical systems. Specifically the simulated AGC gain does not exceed a relatively low value even for very small signal values. Thus several simulated faults do not cause the anticipated monitor responses.

3.3 Conclusions

The objectives of the study as noted in Section 1.0 are the following:

(1) Review and bring together the monitoring methods applicable to state-of-the-art digital ratios; compare these monitoring techniques.

(2) Identify the major link faults common to all modulation types; identify specific types of failures associated with state-of-the-art modulation methods; and identify monitoring methods sensitive to each type of fault.

(3) Develop means for processing instantaneous error indications so as to produce alarms indicating that faults have occurred.

(4) Develop methods for fault isolation.

Conclusions will be drawn with respect to each of these objectives in turn.

Objectives 1 and 2: A literature review was carried out and six general types of monitors are identified. From a fairly large number of possible implementations of these six general types of monitors, six specific implementations are chosen for detailed study.

Three general subsystems, used in every digital communication link, are identified and major faults for each subsystem are listed in Sections 1.1.1, 1.1.2 and 1.1.3. Eleven generic faults conditions produced by these major faults are established and given on pages 11 and 12. In Section 1.5 four-level FM, seven-level partial response/FM and quadrature partial response systems are considered for specific faults, with the conclusion that the major faults for these systems are included in the eleven previously noted.

The response of each of the six monitors to each of the eleven generic faults are worked out in detail in Section 1.6.2 and the results are summarized in Tables 4, 5, 6, and 7. As a part of this study a theoretical investigation of the behavior of the format violation monitor for seven-level partial response is made. The operation of a format violation monitor indicating outputs greater than 3 is analyzed and a monitor with different characteristics is developed by indicating readings greater than 7. The new monitor is analyzed in Section 1.4.2.

The pseudo-error, the format violation greater than 3 and the format violation greater than 7 monitors are studied in detail through simulation with results given in Section 3.2, Tables 13 and 15, and Appendixes A and B. The out-of-frame type of monitor behavior is approximated in the simulation study and the results are also given in Tables 13 and 15. Table 15 gives results from the theoretically derived Table 7 for purposes of comparison.

With reference to Table 15, the theoretical and simulated readings for the pseudo-error monitor are in close agreement for all faults considered. For the format violation greater than 3 monitor, agreement is obtained between the theoretical results and the simulation results for four out of six faults. Lack of agreement for two faults, both involving low ratios of signal to noise, is explained by two facts. First, it was necessary to carry out the simulation study at true error rates orders of magnitude greater than would be experienced in practice. This results in a greatly increased probability of compensating errors in the format violation monitor with a consequent low reading. A second fact accentuates the error compensation, namely, the true errors in the simulation occurred in bursts which seem to be uncharacteristic of true Gaussian noise.

For the format violation greater than 7 monitor, agreement between theoretical and simulated results is obtained for all but fault (3) - loss of signal, normal noise. A high reading is given theoretically because of AGC action in amplifying the noise. In the simulation study the AGC did not provide as high a gain as would be normal in practice so that the two results are effectively for different conditions.

The poor agreement between the theoretical and simulated results for the out-of-frame indication can be explained by several different factors. For fault (7) - loss of bit integrity, the simulation was merely a reversal of the polarity of every twenty fifty bit in the 7-level signal. This adequately approximates loss of bit integrity for the format violation monitors but does not produce the desired effect for the out of frame monitor, since only one bit out of every twenty five is affected.

For faults (2), (1) and (4) either a large noise or an interfering signal causes the fault. Clearly whether or not the out-of-frame indicator reads will depend on the number of frame bits which are rendered in error

by the noise or interference and also on the algorithm for indicating out-of-frame. In the simulation the noise and interference power had less effect than that assumed in obtaining the theoretical results.

It can be noted from Table 15 that of the six generic faults simulated, five result in a high reading from the pseudo-error monitor. The remaining one, fault (7), is indicated by a high reading of either of the format violation monitors. From theoretical considerations it would seem that fault (7) will also cause an out-of-frame indication.

From theoretical considerations faults (11), (5) and (10) will cause either a high or a medium level reading of the pseudo-error monitor. The remaining two faults, (6) and (8) are indicated by an out-of-frame indication.

In summary, the pseudo-error and out-of-frame monitors together will indicate the presence of all of the eleven generic faults.

Objective 3: In Section 1.3 the theoretical background is developed for a technique for processing the output of either the pseudo-error or format violation monitors. A simple running sum over K past bits accomplishes the desired result. The parameter K and the threshold, T, to which the running sum is compared, are related to the two probabilities characterizing the test, namely the probability of false alarm and the probability of correct detection of a fault. The probabilities of an indication from the monitor under fault and no fault conditions must also be given.

For the simulation study K and T are determined for 95% probability of correct detection and 5% probability of false alarm. The results of the test using these values are given in Table 14 for all of the simulated faults and in Table 13 for several no fault conditions.

The data in Table 13 indicates that an alarm based on a running sum with K = 30 and T = 1.5 would give no false alarm, for either the pseudo-error or format violation greater than 3 monitors, if normal operation corresponds to a signal-to-noise ratio as high as 12 db. Further examination of the data in the table indicates that few false alarms would result from either monitor for normal operation at S/N ratios of 9.16 db. and higher. At a normal S/N ratio of 8.4 db. the pseudo-error monitor gives too many false alarms while the format violation monitor result is still satisfactory.

Table 14 shows that an alarm based on the running sum output of the pseudo-error monitor will appropriately indicate the presence of all of the faults to which this monitor responds. The average number of frames before detection for all of the faults is 2.4, with the maximum being 5 and the minimum being 1.

Consideration of the format violation greater than 3 monitor shows, generally, a larger number of frames to indicate the presence of faults to which this monitor is sensitive because of the "error amplification" obtained with the pseudo-error monitor. Note that fault SF7, which simulates loss of bit integrity for the seven-level partial response signal, causes a rapid indication from this monitor.

In summary, the simulation results are consistent with the theory and demonstrate the feasibility of an alarm based on a running sum of either the pseudo-error or format violation greater than 3 monitor outputs. The parameters of the monitor, which must be tailored to the characteristics of a specific system, can be determined from theoretical considerations presented in this report.

Objective 4: Fault profiles in terms of monitor readings are given for theoretical results in Table 7 and for simulated results in Table 15. With the exception of the action of the format violation greater than 3 monitor for faults involving high noise, the theoretical monitor behavior is substantiated by the results of the simulation study. The reason for discrepancies is adequately explained above.

Results for the out-of-frame indication are less conclusive due to difficulties in simulating loss of bit integrity, as discussed above. Even for this case the results of the simulation study are not inconsistent with the theoretical results, although they do not support them in as positive a manner as for the pseudo-error and format violation monitors.

Given the few reservations stated above, it can be concluded that the theoretical results of Table 7 are substantiated by the simulation study and the conclusions of Section 1.6.3 can be taken as valid. These conclusions can be restated as follows. The four monitors

out of band noise

signal power

pseudo-error

format violation greater than 7

will uniquely identify nine faults and one pair of faults out of the eleven generic faults under consideration, given that a fault is known to have occurred. Examination of the entries in Table 7 shows that normal readings result from all four monitors for faults (6) and (8). Thus to determine that a fault has indeed occurred, (in addition to isolating it from other possible faults), the out-of-frame monitor must be added since it is the one monitor giving a nonnormal reading for these faults.

Finally, for non partial response systems as discussed in Section 1.6.3, three of the above monitors, excluding the format violation monitor, will distinguish seven fault groups: four containing a single fault, two containing two faults and one containing three faults.

3.4 Recommendations

As a result of this study it is recommended that five monitors be used with seven-level partial response/FM systems, namely:

out-of-band noise

signal power

pseudo-error

format violation greater than 7

out-of-frame indication

This combination of monitors will detect all eleven generic faults and provide fault isolation between nine individual faults and one pair of faults out of the eleven faults.

It is further recommended that a fault alarm be provided by processing the output of the pseudo-error monitor with a running sum algorithm using values of K and T tailored to the particular system. Such an alarm will provide a prompt indication of eight of the eleven generic faults after they occur. With proper tailoring of the parameters, including the pseudo-error band, an advanced indication of degraded conditions can be obtained for some faults.

The format violation greater than 7 monitor cannot be used with four-level FM. Thus this monitor must be deleted for such systems but the other recommendations remain the same as for partial response systems.

The absence of the format violation monitor, of course, decreases the amount of fault isolation possible but does not offset the ability to detect all eleven generic faults.

For quadrature partial response (QPR) systems, a direct use of the format violation greater than 7 monitor is also not possible. In this case, however, further study is recommended to find another format violation monitor appropriate to this system. In this connection, consideration should be given to the monitor described by Lender [26].

Use of the four monitors recommended for four-level FM with the QPR system should give results analogous to that for FM.

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APPENDIX A

MONITOR RESPONSES FOR SIMULATED NO FAULT CONDITIONS

No Fault: SNF1 - S/N = 8.4 db.

Parameters: 10% pseudo-error band

In a typical 330 bit block there were:

0 true errors

1 pseudo-errors

0 format violations > 3

Pseudo-error		Format Violation > 3	
Number of frames before *threshold* exceeded	Number of Runs	Number of frames† before *threshold* exceeded	Number of Runs
1	1		
2	1		
9	1	no format violations	
No threshold exceedances after 11 frames	1		
Average			
Relative Monitor Reading	Low	Relative Monitor Reading	Low

† In the simulation studies for which data is given in Appendices A and B the duration of one bit is 1.1 ms and of one frame is 33 ms. The time scale factor for the simulation study is 1.4×10^3. Thus the frame duration in the actual system being simulated is approximately 24 microseconds.

No Fault Condition: SNF1 - S/N = 10.7 db.

no true errors, no format violations, 96 pseudo-errors in 3200 bits

Relative Monitor Readings: low

No Fault Conditions: SNF1 - S/N = 9.16 db.

number of true errors = 7

number of format violations = 8

number of pseudo-errors = 16

number of bits = 4147

Relative Monitor Readings: low

No Fault Condition: SNF1 - S/N = 12 db.

Notes: 10% pseudo error band

no true errors, pseudo-errors or format violations in blocks on the order of 330 bits

Relative Monitor Readings: low

No Fault Condition: SNF2 - no noise power, normal signal power

no true errors

pseudo-error load 70% - large number of errors

pseudo-error load 50% - no pseudo-errors

APPENDIX B

MONITOR RESPONSES FOR SIMULATED FAULT CONDITIONS

Fault: SF1 - no noise, FM carrier frequency offset, 0.106 volts output level change

Typical out-of-frame indication - No

In a typical 690 bit block there were:

0 true errors

26 pseudo-errors

1 format violations > 3

Pseudo-error		Format Violation > 3	
Number of frames before threshold exceeded	Number of Runs	Number of frames before threshold exceeded	Number of Runs
less than 1	1	19	1
1	2	no threshold exceedances after frames	9
2	3		
3	2		
5	2		
Average 2.5			
Relative Monitor Reading	Low	Relative Monitor Reading	Low

Fault: SF2 - FM carrier frequency offset, normal noise power

Parameters: FM carrier frequency offset 0.106 volts at output S/N = 9.16 db

Typical out-of-frame indication - No

In a typical 690 bit block there were :

34 true errors

44 pseudo-errors

19 format violations > 3

1 format violation > 7

Pseudo-error		Format Violation > 3	
Number of frames before threshold exceeded	Number of Runs	Number of frames before threshold exceeded	Number of Runs
less than 1	1	less than 1	1
1	4	1	2
2	2	2	2
3	1	3	1
6	1	4	1
		5	2
		13	1
Average 2		4	
Relative Monitor Reading	High	Relative Monitor Reading	High

Fault: SF3 - Increase in noise power, constant signal power

Parameters: no fault S/N = 10.7 db., fault S/N = 8.0 db.

One out of eight runs has out-of-frame indication

In a typical 780 bit block there were:

20 true errors

21 pseudo-errors

7 format violations > 3

Pseudo-error		Format Violation > 3	
Number of frames before threshold exceeded	Number of Runs	Number of frames before threshold exceeded	Number of Runs
less than 1	3	4	1
2	3	5	2
4	2	17	1
		20	1
		21	1
		no threshold exceedance after 23 frames	2
Average 2.1			
Relative Monitor Reading	High	Relative Monitor Reading	Low

Fault: SF3 - Increase in noise power, constant signal power

Parameters: no fault S/N = 12 db., fault S/N = 7.4 db.

Notes: 10% pseudo-error band

Typical out-of-frame indication - No

In a typical 1170 bit block there were:

27 true errors

28 pseudo-errors

14 format violations > 3

Pseudo-error		Format Violation > 3	
Number of frames before threshold exceeded	Number of Runs	Number of frames before threshold exceeded	Number of Runs
1	1	3	2
2	1	7	2
3	2	8	1
4	2	13	1
6	2	19	1
7	1	33	1
8	1	no threshold exceedance after 21 frames	3
12	1		
Average 5			
Relative Monitor Reading	High	Relative Monitor Reading	Low

Fault: SF4 - periodic increases in noise power for short bursts, constant signal power

Parameters: burst length 2 seconds, S/N changed from 10.7 db. to 8 db.

Typical out-of-frame indication - No

In a typical 810 bit block there were:

20 true errors

19 pseudo-errors

9 format violations > 3

Pseudo-error		Format Violation > 3	
Number of frames before threshold exceeded	Number of Runs	Number of frames before threshold exceeded	Number of Runs
less than 1	2	2	1
1	1	3	3
2	1	7	1
3	2	8	1
5	1	10	1
6	1	17	1
14	1	19	1
Average 4		8	
Relative Monitor Reading	High	Relative Monitor Reading	Low

Fault: *SF5 - loss of IF signal*

Parameters: S/N = 7.58 db.

Typical out-of-frame indication - Yes

In a typical 630 bit block there were:

530 true errors

82 pseudo-errors

23 format violations > 3

1 format violation > 7

Pseudo-error		Format Violation > 3	
Number of frames before threshold exceeded	Number of Runs	Number of frames before threshold exceeded	Number of Runs
less than 1	10	less than 1	2
		1	2
		2	4
		4	1
		6	1
Average 1		2.2	
Relative Monitor Reading	High	Relative Monitor Reading	High

Fault: SF6 - off-channel interference from single frequency time plus noise

Parameters: off-channel interference 6.74 volts at a frequency of 4900 hz,

S/N = 8.4 db.

One out of ten has out-of-frame indication.

In a typical 210 bit block there were:

62 true errors

36 pseudo-errors

13 format violations > 3

Pseudo-error		Format Violation > 3	
Number of frames before threshold exceeded	Number of Runs	Number of frames before threshold exceeded	Number of Runs
less than 1	7	1	2
1	2	2	1
2	1	3	1
		4	1
		6	2
		7	1
		no threshold exceedances after 7 frames	1
Average 1.1			
Relative Monitor Reading	High	Relative Monitor Reading	High

Fault: SF7 - inversion of polarity of selected samples of the 7-level signal

Parameters: inverted samples occurrred at rate of $\frac{1}{125}$, S/N = 9.16 db.

Typical out-of-frame indication - No

In a typical 780 bit block there were:

14 true errors

3 pseudo-errors

30 format violations > 3

11 format violations > 7

Pseudo-error		Format Violation > 3	
Number of frames before threshold exceeded	Number of Runs	Number of frames before threshold exceeded	Number of Runs
10	1	less than 1	9
no threshold exceedances after 20 frames	9	1	1
Average		1	
Relative Monitor Reading	Low	Relative Monitor Reading	High

Fault: SF8 - sampling time offset

Parameters: sample time set early, S/N = 9.16 db.

Typical out-of-frame indication - Yes

In a typical 690 bit block there were:

590 true errors

63 pseudo-errors

73 format violations > 3

16 format violations > 7

Pseudo-error		Format Violation > 3	
Number of frames before threshold exceeded	Number of Runs	Number of frames before threshold exceeded	Number of Runs
less than 1	8	less than 1	5
1	2	1	5
2	1	2	1
Average 1.1		1.1	
Relative Monitor Reading	High	Relative Monitor Reading	High

Fault Condition: SF9 - no noise, 0.74 volts peak off-channel interference at a frequency of 4900 hz.

no true errors, pseudo-errors or format violations in blocks of 540 bits

Relative Monitor Readings: low

Fault Condition: SF10 - loss of RF signal, no noise

large number of true errors

no pseudo-errors or format violations in 570 bit blocks

Relative Monitor Readings: low

Fault Condition: SF11 - loss of FM demodulator VCO, no noise

large number of true errors

no pseudo-errors or format violations in 720 bit blocks

Relative Monitor Readings: low

Fault Condition: SF12 - loss of VCO in receiver phase lock loop, S/N = 7.58 db.

large number of true errors

no pseudo-errors or format violations

out-of-frame indication every 2 frames

Relative Monitor Readings: low

APPENDIX C

Simulation Set Up Procedures

This appendix is intended to aid anyone desiring to set up and operate any of the three simulations discussed in Part 2 of this report. It is assumed that all pots[1] on consoles one and two have been set, all oscillators connected, and appropriate digital program loaded into the DCD 1700. For the three-level partial response simulations, the digital program FPSEUD should be loaded. The program FDATA2 should be loaded for the 7-level partial response and 4-level FM simulations.

If the potentiometers on console 4 are to be set manually, the following procedure is recommended.[2]

1. Place the logic mode control switch of console 4 to stop (S) mode.
2. Set all flip-flops on console 4 high.
3. Set pots according to standard procedures.
4. Place console 4 in operate mode and check the outputs of amplifiers 4A04, A34, A64, A94, A09, A39. All should indicate an output of 0.680 volts.
5. Check the output of 4A66. It should be between 2.00 and 2.10 volts. Then place flip-flop 4F3A, F4A, and GPRO all low. 4A66 should be between -2.00 and -2.10 volts. This procedure checks the operation of the 7-level sample and hold used in the format monitor.
6. Return the logic mode control switches to run mode (R).

---

[1] Pot values for all consoles are given at the end of this appendix.

[2] For the three-level partial response simulation, only console 1 is needed.

If all pots are set, the general set up procedure given below may be used. It is assumed that all patching changes necessary for a particular simulation have been made.

1. Remove noise source (+ terminal, no. 119 of console 1).
2. Set pushbuttons 1 and 2 of console 2 high if 7-level PR or 4-level FM simulation are to be run.
3. Set pushbutton 1 high on console 1 for 3-level PR simulation.
4. Set FM source to 5 KHz.
5. Set BIT timing recovery VCO (if used) to a frequency equal to the input data rate.
6. Set FM source peak amplitude to 0.75 volts peak (1PB2 console 1 high, 3.4 low and read 1A25).
7. Set FM demodulator VCO to 1.0 volts peak (1PB3 console 1 high, 2.4 low and read 1A25).
8. Ground the voltage control input to the FM source and adjust the demodulator VCO for zero output (1PB4 high, 2.3 low and read 1A25).

If the 3-level partial response simulation is to be run, refer to the set up procedure given in the previous report [9]. The remaining instructions refer to set up of the 7-level partial response simulation. The 4-level FM simulation is set up in a similar manner.

9. Disconnect sense line 5 console 2. This prevents the digital computer from sensing data errors.
10. Complete typing TTY information into the computer. Choose a test signal for initial set up as this provides a period signal which is easily monitored and also is a known signal which can be used to check for proper performance monitor operation.

Note: For a slow data rate, the signal levels are set up for display on the 8-track stripchart recorder. Button rec1, console 1, gives the performance monitor and counter output. Button rec2 gives signal waveforms at selected points in the system. For initial set up use rec2.

11. For slow speed operation, set PB5 console 1 high, for high speed operation, set PB5 low.
12. Set all monostables for their proper times. Monostable values for all simulations are given at the end of this appendix.
13. Check the partial response waveform. With a test signal, it should range between -2.0 and +1.75 volts or from -1.75 to +2.0 volts depending on precoder initial conditions. If not, adjust pot 2P55 until proper partial response levels are reached.
14. Check the output of the data comparator (already connected to stripchart for slow speed runs). It should consist of narrow pulses which can be adjusted to zero by changing recovery timing and the delay monostable 1M00.
15. Reconnect sense line 5 console 2 if it is desired to count data errors.
16. The digital program may be switched between modes by the pushbutton of console 2. To change data rate from the slow rate, momentarily place 2PB1 low. Similarly, to change from the high rate, place both 2PB1 and 2PB2 low and then return high.

For added versatility, a way of simulating the timing recovery phase lock loop and RF links have been provided as shown in Figures C-1 and C-2. The timing recovery is simulated by breaking the recovery PLL loop at the

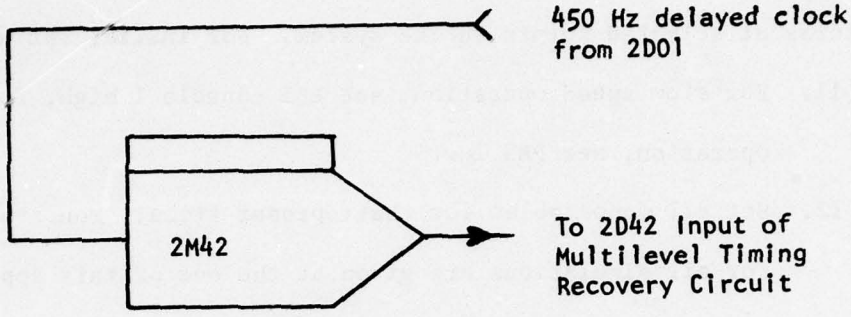


Figure C-1 Timing Recovery Simulator

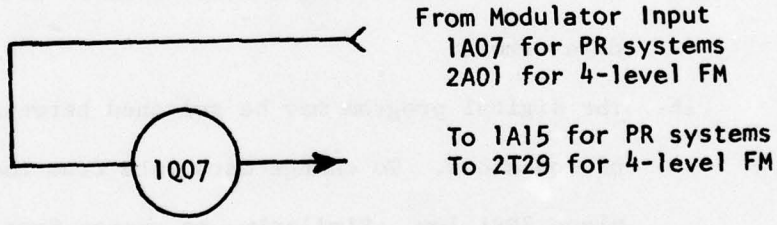


Figure C-2 RF Simulator

input to differentiator 2D42 and connecting monostable 2M42 as indicated in Figure C-1. This feature is particularly useful when running experiments in which timing jitter is to be eliminated. The monostable period of 2M42 is adjusted to provide the proper sampling point for the system decoders.

The RF simulation is achieved by disconnecting the input to the receiver partial response filter and replacing it with a potentiometer connected between the filter input and the first partial response filter output. The pot value is then adjusted to give proper amplitudes at the output of 2A55. This feature is useful for debugging and installing modifications in the simulation without having to set up the signal generators as described previously.

Potentiometer Values

Console 1:

POT	VALUE	POT	VALUE	POT	VALUE
001	0.100	030	0.290	065	0.342
002	0.240	032	0.104	067	0.342
003	0.230	035	0.350	069	0.100
004	0.200	036	0.747	070	0.200
005	0.752	037	0.522	071	0.400
006	0.591	038	0.250	072	0.200
007	0.213	040	0.500	074	0.050
008	0.055	041	0.400	075	0.911
013	0.500	044	0.050	077	0.911
014	0.050	045	0.435	080	0.560
016	0.050	046	0.002	082	0.500
017	0.152	050	0.0576	090	0.395
018	0.272	055	0.112	102	0.800
022	0.261	056	0.040	104	0.050
025	0.050	057	0.050	115	0.100
026	0.100	060	0.993	117	0.300
027	0.628	062	0.993		

Console 2:

POT	VALUE	POT	VALUE	POT	VALUE
000	0.034	035	0.068	071	0.200
001	0.100	036	0.068	074	0.100
005	0.150	039	0.120	079	0.100
006	0.068	040	0.100	084	0.075
007	0.628	044	0.170	085	0.034
010	0.034	049	0.034	090	0.100
011	0.068	050	0.020	091	0.100
013	0.010	051	0.034	092	0.995
015	0.030	052	0.034	094	0.200
016	0.100	053	0.200	095	0.639
017	0.034	055	0.5432	096	0.068
018	0.034	058	0.0200	097	0.995
019	0.050	060	0.100	099	0.200
020	0.800	062	0.639	100	0.609
022	0.800	063	0.995	102	0.034
024	0.075	064	0.110	104	0.034
030	0.034	065	0.609	109	0.170
032	0.100	066	0.068	115	0.034
033	0.995	067	0.995	117	0.200
034	0.110	070	0.100		

Console 4:

POT	VALUE	POT	VALUE	POT	VALUE
005	0.0680	036	0.0680	075	0.1612
006	0.1748	038	0.2030	080	0.0340
008	0.0680	040	0.0272	091	0.0680
010	0.0408	045	0.1088	095	0.0952
015	0.0952	049	0.0750	100	0.0408
016	0.1000	050	0.0340	104	0.1000
019	0.0750	061	0.0680	105	0.1748
031	0.0680	065	0.1088	110	0.0100
035	0.1612	070	0.0272		

Monostable Times

3-LEVEL PARTIAL RESPONSE SIMULATION

MONOSTABLE	TIME
1M00	2.0 ms
1M01	1.2 ms
1M02	1.4 ms
1M41	1.1 ms

7-LEVEL PARTIAL RESPONSE

AND

4-LEVEL FM SIMULATIONS

Monostable	Slow Speed	High Speed
1M00	155 ms	0.70 ms
2M00	40 ms	0.25 ms
2M01	250 ms	1.40 ms
2M02	0.1 ms	0.1 ms
2M40	0.1 ms	0.1 ms
2M41	90 ms	0.40 ms
2M42	110 ms	0.5 ms
4M00	0.05ms	0.05 ms

Potentiometer Settings for Pseudo Error Bands

Pot Console 4	Pseudo Error Band Percentages in Per Cent							
	5	10	15	20	25	30	40	50
6,105	.1697	.1714	.1731	.1748	.1765	.1782	.1816	.1850
35,75	.1663	.1646	.1629	.1612	.1595	.1578	.1544	.1510
65,45	.1037	.1054	.1071	.1088	.1105	.1122	.1156	.1190
95,15	.1003	.0986	.0969	.0952	.0935	.0918	.0884	.0850
10,100	.0357	.0374	.0391	.0408	.0425	.0442	.0476	.0510
40,70	.0323	.0306	.0289	.0272	.0255	.0238	.0204	.0170

APPENDIX D

SOFTWARE LISTING FOR FDATA2

```
      PROGRAM FDATA2                                                    DAT   10
C                                                                       DAT   20
C     THIS PROGRAM GENERATES RANDOM INPUTS FOR ANALOG SIMULATION        DAT   30
C                                                                       DAT   40
      DIMENSION IBIT(1), ICNT(2), IMON(2), ISAM(2)                      DAT   50
      DIMENSION JPD(500), JIF(500), JIFO(500), JIDA(500), JF3(500), JF7(DAT   60
     1500)                                                              DAT   70
      DIMENSION NP0(32), NP3(32), NP4(32), NP7(32), NSTR(5)             DAT   80
      INTEGER PSD,P0,P3,P4,P5,P6,P7                                     DAT   90
      ASSIGN 102 TO IFHI                                                DAT  100
      ASSIGN 110 TO IFLO                                                DAT  110
      ASSIGN 111 TO IPHI                                                DAT  120
      ASSIGN 126 TO IPLO                                                DAT  130
      ASSIGN 113 TO ISHI                                                DAT  140
      ASSIGN 126 TO ISLO                                                DAT  150
      WRITE (4,159)                                                     DAT  160
C                                                                       DAT  170
C     PROGRAM PROTECT SHOULD BE OFF                                     DAT  180
C                                                                       DAT  190
      WRITE (4,160)                                                     DAT  200
      PAUSE 0                                                           DAT  210
      WRITE (4,132)                                                     DAT  220
      READ (4,133) APRT                                                 DAT  230
      NPRT=APRT                                                         DAT  240
      WRITE (4,153)                                                     DAT  250
      READ (4,151) SLOW                                                 DAT  260
      ISLOW=SLOW                                                        DAT  270
      WRITE (4,152)                                                     DAT  280
      READ (4,151) TES                                                  DAT  290
      ITES=TES                                                          DAT  300
      ISQ=1                                                             DAT  310
      WRITE (4,161)                                                     DAT  320
      PAUSE 1                                                           DAT  330
C                                                                       DAT  340
C     IPER CORRESPONDS TO PULSE PERIOD / ( 5.0US )                      DAT  350
C     IPER * 5 MICROSECONDS = 1.1 MS                                    DAT  360
C                                                                       DAT  370
      IPER=220                                                          DAT  380
C                                                                       DAT  390
C     5 MICROSEC * 115 = 575 US                                         DAT  400
C     NST CORRESPONDS TO 0.5* PULSE PERIOD/( 5 US )                     DAT  410
C                                                                       DAT  420
      NST=IPER/2                                                        DAT  430
      CALL STRCLK                                                       DAT  440
      CALL CHGCLK (100)                                                 DAT  450
      ISTRT=0                                                           DAT  460
      ICNT(1)=0                                                         DAT  470
      ICNT(2)=0                                                         DAT  480
```

```
C                                                                       DAT  490
C     NBIT = NUMBER OF BITS IN A FRAME                                  DAT  500
C                                                                       DAT  510
      NBIT=30                                                           DAT  520
      NBIT1=NBIT+1                                                      DAT  530
C                                                                       DAT  540
C     JBIT IS THE BIT COUNTER FOR FRAME GENERATOR                       DAT  550
C     ZERO BIT COUNTER                                                  DAT  560
C                                                                       DAT  570
      JBIT=0                                                            DAT  580
C                                                                       DAT  590
C     1572 TIMER GENERATES A PULSE EVERY 5 MICROSECONDS                 DAT  600
C                                                                       DAT  610
  101 IF (ISLOW.GT.0) WRITE (4,154)                                     DAT  620
      IF (ISLOW) 112,112,102                                            DAT  630
  102 CALL KL1572                                                       DAT  640
      CALL CL1572                                                       DAT  650
C                                                                       DAT  660
C     SET THE BIT COUNTER                                               DAT  670
C                                                                       DAT  680
      JBIT=JBIT+1                                                       DAT  690
C                                                                       DAT  700
C     READ THE TIMER                                                    DAT  710
C                                                                       DAT  720
  103 CALL RD1572 (K)                                                   DAT  730
C                                                                       DAT  740
C     HAS 550 US ELAPSED                                                DAT  750
C                                                                       DAT  760
      IF (K+ISTRT-NST) 103,104,104                                      DAT  770
C                                                                       DAT  780
C     SAMPLE ERROR  MONITORS NEXT                                       DAT  790
C                                                                       DAT  800
C     GENERATE BIT INFORMATION FROM RANDOM NUMBER GENERATOR             DAT  810
C                                                                       DAT  820
  104 CALL IRAND (IBIT(1),1)                                            DAT  830
      L=AND(1,IBIT(1))                                                  DAT  840
      L=OR(L,40)                                                        DAT  850
C                                                                       DAT  860
C     GENERATE THE FRAME BIT                                            DAT  870
C                                                                       DAT  880
      IF (JBIT.EQ.NBIT1) L=1                                            DAT  890
      IF (JBIT.EQ.NBIT1) JBIT=0                                         DAT  900
      IF (ITES) 106,105,105                                             DAT  910
  105 IF (ISQ.EQ.1) L=1                                                 DAT  920
      IF (ISQ.GT.1) L=0                                                 DAT  930
      ISQ=ISQ+1                                                         DAT  940
      IF (ISQ.GT.3) ISQ=1                                               DAT  950
  106 CONTINUE                                                          DAT  960
```

```
C                                                                       DAT  970
C     COUNT THE NUMBER OF DATA BITS                                     DAT  980
C                                                                       DAT  990
      CALL DPRCTR (ICNT)                                                DAT 1000
C                                                                       DAT 1010
C     ALLOW 8000 BITS FOR TRANSIENT DECAY                               DAT 1020
C                                                                       DAT 1030
      IF (ICNT(1)-08000) 108,107,107                                    DAT 1040
  107 ICNT(1)=0                                                         DAT 1050
      ICNT(2)=0                                                         DAT 1060
  108 CALL RD1572 (K)                                                   DAT 1070
C                                                                       DAT 1080
C     HAS 1.1 MS ELAPSED                                                DAT 1090
C     220*5 MICROSECONDS = 1.1 MS                                       DAT 1100
C     IPER * 5 MICROSECONDS = DELAY TIME                                DAT 1110
C                                                                       DAT 1120
      IF (K+ISTRT-IPER) 108,109,109                                     DAT 1130
C                                                                       DAT 1140
C     TRANSMIT DATA TO ANALOG                                           DAT 1150
C                                                                       DAT 1160
  109 CALL LOP (2,L,IER)                                                DAT 1170
      CALL PULSE (2,1,IER)                                              DAT 1180
C                                                                       DAT 1190
C     230  US ELAPSE BEFORE WE START TO CHECK CLOCK AGAIN               DAT 1200
C     46 * 5 MICROSEC = 230 MICROSECONDS                                DAT 1210
C                                                                       DAT 1220
      ISTRT=92                                                          DAT 1230
C                                                                       DAT 1240
C     IF SENSE LINE 1 CONSOLE 2 IS LOW CHECK FOR FURTHER INSTRUCTIONS   DAT 1250
C     OTHERWISE TRANSMIT THE NEXT BIT                                   DAT 1260
C                                                                       DAT 1270
      CALL SENBID (2,1,IFHI,IFLO)                                       DAT 1280
C                                                                       DAT 1290
C     PRINT  TEST RESULTS IF SENSE LINE 2 CONSOLE 2 IS HIGH             DAT 1300
C                                                                       DAT 1310
  110 CALL SENBID (2,2,IPHI,IPLO)                                       DAT 1320
  111 CONTINUE                                                          DAT 1330
      GO TO 102                                                         DAT 1340
C                                                                       DAT 1350
C    ***************************************************              DAT 1360
C     THIS SECTION OF THE PROGRAM DOES THE LOW SPEED DATA GENERATION     DAT 1370
C                                                                       DAT 1380
  112 CONTINUE                                                          DAT 1390
C                                                                       DAT 1400
C     DATA GENERATOR FOR 5 HZ RATE                                      DAT 1410
C                                                                       DAT 1420
      ISQ=1                                                             DAT 1430
C                                                                       DAT 1440
```

```
C     NBIT = NUMBER OF BITS IN A FRAME                                    DAT 1450
C                                                                         DAT 1460
      NBIT=30                                                             DAT 1470
      NBIT1=NBIT+1                                                        DAT 1480
C                                                                         DAT 1490
C     NAVG IS THE  INCREMENTAL COUNTER FOR USE IN ERROR AVERAGES          DAT 1500
C     THIS COUNTER DETERMINES THE LENGTH OF BLOCK AVERAGES                DAT 1510
C                                                                         DAT 1520
      NAVG=40                                                             DAT 1530
C                                                                         DAT 1540
C     INITIALIZE COUNTERS                                                 DAT 1550
C                                                                         DAT 1560
      PSD=0                                                               DAT 1570
      IFR=0                                                               DAT 1580
      IFDR=0                                                              DAT 1590
      IFDR3=0                                                             DAT 1600
      IDATA=0                                                             DAT 1610
      IFDR7=0                                                             DAT 1620
C                                                                         DAT 1630
C     IBLOCK COUNTS THE NUMBER OF DATA BLOCKS GENERATED                   DAT 1640
C                                                                         DAT 1650
      IBLOCK=1                                                            DAT 1660
      IAVG=0                                                              DAT 1670
      MP=0                                                                DAT 1680
      MFR=0                                                               DAT 1690
      MDAT=0                                                              DAT 1700
      MF3=0                                                               DAT 1710
      MF7=0                                                               DAT 1720
C                                                                         DAT 1730
C     JBIT IS THE BIT COUNTER FOR FRAME GENERATOR                         DAT 1740
C     ZERO BIT COUNTER                                                    DAT 1750
C                                                                         DAT 1760
      JBIT=0                                                              DAT 1770
      WRITE (4,155)                                                       DAT 1780
  113 CALL STRCLK                                                         DAT 1790
      CALL CHGCLK (100)                                                   DAT 1800
      IT1=ICLOCK(0)                                                       DAT 1810
C                                                                         DAT 1820
C     SET THE BIT COUNTER                                                 DAT 1830
C                                                                         DAT 1840
      JBIT=JBIT+1                                                         DAT 1850
      IAVG=IAVG+1                                                         DAT 1860
      IF (IAVG.EQ.NAVG) IBLOCK=IBLOCK+1                                   DAT 1870
      JB=IBLOCK-1                                                         DAT 1880
  114 IT2=ICLOCK(0)                                                       DAT 1890
      ITD=IT2-IT1                                                         DAT 1900
      IF (ITD.LT.100) GO TO 114                                           DAT 1910
C                                                                         DAT 1920
```

```
C     SAMPLE ERROR MONITORS NEXT                                        DAT 1930
C     CHECK SENSE LINE 0....PSEUDO ERROR MONITOR                        DAT 1940
C                                                                       DAT 1950
      P0=ISENSE(2,0)                                                    DAT 1960
      IF (P0.EQ.1) PSD=PSD+1                                            DAT 1970
C                                                                       DAT 1980
C      CHECK SENSE LINE 3....FRAME ERROR MONITOR                        DAT 1990
C                                                                       DAT 2000
      P3=ISENSE(2,3)                                                    DAT 2010
      IF (JBIT.EQ.6) GO TO 115                                          DAT 2020
      GO TO 116                                                         DAT 2030
  115 IF (P3.EQ.1) IFR=IFR+1                                            DAT 2040
C                                                                       DAT 2050
C     CHECK SENSE LINE 4....FORMAT ERROR MONITOR TOTAL                  DAT 2060
C                                                                       DAT 2070
  116 P4=ISENSE(2,4)                                                    DAT 2080
      IF (P4.EQ.1) IFOR=IFOR+1                                          DAT 2090
C                                                                       DAT 2100
C     CHECK SENSE LINE 5...REAL DATA ERRORS                             DAT 2110
C                                                                       DAT 2120
      P5=ISENSE(2,5)                                                    DAT 2130
      IF (P5.EQ.1) IDATA=IDATA+1                                        DAT 2140
C                                                                       DAT 2150
C     CHECK SENSE LINE 6...FORMAT ERROR .GT. 3                          DAT 2160
C                                                                       DAT 2170
      P6=ISENSE(2,6)                                                    DAT 2180
      IF (P6.EQ.1) IFOR3=IFOR3+1                                        DAT 2190
C                                                                       DAT 2200
C      CHECK SENSE LINE 7...FORMAT ERROR .GT. 7                         DAT 2210
C                                                                       DAT 2220
      P7=ISENSE(2,7)                                                    DAT 2230
      IF (P7.EQ.1) IFOR7=IFOR7+1                                        DAT 2240
      NZ=ICNT(1)+1                                                      DAT 2250
      IF (NZ-30) 117,117,118                                            DAT 2260
  117 NP0(NZ)=P0                                                        DAT 2270
C                                                                       DAT 2280
C     NP3(NZ)=P3                                                        DAT 2290
C                                                                       DAT 2300
      NP4(NZ)=P4                                                        DAT 2310
      NP7(NZ)=P7                                                        DAT 2320
      GO TO 120                                                         DAT 2330
  118 NP0(1)=P0                                                         DAT 2340
      NP3(1)=P3                                                         DAT 2350
      NP4(1)=P4                                                         DAT 2360
      NP7(1)=P7                                                         DAT 2370
C                                                                       DAT 2380
C     LOAD ANALOG OUTPUT FOR PSEUDO ERROR COUNTER                       DAT 2390
C                                                                       DAT 2400
```

```
      NSTR(1)=ISTRP(NP0)                                                    DAT 2410
C                                                                           DAT 2420
C     LOAD ANALOG OUTPUT FOR FRAME COUNTER                                  DAT 2430
C                                                                           DAT 2440
C     NSTR(2)=ISTRP(NP3)                                                    DAT 2450
C                                                                           DAT 2460
C     LOAD ANALOG OUTPUT FOR FORMAT TOTAL                                   DAT 2470
C                                                                           DAT 2480
      NSTR(3)=ISTRP(NP4)                                                    DAT 2490
C                                                                           DAT 2500
C     LOAD ANALOG OUTPUT COUNTER FOR FORMAT ERRORS  GT 7                    DAT 2510
C                                                                           DAT 2520
      NSTR(4)=ISTRP(NP7)                                                    DAT 2530
C                                                                           DAT 2540
C     ***************************************************                   DAT 2550
C     IFT IS A SCALE FACTOR FOR THE DAC ARRAY                               DAT 2560
C     A DAC OUTPUT OF 10 VOLTS  ON THE ANALOG CORRESPONDS TO                DAT 2570
C     A INTEGER COUNT OF 32767 WITH A 10V DAC REFERENCE                     DAT 2580
C                                                                           DAT 2590
      IFT=655                                                               DAT 2600
C                                                                           DAT 2610
      DO 119 IQ=1,4                                                         DAT 2620
  119 NSTR(IQ)=NSTR(IQ)*IFT                                                 DAT 2630
      CALL QDAC (16,4,1,NSTR)                                               DAT 2640
C                                                                           DAT 2650
C     ***************************************************                   DAT 2660
C                                                                           DAT 2670
  120 CONTINUE                                                              DAT 2680
      IF (IAVG.EQ.NAVG) IAVG=0                                              DAT 2690
C                                                                           DAT 2700
C     THIS COMPLETES THE SENSE LINE COMPUTATIONS                            DAT 2710
C                                                                           DAT 2720
C     GENERATE A RANDOM BIT                                                 DAT 2730
C                                                                           DAT 2740
      CALL IRAND (IBIT(1),1)                                                DAT 2750
      L=AND(1,IBIT(1))                                                      DAT 2760
      L=OR(L,40)                                                            DAT 2770
C                                                                           DAT 2780
C     GENERATE THE FRAME BIT                                                DAT 2790
C                                                                           DAT 2800
      IF (JBIT.EQ.NBIT1) L=1                                                DAT 2810
      IF (JBIT.EQ.NBIT1) JBIT=0                                             DAT 2820
      IF (ITES) 122,121,121                                                 DAT 2830
  121 IF (ISQ.EQ.1) L=1                                                     DAT 2840
      IF (ISQ.GT.1) L=0                                                     DAT 2850
      ISQ=ISQ+1                                                             DAT 2860
      IF (ISQ.GT.3) ISQ=1                                                   DAT 2870
  122 CONTINUE                                                              DAT 2880
```

```
C                                                                       DAT 2890
C     COUNT THE NUMBER OF TRANSMITTED BITS                              DAT 2900
C                                                                       DAT 2910
      CALL DPRCTR (ICNT)                                                DAT 2920
C                                                                       DAT 2930
C     ALLOW 8000 BITS FOR TRANSIENT DECAY                               DAT 2940
C                                                                       DAT 2950
      IF (ICNT(1)-08000) 124,123,123                                    DAT 2960
  123 ICNT(1)=0                                                         DAT 2970
      ICNT(2)=0                                                         DAT 2980
  124 IT3=ICLOCK(0)                                                     DAT 2990
      IDEL=IT3-IT1                                                      DAT 3000
      IF (IDEL.LT.200) GO TO 124                                        DAT 3010
C                                                                       DAT 3020
C     TRANSFER RANDOM BIT TO ANALOG COMUUTER                            DAT 3030
C                                                                       DAT 3040
      CALL LOP (2,L,IER)                                                DAT 3050
      CALL PULSE (2,1,IER)                                              DAT 3060
C                                                                       DAT 3070
C     SET OP LINE 2  HIGH TO SAMPLE FOR DECODED FRAME BIT               DAT 3080
C     SAMPLING FOR FRAME BIT IS DELAYED TO ACCOUNT FOR PROP DELAY       DAT 3090
C                                                                       DAT 3100
      IF (JBIT.EQ.6) CALL SIGNAL (2,2,1)                                DAT 3110
C                                                                       DAT 3120
C     NPRT IS THE NUMBER OF ERRORS REQUIRED BEFORE DATA IS PRINTED      DAT 3130
C                                                                       DAT 3140
      IZ0=IDATA                                                         DAT 3150
      IF (IZ0.GE.NPRT) GO TO 131                                        DAT 3160
  125 CONTINUE                                                          DAT 3170
      CALL SENBID (2,1,ISHI,ISLO)                                       DAT 3180
  126 CONTINUE                                                          DAT 3190
      WRITE (4,156)                                                     DAT 3200
      READ (4,157) FBL                                                  DAT 3210
      WRITE (4,158)                                                     DAT 3220
      READ (4,157) TES                                                  DAT 3230
      ITES=TES                                                          DAT 3240
      IF (FBL) 127,127,130                                              DAT 3250
  127 IF (ISLOW) 128,128,129                                            DAT 3260
  128 ISLOW=9                                                           DAT 3270
      GO TO 101                                                         DAT 3280
  129 ISLOW=-1                                                          DAT 3290
      GO TO 101                                                         DAT 3300
  130 WRITE (4,162)                                                     DAT 3310
  131 CONTINUE                                                          DAT 3320
C                                                                       DAT 3330
C     PROCESS SIMULATION DATA                                           DAT 3340
C                                                                       DAT 3350
C                                                                       DAT 3360
```

```
C      ICNT IS THE NUMBER OF TRANSMITTED BITS                          DAT 3370
C                                                                      DAT 3380
C                                                                      DAT 3390
C      X IS THE TOTAL NUMBER OF BITS TRANSMITTED                       DAT 3400
C      PSD IS THE NUMBER OF PSEUDO ERRORS                              DAT 3410
C      IFR IS THE NUMBER OF FRAME ERRORS                               DAT 3420
C      IDATA IS THE NUMBER OF REAL DATA ERRORS                         DAT 3430
C                                                                      DAT 3440
       X=FLOAT(ICNT(1))+FLOAT(ICNT(2))*2**15                           DAT 3450
C                                                                      DAT 3460
C      IFOR IS THE NUMBER OF FORMAT ERRORS                             DAT 3470
C      IFOR3 IS THE NUMBER OF FORMAT ERRORS .GT. 3                     DAT 3480
C      IFOR7 IS THE NUMBER OF FORMAT ERRORS .GT. 7                     DAT 3490
C                                                                      DAT 3500
C      COMPUTE ACTUAL BIT ERROR RATE                                   DAT 3510
C                                                                      DAT 3520
       BER=FLOAT(IDATA)/X                                              DAT 3530
C                                                                      DAT 3540
C      COMPUTE PSEUDO BIT ERROR RATE                                   DAT 3550
C                                                                      DAT 3560
       PBER=FLOAT(PSD)/X                                               DAT 3570
C                                                                      DAT 3580
C      COMPUTE FORMAT MONITOR ERROR RATE                               DAT 3590
C                                                                      DAT 3600
       FBER=FLOAT(IFOR)/X                                              DAT 3610
C                                                                      DAT 3620
C      COMPUTE FORMAT .GT. 7 ERROR RATE                                DAT 3630
C                                                                      DAT 3640
       F7BER=FLOAT(IFOR7)/X                                            DAT 3650
C                                                                      DAT 3660
C      COMPUTE FORMAT ERRORS .GT. 3 BUT .LT. 7                         DAT 3670
C                                                                      DAT 3680
       FER3=IFOR-IFOR7                                                 DAT 3690
       F3BER=FER3/X                                                    DAT 3700
C                                                                      DAT 3710
C      CHECK SYSTEM SIGNAL TO NOISE RATIOS FOR THE ABOVE DATA          DAT 3720
C                                                                      DAT 3730
C                                                                      DAT 3740
C      PRINT OUT TEST RESULTS                                          DAT 3750
C                                                                      DAT 3760
       WRITE (3,134)                                                   DAT 3770
       WRITE (3,135)                                                   DAT 3780
       WRITE (3,136)                                                   DAT 3790
       WRITE (3,137)                                                   DAT 3800
       WRITE (3,138) X                                                 DAT 3810
       AID=IDATA                                                       DAT 3820
       WRITE (3,139) AID                                               DAT 3830
       WRITE (3,140) BER                                               DAT 3840
```

```
      WRITE (3,141)                                                     DAT 3850
      APSD=PSD                                                          DAT 3860
      WRITE (3,142) APSD                                                DAT 3870
      APBER=PBER                                                        DAT 3880
      WRITE (3,143) APBER                                               DAT 3890
      WRITE (3,144)                                                     DAT 3900
      AFR=IFR                                                           DAT 3910
      WRITE (3,145) AFR                                                 DAT 3920
      WRITE (3,146)                                                     DAT 3930
      AFOR=IFOR                                                         DAT 3940
      WRITE (3,147) AFOR                                                DAT 3950
      WRITE (3,148) FBER                                                DAT 3960
      AFR7=IFOR7                                                        DAT 3970
      WRITE (3,149) AFR7                                                DAT 3980
      AFR3=IFOR3                                                        DAT 3990
      WRITE (3,150) AFR3                                                DAT 4000
      WRITE (4,132)                                                     DAT 4010
      READ (4,133) APRT                                                 DAT 4020
      NPRT=APRT                                                         DAT 4030
C                                                                       DAT 4040
C     RESET ALL COUNTERS                                                DAT 4050
C                                                                       DAT 4060
      PSD=0                                                             DAT 4070
      IFR=0                                                             DAT 4080
      IFOR=0                                                            DAT 4090
      IFOR3=0                                                           DAT 4100
      IFOR7=0                                                           DAT 4110
      IDATA=0                                                           DAT 4120
      ICNT(1)=0                                                         DAT 4130
      ICNT(2)=0                                                         DAT 4140
      IBLOCK=1                                                          DAT 4150
      IAVG=0                                                            DAT 4160
      GO TO 125                                                         DAT 4170
C                                                                       DAT 4180
  132 FORMAT ( 49H NUMBER OF ERRORS BEFORE RESULTS PRINTED(F FORMAT;/, 1DAT 4190
     10H NUMBER = )                                                     DAT 4200
  133 FORMAT (F15.2)                                                    DAT 4210
  134 FORMAT (1H1)                                                      DAT 4220
  135 FORMAT (15X,20H**********/15X,20H* PERFORMANCE DATA */15DAT 4230
     1X,20H**********//)                                                DAT 4240
  136 FORMAT (38H STEADY STATE SIGNAL TO NOISE RATIO = )                DAT 4250
  137 FORMAT (31H FAULT SIGNAL TO NOISE RATIO = )                       DAT 4260
  138 FORMAT (29H TOTAL NUMBER OF BITS SENT = ,E15.5/)                  DAT 4270
  139 FORMAT (27H NUMBER OF ACTUAL ERRORS = ,E15.5/)                    DAT 4280
  140 FORMAT (25H ACTUAL BIT ERROR RATE = ,E15.5/)                      DAT 4290
  141 FORMAT (10X,32H***** PSEUDO ERROR MONITOR *****//)                DAT 4300
  142 FORMAT (27H NUMBER OF PSEUDO ERRORS = ,E15.5/)                    DAT 4310
  143 FORMAT (25H PSEUDO BIT ERROR RATE = ,E15.5//)                     DAT 4320
```

```
  144 FORMAT (10X,27H****** FRAME MONITOR ******//)                          DAT 4330
  145 FORMAT (26H NUMBER OF FRAME ERRORS = ,E15.5/)                          DAT 4340
  146 FORMAT (10X,30H******** FORMAT MONITOR ********//)                     DAT 4350
  147 FORMAT (30H NUMBER OF FORMAT VIOLATIONS =,E15.5/)                      DAT 4360
  148 FORMAT (31H FORMAT VIOLATION ERROR RATE = ,E15.5/)                     DAT 4370
  149 FORMAT (46H NUMBER OF FORMAT VIOLATIONS GREATER THAN 7 = ,E15.5/)      DAT 4380
  150 FORMAT (43H NUMBER OF FORMAT VIOLATIONS LESS THAN 7 = ,E15.5//)        DAT 4390
  151 FORMAT (F10.4)                                                        DAT 4400
  152 FORMAT (24HFOR TEST SEQUENCE TYPE 1/23HFOR RANDOM DATA TYPE -1/7HTDAT 4410
     1YPE = )                                                               DAT 4420
  153 FORMAT (37HIF  5 HZ DATA RATE IS DESIRED TYPE -1/22HFOR 900 HZ RATDAT 4430
     1E TYPE 9/7HTYPE = )                                                   DAT 4440
  154 FORMAT (19HDATA AT 900 HZ RATE)                                       DAT 4450
  155 FORMAT (18H DATA AT 5HZ RATE )                                        DAT 4460
  156 FORMAT (29H TO CHANGE DATA RATE TYPE -1 /28HTO TERMINATE PROGRAM TDAT 4470
     1YPE 1 /7HTYPE = )                                                     DAT 4480
  157 FORMAT (F10.2)                                                        DAT 4490
  158 FORMAT (28H DO YOU WANT A TEST SEQUENCE/25HIF YES TYPE 1, NO TYPE DAT 4500
     1-1/6HTYPE =)                                                          DAT 4510
  159 FORMAT (20HPBS 1 SHOULD BE HIGH)                                      DAT 4520
  160 FORMAT (30H PROGRAM PROTECT SHOULD BE OFF)                            DAT 4530
  161 FORMAT (37HTO TERMINATE PROGRAM PLACE PBS 1 LOW )                     DAT 4540
  162 FORMAT (2X,26H PROGRAM TERMINATED BY PB1)                             DAT 4550
C                                                                           DAT 4560
      END                                                                   DAT 4570

      FUNCTION ISTRP(IX)                                                    IST   10
      DIMENSION IX(32)                                                      IST   20
C                                                                           IST   30
C     ISH IS THE NUMBER OF BITS IN THE DATA AVERAGE                         IST   40
C                                                                           IST   50
      ISH=30                                                                IST   60
C                                                                           IST   70
C     DO A DATA SHIFT TO REPLACE THE OLDEST BIT                             IST   80
C                                                                           IST   90
      DO 101 I=1,ISH                                                        IST  100
         J=ISH+1-I                                                          IST  110
         JH=J+1                                                             IST  120
  101 IX(JH)=IX(J)                                                          IST  130
C                                                                           IST  140
C     DO THE SUMMATION OF ALL ERRORS IN DATA SET                            IST  150
C                                                                           IST  160
      ISTRP=0                                                               IST  170
      ILIM=ISH+1                                                            IST  180
      DO 102 M=2,ILIM                                                       IST  190
  102 ISTRP=ISTRP+IX(M)                                                     IST  200
      RETURN                                                                IST  210
C                                                                           IST  220
```

```
        END                                                    IST  230


        NAM  DPRCTR
*            ROUTINE TO DO A DOUBLE PRECISION COUNT ON AN
*           INTEGER VARIABLE PASSED TO IT.
*             FIRST WORD IN THE ARRAY IS THE LOWER 15 BITS
*            SECOND WORD IN THE ARRAY IS THE UPPER 15 BITS
        ENT  DPRCTR
        EQU  LPMSK(%2)
        EQU  ZERO(%22)
DPRCTR  0    0
        LDQ* (DPRCTR)
        RAO* DPRCTR
        LDA- (ZERO),Q
        INA  1
        SAP  DPR010-*-1
        AND- LPMSK+15
        STA- (ZERO),Q
        LDA- 1,Q
        INA  1
        STA- 1,Q
        JMP* (DPRCTR)
DPR010  STA- (ZERO),Q
        JMP* (DPRCTR)
        END
```

METRIC SYSTEM

BASE UNITS:

Quantity	Unit	SI Symbol	Formula
length	metre	m	...
mass	kilogram	kg	...
time	second	s	...
electric current	ampere	A	...
thermodynamic temperature	kelvin	K	...
amount of substance	mole	mol	...
luminous intensity	candela	cd	...

SUPPLEMENTARY UNITS:

plane angle	radian	rad	...
solid angle	steradian	sr	...

DERIVED UNITS:

Acceleration	metre per second squared	...	m/s
activity (of a radioactive source)	disintegration per second	...	(disintegration)/s
angular acceleration	radian per second squared	...	rad/s
angular velocity	radian per second	...	rad/s
area	square metre	...	m
density	kilogram per cubic metre	...	kg/m
electric capacitance	farad	F	A·s/V
electrical conductance	siemens	S	A/V
electric field strength	volt per metre	...	V/m
electric inductance	henry	H	V·s/A
electric potential difference	volt	V	W/A
electric resistance	ohm		V/A
electromotive force	volt	V	W/A
energy	joule	J	N·m
entropy	joule per kelvin	...	J/K
force	newton	N	kg·m/s
frequency	hertz	Hz	(cycle)/s
illuminance	lux	lx	lm/m
luminance	candela per square metre	...	cd/m
luminous flux	lumen	lm	cd·sr
magnetic field strength	ampere per metre	...	A/m
magnetic flux	weber	Wb	V·s
magnetic flux density	tesla	T	Wb/m
magnetomotive force	ampere	A	...
power	watt	W	J/s
pressure	pascal	Pa	N/m
quantity of electricity	coulomb	C	A·s
quantity of heat	joule	J	N·m
radiant intensity	watt per steradian	...	W/sr
specific heat	joule per kilogram-kelvin	...	J/kg·K
stress	pascal	Pa	N/m
thermal conductivity	watt per metre-kelvin	...	W/m·K
velocity	metre per second	...	m/s
viscosity, dynamic	pascal-second	...	Pa·s
viscosity, kinematic	square metre per second	...	m/s
voltage	volt	V	W/A
volume	cubic metre	...	m
wavenumber	reciprocal metre	...	(wave)/m
work	joule	J	N·m

SI PREFIXES:

Multiplication Factors	Prefix	SI Symbol
$1\,000\,000\,000\,000 = 10^{12}$	tera	T
$1\,000\,000\,000 = 10^{9}$	giga	G
$1\,000\,000 = 10^{6}$	mega	M
$1\,000 = 10^{3}$	kilo	k
$100 = 10^{2}$	hecto*	h
$10 = 10^{1}$	deka*	da
$0.1 = 10^{-1}$	deci*	d
$0.01 = 10^{-2}$	centi*	c
$0.001 = 10^{-3}$	milli	m
$0.000\,001 = 10^{-6}$	micro	μ
$0.000\,000\,001 = 10^{-9}$	nano	n
$0.000\,000\,000\,001 = 10^{-12}$	pico	p
$0.000\,000\,000\,000\,001 = 10^{-15}$	femto	f
$0.000\,000\,000\,000\,000\,001 = 10^{-18}$	atto	a

* To be avoided where possible.

*U.S. GOVERNMENT PRINTING OFFICE: 1977-714-025/126

MISSION
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RADC plans and conducts research, exploratory and advanced development programs in command, control, and communications (C^3) activities, and in the C^3 areas of information sciences and intelligence. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, ionospheric propagation, solid state sciences, microwave physics and electronic reliability, maintainability and compatibility.

