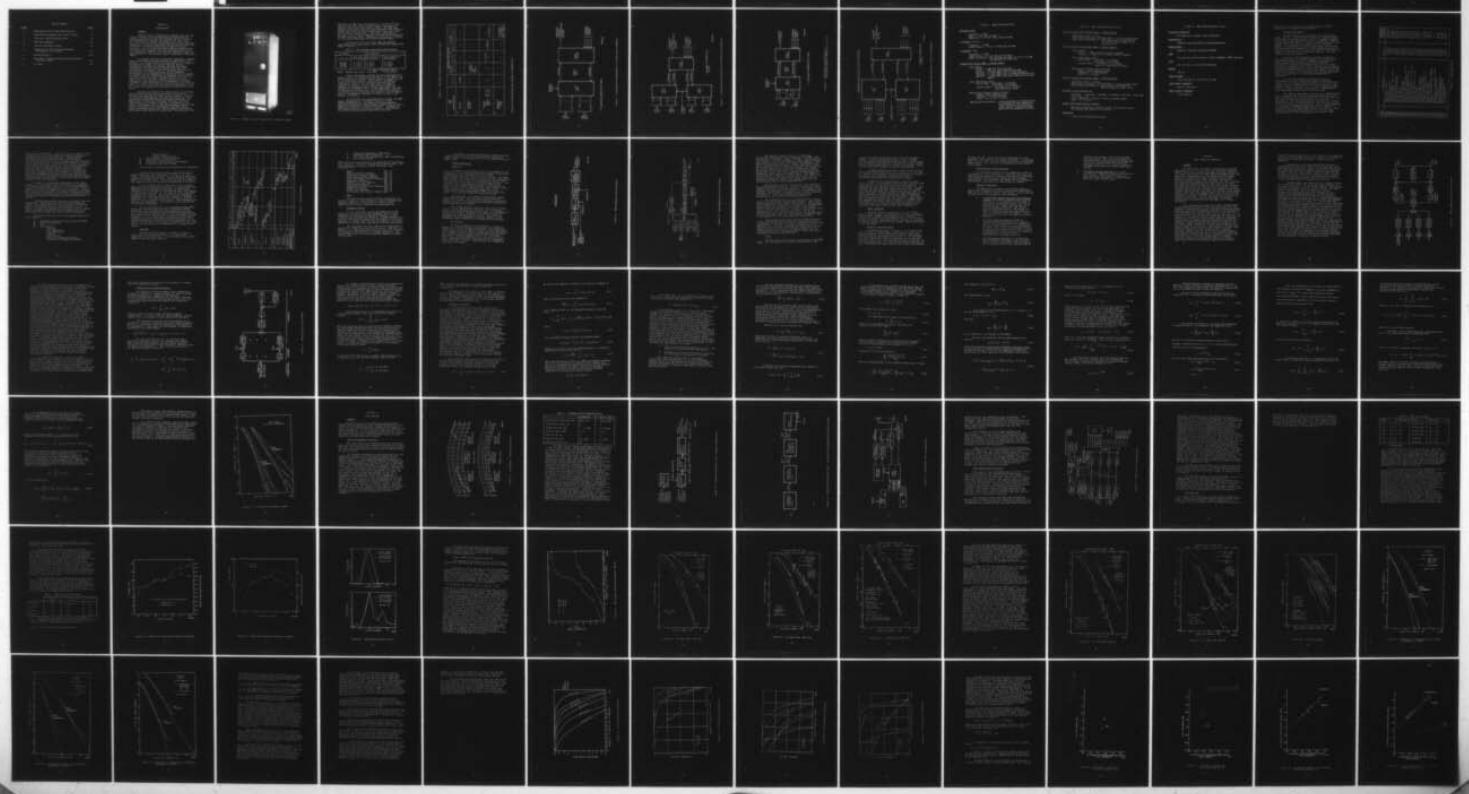
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MEGABIT DIGITAL TROPOSCATTER SUBSYSTEM (MDTS)

FINAL REPORT FOR DECEMBER 1974 - JULY 1976

BY

D.R. KERN, P. MONSEN, et al

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CONTRACT DAAB07-74-C-0040

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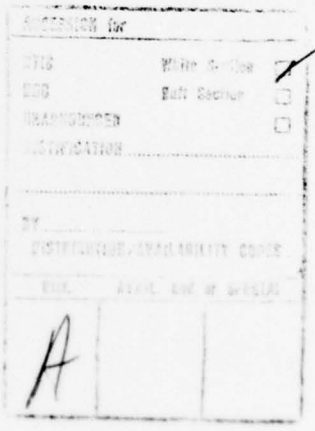
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This document covers the results of work performed on the Megabit Digital Troposcatter Subsystem Program under Contract DAAB07-74-C-0040. The primary objective of the MDTS is to provide a wideband digital data modem and appropriate link modifications to convert established DCS links from analog to digital operation. Results of laboratory and field tests are contained with performance of digital troposcatter communication rates of 1.544, 3.088, 6.276 and 12.6 Mb/s being presented.

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FOREWORD

The MDTS Program provides for the design, development, qualification and production of eight engineering development models of a 12.6 Mb/s strategic digital tropo modem for use by the Defense Communications Agency (DCA) on its worldwide tropo links. The project office is U.S. Army Communications Systems Agency (USACSA) and the contracting agency in USAECOM. The work was performed under Contract No. DAAB07-74-C-0040 and USAECOM Specification EL-CP0144-0001B.

The prime contractor is GTE Sylvania, Inc., Needham, Massachusetts. Signatron, Inc., Lexington, Massachusetts, is the major subcontractor for Systems Engineering, the Quadruple Space Diversity Test Simulator (QSDTS), the Adaptive Forward Equalizer, design of the Time Tracker, and link test data reduction and analysis.

The program featured a dual diversity breadboard system to demonstrate technical feasibility and included four commercial grade audio order wire units, test spares, Quadruple Space Diversity Test Simulator (QSDTS), modification to existing link equipments as required for installation and testing, a forty-hour training program, and extensive data. Factory tests included in the requirements are: Performance, Environmental, EMI, Reliability, Maintainability and Human Factors. A 2000 hour value engineering program was also completed.

The original contract required both CONUS and OCONUS link testing. The CONUS tests were conducted at the Youngstown to Verona, New York test link operated by USAF, RADC, Rome, N.Y. The OCONUS tests were postponed due to the unavailability of an overseas test link. However, DCA is presently planning to conduct a six month test program in Europe commencing approximately January 1977.

Additional simulated tests were performed on the dual diversity breadboard. Under separate contract, RADC with GTE Sylvania support conducted a test program to measure the MDTS performance for tactical operations. These tests were conducted on the QSDTS at RADC. This same breadboard was also tested on a troposcatter link from Tobyhanna, Pa. to ECOM, Ft. Monmouth, N.J. using the AN/GRC-143 radio equipment.

It is the intent of this report to summarize the final hardware configuration, delineate the Decision Feedback Equalizer function which is the technique employed and to discuss in some detail the results of the various tests that were performed.

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SECTION 1

INTRODUCTION

GENERAL

When the use of troposcatter communication has been required, FDM/FM analog systems have provided required channel capacities in both the backbone and tail links of the Defense Communications System (DCS) for many years. With the advent of digital technology and its many inherent advantages, innovative techniques have emerged to enable the conversion of analog troposcatter systems to digital operation. One of these techniques, adaptive equalization, can effectively counteract the multipath perturbations of the troposcatter medium. This was the technique chosen for implementation in the Megabit Digital Troposcatter Subsystem (MDTS).

The Megabit Digital Troposcatter Subsystem, commonly known as the MDTS, and nomenclatured the MD-918/GRC, (see Figure 1), is a Department of the Army effort, in support of DCS RDT&E Task 14106, to develop high-rate digital troposcatter equipment to convert selected DCS analog troposcatter links to digital operation and meet DCS performance requirements. One of the prime objectives of the program is to avoid requiring new RF component developments to the maximum extent possible and thus permit the upgrade of DCS troposcatter RF equipment with currently available commercial grade components where required. To comply with this and other program objectives, various requirements were imposed on the development of the MDTS. The MDTS is required to operate at input Mission Bit Streams (MBS) of N times 1.544 Mb/s (the basic PCM 24-channel rate) for values of N equal to 1,2,4,6 and 8 (1.544 Mb/s to 12.56 Mb/s).

The choice of Mission Bit Stream rates for the MDTS were determined primarily on the basis of multiplexer equipment availability for MDTS testing purposes. Although the prototype MDTS MBS data rates are not compatible with the present planned DCS digital multiplex hierarchy, the DRAMA family of multiplex equipment (TD-1192, TD-1193), compatibility can easily be achieved in production units without development risk or adverse performance impact. DCS digital troposcatter link performance requirements were under development during this effort; however, provisional performance requirements were specified. In particular MDTS

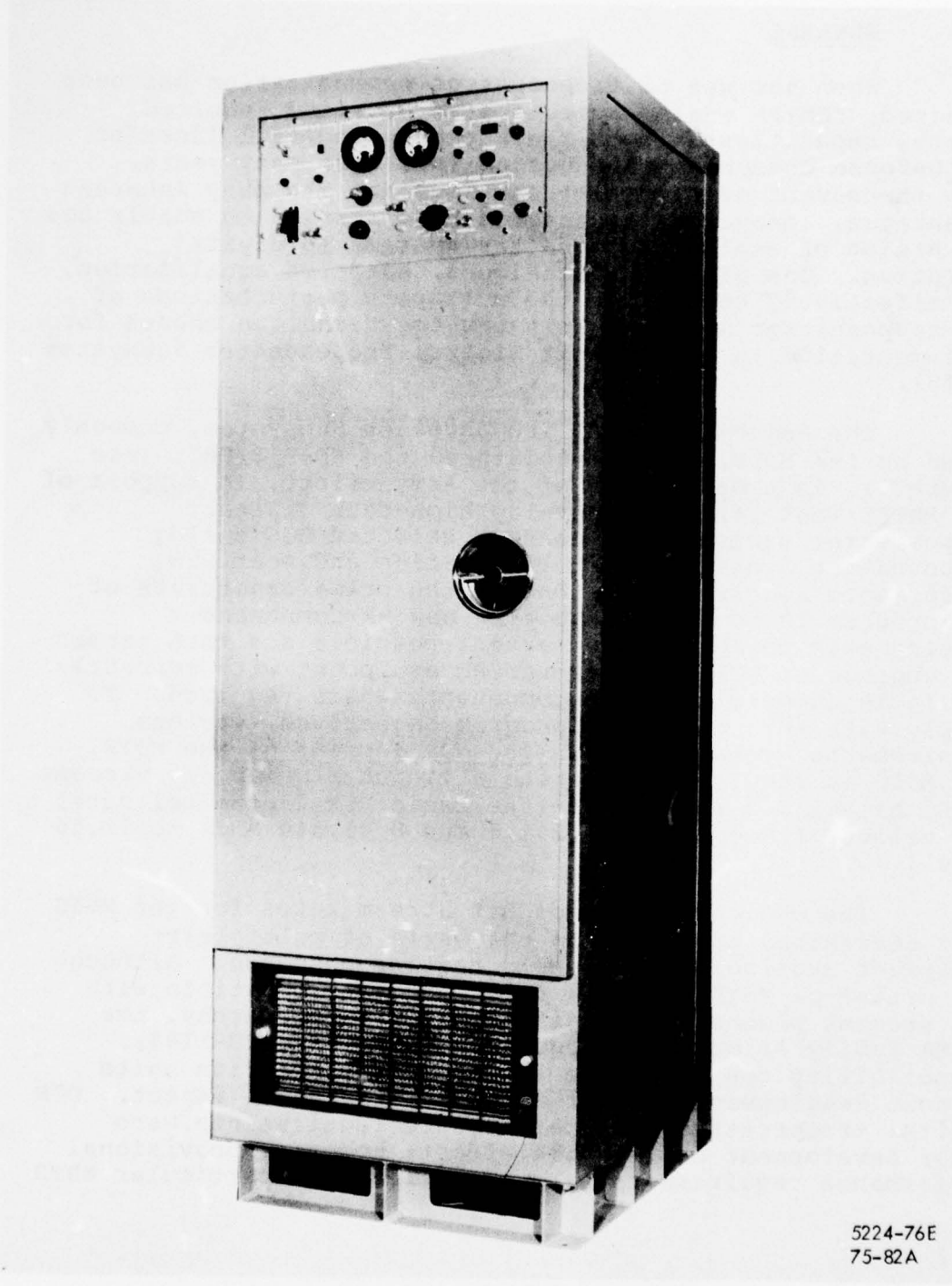


Figure 1. Megabit Digital Troposcatter Subsystem (MDTS)

operation for MBS rates form N equal to 1,2,4,6 and 8 was required over paths whose lengths range from under 100 nautical miles up to 250 nautical miles. The MDTS must operate within the 99-percent power bandwidth constraints of 10 MHz and 15 MHz for data transmission rates of 6.3 Mb/s and 12.6 Mb/s, respectively. Test data, contained in Sections 3 and 4 clearly supports the spectrum efficiency of the MDTS technique with a transmission efficiency in excess of 1 bit/hertz achievable with the prototype models.

Provisional Bit Error Rates (BER) performance requirements were specified in time availability fashion and shown in Table 1.

TABLE 1. MDTS MAXIMUM ERROR RATE SPECIFICATION

All Hours	Path Length L		
Of One Year	Less than 100 N Miles	100 N Miles to 200 N Miles	200 N Miles to 250 N Miles
99.00%	1×10^{-8}	1×10^{-7}	5×10^{-7}
99.90%	1×10^{-7}	1×10^{-6}	5×10^{-6}
99.99%	1×10^{-6}	1×10^{-5}	5×10^{-5}

NOTE: Maximum Data Rate = 12.6 Mb/s 6.3 Mb/s 150<L<250 N Miles L<150 N Miles

Other requirements imposed are the integration of a quality monitor to assess the performance of the MDTS on an on-line basis and a 64-kb/s digital service channel for use as an engineering channel. Additionally, the MDTS is required to electrically interface with existing DCS troposcatter assets. On the radio side, the MDTS is required to interface with the AN/FRC-39A, AN/MRC-85, AN/MRC-113, and AN/TRC-132A. On the video side , the MDTS is required to interface with the TD-968 PCM multiplexer, the VICOM T family of digital multiplexers, and the Walburn (KG-81) Cryptographic equipment as shown in Table 2 and Figures 2 through 5.

To fully meet the requirements of the DCS, the MDTS design implemented is a quadruple-diversity 4-PSK modulator/demodulator. An adaptive decision-feedback equalizer designed for fading channel application is used to combat the troposcatter multipath effects. A summary of MDTS characteristics is given in Figure 6. Additionally, the MDTS has demonstrated compatibility with the

TABLE 2. MDTS MODEM THROUGHPUT DATA RATES IN MB/S

TDM MUX CONFIGURATION[1]		MAXIMUM PATH LENGTH			
		250 NM		150 NM	
	N = 1	N = 2	N = 4	N = 6	N = 8
A. TD-968	1.544000	--	--	--	--
B. PARALLEL TD-968	--	3.088000 (1.544 each input)	--	--	--
C. VICOM-T					
4004 (N = 4)	--	--	6.276000	--	--
PSEUDO (N = 6)	--	--	--	9.414000	--
4008 (N = 8)	--	--	--	--	12.552000
D. PARALLEL VICOM-T 4004	--	--	--	--	12.552000 (6.276000 each input)

[1]EACH MUX CONFIGURATION MAY INCLUDE A WALBURN UNIT.

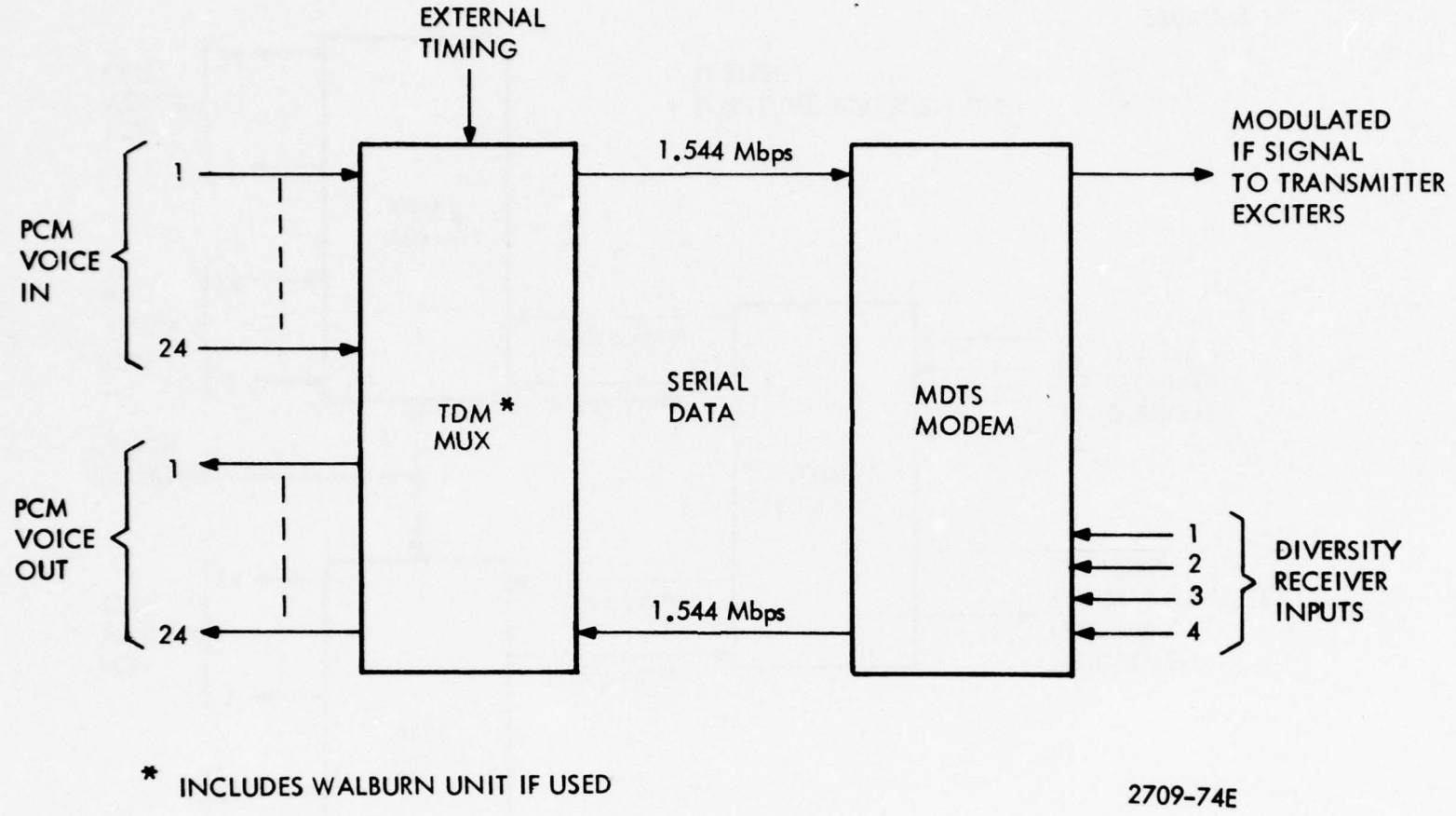


Figure 2. Multiplexer Configuration A (24 PCM Voice Channels)

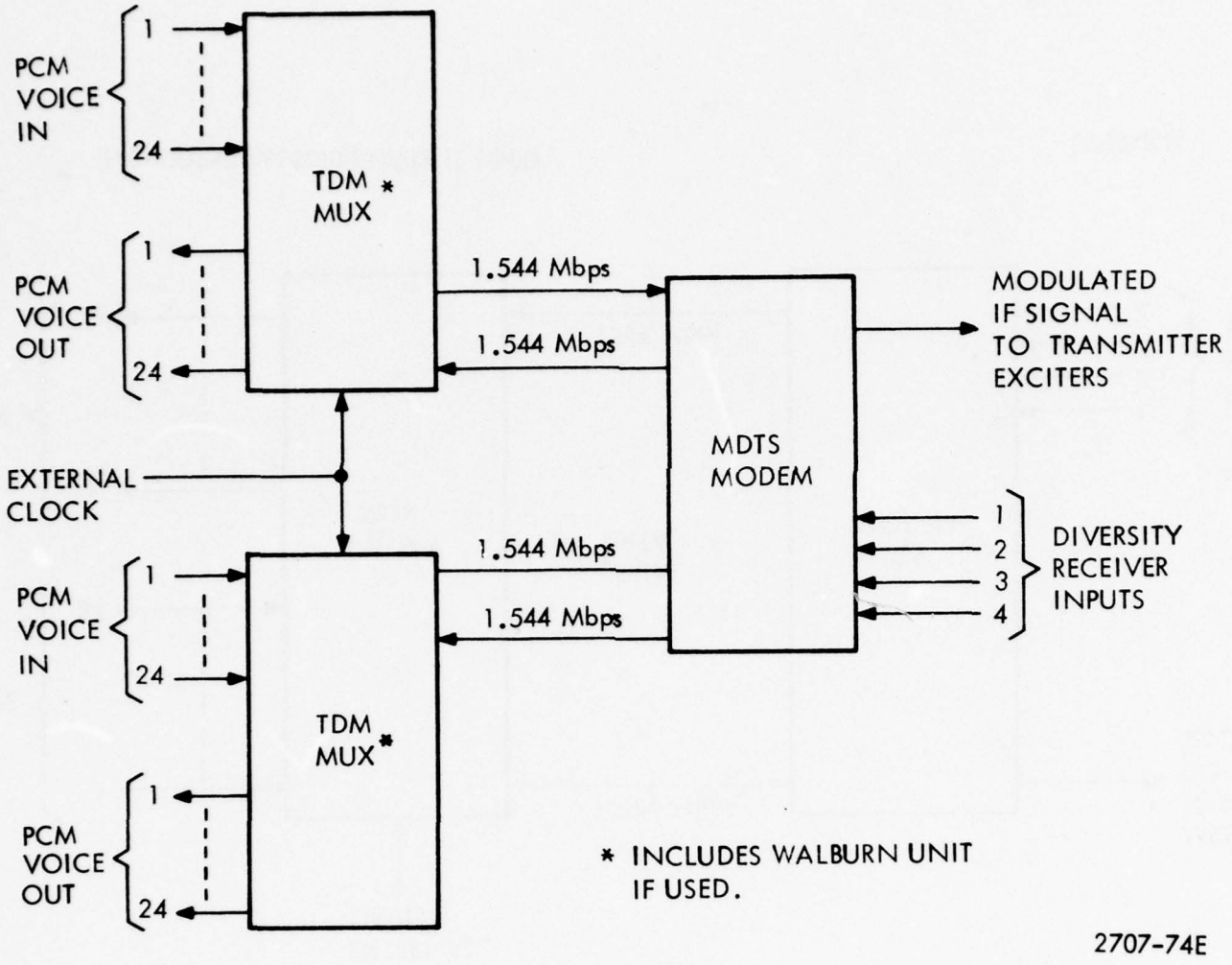
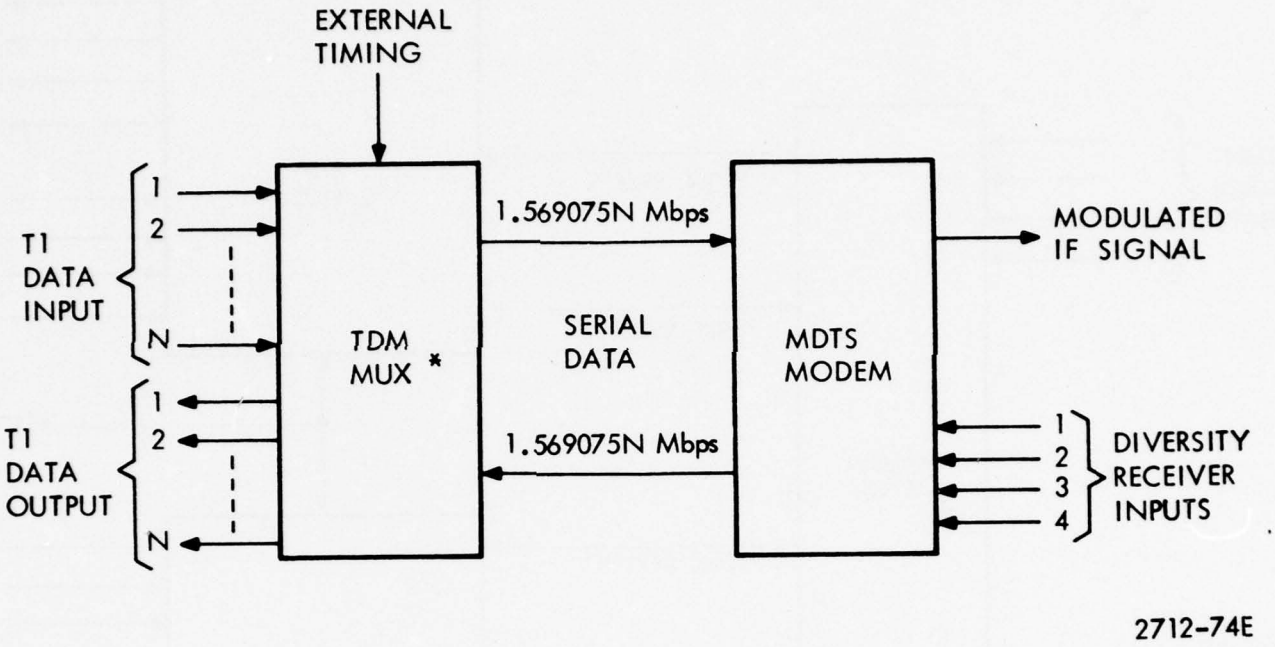


Figure 3. Multiplexer Configuration B (48 PCM Voice Channels)



* INCLUDES WALBURN UNIT IF USED.

Figure 4. Multiplexer Configuration C
(For N-T1 Channels, Where N = 4, 6, 8)

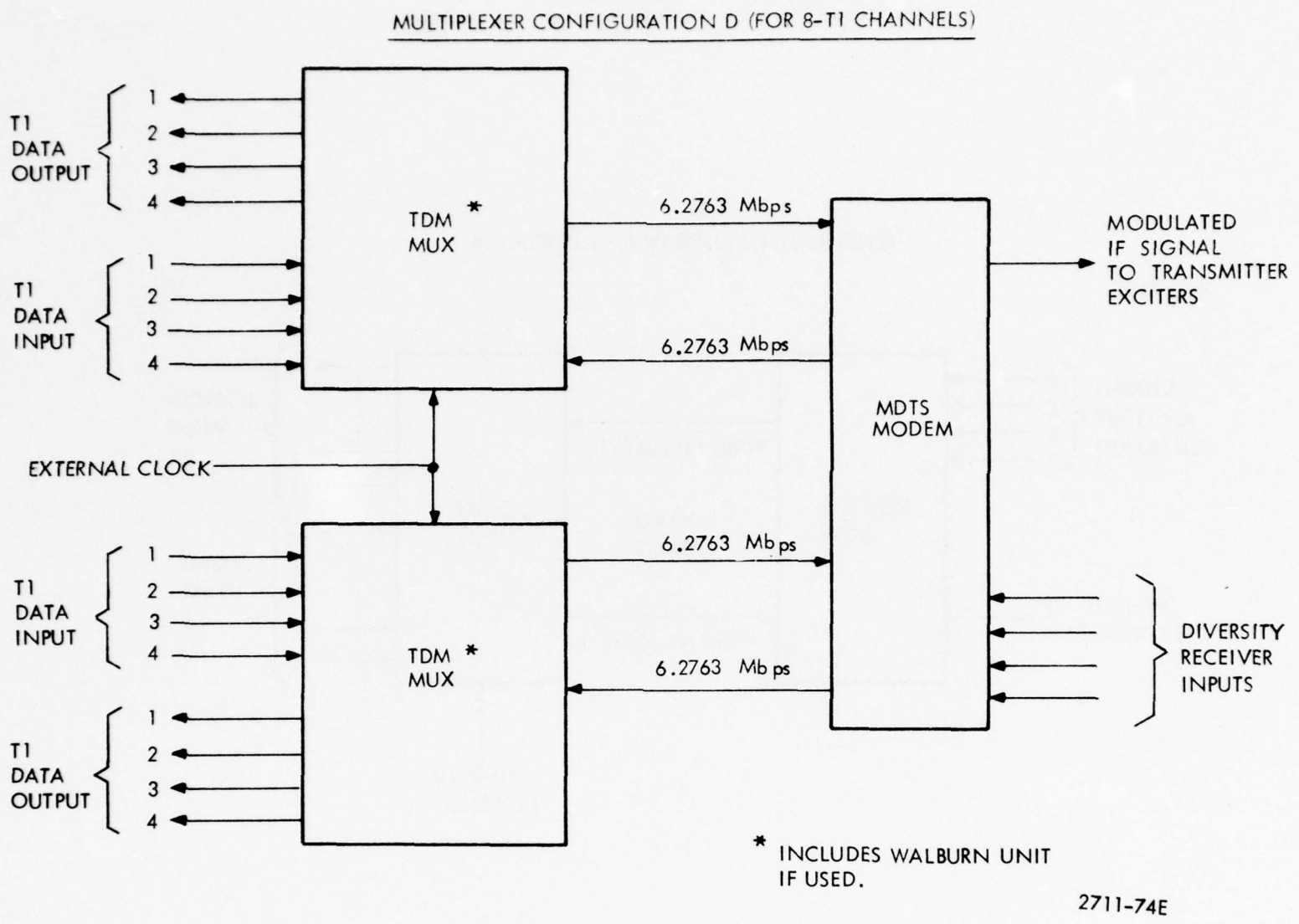


Figure 5. Multiplexer Configuration D (For 8-T1 Channels)

Figure 6. MDTS Characteristics

External Clock

Frequency - 5 MHz
Level - 0 dBm into 50 ohms
Stability - 1 X 10^{-8} (long term) minimum

IF Inputs (up to 4)

Frequency - 70 MHz
Level (input) - -70 to -20 dBm into 50 ohms

IF Outputs (two)

Frequency - 70 MHz
Output level - 0 to 17 dBm into 50 ohms
Power band width - 99% transmitted power in a 10 or 15 MHz BW depending on data rate

Mission Bit Stream (MBS) / Timing Inputs

Input Modes:
Serial - 1 MBS and clock supplied
Serial - 1 MBS and clock derived from MBS
Parallel - 2 input MBS's and 2 clocks supplied
Parallel - 2 input MBS's and one common clock derived
Parallel - 2 input MBS's and clock derived from input MBS's

Input MBS/Timing Rates:
Serial Mode - 1.544 Mb/s, 6.276 Mb/s, 9.414 Mb/s, 12.552 Mb/s
Parallel Mode - 1.544 Mb/s or 6.276 Mb/s each MBS/timing input

MBS/Timing Interface Specifications:
Format - NRZ, balanced input
Impedence - 78 ohms nominal
Level - $\pm$ 0.5 to $\pm$ 3.0 volts

MBS/Timing Relationship - Strap selectable to establish mid bit sampling of data regardless input clock/data relationship in either serial or parallel modes when clock is supplied with data.

Figure 6. MDTS Characteristics (Cont)

Service Channel Bit Stream (SCBS) / Timing Inputs

SCBS/Timing Rate - 64 kb/s
SCBS/Timing Interface - MIL-STD-188C, ± 6 volts single ended.
SCBS/Timing Relationship - SCBS input should transition on the positive going edge of the supplied clock.

Receive Mission Bit Stream (MBS) / Timing Outputs

Output Modes:
Serial - 1 MBS and timing output supplied
Parallel - 2 MBS's and 2 timing outputs supplied

Output MBS/Timing Rates:
Serial Mode - 1.544 Mb/s, 6.276 Mb/s, 9.414 Mb/s, 12.552 Mb/s
Parallel Mode - 1.544 Mb/s or 6.276 Mb/s each of 2 data/timing outputs

MBS/Timing Interface Specifications:
Format - NRZ, balanced output
Impedence - 78 ohms nominal
Level - ± 3.0 volts

Service Channel Bit Stream (SCBS) / Timing Outputs

SCBS/Timing Rate - 64 kb/s
SCBS/Timing Interface - MIL-STD-188C, ± 6 volts single ended.
SCBS/Timing Relationship - Output SCBS transitions on positive edge of output clock.

Transmit Timing Outputs (3)

Frequency - 1.544 MHz, 3.088 MHz, 6.276 MHz, 9.414 MHz, 12.552 MHz
Duty Cycle - 50%
Output Impedence - nominal 78 ohms, balanced output
Level - ± 3.0 volts

Remote Performance Monitor Outputs

Multi-pin connector to monitor alarms, received S/N ratio, AGC and BER (see Table 2 for details).

Modulation

4 PSK with differential encoding

Figure 6. MDTS Characteristics (Cont)

Diversity Combining

Pre-detection, maximal ratio equivalent

Demodulation

Coherent with differential encoding/decoding

Equalization

Adaptive, decision directed feedback

BITE

On-line and off-line built-in test equipment (BITE) provided

Size

24" W X 27" D X 72" H (68" W/O base)

Weight

470 lb

Input Voltage

120 $\pm$ 10% VAC 1ϕ, 47-63 Hz, 6.6 amp

Input Power (nominal)

800 VA, 600 watts

Power Factor (nominal)

0.75 lagging

AN/GSC-24(V) time division multiplexer and the Walburn equipment in an operation configuration.

Program Description

The MDTS Program was organized into six distinct phases, namely: system analysis, detailed hardware design, breadboard, build and checkout of eight development models, factory tests, and CONUS field tests. In addition, special test equipment was built to support checkout and test of the modems. One Quadruple Space Diversity Test Simulator (QSDTS) was delivered as a contract end item. Four 64-kb/s Continuous Variable Slope Delta (CVSD) modulation voice to digital converters were built for use with the modem service channel. A 39 item data package was supplied. The data items are listed in Figure 7.

As part of the GTE Sylvania/Signatron proposal, a significant amount of in depth analysis was presented to show that the adaptive decision-feedback equalizer was a viable approach to providing an efficient digital troposcatter capability at digital rates up to 12.6 Mb/s. The system engineering phase of this program was devoted to refining and expanding this analysis and determining various subsystem parameters such as loop gains, signal levels, and loop time constants to provide the best possible operation within the confines of a reasonable implementation complexity.

The detailed hardware design was initially implemented in a dual diversity breadboard which was utilized to verify the performance over a simulated fading channel using the QSDTS and to verify the accuracy of the hardware design. Releases for P.C. card layouts were made as soon as the verification was complete. Subsequently, eight development models were built and tested.

The MDTS was designed to operate in a quad diversity link configuration. The simulated performance data which was collected at GTE Sylvania proved that the technique was not only feasible but was providing the required performance. This was determined by extending the results at dual diversity to quad diversity. Additionally, as part of a test and evaluation program for tactical communications by the USAF, the MDTS breadboard was sent to RADC for evaluation with the QSDTS under TRI-TAC sponsorship. These tests were conducted with interest in lower data rates (approximately 2.5 Mb/s maximum) and performance under

DATA ITEM	DESCRIPTION	INITIAL	SUBMISSION APPROVAL/ COMPLETED
A001	Monthly Status Report	12-17-73	Continuing
A002	Design Plan	4-22-74	10-17-74
A003	Semi-Annual Tech Report	6-14-74	2-3-75
A004	Final Tech Report	7-1-76	1-17-77
A005	Engineering Accomplishment Report	7-1-76	12-31-76
A006	Installation Plan	5-9-75	5-16-75
B001	Contract Fund Status Report	2-28-74	Continuing
C001	Engineering Design Test Plan	10-4-74	12-29-75
C002	EMI Test Plan	1-3-75	5-1-75
C003	EMI Test Report	5-12-75	5-12-75
D001	Reliability Program Plan	12-12-73	3-27-74
D002	Reliability Math Model	12-20-73	9-30-75
D003	Product Assurance Test Demo & Eval Plan	4-25-75	6-26-75
D004	Reliability Test Reports/Final	5-27-76	5-27-76
D005	Maintainability Demonstration Plan	1-10-74	1-31-74
D006	Maintainability Report	10-6-75	10-30-75
D007	Product Assur Test Demo & Eval Plan (M)	10-13-75	11-17-75
D008	Maintain Demo Report	5-25-76	5-25-76
D009	Reliability Failed Analysis Report	2-20-76	5-27-76
E001	Commercial Manuals	7-1-76	9-30-76
F001	Safety Statement	8-29-75	4-12-76
F002	Preliminary Hazard Analysis	10-4-74	1-7-75
F003	Operational Safety Analysis	8-29-75	-
F004	Radioactive Material Report	11-7-74	12-18-74
F005	Training & Training Equipment Plan	12-12-73	1-18-74
F006	New Equipment Training Course	1-10-74	3-21-74
F007	Training Course Reports	1-7-76	7-1-76
F008	Graphic Aids Training	1-10-74	3-21-74
F009	Training Course Student Info Sheets	1-10-74	3-21-74
G001	Standardization Comp Select & Control	5-14-74	-
G002	NSP List	7-1-76	7-1-76
G003	Standardization Comp Select & Control	5-14-74	-
G004	NSP Statement of Compliance	7-1-76	7-1-76
G005	EMI Control Plan	1-10-74	6-19-74
G006	Configuration Management Plan	12-12-73	4-18-74
G007	Engineering Release Record	6-25-76	6-25-76
H001	Tools & Test Equipment List	3-1-76	3-1-76
J001	V.E. Progress Report	2-25-74	11-27-74
J002	V.E. Fund Report	10-27-75	12-9-75

Figure 7. Data Items List

non-diversity conditions. During the tests at RADC, it was noticed for the first time that non-diversity operation performance was less than desirable. (Non-diversity operation was not an MDTS program requirement since non-diversity operation is not the normal approach for DCS planned configurations. Minimum BER performance at high S/N ratios was found to be higher than theoretically predicted and a function of doppler spread. Further investigation revealed that the observed non-diversity performance resulted from insufficient dynamic range and non-optimum loop time constants within the breadboard. Changes were made in the breadboard to correct these deficiencies and subsequent retesting indicated non-diversity BER performance improved orders of magnitude to levels which were more than acceptable for link operation.

Section 6 is a detailed description of the modem hardware. At the present time, GTE Sylvania and Signatron are implementing changes into four of the eight development models to eliminate the conditions just described. This is being done so that the modem can also be used on a strategic dual diversity configuration for Parallel Transmission with the assurance of acceptable non-diversity operation when one channel has failed. The changes are briefly described in Section 7.

The MDTS test program consisted of factory tests and field tests. The field tests were to be both CONUS and OCONUS. The OCONUS tests were not performed as scheduled due to the unavailability of a DCS troposcatter link. However, planning is underway at the present time to conduct tests in Europe in early 1977 with the models which are being modified to improve low order diversity operation.

The factory test portion of the program consisted of the following:

- Extensive performance tests using the QSDTS
- Power Determination
- EMI
- Environmental
  - Altitude
  - Low Temperature
  - High Temperature
  - Humidity
  - Sand and Dust
  - Shock (in shipping container)
  - Vibration (in shipping container)

Bench Handling
Fungus (samples only)

- Human Engineering Demonstration
- Maintainability Demonstration
- Reliability Demonstration (all modems)
- Acceptance Test (all modems)

The results of these tests are summarized in Section 5.

A three month field test was conducted during the winter months over the Youngstown to Verona, N. Y. test range. The higher data rates, 6.3, 9.4, and 12.6 Mb/s were tested on the AN/TRC-132A radio. The AN/MRC-98 was used for tests at 3.1 and 6.3 Mb/s. Tests were not run at 1.5 Mb/s. The results of the test program are summarized in Section 3.

A test program which was not part of the original MDTS program was conducted by USAECOM. It was desirable for USAECOM to verify and demonstrate that the MDTS could interface with the AN/GRC-143 troposcatter radio and operate at higher data rates than are now used and with significant performance improvement. The transmitter was located at Tobyhanna, Pa., and the receiver was located at USAECOM, Ft. Monmouth, N. J. The MDTS modulator was made up of spare cards from the development model spares. The breadboard was used for the demodulator. The results of this test series is included in Appendix A.

An initial system test of the AN/MRC-98, MDS modem, AN/GSC-24 time division multiplexer and TD-968 PCM/TDM multiplexer was performed over the Youngstown to Verona, N. Y. test link by USAECOM, RADC and Defense Communication Engineering Center (DCEC) personnel with assistance from GTE Sylvania. The test conclusively verified the basic system compatibility of the MDTS modem and implementation with a digital transmission system functionally equivalent to that used in the terrestial and satellite subsystems of DCS. The results of this test will be summarized in a separate DCEC report.

Schedule

The MDTS Program Schedule is shown in Figure 8. Also shown are anticipated dates for initiation and completion of follow-on work. The performance/cost studies shown in the last entry include:

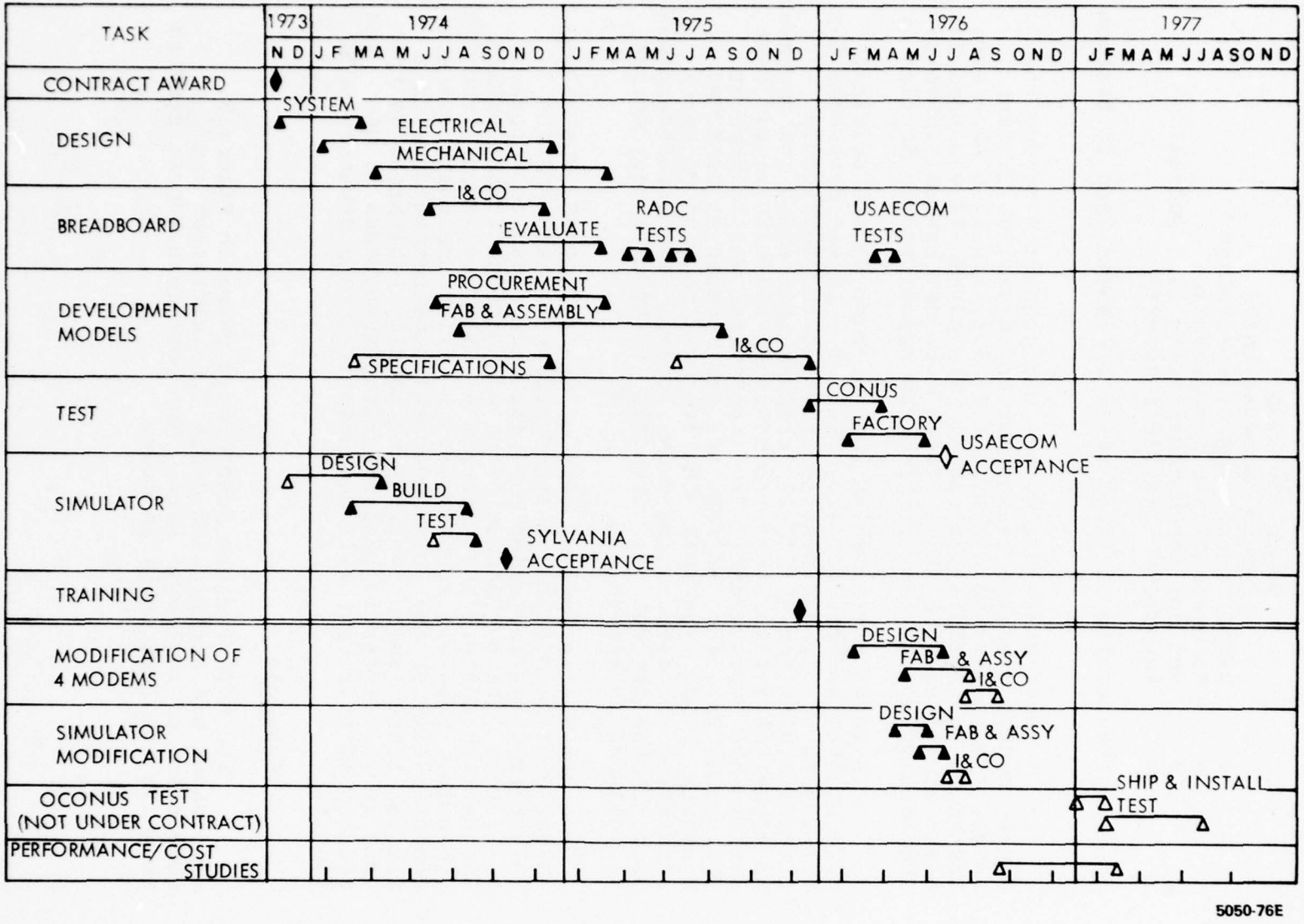


Figure 8. Program Schedule

a. Reduced environmental requirements
b. Component usage evaluation
c. 25, 50 and 100 thousand hour MTBO requirements
d. BITE effectiveness.

These will not be started until the modification program has been completed. The basic program was 31 months long. The total program now planned is about 43 months. Key milestones are:

Award	Nov. 73
QSDTS Acceptance Complete	Aug. 74
Breadboard Checkout Complete	Jan. 75
RADC Simulated Test Complete	June 75
Build Development Models Complete	Sep. 75
CONUS Test Complete	Mar. 76
USAECOM Link Test Complete	Apr. 76
Factory Test Complete	June 76
MDTS/QSDTS Modifications Complete	Aug. 76
OCONUS Test Begins	Jan. 77
OCONUS Test Complete	July 77
Performance/Cost Studies Complete	Apr. 77

Data

The MDTS program required 39 data items which are listed in Figure 7, with the date of initial submittal and approval completed. Items marked (*) have not been submitted and the dates supplied are approximations.

- Equipment Status

As of 1 July 1976, six of the modems are at GTE Sylvania. During July through September, four of these modems will be modified to improve performance on dual diversity and non-diversity channels. Present planning is that the four modified modems will be shipped to test sites somewhere in Europe toward the end of 1976 for a six month system test program under combined DCA and NATO sponsorship.

The two modems that were used on the Youngstown to Verona N.Y. (CONUS) tests are still on-site. They will be used for test and demonstration purposes and will eventually be returned to GTE Sylvania for a final inspection. The final disposition of the four unmodified modems is pending at this time.

The QSDTS is presently undergoing a modification to include a simulation of an aircraft flying through the common volume. This modification will be completed early in August 1976.

Modem Description

Modulator

Figure 9 is a functional level block diagram of the modulator. The transmit data mux and transmit timing serve to synchronize the incoming data to the stable (approximately 10-8 and 10-9) station reference. The modem will operate from either one or two parallel non-synchronous data sources. If clocks are not available from the time division multiplexer they are generated from the data. The framing bits are generated from an m=6 pseudo-random sequence. All timing synchronization is accomplished by means of type two PLL's (phase-locked loops) locked to the 5-MHz station clock. Data rate changes are easily accomplished by changing pluggable VCXO units and moving straps in the digital feedback frequency dividers.

The modulator is a simple differentially encoded 4-PSK modulator utilizing the 5-MHz station clock up converted to 70 MHz. This card also provides a switchable loopback signal to the demodulation baseband converter for maintenance and test purposes.

The 70 MHz spectrum controller and driver provides two 0 to 50 mV (adjustable) outputs to the transmitter exciter and limits 99 percent of the power to a bandwidth of either 10 or 15 MHz. Bandwidth is changed by means of a pluggable two pole Butterworth filter. This card also provides four controlled-level loopback signals to the demodulator AGC IF Amplifiers for operation verification.

Demodulator

The block diagram of the demodulator is shown in Figure 10. Four AGC IF Amplifiers accept receiver output signals from -70 to -20 dBm and provide a -10 $\pm$1 dBm signal to the adaptive forward filter. These amplifiers operate in such a manner that the largest AGC voltage (receiver with the strongest signal) always controls the other three amplifiers. Each AGC Amplifier is on one printed circuit card. Bandwidth limiting is accomplished by a pluggable 2-pole Butterworth Filter. These filters are changed for each data rate change.

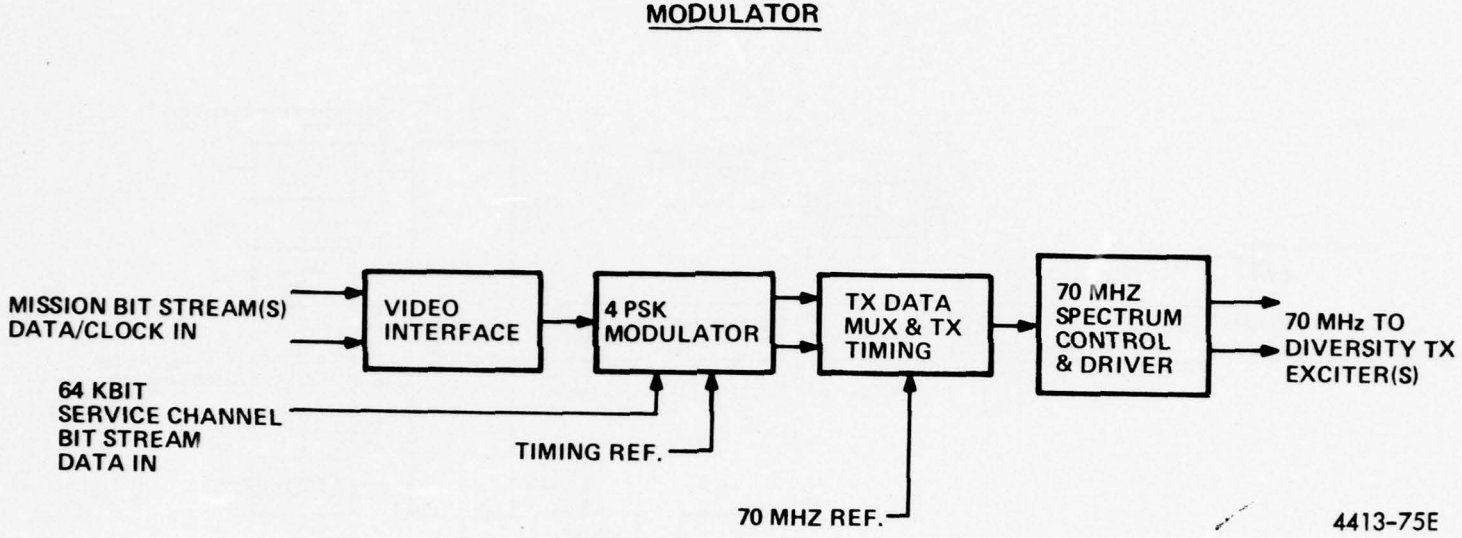


Figure 9. MDTS Modulator Block Diagram

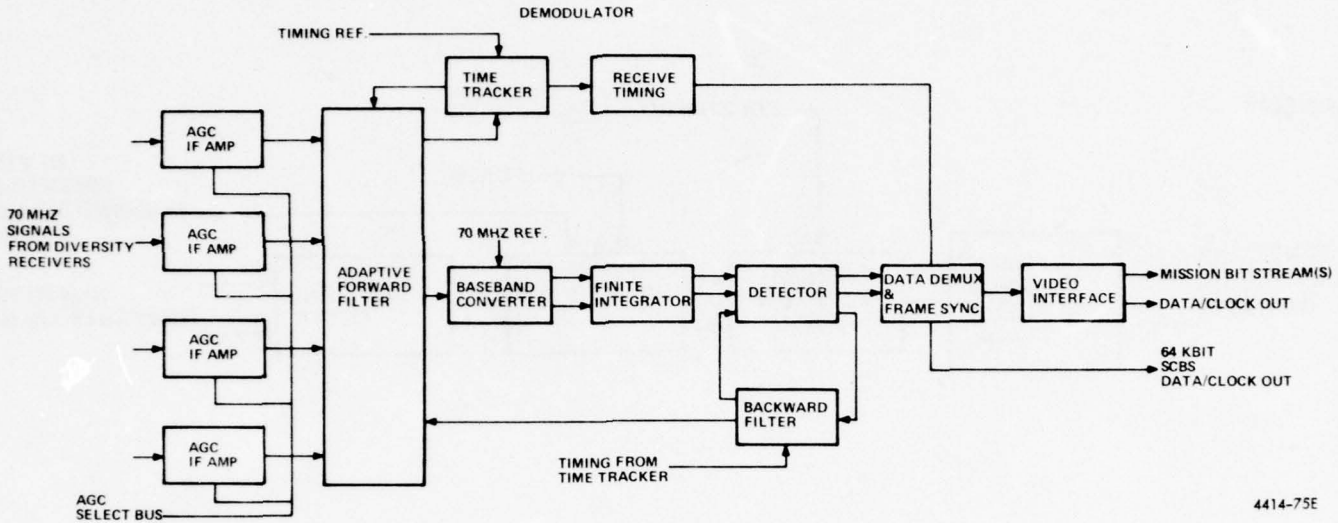


Figure 10. MDTS Demodulator Block Diagram

The adaptive forward filter is a three-tap multichannel transversal filter operating at 70 MHz. The tap spacing is one-half a symbol interval. The function of this filter is to diversity-combine, remove Doppler effects, and eliminate future digit inter-symbol interference. The filter utilizes quartz acoustic surface wave delay lines. The transversal filter weights are generated by correlation of the IF signals with a decision-directed error signal. The signals on the side taps of the three-tap transversal filter are used to form a discriminator characteristic for determining and tracking the symbol epoch. The adaptive forward filter is made up of 19 printed circuit cards - one input/fixed delay card per channel, three identical tap multiplier cards per channel, one tapped delay line, an error detector and an error amplifier card.

The baseband converter functions as the inverse of the 4-PSK modulator; that is, it mixes the equalized input 70-MHz signal with the 70-MHz reference. The output of the converter provides both the In-phase (I) and Quadrature (Q) channels. Each signal is passed through a finite integrator and detector. The I and Q channels are maintained separately up to the data demultiplex operation.

The backward filter is a transversal filter having up to five taps spaced at the symbol interval. This filter removes past digit inter-symbol interference. The backward filter weights are generated by correlation of delayed data with the decision-directed error signal. The backward filter, digitally implemented, consists of two control cards and from one to five identical tap cards. During the simulated link and field test portions of the program only 3 of the 5 taps were used since this number of taps was found to be adequate for the test situations encountered.

The two data demultiplex and frame synchronization cards provide frame synchronization for extraction of the two Mission Bit Streams, the Service Channel Bit Stream, and framing data. The video interface co-located with the modulator video interface provides the transition from TTL levels of ± 0.5 to ± 3.0 volts, 78 ohms balanced line for interfacing with the external mux units. Order wire data interfaces directly to MIL-STD-188C.

BITE

Minimum down time is a major requirement of the MDTS modem. For this reason, the MDTS is designed with high

reliability parts and extensive built-in test equipment (BITE). The Operational/Test panel is almost totally devoted to BITE and performance monitoring. Receiver power is continuously monitored as a function of the AGC voltage; both the bus voltage (which is always the strongest signal) and the individual channel levels can be monitored.

The BER indicator provides a single digit indicator which is the BER in the form of 10-x, where x is 1 through 9. The BER is determined bylong-term averaging of errors in the 14-Kb/s sync sequence. The averaging time is switch-selected between 20 seconds or 5 minutes.

In addition to these monitors, there are three levels of BITE: on-line BITE, off-line BITE, and test point verification. On-line BITE consists of continuously scanning the fault monitors built into each card. For many failures, on-line BITE will isolate the fault to a single card and the only down time required will be the time to change the card. Further analysis of modem operation can be made by placing the modem in the test mode and manually selecting 11 tests in the off-line BITE mode. Each test, when initiated, automatically runs through a complete cycle and indicates the faulty card by number, if indeed a fault is detected. The select switch causes the modem to loop back upon itself at various stages and pre-selects the required known input stimulus and output comparator.

Power Subsystem

The MDTS Circuits require $\pm$15, $\pm$5, and +24 VDC. Each of these voltages is provided by an easily replaceable modular power supply. Each supply has over-current protection, over-voltage protection, and a circuit breaker. Automatic monitors, both high and low voltage, are provided on each DC voltage plus the line voltage. Manual monitoring is also provided.

Physical Characteristics

The MDTS modem shown in Figure 1 is 70 inches high with the base, 27 inches deep, and 24 inches wide. For shelter-mounting the 4-inch base is removed. Replaceable circuit cards are accessed from the front of the card nest. All other replaceable circuit assemblies can be accessed from the front of the unit with the card nest pulled out and in the open position. All interface cabling is made at the top. Air enters the lower front of the cabinet and exhausts

through the top. Sides and back are designed for flush mounting. The complete rack weighs 470 pounds. It operates from a 47 to 63 Hz, 120 ± 10 percent VAC, 1Ø, 6.6 amp prime power source. All circuitry is on printed circuit cards 6 by 10 inches.

Environmental Characteristics

The equipment operates over a temperature range of -25 degrees F to +125 degrees F, 15,000 feet altitude, and meets the requirements for fungus, sand and dust, and shock and vibration consistent with normal military shipping requirements. The equipment also meets the Electromagnetic Interference requirements of MIL-STD-461 for modems.

Ancillary Equipment

The MDTS program provided for the development of special test equipment required to demonstrate performance both in the laboratory and for field tests. To this end the following four test equipments were developed.

a. The Quadruple Space Diversity Test Simulator (QSDTS) is a channel simulator which can be accurately set to simulate a large range of troposcatter propagation paths. The device operates at IF (70 MHz) and provides up to four independent paths with each having sixteen tap delayed gains. Provisions are made for additive noise and flat fading as well as frequency selective fading. A more detailed description of the QSDTS is given in Appendix B.

b. The Audio Order Wire Unit provides an analog-to-digital conversion for technical control voice communication for transmission over the 64 Kb/s order wire line provided in the MDTS. This device is configured so that it can be used at the end of a link or can be interspersed in a relay station for receiving or transmitting order wire voice communications in either direction.

c. The Source Data Simulator is a combination pseudo-random data generator and correlator used to provide test digital data streams at the transmitting MDTS video interface and to

provide error pulses at the receiving MDTS video interface. The unit will provide two high data rate pseudo-random data streams and one 64 Kb/s pseudo-random data stream to simulate either serial or parallel inputs to the MDTS and operate the 64 Kb/s order wire channel.

d. The Static Channel Simulator is a power splitter with separate attenuators in each of four outputs. These provide a means to externally loop the modem in a back-to-back mode for static channel tests.

SECTION 2

MDTS THEORY OF OPERATION

GENERAL

The MDTS modem is capable of operating at nominal data rates of 1.5, 3.1, 6.3, 9.4, and 12.6 Mb/s. Previous digital troposcatter modem prototypes have been limited to less than 3 Mb/s before the MDTS modem develpment began. The successful implementation of an engineering development model of a troposcatter modem at greater than 4 times previous achievable data rates was made possible by a decision-feedback equalization technique [1]. This technique uses adaptive tapped-delay-line (TDL) filters for each diversity branch and an adaptive TDL filter which processes the modem decisions. The diversity TDL filters are called forward filters and their action is to combine the diversity channels and eliminate intersymbol interference under fading channel conditions. The adaptive TDL filter which processes decisions is called a backward filter and its action is to eliminate intersymbol interference from past decisions. The forward filters thus need only eliminate intersymbol interference from decisions not yet made, i.e., future decisions.

This equalization capability allows the MDTS modem to operate when the width of the multipath profile of the channel is significantly greater than the transmitted symbol duration. Since DCS troposcatter systems can be expected to have multipath profiles with widths on the order of 100 to 500 nanoseconds, and require data rates on the order of 6 to 9 Mb/s, it is clear why special techniques are required. In addition to protection from multipath induced intersymbol interference, an adaptive decision-feedback equalizer will coherently recombine the desired signal from each of the multipath channel components. Because each delayed path in the fading channel structure is decorrelated from the other paths, a fade in one path will not produce an outage. Each multipath component can be thought of as a separate diversity channel with some correlation between channels. Since most of the diversity gain is realized even when the normalized correlation coefficient between branches is on the order of 0.5, coherent recombining of the fading multipath components increases the effective diversity order. Thus the decision-feedback equalizer provides an

implicit diversity gain which is in addition to the explicit diversity gain provided by the radio system in the form of additional frequencies, antennas, or angle diversity feedhorns.

Adaptation of the decision-feedback equalizer is accomplished by deriving a common error signal from the modem decisions. The error signal is the difference between the modem decision and the sample upon which the decision was made. This one error signal is used to adapt the TDL weights in both the forward and backward filters. Channel rms Doppler spreads of up to 10 Hz and specular Doppler offsets arising from aircraft reflections of up to 150 Hz can be accommodated by the adaptation algorithm.

The MDTS modem uses differentially encoded 4 PSK as the modulation format. The 99 percent power bandwidth is less than 15 MHz for 12.6 and 9.4 Mb/s and less than 10 MHz for data rates equal to or less than 6.3 Mb/s. The MDTS modem, in principle, could be operated at greater transmission efficiencies than that required for this program. RF bandwidth approaching 1 bit/Hz without significant modifications to the modem or performance degradations could be accomplished. A simplified diagram of the modem structure showing the adaptive decision-feedback equalizer is presented in Figure 11. The average error probability of a decision-feedback equalizer (DFE) operating in a fading multipath channel requires the solution for the optimum weights for a fixed channel, the determination of the error probability function of those weights for a fixed channel, and the computation of the average with respect to the ensemble of channel members. This calculation can be done exactly in the absence of intersymbol interference to produce a lower bound on the DFE performance and to assess its intersymbol interference penalty. When twice the standard deviation of the multipath profile is less than 40 percent of the 4 PSK symbol width, $2\sigma/T < 0.4$, comparison of measured modem performance (3 tap forward filter) and the lower bound show that the bound is tight. The calculation of this lower bound considers the number of taps in the forward filter TDL. The bound is reduced with increasing number of taps until the ideal performance of the one-shot matched filter is realized. The performance calculations presented in this report are all for a three-tap forward filter with tap spacing equal to one-half a symbol interval.

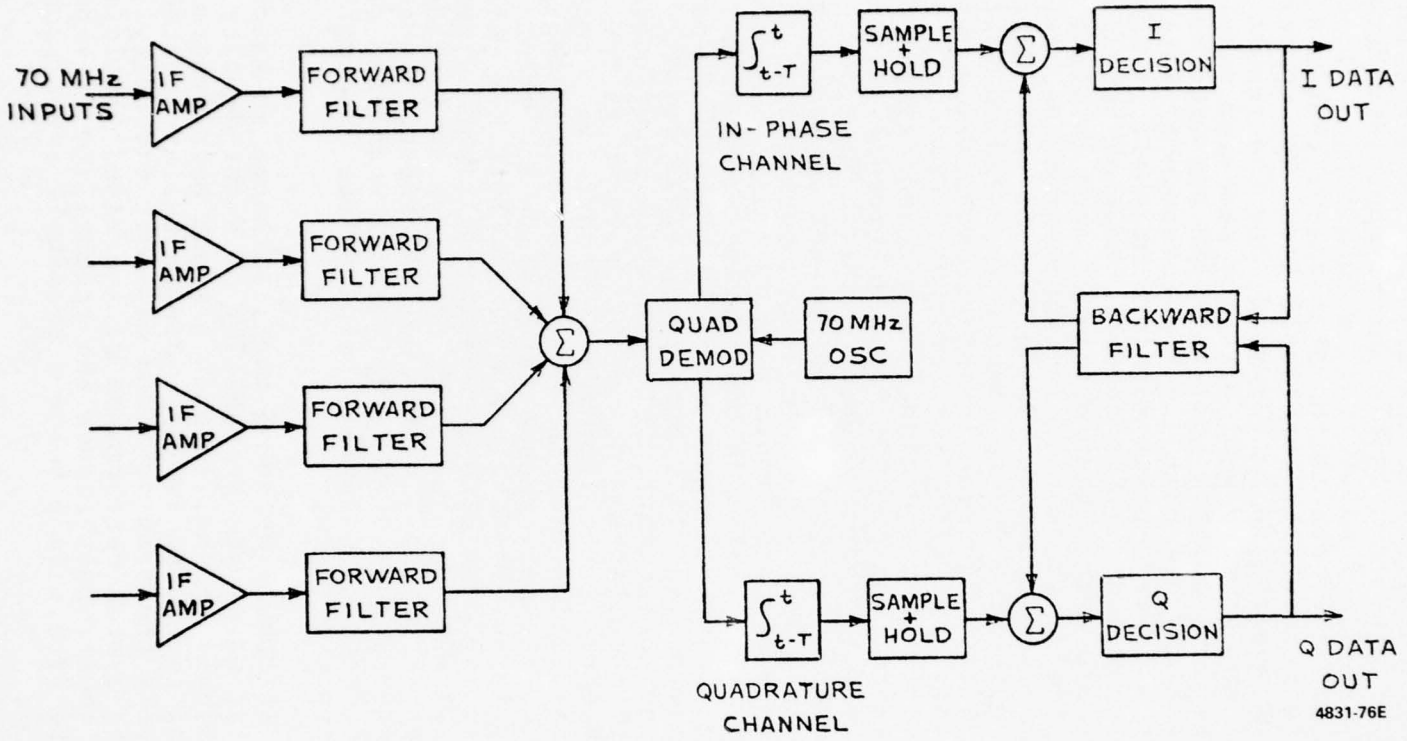


Figure 11. MDTS Modem Structure Block Diagram

At $2\sigma/T$ values larger than 0.4, the presence of multipath energy beyond the span of the 3 tap forward filter results in a non-negligible intersymbol interference penalty. An exact solution is a formidable, if not impossible, task due to the statistical characteristics of the error probability functional form. Two approximations allow the average to be computed, and the resulting calculations compare well with the measured results. The approximations compare well with the measured results. The approximations are that (1) the intersymbol interference is Gaussian with mean power equal to one-half of the binary interference and (2) the ensemble mean of the intersymbol interference correlation matrix is used in place of the matrix itself. The matrix is random with respect to channel members in the ensemble. The effect of these approximations is to require the DFE to operate in a fading multipath channel with a Gaussian interferer with fixed channel characteristics. Since most of the errors occur due to fading of the desired signal, gross approximations in the interference character do not significantly alter the resulting performance characteristics. With one exception, the calculated performance for an average error probability of 10^{-6} is within 1 dB of measured performance for quad diversity tests and within 2 dB of measured performance for dual diversity tests. In one instance at dual diversity under excessive multipath conditions the performance calculations are overly optimistic. This deviation is attributed to saturation effects which occur under extreme multipath conditions and are not included in the theoretical model. A Performance Improvement Program in progress will reduce saturation effects under these conditions. The results of the performance calculation are shown in Figure 13 for some selected values of 2 /T. Note how performance initially improves with increasing multipath (implicit diversity) and then falls off again due to finiteness of the equalizer structure (intersymbol interference penalty). The "optimum" value of 2 /T is larger for quad than dual diversity because diversity helps reduce intersymbol interference effects.

It should be noted that, although an exact determination of the probability of error density function for realistic channel spreads has not been determined, the effect of increased implicit diversity is expected to be essentially the same as added explicit diversity. The effect on system performance of increased implicit diversity will be to strongly reduce the probability of experiencing an outage (i.e., fade below a threshold error probability)

while also reducing the duration of the outage to a lesser but still significant extent.

Communication System Definition

The communication system model under consideration is shown in Figure 12. Complex notation is used to present in-phase and quadrature components and explicit modulation/demodulation operations are not shown. The data to be transmitted (s_k) are selected from the set ($\pm 1 \pm j$) for a quaternary phase-shift-keying system. The transmitted waveform is

$$s(t) = \sum_{k=-\infty}^{\infty} s_k f\ (t-kT)$$

where T is the interval between successive symbol transmission, i.e. symbol interval. The transmitter impulse response f(t) is defined as a unit energy real function.

The troposcatter channel can be represented by an ensemble of zero-mean random functions with complex Gaussian statistics. Individual diversity channels are considered to be independent of each other and the ensemble is completely described by the second moment

$$\overline{h_i(t)\ h_j^*(t)} = \delta_{ij}\delta\ (t-\tau)\bar{E}_b\ p(t)\ ,\ i,j=1,2,\ldots D.$$

The unit area function p(t) is the delay power spectrum or multipath profile. It represents the average power response at each delay value to impulse function excitation. The RMS width of this function is referred to as the RMS multipath spread, σ . The received energy per bit per diversity channel is given by

$$\int_{-\infty}^{\infty} dt \left| \int f(t-u)h_i(u)du \right|^2 = \int_{-\infty}^{\infty} dt \int_{-\infty}^{\infty} f^2(t-u)\bar{E}_b p(u)\ du$$

$$= \bar{E}_b \int_{-\infty}^{\infty} p(u)\ du = \bar{E}_b$$

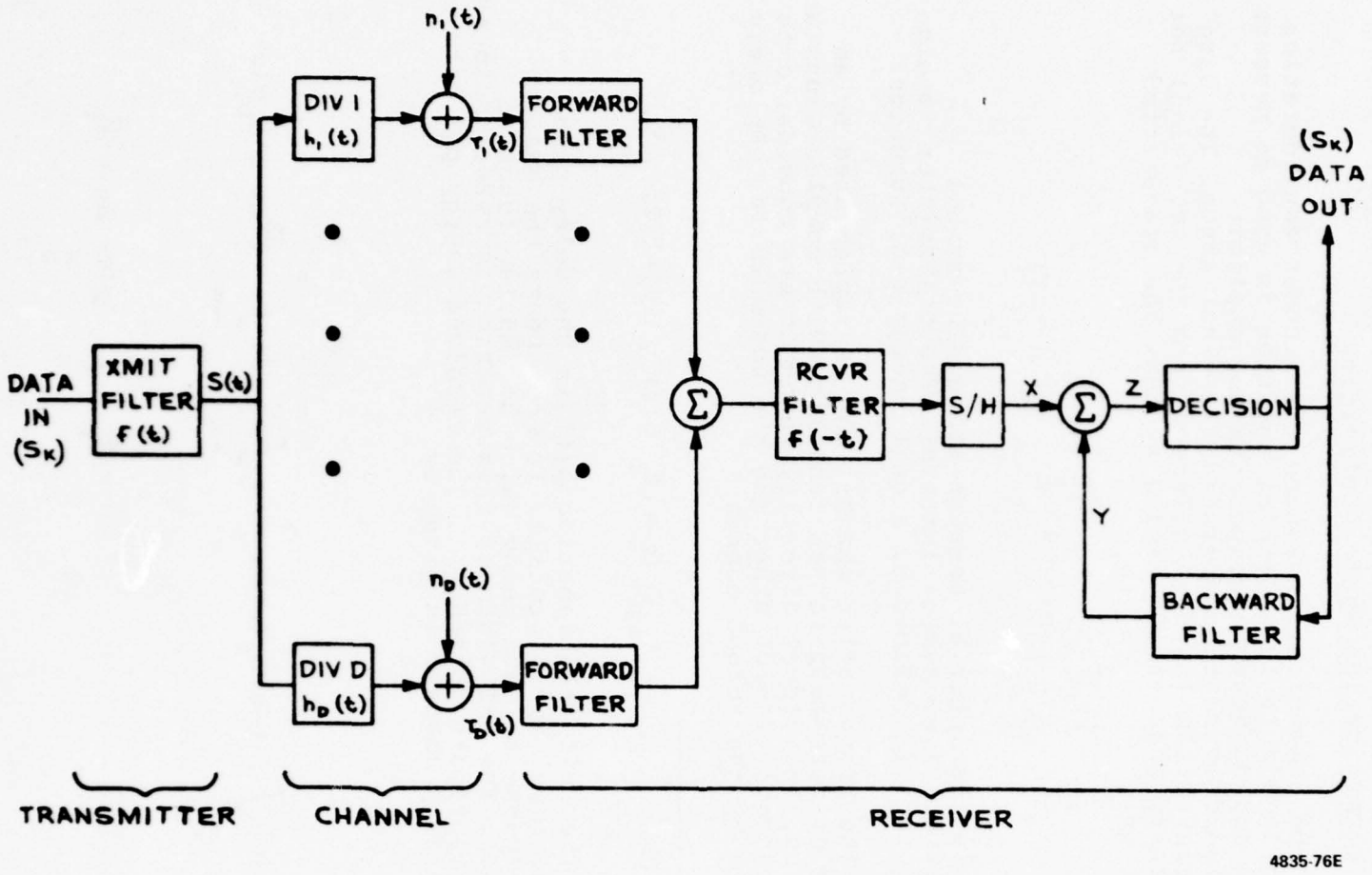


Figure 12. Communication System Model

The ensemble representation is used here because the analysis to follow assumes a slowly varying multipath channel which the equalizer can track. Hence the performance is determined by averaging the bit error probability for the minimum mean square error (MMSE) equalizer over the channel ensemble. An overbar is used to denote channel ensemble averages. Brackets $\langle\ \rangle$ will be used to denote average over noise or source statistics for a particular channel realization. For the white Gaussian noise channels the additive noise terms are zero mean and have second moments

$$\langle n_i(t) n_j^*(t) \rangle = N_o\ \delta_{ij}\ \delta(t-\tau)\ ,\ i,j=1,2,\ldots D.$$

Each forward filter in a realizable DFE consists of a finite length tapped delay line filter with impulse response

$$w_i(t) = \sum_{k=-K_1}^{K_2} w_{ik}^*\ \delta\ (t-k\tau)$$

where the tap gain value is chosen with a complex conjugate for notational convenience later. The receiver filter has impulse response f(-t) which matches the transmit pulse waveform. For this choice in the absence of multipath and after time synchronization, the optimum tap weights for each forward filter reduce to one tap on and the rest off. The output of the receiver filter is sampled at the symbol rate 1/T and held for a symbol interval. The backward filter correction sample is summed with the sampled receiver filter output to produce the detection variable z. The backward filter has a sample output

$$y = \sum_{i=1}^{B} b_i \hat{s}_{k-i}$$

at the decision time for the s_k symbol. The decision on s_k is denoted as $\hat{s}_k$. The decision process takes the form

$$\hat{s}_k = \begin{cases} \text{csgn}\ (z) \text{ for QPSK} \\ \text{sgn}\ (z) \text{ for BPSK} \end{cases}$$

where csg and sgn represent the signum operations applied to the co-phase 1 and quadrature symbol components respectively.

The parameters of the DFE are the number of forward filter taps, $K=K_1+K_2+1$, the forward filter tap spacing, τ, and the number of backward filter taps, B. The optimum DFE requires $K=\infty=B$ and $\tau=1/W$ where W is the two-sided bandwidth. A practical choice of parameters for troposcatter channels was determined to be $K=3=B$ and $\tau=T/2$.

Performance Analysis

Previous methods of determining average error probability performance of practical equalizer structures have been restricted to Monte Carlo simulations [2,3] using an ensemble of multipath channels. An analytic approach for calculating the average error probability is complicated by the presence of an intersymbol interference term in the signal-to-noise ratio (SNR) expression for a particular channel realization. Because of this term, an average over the channel ensemble is a formidable task. On the other hand, omission of the intersymbol interference term leads to an average error probability which for a fixed SNR monotonically decreases with increasing multipath spread. For any practical equalizer with a fixed SNR the average error probability will initially decrease for increasing multipath spread but then increase as the multipath exceeds the equalizer's capability to mitigate the intersymbol interference. Elimination of the intersymbol interference term provides a convenient lower bound which both shows the intersymbol interference penalty and is an accurate performance estimate for small multipath spreads but is too loose for performance calculation when the rms multipath spread is on the order of the forward filter width. The analytic procedure presented below allows an accurate calculation of the lower bound for no intersymbol interference and, by an approximation of the intersymbol interference effect, provides a good performance estimate for the large multipath case.

For notational simplicity this analysis considers a non-diversity channel and extends the final result for higher order diversity systems. Quadrature phase shift keying is used in the analysis as this is the modem modulation format. The received signal has the form

$$r(t) = \sum_{i=-\infty}^{\infty} s_i \int h(u)\, f(t-iT-u)\, du + n(t). \qquad (2\text{-}1)$$

We define the combined transmitter and receiver response as

$$g(t) = \int_{-\infty}^{\infty} f(t+u)\ f(u)\ du \tag{2-2}$$

and its convolution with the channel as

$$\sqrt{\bar{E}_b}\, q(t) = \int_{-\infty}^{\infty} g(t-u)\ h(u)\ du. \tag{2-3}$$

For a sampling time t_o, the detection variable z has the form

$$z = \sum_{k=-K_1}^{K_2} w_k^* \left[\sum_{i=-\infty}^{\infty} s_i \sqrt{\bar{E}_b}\, q(t_o - iT - k\tau) + v(t_o - k\tau) \right] \tag{2-4}$$

where

$$v(t_o) = \int n(t_o - u)\ f(u)\ du \tag{2-5}$$

is a zero-mean Gaussian variate with second momemt

$$\left\langle v(t_o - k\tau)\ v^*(t_o - \ell\tau) \right\rangle = N_o\, g(k\tau - \ell\tau)\ . \tag{2-6}$$

Equation (3.4) has an obvious representation in a $K = K_1 + K_2 + 1$ dimensional column vector form as

$$z = \underline{w}' \left(\sqrt{\bar{E}_b} \sum_{i=-\infty}^{\infty} s_i\, \underline{q}_i + \underline{v} \right) \tag{2-7}$$

where the accent mark refers to complex conjugate transpose. The vector $\underline{w}$ represents the forward filter complex tap gains, $\underline{q}_i$ represents the sampled continuous filter response for the ith transmitted symbol, and $\underline{v}$ is a zero-mean Gaussian noise vector process with positive definite covariance matrix $N_o G_o$ with element values

$$N_o\, G_{k\ell} = N_o\, g(k\tau - \ell\tau). \tag{2-8}$$

For 4 PSK every other bit decision is made on the real part of z and there is quadrature symmetry. The real noise power affecting that decision is

$$\delta_o^2 = \left\langle (\mathrm{Re}\underline{w}'\underline{v})^2 \right\rangle = \frac{N_o}{2}\,\underline{w}'G_o\underline{w} \qquad (2\text{-}9)$$

If one assumes $s_k=0$, $k \neq 0$, there is no intersymbol interference and the analysis for the average error probability leads to an SNR expression for a particular channel realization which is a quadratic form of the type $\underline{g}_o' G_o^{-1} \underline{g}_o$ where $\underline{g}_o$ is a complex Gaussian vector with statistics determined by the channel and G_o is a positive definite matrix. After a diagonalization procedure the average of the error probability function of the SNR can be computed for both coherent and differentially coherent detection. This calculation leads to the lower bound expression. When the intersymbol interference is present an effective signal-to-noise ratio can be defined which leads to a quadratic form but both the vector and the matrix have random components. A method of averaging over a function of this quadratic form is not apparent. One course worth considering is to approximate the intersymbol interference effect in a manner which will modify the G_o matrix but keep its deterministic nature. This can be accomplished if the following two approximations are made.

(1) Assume the interference symbols s_i, $i \neq 0$, are Gaussian distributed rather than binary.

(2) Approximate the matrix contribution to G_o due to intersymbol interference by its mean.

This approach assumes that the intersymbol interference after equalization in a fading multipath channel can be well approximated by an equivalent additive Gaussian noise term. As will be seen this approach does provide performance estimates which compare very well with measured results.

One can reasonably assume that the backward filter cancels the interference contribution due to past symbols, i.e., symbols which arrive before the symbol currently being decided on. If we arbitrarily take the symbol selected for decision as s_o, the remaining interference is classified as future and is given by

$$\sqrt{\bar{E}_b} \sum_{i=1}^{I} s_i \underline{w}' \underline{q}_i \equiv \underline{w}' \underline{v}_1 \cdot \tag{2-10}$$

The sum can be truncated after a few terms as the dot product will disappear for large i due to the finite duration of the pulse function q(t). The first approximation is to take s_i as a zero mean Gaussian with mean squared value y^2. This quantity should be less than unity as approximating a unit magnitude binary variable by a unit variance Gaussian variable will lead to pessimistic performance results due to the tails of the Gaussian distribution. A choice of $y^2 = 1/2$ was found to provide excellent agreement between calculated and measured values.

Equation (2.7) can be rewritten as

$$z = \underline{w}' \left(\underline{q}_o \sqrt{\bar{E}_b}\, s_o + \underline{v} + \underline{v}_1 \right) \tag{2-11}$$

and since the additive noise contribution from $\underline{v}$ is independent of the source digit contribution from $\underline{v}_1$, the effective noise power effecting the decision for the real part of s_o is:

$$\delta^2 = \left\langle \left[\text{Re } \underline{w}' (\underline{v} + \underline{v}_1) \right]^2 \right\rangle$$

$$\delta^2 = \frac{N_o}{2} \underline{w}' G_o \underline{w} + \frac{1}{2} \underline{w}' \left\langle \underline{v}_1 \underline{v}_1' \right\rangle \underline{w}. \tag{2-12}$$

Performing the indicated averaging with respect to the source digits, one has

$$\left\langle \underline{v}_1 \underline{v}_1' \right\rangle = \bar{E}_b \gamma^2 \sum_{i=1}^{I} \underline{q}_i \underline{q}_i' \cdot \tag{2-13}$$

If we augment the G_o matrix by $E_b<\underline{v}_1\underline{v}_1'>/N_o$, the resulting matrix in the quadratic form will have random vector elements due to the presence of the $\underline{q}_i$ terms. The second approximation is to replace the intersymbol interference contribution $<\underline{v}_1\underline{v}_1'>$ by its mean with respect to the channel ensemble, $<\underline{v}_1\underline{v}_1''>$. Thus let

$$G_1 = \frac{\bar{E}_b}{N_o}\,\gamma^2 \sum_{i=1}^{I} \overline{\underline{q}_i\,\underline{q}_i'} \tag{2-14}$$

and augment the G_o matrix to form

$$G = G_o + G_1 \ . \tag{2-15}$$

The equivalent noise power is then given by

$$\delta^2 = \frac{N_o}{2}\,\underline{w}'\,G\,\underline{w} \tag{2-16}$$

where G is a deterministic matrix. We define the signal-to-noise ratio (SNR)

$$\rho \equiv \frac{\bar{E}_b}{2\delta^2}\left[\mathrm{Re}\ \underline{w}'\underline{q}_o\right]^2 \tag{2-17}$$

which we seek to maximize as a function of the forward filter weight $\underline{w}$. Consider the generalized dot product defined on the positive definite matrix G, i.e.,

$$(\underline{u},\ \underline{v}) \equiv \underline{u}'G\underline{v} \ . \tag{2-18}$$

Equation (3.17) can be written as

$$\rho = \frac{\bar{E}_b}{N_o}\,\frac{\left[\mathrm{Re}\,(\underline{w}, G^{-1}\underline{q}_o)\right]^2}{(\underline{w},\underline{w})} \tag{2-19}$$

and by a generalization of the Schwartz Inequality we obtain

$$\rho \le \frac{\bar{E}_b}{N_o}\,\frac{|(w,\ G^{-1}\underline{q}_o)|^2}{(\underline{w},\underline{w})} \le \frac{\bar{E}_b}{N_o}\,(G\underline{q}_o^{-1},\ G^{-1}\underline{q}_o) \tag{2-20}$$

with equality if and only if

$$\underline{w}_{opt} = G^{-1}\underline{q}_o \tag{2-21}$$

The maximum SNR is then

$$\rho_{max} = \frac{\overline{E}_b}{N_o}\, \underline{q}'_o\, G^{-1}\underline{q}_o \tag{2-22}$$

As a check on the normalization, if $\sigma = 0$ and $t_o = 0$ we have from Equation (2.3)

$$q(-k\tau) = g(-k\tau) = G_{ok} \tag{2-23}$$

and then

$$\rho_{max} = \frac{\overline{E}_b}{N_o}\, g(0) = \frac{\overline{E}_b}{N_o} \tag{2-24}$$

as is expected in the absence of multipath.

We will now establish that the mean square error function

$$\langle \varepsilon^2 \rangle = \langle |z - ds|^2 \rangle \tag{2-25}$$

which is minimized by the decision-feedback equalizer leads to the same set of forward filter weights as maximization of the SNR in Equation (2-17) for the appropriate choice of scale factor d. After squaring and averaging (2-25) becomes

$$\langle \varepsilon^2 \rangle = \overline{E}_b\, \underline{w}'\underline{g}_o\underline{g}_o'\underline{w} - 2\sqrt{E_b}\, d\, \mathrm{Re}\underline{w}'\underline{q}_o + N_o\, \underline{w}'\, G\underline{w} \tag{2-26}$$

$$= |\sqrt{\overline{E}_b}\, \underline{w}'\underline{q}_o - d|^2 + N_o\, \underline{w}'\, G\underline{w} - d^2 .$$

Minimization of Equation (2-26) is equivalent to the LaGrange multiplier problem

$$\min \underline{w}'G\underline{w} - 2\beta \underline{w}' \underline{q}_o \tag{2-27}$$

which has solution

$$\underline{w} = \beta G^{-1} \underline{q}_o \ . \tag{2-28}$$

Since equation (2-21) and (2-28) are the same except for an unimportant scale factor, we have established that the maximum signal-to-noise ratio for a minimum mean-square error DFE and a particular channel realization is the quadratic form given by Equation (2-22). The matrix G is a deterministic function of the transmitter and receiver filter characteristics and the channel statistics. The vector $\underline{q}_o$ is a random vector associated with the fading channel ensemble. In order to find the average error probability it will be necessary to average over the channel ensemble. The error probability for a particular channel realization is from Equation (2-11) and (2-21)

$$p_c = \tfrac{1}{2} \text{ pr } \left\{ \varepsilon > 1 \right\} + \tfrac{1}{2} \text{ pr } \left\{ \varepsilon < -1 \right\} \tag{2-29}$$

where is a zero-mean Gaussian random variable with standard deviation equal to $\sqrt{1/2\rho_{max}}$. The bit error probability is

$$p_c = \frac{1}{\sqrt{2\pi}} \int_{2\rho_{max}}^{\infty} e^{-u^2/2} \, du = 1/2 \text{ erfc } \sqrt{\rho_{max}} \tag{2-30}$$

The subscript c denotes that the detection process was coherent, i.e. the receiver knows the transmitted carrier phase. Differential detection of phase-shift-keyed signals yields a bit error probability (4)

$$p_d = 1/2 \ e^{-\rho_{max}} \tag{2-31}$$

Although equalizer systems are normally coherent, Equation (2-31) provides a convenient approximation for the bit error probability performance for practical systems and thus its ensemble average is also of interest.

Let $y(x)$ be the probability density function for ρ_{max} and $Y(S)$ its Laplace transform. We want to calculate

$$\bar{p}_c = \int_0^\infty 1/2 \text{ erfc } \sqrt{x}\, y(x)\, dx \qquad (2\text{-}32)$$

$$\bar{p}_d = \int_0^\infty 1/2\, e^{-x}\, y(x)dx = 1/2\, Y(1) \qquad (2\text{-}33)$$

The Laplace transform $Y(s)$ is easily obtained after a diagnolization of the quadratic from Equation (3.22).

$$x = \frac{\bar{E}_b}{N_o} \underline{g}_o' G^{-1} \underline{g}_o = \frac{\bar{E}_b}{N_o} \underline{\alpha}'\underline{\alpha} \qquad (2\text{-}34)$$

where $\underline{\alpha}$ is a zero-mean complex Gaussian vector with a diagonal covariance matrix $\Gamma_{ij} = \lambda_i \sigma_{ij}$. The diagonalization resulted from the transformation

$$\underline{\alpha} = MG^{-1/2} \underline{g}_o \qquad (2\text{-}35)$$

and M is the normalized model matrix for the matrix

$$G^{-1/2} \overline{\underline{g}_o \underline{g}_o} G^{-1/2}, \text{ i.e.} \qquad (2\text{-}36)$$

$$G^{-1/2} \overline{\underline{g}_o \underline{g}_o} G^{-1/2} M = M\Gamma \qquad (2\text{-}37)$$

$$M'M = I \ .$$

Thus the eigenvalues λ_i are also the eigenvalues of the symmetric matrix $G^{-1/2}\, \underline{g}_o \underline{g}_o' G^{-1/2}$ and the unsymmetric matrix $G^{-1/2}\, \underline{g}_o \underline{g}_o'^{-1/2}$. Since the components of $\underline{\alpha}$ are uncorrelated Gaussian, the probability density for ρ_{max} is the convolution of exponential densities which yields a Laplace transform in product form.

$$Y(s) = \prod_{k=-K_I}^{K_2} \left(1 + \frac{\bar{E}_b}{N_o} \lambda_k s\right)^{-1} \tag{2-38}$$

If there are D explicit diversity channels with identical statistics defined by (2.2), the Laplace transform for the SNR variate becomes

$$Y(s) = \prod_{k=-K_1}^{K_2} \left(1 + \frac{\bar{E}_b}{N_o} \lambda_k s\right)^{-D} \tag{2-39}$$

The error probability for DPSK is

$$\bar{P}_d = Y(1) = \prod_{k=-K_1}^{K_2} \left(1 + \frac{\bar{E}_b}{N_o} \lambda_k\right)^{-D} \tag{2-40}$$

For coherent detection it is necessary to find the coefficients in a partial fraction expansion of Y(s), i.e.

$$Y(s) = \sum_{i=1}^{D} \sum_{k=-K_1}^{K_2} A_{ik} \left(1 + \frac{\bar{E}_b}{N_o} \lambda_k s\right)^{-i} . \tag{2-41}$$

A recursive method for finding the coefficients and the resulting error probability for coherent detection is detailed in [3] where the average error probability for the infinite length optimum single pulse receiver was determined. The result is

$$\bar{p}_c = \sum_{i=1}^{D} \sum_{k=-K_1}^{K_2} A_{ik}\, p_i\,(\lambda_k) \qquad (2\text{-}42)$$

where $p_i\,(\lambda_k)$ can be calculated in closed form as

$$p_i\,(\lambda_k) = \sqrt{\lambda_k}/2\pi \sum_{m=0}^{i-1} G\,(m+0.5)/(1+\lambda_k)^{m+0.5} m! \qquad (2\text{-}43)$$

where G(.) is the Gamma function.

The above form is computationally inconvenient when $p_i << 1$ but taking advantage of knowledge that

$$\lim_{i\to\infty} p_i\,(\lambda_k) = 0 \qquad (2\text{-}44)$$

leads to a rapidly convergent series for $\lambda_K > 1$, i.e.,

$$p_i\,(\lambda_k) = \sqrt{\lambda_k}/2\pi \sum_{m=k}^{\infty} G\,(m+0.5)/(1+\lambda_k)^{m+0.5} m! \qquad (2\text{-}45)$$

The lower bound for coherent detection calculated here differs from the infinite length receiver lower bound in [3] by the eigenvalue distribution. Clearly the infinite length receiver will be superior to any finite realization of an equalizer.

For a DPSK system or for the use of the DPSK expression the Gaussian noise nonfading performance of a practical modem, calculation of the average error probability does not require the determination of the eigenvalues. Note that (2-40) has the determinant form

$$\overline{P_d} = (\det|I + \frac{\overline{E}_b}{N_o} G^{-1}C|)^{-D} \tag{2-46}$$

where the covariance matrix C is a function of the transmitter filter and the multipath profile, i.e.

$$C_{k\ell} = q(t_o - k_\tau)q^*(t_o - \ell\tau) = \int_{\infty} g(t_o - k\tau - u)g(t_o - \ell\tau - u)p(u)du \tag{2-47}$$

For a coherent detection system the eigenvalues of $G^{-1}C$ can be found by a matrix iteration procedure [5] for unsymmetrical matrices. The eigenvalues represent the normalized mean power for each independent implicit diversity branch of which there are $K=K_1+K_2+1$ branches. The sum of the eigenvalues is overbounded by unity. This is most easily shown through the physical observation that the presence of multipath does not increase the mean received energy per bit. We have

$$\rho_{max} = \frac{\overline{E}_b}{N_o} \underline{g}'_o G^{-1} \underline{g}_o \tag{2-48}$$

and its ensemble mean

$$\overline{\rho}_{max} = \frac{\overline{E}_b}{N_o} \overline{\underline{g}' G^{-1} \underline{g}_o} = \frac{\overline{E}_b}{N_o} \text{Trace} \left\{ G^{-1} \overline{\underline{g}_o \underline{g}'_o} \right\} \tag{2-49}$$

$$= \frac{\overline{E}_b}{N_o} \text{Trace} \left\{ G^{-1}C \right\} = \frac{\overline{E}_b}{N_o} \sum_k \lambda_k$$

Since $\bar{p}_{max} < E_b/N_o$ from physical considerations, it follows that the eigenvalue sum is overbound by unity. Thus one criterion in choosing the forward filter number of taps is that the eigenvalue sum be close to unity for the more extreme multipath situations.

As a result of this analysis, Equation (2-46) can be used to compute the predicted performance of the MDTS modem on a fading dispersive channel. The performance estimate includes the effects of both implicit diversity and intersymbol interference penalty as a result of a finite equalizer structure. The average bit error probability obtained from 2-46 is independent of data rate for a fixed value of $\bar{E}_b/N_o$ and a fixed ratio of multipath spread 20 to the symbol interval. Predicted performance curves for the operational range of the MDTS modem are given in Figure 13.

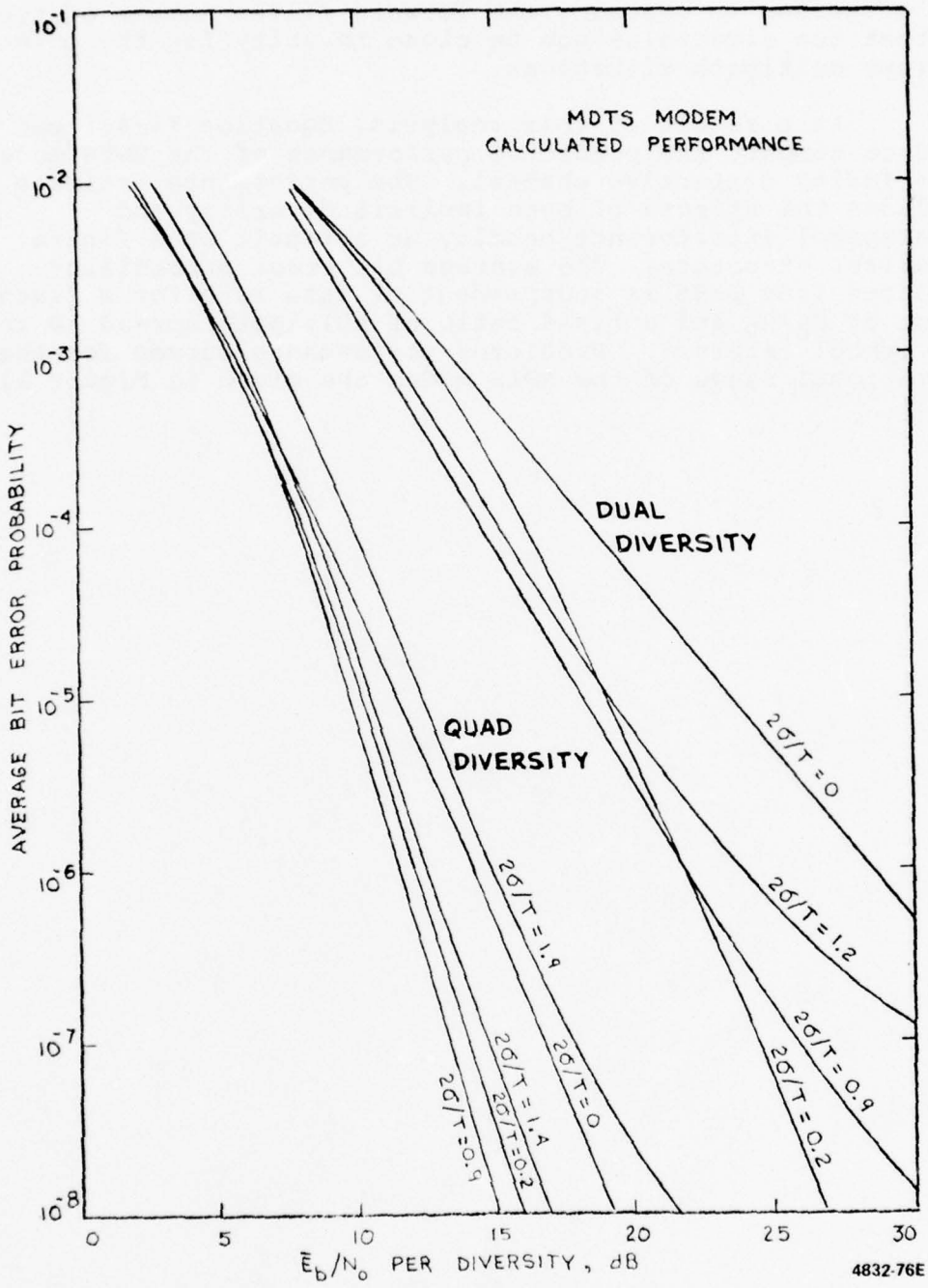


Figure 13. Calculated Performance Results

SECTION 3

FIELD TESTING

GENERAL

The field testing of the MDTS was performed from January 1976 through March 1976. During that period it was tested in dual and quad diversity modes at data rates of 12.6, 9.4, 6.3, and 3.1 Mbs over two radios, the AN/TRC-132A and the AN/MRC-98. In this section we describe the field test configuration, first considering the terminal equipment and path, then the data acquisition facilities, the test sequence and finally the test results.

Terminal Equipment and Path

All field tests were conducted over the 168 statute mile (146 nautical mile) path between Youngstown and Verona, New York. The path profile for this link is shown in Figure 14. The terrain between the terminals can be characterized as gently rolling.

The terminal equipments at each end of the link are identical, consisting of quad diversity AN/MRC-98 and AN/TRC-132A radios. Their important characteristics are shown in Table 3. The Youngstown AN/MRC-98 transmitter is assigned 882 and 907 MHz. Although capable of transmitting 10 kW, the transmitted power was kept at 2 kW for the MDTS tests. The transmitter bandwidth is nominally 7 MHz at the 1 dB points. The receiver has been modified by the addition of a solid-state RF amplifier which establishes its 4 dB noise figure. The 3 dB receiver bandwidth is 12 MHz, and the transmitting and receiving antennas are all 28 ft parabolas. The Youngstown AN/TRC-132A transmitter is assigned 4500 and 4690 MHz. As with the AN/MRC-98, it is capable of transmitting 10 kW but was operated at 2 kW for these tests. The transmitter was broadbanded for the MDTS tests, to a 1 dB bandwidth in excess of 12 MHz. At this power, the exciter required + 11.8 dBm to drive the power amplifier at 2 kW. The receiver noise figure is nominally 6 dB. The receivers were modified by the removal of a tuned circuit to have 3 dB bandwidths of approximately 20 MHz. Transmitting and receiving antennas were all 28 ft parabolas.

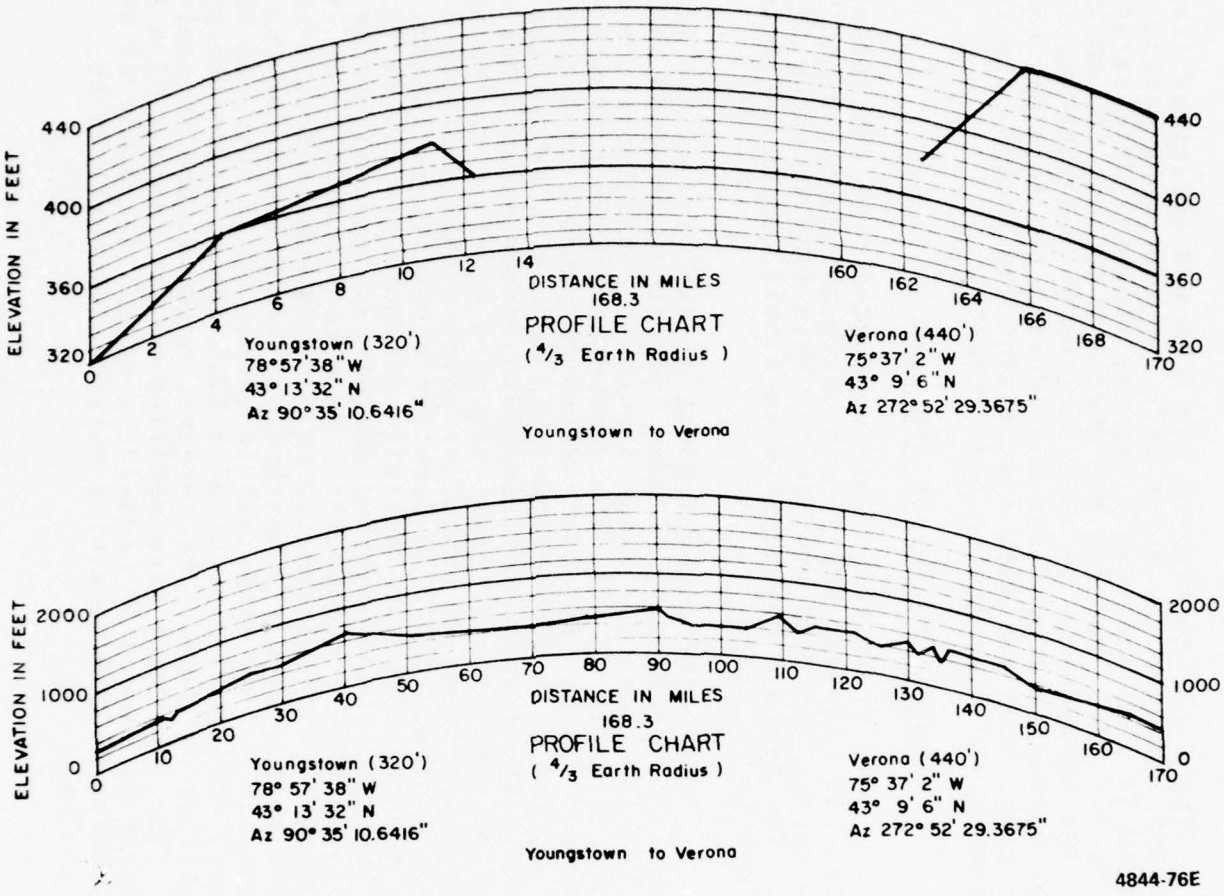


Figure 14. Youngstown - Verona Path Profile

TABLE 3. IMPORTANT RADIO CHARACTERISTICS

	AN/MRC-98	AN/TRC-132A
Transmitter Frequency, MHz	882, 907	4500, 4690
Transmitter Power, kW	2	2
Transmitter BW, MHz	7 (1dB)	$\geq$ 12 (1dB)
Exciter Input, dBm	+1.1	+11.8
Receiver NF, dB	4	6
Receiver BW, MHz	12 (3dB)	20 (3dB)
Antenna Diameter, Ft	28	28

The MDTS receiver modem is designed to operate with a 70 MHz IF input signal. The forward equalizer can remove up to approximately 0.5 kHz of mean Doppler on the received 70 MHz. The AN/MRC-98 and the AN/TRC-132A both have frequency accuracies in the order of 2×10^{-5} and 1×10^{-6}, respectively, which can result in frequency offsets on the received IF in the order of 40 kHz for the AN/MRC-98 and 10 kHz for the AN/TRC-132A. Both the AN/MRC-98 and the AN/TRC-132A require frequency stabilization so that digital data can be transmitted over them. The AN/MRC-98 was stabilized by frequency locking the transmitter and receiver crystal oscillators to HP frequency synthesizers set to the oscillator frequencies. This stabilization has been used on the AN/MRC-98 for a number of years, and is a standard procedure at Youngstown and Verona. The stabilization of the AN/TRC-132A is, however, more complex. Figure 15 shows the standard configuration of the AN/TRC-132A frequency converter. A frequency synthesizer outputs a signal in the 1 GHz range which is then multiplied x 4 and used as the local oscillator to the balanced modulator. Experiments performed at Youngstown prior to the MDTS tests showed that simple frequency stabilizing of the synthesizer did not reduce the phase noise to a sufficient degree to allow it to be used in digital transmission. Instead, the local oscillator was formed as shown in Figure 16. A H.P. crystal frequency standard and synthesizer output a CW signal, which is used as the input to a x-96 multiplier. The multiplier was borrowed from an AN/TRC-97 and its output was used directly as the local oscillator for the AN/TRC-132A. Thus, referring back to Figure 15, the 4 x multiplier of the

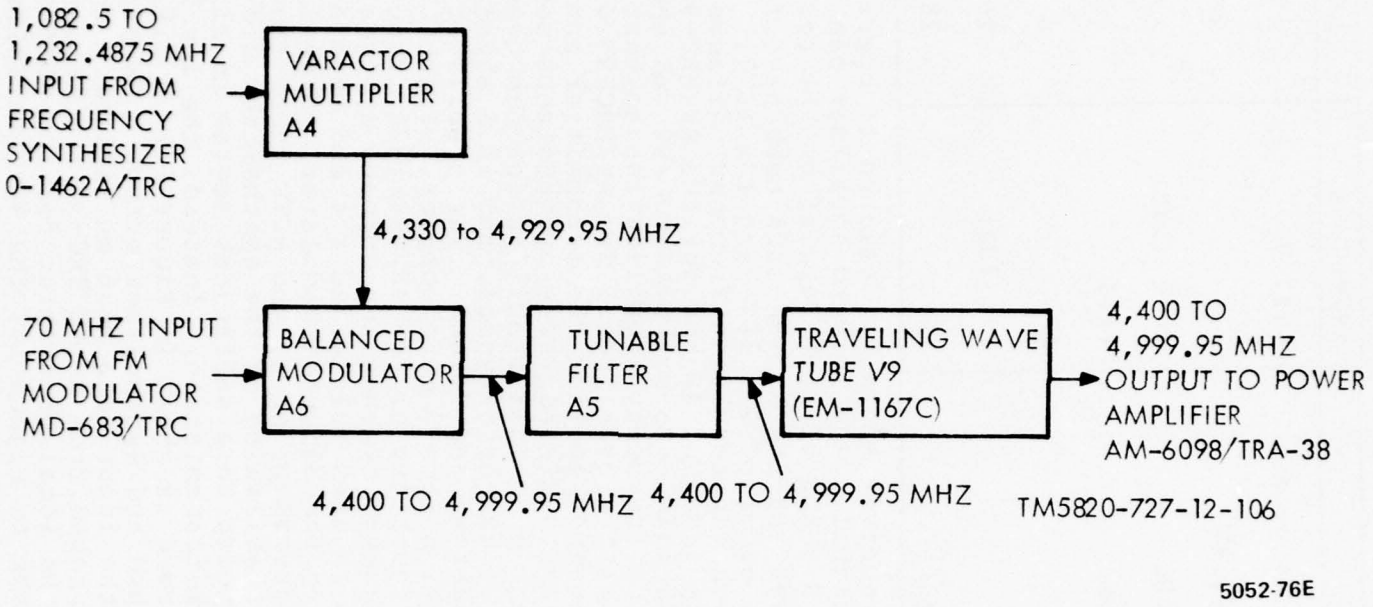


Figure 15. Transmit Converter, Block Diagram, AN/TRC-132A

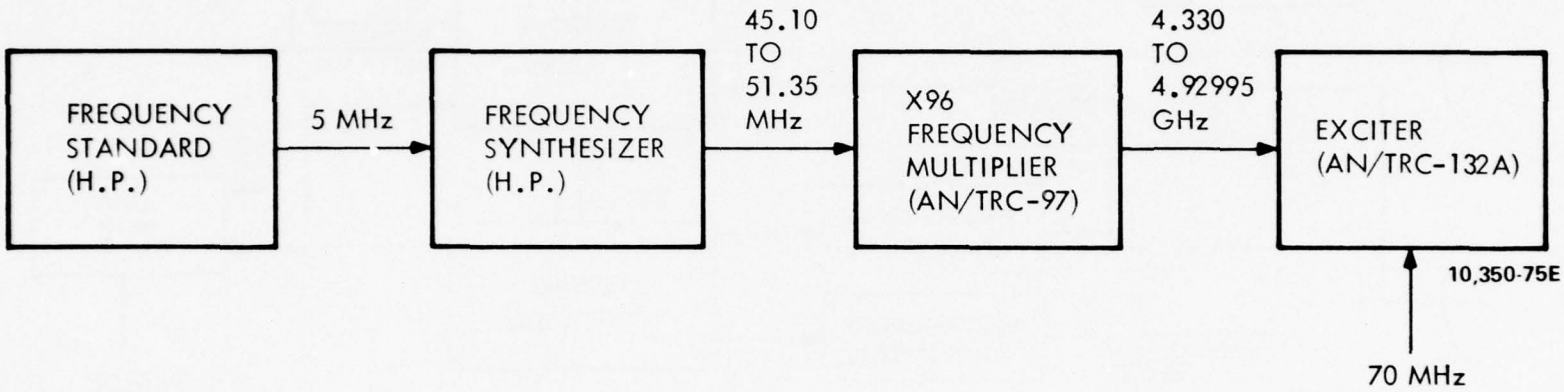


Figure 16. Modified AN/TRC-132A Local - Oscillator Processing Chain Block Diagram

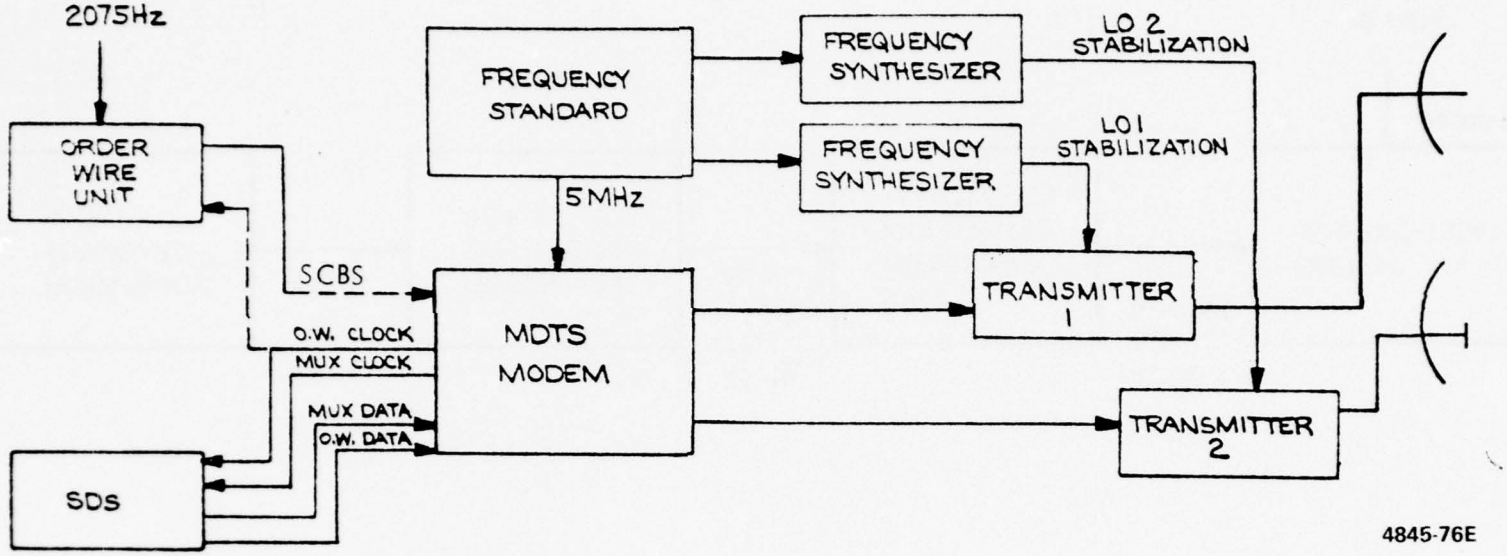


Figure 17. Transmitter Site Instrumentation

AN/TRC-132A was also bypassed in this arrangement. This frequency stabilization was performed at both the transmitter and receiver, and proved to be satisfactory for the MDTS. With this stabilization, the frequency error in the received signal was observed to be in the order of a few Hertz, many orders of magnitude lower than for the unstabilized radios.

The remainder of the terminal equipment was conventional. Tests were run in both quad diversity and dual diversity. In quad diversity, two frequencies were used, transmitted at cross polarizations over two separate antennas. Reception of the two frequencies at two space diversity antennas resulted in quad diversity reception. Dual diversity was achieved by processing only one received frequency using two spaced antennas.

Figure 17 shows a block diagram of the transmitter site instrumentation. All of the blocks have been described except the order-wire unit (OWU) and the source data simulator (SDS). The OWU converts analog speech to 64 Kb/s CVSD, and is connected to the service channel input of the modem. The SDS generates two PN data streams, a 64 Kb/s which can be used in place of the OWU, and a high rate (1.5, 3.1, 6.3, 9.4, 12.6 Mb/s) which is used as the main data stream. All digital outputs of the SDS and OWU are synchronous, being clocked by the modem.

Data Acquisition Facilities

The receiver site instrumentation is shown in Figure 18. Two antennas and two frequencies provided quad diversity reception. The four receivers were frequency stabilized as previously discussed. Each receiver's pre-IF amplifier output was routed to two places, namely the modem and a logarithmic amplifier. The order wire and mux data outputs of the modem were inputs to a SDS, identical to that used at the transmitter. The SDS at the receiver compares its input digital data with internally generated PN sequences, and outputs a pulse for each input which was in error. These were counted on digital counters, thus enabling the bit error rate on both the order wire and the mux data to be simultaneously measured.

The received signal level (RSL) was measured by monitoring the outputs of the four logarithmic amplifiers. In addition, the combined AGC of the four IF amplifiers, and the BITE SNR were monitored. The monitoring was performed in

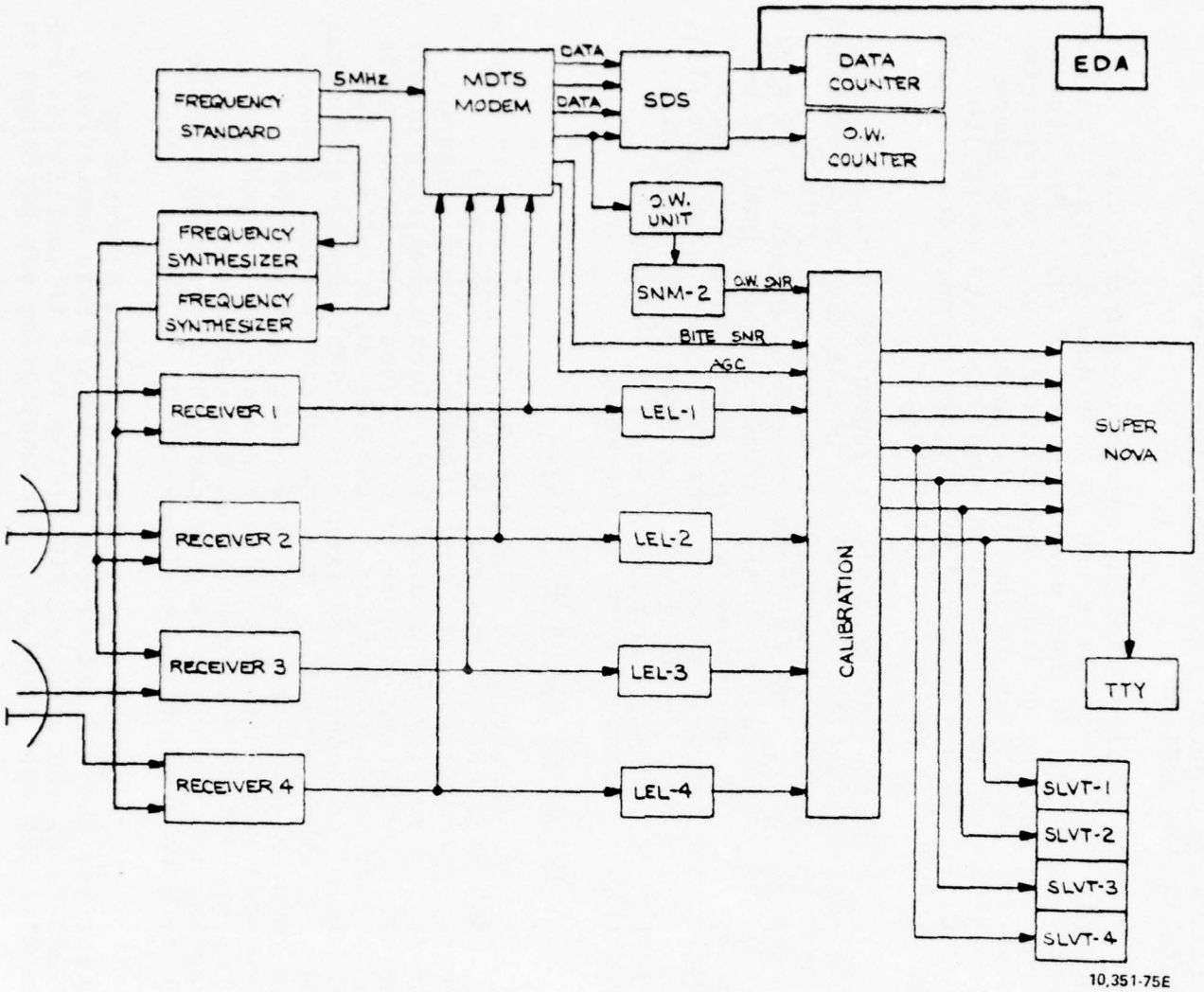


Figure 18. Receiver Site Instrumentation

two ways. The primary means was through 12 bit A/D conversion of the six analog signals and the measurement of their medians on the Super Nova computer. The second means, used as a backup in case of computer failure, was the measurement of the RSL medians on mechanical counters. The mechanical counters are a standard part of the Verona site instrumentation, and are arranged in four groups of seven counters. Each of the four received signal levels is compared, ten times per second, with seven adjustable threshold levels. One threshold is associated with each counter, and if the RSL is above the threshold at the sample time, the counter increments by one. The thresholds are set during system calibration to cover a 30 dB range in 5 dB increments. Thus, at the end of the test, the counters read out a cumulative distribution of signal level during the time interval of the test, from which the median RSL can be evaluated by inspection. The name given the mechanical counting system is the Signal Level Versus Time, or SLVT, system. The data going to either the computer or the SLVT's were calibrated at the beginning of each day over a 40 dB range in 5 dB steps, with the SLVT's being restricted to a usable 30 dB range. The computer interpolated these to 1 dB steps, but the SLVT's remained at 5 dB steps. The data acquisition program used was a slightly modified version of TRODAP, the Troposcatter Data Acquisition Program developed for RADC by SIGNATRON in 1971.

The SDS mux data output was also routed to an Error Distribution Analyzer (EDA). The EDA provides information as to the distribution of errors in time, as opposed to the counter which only gives the total number of errors in the test period.

The RAKE Troposcatter Multipath Analyzer, which is a standard part of the Youngstown and Verona link instrumentation, was used during the test to measure the multipath structure of the channel. The RAKE was interfaced to the Super Nova and the data reduced on-line. Due to instrumentation problems, RAKE data were only available for the latter part of the test series. The RAKE could be used on either or both transmitters as required by the test.

Test Sequence

The field tests were run from January through March 1976. During this three-month period there were 467 tests, each of 20 minutes duration. Table 4 shows the test sequence. The tests started with the AN/TRC-132A running at

12.6 Mb/s. The RSL was too low, so after 20 data runs the rate was switched to 6.3 Mb/s, and 81 tests run. This was followed by 99 tests at 9.4 Mb/s, and then a return to 12.6 Mb/s, at which time 90 tests were run. The modem was then switched to the AN/MRC-98, and 81 runs were made at 3.1 Mb/s followed by 96 runs at 6.3 Mb/s. Thus 6.3 Mb/s was tested on both the AN/MRC-98 and the AN/TRC-132A.

TABLE 4. MDTS TEST SEQUENCE

DATE	DATA RATE	RADIO	TEST NOS.
1/15 - 1/19	12.6	AN/TRC-132A	001 - 020
1/21 - 1/30	6.3	AN/TRC-132A	021 - 101
2/03 - 2/12	9.4	AN/TRC-132A	102 - 200
2/17 - 2/27	12.6	AN/TRC-132A	201 - 290
3/03 - 3/12	3.1	AN/MRC-98	291 - 371
3/17 - 3/26	6.3	AN/MRC-98	372 - 467

Test Results

All tests were of 20 minutes duration. The tests were arranged so that the first half of each hour was at quad diversity, and the second half at dual diversity. The change in diversity was accomplished by disconnecting two IF inputs to the modem terminating them in 50 ohm loads. The RAKE channel prober was used twice daily, at start-up in the morning and at noon time. The tests were run during normal working hours, five days per week, with routine maintenance being scheduled for Monday morning and site calibration performed the first hour of each day.

The live link tests at the RADC troposcatter test facility were designed to determine the MDTS modem performance characteristics, the channel conditions, and the characteristics of the monitoring functions in the modem. The modem performance characteristics were measured by the average bit error rate (ABER) over 20 minute periods as a function of median received power level. In addition, the capability of the modem to hold bit synchronization was assessed in the face of excessive multipath conditions and aircraft reflected signal conditions. The channel was characterized by 20 minute measurements (simultaneous with the ABER measurement) of the received signal level distribution and the channel fade rate. Twice a day a measurement of the multipath profile for each of the two received frequencies was also performed. The multipath profile is defined as the average power response vs. delay for impulse excitation of the channel. It is also termed the delay power spectrum or power impulse response. The monitor functions in the MDTS Modem include an SNR monitor

as part of the Built-In-Test-Equipment (BITE), a median signal level measure derived from the AGC function of the IF amplifiers, and a BER indicator.

The measurement of the multipath profile was accomplished with the GTE Sylvania RAKE processor which uses a 10 Mb/s PN sequence for the probe and a 0.1 microsecond cell display of the profile. The RAKE processor measures the tandem combination of the transmitter, transmission medium, and receiver. For operation on both the TRC-132 and MRC-98, the transmitter characteristics significantly increase the measured multipath spread from that of the medium alone. The transmitter frequency responses are shown in Figures 19 and 20 for the two radio systems. The shape of the multipath profiles did not vary greatly over the course of the tests. The major shape variation observed was the presence of a second hump for large multipath conditions measured on the MRC-98. Typical profiles for the two radio types are shown in Figure 21.

Unfortunately, due to equipment difficulties, RAKE data was available only during the 12.6 Mb/s testing on the TRC-132A and the 3.1 and 6.3 Mb/s testing on the MRC-98. Twice the standard deviation (2σ) of the multipath profile varied from 0.09 to 0.22 microseconds during the 132A tests. On the MRC-98 the 2σ values ranged from 0.17 to 0.54 microseconds. The geometric means of 2σ during each of the data rate tests are summarized in Table 5.

TABLE 5. MEASURED MULTIPATH SPREAD

	Data Rate Mb/s	Geometric Mean 2σ	$2\sigma/T$*
TRC-132A	12.6	0.14 μ sec	0.9
MRC-98	6.3	0.23	0.7
MRC-98	6.3	0.32	1.0
MRC-98	3.1	0.29	0.45

Two entries are shown for the 6.3 Mb/s tests in order to segregate approximately one day of testing where a clear increase in multipath spread was observed.

*NOTE: T = baud length for given data rate.

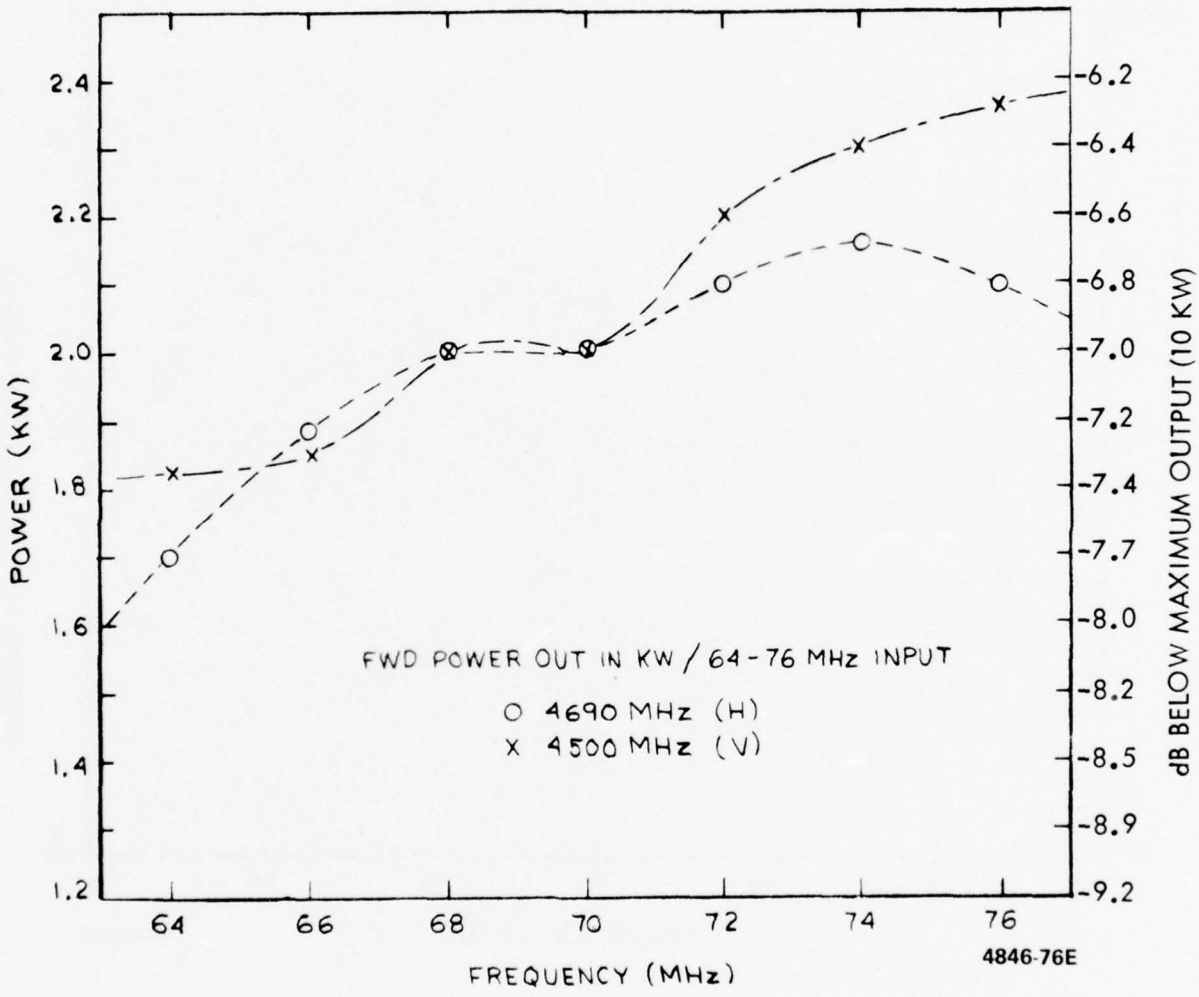


Figure 19. AN/TRC-132A Transmitter Frequency Response

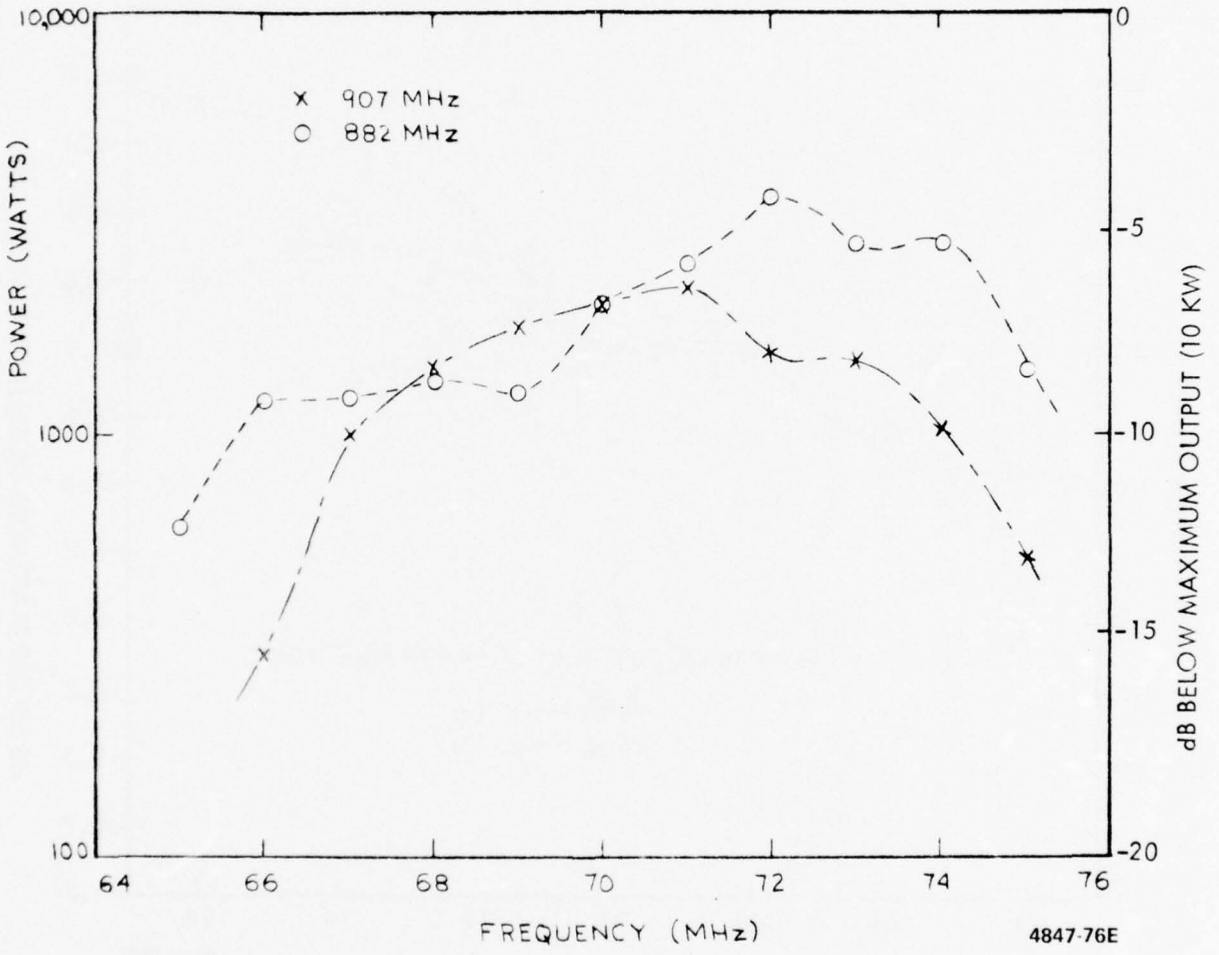


Figure 20. AN/MRC-98 Transmitter Frequency Response

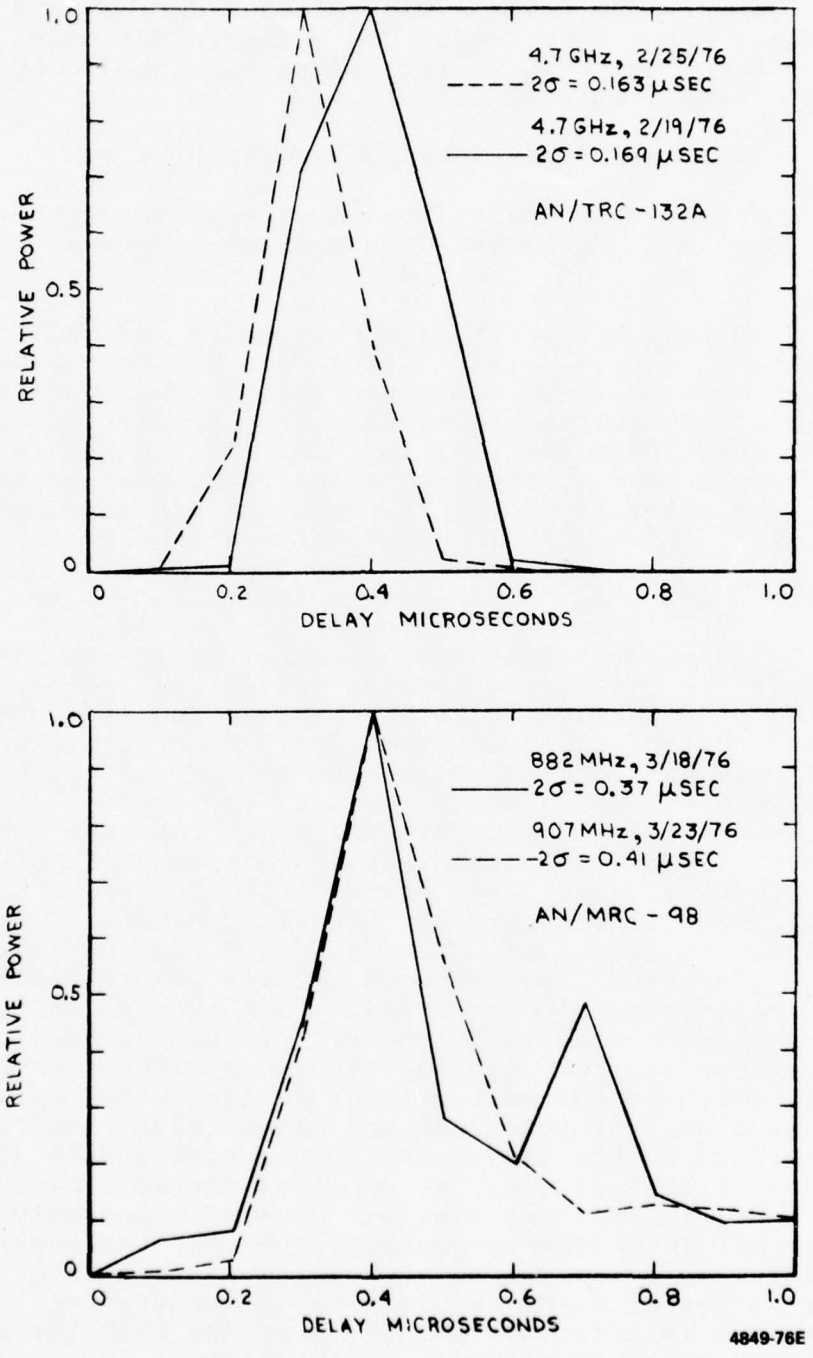


Figure 21. Measured Multipath Profiles

The fade rate as measured by median crossings (one direction only) per minute was recorded during each 20 minute bit error rate test. The standard deviation of the Doppler spectrum, B_{rms} is related to the one directional median crossing rate by (9)

(B_{rms} = Median Crossing Rate/44.3 Hz.)

The measured distribution of B_{rms} for both the L band MRC-98 and C-band TRC-132A system are given in Figure 22.

Average bit error rate testing on the TRC-132A was performed at 6.3, 9.4, and 12.6 Mb/s. The test results are shown in Figures 23 to 25 respectively. The abscissa is defined as the average received energy per bit $\bar{E}_b$ divided by the received noise power N_o in 1 Hz. This quantity is also equal to the average received power P_R divided by the noise power in a bit-rate bandwidth. Thus the median received power P_m in dBm and 10 log $\bar{E}_b/N_o$ are related by

$$10 \log \bar{E}_b/N_o = P_m + 1.6 - (N_F + 10 \log R_B - 174)$$

where N_F is the receiver noise figure, R_B is the bit rate, 1.6 dB is the difference between median and average power for a complex Gaussian scatter channel, and -174 dBm is the receiver noise in 1 Hz of bandwidth. Each sample point on the figures represents a 20 minute average of the bit error probability or equivalently the bit error rate. The test points exhibited the same type of scatter as seen in the simulator tests for a fixed multipath spread. Thus the modem was relatively insensitive to the multipath spread variations which occurred over the test period. This insensitivity is due to more implicit diversity gain but larger intersymbol interference penalty under conditions of an increase in multipath spread. Note that under these large multipath conditions where 2 is nearly equal to the symbol interval, time gating techniques without equalization cannot eliminate the multipath distortion effects. The implicit diversity gain realized under these conditions can be estimated by the amount the curves move toward (or cross) the ideal flat fading curves shown as dotted lines. At small $\bar{E}_b/N_o$ there is no implicit diversity and only small intersymbol interference penalty, and thus the separation from ideal is a measure of the implementation margin. At larger values of $\bar{E}_b/N_o$ the implicit diversity and intersymbol interference penalty increase with the net gain reflected as the dB movement to the left.

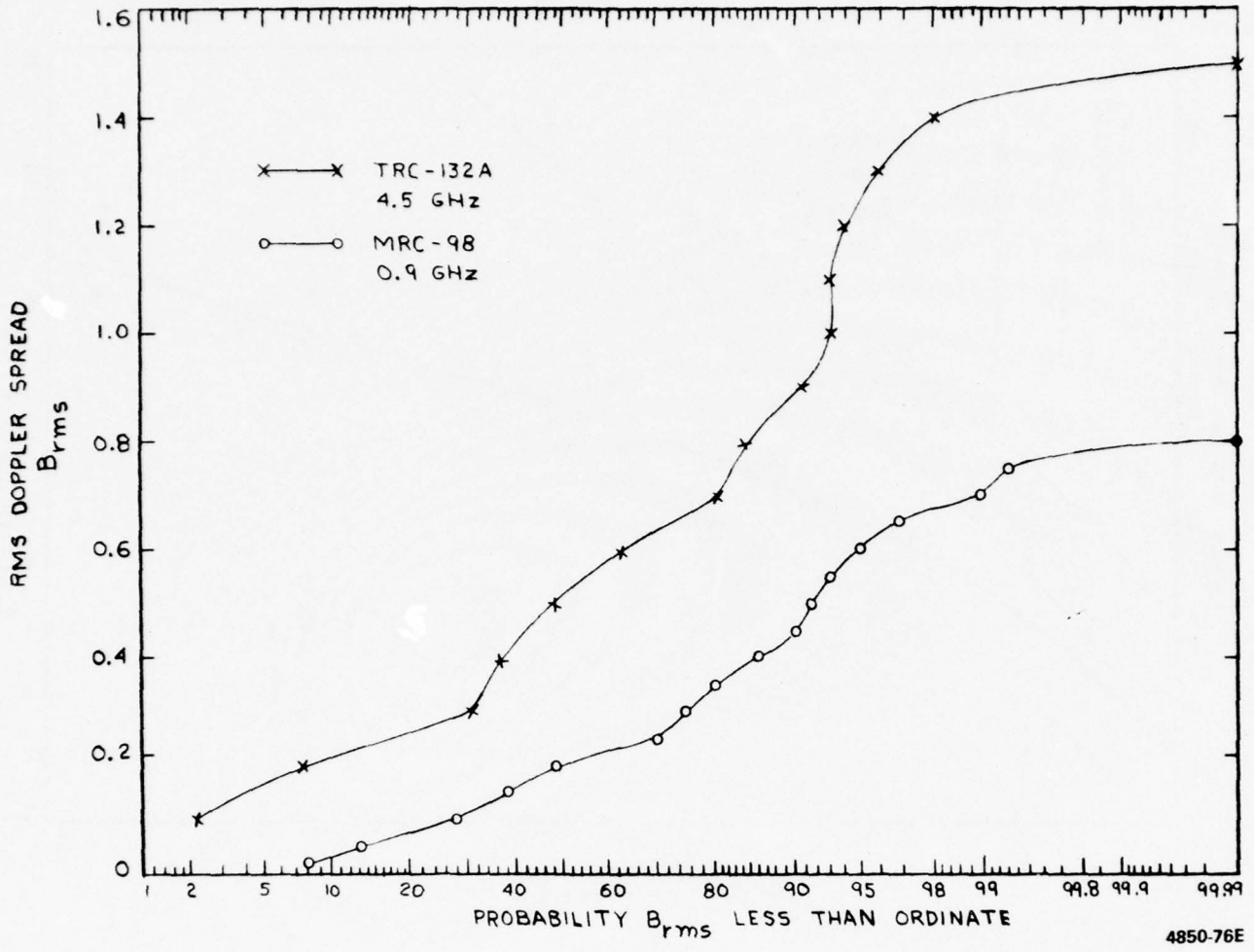


Figure 22. RMS Doppler Spread Distribution, MRC-98

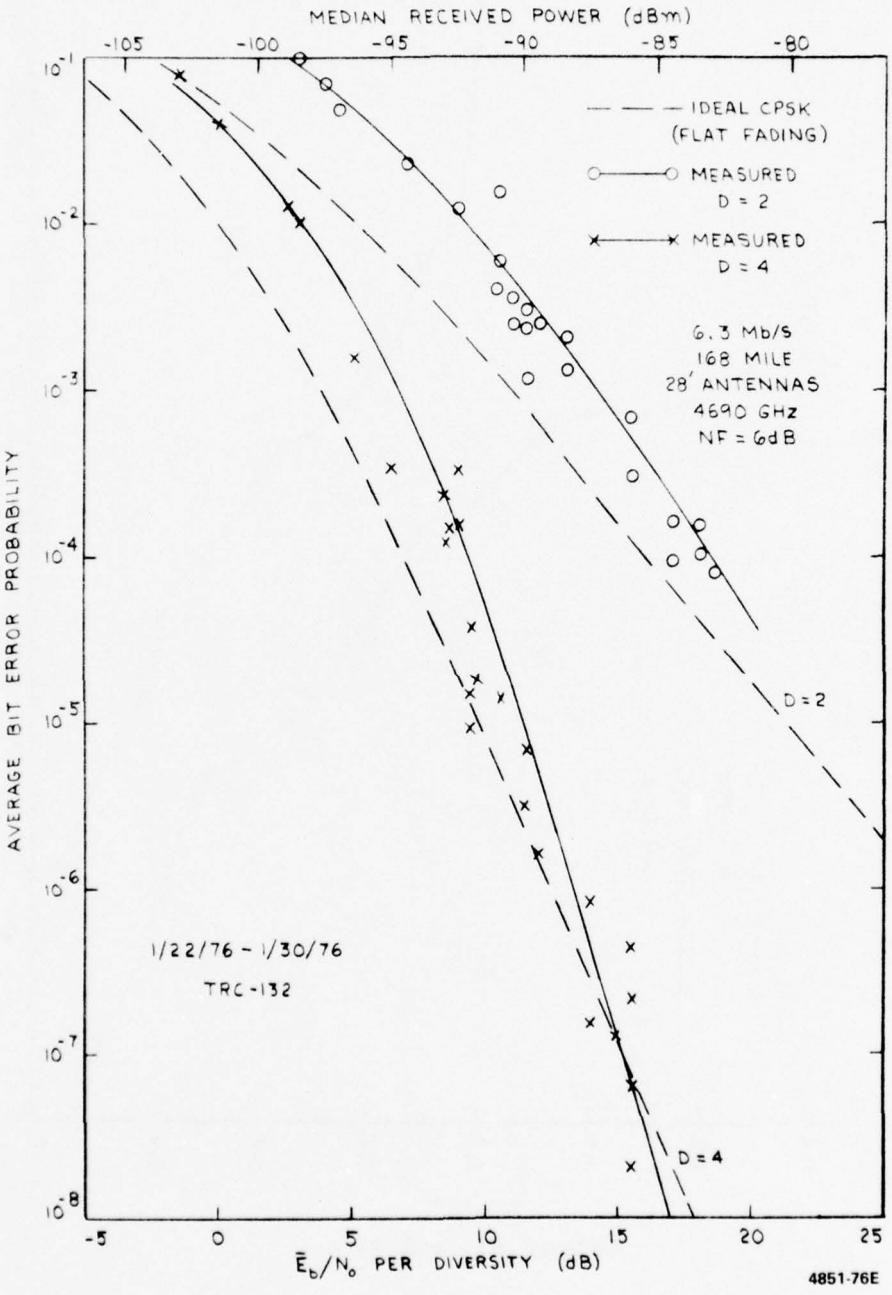


Figure 23. 6.3 Mb/s Test, TRC-132A

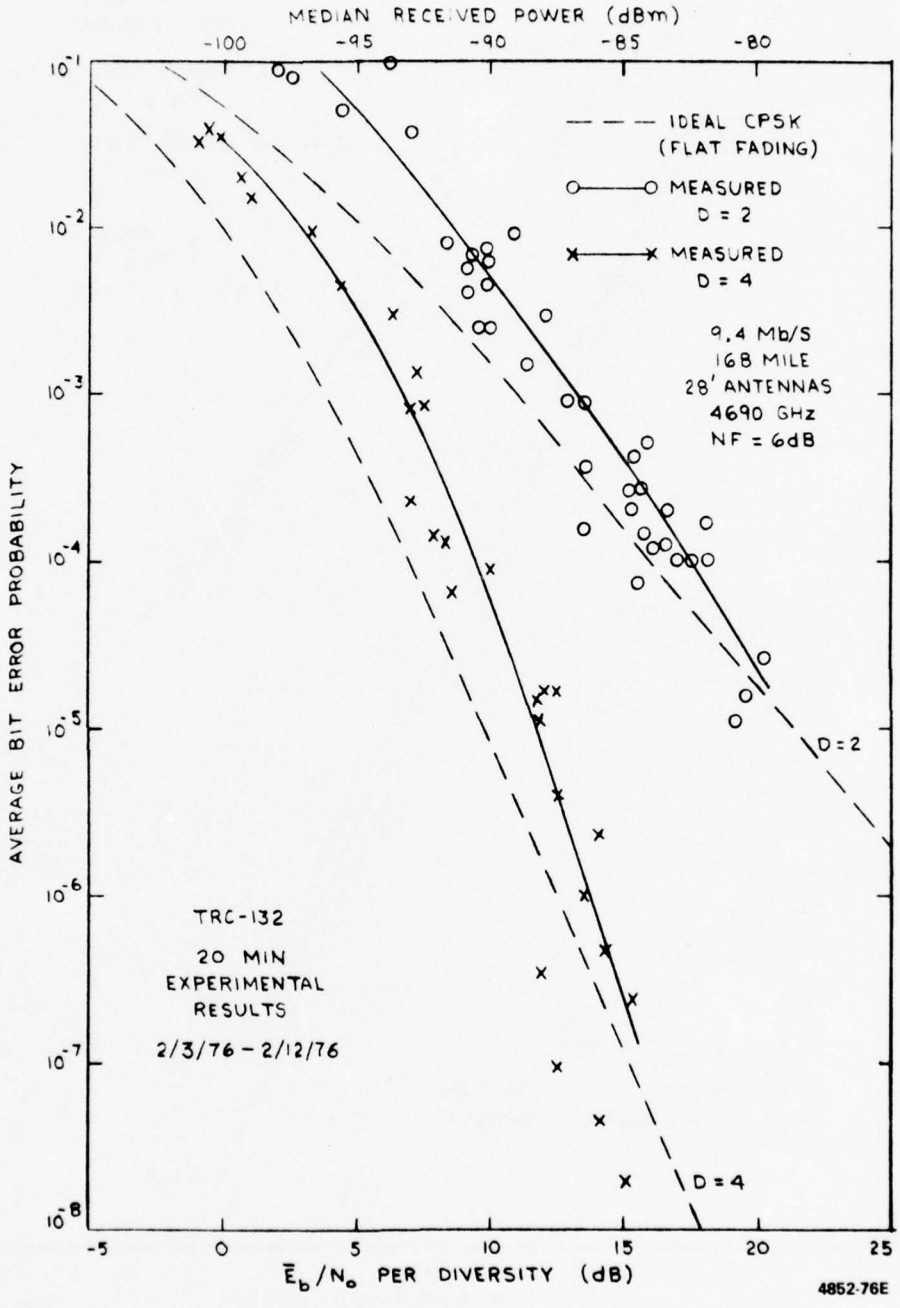


Figure 24. 9.4 Mb/s Test, TRC-132A

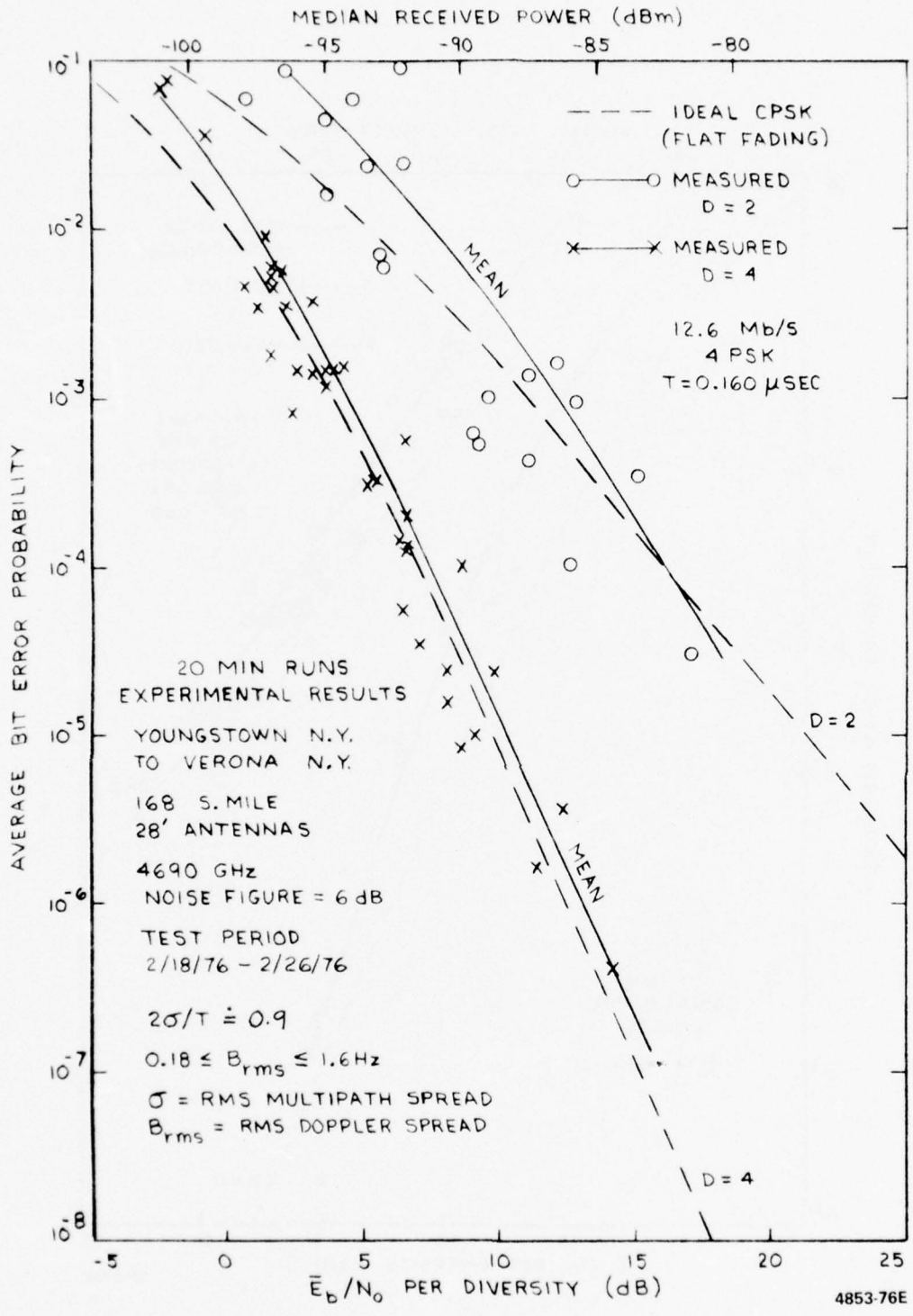


Figure 25. 12.6 Mb/s Test, TRC-132A

The results from the MRC-98 tests were similar to that obtained on the TRC-132A. The MRC-98 tests were performed at approximately 900 MHz which produced both slower fading and increased multipath spread. The results are shown in Figures 26 and 27. Some extreme multipath conditions were observed at 6.3 Mb/s over approximately one day where the rms multipath spread (26) approximately equalled the 4 PSK symbol length. For this amount of multipath, the intersymbol interference penalty is significant as evidenced by the degraded performance shown in Figure 27.

A summary of the link performance tests is shown in Figure 28. Note that the 12 and 9 Mb/s curves for quad diversity on the TRC-132A are reversed from their theoretical relationship. Also, the curves are not separated by exactly the theoretical dB difference associated with the data rate ratios. These factors are an indication of the effects of varying multipath conditions and calibration accuracy which is probably on the order of $\pm$ 1 dB. We next turn our attention to a comparison of these measured results with theoretical performance calculations.

In Section 2 a mathematical model for the calculation of modem performance was developed. The model computes the average bit error rate on a fading channel by considering transmission of a desired bit and two bits of future intersymbol interference. With this model, as the multipath spread increases, performance initially improves due to additional implicit diversity but for sufficiently large multipath spread, the intersymbol interference penalty dominates and performance falls off again. The intersymbol interference penalty becomes significant as the multipath spread exceeds the width of the forward filter in the decision feedback equalizer. The model of course requires knowledge of the channel rms multipath spread, 2σ. RAKE data was available for the link tests at 12.6 Mb/s on the TRC-132A and at 3.1 and 6.3 Mb/s on the MRC-98. The RAKE measurements include the filtering effect of the transmitter power amplifier which produces a non-fading intersymbol interference effect. The model can incorporate the effects of a transmitter filter but the filter impulse response must be known. With only the amplitude response of the transmitter filter transfer function available, the model was used with the measured values of rms multipath spread. As can be seen from Figures 29 through 31, the effect of this approximation is minimal as the measured and calculated results compare very well.

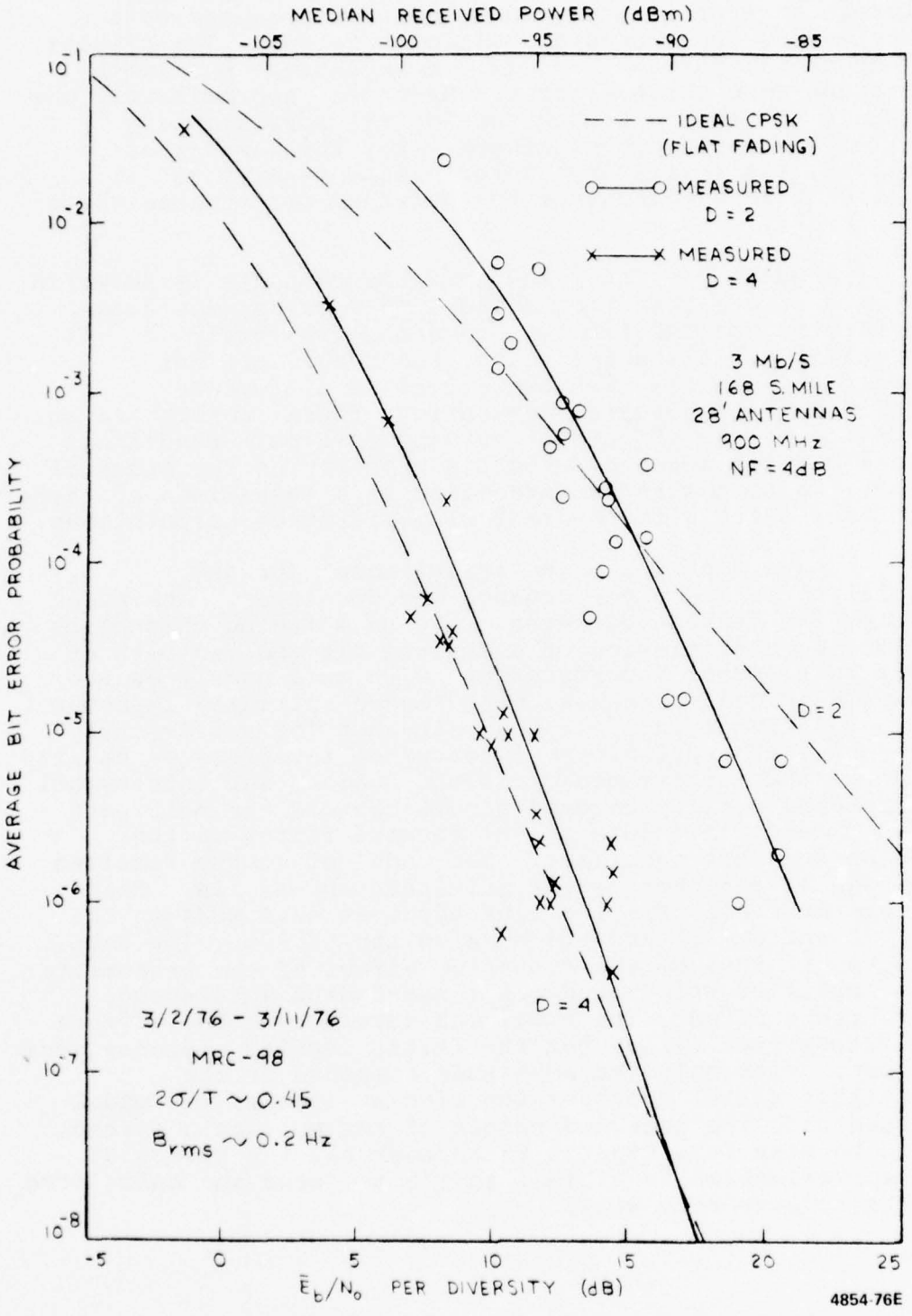


Figure 26. 3.1 Mb/s Test, MRC-98

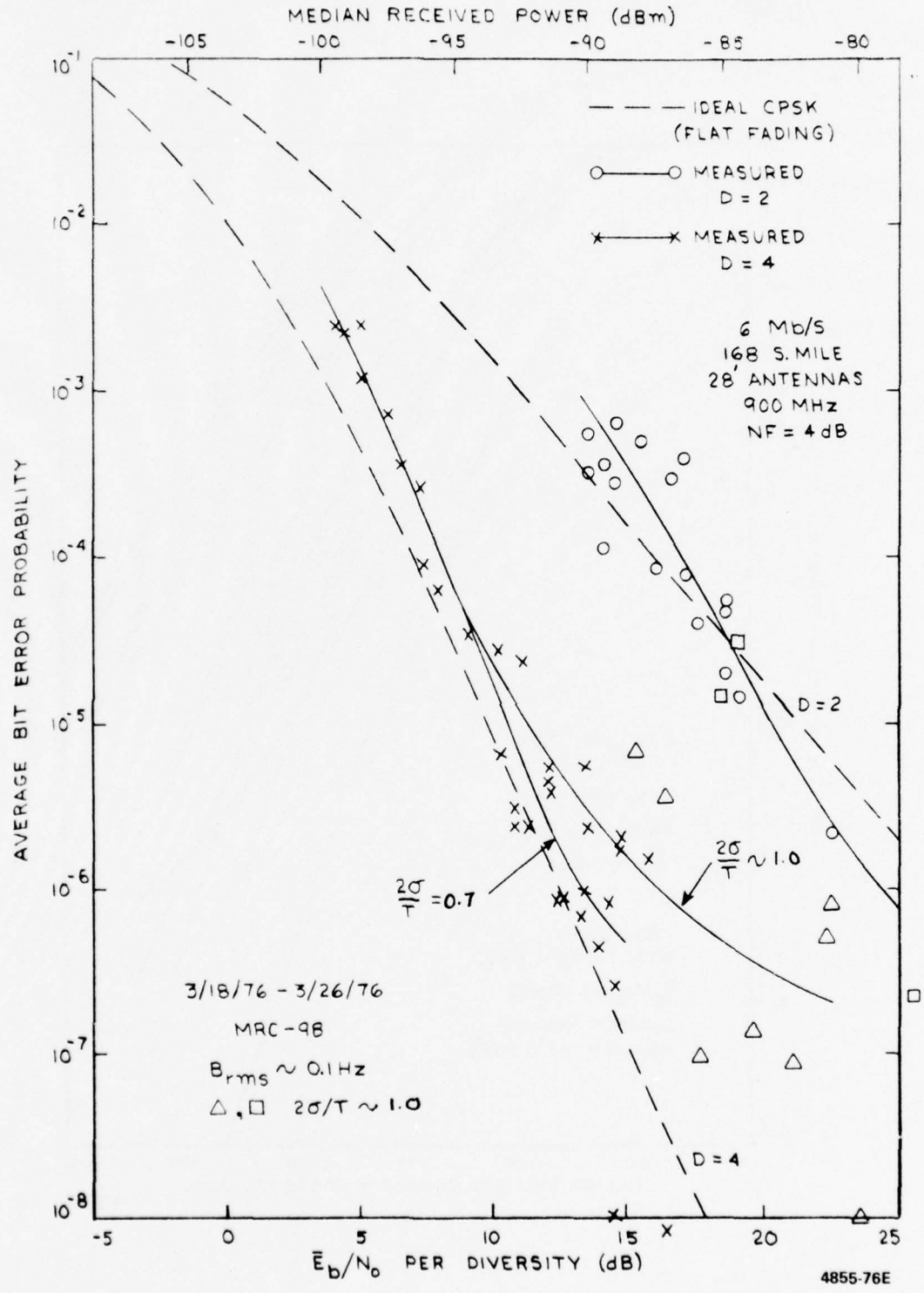


Figure 27. 6.3 Mb/s Test, MRC-98

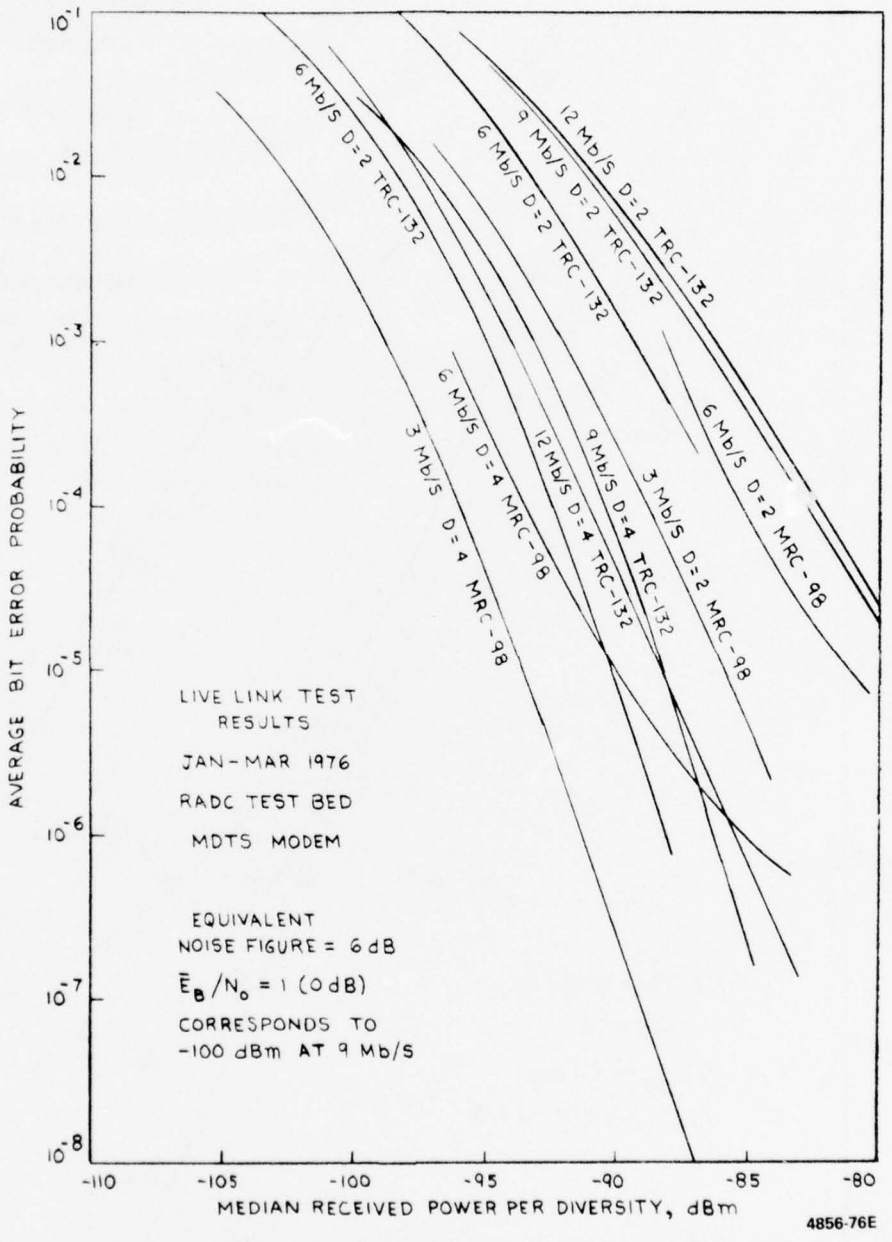


Figure 28. Link Test Summary

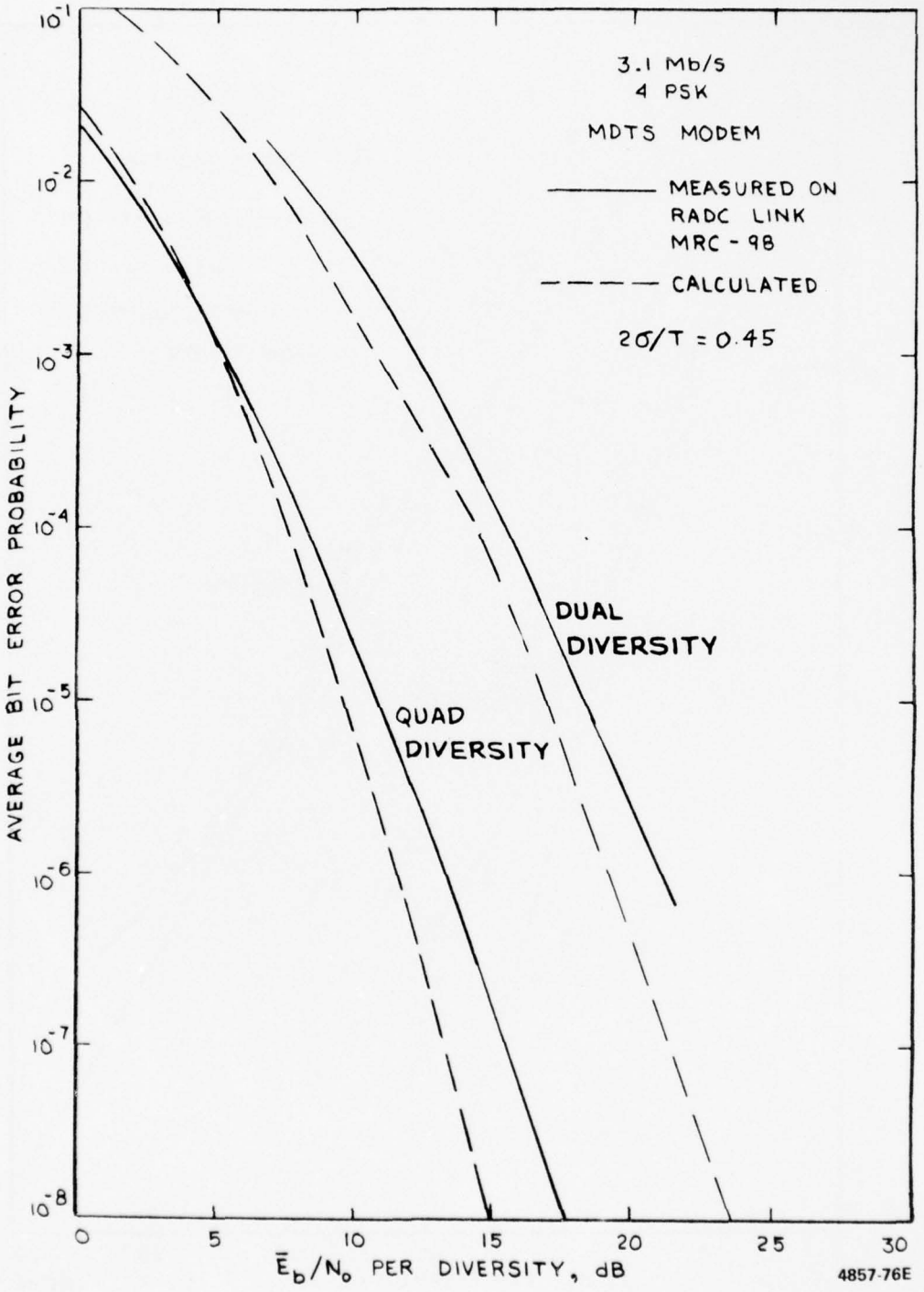


Figure 29. Comparison of Measured and Calculated Performance, 3.1 Mb/s

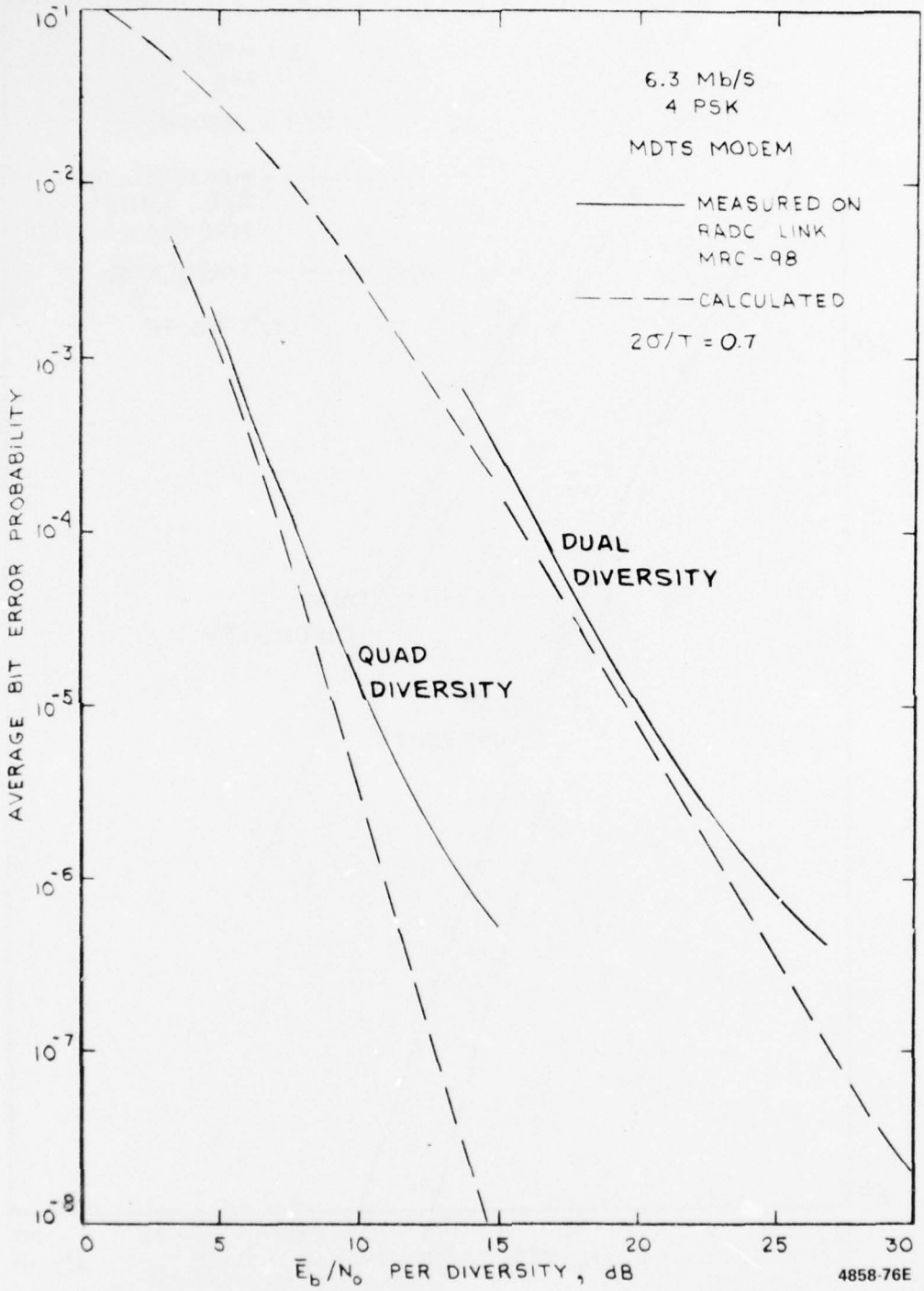


Figure 30. Comparison of Measured and Calculated Performance 6.3 Mb/s

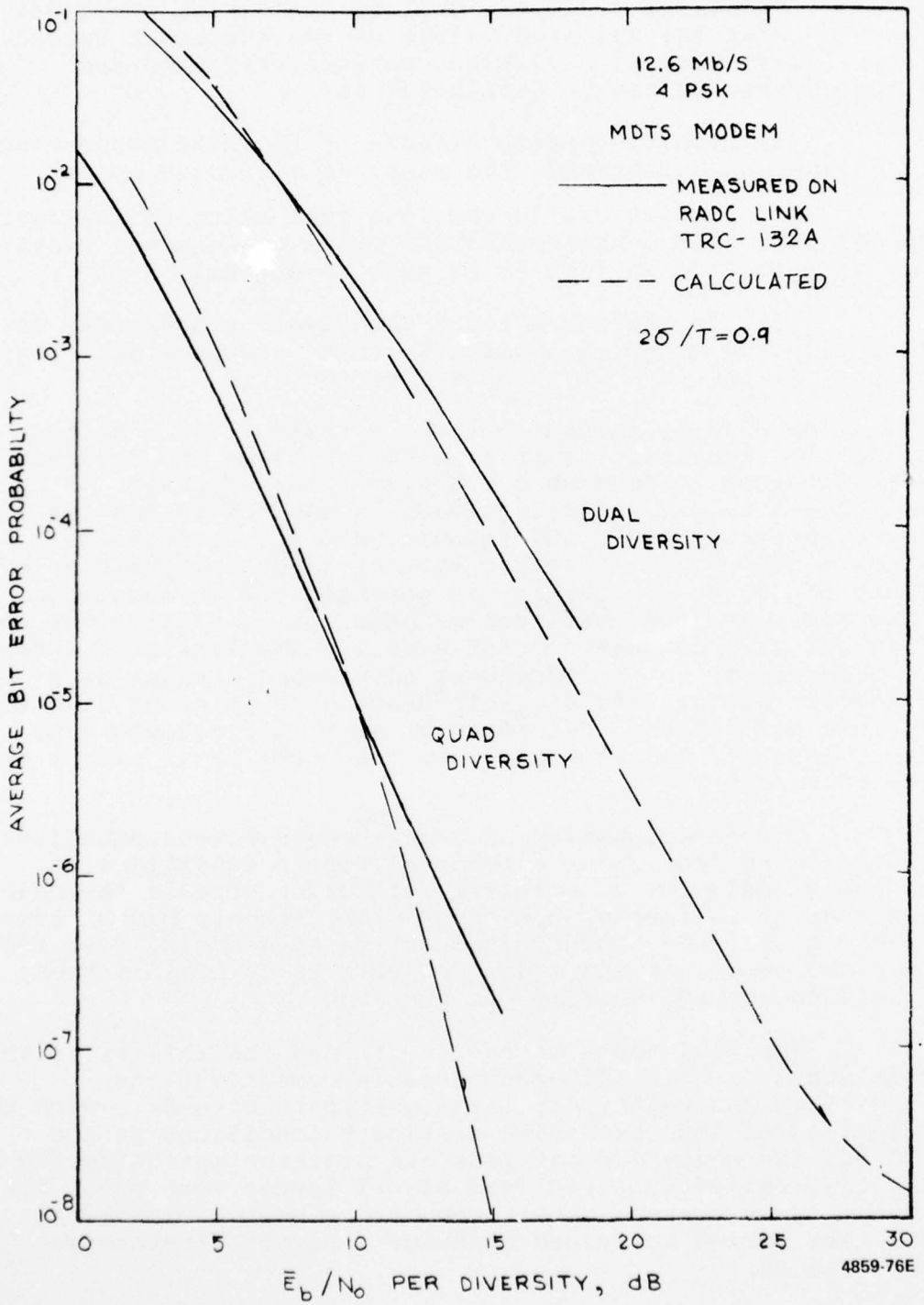


Figure 31. Comparison of Measured and Calculated Performance 12.6 Mb/s

transmitter filter transfer function available, the model was used with the measured values of rms multipath spread. The relatively small deviations between predicted and measured results can be attributed to

(1) additive noise effects in the RAKE measurement technique which increases the measured multipath spread.

(2) variations in the long term value of multipath spread (the RAKE measurements and modem performance tests may be separated in time by as much as one-half a day)

(3) In the 6Mb/s tests the Klystron bandwidth is less than the signal bandwidth which may produce an additional intersymbol interference penalty.

The MDTS modem does not use a transmitter reference signal for equalizer adaptation but utilizes the receiver 4 PSK decisions to form an error signal for adaption. A decision-directed equalizer modem is subject to loss of bit count integrity (BCI) under fading channel conditions. After a deep fade in the presence of large multipath delays where the error probability is one-half for an equalizer time constant, the equalizer weights may re-adapt after the fade and skip or gain a 4 PSK symbol. The loss of BCI due to this effect is an infrequent occurrence because deep fades of this natures are infrequent on high order diversity systems and because the amount of multipath necessary to cause loss of BCI after the deep fade must be in excess of the equalizer width.

The re-adaptation of a decision-directed equalizer after a deep fade under extreme multipath conditions or excessive delay of an aircraft reflection echo is the major contributor to loss of BCI. Loss of BCI due to symbol timing tracking or frame synchronization tracking during deep fades does not occur, as the modem is designed to disable these functions for the duration of the fade.

The link tests at RADC confirmed the ability of the MDTS modem to hold BCI under useable communications conditions and relatively large multipath spreads. With the exception of some excessive multipath conditions on the MRC-98, the modem did not lose bit synchronization during the test period when received signal levels were good, i.e., typically an average error probability better than 10^{-2}. The test period contained numerous aircraft fly-through occurrences.

At 12.6 Mb/s on the TRC-132A, the test period included many subperiods of very weak signal conditions. Loss of BCI occurred during dual diversity tests under conditions where the Average Bit Error Rate (ABER) was always larger than 10^{-2}. One event could be correlated with the presence of aircraft reflections. Loss of BCI occurred during 6 quad diversity tests also when conditions would produce an ABER poorer than 10^{-2}. One of these 6 events also showed aircraft reflection signals on the strip chart near the loss of BCI occurrence. There were a total of 110 tests run at 12.6 Mb/s. All tests are of 20 minute duration and the runs are approximately divided equally between dual and quad diversity.

There were two losses of BCI events in a dual diversity configuration at 9.4 Mb/s TRC-132A again when conditions produced an ABER poorer than 10^{-2}. The modem did not lose BCI in a quad diversity configuration at 9.4 Mb/s. A total of 99 tests were run at 9.4 Mb/s.

At 6.3 Mb/s on the TRC-132A there were four loss of BCI events at dual diversity and two at quad diversity. The events all occured when the ABER was worse than 10^{-2} and were not as a result of aircraft echo. There were 81 tests at 6.3 Mb/s on the TRC-132A

The total test period on the TRC-132A contained 56 identifiable aircraft interference echoes, many of them occurring in the presence of weak scatter conditions. Two of the identified aircraft occurences result in loss of BCI.

At 3.1 Mb/s on the MRC-98 there were five loss of BCI events at dual diversity under conditions of ABER worse than 10^{-2}. In the quad diversity configuration there were two loss of BCI events under conditions of an ABER of approximately 10^{-3} and significant aircraft reflection activity during each test. There were 81 tests at 3 Mb/s.

A combination of transmitter filter selectivity and large multipath conditions ($2\sigma/T > 1.$) during the MRC-98 tests at 6.3 Mb/s produced more loss of BCI events with some occurring under strong signal conditions. The loss of BCI under these conditions is due to instantaneous multipath conditions which exceed the equalizer's capability and cause the decision-directed mechanism to break down. There were 12 loss of BCI events for the dual diversity tests and 11 events for the quad diversity tests. Of these events 4 showed evidence of the presence of aircraft reflection

signals. There were 96 tests at 6.3 Mb/s on the MRC-98. For the MRC-98 tests at both 3.1 and 6.3 Mb/s there were a total of 51 identifiable aircraft interference echoes.

An Error Distribution Analyzer (EDA) was used at the 9.4 and 12.6 Mb/s rates to measure the distribution of the bit error rate as a function of average bit error rate. The measured distributions for the two data rates at both dual and quad diversity are given in Figures 32 through 35. Considerable variation between distributions at the same ABER can be expected as the variation in multipath spread can significantly alter the available implicit diversity and hence the distribution.

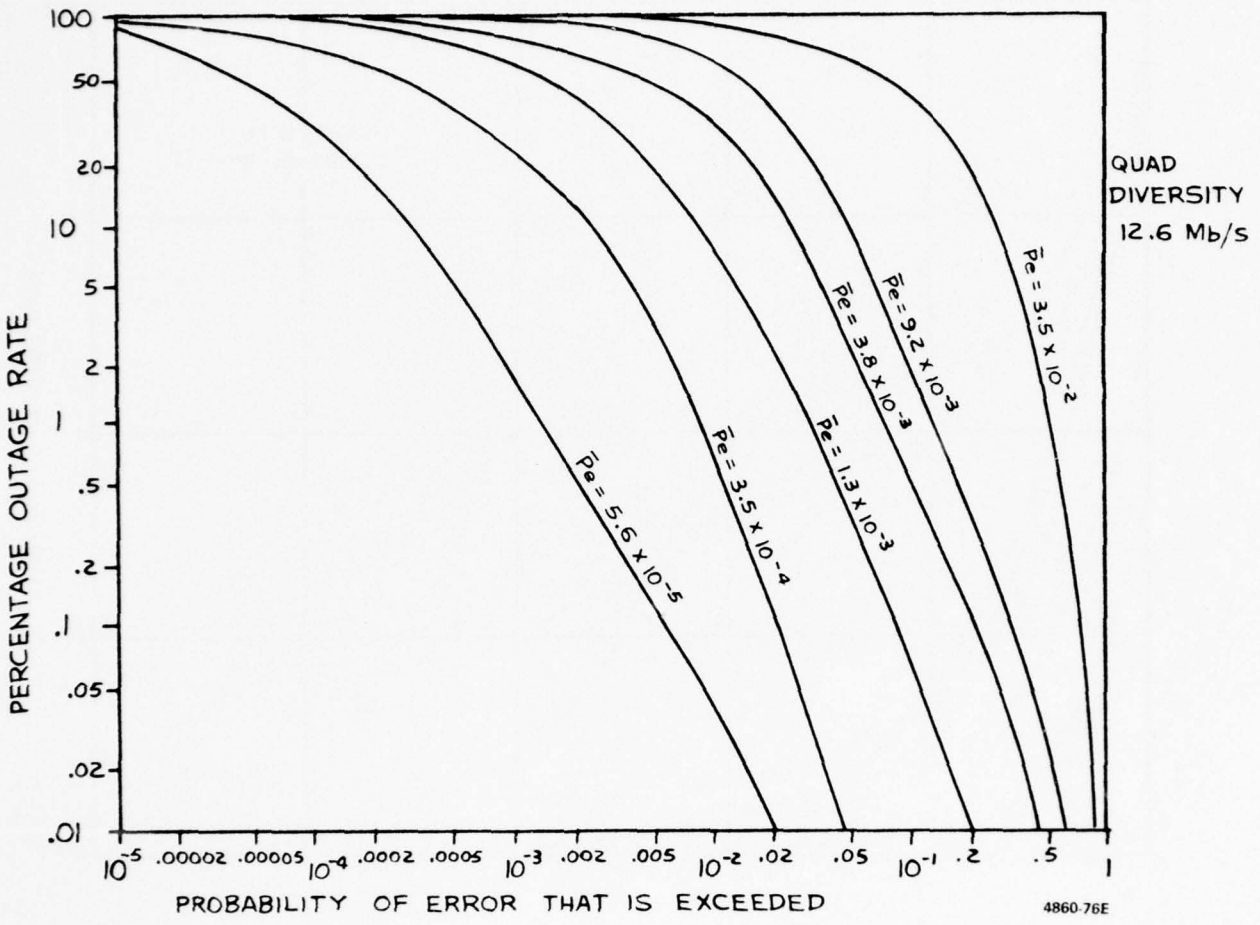


Figure 32. Bit Error Rate Distribution

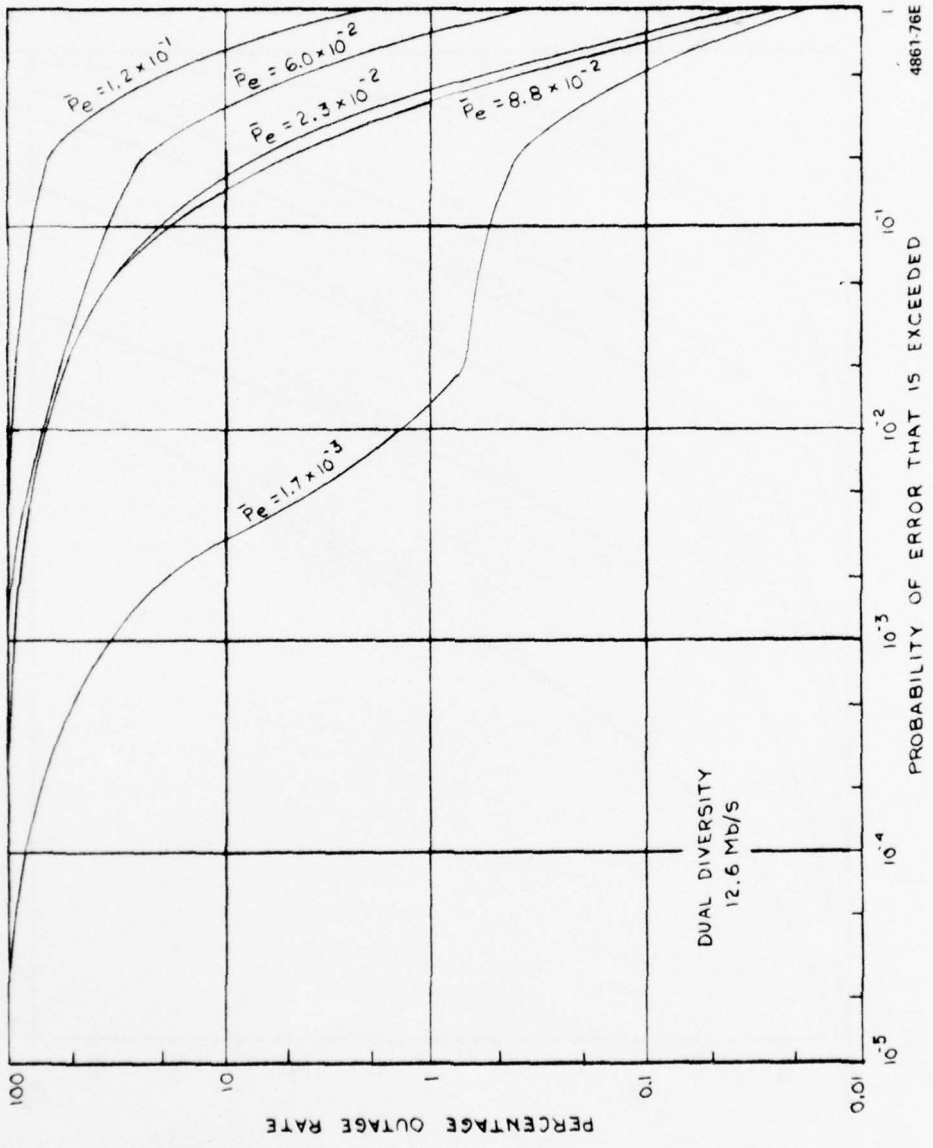


Figure 33. Bit Error Rate Distribution

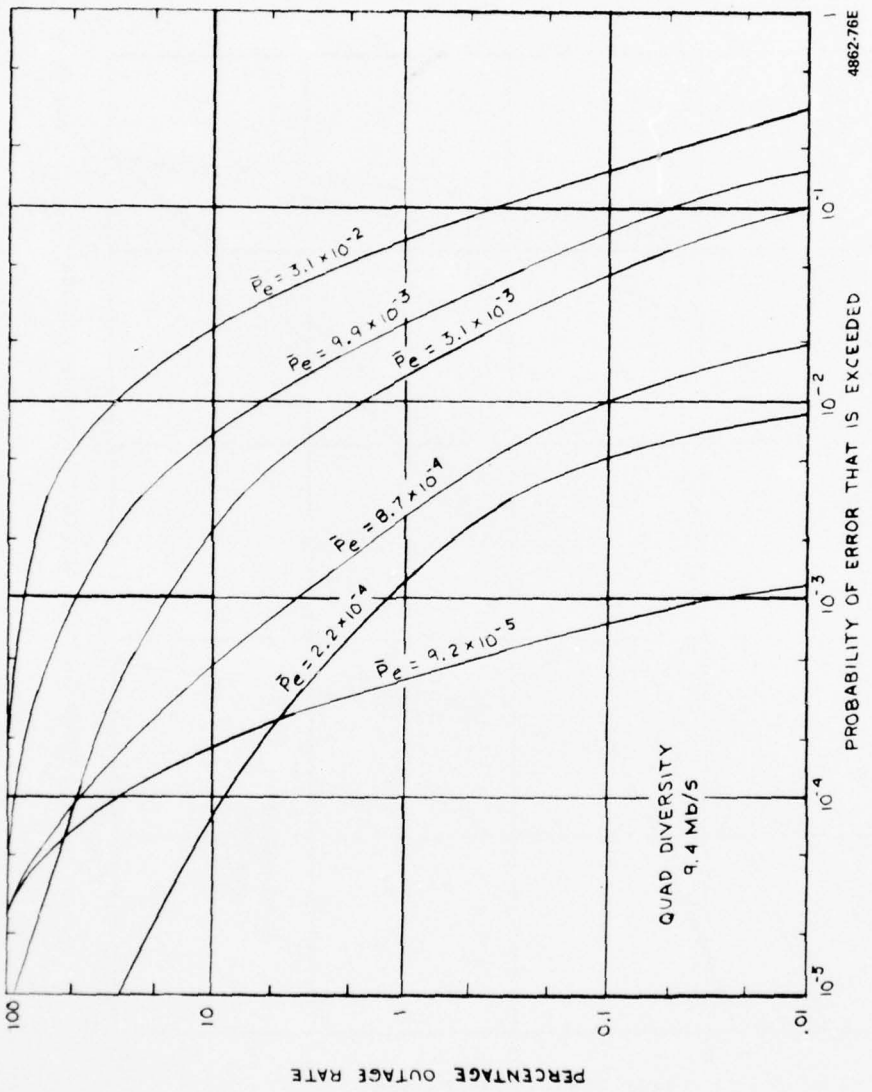


Figure 34. Bit Error Rate Distribution

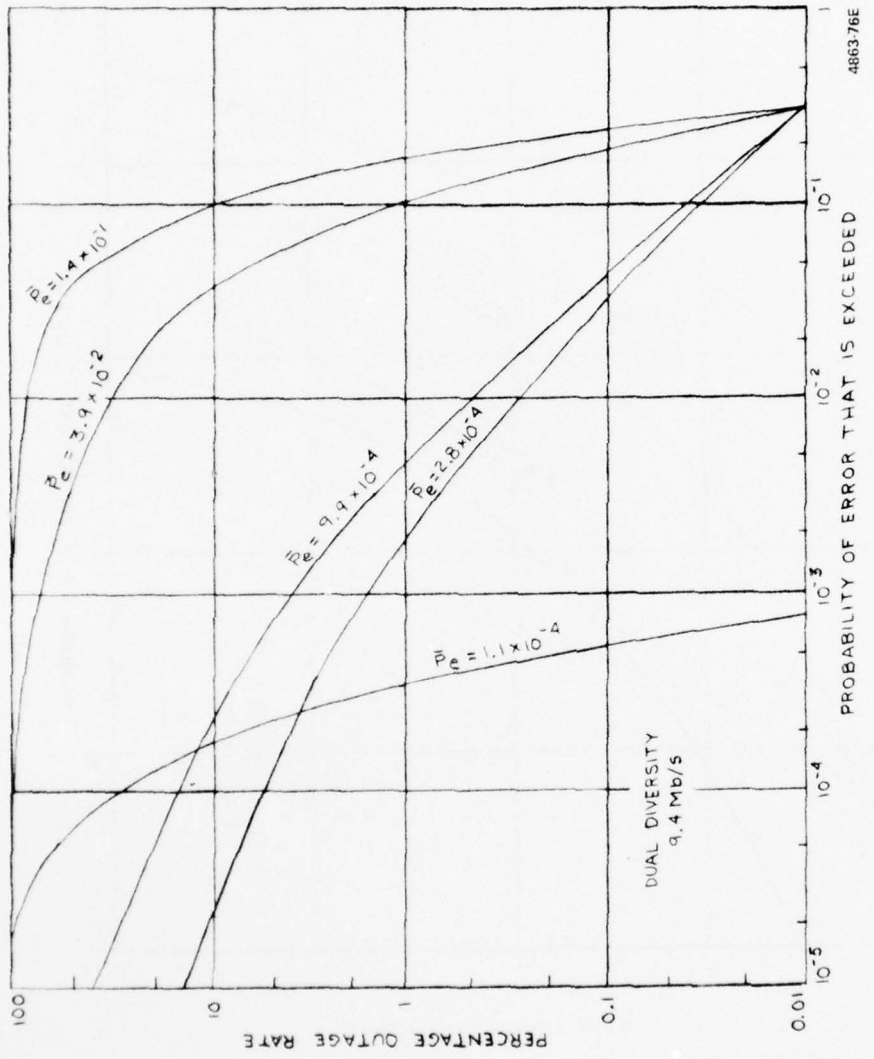


Figure 35. Bit Error Rate Distribution

During the test period the monitor functions of the MDTS Modem were connected to the computer for recording and subsequent evaluation. The MDTS modem has a BITE SNR measure and a measure of the largest received signal strength. The BITE SNR is formed from the adaptation error signal and is a measure of the signal strength relative to combined noise and intersymbol interference powers. In the absence of intersymbol interference the BITE SNR is approximately 10 log $\bar{E}_b/N_o$. The median value of BITE SNR is plotted versus the average (in dB) of the diversity received signal medians in Figures 36 and 37 for dual and quad diversity, respectively. The significant departure from linearity is an indication of the multipath conditions which are not reflected in the median received signal. Thus the BITE SNR is most useful as an overall measure of modem performance and not received signal level.

The median of the largest diversity signal as measured by the IF amplifier AGC voltages is plotted in Figures 38 and 39 for dual and quad diversity, respectively. If X represents the received strength in watts for a single diversity branch, the distribution of x for the complex Gaussian scattering channel is

$$F(x) = pr\ (Y \leq x) = 1 - e^{-0.693x/x_m}$$

where x_m is the median received signal strength. For a Dth order diversity system, the distribution of the maximum received signal strength y is

$$G(y) = [F(y)]^D,$$
$$y = \max\ (x_1, x_2, \ldots x_D)$$

The median of the maximum received signal strength solves

$$(1 - e^{-0.693\ y_m/x_m})^D = 0.5$$

For D = 2 and D = 4 one finds y_m larger than x_m by 2.5 and 4.2 dB, respectively. Figures 38 and 39 show that the AGC median measured by the MDTS modem is a good measure of the statistic y_m.

The MDTS modem has a BER indicator which displays a 5 minute average of the bit error probability. This average

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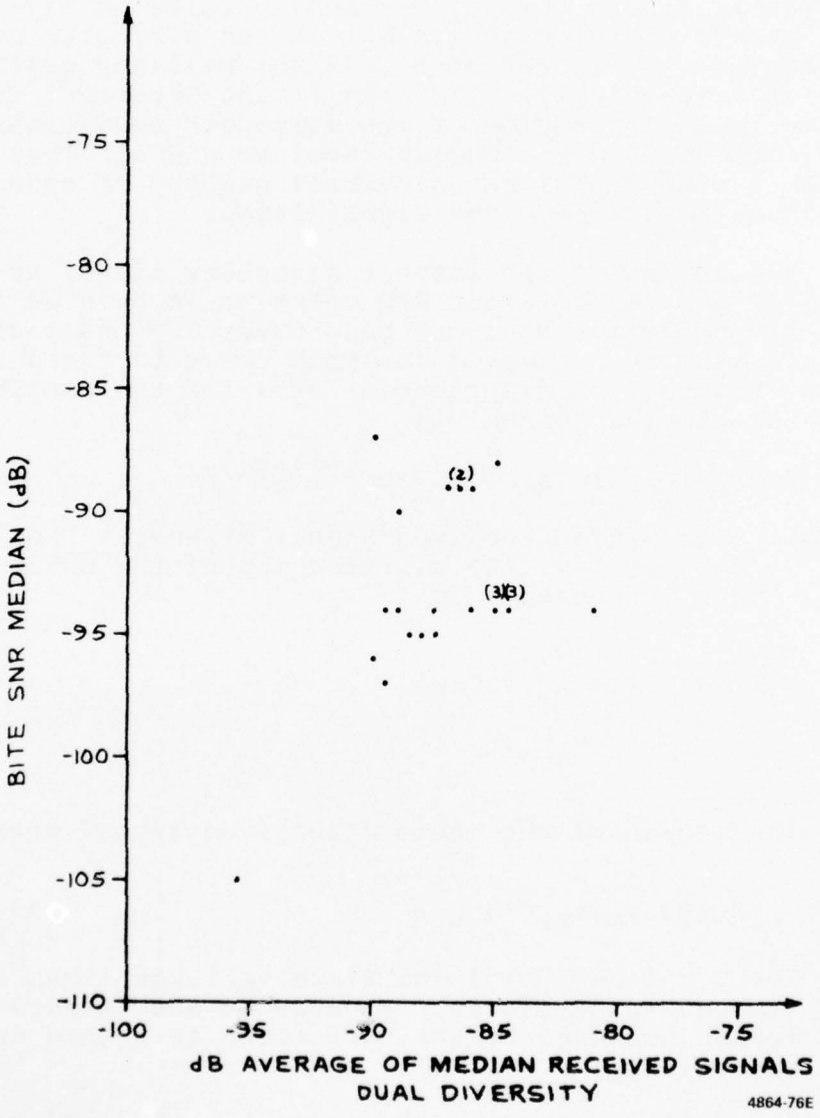


Figure 36. BITE SNR vs. dB Average of Received Median, D=2

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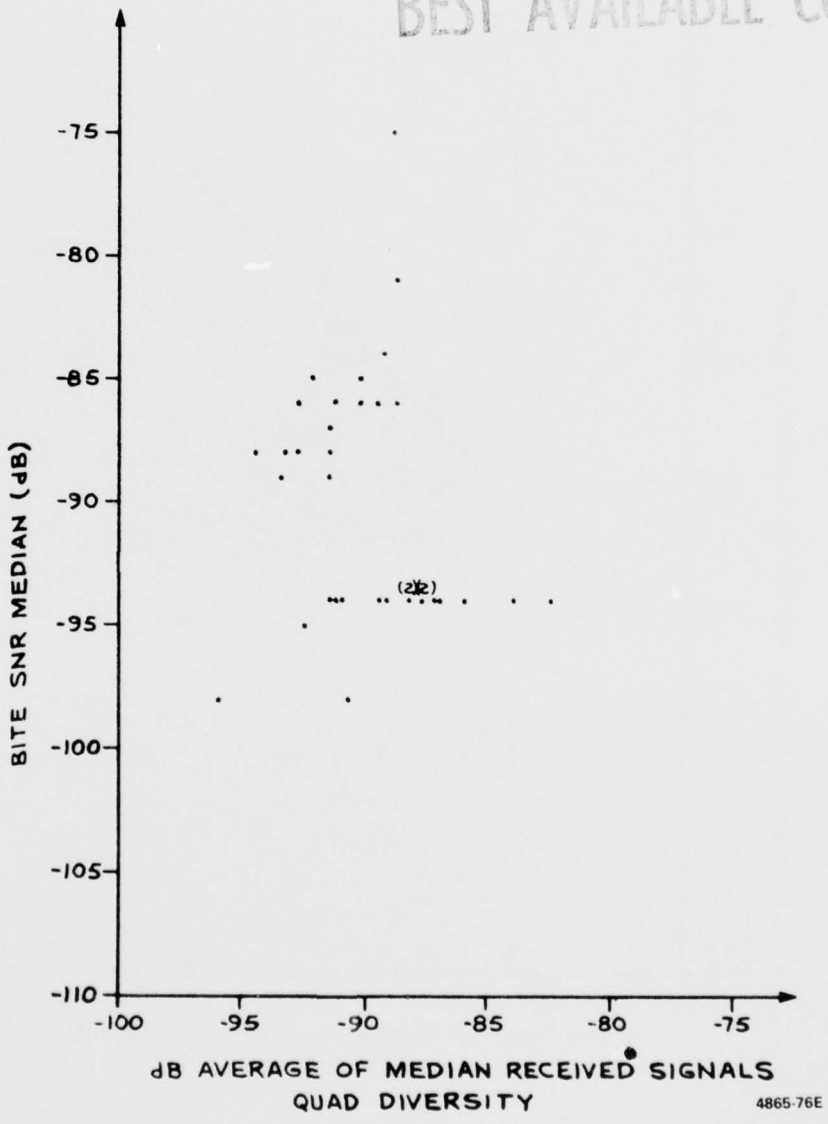


Figure 37. BITE SNR vs. dB Average of Received Median, D=4

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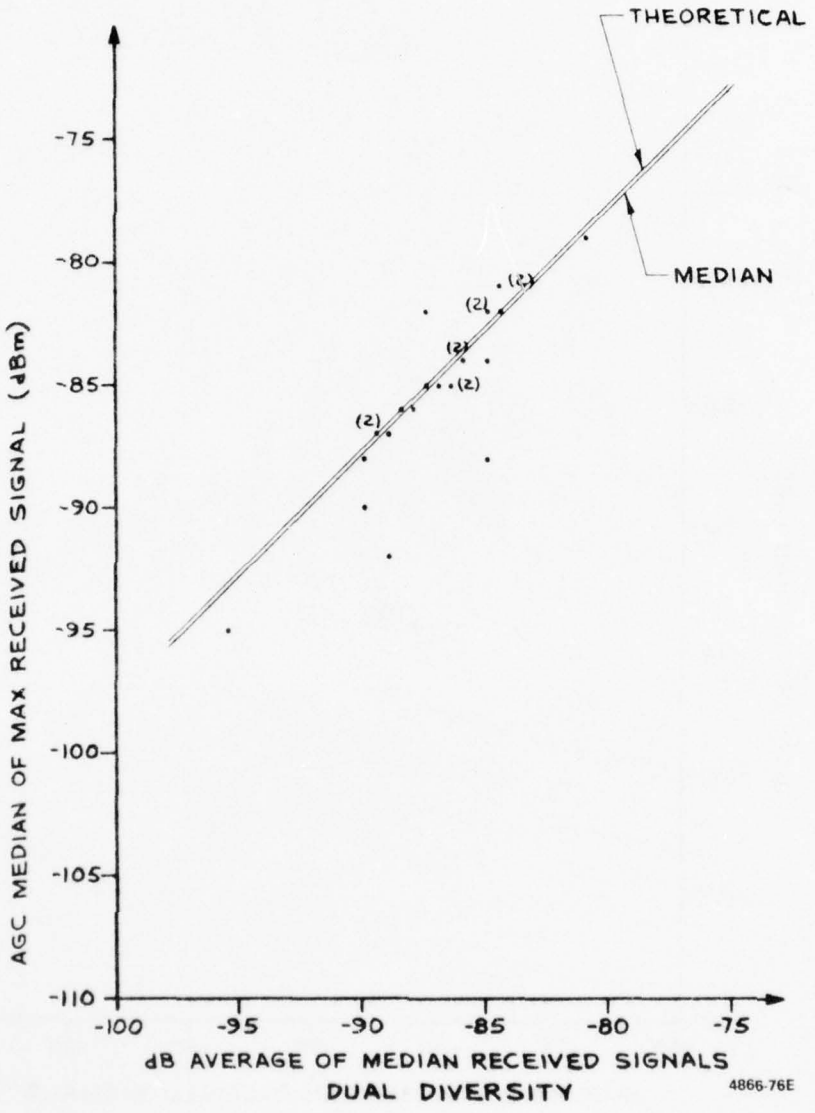
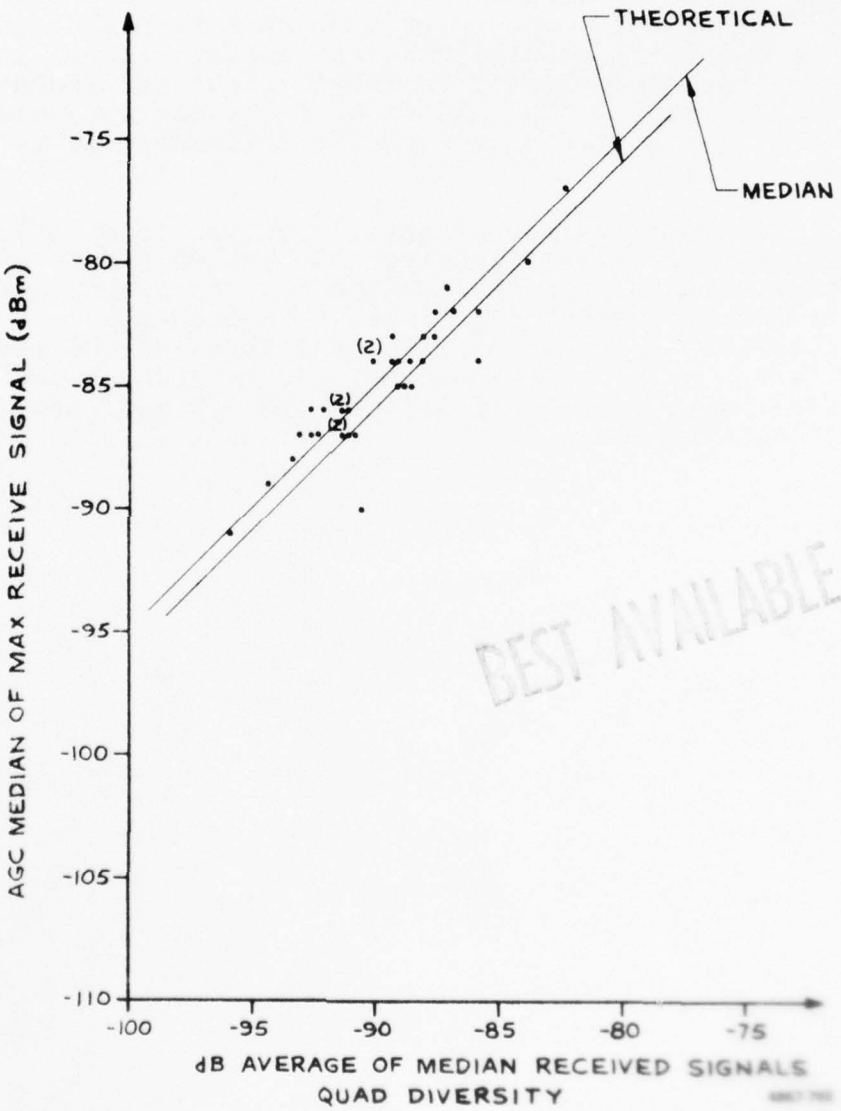


Figure 38. Strongest AGC Median vs. dB Average of Received Median, D=2



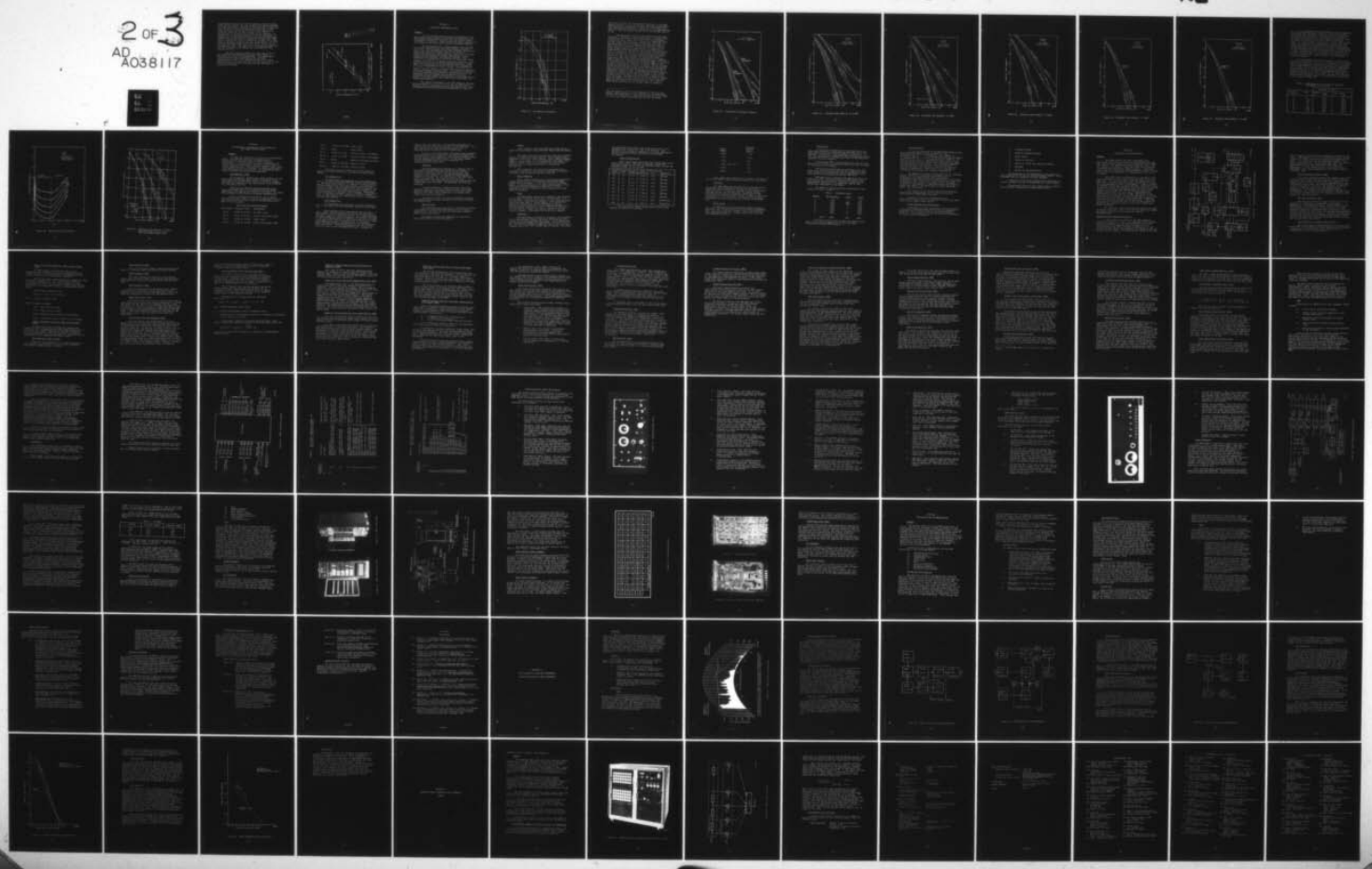
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Figure 39. Strongest AGC Median vs. dB Average of Received Median, D=4

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MEGABIT DIGITAL TROPOSCATTER SUBSYSTEM (MDTS).(U)
FEB 77 D R KERN, P MONSEN DAAB07-74-C-0040

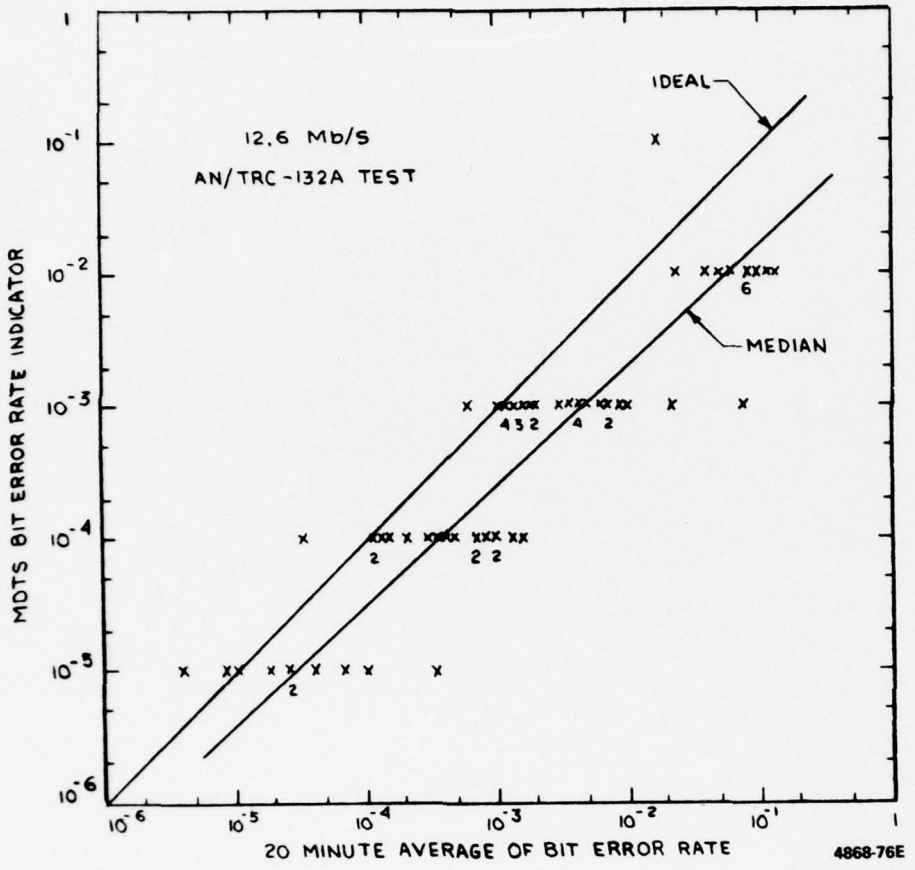
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is obtained from the 13.2 Kb/s PN sequence used to provide frame control between the time division multiplexed message and order wire bits. Because the PN frame rate is much less than the data rate and the measurement duration is four times less than the Average Bit Error Rate (ABER) test duration, there will be more scatter in the monitor measurement. Also the monitor function only displays the exponent of the measured average bit error probability. A scatter plot of the monitor results and the 20 minute ABER tests at the 12 Mb/s rate is presented in Figure 40. The monitor function is seen to provide an estimate of the ABER which is generally smaller than the actual value. It is believed that the offset from ideal is due to truncation of the mantissa digit. The addition of one mantissa digit for the BER indicator would improve the usefulness of this monitor function.

For small values of ABER, say less than 10^{-5}, the BER indicator occasionally presents a value orders of magnitude less than the measured ABER. This phenomenon results from the error contribution to the ABER concentrating in the first fifteen minutes of the test, possibly one or two error bursts, and very few errors in the last five minutes of the test when the BER indicator is extracting its data.



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Figure 40. BER Indicator vs. ABER Measurement

SECTION 4

SIMULATED PERFORMANCE TESTS

GENERAL

In this section fading channel performance of the MDTS modem using a QDSTS is summarized and compared to the performance calculations derived from the analytic model developed in Section 2. These results provide a baseline for evaluation of the performance results from CONUS testing.

The performance of a single channel modem receiver on a white Gaussian noise non-fading channel is shown in Figure 41. The degradation from ideal coherent detection is about 2 dB which is primarily due to the effect of differential encoding (approximately a factor of 2 in error rate), the adaptation self noise, quantization of the backward filter weights, and spectrum control. The expression for differential detection of phase-shift keyed signals, $1/2\ e^{-E_b/N_o}$, is seen to provide a convenient lower bound for the actual non-fading modem performance. Since most of the contribution to the average error probability occurs at instantaneous values of E_b/N_o, corresponding to the 10^{-1} to 10^{-2} region, it follows that bound and measured fading performance would be close. As outlined in Section 2, use of the exponential performance characteristic has the advantage that the average error probability can be determined by calculating a determinant of rank equal to the number of forward filter taps rather than calculating the eigenvalues directly.

The fading performance of the DFE modem was measured at data rates of 1.5, 3.1, 6.3, 9.4, and 12.6 Mb/s over a complete range of multipath profiles and channel fade rates. Performance characteristics can be summarized in terms of

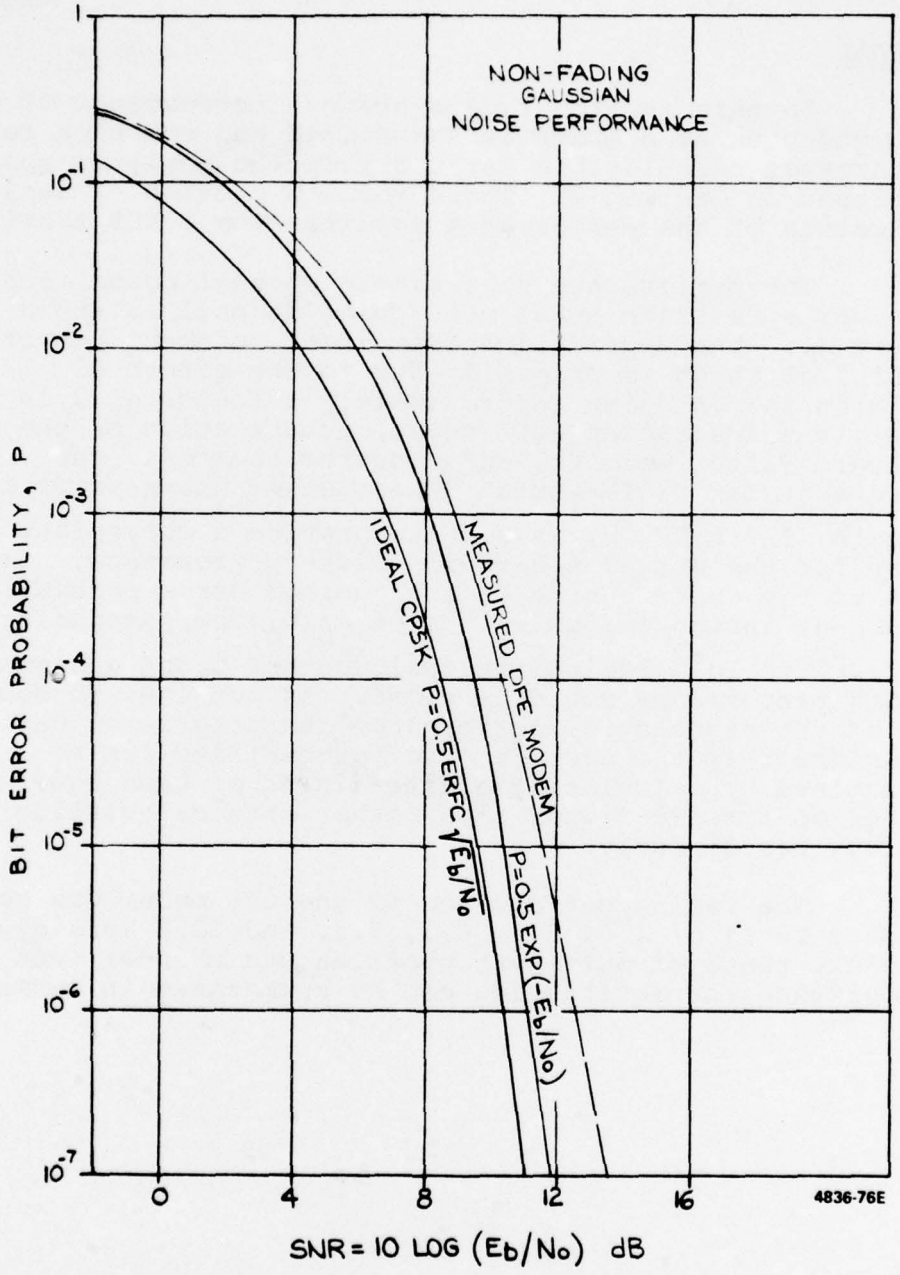


Figure 41. Non-Fading Performance

the ratio of twice the rms multipath spread σ to the QPSK symbol interval T. For a fixed $2\sigma/T$ and E_b/N_o, performance was essentially independent of data rate. Performance for dual and quadruple diversity operation is also unaffected by choice of the rms Doppler spread* up to the maximum rate of 10 Hz.

The performance results calculated from the model developed in Section 2 are presented again in Figure 42 for selected values of $2\sigma/T$. Two future bits of intersymbol interference were used in the calculation. Additional bits did not change the performance results for the range of multipath considered. As expected the "optimum" value of $2\sigma/T$ is greater for larger diversity order as diversity helps reduce intersymbol interference. A summary of the measured MDTS modem performance at all the data rates is given in Figures 43 through 47. The values of $2\sigma/T$ selected for the performance calculation agree with the 12.6 Mb/s values in Figure 43. The calculated and measured compare well at all data rates except for extreme multipath conditions under dual diversity operation. As an example, Table 6 shows the calculated and measured E_b/N_o to achieve a 10^{-6} average error probability. Except for $2\sigma/T = 1.2$ at D = 2, the calculations are accurate to within 2σdB for dual diversity and they are accurate to within 1 dB for all $2\sigma/T$ values for quad diversity. The poorer measured performance under extreme multipath conditions at D = 2 may be due to incomplete removal of past intersymbol interference due to insufficient dynamic range in the backward filter weights or saturation effects due to amplifier dynamic range in the forward filter. The model assumes perfect removal of the past intersymbol interference and of course infinite dynamic range to handle multipath induced peaks. Dual Diversity data was not taken at the lower data rates (3.1 and 1.5 Mb/s) since this was not our primary area of interest).

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*The rms Doppler spread is the standard deviation of the Doppler power spectrum. In the simulator it is established by the 3 dB bandwidth of a two-pole Butterworth filter used to filter the input white noise driving the tap gains.

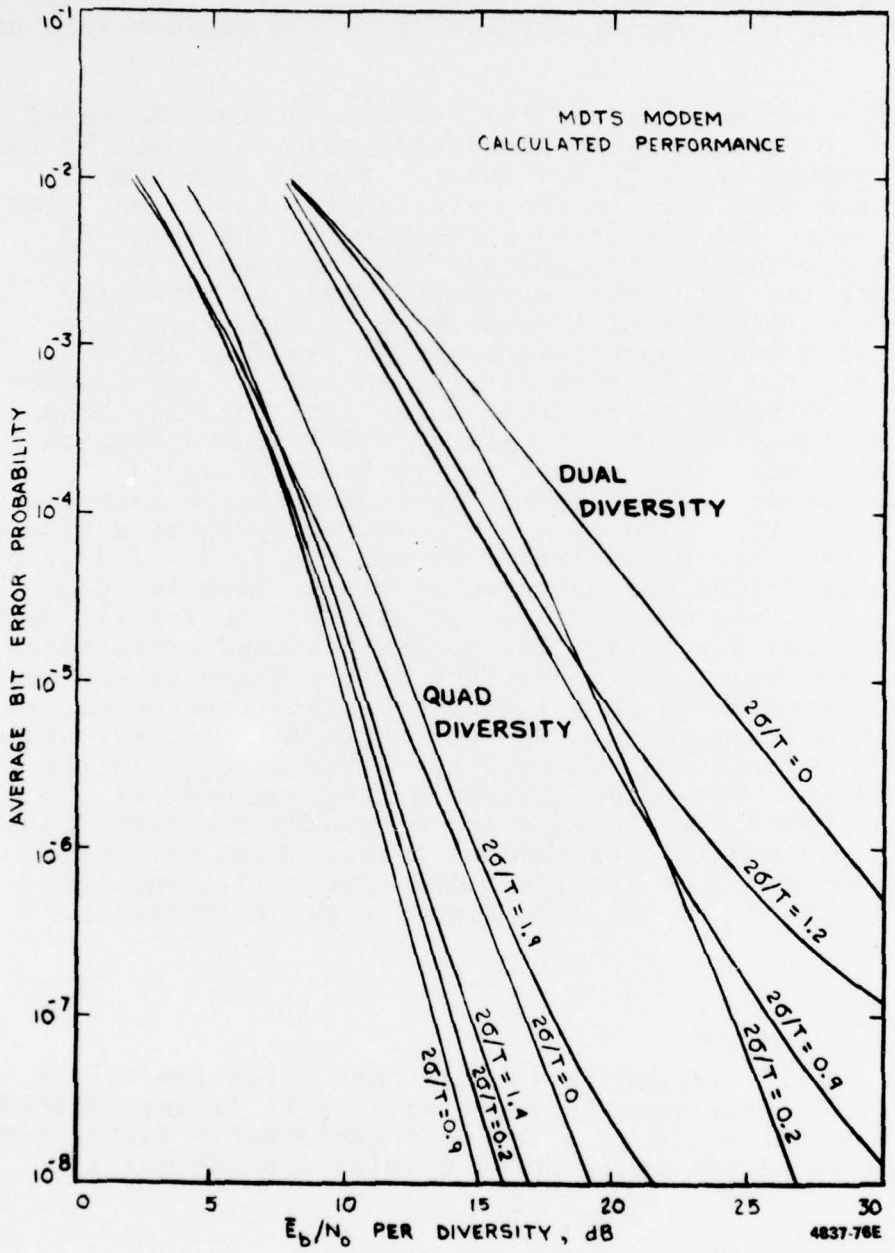


Figure 42. Calculated Performance Results

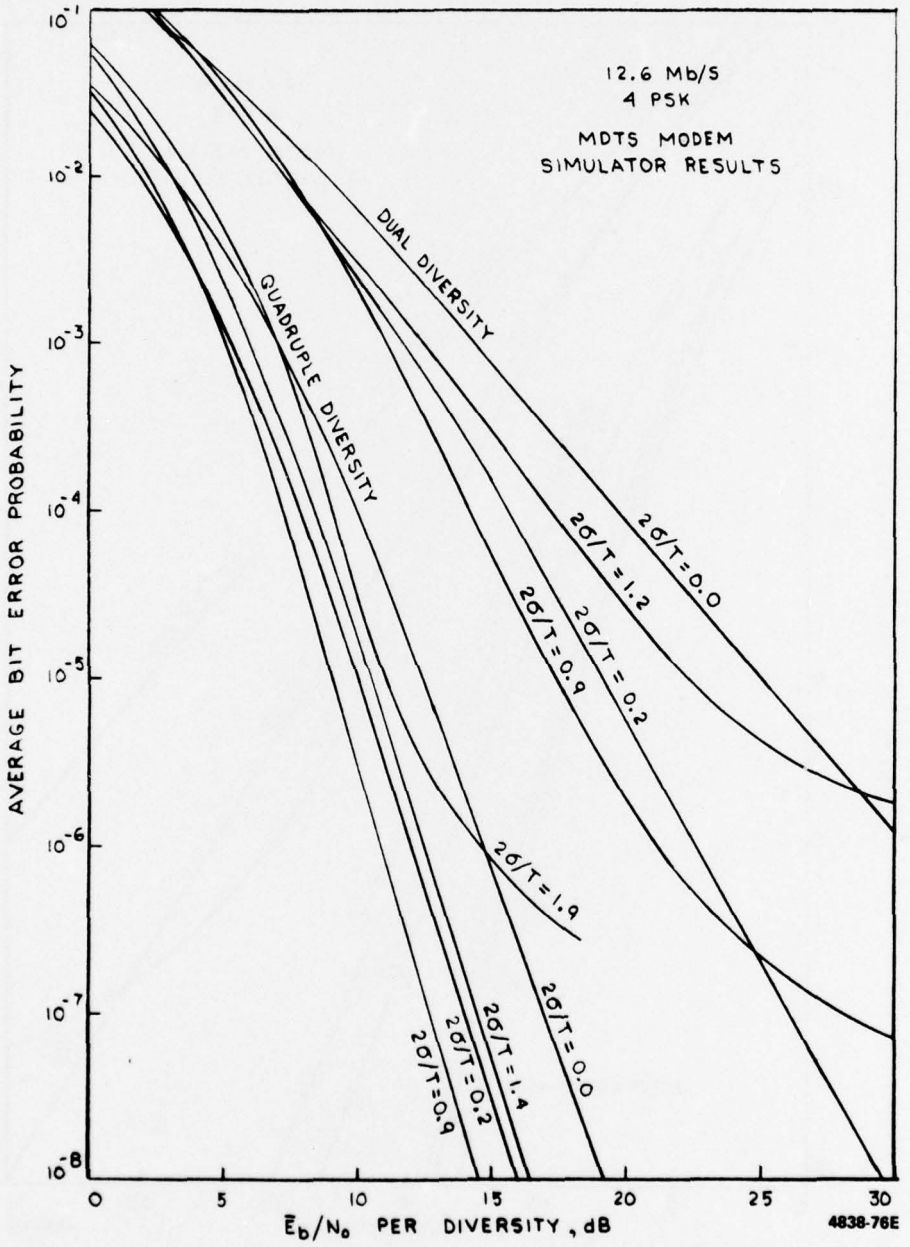


Figure 43. Simulator Test Results, 12.6 Mb/s

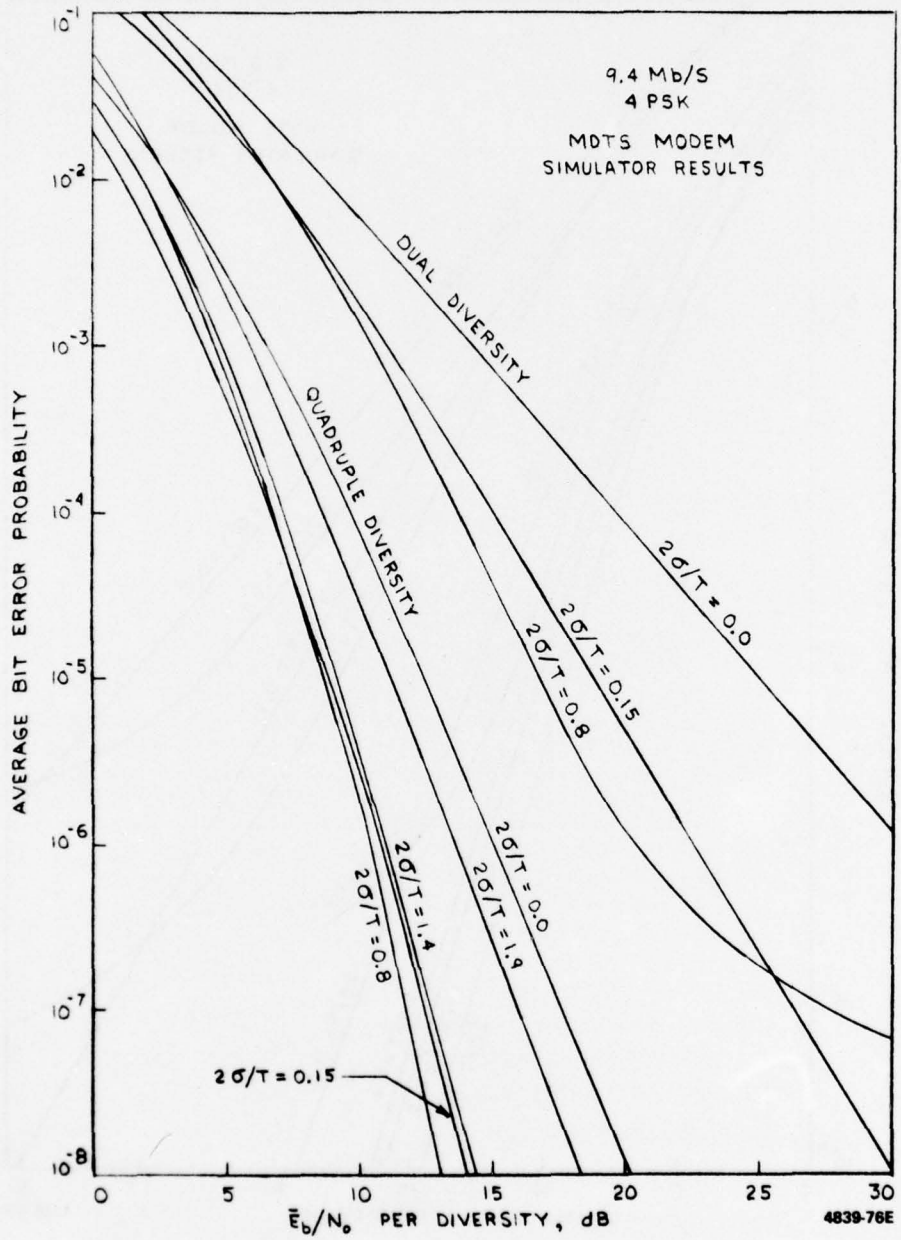


Figure 44. Simulator Test Results, 9.4 Mb/s

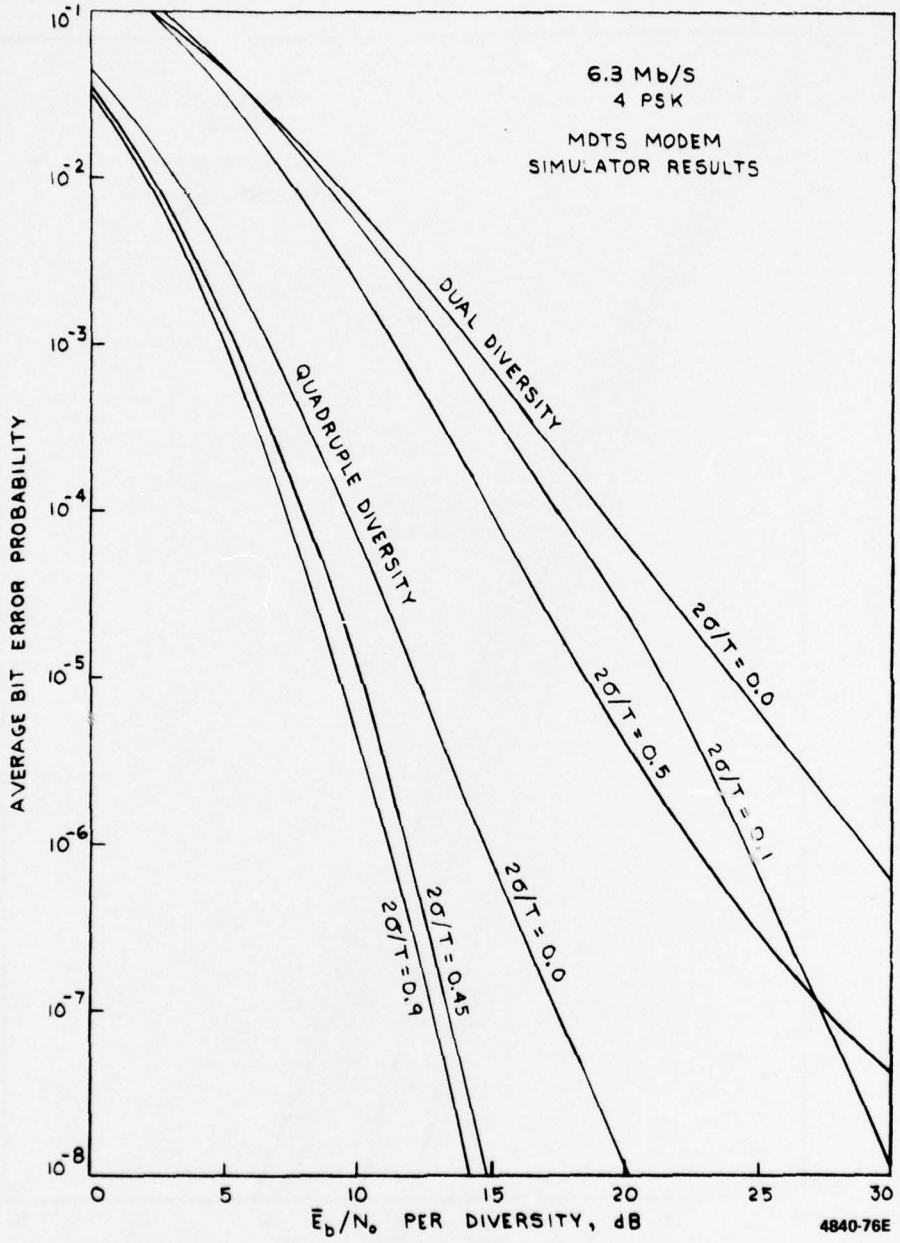


Figure 45. Simulator Test Results, 6.3 Mb/s

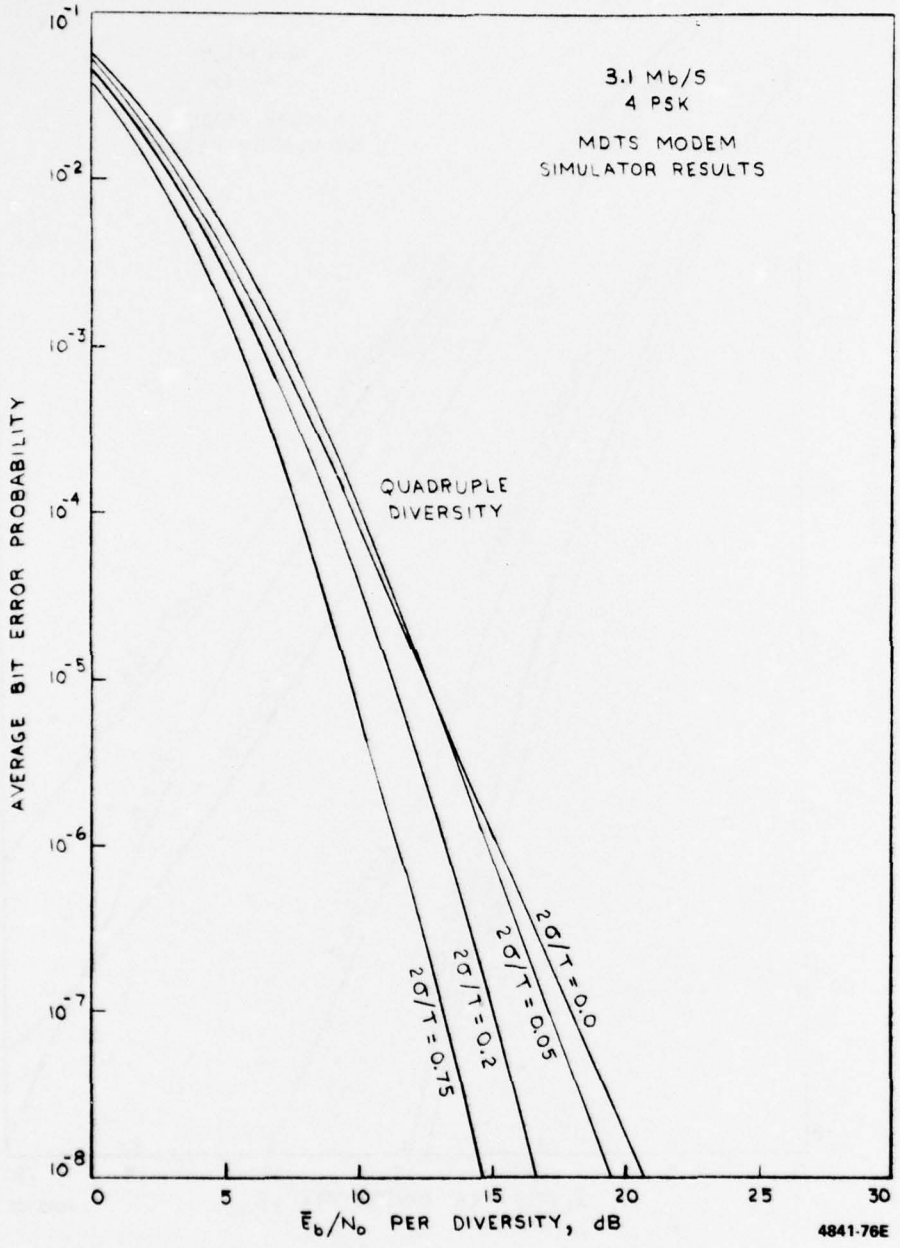


Figure 46. Simulator Test Results, 3.1 Mb/s

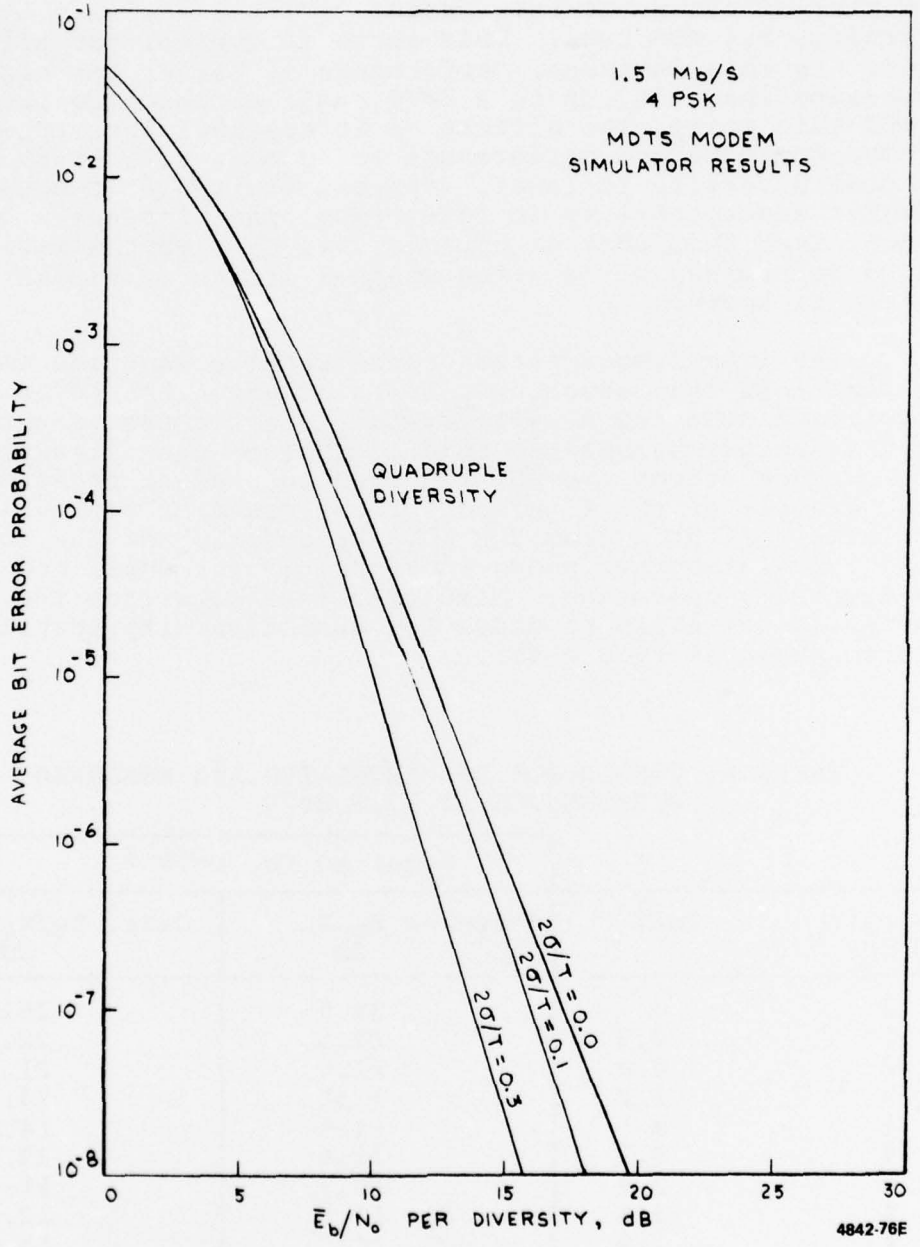


Figure 47. Simulator Test Results, 1.5 Mb/s

It is noteworthy that performance initially improves with increasing multipath relative to data period ($2\sigma/T$ increasing) and then falls off again due to the finiteness of the equalizer structure. This phenomenon, implicit diversity, is exemplified in the curves of Figure 48, which is a plot of bit error rate versus $2\sigma/T$ for the quad diversity, 9.4 MBS case. This curve is typical for all data rates. In this instance, performance is better for high dispersion channels, up to a $2\sigma/T$ ratio approaching 1.0. Beyond this point, the effects of intersymbol interference becomes dominant and performance falls off. The break point for dual diversity is lower, (approximately 0.8) because of a higher susceptability to intersymbol interference. It is evident from this that an optimum data rate approximation can be determined for a given channel if its multipath profile is known.

The intersymbol interference penalty is quite small for $2\sigma/T$ less than about 0.4. In this region the lower bound computation assuming no intersymbol interference is accurate and the approximations required to include the intersymbol interference effect are not required to predict performance. As an example of the tightness of the bound at $2\sigma/T=0.4$, simulator test data from the MDTS breadboard and the lower bound calculation are shown in Figure 49 for dual, and non-diversity operation. Simulator test data from the MDTS engineering development model for quad diversity operation is also shown in Figure 49.

TABLE 6. COMPARISON OF CALCULATED AND MEASURED PERFORMANCE AT 12.6 Mb/s

		Required for $P=10^{-6}$	
Diversity Order	$2\sigma/T$	Measured E_b/N_o dB	Calc. E_b/N_o dB
2	0	30.0	28.5
2	0.2	22.5	22.0
2	0.9	21.0	21.7
2	1.2	> 30	24.0
4	0	14.5	14.2
4	0.2	12.0	12.0
4	0.9	10.7	11.5
4	1.4	12.5	12.5
4	1.9	14.5	15.0

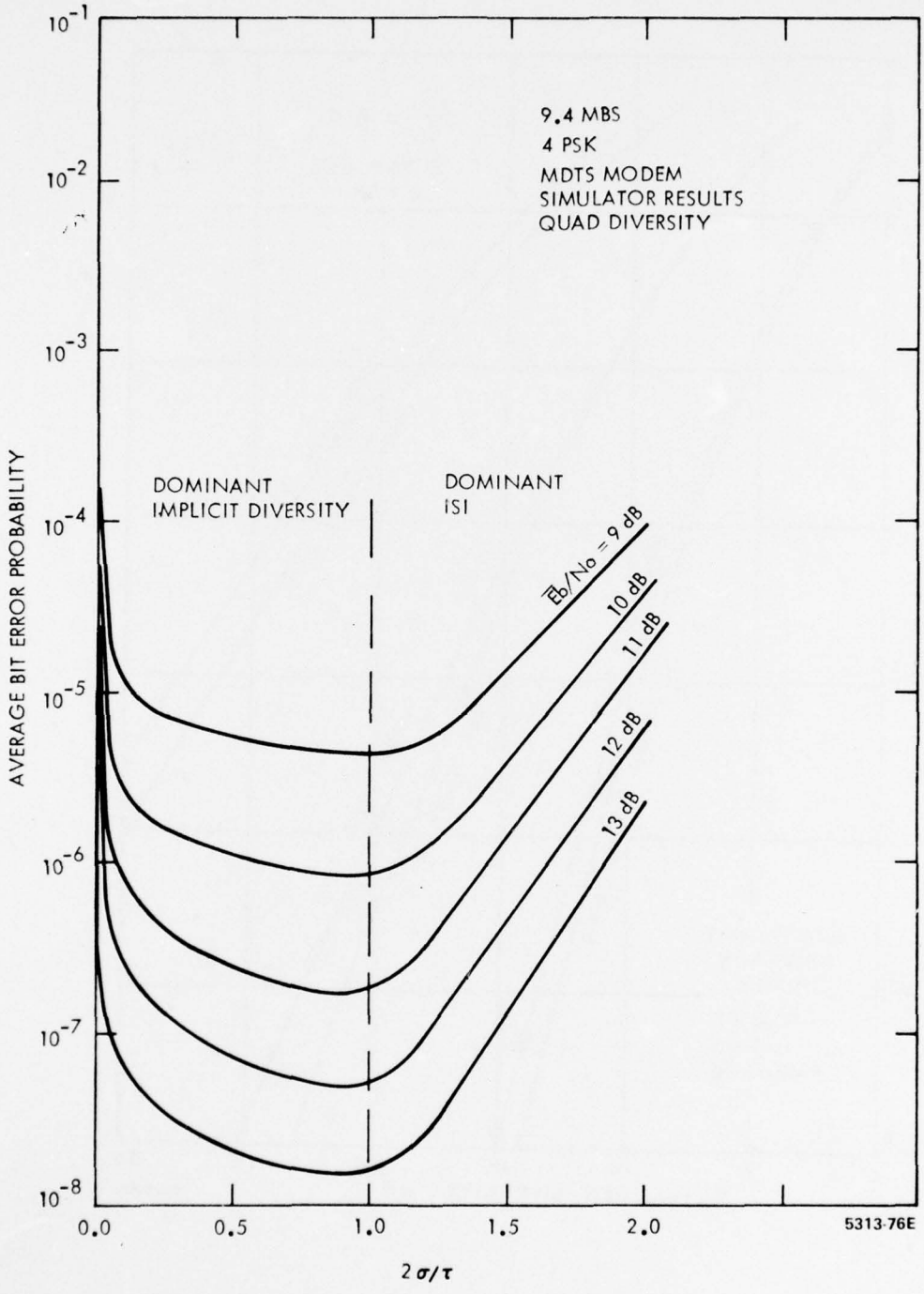


Figure 48. Implicit Diversity Effects

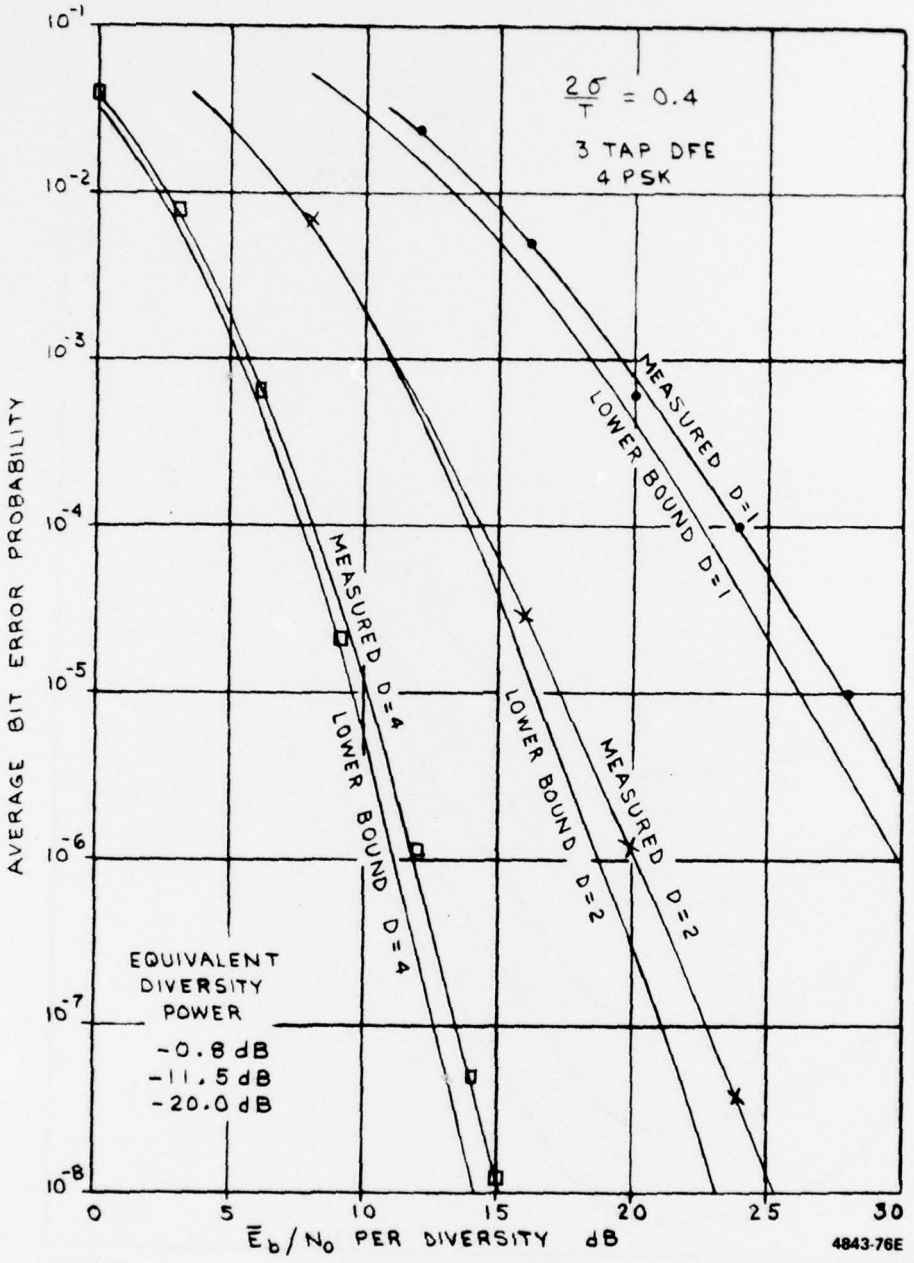


Figure 49. Simulator Test Results, 3.1 Mb/s
MDTS Breadboard for D=1, D=2
MDTS Development Model, D=4

SECTION 5

ENVIRONMENTAL, RELIABILITY, MAINTAINABILITY AND HUMAN FACTORS TESTS

GENERAL

The MDTS was subjected to a series of Environmental Tests, a 16,000-hour Reliability Demonstration, a Maintainability Demonstration, and Human Factors Demonstration. The Environmental Test included EMI, low temperature, high temperature, humidity, sand and dust, fungus (samples only), bench handling (samples only), shock (in shipping container), vibration (in shipping container), power determination, and altitude. In this section the results of these tests have been summarized.

ENVIRONMENTAL TESTS

Electromagnetic interference tests conducted on the MDTS Modem successfully demonstrated conformance to the requirements of MIL-STD-461A, Table VI, Notice 4 (modems). The modem was designed to the requirements of RS 03 and RS 03.1 in lieu of RS 03.2.

Conducted and radiated emission/susceptibility tests, tabulated below, were performed with the modem operating at the maximum bit rate of 12.552 Mb/s. All tests were conducted at GTE Sylvania, Needham, Massachusetts.

Final recommendations advise the use of double shielded interface cables to maintain a comparable level of EMI integrity at the system level as demonstrated by the modem as a subassembly.

EMI Tests Conducted And Passed

TEST METHOD	FREQUENCY RANGE	MEASUREMENT
CE 02	10 KHz to 50 KHz	AC Power Leads
CE 03	30 Hz to 50 KHz	Control and Signal Leads
CE 04	50 KHz to 50 MHz	Power Leads
CE 05	50 KHz to 50 MHz	Control and Signal Leads

CS 02	50 KHz to 400 MHz	Power Leads
CS 06	Spike	Power Leads
RE 02	14 KHz to 1 GHz	Electric Field - Broadband
RE 02.1	1 KHz to 10 GHz	Electric Field - Narrowband
RS 02	Spike	Magnetic Introduction Field
RS 03	10 KHz to 400 MHz	Electric Field
RS 03.1	2 MHz to 12.4 GHz	Electric Field

Detailed results of these tests can be found in Appendix D of Data Item A005, Engineering Accomplishment Report.

Low Temperature

The MDTS Modem was subjected to a low temperature test in accordance with MIL-STD-810B, Method 502, Procedure I. The results performed at -25 degrees F, indicated Link BER performance to be 5 db below nominal, and the modem failed to maintain synchronization for long periods of time relative to SNR. Control panel tests were successful, but off-line bite tests indicated some failures. Additional tests performed at 0 degrees F and 33 degrees F indicated a direct relationship between temperature and performance, until at room ambient all results were normal. No permanent failures had occurred.

High Temperature

The MDTS Modem was subjected to a high temperature test in accordance with MIL-STD-810B, Method 501, Procedure II.

Three problems were discovered during the tests. A power supply start-up problem occurred at +125 degrees F. Removing two circuit cards and cycling the AC power enabled the power supply to function normally. The supply continued to function normally after re-seating the two circuit cards. An IFA card failed during the test, but allowing it to reach room temperature, then re-installing it in the modem permitted quad diversity operation until the IFA heated up again and failed. Link BER performance was below normal, just as it was in the low temperature test. However, no

loss of sync was observed. The degraded performance is primarily due to shifting of offsets in the FEP cards. To a much lesser degree some deterioration may be due to observed poorer tracking of the IF amplifiers.

As part of the performance improvement task presently being performed, the IF amplifier is being redesigned and the FEP card is being improved. This should eliminate these as high temperature problem areas. As the power supply failure disappeared and has not re-appeared, no investigation has taken place.

Humidity

The MDTS Modem was subjected to a humidity test in accordance with MIL-STD-810B, Method 507, Procedure II. Electrical problems incurred during testing were due primarily to RF connectors. Link BER performance was generally below nominal. Re-seating RF cards sometimes cleared up problems. At the conclusion of the test cycle, after the modem had stabilized for a day at room temperature, all tests were successful and the Link BER test results were back to normal. No permanent failures had occurred.

A visual mechanical inspection found that minor corrosion and paint blistering had occurred. Also, some physical deformation had taken place in a plastic safety shield on the power supply frame and in the nylon card guides and card guide spacers.

The quality control of the RF connectors is being investigated and alternate connectors are being considered for future units.

Sand and Dust

The MDTS Modem was subjected to a Sand and Dust Test in accordance with MIL-STD-810B, Method 510, Procedure I, except the air velocity was not less than 200 or greater than 300 feet per minute.

The modem successfully completed all electrical tests and showed no visual degradation.

Fungus

Eight selected items from MDTS were subjected to a Fungus Test according to MIL-STD-810B, Method 508, Procedure I.

The three printed circuit modules that were included showed no evidence of fungus growth. Minor fungus growth appeared on some soft vinyl sleeving, and an adhesive backed rubber. In all cases, it is believed that the growth took place on foreign materials entrapped within the subject material, as the subject materials are classified non-nutrient.

After cleaning, all electrical assemblies were returned to active service within a modem and no problems relative to the fungus testing have occurred.

Bench Handling

Three items from MDTS were selected and subjected to a Bench Handling Test in accordance with MIL-STD-810B, Method 516.1, Procedure V. The items included a digital module, an analog module, and a power supply module. Post bench handling tests showed no mechnical or visual degredation, and all electrical tests resulted in normal modem performance.

Shock

The MDTS Modem, packaged for shipment, was subjected to six impact shocks of 15 g's and a time duration of 11 milliseconds. One shock was applied in each direction along the three major axes of the equipment. Post shock Tests showed no mechanical or visual degredation, and all electrical tests resulted in normal modem performances. A circuit breaker failure did occur at the end of this test, but this was as a result of a defect common to all the circuit breakers. This defect has since been remedied.

Vibration

The MDTS Modem, packaged for shipment, was subjected to a simple harmonic motion, having an amplitude of 0.015 inches (0.030 inches maximum excursion). The frequency was varied uniformly between the approximate limits of 10 to 55 Hz. The rate of frequency change was linear and such that a complete cycle (10 - 55 - 10 Hz) took 30 minutes. One cycle

was performed along each of the three major axes of the equipment for a total test time of 90 minutes. Post vibration tests showed no mechanical or visual degredation, and all electrical tests resulted in normal modem performance.

Power Determination

Power measurements were taken for both primary input power and DC power. Recorded prime power values and calculated power factors for the specified input voltage and frequency ranges are as follows:

Voltage (VAC)	Frequency (Hz)	Current (Amps)	Power (K Watts)	Power Factor (%)	Operation
120	60	6.55	0.595	75.5	Normal
120	47	7.2	0.610	70.5	Normal
108	47	6.95	0.550	73.0	Normal
132	47	7.8	0.690	67.0	Normal
120	63	6.55	0.610	77.5	Normal
108	63	6.85	0.580	78.5	Normal
132	63	6.45	0.650	76.0	Normal
132	47	7.85	0.710	68.6	Lamp Test
120	60	6.7	0.605	75.0	Lamp Test

The following DC power measurements reflect power margins in excess of 27 percent.

Power Supply	Measured Current (amps.)
-15VDC	1.75
-5VDC	0.26
+5VDC	32.5
+5VDC lamp test	33.0
+15VDC	3.5
+24VDC	0.57

With blower power measured at 135 Watts (120 VAC, 60 Hz), the DC power supply efficiency computes to 55 percent.

Altitude

The MDTS Modem was subjected to an altitude test in accordance with MIL-STD-810B, Method 500, Procedure I, except the rate of change of altitude did not exceed 2,500 feet per minute. As entrance into the chamber during altitude testing was not permitted, those parts of the functional test requiring manipulation of MDTS switches were eliminated for this test only. No deviation from normal performance was seen either during or after the altitude test.

Other Tests

In addition to the environmental tests previously discussed, the following tests were successfully completed: Order Wire Test, Spectrum Occupancy Test, Quality Monitor Test, Synchronization Test, Signal Acquisition Test, and Interchangeability Test.

Reliability

A reliability demonstration test conducted on the MDTS Modem successfully demonstrated compliance with the specified operational reliability MTBF of 2500 hours. In addition, a reliability improvement was developed by culling out, and implementing a design correction to one defective component (circuit breaker).

The observed MTBF, as calculated from the test data, was 2677 hours based on accumulated operating time in excess of 16,000 hours on 8 modems.

The tests were performed in accordance with test level A1 of MIL-STD-781B at GTE Sylvania commencing after final integration and checkout, and in operational field environments at Youngstown and Verona, New York.

Extended hours of failure free operation after the 1,000 hours mark, as demonstrated by 4,200 failure free hours during the field tests, indicates a potential for considerable improvement in reliability figures upon operational deployment of the modem.

The number of operating hours accumulated by the system is listed in Table 7.

TABLE 7. OPERATING HOURS

System	GTE Sylvania	Field	Total
1	790	--	790
2	1397	2826	4223
3	1258	2867	4125
4	1112	--	1112
5	1140	--	1140
6	1633	--	1633
7	1727	--	1727
8	1311	--	1311
Total	10368	5693	16061

Detailed results of the reliability demonstration test can be found in Appendix E of Data Item A005, Engineering Accomplishment Report.

Maintainabilty

A test was conducted on the MDTS Modem demonstrating maintenance and repair of the equipment at the Organizational Level of maintenance. The concept of maintenance at this level is that malfunctions are corrected by removal and replacement of faulty plug-in modules. The specified mean corrective maintenance time, (Mct), is 15 minutes and the maximum corrective maintenance time, Maxct (95 percentile), is 45 minutes. The associated computed mean and maximum values based on test results were confortably within the specified limits at 9.2 and 25.3 minutes, respectively. These values were computed in accordance with MIL-STD-471, Method 2, Appendix B.

The demonstration was accomplished with 50 simulated faults, selected in accordance with Appendix A of MIL-STD-471 for apportionment among the various subassemblies according to their contributions to the total maintenance task. Faults were simulated one at a time, and a technician with 20 hours training, a set of standard handtools, a voltohmeter, a technical manual and a set of spares was timed in the performance of fault isolation, repair and verification.

The utility of the on-line and off-line BITE was successfully demonstrated, with no specific areas of maintainability improvement required.

Detailed results of the maintainability demonstration can be found in Appendix F of Data Item A005, Engineering Accomplishment Report.

Human Engineering Demonstration

Conformance to human engineering design principles established by MIL-STD-1472A was verified by systematic examination of the modem using an Equipment Adequacy checklist. The checklist covered the following categories for human factors assessment:

a. workspace design

b. general workspace hazards

c. panel layout

d. design of controls

e. design of visual and auditory displays

f. markings

g. design for maintainability

An evaluation of the operability of the modem was also conducted as the part of the performance tests. It was concluded that the modem was suitably operable.

Conversion of the semi-automatic BITE capability to a fully automatic system is recommended for future modems.

The detailed results of all testing can be found in Data Item A005, Engineering Accomplishment Report.

SECTION 6

EQUIPMENT AND CONFIGURATION

GENERAL

The MDTS hardware has been constructed with particular attention to reliability, maintainability, and the ease by which changes can be incorporated with minimum cost impact. The packaging concept allows for ample room for expansion or changes. There are seven card locations unused and additional power supply capacity. Additional panel space is available on the Power Monitor Panel and room is available for additional I/O connections at the top of the rack.

Additional major considerations in the design were ease of changing operating data rates and data interfacing circuitry. All circuitry which requires changes when the data rate is changed, employ plug-in modules and/or straps. All rate dependent filters are pluggable. Timing circuitry is changed by replacing pluggable Voltage Controlled Crystal Oscillators (VCXO) and changing digital dividers by means of straps. Four of the eight modems plus one set of spare cards were delivered with all the necessary modules to operate each at the five data rates. Two modems were delivered at a fixed rate of 3.1 Mb/s and 44 at 6.3 Mb/s. These latter four modems can also be operated at any of the five data rates by using the prescribed modules supplied with the first four systems on the spare set. Other data rates can be utilized with the 1.5 to 12.6 Mb/s ranges by providing the required filters, delay lines, VCXO's and proper strapping.

All input/out drivers have been located in the same printed circuit card. This will allow for interface changes by simply replacing one card with the required characteristics.

Physical Block Diagram Description.

A functional description of the MDTS modem was presented in Section 1. Here, the modem will be described from the standpoint of each functional/physical printed circuit card. The modem as shown in Figure 50 is a functional/physical block diagram identifying all of the printed circuit cards. The modulator is located at the top section of the diagram, illustrating data inputs on the left

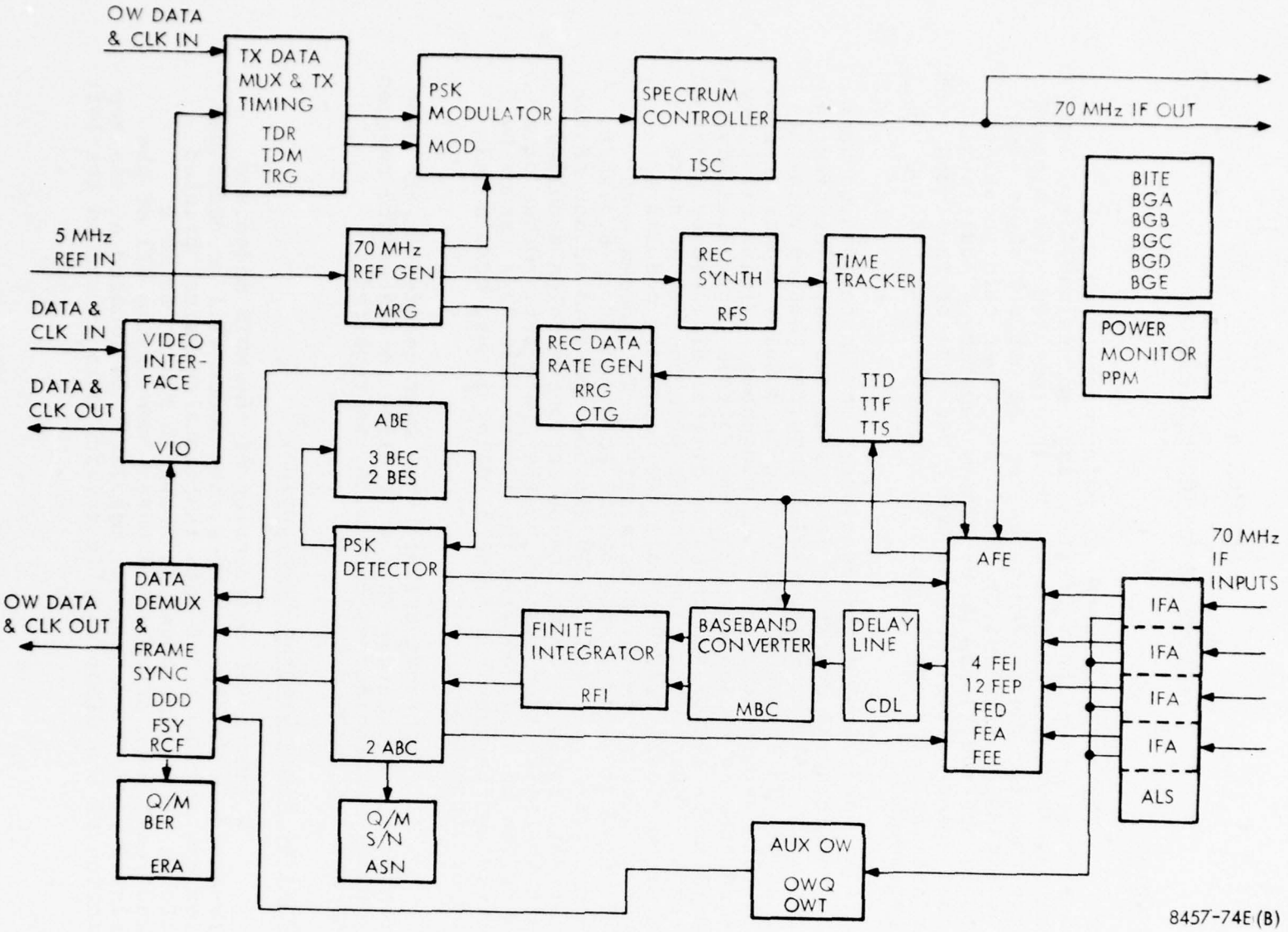


Figure 50. Functional/Physical Block Diagram

and IF outputs to the diversity transmitter exciters on the right. The demodulator is at the bottom with the diversity receiver IF inputs on the left and the data outputs on the right. The timing circuits are generally located in the center of the diagram. The BITE and Power monitor cards are shown independent of the modem functional flow. The description of each card presented in the following paragraphs is listed alphabetically by the three letter designator rather than attempting to list them in order of functional flow.

Analog Baseband Combiner (ABC)

The Analog Baseband Combiner card samples one of the cophasal receive signal outputs from the finite integrator card (RFI) and combines the ABE correction signal with the sampled signal to form an eye pattern compensated for past intersymbol interference The compensated eye is applied to a set of comparators (slicers); the outputs of which are sampled to form the output data and baseband error information. The sampling of the analog eye pattern is accomplished with a sample and hold circuit. Two ABC cards are used in the MDTS, one for the cophasal and one for the quadrature baseband channels.

AGC Level Selector (ALS)

The AGC Level Selector is part of the AGC circuits required in the Receiver IF Interface to the data demodulator. The module provides a digital command to the appropriate IF/AGC module to select the single IF output corresponding to the highest IF input level of the four diversity channels to be switched to the Auxiliary Orderwire (Service Channel) Receiver when it is placed into operation. In addition, the AGC Level Selector interfaces with both the Control Panel Monitors (CPL) and the Rack Interface Panel (RIP) by providing the required AGC voltage levels to drive the Receiver Power (AGC) meter.

Quality Monitor, Signal-to-Noise (ASN)

The Quality Monitor Card processes the digital error magnitudes in the cophasal Baseband channel only to generate an analog level proportional to the signal-to-noise-interference level at the PSK Detector.

Adaptive Backward Equalizer (ABE) Channel Cards (BEC)

The ABE Channel Card processes the product operations and accumulator function to generate the ABE weight vectors. It also generates the components of the correction vector by a final product operation.

Each of the three cards process the in-phase (I) and quadrature components (Q), for a single delay value of intersymbol interference. The basic operation is error correlation of a past signal vector (n baud times) and the averaging of the correlation values to generate the weight vector.

The two basic operations are

$$W_m(n+1) = E(n)\ D\ (n-m)^* + Wm(n)$$

and $$V_m(n+1) = W_n(n)\ D\ (n-m)$$

where* =complex conjugate

D(n) = Data vector at baud

E(n) = Error vector at baud

$W_m(n)$ = Weight vector at baud in m'th channel

$V_m(n)$ = Correction vector at baud in m'th channel

Adaptive Backward Equalizer (ABE) Control Cards (BES)

The ABE control Card combines the inphase and quadrature vector components from ABE Channel Cards 2 and 3 to produce the I and Q components of the ABE correction vector for past symbol interference from these channels. The two quadrature (I and Q) processes are identical and are implemented on two identical ABE Control Cards.

BITE Generator (BGA and BGB)

These two cards contain all the logic necessary to scan through all of the BITE circuits on the individual cards while the MDTS system is on-line.

BITE Generator (BGC)

This card contains transmit signal processing and BER error detection logic used during off-line testing.

BITE Generator (BGD)

This card contains the majority of the control logic, error detection logic, front panel interface logic, and lamp driver functions necessary to provide off-line BITE.

BITE Generator (BGE)

This card contains error detection logic, numeric display logic, and ABE test signal genration circuits necessary to provide off-line BITE functions. This card works in conjunction with both the BGD and BGE cards.

Cable Delay Line (CDL)

The Cable Delay Line card is a coaxial cable delay line placed in the signal path between the output of the AFE (FED card) and the input of the baseband converter (MBC). The purpose of the delay line is to delay the signal around the AFE loop so that the delayed IF signal and upconverted error signal are time synchronous at the input to the FEP cards. (Note: This additional delay will be added to the fixed delay lines on the FEI cards on any additional production.)

Data Decoder and Demultiplexer (DDD)

The Data Decoder and Demultiplexer Circuitry converts the received differentially encoded data from the PSK Processor to Bit Rate Data with clock for presentation to the Received Mux through the interface drivers. For parallel operation, the parallel to serial converter is not used and two output data streams plus synchronous clock signals are formatted. Aided by the Frame Synchronizer (FSY), the multiplexer data is stripped from the received data stream using a four-phase clock to sample and buffer only the multiplexer data. Also, the orderwire data (SCBS) is appropriately gated to a 64-bit FIFO which uses 32 kHz as its output clock. The parallel orderwire data is converted to a serial stream with a 64-kHz clock. Orderwire samples are sent to the Frame Synchronizer (FSY) to determine

correct framing and synchronization. When loss of sync is detected, circuitry automatically routes the auxiliary orderwire data to the SCBS output.

Quality Monitor Error Rate Average (ERA)

The quality monitor error rate average card generates error rate over either 5 minutes or 20 seconds. The error rate is defined as values between 1 and 9.9 multiplied by a negative power of ten with the negative exponent displayed on the control panel. Comparisons are made on th pseudo-random fill bit sequence.

The continuous error average measures the period between errors and then averages the periods over a triangular weight of past measurements, which is almost identical to an analog RC time constant filter weighing factor equal to the selected interval.

The equation for implementing the averaging operation is

$$P_{AV}(n + m) = P_{AV}(n) - P_{AV}(n) - (m + 1) \quad /N$$

P_{AV} = period average at clock time n

m = clock pulses between errors in orderwire bits

N = orderwire bits in measurement period of 5 minutes or 20 seconds (1.9×10^6 or 1.25×10^5)

Clock rate = orderwire bit rate equals 6.6 kb/s. The actual implemented equation is geared to the cross-over points and is

$$P_{AV}(n+m)-1 = P_{AV}(n)-1 - \frac{K(P_{AV})}{N} + \frac{m}{N}$$

The values of K(PA) are related to P_A (where P_A is normalized to orderwire bits).

Adaptive Forward Equalizer Error Up-Converter Amplifier (FEA)

This card has three identical amplifiers which amplify the 70-MHz error signals used to correlate the delayed input signals in the 12 processor cards. This card accepts inputs from the FEE card and provides the drive to the three four-way power splitters.

Adaptive Forward Equalized Tapped Delay Line (FED)

The tapped delay line is the delay and diversity summing mechanism of the four diversity pre-detection combiners. One is required per system. There are twelve inputs to the tapped delay line composed of one output from each of the three signal processors from the four diversities. These signals are summed into three groups of four each according to tap delay position. The signal summers are four-way hybrid power summers, followed by impedance matching buffers to drive the high impedance tapped delay line. The output of the tapped delay line, about 45 dB below the input, is amplified and sent to the down-converter and data detection system. The two sidetap inputs to the tapped delay line are applied to the diode detector. The resulting DC outputs are proportional to the energy in the first and third tap and are used to drive the time tracker.

Adaptive Forward Equalizer Error Up-Converter (FEE)

The error up-converter card in conjunction with the FEA develops twelve modulated 70-MHz error signals which are used to correlate the delayed input signals in twelve signal processor cards.

The inphase and quadrature digital error signals are each delayed by a 3 stage shift register. The outputs of the shift registers are three pairs of I and Q signals. The second pair is delayed by half a baud from the first and the third pair is delayed a baud from the first. These delays correspond to IF delays generated on the FED card. The 6 pairs of error signals are used to drive the three 4 phase modulators that up-convert the error data to 70 MHz for use by the AFE processor (FEP) cards.

Adaptive Forward Equalizer IF Input/Fixed Delay Line (FEI)

The IF Input/Fixed Delay Line Card provides the IF-to-pre-detection combiner interface. One is required for each diversity. On this card the IF input signal is amplified and split four ways in a four-way hybrid power divider. Three of the four identical signals are sent off the card and form the multiplier input signals to the three signal processor cards.

The fourth output of the four-way power divider is amplified and drives an untapped surface wave delay line having approximately 2.6 μ seconds delay. The output of the delay line, which is about 45 dB below the input, is amplified and split three ways in a hybrid power divider. The three outputs from the three-way divider are sent off the card and serve as the correlator signal inputs on the three signal processor cards (FEP).

Adaptive Forward Equalizer Processor (Weight/Error Correlator) (FEP)

There are three processor cards per diversity, each operating at a different signal delay point on the tapped delay line. Therefore, a quad diversity pre-detection combiner system contains a total of twelve processor cards. Each processor card contains

a. A complex multiplier or "weight unit"
b. A complex error correlator
c. A pair of baseband weight amplifier/filters.

(The terminology "complex" refers to the quadrature correlation and multiplication processes.)

In operation, the error modulator 70-MHz signal from the error up-converter card serves as the reference signal in the error correlator. The 2.6μ sec delayed input from the IF Input/Fixed Delay Line card FEI, after a quadrature split, provides the quad phase signal input to the correlator.

The correlator provides two baseband output signals representing the in-phase (I) and quadrature (Q) weights or control signals for the complex modulator. The I and Q control signals are low-pass filtered to establish the loop bandwidth and converted to push-pull to drive the balanced multipliers.

The undelayed IF input signal from the IF Input/Fixed Delay Line Card is split in quadrature and applied to each of the biphase balanced multipliers which form the quad phase complex multiplier.

The application of the I and Q control signals to the complex multipliers completes the feedback control loop which adjusts the gain and phase at each tap position to provide optimum signal summing in the tapped delay line signal and diversity summer.

Frame Synchronizer (FSY)

The frame synchronizer determines the location of the orderwire bit and the positioning of the synchronization bits within the orderwire bit frame by correlating the received decoded data bits with a locally generated replica of the transmitted sync pattern. Once frame synchronization is established, the incoming data stream is constantly monitored.

The selected synchronization scheme involves three synchronizer operational modes:

a. Search mode - The synchronizer attempts to establish synchronization by correlating the incoming orderwire data stream from the data demux with a locally generated replica of the sync sequence. Correlations are made at the orderwire bit rate. If 512 orderwire bits have been checked without a successful correlation (29 out of 33 sync bits) then the synchronizer assumes the sampled bits are not orderwire bits and a command to retard receive timing by one baud is generated.

b. Monitor mode - The circuit is considered synchronized in this mode. Continued correlations of the sync sequence are performed and the average SNR is monitored to insure maintaining sync.

c. Loss of Signal (LOS) mode - In this mode, resynchronization is attempted via a limited time search.

IF Amplifiers (IFA)

The 70-MHz quad-diversity input data signals are amplified in four separate IF channels. The IF amplifiers with their corresponding AGC circuits provide a signal level of -10 dBm $\pm$ 0.5 dB for the adaptive forward filters for an input range of -20 to -70 dBm. The AGC Level Select circuit processes the instantaneous amplitude relationship among the four diversity IF channels, and develops a common AGC voltage from the highest IF input signal level. To accommodate five data rates, a linear phase, 2 pole Butterworth plug-in filter is selected to optimize data rate performance.

A 70-MHz output from the IF amplifier via an RF analog switch is developed for the auxiliary orderwire card (OWQ). The 70-MHz auxiliary orderwire signal is subsequently processed by the AGC Level Selector circuit that selects the largest IF signal level of the four IF channels.

A secondary input is provided to each IFA to accept a 70-MHz modulated signal from the TSC card for BITE loop back.

Baseband Converter (MBC)

The Baseband Converter receives the 70-MHz, 4-PSK signal from the Quad-Diversity Predetection Combiner, coherently mixes the signal to baseband, and outputs the filtered in-phase and quadrature components to the Finite Integrators. The 70-MHz in-phase and quadrature signals at + 11 dBm are applied to the LO ports of the mixers. In the normal operating mode the QPSK output from the Quad Combiner drives a hybrid transformer to produce the two mixer RF drive levels with 0 $\pm$ 2 phase difference between channels. Each of the coherent quadratur mixer output signals is filtered by a separate 3-pole Butterworth low-pass filter in each channel. The filtered in-phase and quadrature signals at -14 dBm in 50 ohms are outputted to the Finite Integrators.

PSK Modulator (MOD)

The PSK Modulator is a four-phase modulator which translates the input formatted data from the Transmit Data Multiplexer and Encoder (TDM) to a 70-MHz phase-modulated data output.

70-MHz Reference Genreator (MRG)

The 70-MHz Reference Generator provides phase stable 70-MHz reference signals at the specified eesign amplitudes to the Adaptive Forward Equalizers, the Auxiliary Orderwire RF, PSK Modulator, and Baseband Converter. A TTL level 5-MHz clock reference output is alos provided to the Receive Synthesizer (RFS).

Output Timing Generator (OTG)

The Output Timing Generator converts the time-tracked received baud rate clock to the data output clock utilziing a type 2-phase lock loop. It is used primarily as a stable phase output clock to permit clocking of time division multiplex (TDM) equipment. The data output clock and twice the data output clock are sent to the Data Decoder and Demux (DDD) for timing purposes.

The OTG also contains a 64 kHz genertor circuit. Its primary purpose is to genrate a 64-kHz reference frequency to the Data Decoder and Demux (DDD). It additionally provides a 2.56-MHz output to the AUX Orderwire. A phase lock loop generates the 64 kHz and the 2.56 MNz based on a 12.8-MHz VCXO and divider chain which is synchronized with its associated bit rate clock(s) to achieve phase coherency. All output signal levels are TTL compatible.

Auxiliary Orderwire Analog Quantizer (OWQ)

The 70 MHz IF input signal to the Auxiliary Orderwire Analog Quantizer comes from the IFA cards via four analog IF switching circuits. Only the strongest IF channel is used as established in the AGC Level Selector Circuit (ALS). The signal is processed through an 85 kHz wide crystal filter to limit the noise bandwidth consistent with 64 Kb/s. The signal is baseband converted into I and Q channels. These signals are applied to the comparator circuits which make eight decisions relative to the magnitudes of the two analog signals. From this, a four-bit word is generated that represents the phase of the incoming RF signal with respect to the internally generated 70-MHz RF. This four-bit word is further processed in the Time Tracking card (OWT).

AOW Time Tracker (OWT)

The two inputs to this card are a four-bit word, derived on the Analog Quantizer Card and a 2.56-MHz clock. The two outputs are a 64 Kb/s data stream (SCBS) and synchronous 64-kHz clock.

The four-bit word at the input of this card represents the instantaneous relative phase of the 70-MHz IF signal presented to the Analog Quantizer. The time tracking card samples this phase information at a rate 16 times per baud and compares each sample with the best sample from the previous baud. A subtractor and a data decoder make the comparison, the output being two bits, equivalent to the transmitted information.

Each baud is separated into an early and a late period, which contains eight samples apiece. An up-down counter monitors one of the data bits and counts up for ones during the early period and down for ones during the late period. The sampling pulse used to output data from this system occurs between the up and down counts. An early/late decoder analyzes the up-down counter and makes a decision whether to advance, retard, or leave alone the sampling time such that the count will tend toward zero. These decisions are passed to an excess up/down counter. When this counter overflows, timing is advanced, when it underflows, timing is retarded. Each time the timing is altered, the excess counter is returned to its mid-position.

The final function of the time tracking card is to generate a 64 kHz clock and multiplex the two-bit data word into a single 64 K baud data stream (SCBS).

Power Supply Monitor (PPM)

The Power Supply Monitor Card monitors the AC input and DC output voltages of the power supply modules. It illuminates the "Power Supply" fault lamp and sounds the Audio Alarm in the event any of these voltages exceeds normal operating limits either high or low.

Receive Control Function (RCF)

The Receive Control Function card contains several circuits associated with receive signal processing and off-line BITE functions. The receiver related circuits include the FEE card clock generating circuit, re-adapt command processing circuit, VICOM multiplexer mode fill bit verification circuit, and the ABE reset generation circuit. The BITE circuits include the off-line test AFE fault detection circuit and the off-line BITE orderwire and traffic data generators.

Finite Integrators (RFI)

The Finite Integrators employ two passive matched filters, one each for each of the two baseband data stream outputs from the Baseband Converter. The matched filter implementation insures optimum definition of the orthogonal components of the baud vector with minimum circuit complexity.

Receive Synthesizer (RFS)

The Receive Synthesizer provides the reference baud rate clock to the adaptive time tracking circuitry in the receiver. It also provides the transmit bit rate clock to the Transmit Mux. This is accomplished through the use of two phase locked loops (PLL). The transmit bit rate clock is developed by referencing a PLL to the 5-MHz standard and selecting an appropriate divide down to send to the Transmit Mux. The reference baud rate clock is developed by referencing a PLL to the bit rate clock above and selecting the 0 dBm, 50 ohm output off the VCXO to send to the Adaptive Time Track circuitry.

Receive Data Rate Generator (RRG)

The Receive Data Rate Generator converts the time-tracked received baud rate clock to the data output Mux clock utilizing a Type 2 phase-locked loop. The RRG also provides a four-phase baud rate clock to the receive data demux along with timing gates for proper synchronization. The RRG allows its input divide chain to be retarded by one count or advanced by two counts on command to assist the frame synchronizer in its search routine. It also provides the orderwire baud sample used by the frame synchronizer (FSY) to locate the orderwire baud. In addition, the baud slip detection circuits and re-adapt command generation circuits are located on this card. All signal level outputs are TTL compatible.

Transmit Data Multiplexer and Encoder (TDM)

The Transmit Data Multiplexer and Encoder retimes the two data channels for inclusion of orderwire data, mux's the data with the orderwire data (with sync bits), reads the combined data plus orderwire at the data rate, and encodes the data with a Gray code to convert the two data bits per baud to a set of two PSK bauds.

The Orderwire Multiplexer section of the card splits the incoming 64 Kb/s Service Channel Bit Stream into two 32 Kb/s data streams. It also provides FIFO storage for the data, since the data is continuously read in at 32 kHz and read out at a gated (160 out of 193) 38.6 kHz rate. Two codes are generated, each 33 bits long, with a sequence generator clocked at 38.6 kHz and gated at 33 out of 193. One is the sync code and the other is the stuff code. Sync code is sent at the beginning of each frame.* The sync code is stuffed between blocks of orderwire data. Thirty-three sync or stuff bits follow each 160 orderwire data bits. Final data plus code is clocked out with the 38.6 kHz clock.

Multiplexer Data Retime (TDR)

The Multiplexer Data Retime Card derives bit and baud rate clocks from the incoming data stream(s) (MBS(s)) when these clocks are not supplied and multiplexes a single serial data stream into two streams clocked at the baud rate

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*For the 12.55200 MHz family, 25 filler bits complete the frame.

each taking alternate bits; 2 bits/baud. When two data streams are present, the circuit adjusts the phase of one channel to bring it close enough in phase-sync with the other allowing the baud rate clock to sample mid-bit.

Transmit Data Rate Generator (TRG)

The Transmit Data Rate Generator converts the Transmit Multiplexer bit rate clock to the desired MDTS baud rate clock. A Type 2 phase locked loop (PLL) is utilized to assemble the input data stream with framed orderwire information. This loop insures a phase lock between the input data stream and the output data stream without loss of data. This section of the TRG provides a four-phase clock, a timing gate and the orderwire baud rate clock to the Transmit Data Mux and Encoder (TDM) for proper data phasing and for proper orderwire data to orderwire sync bit framing.

The TRG also contains a 64-kHz generator circuit. The primary purpose of this unit is to provide the 64-kHz reference frequency to operate the orderwire. It also provides a 32-kHz clock to the Transmit Data Mux and Encoder and Orderwire Mux. A phase locked loop generates the 64-kHz based on a 12.8-MHz VCXO and divider chain which is synchronized with its associated bit rate clock(s) to achieve phase coherency.

Spectrum Controller (TSC)

The Spectrum Controller provides control of the modulated 70 MHz bandwidth and variable power output to the Transmitter Exciter. The 70 MHz input bandwidth is controlled by a plug-in, 3-section Butterworth bandpass filters. The selected 3 dB bandwidths of 13.3 MHz or 8.9 MHz process the MDTS IF output signals to contain 99 percent of the signal power within 15 MHz and 10 MHz, respectively. The RF output is matched to drive a 50 ohm hybrid junction power splitter. The hybrid junction is connected to provide two in-phase output ports to the exciter. The output range (zero to +17 dBm) of the two hybrid junction output ports is established by the manual gain control of the RF amplifier. A sample of the +17 dBm 70 MHz signal is attenuated and power divided into four separate loop test signals, each attenuated to -45 dBm. These four signals provide loop test sources to feed the quad-diversity IF amplifiers (IFA) for off-line BITE.

Time Tracker Weight Detector (TTD)

The time tracker weight detector card produces a phase error signal from the difference between the detected outputs of the first and third AFE Taps. The error signal is digitized and outputted to the TTF card. The TTF card timing signals are also derived from the 64-kHz clock on this card.

Time Tracker Digital Filter (TTF)

The TTF low pass filters the phase-error signal from the TTD card and produces the sine and cosine of the filtered phase error. The digital filter is equivalent to a filter with the transfer function

$$K_f = \frac{2^{-19}2000}{M_s}\left(2^9 + \frac{C\ell}{Ms}\right) \quad ; \; C\ell = \text{clock rate.}$$
$$M = 1, 2, 4, 8, 16.$$

The sine and cosine output is then produced by a digital sine/cosine converter.

Time Tracker Phase Shifter (TTS)

The phase shifter accepts the sine and cosine outputs of the digital filter, and also a tone from the demodulator synthesizer. The phase of the tone is shifted by the angle, determined by the sine and cosine inputs. The digital sine and cosine inputs are converted to analog by two DAC's. The DAC's drive the IF ports of two double balanced mixers. The input tone is amplified, then split by a 0-degree hybrid. The two hybrid outputs drive the L.O. ports of the balanced mixers. The outputs of the mixers are summed in a quadrature hybrid, then filtered and amplified. The input tone is at a frequency equal to four times the baud rate. Therefore it varies from 3 to 25 MHz. The input and output RF levels are 0 dBm.

Video Input/Output Interface (VIO)

The video input lines are two data lines and two clock lines. All four inputs are needed to interface with two TD-968 multiplexers in parallel. A single Walburn key generator would use one data line and one clock line, a single VICOM multiplexer would use just one data line, two VICOM 4004 or AN/GSC-24(U) multiplexers will use both data lines.

There are four identical circuits on the input section of this card. The function of each circuit is to translate the ±0.5 volts to ±3.0 volts at 78 ohms input levels to standard TTL levels of 0.2 volts to 3.4 volts. All lines are balanced.

The Video Output Interface Circuit provides the digital output signal interface to the external multiplexer(s) and/or encryption devices. Seven identical circuits are provided. The inputs are at TTL levels. The desired outputs are ±0.5 volts to ±3.0 volts depending on the multiplex equipment or key generator used. The output impedance is 78 ohms. Two data and associated clock lines are provided. Also, their identical mux clock lines are provided to clock the transmitting mux units if desired.

BITE

Requirements for MDTS built-in test equipment (BITE) include:

a. Facilities to monitor DC voltages

b. GO/NO GO fault location capability to the circuit card level.

c. Operation without interruption of normal traffic data.

d. Test points (color coded) on each circuit card.

e. Metering facilities to insure proper operation of the equipment.

A multilevel test facility has been incorporated to meet these requirements. The first level involves performance monitoring of the operating system via the control panel quality monitor indicators. These indicators display average received power to the modem, bit error rate based on the received synchronization sequence, and received S/N ratio based on error at the output of the demodulator detector. Periodic monitoring of these control panel indicators provides an indication of proper on-line operation of the equipment. The second level is the on-line BITE.

The on-line BITE monitors the fault status of selected MDTS circuit cards by periodically scanning the fault status lines generated by each card. A fault indication on one or more lines results in sounding of the fault alarm and display of a card associated number on an operation/control panel numeric indicator. The on-line BITE continuously scans the fault lines during normal on-line operation.

The on-line BITE, while quite effective, will detect only about 70 percent of all possible fault situations in the MDTS. To further aid in fault isolation a third level, the off-line BITE, has been included. The off-line BITE generates special internal test signals and establishes internal test loop back paths within the MDTS as a function of a test select switch on the operational/test panel. System response to the test signals is analyzed to determine if a card or a group of cards is malfunctioning. Fault information is displayed to the operator via an operational/test panel numeric display. Test signal generation and system response analysis are performed automatically upon initiation of the test via a pushbutton on the control panel. It is necessary to take the MDTS off-line via the test/operate switch to use this BITE.

The fourth level of BITE is test points. Color coded test points are provided on each card and are accessible without putting the card on an extender.

A special power supply monitor circuit monitors DC voltage levels within the power subsystem and sounds an audible alarm whenever any one of the 5 DC voltages goes above or below specified limits.

INTERFACES

All interfacing connections to the MDTS are made at the I/O panel located at the top of the rack. There are five types of interfaces, namely AC power, video, orderwire, I.F., and remote monitoring. Figure 51 depicts the rack panel connector interface.

The AC power is 120 VAC $\pm$ 10 percent, 1 Ø, 47-63 Hz. It is a 3-wire input, phase, neutral, and safety ground.

The video lines are the MBS and timing from/to the interfacing multiplexer units at the selected data rates. These provide the primary digitized data to be transmitted/received over the troposcatter link. Provision is made for accepting two parallel non-phased data inputs with associated clocks, if available, to the modulator, (4 inputs). There are two receive (output) data lines and three associated receive clock lines. In addition, two identical mux clocks are made available. The mux clocks may be used to clock the transmitting multiplexers if so desired. Each of these lines are balanced, 78 ohms $\pm$ 10 percent from a maximum of $\pm$ 3 volts to a minimum of $\pm$ 0.5 volts bipolar signals. TNC twinax connectors are used with type RG-108A cable. All of the signals are converted to TTL levels on the VIO card.

The orderwire interfaces consist of one set each of a 64-Kb/s data and clock input and output. The interface levels are $\pm$ 6 volts, MIL-STD-188C levels. For consistency, the same TNC twinax connectors and RG-108A cables are used.

Seven 50 ohm IF interfaces are available. The station clock input is a 1 VRMS, 50 ohms 5 MHz sine wave used for all MDTS timing. The four receiver inputs (quad diversity) are 50 ohm 70 MHz signals from the troposcatter receiver. The input signal range is specified to be between -70 and -20 dBm. Only two of the four inputs would be used in a dual diversity mode of operation. The two transmitter outputs are 50 ohms 70 MHz, with an adjustable output power between 0 and +17 dBm. Both outputs are identical supplying drive to two transmitter exciters for quad diversity operation. For dual diversity operation, only one output would be used.

The remote monitoring interface provides for remote alarming and monitoring of the MDTS (as shown in Table 8).

Table 8 lists all the rack panel interface signals and their associated connector number.

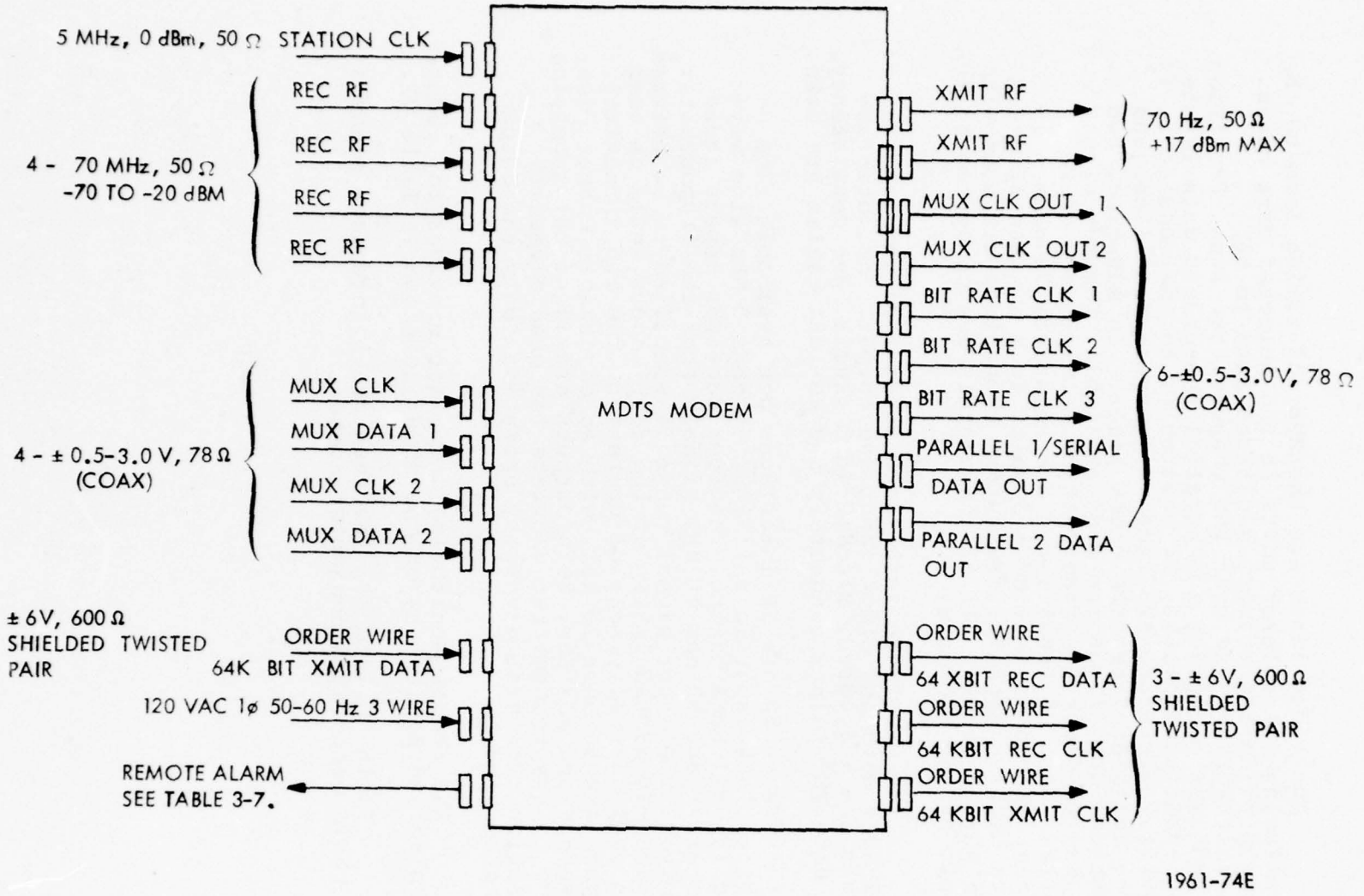


Figure 51. MDTS Interface Diagram

TABLE 8. RACK PANEL INTERFACE SIGNALS AND ASSOCIATED CONNECTOR NUMBER

Connector Designation		Description	Electrical Characteristics
J1		AC Power	108-132 Vac, 10 47-63 Hz 3 wire, 6.6 amp max.
J2		Remote Monitor	
	A	Millisecond Analog S/N Signal	Analog signal level → 0 to 8 volts → −8.5 = S/N ≤ +31.5 db, Time Constant = 1 ms.
	B	Millisecond Analog S/N Signal Return	
	C	1 Second Analog S/N Signal	Analog signal level → 0 to 8 volts → −8.5 db S/N ≤ + 31.5 db, Time Constant = 1 sec.
	D	1 Second Analog S/N Signal Return	
	E	AGC Composite Remote Monitor	Analog signal level → 0 → to 1 volt → -70 dbm ≤ P_{roc} ≤ -20 dbm
	F	AGC Composite Remote Monitor Return	
	G	Error Rate exponent 4th MSB	TTL level, active high signals
	H	Error rate exponent 3d MSB	
	J	Error rate exponent 2nd MSB	
	K	Error rate exponent 1st MSB	
	L	Error rate print command	TTL level, active high signal
	M	Remote relay contact normally open	
	N	Remote relay contact normally closed	
	P	Remote relay contact common	
	R	Error rate mantissa 4th MSB	TTL level, active high signals
	S	Error rate mantissa 3d MSB	
	T	Error rate mantissa 2nd MSB	
	U	Error rate mantissa 1st MSB	

TABLE 8. RACK PANEL INTERFACE SIGNALS AND ASSOCIATED CONNECTOR NUMBER (Cont.)

Connector Designation	Description	Electrical Characteristics
V	Selected AGC remote monitor	Analog signal level → 0 to 1 volt
W	Selected AGC remote monitor return	
X	Ground	
J3	TX mux clock in 1	Differential input/output ± 3V driving 78 ohms
J4	TX mux clock in 2	
J5	Rec bit rate clock out 1	
J6	Rec bit rate clock out 2	
J7	Rec bit rate clock out 3	
J8	Parallel data out 1	
J9	Serial/parallel data out 2	
J10	TX mux clock out 1	
J11	TX mux clock out 2	
J12	TX mux data in 1	
J13	TX mux data in 2	
J14	Service channel 64K bit TX data	MIL-STD-188C ± 6V
J15	Service channel 64K bit Rec data	
J16	Service channel 64K bit Rec clk	
J17	Service channel 64K bit TX clk	
J18	Rec RF channel 1	-70 to -20 dbm, 50 ohms at 70 MHz
J19	Rec RF Channel 2	
J20	Rec RF Channel 3	
J21	Rec RF Channel 4	
J22	TX RF Out 1	0 to +17 dbm, 50 ohms at 70 MHz (adjustable)
J23	TX RF Out 2	
J24	5 MHz station clock	5 MHz sinusoid, 0 dbm, 50 ohms

OPERATIONAL/TEST PANEL DESCRIPTION

The Operational/Test Panel (Figure 52) located at the uppermost section of the rack contains all controls and indicators used in the operation test and maintenance of the MDTS except the power monitors and adjustments.

The operational function of each control and indicator is as follows:

a. Bit Error Rate Interval 5 min/20 sec - This two-position toggle switch determines the time interval (5.0 minutes or 20 sec) over which the bit error rate (BER) sample is measured.

b. Bit Error Rate Indicator - This seven segment LED indicator displays the bit error rate (BER) as a negative exponent (power of 10). For example the number 5 would indicate the BER was between 2 and 9 x 10^{-5}.

c. SNR Meter - This meter indicates the relative signal-to-noise (SNR) ratio as determined by the vector error components being processed in the demodulator circuitry. Full scale reading is -10dBm to +30dBm. Meter calibration can be checked via a switch located on the Power Monitor Panel.

d. Receive Power (AGC) - This meter indicates received signal power by displaying the selected AGC voltage or the difference between the selected AGC voltage and the AGC voltage for a particular receiver as determined by the Channel Select Switch. Full Scale reading is -70 to -20 dBm (Black Scale) for the selected AGC voltage and 0 to -20dB (red scale) for individual receivers).

e. Fault Monitor Power Supply - The RED indicator illuminates when any system in DC voltage varies more than $\pm$ 10 percent about nominal value or if the primary line voltage is 10 percent greater or 10 percent less than the nominal 120 VAC.

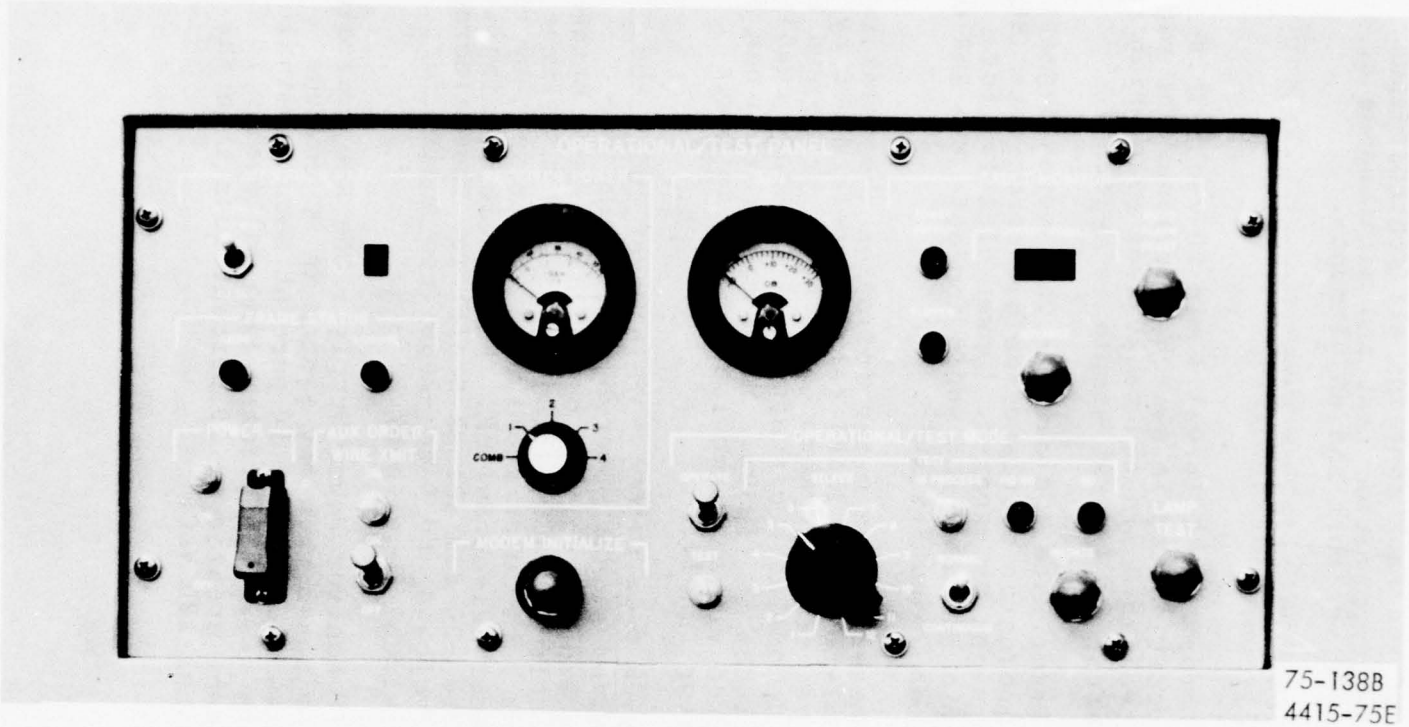


Figure 52. Operational/Test Panel

f. Fault Monitor, Blower - This RED indicator illuminates when a thermal overload is detected by a temperature sensor located on the +5 VDC power supply.

g. Fault Monitor, Circuit Module Display - This two digit seven segment LED indicator displays fault information in both on-line and off-line test modes. During the on-line test mode the displayed number (00 to 34) is associated with a particular malfunctioning circuit card. During off-line testing the displayed number is associated with a particular failed subtest. In both modes, the display is blanked when no fault is detected.

h. Fault Monitor, Circuit Module Advance - This momentary push button switch, when depressed, forces the fault monitor sequencer to continue its cycle until a new fault number is displayed or the original fault number is displayed. This switch functions only if the sequencer has stopped on a fault and does not operate in the off-line test mode.

i. Fault Monitor Audio Alarm Reset - This momentary push button switch, when depressed, disables the Audible Alarm. The Audible Alarm is re-energized whenever a new fault is detected or the Fault Monitor is recycled by the Fault Monitor Circuit Advance Switch or any other maintenance operation such as the removal of selected printed circuit cards.

j. Frame Status, Loss - This RED indicator illuminates whenever Order Wire Framing is lost. It remains illuminated until Frame Synchronization is established or re-established.

k. Frame Status, Acquire - This GREEN indicator illuminates whenever Order Wire Framing is established or re-established. The Acquire light is illuminated whenever the Loss light is extinguished; and is extinguished whenever the Acquire light is illuminated.

l. Aux Order Wire, Xmit, On - This WHITE indicator illuminates whenever the transmitter auxiliary order wire is enabled. Note: The Receive Aux Order Wire is automatically selected upon loss of order wire frame synchronization.

m. Aux Order Wire, Xmit Switch - This two-position toggle switch selects the auxiliary order wire mode of transmission when placed in the up position. The down position restores normal order wire operation.

n. Modem Initialize - This momentary push button switch provides for certain reset functions and changes in system time constants during initial system turn-on or after certain fault conditions. This switch is provided with a guard to prevent accidental actuation during normal operation.

o. Channel Select - This five-position rotary switch determines which AGC voltage is displayed on the Receive Power AGC meter. The switch selects either the selected receiver AGC (COMB) or the difference between the selected AGC voltage and any of the four independent AGC voltages.

p. Power On - This WHITE indicator illuminates whenever AC power is applied to the MDTS by means of the power on/off switch.

q. Power On/Off - This two-position Circuit Breaker Toggle Switch when actuated provides primary power to the MDTS. The circuit breaker functions provide overall primary power protection. An overload will cause the switch to drop to the OFF position. The MDTS is re-energized by moving the switch to the ON position.

r. Operational/Test Mode, Operate/Test Switch - In the operate position, this two-position toggle switch places the MDTS in the normal operational mode. In the test position the MDTS is placed in an off-line condition for the purpose of performing various off-line tests.

s. Test Select - This 12-position rotary switch selects one of a series of 11 off-line looping tests which aid in further determining the location of a given fault. The switch is generally operated from the lowest number to the highest in order that progressively larger portions of the system are added to the test sequence. Position twelve is an open position with no associated test.

t. Test, In Process - This WHITE indicator illuminates whenever one of the 11 off line tests are in process.

u. Test, No Go - This RED indicator illuminates whenever any one of the 11 tests fails to pass. A Fault Monitor, Circuit Module Fault Number will also be displayed.

v. Test, Go - This GREEN indicator illuminates whenever a test sequence has successfully passed.

w. Test Normal/Continuous - This two-position switch determines whether the selected test cycle will cycle one time (NORMAL), or if the cycle will continue until a new test is selected or the switch is placed in the NORMAL mode. In the continuous mode, the In Process Indicator will remain illuminated. The continuous mode is generally used when probing printed circuit card test points or other more detailed troubleshooting.

x. Test Initiate - This momentary push button switch is used to initiate both on-line and off line tests.

y. Lamp Test - This momentary push button switch, when depressed, appies a lamp test voltage to all indicators, including all 8's on the numeric indicators. The Audio Alarm is also enabled.

z. Audio Alarm - The audio alarm located behind the panel sounds whenever any one of the following faults occurs:

Circuit Module Fault
Power Supply Fault
Blower Fault
Frame Status - Loss.

The audio alarm can be reset by depressing the Audio Alarm Reset.

Power Monitor Panel

The Power Monitor Panel, Figure 53, is located behind the door on the uppermost section of the printed circuit card nest, and contains all the controls and indicators used in the operation and maintenance of the power supplies.

The operational function of each control and indicator is as follows:

a. AC Voltmeter - This meter calibrated in VAC (RMS) monitors the primary line voltage.

b. DC Voltmeter - This meter calibrated in VDC measures the selected DC voltage.

c. DC Volts Select - This five position rotary switch selects either the -15, -5, +5, +15, or +24 DC voltage for monitoring on the DC voltmeter.

d. CB1 through CB5 - These five toggle type circuit breakers provide primary and secondary protection for the +24, +15, +5, -5, and -15 VDC power supplies. Specific over-current conditions will cause the associated circuit breaker to open. The breaker is reset by moving the toggle switch to the ON position after the overload condition has been removed.

e. TP1 through TP6 - Five test points are used to monitor the DC voltages (+24, +15, +5, -5, and -15 DVC) with an external meter. TP6 is a common ground return for all DC voltages. These test points accept a standard 0.080-inch diameter test probe.

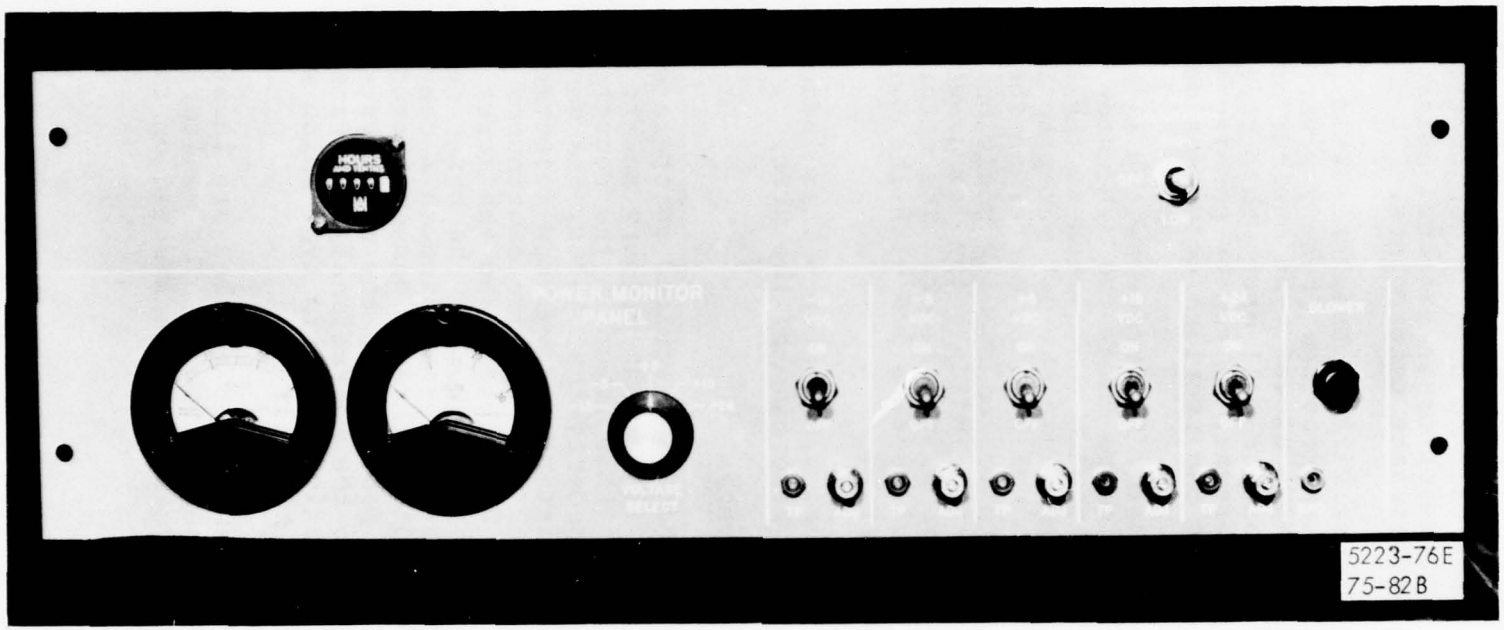


Figure 53. Power Monitor Panel

f. Voltage Adjustments - These five potentiometers provide for remote adjustment for each of the DC voltages (+24, +15, +5, -5, and -15 VDC). They will be used in conjunction with the DC voltmeter or an external meter connected to the appropriate test points.

g. Blower Circuit Breaker - This push pull type breaker provides primary power protection to the MDTS blower. An overcurrent condition in the blower will cause this breaker to trip. The breaker is set by pushing the plunger in after the overload condition has been removed.

h. S/N Meter Calibrate Switch - This toggle switch is used to check the S/N meter calibration. Positioning the switch to the high position should cause the S/N meter to indicate the high green calibration marker on the meter. Moving the switch to the low position should cause the meter to indicate the low green calibration marker on the meter. The meter indicates actual receive S/N with the switch in the off position.

i. Elapsed Time Meter - This indicator records operating time of the MDTS.

Power Subsystem

The MDTS modem is required to operate from 120 volts ± 10 percent, 10, 47 to 63Hz primary power. The power subsystem converts this input to the required DC voltage. It also includes meters, test jacks, and controls for on-line fault isolation and voltage adjustment. A Performance Monitor will provide continuous automatic monitoring of the DC voltages and the input AC voltage. Figure 54 is a block diagram of the power subsystem. Primary power enters the rack through a connector located on the top of the equipment rack, passes through the RFI filters, and then proceeds to the main system circuit breaker located at the Operational/Test Panel. The circuit breaker is a magnetic dual-trip type which will interrupt both sides of the AC line.

The five AC/DC power modules are located on a frame behind the Card Nest Assembly. The monitoring components, and overvoltage protectors are located on the power monitor

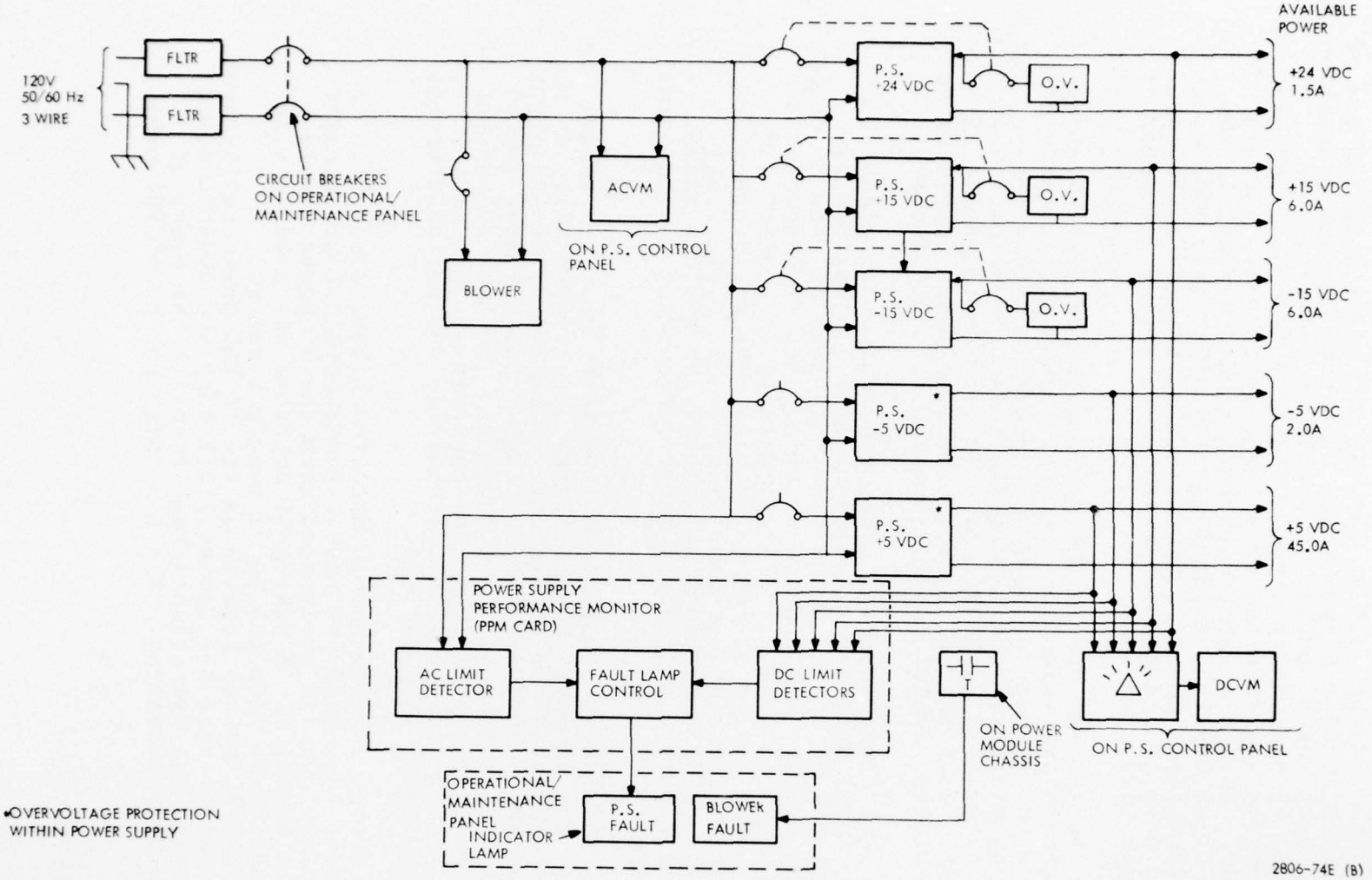


Figure 54. Power Subsystem Block Diagram

panel. The +24 VDC, +15 VC and -15 VDC power supplies are of the series regulated type which have over current protection within each power module. Overvoltage protection is provided by external overvoltage detector/crowbar modules. Each module is protected by a two pole magnetic circuit breaker. One pole interrupts the primary circuit in the event of an overload condition. The other pole will open the overvoltage shunt to prevent burnout which could occur if and only if the module was short circuited (crowbarred) for some time.

The +5 VDC and -5 VDC power supplies are switching regulator types which are more efficient, particularly at the low DC voltages. They have internal overcurrent limiting and also internal overvoltage protection. The input circuit is protected by a single pole magnetic circuit breaker. Both the series and switching power suppliers are encapsulated, sealed units, repairable at the factory.

The Power Supply Performance Monitor consists of AC and DC level detector circuits which will continuously monitor the AC input to the power modules, and the DC output of each supply. In the event any DC output is beyond 10 percent of its normal operating voltage, or the AC line exceeds the limits of 120 $\pm$ 10 volts, the Performance Monitor illuminates the FAULT lamp on the Operational Maintenance Control Panel and sounds the audible alarm. A time delay circuit prevents fault indications during normal turn-on.

The meters, test jacks, and meter selector switch are located on the Power Control Panel (see Figure 11). An AC voltmeter provides a continuous indication of the AC input to the power modules. A DC voltmeter and selector switch allows measurement of all DC outputs. Voltage adjustment of all supplies is performed from controls on this panel. Test jacks are co-located with the controls for use of external test equipment when desired.

Power is also provided to the blower located in the bottom of the equipment rack. A magnetic circuit breaker for this blower is co-located with the DC power supply circuit breakers. A push-pull actuator was used here to distinguish it from the power supply breakers. A thermostatic switch located on the +5 VDC power supply heat sink will actuate the blower fault lamp and audible alarm located on the Operational/Test Panel in the event of equipment overheating. The heat sink on the +5 VDC power

supply will have the fastest temperature rise if the blower fails. If the blower circuit breaker is inadvertently left off the "Power Fault" and audible alarm will sound.

Table 9 below is a summarization of the DC power available from each power supply and that required of the MDTS during normal operation at room temperature, 120 VAC, 60 Hz.

TABLE 9. DC POWER

Voltage	Available (amps)	Required (amps)
+24	1.5	0.6
+15	6.0	3.6
+5	45.0	33.0
-5	2.0	0.3
-15	6.0	1.8

Total input power at nominal line voltage and frequency (120 VAC, 60Hz) is 600 watts. Input current is 6.6 amps. The power factor is 0.75.

In addition, the power supplies will operate satisfactorily with primary AC power from generator sets with characteristics of Type I and II, Class 1 and 2 and Mode I and III per MIL-STD-1332. Regarding the 30 percent, 4-second recovery rise, and 40 percent, 5-second recovery dip transients for Utility (Class 2) generators, the MDTS and associated power supplies will survive these transients without damage, but may not provide normal operation during the dip transient.

The MDTS design utilized off-the-shelf power supplies which were readily available, previously tested to many of the MIL-Specifications, and relatively inexpensive. By providing a customized power supply, the size and weight can be greatly reduced, and the efficiency can be greatly increased.

Physical Description

All of the elements of the MDTS are contained in a custom designed closed rack as shown in Figure 55 and 56. Physical details of the rack are specified in Figure 57. The unit can be broken down into basic sections namely:

a. Rack
b. Blower Assembly
c. Nest Assembly
d. Power Monitor Panel
e. Power Supply Assembly
f. Control/Maintenance Panel
g. I/O Assembly
h. Intra-Rack Cabling.

Rack

The rack is totally constructed of aluminum. A hinged front door is provided to gain access into the printed circuit card nest and power supply assemblies. The door as well as openings for panels and blower is fitted with both an EMI gasket and a dust gasket. The door utilizes a heavy 3-point locking mechanism to ensure EMI integrity. The sides of the rack are removable only from the inside and then are non-removable after the rack is assembled. The rear panel is removable from the outside. However, all maintenance accessability has been designed to be from the front, thus allowing the rack to be permanently mounted directly against a rear wall. Cooling air enters from the lower front through a removable air filter rising through the nest and power supply heat sinks, and exiting through the top rear. The four-inch high fork lift base plate is removable to reduce the height of the modem for ease of installation in an S-280 shelter. The assembled unit is painted with a semi-gloss, light gray enamel in accordance with Federal Specification TT-E-529, color No. 26250, in accordance with FED-STD-595.

BLOWER ASSEMBLY

The blower assembly is a Kooltronic, Inc. Model No. KPRC729C (modified). The blower is removable from the front. Wiring is sufficiently long so that connection/disconnection can be made with the blower removed from the rack.

NEST ASSEMBLY

The nest assembly less the connector backplane was built from standard parts. The nest is approximately 37 inches high, 13 inches deep and 19 inches wide. The nest will hold 14 printed circuit cards per row times five rows for a total of 70 locations. The present configuration utilizes 60 printed circuit cards and two extender cards.

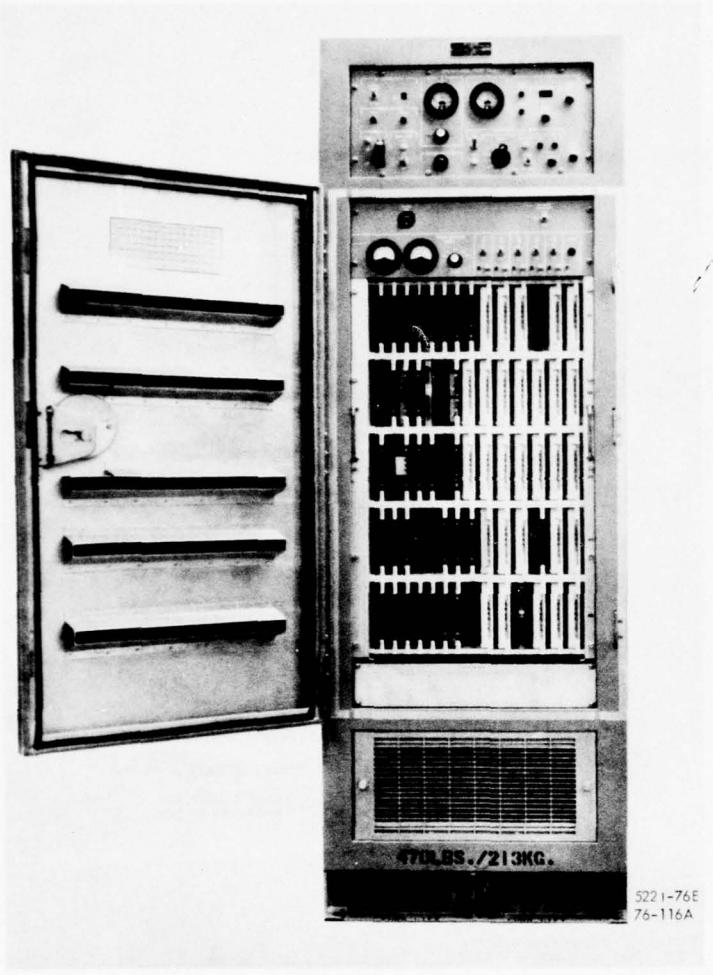


Figure 55. MDTS (Front Door Open)

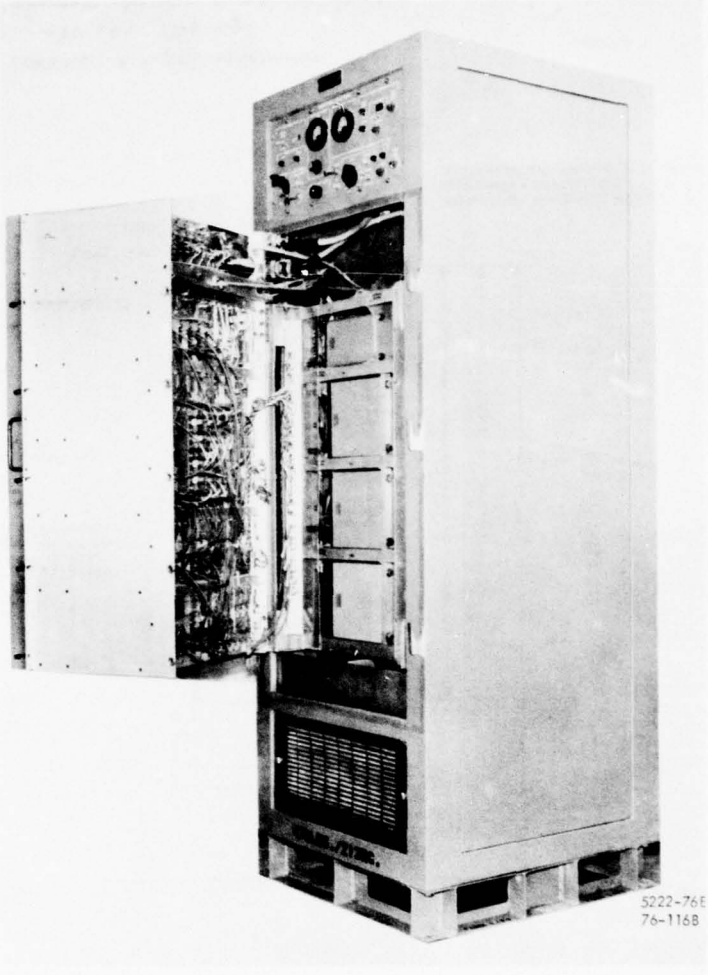
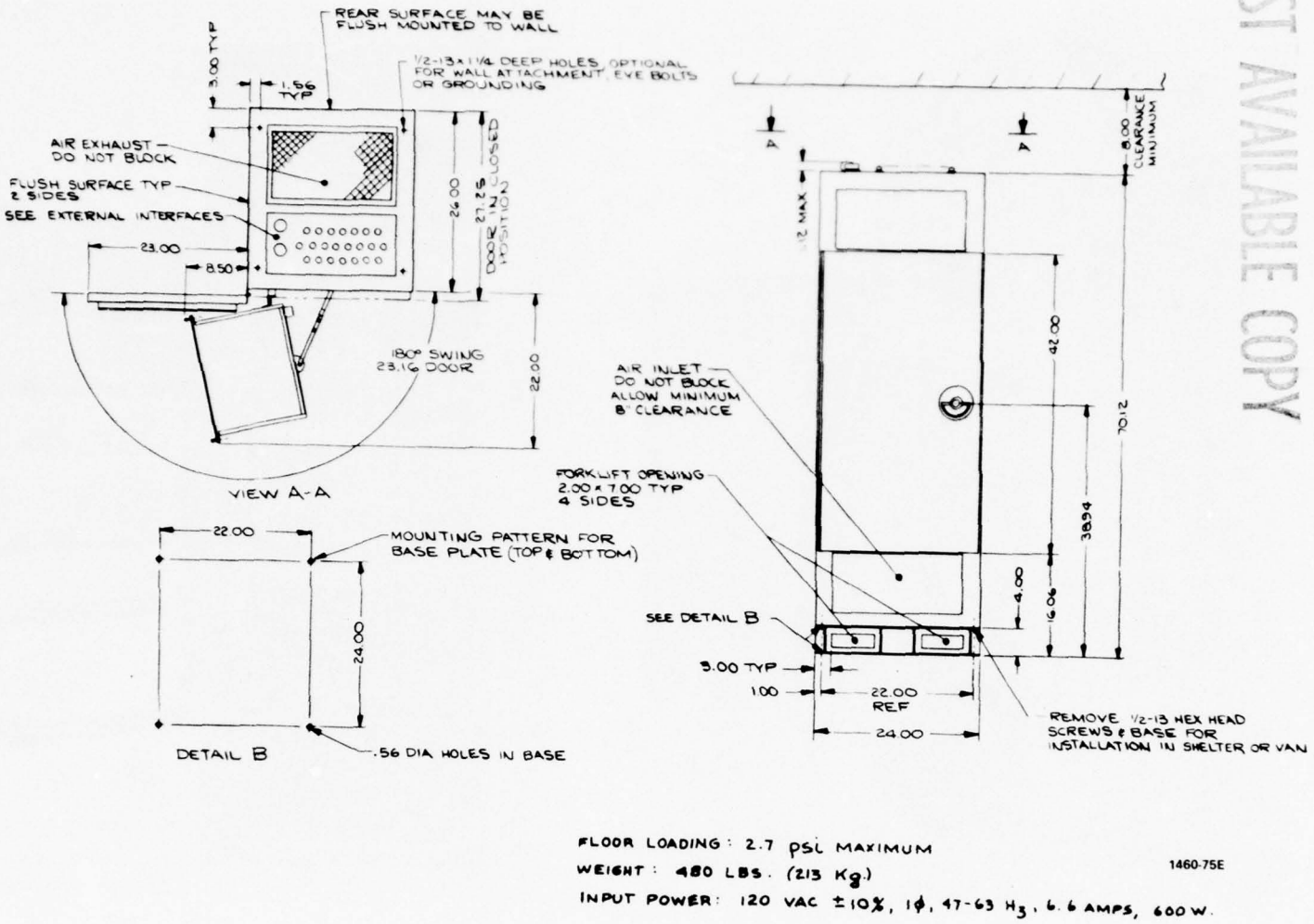


Figure 56. MDTS (Nest Open)

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FLOOR LOADING: 2.7 psi MAXIMUM
WEIGHT: 480 LBS. (213 Kg.)
INPUT POWER: 120 VAC ±10%, 1φ, 47-63 H_3, 6.6 AMPS, 600 W.

1460-75E

Figure 57. MDTS Rack Mounting Requirements

One additional location is occupied by an oversize card. Thus seven spare card slots are available with expansion to nine if the extender cards are removed. The card locations are shown in Figure 58. The card location pitch is 1 inch for digital cards which are located in the first seven columns from the left and 1 3/8 inches for shielded cards (generally operating at 70 MHz) which are located in columns 8 through 14. The basic printed circuit card is 5 1/2 inches x 10 inches. A typical digital and RF card are shown in Figures 59 and 60.

The back plane is electrically isolated from the main frame in order to provide single point grounding at the Power Monitor Panel. All cards are grounded to wire wrap pins located near the individual connectors. The +5, +15, and -15 volts are bussed along each row by means of a multilayer voltage bus. The -5 and +24 volts are distributed by wire wrap. All electrical connections are made by wire wrap or double shielded 50 ohm RF cables.

The uppermost section of the nest contains the Power Monitor Panel which is discussed below.

POWER MONITOR PANEL ASSEMBLY

The Power Monitor Panel Assembly contains the AC and DC power monitoring and adjustments, individual DC circuit breakers, a blower circuit breaker, elapse time meter and S/N meter calibration switch on the front panel. In addition the overvoltage protection devices for the series regulated power supplies (+24, +15, and -15 VDC) are located within the unit. The back panel provides a means of termination and distribution of AC and DC power to and from the power supplies and to the nest back plane. The entire unit is removable from the nest assembly by disconnecting all the AC and DC lines terminated on screwdriver type terminal boards.

POWER SUPPLY ASSEMBLY

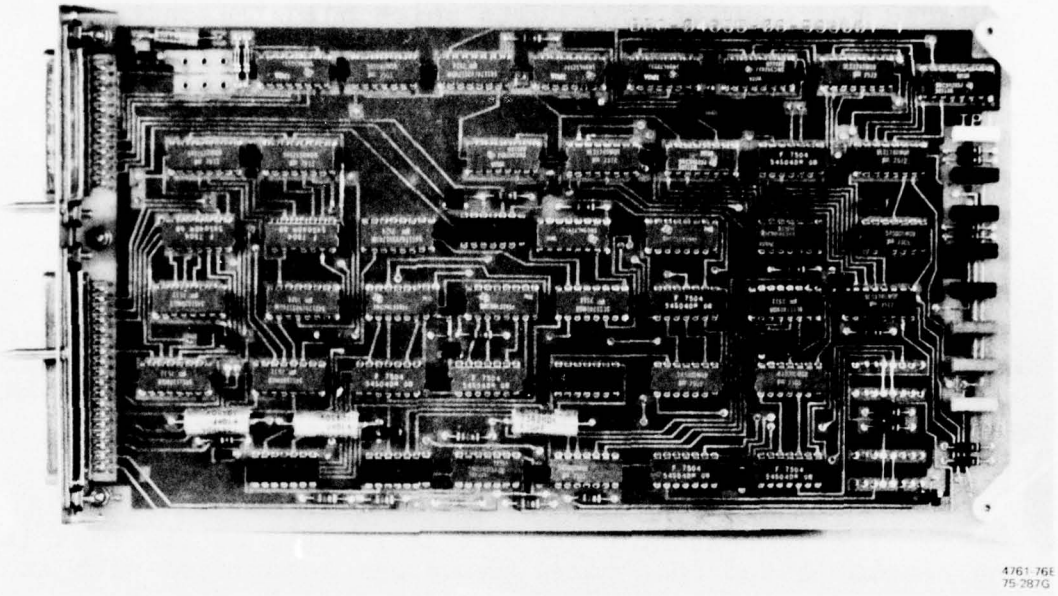
The power supply assembly is a simple structure made primarily of extruded angle aluminum. It is fitted with slides allowing it to move from the back to the front of the rack. The nest is hinged to the left front of the power supply assembly for maintenance in the closed position. The right side of the nest and power supply assembly are held together with five screws. The power supply assembly provides mounting for the five power supply modules. Each

A1	593014 PPM	593004 BGA	593005 BGB	593006 BGC	592973 BGD	592980 BGE	593024 ALS	593012 OWT	593013 OWQ	510232 FEI	593003 IFA	SPARE	510232 FEI	593003 IFA
A2	SPARE	593021 TDR	593019 TRG	593020 TDM	593065 DIG EXT	SPARE	593018 RFS	510235 FEA	510233 FEP	510233 FEP	510233 FEP	510233 FEP	510233 FEP	510233 FEP
A3	593023 VIO	593030 TTS		593029 TTF	593028 TTD	SPARE	593025 ASN	510234 FEE	510233 FEP	510233 FEP	510233 FEP	510233 FEP	510233 FEP	510233 FEP
A4	593007 DDD	593009 FSY	593016 RRG	593001 BEC NOT USED	593001 BEC NOT USED	593002 BES	593081 ABC	593088 RCF	510236 FED	510232 FEI	593003 IFA	593146 CDL	510232 FEI	593003 IFA
A5	593008 ERA	593001 BEC	593001 BEC	593001 BEC	593002 BES	593081 ABC	593026 OTG	SPARE	593017 RFI	593010 MBC	593069 RF EXT	593011 MRG	593040 MOD	593022 TSC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14

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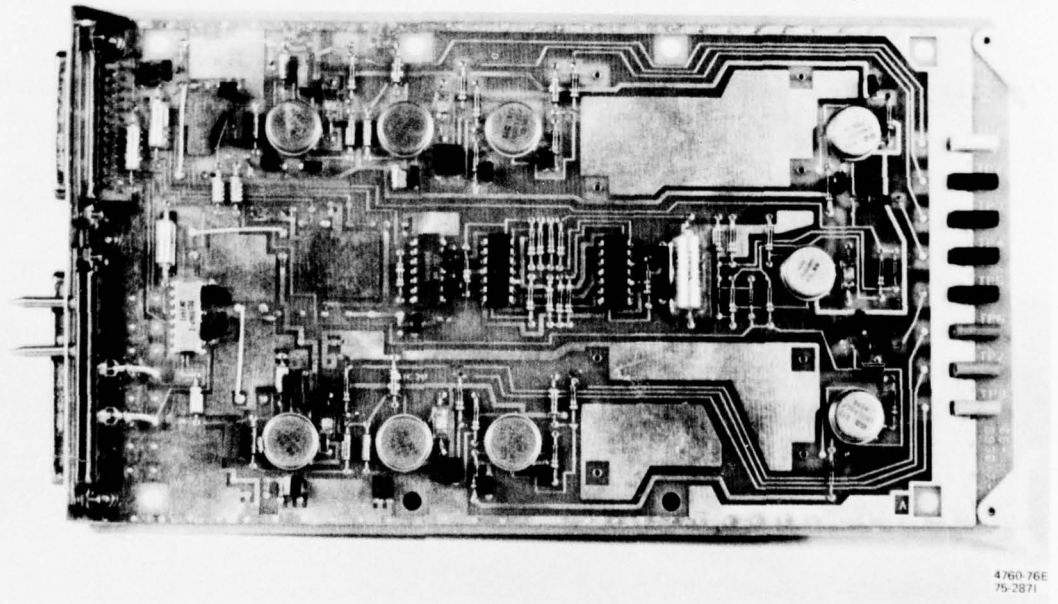
5049-76E

Figure 58. Card Location Chart



4761-76E
75-287G

Figure 59. Typical Digital Card



4760-76E
75-287I

Figure 60. Typical Analog Card (Cover Removed)

module is supplied with a "pigtail" terminated on a screw type terminal block. Thus, power supplies are readily replaced by removing four bolts which hold the units to the structure and disconnecting seven electrical connections.

OPERATIONAL/TEST PANEL

The Operational/Test Panel contains all operational and maintenance controls and indicators required to operate the modem. These functions are available from the front of the rack with the door closed. The rear of the panel can be accessed easily by removing the front panel screws and turning the panel down 90 degrees. The panel can be completely removed by disconnecting one multipin connector and removing five AC wires from a screw type terminal board. All components on the panel are supplied or fitted with EMI gasketing.

I/O ASSEMBLY

The I/O assembly located at the top of the rack is the removable top rack panel which has associated with it the exhaust air filter, 22 TNC video and IF connectors, one power connector, one multipin monitor connector, and the power line input filters. All connectors have dust covers permanently attached by chains and are mounted with EMI gasketing.

INTRA-RACK CABLING

The intra-rack cables consist of 22 video and IF cables from the I/O Panel to the nest/power supply assembly and two multiwire cables from the nest to the Operational/Maintenance Panel and the I/O Panel. The only other intra-rack wiring is blower power and AC power from the I/O Panel (line filter) to the Operational/Maintenance Panel.

SECTION 7

CONCLUSIONS AND RECOMMENDATIONS

GENERAL

The primary objective of the MDTS program was to design, develop and fabricate a modem to convert the DCS from analog to digital operation at megabit rates. This was accomplished. The specified performance was demonstrated by simulation on 8 Engineering Development Models and was further demonstrated during three months of field testing on the Youngstown-Verona, N.Y. test range. Additionally, it was demonstrated that the MDTS could operate in the presence of aircraft in the common volume. The Adaptive Feedback Equalization technique was shown to be a most desirable method of meeting the requirements of the USAECOM specification EL-CPO144-0001B.

Conclusions and recommendations are now made pertaining to the following areas:

a. Breadboard Modifications
b. Factory Tests
c. Performance Tests
d. CONUS Tests
e. Reliability
f. BITE
g. Parts and Processes
h. Hardware Packaging
i. Performance Improvement
j. AN/GRC-143 Test Program.

Breadboard Modifications

The MDTS dual diversity breadboard was tested by RADC at Rome, N.Y. using their Quad Space Diversity Test Simulator (QSDS). As part of this test series the modem was operated in a non-diversity mode. In this mode the BER performance was found to limit at BER values greater than expected, particularly at large values of Doppler spread (5-10 Hz). It was subsequently found that this condition was caused by insufficient dynamic range and non-optimum loop time constants. The breadboard was modified to increase the dynamic range and several loop time constants were altered. The modem was then retested showing an improvement of many orders of magnitude in BER Performance. These changes were

not incorporated into the Engineering Development Models because they were not necessary for quad diversity operation. Additionally, cost and schedule would not permit their incorporation at that time.

These tests clearly demonstrated that the decision feedback equalizer could also be applied to low data rate (< 3 Mb/s) tactical operations with excellent results.

GTE Sylvania has recommended that further analysis be done in that area and the results of this analysis be incorporated into only future production. At the present time, GTE Sylvania is under contract to design, build, and retrofit four of eight modems prior to OCONUS tests presently scheduled for January, 1977 as part of a Performance Improvement Task (PIT). This work is scheduled to be completed by mid-September 1976.

Factory Tests

The MDTS factory tests results are summarized below:

a. Environmental tests - The MDTS successfully passed the sand and dust, fungus, shock, vibration and altitude tests without any visible degradation in performance. Some performance problems were encountered at the extreme limits of the temperature tests. However, no permanent damage was detected after the system was returned to room temperature. The humidity tests resulted in some connector problems due to minor corrosion as well as some deformation of plastic parts.

b. EMI tests - The MDTS conformed to the specified EMI standards.

c. Operational Reliability - MTBF of 2500 hours exceeded.

d. Maintainability - M_{ct} and M_{acxt} specifications were met.

e. Human engineering - The MDTS was found to be suitably operable.

Performance Tests

The simulated performance test results agreed quite favorably with the theoretical performance predictions derived from analytic models and clearly demonstrate the multipath handling capability derived from the Adaptive Equalization Technique, and the bandwidth efficiency of the MDTS 4-PSK system. The calculated and measured data compares well at all data rates except for extreme multipath conditions under dual diversity operation. The poorer dual diversity performance under extreme multipath conditions was probably due to incomplete removal of past intersymbol interference resulting from insufficient dynamic range in the backward filter or saturation effects in the forward filter. The mathematical model assumed total removal of intersymbol interference and infinite dynamic range in the forward filter. These problems are currently being addressed under an awarded performance improvement task (PIT). A considerable amount of data was taken for extremely long DCA links with severe multipath profiles. The data showed the modem performed satisfactorily over these links within the performance limitations set by the three tap forward filter and backward filter dynamic range.

CONUS Tests

The series of tests conducted over the Youngstown-Verona, N.Y. test range demonstrated the ability of the MDTS to operate successfully over an actual troposcatter link. The collected data were shown to compare very well with calculated results. In addition, it was demonstrated that the MDTS can operate in the presence of aircraft in the common volume. Bit synchronization was lost only infrequently and then only under severe multipath situations or poor signal to noise ratios where the BER was greater than 10^{-2}. A system test of the MDTS, AN/GSC-24 and TD-968 multiplexers on the test link verified the capability of the modem in a digital transmission system equivalent to that used on the DCS.

Reliability

Specification EL-CP0144-001B required that the modem have an MTBF of 2500 hours when operated at an ambient operating temperature of 25 degrees C $\pm$ 5 degrees C, fixed ground environment, continuous duty cycle. The calculated MTBF at 40 degrees C is 2529 hours for a dual diversity modem. The 16,000-hour reliability demonstration showed a

quad diversity modem having 2677 hours MTBF. There are design changes that would be economically feasible in production which could substantially increase the MTBF. These changes are being addressed as part of the Performance Improvement task.

BITE

The built-in-test-equipment (BITE), as presently configured, seems to be quite effective in detecting faults in either the on-line or off-line modes. A successful maintainability demonstration was run using the BITE for fault isolation and all MTTR requirements were met. However, several areas for improving BITE performance exist and should be evaluated. These include:

a. Re-evaluation of the on-line BITE scan sequence - The order in which the cards are scanned could be revised to decrease the probability of displaying a fault indication resulting from a fault on a card other than the one displayed on the fault module indicators. The revision could be accomplished with some simple back plane wiring changes.

b. Advance function - The on-line BITE contains a function that allows the operator to advance the scanner to the next detectable fault by pressing the ADVANCE button on the control panel. To date, the use of this function as an added diagnostic aid has not been investigated in any detail. Further investigation in this area could lead to improvements in on-line fault detection capability.

c. Off-line test duration - At present, each off-line test takes 20 seconds to run. This duration is based on the test requiring the longest time to run. Selecting this duration to run all tests simplified off-line BITE circuit design. However, many of the tests could be run in a much shorter period. Modifying the off-line BITE timing to optimize individual test durations should be studied to see if test durations can be reduced.

d. A test re-evaluation - The forward equalizer tests (off-line tests 6,7,8,9) should be reviewed. Re-design in this area could make the four tests more effective in isolating a fault to a particular AFE card.

e. Off-line test automation - The off-line test procedure could be automated to simplify operation and reduce operator attendance requirements.

Parts and Processes

During the fabrication, assembly and test phases of the program, some parts and processes were found to be less than desirable from either a reliability or a manufacturability consideration. The following are items that should be changed prior to any follow-on production.

a. RF Connector, GTE Sylvania Part No. 72-509792 - 1 and 2 - This RF Connector set used on the RF printed circuit cards was found to have an unreliable ground connection. The parts are manufactured by Cannon Electric Co. (DM53740-5001 and DM53742-5001) and others. The apparent problem is due to tolerances between mating pairs and ground spring tension of the socket. It is recommended that a replacement connector be investigated before further production.

b. Summers and Splitters, GTE Sylvania Part No. 03-510237-1 and 03-510238-1 - These units were designed with connector centerline spacing which was too small for some TNC connector manufacturers. The spacing should be enlarged slightly to allow the use on any qualified TNC connector manufacturer.

c. RF Cables, GTE Sylvania Part No. 09-592887 - Some of these interconnecting cables in the nest should be lengthened to provide easier assembly and reduce bend radii.

d. Indicator Lamps - The use of LED indicator lamps should be allowed to reduce the current drain in the power supplies, improve reliability, and reduce heat loss.

e. Captive Nuts - The captive nuts supplied by the rack manufacturer should be replaced by more reliable units.

f. Power Supplies, GTE Sylvania Part No. 28-509917-1 and 2 and 28-509919-1 and 2 and associated overvoltage protector - For reasons of cost, the power supplies were high quality off-the-shelf sealed units with relatively low efficiency. These units could be replaced by a

single replaceable module with much greater efficiency if the non-recurring costs are prorated over production quantities. Such a change would also eliminate some of the circuit breakers. A single power supply module would greatly increase reliability (MTBF) by virtue of fewer electrical components and MTTR would be decreased since only replaceable cards need be changed in most instances instead of the entire sealed power supply. A major size and weight reduction would also be gained.

Hardware Packaging

The racks in which the MDTS is presently packaged was chosen to minimize cost and allow room for expansion. This was an engineering development program. The possibility of change due to changes in equalizer algorithms and to a better understanding of the implementation requirements on the program suggested that allowances be made for expansion. In addition, the strategic troposcatter requirements changed and at this time are still somewhat fluid. With the package as shown one could easily adapt to changes and, in fact, most future changes can be easily retrofitted into the existing units.

The MDTS specification required that good design practices be used to minimize weight and size without specific limits. This was accomplished.

For new procurements, the rack structure can be replaced by a single 15 3/4 inch high relay rack mounted assembly with a separate 7 inch power supply drawer. A dual diversity modem could have the power supply located within the 14 inch high modem. Packaging density would be somewhat dependent on the number of data rates, complexity of interfaces and complexity of BITE and Quality Monitors in any future requirement.

Performance Improvement Task

As with any techniques program such as MDTS there are a certain number of improvements, either performance or cost, that can be made as a result of the test programs. GTE Sylvania has been under contract to conduct studies and incorporate certain recommendations into the equipment. This effort is collectively called a Performance Improvement Task. It consists of two phases. Phase I consists of study, design, fabrication, assembly and test tasks that result in the delivery of four improved MDTS modems. Delivery of these modified units is time-phased to the requirements of the OCONUS Test Program scheduled for January, 1977. Phase II is a nine-month study to reduce cost and provide design recommendation based on future operational requirements. Phase II is to be completed by July 1977.

These tasks are summarized below.

Task I-1 - Doppler spread and dynamic range study - These are analytical studies to verify and detail the design parameters based on the work done on the breadboard during the Breadboard Tests at RADC, Rome, N.Y. This task is complete.

Task I-2 - This task consists of implementing changes as a result of Task I-1 into four of the eight modems. This task includes changes to the IF Amplifier to incorporate a 1/4 baud matched filter at 70 MHz, changes in the dynamics of both the forward and backward filters, and gain changes in the baseband finite integrator.

Task I-3 - Improve the AGC tracking and manufacturability of the IF amplifiers. With the increasing availability of hybrid microwave amplifiers and attenuators, it has become desirable to change the design of this IF amplifier to simplify test and check-out and obtain improved performance characteristics, in particular, AGC tracking between amplifiers.

Task II-1 - Study the effect on cost to reduce the environmental requirements to be more consistent to intended usage.

Task II-2 - Evaluate the selection and use of components on cost and reliability in production quantities.

Task II-3 - Study and propose an MDTS implementation that would be required to meet Mean-Time-Between-Outages (MTBO) of 25,000, 50,000 and 100,000 hours.

Task II-4 - Conduct a trade-off study to evaluate the usefulness of BITE compared to the added cost and complexity in various operational situations.

AN/GRC-143 Test Program

The test program and test results discussed in Appendix A show conclusively that the MDTS with adaptive decision feedback equalization can be used to upgrade the performance of existing AN/GRC-143 radio equipment in both performance and data rate capability for tactical troposcatter communications.

SECTION 8

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APPENDIX A

FIELD TESTING OF THE MDTS BREADBOARD WITH THE AN/GRC-143 RADIO EQUIPMENT

Abstract

A field test program was conducted to quantitatively determine the performance of the Army tactical troposcatter radio equipment, AN/GRC-143 when interfaced with breadboard model of the Megabit Digital Troposcatter Subsystem (MDTS). The MDTS increased the bit rate capability of the AN/GRC-143 from 1 Mb/s to 3 Mb/s. This report contains Bit Error Rate (BER) and received signal level information gathered from operational tests conducted over the Army's Tobyhanna Army Depot to Fort Monmouth, NJ troposcatter test path. The tests are described in detail and the test results are presented.

Purpose

This field test program was conducted by Comm/ADP Laboratory, (CADPL) in support of Project Manager (PM) - MSCS. The purpose of the program was three-fold.

a. Demonstration of the feasibility of interfacing the MDTS, with the Army tactical troposcatter radio equipment, AN/GRC-143.

b. Demonstration of the capability of extending the data rate of the AN/GRC-143 from nominally 1 Mb/s to 3 Mb/s.

c. Determination of expected tactical Bit Error Rate (BER) performance over an actual troposcatter link utilizing approximtely TRI-TAC data rates.

Description

Path

The troposcatter test path used for this program was located between Tobyhanna Army Depot, Tobyhanna, Pennsylvania and the Hexagon Building, Fort Monmouth, New Jersey; a distance of approximately 94 statute miles over relatively hilly terrain. The path profile for this test link is shown in Figure 61 and indicates a scatter angle of 0.67 degrees. In the testing, the link was operated with the transmitting site located at Tobyhanna and the receive site located in the Hexagon building.

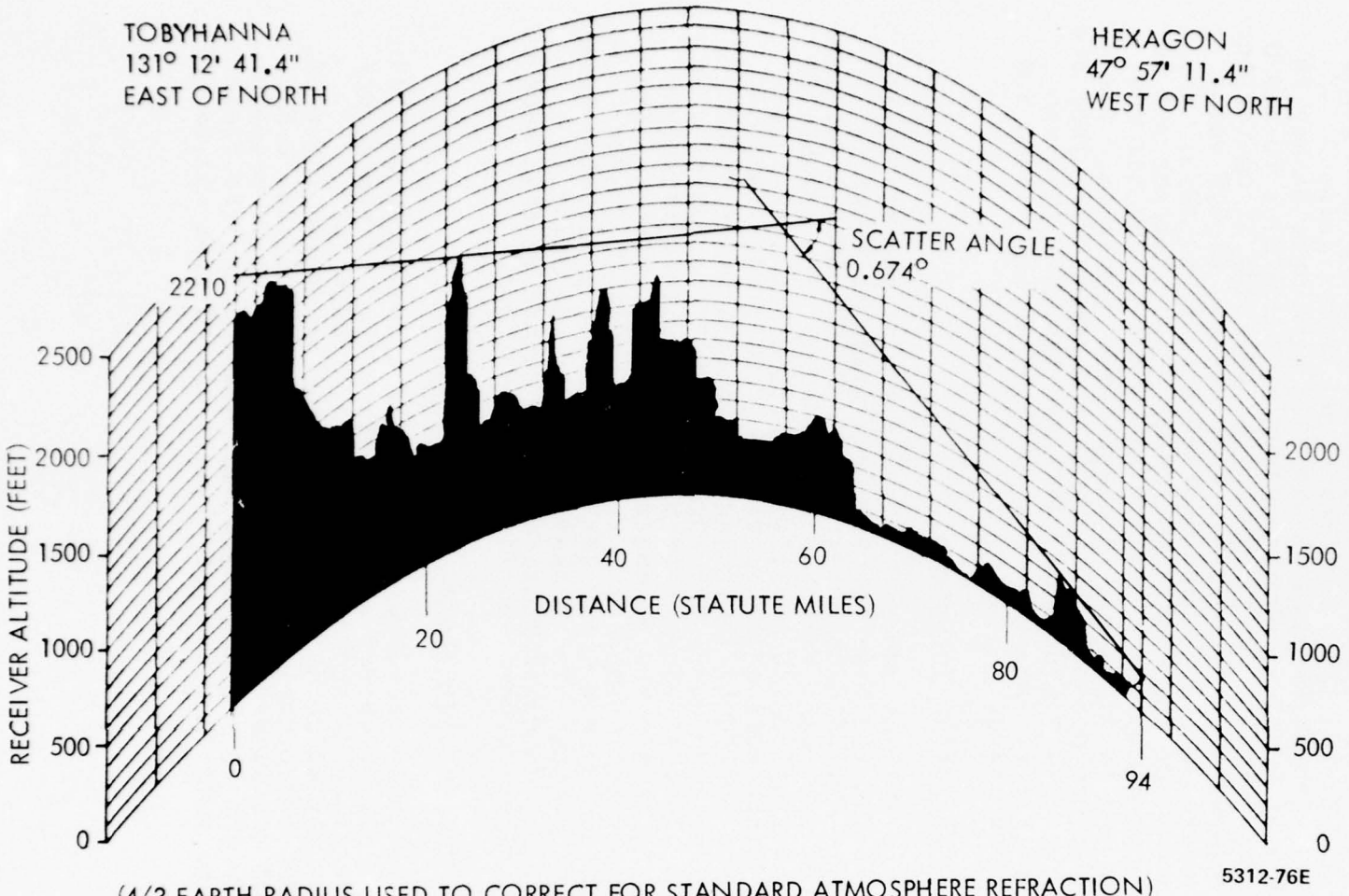


Figure 61. Path Profile for Test Link

Radio Equipment Description

The radio equipment utilized during the test program was the AN/GRC-143 Army tactical troposcatter radio equipment. The AN/GRC-143 in standard form uses binary FM modulation of PCM data obtained from a TD-352/U or TD-660/U multiplexer. In the 12-PCM voice channel mode of operation, the throughput data rate is 576 Kb/s and for 24 PCM voice channel operation, the throughput rate is 1.152 Mb/s. The nominal range of the radio equipment (which utilizes a 1 kW klystron power amplifier) is 100 miles for 12-channel PCM operation and 80 miles for 24 channel PCM operation. The basic radio set consists of three equipment racks. They are the transmitter, the dual receiver and the 1-kW klystron power amplifier. The radio set operated in the 4.4 to 5.0 GHz frequency range.

Transmitter Interface

The MDTS breadboard interfaces with the AN/GRC-143 transmitter at the mixer/upconverter stage as shown in Figure 62. The MDTS breadboard has a 70-MHz QPSK modulated output for interface with radio equipment. The AN/GRC-143 transmitter uses a 150-MHz mixer amplifier to introduce modulated information to the carrier. This interface problem was solved by replacing the 150-MHz mixer with a 70-MHz mixer. However, the MDTS can easily be modified to utilize a 150-MHz transmit IF to eliminate this interface problem and retain the standard GRC-143 transmitter. The mixer/upconverter translates the QPSK modulated 70-MHz signal up to the 4.4 - 5.0 GHz band by mixing with the local oscillator output. The C band output of the mixer is amplified and bandpass filtered. The signal is then sent to the 1-kW klystron power amplifier and antenna.

Receiver Interface

The MDTS breadboard interfaced with the AN/GRC-143 dual diversity receiver at the 70-MHz output of the mixer/amplifier stage as shown in Figure 63. There is approximately 40 dB of gain between the waveguide input of the AN/GRC-143 preselector bandpass filter and the 70-MHz output of the mixer/amplifier. Thus with receive signals from -100 dBm to -60 dBm (typically seen during the field tests) the MDTS 70-MHz input signals varied from -60 to -20 dBm.

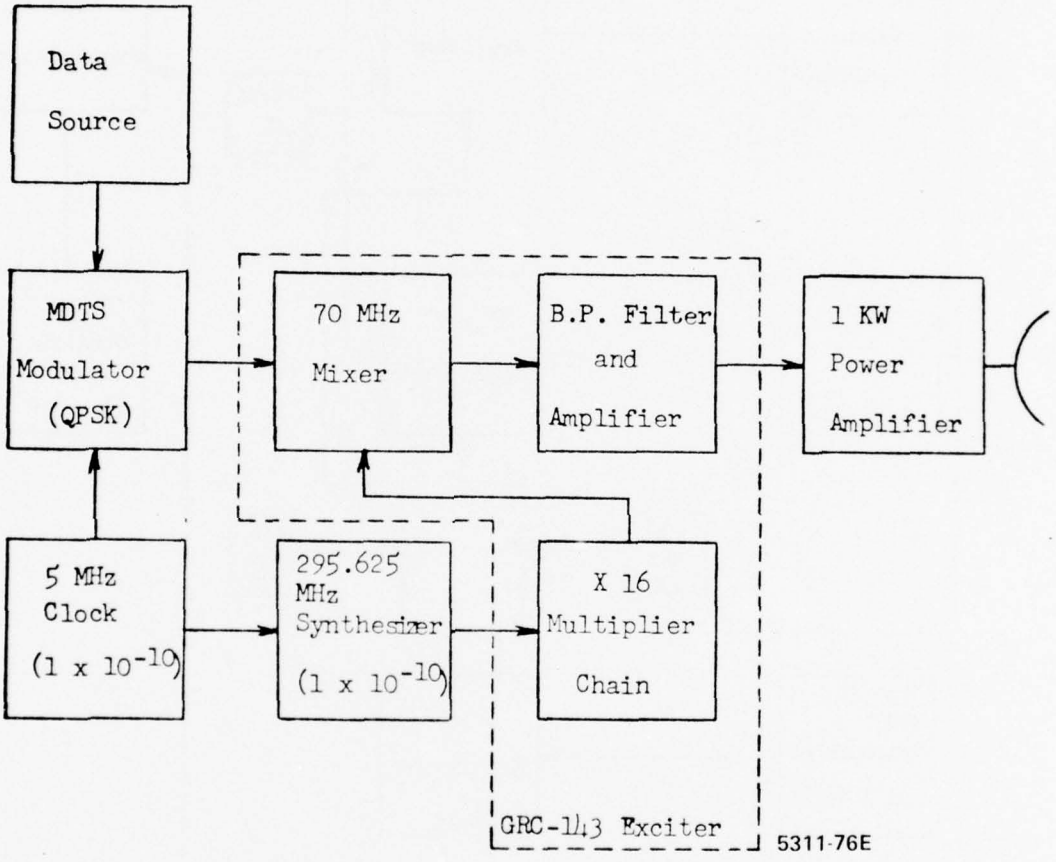


Figure 62. MDTS Interface Diagram Transmitter

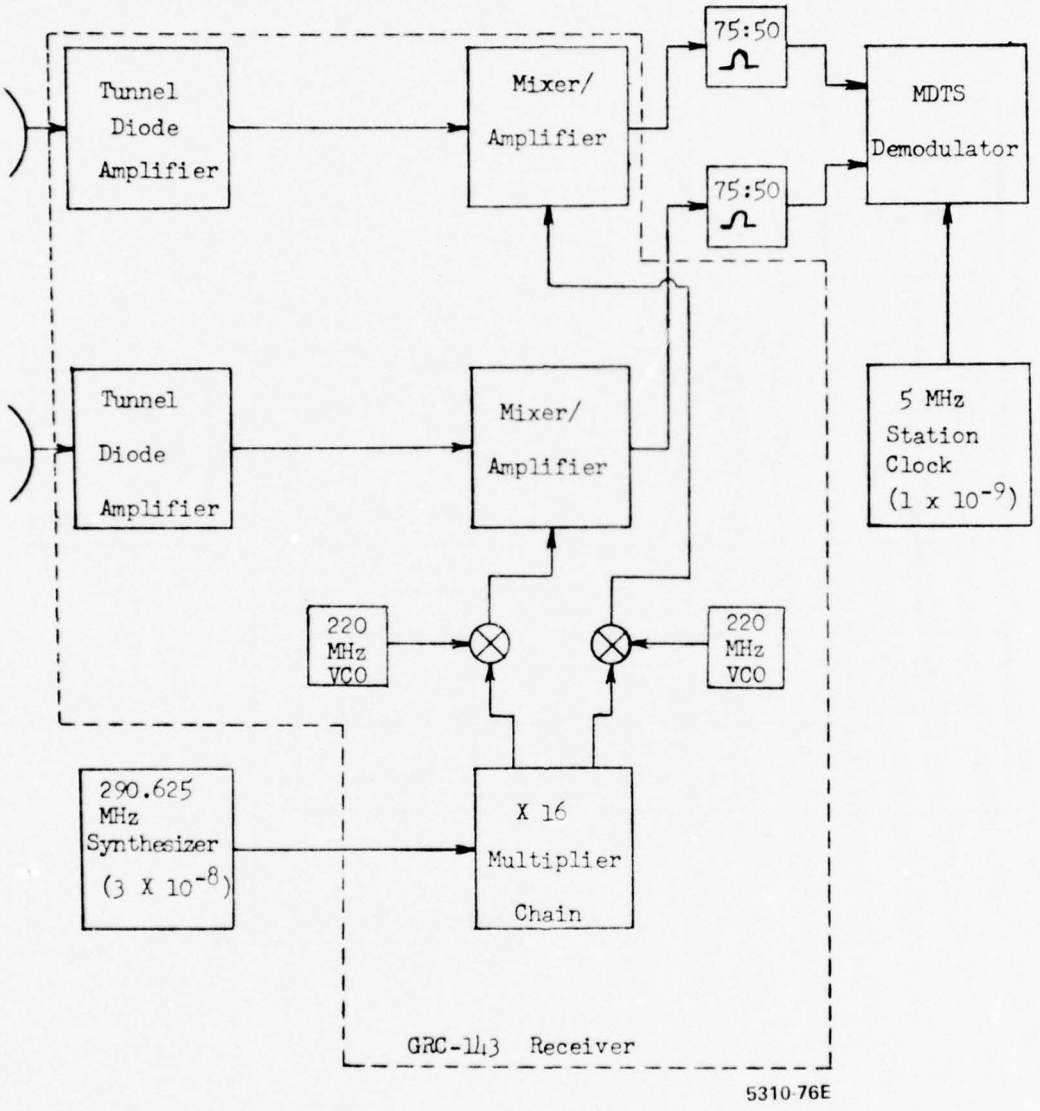


Figure 63. MDTS Interface Diagram Receiver

Instrumentation

The instrumentation and equipment block diagram for average receive signal level, RSL, and average bit error rate, BER, measurements are shown in Figure 64. The 70-MHz output of each receiver in the AN/GRC-143 are coupled together through 15-dB directional couplers. This combined signal is sent to a log linear amplifier (LLA) and detector. The DC voltage output from the detector is a function of RSL and is used as the frequency control voltage for a voltage controlled oscillator (VCO). The output frequency of the VCO is counted on a digital counter for 10-second periods and is printed by a digital printer. These 10-second printouts are then arithmetically averaged for the 20-minute run and the RSL corresponding to that frequency is read off a calibration chart.

A second LLA provides a DC voltage proportional to RSL for a strip chart recorder. The strip chart is used to document the tropo channel behavior such as fade rate, fade depth and aircraft in the common volume.

Data Collection Procedure

Tests were conducted on a one way troposcatter radio circuit operating at an RF frequency of 4800-MHz with the transmitting site located at Tobyhanna Army Depot, Tobyhanna, Pennsylvania. The receiving site and instrumentation were located in the Hexagon Building at Fort Monmouth, N.J. Data was collected from 26 February 1976 to 6 April 1976, each data test having a minimum duration of 20 minutes.

A system warm-up time of thirty (30) minutes was required to insure stability of both the RF equipment and test instrumentation. After the required warm-up period, the received signal level recording oscillator and the strip chart recorder were calibrated through the AN/GRC-143 receivers. A coaxial power divider was used at the output of a Hewlett Packard model 618B signal generator to enable simultaneous calibration of both receivers on the strip chart recorder.

After calibration, the data correlator used to determine bit error rate was initiated and synchronized with the incoming pseudo random data stream. Errors were counted and accumulated on the average BER error counter. Simultaneously, the received signal level information was

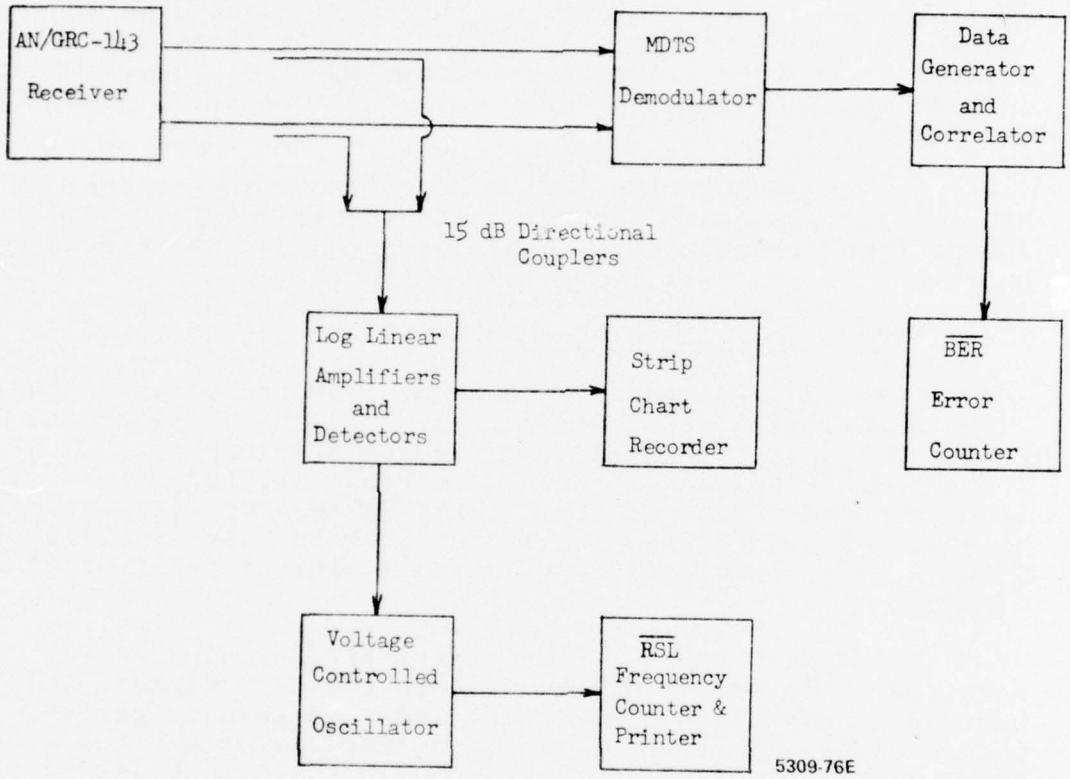


Figure 64. Data Collection Instrumentation

recorded on both the Sanborn Strip Chart recorder for a visual display of the data and on a frequency deviation counter with 10-second printouts to obtain a quantitative measure of the received signal level average.

Data Reduction

The data collected was reduced in two steps. First, the average frequency count of the deviated oscillators was calculated from the digital counter printouts. This average frequency count was then converted to an equivalent average received signal level (RSL) by comparison to a calibration curve. Secondly, the total number of bit errors was divided by the total number of bits sent during the data test thus yielding the average bit error rate for that run. The bit error rate versus received signal level for that run are then plotted on a graph as a sample point. The composite of all the reduced data points yields the bit error rate performance of the MDTS and is compared to the theoretical limits.

Test Results

The reduced data for dual diversity reception is depicted in Figure 65. Data was collected at 3.088 Mb/s and each point represents a minimum 20-minute data run. It can clearly be seen that the resultant BER performance approaches theoretical limits and that its performance exceeds any previously recorded tactical data collected over an operational link. This previously collected test data indicated the occurrence of an irreducible error rate at approximately 10^{-5} for 1-Mb/s transmission over paths of 100 miles. The reduced data in Figure 65 clearly shows operation to 10^{-8} at 3-Mb/s transmission without indication of an irreducible error rate. The results are that higher data rates can be employed with satisfactory performance requirements being met.

Additionally, non-diversity tests were performed and the results are shown in Figure 66. Again theoretical limits are approached. It should be noted that the expected degradation of performance occurred when going from dual to single channel operation. Of prime importance is the fact that during the entire test program, loss of synchronization did not occur.

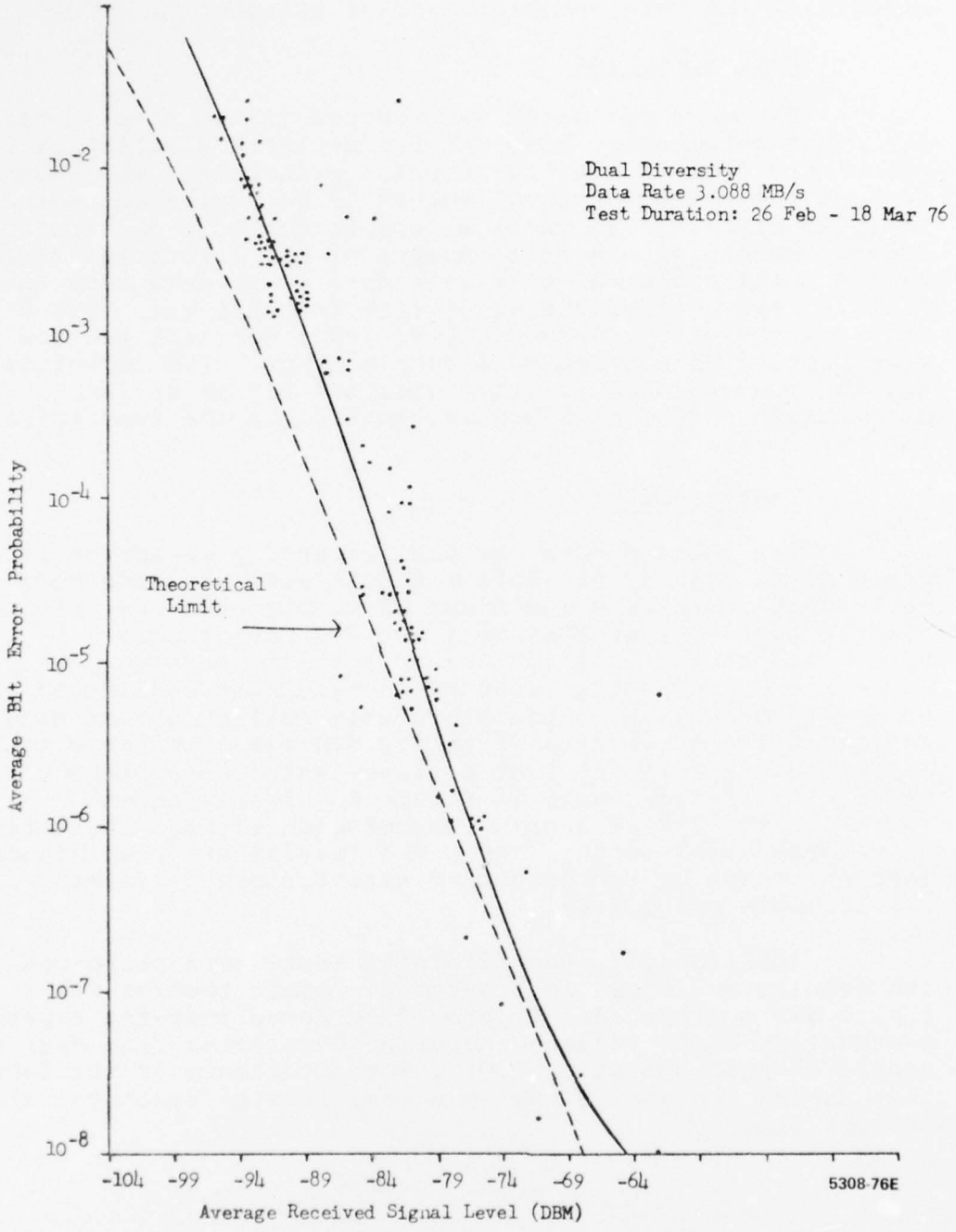


Figure 65. MDTS Breadboard Field Test Data

recorded on both the Sanborn Strip Chart recorder for a visual display of the data and on a frequency deviation counter with 10-second printouts to obtain a quantitative measure of the received signal level average.

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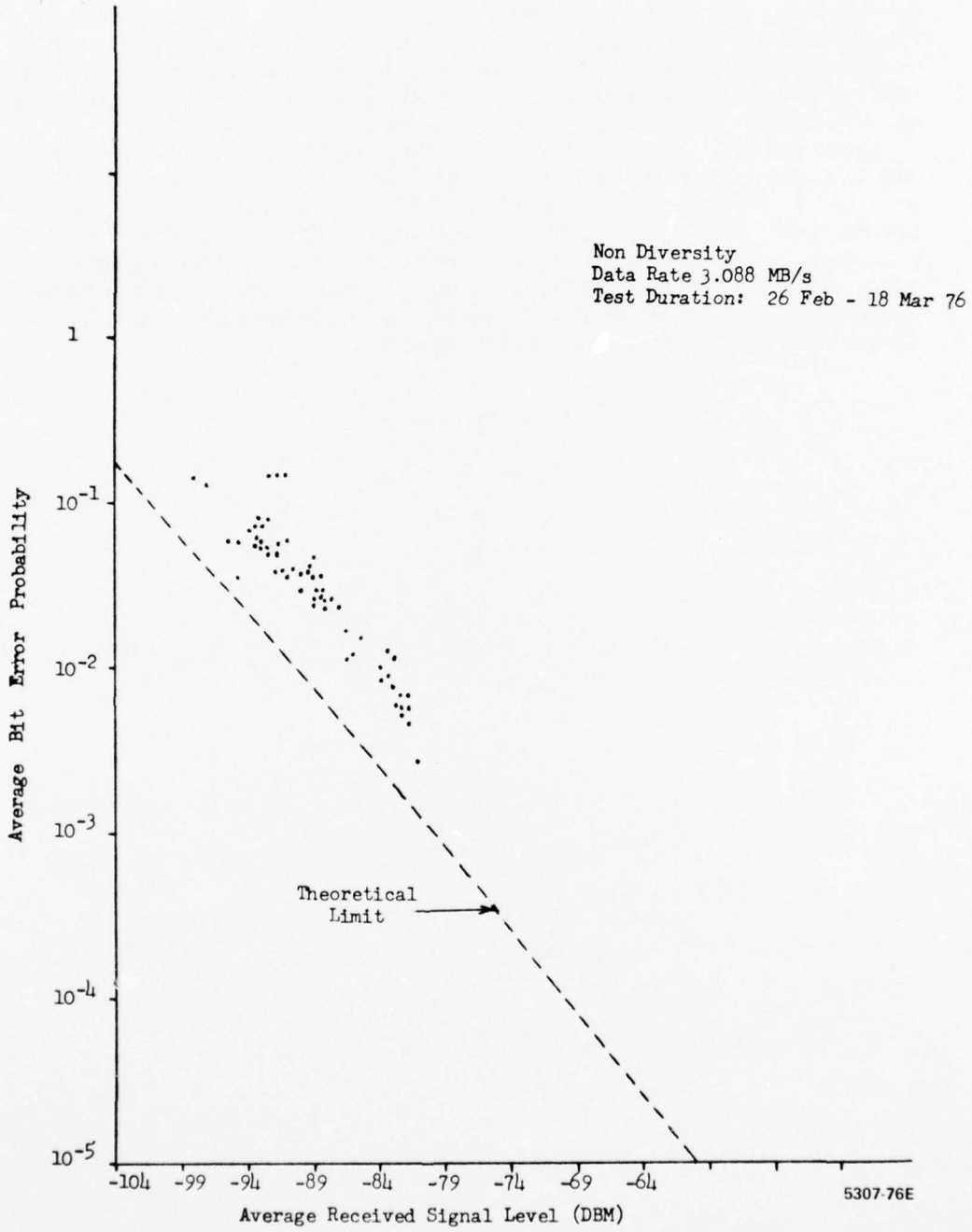


Figure 66. MDTS Breadboard Field Test Data

Conclusions

The purpose of the test program conducted over the tactical troposcatter test link by CADPL in support of PM-MSCS was completely fulfilled. The feasibility of extending the data rate capability of the AN/GRC-143 from its present limitation of 576 Kb/s at 100 miles and 1 Mb/s at 80 miles to at least 3 Mb/s has been clearly demonstrated. Thus with the MDTS modem, the AN/GRC-143 can easily meet the 2.048-Mb/s bit rate requirement of TRI-TAC or the 2.3-Mb/s signals of ATACS. All data tests were conducted at 3.088-Mb/s throughput data rate over the nominal 100-mile troposcatter test link. The test results clearly show that satisfactory performance at bit rates in excess of the current 2.3 megabit requirement can be obtained utilizing the MDTS modem.

APPENDIX B

QUADRUPLE SPACE DIVERSITY TEST SIMULATOR

(QSDTS)

QUADRUPLE SPACE DIVERSITY TEST SIMULATOR

GENERAL

The Quadruple Space Diversity Test Simulator (QSDTS) provides accurate and repeatable simulation of multipath effects over a range of signal to noise ratios typical of troposcatter communications links. This versatile laboratory instrument is the Signatron Model S-139C. Figure 67 is a photograph of the unit. The Simulator is designed to be used between modem equipment operating at an IF frequency of 70 MHz and having a signal bandwidth up to 15 MHz.

The S-139C simulator generates four complex statistically independent multipath signal channels representative of the four diversity channels encountered in quad diversity troposcatter communication systems. Each multipath channel is composed of sixteen statistically independent channels having a total delay spread of 1.0 microsecond and a relative amplitude adjustable over a 60-dB range.

The rms bandwidth of the multipath channel phase and gain variations (fading rate) are adjustable as are the levels of each diversity output.

The "noise" voltages used to cause the random gain and phase fluctuations of the multipath channels are generated digitally. As a result they can be stopped or "frozen" or reset to a known starting point so that truly reproducible channels are simulated.

The S-139C simulator includes separate precision thermal noise sources on each diversity output to simulate the additive noise effects of receiver front end circuits and received background noise.

Additionally, a built-in test system is provided to facilitate rapid and accurate equipment setup, calibration, and maintenance.

TROPOSCATTER CHANNEL SIMULATION THEORY AND PARAMETERS

It has been shown that the troposcatter channel can be modeled as a linear time-varying channel whose average multipath properties are given by the delay power profile or power impulse response while the average fluctuation

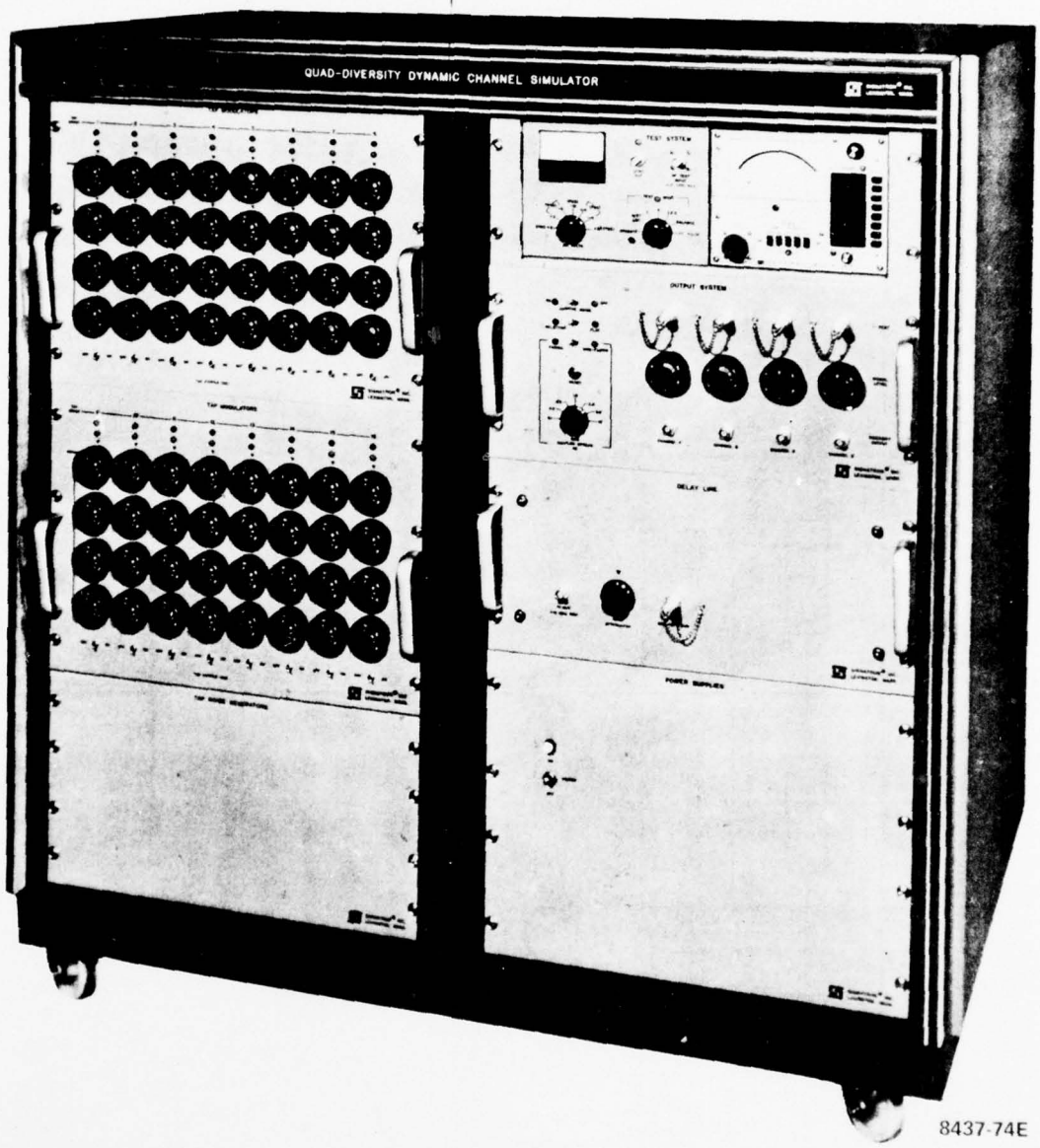


Figure 67. Quadruple Space Diversity Test Simulator (QSDTS)

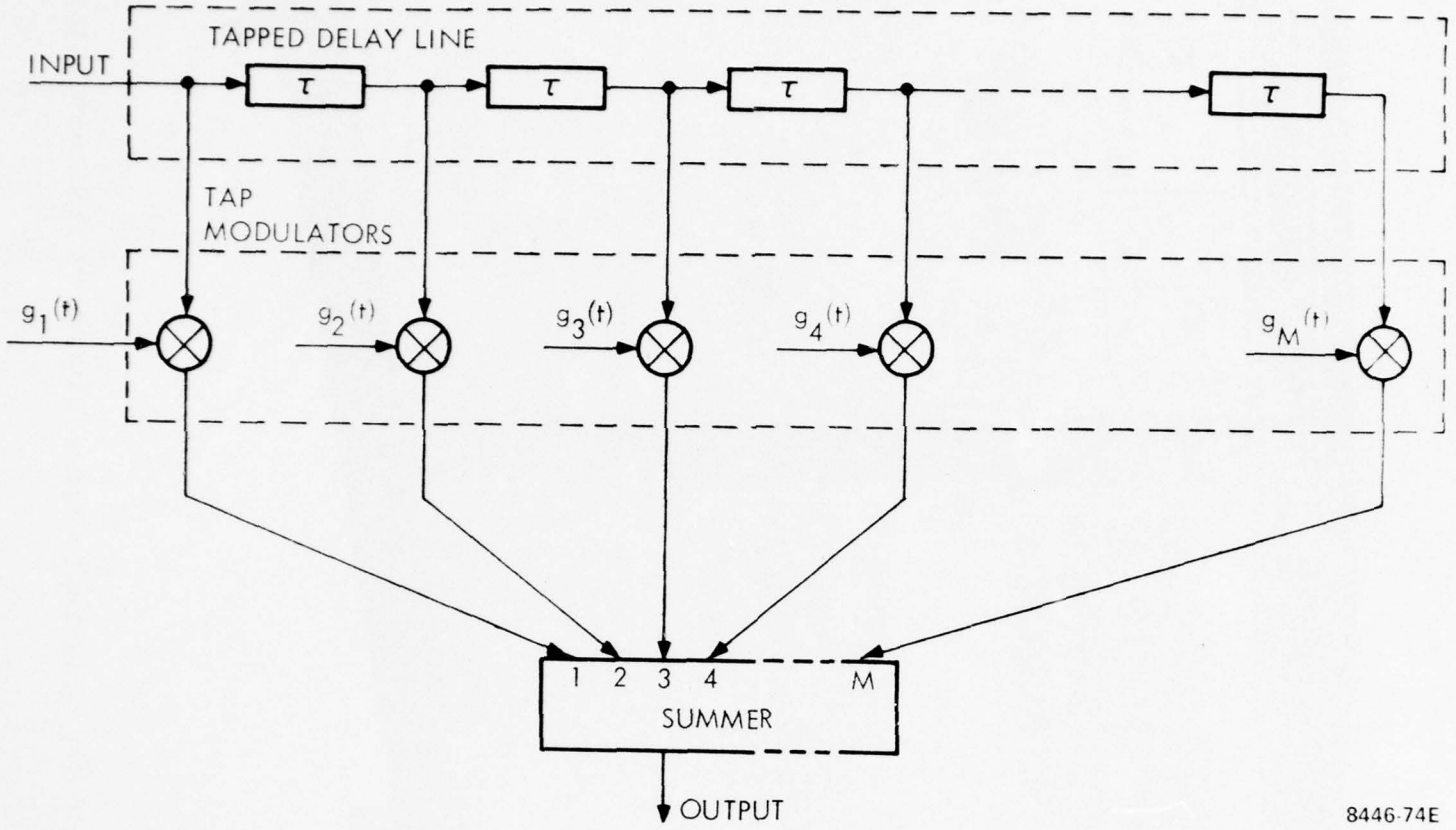


Figure 68. QSDTS Delay Structure

properties are characterized by the rms Doppler spread. The delay power profile may span as much as one microsecond of delay and the Doppler spread may range from 0.1 to 10 Hz.

Many theoretical studies, e.g., Kailath (1961)[6], Stein (1956)[7], Bello, Ehrman, Crystal (1967)[8], have shown that troposcatter channels can be simulated by a tapped delay line structure such as is shown in Figure 68. The delay line is tapped at intervals of = 1/W, where W is the bandwidth of the input signal. The output of tap n is multiplied by a complex Gaussian random process, $g_n(t)$, which has the correlation properties

$$\overline{g^*_n(t)g_m(t)} = \begin{cases} 0 & m \neq n \\ \frac{1}{W} Q\left(\frac{n}{W}\right) & ; \quad m = n \end{cases}$$

where Q(n/W) is the delay power profile of the channel. Thus, the tap gains are uncorrelated Gaussian random processes, with variances proportional to the delay power profile evaluated at the tap position, i.e., Q(n/W). The simulator output is the sum of all of the multiplier outputs. The delay line tap spacing must be 67 nanoseconds to correctly simulate a channel for a 15-MHz bandwidth signal. A 16 tap design with 67-nanosecond spacing provides the capability of simulating paths whose power impulse responses span a maximum of 1.0 microsecond. In order to simulate the expected range of fade rates found on troposcatter links, the rms Doppler spread should cover the range 0.1 to 10 Hz.

PERFORMANCE SPECIFICATIONS

The Performance Specifications for the Signatron Quadruple Space Diversity Test Simulator Model S-139C are defined herein.

Operating Modes	Fading, Frequency Selective
	Fading, Flat
	Nonfading, Frequency Selective
	Nonfading, Flat

Input

Modulation	FM, PM, FSK, FDM/FM, PSK, TDM-FSK/PSK
Center Frequency	70 MHz
Signal Level Minimum	0 dBm
Signal Level Maximum	+ 10 dBm
Impedance	50 ohms

Multipath Tapped Delay Line Path Model

Signal Bandwidth for valid simulation	15 MHz maximum
Number of taps	16
Delay between taps	67 Nanoseconds
Total delay	1.0 microsecond

Tap Modulator Group

Number of tap modulator groups	16
Tap modulators per group	4
Tap gain level control	60-dB range in 1-dB steps (separate on/off switch)
Feedthrough unbalance	35-dB down minimum
Modulator linearity	2 percent minimum

Tap Modulation Generator

Number of independent generators	128 (8 for each tap modulator group)
RMS Doppler Spread	Switch selectable, 0.1, 0.2, 0.5, 1, 2, 5, 10 Hz
Modulation power spectrum	Second-order Butterworth

Output

Number of independent diversity outputs	4
Center frequency	70 MHz
Signal level (front panel controller any single tap modulator group operating, all others off)	-20 dBm maximum to -70 dBm minimum
Signal bandwidth	15 MHz minimum
Signal-to-equipment-noise ratio, 15-MHz bandwidth, Additive noise off	45 dB minimum at -30 dBm output
Internal additive noise source	-70 dBm/MHz, factor set
Impedance	50 ohms

Built-In Test Functions

Selectable inputs to modulator	I on, Q off I off, Q on I on, Q on I off, Q off (Balance)
RF power measurement	(Specification per General Microwave Model 460B power meter, N240C power head)
Internal test signal generator	70 MHz CW and 80 nanoseconds RF pulse, crystal controlled
AC Power Input	115 Vac 50-60 cycle, 6.7 amps
Cabinet Dimensions	Height 50 inches, Width 44 inches, Depth 30 inches
Weight	400 lbs.

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