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A PROGRAMMABLE SIGNAL PROCESSOR FOR THE EXPERIMENTAL ARRAY RADA--ETC(U)
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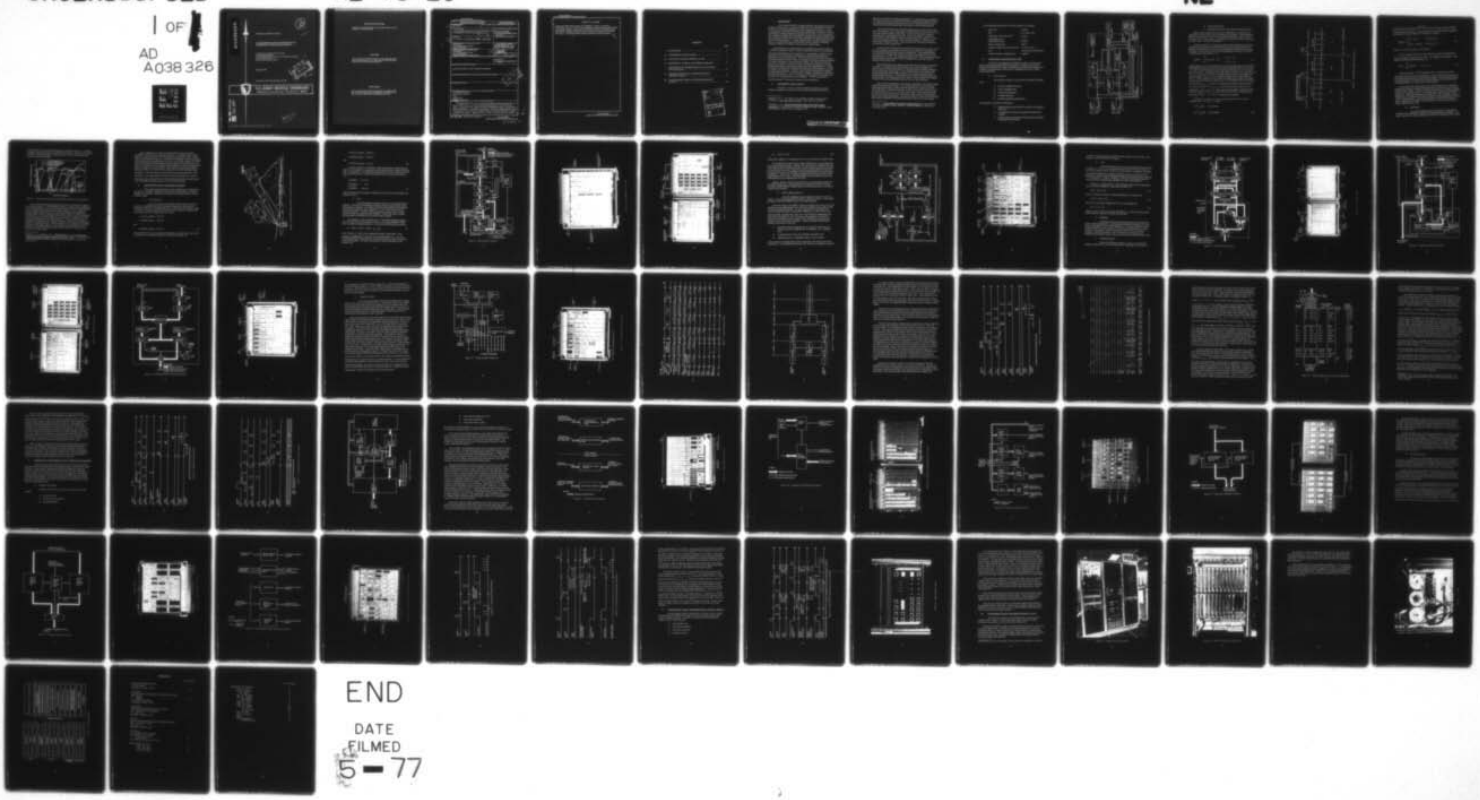

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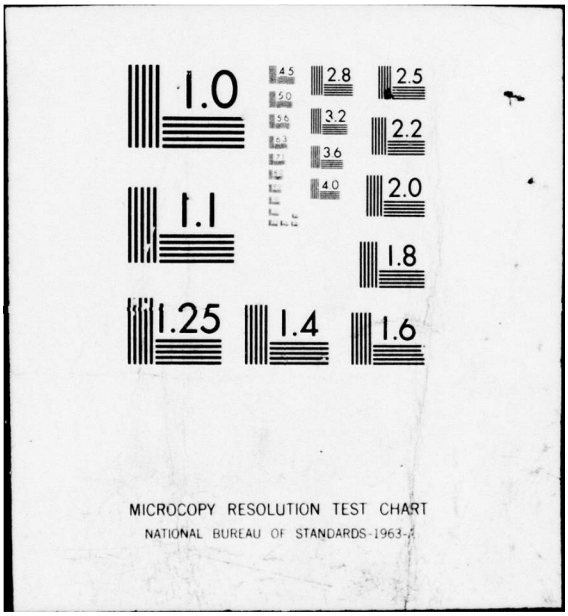
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TECHNICAL REPORT RE-76-20

A PROGRAMMABLE SIGNAL PROCESSOR FOR THE EXPERIMENTAL ARRAY RADAR (VOLUME I)

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February 1976

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A detailed description of the programmable signal processor developed for use in the US Army Missile Command experimental array radar is presented in this report. The programmable signal processor has quadrature channel, moving target indicators followed by post detection integration. The moving target indicators can be programmed to have any desired frequency response and can be adapted as a function of antenna beam position, range bin sector, or time. The processor also contains

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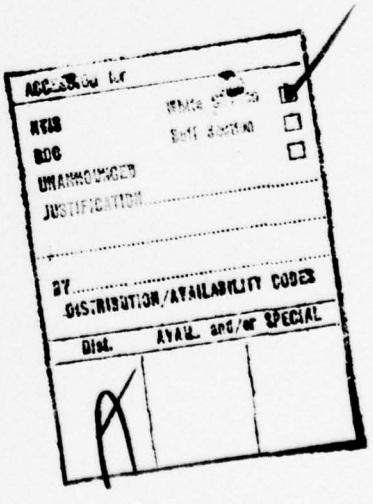
ABSTRACT (Concluded)

a high speed buffer which provides the capability to record, in real-time, unprocessed raw video as well as corresponding processed moving target indicators and integrator outputs. Functional characteristics, hardware descriptions, and details of the programmable signal processor timing and control are provided in this volume. Volume N contains operator instructions and logic diagrams.

CONTENTS



I. BACKGROUND

The US Army Missile Command (MICOM) experimental array radar (EAR) was conceived as a project to facilitate in-house development of radar hardware and technology applicable to short-range missile systems. Phase array antennas were selected because of the significance of electronic scanning in obtaining a multiple engagement capability for tactical air defense systems. Other subsystem designs were developed to emphasize the radar/computer interface aspects of modern radar and to allow exploitation of digital signal processing and control technology. A major objective was to develop and operate (in-house) a versatile radar test bed which permits the creation of technology uniquely oriented to air-defense radar hardware requirements.

One of the primary requirements of a low-altitude air-defense radar is an effective technique to suppress clutter interference without a corresponding reduction in detectability of moving targets.[1] Consequently, emphasis of the EAR test bed is on techniques for analysis of clutter and development of algorithms for clutter suppression. The subject of this report is the EAR programmable signal processor (PSP), the tool that has been developed specifically for clutter measurement and suppression studies. This report has been prepared in two volumes. Volume I contains a functional description of the PSP, layouts and pictures of the hardware structure, and timing diagrams. Volume II contains a complete set of detailed logic diagrams and information on manual operation of the processor. Neither volume contains information on adaptive programming of the PSP to exhibit dynamic frequency responses nor techniques for using the device in a radar. The purpose of the EAR/PSP long-range test program is to develop these types of techniques. The PSP replaces the original processor[2] constructed during the EAR development.

II. EXPERIMENTAL ARRAY RADAR

The EAR is a C-band, phase monopulse, phased-array radar designed to perform the functions of sector search and target track for low

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[1] Burlage, D. W.: "The Digital Filter Problem in Radar Moving Target Indication," Proc. IEEE Region 3 Conf., April 1974, pp. 496-499.

[2] Lancaster, J. F., MICOM Experimental Array Radar Digital Signal Processor, US Army Missile Command, Redstone Arsenal, Alabama, Technical Report No. RE-73-14, 22 February 1973.

altitude, all-weather air-defense applications[3]. A single antenna consisting of one vertical and one horizontal line array of 64 elements each, gains of 26 dB, and vertical polarizations can perform search over approximately 100 deg in azimuth and can provide target track information in azimuth and elevation.

For azimuth search, the horizontal antenna array is used to form a fan beam approximately 2 by 40 deg which is electronically steered over the search sector in variable (usually 2 deg) steps. The size of the search sector is selectable up to approximately 100 deg. The time on target, or dwell time interval (DTI), is nominally 10 msec for transmission of 50 pulses at a maximum pulse repetition frequency (PRF) of 5 kHz; therefore, a full 100-deg search raster requires 0.5 sec. In the search mode, the EAR transmits and receives only on the azimuth beam.

In track, EAR transmits on the azimuth beam and receives on both. Four receiver channels are provided to receive sum and difference components of the azimuth and elevation information simultaneously. The superheterodyne receivers have IF frequencies of 390 and 30 MHz, noise figures of 7 dB, and sensitivities of -100 dB. The quadrature channel PSP, which normally processes only the single search channel, is time-multiplexed over all four receiver channels in the track mode.

The EAR system uses a general purpose SEL 8600 computer as a system controller. For simple sector scan search, this computer generates the search raster for the B-scope display of detections from the signal processor and raw video from the receiver. It also transfers data to the antenna phase command generator which shifts the phase of the antenna elements to electrically position the beam. In the track mode, processed data produced by the signal processor are transferred to the computer where tracking error signals are derived for closing the digital tracking loops in range and angle.

Other system components are the exciter, transmitter, and programmable system timing generator (PSTG). The exciter functions as a driver for the transmitter and provides a stable coherent signal for the receiver and PSTG. The transmitter is capable of producing 2.5 kW average power and can be used to transmit either 0.2, 1.0, or 6.6 μsec wide pulses. The PSTG provides all the major timing functions for the EAR system, including the clocking of data between the various components. The PSTG provides a variety of programmable PRF and DTI capabilities other than the nominal 5-kHz and 10-msec values.

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[3] Low, W. L., Experimental Array Radar (EAR) Test Bed, US Army Missile Command, Redstone Arsenal, Alabama, Technical Report No. RE-72-18, November 1972.

The significant parameters for the EAR system are as follows:

Dwell time	Variable
PRF	0 to 5 kHz (max)
Pulsewidth, short pulse mode	0.2 μsec
Pulsewidth, pulse compression modes	1 μsec 6.6 μsec
Range sampling rate	5 MHz
Number of range bins processed (R)	0 to 1024 (max)
MTI	Programmable digital filter
Number of pulses, integrated (K)	Variable

III. FUNCTIONAL CHARACTERISTICS OF PSP

The PSP is an aggregrate of multipliers, adders, and memories capable of performing high-order MTI filtering at radar operating speeds. Various MTI algorithms for clutter cancellation and adaptive processing can be evaluated, and performance criteria can be established for future missile system applications.

A. Block Diagram

The processor (Figure 1) consists of five distinct functional units:

1) MTI and coefficient memory.
2) Vector magnitude unit.
3) Noncoherent integrator.
4) Threshold detector.
5) Programmable data transfer unit.

The processor is capable of performing:

1) Signal-to-clutter improvement by means of the programmable MTI.
2) Combination of in-phase and quadrature channel MTI residues.
3) Signal-to-noise improvement by noncoherent integration of combined MTI residues.

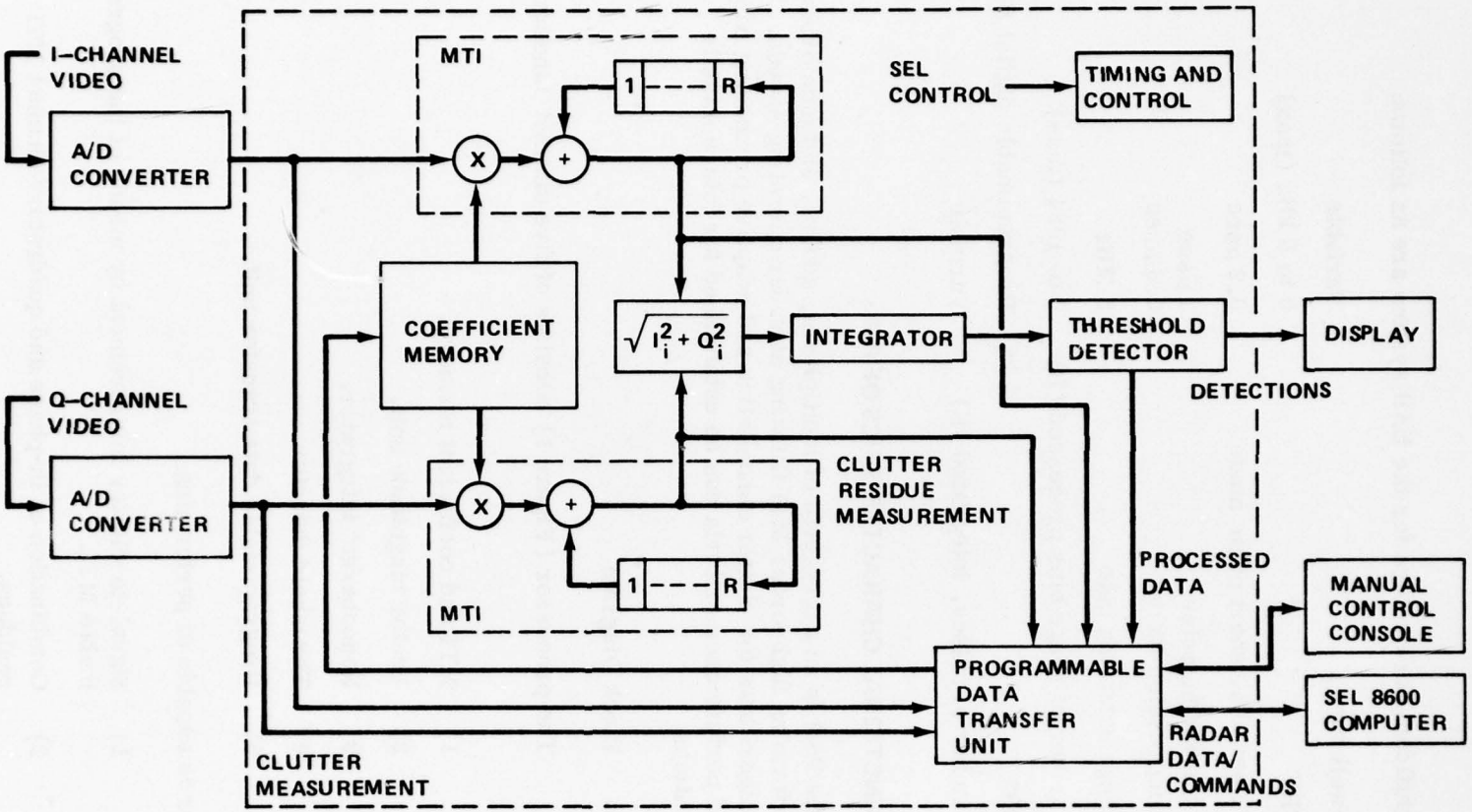

Figure 1. Block diagram of programmable signal processor.

4) Threshold detection.

5) Data transfers to other radar system hardware elements.

Bipolar video signals from the receiver multiplexers are input to A/D converters for the in-phase (I) and quadrature (Q) channels. These continuous signals are sampled at a 5-MHz rate, thus forming discrete range samples at 30-m intervals. Each sample is represented by a digital word and is composed of clutter, noise, and target components.

Clutter components are suppressed with two MTI digital filters providing bandstop characteristics for attenuation of fixed or slow moving clutter and bandpass characteristics to pass all signal components associated with targets of interest. Nonrecursive fixed-window digital filters of order N were chosen to implement the MTI function, viz.,

$$y_i(kNT) = \sum_{n=0}^{N-1} C_n x_i(kNT - nT) \qquad \begin{matrix} i = 1,2,\ldots,R \\ k = 1,2,\ldots,K \end{matrix} \quad . \qquad (1)$$

Although filters must be implemented for all R radar range bins, a fixed-window implementation requires that only one output be calculated every NT sec, where T = 1/PRF. Figure 2 illustrates the fixed-window MTI process for a multiple range bin system. The partial sums of the MTI accumulator, [A], are only shown for k = 1. Note that range bins are numbered from 1 to R and MTI outputs are numbered from 1 to K; however, multiplier coefficients are numbered from 0 to N-1. At the beginning of a beam dwell and during the first PRI, video range samples from each range bin denoted by $x_i(T)$ are weighted with the appropriate filter coefficient C_{N-1}. During the next interval, the digital samples denoted by $x_i(2T)$ are weighted with C_{N-2} and added to the previous value to form a partial sum. This process will continue for each PRI until N-weighted samples have been summed to form the desired MTI output $y_i(NT)$ for each range bin within that N^{th} PRI. In each DTI, K sequences are repeated.

Each MTI will output a processed sample every NT sec to a vector magnitude unit (VMU) for combination.

$$I_i \triangleq y_i(kNT) \quad \text{for I-channel}$$

$$Q_i \triangleq y_i(kNT) \quad \text{for Q-channel} \quad . \qquad (2)$$

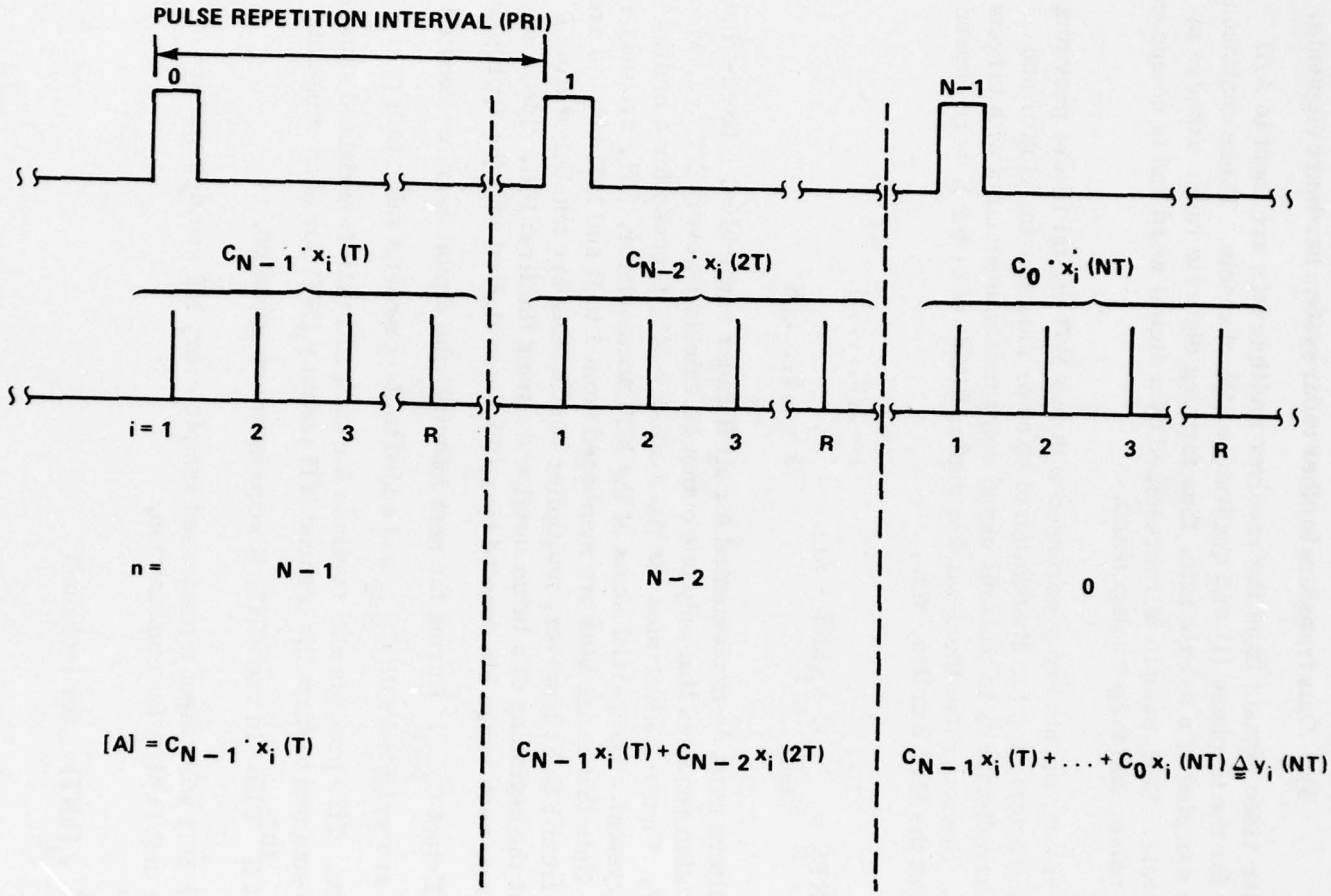

Figure 2. Typical fixed window MTI process.

A perfect VMU would perform $\sqrt{I_i^2 + Q_i^2}$; however, because of the complexity of implementing this function, it is necessary to use an approximation algorithm. Consequently, I_i and Q_i outputs are combined according to

$$Y_i(kNT) \triangleq \begin{cases} L_i + 3S_i/16 & \text{for } S_i/L_i \leq 0.5 \\ 3L_i/4 + 11S_i/16 & \text{for } S_i/L_i > 0.5 \end{cases} , \tag{3}$$

where $L_i = \max [I_i, Q_i]$ and $S_i = \min [I_i, Q_i]$.

The VMU outputs $Y_i(kNT)$ are then clocked to a noncoherent integrator for improvement of signal-to-noise ratios. The integrator accumulates K VMU outputs each DTI for all R range bins, i.e.,

$$INT_i = \sum_{k=1}^{K} Y_i(kNT) \qquad i = 1,2,\ldots,R \quad . \tag{4}$$

After the last PRI, or K^{th} integration, INT_i is compared to a preset reference threshold in the threshold detector, and an alarm bit is produced for each range bin where this sum exceeds the threshold. The alarm bits are used to indicate threshold crossings on the B-scope display and to control transfer of processed data (viz., INT_i values) to the computer.

The programmable data transfer unit (PDTU) functions as a multimode interface for data communications between the PSP and the control computer or manual control console. Control commands generated by the computer configure the unit for a predefined mode (i.e., search, track, measurement, loading, or diagnostic). Subsequent data transfers furnish the control computer or PSP with the necessary information for performing the various algorithms associated with the radar operation. Typical data transfers are video clutter measurements, resulting MTI residues, and processed track data to the computer or filter coefficients to the PSP.

B. Applications

As a radar subsystem, the PSP will offer a wide range of flexibility in the evaluation of various MTI filter designs and techniques. In a radar environment, clutter interference is caused by reflections from a variety

of backscatters with typical doppler spectra as depicted in Figure 3. Although complete rejection of clutter is impossible, the PSP is a viable tool for developing higher order filter designs to obtain maximum clutter suppression with increased target detectability.

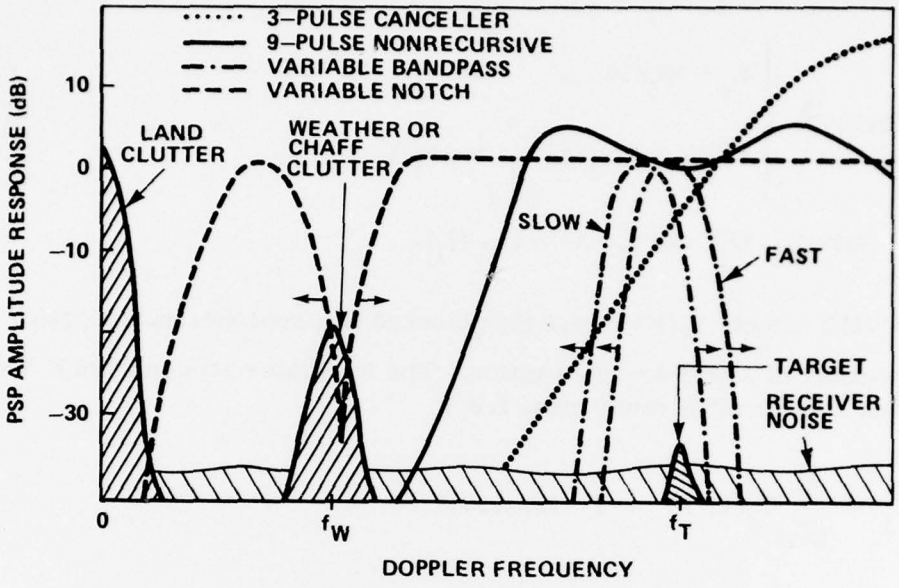

Figure 3. Radar video spectrum and typical PSP frequency characteristics.

The improved capability expected from the PSP is illustrated in Figure 3 for a variety of filters. A nine-tap filter response is shown with a significantly improved passband over the conventional three-pulse canceller while maintaining good stopband characteristics for clutter attenuation. The coefficient memory design results in a real time operating capability for adaptive processing studies. Filter coefficients developed for various radar environments[4] can be stored in the control computer and, consequently, loaded into the PSP at any time during the normal radar operation. An example of the adaptive capabilities is depicted by the variable notch filter which tracks and suppresses weather or chaff interference. Similar techniques can be applied for isolation of targets using bandpass filters. Once isolated, the target doppler can be effectively tracked with narrowband filters eliminating most of the receiver noise as well as the clutter.

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[4] Burlage, D. W. and Houts, R. C., Design Techniques for Improved Bandwidth Moving Target Indicator Processors in Surface Radars, US Army Missile Command, Redstone Arsenal, Alabama, Technical Report No. RE-75-35, 20 June 1975.

Filter coefficients are stored in programmable memory and can be modified as a function of beam position and range. The adaptive nature of the PSP for real-time changing of filter frequency characteristics yields a unique feature as illustrated in Figure 4. This hardware technique involves partitioning the total range coverage into either one, two, or three range sectors for a given radar beam position and implementing separate filter characteristics for each sector. Consequently, areas of high clutter interference, such as the rain cloud depicted in Figure 4, can be isolated. Once isolated, particular MTI filters (MTI_2 and MTI_3) can be used in these range bins to provide maximum clutter attenuation. Similarly, filters providing increased target detectability (MTI_1 and MTI_4) can be implemented in regions of minimum interference. Range-sectoring can be performed on every radar beam position in the azimuth search sector with different range sectors used on each beam position.

IV. DESCRIPTION OF SIGNAL PROCESSING HARDWARE

The hardware implementation of each functional unit is described in this section. Hardware structures, dual-in-line package layouts, and timing diagrams are included. Detailed logic diagrams are contained only in Volume II of this report.

A. A/D Converters

The A/D converters of the PSP convert bipolar video radar returns to a suitable binary format for digital processing. Because EAR parameters require an A/D that operates at a 5-MHz rate with a dynamic range of ±1024 mV, Computer Labs Model HS-5905 9-bit converters are being used. The output format is an offset binary code where,

1.11111111 denotes + 1024 mV,

1.00000000 denotes 0000 mV,

and

0.00000000 denotes - 1024 mV. (5)

Because the PSP uses 2's complement arithmetic, the offset binary code can be converted to 2's complement simply by inverting the sign bit, i.e.,

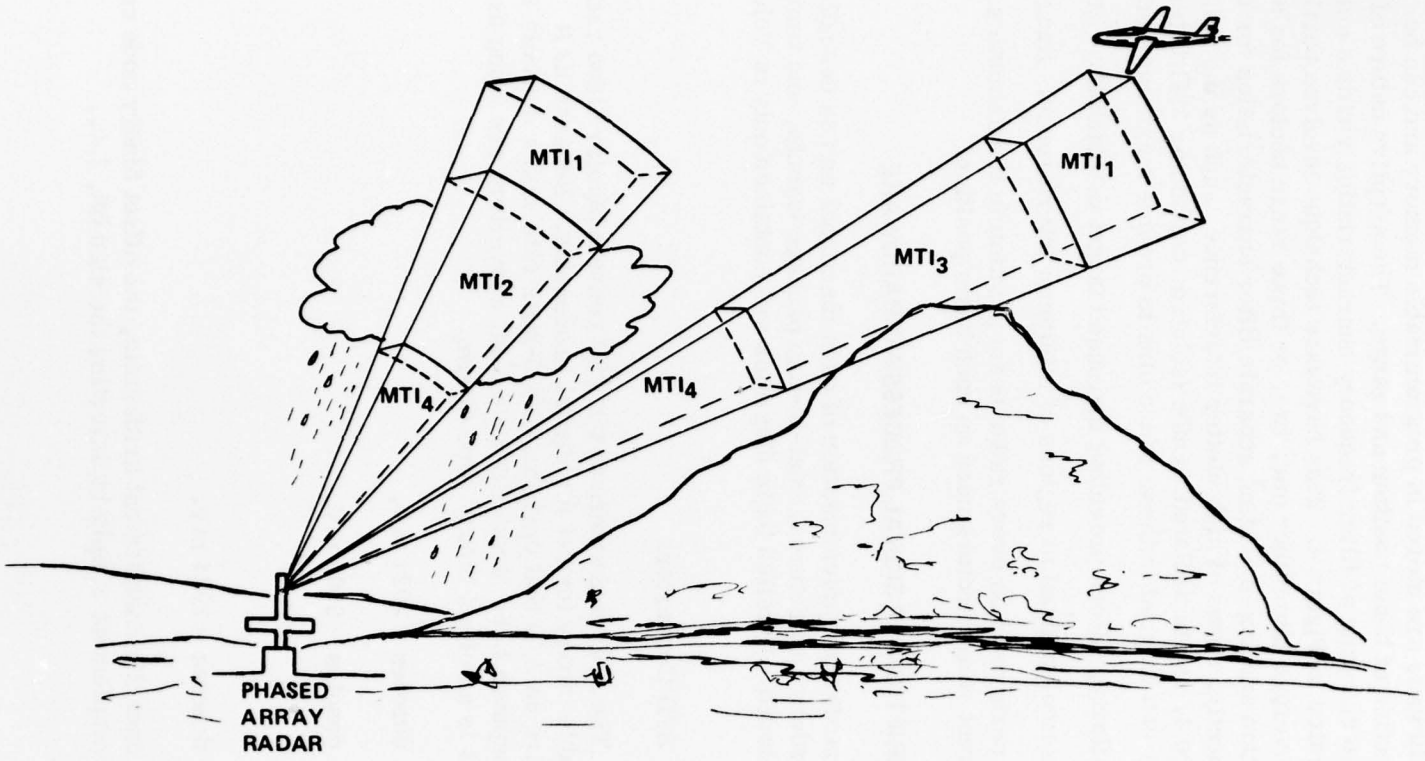


Figure 4. MTI filtering as a function of range sector and beam position.

0.11111111 denotes + 1024 mV,

0.00000000 denotes 0000 mV,

and

1.00000000 denotes - 1024 mV. (6)

The binary number (1.00000000), which represents the largest negative number, is an invalid 2's complement number because it has no positive counterpart. Consequently, it is elminated as an input to the PSP by adding ONE to the LSB each time it occurs, thereby producing a valid 2's complement number, i.e.,

$$\begin{aligned} 1.00000000 &= -1024 \text{ mV} \\ 0.00000001 &= +\quad 4 \text{ mV} \\ \hline 1.00000001 &= -1020 \text{ mV} \quad . \end{aligned} \tag{7}$$

Logic to perform this correction is included on each of the I and Q channel MTI multiplier cards.

B. MTI

The MTI hardware structure (Figure 5) is identical for both channels. Internal and external data transfer paths and timing/control signal information are included. The digital hardware implementing the MTI function is physically contained on three separate 8- × 6-in. socket cards for each processing channel. The three cards are shown in Figures 6 and 7 with the various circuits comprising the MTI identified. Each of the cards is totally interchangeable with identical cards from the other channel.

The multiplier module consists of a 9- × 9-bit sign-magnitude multiplier with correction circuitry necessary to form a 2's complement digital output. The 2's complement output product, P, is formed by the following summation:

$$P = (XY) + (Y_S\bar{X}) + (X_S\bar{Y}) + (X_S + Y_S) \quad , \tag{8}$$

where X and X_S (Y and Y_S) are magnitude and sign, respectively, of the multiplier (multiplicand). $\bar{X}$ denotes the complementation of X. All of the terms following the XY product are correction terms for forming a correct 2's complement product. The sign of the product is formed separately by the exclusive OR

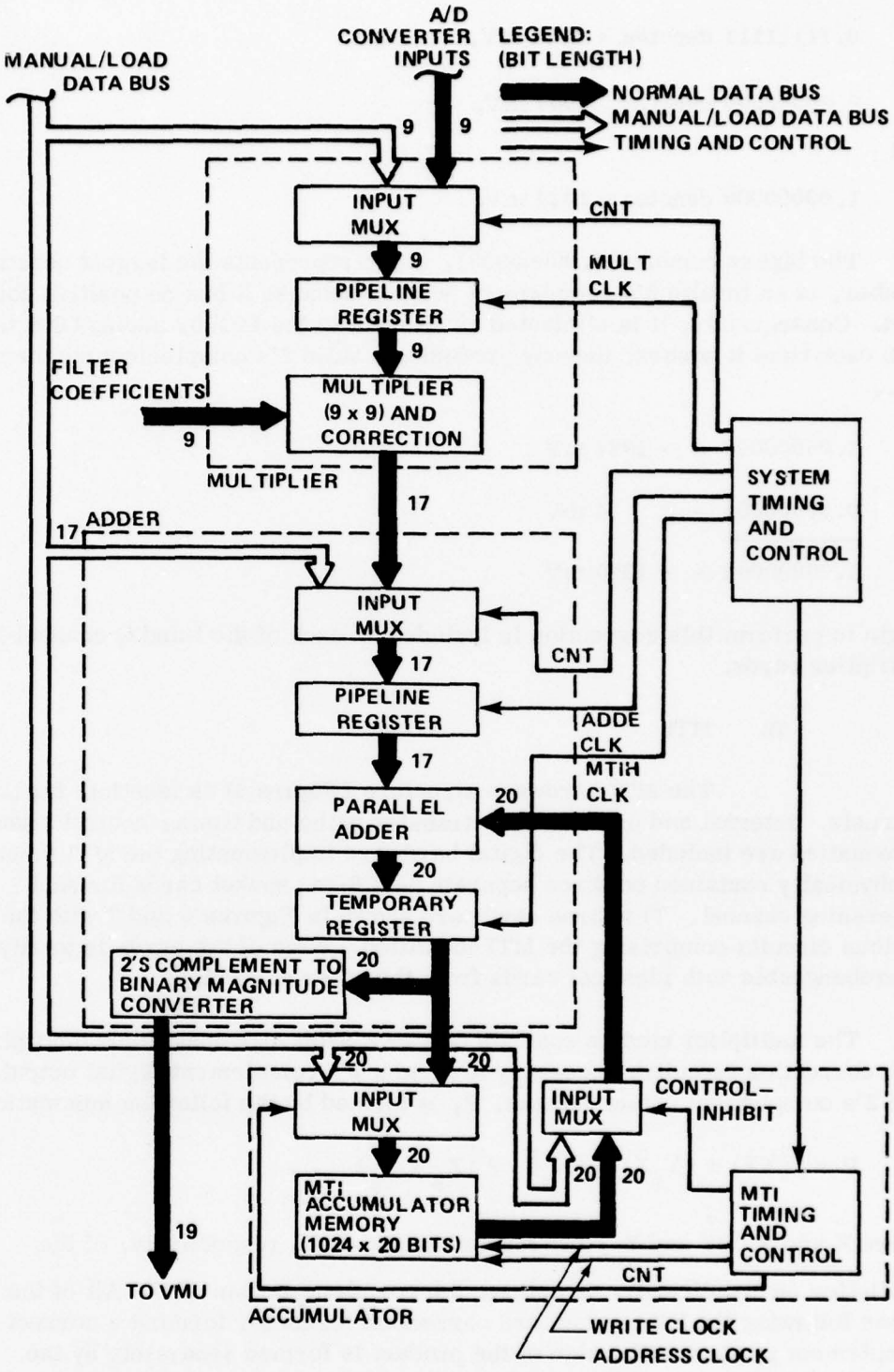


Figure 5. MTI hardware structure.

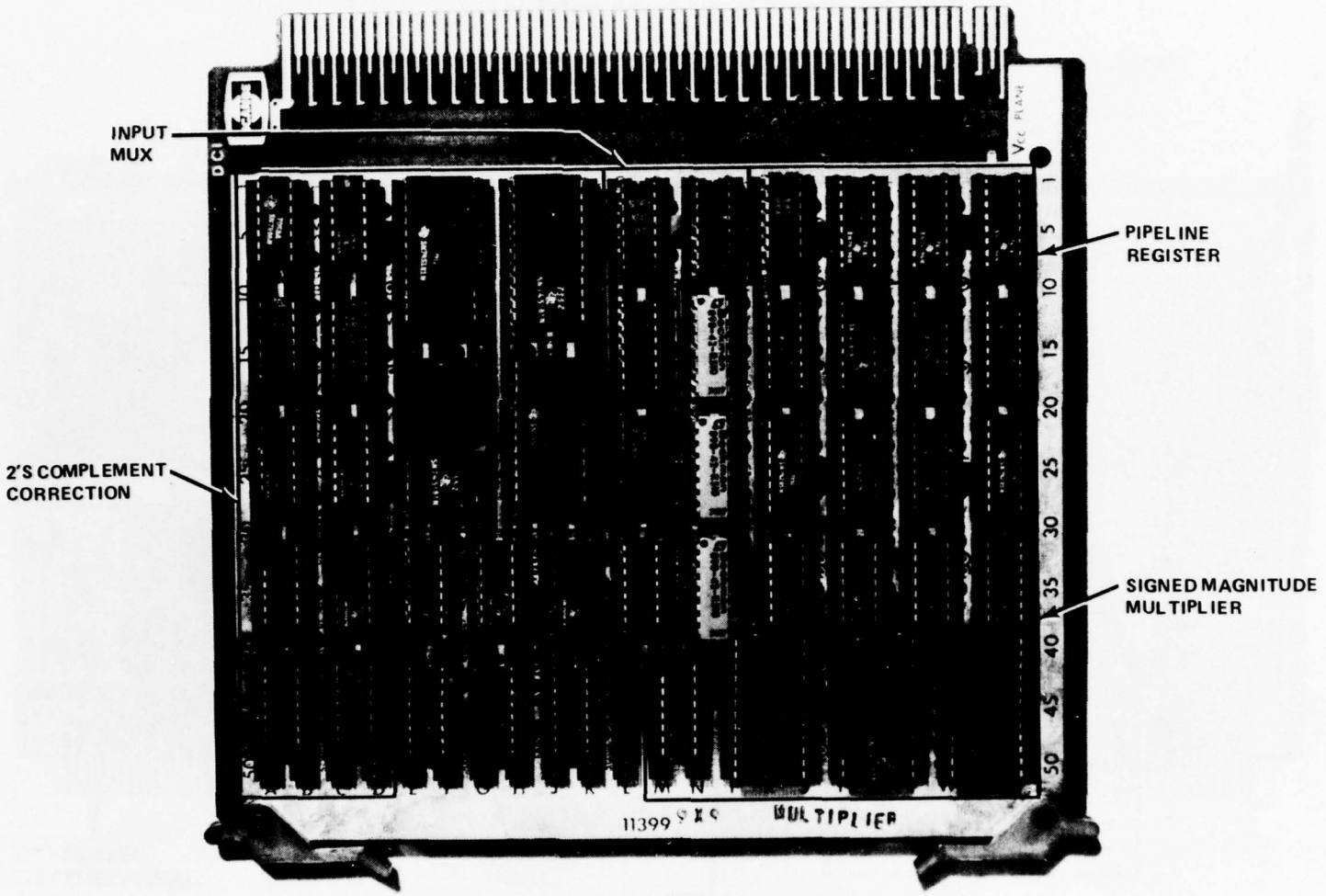


Figure 6. MTI multiplier socket card.

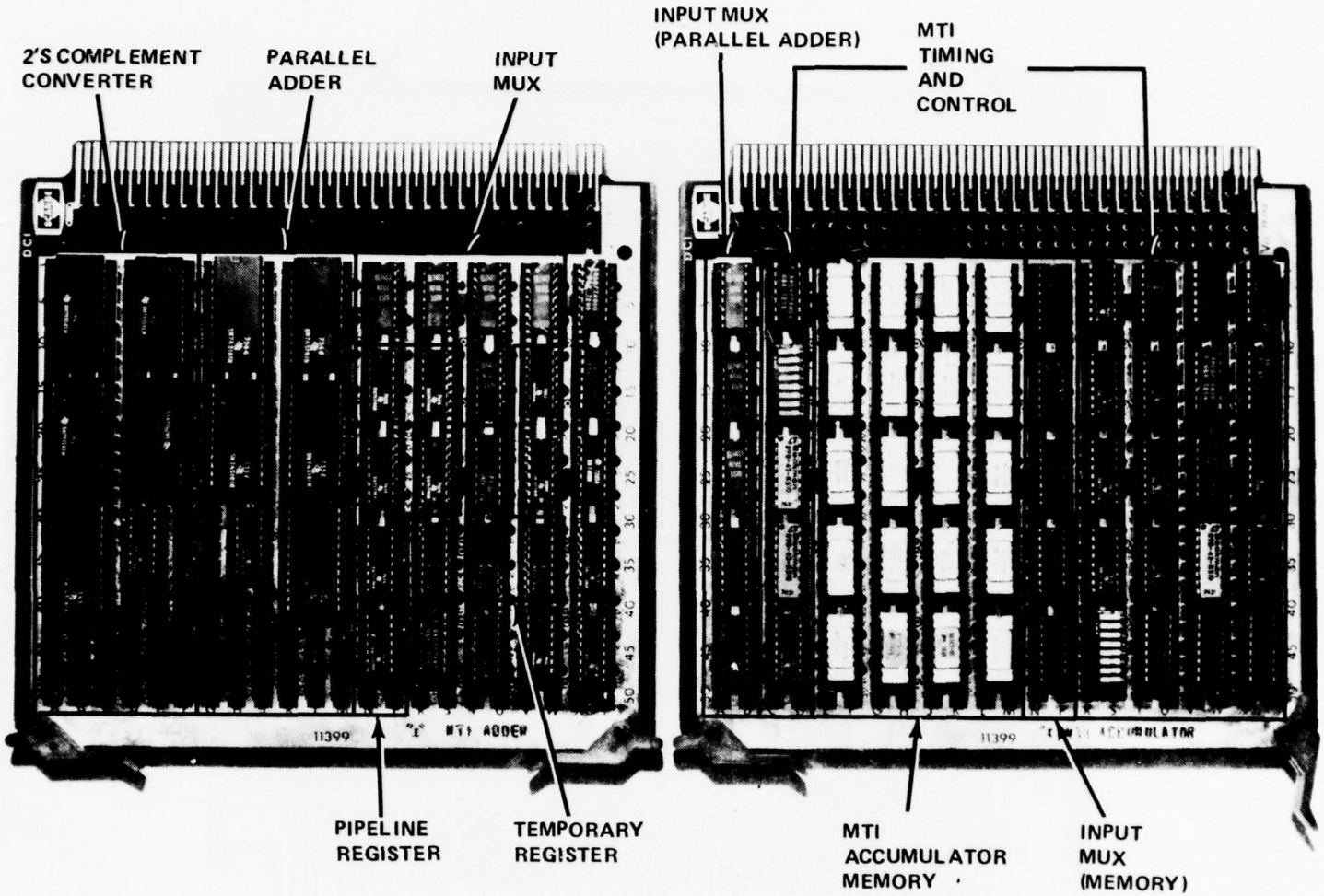


Figure 7. MTI adder and accumulator socket cards.

$$P_s = (X_s) \oplus (Y_s) \quad . \tag{9}$$

If either the multiplier or multiplicand is zero, P_s is forced to a positive value.

The parallel adder and memory hardware functions as an accumulator for processing multiplier outputs. During a PRI, data from the multiplier is added to the contents of the accumulator memory and the results restored (as they are produced) back into memory. However, memory outputs during the first PRI for each N-pulse group are inhibited to insure initial samples are stored without modification. This process continues throughout the DTI with R-valid outputs produced once every N PRI. Valid MTI outputs are reformatted to binary magnitude before they are transferred to the VMU.

Internal control of data flow is performed by on-card timing circuits and the system timing card. Lines denoted as CNT and LD for all PSP circuits are active during computer loading sequences and input operations involving the manual control console.

C. MTI Coefficient Memory

The MTI coefficient memory hardware structure is shown in Figure 8. The card containing the hardware is shown in Figure 9. This circuit provides the PSP with flexible signal processing capability.

The main memory and address counter are used as a nine-bit parallel shift register to clock coefficients to the I and Q MTI multiplier inputs under control of various programmed options. For the simplest mode of operation, the memory circuit will output a single filter coefficient C_n to the I and Q multipliers each PRI, alert the PSP (after each cycle through N coefficients) that MTI outputs are ready for VMU processing, and repeat the cycle K times. However, the flexibility of the memory circuit extends the processing capabilities to more complicated algorithms. Options available through proper loading of the memory circuit are:

1) Sectoring of the R-range bins into two or three regions for processing of each by a different set of coefficients, i.e., different MTI.

2) Varying the filter order and coefficient set within a DTI.

3) Repeating blocks of coefficients within a DTI as desired.

(These options and related timing will be discussed in the timing and control subsection.) By combining these options, the PSP can be configured to perform

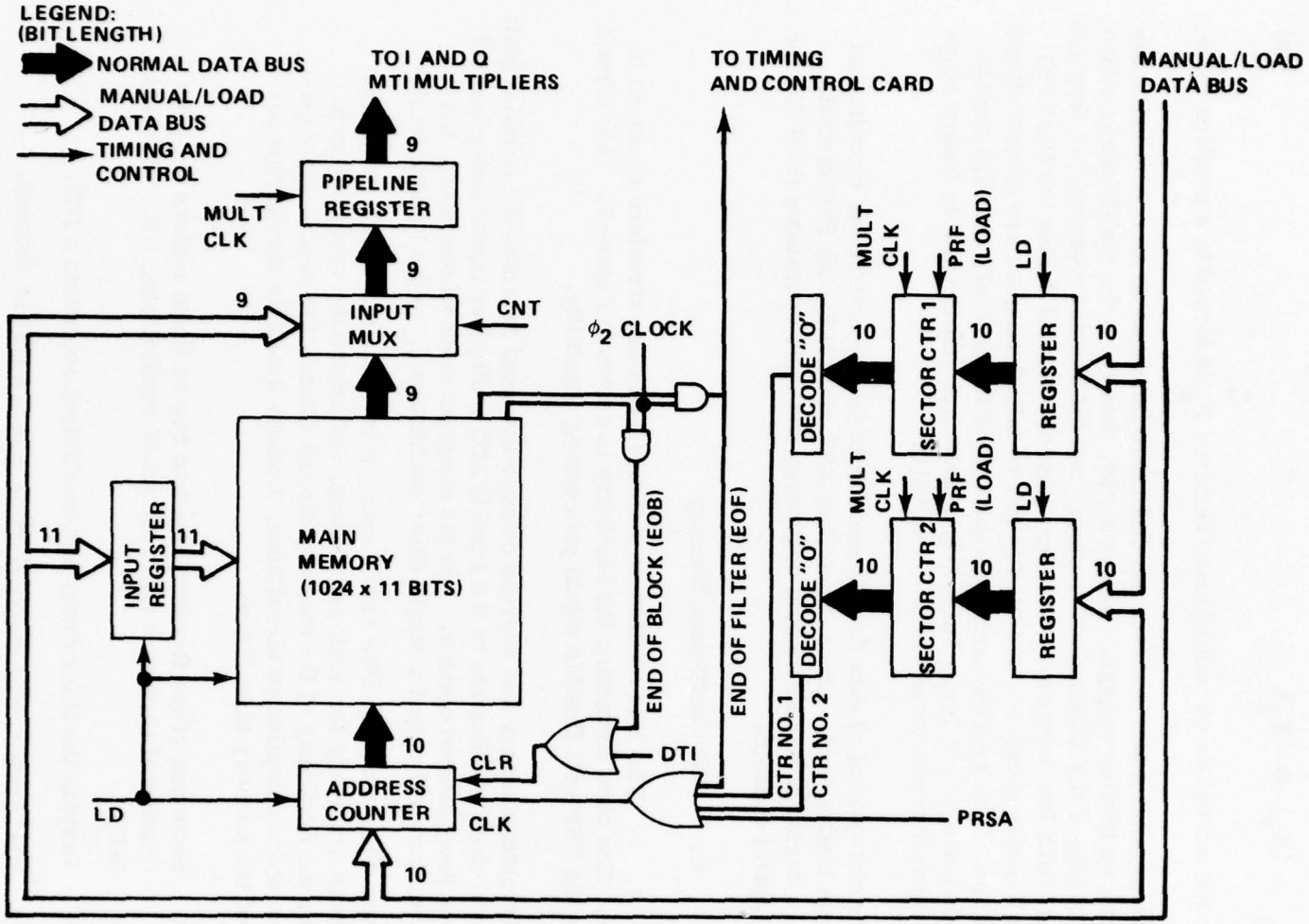


Figure 8. MTI coefficient memory hardware structure.

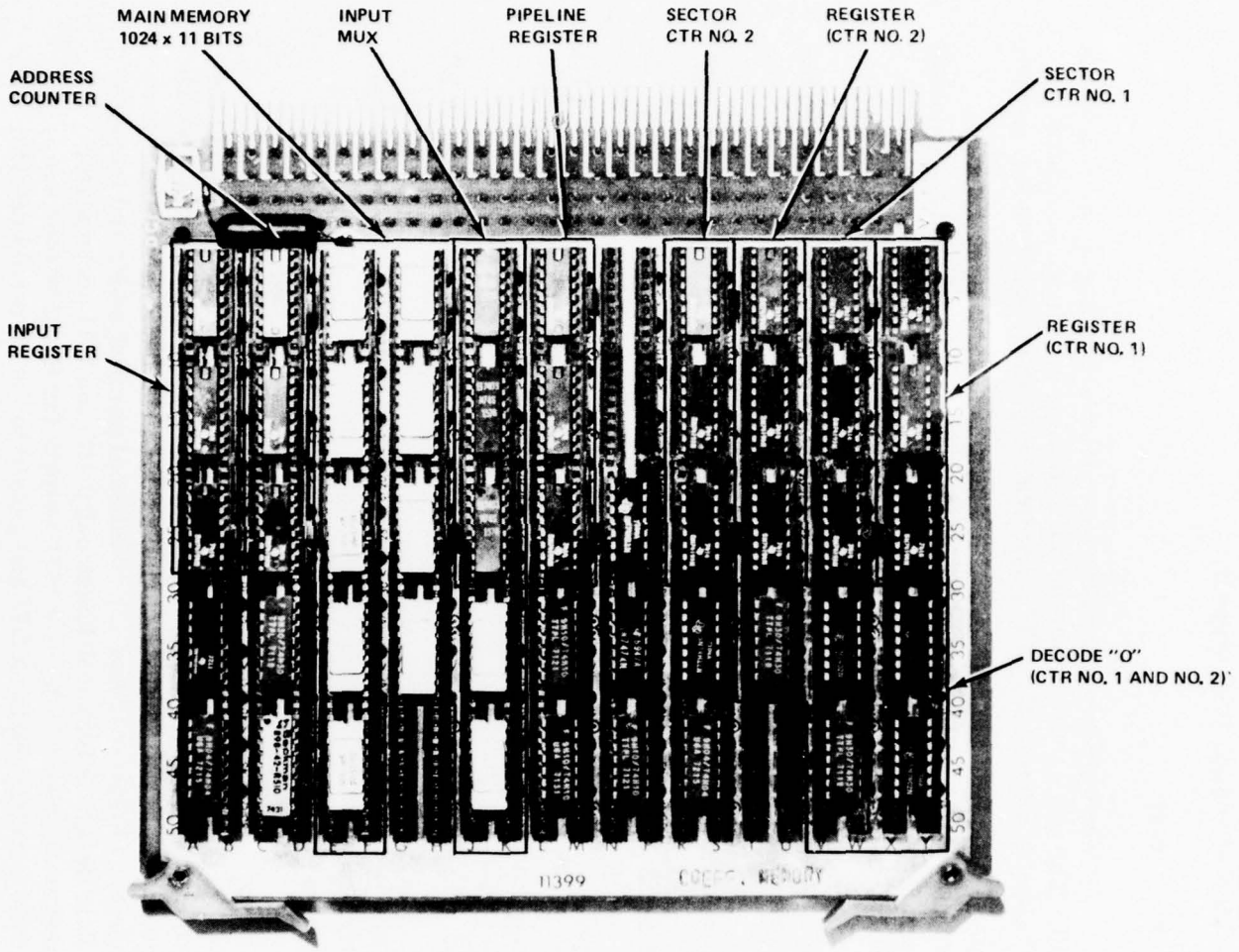


Figure 9. MTI coefficient memory socket card.

a variety of processing tasks, including range adaptivity, pulse-to-pulse PRF stagger, or block-to-block PRF stagger.

D. VMU

The VMU hardware structure to implement Equation (3) is shown in Figure 10. The two cards containing the hardware are shown in Figure 11. The I and Q channel values, $Y_i(kNT)$, are first input to a magnitude comparator and selection multiplexer to determine which is L and S. Once L and S are determined, they are sent to appropriate shifting and adding circuits to calculate L + 3S/16 and 3L/4 + 11S/16. Finally, L/2 and S are compared to determine which of the two calculated approximations to route to the integrator.

Because L + 3S/16 and 3L/4 + 11S/16 require division, their implementation is performed digitally by right shifts and adds, i.e.,

$$3S/16 = S/16 + S/8 \quad , \tag{10}$$

where S/16 and S/8 are four- and three-bit shifts of S, respectively;

$$11S/16 = 3S/16 + S/2 \quad , \tag{11}$$

where 3S/16 is already available and S/2 is a one-bit shift; and

$$3L/4 = L/2 + L/4 \quad , \tag{12}$$

where L/2 and L/4 are one- and two-bit shifts of L. These outputs are added appropriately to obtain the preceding approximation.

E. Integrator

Following the VMU in the signal processor and providing the system signal-to-noise gain is the integrator [defined by Equation (4)] which simply accumulates K VMU outputs during a DTI. The basic hardware layout for the integrator (Figures 12 and 13) consists of parallel adder and memory modules. This design is identical functionally with the MTI accumulator hardware previously described. The VMU outputs for R-range bins are integrated noncoherently during a DTI and passed to the threshold detector unit.

F. Threshold Detector

The threshold detector (Figures 14 and 15) compares the integrator outputs, INT_i, to a preset threshold. Depending on the results of

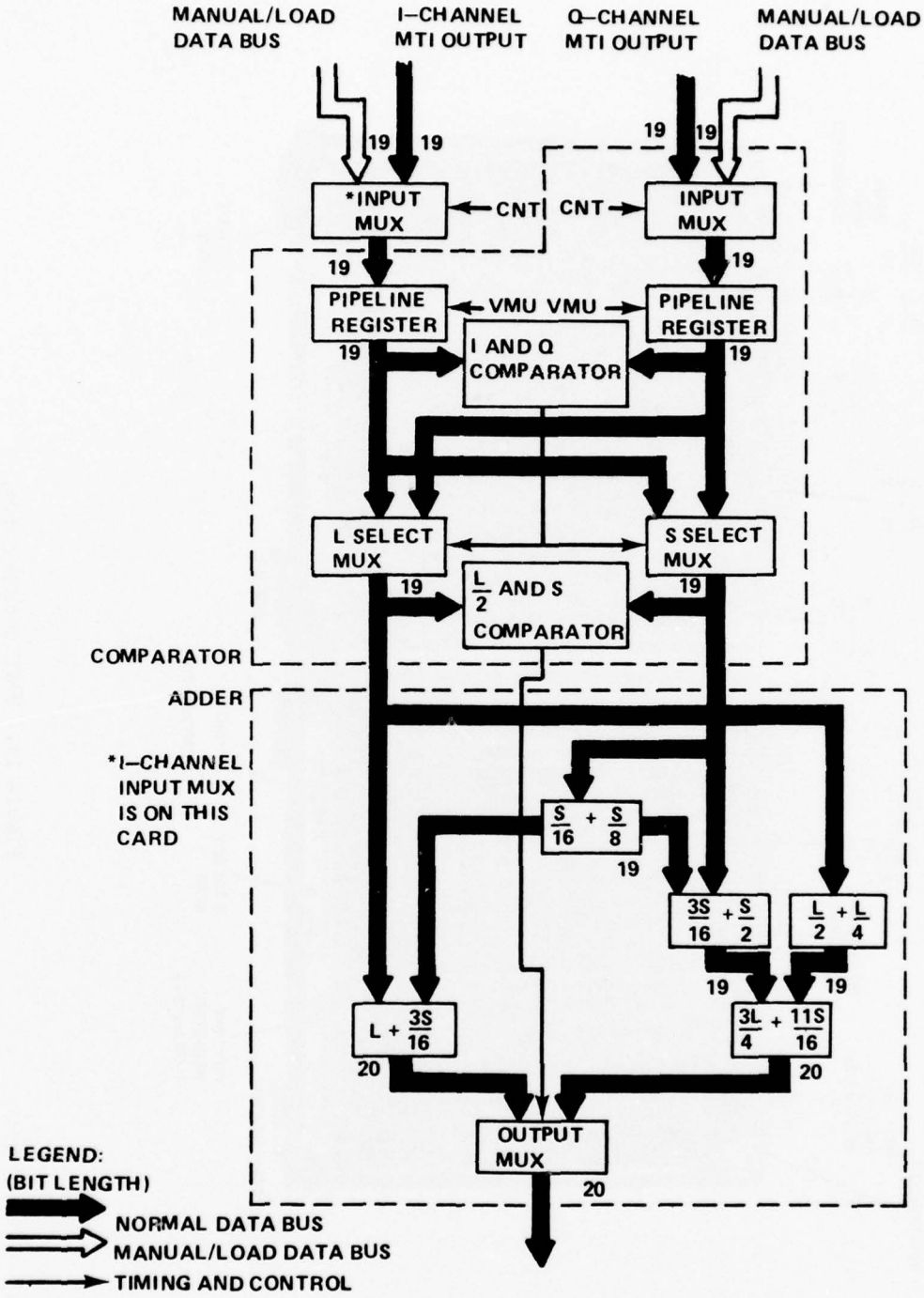


Figure 10. VMU hardware structure.

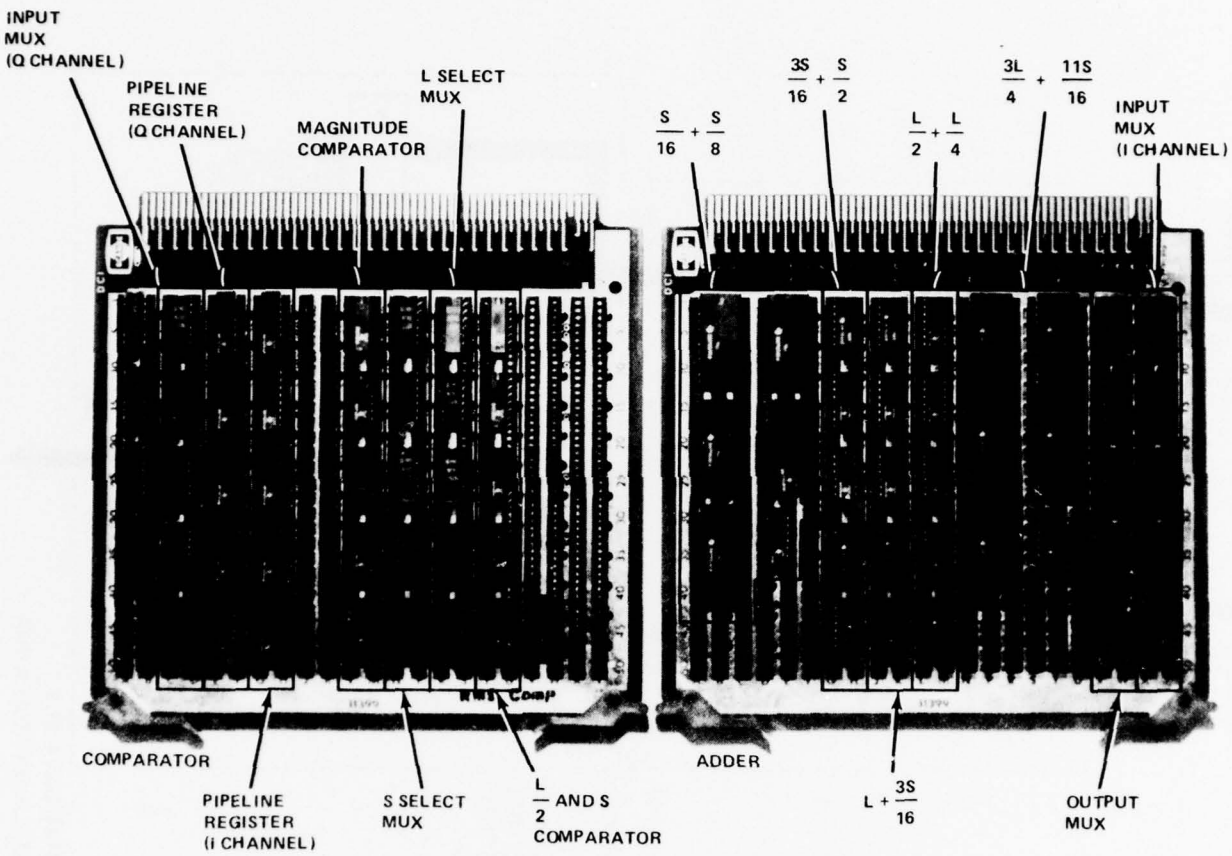


Figure 11. VMU socket cards.

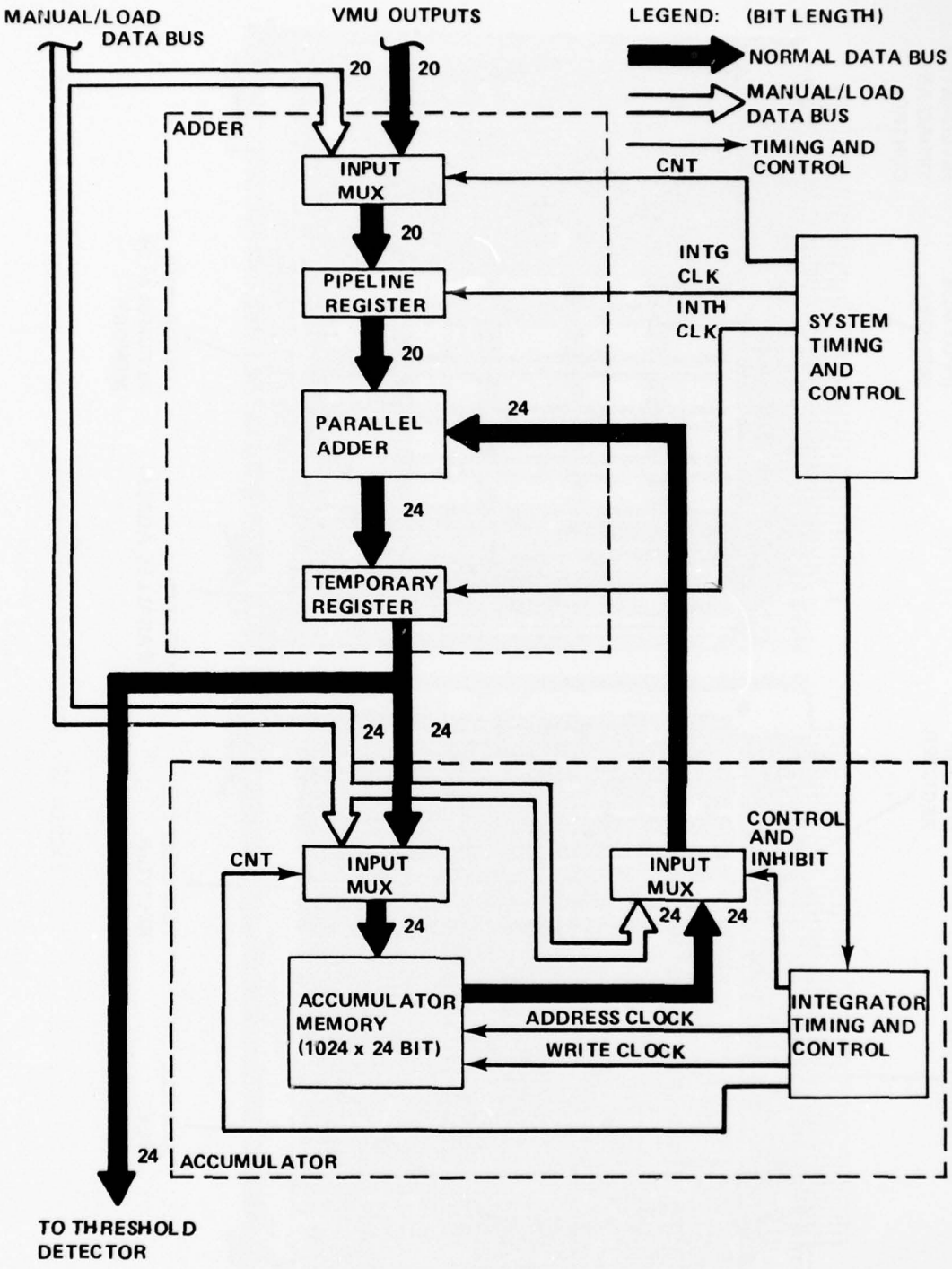


Figure 12. Integrator hardware structure.

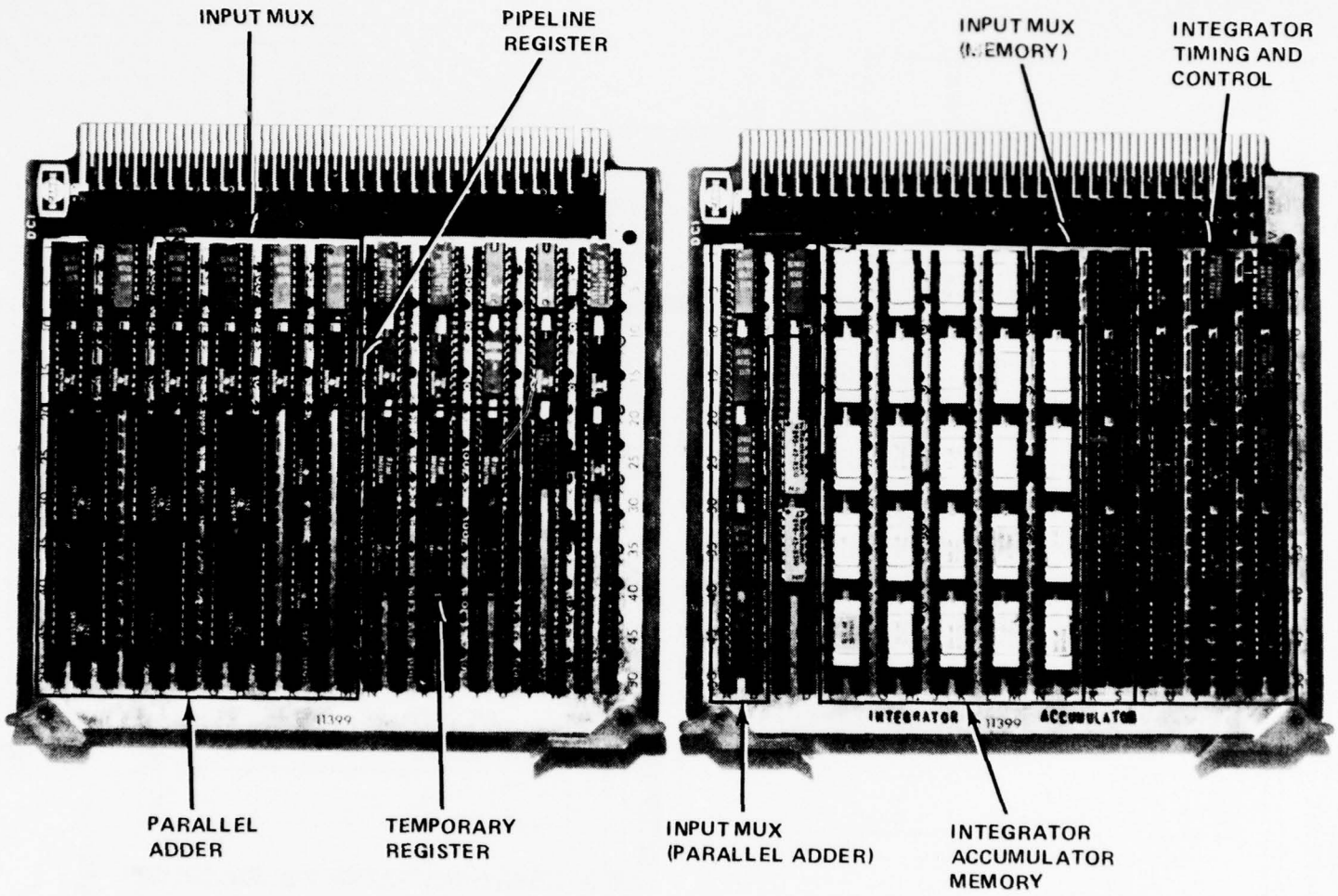


Figure 13. Integrator socket cards.

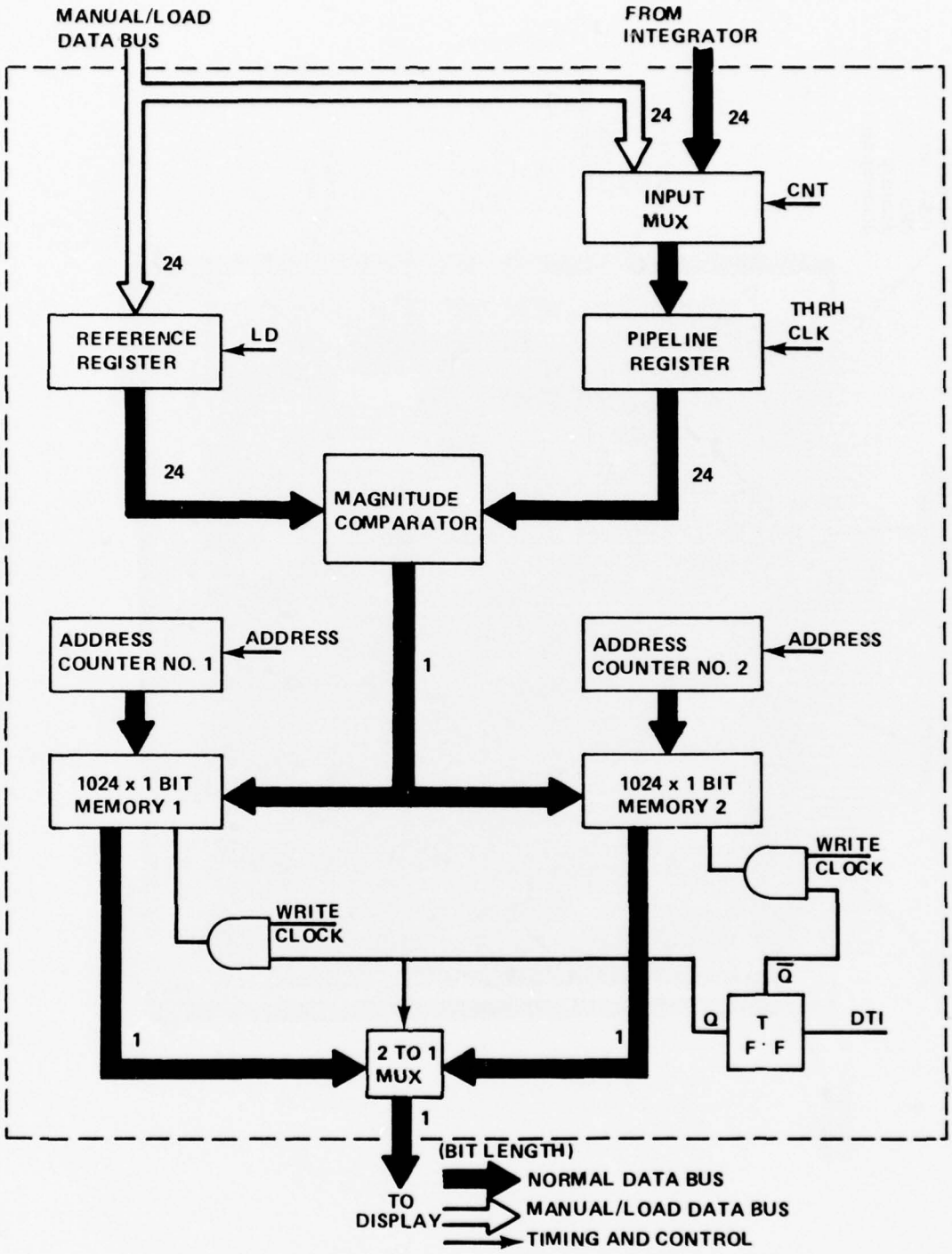


Figure 14. Threshold detector hardware structure.

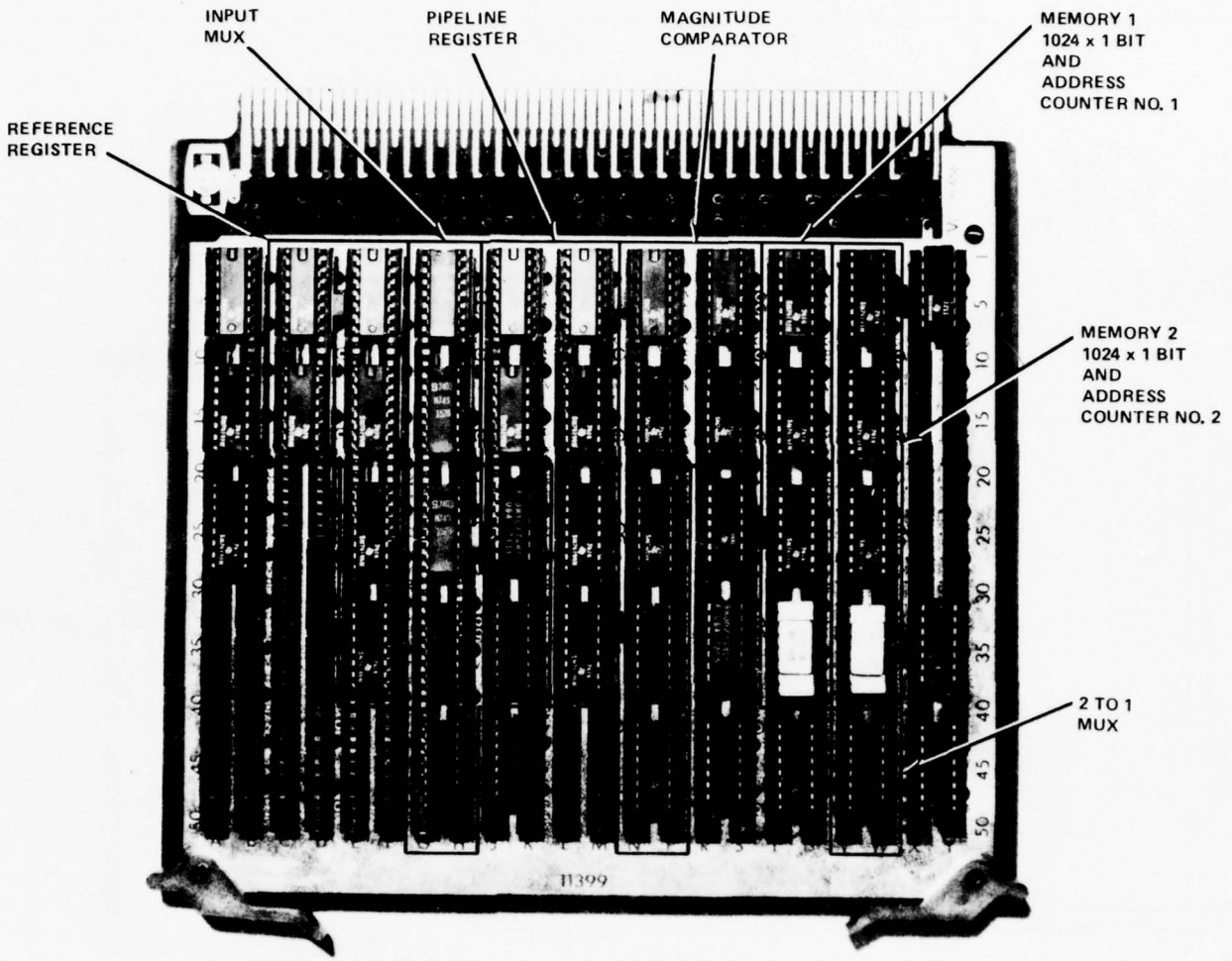


Figure 15. Threshold detector socket card.

the comparison, a target alarm bit is either set to a ONE if the threshold is exceeded (target present), or reset to ZERO (no target) in one of two available memories. While one memory is being used to store alarm bits for the current DTI, the other memory will be transferring bits produced during the previous DTI to the radar display.

G. Timing and Control

All major timing signals for the PSP originate from a single timing card as shown in Figures 16 and 17. This module consists of the digital logic necessary for data control and sequencing for each section of the PSP. All external timing commands relating to PSP operation enter the timing card and are subsequently distributed throughout the entire system. Other functions performed on the socket card include generation of various manual timing commands and miscellaneous control circuitry.

Inputs from the PSTG consist of the PRF, DTI, and 20-MHz system clocks. These clocks enter the timing logic through MECL line receivers, and are used either directly or indirectly for initialization and data sequencing. There are two major timing cycles for the PSP, viz., a DTI cycle which is controlled with a PRF counter, and a PRI cycle which is controlled with a master range bin counter. The PRF counter, located in the timing and control card, is reloaded with the value K • N by the system DTI pulse and clocked down by the system PRF. When the count reaches zero the counter signals the PSP that processing is complete for that beam position. The range bin counter is actually the address counter for the MTI accumulator memory located in the MTI timing and control section of that card. It is reset to zero by a derivative of the system PRF clock (the PRST pulse) and clocked by a derivative of the 20-MHz clock (the MULT signal). When the count reaches R + 3 all operations in the PSP cease. At that time, all R range bins have been processed for one PRF and the processor is in a hold status until the next PRF pulse which restarts the PRI cycle. Numerous other timing signals occur within each of the PRI cycles as illustrated in Figure 18. Figure 18 also shows the system DTI and PRF signals with their relationship to 5-MHz Phase 1(ϕ_1) and Phase 2(ϕ_2) clocks which are derived from the 20-MHz signal and used throughout the PSP hardware for register and memory control functions. To control data flow through the PSP pipeline as shown in Figure 19, the ϕ_1 clock was used as a universal data strobe. The series of clocks in Figure 18, beginning with the MULT clock through THRH clock, were derived from the ϕ_1 signal to provide input register control for each stage of the system pipeline.

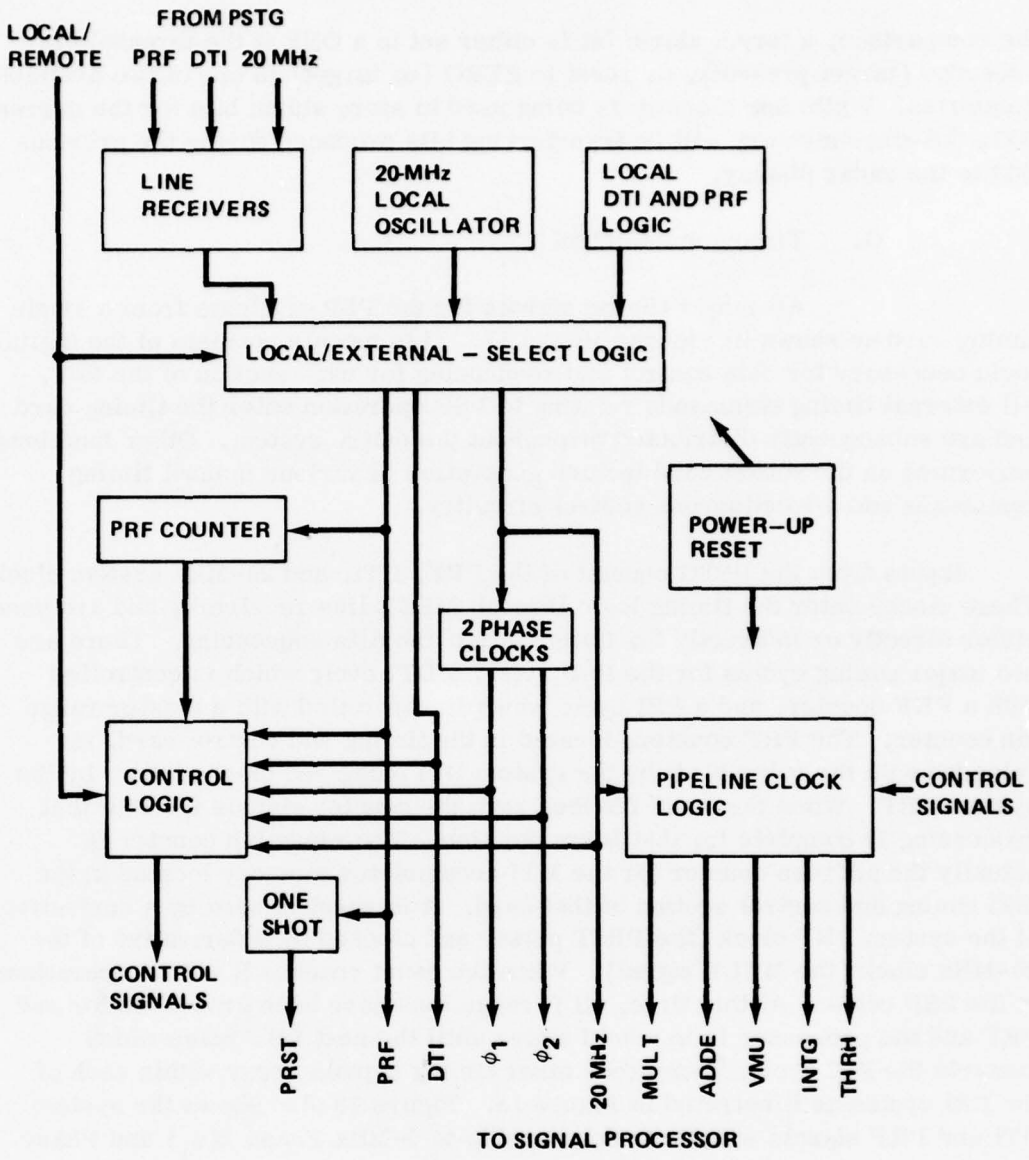
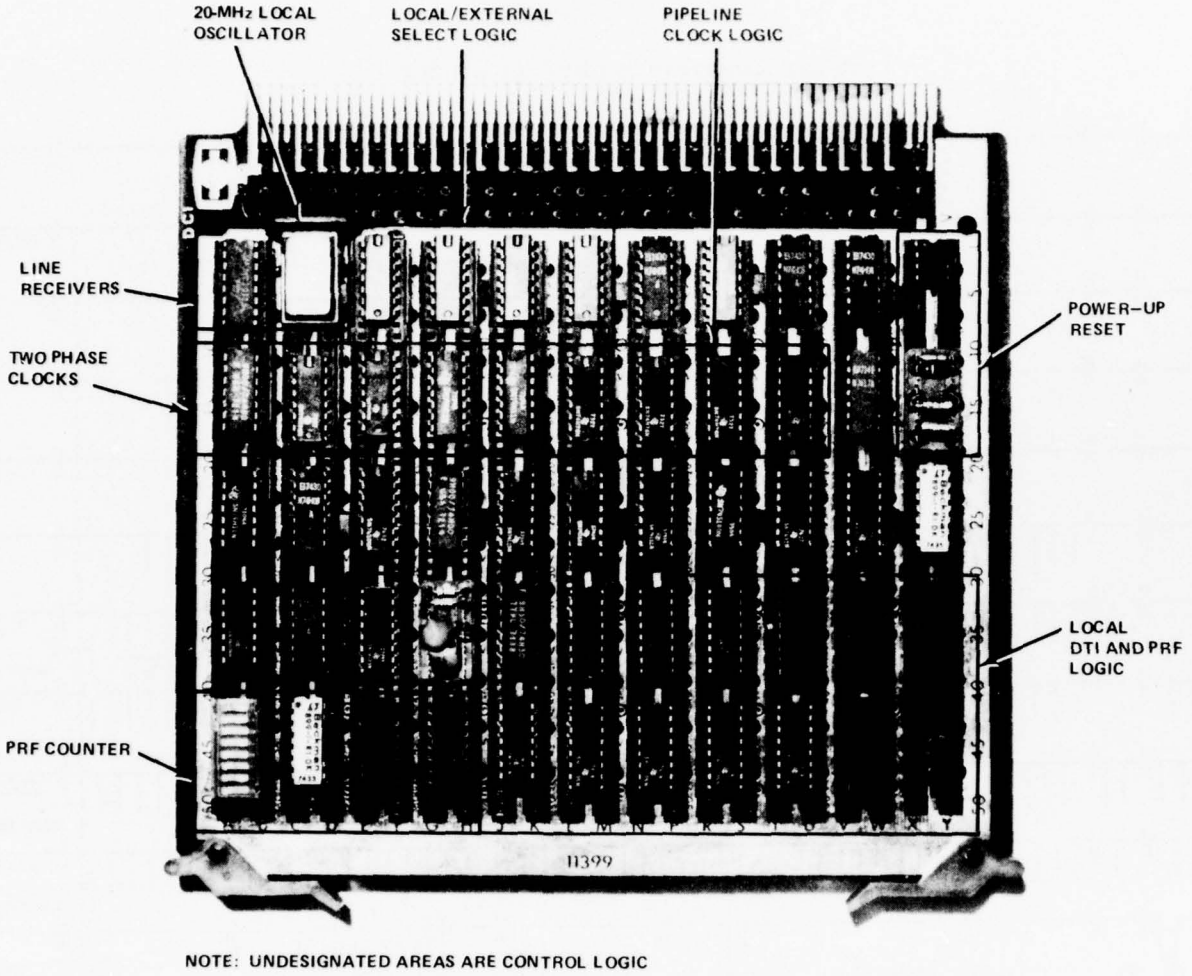


Figure 16. Timing hardware structure.



NOTE: UNDESIGNATED AREAS ARE CONTROL LOGIC

Figure 17. Timing and control socket card.

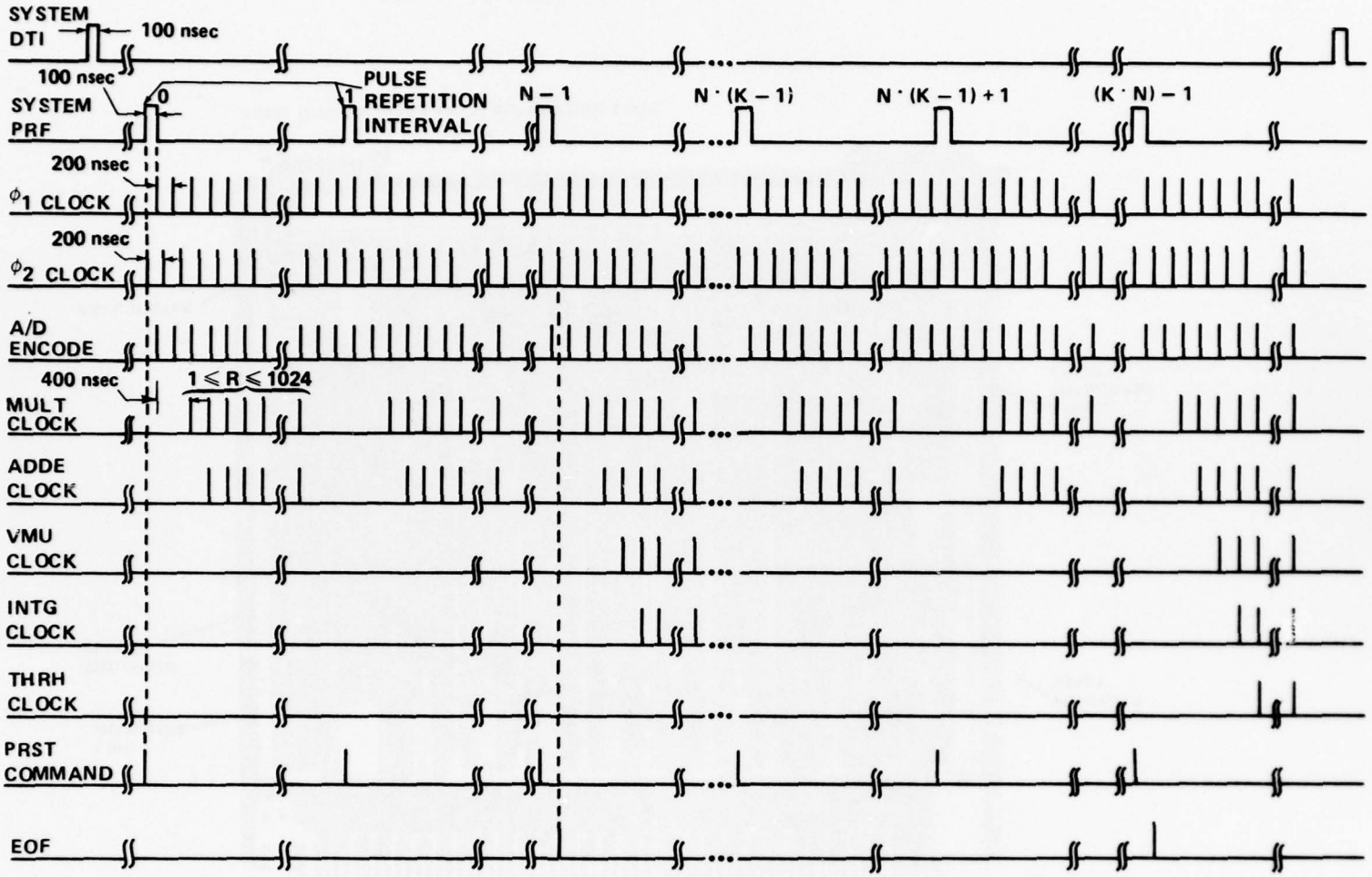


Figure 18. Signal processor timing.

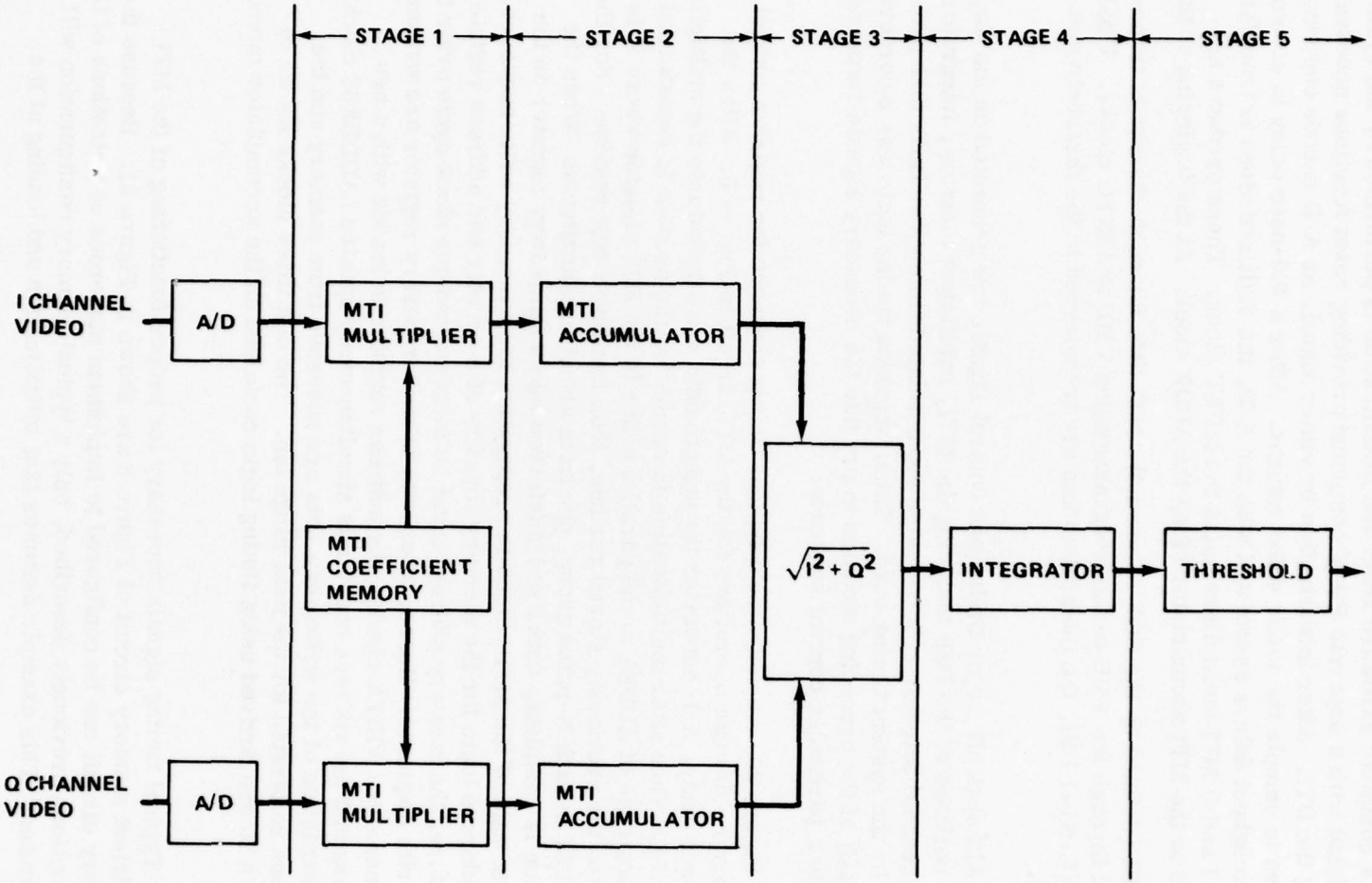


Figure 19. Pipeline stages in PSP hardware.

A complete hardware reset and initialization is performed by the system DTI signal with a separate PRST command providing reset functions necessary during the DTI. After initialization by either signal, an A/D encode command is given to sample the radar video returns. After a 400-nsec delay to account for throughput delays associated with the A/D, the digitized video is transferred to the I and Q MTI multipliers using the MULT clock. These products are passed to the MTI accumulator using the ADDE clock. At the beginning of the N^{th} PRI (defined by the EOF command), MTI data for each channel is transferred through the VMU to the integrator using VMU and INTG clocks. Finally, after (K·N)-1 PRI, the integrated data are transferred to the threshold unit by THRH.

Although all major timing and control signals are generated on the timing card, portions of the PSP including the MTI, coefficient memory, integrator, and threshold detector require more sophisticated timing functions than provided by the system timing card. Thus, separate timing logic was incorporated into each of the preceding modules to provide the necessary signals required to execute a particular control sequence.

Figure 20 demonstrates a typical timing sequence for register control and memory read/write operations for the MTI circuit in Figure 5. After the 400-nsec delay, A/D converter throughput data are strobed into the multiplier (MULT). Then after multiplication is complete, the product is transferred (leading edge of ADDE) to the parallel adder in the MTI pipeline where it is added to the previously stored residue, thus forming a new residue. For the first PRI in each N-pulse group, products are stored unaltered. When the addition is complete, data are transferred into a temporary register on the leading edge of the MTIH clock in preparation for a memory write sequence. The address logic for the memory consists of a counter and address register, therefore, the memory address must be incremented one clock cycle prior to the write sequence. Hence, after data in the temporary register are written into memory (WRITE clock), the address register is loaded with a new address and the address counter is simultaneously updated (ADDRESS clock). On completion of the write, new data are accessed from memory and the process reiterated for the next range bin. The last three clocks shown in Figure 20 are derived using timing logic contained on the accumulator memory card.

Typical timing signals necessary for proper functioning of the MTI coefficient memory circuit of Figure 8 are shown in Figure 21. Because the memory circuit can be configured to implement numerous combinations of the MTI options previously described, only a typical memory configuration will be illustrated. This example assumes that initialization and loading of the

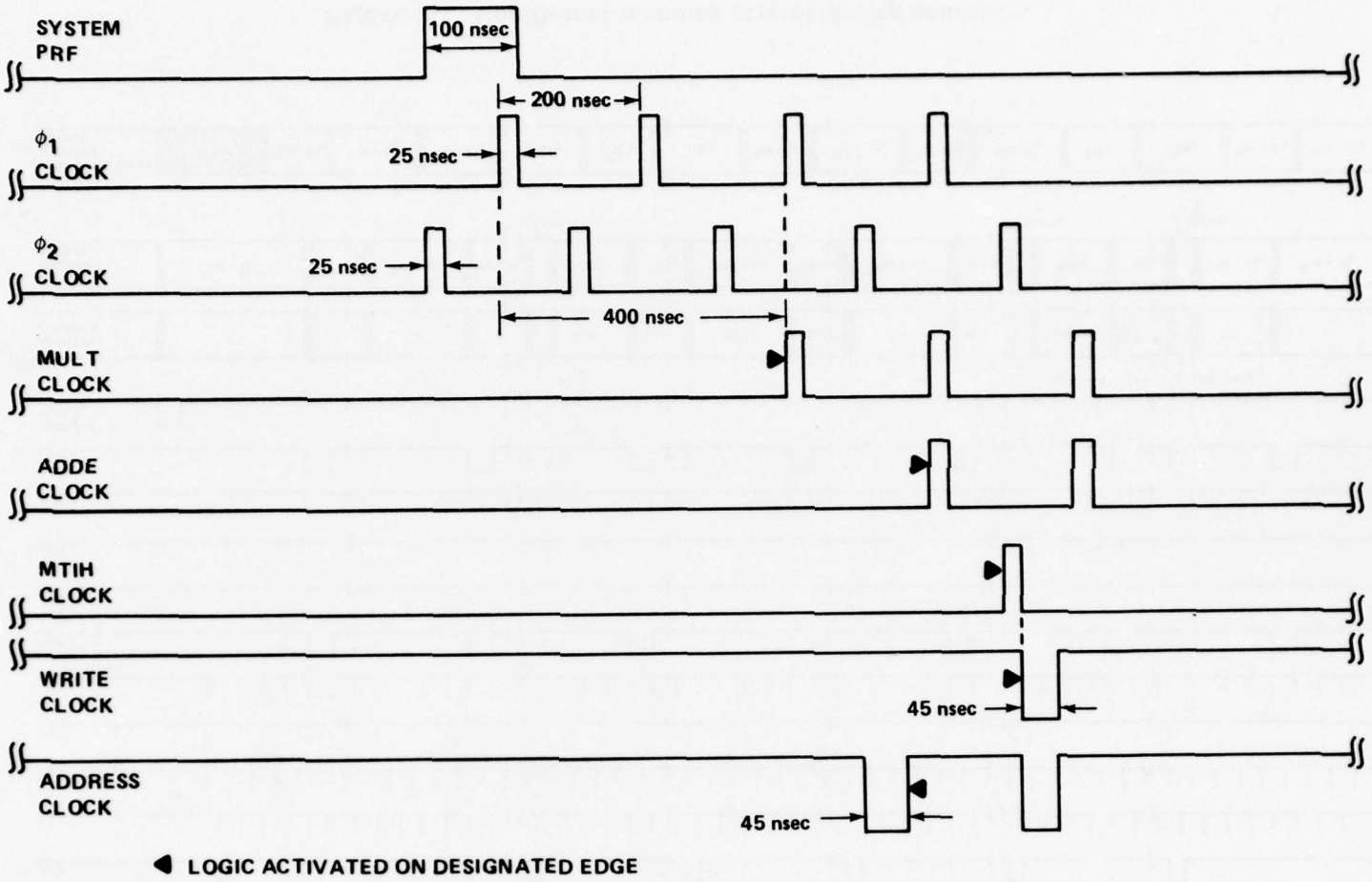


Figure 20. MTI timing sequence.

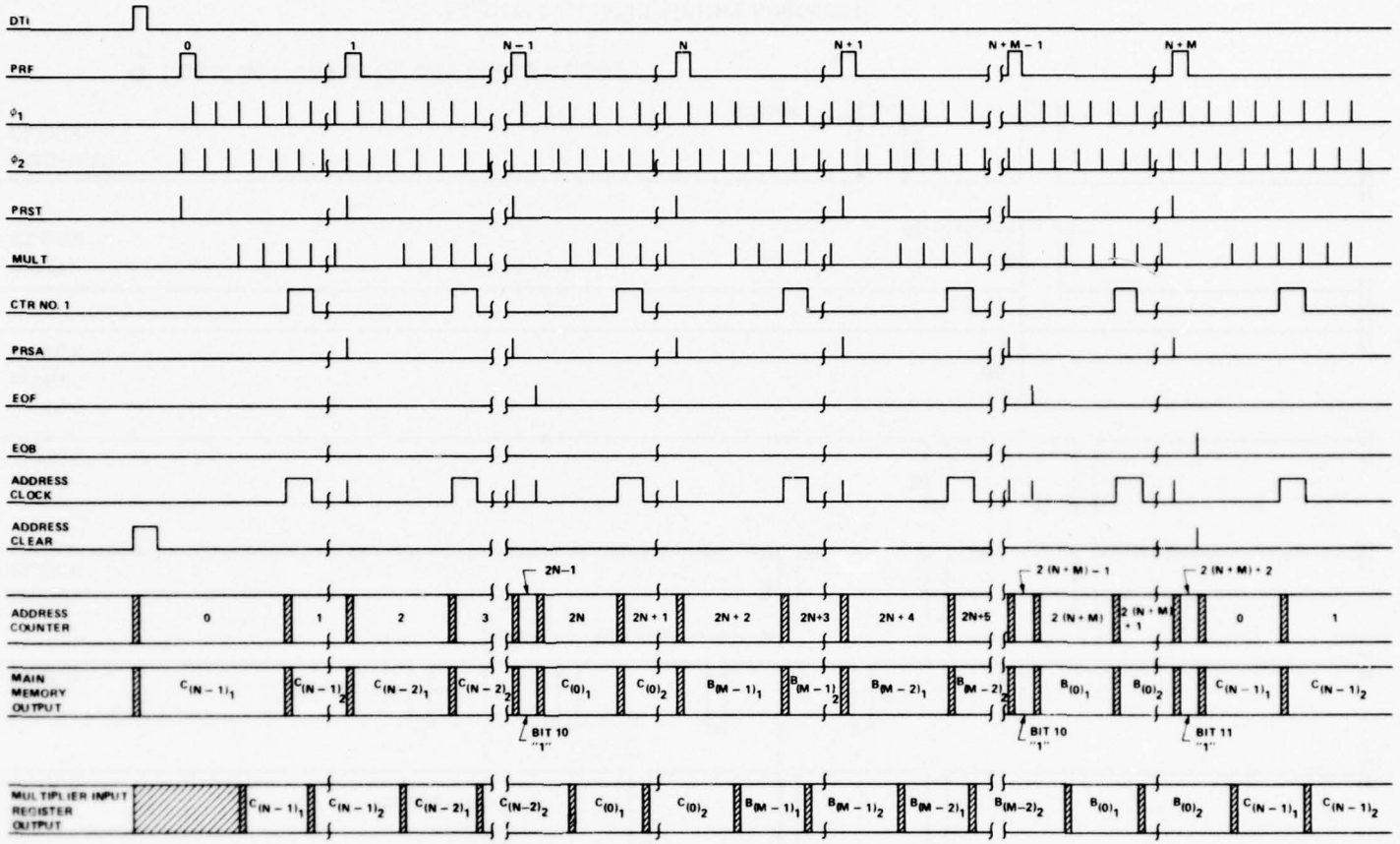


Figure 21. Coefficient memory circuit timing sequence.

coefficient memory circuit (discussed in Volume II) are complete and that the unit is ready for real-time operation. The number of processed range bins will be assumed to be R = 1000, with the first three bins processed different from the remaining 997. That is, there will be two range bin sectors for the example DTI with an MTI_1 containing multiplier coefficient denoted as C_{n_1} (where n = N-1, N-2, ..., 0 for the first sector) and MTI_2 with C_{n_2} (where n = N-1, N-2, ..., 0 for the second). This concept of range bin sectoring is illustrated in Figure 4. Note that although two different filters are being implemented, they have the same order N. The range sectors must always have filters of equal order because of the main memory organization. However, as will be shown in this example, the filter order can be changed within the DTI simultaneously for all sectors. After transmitting N pulses and processing the returns with the coefficient set $\left\{C_{n_1}, C_{n_2} : n = N-1, N-2, \ldots, 0\right\}$, the returns from the next M transmissions are processed with the set $\left\{B_{n_1}, B_{n_2} : n = M-1, M-2, \ldots, 0\right\}$, which defines a new MTI_1 and MTI_2 of order M. The two sets of coefficients are alternated until (N+M)K/2 pulses have been transmitted, thus completing the DTI. When the DTI is completed, K-processed pulses will have been integrated for each range bin of each of the two range sectors. The proper load of these coefficients into main memory is illustrated in Figure 22. Bits 10 and 11 of "0" value must be appended to each of the nine-bit coefficients, an end of filter (EOF) word with bit 10 set to "1" must precede the last coefficient in each set of N (or M), and an end of block (EOB) word with bit 11 set to a "1" must be the last word in the load. These bits are decoded and used as clock and control signals within the DTI.

A memory address counter (MAC), two sector counters (SC), and the EOF/EOB decode gates are required to control the clocking of coefficients. One cycle through the MAC and N + M cycles through the two SC are shown in Figure 22. For each beam position, the DTI initially clears the MAC, thereby positioning $C_{(N-1)_1}$ at the memory output because of the zero address. The MAC then counts sequentially, transferring new coefficients to the memory output until cleared by a decoded EOB pulse, at which time a complete cycle has been traversed through the 2(N + M) stored coefficients. The MULT clock actually transfers coefficients from the memory output to the multiplier input and causes each coefficient to be used a number of times between MAC counts. Clock signals for the MAC are generated with an "OR" combination of the decoded EOF signal, a PRSA clock, and SC No. 1 and SC No. 2 outputs. As can be seen from Figure 21, PRSA is nothing but PRST from the timing and control

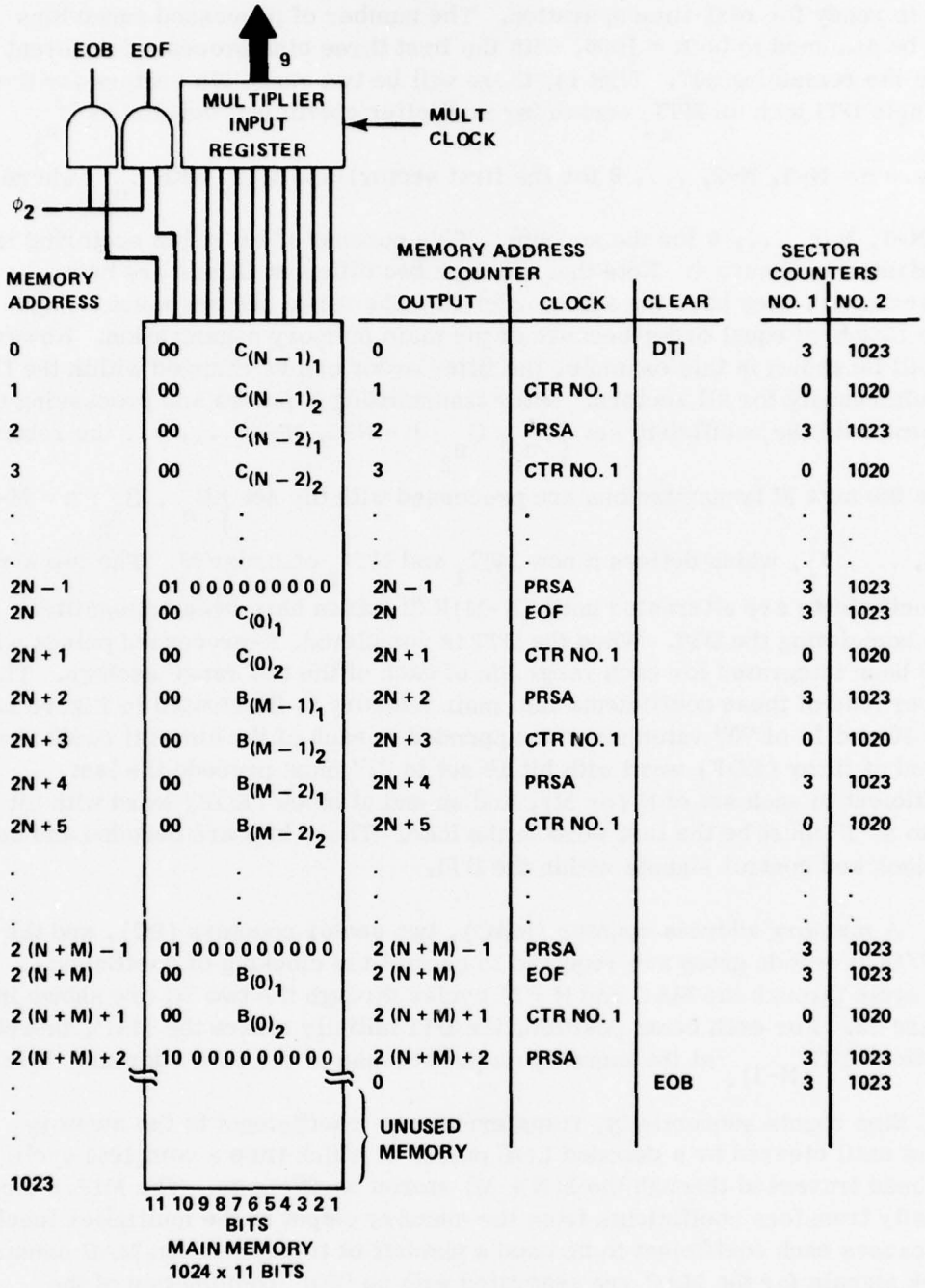


Figure 22. Typical coefficient memory load configuration.

card with the first pulse blanked, whereas the SC No. 1 and SC No. 2 output pulses (defined as CTR No. 1 and CTR No. 2, respectively) are generated each time the counters reach a zero count.

Comparing Figure 8 with the sequence of clock pulses in Figures 21 and 22, the rationale behind the sector counters and various MAC clock pulses can be seen. First, SC No. 1, which is clocked by the MULT signal, counts the number of range bins in the first sector. When the last range bin in the sector has been processed, the counter will be at zero, thus resulting in a CTR No. 1 pulse that shifts a C_{n_2} coefficient to the memory output to replace a C_{n_1} coefficient. In a similar manner, SC No. 2 counts the total number of range bins in the first two sectors and changes C_{n_2} to C_{n_3} when its count reaches zero. Consequently, for this example, the SC No. 1 input register must be loaded with range bin No. 3 and SC No. 2 with 1023 (the maximum possible count). This maximum value will insure that the count for the second and last sector in the example never reaches zero. Although not shown in Figure 22, the master range bin counter in the MTI will halt MULT pulses and the SC No. 2 will only be at 19 at the end of the 1003 range bins.* The complete sequence of counts are not listed in the sector counter columns. Only the counts at timing corresponding to MAC output changes are given. When clocking is halted at the end of the PRI cycle, the first three range bins will have been processed with C_{n_1}, the following 997 will have been processed with C_{n_2}. The processor will remain in a dormant state until the next PRF pulse. The PRF reloads the sector counters with 3 and 1023, respectively, and generates a PRSA clock that transfers $C_{(n-1)_1}$ to the memory output to replace C_{n_2}. The only remaining type of clock signal is EOF which occurs when bit 10 is "1". It is used to signal the MTI that the last coefficients in the filter, C_{0_1} and C_{0_2}, will be transferred to the multiplier next, and that an MTI residue is to be output to the VMU after these two coefficients are used for processing. The EOF clock must also be used to transfer C_{0_1} to the main memory output because the normal clock, PRSA, was already used to transfer the EOF word out of memory. In addition, the two MAC clear signals are shown: DTI which clears the counter at the beginning of each DTI cycle, and EOB which clears the counter after each cycle through the 2(N+M) coefficients.

*Although R = 1000, the master range counter must be loaded with R + 3 to insure that processing is completed for the remaining pipeline stages when MULT is halted.

Figure 23 shows a typical timing sequence for register control and memory read/write operations for the integrator structure shown in Figure 12. At the beginning of the N^{th} PRI, VMU data are transferred (INTG clock) to the integrator input register where it is added with the previously stored residue forming a new integrator residue for a given range bin. Once addition is complete, data are stored into the temporary register on the leading edge of the INTH clock in preparation for a memory write sequence. The memory write function is identical to the procedure described for the MTI. Data in the temporary register are written into memory, the address register is loaded with a new address, and the address counter is updated simultaneously. After completion of the write, new data are accessed from memory and the process reiterated for a new range bin. The last three clocks shown in Figure 23 are derived using timing logic contained on the integrator memory card.

Figure 24 shows a typical timing sequence associated with the circuit of Figure 14. The integrator outputs are clocked into the threshold detector by the THRH clock. Outputs (ALARM BITS) from the magnitude comparator ("1" for a target and "0" for no target) are written into a memory cell corresponding to a particular range bin by the WRITE clock. Then, the ADDRESS clock increments the memory address for storage of the next ALARM BIT. This cycle continues until R range bins have been processed.

V. DESCRIPTION OF PROGRAMMABLE DATA TRANSFER UNIT HARDWARE

The PDTU was incorporated into the PSP as a multimode interface designed to provide a flexible means of transferring data in and out of the signal processor. Data transfer requirements between the signal processor and external hardware systems are controlled by the PDTU for five operational modes: search, track, measurement, loading, and diagnostics. During local operations which use the manual control console, the PDTU provides loading and diagnostic capabilities. As a subsystem under direct software command from the control computer, the PDTU provides data communications for either of the five operational modes.

A. Hardware Description

As shown in Figure 25, the PDTU is composed of several modules:

1) Console control.

2) Computer communications.

3) Input data transfer.

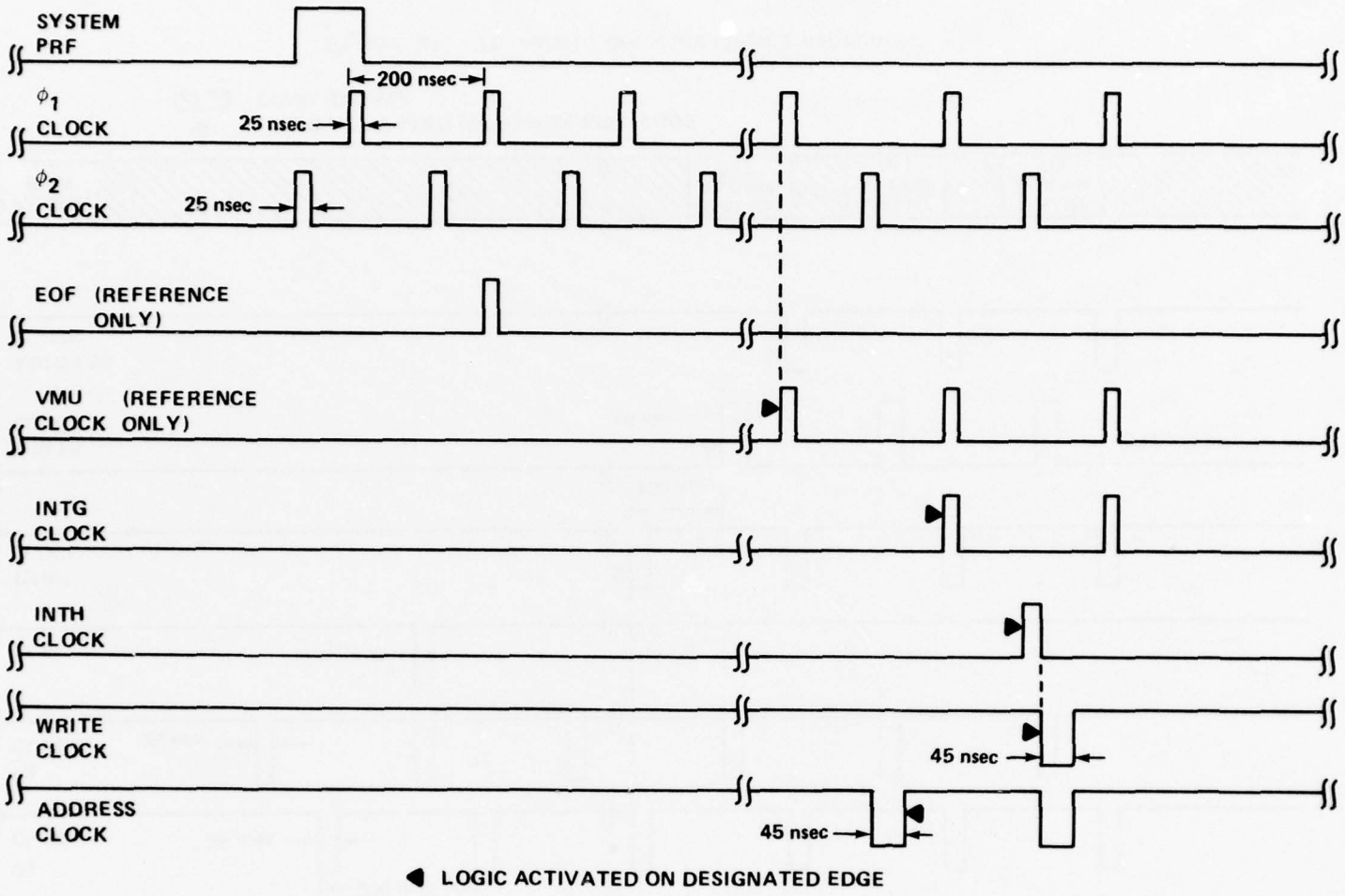


Figure 23. Integrator timing sequence.

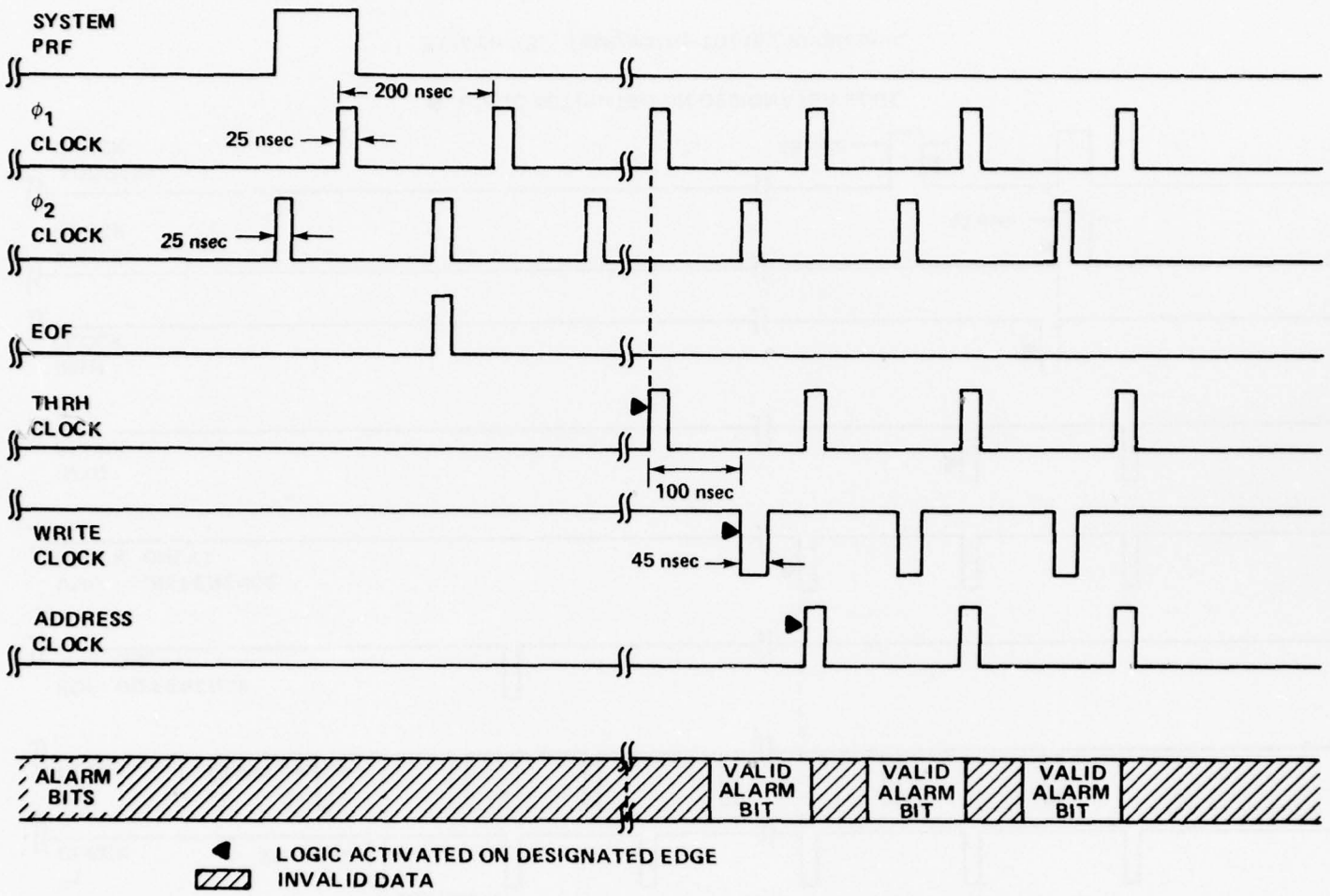


Figure 24. Threshold detector timing sequence.

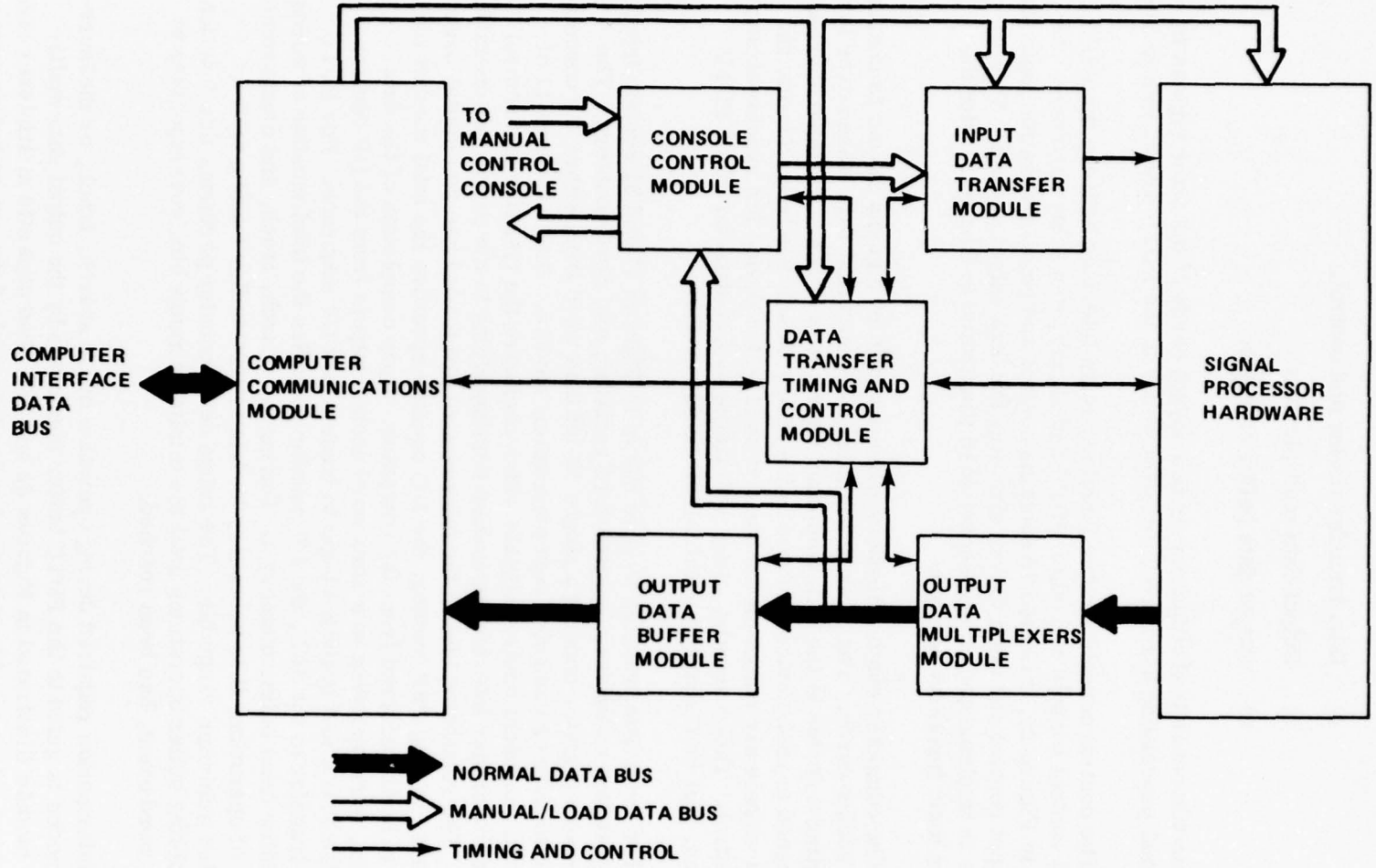


Figure 25. Block diagram for PDTU.

4) Data transfer timing and control.

5) Output data multiplexer.

6) Output data buffer modules.

Each module consists of either one or two socket cards of the same type as in the signal processing hardware. All data words in the PDTU are 32 bits in length.

The control console module functions as an interface between the PSP manual control console and other PDTU and signal processing hardware. As shown in Figure 26, this module contains control and pulse generation logic for data input control and lamp driver circuitry for data output control. This module is implemented on one socket card illustrated in Figure 27 with the various logic functions denoted.

The computer communications module shown in Figures 28 and 29 consists of two socket cards. The module functions as a universal data transceiver for connecting a device to the SEL computer interface data bus. A unique address is assigned to each device attached to the bidirectional data bus. Timing and control signals are output on the bus and used by the device for synchronization and control. These signals, along with timing and control for other PDTU modules, will be discussed in the PDTU timing section.

The input data transfer module shown in Figures 30 and 31 contain input data multiplexers/drivers, micro-word register, and word counters. The micro-word register accepts a single 32-bit data word from either the control console module or computer communications module. Bits 0 through 11 of this word represent control signals which configure the transfer and control module for proper interface operation corresponding to the particular operating mode. The remaining bits in the micro-word are loaded into two digital down counters. During PSP loading, the I/O counter specifies the total number of words to be transferred from the computer. Upon completion of the data transfer, corresponding to a zero word count, outputs from the I/0 counter reset the PDTU and initialize logic to begin a new I/0 sequence. For PDTU buffer transfer to the SEL, the I/0 counter specifies the total number of words to transfer from buffer memory 1. During the search, track, and measurement modes of operation, it is necessary to delay PDTU buffer loading until a specified minimum range bin. The range delay counter performs this function by disabling buffer operations until the minimum range bin, corresponding to a zero word count, has been reached.

Information required during operation in the search, track, or measurement modes is gated to the PDTU buffer memories by the output data multiplexer module illustrated in Figures 32 and 33. Two separate multiplexer circuits are used to select specific data for loading into each of the output buffer memories.

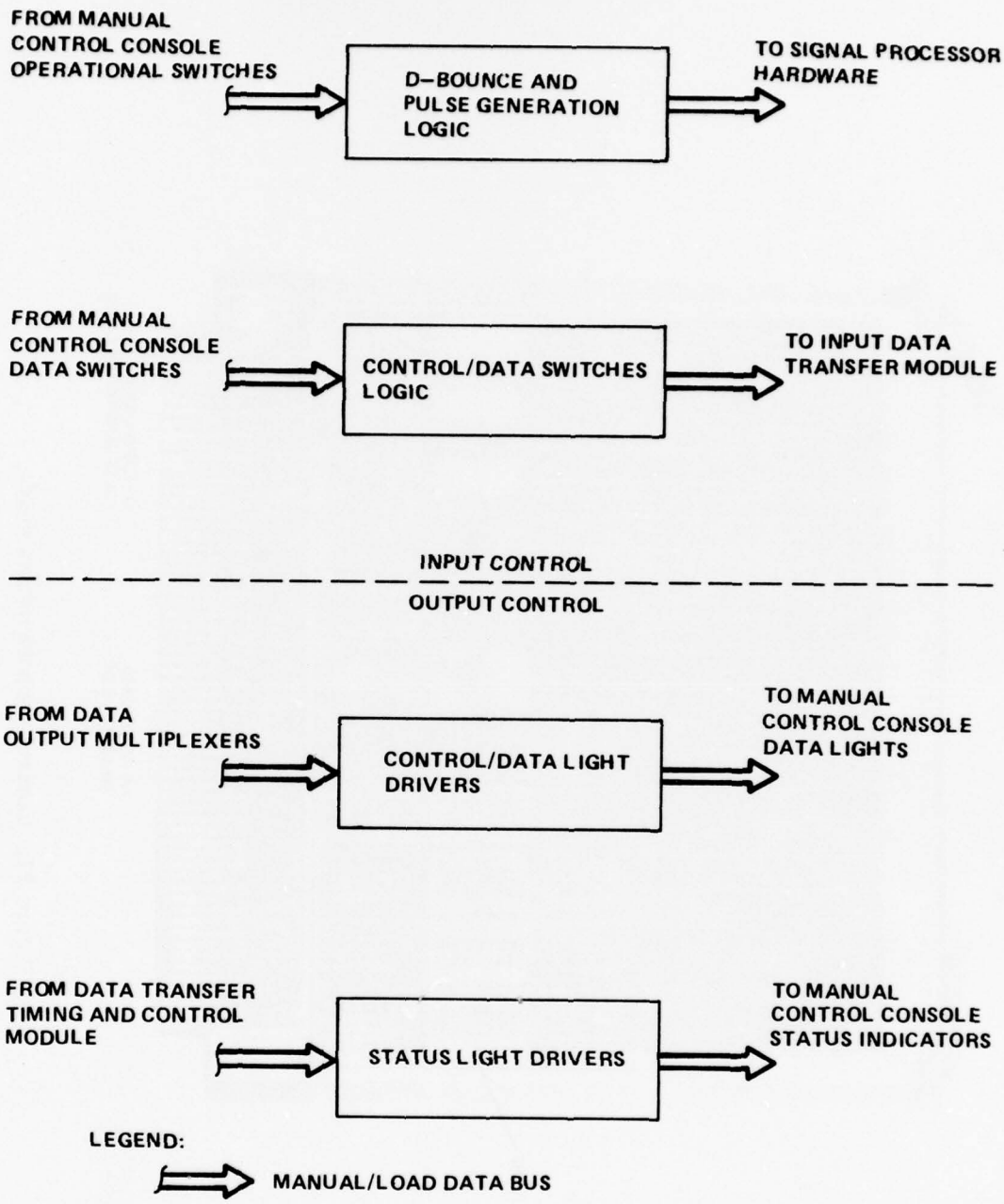


Figure 26. Control console structure.

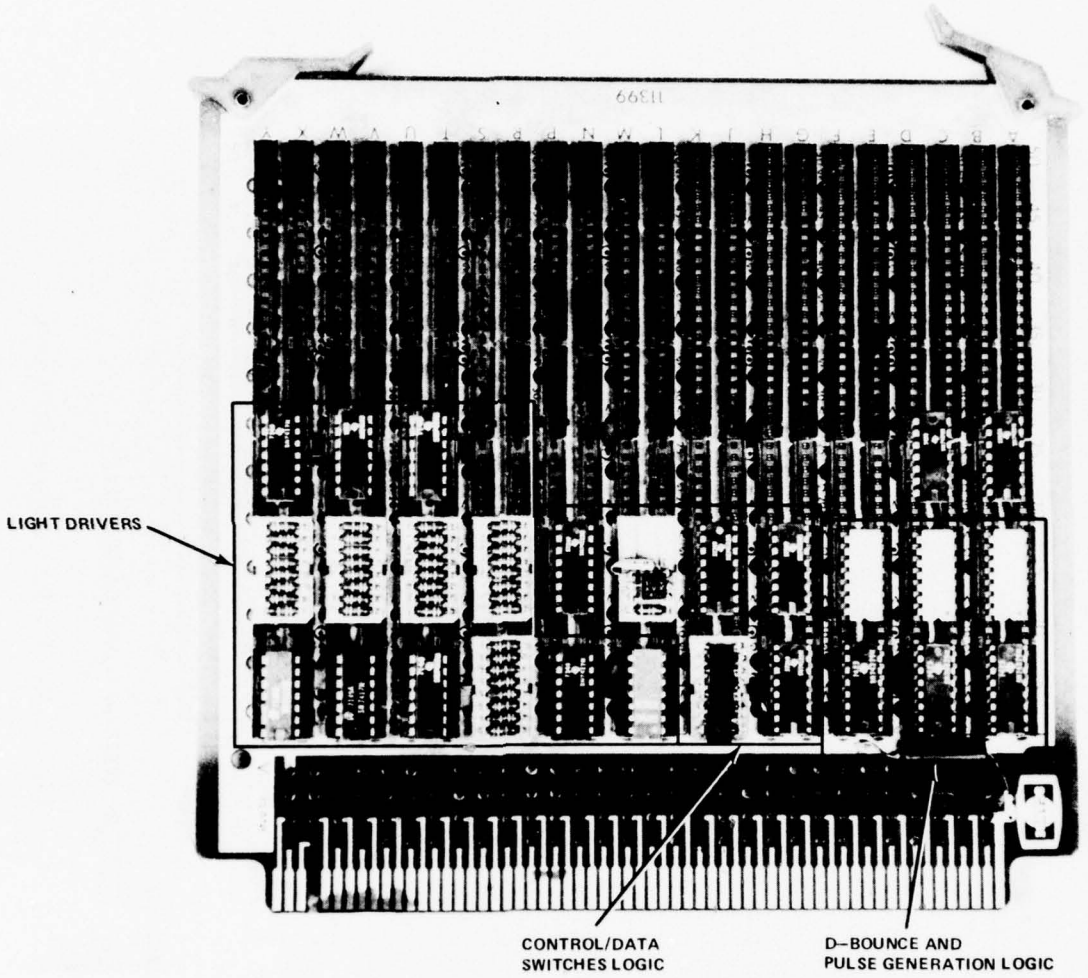


Figure 27. Control console socket card.

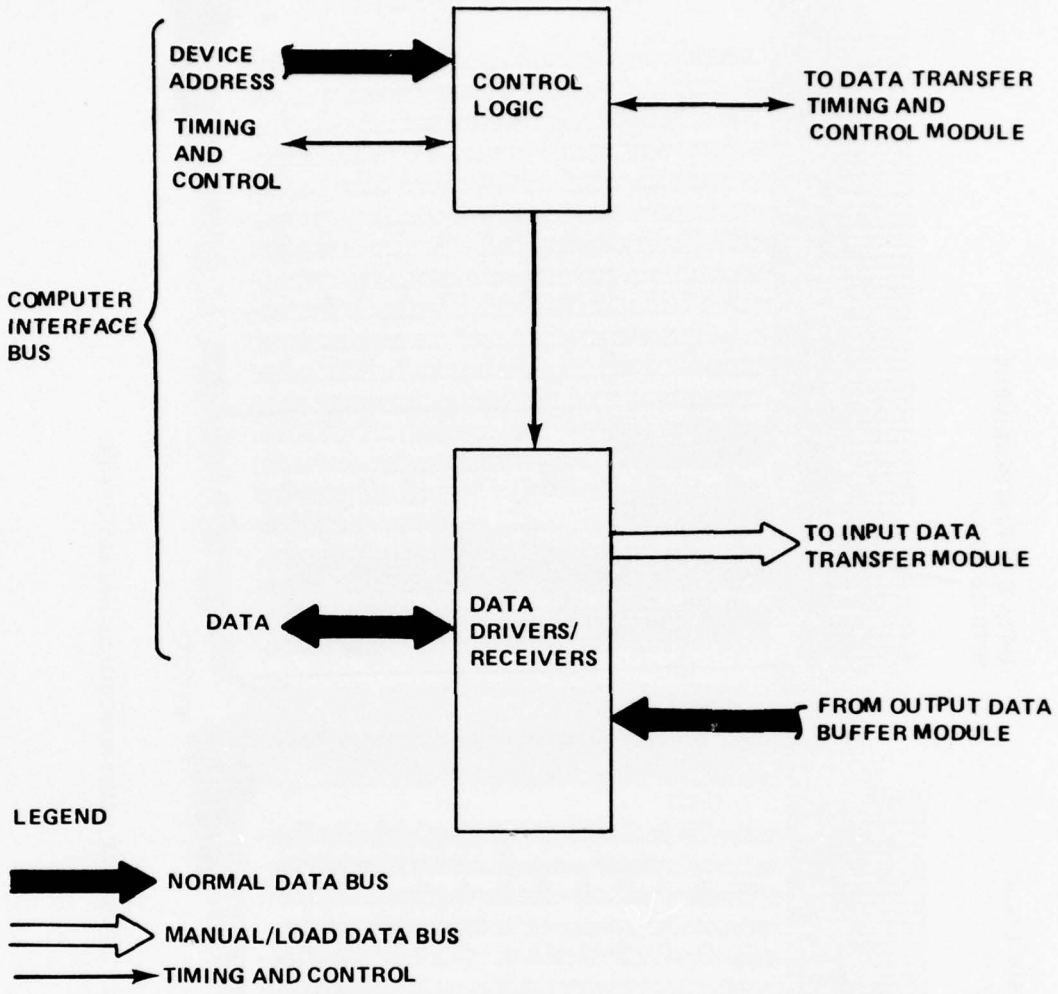


Figure 28. Computer communications structure.

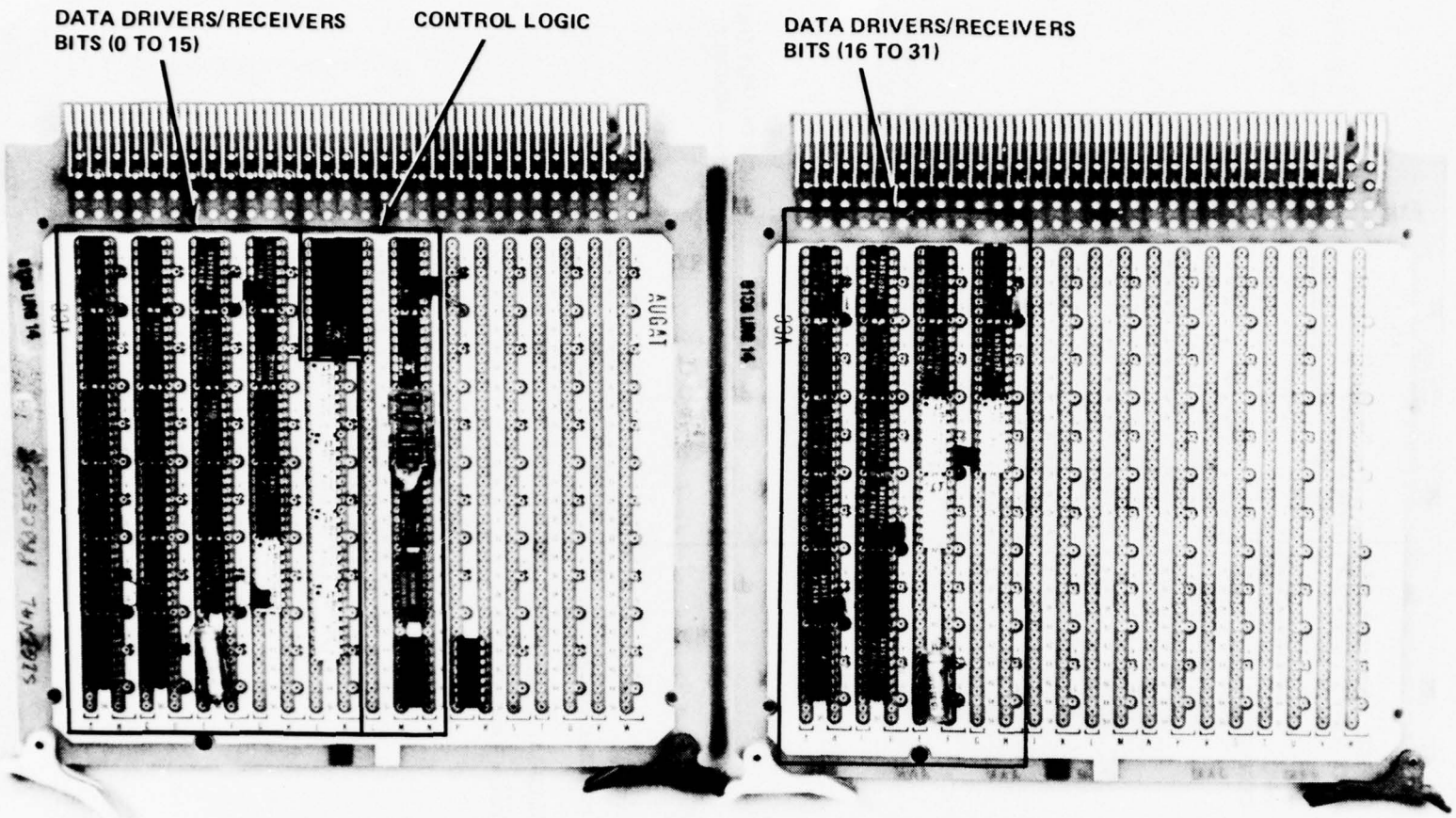


Figure 29. Computer communications socket cards.

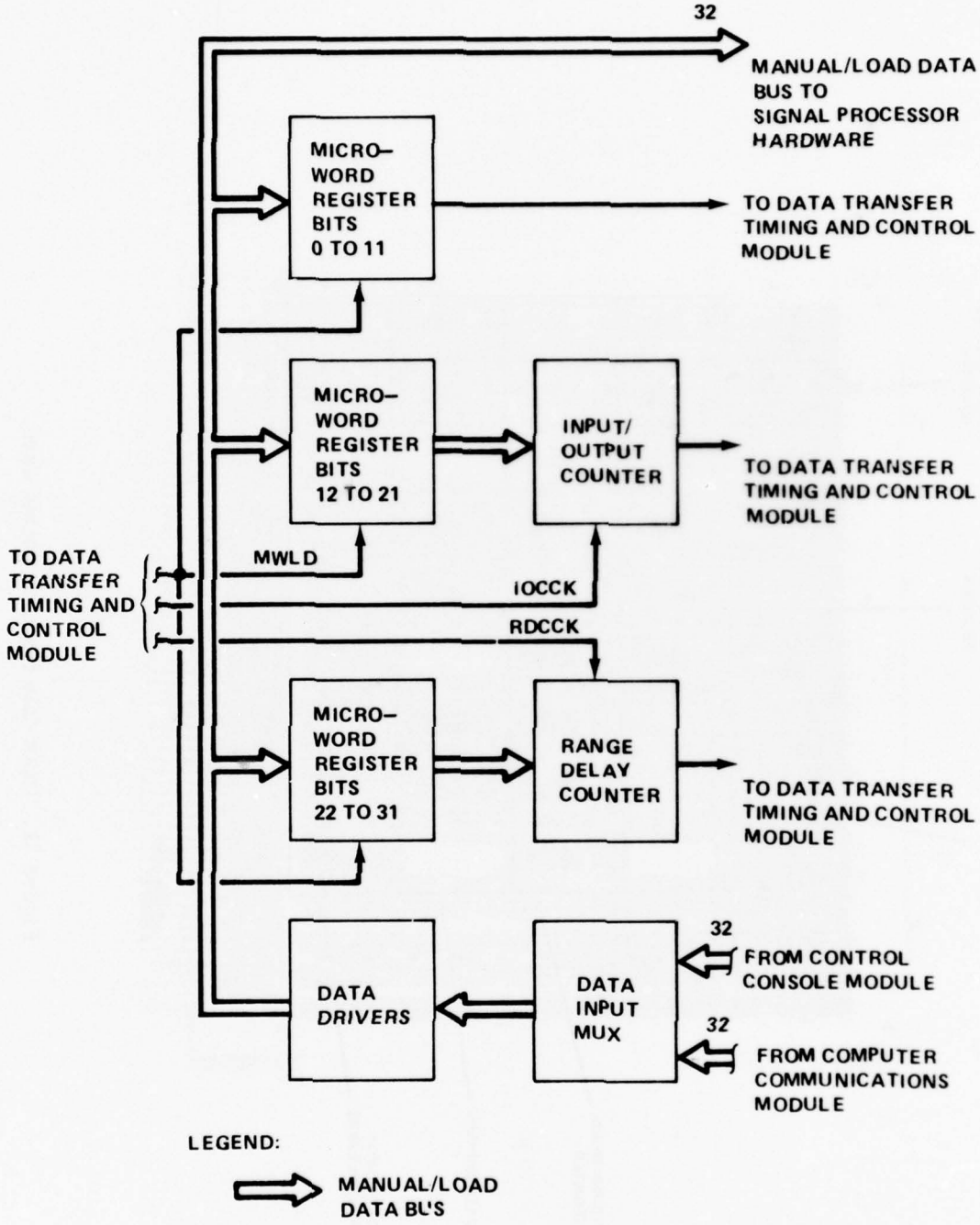


Figure 30. Input data transfer structure.

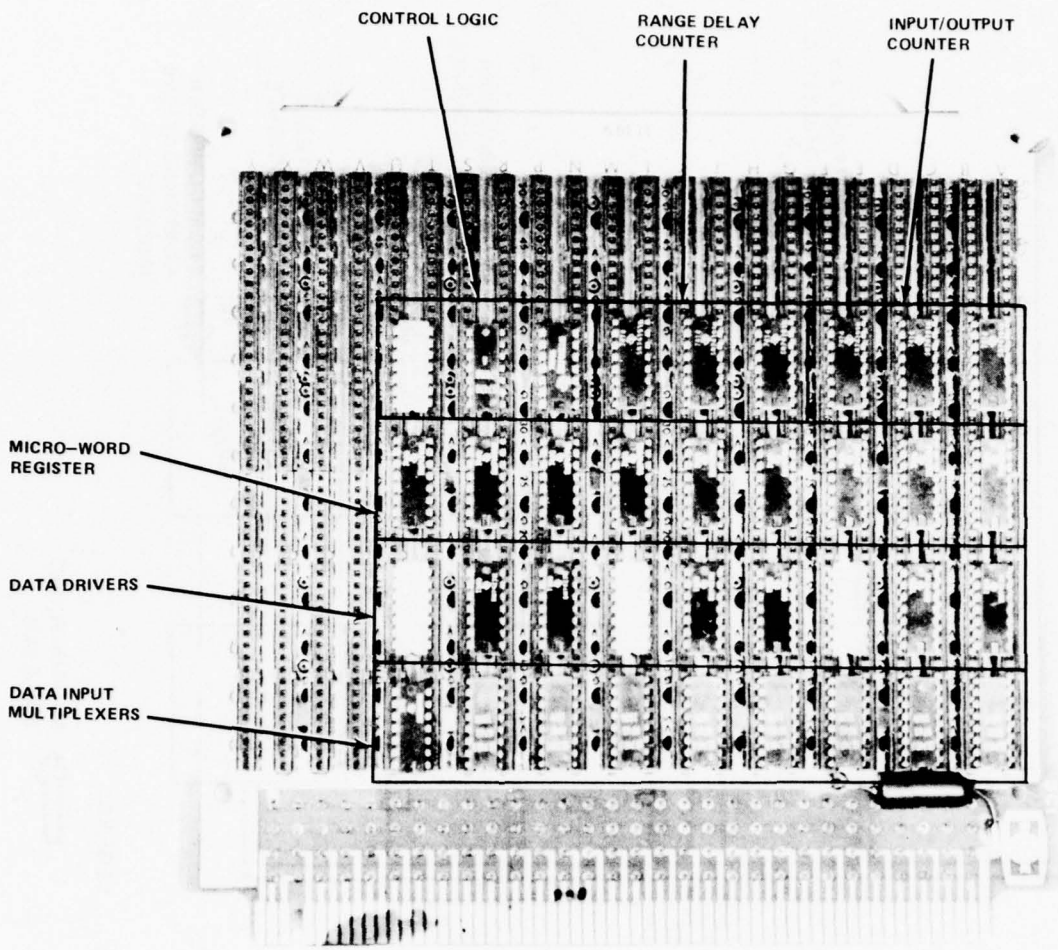


Figure 31. Input data transfer socket card.

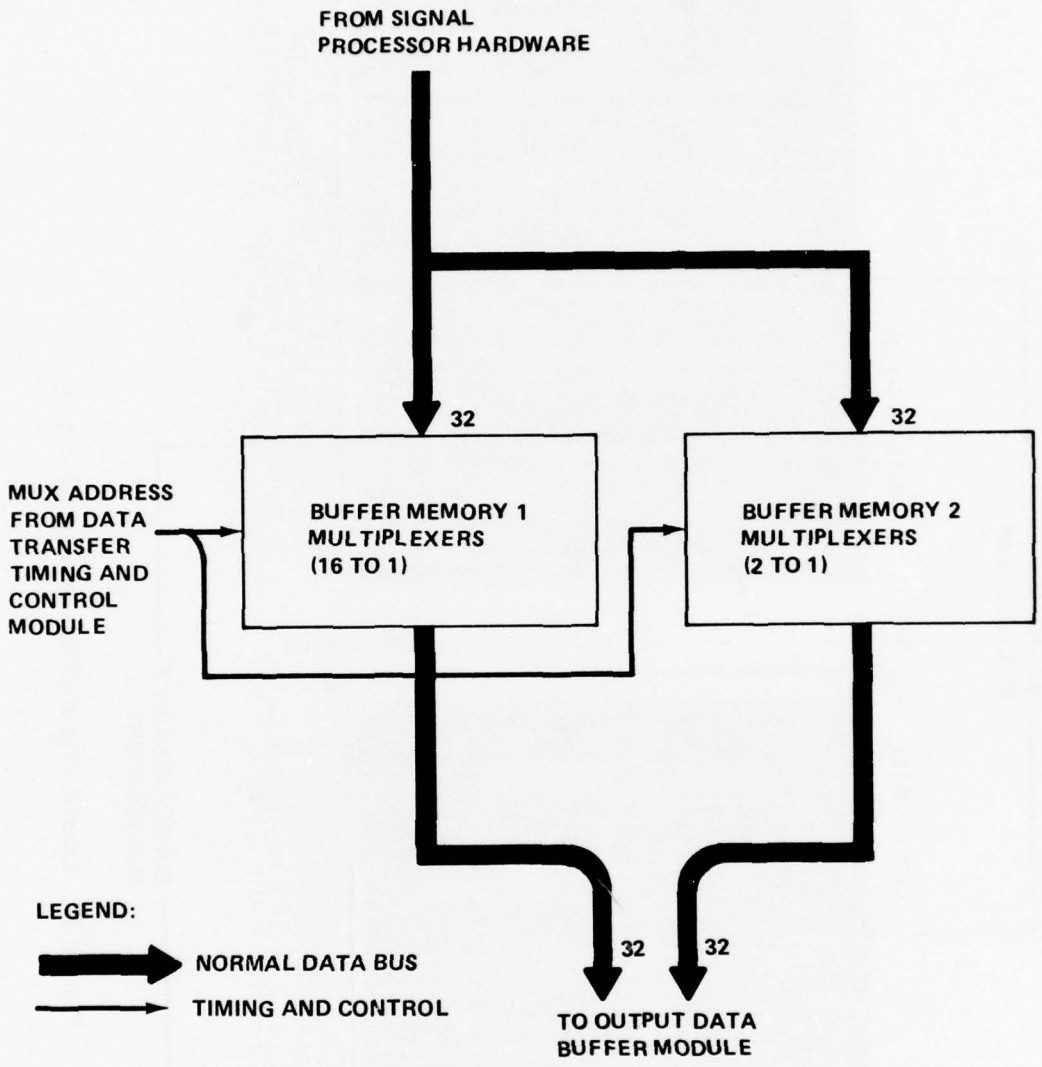


Figure 32. Output data multiplexer structure.

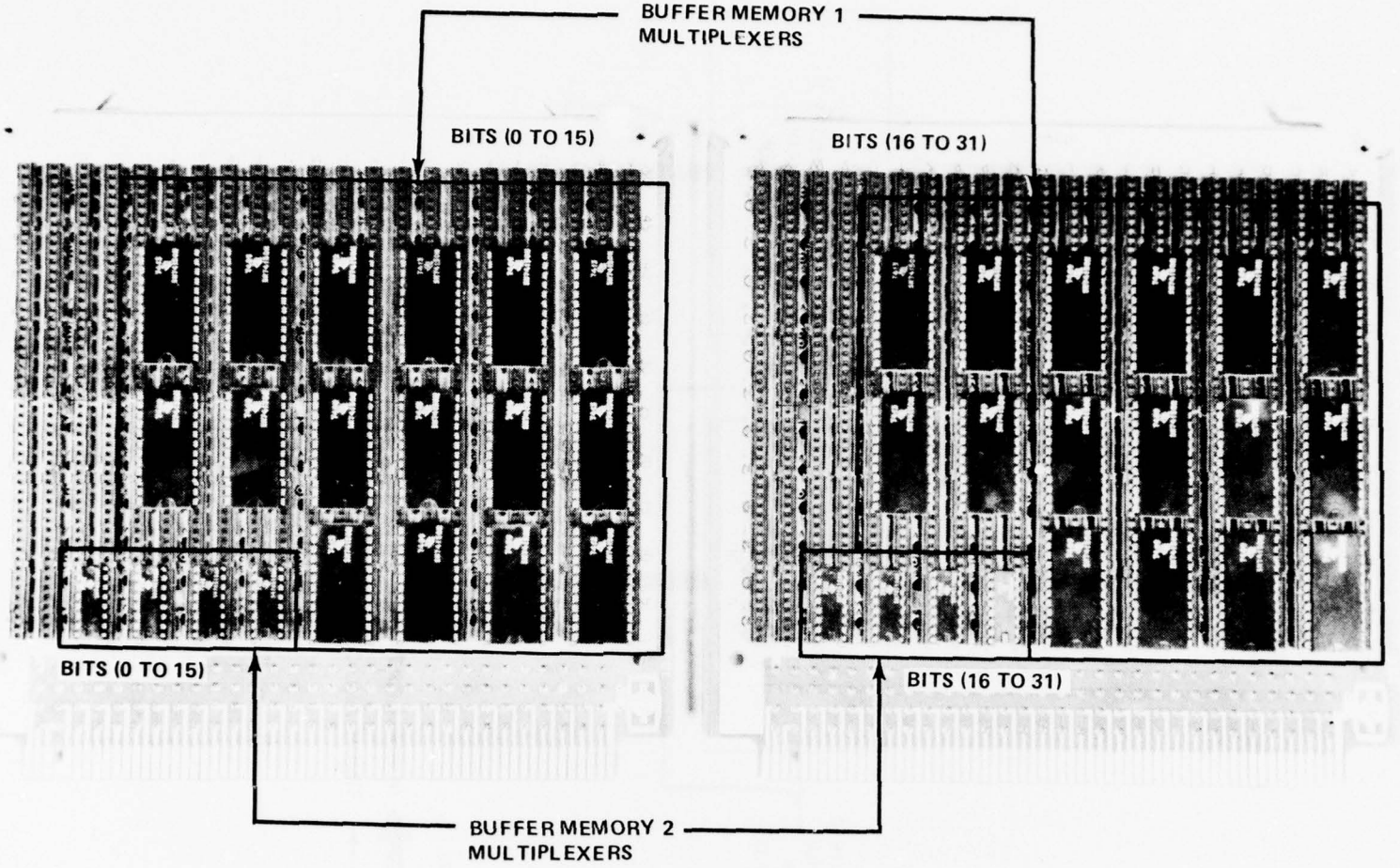


Figure 33. Output data multiplexer socket cards.

The output data buffer module (Figures 34 and 35) stores the selected PSP data into the two buffer memories. Two memory circuits are required because of the necessity of storing simultaneous data from separate signal sources. When the two buffers are loaded, a data ready command is sent to the data transfer timing and control module alerting the SEL computer to access the stored information.

The data transfer timing and control module performs all synchronization and control for the PDTU hardware. As illustrated in Figure 36, the module performs five separate logic functions. These functions consist of digital hardware which synchronizes PDTU timing and controls data flow within the unit as required by the particular mode of operation. In addition, logic is included on the module to format and display the memory address during manual operations involving one of the signal processor memories previously described. Figure 37 shows the timing and control module with the specific hardware functions denoted.

B. Timing and Control

Timing and control functions for the PDTU are formulated for two phases of operation: PSP loading and PDTU buffer memory operations. Timing involving the buffer memories is further subdivided into two categories involving loading and transferring of stored data to the SEL computer for each of the three radar operational modes: search, track, and measurement.

Loading of the PSP will be initiated at the beginning of each DTI prior to the first PRI as illustrated in Figure 38. A data ready signal coming from the output data buffer module is set to a high state at the beginning of each dwell. This enables data to be loaded into the PSP from the computer communications module during each radar dwell.

During the search, track, and measurement phases of operation, specific information beginning with a preselected minimum range bin r_t must be loaded into the PDTU data buffers and transferred to the SEL 8600 to provide a sufficient data base for radar tracking algorithms and general analysis programs. For the search mode, integrator outputs and coinciding range bin numbers for the $(K \cdot N)-1$ PRI are loaded into buffer memory 1 for each detection after the minimum range r_t for up to 64 detections. Timing associated with this process is shown in Figure 39. For the example, $r_t = 3$ and detections

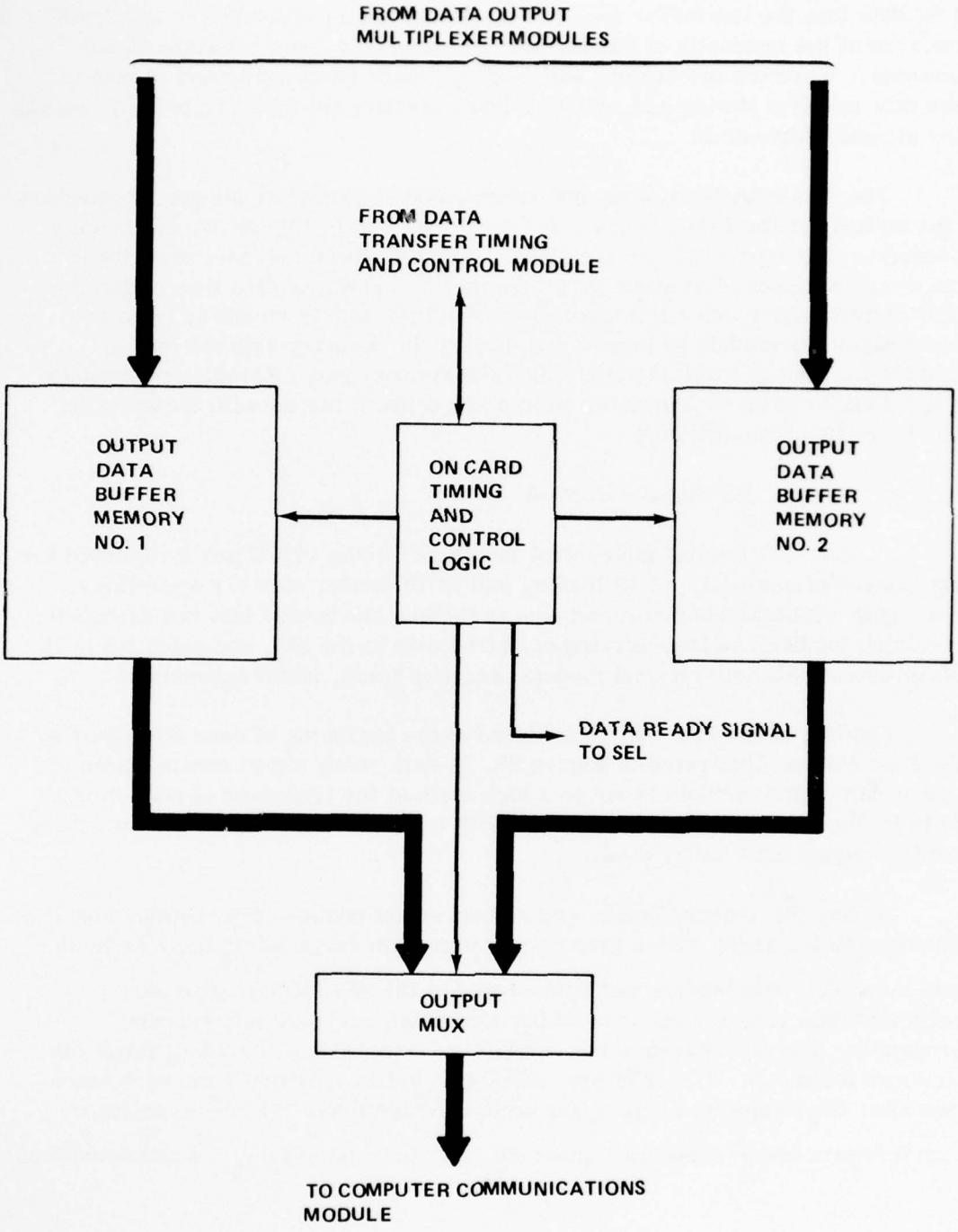


Figure 34. Output data buffer structure.

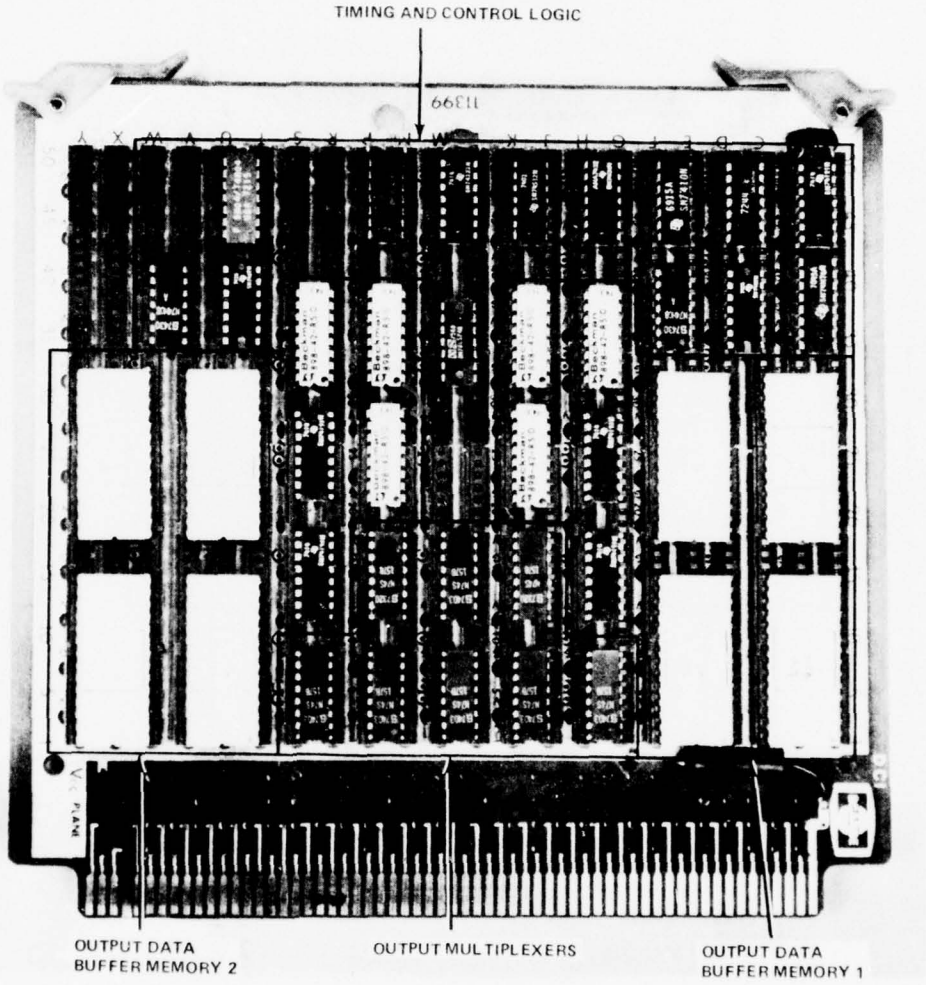


Figure 35. Output data buffer socket card.

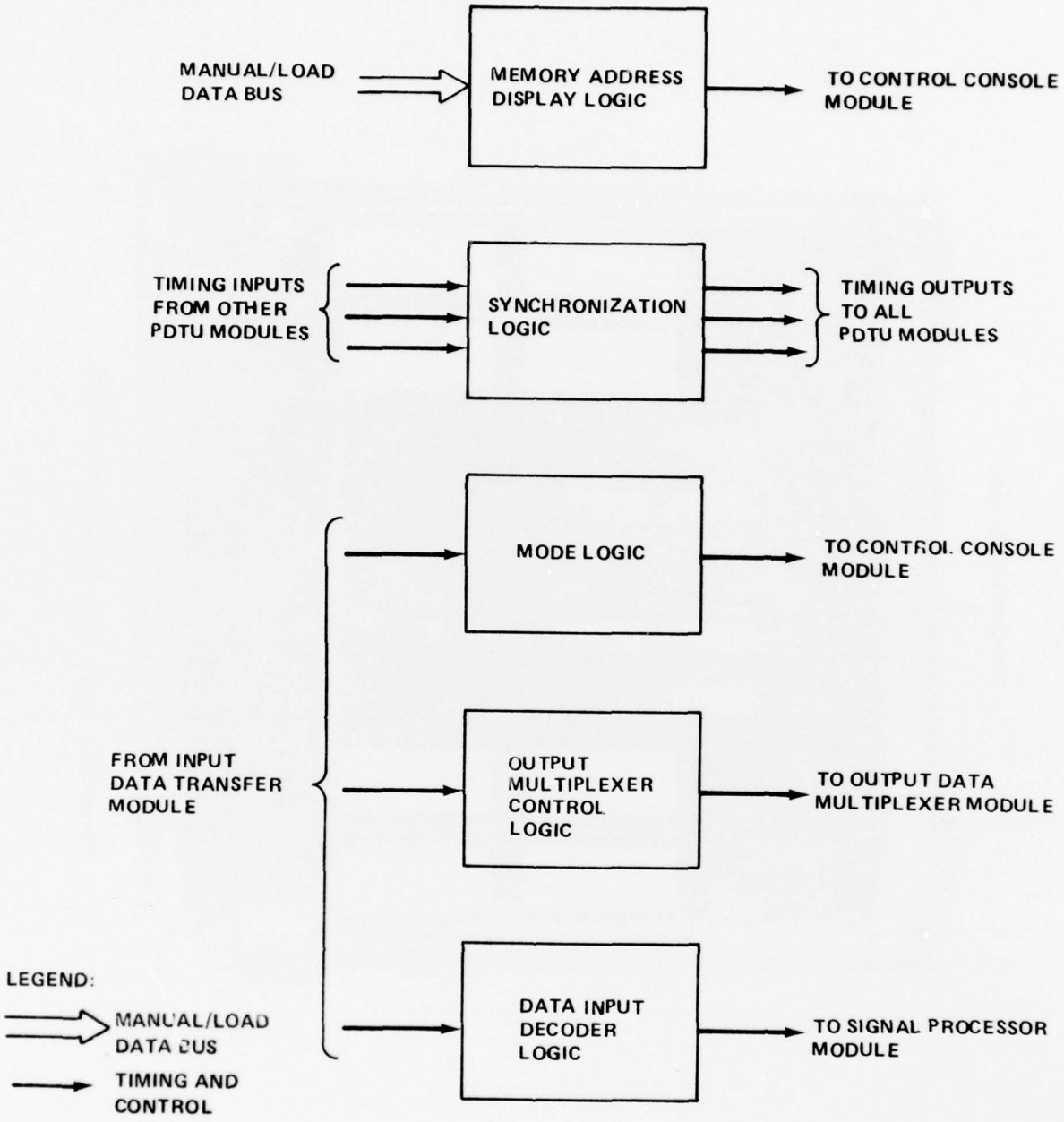


Figure 36. Data transfer timing and control structure.

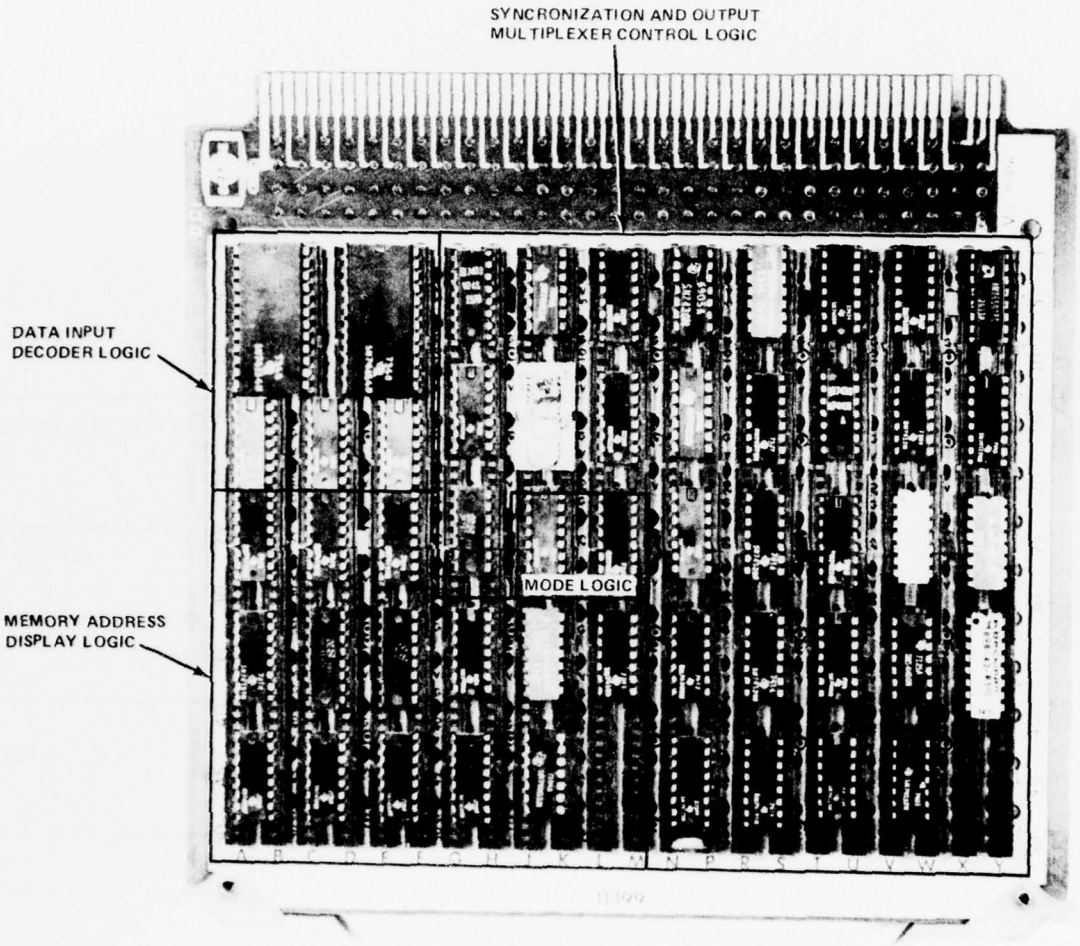


Figure 37. Data transfer timing and control socket card.

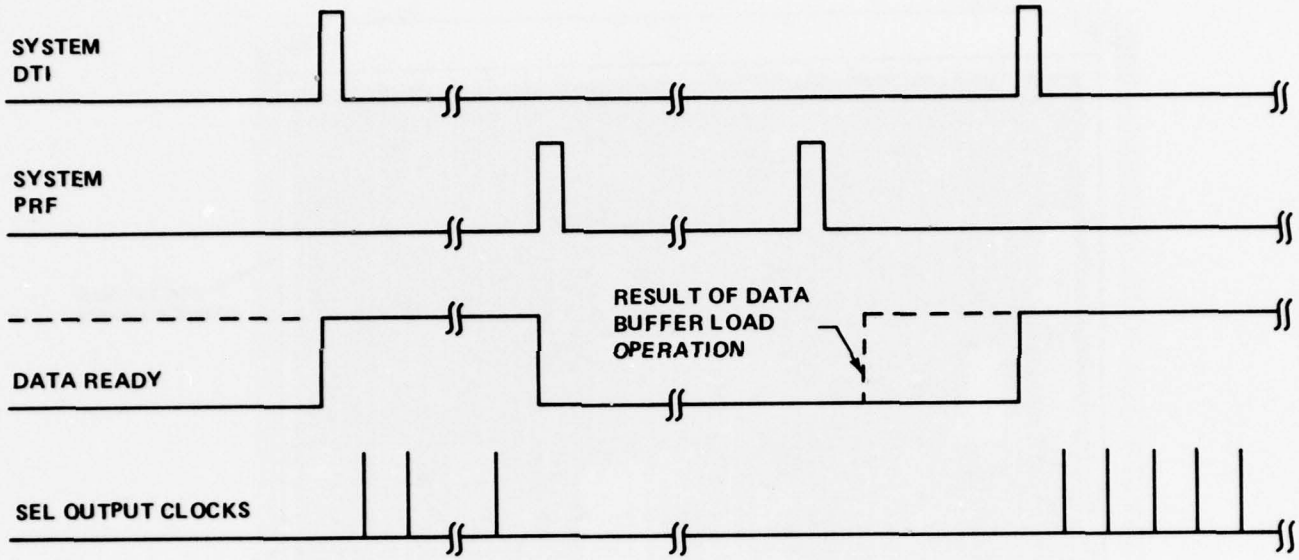


Figure 38. Typical PSP loading sequence.

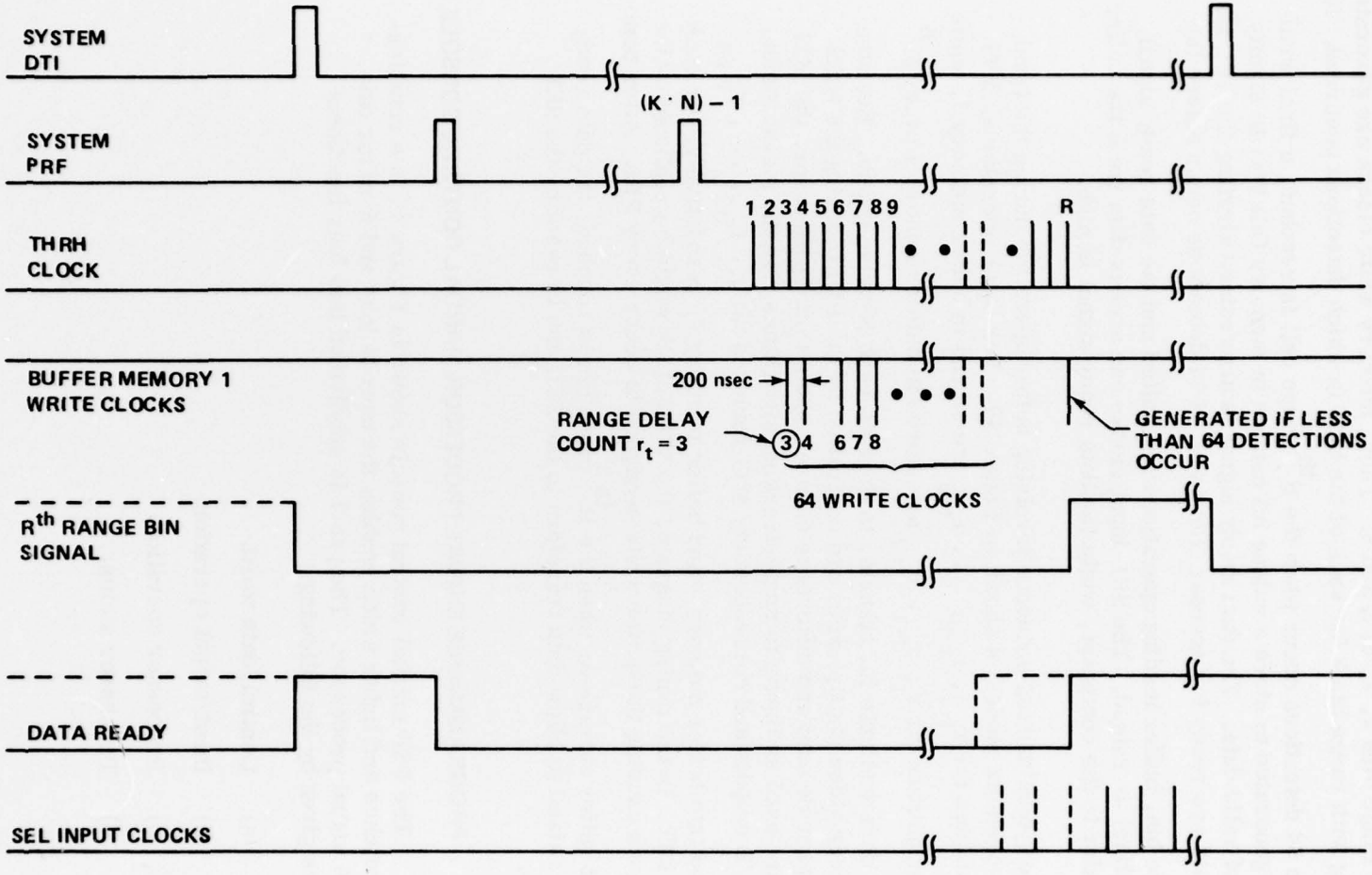


Figure 39. PDTU timing during search operations.

occur in range bins 3, 4, 6, 7, and 8. Thus, memory write clocks are generated beginning with range bin 3 for each of the bins in which detections occurred. If less than 64 detections occur when the R^{th} range cell is reached, a final write clock is generated to store a unique bit pattern in memory (all 0's) to signify the end of valid data. The data ready signal is also raised alerting the SEL that buffer data are ready for access. However, if 64 detections occur before the R^{th} range bin, buffer loading operations are halted and the data ready signal (dashed line) is raised. The SEL input clocks can access data from the buffer for transfer to the computer, while the data ready signal is high.

The typical timing sequence involving buffer operation during the track and measurement modes is shown in Figure 40. For track operations, MTI output samples for r_{t+1}, r_{t+2}, ..., r_{t+8} are stored in buffer memory 1, while integrator outputs for r_t, r_{t+1}, r_{t+2} are stored in buffer memory 2 every N^{th} PRI with data available for transfer to the SEL each N-pulse group. Because the receiver video multiplexers are controlled by the PDTU during the track mode to provide sum and difference channel inputs to the processor, the MTI outputs are used as inputs to angle-tracking algorithms. In the measurement mode, A/D outputs and corresponding MTI residues for r_t, r_{t+1}, ..., r_{t+64} are loaded into buffer memory 1 and buffer memory 2, respectively, for each PRI in a DTI. In the timing diagram, the VMU clock would be replaced by the MULT clock causing the buffer write sequence to occur every PRI. After completion of buffer storage or when the R^{th} range bin is reached, the data ready signal is raised to allow data transfers to the SEL and is reset by the SEL interface.

VI. PROGRAMMABLE SIGNAL PROCESSOR MANUAL CONTROL CONSOLE

The PSP manual control console shown in Figure 41 is a combination of switches and lights which enables the user to load and monitor data within the signal processor. The panel is subdivided into four functional categories given by the following:

a) Control/data word.

b) Input/output operation.

c) Processor operation.

d) Processor status.

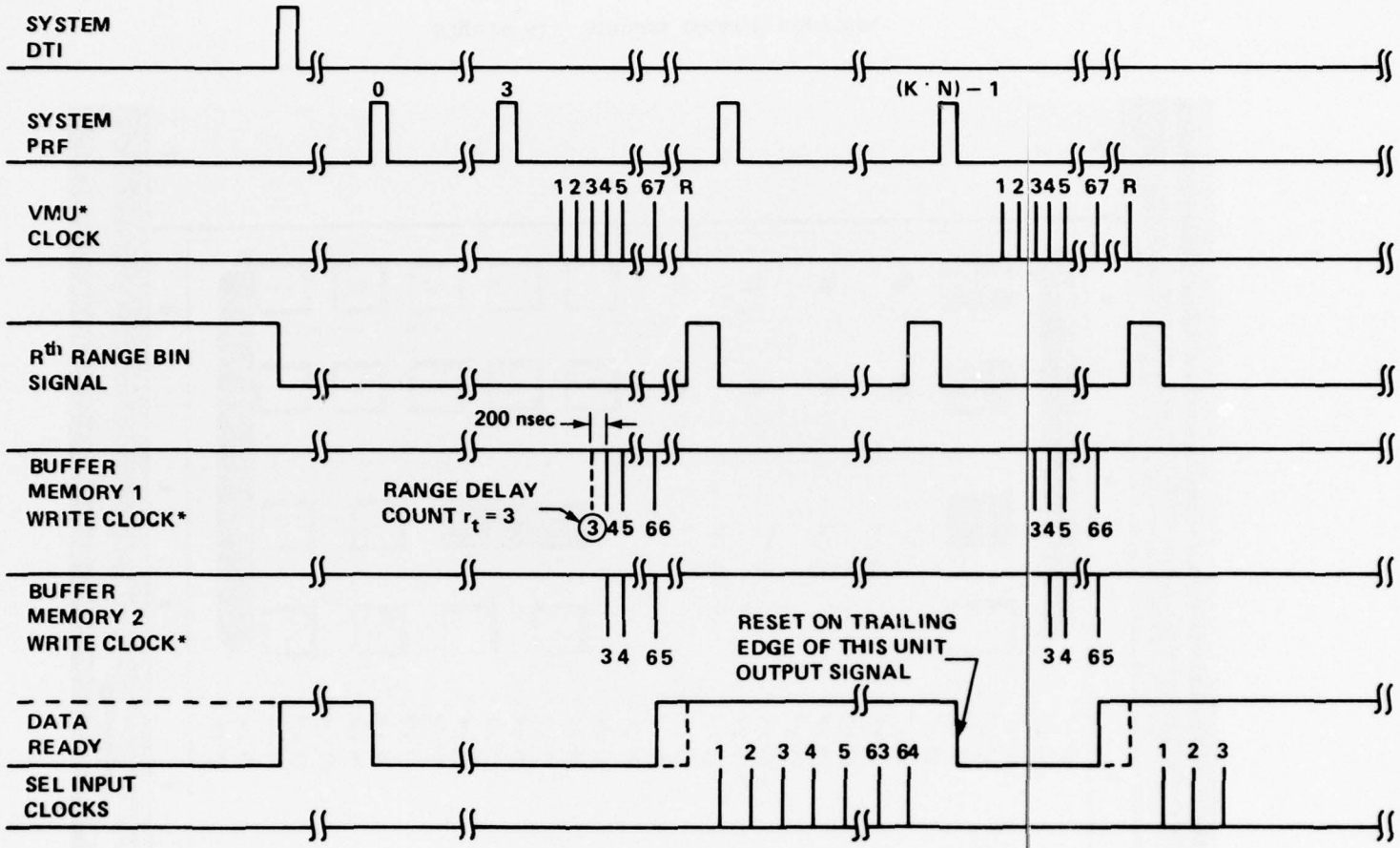


Figure 40. Typical PDTU timing during track operations.

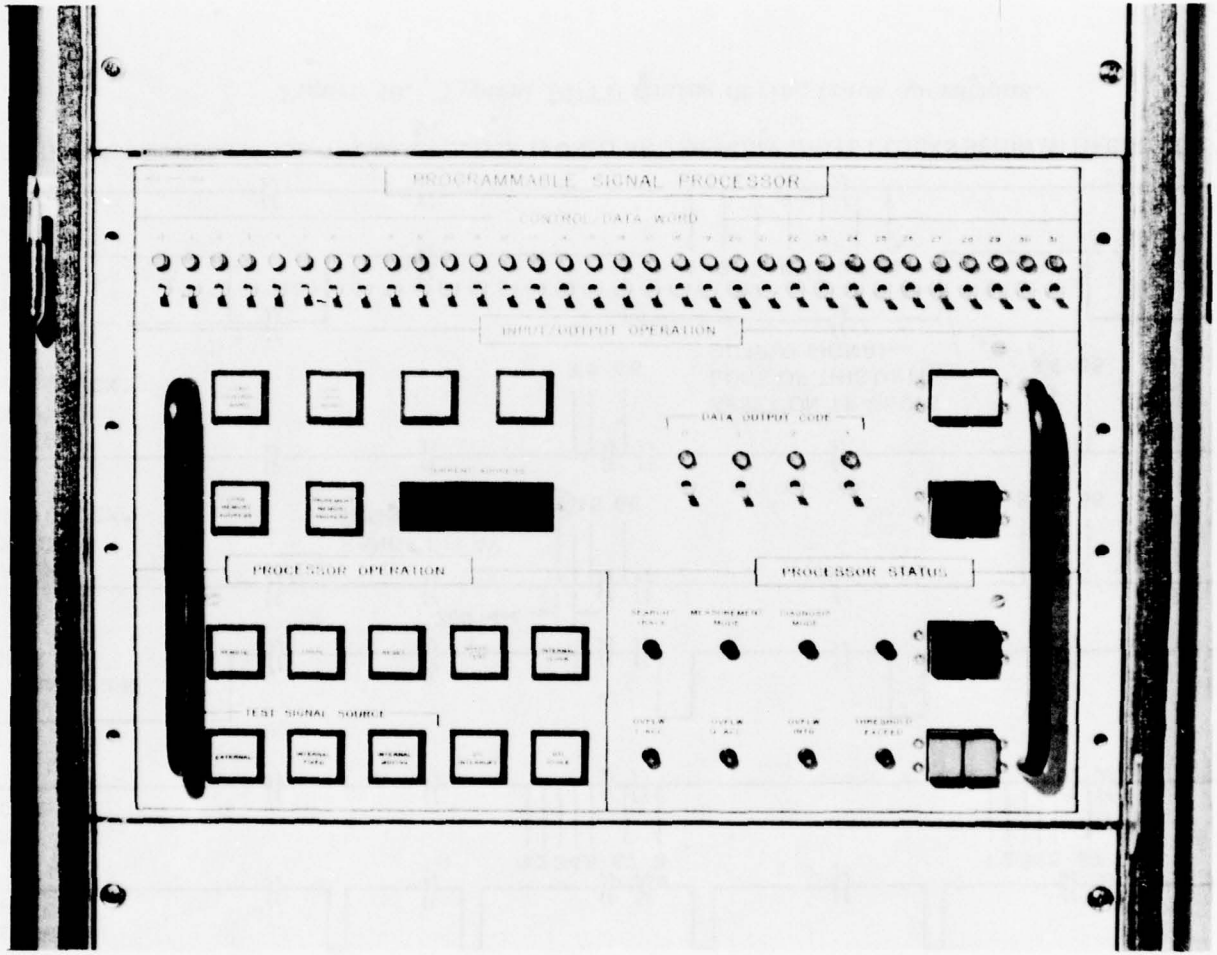


Figure 41. Manual control console.

The control/data word consists of a 32-bit data field which enables the user to monitor internal data or select a word which can be loaded into the PSP as data or a control word.* The control/data section is under direct supervisory control by the I/0 section. This portion of the control panel is split into two functions: (a) data input control (left-hand portion of panel) and (b) data output control (right-hand portion of panel). The input control portion consists of four control switches and a display. Three of the switches operate in conjunction with the data switches and can either load PSP control words, data, or memory addresses. The fourth switch is a memory address autoincrement and, when activated, will update the current memory address by one. The output control portion consists of four toggle switches and functions as control lines to the data output multiplexer offering 16 possible sources of data display.

The processor operational section provides system control for selection of either remote or local operation. In the remote mode, input and output control along with major system timing signals are provided by the PSTG and the control computer. During remote operation, all local control is inhibited, thus eliminating possible errors which could be induced through the manual control console.

Other control functions are provided via the processor operation section for checkout and monitoring during local operation. These switches provide system reset, static data control, and DTI control for three different test signal sources or for normal inputs coming from the A/D converters.

The processor status section is an information display which indicates the operational status of the PSP. During normal operation, indicator lamps display the processor mode and also any overflow condition which might have occurred during the processing sequence.

VII. PROGRAMMABLE SIGNAL PROCESSOR HARDWARE LAYOUT

The PSP logic circuits and associated hardware are housed in a standard 19-in. cabinet. A front view of this cabinet with all the signal processing components is shown in the center of Figure 42.

The PSP is mounted in a slide out chassis which houses the 21 logic cards associated with the PSP. The PSP can be easily extended from the normal mounting position, as shown in Figure 43, to expose all logic components for maintenance purposes. The manual control console can be easily removed from the PSP chassis by removal of four mounting screws and disconnecting the associated signal cable assembly.

*Instructions for use of the manual control console are contained in Volume II.

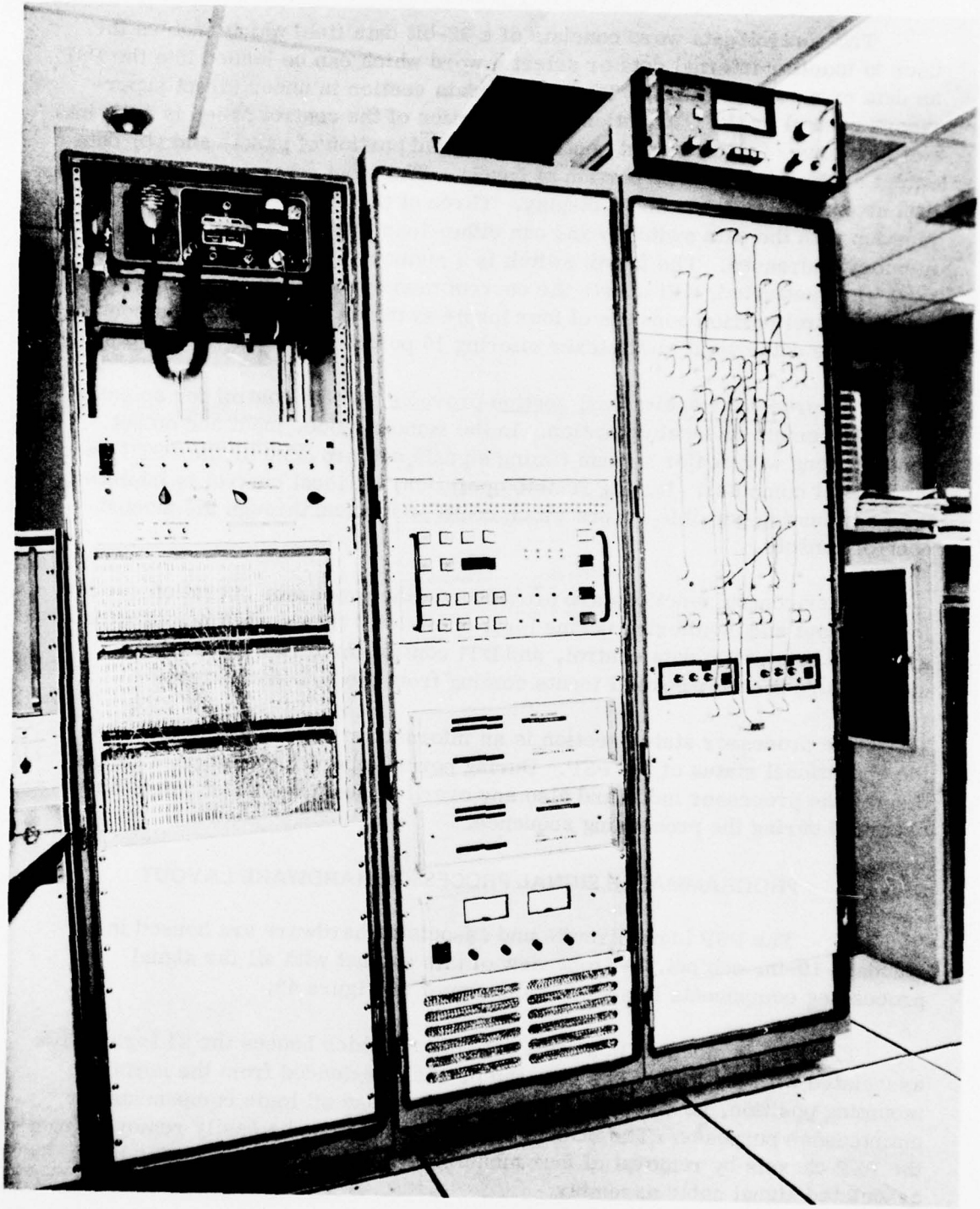


Figure 42. Signal processing hardware.

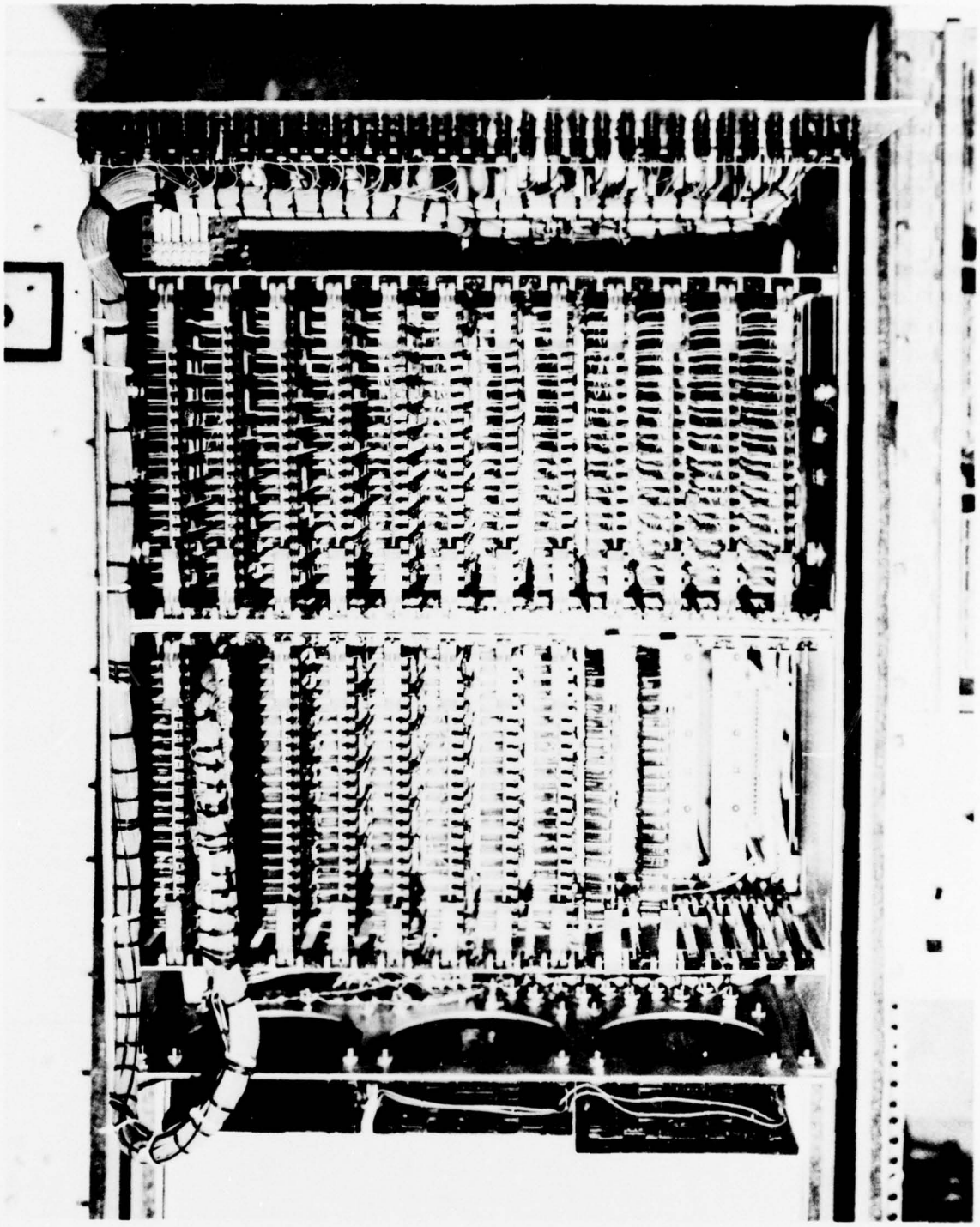


Figure 43. PSP in maintenance configuration.

All external I/0 enters the signal processor from the rear chassis panel as shown in Figure 44. Three 104 pin amp connectors are supplied for data communication between the receiver, PSTG, display, and control computer subsystems. Signals coming from the A/D converters enter through standard BNC connectors.

Logic circuits in the PSP are mounted on standard 8- × 6-in. wirewrap socket cards and arranged in the drawer as shown in Figure 45. Approximately 1000 dual-in-line integrated circuits, ranging from 14-pin to 24-pin packages, are mounted on the socket cards. Standard TTL, including high-speed and Schottky logic, was used for all design implementations with some MECL logic used as line receivers.

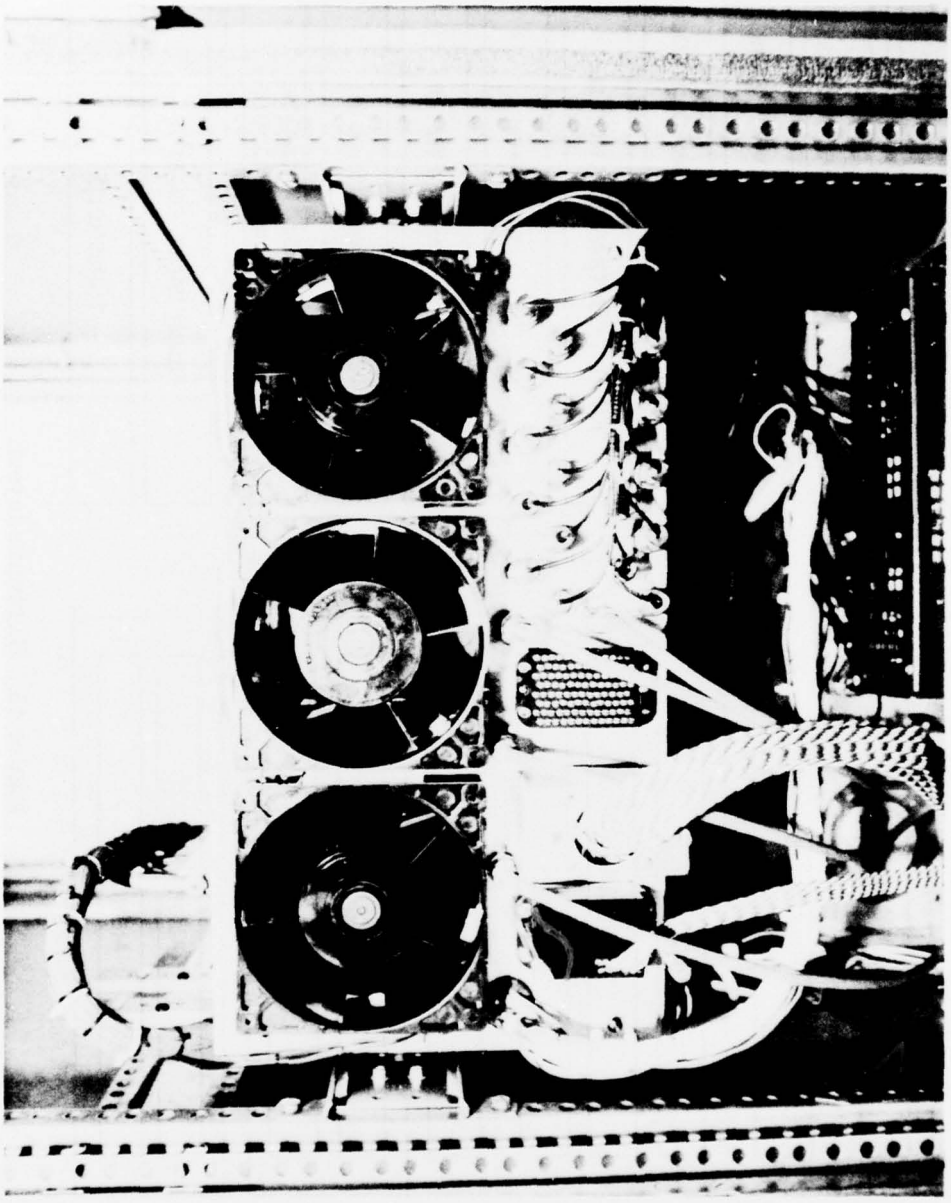


Figure 44. I/O panel.

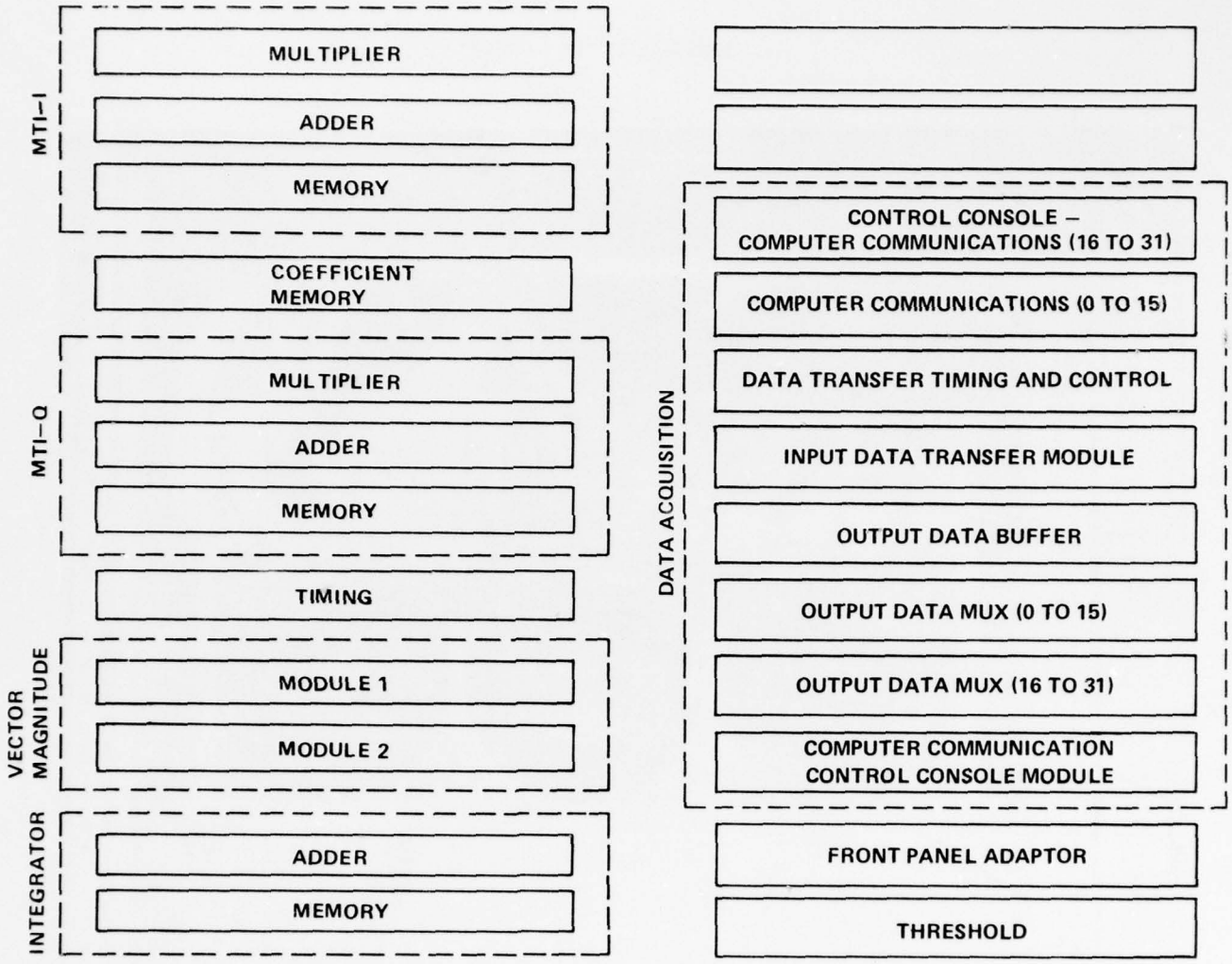


Figure 45. Hardware layout.

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