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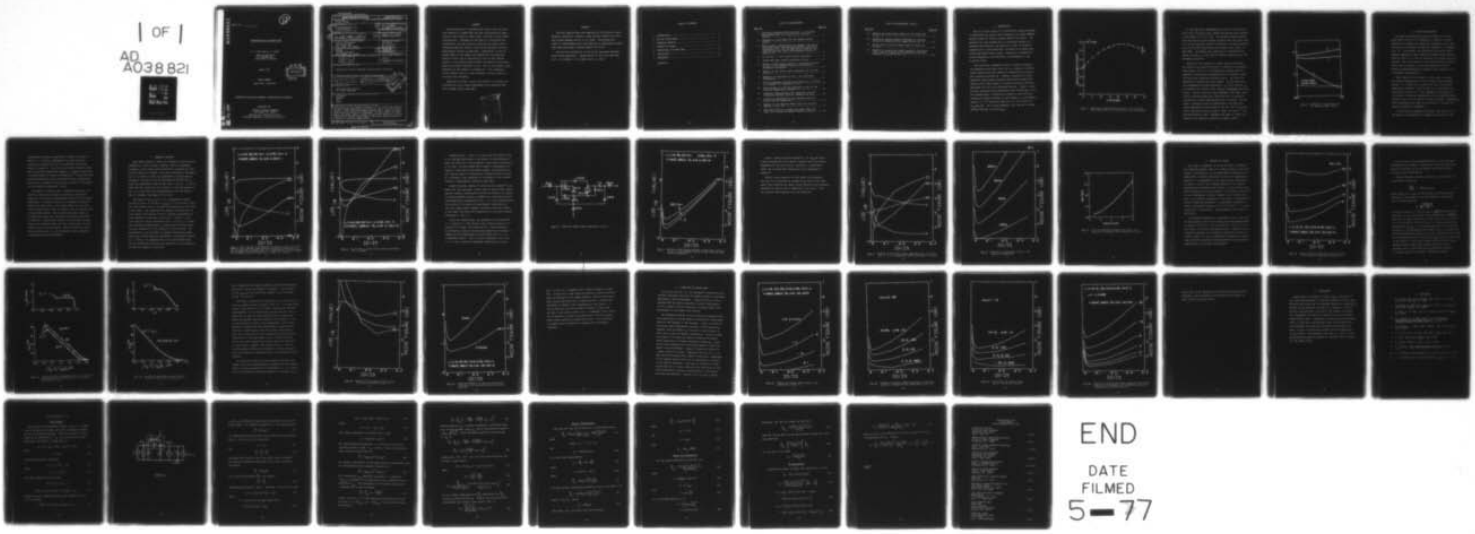

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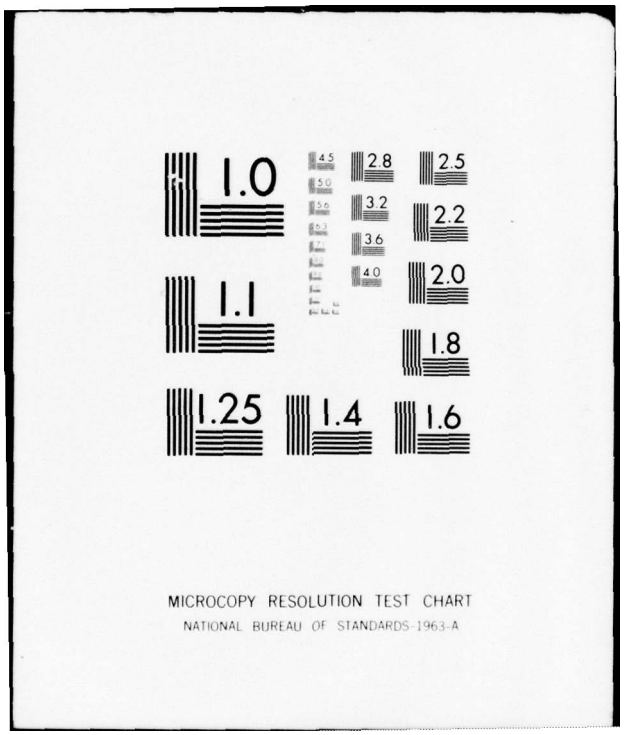
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Report No. _____

Investigation of InGaAs FETs

R. L. Bell and S. G. Bandy

Varian Associates
611 Hansen Way
Palo Alto, CA 94303

March 1977

FINAL REPORT

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Application of the theory of Statz et al. to the noise behavior of early InGaAs FETs shows that this is due to flow of channel current in the substrate/InGaAs grading layer, where the saturated electron velocity is degraded. If this defect is eliminated, the model shows a return to GaAs-like behavior, but with significantly better noise figure than GaAs, despite possible increase in electron temperature.

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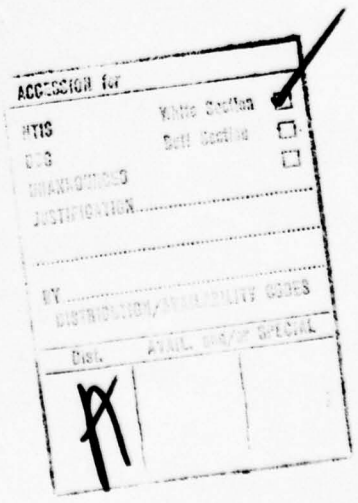
SUMMARY

The occurrence of a minimum noise figure near zero gate bias observed in InGaAs FETs has been investigated by application of the theory of Statz, Haus, and Pucel to the InGaAs configuration. Treatment of the gate as a distributed RC transmission line was found to reconcile the theory with a reasonable physical model of the electron dynamics and with experimental results on GaAs FETs. Application of the improved model to the InGaAs case showed that the observed behavior could only be explained by flow of some channel current in the grading layer between the InGaAs and the GaAs, where the electron velocity is low. Flow in the grading layer dominates as the channel is pinched off. The increasing transit angles lead to a rapid increase in noise figure as the gate bias increases.

Modeling of an FET in which this defect is corrected illustrates the noise figure improvement to be expected from use of InGaAs rather than GaAs.



PREFACE

The work reported here was supported by the Office of Naval Research, Arlington, Virginia, under contract N00014-76-C-1056. The Program Manager was Mr. M. N. Yoder. The program was aimed at understanding the noise behavior of experimental InGaAs FETs fabricated under contract N00014-75-C-0125.

The work was carried out in the Varian Corporate Research Solid State Laboratory. Contributions to this work were made by C. K. Nishimoto, S. G. Bandy, and R. L. Bell.

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1. INTRODUCTION

This is a final report on a three-month program designed to understand the unusual noise properties of InGaAs MESFETs observed under an earlier program (N00014-75-C-0125). The objective of that program was to investigate InGaAs as a microwave FET material, by growth of a range of different compositions on GaAs substrates (including a Cr-doped semi-insulating graded buffer layer), fabrication of MESFETs of micron dimensions, and evaluation of performance in the microwave bands.

The relatively rudimentary state of InGaAs technology (by comparison with GaAs) gave rise to a number of fabricational difficulties and resulted in domination of performance largely by parasitics. However, extraction of basic parameters from network analyzer observations showed that InGaAs alloys indeed appear to possess important potential advantages for low noise microwave devices. Figure 1 shows one plot extracted from experimental data accumulated so far. This demonstrates a significant increase in the effective saturation electron velocity in the channel v_s, from approximately 1.3×10^7 cm/sec for GaAs to 2.2×10^7 cm/sec for $In_{0.2}Ga_{0.8}As$. For a given geometry, this implies a corresponding increase in F_T and F_{max}.

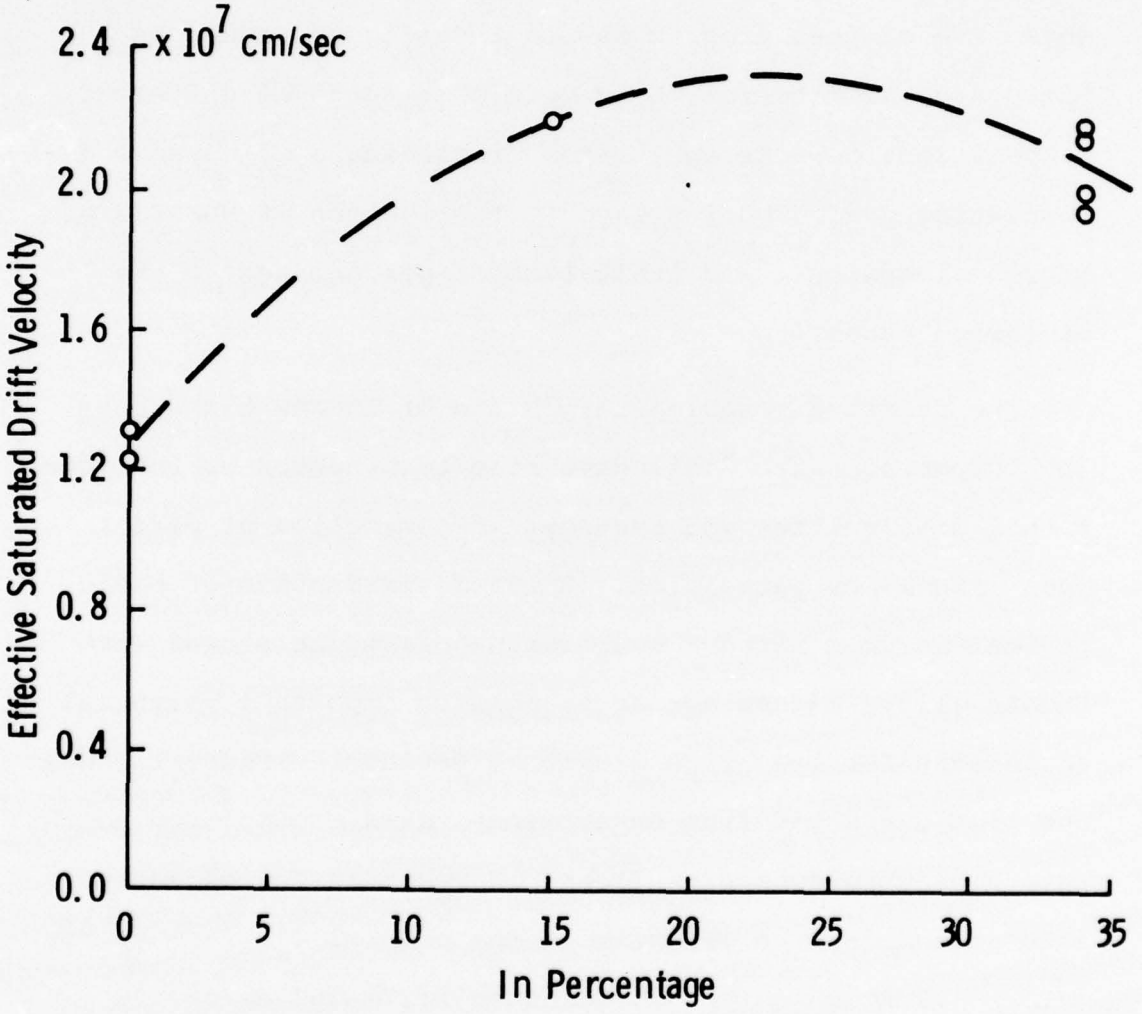

Fig. 1: Effective saturated drift velocity in 1.4-micron gate InGaAs FETs, as a function of InAs percentage.

At the same time, measurements at 8 GHz on 15% InAs devices with 1.4-micron gates showed encouraging noise figures, in the region of 3.5 to 4 dB. The unusual feature observed here was that the noise minimum occurred near zero gate bias, i.e. in the high-gain region of operation, in sharp contrast with the low gain associated with minimum noise figure in GaAs FETs. An analysis was undertaken to understand this effect in detail, in the hope of further exploiting any new phenomena uncovered.

Because of the increase in energy separation between the central and satellite valleys in InGaAs with increasing InAs content (Fig. 2), an accompanying increase would be expected in the electron temperature in the channel, under the high field conditions existing there. This would be expected to increase the noise figure. At the same time, the accompanying increase expected in v_s would increase g_m and decrease the transit time, tending to <u>decrease</u> the noise figure. The net effect of these phenomena, and their sensitivity to device parasitics, were difficult to assess by qualitative, or even semi-quantitative, arguments. Accordingly, a detailed study was undertaken of the FET noise theory developed over the years by Van der Ziel,[1] by Baechtold,[2] and more recently by Statz, Haus, and Pucel,[3,4] abbreviated below as SHP. Attempts were made to relate the theory to the observed situation in InGaAs alloys.

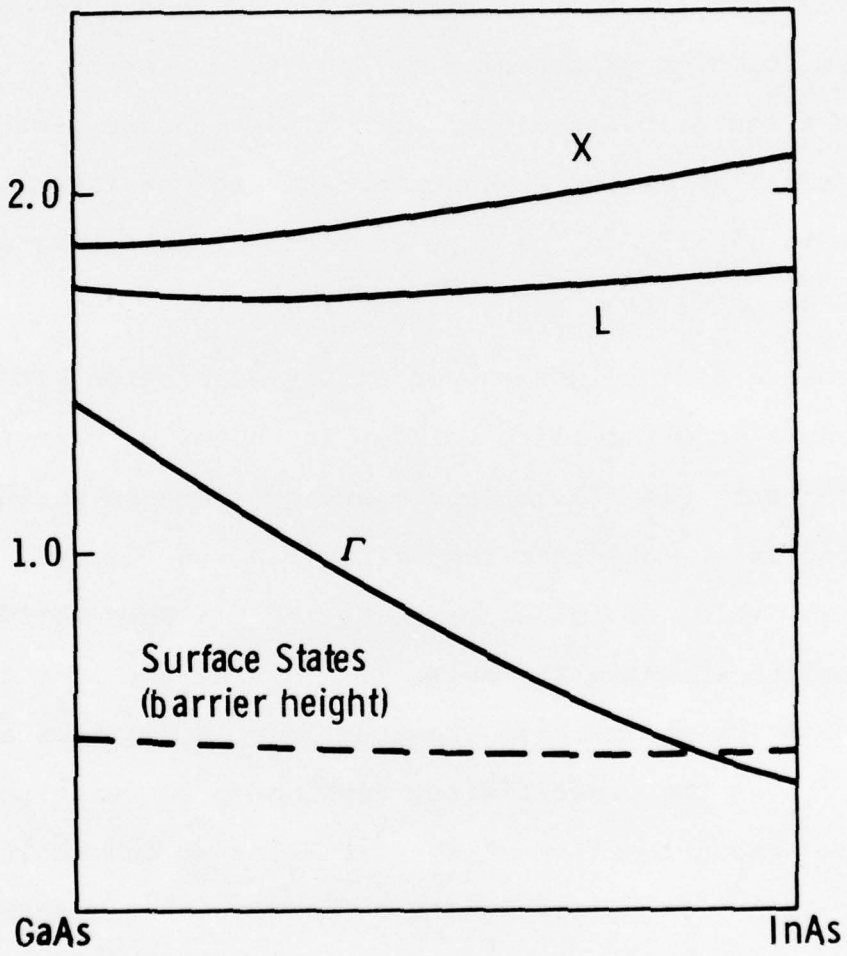

Fig. 2: Schematic of band edges for the InGaAs ternary system.

2. THE FET NOISE MODEL

The negative-differential-mobility region of the velocity-field curve for 3-5 compounds of interest for FETs represents an impasse for analytical treatments of the FET, and can only be handled by numerical methods (e.g. Yamaguchi et al.[5]). Fortunately, the relatively high doping levels commonly employed in FETs effectively suppress the negative mobility region (at least for GaAs--see for example Bott and Hilsum[6]). Thus the division of the velocity-field characteristic into two regions, of strictly ohmic and strictly velocity-saturated behavior, assumed by SHP, appears to be a reasonable approximation.

Heavy doping of the channel is also likely to reduce the electron temperature in the low field region somewhat. However, it is difficult to accept the very low electron temperature parameter δ used by SHP (1.2 vs measured[2] and calculated[7] values of 6). This assumption corresponds to a reduction in electron temperature at the boundary between regions I and II of the FET by a factor of three. Accordingly, some investigation was made of the effects of varying the electron temperature parameter δ.

A high electron temperature persists into region II of the device, as manifested for example by a decline in the

longitudinal diffusion coefficient D along the length of region II. A further approximation is made by SHP in choosing an average value of D to represent the entire length of region II. In view of the rather cavalier treatment of electron temperature effects, it appears unnecessary to include explicit account of Baechtold's[2] intervalley scattering contribution to the effective electron temperature, which may be regarded as having been included in the theory via the arbitrary parameters δ and D.

FET models in general treat a double-sided device, in order to simulate the presence of perfectly insulating substrate. In practice, experimental results are for single-sided FETs on substrates which are not perfect insulators. Reiser[8] has shown that in the single-sided case the drain field extends further down the channel than is possible with a double-sided device. The velocity-saturated region II is therefore longer than calculated for double-sided FETs. In addition, a significant fraction of the channel current flows in the substrate when the FET is biased near cut-off (normally the low noise region). Thus the substrate parameters, particularly v_s in the substrate, may be important in determining noise performance.

3. NUMERICAL RESULTS

With these caveats in mind, the treatment of SHP was programmed for a small digital computer, with an independent treatment of the noise figure calculation including the most critical parasitic element --the source resistance (see Appendix I). In order to check the programming and minimization procedure, the case of the FET described by Brehm[9] was run using the parameters listed by SHP (Figs. 3 and 4). It can be seen that the results are very similar to the calculations of Ref. 4, so that both the interpretation of the SHP theory and the computer code appear to be valid.

The range of I_d/I_s from 0 to 0.3 encompasses roughly the whole of Fig. 27 of Ref. 4 ($I_{dss}/I_s \simeq 0.24$ for this case.) The noise figure curve is plotted with reference to the scale on the right. Also shown are the separate contributions to noise figure from regions I and II, plotted logarithmically with reference to the scale on the left. Figure 3 is for a low value of source resistance, Fig. 4 is for R_s = 15 ohms. The correlation coefficient C_{11} between gate and drain fluctuations (labeled C1 in the figures) is also plotted. The contribution to noise figure of thermal fluctuations generated by the source parasitic resistance is displayed (labeled R_s). Finally, the component due to the uncorrelated gate current fluctuations was was also computed, but was generally too small to appear on the plots.

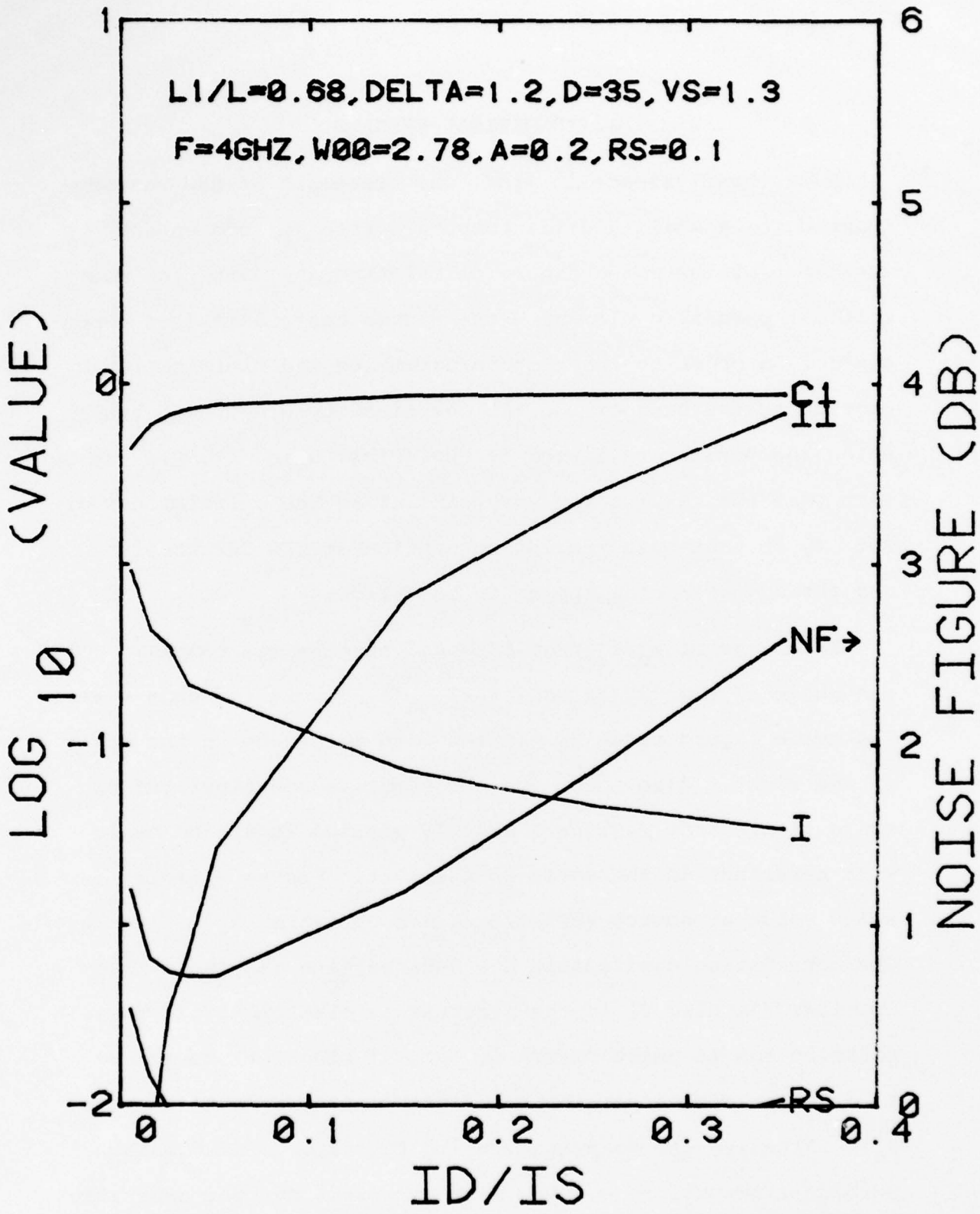

Fig. 3. Noise figure, contributions of regions I and II to the noise factor, and the gate-current correlation coefficient C_{11}, for the GaAs FET of Brehm (Ref. 9) as calculated using the theory and parameter values of Statz et al. (Ref. 3). Rs = 0.

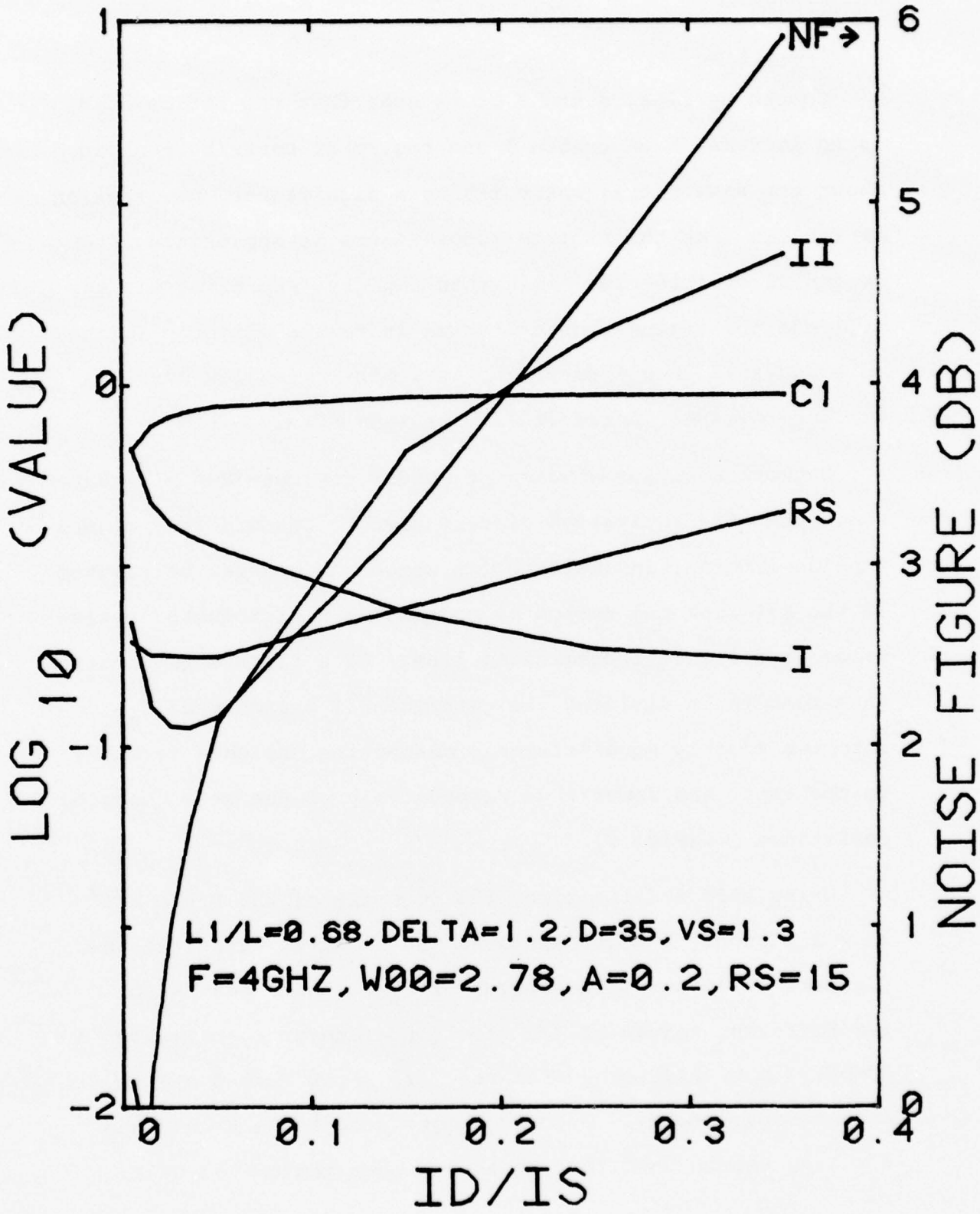

Fig. 4. As for Fig. 3, with finite source resistance (Rs = 15 ohms).

Comparing Figs. 3 and 4 it is seen that the effect of R_s is to increase both region I and region II contributions in about the same ratio, while making a significant contribution of its own. As the minimum noise figure is approached, the region II contribution diminishes rapidly (approximately as I_d^3) and the region I contribution increases slightly (owing to a decrease in g_m) resulting in a minimum at low currents similar to experimental results on GaAs FETs.

Network analyzer studies of actual devices (Bandy[10]) have shown that the equivalent circuit used by SHP and many others implies internal inconsistencies which can however be removed if the gate/channel region is modeled as a distributed resistance/capacitance transmission line. As a first approximation this results in dividing the gate/channel capacitance C_g into two roughly equal elements connecting the gate terminal to the upper and lower ends respectively of the gate charging resistance R (Fig. 5).

Using this modification, the geometry of the Brehm FET[9] (L = 2 microns, Z = 285 microns) and a source parasitic resistance of 10 ohms, the curves of Fig. 6 were generated for different values of the electron temperature parameter δ. Comparison with experimental results[9] shows that $\delta = 4$ is a reasonable choice. This is a more acceptable value than $\delta = 1.2$, and is used for subsequent computations on GaAs.

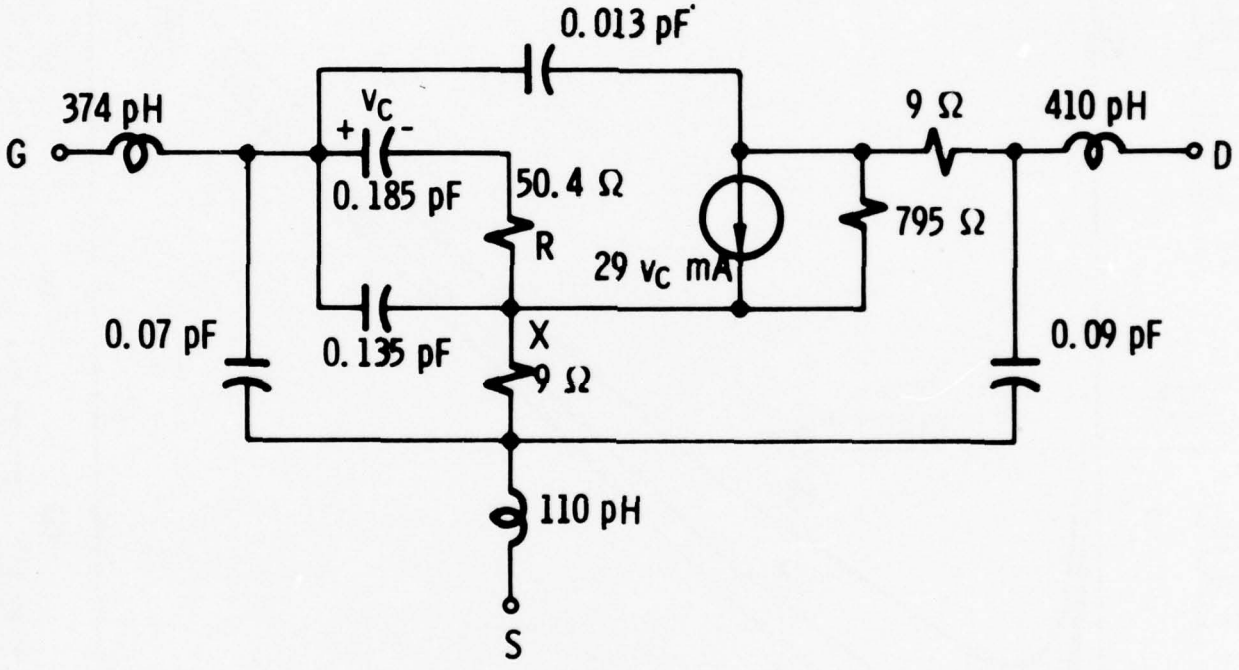

Fig. 5. InGaAs FET small-signal equivalent circuit.

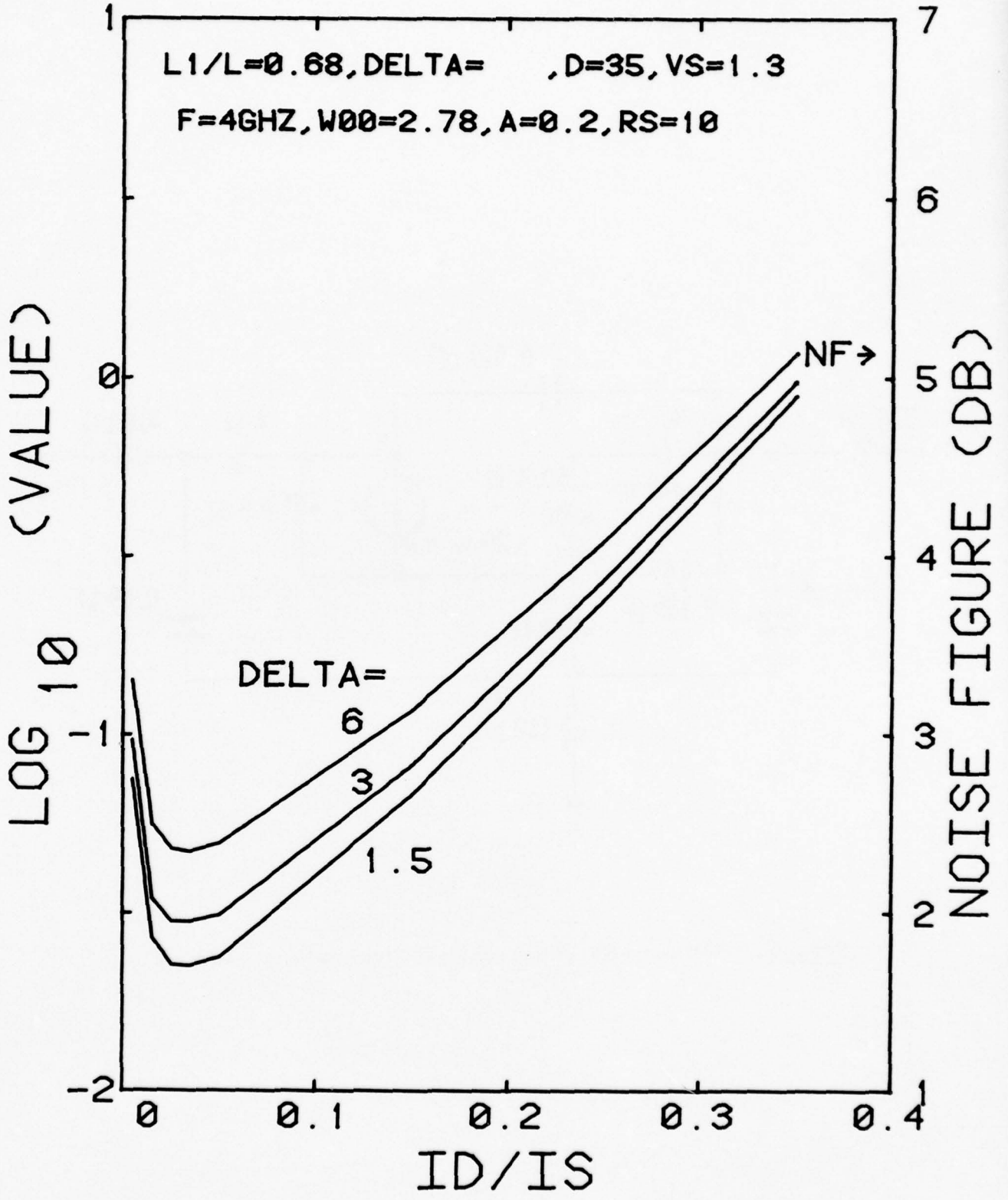

Fig. 6. Results of SHP theory applied to equivalent circuit of Fig. 5 for different values of the electron temperature parameter δ.

Figure 7 shows the noise figure NF = 10 $\log_{10}$(N) where N may be termed the noise factor, together with the various components of the noise factor, plotted on a logarithmic scale. The uncorrelated induced gate noise component is labeled G.

Figure 8 shows behavior of this model with frequency, and Fig. 9 the variation of minimum noise factor with frequency. This exhibits the nearly linear behavior with frequency predicted by Van der Ziel,[1] Baechtold,[2] and others. Thus the computer model appears to be well-behaved.

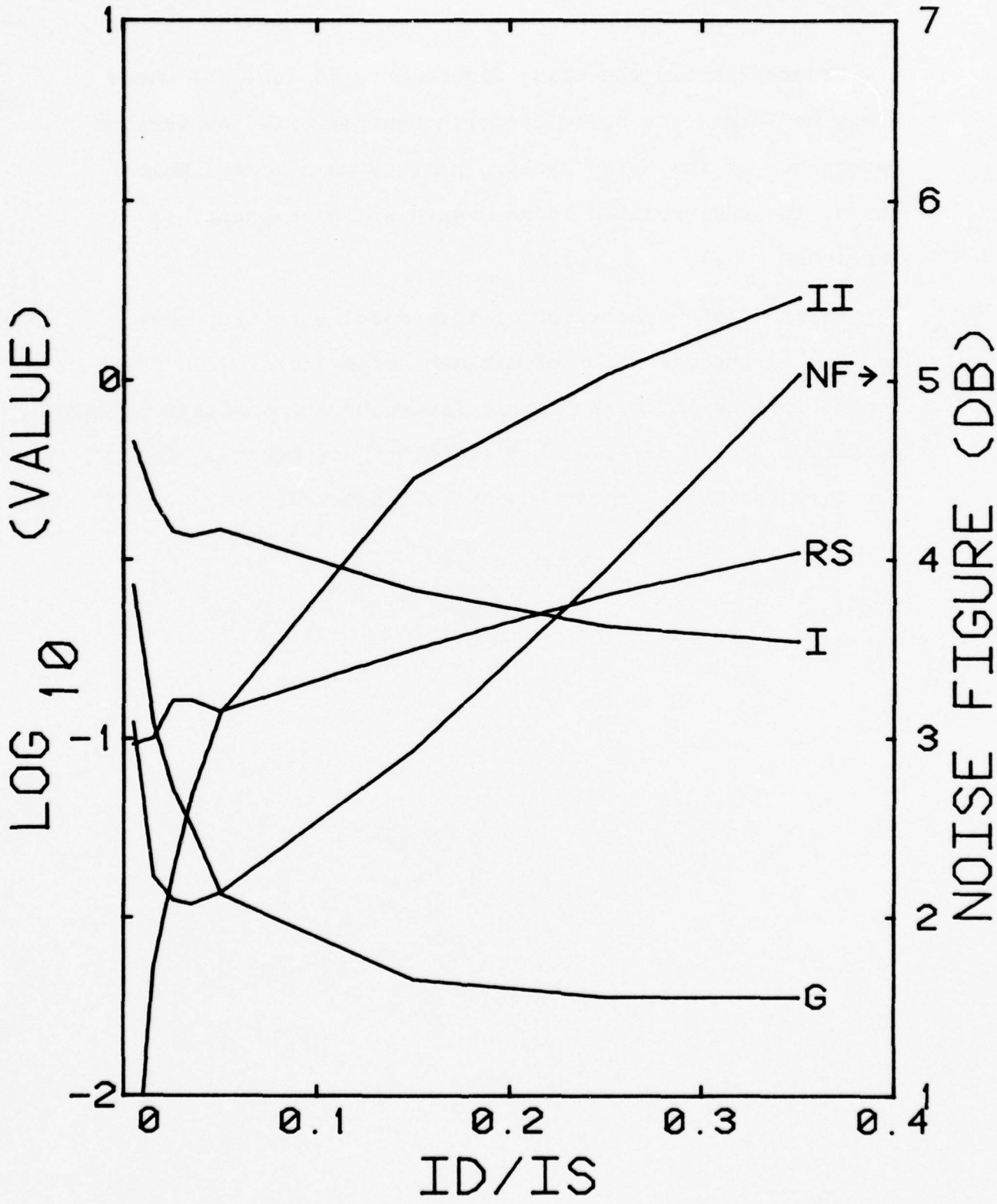

Fig. 7. Details of the noise figure components for the FET of Fig. 5. $\delta = 4$, parasitic source resistance = 10 ohms.

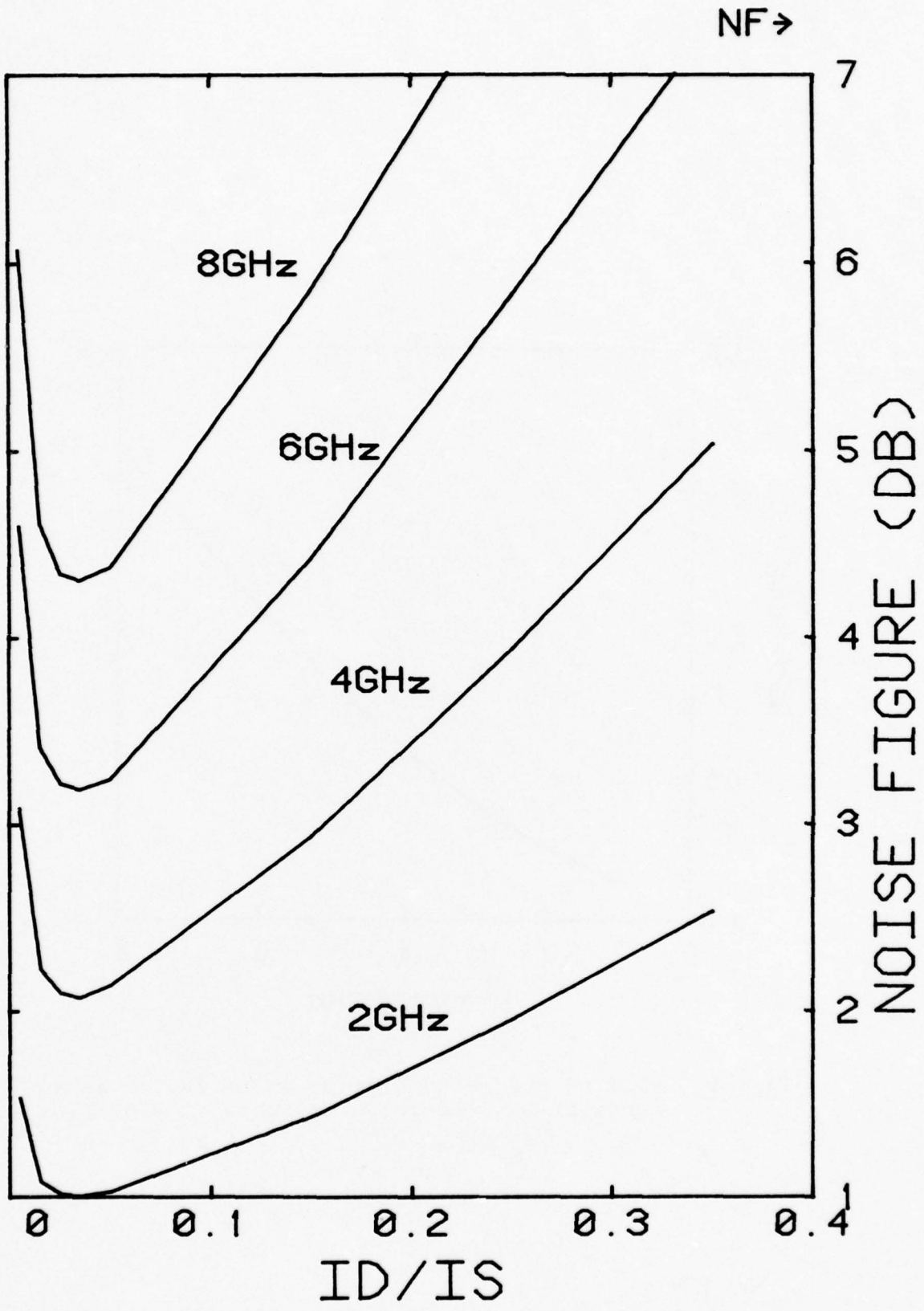

Fig. 8. Behavior of transistor of Fig. 7 for different frequencies.

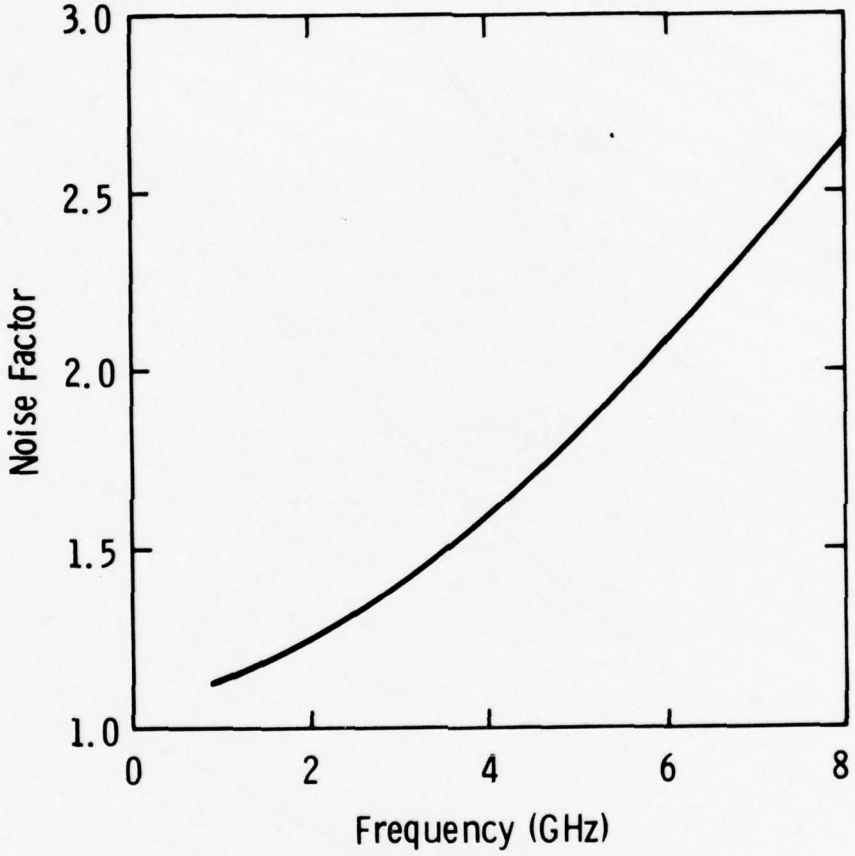

Fig. 9. Plot of predicted minimum noise factor as a function of frequency for transistor of Fig. 7.

4. RESULTS ON InGaAs

The region I component of the noise factor, plotted in the foregoing figures, shows the inverse behavior with drain current, characteristic of the experimental observations on InGaAs FETs. A natural conclusion is that the experimental behavior is a consequence of the high electron temperature in region I, due to the increased spacing of the central and satellite conduction band valleys, or the electron overshoot conditions in a short channel (e.g. Maloney and Frey[11]) or to a combination of these. However, Fig. 10 shows that this is an unlikely explanation. This figure is computed for typical InGaAs FET parameters, a measurement frequency of 8 GHz, a saturated velocity of 2.2×10^7 cm/sec, L = 1.4 microns and Z = 200 microns. Other parameters are noted on the figure.

The electron temperature is assumed to vary as the cube of the electric field in the channel with peak temperatures of 2700K or 0.23 eV ($\delta = 8$) to 19,500K or 1.68 eV ($\delta = 64$). The latter is of course unreasonably high. However the experimental behavior of a minimum at high drain currents is clearly absent. In fact no reasonable combination of parameters could be found which would reproduce the experimental observations in the model as described.

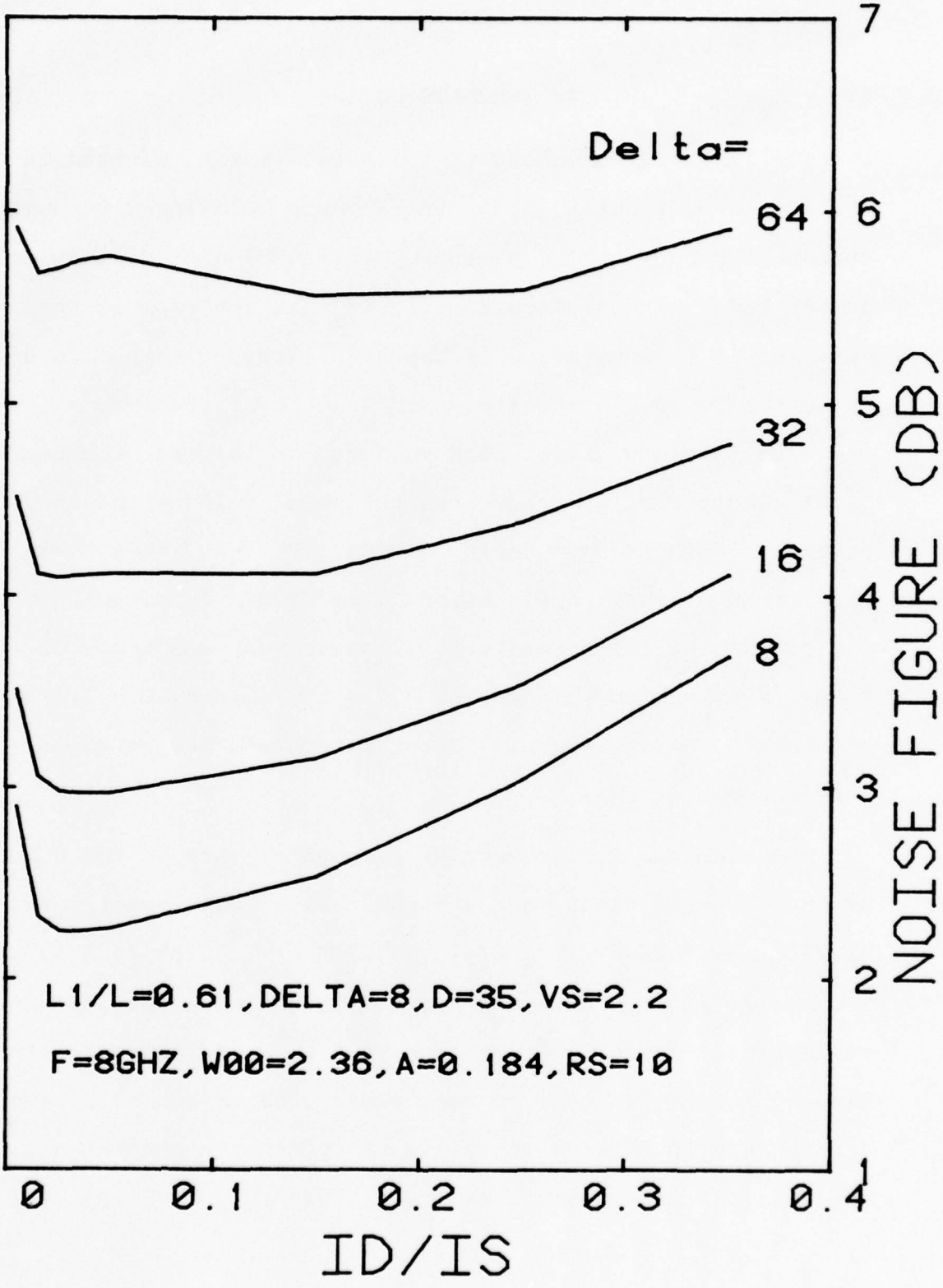

Fig. 10. Noise figure at 8 GHz for different values of the electron temperature parameter δ.

At this point, other experimental data on the FETs were re-examined for evidence of variations in the saturated drift velocity with depth x_d in the InGaAs, which might explain the noise figure observations.

Assuming complete velocity saturation in the channel, it is not hard to show that

$$\frac{\partial I_{DSS}}{\partial x_d} = - qZN_D(x_d)v_s(x_d) \qquad (1)$$

where $N_D(x_d)$ and $v_s(x_d)$ are the doping and saturated drift velocity in the channel at the gate depletion region edge. For a uniform doping N_D,

$$x_d = \sqrt{\frac{2\epsilon(\phi_B - V_G)}{qN_D}} \qquad (2)$$

so that the slope of a plot of I_{DSS} vs $\sqrt{\phi_B - V_G}$ should be proportional to v_s at that value of x_d corresponding to $\sqrt{\phi_B - V_g}$. Such data are shown plotted for a GaAs device in Fig. 11 and for a 15% In device (53-11) in Fig. 12. Taking the value of the abscissa at $I_{DSS} = 0$ as being proportional to the channel thickness a, and normalizing the slope at $V_G = 0$ to agree with previously-determined values of v_s, the v_s profile of the channel as determined by the slope of the I_{DSS} curves is also shown in the figures. Clearly the InGaAs velocity profile begins degrading much further away from the epi-buffer layer interface than it does from the epi-substrate interface (no buffer layer) for the GaAs. Perhaps the buffer

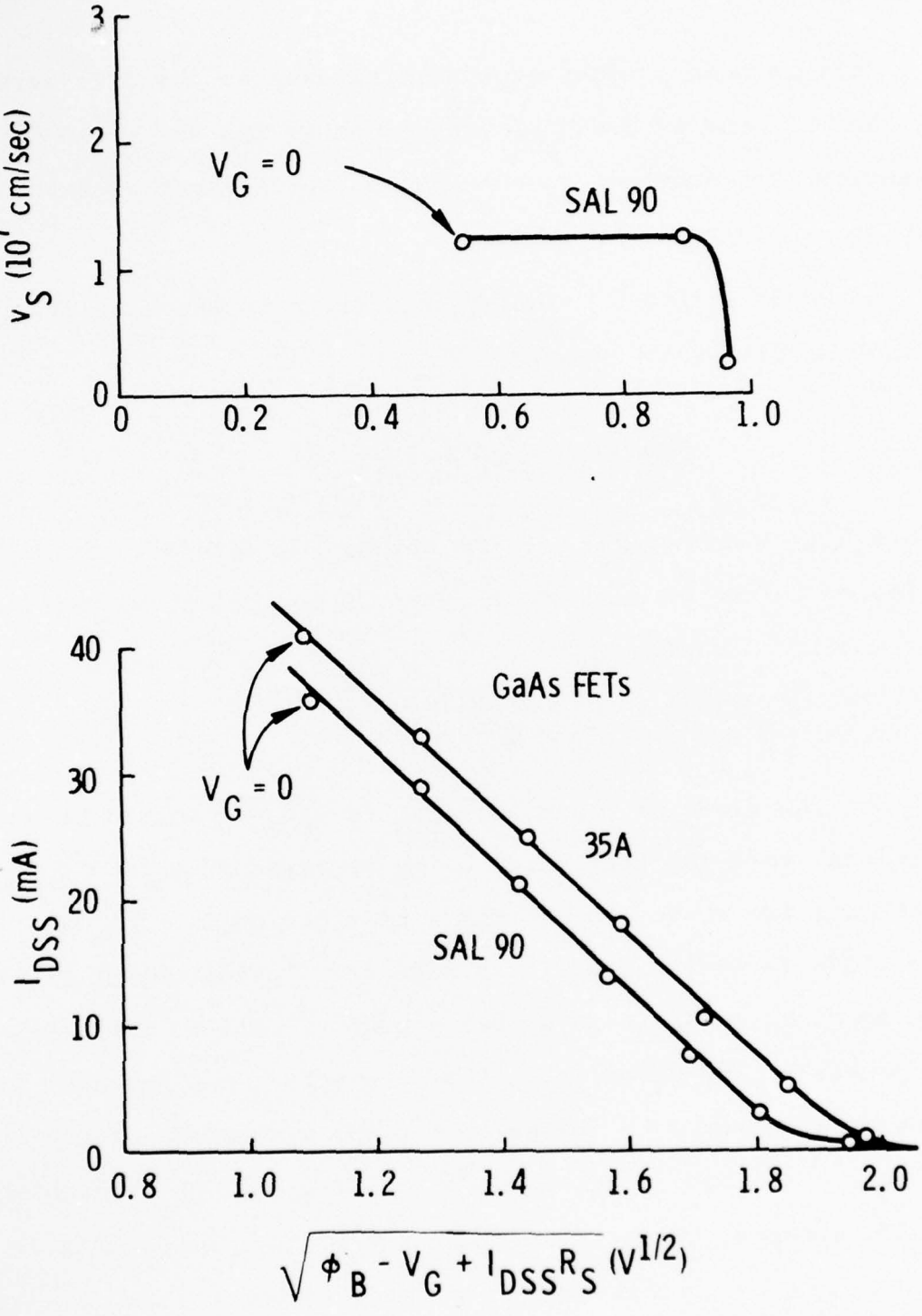

Fig. 11. (Lower) Pinch-off characteristic of a GaAs FET, and (upper) the "saturated velocity profile" deduced from this.

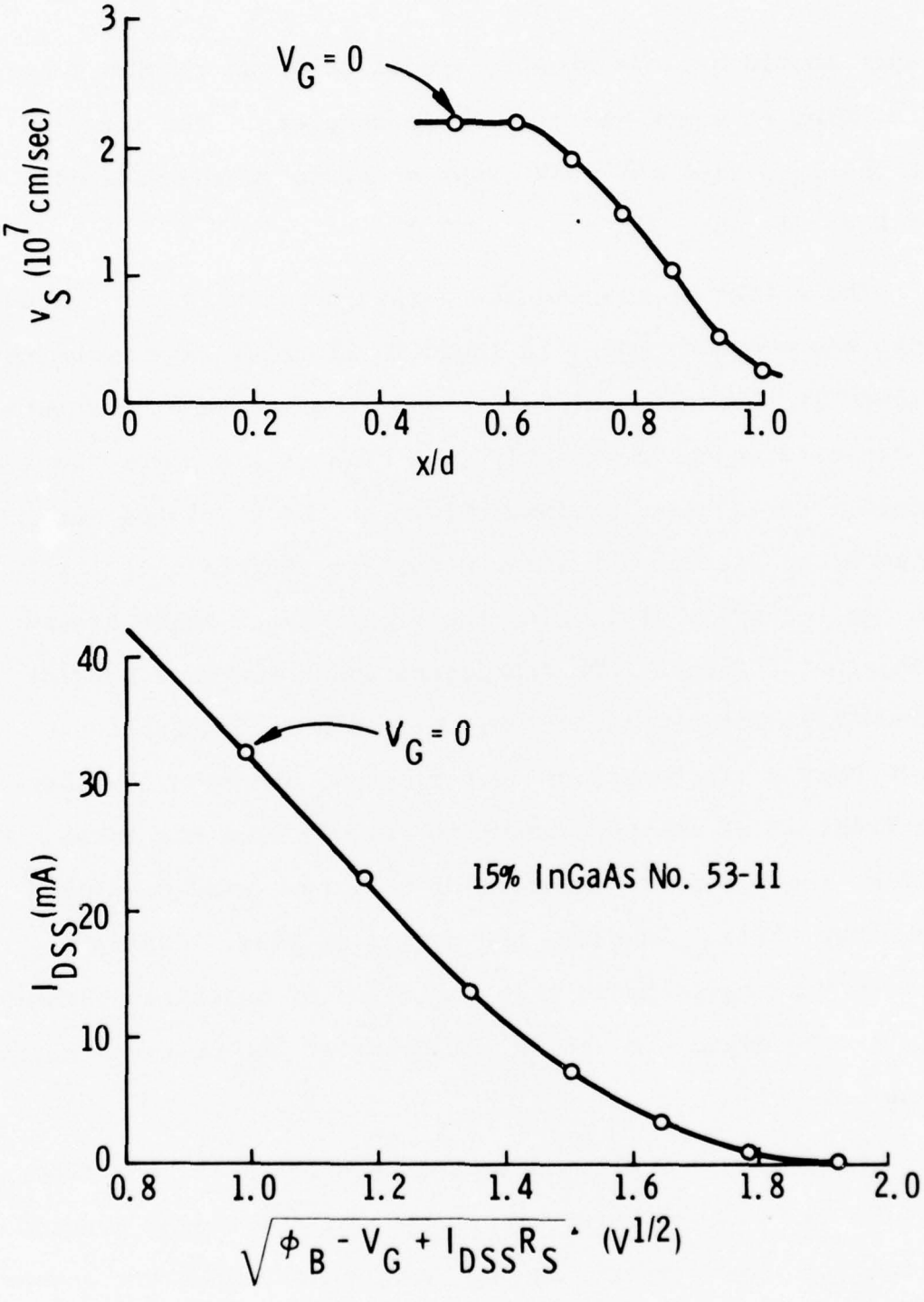

Fig. 12. Pinch-off characteristic and saturated velocity profile for an InGaAs FET.

layer should be less steeply graded or grown thicker beyond the point at which the grading is complete. The linearity of the I_{DSS} plot for GaAs gives credence to the validity of Eqs. (1) and (2).

The effect of placing the variation of v_s given in Fig. 11 into the computer model is shown in Fig. 13. A minimum noise figure in the region of 3.5 to 4db is obtained at currents corresponding to very nearly zero bias on the gate, and a rapid rise is seen for lower drain currents (higher gate biases and greater depletion widths in the channel). This is qualitatively similar to the experimental noise figure behavior of InGaAs FETs fabricated under contract N00014-75-C-0125. Unfortunately, the noise figure observations were only a minor part of that program, and detailed characteristics of the type shown in Fig. 13 were not taken. All of the "good" transistors of this type were destroyed in other tests. However, the curves of Figs. 11 and 13 are convincing evidence that variation of materials parameters with depth are indeed the cause of the observed noise behavior.

The question arises as to the benefits available from InGaAs, given that these materials problems can be overcome. Figure 14 shows computations of performance of a 15% InGaAs FET of the geometry fabricated (assuming a uniformly high v_s

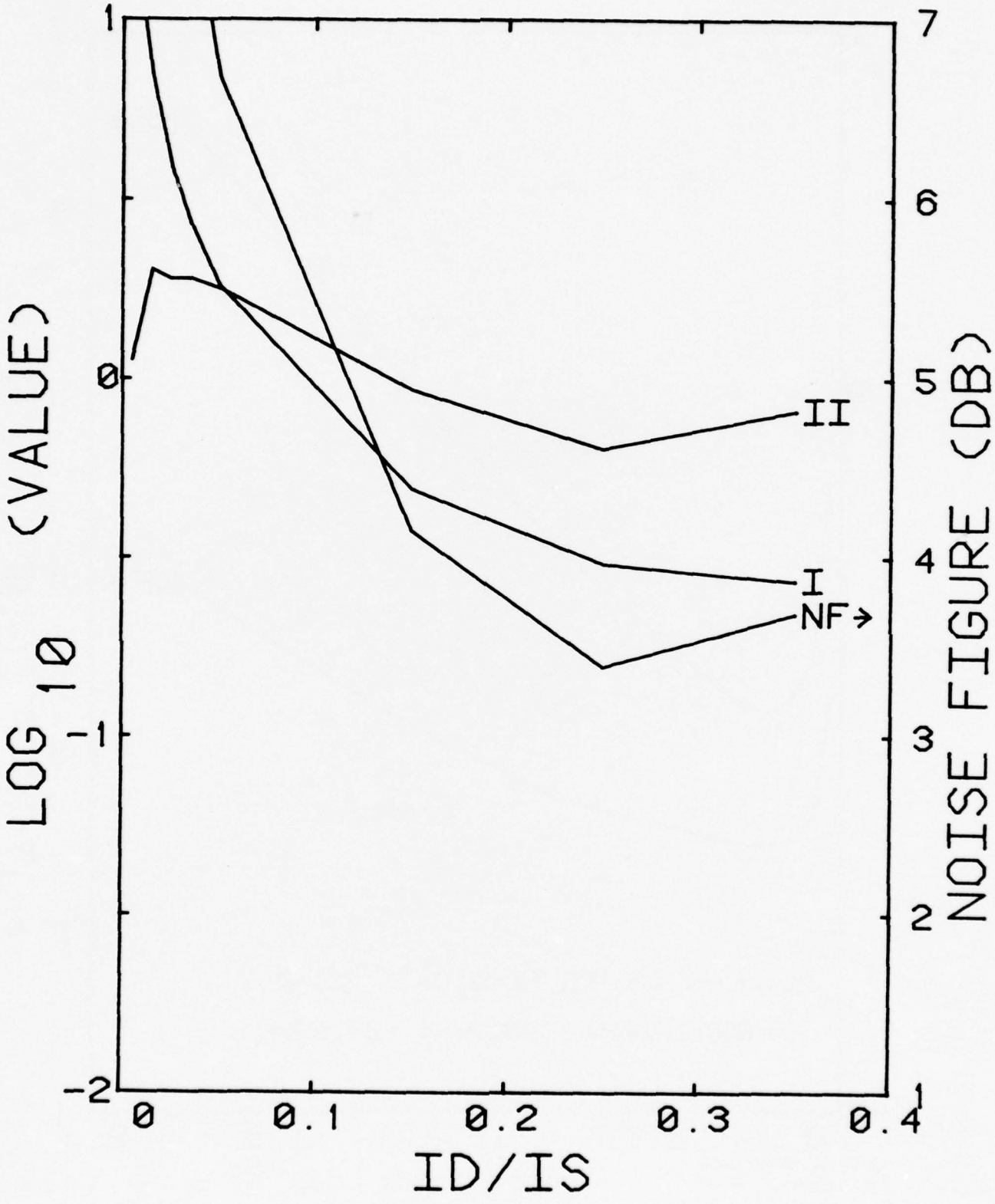

Fig. 13. Results of the computer model using the velocity profile of Fig. 12.

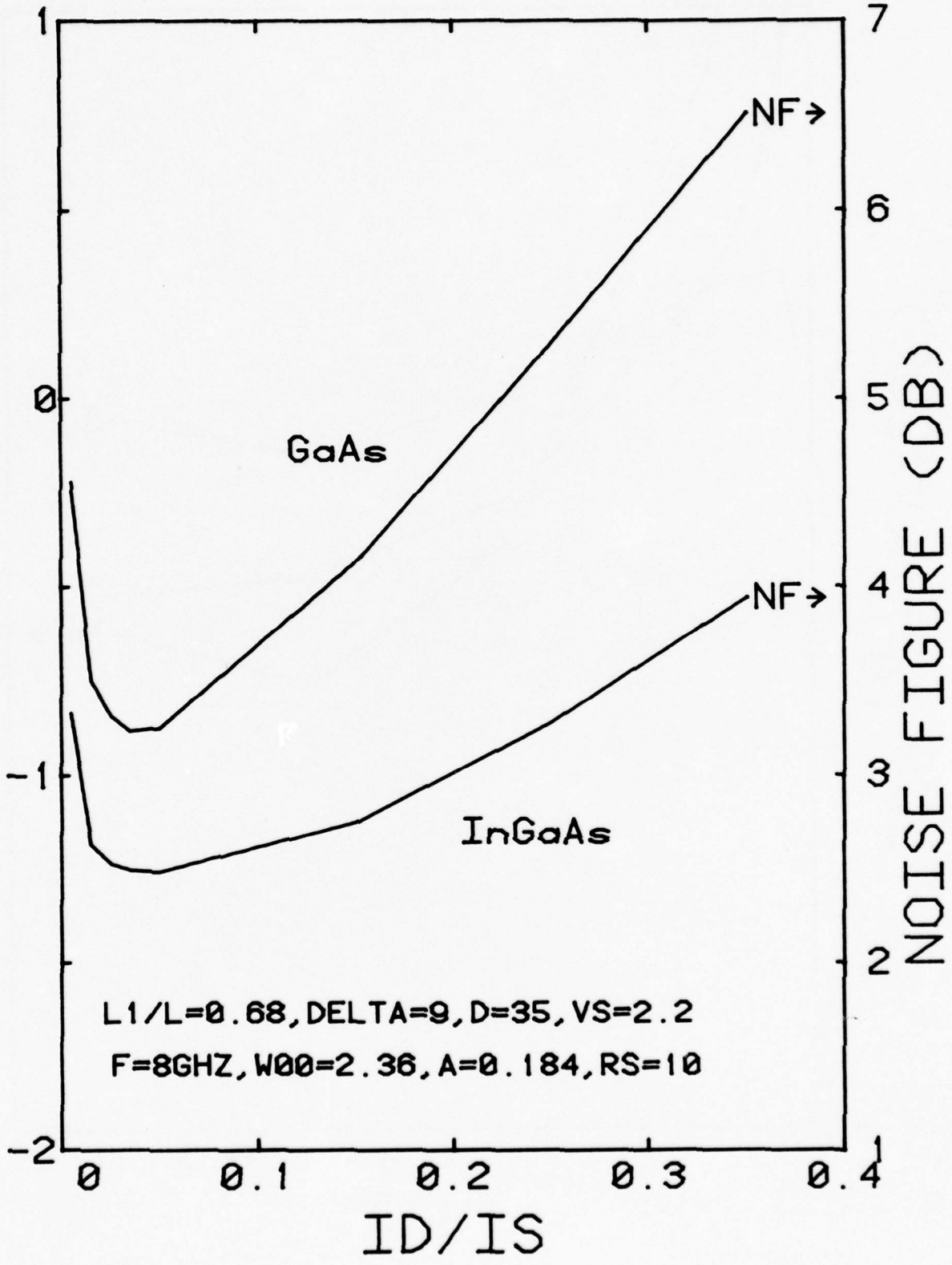

Fig. 14. Predicted behavior of GaAs and InGaAs FETs (15% InAs) with uniform saturated velocity profiles.

and a δ value of 9) compared with a similar geometry of GaAs FET. In practice a lower value of parasitic source resistance might be expected on the InGaAs material, owing to more favorable contact metallurgy and a higher mobility. However this advantage of InGaAs is not incorporated in the figure. It can be seen that the noise figure of InGaAs is lower than for GaAs at any given current (i.e., a comparable noise figure can be expected at higher associated gain), and the minimum noise figure expected is appreciably lower. This advantage of InGaAs would be expected to increase with increasing frequency.

5. DIRECTIONS OF FUTURE WORK

As we see from Fig. 14, the increase of saturation drift velocity available from even 15% InGaAs affords a significant advantage in noise performance. Future efforts in the 3-5 compound FET area should therefore include investigation of still higher velocity materials, including higher InAs percentages in the InGaAs alloy series.

The remaining figures in this report show quantitatively the predictions of the SHP model as regards the other parameters at the disposal of the designer. Figure 15 shows the well-known rapid improvement available on decreasing gate lengths, with the length L_2 of region II held constant at about three times the channel thickness a. Figure 16 shows the effects of varying the channel thickness and doping while maintaining a constant pinch-off voltage W_{oo}. Relatively thick channels and light doping appear to give the better noise performance. Figure 17 shows the effects of a lower pinch-off voltage. Comparing with Fig. 16, it is seen that the minimum noise figure is relatively independent of the channel doping level, but is principally a function of the channel thickness. The range of validity of these conclusions are of course limited by the occurrence of negative differential mobility instabilities at low dopings and large thicknesses.[5] Finally, Fig. 18 gives a quanti-

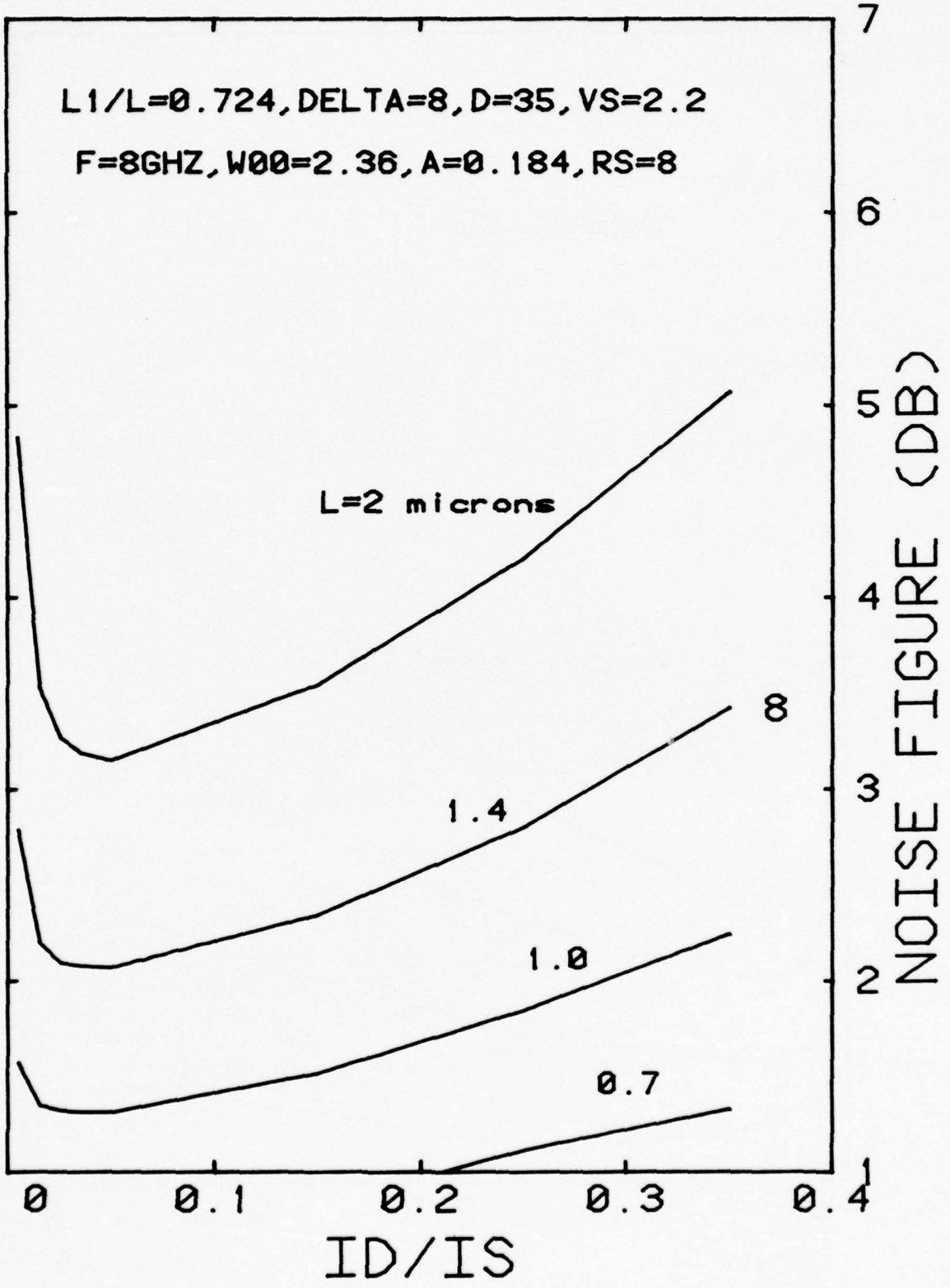

Fig. 15. Effects of varying gate length on the InGaAs FET of Fig. 14.

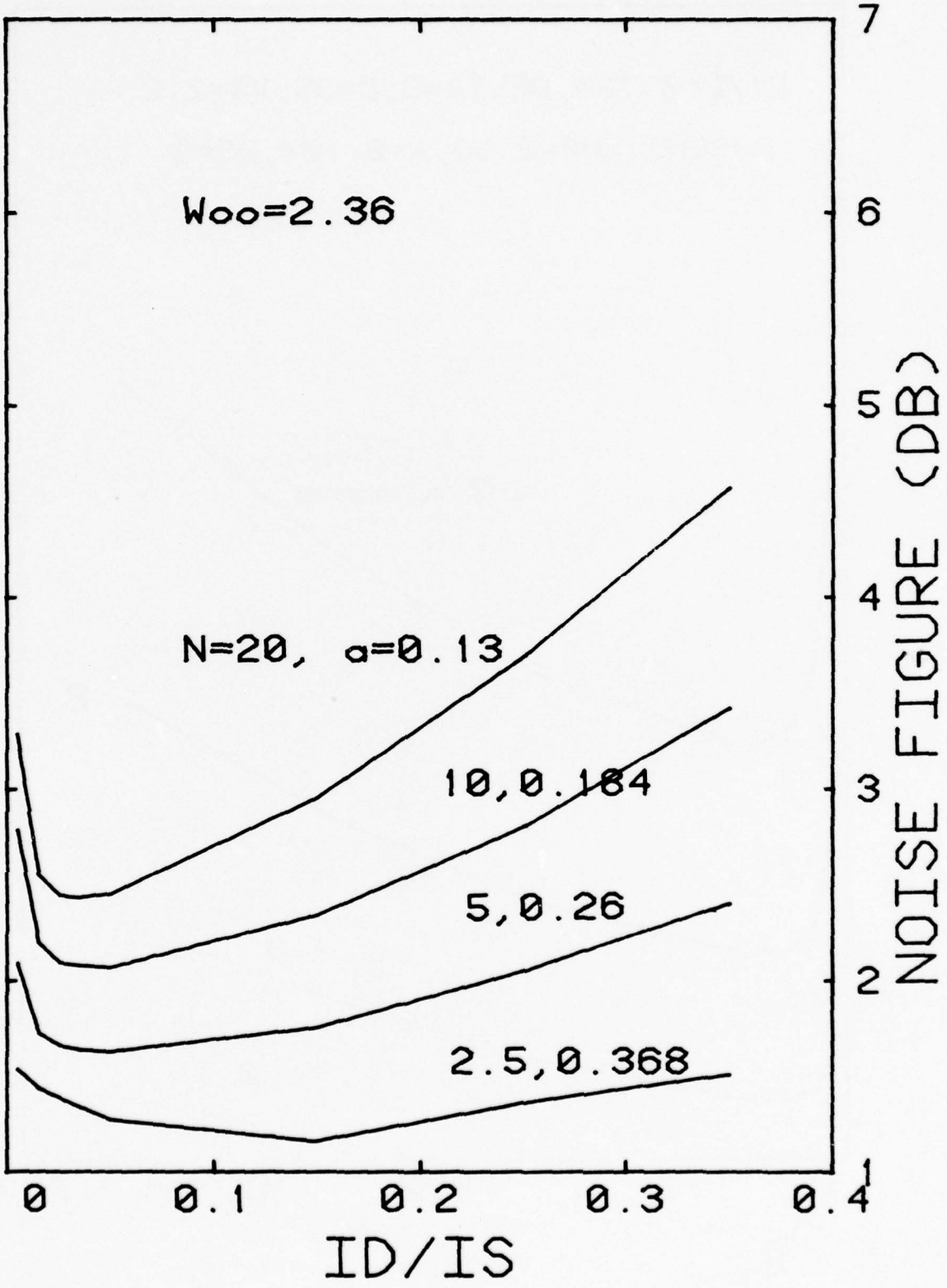

Fig. 16. Effects of varying channel thickness at constant pinch-off voltage for the InGaAs FET of Fig. 14.

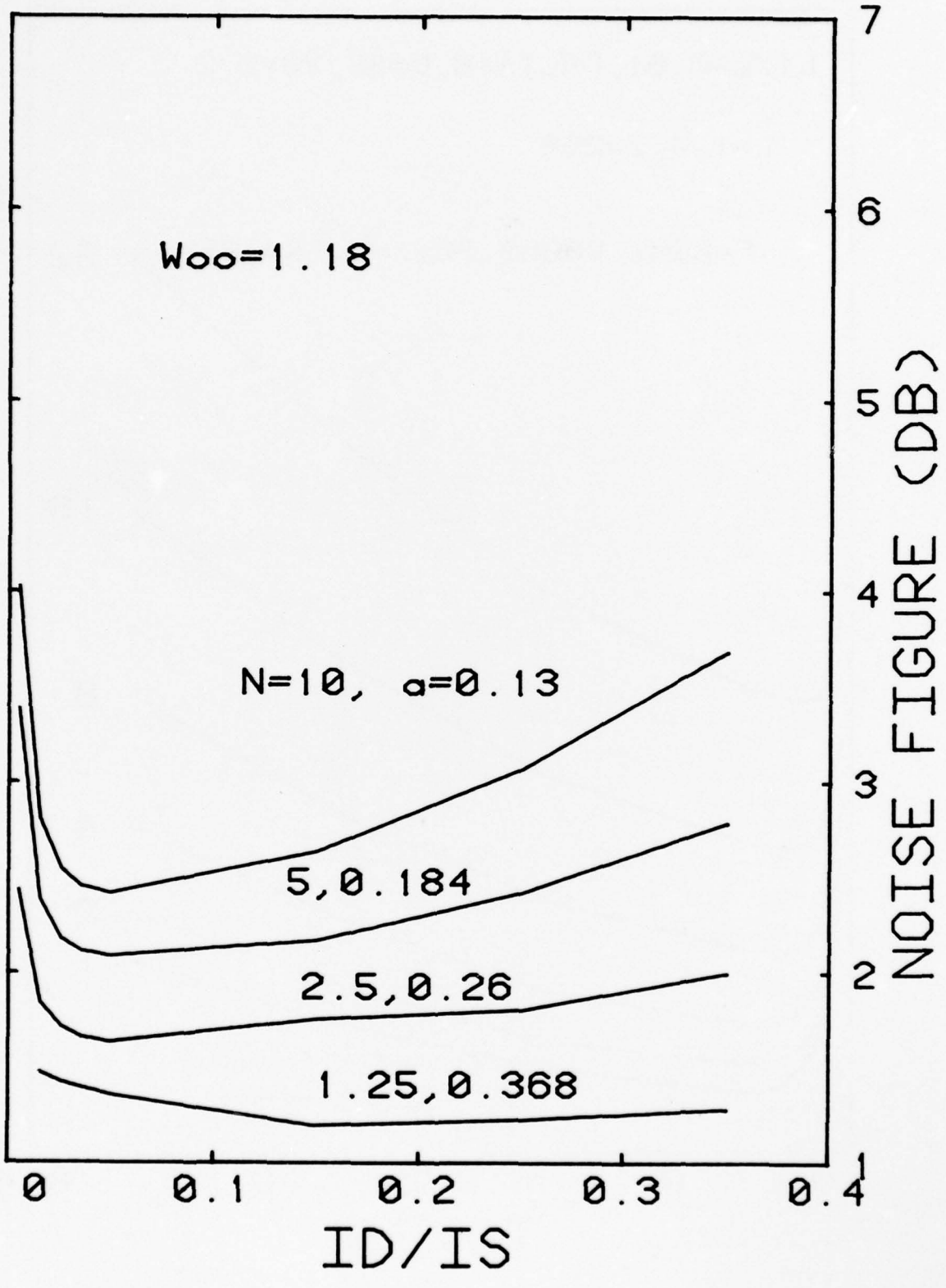

Fig. 17. As for Fig. 16, with a lower value of pinch-off voltage.

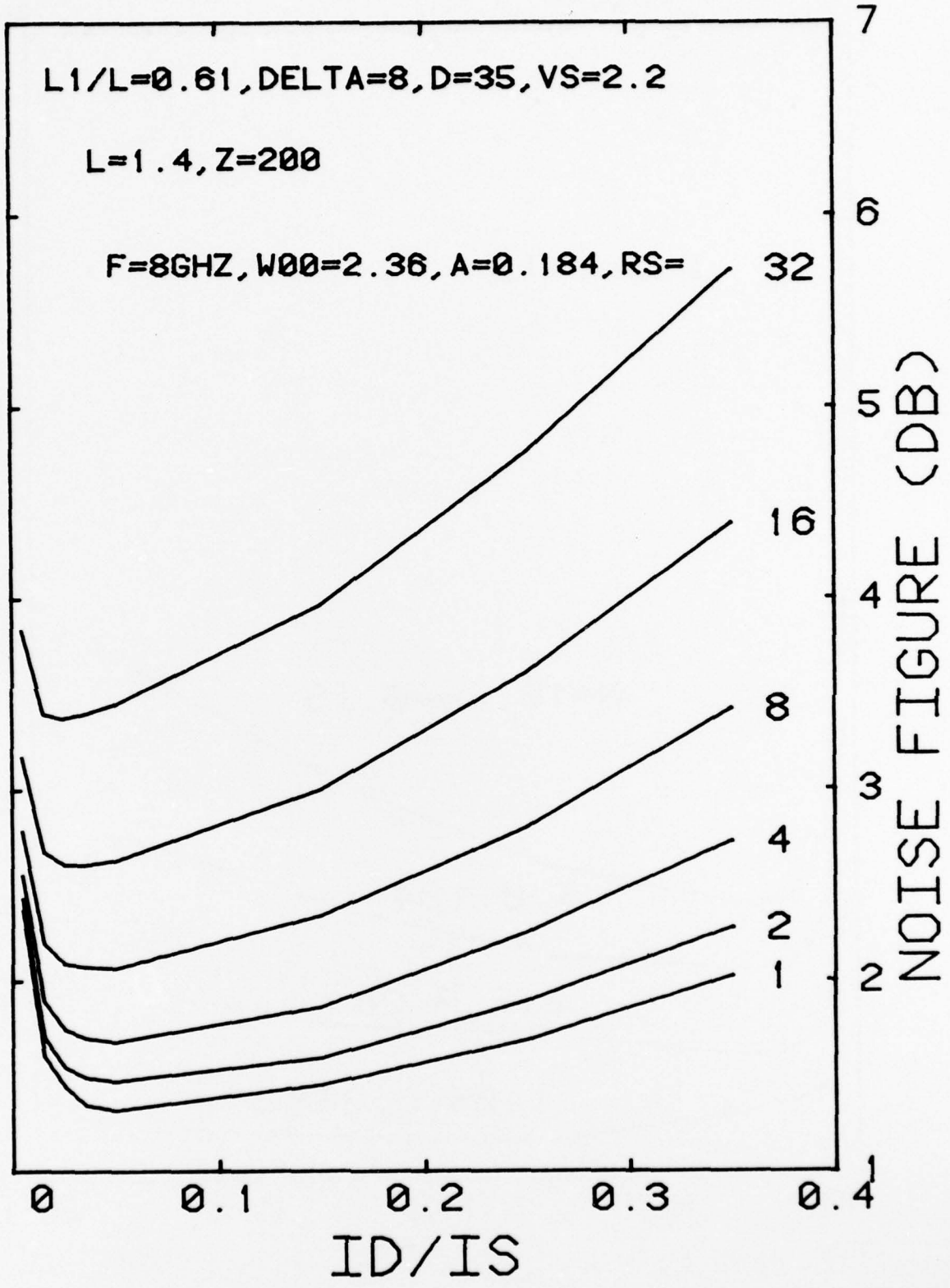

Fig. 18. Effects of varying the source parasitic resistance from 1 ohm to 32 ohms on the predicted noise performance of the FET of Fig. 14.

tative idea of the importance of the source parasitic series resistance, and the benefits to be derived from efforts to lower R_s below any given value.

6. CONCLUSIONS

Application of the model of Statz, Haus, and Pucel,[3,4] with minor modifications, to the noise behavior of the InGaAs microwave FET shows that the observed behavior of experimental devices can be explained in terms of a reduction in the effective saturated drift velocity as the channel is pinched off, presumably the result of current flow in the Cr-doped graded buffer layer. Prevention of this deterioration should result in FETs with significantly lower noise figures for a given geometry and given gain settings than possible with GaAs, in spite of potentially higher electron temperatures in the channel. The advantage over GaAs is a result of the experimentally-observed increase in saturated drift velocity for the InGaAs alloys.

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A P P E N D I X A

Noise Figure

The circuit to be analyzed is shown in Fig. A.1. Nodes 1 and 2 are gate and source; the drain is assumed grounded for the noise figure analysis. The signal source is represented by an admittance $y_1 = g_1 + jb_1$ and the gate-source admittance, enclosed in a dashed box, by

$$y_2 = g_2 + jb_2 = j\omega C_2 + j\omega C_1/(1 + j\omega t) \tag{1}$$

where

$$t = R_1 C_1 \quad . \tag{2}$$

We need the potential difference

$$v_1 - v_3 = \alpha(v_1 - v_2) \tag{3}$$

where

$$\alpha = (1 + j\omega t)^{-1} \quad . \tag{4}$$

The nodal equations can be written

$$(y_1 + y_2)v_1 - y_2 v_2 = i_1 \tag{5}$$

$$-y_2 v_1 + (y_2 + g_3 + g_d)v_2 = i_2 + \alpha g_m (v_1 - v_2) \quad . \tag{6}$$

Neglecting g_d by comparison with g_3 (or lumping it in g_3) Eq. (6) becomes

$$-(\alpha g_m + y_2)v_1 + (y_2 + g_3 + \alpha g_m)v_2 = i_2 \ , \tag{7}$$

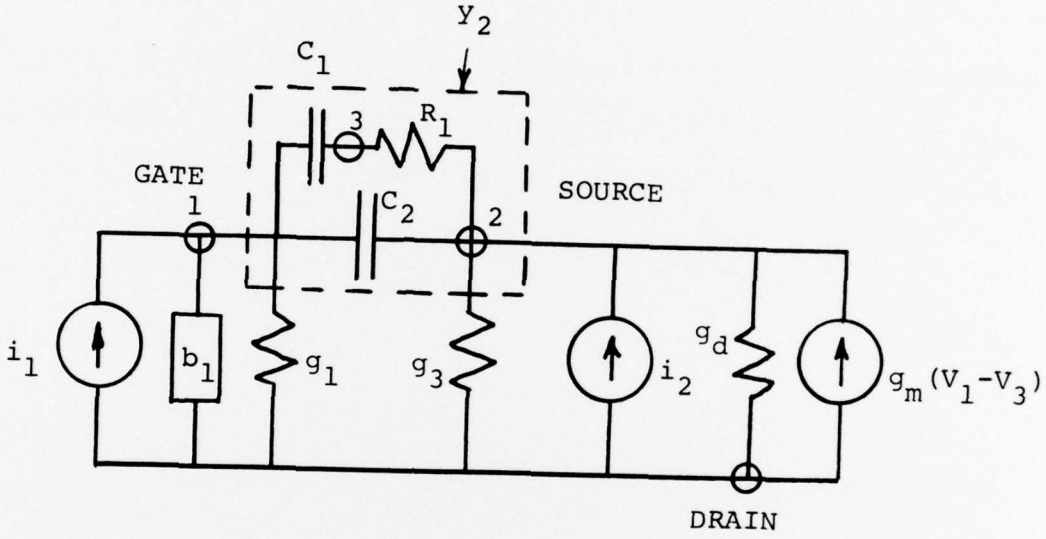

Figure A.1

i_1 and i_2 are effective noise currents injected into gate and source nodes. For thermal fluctuations in the signal source,

$$\overline{i_1^2} = 4kT_1 g_1 df \quad . \tag{8}$$

For induced gate noise currents circulating in the gate/source loop, i_1 and i_2 are fully correlated

$$i_1 = -i_2 \tag{9}$$

and

$$\overline{i_1^2} = \overline{i_2^2} = \overline{i_g^2} \tag{10}$$

calculated for regions I and II by Pucel, Statz, and Haus.[4] For thermal fluctuations generated in the source parasitic resistance,

$$\overline{i_2^2} = 4kT_3 g_3 df \quad . \tag{11}$$

For current fluctuations $\overline{i_d^2}$ in the channel,

$$\overline{i_2^2} = \overline{i_d^2} \tag{12}$$

calculated for regions I and II. From Eqs. (5) and (7) we have

$$v_1 \Delta = i_1 (y_2 + g_3 + \alpha g_m) + i_2 y_2 \tag{13}$$

where

$$\Delta = (y_1 + y_2)(y_2 + g_3 + \alpha g_m) - (\alpha g_m + y_2) y_2$$

$$= y_1 (y_2 + g_3 + \alpha g_m) + y_2 g_3 \tag{14}$$

$$v_2\Delta = i_1(y_2 + \alpha g_m) + i_2(y_1 + y_2) \quad . \tag{15}$$

Hence

$$(v_1 - v_2) = i_1 g_3 - i_2 y_1 \quad . \tag{16}$$

The current generated in the drain lead is then

$$i_d = \alpha g_m (i_1 g_3 - i_2 y_1)/\Delta \quad . \tag{17}$$

For signal-source fluctuations, i_1 is given by (8) and the injected current at node 2, i_2, is zero. Hence the resulting drain current fluctuations are

$$\overline{i_1^2} = |\alpha g_m g_3/\Delta|^2 \; 4kT_1 g_1 df \quad . \tag{18}$$

For thermal fluctuations in the source parasitic resistance, the the corresponding drain terminal fluctuation is

$$\overline{i_2^2} = |\alpha g_m y_1/\Delta|^2 \; 4kT_3 g_3 df \quad . \tag{19}$$

For fluctuations $i_{d_{II}}$ generated in region II, a component $-j\beta_2 i_{d_{II}}$ circulates in the gate-source loop, completely correlated with $i_{d_{II}}$. The fluctuation in the channel alone gives a component at the drain terminal

$$\overline{i_3^2} = \overline{i_{d_{II}}^2} \; \left|1 - \frac{\alpha g_m y_1}{\Delta}\right|^2 \tag{20}$$

(using (17) with $i_1 = 0$) and, adding the correlated gate current with $i_1 = -j\beta_2 i_{d_{II}}$, $i_2 = +j\beta_2 i_{d_{II}}$, the net drain terminal fluctuation is

$$\overline{i_3^2} = \overline{i_{d_{II}}^2} \left| 1 - \frac{\alpha g_m y_1}{\Delta} - \frac{j\beta_2 \alpha g_m}{\Delta} (g_3 + y_1) \right|^2 \qquad (21)$$

The fluctuations i_{d_I} in region I generate a correlated component of gate current $-j\beta_1 C_{11} i_{d_I}$ and an uncorrelated component $-j\beta i_{d_I} \sqrt{1-C_{11}^2}$. Hence the drain terminal fluctuation due to i_{d_I} is

$$\overline{i_4^2} = \overline{i_{d_I}^2} \left| 1 - \frac{\alpha g_m y_1}{\Delta} - \frac{j\beta_1 \alpha g_m C_{11}}{\Delta} (g_3 + y_1) \right|^2$$

$$+ \overline{i_{d_I}^2} (1-C_{11}^2) \left| \frac{\alpha g_m \beta_1}{\Delta} (g_3 + y_1) \right|^2 . \qquad (22)$$

Summing Eqs. (18), (19), (21), and (22) and dividing by (18) we have a noise figure

$$NF = 10 \log_{10} (1 + N_2 + N_3 + N_4 + N_5) \qquad (23)$$

where

$$N_2 = \left| \frac{y_1}{g_3} \right|^2 \frac{T_3 g_3}{T_1 g_1} \qquad (24)$$

$$N_3 = \frac{\overline{i_{d_{II}}^2}}{4kT_1 g_1 df\, g_m^2 g_3^2} \left| \begin{array}{c} (1+j\omega t)(y_1 y_2 + y_1 g_3 + y_2 g_3) \\ - j\beta_2 g_m (g_3 + y_1) \end{array} \right|^2 . \qquad (25)$$

N_4 is a similar expression with $\overline{i_{d_I}^2}$ substituted for $\overline{i_{d_{II}}^2}$, and $\beta_1 C_{11}$ substituted for β_2. Finally, the term due to the uncorrelated gate current (last term of (22)) is

$$N_5 = \frac{\overline{i_{d_I}^2} (1-C_{11}^2)}{4kT_1 g_1 df g_3^2} |\beta_1 (g_3 + y_1)|^2 . \qquad (26)$$

Region I Fluctuations

From PHS (55) and (25) we have for a single-sided device

$$\overline{i_{d_I}^2} = 4kT_o df \left(\frac{L_1}{g_o Z}\right) \frac{P}{(1-p)^2} \frac{\cosh^{2(\pi L_2/2a)}}{r_d^2} \tag{27}$$

where

$$g_o Z E_s = I_s, \quad P = P_o + P_\delta$$

and

$$r_d = (W/I_s) f_r(s_1 p) \tag{28}$$

To a very close approximation

$$r_d = \frac{WV}{I_d} \cosh \frac{\pi L_2}{2a} \tag{29}$$

where

$$V = 2p(1-p) + \xi L_1/L \tag{30}$$

Hence

$$\overline{i_{d_I}^2} = 4kT_o df \left(\frac{\xi L_1}{L}\right) \frac{PI_s}{Wv^2} \quad . \tag{31}$$

The gate circuit fluctuations induced by region I are [PHS (71)]

$$\overline{i_{g_I}^2} = 16\omega^2 kT_o df \left(\frac{L_1 Z}{g_o}\right) \left(\frac{kL_1}{\gamma_a}\right)^2 R \tag{32}$$

where $R = R_o + R_\delta$. Using

$$I_s = 2kWv_s Z/a \tag{33}$$

[PHS (65b), (13), and (25)] this can be written

$$\overline{i_{g_I}^2} = (\omega t_{ls}\eta)^2 (R/P)\ \overline{i_{d_I}^2} \tag{34}$$

where

$$t_{ls} = L_1/v_s \tag{35}$$

and

$$\eta = \xi L_1/L \quad . \tag{36}$$

Thus

$$\beta_1 = \eta\omega t_{ls}\sqrt{(R/P)} \quad . \tag{37}$$

Region II Fluctuations

For the single-sided device, from PHS (61)

$$\overline{i_{d_{II}}^2} = \frac{16\ I_d\ a^2\ q\ df\ S^2\ \Gamma^2}{\pi^3 v_s^{\,2} k^2 Z^2 r_d^{\,2}}\ U \tag{38}$$

where

$$S = \frac{2}{\pi(1-p)} \sin\frac{\pi}{2}(1-p) \quad , \tag{39}$$

$$\Gamma^2 = D/(av_s) \quad , \tag{40}$$

and

$$U \simeq \exp\frac{\pi L_2}{a} \tag{41}$$

to a close approximation, i.e.

$$U \simeq 4\left[\frac{1}{2}\exp\frac{\pi L_2}{2a}\right]^2$$

$$= 4\cosh^2(\pi L_2/2a) \quad . \tag{42}$$

Using Eqs. (29) and (33) above, we then have

$$\overline{i^2_{d_{II}}} = \frac{8.256\ q\ I_d^{\,3}\ S^2\ \Gamma^2\ df}{V^2\ I_s^{\,2}} \tag{43}$$

From PHS (78) we have for the gate current fluctuation, after some reduction,

$$\overline{i^2_{g_{II}}} = \left[\frac{\omega t_{1s} k'(\gamma=0)}{1-p}\right]^2 \overline{i^2_{d_{II}}} \tag{44}$$

or, for use in (21) above

$$\beta_2 = \frac{\omega t_{1s}(k'-\gamma p)}{1-p} \quad . \tag{45}$$

NF Expressions

Expanding the above in detail for computation, we have

$$N_2 = (g_1 + b_1^{\,2}/g_1)T_3/g_3T_1 \tag{46}$$

$$N_3 = \frac{2.064\ I_s(1-p)^3\ S^2\Gamma^2}{V^2(kT/q)g_m^{\,2}g_3^{\,2}g_1} \left|x_2^2 + y_2^2\right| \tag{47}$$

$$x_2 = g_1g_2 - b_1b_2 + g_3(g_1+g_2) + \beta_2 g_m b_1 - \omega t\left[b_1g_2 + g_1b_2 + g_3(b_1+b_2)\right] \tag{48}$$

$$y_2 = \omega t\left[g_1g_2 - b_1b_2 + g_3(g_1+g_2)\right] + b_1g_2 + g_1b_2 + g_3(b_1+b_2) - \beta_2 g_m(g_1+g_3) \tag{49}$$

$$N_4 = \left(\frac{T_o}{T_1}\right)\left(\frac{L_1}{L}\right) \frac{PI_s}{WV^2 g_m{}^2 g_3{}^2 g_1} \left| x_1^2 + y_1^2 \right| \qquad (50)$$

where x_1 and y_1 are identical to x_2 and y_2, except that $\beta_1 C_{11}$ is substituted for β_2. Finally,

$$N_5 = \frac{T_o}{T_1} \left(\frac{\omega t L_1}{L}\right)^2 \left(\frac{\xi L_1}{L}\right)^3 \frac{R\, I_s (1-C_{11}^2)}{WV^2 g_1} \left(1 + \frac{g_1}{g_3}\right)^2 + \left(\frac{b_1}{g_3}\right)^2 . \qquad (51)$$

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