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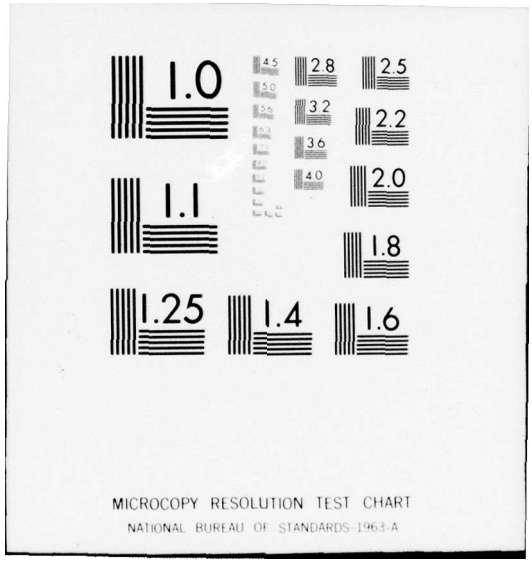
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MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING (MM&TE) PROGRAM FOR THE ESTABLISHMENT OF PRODUCTION TECHNIQUES FOR HIGH DENSITY THICK FILM CIRCUITS USED IN CRYSTAL OSCILLATORS

FIRST QUARTERLY PROGRESS REPORT

6 AUGUST 1976 - 21 NOVEMBER 1976

CONTRACT NO. DAAB07-76-C-8119

PLACED BY

PRODUCTION DIVISION
PROCUREMENT AND PRODUCTION DIRECTORATE
USAECOM, FORT MONMOUTH, N.J. 07703

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PREPARED BY

RAYTHEON COMPANY
INDUSTRIAL COMPONENTS OPERATION
QUINCY, MASSACHUSETTS 02169

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period: the configuration design of the TCVCXO module, the detailed layout design of the hybrid microcircuitry used in the TCVCXO module, the detailed design of piece-parts to be used in hermetically sealing the hybrid microcircuits and encapsulating the modules, the breadboard analysis of the TCVCXO electrical design, the establishment of process flow plans for producing the modules, and the selection and procurement of component parts and materials for the construction of the TCVCXO modules. Details of this work are reported.

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6 AUGUST 1976 - 21 NOVEMBER 1976

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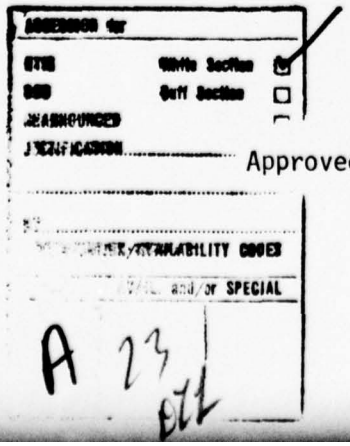
PREPARED BY

CHARLES T. MARTIN

OBJECT OF STUDY

The objectives of the program are to establish production techniques for high density thick film hybrid microcircuits used in crystal oscillators and to produce quantities of a 20 MHz temperature-compensated, voltage-controlled crystal oscillator (TCVCXO) using those techniques.



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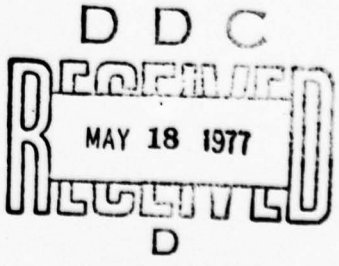

ABSTRACT

Production techniques are being established for a thick film hybrid microelectronic 17-22 MHz, temperature-compensated, voltage-controlled crystal oscillator. The program requirements, the plan for meeting those requirements, the technical approach being pursued and the technical work that has been accomplished are described. The program is subdivided into an engineering phase and a production phase. The engineering phase was started, with the following being accomplished during this reporting period: the configuration design of the TCVCXO module, the detailed layout design of the hybrid microcircuitry used in the TCVCXO module, the detailed design of piece-parts to be used in hermetically sealing the hybrid microcircuits and encapsulating the modules, the breadboard analysis of the TCVCXO electrical design, the establishment of process flow plans for producing the modules, and the selection and procurement of component parts and materials for the construction of the TCVCXO modules. Details of this work are reported.

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1.0 INTRODUCTION

This report covers the first quarter of a two-year manufacturing methods and technology engineering program underway at Raytheon under contract no. DAAB07-76-C-8119. The objectives of the program are to establish production techniques for high density thick film hybrid microcircuits used in crystal oscillators and to produce quantities of a 20 MHz temperature-compensated, voltage-controlled crystal oscillator (TCVCXO) using those techniques. This report describes the program requirements, Raytheon's program plan for meeting those requirements, Raytheon's technical approach and the technical work performed on this program to date.

1.1 Basic Theory of Operation (Ref. 1)

The temperature-compensated, voltage-controlled, crystal oscillator, being put into production on this program, is a wide-temperature range, gun-hardened module for use in remotely-monitored battlefield sensor transmitters. It features ± 5 ppm overall frequency stability (± 2 ppm frequency/temperature stability plus ± 3 ppm from sh ock, aging and other effects). It has the capability for both digital and frequency-shift keying (fsk) and analoge modulation. Deviation sensitivity is 500 Hz per volt and deviation linearity is better than 5%. The unit is powered by a single 12 VDC supply and dissipates a nominal 50 mW. Physically, the TCVCXO has the geometry of a truncated cylinder and is designed to be inserted directly into a printed-circuit-board type connector.

The functional block diagram for the TCVCXO is as shown in figure 1. The oscillator stage is an antiresonant Pierce crystal oscillator circuit which contains a voltage-variable capacitance (VVC diode) in series with the crystal. The output frequency is changed in response to a variation in the voltage applied across this capacitance. The linearization of the nonlinear relationship between output frequency and applied voltage is accomplished by a diode function generator which produces a two-segment voltage transfer characteristic having a nonlinearity approximately the reverse of the oscillator's frequency/voltage tuning characteristic. Thus linearization to better than 5% over a deviation range of 100 ppm is achieved, and simultaneous digital, fsk or linear analog modulation, temperature compensation and frequency trim are possible.

The temperature compensation is accomplished by a six-segment DFG which produces both positive and negative slope segments to approximate a cubic function, which is the reverse of the crystal's frequency- temperature characteristic. The compensating DFG is driven by a temperature sensing circuit employing the repeatable temperature characteristics of a silicon diode to sense the package temperature.

The summing amplifier is a differential operational amplifier which combines six separate voltages for operation within the linearized section of the frequency voltage tuning characteristic. The six inputs are voltages for (1) temperature compensation, (2) digital (fsk) modulation, (3) analog control (logic 0 or 1 which restores center frequency for analog modulation),(4) analog modulation, (5) frequency adjust for frequency calibration of the TCVCXO, and (6) a voltage derived from a silicon diode temperature sensor to cancel the temperature effects of similar diodes in the linearization DFG. The voltage regulator, shown in the block diagram, supplies a regulated 9V derived from the input supply voltage which can vary from 10 to 15 VDC.

Nominal frequency of operation of the TCVCXO is established by use of a crystal having a resonant frequency in the range 17 MHz to 22 MHz. The TCVCXO is designed to use a new ceramic flatpack crystal which is microcircuit-compatible. This flatpack crystal is government-developed and government-furnished.

To achieve, in manufacture, the exact performance required of the TCVCXO, functional resistor trimming is used advantageously. Initially the 105 resistors in the TCVCXO are passively trimmed to a 5% tolerance and 12 of them are subsequently functionally trimmed: seven to provide a given dc voltage, two to provide ac (audio) voltage and three to provide a given rf output frequency. (See Appendix B herein.)

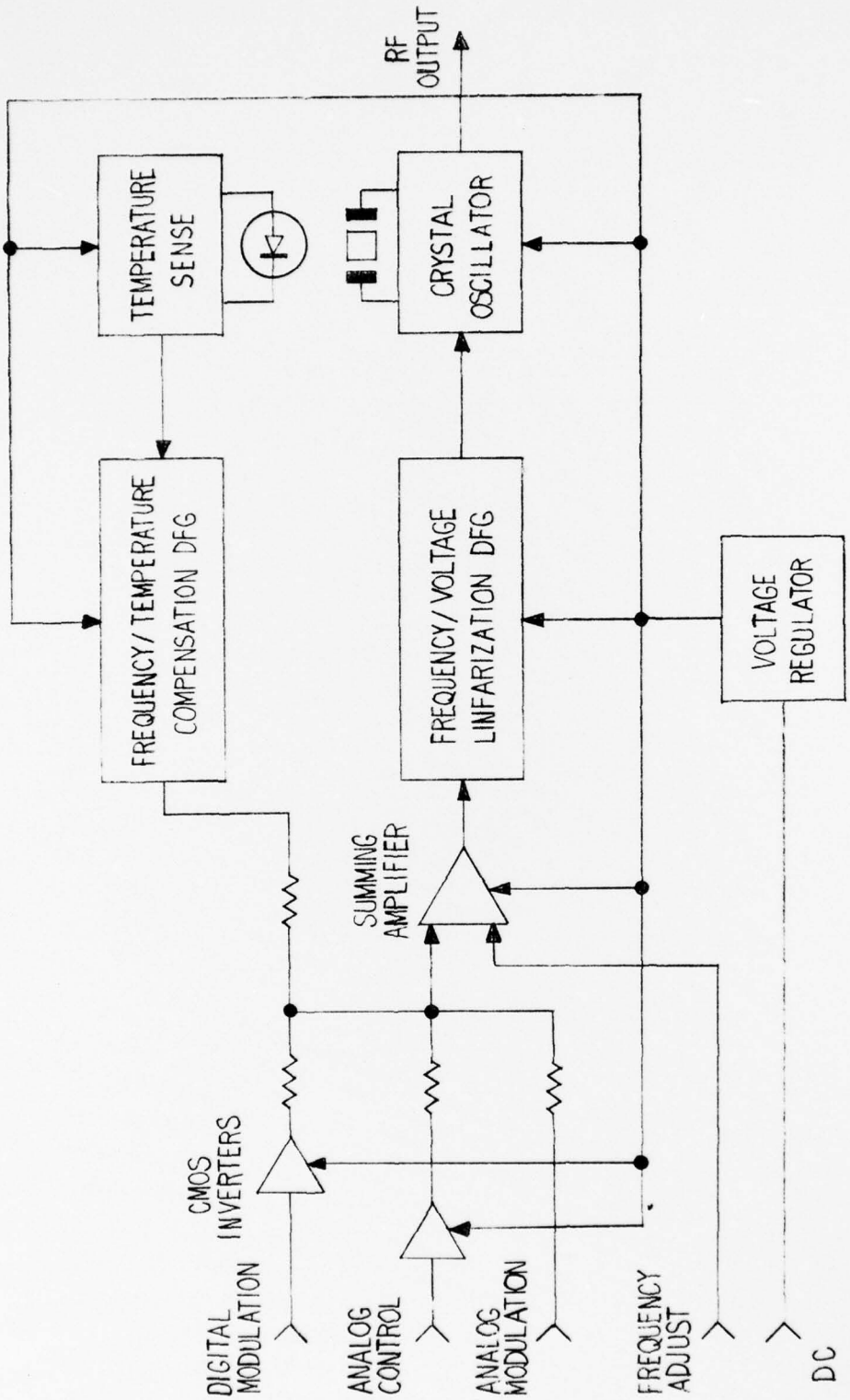


Figure 1. TCVCXO Block Diagram

2.0 PROGRAM OBJECTIVES

Raytheon is carrying out this Manufacturing Methods and Technology Engineering (MM&TE) program in accordance with Electronics Command Industrial Preparedness Procurement Requirements meeting Electronics Command Technical Requirements SCS-483 (Appendix A herein) for a hermetically-sealed 17 MHz to 22 MHz temperature-compensated, voltage-controlled crystal oscillator (TCVCXO). The objective of the Industrial Preparedness program is to establish a production capability for meeting estimated military needs for a period of two years after completion of the MM&TE program and to establish a base and plans which may be used to meet expanded production requirements. The objectives of the subject MM&TE program are to establish the producibility of the TCVCXO module by mass production techniques and with mass production facilities, to establish a quality control system for production, and to take actions necessary to reduce the time required for delivery of modules in large quantity.

The MM&TE program encompasses the following:

a) Performance of the necessary design, development engineering, fabrication of special tooling, and construction of test facilities and limited production equipment as required, to obtain confirmatory sample approval, establish a pilot line and make a pilot run for proving out a manufacturing process using production methods and techniques.

b) Accomplishment of all production planning necessary to expand to produce according to the planned production schedule on a mass production basis, short of procuring tooling, equipment and materials, and short of actual manufacture of the planned production schedule quantities.

TCVCXO modules are to be fabricated and delivered on this program in four lots as follows:

- Engineering Samples
  - First Submission 10 ea.
  - Second Submission 15 ea.
- Confirmatory Samples 50 ea.
- Pilot Run Units 100 ea.

The TCVCXO module is a ± 5 ppm frequency tolerance quartz oscillator designed to operate over a wide temperature range (-40°C to + 85°C) and in a mechanical shock environment (1000 g's). The electrical and mechanical design and performance are as defined in the ECOM Technical Requirements SCS-483, with exceptions to be noted. The electrical approach taken by the government avoids the use of inductors, which do not readily lend themselves to microcircuit construction, and uses functional thick film resistor trimming to achieve exact required performance in terms of frequency linearization and temperature compensation. A government-prepared functional resistor trimming procedure has been supplied to Raytheon for use on this program and is included in this report as Appendix B.

The specified mechanical approach uses a crystal enclosed in a custom hermetically-sealed ceramic flatpack that is compatible with hybrid microcircuit construction. This package, developed by ECOM, is 0.40" x 0.40 x 0.10" in size. These crystals are to be government-furnished parts on the current program.

Early in the program, changes were prescribed by ECOM in the TCVCXO module outline dimensions and electrical design from that shown in the SCS-483 specification. Figures 2 and 3 show the original and the revised electrical schematics. The revised module outline is reflected later in figure 4.

Also, due to the expected non-availability of the ceramic flatpack until late in the program, it was further specified that crystals housed in a conventional HC-18 holder be used in fabricating the engineering samples. The impact of this change in the module design will be shown later in Section 4.1 of this report.

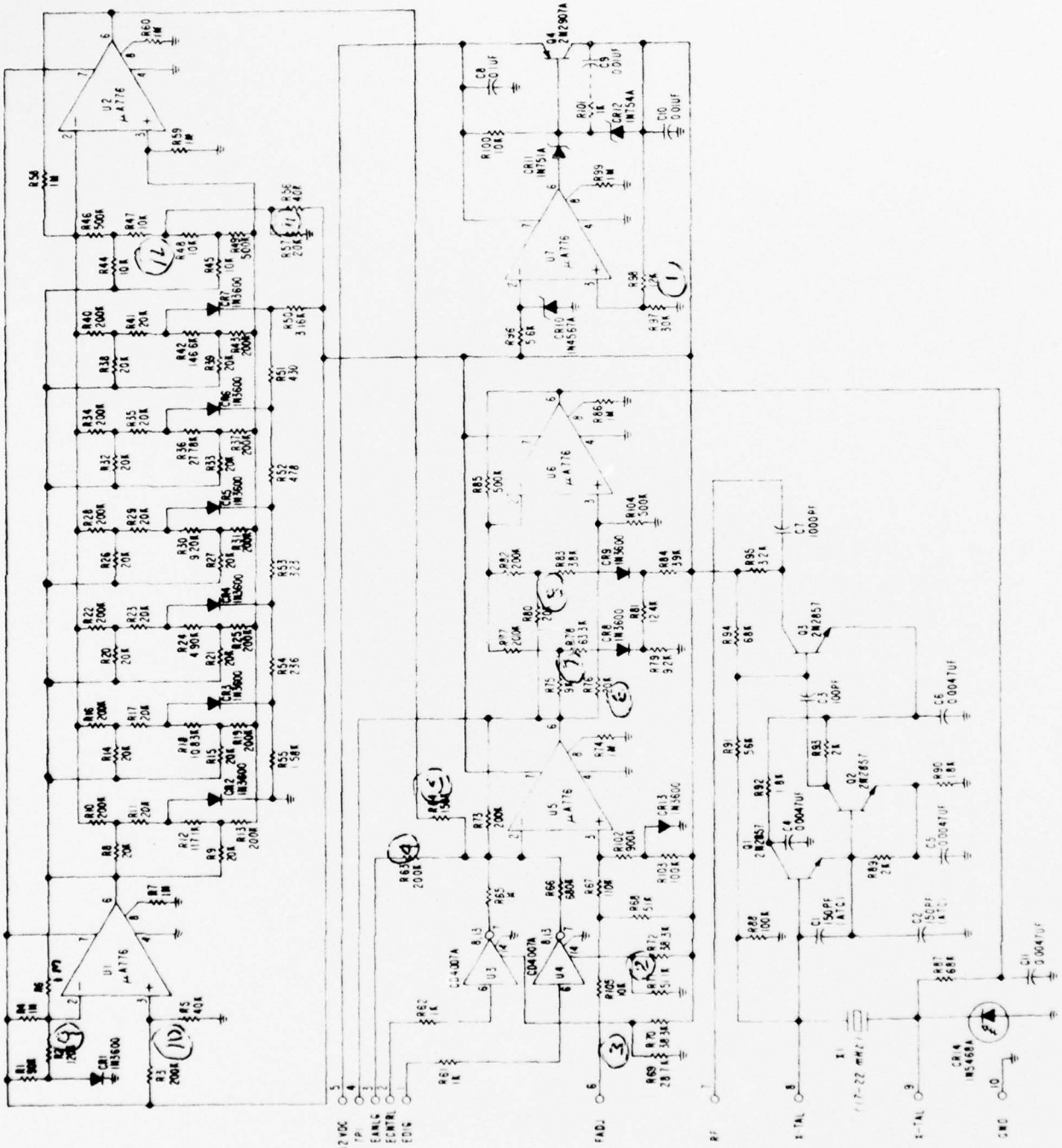


Figure 2. TCVCXO Electrical Schematic (original)

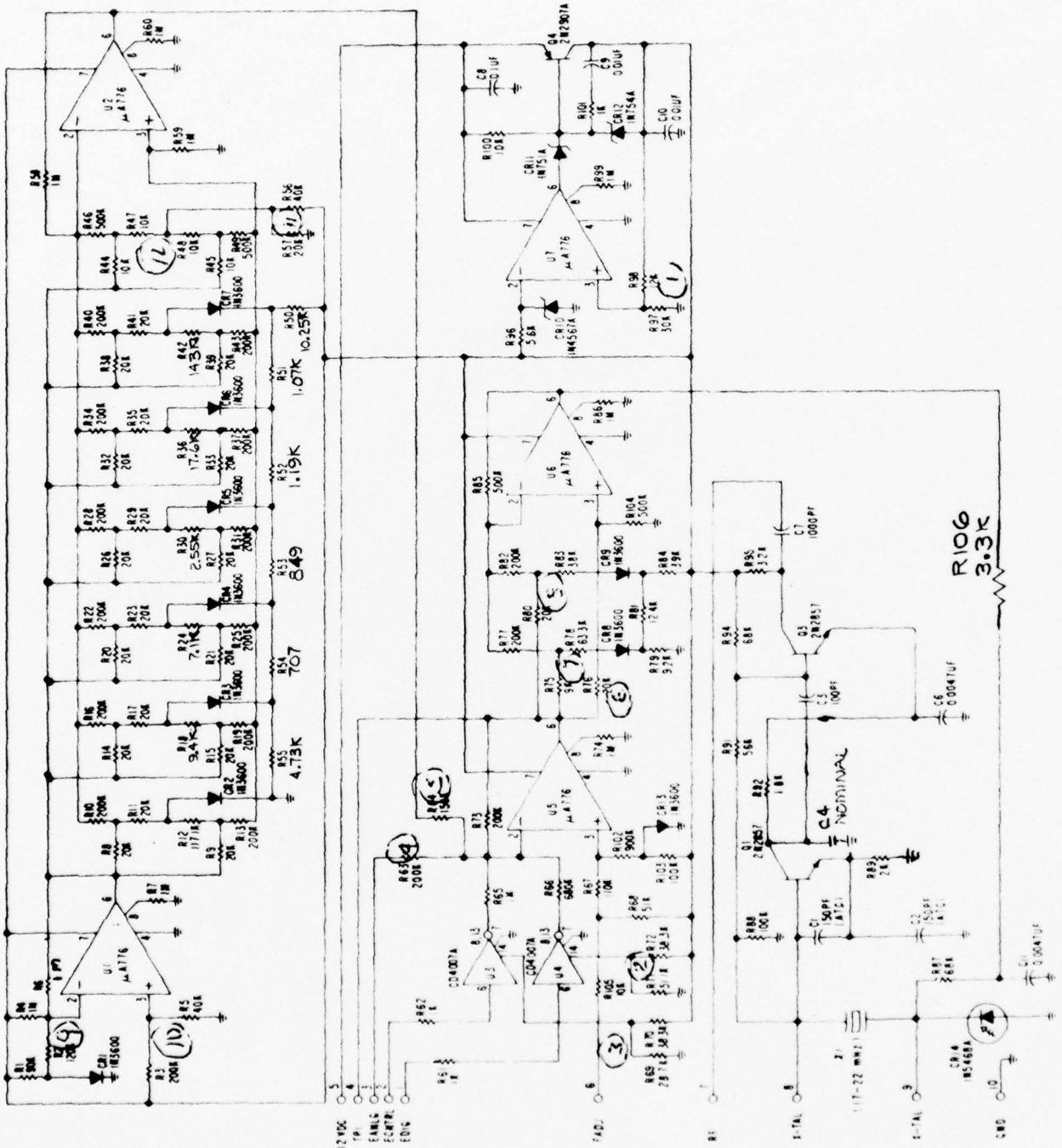


Figure 3 TCVCXO Electrical Schematic (revised)

3.0 PROGRAM PLAN

The MM&TE program has been divided into two distinct phases: an engineering phase of ten months duration and a production phase of 12 months duration. An additional month is allocated between the engineering and production phases for customer review and approvals, and following the production phase for final report preparation and submission.

The engineering phase consists of the following principal efforts:

- breadboard analysis of the electrical design
- hybrid microcircuit and module design and design documentation
- generation of the process flow plan
- development of processes that are new or have aspects that are unique to the TCVCXO and documentation of these processes
- design and fabrication of special tooling, test fixturing and test boxes
- fabrication and testing of engineering samples in two lots of 10 and 15 each.

The production phase consists of the following principal efforts:

- generation of source control documentation for purchased parts and materials
- generation of incoming inspection procedures for purchased parts and materials
- generation of production operation standards for each process step
- generation of production test procedures and test specifications
- fabrication and testing of 50 confirmatory samples
- fabrication and testing of 100 pilot run units at the specified rate

4.0 TECHNICAL APPROACH

4.1 Module Configuration and Construction

The TCVCXO module, as specified by ECOM, consists of two hermetically-sealed hybrid microcircuit substrate assemblies bonded together, back-to-back, having a frequency-adjust potentiometer attached thereto and encapsulated in the form of a truncated cylinder. (See Appendix A for details of the specification.) Accordingly, the approach Raytheon has taken to implement these requirements was first to generate a dimensioned module configuration drawing (figure 4) showing construction details down to the hybrid microcircuit level. The substrate size was fixed at 1.515" x 0.900" x 0.030" nominal, both hybrids utilizing the same size substrate. Hermetic sealing of the substrate assemblies is to be accomplished using alumina ceramic corrals and flat metal covers, as shown. The drawing also shows two alternative crystal packages and locations, as required. The specified module outline is to be achieved by using a plastic potting shell.

The alumina corral is to be sealed to the processed thick film substrate using a conventional solder glass. The top surface of the corral is metallized and has a Kovar frame brazed to it. The flat Kovar cover is to be sealed to this frame by parallel seam welding. Details on the design and construction of the corrals, frame, brazing alloy preform and cover are given in figures 5 through 8.

The approach selected for encapsulating the module to the required form factor is to insert the module assembly into a potting shell and back fill the shell with a low density epoxy, so as to meet the weight specification. The potting shell design concept is pictured in figure 9.

The two hybrid microcircuits are to be bonded together using an epoxy preform. Plans are to use Ablefilm 550 epoxy film adhesive for this bond. The potentiometer and the HC-18 crystal can (when used) will be epoxied to the top of the sealed VCXO hybrid and the leads soldered to appropriate termination pads on the substrate, as shown in figure 4.

Two modifications to the design of the module have been requested by ECOM, but not yet implemented. These are (1) a means for withdrawing the module from a cavity in its next level of assembly wherein only the end face opposite the connector is accessible and (2) a means for protecting the potentiometer from excessive moisture such as would be provided by a

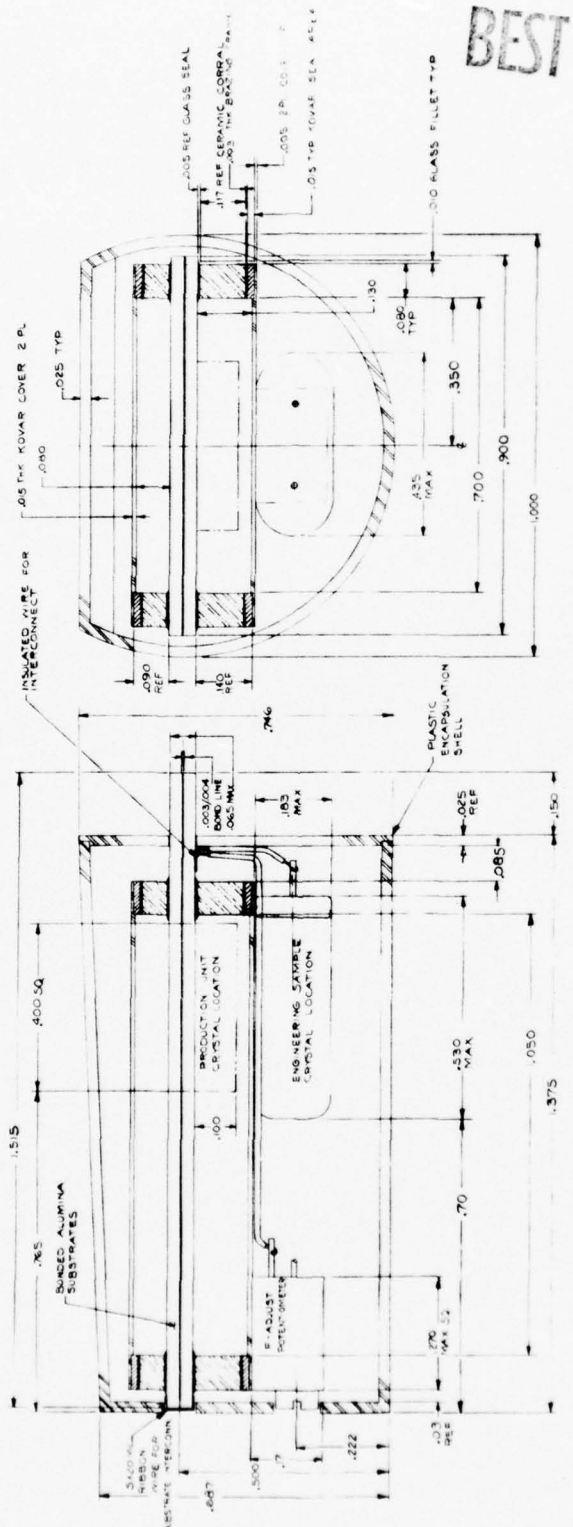
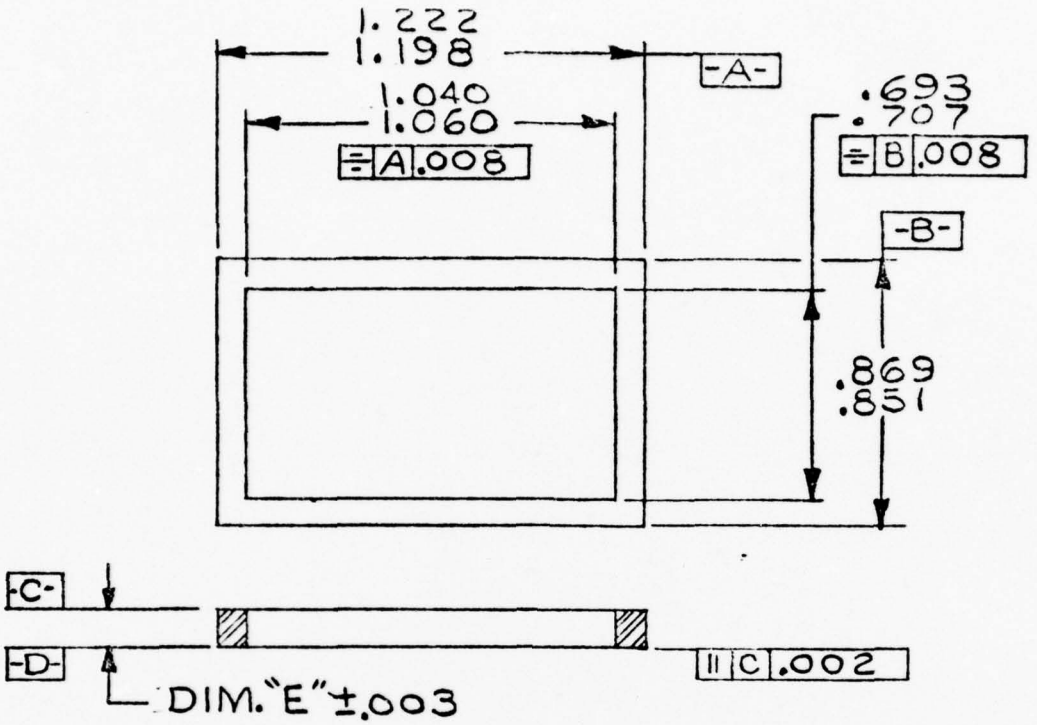


Figure 4. TCVCXO Module Assembly

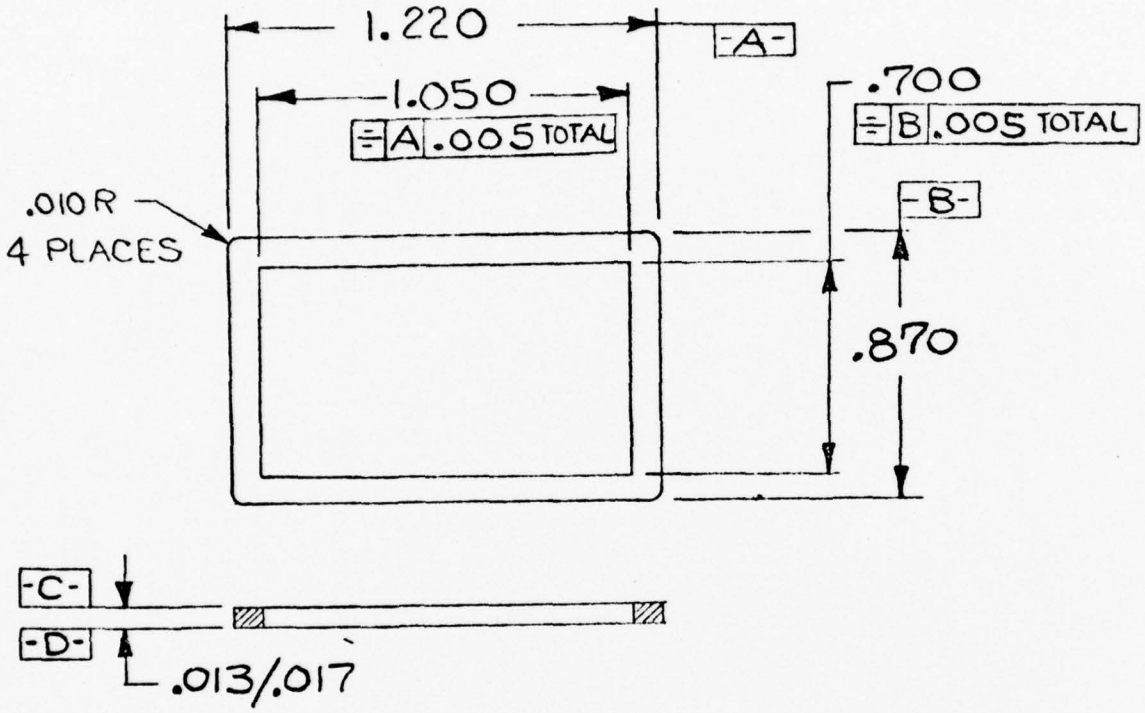


PART NO.	DIM. "E"
950190-1	.117
950190-2	.067

NOTES

1. MATL: ALUMINA, 96 % Al_2O_3, COLOR - WHITE
2. REMOVE ALL BURRS AND SHARP EDGES .005 R MAX
3. SURFACES C AND D TO BE FLAT WITHIN .001
4. SURFACE C TO BE MOLY-MANGANESE METALLIZED THEN NICKEL PLATED & GOLD FLASH 50 µIN MIN.
5. TOL: UNLESS OTHERWISE SPECIFIED: XXX ±.005

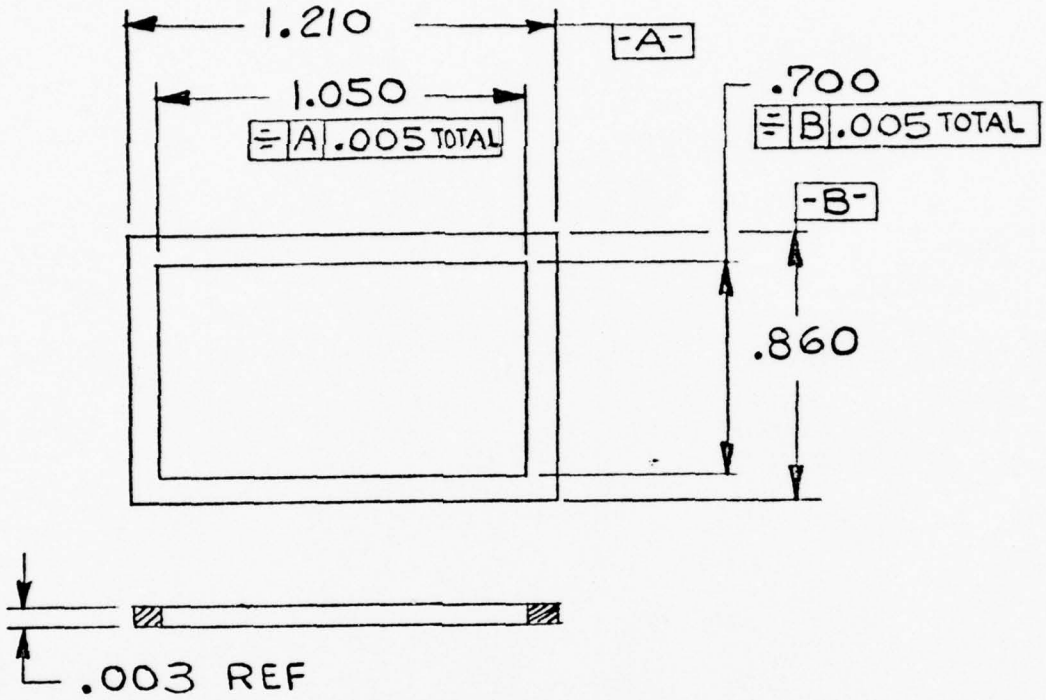
Figure 5. Ceramic Corral Design



NOTES

1. MATL: KOVAR
2. PLATING: SULFAMATE NICKEL PER MIL-P-27418, .0003/.0005 THK
3. TOL: UNLESS OTHERWISE SPECIFIED; XXX ±.005
4. SURFACES C AND D TO BE FLAT WITHIN .001
5. TEMPER - ANNEALED

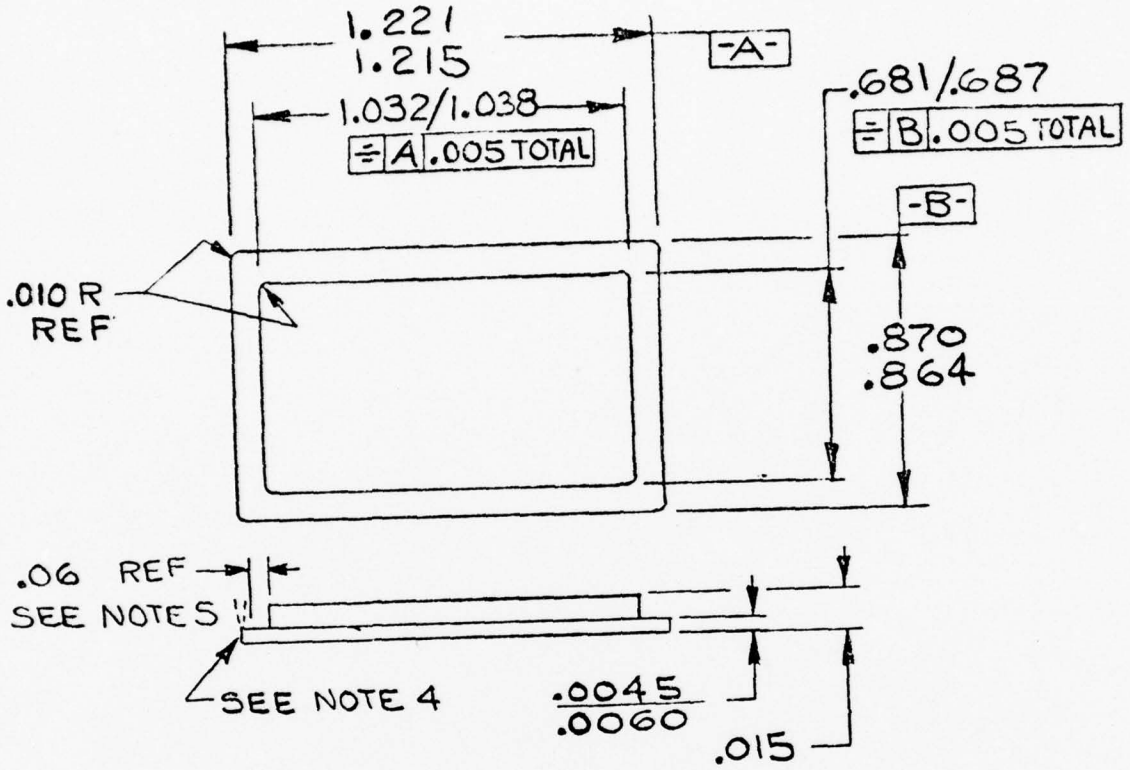
Figure 6. Metal Frame Design



NOTES

1. MATL: .003 THK CUSIL, 72% SILVER, 28% COPPER PER ASTM-AWS BAg-8 OR EQUIV.
2. TOL: UNLESS OTHERWISE SPECIFIED, XXX ±.005

Figure 7. Brazing Alloy Preform Design



NOTES

1. MATL: KOVAR
2. PLATING: TBSL
3. TOL: UNLESS OTHERWISE SPECIFIED XXX ± .003
4. THIS EDGE TO BE SQUARE WITHIN .0005
5. ZONE FOR THICKNESS MEASUREMENT
6. TEMPER - ANNEALED

Figure 8. Metal Cover Design

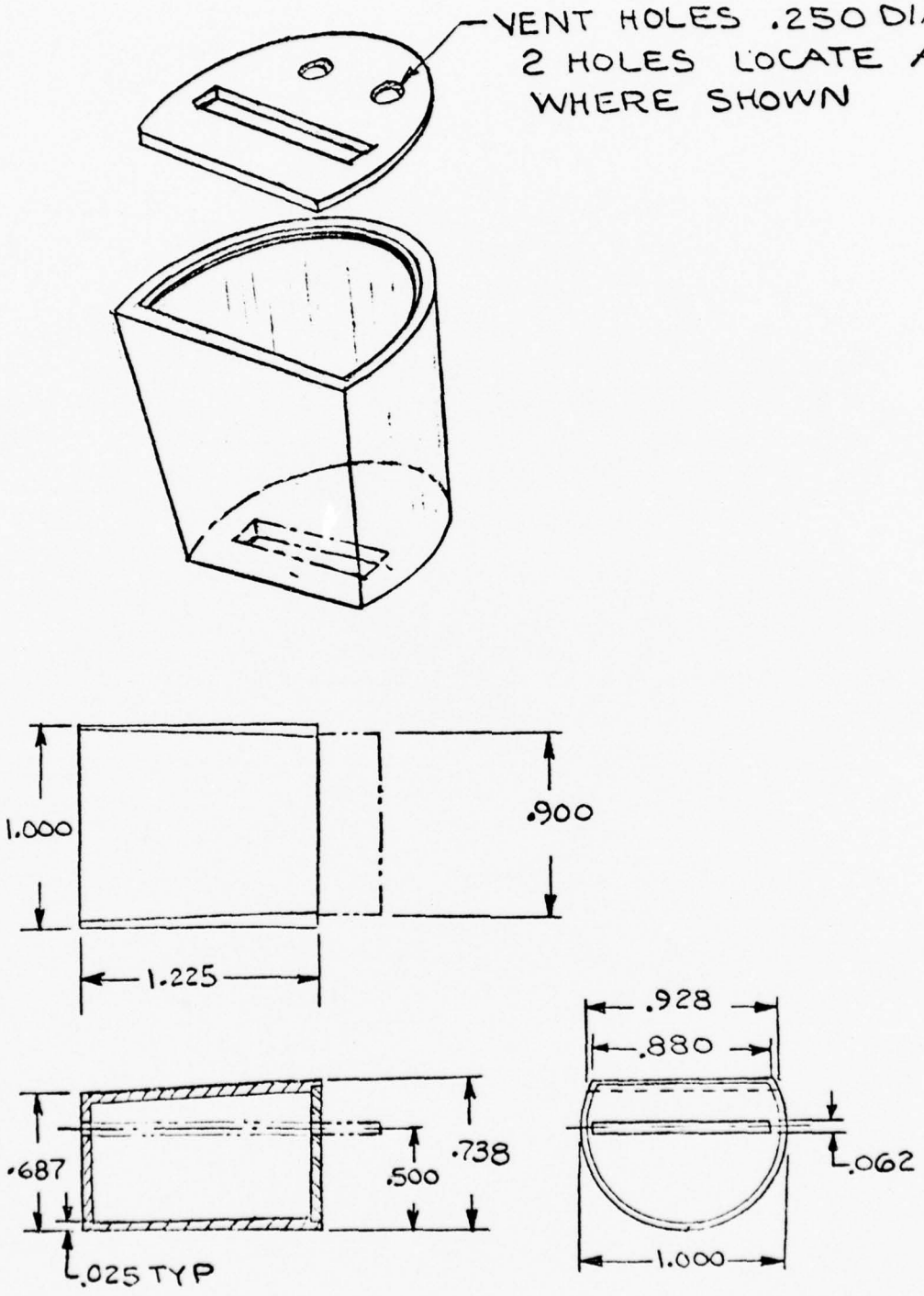


Figure 9. Potting Shell Design

flush nylon screw plug covering the adjustment screw access hole.

The basic construction of the two hybrid microcircuits is described in the following section.

4.2 Hybrid Microcircuit Construction

The electrical circuit for the TCVCXO has been partitioned into two functional parts, called the linearized voltage-controlled crystal oscillator (or VCXO) section and the temperature-compensated diode function generator (or TC) section. The partitioning is as shown in figure 10. Each part will be fabricated as a separate hybrid microcircuit. Each hybrid consists of a 1.515" x 0.900" x 0.030" alumina substrate metallized with a thick film conductor-resistor pattern. Integral crossover connections are achieved by means of thick film conductor segments insulated from the main pattern by thick film dielectric material. Chip components attached to the metallized substrates complete the circuits. The chip components consist of diodes and transistors in both beam lead and chip-and-wire form, integrated circuits in chip-and-wire form, and chip capacitors. In addition, the VCXO hybrid contains a crystal which is housed in a custom ceramic flatpack. Table 1 gives the component count by generic type and the method of component assembly for each hybrid type.

4.3 Process Flow Plan

A tentative process flow has been defined for each of the hybrid microcircuit types and for the module. The flow plan is shown in three parts in figures 11, 12 and 13. These figures also show the hierarchy of processing and testing temperatures for the hybrids and modules. Where no temperature is shown, that process step occurs at room temperature.

It has been specified that the first lot of engineering samples (10 lot) are not to be encapsulated and that no more than six of the second lot (15 lot) are to be encapsulated. Also, the engineering samples are to be built using non-ruggedized crystals in the HC-18 cans rather than ruggedized crystals in the ceramic flatpacks, the latter not yet being available. Consequently the flow plans have been modified for the engineering samples, figures 14, 15 and 16. The flow plans are all subject to revision or refinement based on results of their implementation on the engineering sample build.

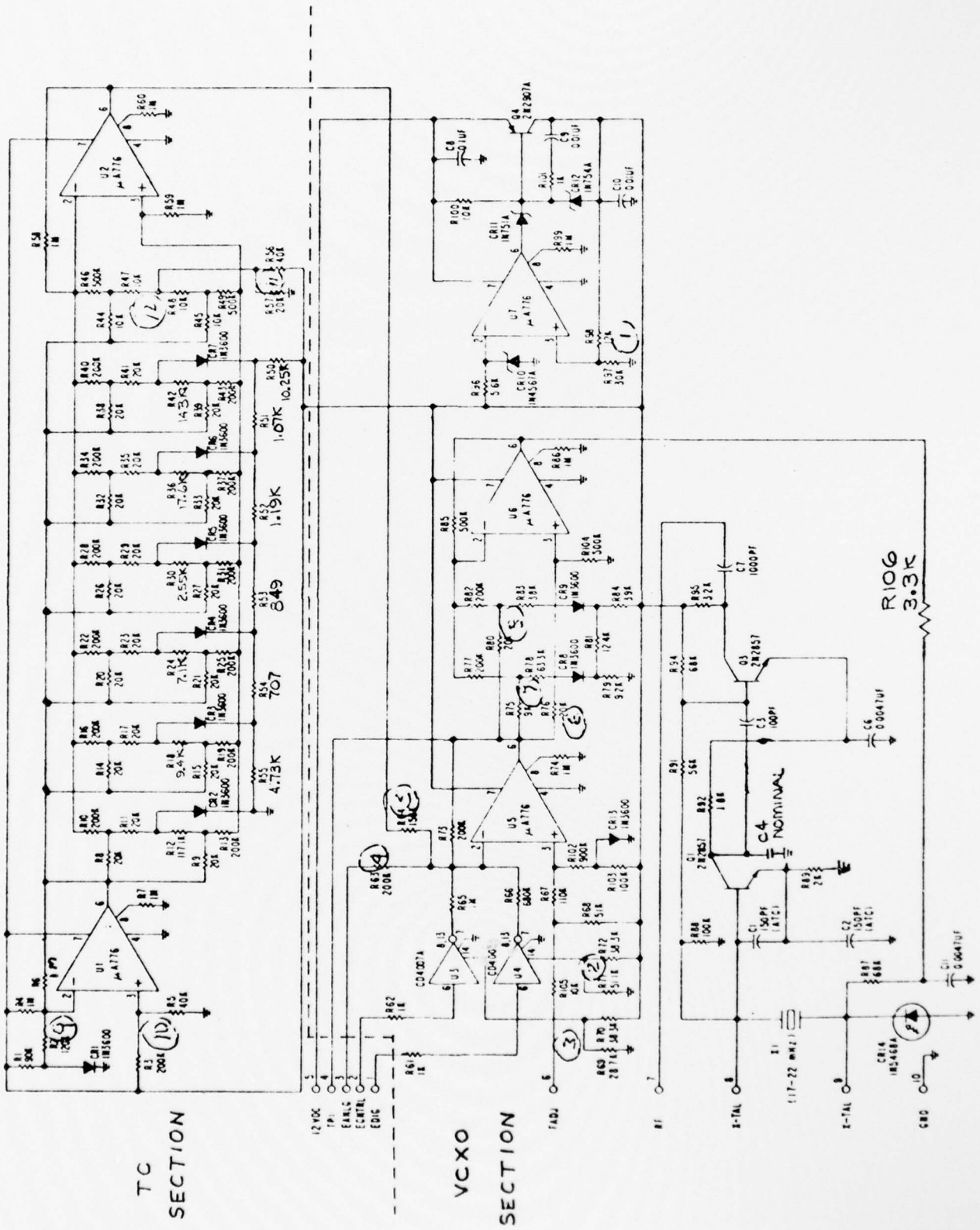


Figure 10. Partitioned TCVCXO Circuitry

TABLE 1. COMPONENT COUNT AND ASSEMBLY

Component	Assembly Method	Qty./Substrate Type TC	VCXO
Ceramic Chip Capacitors	Soldering	--	9
Porcelain Chip Capacitors		--	2
Bipolar IC Chips	Eutectic die bonding	2	3
Transistor Chips	& ultrasonic (gold)	--	2
Diode Chips	ball bonding	--	4
Beam Lead Transistors	Wobble TC	--	1
Beam Lead Diodes	bonding	7	3
C-MOS IC Chips	Epoxy die bonding & ultrasonic (gold) ball bonding	--	2
Crystal Flatpack	Soldering (case & leads)	--	1
TOTAL		9	27

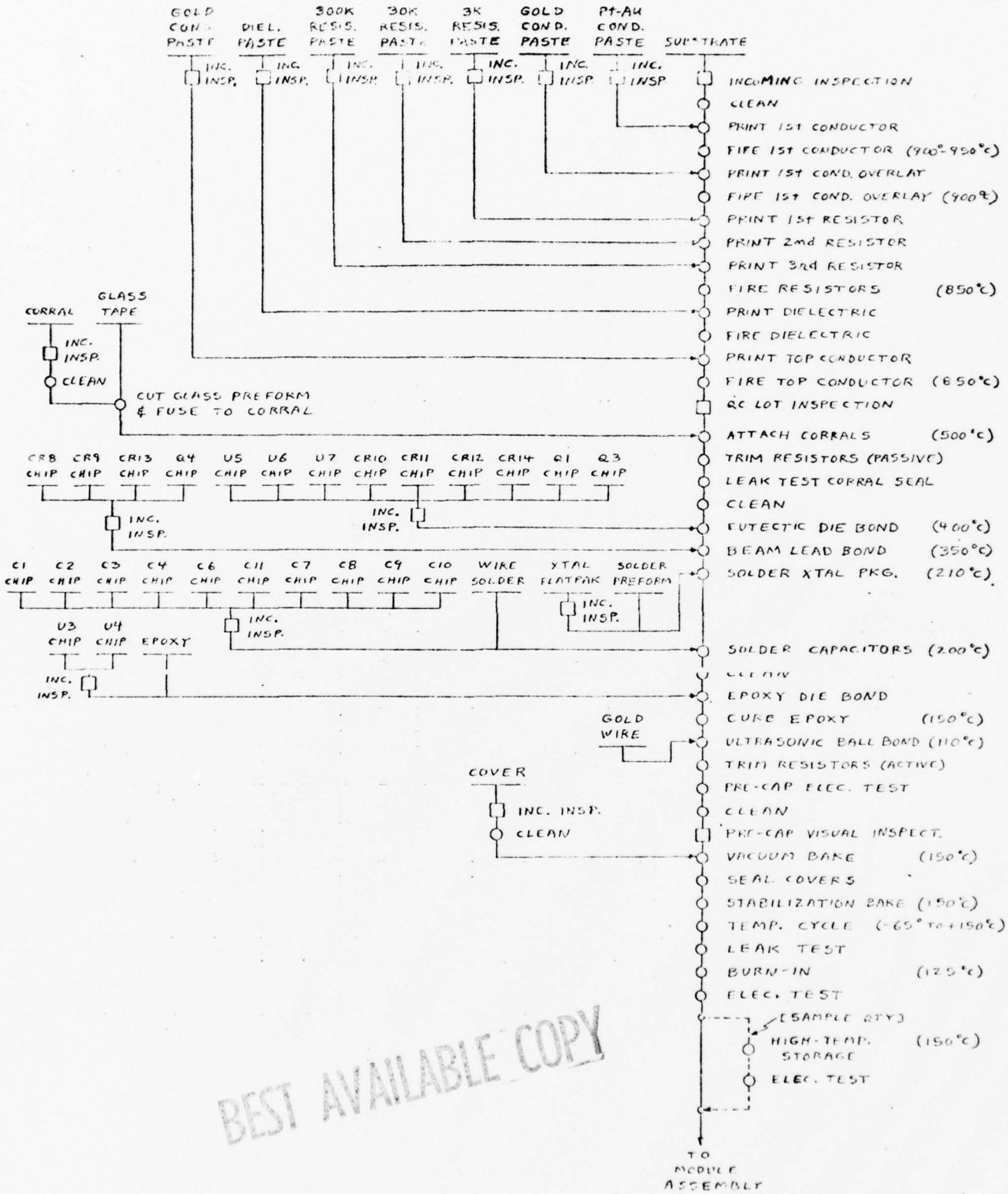


Figure 11. Process Flow Plan for VCXO Hybrid

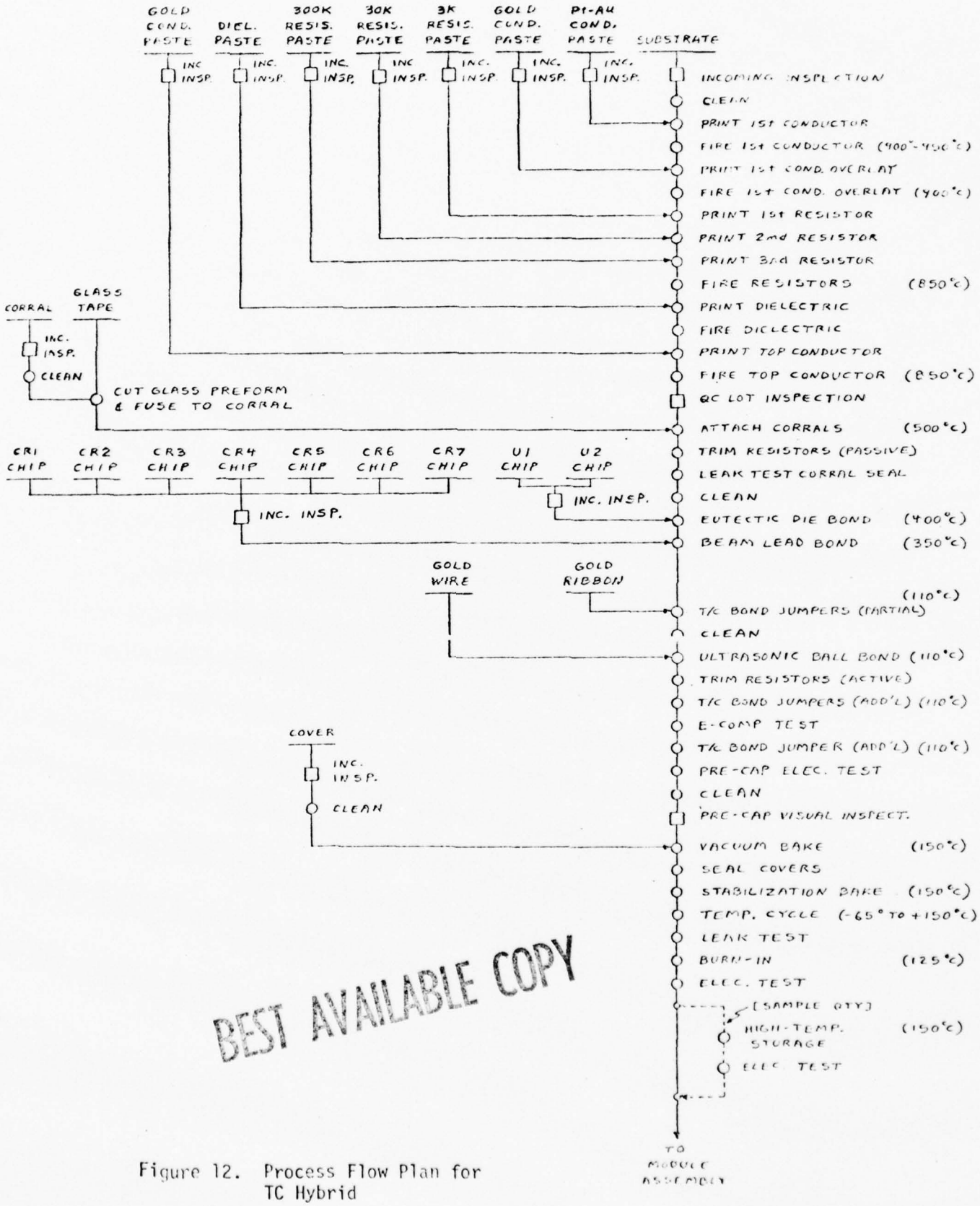


Figure 12. Process Flow Plan for TC Hybrid

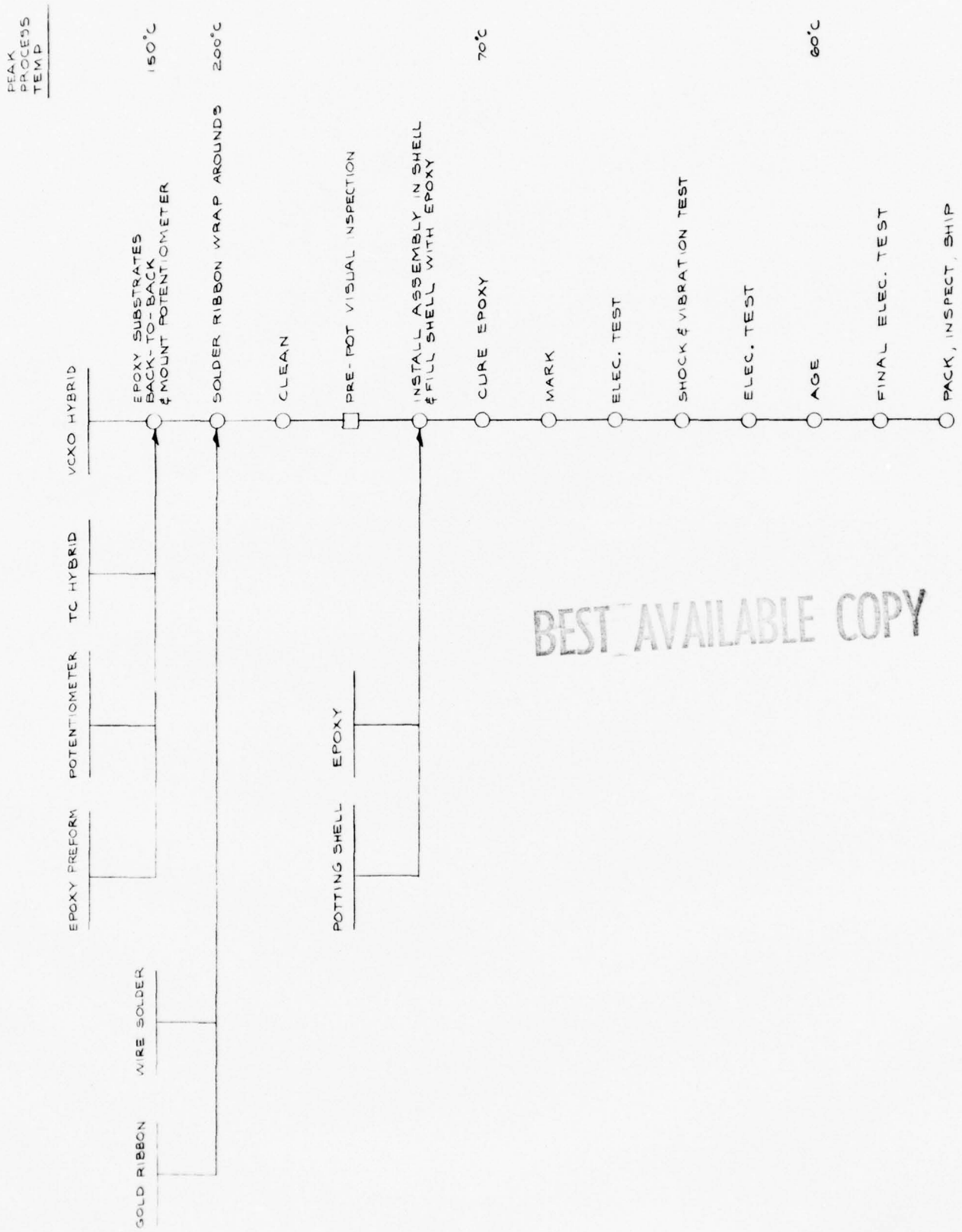


Figure 13. Process Flow Plan for TCVCXO Module

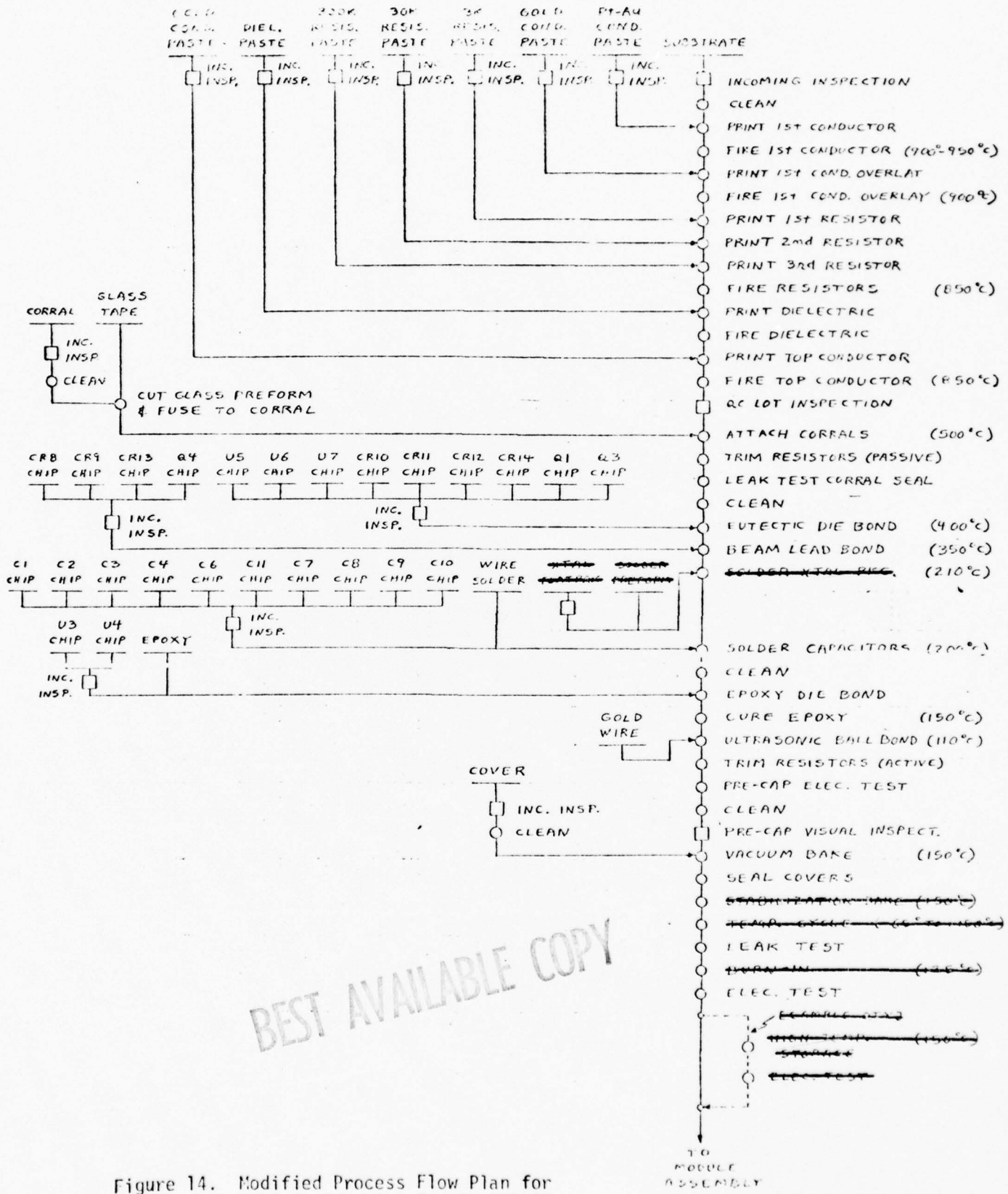


Figure 14. Modified Process Flow Plan for VCXO Engineering Sample Hybrids

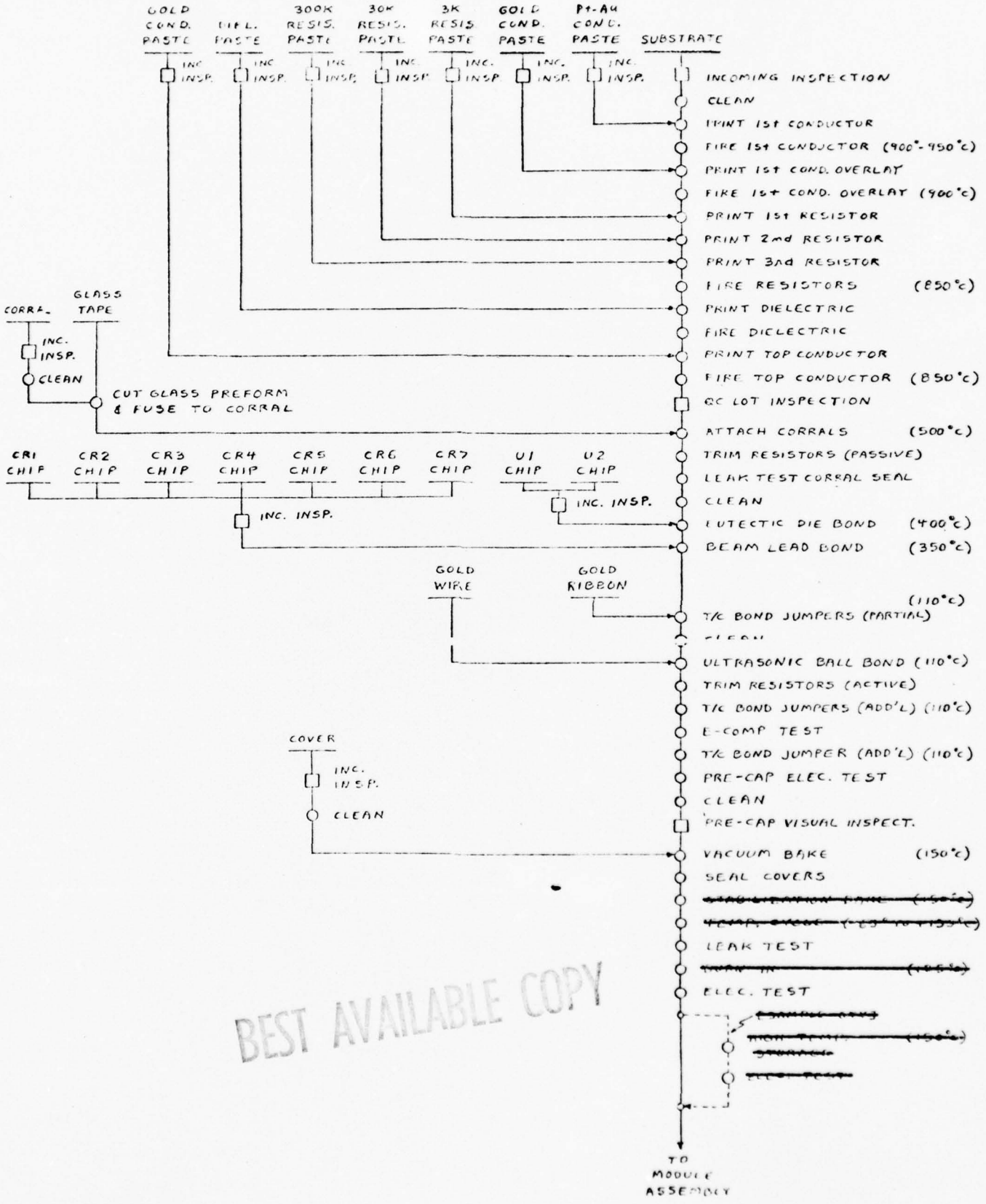


Figure 15. Modified Process Flow Plan for TC Engineering Sample Hybrids

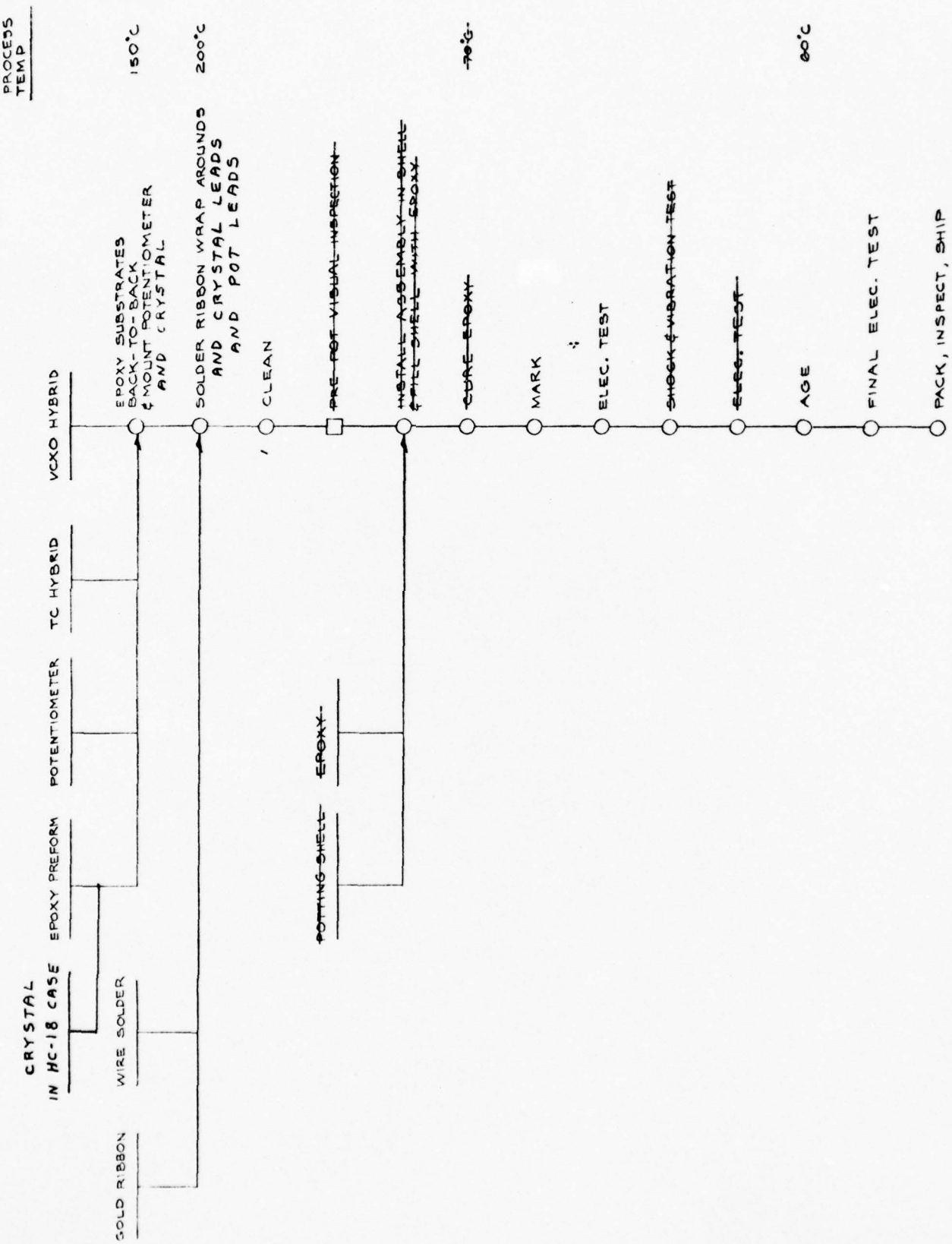


Figure 16. Modified Process Flow Plan for TCVCXO Engineering Samples Modules

Ultrasonic ball-bonded gold wire will be used for the interconnection of non-beam-leaded semiconductor chips. Gold wire has been selected over aluminum out of deference to the well-documented reliability problems associated with aluminum wire bonds on most thick film gold materials. Ultrasonic ball bonding was selected over conventional thermocompression bonding to avoid exposure of the gold wire-to-aluminum film interface on the chips to excessively high temperatures and an attendant "purple plague" intermetallic problem.

Th selection of soldering and eutectic die bonding as the processes for attaching chip capacitors and semiconductor dice, respectively, was made because the use of conductive epoxy was expressly prohibited on this program.

5.0 ELECTRICAL DESIGN ANALYSIS

The electrical design of the TCVCXO, as defined in the ECOM Technical Requirements SCS-483 and as later modified by ECOM, was breadboarded by Raytheon at the start of the Engineering Phase. The objectives in so doing were to gain a working familiarity with the electrical design and performance prior to microcircuit design, fabrication and testing and to have a vehicle for use in developing test procedures and test set-ups for use in module testing later in the program.

The breadboard was built using standard discrete components, with the exception of the two capacitors C1 and C2 in the oscillator stage. The actual porcelain chip capacitors were used in the breadboard but with leads pre-attached.

The basic approach pursued in testing the breadboard was to first obtain an operating circuit, then to implement the resistor functional trim procedure, and then to check the performance of the breadboard against the specifications in SCS-483.

Progress was initially impeded by a problem encountered with spurious oscillations in the breadboard and then with a distorted RF output voltage waveform. The spurious oscillation problem was eventually solved by a slight change in breadboard layout and by grounding the transistor cases in the oscillator stage. The distorted output turned out to be characteristic of the electrical design, and hence solvable only by a change in design. This was not attempted, since output distortion is not an item in the performance specification and since development of the electrical design is out of the scope of this program, as defined.

Another significant problem encountered early in breadboard testing was a limited modulation capability. As the oscillator stage was laid out, stray capacitances tended to swamp out the effect of the variable capacitance diode CR14 and therefore limited the shift in frequency achievable by modulation. A layout revision solved the problem.

The net effect of the problems encountered were to impede progress sufficiently to prevent complete performance testing of the circuit to specification during this reporting period. The resistor functional trimming procedure was fully evaluated, however, and the results used in designing the layouts for the hybrid microcircuits.

A summary of the accumulated observations resulting from breadboard testing are as follows:

a) The layout of the oscillator stage of the TCVCXO must be tight to reduce stray impedances.

b) The temperature-sensing diode CR1 must be located physically close to the crystal in order to achieve proper temperature compensation.

c) The VCXO deviation linearity appears to be marginal. Apparently the one break-point in the linearization network is not effective. A redesigned network having two break-points would seem to be in order.

d) The frequency adjustment range appears to be excessive, resulting in rather low adjustment sensitivity.

e) The RF voltage waveform is not sinusoidal.

f) The oscillator transient frequency stability is within 2 Hz from 5 ms to 100 ms after initial turn-on.

g) The 9-volt regulator output varies -0.003%/°C. A 40 mV change in the 9 volt supply causes a $\pm$ 0.5 ppm frequency shift.

h) It is apparently necessary to follow precisely the ECOM twelve-step functional trim procedure for resistors, in order to obtain adequate temperature compensation.

i) The best frequency-temperature stability achieved in the breadboard over the range -40°C to + 75°C was 6.4 ppm ($\pm$ 3.2 ppm) at center frequency. This was achieved using crystal S/N 19 which has a nominal frequency of 18 MHz and a turning point separation of 20 ppm or 360 Hz. The frequency-temperature stability at each of the frequency deviation limits was $\pm$ 2.65 ppm. (Ref. para. 3.10 of SCS-483)

There is good reason to expect that the temperature stability of the hybrid version will be better than that of the breadboard. The smaller size of the hybrid module and the tighter thermal homogeneity is expected to contribute to improved performance.

Much of the effort expended in evaluating the resistor functional trim procedure focused on paragraph 6, F/V Linearization, of the VCXO Network Adjustment and Trim Procedure, i.e. on steps 7,8 and 9 of the 12-step trim procedure. Table 2 shows data taken on the breadboard using 10 different crystals. The table shows the impact of changing crystals on the trim values required for resistors R75, R76, R78, R80, R83 and R104. Similar data was recorded for the other steps in the trim procedure, and the trim range requirements deduced for use in hybrid layout design. These requirements are included in tables 4 and 5 which list all resistors in the TCVCXO.

TABLE 2. TCVCXO BREADBOARD RESISTOR TRIM DATA
FOR F/V LINEARIZATION DFG

XTAL #	R76	R104	V @ TP2	FREQ.	R75	R78	V @ TP2	FREQ.	R80	R83	V @ TP2	FREQ.
7	31.23K	500K	1.00V	17,999,088	13.6K	63.3K	3.01V	18,000,088	20K	38K	6.16V	18,001,089
8	31.31K	500K	1.00V	17,999,030	13.6K	63.3K	3.01V	18,000,030	20K	38K	6.15V	18,001,030
9	31.3K	500K	1.00V	17,999,135	13.6K	63.3K	3.02V	18,000,134	20.4K	38K	6.16V	18,001,135
10	31.3K	500K	1.00V	17,999,095	13.6K	63.3K	3.01V	18,000,095	20K	38K	6.16V	18,001,095
19	31.3K	500K	1.00V	17,999,089	13.6K	63.3K	3.01V	18,000,089	20.4K	38K	6.17V	18,001,089
36	31.3K	500K	1.00V	20,998,805	9K	102.6K	2.66V	20,999,805	20K	70K	5.11V	21,000,805
52	31.13K	500K	1.00V	20,998,837	9K	108.7K	2.65V	20,999,837	20K	70K	5.08V	21,000,837
57	31.3K	500K	1.00V	20,998,824	9K	103.3K	2.66V	20,999,824	20K	68K	5.12V	21,000,824
60	31.3K	500K	1.00V	20,998,970	9K	99.5K	2.66V	20,999,970	20K	69.5K	5.13V	21,000,970
63	31.3K	500K	1.00V	20,998,867	9K	97.9K	2.66V	20,999,867	20K	69.4K	5.14V	21,000,867
NOMINALS	20K	500K			9K	63.3K			20K	38K		

6.0 MICROCIRCUIT AND MODULE DESIGN

6.1 Parts and Materials

Based on the electrical schematic included in the ECOM Technical Requirements no. SCS-483 document (see Appendix A), a parts list was generated to the TCVCXO module. The selected parts are as shown in table 3 , broken down by quantity per hybrid microcircuit type or module. Also included in table 3 is a listing of those materials to be used in the assembly, hermetic sealing and encapsulation that have been selected or are yet to be selected. Indicated also is whether each item is made (in-house or outside) or bought or, in the case of the crystals, a government furnished part.

Semiconductor device chips were selected in beam-leaded form, as specified, where such were available. The only beam-leaded devices found to be available were the BD3600B (IN3600 equivalent) diode and the BT2907A (2N2907A equivalent) transistor.

In the selection of ceramic chip capacitors, an attempt was made to use military standard chip sizes wherever possible. Consequently, the CDR01 size (0.080" x 0.050") was selected for all capacitors except C1, C2 and C8. C1 and C2 are high Q porcelain chip capacitors, as specified, whereas C8 is a non-standard size 0.1 uF ceramic chip capacitor (0.125" x 0.095"). A military standard 0.1 uF ceramic chip capacitor comes in a CDR04 size (0.180" x 0.125") size and was determined to be too large for use in the extremely dense VCXO hybrid (see figure 18 below). The 0.01 uF capacitors were found to be available in the small CDR01 size, but from only one vendor in that size. Consequently, that vendor, a QPL vendor, was the selected source for all ceramic chip capacitors.

The assembly, hermetic sealing and encapsulation materials have been discussed already in Section 4.1.

6.2 Hybrid Microcircuit Layout Design

Layout designs for the two types of hybrid microcircuits used in the TCVCXO module have been completed. Figures 17 and 18 are the resultant hybrid assembly drawings. To facilitate comprehension of these designs, several key features will be noted:

TABLE 3. TCVCXO PARTS AND MATERIALS

ITEM	TYPE OR VALUE	M/B	UNIT USAGE		
			VCXO	TC	MODULE
Int. Circuit	uA776	B	3	2	--
Int. Circuit	CD4007AH	B	2	--	--
Diode (Beam Lead)	BD3600B	B	3	7	--
Diode	1N4567A	B	1	--	--
Diode	1N751A	B	1	--	--
Diode	1N754A	B	1	--	--
Diode	1N5468A	B	1	--	--
Transistor (Beam Lead)	BT2907A	B	1	--	--
Transistor	2N2857	B	2	--	--
Capacitor	150 pf	B	2	--	--
Capacitor	100 pf	B	1	--	--
Capacitor	1000 pf	B	1	--	--
Capacitor	4700 pf	B	3	--	--
Capacitor	0.01 uF	B	2	--	--
Capacitor	0.1 uF	B	1	--	--
Potentiometer	25 K	B	--	--	1
Crystal:					
a) in HC-18	--	GFP	--	--	1
b) in Flatpack	--	GFP	1	--	--
Thick Film Substrate	--	M	1	1	--
Epoxy Preform	Ablefilm 550	B	--	--	1
Gold Wire (1-Mil)	--	B	AR	AR	--
Copper Ribbon	--	B	--	--	AR
Gold Ribbon	--	B	--	AR	--
Corral	--	M	1	1	--
Brazing Frame	--	M	1	1	--
Brazing Alloy Preform	--	M	1	1	--
Sealing Glass Preform	--	M	1	1	--
Cover	--	M	1	1	--
Epoxy Encapsulant	--	B	--	--	AR
Potting Shell	--	M	--	--	1

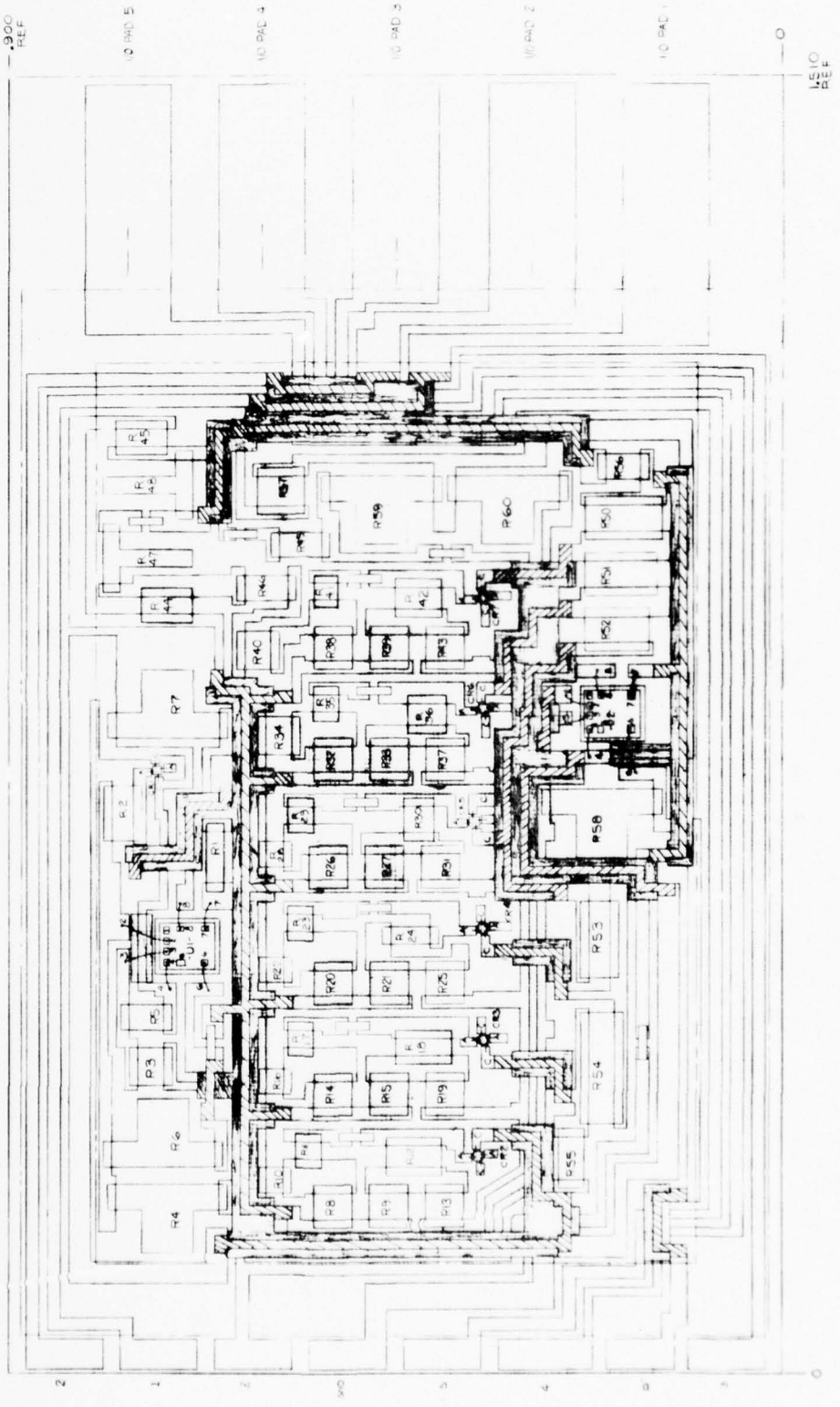


Figure 17. TC Hybrid Assembly

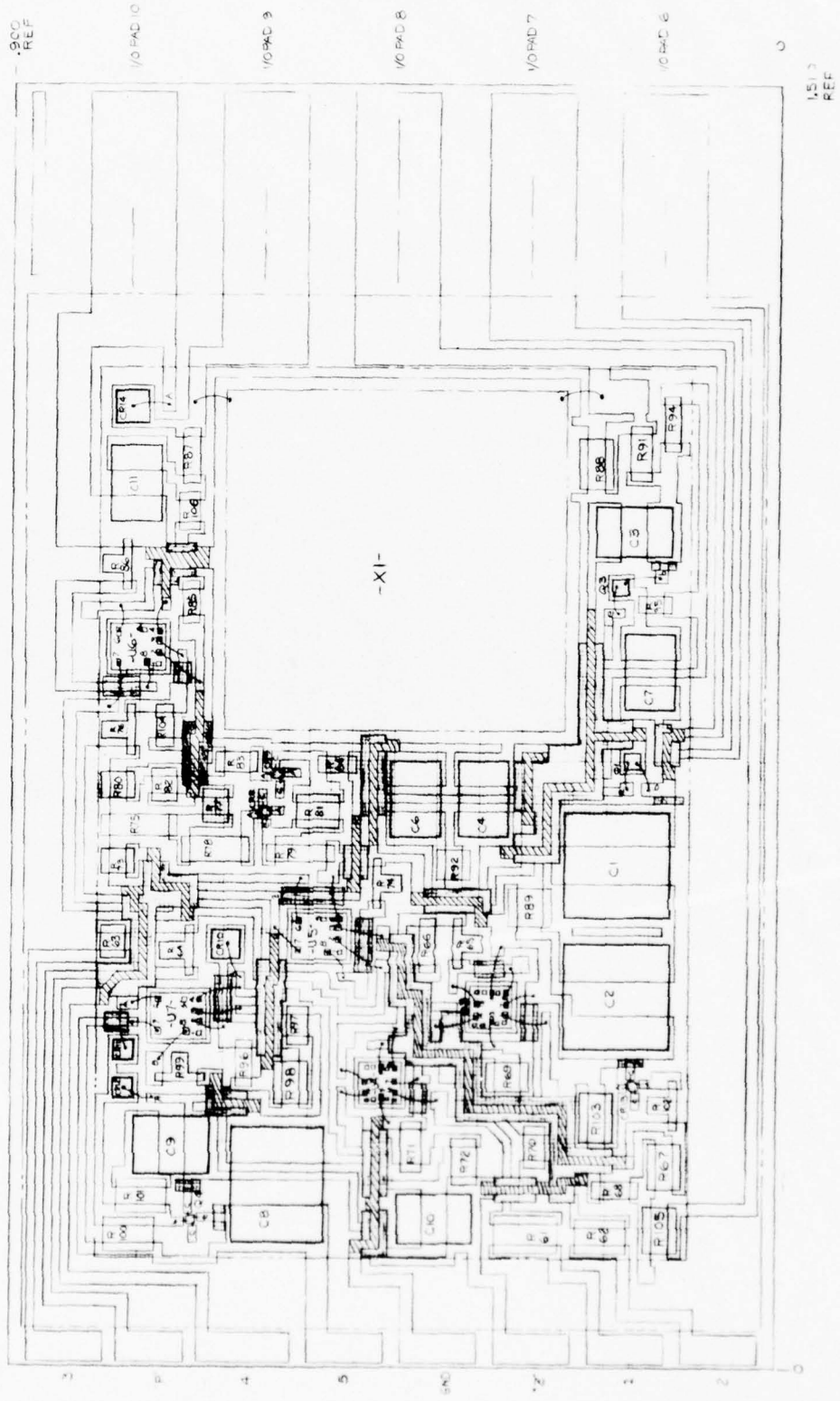


Figure 18. VCXO Hybrid Assembly

a) The wide border (shown by broken lines) surrounding the component area on the substrates is the glass-seal area for the ceramic corral. The seal ring is 0.090" wide.

b) The long conductor "fingers" at one end of each substrate are the input-output pads for the module which mate with an external connector. The short fingers at the opposite end are the termination pads for the interconnections to be made between the two hybrids.

c) Patches of thick film dielectric are used under thick film cross-over conductors (shown cross-hatched) and under wire bonds which cross over thick film conductor runs. In the VCXO hybrid, dielectric patches are also used as solder dams between solder termination pads for capacitors and wire bond pads for active devices.

d) In the TC hybrid design, several ribbon jumpers are shown. They are necessary for two reasons. Both reasons pertain to resistor trimming, one to passive trimming and the other to functional trimming. Although the laser trimming system to be used is generally capable of trimming individual resistors connected in a closed loop, the TC circuit has too complex an array of closed loops inside loops for the system to handle. Therefore, some of these loops have to be temporarily broken to allow for passive trimming of the resistors. The other reason for jumpers is that the functional resistor trim procedure requires that certain electrical connections be temporarily broken to permit injection of test signals or precise measurement of test voltages. All of the jumpers are to be completed by thermocompression gold ribbon bonding.

Tables 4 and 5 list the resistors for the TC hybrid and the VCXO hybrid, respectively. Included for each resistor is the nominal value, the passive trim tolerance and range, the functional trim range, where applicable, and the sheet resistivity of the thick film material to be used in fabrication.

TABLE 4. RESISTOR LIST FOR TC HYBRID

RESISTOR DESIG.	NOMINAL VALUE	TRIM RANGE RESISTANCE MIN.	TRIM RANGE RESISTANCE MAX.	PASTE Ω/□	SEE NOTE	ACTIVE TRIM RANGE	TOL.
R1	90K	85.5K	94.5K	30K			
R2	120K	114K	126K	300K	1	Negligible	5%
R3	200K	190K	210K	300K	1	Negligible	
R4	1M	950K	1050K	300K			
R5	40K	38K	42K	30K	1	40K-48K	
R6	1M	950K	1050K	300K	1	1M -1.3M	
R7	1M	950K	1050K	300K			
R8	20K	19K	21K	30K			
R9	20K	19K	21K	30K			
R10	200K	190K	210K	300K			
R11	20K	19K	21K	30K			
R12	200K	190K	210K	300K			
R13	200K	190K	210K	300K			
R14	20K	19K	21K	30K			
R15	20K	19K	21K	30K			
R16	200K	190K	210K	300K			
R17	20K	19K	21K	30K			
R18	9.4K	8,930	9,870	30K			
R19	200K	190K	210K	300K			
R20	20K	19K	21K	30K			
R21	20K	19K	21K	30K			
R22	200K	190K	210K	300K			
R23	20K	19K	21K	30K			
R24	7.1K	6,745	7,455	3K			
R25	200K	190K	210K	300K			
R26	20K	19K	21K	30K			
R27	20K	19K	21K	30K			
R28	200K	190K	210K	300K			
R29	20K	19K	21K	30K			
R30	2.55K	2,422.5	2677.5	3K			
R31	200K	190K	210K	300K			
R32	20K	19K	21K	30K			
R33	20K	19K	21K	30K			
R34	200K	190K	210K	300K			
R35	20K	19K	21K	30K			
R36	17.6K	16,720	18,480	30K			
R37	200K	190K	210K	300K			
R38	20K	19K	21K	30K			
R39	20K	19K	21K	30K			
R40	200K	190K	210K	300K			
R41	20K	19K	21K	30K			
R42	143K	135,850	150,150	300K			
R43	200K	190K	210K	300K			
R44	10K	9.5K	10.5K	30K			
R45	10K	9.5K	10.5K	30K			

TABLE 4. (CONT'D)

RESISTOR DESIG.	NOMINAL VALUE	TRIM RANGE RESISTANCE MIN	MAX.	PASTE Ω/□	SEE NOTE	ACTIVE TRIM RANGE	TOL.
R46	500K	475K	525K	300K			5%
R47	10K	9.5K	10.5K	3K	1	10K - 50K	
R48	10K	9.5K	10.5K	3K	1		
R49	500K	475K	525K	300K			
R50	10.25K	9,737.5	10,762.5	30K			
R51	1.07K	1,016.5	1,123.5	3K			
R52	1.19K	1,130.5	1,249.5	3K			
R53	849	806.55	891.45	3K			
R54	707	671.65	742.35	3K			
R55	4.73K	4,493.5	4,966.5	3K			
R56	40K	38K	42K	30K	1	Negligible	
R57	20K	19K	21K	30K	1	20K - 40K	
R58	1M	950K	1050K	300K			
R59	1M	950K	1050K	300K			
R60	1M	950K	1050K	300K			

Note 1: Subject to functional trim after initial passive trim to ± 5%

TABLE 5. RESISTOR LIST FOR VCXO HYBRID

RESISTOR DESIG.	NOMINAL VALUE	TRIM RANGE RESISTANCE MIN.	TRIM RANGE RESISTANCE MAX.	PASTE Ω/□	SEE NOTE	ACTIVE TRIM RANGE	TOL.
R61	1K	950	1050	3K			5%
R62	1K	950	1050	3K			5%
R63	200K	192K	208K	300K	1	Negligible	4%
R64	150K	142.5K	157.5K	30K	1	150K-263K	5%
R65	1M	950K	1050K	300K			
R66	680K	646K	714K	300K			
R67	110K	104.5K	115.5K	300K			
R68	51K	48,450	53,550	30K			
R69	28.7K	27,265	30,135	30K	1	28.7K-35.6K	
R70	38.3K	36,385	40,215	30K	1	38.3K-47.5K	
R71	51.1K	48,545	53,655	30K	1	Negligible	
R72	38.3K	36,385	40,215	30K	1	38.3K-71K	5%
R73	200K	198K	202K	300K			1%
R74	1M	950K	1050K	300K			5%
R75	9K	8550	9450	3K	1	9K - 16K	
R76	20K	19K	21K	3K	1	20K- 34K	
R77	200K	190K	210K	300K			
R78	63.3K	60,135	66,465	30K	1	63.3K-111K	
R79	9.2K	8,740	9,660	3K			
R80	20K	19K	21K	30K	1	20K - 23K	
R81	12.4K	11,780	13,020	30K			
R82	200K	190K	210K	300K			
R83	38K	36.1K	39.9K	30K	1	38K - 76K	
R84	39K	37,050	40,950	30K			
R85	500K	475K	525K	300K			
R86	1M	950K	1050K	300K			
R87	68K	64.6K	71.4K	30K			
R88	100K	95K	105K	300K			
R89	2K	1900	2100	3K			
R90	Deleted						
R91	56K	53.2K	58.8K	30K			
R92	1.8K	1710	1890	3K			
R93	Deleted						
R94	68K	64.6K	71.4K	30K			
R95	3.2K	3040	3360	3K			
R96	5.6K	5320	5880	3K			
R97	30K	28.5K	31.5K	30K	1	30K-36K	
R98	12K	11.4K	12.6K	30K	1	12K-14.4K	
R99	1M	950K	1050K	300K			
R100	10K	9.5K	10.5K	30K			
R101	1K	950	1050	3K			
R102	900K	855K	945K	300K			
R103	100K	95K	105K	300K			
R104	500K	475K	525K	300K	1	Negligible	
R105	10K	9.5K	10.5K	30K			
R106	3.3K	3135	3465	3K			5%

NOTE 1: Subject to functional trim after initial passive trim

7.0 CONCLUSION

The major accomplishments to date on this program have been the detailed configuration design of the TCVCXO module, the detailed layout design of the hybrid microcircuitry used in the TCVCXO module, the detailed design of piece-parts to be used in hermetically sealing the hybrid microcircuits and encapsulating the modules, the breadboard analysis of the TCVCXO electrical design, the establishment of process flow plans for producing the modules and the selection and procurement of component parts and materials for the construction of the TCVCXO modules. The results of this work have demonstrated two points worth noting already: (1) that the electrical design is a sophisticated one requiring careful construction and precise trimming to achieve the specified tight performance and (2) that the hybrid microcircuitry is extremely dense and, as such, will be rather difficult to build and may be impossible to repair, considering the array of assembly techniques and the precise functional trimming required.

8.0 PROGRAM FOR NEXT QUARTER

During the next reporting period, work will continue on the development of the hermetic sealing and encapsulating processes, on the establishment of module test procedures and on the fabrication and testing of the first lot of engineering samples of the TCVCXO.

9.0 IDENTIFICATION OF PERSONNEL

The following Raytheon Equipment Development Laboratories professional personnel performed work on this program during the first quarter. The man-hours of work performed by each individual is reported, as is the program contributions and technical background of each.

Charles T. Martin (300 hrs.)

TCVCXO Engineering Phase Project Manager; also prepared engineering phase PERT plan and monthly technical and first quarterly reports

A.B., M.S.E.E., Sr. Engineer and Microcircuit Engineering Section Manager, responsible for applications engineering, design, technology development, prototype development and testing of hybrid microcircuits.

Leland Woodworth (44 hrs.)

Prepared TCVCXO engineering phase monthly cost reports and supervised production control activity for TCVCXO parts and materials procurement

B.S.E.E., Sr. Engineer and Microcircuit Processing Section Manager (and acting Department Administrator), responsible for hybrid microcircuit production and for lab facilities.

James Zaffini (106 hrs.)

Accomplished TCVCXO configuration design, hybrid layout design and detailed design of piece-parts for TCVCXO hermetic sealing and encapsulation

B.S. Ind.Tech., Sr. Engineer, Microcircuit Engineering Section, responsible for hybrid layout design and detailed mecharical design and for assembly process and equipment development.

Stanley Czerepak (128 Hrs.)	Accomplished TCVCXO hybrid layout design and design documentation B.S.E.E., Sr. Engineer, Microcircuit Engineering Section, responsible for hybrid layout, artwork generation and design documentation.
Richard Colson (120 hrs)	Performed TCVCXO breadboard analysis of electrical performance A.B., M.S., Sr. Engineer, Special Projects Section, engaged in analog circuit design for various major system development programs.
Richard Bemis (133 hrs)	Performed TCVCXO breadboard analysis of electrical performance Sr. Engineering Assistant, Special Projects Section, responsible for testing and evaluation of oscillators and crystals.
Charles Morris (80 hrs)	Assisted in TCVCXO breadboard analysis of electrical performance B.S.E.E., Engineer, Microcircuit Engineering Section, responsible for hybrid microcircuit test engineering.

Nicholas Gregory (9 hrs)	Consulted for the TCVCXO breadboard analysis effort
	B.S.E.E., Principal Engineer, Communications Systems Lab, responsible for electrical design of high frequency sources for various programs.

The above listed personnel were assisted by the following support functions at the level of effort indicated:

QC engineering	17 hrs
QC inspection	9 hrs
Electrical technician	24 hrs
Production control	65 hrs
Machine shop	5 hrs
Drafting	17 hrs
Clerical	21 hrs
Supervisory & administrative	10 hrs

Total level of effort for this first quarter was 1088 man-hours.

10.0 REFERENCES

1. S. Schodowski and H. C. Frankel, "Design and Fabrication of a Temperature-Compensated Voltage - Controlled Crystal Oscillator." 1976 Proceeding E COM Hybrid microcircuit symposuim.

APPENDIX A
ELECTRONICS COMMAND
TECHNICAL REQUIREMENTS
SCS-483

ELECTRONICS COMMAND
TECHNICAL REQUIREMENTS

SCS-483
AMENDMENT-3
14 June 1976
SUPERSEDING
AMENDMENT-2
13 January 1976

OSCILLATOR, CRYSTAL, TEMPERATURE COMPENSATED
VOLTAGE CONTROLLED (TCVCXO) 17 MHz to 22 MHz
HERMETIC SEAL

This amendment forms a part of Electronics Command Technical Requirements SCS-483
17 January 1975

Page 1

2.1 Delete title heading "SPECIFICATION" and substitute "SPECIFICATIONS"

Under SPECIFICATIONS delete "SCS-463" and substitute "SCS-512"

Page 2

3.3 Add following sentence to end of paragraph: "Epoxy adhesives shall be permitted for mechanical attachment of IC devices within the hermetic enclosures."

3.5 delete and substitute:

"3.5 Package.- The TCVCXO package shall be in accordance with outline and assembly drawings Figures 3 and 4 respectively."

3.6 delete "SCS-463" and substitute "SCS-512".

3.7 delete and substitute:

"3.7 Seal.- The TCVCXO assembly, without encapsulation, shall be sealed in an atmosphere of dry helium or nitrogen. Maximum leak rate shall be $1X10^{-8}$ atm cc/sec. (See 4.7)."

3.8 delete "20 grams" and substitute "30 grams".

Page 3

3.10 delete "(375/F+3)ppm" and substitute "(325/F+5)ppm".

3.13 delete "6 Hz" and substitute "10 Hz".

3.16 delete "$\pm$ 0.5 ppm" and substitute "$\pm$ 0.25 ppm".

3.17 delete "external to the TCVCXO".

3.18 delete and substitute:

"3.18 Modulation input voltage.- The modulation input voltage shall be defined as follows:

Digital modulation (FSK): SPACE-logic zero, MARK-logic one (5 V positive), CMOS inverter input.

Digital modulation rate: FSK of 1200 data bits per second.

Analog modulation voltage: ± 0.75 V peak max.

Analog modulation rate: DC to 10 kHz max.

Analog transmission control: Analog transmit +5 ± 1 VDC,
Digital transmit 0 to +1 VDC. (see 4.13)."

3.19 delete and substitute:

"3.19 Analog modulation input impedance.- The analog modulation input impedance shall be > 200,000 ohms. (see 4.14)."

3.20 delete and substitute:

"3.20 Frequency deviation.- The FSK frequency deviation from center frequency shall be +300 Hz to +325 Hz for MARK and -300 Hz to -325 Hz for SPACE. Analog frequency deviation sensitivity shall be 500 Hz per volt. (see 4.15)."

3.21 delete and substitute:

"3.21 Analog deviation linearity.- The analog deviation linearity shall be less than 5%. (see 4.16)."

Page 4

3.22 delete and substitute:

"3.22 Supply voltage.- +10 VDC min to +15 VDC max, nominal +12 VDC. (see 4.17)."

3.23 delete and substitute:

"3.23 Input power.- 50 mW maximum. (see 4.18)."

3.24 delete and substitute:

"3.24 Output voltage.- The RF output voltage shall be not less than 0.5 V rms when loaded by 1000 ohms ± 10%. (see 4.19)."

Page 8

Fig 2, delete present Fig 2 and substitute new Fig 2, "REMBASS TCVCXO SCHEMATIC"

Page 9

add Page 9, Fig 3, "TCVCXO MODULE OUTLINE DRAWING"

Page 10

add Page 10, Fig 4, "TCVCXO MODULE ASSEMBLY"

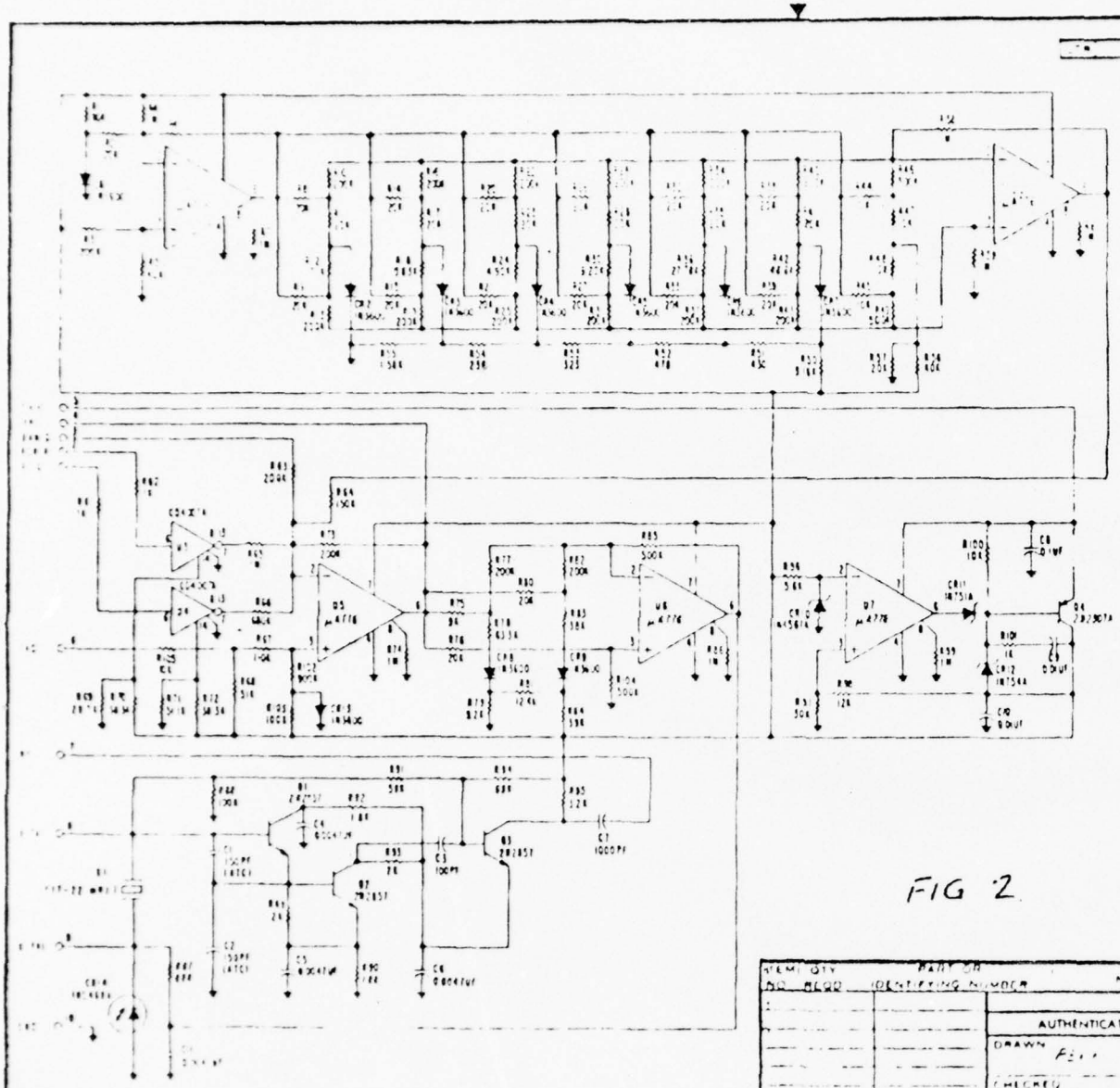


FIG 2

ITEM	QTY	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	SPEC	CAT
NO. REQD					

NEXT ASSY | USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS DECIMALS ANGLES

AUTHENTICATION

DRAWN

CHECKED

VERIFIED

APPROVED

DATE

PARTS LIST

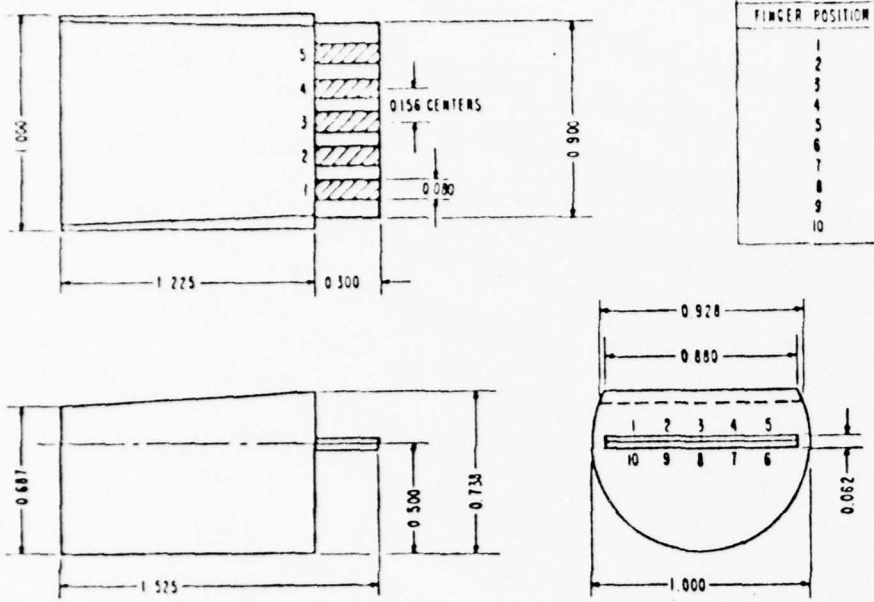
RESEARCH DEVELOPMENT LABORATORIES

REMBASS RCVCAO
SCHEMATIC

SIZE	CODE IDENT NO.	
C	20309	

SCALE — SHEET

ASSIGNMENT-3



CONNECTIONS	
FINGER POSITION	FUNCTION
1	DIGITAL MOD
2	ANALOG CONTROL
3	ANALOG MOD
4	TP1
5	B+ (10-15 VDC)
6	F-ADJUST
7	RF
8	XTAL
9	XTAL
10	GND

REVISIONS			
LTR	DESCRIPTION	DATE	APPRC

FIG. 3.

AMENDMENT-3

ITEM NO	QTY REQD	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS
DECIMALS ±0.003
ANGLES

NEXT ASSY | USED ON
APPLICATION

AUTHENTICATION
DRAWN D. PERKINS
CHECKED
VERIFIED
APPROVED JRC
DATE 16 OCT 75

U. S. ARMY ELECTRONICS COMMAND
R&D DIRECTORATE AND LABORATORIES
FORT MONMOUTH, NEW JERSEY 07703

TCVCXO MODULE
OUTLINE DRAWING

SIZE B | CODE IDENT NO 20309 | ES-B-21277

SCALE | SHEET

WHEN REFERRING TO THIS DRAWING STATE DRAWING NO., APPLICABLE ISSUE, LETTER IF ANY

REVISIONS			
LTR	DESCRIPTION	DATE	APPD

SCD-103
AMENDMENT-3

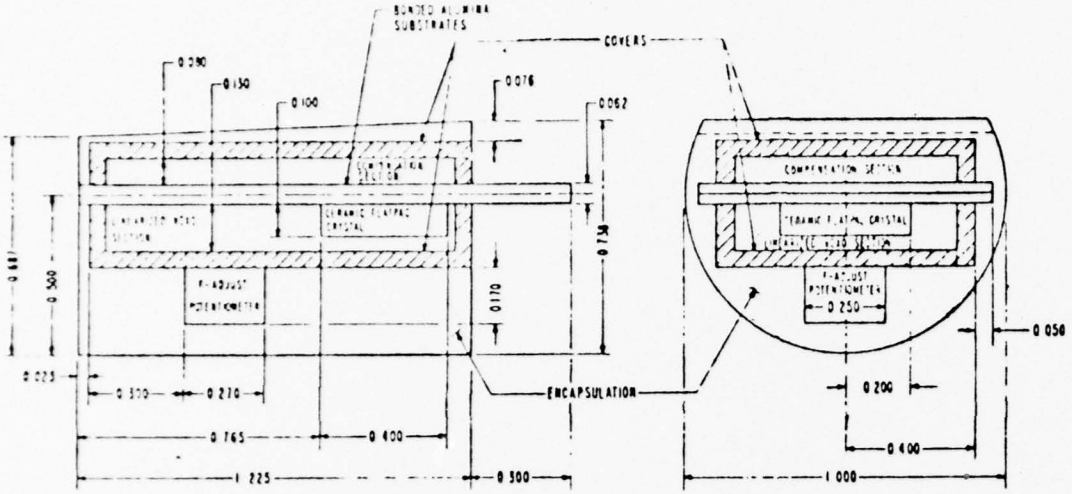


FIG. 4.

ITEM NO.	QTY REQD	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	SPECIFICATION
			PARTS LIST	

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS DECIMALS ANGLES
±0.005

AUTHENTICATION	
DRAWN	D PERKINS
CHECKED	
VERIFIED	
APPROVED	JRC
DATE	18 OCT 75

US ARMY ELECTRONICS COMMAND
RESEARCH AND DEVELOPMENT LABORATORIES
FORT MONMOUTH, NEW JERSEY

TCVCXO MODULE ASSEMBLY

SIZE	CODE IDENT NO.	
C	20309	ES-C-212775

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OSCILLATOR, CRYSTAL, TEMPERATURE COMPENSATED VOLTAGE CONTROLLED (TCVCXO) 17MHz to 22 MHz HERMETIC SEAL

1. SCOPE

1.1 Scope.- This specification covers the detailed requirements for a ± 5 ppm overall frequency tolerance temperature compensated voltage controlled crystal oscillator (TCVCXO).

2. APPLICABLE DOCUMENTS

2.1 The following documents of the issue in effect on the date of invitation for bid, forms a part of this specification to the extent specified herein.

SPECIFICATION

MIL-M-38510	Microcircuits, General Specification.
MIL-O-55310	Oscillators, Crystal, General Specification For.
SCS-463	Shock Resistant Crystal Units.

STANDARDS

MIL-STD-202	Test Methods for Electronic and Electrical Component Parts.
MIL-STD-883	Test Methods and Procedures for Microelectronics.

(Copies of specifications required by contractors in connection with specific procurement functions may be obtained from or as directed by the contracting officer. Both titles and identifying number or symbol should be stipulated when requesting copies.)

3. REQUIREMENTS

3.1 General.- The complete requirements for the crystal oscillator described herein shall consist of this document and the latest issue of specification MIL-O-55310.

3.2 Electrical.- The TCVCXO shall be consistent with the functional block diagram and schematics, Figure 1 and 2 respectively. The TCVCXO shall operate at antiresonance and not include inductors. Linearization of the VCXO frequency-voltage tuning characteristic shall be obtained by means of a diode function generator (DFG) which produces a piecewise linear approximation of the linearizing voltage transfer function. Frequency-temperature (F-T) compensation shall be obtained with a similar DFG which generates a cubic transfer function approximating the characteristic of the uncompensated VCXO. The compensating DFG shall also incorporate a capability for rotating the DFG cubic transfer characteristic to correct for deviation of the crystal unit F-T characteristic from the design center curve. Provision (not included in Figure 2) shall also be made for adjusting the compensating characteristic to accommodate the range of frequencies given in 3.9.

3.3 Microcircuit Design and Construction.- Microcircuit design and construction shall be in accordance with paragraph 3.5 of MIL-M-38510 and specified herein. Thick film hybrid circuitry shall be employed. The number of bonded interconnections shall be minimized by employing multiple layer conductors with dielectric crossovers. Leads and bonds shall be confined to interconnections with the semiconductor devices. Beam leaded devices shall be used wherever possible. Maximum length of intercornecting leads shall be 0.050 inches and leads shall not cross over uninsulated conductors.

3.4 Film Resistor Trimming.- Passive and active resistor trimming shall be accomplished using a resistance laser trim system.

3.5 Package.- The package shall be a multiple pin enclosure having a volume not exceeding 0.45 cubic inches (TEKFORM, FSCM 29172, Parts #20269 and #20270 or equivalent).

3.6 Quartz Crystal.- Quartz crystal unit CR-(XM-159)/U in accordance with SCS-463 shall be employed in the TCVCXO.

3.7 Seal.- The TCVCXO shall be sealed in an atmosphere of dry helium or nitrogen. Maximum leak rate shall be $1X10^{-8}$ atm cc/sec. (See 4.7).

3.8 Weight.- The maximum weight shall be 20 grams. (See 4.3).

3.9 Frequency Range.- The frequency range of the TCVCXO shall be 17 MHz to 22 MHz. (See 4.3).

3.10 Frequency-Temperature Stability.- The frequency change of the TCVCXO shall not exceed ± 2 ppm over the range of -40°C to ± 75°C at center frequency and at frequency deviation limits of ± (375/F +3) ppm where F is the nominal frequency in MHz. (See 4.8).

3.11 Frequency-Voltage Stability.- The frequency change for a power supply variation given in 3.22 shall not exceed ± 0.25 ppm. (See 4.3).

3.12 Frequency-Load Stability.- The frequency change for an output termination resistance change of ± 20% shall not exceed ± 0.25 ppm. (See 4.3).

3.13 Transient Frequency Stability (initial turn on).- The transient frequency shift between the first 5 msec to 100 msec following application of power shall be less than 6 Hz. (See 4.3).

3.14 Aging.- The frequency aging at 60°C ± 0.1°C shall not exceed $1X10^{-8}$ over any one week interval following a 14 day stabilization period at 60°C. (See 4.9).

3.15 Shock.- The frequency change following a 1000g, 6 millisecond shock shall be less than ± 0.5 ppm. (See 4.10).

3.16 Vibration.- The difference between TCVCXO frequency measured before and after vibration at 0.06" double amplitude, 10 to 70 Hz and at constant 15g from 70 Hz to 2000 Hz shall be less than ± 0.5 ppm. (See 4.11).

3.17 Frequency Adjustment.- Frequency adjustment shall be accomplished external to the TCVCXO by means of a 25K ohm potentiometer. The minimum frequency adjustment range shall be ± 5 ppm of the nominal frequency. (See 4.12).

3.18 Modulation Input Voltage.- The magnitude of the applied modulation voltage shall be 1.5V ± 0.01V peak to peak for a 300 bit per second square wave (FSK) or 1.5V ± 0.01V peak to peak (DC to 2000 Hz) sine wave (analog). The dc level is 0.0V ± 0.01V. (See 4.13).

3.19 Modulation Input Impedance.- The modulation input impedance shall be 20K ohms ± 10%. (See 4.14).

3.20 Frequency Deviation.- The modulation deviation of the TCVCXO corresponding to the peak to peak modulation input voltages of 3.18 shall be ± 375 Hz ± 5% of center frequency. (See 4.15).

3.21 Deviation Linearity.- The deviation linearity of the TCVCXO shall be less than 1%. (See 4.16).

3.22 Supply Voltages.- + 9V ± 0.01V dc, -9V ± 0.01V dc. (See 4.17).

3.23 Input Power.- 85mW maximum. (See 4.18).

3.24 Output Voltage.- The RF output voltage shall be not less than 80mV rms when loaded by 50 ohm ± 10%. (See 4.19).

3.25 Marking.- The TCVCXO shall be marked with index point, serial number, manufacturers code designation, week and year of manufacture and calibration ΔF offset at 30° ± 1°C as a minimum. (See 4.20).

4. QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for inspection.- The contractor is responsible for the performance of all inspections specified herein. The contractor may utilize his own facilities or any commercial laboratory acceptable to the Government. Inspection records of the examinations and tests shall be kept complete and available to the Government as specified in the contract.

4.2 Classification of inspection.- Inspection shall be classified as follows:

(a) First article inspection (does not include preparation for delivery). (See 4.4).

(b) Quality conformance inspection. (See 4.5).

4.3 Test plan.- The contractor prepared Government-approved test plan as cited in the contract shall contain:

(a) Time schedule and sequence of examinations and tests.

(b) A description of the method of test and procedures.

(c) Programs of any automatic tests including flow charts and block diagrams.

(d) Identification and brief description of each inspection instrument with date of most recent calibration.

4.4 First article inspection.- This inspection shall consist of all the tests contained in Table II of MIL-O-55310 and as specified below. No failures shall be permitted.

4.5 Quality conformance inspection.- This inspection shall be performed on samples selected from the pilot production as specified in the bid request and contract. Quality conformance inspection shall be conducted in accordance with Paragraph 4.7 of MIL-O-55310 and as specified below.

4.6 Screening.- Prior to first article and quality conformance inspection, each TCVCXO shall have been screened according to method 5004.1, "Screening Procedures", Class B, MIL-STD-883 except for 3.1.5 mechanical shock, 3.1.6 constant acceleration and 3.1.7 seal. Qualification or quality conformance inspection, 3.1.14 of the screening tests, shall be limited to the high temperature storage test, Group C, subgroup 4 of method 5005.1.

4.7 Seal.- The TCVCXO shall be tested in accordance with Test Condition C, Procedure IV, Method 112A of MIL-STD-202D.

4.8 Frequency-Temperature Stability.- The TCVCXO shall be tested in accordance with 4.8.8.1 of MIL-O-55310.

4.9 Aging.- The aging shall be tested in accordance with 4.8.29 of MIL-O-55310. Continuous measurement period 8 weeks; measurement interval 24 hrs.

4.10 Shock.- Shock performance shall be tested in accordance with Condition E, Method 213A of MIL-STD-202D except shock duration shall be 6 milliseconds.

4.11 Vibration.- Vibration performance shall be tested in accordance with Condition B, Method 204B of MIL-STD-202D.

4.12 Frequency Adjustment.- The frequency adjustment range shall be tested in accordance with 4.8.9 of MIL-O-55310.

4.13 Modulation Input Voltage.- The modulation input voltage shall be tested in accordance with 4.8.4.3 of MIL-O-55310.

4.14 Modulation Input Impedance.- The modulation input impedance shall be tested in accordance with 4.8.5 of MIL-O-55310.

4.15 Frequency Deviation.- The frequency deviation shall be tested in accordance with 4.8.25 of MIL-O-55310.

4.16 Deviation Linearity.- The deviation linearity shall be tested in accordance with 4.8.27 of MIL-O-55310.

4.17 Supply Voltage.- The supply voltage shall be tested in accordance with 4.8.4.1 of MIL-O-55310.

4.18 Input Power.- The input power shall be tested in accordance with 4.8.6.1 of MIL-O-55310.

4.19 Output Voltage.- The output voltage shall be tested in accordance with 4.8.12.1 of MIL-O-55310.

4.20 Marking.- Marking shall be in accordance with 3.8 of MIL-O-55310.

5. PREPARATION FOR DELIVERY

5.1 Preparation for Delivery.- Preparation for delivery shall be as specified in the contract.

6. NOTES

6.1 Overall Frequency Tolerance.- The intended application for this device requires that the frequency remain within ± 5 ppm from nominal frequency under any combination of environment and input voltage conditions contained herein and over a period of 1 year following initial calibration.

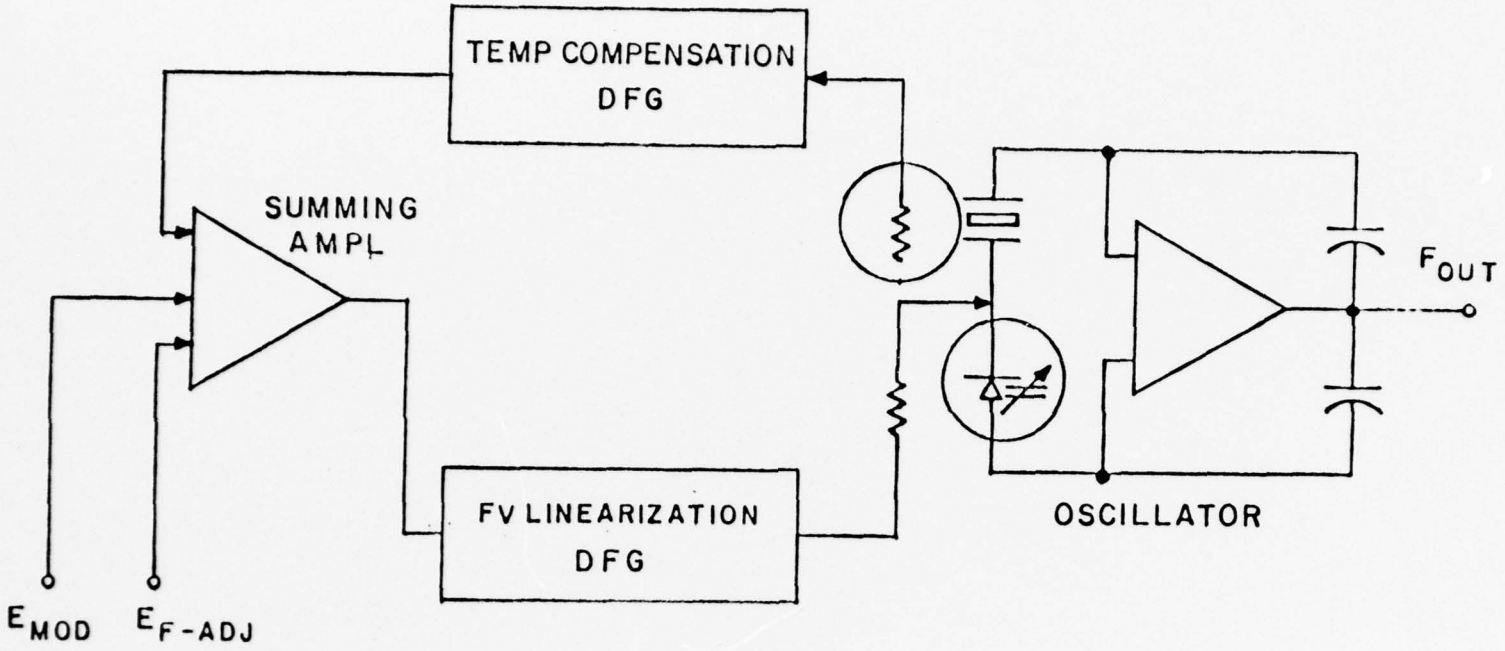


FIG i TCVCXO BLOCK DIAGRAM

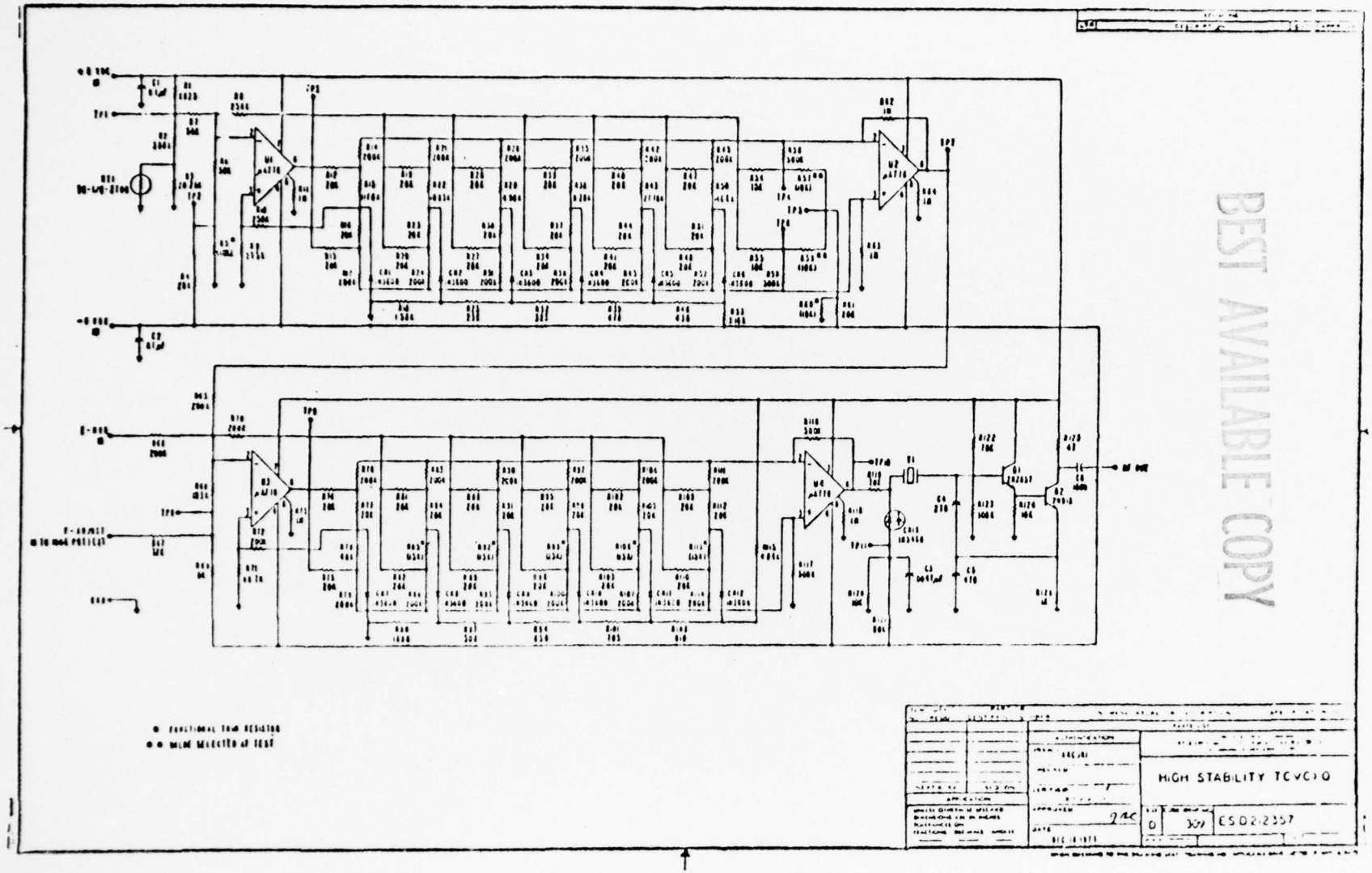


FIG 2 TCVCXO SCHEMATIC

APPENDIX B
TCVCXO NETWORK ADJUSTMENT
AND RESISTOR TRIM PROCEDURE

VCXO NETWORK ADJUSTMENT AND TRIM PROCEDURE

1. 9 V REGULATOR

OBJECT: Adjust regulator output to 9.000 V ±0.002 V

CONDITIONS: a. 12 V power supply across 12 V interconnect and ground.
b. DVM across 9 V interconnect and ground.

TRIM PROCEDURE: If DVM <8.998 V, trim R98
If DVM >9.002 V, trim R97

2. DIGITAL DEVIATION

OBJECT: Adjust U4 voltage level such that TPI difference voltage, corresponding to logic 0 and 1 inputs at the E_{DIG} interconnect equals 1.250 V ±0.002 V

CONDITIONS: a. 12 V power supply across 12 V interconnect and ground
b. DVM across TPI interconnect and ground
c. 25 kΩ potentiometer across Fadj (Pin 6) and ground
d. 3.5 V across E_{COMP} interconnect and ground
e. $E_{CNTRL} = E_{ANLG} = 0$ V (interconnects at ground potential.
f. $E_{DIG} = 5$ V

TRIM PROCEDURE: Set TPI = 4.000 V ±0.001 V using 25 kΩ pot.
Make $E_{DIG} = 0$ V (ground potential).
If DVM <2.749 trim R72
If DVM >2.751 trim R71

3. ANALOG CENTER FREQUENCY

OBJECT: Adjust U3 voltage level such that TPI difference voltage, corresponding to logic 0 and 1 inputs at the E_{CNTRL} interconnect, equals 0.625 ±0.002 V.

CONDITIONS: a. 12 V power supply across 12 V interconnect and ground.
b. DVM across TPI interconnect and ground.
c. 25 kΩ potentiometer across Fadj (Pin 6) and ground.
d. 3.5 V across E_{COMP} interconnect and ground.
e. $E_{ANLG} = E_{DIG} = 0$ V (ground potential).
f. $E_{CNTRL} = 5$ V

TRIM PROCEDURE: Set TPI = 4.125 V ±0.001 using 25 kΩ pot.
Make $E_{CNTRL} = 0$ V (ground potential).
If DVM <3.499 V, trim R70
If DVM >3.501 V, trim R69

4. ANALOG DEVIATION

OBJECT: Adjust R63 summing resistor such that analog voltage gain at U5 equals 1.0 ±5%.

CONDITIONS:
a. 12 V power supply across 12 V interconnect and ground.
b. DVM (AC/DC) across TPI interconnect and ground.
c. 25 kΩ potentiometer across Fadj (Pin 6) and ground.
d. 3.5 V across E_{COMP} interconnect and ground.
e. E_{CNTRL} = 5 V.
f. $E_{ANLG} = E_{DIG}$ = 0 V (ground potential).

TRIM PROCEDURE: Set TPI = 3.5 V d.c. using 25 kΩ pot.
Inject 1 V ±0.02 V rms 1 kHz signal across E_{ANLG} interconnect and ground.
Trim R63 to get 1 V ±0.02 V rms at TPI.

5. COMPENSATION GAIN

OBJECT: Adjust R64 summing resistor such that temperature compensation voltage gain at U5 equals Fx/Fs volts, where Fx is the nominal frequency of the assigned crystal and Fs is the nominal frequency of the crystal from which the standard cubic correction function was derived. Fs = 20.50 MHz for compensation DFG resistor values in TCVCXO Schematic ES-C-215261.

CONDITIONS:
a. 12 V power supply across 12 V interconnect and ground.
b. DVM (AC/DC) across TPI interconnect and ground.
c. 25 kΩ potentiometer across Fadj (Pin 6) and ground.
d. E_{CNTRL}=5 V.
e. $E_{DIG} = E_{ANLG}$ = 0 V (ground potential)
f. E_{COMP} = 3.5 V d.c.

TRIM PROCEDURE: Set TPI = 3.5 V d.c. using 25 kΩ pot.
Inject 1 V ±0.02 V rms 1 kHz signal at E_{COMP} (audio generator in series with 3.5 V supply).
Trim R64 to get $\frac{Fx}{Fs}$ V ±0.02 V rms at TPI.

6. F/V LINEARIZATION

OBJECT: Adjust linearization DFG segment gains to linearize VCXO frequency/voltage tuning characteristic for a slope of 500 Hz/V.

CONDITIONS:
a. 12 V power supply across 12 V interconnect and ground.
b. 25 kΩ potentiometer across Fadj (Pin 6) and ground.
c. 1 kΩ load and frequency counter across RF (Pin 7) and ground.
d. Crystal connected across Pin 8 and 9.
e. DVM at E_0 (term. 6, U6) and at TPI

TRIM PROCEDURE:

Set TPI = 1.5 V ±0.001 V using 25 kΩ pot.
If E_0 >1.001 Trim R76
If E_0 <0.999 Trim R104
At E_0 = 1.000 V ±0.001 V, record freq. (F_{REF})
Set TPI = 3.5 V ±0.001 V using 25 kΩ pot. Note frequency (F_1)
If (F_1-F_{REF}) >1002 Hz, trim R78
If (F_1-F_{REF}) <998 Hz, trim R75
(F_1-F_{REF}) should equal 1000 Hz ±2 Hz
Set TPI = 5.5 V ±0.001 V using 25 kΩ pot. Note frequency (F_2)
If (F_2-F_{REF}) >2002 Hz, trim R83
If (F_2-F_{REF}) <1998 Hz, trim R80
(F_2-F_{REF}) should equal 2000 Hz ±2 Hz

COMPENSATION NETWORK ADJUSTMENT AND TRIM PROCEDURE

1. THERMOMETER GAIN

OBJECT: Adjust R2 or R6 summing resistors such that the gain for the voltage across CRI equals 8.5 ±5%.

CONDITIONS:
a. Regulated 9 V ±0.001 V across 9V interconnect and ground.
b. DVM (ac) at E_1 (term 6, U1) and across CRI.
c. Audio signal generator in series with 5 kΩ resistor across CRI.

TRIM PROCEDURE: Set level of 1 kHz signal at Node CR1, R1, R2 to 0.1 V ±0.002 V rms
If E_1 >0.852 V rms, trim R2
If E_1 <0.848 V rms, trim R6

2. THERMOMETER REFERENCE

OBJECT: Adjust R3 or R5 divider resistors such that E_1 (term 6, U1) equals 4.120 V ±0.005 V d.c. at 26°C. To correct for temperature difference between actual microcircuit temperature and 26°C use the formula $E_1 = 4.120 + 0.018\ (TA-26^{\circ}C)$ where TA is measured temperature of the microcircuit and 0.018 is the thermometer sensitivity in V/°C.

CONDITIONS:
a. Regulated 9 V ±0.001 V across 9 V interconnect and ground.
b. DVM (dc) at E_1 (term 6, U1)

TRIM PROCEDURE: If DVM >(E_1 corrected +0.005 V), trim R3
If DVM <(E_1 corrected -0.005 V), trim R5

3. COMPENSATION DFG CURVE ROTATION

OBJECT: Adjust R56, R57 divider resistors to set voltage across R57 equal to 4.120 V such that the standard (design center) correction curve may be linearly rotated at the 26°C reference temperature.

CONDITIONS:
a. Regulated 9 V ±0.001 V across 9 V interconnect and ground.
b. Branches containing R47 and R48 are open.
c. DVM across R57

TRIM PROCEDURE: If DVM >4.122 V, trim R56.
If DVM <4.118 V, trim R57.

4. COMPENSATING CURVE SELECTION

OBJECT: Select a compensating curve (described by a set of R47 and R48 values) from a family of rotated curves, by matching the frequency difference between upper and lower turning points (UTP-LTP) obtained from a corrected·

F/T curve of the assigned crystal unit.

CONDITION: a. F/T curve for crystal unit obtained in test set with crystal load capacitance at 20 pF.
b. Available family of F/T curves previously generated by rotation of the standard curve (R47 = R48 = 10 K) using various combinations of R47 and R48 with crystal oscillator maintained at constant room temperature.

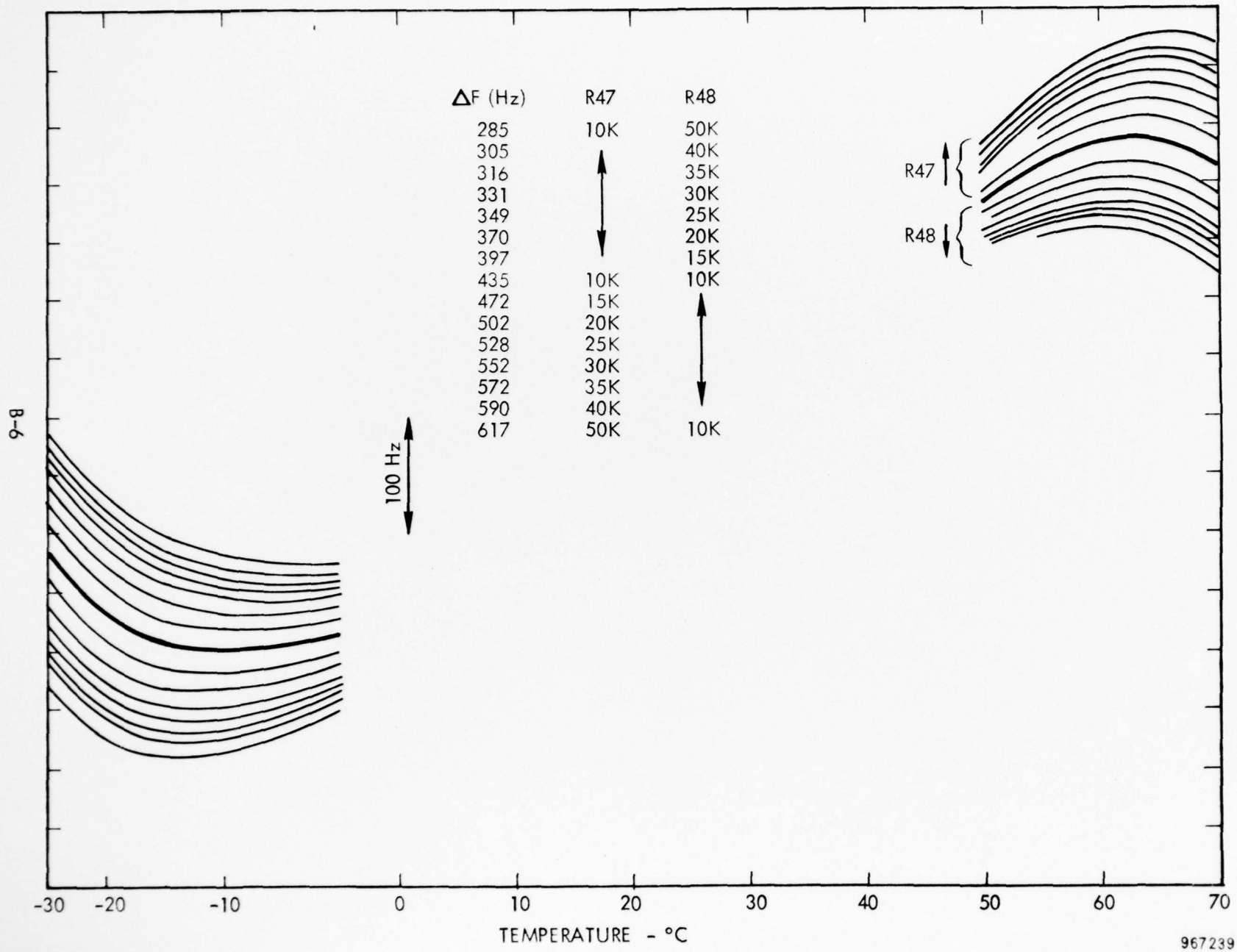
PROCEDURE: Correct for circuit F/T contribution by adding 3 ppm to crystal F/T curve (UTP-LTP) difference. (A near linear repeatable clockwise rotation of the crystal F/T characteristic is produced by the positive TC of the crystal load capacitance). Select a curve (set of R47 and R48 values) which will provide a frequency change equal to the corrected crystal F/T curve (UTP-LTP) difference.

5. COMPENSATING CURVE ADJUSTMENT.

OBJECT: Adjust R47 or R48 such as to provide the required rotated compensating F/T curve.

CONDITIONS: a. DVM (ohms) or resistance bridge across R47 or R48.
b. Branches containing R47 and R48 are open.

TRIM PROCEDURE: Perform passive trim of R47 or R48 to within ±5% of values determined in Step 4, "COMPENSATION CURVE SELECTION". As a final step, close branches containing R47 and R48.


ΔF (Hz)
R47
R48
285 10K 50K
305 40K
316 35K
331 30K
349 25K
370 20K
397 15K
435 10K 10K
472 15K
502 20K
528 25K
552 30K
572 35K
590 40K
617 50K 10K
R47
R48
100 Hz
-30 -20 -10 0 10 20 30 40 50 60 70
TEMPERATURE - °C
967239

CHANGES TO COMPENSATION NETWORK ADJUST AND TRIM PROCEDURE FOR LOW CURRENT DIVIDER CIRCUIT

1. THERMOMETER GAIN. Change gain from 8.5 ±5% to 10 ±5%. Change trim procedure to read:

If E_1>1.002 V rms, trim R2.
If E_1 <0.998 V rms, trim R6

2. THERMOMETER REFERENCE. Change reference voltage E_1 from 4.120 V ±0.005 V at 26°C to 4.355 V ±0.005 V at 26.2°C. Change formula for corrected E_1 from 4.120 V + 0.018 (TA-26°C) to E_1 = 4.355 V + 0.021 (TA-26.2°C)

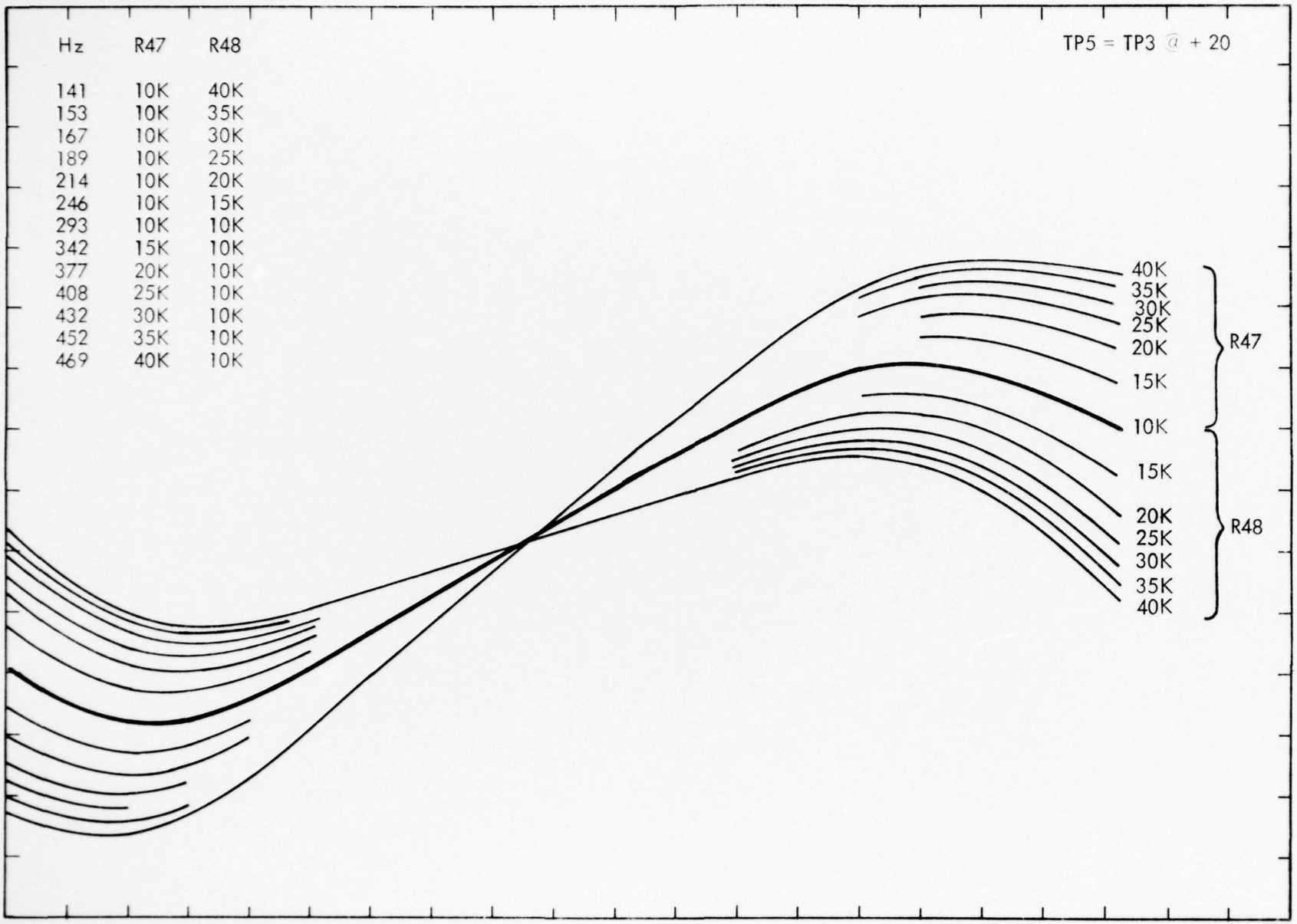
3. COMPENSATION DFG CURVE ROTATION. Change R57 voltage set from 4.120 V to 4.355 V, change trim procedure to read.

If DVM >4.357 V, trim R56
If DVM <4.353 V, trim R57

CHANGES TO VCXO NETWORK ADJUSTMENT AND TRIM PROCEDURE FOR LOW CURRENT DIVIDER CIRCUIT

1. COMPENSATION GAIN: Change F_s from 20.50 MHz to 19.88 MHz.

DIVIDER (LOW CURRENT)



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