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APR 77 J MCGARRY, V WEISSFLUG, E SISUL DAAH01-74-C-0928
UNCLASSIFIED MDC-E1601 NL

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REPORT MDC E1601

STORAGE RELIABILITY OF MISSILE MATERIEL

FINAL REPORT

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Prepared for
U.S. ARMY MISSILE R & D COMMAND
REDSTONE ARSENAL

MCDONNELL DOUGLAS ASTRONAUTICS COMPANY - EAST

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

Samples of 200 each of 21 different parts, planned for use in the PATRIOT missile system, were subjected to a comprehensive test program to determine their storage reliability potential. The test parts included beam lead and chip and wire integrated circuits, transistors, diodes, resistors, capacitors, inductors, and a ceramic substrate. The objectives of the program were:

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1. To generate and execute designed experiment test plans for accelerating the failure mechanisms and inducing failures relating to non-operating and storage conditions for the selected items of microelectronic and semi-conductor hardware.

2. To analyze the data obtained from accelerated testing of the selected items, using such techniques (but not limited to) as the Arrhenius model and regression analysis to generate meaningful predictions of failure rates (MTBF) for the devices under actual storage conditions.

3. To determine by use of Analysis of Variance Techniques (or other suitable techniques) the relative effects of quantitative and qualitative variables on the reliability of the tested material when subjected to long non-operating periods.

The report documents the testing approach used; detailed test results on each part type; detailed analysis of the test data; failure analysis results of failed parts, including failure modes, failure mechanisms, and cause of failure. High temperature and applied electrical bias were employed as accelerating factors in the testing, and both the Arrhenius and Eyring reaction rate models were employed in analysis of the data.

Conclusions and recommendations relative to the storage reliability potential of each part type tested in the program are derived and documented.

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29 APRIL 1977 **REPORT MDC E1601**

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Prepared for

U.S. ARMY MISSILE R & D COMMAND
REDSTONE ARSENAL, ALABAMA 35812
Under Contract No. DAAHO1-74-C-0928

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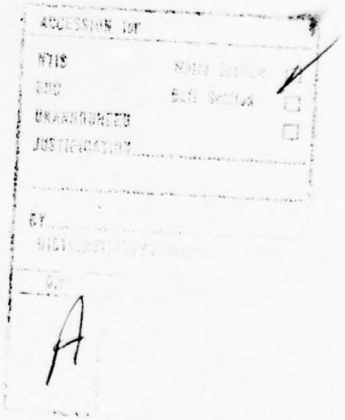
PREFACE

The work described in this report was performed by the Parts Application Engineering section of the McDonnell Douglas Astronautics Company-East (MDAC-EAST) Engineering Reliability Department during the period between June 1974 and April 1977. The work was initiated for the U.S. Army Missile Command (MICOM) under Contract Number DAAH01-74-C-0928. Subsequent reorganization at MICOM resulted in a name change to U.S. Army Missile Research and Development Command (MIRADCOM). Messrs. Maury Bahan and Les Conger of MIRADCOM's Product Assurance Directorate provided contract coordination and technical direction and were instrumental in solving many of the problems associated with a program of this scope. To them a special thanks is extended. The MDAC-EAST Program Manager was Jim McGarry with full time assistance from Mr. Van Weissflug, who deserves special recognition as the man most responsible for making everything happen. In addition to the many MDAC-EAST personnel who contributed to the program, particular thanks is extended to Mr. Ed Sisul for his analysis of failed parts, Mr. Bob Watson for his assistance in electrical testing, Mr. Larry Conaway for his laboratory assistance, Mr. Bruce Kirk for his assistance in data analysis, and finally to Messrs. Mort Stitch, Ron Mackin, and Gordon Johnson for their many contributions to the overall program.



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1.0 INTRODUCTION

Material in the Army inventory, particularly missile systems, must withstand long periods of storage and "launch ready" non-activated dormancy. Within the Department of Defense, the U.S. Army Missile Research and Development (MIRADCOM) (formerly MICOM), Redstone Arsenal, Alabama, has lead responsibility for developing the data bank and supporting methodology required to design, manufacture, and package hardware for this non-operating environment. One facet of this comprehensive program is to conduct accelerated life tests on selected SAM-D (now "Patriot") missile parts to provide a "before the fact" indication of storage reliability potential. In June 1974, MICOM contracted with McDonnell Douglas Astronautics Company-East (MDAC-EAST) to conduct accelerated life tests on twenty-one part types, including both "active" parts (integrated circuits, transistors, and diodes) and passive parts (resistors, capacitors, and inductors). The objectives of the program are as follows:

- To generate and execute designed experiment test plans for accelerating the failure mechanisms and inducing failures relating to non-operating and storage conditions for selected items of microelectronic and semiconductor hardware.
- To analyze the data obtained from accelerated testing of the selected items, using such techniques (but not limited to) as the Arrhenius model and regression analysis to generate meaningful predictions of failure rates (MTBF) for the devices under actual storage conditions.
- To determine by use of Analysis of Variance Techniques (or other suitable techniques) the relative effects of quantitative and qualitative variables on the reliability of the tested material when subjected to long non-operating periods.

MDAC-EAST has drawn upon its past experience in conducting High Temperature Operating Tests (HTOT) to design an accelerated life test program meeting MICOM's objectives. The traditional approach to storage reliability evaluations, long term non-operating high temperature tests, has been selectively supplemented with voltage tests to provide an added accelerator for the generation of storage related failure mechanisms. The rationale and results of this technical approach are presented in this report.

2.0 TEST CRITERIA

Previous storage reliability evaluations have included "real time" investigations in an actual storage environment, and non-operating accelerated tests with temperature as the accelerating stress. A "real time" storage program under actual storage conditions offers the ultimate in providing applicable data. Unfortunately, it is an "after the fact" type program and the data obtained is a measure of how a system or equipment is currently performing with little or no capability to project its continuing performance. At the completion of such a program, the data obtained is applicable to parts which may be obsolete for new design, a situation especially applicable to the constantly changing semiconductor industry. An alternative is to devise accelerated tests that not only identify storage capability in a reasonable time period but also provide the information during the equipment design phase, where the data can be most advantageously utilized. Unfortunately, temperature alone is not always an adequate accelerator for electronic parts, especially microcircuits. The combined use of an applied bias and high temperature has been observed[1] to induce failures where temperature only has not been effective. In addition, the number of failures induced appeared to be sensitive to the magnitude of the applied voltage, suggesting an Eyring relationship.

Reference [2] reports the results of a NASA sponsored study investigating the applicability of an Eyring reaction rate model [3], which includes both temperature and a non-thermal stress factor, to describe microcircuit aging characteristics. The Eyring reaction rate model, which would allow the calculation of a median lifetime as the applied voltage (the non-thermal stress factor) approached zero (a storage condition), can be expressed as:

$$t_{50\%} = \frac{Gh}{kT} \exp\{\frac{E_{TA}}{kT} - f(V)\ [C + \frac{D}{kT}]\}$$

where:

$t_{50\%}$ = device median life
G, C, and D are positive constants
E_{TA} = activation energy in electron volts
f(V) = some function of bias voltage
k = Boltzman's constant = 8.617×10^{-5} eV/K
h = Planck's constant = 1.149×10^{-18} eV hr
T = absolute junction temperature (K)

Although the data [2] was insufficient for a rigorous evaluation of an Eyring model, the results did suggest the model's applicability. Therefore in this storage reliability test program, an applied voltage was utilized as an added accelerator when temperature alone was considered inadequate. Details of the individual life test configurations are provided in the Appendices.

Seven integrated circuits were included in the accelerated life test program. All were subjected to combinations of voltage (including zero volts) and temperature during the life tests. Without the presence of voltage as an added accelerating stress, none of the seven integrated circuits would have produced sufficient failures for analysis. Even with the added voltage stress, four integrated circuits still produced too few failures for analysis purposes.

The applicability of voltage/temperature induced failure mechanisms are assessed in each individual case in the Appendices. Regardless of the applicability or non-applicability of the failure mechanism to a storage environment, the occurrence of voltage induced failures allows the calculation of a "no worse than" failure rate for a storage environment. This is a preferred alternative to a non-operating accelerated life test which may produce too few failures for analysis.

3.0 PROGRAM DESCRIPTION

Twenty-one parts, Figure 3-1, used or planned for use in the SAM-D missile, were provided as Government Furnished Equipment, GFE, for the test program. Included were integrated circuits, transistors, diodes, resistors, capacitors, inductors, and a ceramic substrate. The test parts were actually procured by the Raytheon Missile Systems Division under a separate MICOM contract, screened and preconditioned to existing preliminary SAM-D drawings, and delivered to MDAC-EAST as GFE. Since most of the parts were applicable to hybrid applications, some part reconfiguration was necessary to provide a device suitable for use in a high temperature life test. Two hundred pieces of each part type were provided for the test program. In addition ten pieces of each part type were submitted configured to the actual SAM-D use condition. These SAM-D configured parts provided a basis for distinguishing between applicable and non-applicable failure modes/mechanisms.

The test program, conducted according to the comprehensive phases identified in Figure 3-2, is discussed in detail in the following paragraphs.

3.1 Test Preparation

The 100% visual examination of the test parts revealed several anomalous conditions described in detail in the Appendices. However, these anomalies had no detectable influence on program results.

Electrical test criteria, developed utilizing the preliminary SAM-D drawings, included, but were not limited to, all DC tests specified for 100% inspection. In some cases, functional and AC tests supplemented the DC tests. Electrical tests were conducted upon receipt of part (initial tests), at selected times during the test program (interim tests) and after test completion (final tests). The initial electrical parameter characterization served as a zero time baseline data set. Initial and final electrical tests were typically conducted at the test devices' rated temperature unless other constraints were imposed by the part test configuration. The interim electrical tests were performed at room ambient temperature, typically 25°C at specified intervals during the test program. A failure occurred when a measured parameter exceeded its specified limits.

A control sample, typically 5 parts, was established for each part type in the test program. These control samples, stored at laboratory ambient conditions, and tested prior to performing the periodic interim electrical tests on life test parts, provided a reference for data integrity.

CONTRACT ITEM NUMBER	ITEM	TYPE	SCD NUMBER	SCD REVISION LETTER AND DATE	
1	QUAD, 2-INPUT NAND GATE TTL/SSI	5400	772921	BASIC	7 JUN 74 ⚠1
2	MULTIPLEXER TTL/MSI	9309FM	M38510/ 01404	A	5 APR 73
4	NAND BUFFER TTL/SSI	5438	M38510/ 00303	B	23 DEC 71
5	RANDOM ACCESS MEMORY, 256 BIT TTL/LSI	93410	773050	BASIC	10 JUN 74 ⚠1
6	60 GATE RAYPACK CHIP	——	785072	A	25 JUN 73
7	OPERATIONAL AMPLIFIER	LM101A	772926	BASIC	7 JUN 74 ⚠1
8	VOLTAGE REGULATOR	LM104H	773051	BASIC	11 NOV 74 ⚠1
10	NPN LOW POWER SWITCH	2N3960	772928	BASIC	6 JUN 74 ⚠1
12	PNP LOW POWER AMPLIFIER	2N4260	772929	BASIC	11 SEP 75 ⚠1
13	NPN LOW POWER AMPLIFIER	2N5652	773052	BASIC	10 JUN 74 ⚠1
15	N CHANNEL FET	2N4857	772931	BASIC	10 JUN 74 ⚠1
16	GEN. PURPOSE SWITCH	1N914	772932	BASIC	7 JUN 74 ⚠1
18	HIGH CURRENT SWITCH	1N4942	773053	BASIC	7 JUN 74 ⚠1
19	PORCELAIN CHIP CAPACITOR	——	773054	BASIC	10 JUN 74 ⚠1
20	CERAMIC CHIP CAPACITOR	——	773055	BASIC	10 JUN 74 ⚠1
21	TANTALUM CHIP CAPACITOR	——	773056	BASIC	7 JUN 74 ⚠1
22	CERAMIC AXIAL LEAD CAPACITOR	——	773057	BASIC	10 JUN 74 ⚠1
23	CHIP-HIGH SELF-RESONANT FREQ. INDUCTOR	——	773058	BASIC	10 JUN 74 ⚠1
24	FERRITE BEAD INDUCTOR	——	773059	BASIC	7 JUN 74 ⚠1
25	CERAMIC CHIP RESISTOR	——	773060	BASIC	10 JUN 74 ⚠1
26	SPECIAL HYBRID TECHNOLOGY SUBSTRATE	——	773207	BASIC	6 MAY 74 ⚠1

⚠1 DRAWN DATE; ADVANCE DRAWING-NOT OFFICIALLY SIGNED OFF

FIGURE 3-1 TEST PROGRAM PARTS

PHASE	TITLE	ACTIVITY
A	TEST PREPARATION	o PHASE TEST PLANS o SOFTWARE PREPARATION FOR ELECTRICAL TESTS o ELECTRICAL PARAMETER CHARACTERIZATION
B	PHYSICAL EVALUATION	o CONSTRUCTION ANALYSIS o SAM-D CONFIGURED DEVICES o TEST CONFIGURED DEVICES
C	TEST CONFIGURATION EVALUATION	o TEST CIRCUIT DESIGN o HIGH TEMPERATURE EVALUATION o THERMAL CHARACTERIZATION o STEP STRESS TESTS o FINAL TEST CIRCUIT/TEST CONDITION SELECTION
D	ACCELERATED LIFE TESTS	o ACCELERATED LIFE TESTS o WITH BIAS o WITHOUT BIAS o FAILURE ANALYSIS-ALL FAILURES
E	DATA CORRELATION	o DATA EVALUATION o FAILURE MODE AND MECHANICAL EVALUATION o DATA CORRELATION BETWEEN TEST AND SAM-D PACKAGES o FAILURE RATE AND MEDIAN LIFE

FIGURE 3-2 TEST PROGRAM DESCRIPTION

Six of the test parts were received in chip form, i.e., without leads attached for test purposes. Figure 3-3 identifies these parts and summarizes their reaction to lead attach. The results were satisfactory in all but two cases:

3.2 Physical Evaluation

Samples of each part type submitted to the test program were subjected to a construction analysis to (a) positively identify the test devices' physical configuration, (b) identify any physical limitations or features which might influence the selection of temperature limits and (c) provide a baseline for failure analysis activities. Construction details are summarized in Figures 3-4 and 3-5 for semiconductors and passive parts respectively.

The life test parts were for the most part configured differently from their intended SAM-D use. Samples of the SAM-D use configurations were analyzed to establish which test accelerated failure mechanisms would be applicable and which would be discounted. For example, failures associated with the MDAC-EAST installed leads on the chip devices are not counted as applicable failures. Similarly, package related failures for beam lead semiconductors were carefully scrutinized for applicability.

The physical evaluation of the test devices was successful in revealing temperature limiting features but did not identify any characteristics or limitations which would impede program completion.

3.3 Test Configuration

Candidate life test circuits were selected and current/temperature relationships established using the Figure 3-6 test sequence. Candidate semiconductor bias circuits were evaluated at elevated ambient temperatures (up to 275°C for some devices) to find a bias circuit that:

(a) Maintained maximum rated voltage at the device terminals over the temperature range to provide a consistent voltage acceleration factor.

(b) Maintained the device current at a controlled low level to minimize failures due to thermal runaway and electromigration, and

(c) Maintained a consistent set of internal microcircuit stress conditions over the temperature range (a change in device state would indicate a significant change in internal stress conditions).

CONTRACT ITEM NO.	PART NO.	PART DESCRIPTION	DELIVERED CONFIGURATION	TEST CONFIGURATION	LEAD INTEGRITY	EFFECT OF LEAD ATTACH ON INDUCED FAILURES
18	773053	DIODE HIGH CURRENT	CHIP	LEADS ATTACHED USING HIGH TEMPERATURE SOLDER	SATISFACTORY LEAD DEGRADATION OCCURRED LATE IN TEST	NONE
19	773054	CHIP CAPACITOR	CHIP	LEADS ATTACHED USING HIGH TEMPERATURE SOLDER	UNSATISFACTORY-ALL LEADS FELL OFF BEFORE 1000 HOURS OF LIFE TESTS DUE TO SOLDER DEGRADATION	NONE
20	773055	CERAMIC CHIP CAPACITOR	CHIP	LEADS ATTACHED USING HIGH TEMPERATURE SOLDER	UNSATISFACTORY-ALL LEADS FELL OFF BEFORE 1000 HOURS OF LIFE TESTS DUE TO SOLDER DEGRADATION.	NONE
21	773056	TANTALUM CHIP CAPACITOR	CHIP	LEADS ATTACHED USING HIGH TEMPERATURE SOLDER	SATISFACTORY-LESS THAN 5% OF LEADS LOST DURING TEST PROGRAM	NONE
23	773058	INDUCTOR CHIP	CHIP	LEADS ATTACHED USING HIGH TEMPERATURE SOLDER	SATISFACTORY-LESS THAN 5% OF LEADS LOST DURING TEST PROGRAM	NONE
24	773059	FERRITE BEAD CHIP	CHIP	LEADS ATTACHED USING HIGH TEMPERATURE SOLDER	SATISFACTORY-LESS THAN 5% OF LEADS LOST DURING TEST PROGRAM	NONE

FIGURE 3-3 PARTS REQUIRING RECONFIGURATION

					LEAD MATERIAL				DIE CHARACTERISTICS			INTERCONNECTION BONDS		
DEVICE SCD NO.	GENERIC TYPE	PACKAGE TYPE	PACKAGE MATERIAL	LID SEAL	EXTERNAL	INTERNAL WIRE/BEAM	FRAME/POST/ METALLIZATION	DEVICE CONSTRUCTION	ATTACH	METALLIZATION	SCRIBE METHOD	DIE	FRAME/POST METALLIZATION	IDENTICAL TO SAM-D USAGE
772921	5400	16 PIN DIP	CERAMIC-Au-PLATED KOVAR LID	WELD	Au-PLATED KOVAR	Au BEAM LEADS	Au-PLATED REFRACTORY METAL	BEAM LEAD	N/A	Au/Ti/Pt	ETCH	Au/Au THERMO-COMPRESSION	N/A	NO
M38510/ 01404	9309	16 LEAD 1/4" x 3/8" FLAT PACK	CERAMIC-Au-PLATED KOVAR TOP AND BOTTOM	SOLDER	Au-PLATED KOVAR	Al WIRE	Au-PLATED KOVAR	CHIP & WIRE	Au-Si EUTECTIC	Al	MECHANICAL	Al/Al ULTRASONIC	Al/Au ULTRASONIC	YES
M38510/ 00303	5438	14 LEAD 1/4" x 3/8" FLAT PACK	CERAMIC - CERAMIC TOP	GLASS	Au-PLATED KOVAR	Al WIRE	Au-PLATED KOVAR	CHIP & WIRE	Au-Si EUTECTIC	Al	MECHANICAL	Al/Al ULTRASONIC	Al/Au ULTRASONIC	YES
773050	93410	16 LEAD 1/4" x 3/8" FLAT PACK	CERAMIC-Au-PLATED KOVAR TOP AND BOTTOM	SOLDER	Au-PLATED KOVAR	Al WIRE	Au-PLATED KOVAR	CHIP & WIRE	Au-Si EUTECTIC	Al	MECHANICAL	Al/Al ULTRASONIC	Al/Au ULTRASONIC	YES
785072	---	50 PIN 1 1/4" x 1 3/4" PLUG-IN PACKAGE	Au-PLATED KOVAR	WELD	Au-PLATED KOVAR	Au WIRE/ Au METALLIZATION/ Au BEAM LEADS	Au-PLATED KOVAR	BEAM LEAD	N/A	Au/Ti/Pt	ETCH	Au/Au THERMO-COMPRESSION	N/A	NO
772926	LM101A	16 PIN DIP	CERAMIC - Au-PLATED KOVAR LID	WELD	Au-PLATED KOVAR	Au BEAM LEADS	Au-PLATED REFRACTORY METAL	BEAM LEAD	N/A	Au/Ti/Pt	ETCH	Au/Au THERMO-COMPRESSION	N/A	NO
773051	LM104	10 PIN, TO-5	STEEL	WELD	Au-PLATED KOVAR	Al WIRE	Au-PLATED KOVAR	CHIP & WIRE	Au-Si EUTECTIC	Al	MECHANICAL	Al/Al ULTRASONIC	Al/Au ULTRASONIC	NO
772928	2N3960	3 LEAD, TO-18	STEEL	WELD	Au-PLATED KOVAR	Au BEAM LEADS	Au-PLATED KOVAR	BEAM LEAD	N/A	Au/Ti/Pt	ETCH	Au/Au THERMO-COMPRESSION	N/A	NO
772929	2N2907	3 LEAD, TO-18	STEEL	WELD	Au-PLATED KOVAR	Au BEAM LEADS	Au-PLATED KOVAR	BEAM LEAD	N/A	Au/Ti/Pt	ETCH	Au/Au THERMO-COMPRESSION	N/A	NO
773052	2N5652	4 LEAD, TO-72	STEEL	WELD	Au-PLATED KOVAR	Al WIRE	Au-PLATED KOVAR	CHIP & WIRE	Au-Si EUTECTIC	Al	MECHANICAL	Al/Al ULTRASONIC	Al/Au ULTRASONIC	NO
772931	2N4957	3 LEAD, TO-18	STEEL	WELD	Au-PLATED KOVAR	Au BEAM LEADS	Au-PLATED KOVAR	BEAM LEAD	N/A	Au/Ti/Pt	ETCH	Au/Au THERMO-COMPRESSION	N/A	NO
772932	1N914	3 LEAD, TO-18	STEEL	WELD	Au-PLATED KOVAR	Au BEAM LEADS	Au-PLATED KOVAR	BEAM LEAD	N/A	Au/Ti/Pt	ETCH	Au/Au THERMO-COMPRESSION	N/A	NO
773053	1N4942	PILL-BOX	CERAMIC - Au-PLATED KOVAR LID	SOLDER	THICK FILM GOLD	Al WIRE	THICK FILM GOLD	CHIP & WIRE	Au-Si EUTECTIC	Al	MECHANICAL	Al/Al ULTRASONIC	Al/Au ULTRASONIC	NO

FIGURE 3-4 CONSTRUCTION SUMMARY - SEMICONDUCTOR DEVICES

DEVICE SCD. NO.	DESCRIPTION	PACKAGE FORM	CONSTRUCTION	END CAPS/ CONDUCTOR PADS/ LEADS	TERMINATION TECHNIQUE	IDENTICAL TO SAM-D USAGE
773054-21	PORCELAIN CHIP CAPACITOR	SELF-ENCAPSULATED NON-POROUS PORCELAIN (0.117 in. X 0.117 in. X 0.075 in.)	PALLADIUM ELECTRODES SEPARATED BY NON-POROUS PORCELAIN DIELECTRIC	20% PALLADIUM, 80% SILVER	MDAC-EAST ATTACHED LEADS (NICKEL)	NO
773055-6	CERAMIC CHIP CAPACITOR	SELF-ENCAPSULATED CERAMIC (0.022 in. X 0.057 in. X 0.102 in.)	PLATINUM AND GOLD ELECTRODES SEPARATED BY CERAMIC DIELECTRIC	SILVER	MDAC-EAST ATTACHED LEADS (NICKEL)	NO
773056-20	TANTALUM CHIP CAPACITOR	MOLDED EPOXY (0.143 in. X 0.100 in. X 0.088 in.)	TANTALUM ANODE AND MANGANESE DIOXIDE CATHODE SEPARATED BY TANTALUM PENTOXIDE DIELECTRIC	GOLD PLATED NICKEL	MDAC-EAST ATTACHED LEADS (NICKEL)	NO
773057-18	CERAMIC AXIAL LEAD CAPACITOR	MOLDED EPOXY (0.256 in. X 0.096 in. Dia.)	RARE METAL ELECTRODES SEPARATED BY CERAMIC DIELECTRIC	NICKEL	NICKEL	YES
773058-39	HIGH SELF-RESONANT FREQUENCY CHIP INDUCTOR	MOLDED DIALLYL PHTHALATE (0.160 in. X 0.126 in. X 0.126 in.)	POLYNYLON INSULATED COPPER WIRE WOUND ON A FERRITE CORE	GOLD OVER NICKEL OVER TUNGSTEN	MDAC-EAST ATTACHED LEADS (NICKEL)	NO
773059	FERRITE BEAD INDUCTOR (CHIP)	MOLDED DIALLYL PHTHALATE (0.160 in. X 0.125 in. X 0.125 in.)	POLYNYLON INSULATED COPPER WIRE WOUND ON A FERRITE TOROID CORE	NICKEL OVER TUNGSTEN	MDAC-EAST ATTACHED LEADS (NICKEL)	NO
773060-300	FIXED FILM RESISTOR (CHIP)	96% ALUMINA CERAMIC CARRIER (0.153 in. X 0.050 in. X 0.014 in.)	RUTHENIUM BASE FIRE ON RESISTOR MATERIAL FIRED ON A CERAMIC CARRIER	PLATINUM/GOLD	NO LEADS	YES
773207	SPECIAL HYBRID TECHNOLOGY SUBSTRATE (1.16 in. X 1.16 in. X 0.041 in.)	CERAMIC SUBSTRATE	RESISTOR, CONDUCTOR AND DIELECTRIC COMPOSITIONS FIRED ON A CERAMIC SUBSTRATE	PLATINUM/GOLD CONDUCTOR COMPOSITION	SUBSTRATES PLUG INTO EDGE CONNECTOR	N/A

FIGURE 3-5 CONSTRUCTION SUMMARY - PASSIVE PARTS

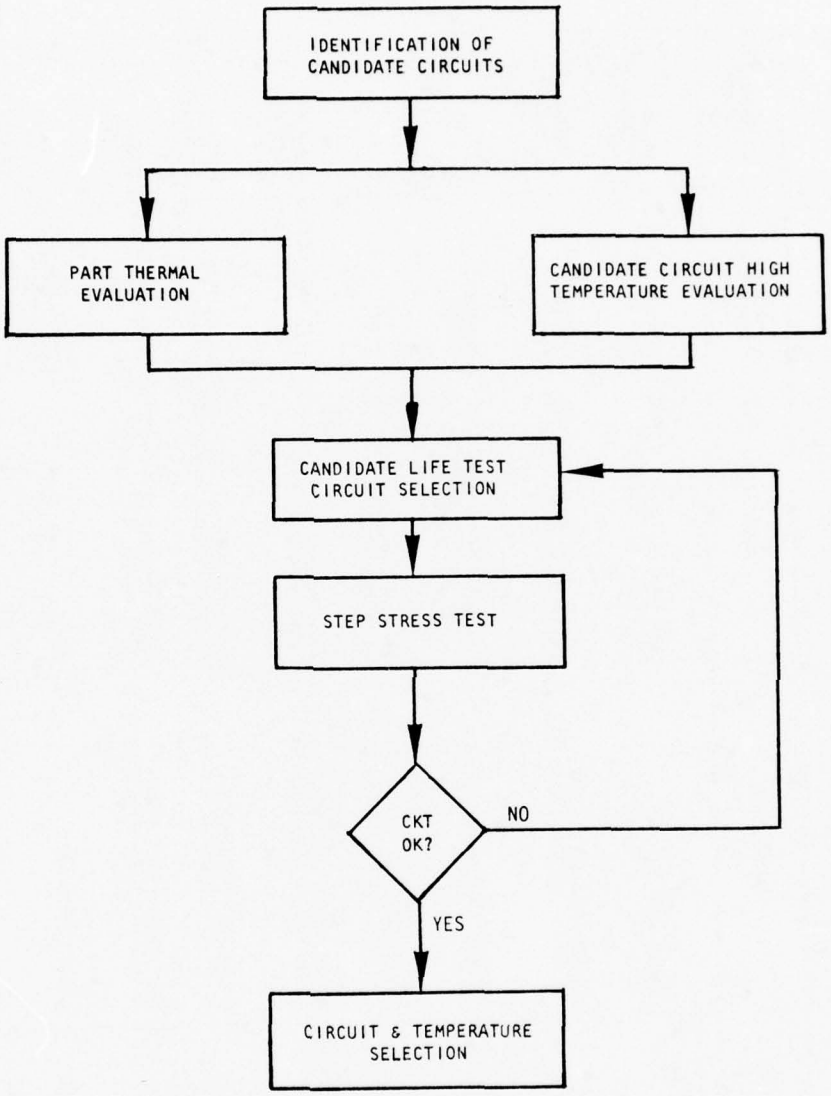

FIGURE 3-6 HIGH TEMPERATURE BIAS CIRCUIT AND TEMPERATURE SELECTION SEQUENCE

When a bias circuit satisfied the above objectives, a thermal characterization was performed with the device operated in the selected bias circuit. Electrical techniques were then used to establish the maximum internal temperature. Step stress testing was then accomplished to verify the suitability of the bias circuit and to aid in the selection of accelerated life test temperatures.

The passive parts, all two terminal devices except for the Special Hybrid Substrate, P/N 773207, were straightforward as far as bias circuit evaluations were concerned. Each passive part was evaluated under rated voltage conditions and temperature response established. The diodes and transistors also were straightforward and required only a few bias circuit configurations for evaluation. The microcircuits, being the most complex devices, required extensive bias circuit evaluation. The microcircuit candidate bias circuits evolved from a study of the device schematic and previous experience with similar parts.

Concurrent with the candidate bias circuit high temperature investigation, a part thermal evaluation was accomplished to determine the device internal temperature over the ambient temperature range of interest. Only those devices dissipating power were included in this activity, thus excluding all the capacitors. Resistors were evaluated using the change in resistance as a function of material temperatures. Semiconductor devices were investigated using an input diode as a temperature sensitive parameter to determine maximum junction temperatures using a technique similar to MIL-STD-883, Method 1012, Condition C. The transistors and diodes drew insufficient current at the test temperatures to account for any appreciable internal temperature rise.

After establishing the device internal temperature rise in the candidate bias circuit, a step stress test was accomplished to: (1) validate the non-destructive nature of the selected high temperature bias circuit, and (2) obtain sufficient failure data on a reasonable quantity of parts to make a final determination of the accelerated test conditions. Temperature step stress tests were typically accomplished using 20 parts in the candidate bias circuit configuration. The starting temperature was determined by the part material limitations and analysis of the preliminary thermal evaluations. Each step duration was usually 16 hours with the ambient temperature increased in 25°C increments. Tests were typically continued until the ambient temperature reached 275°C or 50% failure occurred, whichever came first. Failure analysis was accomplished to determine cause of failure.

3.4 Accelerated Life Tests

Circuit evaluations, thermal studies and the temperature step stress results were used collectively to establish the bias circuit configuration and the maximum ambient temperature for the accelerated life tests. For three parts (P/Ns 772928, 773053, 773060) this assessment resulted in the decision to conduct life tests without an applied bias. Figure 3-7 defines the typical test matrix for both the active (semiconductor devices) and the passive parts. The standard test configuration consisted of 5 test cells, 30 parts in each cell; the maximum bias voltage was applied at 3 test temperatures, providing data suitable for evaluation by an Arrhenius Reaction Rate Model. Two other cells, one without an applied voltage, and one with a reduced voltage, were tested at the maximum temperature to obtain voltage sensitivity data. In order to provide additional voltage effect data for an Eyring reaction rate evaluation, four of the semiconductors (P/Ns M38510/01404, M38510/10304, 772926, and 773052) were subjected to a special test matrix which provided four test cells at maximum ambient temperature, each cell having a different voltage level, including zero; the fifth test cell operated at maximum bias conditions at a lower temperature.

The selected life test ambient temperatures were separated by a minimum of 25°C. The test duration was 4000 hours for active devices and 6000 hours for a passive parts; however, a test cell could be terminated as soon as 50% failure occurred for the active parts or 63% for passive parts.

Interim electrical measurements were performed typically at 4, 8, 16, 32, 64, 128, 256, 512, 1000, 2500, 4000, and 6000 (passive parts only) hours. The initial electrical tests were accomplished at zero hours and the final electrical tests were accomplished at 4000 hours for active parts or 6000 hours for passive parts. Flexibility was maintained throughout the test program to incorporate additional tests as the need arose. For example, the 2N5652 transistor, P/N 773052, eventually included additional measurements at 0.5, 1.0, and 2.0 hours and the two inductors, P/N 770358-39 and P/N 770359, incorporated tests at 500 hour intervals after 1000 hours of test. In addition, test cells were selectively added to three part types when data analysis indicated the added cells could provide useful information.

All failures in the test program were analyzed to establish the cause of failure and the likely failure mechanism.

. ACTIVE PARTS

		TEMPERATURE		
		HIGH	MID	LOW
BIAS VOLTAGE	ZERO	S / E		
	MAXIMUM	S / E	S / E	S
	V_1	S / E		
	V_2	/ E		

S = STANDARD TEST

E = SPECIAL EYRING TEST

PASSIVE PARTS

		TEMPERATURE		
		HIGH	MID	LOW
BIAS VOLTAGE	ZERO	S		
	MAX	S	S	S
	V_1	S		

FIGURE 3-7 TEST MATRIX

3.5 Failure Analysis Procedure

All semiconductors that failed an electrical test during Step Stress or Life Tests were analyzed to determine the particular failure mode, failure mechanism, and probable cause of failure. The general analysis procedure was as follows:

1) All failures were retested separately on the automatic test set to verify the failure.
2) All failed parameters were confirmed using a curve tracer, or if necessary, a bench test set.
3) The failure was isolated to a specific junction or element to the extent possible via external pin-pin curve tracer measurements.
4) The failures were classified into subgroups, on the basis of the analysis findings to this point.
5) A representative sample of parts from each subgroup was subjected to detailed analysis including external optical examination, delidding, internal optical and SEM examination, die level probing, and chemical or metallurgical dissectioning. Die level probing of defective junctions or components included stripe severing, followed by complete metallization removal to isolate the degradation to the exact responsible active, parasitic, or spurious element. (For surface instability related failures, this was done only if external pin-pin curve tracer tests had indicated which component was degraded. Otherwise the part was delidded and examined only).
6) A representative sample of the remaining parts from each subgroup were subjected to the following steps to confirm their categorization and to obtain any additional information:
   a) Unpowered Bake - Each device was baked, then 25°C DC electrical data was obtained. The exact time and temperature of the bake depended on the time and temperature at which the failure occurred. Usually, an overnight bake (16 hours) at the test cell temperature sufficed. In most instances, no attempt was made to obtain any quantitative information from these bakes other than whether or not the device cured or improved sufficiently to establish that a surface-related mechanism existed.
   b) Leak Tests - Each device was subjected to a helium bomb fine leak test and a fluorocarbon gross leak test. Unless stated otherwise in the report, the devices did not exhibit any loss of hermiticity.

c) Delidding - Each device was delidded and subjected to routine optical examinations and documentation.

This same general approach was used in analyzing the passive components. Only the specific techniques would vary.

The results of the detailed failure analyses of the test program failures are summarized in the Appendices. The failure summary tables contain a delineation of the failure symptoms, mode, mechanism, and cause for each failure subgroup.

3.6 Data Correlation

The evaluation of the accelerated test data generally followed published techniques [4][5][6]. Part failure analysis resulted in the grouping of failures by failure mechanism for data analysis. The times to failure for applicable failures were established and cumulative failure distributions fitted to the test data. Due to a substantial test history [1][4][5][6] the lognormal failure distribution [7] was assumed to be applicable for semiconductor surface related failure mechanisms. Using data obtained at different test temperatures, the Arrhenius and/or Eyring models were evaluated; the selected model allowed data extrapolation to storage temperatures of interest. The maximum instantaneous failure rate for a 20 year storage period was calculated for a storage temperature range of 25°C to 100°C and appears in the text as $\lambda(t)_{MAX}$. The failure rate equation is presented to allow calculation for other times and temperatures.

When the accelerated tests yielded insufficient failures for statistical distribution analysis, parametric test data was evaluated for obvious trends so that times to failure could be extrapolated and a distribution defined. When no obvious parameter trends existed, failure rates were still estimated by assuming certain characteristics for the failure distribution and the Arrhenius relationship, thus allowing the calculation of a conservative failure rate for the storage condition.

The following paragraphs describe in more detail the methodology used for data analysis (determination of failure distribution) and data synthesis (failure rate estimation).

3.6.1 Data Analysis

3.6.1.1 Failure Time Interpolation - All test cells were subjected to electrical measurements at specified time intervals. Failures were detectable only at these discrete measurement times. When failures were catastrophic, the time at failure was taken to be the midpoint of the measurement time interval.

$$t_F = t_1 + \frac{t_2 - t_1}{2} = \frac{t_1 + t_2}{2} \qquad (1)$$

t_F = failure time

t_1 = last measurement before failure

t_2 = time at which a catastrophic failure was detected

This approach is used by others when evaluating catastrophic failures encountered in life tests [8]. Catastrophic failures were primarily encountered in the passive parts.

The semiconductor device failures primarily exhibited parameter value changes with respect to time. At each measurement time the values of all test parameters were recorded. After a device had failed, the failed parameter value and previous non-failed values of the parameter were obtained from the test records. The failed and the two previous non-failed values of the parameter, with the corresponding measurement times, were used either to generate an empirical equation that related time to the parameter value, or were graphically evaluated. Solving the empirical equation, using the parameter failure limit, provides an interpolated estimate of the actual failure time of the device. A graphical solution for the interpolated estimate of failure time is illustrated in Figure 3-8. When a failed device exhibited more than one failed parameter, each failed parameter was interpolated and the earliest estimated failure time was used for the device. Using this interpolation procedure to estimate the failure time for each failed device allowed the number of data points to reflect the number of device failures.

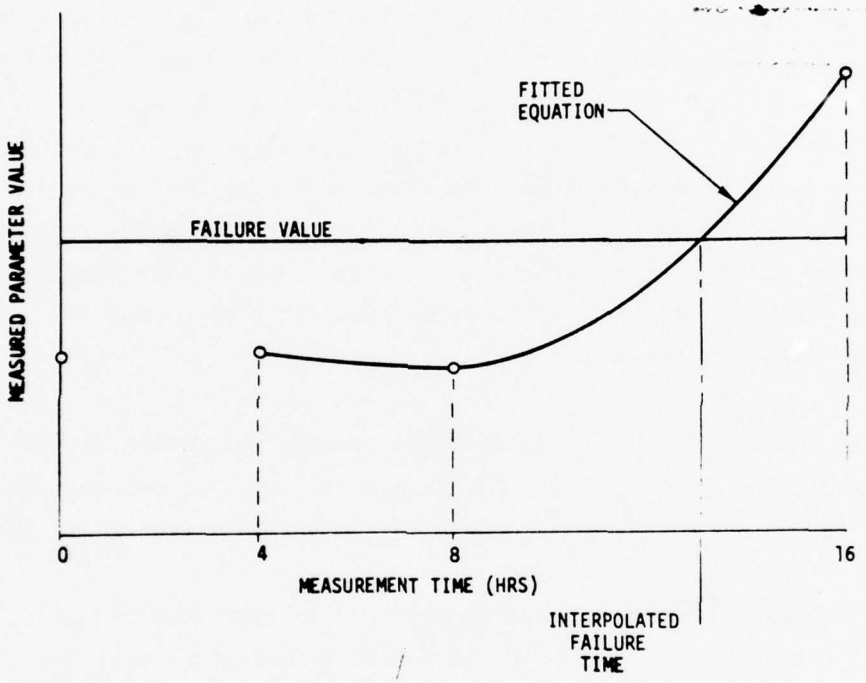

FIGURE 3-8 FAILURE TIME INTERPOLATION

3.6.1.2 Failure Time Extrapolation - Some of the test parts yielded few failures during the accelerated life test program. When this occurred, the parametric test data was evaluated for obvious trends which would allow extrapolation of time to failure, either by fitting an equation to the data or by graphical means. Since indiscriminate parameter extrapolation may result in orders of magnitude error in median life estimation, only that data which indicated obvious trends were used. Also, wherever it appeared that extrapolation would be required, the life tests were continued as long as possible to verify that the trend continued.

3.6.1.3 Failure Distribution Evaluation - All test cell data was fitted to a statistical distribution which not only adequately described the data, but also conformed, where known, to the behavior of the underlying physical phenomena. For example, sufficient test history is available to justify the selection of the lognormal distribution for surface related semiconductor failure mechanisms [1] [4][5][6], an assumption completely substantiated by the test results. The lognormal distribution has also been used to evaluate insulation life characteristics [8]; the two inductive devices in the test program both displayed insulation degradation, and their failure distribution provided a very good fit for the lognormal distribution.

Data plotting and testing for distributional assumptions generally followed published techniques [1][5][6][8]. Goodness-of-fit evaluations were accomplished using such techniques as the chi-square and Kolmogorov-Smirnov tests [9].

Bimodal lognormal distributions were encountered in some semiconductor devices. This has been encountered previously and was therefore not unexpected. The bimodal failure distribution is:

$$\text{Cdf life}_{\text{TOTAL}} = \left\{ \frac{1}{\sigma_F\sqrt{2\pi}} \int_0^t \frac{1}{t'} \left\{ \exp - \frac{(\ln t' - \mu_F)^2}{2\sigma_F^2} \right\} dt \right\} \quad (\%F)$$

$$+ \left\{ \frac{1}{\sigma_M\sqrt{2\pi}} \int_0^t \frac{1}{t'} \left\{ \exp - \frac{(\ln t' - \mu_M)^2}{2\sigma_M^2} \right\} dt \right\} \quad (\%M) \qquad (2)$$

where:

μ_F = ln (median life of the freak distribution)

σ_F = standard deviation of the freak distribution

μ_M = ln (median life of the main distribution)

σ_M = standard deviation of the main distribution

%F = the percentage of the total population that is described by the freak distribution

%M = the percentage of the total population that is described by the main distribution

t = use time

A two parameter Weibull distribution was found to adequately describe the performances of some passive parts. The Weibull Cumulative Distribution Function (CDF) can be expressed as follows:

$$CDF = 1 - \exp - \left(\frac{t}{\theta}\right)^{\beta} \qquad (3)$$

where:

θ = Weibull scale parameter (the 63rd percentile)

β = Weibull shape parameter

t = time

3.6.2 Data Synthesis

3.6.2.1 Arrhenius Model - The Arrhenius model describes the median device lifetime as a function of temperature at a fixed voltage, and may be expressed as follows:

$$t_{50\%}(\text{or } \theta) = A \exp \frac{E_A}{kT} \qquad (4)$$

where:

$t_{50\%}$ = device median life at temperature (for lognormal distribution)

θ = device scale parameter at temperature (for Weibull distribution)

A = a constant

E_A = apparent activation energy in electron volts (eV)

k = Boltzmann's constant = 8.617×10^{-5} eV/K

T = absolute junction temperature (K)

Evaluation of the Arrhenius model using the median life data derived from the matrix of accelerated life tests results in the Arrhenius plots shown in Figure 3-9. The temperature scale for the plots is a linear function of 1/kT and the time scale is log (time). Thus, a plot of the Arrhenius equation will appear as a straight line, since

$$\ln t_{50\%} = \ln A + \frac{E_A}{kT} \tag{5}$$

3.6.2.2 Eyring Model - The Eyring reaction rate model described device lifetimes as a function of both temperature and voltage, and may be expressed as [3]:

$$t_{50\%} = \frac{Gh}{kT} \exp\{\frac{E_{TA}}{kT} - f(V) \left[C + \frac{D}{kT}\right]\} \tag{6}$$

where:

$t_{50\%}$ = device median life at temperature

G, C, and D are positive constants

E_{TA} = activation energy in electron volts (eV)

f(V) = some function of bias voltage

k = Boltzmann's constant = 8.617×10^{-5} eV/k

h = Planck's constant = 1.149×10^{-18} eV hr

T = absolute junction temperature (K)

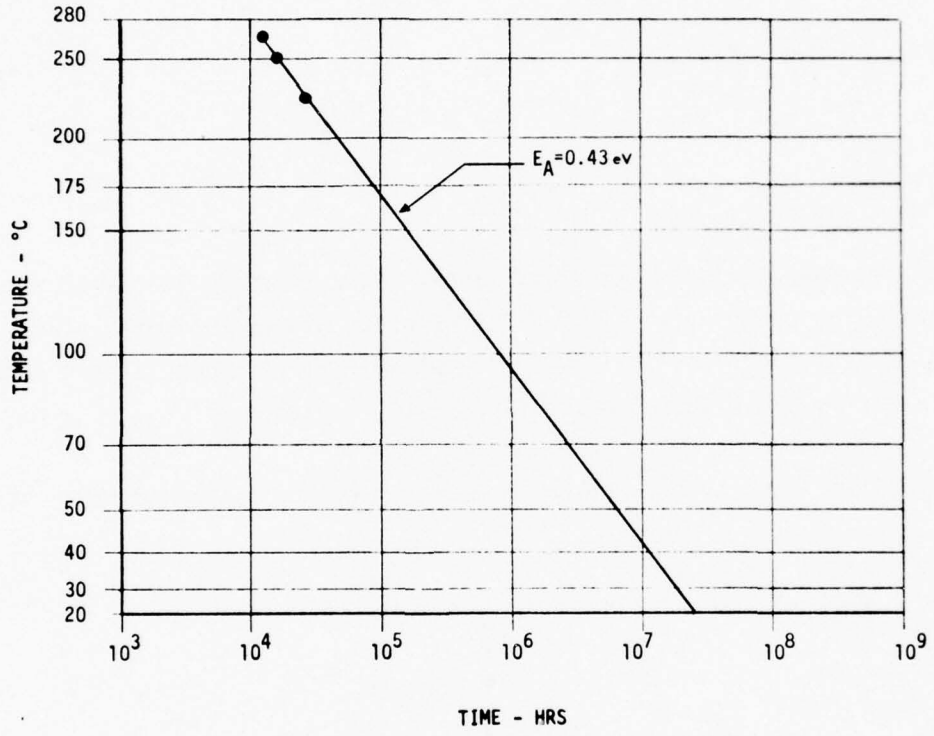

FIGURE 3-9 ARRHENIUS PLOT

The first step in evaluating the unknowns in equation (5) is to determine the form of the f(V) function. A plot of ln $t_{50\%}$ as a function of voltage, but at a fixed temperature, provides a means for examining the shape of f(V) since,

$$\ln t_{50\%} = \ln \frac{Gh}{kT} + \frac{E_{TA}}{kT} - f(V) \left[C + \frac{D}{k}\right] \tag{7}$$

and at fixed temperature, equation (6) reduces to

$$\ln t_{50\%} = a - b\, f(V) \tag{8}$$

where:

a and b are constants

Thus, an f(V) function equal to V will appear as a straight line, and other functions can be evaluated using curve fitting techniques. Although several of the test parts displayed a sensitivity to the level of applied voltage, insufficient data was available for an Eyring Model Analysis.

3.6.2.3 Failure Rates - The failure rate for a single distribution is defined as [10]:

$$\lambda(t) = \frac{f(t)}{R(t)} \tag{9}$$

where:

$\lambda(t)$ = the instantaneous failure rate at time t

$f(t)$ = the failure density at time t

$R(t)$ = the reliability at time t

The failure rate for the lognormal distribution, used throughout this report, is defined as:

$$\lambda(t) = \frac{\frac{1}{t\,\sigma\,\sqrt{2\pi}}\ \exp - \frac{(\ln t - \mu)^2}{2\sigma^2}}{\frac{1}{\sigma\,\sqrt{2\pi}}\int_t^\infty \frac{1}{t}\ \exp - \frac{(\ln t - \mu)^2}{2\sigma^2}} \qquad (10)$$

where:

μ = ln (median life)

σ = the standard deviation

Assuming that an Arrhenius equation defines the median life at a junction temperature provides the following temperature dependent, lognormal failure rate:

$$\lambda(t) = \frac{\frac{1}{t\,\sigma\,\sqrt{2\pi}}\ \exp - \frac{[\ln t - (\ln A + E_A/k\,T)]^2}{2\sigma^2}}{\frac{1}{\sigma\,\sqrt{2\pi}}\int_t^\infty \frac{1}{t}\ \exp - \frac{[\ln t - (\ln A + E_A/k\,T)]^2}{2\sigma^2}} \qquad (11)$$

For a bimodal distribution consisting of two lognormal failure rates, the total instantaneous failure rate is:

$$\lambda(t)_{Total} = \lambda(t)_{Freak}\ \ (\%\ Freak) + \ \lambda(t)_{Main}\ \ (\%\ Main) \qquad (12)$$

The standard deviation (6) used in calculating the failure rate was established by "pooling" the standard deviations calculated for identically biased test cells as follows:

$$\sigma^2 = \frac{(\sigma_1)^2 N_{F_1} + (\sigma_2)^2 N_{F_2} + \ldots (\sigma_N)^2 N_{F_N}}{N_{F_1} + N_{F_2} + \ldots N_{F_N}} \tag{13}$$

where:

σ_i = calculated standard deviation in cell i

N_{F_i} = number of failures in cell i

The failure rate for the Weibull distribution used in this report is defined as:

$$\lambda(t) = \left[\frac{\beta}{t}\right] \left[\frac{t}{\theta}\right]^{\beta} \tag{14}$$

where:

β = shape parameter

θ = scale parameter (the 63rd percentile)

t = time

Assuming that an Arrhenius equation defines the scale parameter at a storage temperature provides the following temperature dependent Weibull failure rate:

$$\lambda(t) = \left[\frac{\beta}{t}\right] \left[\frac{t}{A \exp \frac{E_A}{kT}}\right]^{\beta} \tag{15}$$

The developed failure rate equations were used to calculate the maximum instantaneous failure rate for a storage condition. $\lambda(t)_{MAX}$ as used in this report is the maximum value of instantaneous failure rate for a storage temperature range of 25°C to 100°C for a 20 year time period. The failure rate equations for each part are presented in the Appendices and failure rates can be calculated for any specific time and temperature combinations.

The term "high storage reliability potential" is used in this report when describing a part which experienced insufficient life test failures for a failure distribution/failure rate analysis. As a basis for reference, a failure rate was calculated for these parts by assuming the cumulative percentage of failures at the end of the life test (4000 or 6000 hours) would be either a lognormal or Weibull distribution (depending on the part) having a conservative standard deviation or shape parameter. An Arrhenius model having an activation energy of 1.0 eV was assumed to be applicable, allowing the calculation of failure rates in the storage temperature range of interest. In all cases the calculated failure rate was very small, and $\lambda(t)_{MAX} << 10^{-10}$ failures per hour is used in this report to quantify the term "high storage reliability potential".

4.0 SUMMARY OF RESULTS

Details of the accelerated life tests are provided for each part in an individual appendix in this report. A summary of program findings is given by part category in Figure 4-1.

Category 1 (11 parts) - Parts having sufficient life test failures for failure distribution/failure rate analysis.

Category 2 (2 parts) - Parts with few life test failures but displaying an obvious parameter degradation trend allowing failure time extrapolation and subsequent failure distribution/failure rate analysis.

Category 3 (8 parts) - Parts having no obvious parameter degradation trends and too few life test failures (or applicable failures) for failure distribution/failure rate analysis.

Included in Figure 4-1 are the life test failure percentage, major failure mechanism identification, failure distributions, calculated maximum instantaneous failure rate, recommendation status, and Appendix references for detail information.

Thirteen parts (eleven Category 1 plus two Category 2) provided sufficient failures for failure distribution/failure rate analysis. Nine of these parts (seven Category 1 and two Category 2) had temperature induced failure mechanisms and are therefore considered applicable to a storage environment. The remaining four Category 1 parts had failure mechanisms induced by the combined effects of voltage and temperature and provide a conservative estimate for storage failure rates. Evidence of voltage sensitivity was observed in several semiconductor devices but the data was not adequate for a comprehensive Eyring model evaluation. The log-normal failure distribution was found to adequately describe all semiconductor failure distributions and some passive parts failure distributions. The Weibull failure distribution provided a good fit for the balance of the passive parts.

The eight parts comprising Category 3 include four TTL integrated circuits, the two diodes, and two chip capacitors. The TTL integrated circuit results corroborate previous findings [1][11] on the high potential reliability which can be obtained from this mature technology when properly manufactured and screened. Even though one of the diodes encountered only a few failures, a recommendation is made for further investigation of what is considered to be a potentially

DEVICE SCD NO.	ITEM	APPENDIX	LIFE TEST FAILURE PERCENTAGE	MAJOR LIFE TEST FAILURE MECHANISMS		ACTIVATION ENERGY (eV)		FAILURE DISTRIBUTION	$\lambda(t)_{MAX}$ (1) FAILURES/HOUR	RECOMMENDATIONS
				DESCRIPTION	PERCENTAGE OF TOTAL FAILURES	FREAK	MAIN			
CATEGORY 1										
773050	256 BIT RANDOM ACCESS MEMORY	D	62.0%	MOBILE ION DRIFT	12.9%	---	---	---	---	
				CATION DRIFT	41.9%	0.5 (3)	1.0 (4)	LOGNORMAL	4.3×10^{-5} (5)	YES
				ALUMINUM SPEARING	39.8%	---	---	---	---	
772926	OPERATIONAL AMPLIFIER	F	36.0%	MOBILE ION DRIFT	98.1%	---	3.09	LOGNORMAL	1.8×10^{-18} (5)	YES
773051	VOLTAGE REGULATOR	G	28.0%	MOBILE ION DRIFT	97.6%	1.36	2.01	LOGNORMAL	3.25×10^{-10} (5)	YES
772928	LOW POWER SWITCH	H	69.3%	MOBILE ION DRIFT OR SURFACE STATES	100%	---	1.81	LOGNORMAL	5.66×10^{-6}	YES
773052	NPN LOW POWER AMPLIFIER	J	75.7%	INCREASE IN SURFACE STATE DENSITY	78%	2.07	2.24	LOGNORMAL	6.97×10^{-15}	YES
				MOBILE ION DRIFT	18.9%	---	---	---	---	
772931	N CHANNEL FET	K	36.5%	MOBILE ION DRIFT	69.4%	0.11	0.67	LOGNORMAL	1.3×10^{-6} (5)	YES
773056-20	TANTALUM CHIP CAPACITOR	P	40.0%	DIELECTRIC DEGRADATION	61%	---	1.27	WEIBULL	1.13×10^{-6}	YES
773057-18	CERAMIC AXIAL LEAD CAPACITOR	Q	78%	MATERIAL DEGRADATION	98%	---	1.18	WEIBULL	9.4×10^{-10}	NO
773058-39	HIGH SELF-RESONANT FREQUENCY INDUCTOR CHIP	R	40%	INSULATION DIFFUSION	84%	---	2.93	LOGNORMAL	4.4×10^{-10}	YES
773059	FERRITE BEAD INDUCTOR	S	52.0%	INSULATION DIFFUSION	100%	---	1.31	LOGNORMAL	5.1×10^{-14}	YES
773207	SPECIAL HYBRID SUBSTRATE	U	13.7%	NOT ESTABLISHED	100%	---	1.91	WEIBULL	2.96×10^{-10}	NO
CATEGORY 2										
772929	LOW POWER AMPLIFIER	I	7.3%	HEADER BURRS	82%	---	0.43	LOGNORMAL (4)	2.9×10^{-10} (4)	YES
773060-300	CERAMIC CHIP RESISTOR	T	2.0%	NOT ESTABLISHED	100%		0.27	LOGNORMAL (4)	3.3×10^{-6} (4)	YES

FIGURE 4-1 SUMMARY - PROGRAM RESULTS (CONT. NEXT PAGE)

DEVICE SCD NO.	ITEM	APPENDIX	LIFE TEST FAILURE PERCENTAGE	MAJOR LIFE TEST FAILURE MECHANISMS		ACTIVATION ENERGY (eV)		FAILURE DISTRIBUTION	$\lambda(t)_{MAX}$ (1) FAILURES/HOUR	RECOMMENDATIONS
				DESCRIPTION	PERCENTAGE OF TOTAL FAILURES	FREAK	MAIN			
CATEGORY 3										
772921	QUAD 2-INPUT NAND GATE	A	3.3%	BEAM TO DIE SHORT	60%	---	---	(2)	(2)	NO
M38510/ 01404	DUAL 4-INPUT MULTIPLEXER	B	1.3%	LIFTED Al-Al BOND	100%	---	---	(2)	(2)	NO
M38510/ 00303	QUAD 2-INPUT NAND BUFFER	C	8.7%	MULTIPLE	---	---	---	(2)	(2)	NO
785072	60 GATE RAYPACK CHIP	E	3.3%	MULTIPLE	---	---	---	(2)	(2)	NO
772932	GENERAL PURPOSE SWITCH	L	3.3%	MOBILE ION DRIFT	40%	---	---	(2)	(2)	NO
773053	HIGH CURRENT SWITCH	M	43.1%	GOLD SCAVENGING	93.5%	---	---	(2)	(2)	YES
773054-21	PORCELAIN CHIP CAPACITOR	N	3.3%	SILVER SCAVENGING	100%	---	---	(2)	(2)	NO
773055-6	CERAMIC CHIP CAPACITOR	O	2.0%	NOT DETERMINED	100%	---	---	(2)	(2)	NO

(1) MAXIMUM CALCULATED INSTANTANEOUS FAILURE RATE FOR A 20 YEAR STORAGE PERIOD (TEMPERATURE RANGE: 25°C TO 100°C).

(2) INSUFFICIENT FAILURES (OR APPLICABLE FAILURES) FOR FAILURE DISTRIBUTION ANALYSIS - NO OBIVOUS PARAMETER DEGRADATION TRENDS.

(3) THESE ARE ASSUMED VALUES. INSUFFICIENT DATA FOR ARRHENIUS EVALUATION.

(4) PARAMETER DEGRADATION TREND ALLOWED EXTRAPOLATION OF TIMES TO FAILURE.

(5) BASED ON OPERATIONAL CONDITION. STORAGE FAILURE RATE SHOULD BE MANY ORDERS OF MAGNITUDE LESS.

(6) CATEGORY 1 - PARTS HAVING SUFFICIENT LIFE TEST FAILURES FOR FAILURE DISTRIBUTION/FAILURE RATE ANALYSIS.

CATEGORY 2 - PARTS WITH FEW LIFE TEST FAILURES BUT DISPLAYING AN OBVIOUS PARAMETER DEGRADATION TREND ALLOWING FAILURE TIME EXTRAPOLATION.

CATEGORY 3 - PARTS HAVING NO PARAMETER DEGRADATION TRENDS AND TOO FEW FAILURES (OR APPLICABLE FAILURES) FOR FAILURE DISTRIBUTION/ FAILURE RATE ANALYSIS.

FIGURE 4-1 SUMMARY - PROGRAM RESULTS (CONT.)

marginal design configuration. The two chip capacitors originally were intended to have an applied voltage as an additional life test accelerator. The early loss of the MDAC-East installed test leads due to solder degradation precluded use of voltage as an accelerator for most of the test, and temperature alone induced only a few failures.

5.0 CONCLUSIONS AND RECOMMENDATIONS

Specific conclusions and recommendations for each part in the test program are summarized in Figure 5-1. The Category 3 parts are grouped for a common entry.

In general the parts tested should have a good storage reliability potential. However, seven parts displayed characteristics which merit further investigation.

P/N 773050, 256 Bit Random Access Memory - There were five different date codes and two different device designs in the test program parts, resulting in a reduced data base for analysis. The tests on this part should be repeated using a homogenius lot.

P/N 772928, Low Power Switch - This transistor has a specified storage temperature limit of 200°C. Severe gain degradation (50% at 4000 hours) was encountered by this part at temperatures as low as 150°C. Further investigation of the failure mechanism, lot-to-lot variability, and appropriateness of the specified 200°C part storage temperatures are required.

P/N 772929, Low Power Amplifier - This transistor also experienced gain degradation during the life tests, but much less severely than P/N 772928. However the data analysis projects significant gain degradation at storage temperatures above 150°C. Since the part specification establishes 200°C as the upper storage temperature limit, additional investigation into lot-to-lot variability and the appropriateness of the 200°C storage temperature limit are in order.

P/N 773052, NPN Low Power Amplifier - This transistor, while also experiencing gain degradation under a storage test condition, evidenced contamination by mobile ions in the oxide which could affect operational performance. The impact of the mobile ion contamination should be investigated. In addition, this transistor specification also identifies 200°C as the upper storage temperature limit; however, the freak population (10% of total parts) will have marginal life characteristics at temperatures above 150°C. The appropriateness of the specified 200°C storage temperature limit should be investigated.

P/N 773058-39 and 773059 Inductors - Both of these inductors exhibited insulation degradation at temperatures below or at the specified maximum limit (125°C). The acceptibility of the 125°C temperature limit and lot-to-lot variability of the insulation diffusion failure mechanism should be investigated.

P/N 773056-20, Tantalum Chip Capacitor - The part specification establishes 125°C as the upper storage temperature limit. Data analysis indicates this part will have marginal life characteristics at temperatures above 100°C. The validity of the 125°C part storage temperature limit should be investigated.

DEVICE SCD NO.	ITEM	CATEGORY	CONCLUSIONS	RECOMMENDATIONS
773050	256 BIT RANDOM ACCESS MEMORY	1	o THE PRESENCE OF TWO DIFFERENT INTEGRATED CIRCUIT DICE IN THE TEST SAMPLE IMPACTED DATA ANALYSIS BY REDUCING THE SAMPLE SIZE. o THE ZERO VOLT TEST CELL YIELDED NO FAILURES, INDICATING A HIGH STORAGE RELIABILITY POTENTIAL. o FAILURES INDUCED UNDER A VOLTAGE STRESS CONDITION ("LARGE" DIE) INDICATED A BIMODAL FAILURE DISTRIBUTION.	o ADDITIONAL LIFE CHARACTERIZATION IS NECESSARY FOR EACH INTEGRATED CIRCUIT DICE INTENDED FOR USE IN THIS DEVICE TO PROVIDE A MORE SUBSTANTIAL DATA ANALYSIS BASE. o THE PRESENCE OF A BIMODAL FAILURE DISTRIBUTION WOULD INDICATE A RELIABILITY IMPROVEMENT IS POSSIBLE WITH A PRECONDITIONING SCREENING TEST.
772926	OPERATIONAL AMPLIFIER	1	o THE ZERO VOLT TEST CELL PRODUCED ONLY TWO MARGINAL FAILURES, INDICATING A HIGH STORAGE RELIABILITY POTENTIAL. o THE FAILURES INDUCED UNDER VOLTAGE STRESS CONDITIONS PROVIDE FAILURE RATES WHICH CORROBORATE THE HIGH STORAGE RELIABILITY POTENTIAL. o THE DEVICE DEMONSTRATED A VOLTAGE SENSITIVITY, INDICATING A RELIABILITY IMPROVEMENT CAN BE REALIZED WHEN OPERATED UNDER REDUCED VOLTAGE STRESS. o FAILURES INDUCED UNDER A VOLTAGE STRESS CONDITION INDICATED A BIMODAL FAILURE DISTRIBUTION.	o THE PRESENCE OF A BIMODAL FAILURE DISTRIBUTION WOULD INDICATE A RELIABILITY IMPROVEMENT IS POSSIBLE WITH A PRECONDITIONING SCREENING TEST.

FIGURE 5-1 CONCLUSIONS AND RECOMMENDATIONS (CONT. NEXT PAGE)

DEVICE SCD NO.	ITEM	CATEGORY	CONCLUSIONS	RECOMMENDATIONS
773051	VOLTAGE REGULATOR	1	o NO FAILURES WERE ENCOUNTERED IN THE ZERO VOLT TEST CELL, INDICATING THIS DEVICE HAS A HIGH STORAGE RELIABILITY POTENTIAL. o THE FAILURES INDUCED UNDER VOLTAGE STRESS CONDITIONS PROVIDE FAILURE RATES WHICH CORROBORATE THE HIGH STORAGE RELIABILITY POTENTIAL. o FAILURES INDUCED UNDER A VOLTAGE STRESS CONDITION INDICATED A LOGNORMAL BIMODAL FAILURE DISTRIBUTION.	o THE PRESENCE OF A BIMODAL FAILURE DISTRIBUTION WOULD INDICATE A RELIABILITY IMPROVEMENT IS POSSIBLE WITH A PRECONDITIONING SCREENING TEST.
772928	LOW POWER SWITCH	1	o THIS PARTICULAR LOT OF BEAM LEAD TRANSISTORS IS NOT CAPABLE OF RELIABLE PERFORMANCE AT SPECIFIED MAXIMUM STORAGE AND JUNCTION TEMPERATURES. o GAIN (h_{FE1}) DEGRADATION WAS EXPERIENCED USING TEMPERATURE ONLY AS AN ACCELERATOR. o AVALANCHING THE EMITTER BASE JUNCTION CAUSES GAIN TO REVERT (INCREASE) TO PRETEST VALUES. o ANY ELECTRICAL TEST WHICH REVERSE BIASES THE BASE EMITTER JUNCTION CAUSES THE GAIN TO INCREASE. o NO "FREAK" POPULATION IS EVIDENT.	o ADDITIONAL TESTING SHOULD BE ACCOMPLISHED TO DETERMINE EXTENT OF LOT TO LOT h_{FE} VARIABILITY. o A LOT SAMPLING TEST FOR PRODUCTION PARTS (200°C FOR 100 HOURS) WOULD QUICKLY REVEAL IF THIS GAIN DEGRADATION MECHANISM IS PRESENT - AVOID ANY ELECTRICAL TEST WHICH REVERSE BIASES THE EMITTER BASE JUNCTION DURING THIS EVALUATION.

FIGURE 5-1 CONCLUSIONS AND RECOMMENDATIONS (CONT.)

DEVICE SCD NO.	ITEM	CATEGORY	CONCLUSIONS	RECOMMENDATIONS
772929	LOW POWER AMPLIFIER	2	o THIS BEAM LEAD TRANSISTOR WILL EXPERIENCE GAIN (h_{FE}) DEGRADATION AS A FUNCTION OF TIME AND TEMPERATURE; HOWEVER, THE SLOW DEGRADATION RATE FOR THIS PARTICULAR LOT OF PARTS INDICATES A GOOD STORAGE RELIABILITY POTENTIAL AT TEMPERATURES BELOW 100°C. o THE TRANSISTOR HAS A SPECIFIED MAXIMUM STORAGE OR JUNCTION TEMPERATURE OF 200°C. SIGNIFICANT GAIN DEGRADATION IS PROJECTED AT TEMPERATURES BETWEEN 150°C AND 200°C. o THE USE OF EXTRAPOLATION TECHNIQUES TO PREDICT FAILURE TIMES RESULTS IN A CONSERVATIVE PREDICTION OF STORAGE RELIABILITY.	o ADDITIONAL TESTING SHOULD BE ACCOMPLISHED TO VERIFY LOT TO LOT h_{FE} REPEATIBILITY. o PRODUCTION LOT SAMPLE TESTING (225°C, 100 HRS) WILL PROVIDE A GOOD MONITOR FOR GAIN DEGRADATION. (E.G., >10% h_{FE} DEGRADATION WOULD INDICATE ATYPICAL RESPONSE BASED ON OBSERVED RESULTS). o THE SPECIFIED MAXIMUM STORAGE TEMPERATURE OF 200°C SHOULD BE RE-EVALUATED. THE TEST PROGRAM RESULTS WOULD SUGGEST A LOWER TEMPERATURE.
773052	NPN LOW POWER AMPLIFIER	1	o THIS TRANSISTOR WILL EXPERIENCE GAIN (h_{FE}) DEGRADATION AS A FUNCTION OF TIME AND TEMPERATURE; HOWEVER, THE RELATIVELY SLOW DEGRADATION RATE FOR THIS PARTICULAR LOT OF PARTS INDICATES A GOOD STORAGE RELIABILITY POTENTIAL. o THE TEST INDUCED FAILURES EXHIBITED A DISTINCT LOGNORMAL BIMODAL FAILURE DISTRIBUTION. o THE ENTIRE LOT WAS CONTAMINATED WITH MOBILE IONS IN THE OXIDE. o 15% OF THE TEST PARTS CONTAINED A COLLECTOR TO EMITTER PIPE AS A RESULT OF SOME BULK DEFECT. o SOME DIE BONDS EXHIBITED MARGINAL STRENGTH AFTER THE ACCELERATED LIFE TESTS. o THIS TRANSISTOR HAS A SPECIFIED MAXIMUM STORAGE TEMPERATURE OF 200°C. THE FREAK POPULATION (10% OF TOTAL PARTS) HAS MARGINAL STORAGE LIFE AT TEMPERATURES ABOVE 150°C.	o ADDITIONAL TESTING SHOULD BE ACCOMPLISHED TO VERIFY LOT TO LOT h_{FE} REPEATIBILITY.

FIGURE 5-1 CONCLUSIONS AND RECOMMENDATIONS (CONT.)

DEVICE SCD NO.	ITEM	CATEGORY	CONCLUSIONS	RECOMMENDATIONS
772931	N CHANNEL FET	1	o THE STORAGE TEST CELL EXPERIENCED ONLY TWO FAILURES, INDICATING A HIGH STORAGE RELIABILITY POTENTIAL FOR THIS BEAM LEAD FIELD EFFECT TRANSISTOR. THIS WAS CORROBORATED BY FAILURE RATES CALCULATED UNDER OPERATIONAL (VOLTAGE) CONDITIONS. o FAILURES INDUCED UNDER A VOLTAGE STRESS CONDITION INDICATED A LOGNORMAL BIMODAL FAILURE DISTRIBUTION.	o THE PRESENCE OF A BIMODAL FAILURE DISTRIBUTION WOULD INDICATE A RELIABILITY IMPROVEMENT IS POSSIBLE WITH A PRECONDITIONING SCREENING TEST.
773056-20	TANTALUM CHIP CAPACITOR	1	o THIS CAPACITOR WILL EXPERIENCE DIELECTRIC DEGRADATION IN A STORAGE ENVIRONMENT; HOWEVER, THIS DEGRADATION (MANIFESTED BY HIGH LEAKAGE CURRENT) MAY RECOVER UPON VOLTAGE APPLICATION. o FAILURE DATA SHOWED A VERY GOOD FIT TO WEIBULL DISTRIBUTION. o A SMALL (1.7%) "FREAK" POPULATION WAS PRESENT. o THIS CAPACITOR SHOULD BE CONSIDERED MARGINAL FOR EXTENDED STORAGE AT TEMPERATURES ABOVE 75°C.	o A LOT SAMPLING TEST (1000 HOURS AT 175°C) SHOULD BE INVESTIGATED TO ESTABLISH CRITERIA FOR DETECTING MARGINAL LOTS. THIS WOULD ALSO PROVIDE ADDITIONAL "FREAK" POPULATION INFORMATION TO FURTHER ASSESS THE NEED FOR A 100% SCREENING TEST.
773057-18	CERAMIC AXIAL LEAD CAPACITOR	1	o INDUCED FAILURES AT TEMPERATURES ABOVE 150°C MAY BE RESULT OF OVERSTRESS CONDITION. o FAILURE DATA SHOWED A GOOD FIT TO WEIBULL DISTRIBUTION. o NO FREAK POPULATION IS EVIDENT. o THIS CAPACITOR SHOULD HAVE A HIGH STORAGE RELIABILITY POTENTIAL.	o NONE

FIGURE 5-1 CONCLUSIONS AND RECOMMENDATIONS (CONT.)

DEVICE SCD NO.	ITEM	CATEGORY	CONCLUSIONS	RECOMMENDATIONS
773058-39	HIGH SELF-RESONANT FREQUENCY INDUCTOR CHIP	1	o INSULATION DIFFUSION WAS A FUNCTION OF THE TIME AND TEMPERATURE AND DISPLAYED A LOGNORMAL FAILURE DISTRIBUTION. o THIS PARTICULAR LOT OF PARTS PROVIDES AN ACCEPTABLE STORAGE RELIABILITY AT TEMPERATURES UP TO 100°C; HOWEVER, THIS LOT IS MARGINAL FOR OPERATION OR STORAGE AT >100°C (SPECIFIED PART LIMIT IS 125°C).	o LOT TO LOT VARIABILITY OF THE INSULATION DIFFUSION FAILURE SHOULD BE INVESTIGATED TO ESTABLISH NEED AND CRITERIA FOR A LOT SAMPLING TEST.
773059	FERRITE BEAD INDUCTOR	1	o INSULATION DIFFUSION WAS A FUNCTION OF TIME AND TEMPERATURE AND DISPLAYED A LOGNORMAL FAILURE DISTRIBUTION. o THIS PARTICULAR LOT OF PARTS PROVIDES AN ACCEPTABLE STORAGE RELIABILITY AT TEMPERATURES UP TO 100°C; HOWEVER, OBSERVED DEGRADATION AT 125°C (SPECIFIED PART LIMIT) WOULD INDICATE THE LOT IS MARGINAL.	o LOT TO LOT VARIABILITY OF THE INSULATION DIFFUSION FAILURE MECHANISM SHOULD BE INVESTIGATED TO ESTABLISH NEED AND CRITERIA FOR A LOT SAMPLING TEST.
773060-300	CERAMIC CHIP RESISTOR	2	o THIS RESISTOR DISPLAYED A POSITIVE TEMPERATURE DRIFT AS A FUNCTION OF TIME AND TEMPERATURE. o EXTRAPOLATION OF FAILURE TIMES ALLOWED A CONSERVATIVE ESTIMATE OF WHAT IS CONSIDERED AN ACCEPTABLE STORAGE RELIABILITY.	o A HIGH TEMPERATURE (200°C) SAMPLING TEST SHOULD BE INVESTIGATED TO ASSESS LOT TO LOT VARIABILITY.
773207	SPECIAL HYBRID SUBSTRATE	1	o DEPOSITED RESISTORS DEMONSTRATED GOOD STABILITY AS A FUNCTION OF TIME AND TEMPERATURE.	o NONE

FIGURE 5-1 CONCLUSIONS AND RECOMMENDATIONS (CONT.)

DEVICE SCD NO.	ITEM	CATEGORY	CONCLUSIONS	RECOMMENDATIONS
773053	HIGH CURRENT SWITCH	3	o INSUFFICIENT FAILURES WERE ENCOUNTERED TO ALLOW FAILURE DISTRIBUTION/FAILURE RATE ANALYSIS. o INTERNAL LEAD SHORTING, OBSERVED IN TWO FAILURES, INDICATED A POTENTIALLY MARGINAL LEAD DRESS CONFIGURATION. o THIS DEVICE DEMONSTRATED A HIGH STORAGE RELIABILITY POTENTIAL. HOWEVER, THE MARGINAL LEAD DRESS CONFIGURATION MUST BE FULLY ASSESSED IF THIS POTENTIAL IS TO BE REALIZED.	o A POTENTIALLY MARGINAL LEAD DRESS CONFIGURATION WAS OBSERVED IN THIS PART. ADDITIONAL TEMPERATURE EVALUATIONS ARE RECOMMENDED FOR THIS DESIGN TO ASSESS THE NEED FOR DESIGN CHANGES. AND/OR A LOT SCREENING TEST.
772921 M38510/ 01404 M38510/ 00303 785072 772932 773054-21 773055-6	QUAD 2-INPUT NAND GATE DUAL 4-INPUT MULTIPLEXER QUAD 2-INPUT NAND BUFFER 60 GATE RAYPACK CHIP GENERAL PURPOSE SWITCH PORCELAIN CHIP CAPACITOR CERAMIC CHIP CAPACITOR	3	o INSUFFICIENT FAILURES WERE ENCOUNTERED TO ALLOW FAILURE DISTRIBUTION/FAILURE RATE ANALYSIS. o NO OBVIOUS PARAMETER DEGRADATION TREND WAS OBSERVED. o THESE DEVCIES SHOULD HAVE A HIGH STORAGE RELIABILITY POTENTIAL.	o NONE

FIGURE 5-1 CONCLUSIONS AND RECOMMENDATIONS (CONT.)

6.0 REFERENCES

[1] G. M. Johnson, "Evaluation of Microcircuit Accelerated Test Techniques", RADC-TR-218, page 88, July 1976.

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[5] D. S. Peck, "The Analysis of Data from Accelerated Stress Tests", Proceedings 9th Annual Reliability Physics Symp., pp. 68-83, 1971.

[6] F. H. Reynolds, "Thermally Accelerated Aging of Semiconductor Components", Proceedings of the IEEE, Vol. 62, pp. 212-222, February, 1974.

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[8] Wayne Nelson, "Analysis of Accelerated Life Test Data", IEEE Transactions on Electrical Insulation", Part I, Dec, 1971; Part II, March, 1972; and Part III, June, 1972.

[9] P. G. Hoel, "Introduction to Mathematical Statistics", John Wiley and Sons, N.Y., 1971.

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[11] M. Stitch, "High Temperature Operating Tests (HTOT), A Control For Contaminated Microcircuit Processes", Proceedings 13th Annual Reliability Physics Symp., pp. 260-262, 1975.

APPENDIX A

P/N 772921

QUAD 2-INPUT NAND GATE

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A1.0 PART DESCRIPTION

The Quad, 2-Input NAND Gate, P/N 772921, a generic type 5400, is a beam lead monolithic integrated circuit intended for hybrid circuit application. The beam lead die, manufactured by the Raytheon Company, Semiconductor Division, was specially packaged by the Raytheon Missile Systems Division in a hermetic 16 pin dual-in-line package (DIP) for this storage reliability test program.

The Acceptance Test record accompanying the parts noted that some of the DIP packages contained microcracks, Figure A1, which had been induced during the fine and gross leak tests. The packages could not withstand the necessary bomb pressure for these leak tests. Therefore, subsequent leak testing was restricted to a non-pressurized fluorocarbon bubble gross leak test during Acceptance Tests at Raytheon.

Due to the potentially severe temperature cycling effects which these devices would experience in the test program, preliminary testing of the packages was accomplished. Sixteen of these devices and twelve operational amplifiers, P/N 772926, which had the same problem (reference Appendix "F"), were subjected to the hermeticity evaluation described in Table A1. Sixteen temperature cycles, laboratory ambient to 250°C, simulated the thermal cycles the parts would experience in the life test. The results indicated that loss of hermeticity could be expected to occur during the test program. However, the lack of suitable replacement parts resulted in the decision to use this lot of parts in the accelerated life test. It should be pointed out that none of the failures which were generated during the accelerated life test could be associated with a package hermeticity problem.

A2.0 CONSTRUCTION ANALYSIS

Table A2 summarizes the physical details of the test configuration part, while Figures A2, A3 and A4 offer visual details and a schematic diagram of the device. Typical beam lead bonds are pictured in Figure A5. This device contains no materials which would restrict testing below 300°C.

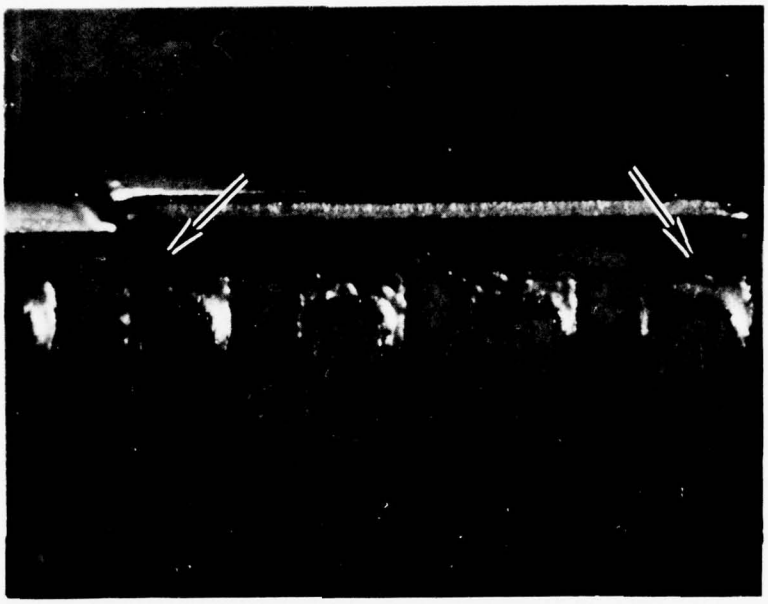

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FIGURE A1. DIP PACKAGE MICROCRACKS - P/N 772921 - QUAD 2-INPUT NAND GATE

TABLE A1. HERMETICITY EVALUATION - P/N 772921 AND P/N 772926

OBJECTIVE - EVALUATE THE HERMETIC INTEGRITY FOR "CRACKED" AND "NON-CRACKED" 16 PIN DIP PACKAGES UNDER SIMULATED LIFE TEST TEMPERATURE CYCLING CONDITIONS.

TEST PROFILE - 16 TEMPERATURE CYCLES (AMBIENT TO 250°C, ONE HOUR AT EACH CONDITION) - PERFORM ELECTRICAL TEST AND HERMETICITY TEST (IMMERSION, 125°C FLUROCARBON, OBSERVE FOR BUBBLES) - VISUAL EXAMINATION.

TEST RESULTS

PART NO.	QUANTITY TESTED AND INITIAL CONDITION	ELECTRICAL	HERMETICITY	COMMENTS
772921	9 - CRACKED PARTS (PASSED HERMETICITY TEST)	1 FAILURE (1) (POST 12 CYCLES)	1 FAILURE (POST 4 CYCLES - CERAMIC)	(1) HIGH I_{IH1} VERIFIED NO VISIBLE CAUSE OF FAILURE.
	4 - CRACKED PARTS (FAILED HERMETICITY TEST)	NO FAILURES	NOT TESTED	
	3 - NO CRACKS (PASSED HERMETICITY TEST)	NO FAILURES	NO FAILURES	FOUR PARTS DECAPPED - NO VISIBLE SIGN OF MOISTURE
772926	8 - CRACKED PARTS (PASSED HERMETICITY TEST)	1 FAILURE (POST 8 CYCLES - MARGINAL FROM BEGINNING)	3 FAILURES (1 - POST 4 CYCLES - LID) (2 - POST 12 (CYCLES - CERAMIC)	NO CONTAMINATION NOTED
	4 - NO CRACKS (PASSED HERMETICITY TEST)	1 FAILURE (POST 8 CYCLES - NOT RELATED TO HERMETICITY)	NO FAILURES	FAILURE NOT ANALYZED

TABLE A2. PART CONSTRUCTION DETAILS - P/N 772921 - QUAD 2-INPUT NAND GATE

A. IDENTIFICATION

1. Part Name: Quad 2-Input NAND Gate (5400)
2. Part Manufacturer: Raytheon Co., Semiconductor Division
3. Part Number: 772921
4. Date Code: None

B. PACKAGE

1. Type: 16-Pin Ceramic Dual-In-Line Package (Drawing No. 757437)
2. Weight: 1.26 grams
3. Material:

   a) Lid: Kovar, gold-plated
   b) Leads: Gold-plated Kovar which is braze welded to a refractory metal feedthru. The refractory metal is gold-plated in the internal area of the package.
   c) Seals: The lid is brazed to the lid frame and the seal around the leads is fired ceramic.

C. INTERNAL GEOMETRY

1. Interconnections: Beam leads bonded to gold-plated refractory metal conductors.

2. Die:

   a) Type: Silicon, planar (beam lead)
   b) Scribe Method: Etch
   c) Die Dimensions: .044 inch x .033 inch
   d) Passivation: Silicon Nitride over Silicon Dioxide

3. Metallization:

   a) Type: Gold/Titanium/Platinum
   b) Metallization Layers: One

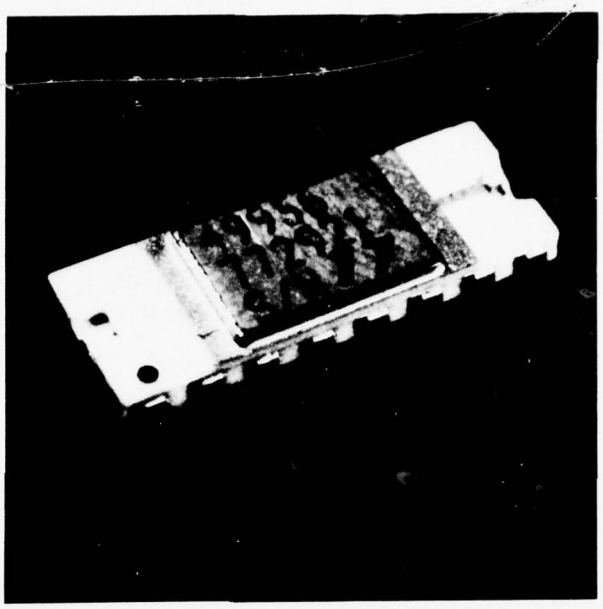

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FIGURE A2. EXTERNAL CONSTRUCTION - P/N 772921 - QUAD 2-INPUT NAND GATE

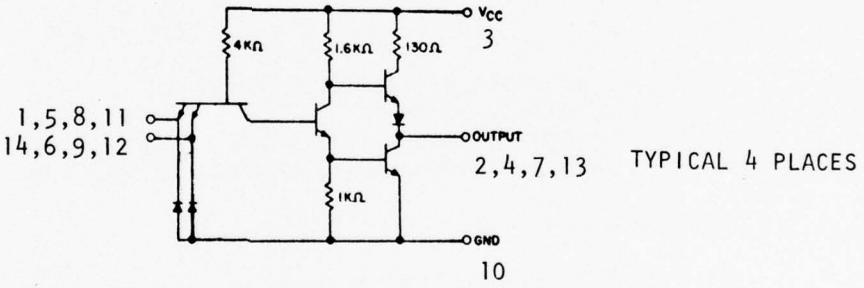
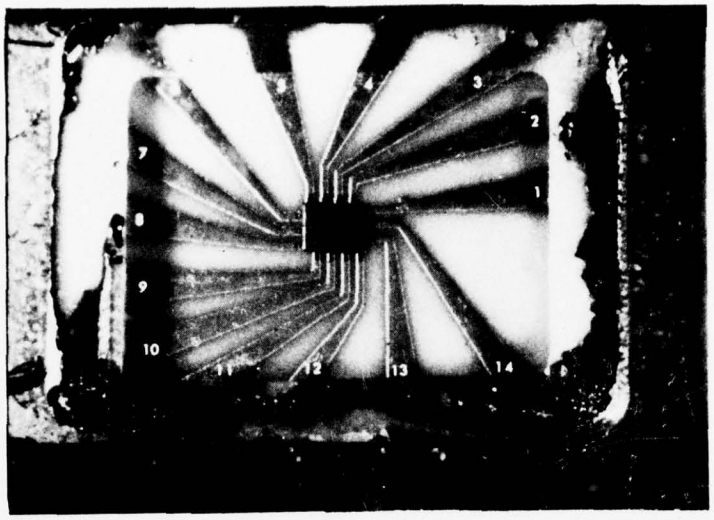


FIGURE A3. SCHEMATIC DIAGRAM - P/N 772921 - QUAD 2-INPUT NAND GATE



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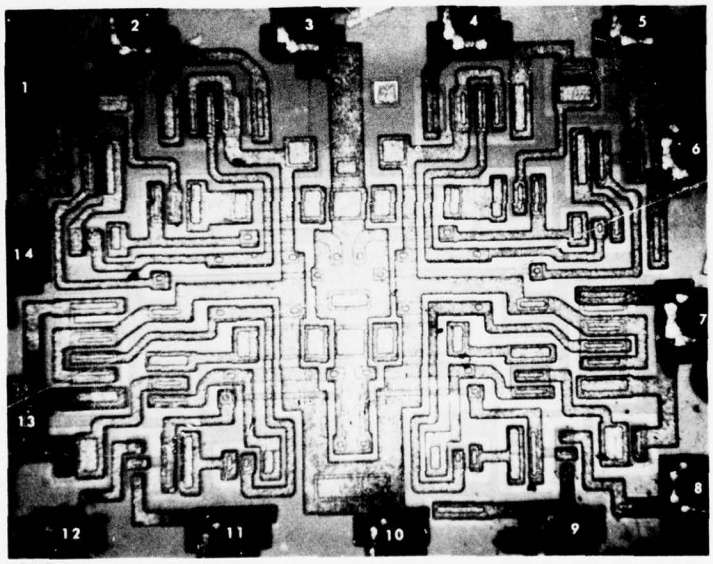
VIEW WITH LID REMOVED



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DIE TOPOGRAPHY

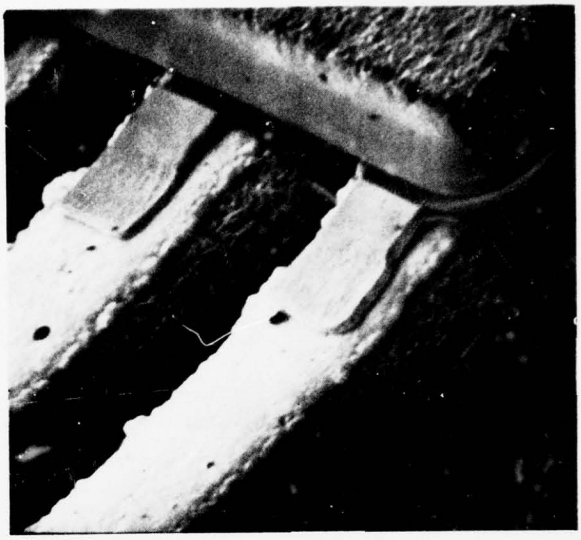
FIGURE A4. INTERNAL CONSTRUCTION DETAILS - P/N 772921 - QUAD 2-INPUT NAND GATE

STORAGE RELIABILITY
OF MISSILE MATERIEL

REPORT MDC E1601
29 APRIL 1977

B1.0 PART DESCRIPTION

39X (SEM)



150X (SEM)

300X (SEM)

210X (SEM)

FIGURE A5. BEAM LEAD BONDS - P/N 772921 - QUAD 2-INPUT NAND GATE

STORAGE RELIABILITY
OF MISSILE MATERIEL

REPORT MDC E1601
29 APRIL 1977

The typical SAM-D configuration, Figure A6, has the die beam lead bonded to gold-plate metallization deposited on a ceramic substrate.

A3.0 ELECTRICAL TEST CRITERIA

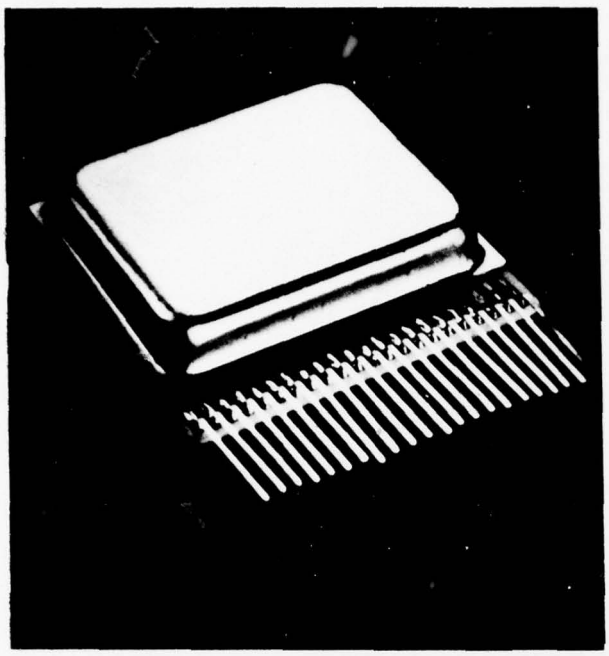
All D.C. electrical tests required by 772921, plus the input clamp voltage (V_{IC}) for each input, as summarized in Table A3, comprise the electrical tests for this device.

A4.0 BIAS CIRCUIT ANALYSIS

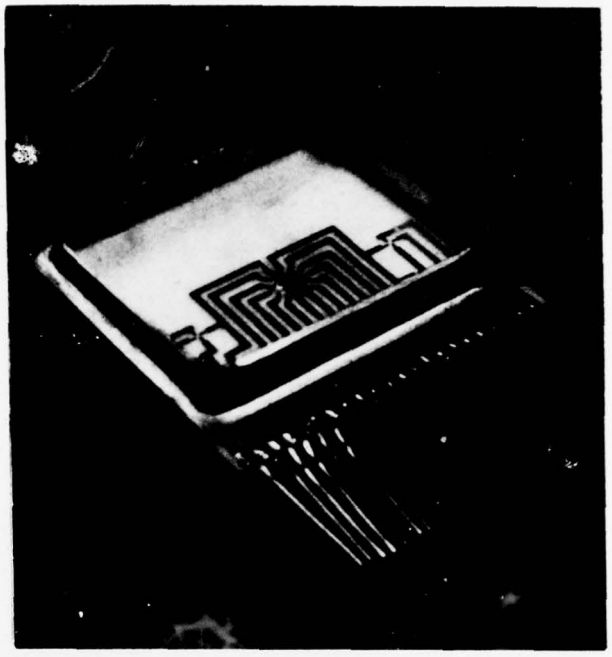
Bias circuit evaluation was facilitated by previous MDAC-EAST experience with similar parts [A1][A2]. Two bias circuits, shown in Figure A7, offering variations of high and low inputs were investigated. Bias circuit 1 had three gates with one high and one low input, and one gate with both inputs high. Bias circuit 2 had two gates with one high and one low input, one gate with both inputs high, and one gate with both inputs low.

Both bias circuits remained thermally stable at an ambient temperature of 250°C with a device voltage (V_{CC}) of 5.0 volts and experienced thermal runaway at 275°C. Neither bias circuit could be operated in an ambient temperature of 250°C with a supply voltage of 5.25 volts without being dangerously close to thermal runaway. Plots of supply current versus ambient temperature for both bias circuits and supply current as a function of supply voltage at specific ambient temperatures for bias circuit 2 are provided in Figure A7. Current densities were sufficiently low to preclude electromigration failures within the life test duration.

Bias circuit 2 was selected as the candidate life test circuit because it drew less current at the higher temperatures and optimized gate biasing conditions. Maximum test conditions of 5.0 volts applied bias and 250°C ambient temperature were tentatively selected for the accelerated life test and were the conditions used in the step stress test. A 40 ohm current limiting resistor was selected to preclude catastrophic damage in the event of device failure.



1.9X



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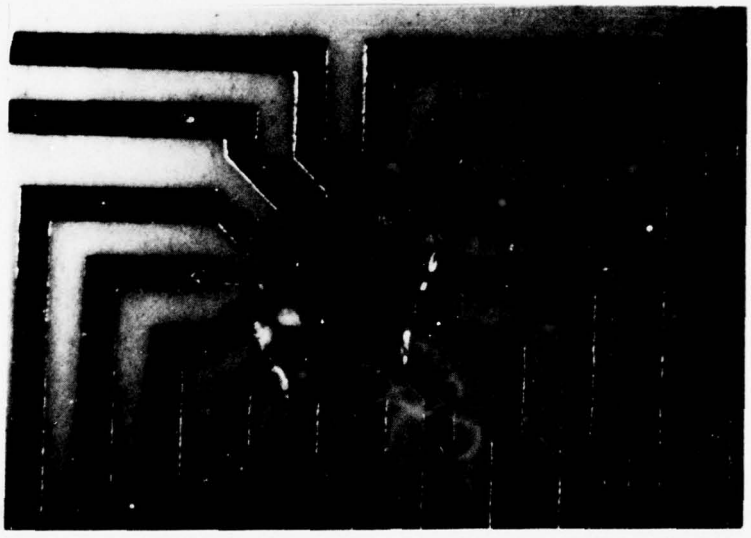
EXTERNAL

INTERNAL



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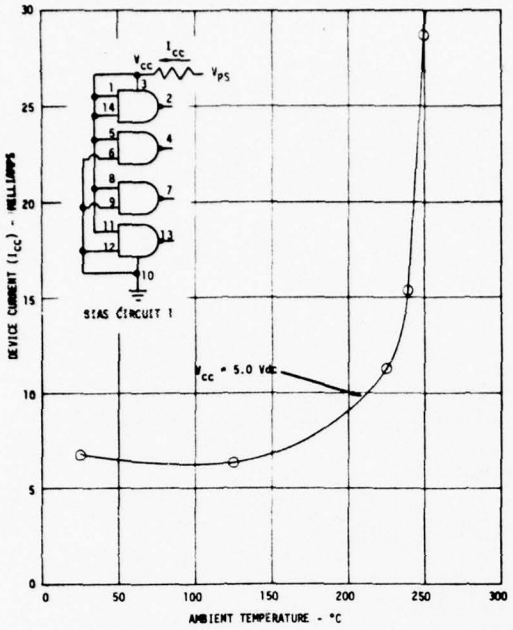
DIE MOUNTED IN SAM-D CONFIGURATION

FIGURE A6. TYPICAL SAM-D CONFIGURATION - P/N 773351 - QUAD 2-INPUT NAND GATE

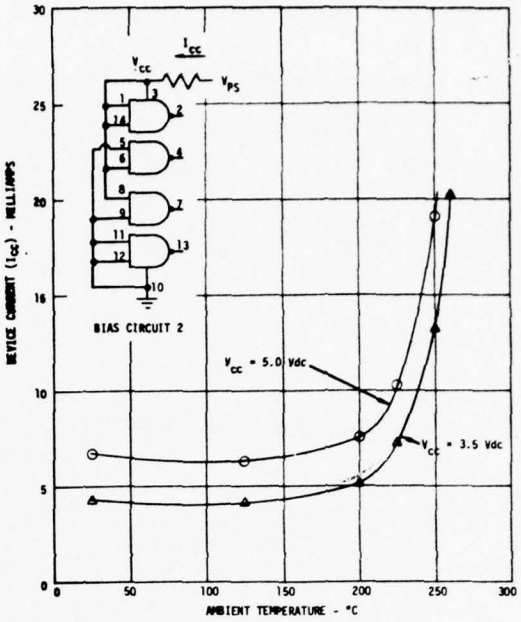
TABLE A3. ELECTRICAL TEST CONDITIONS - P/N 772921 - QUAD 2-INPUT NAND GATE

Symbol	MIL-STD-883 Method	16 PIN DIP Test No.	1A	1	2	3	4	5	6	7	8	9	10	11	12	13	Meas. PIN	Test Limits Min	Max	Units
V_{OL}	3007	1	2.0v	2.0v	16mA	4.5v		4.5v	4.5v		4.5v	4.5v	GND	4.5v	4.5v		2		.4	V
V_{OL}		2	4.5v	4.5v			16mA	2.0v	2.0v		4.5v	4.5v					4		.4	V
V_{OL}		3						4.5v	4.5v	16 mA	2.0v	2.0v					7		.4	V
V_{OL}		4						4.5v	4.5v		4.5v	4.5v		2.0v	2.0v	16mA	13		.4	V
V_{OH}	3006	5	.8v	4.5v	-.4mA			4.5v	4.5v		4.5v	4.5v		4.5v	4.5v		2	2.4		V
V_{OH}		6	4.5v	.8v	-.4mA			4.5v	4.5v		4.5v	4.5v		4.5v	4.5v		2	2.4		V
V_{OH}		7	4.5v	4.5v			-.4mA	.8v	4.5v								4	2.4		V
V_{OH}		8					-.4mA	4.5v	.8v			4.5v					4	2.4		V
V_{OH}		9							4.5v	-.4mA	.8v	4.5v					7	2.4		V
V_{OH}		10								-.4mA	4.5v	.8v					7	2.4		V
V_{OH}		11										4.5v		.8v	4.5v	-.4mA	13	2.4		V
V_{OH}		12										4.5v		4.5v	.8v	-.4mA	13	2.4		V
I_{OS}	3011	13	GND	GND	GND	5.5v											2	-20	-55	mA
I_{OS}		14					GND	GND	GND								4	-20	-55	mA
I_{OS}		15								GND	GND	GND					7	-20	-55	mA
I_{OS}		16												GND	GND	GNr	13	-20	-55	mA
I_{IH1}	3010	17	2.4v	GND				GND	GND		GND	GND		GND	GND		14		40	µA
I_{IH1}		18	GND	2.4v				GND									1		40	µA
I_{IH1}		19		GND				2.4v									5		40	µA
I_{IH1}		20						GND	2.4v								6		40	µA
I_{IH1}		21							GND		2.4v						8		40	µA
I_{IH1}		22									GND	2.4v					9		40	µA
I_{IH1}		23										GND		2.4v			11		40	µA
I_{IH1}		24												GND	2.4V		12		40	µA
I_{IH2}		25	5.5v												GND		14		1000	µA
I_{IH2}		26	GND	5.5v													1		1000	µA
I_{IH2}		27		GND				5.5v									5		1000	µA
I_{IH2}		28						GND	5.5v								6		1000	µA
I_{IH2}		29							GND		5.5v						8		1000	µA
I_{IH2}		30									GND	5.5v					9		1000	µA
I_{IH2}		31										GND		5.5v			11		1000	µA
I_{IH2}		32												GND	5.5v		12		1000	µA
I_{IL}	3009	33	0.4v	4.5v				4.5v	4.5v		4.5v	4.5v		4.5v	4.5v		14		-1.6	mA
I_{IL}		34	4.5v	0.4v				4.5v	4.5v								1		-1.6	mA
I_{IL}		35	4.5v	4.5v				0.4v	4.5v								5		-1.6	mA
I_{IL}		36						4.5v	0.4v								6		-1.6	mA
I_{IL}		37							4.5v		0.4v	4.5v					8		-1.6	mA
I_{IL}		38									4.5v	0.4v					9		-1.6	mA
I_{IL}		39										4.5v		0.4v	4.5v		11		-1.6	mA
I_{IL}		40												4.5v	0.4v		12		-1.6	mA
I_{CCH}	3005	41	GND	GND		5.5v		GND	GND		GND	GND	GND	GND	GND		3		8	mA
I_{CCL}	3005	42	5.0v	5.0v		5.5v		5.0v	5.0v		5.0v	5.0v		5.0v	5.0v		3		22	mA
V_{IC}		43	-12mA			4.5v											14		F	V
		44		-12mA													1		0	
		45						-12mA									5		R	
		46							-12mA								6			
		47									-12mA						8		I	
		48										-12mA					9		N	
		49												-12mA			11		F	
		50													-12mA		12		0	

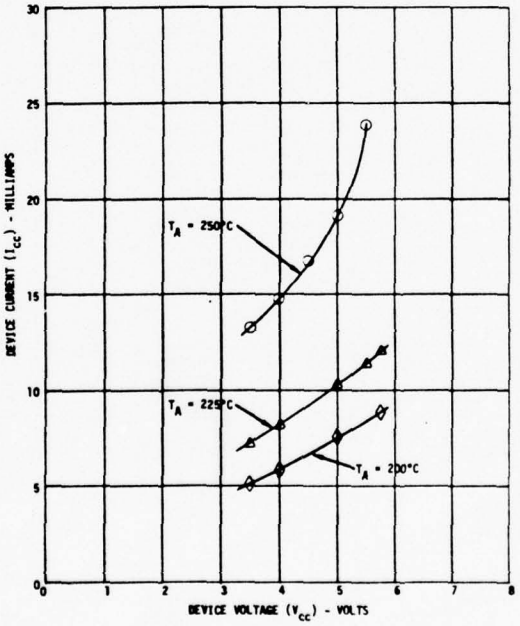
Initial and final test conducted at +25°C and +125°C. Interim test conducted at +25°C.



BIAS CIRCUIT 1



BIAS CIRCUIT 2



BIAS CIRCUIT 2

FIGURE A7. BIAS CIRCUIT EVALUATION - P/N 772921 - QUAD 2-INPUT NAND GATE

A5.0 STEP STRESS TEST RESULTS

A step stress test was conducted on twenty test devices utilizing bias circuit 2 with V_{CC} equal to 5.0 volts. Four sixteen hour steps, Figure A8, starting at 175°C and concluding at 250°C, generated no failures, and were concluded with no anomalous conditions. Therefore, the test conditions were considered acceptable for the accelerated life test program.

A6.0 LIFE TEST CONDITION AND RESULTS

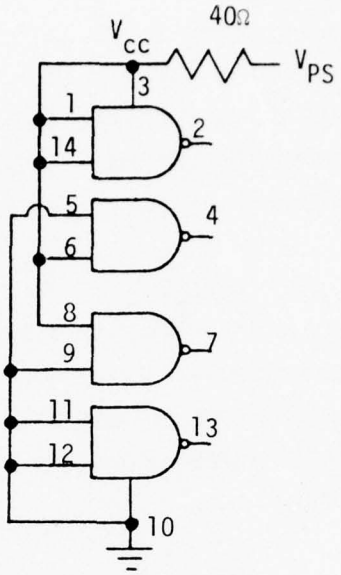
The accelerated life test conditions for this device are summarized in Figure A8. The Table A4 life test summary reveals the life tests lasted the full 4000 hours, producing only five device failures or less than 4% of the devices in the life test. The test failures were spread among the three 250°C cells, each having a different V_{CC}, including zero.

A7.0 FAILURE ANALYSIS

A summary of the failure analysis results is presented in Table A5. Three parts, two in Cell 1 and one in Cell 2, exhibited excessive I_{IH1} due to exponential leakage between pin 1 and ground. Initial curve tracer testing showed an intermittent condition, suggesting a mechanical problem. After delidding, the amount of leakage would vary intermittently if the pin 1 beam lead was nudged with a probe, and in each instance the leakage disappeared when the die was removed from the package by cutting the beams free. Microscopic examination disclosed no loose conductive particles or any other discrepancies. These findings indicated that the leakage probably was caused by contact between the beam and the edge of the substrate (ground). However, examinations of the die before and after removal of the beams failed to disclose where contact occurred; thus, the exact cause of failure was not determined. The pin 1 beam was wider than all other beams, apparently to accommodate the part number (5400) etched into it as shown in Figure A9. This may have contributed to the failure of pin 1, but no supportive evidence was found.

The two Cell 3 failures at 4 hours displayed negative values of I_{IH1}, one at pin 8 (-10 μA) and one at pin 5 (-22 μA). Curve tracer tests indicated that the negative I_{IH1} was due to excessive series resistance in the input stage transistor. After

STEP STRESS AND LIFE TEST CIRCUIT



STEP STRESS TEST - FAILURE SUMMARY (20 DEVICES)

AMBIENT TEMP. (°C)	V_{CC} (V)	CUMULATIVE FAILURES
175	5.0	0
200	5.0	0
225	5.0	0
250	5.0	0

LIFE TEST CONDITIONS

TEST CELL NUMBER	T_A AMBIENT TEMPERATURE (°C)	V_{CC} DEVICE VOLTAGE (VOLTS)	I_{CC} DEVICE CURRENT (MILLIAMPS)	P_d POWER DISSIPATION (MILLIWATTS)	T_J JUNCTION TEMPERATURE (°C)
1	250	5.0	19.1	96	259
2	250	3.5	13.2	46	254
3	250	0	0	0	250
4	225	5.0	10.3	52	230
5	200	5.0	7.5	38	204

FIGURE A8. STEP STRESS RESULTS AND LIFE TEST CONDITIONS - P/N 772921 - QUAD 2-INPUT NAND GATE

TABLE A4. LIFE TEST SUMMARY - P/N 772921 - QUAD 2-INPUT NAND GATE

TEST CELL DESCRIPTION				CUMULATIVE FAILURES AT HOURS OF TEST										
CELL NUMBER	APPLIED BIAS	AMBIENT TEMPERATURE	QUANTITY	4	8	16	32	64	128	256	512	1000	2504	4000
1	5 VDC	250°C	30	0	0	0	1	1	1	1	1	1	2	2*
2	3.5 VDC	250°C	30	0	0	0	0	0	0	0	0	0	1	1*
3	0 VDC	250°C	30	2	2	2	2	2	2	2	2	2	2	2*
4	5 VDC	225°C	30	0	0	0	0	0	0	0	0	0	0	0*
5	5 VDC	200°C	30	0	0	0	0	0	0	0	0	0	0	0*

* TEST TERMINATED

TABLE A5. FAILURE ANANYSIS SUMMARY - P/N 772921 - QUAD 2-INPUT NAND GATE

	A. FAILED PARAMETER OR SYMPTOMS	QUANTITY OF FAILURES AND TIME OF FAILURE				
	B. FAILURE MODE	250°C			225°C	200°C
	C. FAILURE MECHANISM	5V	3.5V	0V	5V	5V
	D. CAUSE OF FAILURE	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5
MECHANICAL FAILURES	A. I_{IH1} (PIN 1)	1@32	1@2504			
	B. INPUT TO GROUND LEAKAGE	1@2504				
	C. BEAM TO DIE SHORT					
	D. NOT DETERMINED					
	A. I_{IH1} (NEGATIVE)			2@4		
	B. EXCESSIVE RESISTANCE					
	C. NOT DETERMINED					
	D. NOT DETERMINED					
	TOTAL NUMBER OF FAILED PARTS	2	1	2	0	0

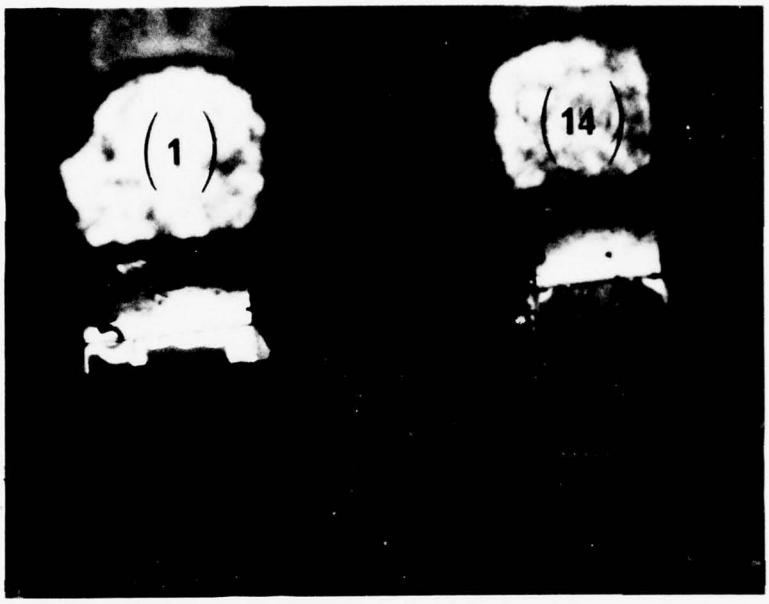


FIGURE A9. CLOSEUP OF THE WIDE BEAM (PIN 1) AND A TYPICAL BEAM (PIN 14) - P/N 772921 - QUAD 2-INPUT NAND GATE

removing the dice from the packages, the defective pins displayed normal values of I_{IH1}. This indicated that the cause of excessive series resistance was mechanical in nature, but analysis of these parts did not disclose the specific cause.

A8.0 DATA CORRELATION

Insufficient failures, Table A5, were encountered in the test program, precluding the identification of failure distributions. Although the cause of the five test failures (all I_{IH1}) could not be established, the presence of two failure modes, input to ground leakage and excessive resistance, suggests the possibility of two failure causes. The lot acceptance records accompanying the parts showed one I_{IH1} failure occurred during initial acceptance testing.

Even though the failures all occurred in the 250°C test cells, the data is inadequate to infer either a temperature or a voltage sensitivity. The parameter I_{IH1} revealed no trends during the test program. Since there were insufficient failures for data analysis, other parameter trends were investigated to establish feasibility of extrapolating times to failure. The parameters I_{IH1}, I_{IH2}, V_{IC}, I_{IL}, I_{OS}, and I_{CC} displayed good stability throughout the 4000 hour life test. The percent change from pretest values for three typical parameters, I_{IH1}, I_{OS}, and I_{CCL}, at the highest temperature and stress are shown in Figure A10 for the discrete measurement times.

The lack of test failures and the absence of parameter trends preclude the calculation of a storage failure rate; however, it appears that the beam lead chip should exhibit a high storage reliability potential ($\lambda(t)_{MAX} << 10^{-10}$ failures per hour).

A9.0 CONCLUSIONS AND RECOMMENDATIONS

- Although insufficient failures were accumulated to allow a failure rate calculation, the beam lead chip should have a high reliability potential in both storage and operating modes.
- The 16 pin DIP package (and its associated microcracks in the ceramic) did not influence the outcome of the test program.
- The five test failures appear mechanical in nature and should be applicable to a storage environment.

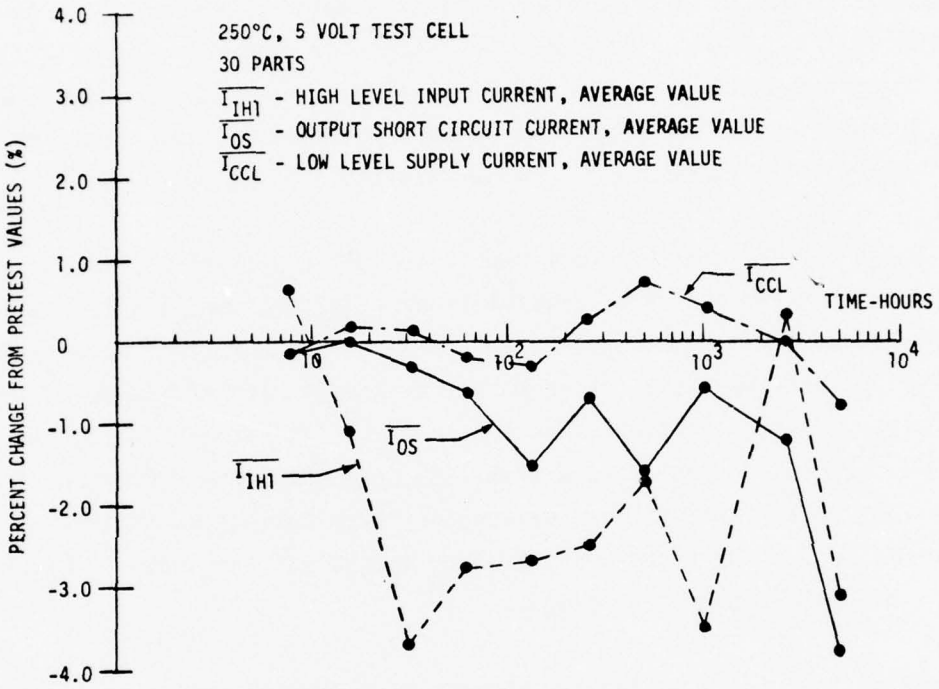


FIGURE A10. BEHAVIOR OF SELECTED PARAMETERS DURING LIFE TEST - P/N 772921 - QUAD 2-INPUT NAND GATE

A10.0 REFERENCES

[A1] G. M. Johnson, "Evaluation of Microcircuit Accelerated Test Techniques", RADC TR-76-218, July 1976.

[A2] J. J. McGarry, Jr., "Integrated Circuit Life Test Results at 300°C", presented at Government Microcircuit Applications Conference, June 1972.

APPENDIX B

P/N M38510/01404

DUAL 4-INPUT MULTIPLEXER

TABLE OF CONTENTS

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B4.0	BIAS CIRCUIT ANALYSIS.	B2
B5.0	STEP STRESS TEST RESULTS	B10
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B1.0 PART DESCRIPTION

The Dual 4-Input Multiplexer, P/N M38510/01404, is the logic implementation of a two-pole, four position switch with the switch position determined by the logic signals applied to the select inputs, pins 3 and 13. The part was manufactured by Advanced Micro Devices. This test configuration is identical to the SAM-D use configuration.

B2.0 CONSTRUCTION ANALYSIS

The pertinent physical details of the test configuration part are provided in Table B1. Figures B1, B2 and B3 are a photograph of the external construction, a logic diagram and the internal construction, respectively. The device contained no materials which limited testing below 300°C.

The typical SAM-D configuration, Figure B4, consists of a device, identical to the life test part, soldered to the metallization on a fiber glass circuit board.

B3.0 ELECTRICAL TEST CRITERIA

The electrical test criteria used to examine this part consisted of the Table III, Subgroups 1 and 7, tests for the 04 type device of M38510/014, as summarized in Table B2.

B4.0 BIAS CIRCUIT ANALYSIS

Three candidate life test bias circuits, illustrated in Figure B5, were evaluated. Data plots are shown in Figure B6. Bias circuit 1 had all of the inputs to the device connected to V_{CC}. Bias circuit 2 differed in that pins 7 and 9 were connected to ground. The supply currents of bias circuits 1 and 2 were both excessive at 200°C (potential electromigration failures). With the part at a 200°C ambient temperature the inputs were moved from V_{CC} to ground, one at a time, and the supply current decreased to a minimum when all inputs were at ground potential. This configuration (all inputs at ground potential) is bias circuit 3.

Figure B6 shows bias circuit 3 supply current versus ambient temperature for three different supply voltages. The device could not be operated in a 250°C ambient temperature with a supply voltage of 5.0 volts due to thermal runaway. Reducing

TABLE B1. PART CONSTRUCTION DETAILS - P/N M38510/01404 - DUAL 4-INPUT MULTIPLEXER

A. IDENTIFICATION

1. Part Name: Dual 4-Input Multiplexer (9309)
2. Part Manufacturer: Advanced Micro Devices
3. Part Number: M38510/01404
4. Date Code: 7403

B. PACKAGE

1. Type: 16-Lead ceramic/metal Flatpack
2. Weight: 0.469 gram
3. Materials:
   a) Lid: Kovar, gold-plated
   b) Leads: Kovar, gold-plated external and internal
   c) Lid Seal: Solder

C. INTERNAL GEOMETRY

1. Interconnections:
   a) Type: Aluminum Wire
   b) Diameter: 0.001 inch
   c) Bonds:
      1) Aluminum-Aluminum ultrasonic at the die
      2) Aluminum-Gold ultrasonic at the frame

2. Die:
   a) Type: Silicon, Planar
   b) Scribe Method: Mechanical
   c) Dimensions: 0.060 inch x 0.076 inch
   d) Attach Method: Gold eutectic
   e) Glassivation: Silicon Dioxide

3. Metallization
   a) Type: Aluminum
   b) Number of Layers: One

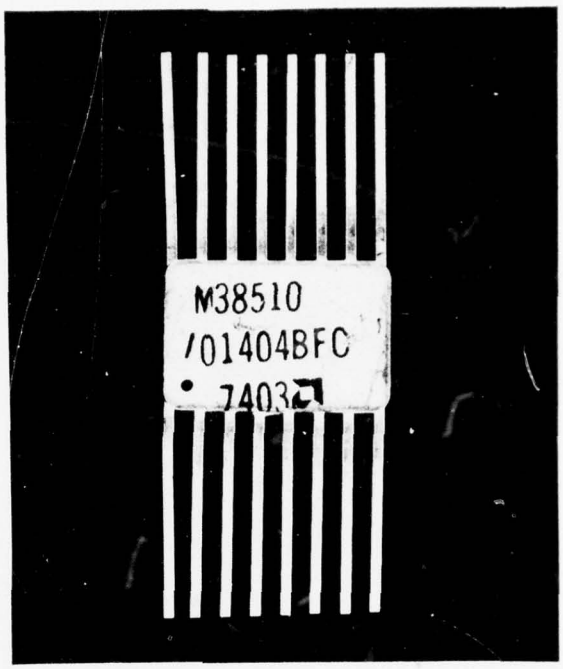

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FIGURE B1. EXTERNAL CONSTRUCTION - P/N M38510/01404 - DUAL 4-INPUT MULTIPLEXER

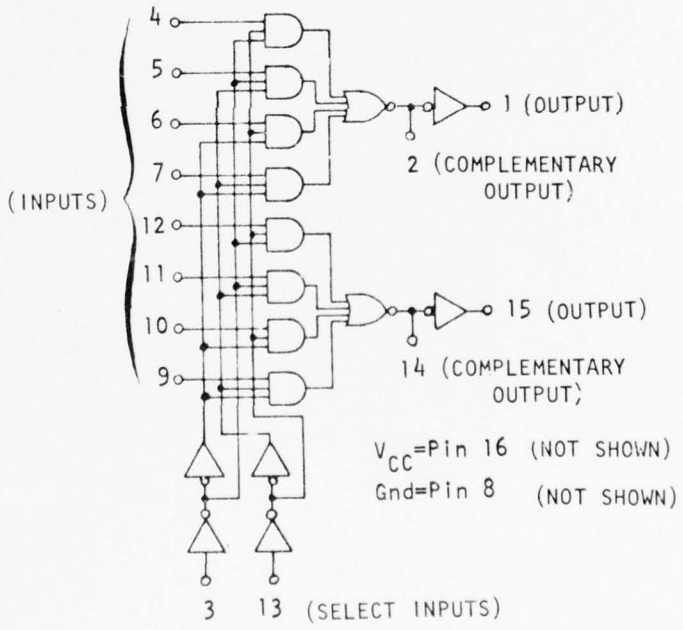
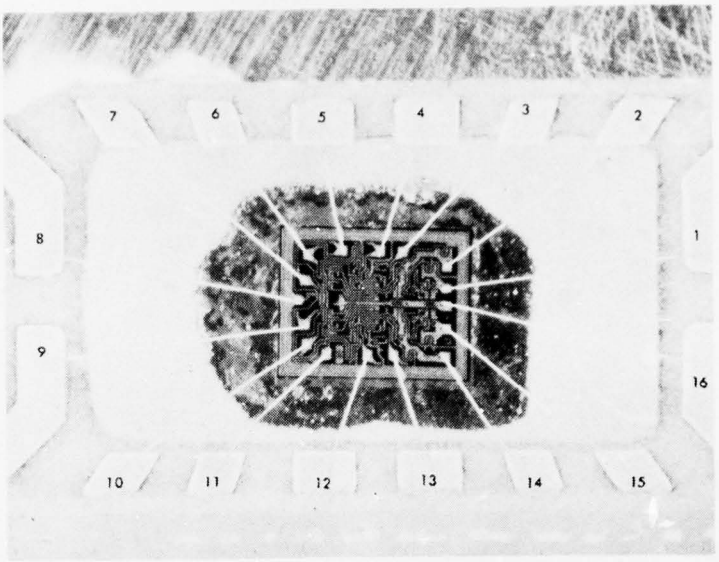


FIGURE B2. LOGIC DIAGRAM - P/N M38510/01404 - DUAL 4-INPUT MULTIPLEXER

STORAGE RELIABILITY
OF MISSILE MATERIEL

REPORT MDC E1601
29 APRIL 1977



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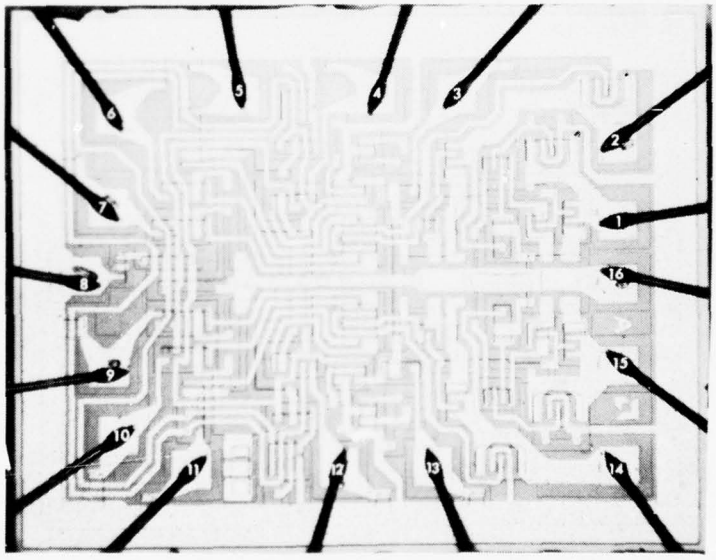
VIEW WITH LID REMOVED



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DIE TOPOGRAPHY

FIGURE B3. INTERNAL CONSTRUCTION DETAILS - P/N M38510/01404 - DUAL 4-INPUT MULTIPLEXER

STORAGE RELIABILITY
OF MISSILE MATERIEL

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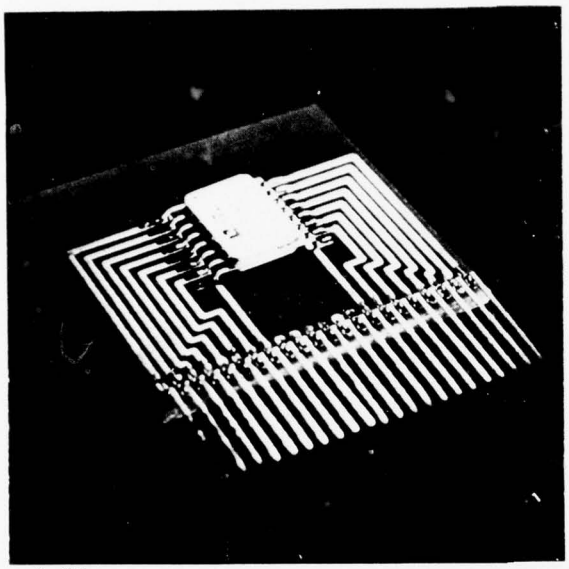

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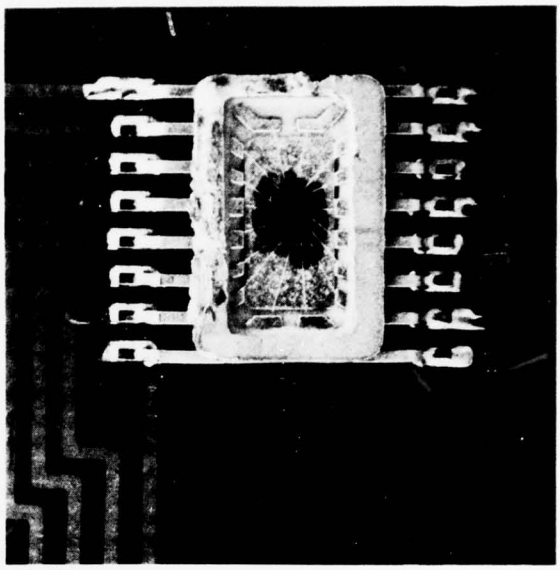
EXTERNAL



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INTERNAL

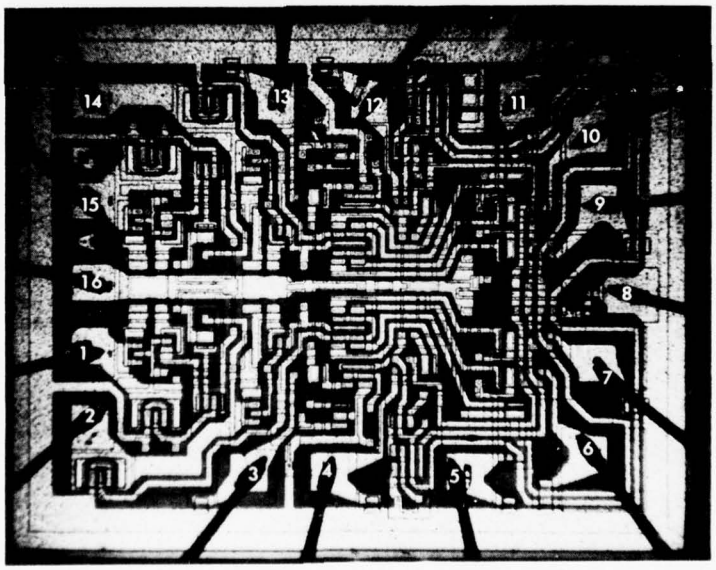

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FIGURE B4. TYPICAL SAM-D CONFIGURATION - P/N 773427 - DUAL 4-INPUT MULTIPLEXER

STORAGE RELIABILITY
OF MISSILE MATERIEL

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29 APRIL 1977

TABLE B2. ELECTRICAL TEST CONDITIONS - P/N M38510/01404 - DUAL 4-INPUT MULTIPLEXER

Symbol	MIL-STD-883 method	LEAD Test No.	1 1Y	2 1W	3 B	4 $1C_0$	5 $1C_1$	6 $1C_2$	7 $1C_3$	8 GND	9 $1C_3$	10 $1C_2$	11 $1C_1$	12 $1C_0$	13 A	14 1W	15 1Y	16 V_{CC}	Meas. terminal	Test limits Min	Max	Unit
V_{OH}	3006	1 2 3 4	-0.8mA	-0.8mA	0.8 v	2.0 v 0.8 v				GND				2.0 v 0.8 v	0.8 v	-0.8mA	-0.8mA	4.5 v	1Y 1W 2Y 2W	2.4		V
V_{OL}	3007	5 6 7 9	16 mA	16 mA		2.0 v 0.8 v								2.0 v 0.8 v		16 mA	16 mA		1W 1Y 2W 2Y		0.4	
V_{IC}		9 10 11 12 13 14 15 16 17 18			-12 mA	-12 mA	-12 mA	-12 mA	-12 mA		-12 mA	-12 mA	-12 mA	-12 mA	-12 mA				A B $1C_0$ $1C_1$ $1C_2$ $1C_3$ $2C_0$ $2C_1$ $2C_2$ $2C_3$		-1.5	
I_{IL}	3009	19 20 21 22 23 24 25 26 27 28			0.4 v GND GND 5.5 v 5.5 v GND GND 5.5 v 5.5 v	0.4 v	0.4 v	0.4 v	0.4 v		0.4 v	0.4 v	0.4 v	0.4 v	0.4 v GND 5.5 v GND 5.5 v 5.5 v GND 5.5 v GND 5.5 v			5.5 v	A B $1C_0$ $1C_1$ $1C_2$ $1C_3$ $2C_0$ $2C_1$ $2C_2$ $2C_3$	-0.7	-1.6	mA
I_{IH1}	3010	29 30 31 32 33 34 35 36 37 38			2.4 v 5.5 v 5.5 v GND GND 5.5 v 5.5 v GND GND	2.4 v	2.4 v	2.4 v	2.4 v		2.4 v	2.4 v	2.4 v	2.4 v	2.4 v 5.5 v GND 5.5 v GND 5.5 v 5.5 v GND 5.5 v GND				A B $1C_0$ $1C_1$ $1C_2$ $1C_3$ $2C_0$ $2C_1$ $2C_2$ $2C_3$	0	40	µA
I_{IH2}		39 40 41 42 43 44 45 46 47 48			5.5 v GND GND 5.5 v 5.5 v GND	5.5 v	5.5 v	5.5 v	5.5 v		5.5 v	5.5 v	5.5 v	5.5 v	5.5 v 5.5 v GND 5.5 v GND 5.5 v GND 5.5 v GND				A B $1C_0$ $1C_1$ $1C_2$ $1C_3$ $2C_0$ $2C_1$ $2C_2$ $2C_3$		100	
I_{OS}	3011	49 50 51 52	GND	GND		GND 5.5 v	GND	GND	GND		GND GND	GND GND	GND GND	GND 5.5 v		GND	GND		1W 1Y 2W 2Y	-50	-120	mA
I_{CC}	3005	53				5.5 v					GND	GND	GND	5.5 v					V_{CC}	0	45	
Truth table test		54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69	L H L H L H L H	H L H L H L H L	B A B	B A	B A	B A	B A	GND	B A	B A	B A	B A	B B A A B B A A B B A A	H L H L H L H L	H L H L H L H L	4.5 v		See note 1		

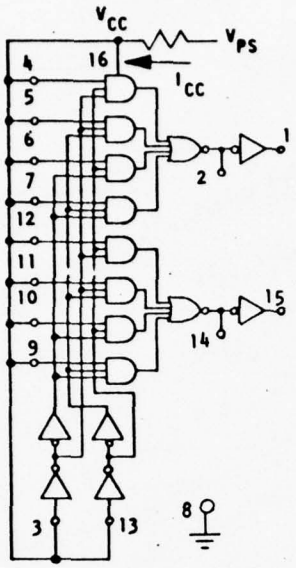
Initial and final test conducted at +25°C and +125°C. Interim test conducted at 25°C.

NOTE:

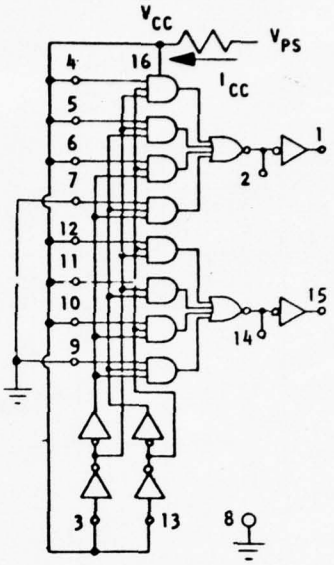
1. INPUTS: A = 4.5v and B = GND
   OUTPUTS: Output voltages shall be either:
   (a) H = 2.4 volts minimum and L = 0.4 volt maximum when using a high speed checker double comparator, or
   (b) H $\geq$ 1.5 volts and L < 1.5 volts when using a high speed checker single comparator

STORAGE RELIABILITY
OF MISSILE MATERIEL

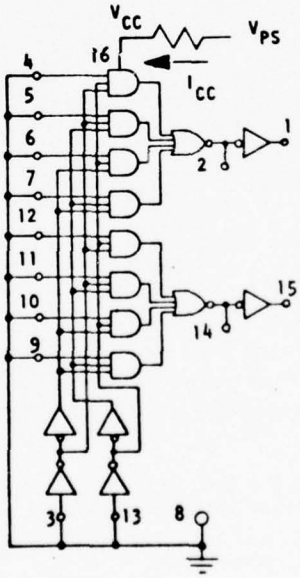
REPORT MDC E1601
29 APRIL 1977



BIAS CIRCUIT 1

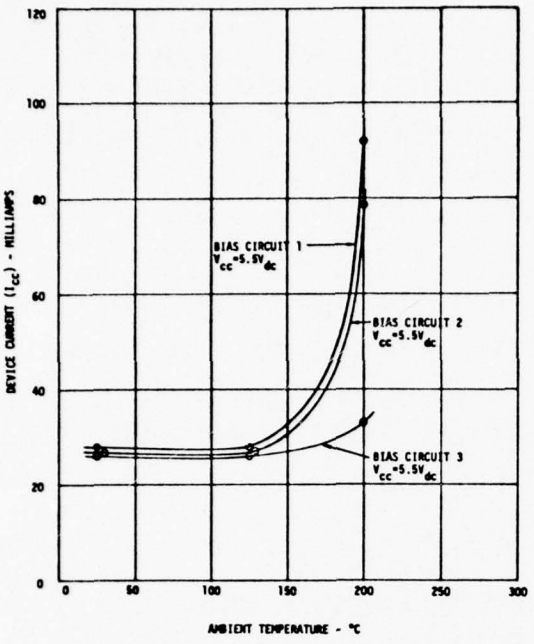


BIAS CIRCUIT 2

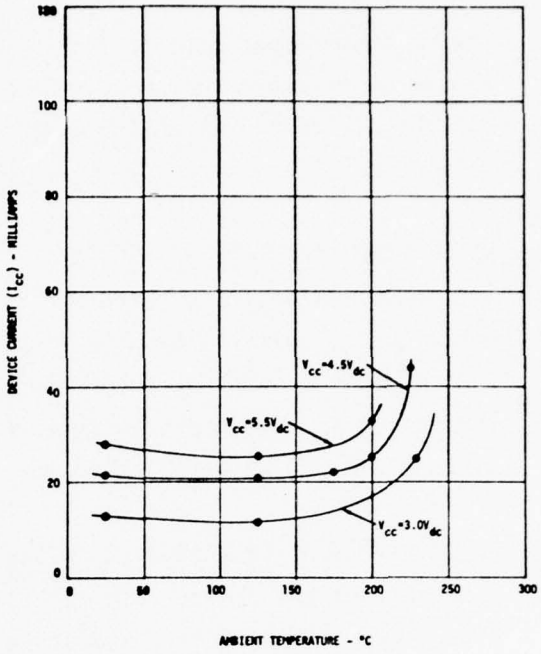


BIAS CIRCUIT 3

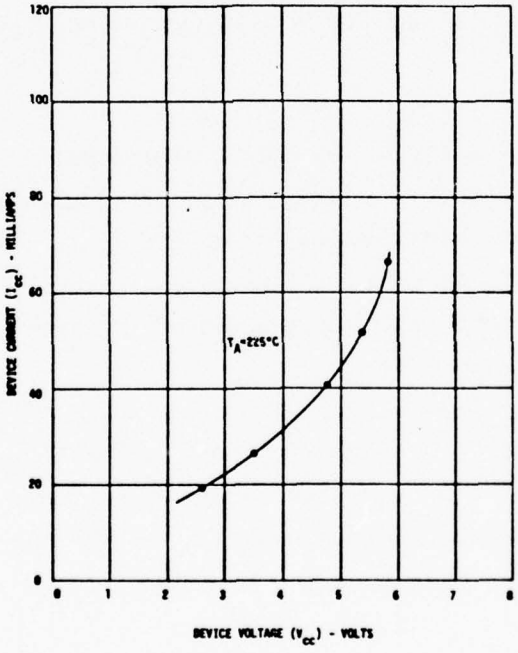
FIGURE B5. BIAS CIRCUITS - P/N M38510/01404 - DUAL 4-INPUT MULTIPLEXER



BIAS CIRCUITS 1, 2 AND 3



BIAS CIRCUIT 3



BIAS CIRCUIT 3

FIGURE B6. BIAS CIRCUIT EVALUATION - P/N M38510/01404 - DUAL 4-INPUT MULTIPLEXER

the maximum temperature to 225°C allowed V_{CC} = 5.0 volts. The third plot of Figure B6 is supply current versus supply voltage with the device operating in an ambient of 225°C. Circuit 3 with a 5 volt V_{CC} was selected as the candidate life test circuit.

B5.0 STEP STRESS TEST RESULTS

A step stress test was performed on 20 devices utilizing bias circuit 3 with V_{CC} equal to 5.0 volts. The step stress test consisted of 2 steps of sixteen hours, the first in an ambient temperature of 200°C and the second at 225°C. As summarized in Figure B7, no failures were encountered, indicating that bias circuit 3 could be safely used for the life test.

B6.0 LIFE TEST CONDITION AND RESULTS

A summary of the accelerated life test conditions for each cell appears in Figure B7. Table B3 is a summary of the life test showing cumulative failures at the various interim test times. Cells 1, 2, 3 and 5 were terminated after 4000 hours of life test. Cell 4 was left on test until it reached 6000 hours. Only two failures, one in Cell 4 and one in Cell 5, were generated.

B7.0 FAILURE ANALYSIS

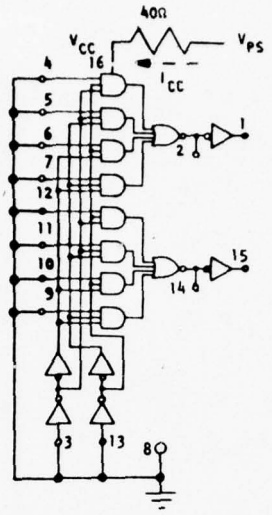
A summary of the failure analysis results is presented in Table B4. One part displayed an open pin 11 that was traced to a lifted aluminum ultrasonic wire bond at the die metallization. The bond pad contained an imprint of the bond, but almost no sign of welding as shown in Figure B8. Insufficient ultrasonic energy was transmitted to the bond interface because of improper machine settings or insufficient bond time.

One part exhibited an open pin 14 that was not confirmed during bench testing. Microscopic examination of the interior of the part and pull testing of the wire bonds disclosed no anomaly which could account for the symptoms; therefore, the failure was attributed to an open in the test card or test set socket.

B8.0 DATA CORRELATION

There were insufficient test failures to allow failure distribution analysis. The Table B4 Failure Analysis Summary reveals only two failures. The lifted bond

STEP STRESS AND LIFE TEST CIRCUIT



STEP STRESS TEST - FAILURE SUMMARY (20 DEVICES)

AMBIENT TEMP. (°C)	V_{CC} (V)	CUMULATIVE FAILURES
200	5.0	0
225	5.0	0

LIFE TEST CONDITIONS

TEST CELL NUMBER	T_A AMBIENT TEMPERATURE (°C)	V_{CC} DEVICE VOLTAGE (VOLTS)	I_{CC} DEVICE CURRENT (MILLIAMPS)	P_D POWER DISSIPATION (MILLIWATTS)	T_J JUNCTION TEMPERATURE (°C)
1	225	5.0	44.8	224	245
2	225	4.0	31.5	126	236
3	225	3.0	22.5	68	231
4	225	0	0	0	225
5	200	5.0	28.5	143	214

FIGURE B7. STEP STRESS RESULTS AND LIFE TEST CONDITIONS - P/N M38510/01404 - DUAL 4-INPUT MULTIPLEXER

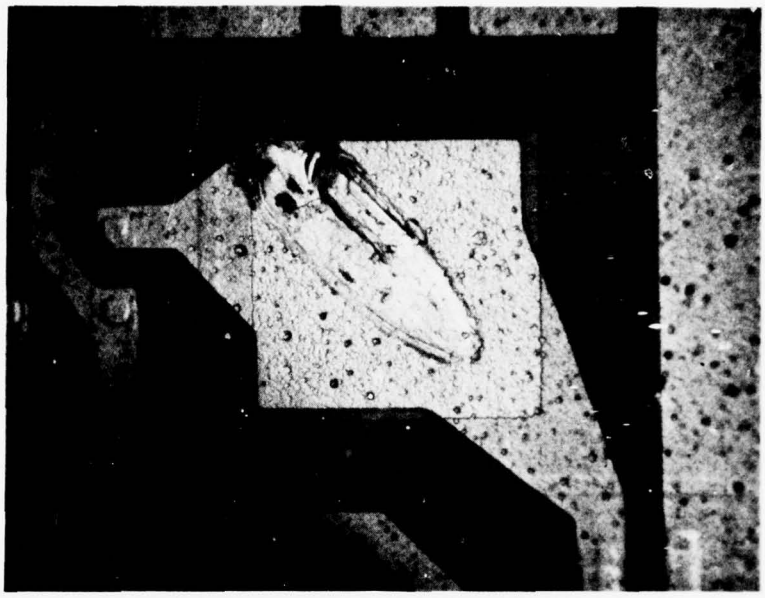
TABLE B3. LIFE TEST SUMMARY - P/N M38510/01404 - DUAL 4-INPUT MULTIPLEXER

TEST CELL DESCRIPTION				CUMULATIVE FAILURES AT HOURS OF TEST											
CELL NO.	APPLIED BIAS	AMBIENT TEMP.	QUANTITY	4	8	16	32	64	128	256	512	1000	2504	4000	6000
1	5 VDC	225°C	30	0	0	0	0	0	0	0	0	0	0	0*	
2	4 VDC	225°C	30	0	0	0	0	0	0	0	0	0	0	0*	
3	3 VDC	225°C	30	0	0	0	0	0	0	0	0	0	0	0*	
4	0 VDC	225°C	30	0	0	0	0	0	0	0	0	0	1	1	1*
5	5 VDC	200°C	30	0	0	0	0	1	1	1	1	1	1	1*	

* TEST TERMINATED

TABLE B4. FAILURE ANALYSIS SUMMARY - P/N M38510/01404 - DUAL 4-INPUT MULTIPLEXER

	A. FAILED PARAMETER OR SYMPTOMS	QUANTITY OF FAILURES AND TIME OF FAILURE (HOURS)				
	B. FAILURE MODE	225 C				200 C
	C. FAILURE MECHANISM	5V	4V	3V	0V	5V
	D. CAUSE OF FAILURE	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5
MECHANICAL	A. OPEN PIN					1@64
	B. LIFTED Al-Al BOND					
	C. UNDERBONDED					
	D. INSUFFICIENT ULTRASONIC ENERGY					
TEST ERROR	A. OPEN PIN				1@2504	
	B. NONE (RETEST OK)					
	C. NONE					
	D. TEST SET FAULT					
	TOTAL NUMBER OF FAILED PARTS	0	0	0	1	1



345X

FIGURE B8. LIFT-OFF PATTERN OF THE OPEN PIN 11 BOND - P/N M38510/01404 - DUAL 4-INPUT MULTIPLEXER

failure is applicable to a storage environment and the failure due to test set fault is not applicable. Since the failure data is inadequate for distributional analysis, the parametric test data was investigated for obvious trends that would allow extrapolation of times to failure. No obvious trends were detected. The behavior of six parameters, V_{IC}, V_{OH}, I_{IL}, I_{OS}, I_{IH1}, and I_{IH2}, at the highest temperature and voltage stress, is shown in Figure B9.

The lack of test induced failures or parameter degradation trends indicates the test device has a high storage reliability potential ($\lambda(t)_{MAX} << 10^{-10}$ failures per hour).

B9.0 CONCLUSIONS AND RECOMMENDATIONS

- The one applicable failure encountered in the life test program was inadequate for failure rate analysis.
- This dual 4-input multiplexer has demonstrated a high storage reliability potential ($\lambda(t)_{MAX} << 10^{-10}$ failures per hour).

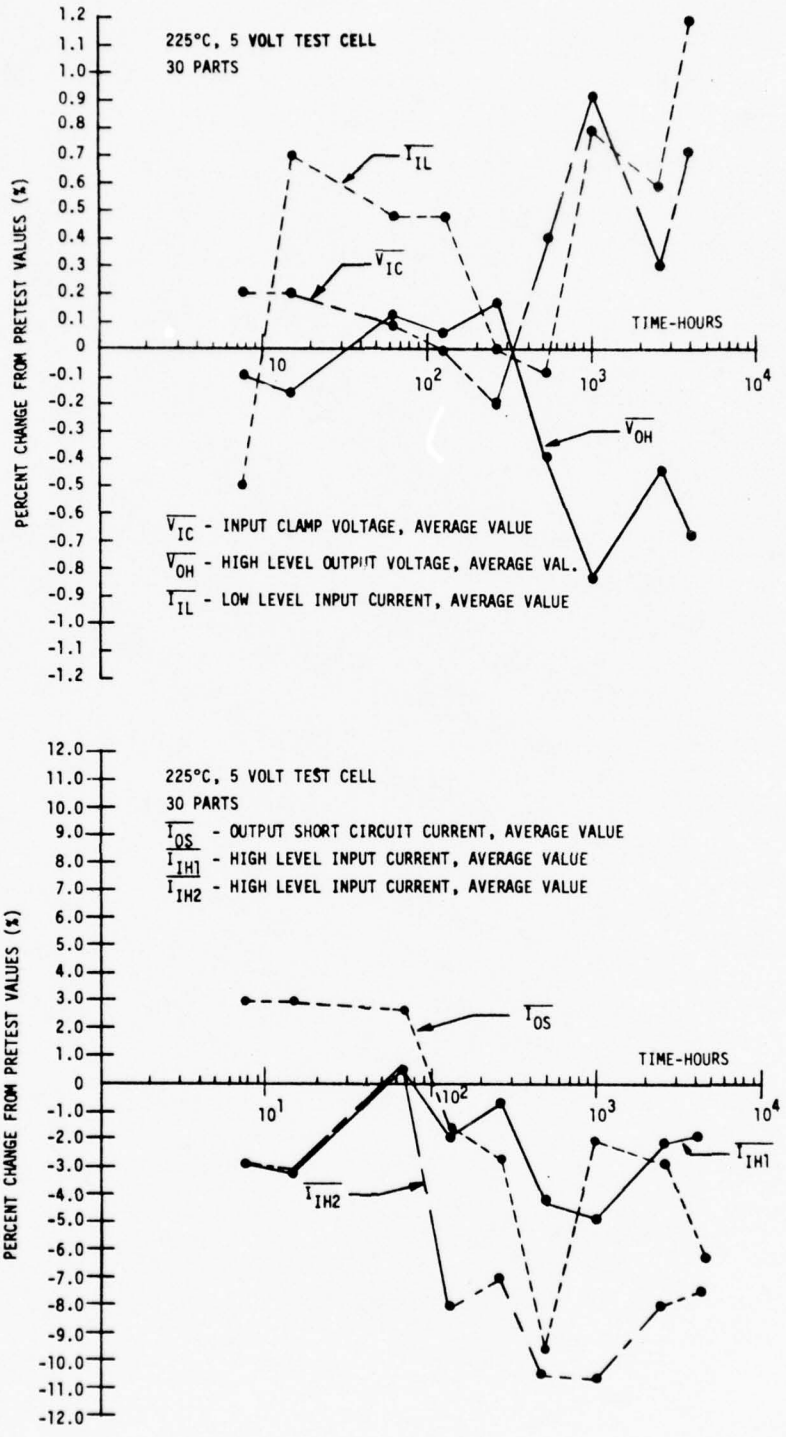


FIGURE B9. BEHAVIOR OF SELECTED PARAMETERS DURING LIFE TEST - P/N M38510/01404 - DUAL 4-INPUT MULTIPLEXER

APPENDIX C

P/N M38510/00303

QUAD 2-INPUT BUFFER

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C3.0	ELECTRICAL TEST CRITERIA	C2
C4.0	BIAS CIRCUIT ANALYSIS	C2
C5.0	STEP STRESS TEST RESULTS	C9
C6.0	LIFE TEST CONDITIONS AND RESULTS	C9
C7.0	FAILURE ANALYSIS	C9
C8.0	DATA CORRELATION	C16
C9.0	CONCLUSIONS AND RECOMMENDATIONS	C16

C1.0 PART DESCRIPTION

The Quad 2-Input NAND Buffer, P/N M38510/00303, is a high sink current, open collector output device. The part, manufactured by Signetics Corporation, is a monolithic die mounted in a ceramic flatpack package in the conventional chip and wire manner. This test configuration is identical to the SAM-D use configuration.

C2.0 CONSTRUCTION ANALYSIS

Table C1 contains a summary of the pertinent physical details of the test configuration part. Figure C1 is a photograph of the external construction of the device. Figure C2 is a schematic diagram of one of the four identical buffers. A view of the internal cavity of this part and a photograph of the die topography make up Figure C3. The device contains no materials which limited testing below 300°C.

The typical SAM-D configuration of this part, Figure C4, consists of the test part (M38510/00303) soldered to the metallization of a fiber glass circuit board.

C3.0 ELECTRICAL TEST CRITERIA

All of the Subgroup 1 tests of the Group A inspection for device type 03 from M38510/003 were performed for this device. Table C2 identifies these tests, terminal conditions and limits.

C4.0 BIAS CIRCUIT ANALYSIS

Various bias circuits were examined and two were found which could be operated at 250°C with V_{CC} = 5.0 volts, as shown in Figure C5. Bias circuit 1 had one input high and one input low on each buffer input and all of the outputs connected to a common pull-up resistor. Bias circuit 2 had one input high and one input low on two buffers and both inputs high on the other two buffers. Each output had a pull-up resistor. Bias circuit 1 required less supply current at room temperature than bias circuit 2 and could safely operate at ambient temperatures up to 250°C, whereas bias circuit 2 was dangerously close to thermal runaway at 250°C. Bias circuit 1 was chosen as the candidate life test circuit for this reason. The maximum life test temperature would have to be limited to 250°C to preclude thermal runaway.

TABLE C1. PART CONSTRUCTION DETAILS - P/N M38510/00303 - QUAD 2-INPUT NAND BUFFER

A. IDENTIFICATION

1. Part Name: Quad 2-Input NAND Buffer (5438)
2. Part Manufacturer: Signetics Corporation
3. Part Number: M38510/00303
4. Date Code: J7208

B. PACKAGE

1. Type: 14-Lead Ceramic Flatpack
2. Weight: 0.296 gram
3. Materials:
   a) Lid: Ceramic
   b) Leads: Kovar, gold-plated
   c) Lid Seal: glass

C. INTERNAL GEOMETRY

1. Interconnections:
   a) Type: Aluminum Wire
   b) Diameter: 0.00105 inch
   c) Bonds:
      1) Aluminum-aluminum ultrasonic at the die
      2) Aluminum-gold ultrasonic at the frame
2. Die
   a) Type: Silicon, Planar
   b) Scribe Method: Mechanical
   c) Dimensions: 0.062 inch x 0.051 inch
   d) Attach Method: Gold eutectic
   e) Glassivation: Silicon Dioxide
3. Metallization:
   a) Type: Aluminum
   b) Number of Layers: One

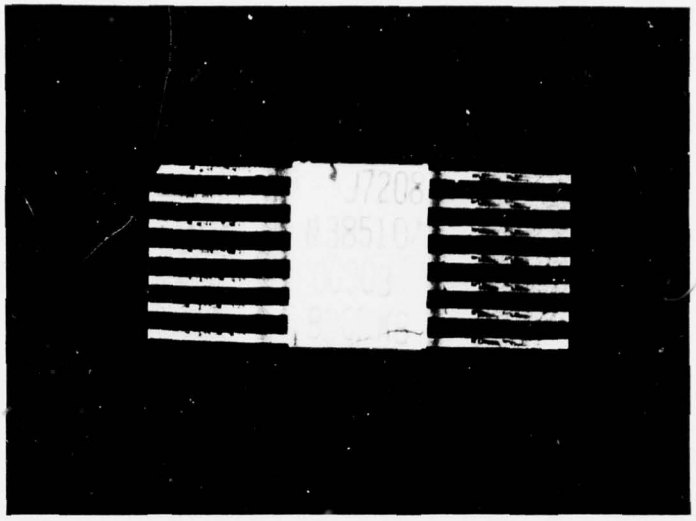

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FIGURE C1. EXTERNAL CONSTRUCTION - P/N M38510/00303 - QUAD 2-INPUT NAND BUFFER

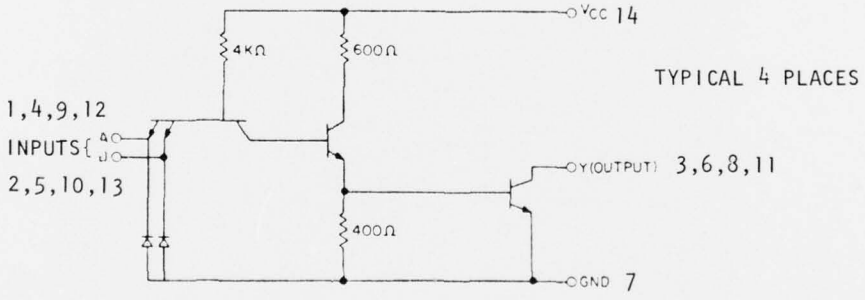
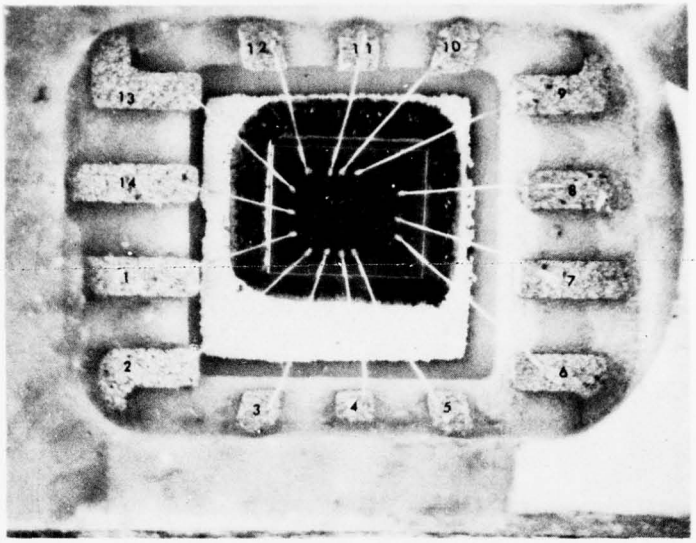


FIGURE C2. SCHEMATIC DIAGRAM - P/N M38510/00303 - QUAD 2-INPUT NAND BUFFER



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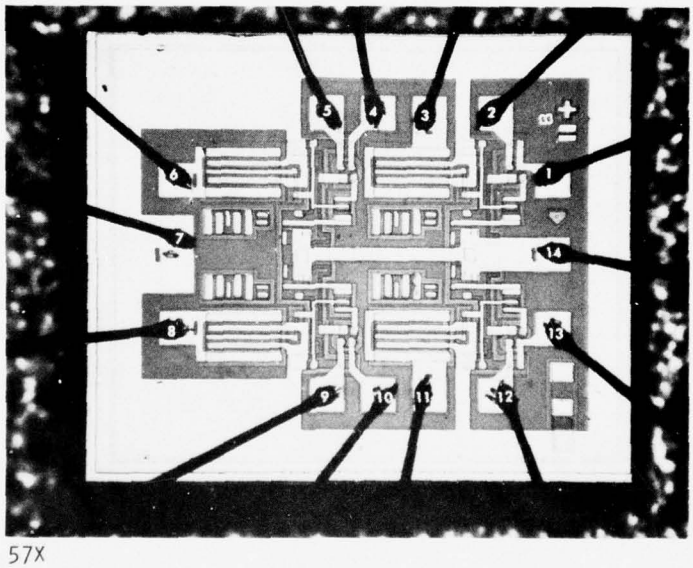
VIEW WITH LID REMOVED



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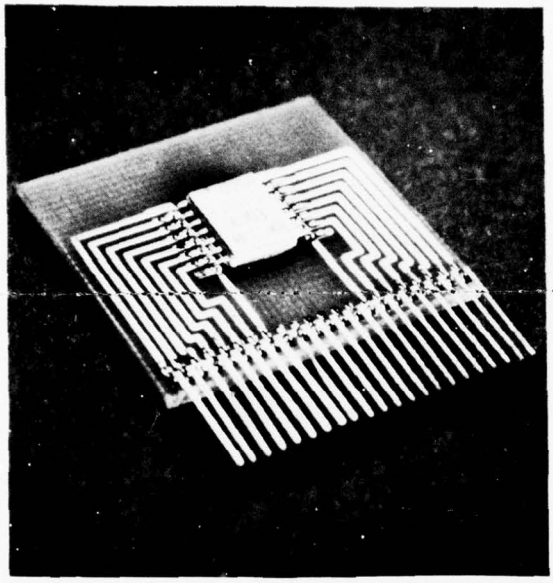
DIE TOPOGRAPHY

FIGURE C3. INTERNAL CONSTRUCTION DETAILS - P/N M38510/00303 - QUAD 2-INPUT NAND BUFFER



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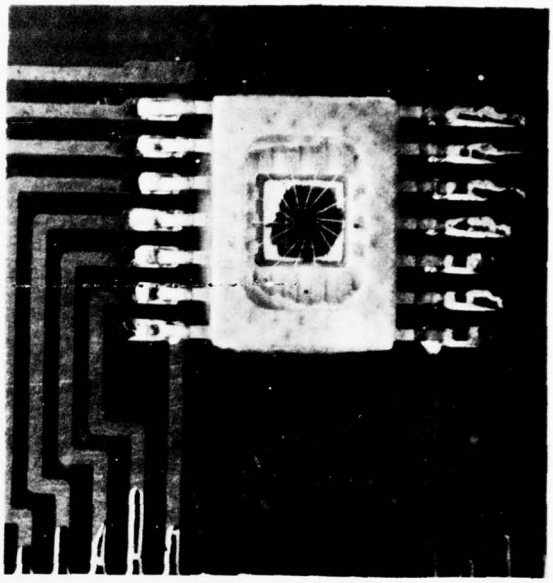
EXTERNAL



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INTERNAL

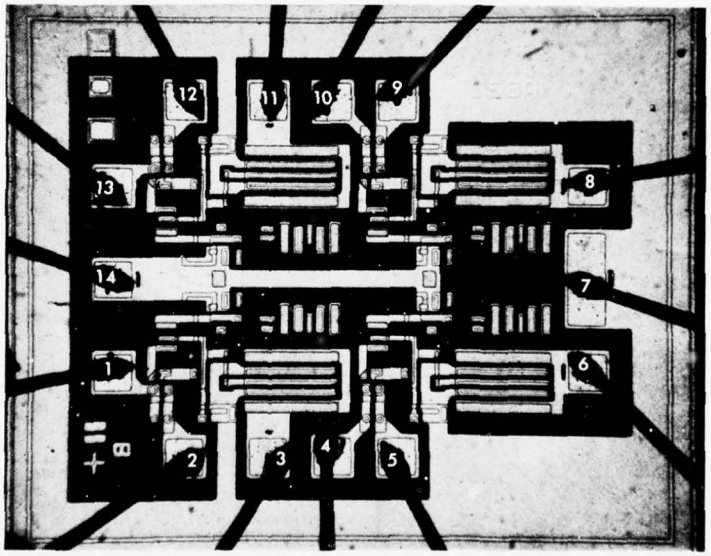

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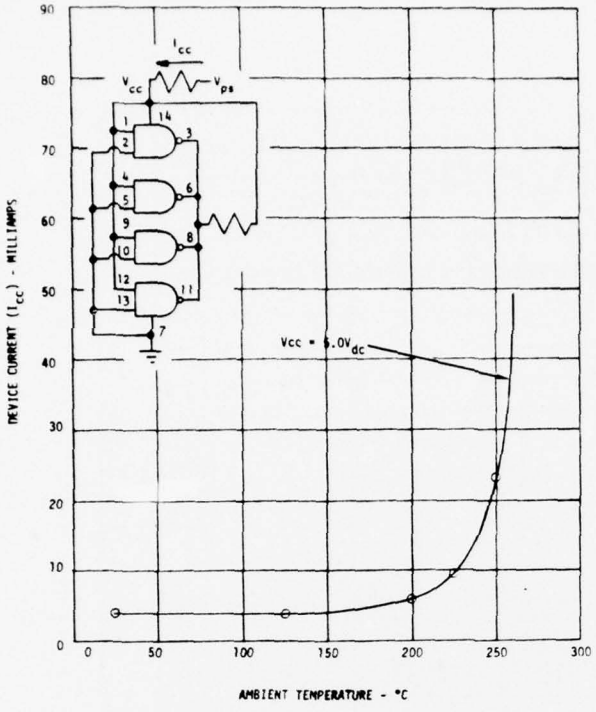
FIGURE C4. TYPICAL SAM-D CONFIGURATION - P/N 773428 - QUAD 2-INPUT NAND BUFFER

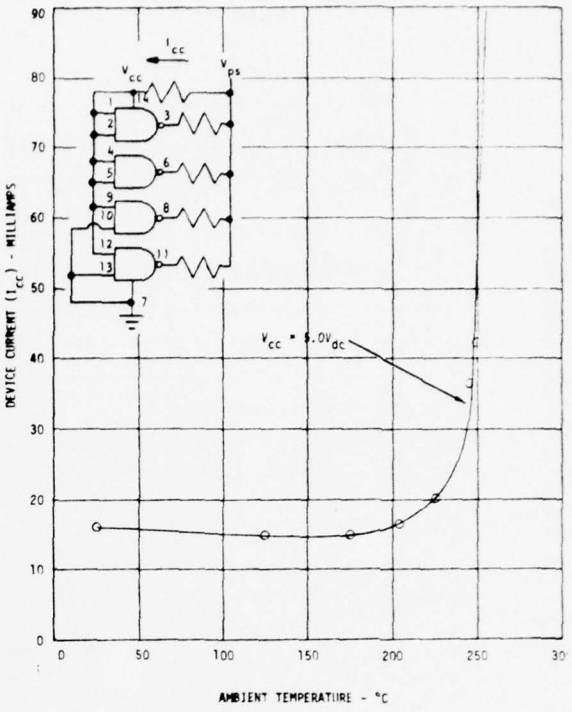
TABLE C2. ELECTRICAL TEST CONDITIONS - P/N M38510/00303 - QUAD 2-INPUT NAND BUFFER

Symbol	MIL-STD-883 method	LEAD	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. Terminal	Test limits		
		Test No.	1A	1B	1Y	2A	2B	2Y	GND	3Y	3A	3B	4Y	4A	4B	VCC		Min	Max	Unit
V_{OL}	3007	1	2.0 v	2.0 v	48 mA	5.5 v	5.5 v	48 mA	GND		5.5 v	5.5 v		5.5 v	5.5 v	4.5 v	1Y		0.4	V
		2	5.5 v	5.5 v		2.0 v	2.0 v				5.5 v	5.5 v					2Y		0.4	V
		3				5.5 v	5.5 v			48 mA	2.0 v	2.0 v					3Y		0.4	V
		4									5.5 v	5.5 v	48 mA	2.0 v	2.0 v		4Y		0.4	V
I_{CEX}		5	0.8 v		5.5 v									5.5 v	5.5 v		1Y		250	µA
		6	5.5 v	0.8 v	5.5 v												2Y		250	µA
		7		5.5 v		0.8 v	0.8 v	5.5 v									2Y		250	µA
		8				5.5 v	5.5 v	5.5 v									3Y		250	µA
		9								5.5 v	0.8 v	0.8 v					3Y		250	µA
		10								5.6 v	5.5 v	5.5 v		0.8 v			4Y		250	µA
		11										5.5 v	5.5 v	5.5 v	0.8 v		4Y		250	µA
		12																		
V_{IC}		13	-12 mA														1A		-1.5	V
		14		-12 mA													1B		-1.5	V
		15				-12mA	-										2A		-1.5	V
		16					-12 mA										2B		-1.5	V
		17									-12 mA	-12 mA					3A		-1.5	V
		18												-12 mA			3B		-1.5	V
		19													-12 mA		4A		-1.5	V
		20															4B		-1.5	V
I_{IH_1}	3010	21	2.4 v	GND		GND	GND				GND	GND		GND	GND	5.5 v	1A		40	µA
		22	GND	2.4 v		GND											1B		40	µA
		23		GND		2.4 v	2.4 v				2.4 v			2A			40	µA
		24				GND	GND				GND	2.4 v					2B		40	µA
		25									2.4 v	GND		2.4 v	2.4 v		3A		40	µA
		26									GND			GND			3B		40	µA
		27															4A		40	µA
		28															4B		40	µA
I_{IH_2}	3010	29															1A		100	µA
		30	GND	5.5 v		5.5 v	5.5 v				5.5 v	5.5 v			GND		1B		100	µA
		31		GND		GND	GND				GND	GND					2A		100	µA
		32															2B		100	µA
		33									5.5 v	5.5 v		5.5 v	5.5 v		3A		100	µA
		34									GND	GND					3B		100	µA
		35															4A		100	µA
		36															4B		100	µA
I_{IL}	3009	37	0.4 v	5.5 v		5.5 v	5.5 v		GND		5.5 v	5.5 v		5.5 v	5.5 v	5.5 v	1A	-0.7	-1.6	mA
		38	5.5 v	0.4 v		5.5 v											1B	-0.7	-1.6	mA
		39		5.5 v		0.4 v											2A	-0.7	-1.6	mA
		40				5.5 v	0.4 v				0.4 v	0.4 v		0.4 v			2B	-0.7	-1.6	mA
		41					5.5 v				5.5 v						3A	-0.7	-1.6	mA
		42										5.5 v					3B	-0.7	-1.6	mA
		43												0.4 v	0.4 v		4A	-0.7	-1.6	mA
		44												5.5 v	0.4 v		4B	-0.7	-1.6	mA
I_{CCL}	3005	45												5.5 v	5.5 v		VCC		54	mA
I_{CCH}	3005	46	GND	GND		GND	GND				GND	GND		GND	GND		VCC		8.5	mA

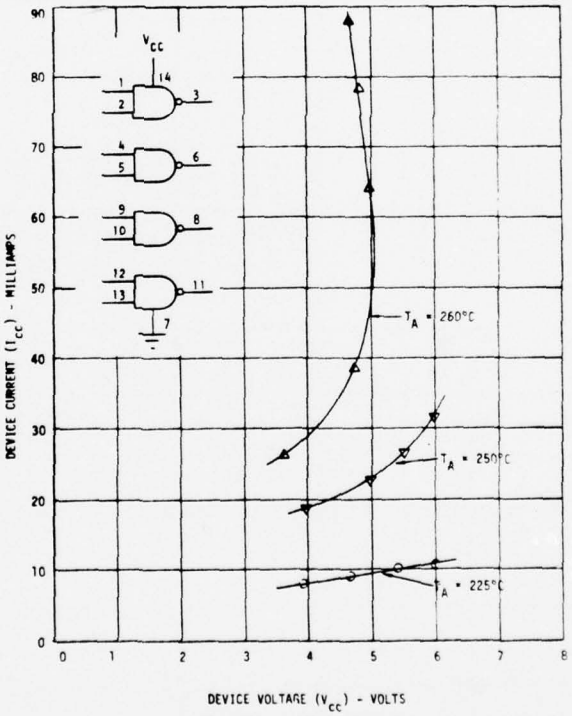
INITIAL AND FINAL TEST CONDUCTED AT +25°C AND +125°C. INTERIM TEST CONDUCTED AT 25°C.



BIAS CIRCUIT 1



BIAS CIRCUIT 2



BIAS CIRCUIT 1

FIGURE C5. BIAS CIRCUIT EVALUATION - P/N M38510/00303 - QUAD 2-INPUT NAND BUFFER

C5.0 STEP STRESS TEST RESULTS

A step stress was performed on 20 parts configured in bias circuit 1 with V_{CC} = 5.0 volts. The first step was 175°C and the ambient temperature was increased 25°C for each subsequent step. The duration of each step was 16 hours. As shown in the Figure C6 summary, the step stress test was discontinued following the 250°C step (at 275°C, the parts would have been in thermal runaway) with no failures having been generated, thus verifying that the devices could be safely operated in bias circuit 1.

C6.0 LIFE TEST CONDITIONS AND RESULTS

Figure C6 summarizes the life test conditions of each cell. Cells 1, 2, 3 and 4 were terminated at 4000 hours. Cell 5 remained in life test for 6000 hours. Thirteen failures were generated, two in each of Cells 1, 2 and 5, three in Cell 3 and four in Cell 4. Table C3 is a summary of the life test providing the cumulative number of failures at each interim test time.

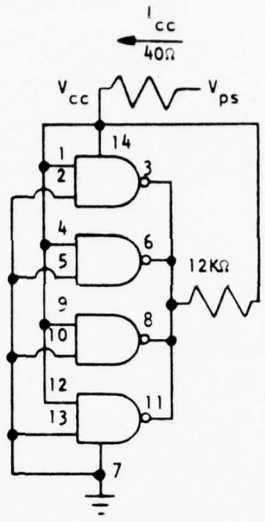
C7.0 FAILURE ANALYSIS

A summary of the failure analysis results is presented in Table C4.

Bulk and Mechanical Failures - One part exhibited excessive I_{IH1} and I_{IH2} at pin 12 that was traced to a degraded clamp diode. The aluminum metallization had penetrated the junction because the cathode ohmic contact window was too large, as shown in Figure C7. The oversized window was caused by a photolithographic or etch error during manufacturing.

One part exhibited an open pin 14 that was traced to a broken aluminum ultrasonic wire bond at the gold-plated lead frame. The bond had opened at the heel and the bond was encircled with purple colored intermetallic growth. This indicated that the failure was the result of voiding in $AuAl_2$. Optical examinations of unstressed parts and life test parts that failed for other reasons disclosed that most of the life test parts contained $AuAl_2$ around the frame bonds whereas the unstressed parts contained no visible $AuAl_2$. Because only one failure due to $AuAl_2$ was encountered, no metallurgical analysis was performed to determine if the failure was caused solely by the test temperature or if it involved any manufacturing deficiency as well.

STEP STRESS AND LIFE TEST CIRCUIT



STEP STRESS TEST - FAILURE SUMMARY (20 DEVICES)

AMBIENT TEMP. (°C)	V_{CC} (V)	CUMULATIVE FAILURES
175	5.0	0
200	5.0	0
225	5.0	0
250	5.0	0

LIFE TEST CONDITIONS

TEST CELL NUMBER	T_A AMBIENT TEMPERATURE (°C)	V_{CC} DEVICE VOLTAGE (VOLTS)	I_{CC} DEVICE CURRENT (MILLIAMPS)	P_D POWER DISSIPATION (MILLIWATTS)	T_J JUNCTION TEMPERATION (°C)
1	250	5.0	35	175	277
2	250	4.0	26	104	266
3	250	3.0	20	60	259
4	250	0	0	0	250
5	225	5.0	21	105	238

FIGURE C6. STEP STRESS RESULTS AND LIFE TEST CONDITIONS - P/N M38510/00303 - QUAD 2-INPUT NAND BUFFER

TABLE C3. LIFE TEST SUMMARY - P/N M38510/00303 - QUAD 2-INPUT NAND GATE

TEST CELL DESCRIPTION				CUMULATIVE FAILURES AT HOURS OF TEST													
CELL NO	APPLIED BIAS	AMBIENT TEMP	QUANTITY	1	2	4	8	16	32	64	128	256	512	1000	2504	4000	6000
1	5 VDC	250°C	30	-	-	0	0	0	0	1	1	1	1	2	2	2*	
2	4 VDC	250°C	30	-	-	0	0	0	0	0	1	1	1	1	2	2*	
3	3 VDC	250°C	30	-	-	0	0	0	0	0	0	0	0	1	1	3*	
4	0 VDC	250°C	30	-	-	0	0	0	0	0	0	0	1	1	1	4*	
5	5 VDC	225°C	30	0	0	0	0	0	0	0	0	0	0	1	1	2	2*

* TEST TERMINATED

TABLE C4. FAILURE ANALYSIS SUMMARY - P/N M38510/00303 - QUAD 2-INPUT NAND GATE

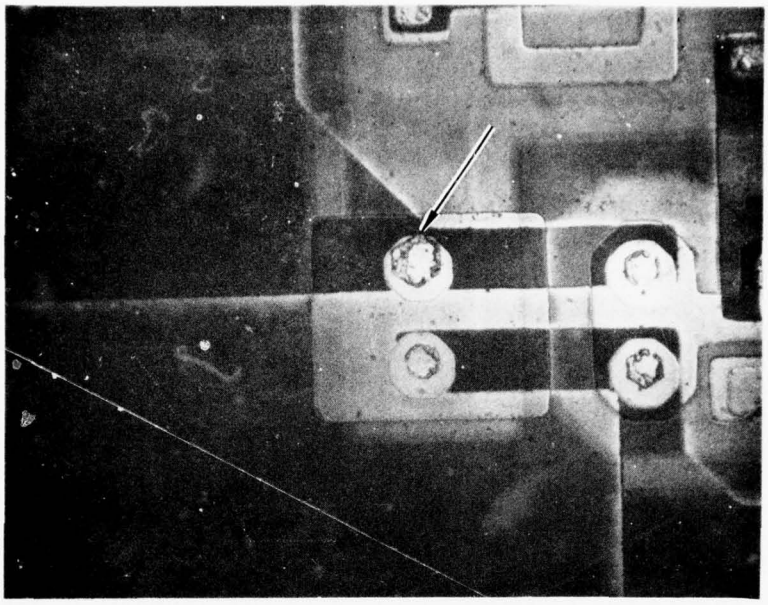
	A. FAILED PARAMETER OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TIME OF FAILURE (HOURS)				
		250°C				225°C
		5V	4V	3V	0V	5V
		CELL 1	CELL 2	CELL 3	CELL 4	CELL 5
BULK AND MECHANICAL FAILURES	A. EXCESSIVE I_{IH} B. DEGRADED PIN 12 CLAMP DIODE C. ALUMINUM PENETRATION D. PHOTOLITHOGRAPHIC OR ETCHING ERROR		1@128			
	A. OPEN PIN 14 B. BROKEN Al-Au BOND C. VOIDING IN $AuAl_2$ D. PROBABLY EXCESSIVE TEMPERATURE		1@2504			
	A. EXCESSIVE I_{CEX} B. DEGRADED COLLECTOR TO SUBSTRATE JUNCTION C. NOT DETERMINED (INITIALLY MARGINAL) D. PROBABLY A MICRODEFECT IN THE JUNCTION	1@64				
	A. I_{IL} TOO LOW B. RESISTIVE OHMIC CONTACT C. SILICON ELECTROMIGRATION D. EXCESSIVE CURRENT DENSITY			1@4000		
TEST ERRORS	A. EXCESSIVE I_{CEX} B. C-E SHORT IN THE OUTPUT TRANSISTOR C. SECOND BREAKDOWN D. ELECTRICAL OVERSTRESS			1@1000 1@4000	1@512 2@4000	1@1000 1@4000
	A. EXCESSIVE I_{IH} B. SHORTED CLAMP DIODE C. FLASH-OVER SHORT D. ELECTRICAL OVERSTRESS	1@1000			1@4000	
	TOTAL NO. OF FAILED PARTS	2	2	3	4	2

One part exhibited excessive I_{CEX} at pin 8 traced to a degraded collector-substrate (isolation) junction in the output transistor. The degradation was not bake reversible and this device exhibited a marginal value of I_{CEX} at pin 8 (213 μA) upon receipt, which indicated that the leakage was caused by a bulk defect introduced during manufacturing. Chemical etching of the junction did not reveal the flaw, thus the exact failure mechanism was not established.

One part exhibited low I_{IL} at pin 2 that was traced to a resistive ohmic contact at the input transistor emitter diffusion. Silicon had migrated down the aluminum stripe in the direction of electron flow (pin 2 was grounded during life test) and had accumulated in the ohmic contact, increasing its resistance. Silicon migration is primarily dependent on the current density; therefore, this failure did not represent a valid storage reliability problem.

Test Errors - Seven parts exhibited excessive I_{CEX} traced to nonreversible collector-emitter degradation in the output transistor. The transistors contained visible surface damage such as burn marks on the emitter metallization fingers, Figure C8, or burn spots in the emitter ohmic contacts as shown in Figure C9. Examinations of the failed transistors after etching the silicon disclosed no lateral surface damage, only deep pits in the end of the ohmic contact beneath the burn sites. This indicated that the degradation was due to vertical collector-emitter melt-throughs. Examination of undamaged transistors disclosed alloy pits in the emitter ohmic contacts, as shown in Figure C10, at the same point where the damage occurred in the failed transistors. The pits are caused by silicon dissolution and aluminum penetration into the silicon during the aluminum alloying cycle. The degraded transistors each failed abruptly with no sign of prior degradation. This, in conjunction with the signs of overheating present, indicated that the damage was caused primarily by electrical overstress. The alloy pits in the emitter ohmic contacts probably reduced the ability of the transistors to withstand electrical transients.

Two parts displayed excessive I_{IH1} and I_{IH2} traced to shorted clamp diodes. The diodes contained flashover shorts as illustrated in Figure C11 and this damage indicated that the diodes had been electrically overstressed.



490X

FIGURE C7. PINS 12 AND 13 INPUT CLAMP DIODES AFTER METALLIZATION REMOVAL SHOWING WHERE THE OVERSIZED CONTACT WINDOW AT PIN 12 OVERLAPPED THE JUNCTION (ARROW) - P/N M38510/00303 - QUAD 2-INPUT NAND GATE

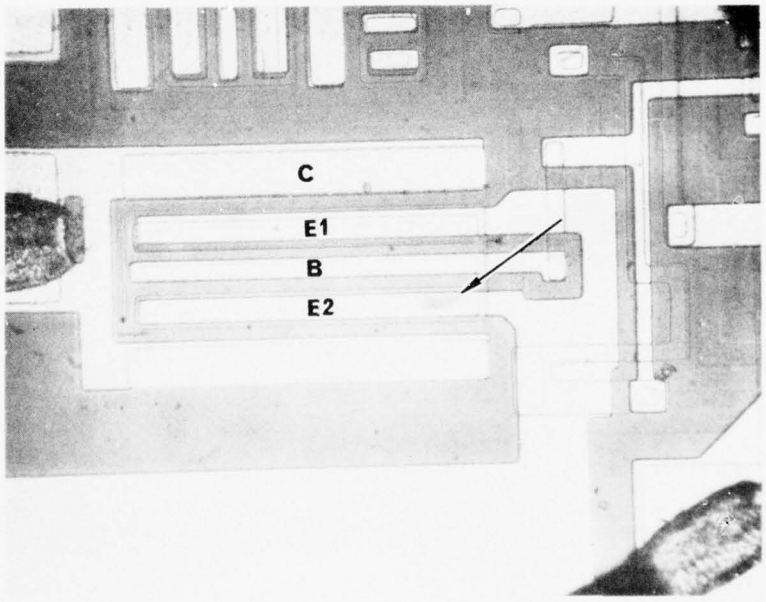


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FIGURE C8. PIN 8 OUTPUT TRANSISTOR SHOWING BURN MARK (ARROW) ON THE EMITTER METALLIZATION FINGER - P/N M38510/00303 - QUAD 2-INPUT NAND GATE

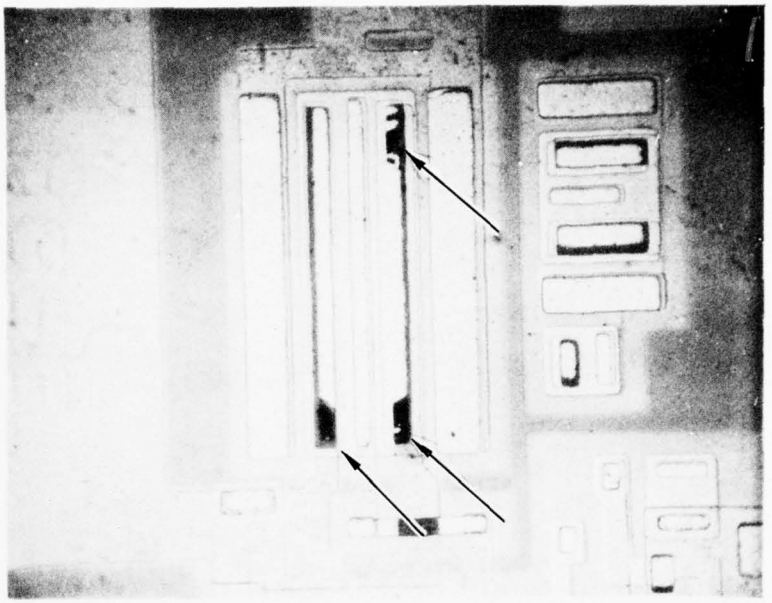

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FIGURE C9. PIN 8 OUTPUT TRANSISTOR AFTER REMOVAL OF THE METALLIZATION SHOWING BURN MARKS (ARROWS) IN THE EMITTER OHMIC CONTACTS - P/N M38510/00303 - QUAD 2-INPUT NAND GATE

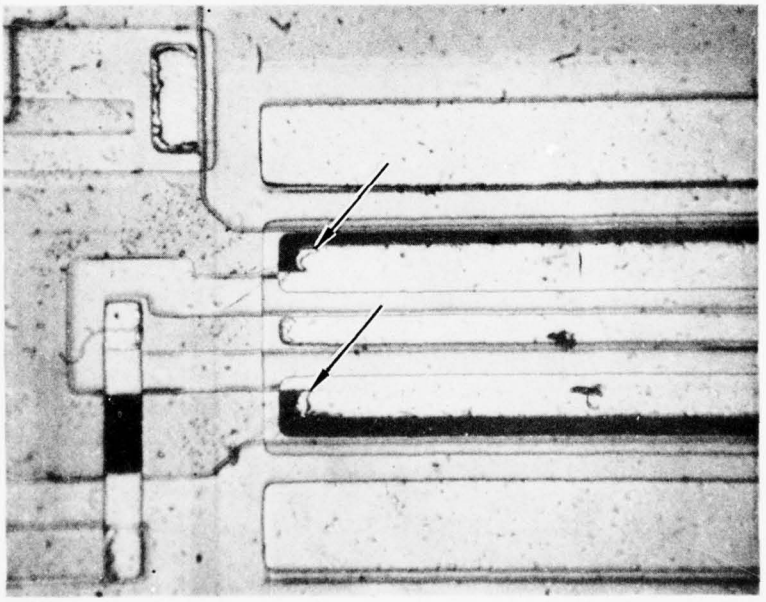

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FIGURE C10. NORMAL PIN 8 OUTPUT TRANSISTOR AFTER REMOVAL OF THE METALLIZATION SHOWING ALLOY PITS (ARROWS) IN THE EMITTER CONTACTS AT THE POINT OF STRIPE ENTRY - P/N M38510/00303 - QUAD 2-INPUT NAND GATE

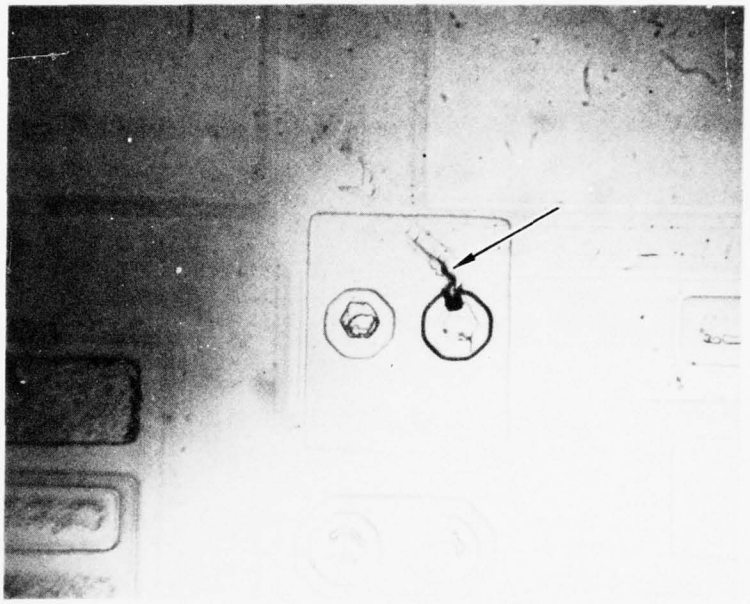

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FIGURE C11. PIN 9 AND 10 CLAMP DIODES AFTER SILICON ETCH SHOWING FLASHOVER (ARROW) ON THE PIN 9 DIODE - P/N M38510/00303 - QUAD 2-INPUT NAND GATE

C8.0 DATA CORRELATION

Insufficient failures were encountered in the test program to allow statistical failure distribution analysis. The first three failure mechanisms identified in Table C4, Failure Analysis Summary, are the only ones applicable to a storage environment. These three failure mechanisms account for only one failure each, an amount inadequate for data analysis. The balance of the thirteen failures were caused by electrical overstress or were test induced, and therefore were not applicable for data analysis.

The parameters V_{OL}, I_{CEX}, V_{IC}, I_{IH1}, I_{IH2}, I_{IL}, I_{CCL}, I_{CCH} were evaluated and found to contain no obvious trends which would allow extrapolation of times to failure. Three typical parameters, V_{IC}, I_{IH1} and I_{IL} are shown in Figure C12.

Test Cell 5, 225°C, 5 Vdc, was operated an additional 2000 hours for a cumulative 6000 hours with no additional failures and no discernible data trends.

C9.0 CONCLUSIONS AND RECOMMENDATIONS

- The lack of accelerated life test failures indicate this part has a high storage reliability potential ($\lambda(t)_{MAX} << 10^{-10}$ failures per hour).
- The parametric test data exhibited good stability.

AD-A039 788 MCDONNELL DOUGLAS ASTRONAUTICS CO-EAST ST LOUIS MO F/G 9/1
STORAGE RELIABILITY OF MISSILE MATERIEL (ACCELERATED TESTING OF--ETC(U)
APR 77 J MCGARRY, V WEISSFLUG, E SISUL DAAH01-74-C-0928
UNCLASSIFIED MDC-E1601 NL

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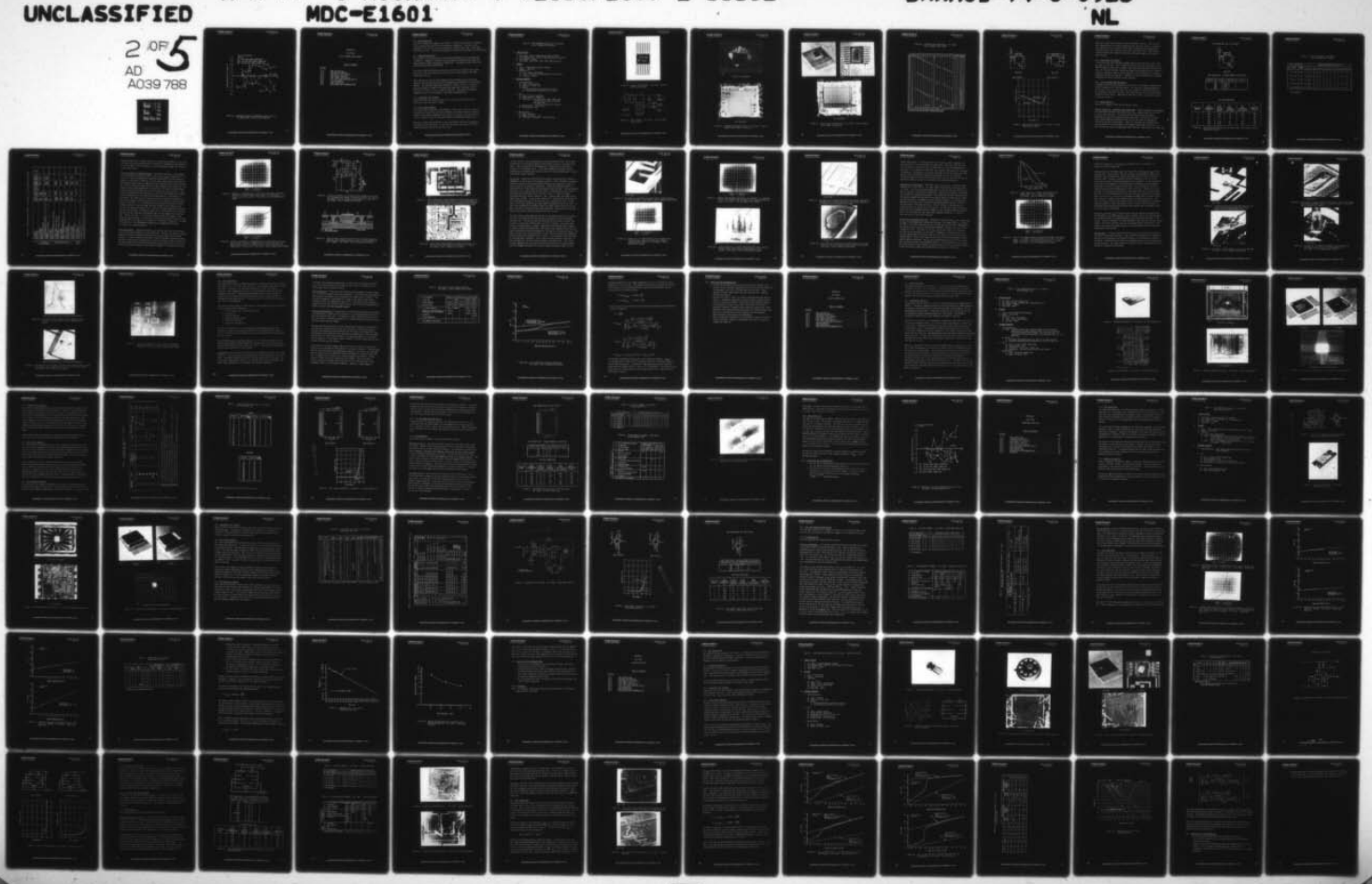

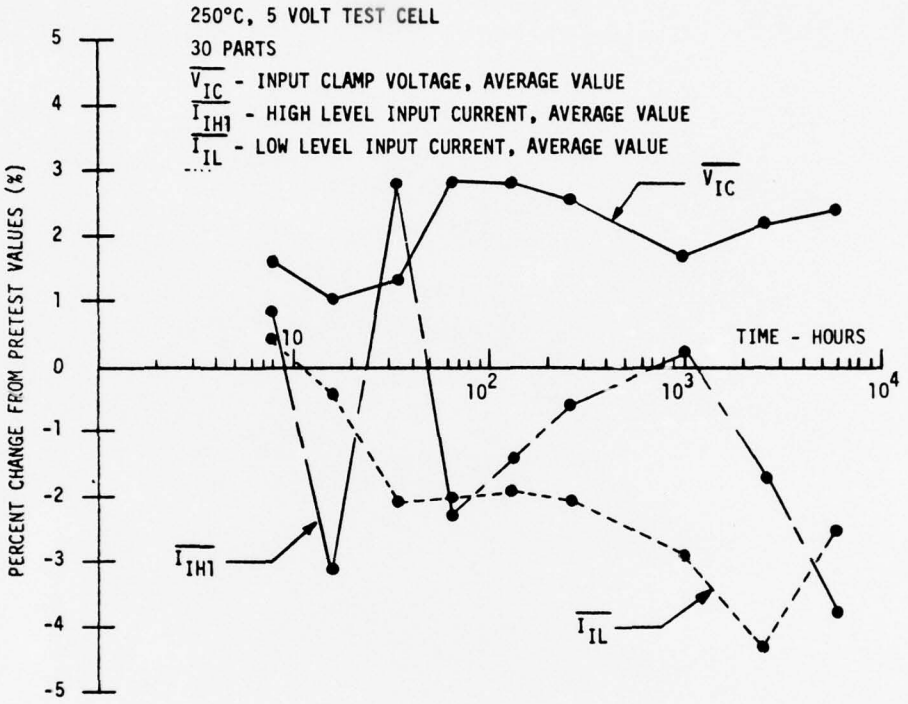

FIGURE C12. BEHAVIOR OF SELECTED PARAMETERS DURING LIFE TEST - P/N M38510/00303 - QUAD 2-INPUT NAND GATE

APPENDIX D

P/N 773050

256 BIT RANDOM ACCESS MEMORY

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D1.0 PART DESCRIPTION

The 256 Bit Random Access Memory, P/N 773050, is a 93410 type monolithic integrated circuit manufactured by Fairchild Semiconductor Corporation. The devices were packaged in a 16 pin flat pack and included the following date codes: 7250, 7302, 7304, 7308 and 7320. This test configuration is identical to the SAM-D use configuration.

D2.0 CONSTRUCTION ANALYSIS

The pertinent construction details of the test configuration part are summarized in Table D1. Figures D1, D2 and D3 are the external construction, the logic diagram, and the internal construction, respectively. The material used in this part did not restrict testing below 300°C.

The typical SAM-D configuration, Figure D4, utilizes this identical part; therefore, all of the test program device failures will be applicable to the SAM-D configuration device.

After the start of the life test program, initial failure analysis activities revealed that the delivered test parts contained two different die sizes and mask designs. The 7250 date coded parts contained a "large" (0.129 in. x 0.100 in.) die, as depicted in Figure D4; the other date coded parts contained a "small" (0.079 in. x 0.097 in.) die, as shown in Figure D3. The effect of these two different die on the test program is discussed in paragraph D8.0.

D3.0 ELECTRICAL TEST CRITERIA

Table D2 contains the electrical tests for this device and includes all D.C. electrical tests specified in 773050.

D4.0 BIAS CIRCUIT ANALYSIS

Two bias circuits, Figure D5, were evaluated. Bias circuit 1 had all inputs at V_{CC} and bias circuit 2 had the inputs grounded. The Figure D5 plots of device current versus ambient temperature, V_{CC} equal to 2.25 volts, show that the bias circuit 1 supply current was the least through the temperature range tested.

Both bias circuits put the device in the "not selected" mode and, consequently, the output in the high state. A 12 KΩ pull-up resistor was used to limit the output transistor current to less than .5 ma.

TABLE D1. PART CONSTRUCTION DETAILS - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY

A. IDENTIFICATION

1. Part Name: 256 Bit Random Access Memory (93410)
2. Part Manufacturer: Fairchild Semiconductor Corporation
3. Part Number: 773050
4. Date Code: 7250, 7302, 7304, 7308, 7320 (see text)

B. PACKAGE

1. Type: 16-Lead Ceramic/Metal Flatpack
2. Weight: .506 gram
3. Materials:
   a) Lid: Kovar, gold-plated
   b) Leads: Kovar, gold-plated external and internal
   c) Lid Seal: Solder

C. INTERNAL GEOMETRY

1. Interconnections:
   a) Type: Aluminum Wire
   b) Diameter: 0.0012 inch
   c) Bonds:
      1) Aluminum-Aluminum ultrasonic at the die
      2) Aluminum-Gold ultrasonic at the frame

2. Die:
   a) Type: Silicon, Isoplanar
   b) Scribe Method: Mechanical
   c) Dimensions: Date Codes 7302, 7304, 7308, 7320
      0.079 inch x 0.097 inch (Small)
      Date Code 7250
      0.129 inch x 0.100 inch (Large)
   d) Attach Method: Gold eutectic
   e) Glassivation: None

3. Metallization:
   a) Type: Aluminum
   b) Number of Layers: Two
   c) Interlayer Insulation: Silicon Dioxide

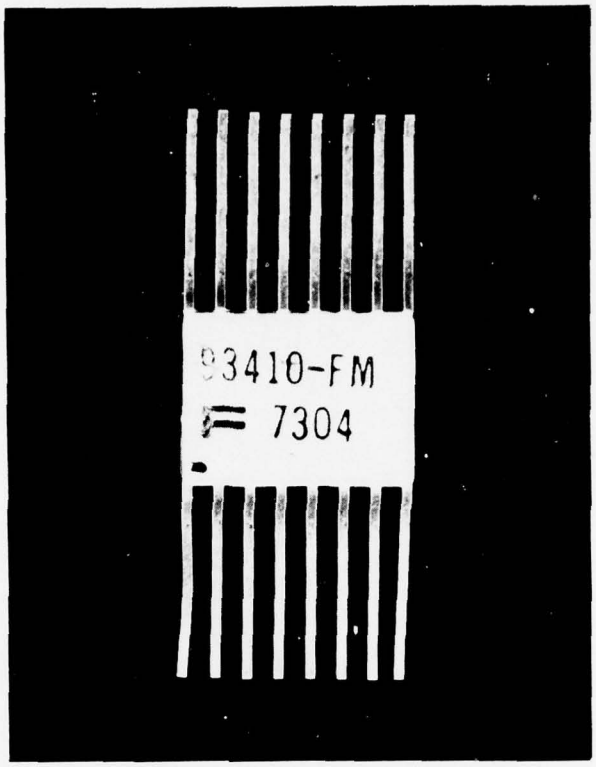

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FIGURE D1. EXTERNAL CONSTRUCTION - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY

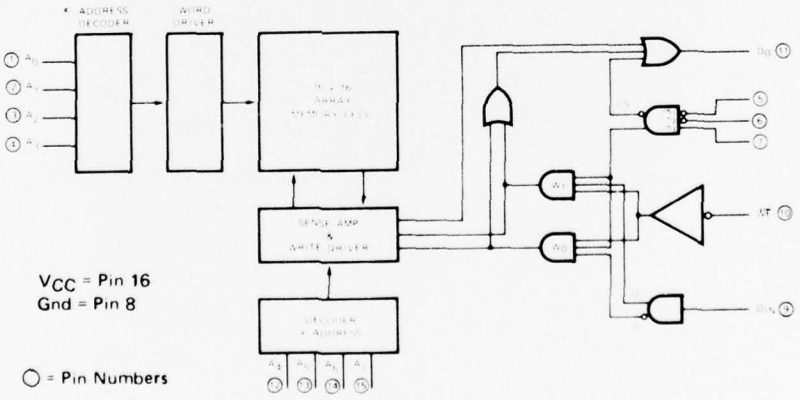
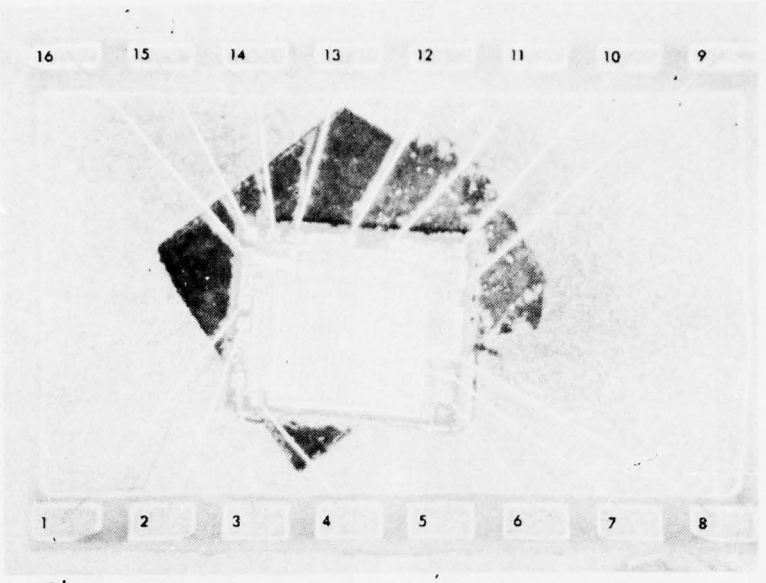


FIGURE D2. LOGIC DIAGRAM - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY



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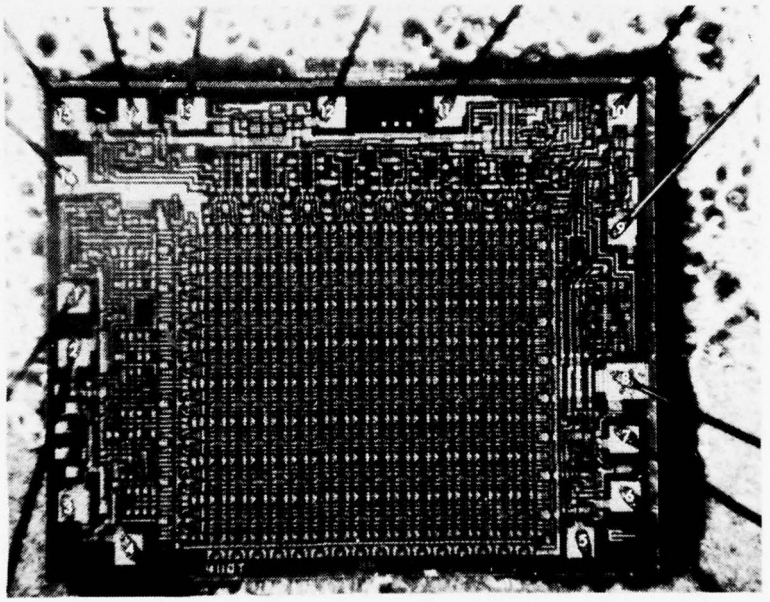
VIEW WITH LID REMOVED



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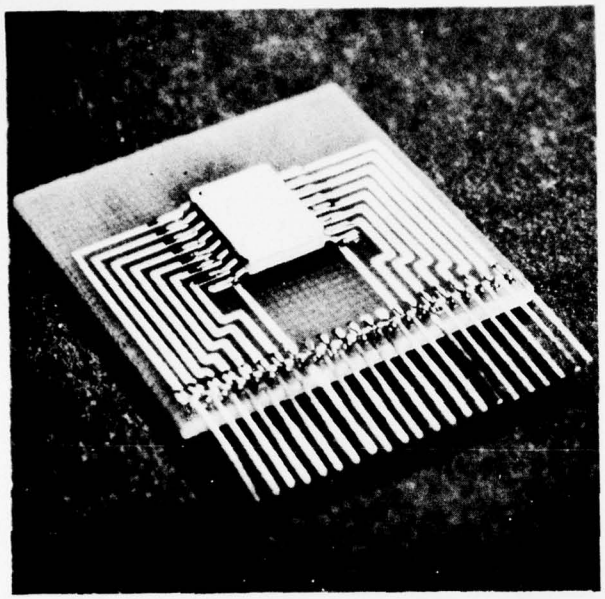
DIE TOPOGRAPHY

FIGURE D3. INTERNAL CONSTRUCTION DETAILS - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY ("SMALL DIE")



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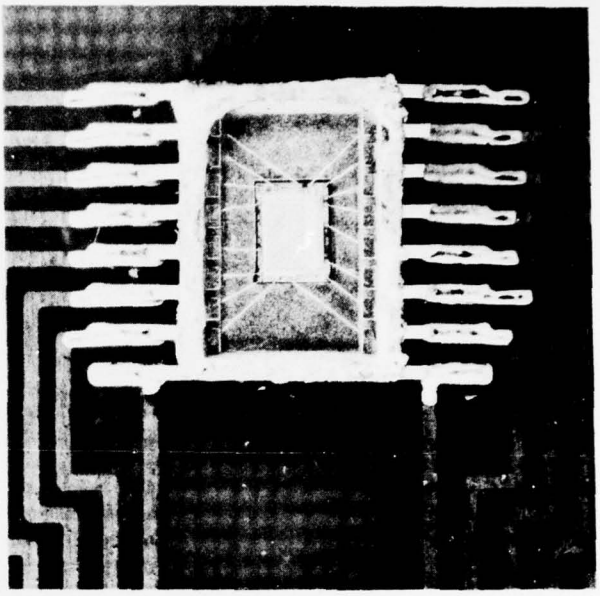

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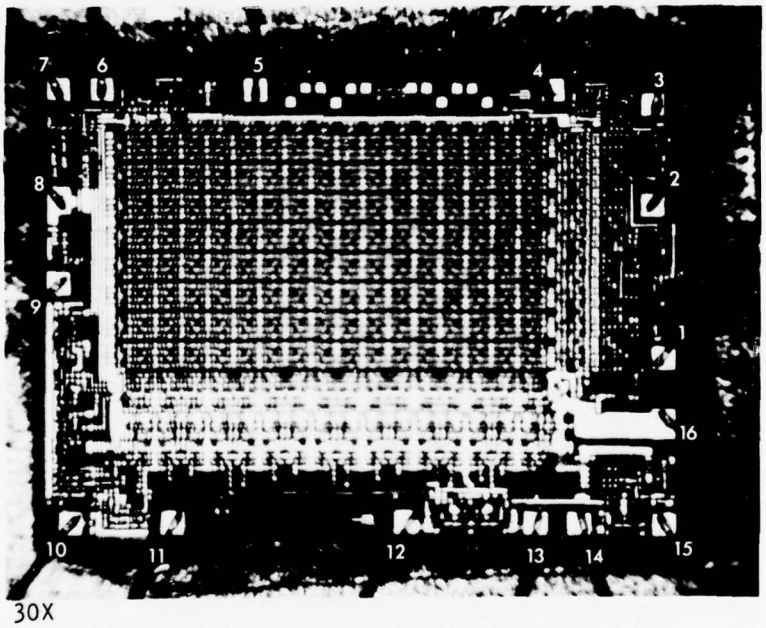
INTERNAL EXTERNAL



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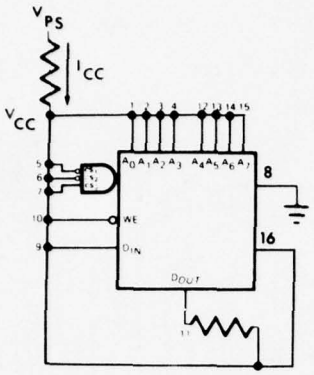
DIE TOPOGRAPHY

FIGURE D4. TYPICAL SAM-D CONFIGURATION - P/N 773429 - 256 BIT RANDOM ACCESS MEMORY ("LARGE DIE")

TABLE D2. ELECTRICAL TEST CONDITIONS - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY

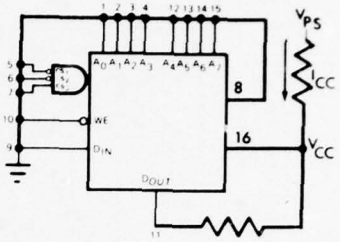
SYMBOL	PIN / TEST NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	MEAS. PIN	TEST LIMITS MIN	MAX	UNITS
V_{CD}	1	-10mA							GND								5.25v	1	-	-1.5	V
V_{CD}	2		-10mA															2	-	-1.5	V
V_{CD}	3			-10mA														3	-	-1.5	V
V_{CD}	4				-10mA													4	-	-1.5	V
V_{CD}	5					-10mA												5	-	-1.5	V
V_{CD}	6						-10mA											6	-	-1.5	V
V_{CD}	7							-10mA										7	-	-1.5	V
V_{CD}	8									-10mA								9	-	-1.5	V
V_{CD}	9										-10mA							10	-	-1.5	V
V_{CD}	10												-10mA					12	-	-1.5	V
V_{CD}	11													-10mA				13	-	-1.5	V
V_{CD}	12														-10mA			14	-	-1.5	V
V_{CD}	13															-10mA		15	-	-1.5	V
I_{IH}	14	4.5v																1	-	20	µA
I_{IH}	15		4.5v															2	-	20	µA
I_{IH}	16			4.5v														3	-	20	µA
I_{IH}	17				4.5v													4	-	20	µA
I_{IH}	18					4.5v												5	-	20	µA
I_{IH}	19						4.5v											6	-	20	µA
I_{IH}	20							4.5v										7	-	20	µA
I_{IH}	21									4.5v								9	-	20	µA
I_{IH}	22										4.5v							10	-	20	µA
I_{IH}	23												4.5v					12	-	20	µA
I_{IH}	24													4.5v				13	-	20	µA
I_{IH}	25														4.5v			14	-	20	µA
I_{IH}	26															4.5v		15	-	20	µA
I_{IL}	27	GND																1	-	-800	µA
I_{IL}	28		GND															2	-	-800	µA
I_{IL}	29			GND														3	-	-800	µA
I_{IL}	30				GND													4	-	-800	µA
I_{IL}	31					GND												5	-	-800	µA
I_{IL}	32						GND											6	-	-800	µA
I_{IL}	33							GND										7	-	-800	µA
I_{IL}	34									GND								9	-	-800	µA
I_{IL}	35										GND							10	-	-800	µA
I_{IL}	36												GND					12	-	-800	µA
I_{IL}	37													GND				13	-	-800	µA
I_{IL}	38														GND			14	-	-800	µA
I_{IL}	39															GND	5.25v	15	-	-800	µA
V_{OL}*	40					GND	GND					16mA					4.75v	11	-	0.45	V
I_{CEX}	41											4.5v					5.25v	11	-	50	µA
I_{CC}	42	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND		GND	GND	GND	GND	5.25v	16	-	135	mA

*A I_O must be stored in the location corresponding to all Address lines HI prior to test.
Initial and final test conducted at +25°C and +125°C. Interim test conducted at +25°C.



V_{CC} = Pin 16
Gnd = Pin 8

BIAS CIRCUIT 1



V_{CC} = Pin 16
Gnd = Pin 8

BIAS CIRCUIT 2

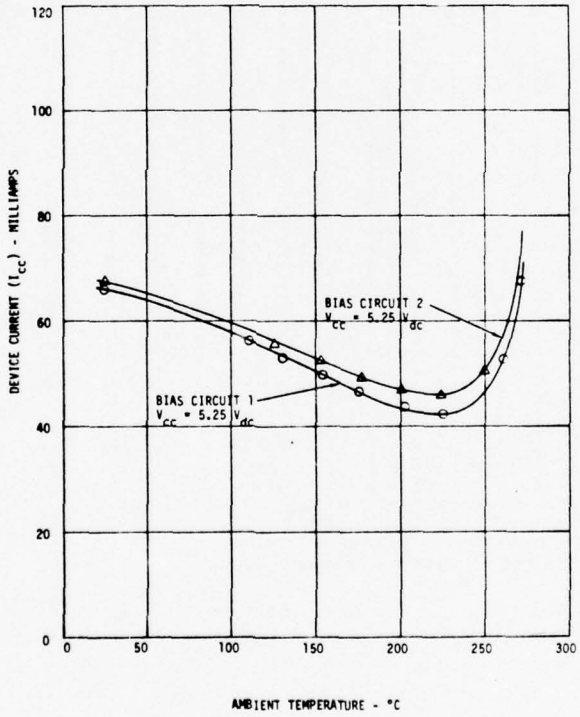


FIGURE D5. BIAS CIRCUIT EVALUATION - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY

Both bias circuits were suitable for the accelerated life test. Bias circuit 1 was selected because its supply current was less than bias circuit 2. Maximum test conditions of 5.25 volts and 250°C ambient temperature were tentatively selected and were the conditions used in the step stress test. A 40Ω current limiting resistor was selected to preclude catastrophic damage in the event of device failure.

D5.0 STEP STRESS TEST RESULTS

A step stress test was performed on twenty devices utilizing bias circuit 1 with V_{CC} equal to 5.25 volts. Four sixteen hour steps, Figure D6, starting at 175°C and concluding at 250°C were performed. One failure was observed after the 175°C step. An input emitter-base junction was found to be shorted due to an electrical overstress caused by either a tester transient or static electricity. No other anomalous condition was observed. Therefore, the test conditions were considered acceptable for the accelerated life test program.

D6.0 LIFE TEST CONDITIONS AND RESULTS

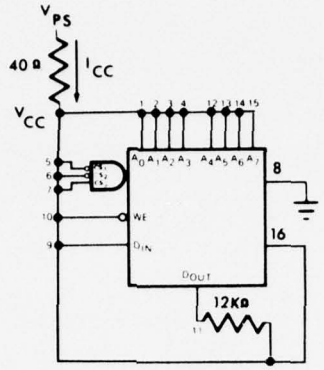
A summary of the life test conditions for each cell is included in Figure D6 and Table D3 summarizes the life test results. All five cells completed 4000 hours of life test; Cell 3, the zero volt cell, was allowed to continue to 6000 hours but produced no additional failures. There were 94 failures of which 23 occurred in each of Cells 2 and 5. There were 25 failures in Cell 1, one in Cell 3, and 21 failures in Cell 4.

D7.0 FAILURE ANALYSIS

Table D4 is a summary of the failure analysis results.

Surface Instability - Channeled Input Clamp Diode - Twelve (12) parts in the powered cells exhibited excessive input current high (I_{IH}), ranging from 21 μA to 83 μA, at one or more input pins. In each instance the failed input displayed a channeled characteristic between the input and ground. Via die level probing after severing appropriate metallization stripes, the excessive leakage was isolated to the input clamp diodes. Figure D7 illustrates the channeled type reverse characteristics displayed by two degraded clamp diodes in one part. In each instance the excessive leakage was bake reversible, indicative of a surface

STEP STRESS AND LIFE TEST CIRCUIT



V_{CC} = Pin 16
Gnd = Pin 8

STEP STRESS TEST - FAILURE SUMMARY (20 DEVICES)

AMBIENT TEMP. (°C)	V_{CC} (V)	CUMULATIVE FAILURES
175	5.25	1
200	5.25	1
225	5.25	1
250	5.25	1

LIFE TEST CONDITIONS

TEST CELL NUMBER	T_A AMBIENT TEMPERATURE (°C)	V_{CC} DEVICE VOLTAGE (VOLTS)	I_{CC} DEVICE CURRENT (MILLIAMPS)	P_D POWER DISSIPATION (MILLIWATTS)	T_J JUNCTION TEMPERATURE (°C)
1	250	5.25	47	247	266
2	250	3.50	36	126	258
3	250	0	0	0	250
4	225	5.25	42	221	242
5	200	5.25	44	231	219

FIGURE D6. STEP STRESS RESULTS AND LIFE TEST CONDITIONS - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY

TABLE D3. LIFE TEST SUMMARY - P/N 773050 -
256 BIT RANDOM ACCESS MEMORY

TEST CELL DESCRIPTION				CUMULATIVE FAILURES AT HOURS OF TEST											
CELL NO.	APPLIED BIAS	AMBIENT TEMP.	QTY	4	12	16	32	64	128	256	512	1000	2500	4000	6000
1	5.25 VDC	250°C	30	1	2	2	2	2	2	3	5	9	18	25*	
2	3.5 VDC	250°C	30	0	0	0	0	0	0	1	3	5	19	23*	
3	0 VDC	250°C	30	1	1	1	1	1	1	1	1	1	1	1	1*
4	5.25 VDC	225°C	30	0	0	0	1	3	4	4	7	10	14	21*	
5	5.25 VDC	200°C	30	0	0	0	1	1	1	3	10	14	22	23*	

*Test terminated

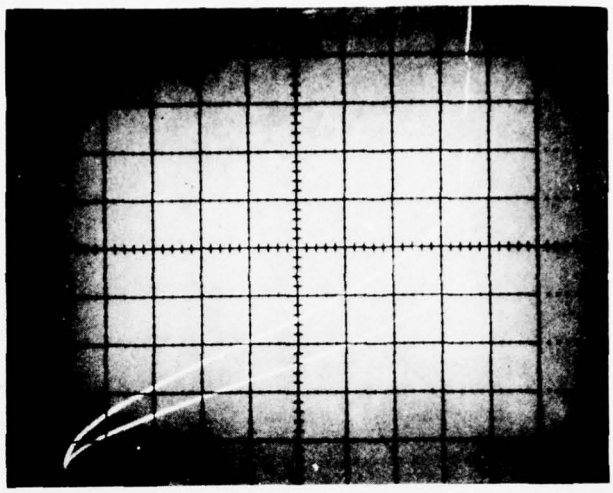
TABLE D4. FAILURE ANALYSIS SUMMARY - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY

	A. FAILED PARAMETER B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TIME (HOURS) OF FAILURE					STEP STRESS
		250°C			225°C	200°C	
		5.25V	3.5V	0V	5.25V	5.25V	
		CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	
SURFACE INSTABILITY FAILURES	A. I_{IH} (INPUT CHANNELED) B. CHANNELED CLAMP DIODE C. DRIFT OF MOBILE IONS D. CONTAMINATION IN THE PASSIVATION	1@4 1@512 1@1000	1@256 1@512 1@1000 1@2500		1@32 2@1000	1@32 1@1000	
	A. I_{CEX} (OUTPUT CHANNELED)("LARGE" DIE ONLY) B. EXCESSIVE COLLECTOR LEAKAGE DUE TO INVERSION OF THE P-TYPE SUBSTRATE C. CATION DRIFT D. CONTAMINATION IN THE PASSIVATION	1@256 2@1000 1@2500	5@2500 3@4000		1@512 1@1000 2@2500 4@4000	2@256 6@512 3@1000 8@2500	
BULK AND MECHANICAL FAILURES	A. I_{IH} (INPUT SHORTED) B. WIRE-TO-DIE SHORT C. SAGGING OF THE Al WIRE D. INSUFFICIENT INITIAL CLEARANCE DUE TO MISPLACED BOND	1@4 1@12	1@2500				
	A. V_{OL} ("LARGE" DIE ONLY) B. E-B DEGRADATION IN THE OUTPUT TRANSISTOR, Q1 C. ALUMINUM SPEARING D. HIGH DISSIPATION DUE TO OUTPUT STATE CHANGE	1@1000 5@2500 1@4000	10@2500 4@4000		2@2500 6@4000		
	A. I_{IH} (PIN 9 DEGRADED) B. DEGRADED CLAMP DIODE C. PROBABLY A FORM OF ALUMINUM SPEARING D. PROBABLY A SECONDARY EFFECT OF THE OUTPUT STATE CHANGE	3@2500 1@4000	2@4000		2@4000		
	A. V_{OL} (OUTPUT STUCK HIGH) B. OPEN IN THE V_{CC} STRIPE C. ALUMINUM ELECTROMIGRATION D. CURRENT DENSITY IN THE STRIPES	1@1000 4@2500 6@4000	1@1000 1@2500		1@128 1@2500 1@4000	1@4000	
	A. I_{CEX} (OUTPUT STUCK LOW) B. STRIPE TO STRIPE SHORT C. ALUMINUM ELECTROMIGRATION D. CURRENT DENSITY IN THE STRIPES	1@512 1@1000	1@512 1@2500		1@64 2@512 1@2500	1@512 1@1000	
TEST ERROR	A. I_{IH} (INPUT SHORTED) B. SHORTED INPUT E-B JUNCTION C. ELECTRICAL OVERSTRESS D. TESTER TRANSIENT OR STATIC ELECTRICITY		2@2500	1@4	1@64 1@4000		1@175°C STEP
	TOTAL NUMBER OF FAILED PARTS (Columns do not add up to the total number of failed parts because many parts contained more than one failure mechanism.)	25	23	1	21	23	1

instability mechanism. During life test, all inputs were connected to V_{CC}, thus the clamp diodes were reverse biased. Therefore, the degradation was attributed to drift of mobile ions or charges in or on the passivation under the influence of the reverse bias.

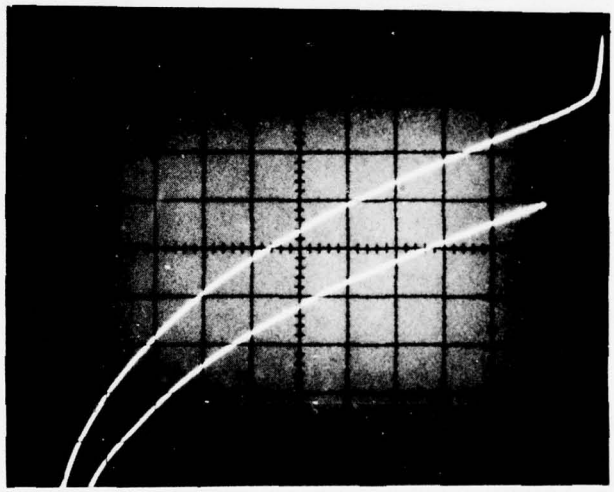
Surface Instability - Channeled Output - Thirty-nine (39) parts in the powered cells failed due to excessive output cut-off current (I_{CEX}), ranging from 51 μA to 350 μA. Each part displayed a channeled characteristic from the output to ground as illustrated in Figure D8. Via die level probing and stripe severing, the degradation was traced to leakage from the collector of the output transistor (Q1) to the collector of transistor Q2 as shown schematically in Figure D9. The leakage current flowed between the collector tubs of Q1 and Q2 and the leakage could be eliminated by baking the part or removing the SiO_2 passivation. These findings indicated that the leakage was the result of the formation of a channel in the substrate due to inversion of the p-type material as illustrated in Figure D10. The inversion of the p-type silicon was caused by accumulation of a net positive charge in the SiO_2 passivation at the silicon/SiO_2 interface where shown in Figure D10. It is believed that the accumulation resulted from drift of mobile cations in the SiO_2 under the metallization stripe connecting the emitter of Q2 and the collector of Q1. Only the 7250 date coded parts exhibited this failure mechanism. As shown in Figure D11, in the 7250 parts Q1 and Q2 are adjacent and the connecting stripe passes over the SiO_2 between their collector tubs. During life test this stripe was biased positive with respect to the substrate (V_{OUT} was high). Positive bias on this stripe would drive mobile cation contamination in the SiO_2 to the interface as illustrated in Figure D10. As shown in Figure D12, in the 73XX parts Q1 and Q2 are not adjacent and thus did not exhibit this failure mechanism.

Wire-to-Die Shorts - Three parts failed I_{IH} at an input due to a high resistance (2 KΩ to 4 KΩ) short between the input and ground. The short was traced to contact between the internal aluminum interconnect wire and the edge of the substrate (ground). In each instance the wire bond at the die had been misplaced such that the heel of the bond was situated almost in the scribe area as shown in Figure D13. The bond placement plus the inherently shallow angle between the wire and the die of this type of bond resulted in insufficient clearance. In the earliest (4 and



HORIZ. = 2 VOLTS/DIV
VERT. = 50 μA/DIV

FIGURE D7. REVERSE I-V CHARACTERISTICS OF THE PIN 9 CLAMP DIODE (TOP TRACE) AND THE PIN 10 CLAMP DIODE (BOTTOM TRACE) OF A DEVICE THAT FAILED I_{IH} AT PINS 9 AND 10 - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY



HORIZ. = 0.5 VOLTS/DIV.
VERT. = 10 μA/DIV.

FIGURE D8. OUTPUT (+) TO GROUND I-V CHARACTERISTICS OF A PART THAT FAILED I_{CEX}. THE TOP TRACE IS OUTPUT TO GROUND WITH ALL OTHER PINS OPEN. THE BOTTOM TRACE IS OUTPUT TO GROUND WITH THE DEVICE BIASED USING THE CONDITIONS OF THE I_{CEX} TEST - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY

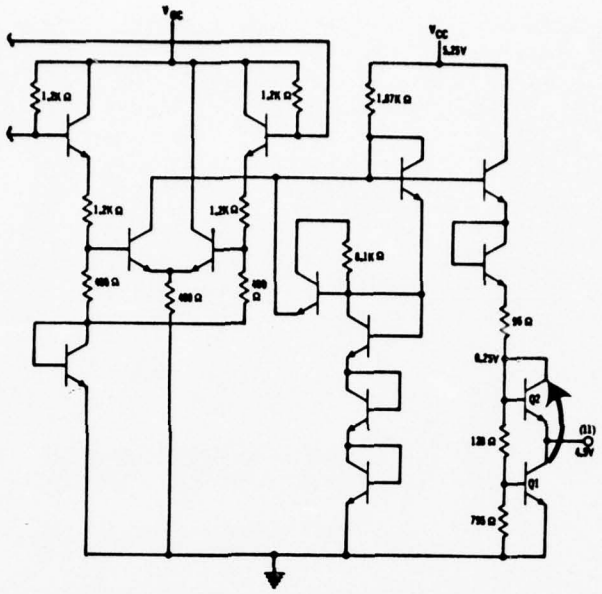


FIGURE D9. ELECTRICAL SCHEMATIC OF THE OUTPUT STAGE SHOWING THE LOCATION OF THE LEAKAGE PATH (ARROW) THAT RESULTED IN THE I_{CEX} FAILURES AND SHOWING SOME OF THE NODE VOLTAGES DURING THE I_{CEX} TEST - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY

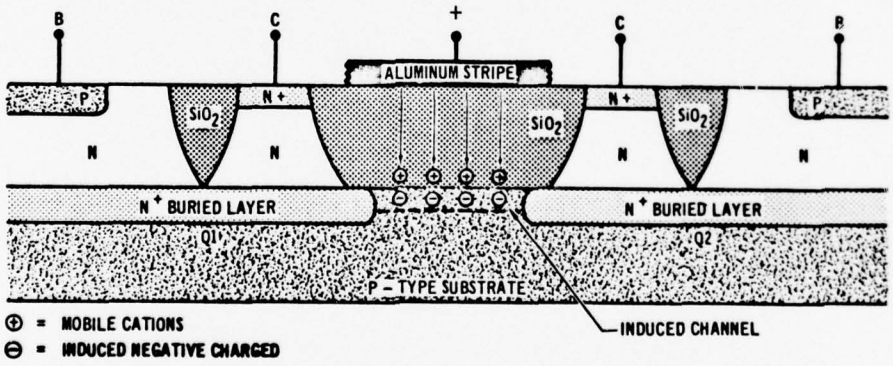
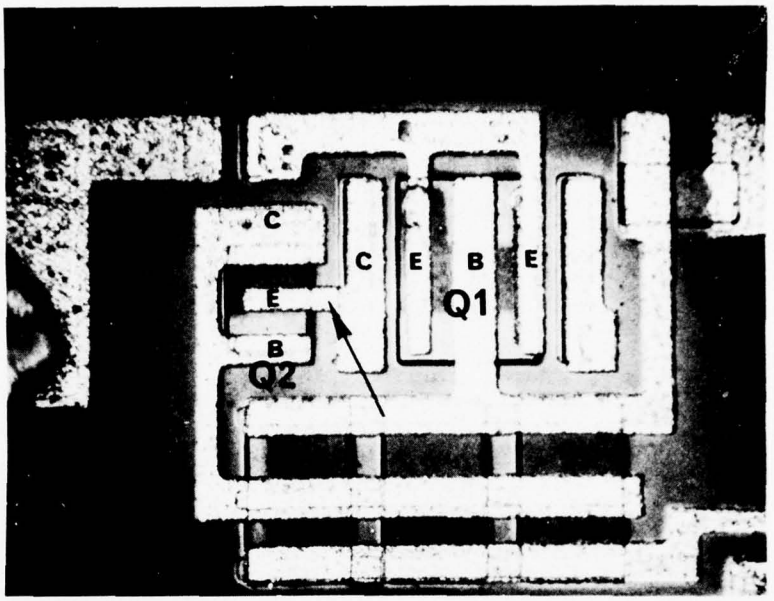
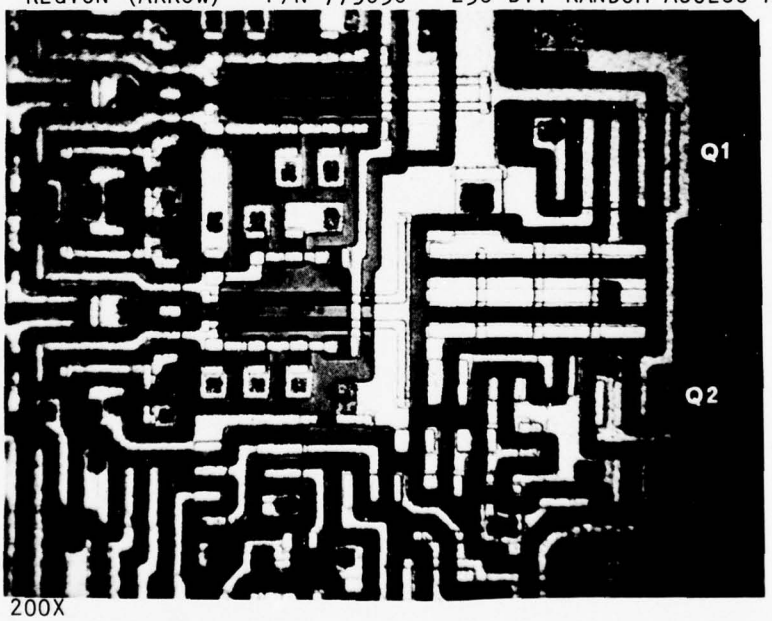


FIGURE D10. CROSS-SECTIONAL SKETCH (NOT TO SCALE) OF Q1 AND Q2 SHOWING THE INVERSION LAYER (INDUCED CHANNEL) IN THE P-TYPE SUBSTRATE AND HOW IT FORMED - P/N 773050-- 256 BIT RANDOM ACCESS MEMORY



395X

FIGURE D11. OUTPUT TRANSISTORS (AFTER REMOVING THE UPPER LEVEL METAL) OF A 7250 DATE CODE PART SHOWING WHERE THE STRIPE INTERCONNECTING THE Q1 COLLECTOR AND THE Q2 EMITTER PASSES OVER THE INVERTED REGION (ARROW) - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY



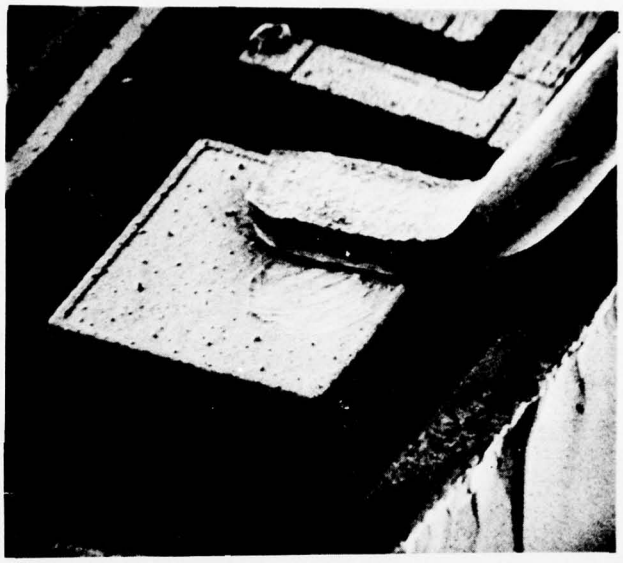
200X

FIGURE D12. OUTPUT STAGE (AFTER REMOVING THE UPPER LEVEL METAL) OF A 7304 DATE CODE PART SHOWING THE LOCATION OF Q1 AND Q2 - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY

12 hour) failures the wire probably was actually touching the die, but no short existed due to the rectifying nature of the contact or due to a residual oxide layer. After an exposure to high temperature, the barrier was penetrated, resulting in a measurable short. In the later (2500 hour) failure, the wire probably was not touching and required a period of time and temperature to sag or creep before contact occurred.

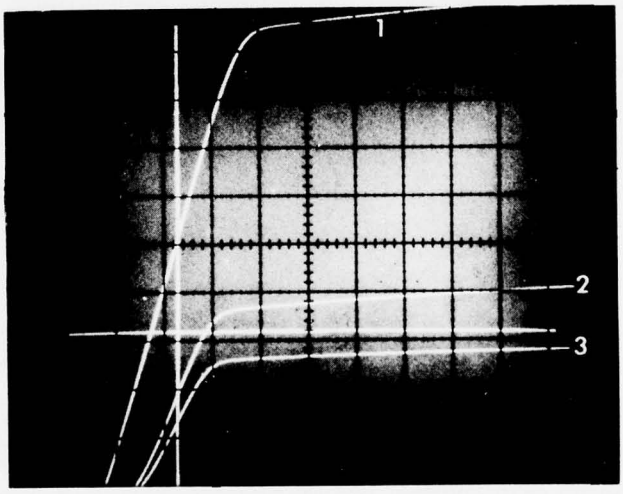
V_{OL} Failure - Twenty-nine (29) parts failed output voltage low (V_{OL}) traced to degradation of the DC gain of the output transistor. Due to low gain, the output transistor would not fully saturate during the V_{OL} test causing two ranges of failed valued as illustrated in Figure D14. Figure D14 shows the output I-V characteristics of three parts with the output in the low state. The superimposed horizontal line is the V_{OL} test current level of 16 mA and the vertical line is the specified maximum V_{OL} limit of .45 volt. Trace 1 is that of a normal unstressed part; V_{OL} in this instance is .34V. Traces 2 and 3 are those of two types of V_{OL} failure. In case 2 the characteristic intersects the 16 mA level in the linear region and, due to the low gain, V_{OL} is greater than .45V. Failed parts of this type exhibited V_{OL} values usually ranging from .46 to .60 volt. In case 3 the characteristic saturates before the linear portion reaches 16 mA and does not intersect 16 mA until the output avalanches. Failed parts of this type exhibited V_{OL} values usually ranging from 6.2 to 7.6 volts.

Die level probing established that the gain of the output transistor was usually less than 1 and that the low gain was due to degradation of the emitter-base junction of Q1. The emitter junctions exhibited resistive shorts ranging from 1K ohm, as illustrated in Figure D15, to as low as 100 ohms. The shorts were caused by aluminum spikes or "spears" emanating from the emitter ohmic contacts as shown in Figures D16 through D18. The emitters are "washed" emitters and the spears penetrated the vertical sidewalls of the junction, causing the shorts. The spears are the result of dissolution of silicon into the aluminum and subsequent lateral migration of aluminum into the silicon. This mechanism can be the result of localized power dissipation. All of these failures occurred in the 225°C or 250°C powered cells; no such failure occurred in the 200°C cell. Thus, these findings suggested that the output state of the failed parts may have switched from the intended off-state to an on-state (higher dissipation level) at the



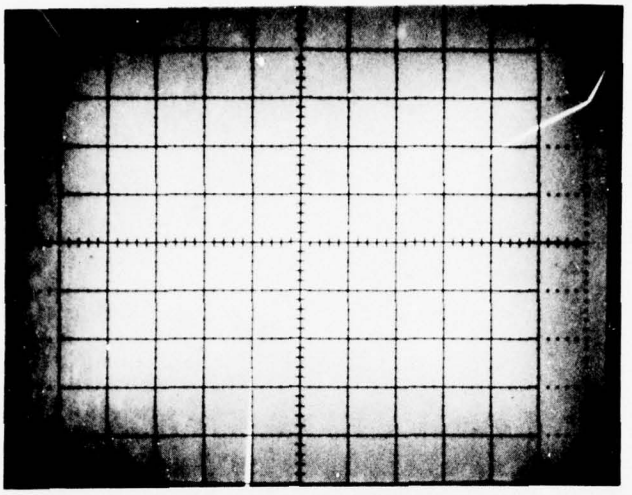
200X (SEM)

FIGURE D13. SEM PHOTO OF A MISPLACED WIRE BOND (AFTER LIFTING THE WIRE TO CLEAR THE SHORT) - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY



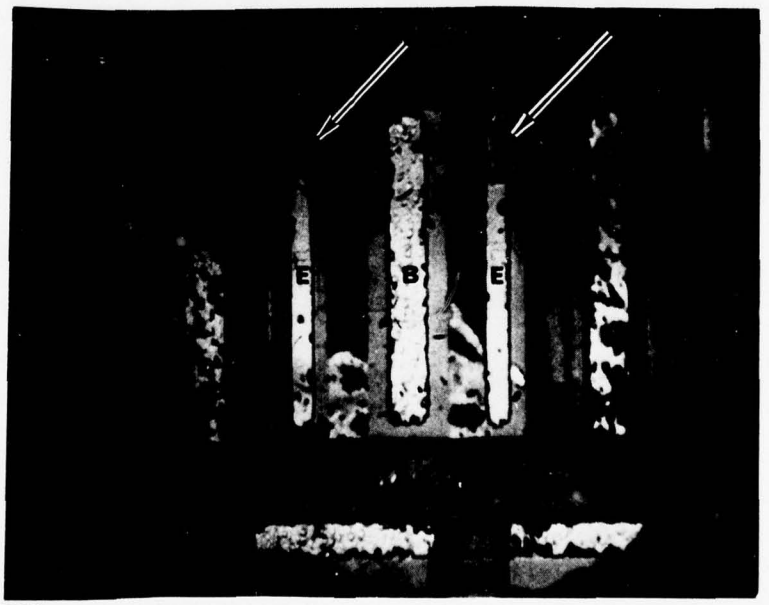
HORIZ. = 0.2 VOLT/DIV.
VERT. = 5 mA/DIV.

FIGURE D14. OUTPUT LOW, I-V CHARACTERISTICS OF TWO FAILED PARTS (TRACES 2 AND 3) AND, FOR COMPARISON, A NORMAL UNSTRESSED PART (TRACE 1) - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY



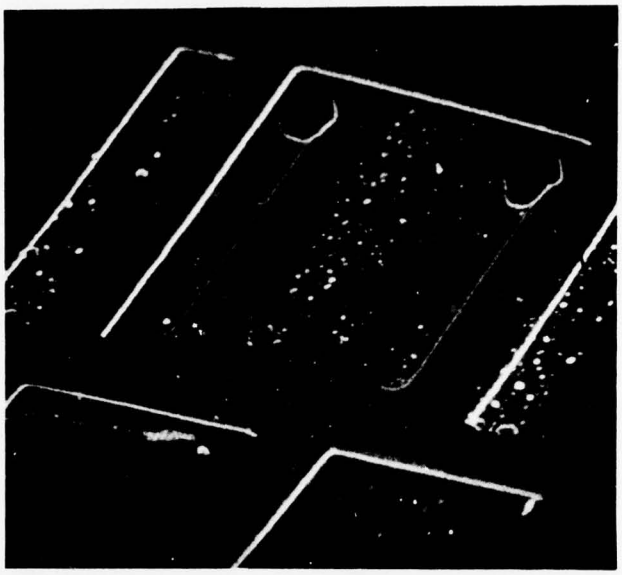
HORIZ. = 1 VOLT/DIV.
VERT. = 2 mA/DIV.

FIGURE D15. FORWARD (3RD QUADRANT) AND REVERSE (1ST QUADRANT) I-V CHARACTERISTICS OF THE EMITTER BASE JUNCTION OF A Q1 TRANSISTOR WITH LOW DC GAIN - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY



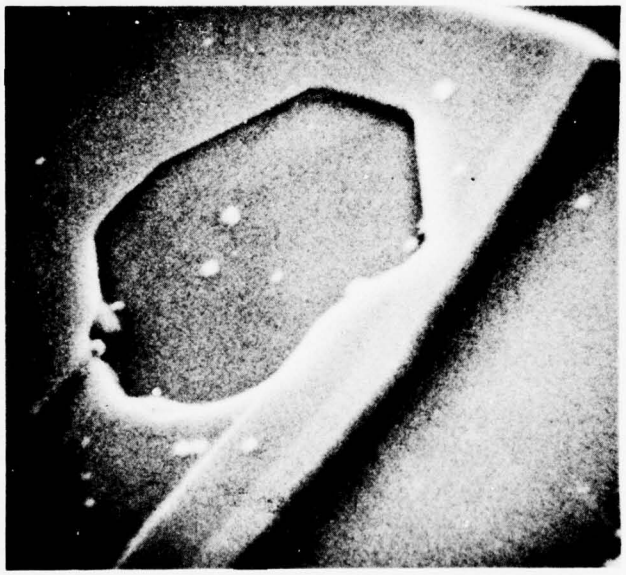
750X

FIGURE D16. OPTICAL PHOTO OF A Q1 OUTPUT TRANSISTOR AFTER METALLIZATION REMOVAL SHOWING THE ALUMINUM SPEARS (ARROWS) IN THE EMITTERS - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY



1000X (SEM)

FIGURE D17. SEM PHOTO OF A Q1 TRANSISTOR AFTER OXIDE REMOVAL SHOWING THE ALUMINUM SPEARS (ARROWS) PENETRATING THE EMITTER JUNCTIONS - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY



10,000X (SEM)

FIGURE D18. SEM CLOSEUP OF AN EMITTER SPEAR AFTER ETCHING THE SILICON LIGHTLY TO SHOW THE AMOUNT OF DAMAGE CAUSED BY THE SPEAR - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY

higher temperatures. To investigate this, plots of V_{OUT} versus temperature in the life test circuit were obtained for sample parts. This disclosed that the parts do exhibit a transition from the high state to a low state between 200°C and 250°C, as illustrated in Figure D19, which explains the presence of the spearing mechanism. Although Q1 is physically the same in both the 7250 and the 73XX devices, only the 7250 date code devices exhibited this failure mechanism. Figure D19 suggests that this may have been due to the fact that the 7250 devices may be more prone to switch to a low state at the higher temperatures.

Degraded Pin 9 Clamp Diode - Eight parts failed I_{IH} at pin 9. The failed values ranged from 117 μA to 204 μA. All other inputs of each device displayed normal I_{IH} values. Each part exhibited exponentially increasing, excessive leakage from pin 9 to ground as illustrated in Figure D20. Via die level probing, the leakage was isolated to a degraded clamp diode. The leakage was not bake reversible, but microscopic examinations and chemical etchings of defective diodes did not reveal any bulk deficiency. Although no visible evidence existed, it is believed that degradation was caused by an aluminum migration/penetration mechanism similar to that discussed in the previous section. The pin 9 diode is located near the output transistor as can be seen in Figure D11. All but one of these eight parts failed V_{OL} due to aluminum spearing caused by output transistor power dissipation. Thus, it is suspected that the clamp diodes degraded similarly as a result of their proximity to the output transistor.

Aluminum Electromigration Failures - Seventeen (17) parts failed V_{OL} and 10 parts failed I_{CEX} in the powered cells during the life test. The output of the V_{OL} failures was stuck in the high state and could not be switched to an on state. Consequently, the measured value of V_{OL} was the avalanche breakdown voltage of the output which is about 6-7 volts. The output of the I_{CEX} failures was stuck in the low state and could not be switched to an off state. Consequently, the measured value of I_{CEX} was approximately the maximum short-circuit current of the test supply which is about 400 mA. After curve tracer pin-pin tests disclosed no anomaly, the parts were delidded and examined. The V_{CC} and the ground metallization stripes of each part contained aluminum electromigration effects. The high potential ends (toward which the electron current flowed) of ground stripes and the V_{CC} bond pad contained hillock and whisker growth from accumulation of aluminum as illustrated in

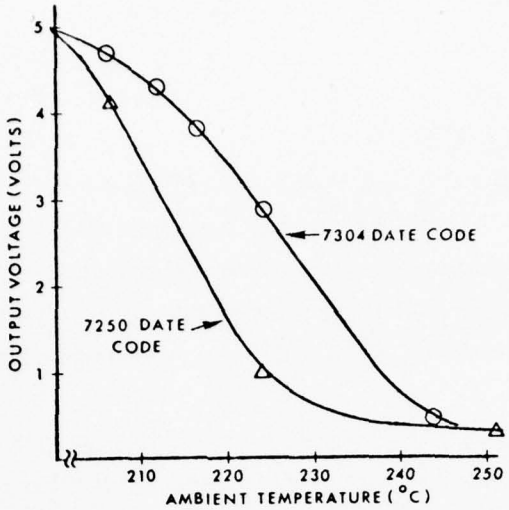
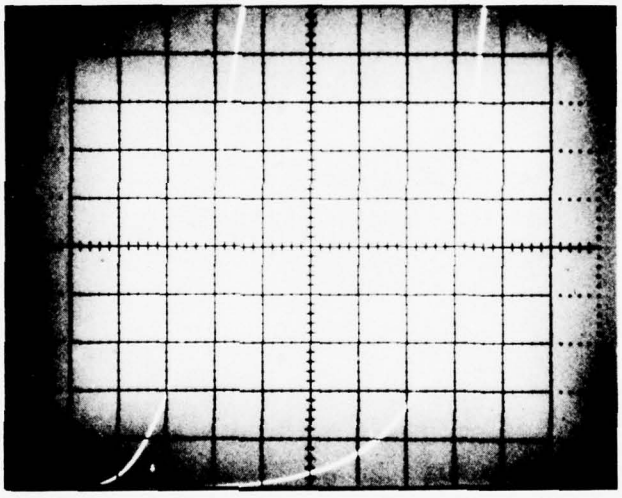


FIGURE D19. OUTPUT VOLTAGE VS. AMBIENT TEMPERATURE OF TWO SAMPLE PARTS (V_{CC} = 5.25V, R_S = 12K OHMS) - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY



HORIZ. = 0.5 VOLT/DIV.
VERT. = 100 μA/DIV.

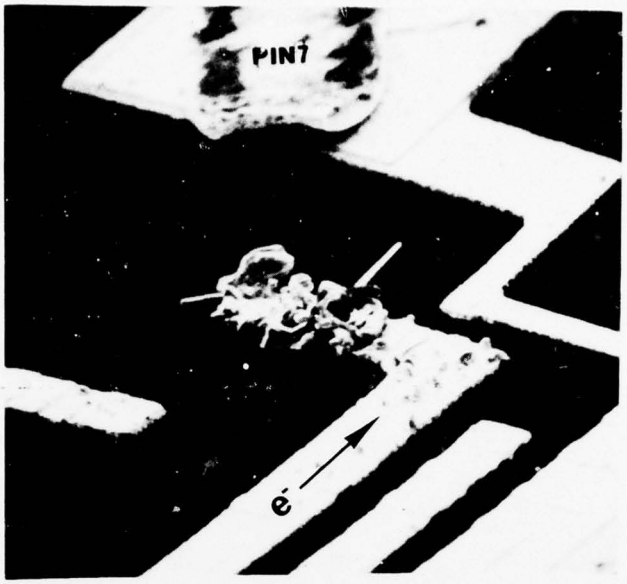
FIGURE D20. PIN 9 (+) TO GROUND LEAKAGE DISPLAYED BY TWO PARTS THAT FAILED $I_{IH(9)}$. (L/H TRACE = S/N 333 WHICH FAILED IN CELL 4 AT 4000 HOURS: R/H TRACE = S/N 94 WHICH FAILED IN CELL 1 AT 2500 HOURS) - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY

Figures D21 through D23. The ground pad contained voids from depletion of aluminum as shown in Figure D24.

Troubleshooting of the output stage (see Figure D9) of both V_{OL} and I_{CEX} failures disclosed that in each instance the entire output stage functioned properly and, therefore, that the malfunction causing the outputs to stick high or low was in a preceding stage. Because no complete electrical schematic of the rest of the circuit was available, Fairchild Semiconductor was contacted. It was learned that the schematics and component layout diagrams were proprietary and considerable time would be involved in order to obtain them. As an alternative, Fairchild offered to perform the troubleshooting in their facilities. Therefore, to avoid any delay to the program, representative failed parts were sent to Fairchild for analysis. Fairchild determined that the stuck high (V_{OL}) failures were caused by open circuits in a V_{CC} stripe at a via between an upper level stripe and a lower level stripe as a result of the electromigration as shown in Figure D25. The stuck low (I_{CEX}) failures were caused by a short-circuit between the 2ϕ reference voltage stripe and a lower level ground stripe. Hillock or whisker growths in the ground stripe punctured the insulating glassivation layer and shorted to the 2ϕ line as shown in Figure D26.

Both the V_{OL} and the I_{CEX} failures were the result of aluminum electromigration. The damage was severe and widespread, which indicates that it was caused primarily by prolonged exposure to elevated temperature and high current densities in the stripes. Since the mechanism is current dependent, these failures were not storage related. Therefore, the parts were not investigated further to determine if any anomaly such as excessive supply current or a metallization deficiency may have contributed to the failures.

Shorted Inputs - Six parts exhibited excessive I_{IH} at a pin traced to an emitter-base short in the input transistor. Each transistor contained a small damage site (melted silicon-aluminum) on the emitter junction, as illustrated in Figure D27. The damage is characteristic of electrical overstress due to a static discharge or voltage transient. The input emitters are "washed" emitters and, therefore, would tend to be susceptible to transients.

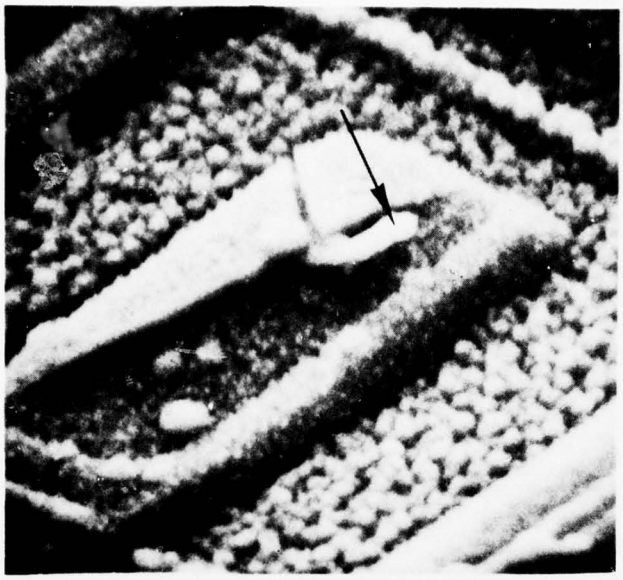


300X (SEM)

FIGURE D21. SEM PHOTO OF HILLOCKS AND WHISKER GROWTH AT THE END OF AN UPPER LEVEL GROUND STRIPE - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY

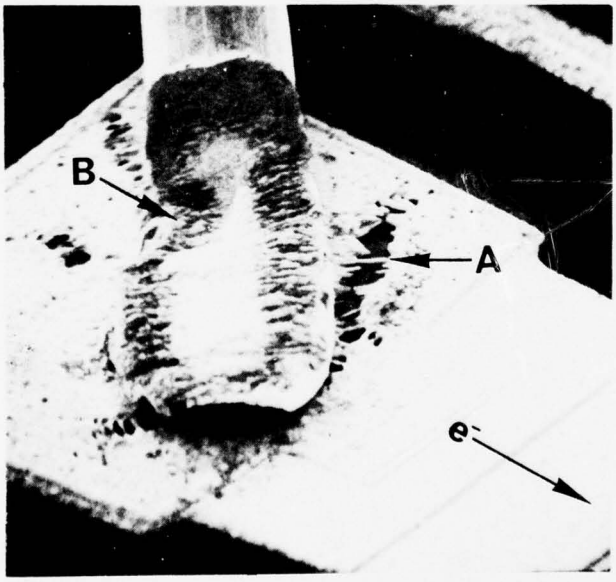
300X (SEM)

FIGURE D22. SEM PHOTO OF HILLOCK GROWTH IN THE V_{CC} PAD AND BOND - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY



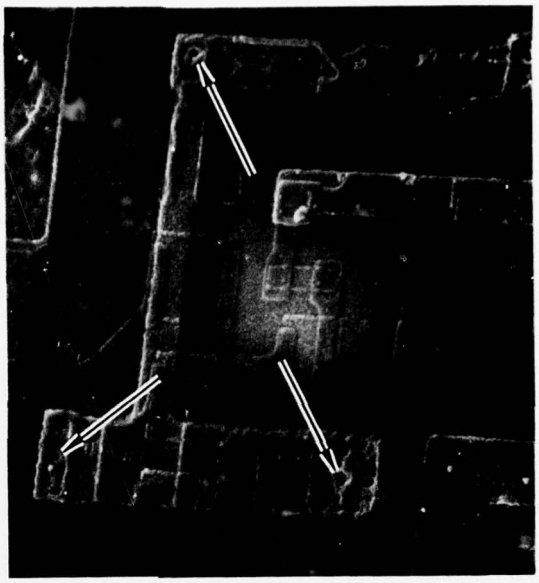
3500X (SEM)

FIGURE D23. SEM PHOTO OF A HILLOCK (ARROW) AT THE END OF A LOWER LEVEL GROUND STRIPE THAT PROTRUDED THROUGH THE INSULATION LAYER - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY



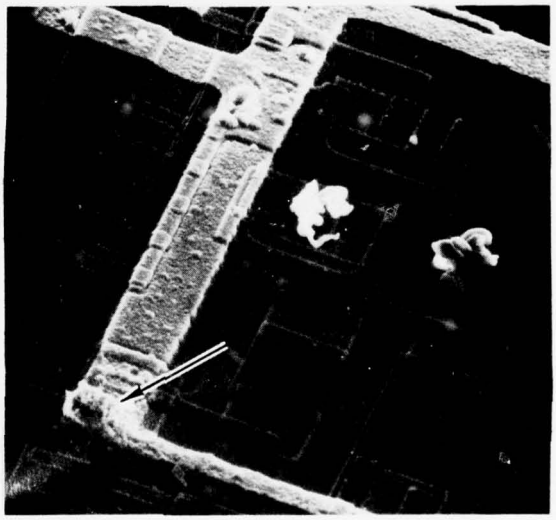
400 (SEM)

FIGURE D24. SEM PHOTO OF THE GROUND PAD SHOWING VOIDS IN THE PAD (A) AND DEPLETION OF ALUMINUM (B) FROM THE BOND FOOT - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY



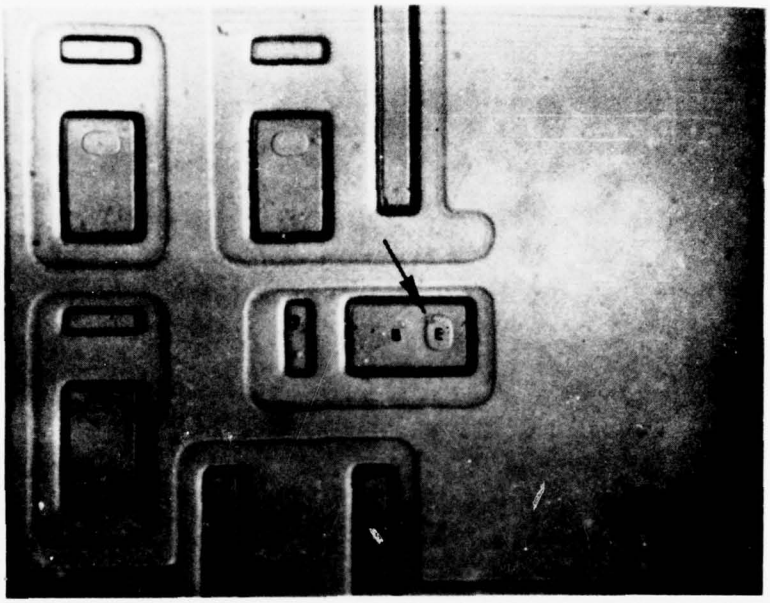
440X (SEM) (COURTESY OF FAIRCHILD SEMICONDUCTOR)

FIGURE D25. SEM PHOTO OF VOIDS (ARROWS) IN THE UPPER V_{CC} STRIPE AT THE VIAS - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY



650X (SEM) (COURTESY OF FAIRCHILD SEMICONDUCTOR)

FIGURE D26. SEM PHOTO OF THE 2ϕ REFERENCE VOLTAGE STRIPE SHOWING WHERE A HILLOCK IN THE LOWER LEVEL GROUND STRIPE SHORTED TO THE 2ϕ LINE (ARROW) - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY



750X

FIGURE D27. PIN 10 INPUT TRANSISTOR AFTER 5 SECOND SILICON ETCH SHOWING THE DAMAGE SITE (ARROW) ON THE EMITTER-BASE JUNCTION - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY

D8.0 DATA CORRELATION

The delivered test samples included two different integrated circuit dice and five date codes (7250, 7302, 7304, 7308, and 7320). The 7250 date codes had the "large" die shown in Figure D4. The 73XX date codes had the "small" die shown in Figure D3. This nonhomogeneity of parts was recognized after the start of the accelerated life tests. Coordination with MICOM resulted in the decision to continue the test program with the delivered parts and to analyze the data in homogeneous groups where possible. Sixty-one percent of the life test parts were the "large" die configuation.

The Table D4 failure analysis summary reveals a large number of failures attributed to the following failure mechanisms.

- o Drift of mobile ions in the thermal oxide
- o Cation drift
- o Aluminum spearing
- o Aluminum electromigration
- o Electrical overstress
- o Sagging of aluminum wire.

The electrical overstress is not applicable for data analysis and the three failures attributed to the sagging aluminum wire are insufficient for analysis. Each of the remaining failure mechanisms will be discussed below for applicability for data analysis.

Drift of Mobile Ions in the Thermal Oxide - The 12 failures attributed to this mechanism were equally divided between the large and small dice and the failures were distributed among the four powered test cells. The resultant distribution of failures was insufficient for data analysis.

Cation Drift - The 39 failures attributed to this mechanism occurred in the large dice only. The failures were distributed among the four powered test cells with Cell 5, the lowest temperature test cell (200°C), experiencing 19 failures. The Cell 5 data is adequate for analysis but the other cells are not, because of an output state change which is discussed in the following paragraphs.

The cation drift mechanism appeared only in those test cells having an applied bias, but insufficient data is available in Cells 1 and 2 to establish if an Eyring model voltage sensitivity exists.

Aluminum Spearing - Thirty-seven (37) failures were attributed to aluminum spearing, a condition caused by localized overheating. All failures were attributed to the large dice and occurred in all powered cells excepting Cell 5 (200°C). The localized overheating is attributed to a change in the output state (higher dissipation level) at temperatures above 225°C. These failures are considered nonapplicable for data analysis purposes because the failures were induced by the change in output state and subsequent heating.

Aluminum Electromigration - Twenty-seven (27) failures were attributed to aluminum electromigration, a condition which occurred in all the powered test cells and in both the large and small dice. The majority of these failures occurred late in test and were not considered applicable for a storage environment analysis because they were current density induced.

The data available for analysis has been significantly reduced by the presence of two different integrated circuit dice, the occurrence of the aluminum electromigration and spearing failure mechanisms, and the output state change which was encountered by the biased test cells operating at temperatures of 225°C and above. The net effect of these various factors is to reduce the quantity of applicable data for analysis. This results in Cell 5 (200°C, 5.25 volts) being the only cell having sufficient data for analysis.

Since these failures were induced under an applied bias life test, the analysis results will be conservative when applied to a zero volt condition. The applicable failures for data analysis are summarized in Table D5. Only Cell 5 has sufficient data for analysis and the cumulative failure distribution is shown in Figure D28. The "S" shaped curve is typical for a bimodal lognormal distribution, and the resultant "freak" and "main" populations are included. The lack of data at another temperature precludes the calculation of an activation energy and the subsequent solution to the Arrhenius equation. However, a likely range of

TABLE D5. APPLICABLE FAILURES FOR DATA ANALYSIS - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY

A. FAILED PARAMETER	QUANTITY OF FAILURES AND TIME OF FAILURE (HOURS)				
B. FAILURE MODE	250°C			225°C	200°C
C. FAILURE MECHANISM	5.25V	3.5V	OV	5.25V	5.25V
D. CAUSE OF FAILURE	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5
A. I_{CEX} (OUTPUT CHANNELED)	1@256	2@2500		1@512	2@256
B. EXCESSIVE COLLECTOR LEAKAGE DUE TO INVERSION OF THE P-TYPE SUBSTRATE	1@1000			1@1000	6@512
C. CATION DRIFT	1@2500			1@2500	3@1000
D. CATION CONTAMINATION					8@2500
TOTAL NUMBER OF FAILED PARTS	3	2	0	3	19

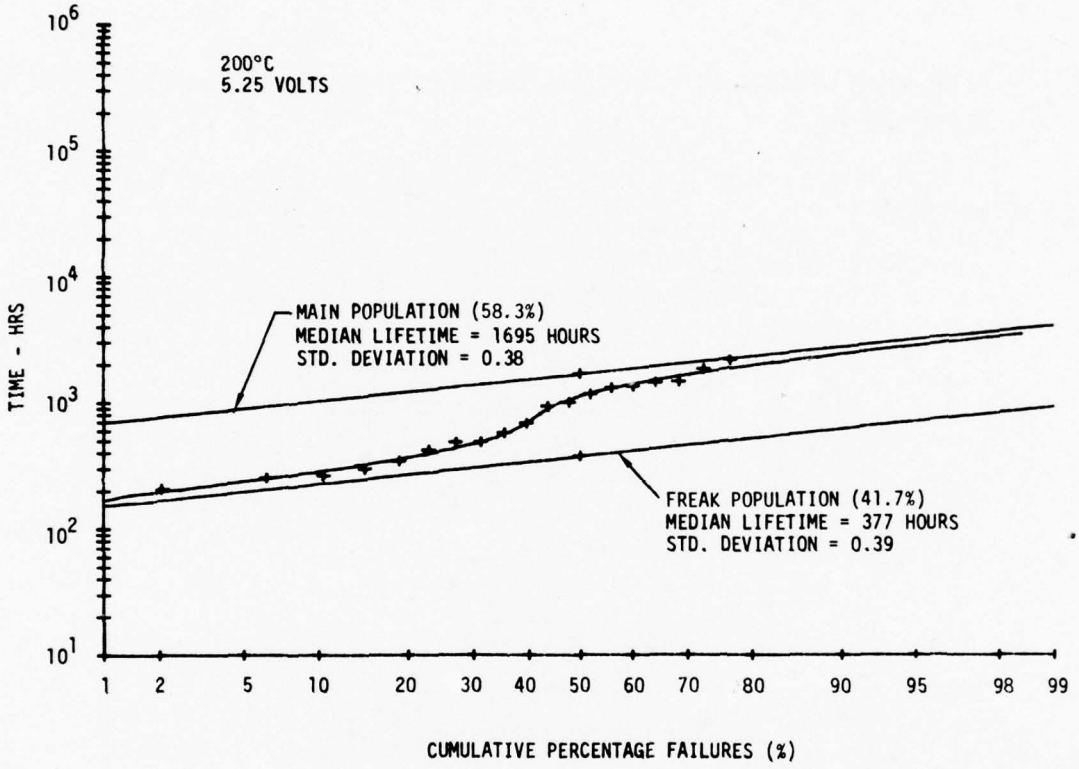


FIGURE D28. CELL 5 CUMULATIVE FAILURE DISTRIBUTION - P/N 773050 - 256 BIT RANDOM ACCESS MEMORY

activation energies for the "freak" population is 0.5 to 1.0 eV and the "main" population is 1.0 to 2.0 eV. The smallest activation energy represents the worst case situation so the following Arrhenius equations were developed using the minimum values of activation energy:

$$\ln t(50\%)_{freak} = -5.85763 + \frac{0.5}{kT}$$

$$\ln t(50\%)_{main} = -16.14423 + \frac{1.0}{kT}$$

Failure rates were calculated using the following relationship and the lognormal failure distribution:

$$\lambda(t) = \frac{f(t)}{R(t)}$$

$$\lambda(t)_{freak} = \frac{\frac{1}{t} \exp - \frac{\left[\ln t + 5.85763 - 0.5\left(\frac{1}{kT}\right)\right]^2}{2(0.39)^2}}{\int_t^{\infty} \frac{1}{t'}\left[\exp - \frac{\left[\ln t' + 5.85763 - 0.5\left(\frac{1}{kT}\right)\right]^2}{2(0.39)^2}\right] dt'}$$

$$\lambda(t)_{main} = \frac{\frac{1}{t} \exp - \frac{\left[\ln t + 16.14423 - \frac{1}{kT}\right]^2}{2(0.383)^2}}{\int_t^{\infty} \frac{1}{t'}\left[\exp - \frac{\left[\ln t' + 16.14423 - \frac{1}{kT}\right]^2}{2(0.383)^2}\right] dt'}$$

$$\lambda(t)_{Total} = \lambda(t)_{freak} \times (0.417) + \lambda(t)_{main} (0.583)$$

The maximum instantaneous failure rate in the storage environment, $\lambda(t)_{MAX}$, is calculated to be 4.3368×10^{-5} failures per hour and is contributed entirely to the freak distribution. Elimination of the freak population by screening would reduce the failure rate to 1.787×10^{-18} failures/hour. Since these failure rates are for a voltage condition, the storage failure rate is expected to be significantly smaller.

D9.0 CONCLUSIONS AND RECOMMENDATIONS

- The test program could not yield the desired results because of the presence of two different integrated circuit dice in the test sample and the subsequent occurrence of nonapplicable test failures. These combined to reduce significantly the data available for a complete failure rate analysis.
- One test cell (Cell 5, 200°C, 5.25 volts) provided sufficient data for analysis. Assumptions regarding activation energies allowed calculation of conservative estimates of operational and storage reliability.
- The presence of a "freak" and a "main" distribution in the Cell 5 population indicates a preconditioning screen to eliminate the "freak" population would improve both the operational and storage failure rates. The lack of test defined activation energies precludes detailed quantification of the failure rate improvements.
- Since two different integrated circuit dice were included in the test samples, additional testing is recommended on each die, if both are intended for SAM-D use.

APPENDIX E

P/N 785072

60 GATE RAYPACK CHIP

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E1.0 PART DESCRIPTION

The 60 Gate Raypack Chip, P/N 785072, is a logic array utilizing medium scale integration and beam lead construction. The die was manufactured by Raytheon Company, Semiconductor Division and procured by Raytheon Missile Systems Division. The dice were beam lead mounted to ceramic substrates. The substrates were then mounted in 50-pin plug-in packages manufactured by Isotronics Inc.

E2.0 CONSTRUCTION ANALYSIS

The pertinent physical details of this test configuration part are summarized in Table E1. The plug-in package utilized for this test device was a metal container of monolithic construction with a lid which was welded to the package. The lid and package are gold-plated. A glass seal at each pin and the weld seal at the lid provided a hermetic package suitable for life testing. The package is pictured in Figure E1 and a logic diagram is provided in Figure E2.

Internally, this device is of a nonstandard construction established specifically for this test program (Figure E3). The die is beam lead bonded to a ceramic substrate which is attached to the bottom of the 50-pin plug-in package by means of a gold eutectic bond. Interconnections between the gold-plated nail head post of the plug-in package and the gold conductors on the ceramic substrate are made using .002 inch gold wire. Thermocompression bonds are used to attach the gold interconnection wires. The materials and the method of construction used for the test configuration of this device were not expected to dictate any limitations to the life test of this part.

The part is pictured in Figure E4 in typical SAM-D mounting configuration. The die is beam lead mounted to a substrate. A ceramic cover is attached to the substrate using a polymer preform. The substrate of this device and the substrate of the test part are different. Because of this fact, failures due to faults in the substrate were not considered applicable to the SAM-D configuration. Obviously, failures due to the interconnecting wire of the test part were not considered as applicable to the SAM-D configuration part. In general, die failures and possible beam lead bond failures were considered to be applicable failures but each failure was considered during failure analysis as to its applicability to the SAM-D configuration.

TABLE E1. PART CONSTRUCTION DETAILS - P/N 785072 - 60 GATE RAYPACK CHIP

A. IDENTIFICATION

1. Part Name: 60 Gate Raypack Chip
2. Part Manufacturer: Raytheon Co., Semiconductor Div.
3. Part Number: 785072
4. Date Code: None

B. PACKAGE

1. Type: 50-Pin Metal Plug-In Package
2. Weight: 22.5 grams
3. Materials:
   a) Lid: Kovar, gold-plated
   b) Leads: Kovar, gold-plated
   c) Lid Seal: Weld

C. INTERNAL GEOMETRY

1. Interconnections:
   a) Type: The beam leads of the chip are bonded to gold conductors deposited on a ceramic substrate which in turn is attached to the gold-plated Kovar package. The gold conductors are connected to the nail head posts of the package using .002 inch gold wire.
   b) Bonds:
      a) Gold-gold thermocompression ball bond at the gold conductor
      b) Gold-gold thermocompression wedge bond at the nail head post
2. Die:
   a) Type: Silicon, planar (Beam Lead)
   b) Scribe Method: Etch
   c) Dimensions: 0.132 inch x 0.088 inch
   d) Passivation: Silicon Nitride over Silicon Dioxide
3. Metallization:
   a) Type: Gold/Titanium/Platinum
   b) Number of Layers: One

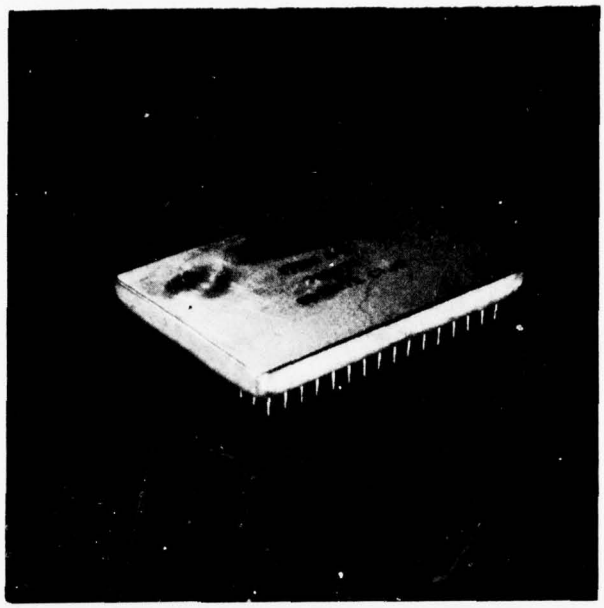

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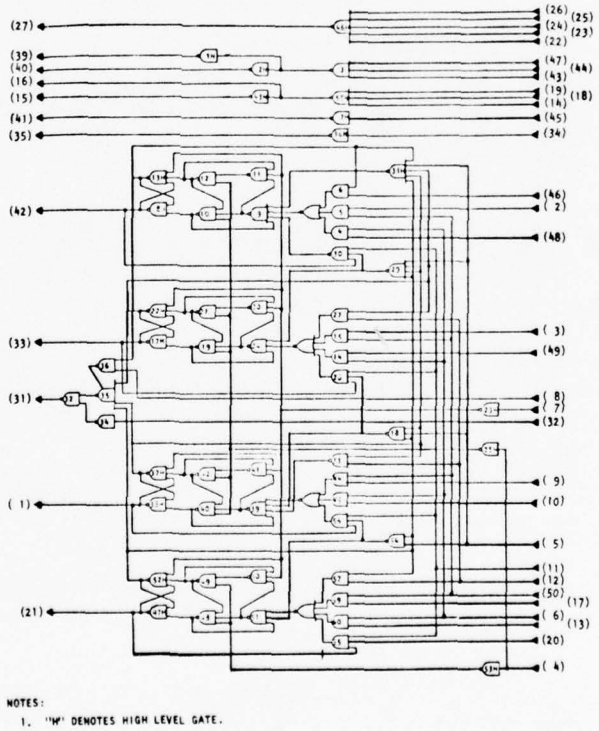
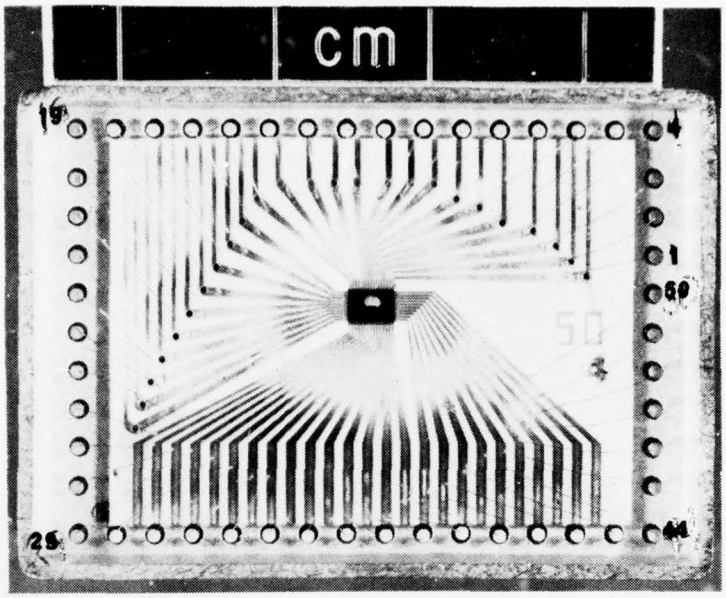
FIGURE E1. EXTERNAL CONSTRUCTION - P/N 785072 - 60 GATE RAYPACK CHIP



NOTES:
1. 'H' DENOTES HIGH LEVEL GATE.

FIGURE E2. LOGIC DIAGRAM - P/N 785072 - 60 GATE RAYPACK CHIP



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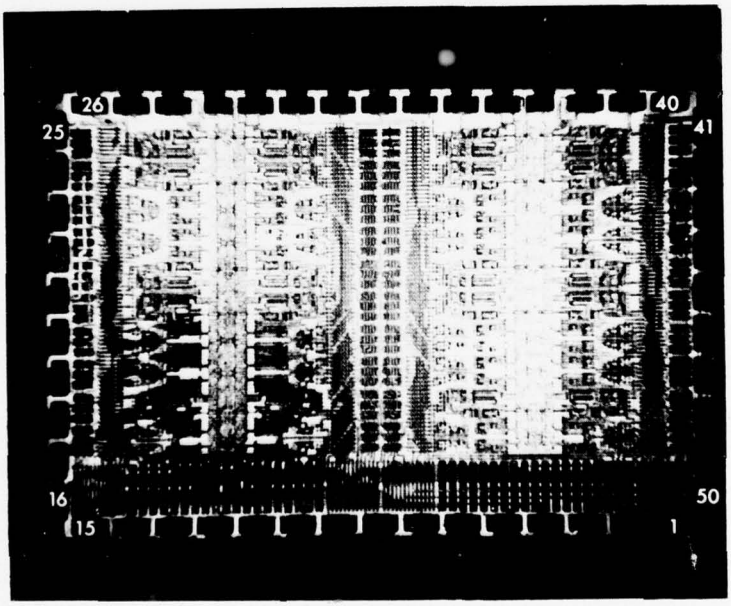

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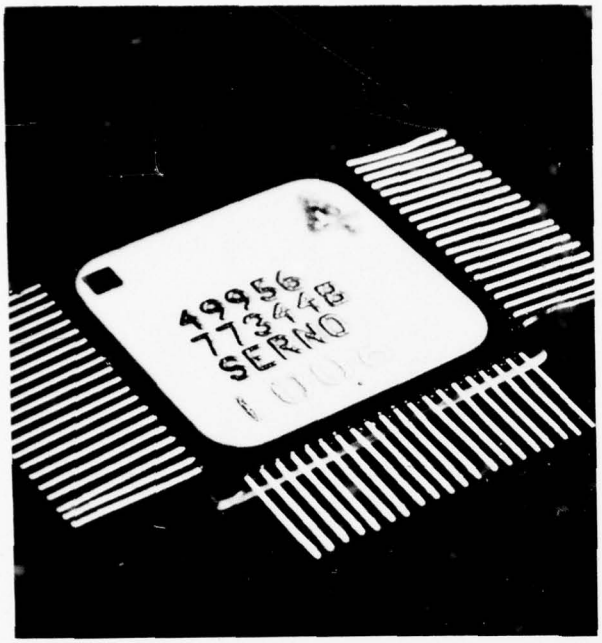
DIE TOPOGRAPHY

FIGURE E3. INTERNAL CONSTRUCTION DETAILS - P/N 785072 - 60 GATE RAYPACK CHIP



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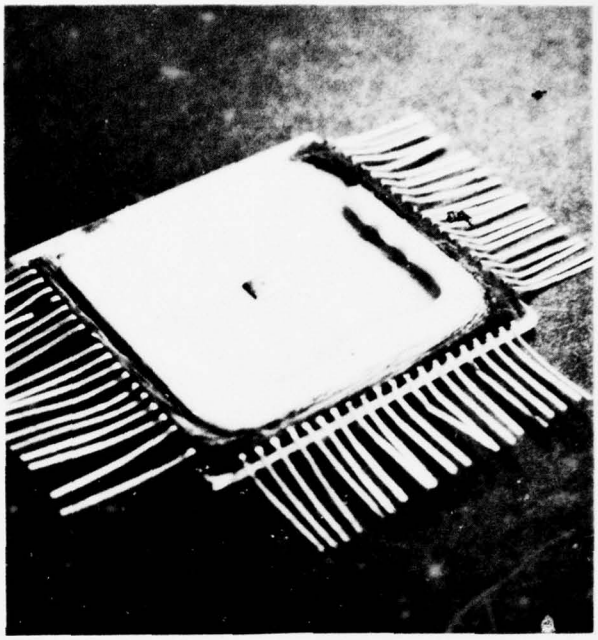
EXTERNAL



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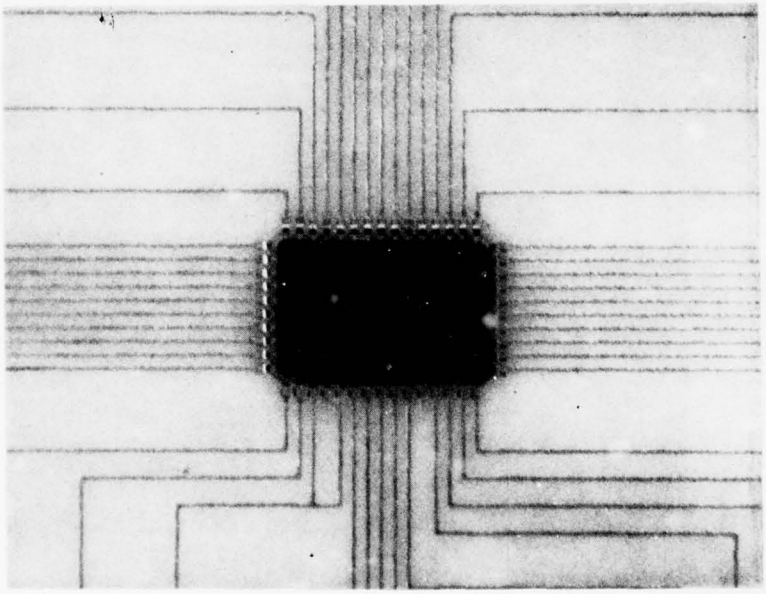
INTERNAL



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DIE MOUNTED IN SAM-D CONFIGURATION

FIGURE E4. TYPICAL SAM-D CONFIGURATION - P/N 773448 - 60 GATE RAYPACK CHIP

E3.0 ELECTRICAL TEST CRITERIA

The electrical measurements used to examine this device were the parametric tests plus the logic function tests defined in 785072. Table E2 lists the parametric tests, conditions of the test, and the test limits. Those parameters which are input tests are performed on all of the inputs and the output tests are performed on all outputs. All of the inputs and outputs do not have the same unit load factor; therefore, the test limits are expressed in terms of unit load factors. Table E3 provides a list of all the inputs by their pin numbers and their corresponding unit load factor and the same kind of list for the outputs. The parts were also tested for their compliance to the logic function data specified in 785072.

Several parts failed initial electrical tests due to loose substrates, but no further failures of this nature were encountered in the test program.

E4.0 BIAS CIRCUIT ANALYSIS

The first bias circuit examined for this device, designated bias circuit 1, had all of the inputs connected to 5.0 volts. With the data obtained from this bias circuit as a base, other bias circuits were examined to determine if they required more or less supply current with increasing ambient temperature. Bias circuit 2, with 5.0 volts applied to V_{CC} and open inputs and outputs, required less supply current than bias circuit 1, as shown in Figure E5.

Several other bias circuits, including one with all of the inputs grounded, required more supply current than bias circuits 1 and 2 at high ambient temperatures. Therefore, these two bias circuits were the prime life test circuit candidates. Because bias circuit 1 had a voltage applied to the inputs, it provided more reverse biased junctions than bias circuit 2 and was, therefore, selected to be the candidate life test circuit. A maximum ambient temperature of 225°C was selected for the life test and the maximum V_{CC} selected was 5.0 volts.

E5.0 STEP STRESS TEST RESULTS

The step stress test format was modified for this device to perform sequential testing on two groups of 10 parts each. The step stress test consisted of three 16-hour steps at ambient temperatures of 175°C, 200°C and 225°C. V_{CC} was 5.0 volts.

TABLE E2. ELECTRICAL TEST CONDITIONS - P/N 785072 - 60 GATE RAYPACK CHIP

PARAMETER	NOTE	APPLY TO PIN UNDER TEST (VOLTS)	V_{CC}	TEST LIMITS		UNITS
				MIN	MAX (7)	
II_L	(1)	0.4	5.5	0	-1.33 x U. L.	mAdc
II_H	(2)	2.4	5.5	0	100 x U. L.	μAdc
BII_H	(2)	5.5	5.5	0	0.8 + 0.2 x U. L.	mAdc
IO_L	(3)	0.4	4.5	1.4 x U. L.	0	mAdc
IO_H	(4)	2.4	4.5	0.1 x U. L.	-	mAdc
IO_S	(4) (5)	0.4	5.5	-30	-90	mAdc
I_{CC}	(6)	-	5.0	0	170	mAdc

(1) All other inputs to the current contributing gates are in the logic "1" state.
(2) A maximum number of inputs to the current contributing gates are in the logic "0" state.
(3) Inputs are such that the output assumes a logic "0" state.
(4) Inputs are such that the output assumes a logic "1" state.
(5) Maximum duration is less than 30 seconds per output and only one output is shorted at a time.
(6) All available inputs are in the logic "1" state.
(7) U. L. is the unit load for the pin under test. See TABLE E3 for the U. L. of each pin.

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TABLE E3. INPUT AND OUTPUT UNIT LOADS - P/N 785072 - 60 GATE RAYPACK CHIP

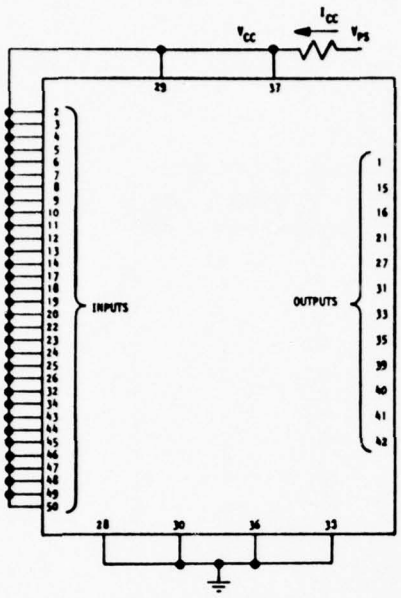
INPUTS

PIN NO.	UNIT LOAD (1)	PIN NO.	UNIT LOAD (1)
2	1	20	1
3	1	22	1
4	2	23	1
5	4	24	1
6	4	25	1
7	1	26	1
8	1	32	1
9	1	34	1
10	1	43	1
11	4	44	1
12	3	45	1
13	1	46	1
14	1	47	1
17	1	48	1
18	1	49	1
19	1	50	4

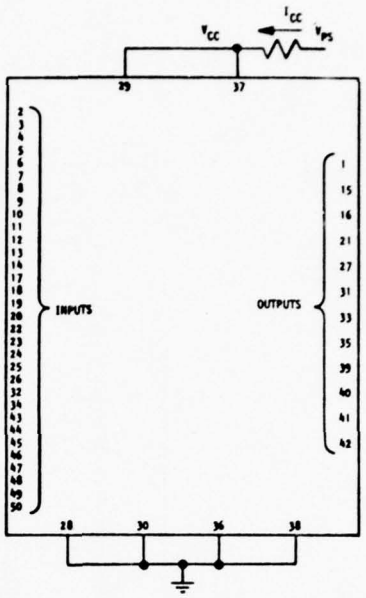
OUTPUTS

PIN NO.	UNIT LOAD (1)
1	8
15	10
16	9
21	8
27	10
31	10
33	8
35	10
39	10
40	10
41	10
42	8

(1) Reference Table E2 for definition of unit load.



BIAS CIRCUIT 1



BIAS CIRCUIT 2

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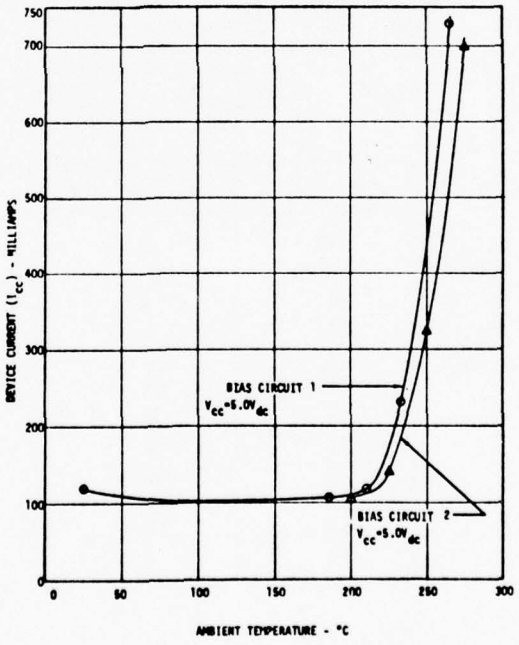

'FIGURE E5. BIAS CIRCUIT EVALUATION - P/N 785072 - 60 GATE RAYPACK CHIP

As shown in Figure E6 the first ten devices experienced no failures. It was then decided that the step stress test objective (to verify that operating the device in bias circuit 1 at the desired life test temperatures was nondestructive) had been obtained. Therefore, the second group of ten parts was not subjected to a step stress test and was kept for life test spares.

E6.0 LIFE TEST CONDITIONS AND RESULTS

Figure E6 contains a summary of the life test conditions for each cell. The accelerated life test reached 4000 hours and produced five failures, three in Cell 1, one each in Cells 3 and 5, and zero in Cells 2 and 4. Table E4 summarizes the accelerated life tests showing the cumulative failures at each interim test time.

E7.0 FAILURE ANALYSIS

The failure analysis summary results are provided in Table E5.

Mechanical Failures - Two parts failed due to open pins that were traced to open wire bonds. The part that failed at 64 hours in Cell 1 contained a lifted gold ball bond at the pin 40 gold substrate conductor. The separation occurred at the Au-Au interface, indicating that conductor surface had not been cleaned properly or that the bonding temperature was too low. The part that failed at 152 hours in Cell 5 contained a cracked Au-Au wedge bond at the pin 35 package terminal. The bond cracked at the heel, indicating that it had been damaged by excessive tool force. One part failed at 4 hours in Cell 3 due to a short-circuit between pin 27 (output) and pin 28 (ground). The short was traced to smeared gold metal bridging across the pins 27 and 28 substrate conductors as shown in Figure E7. The smear was caused by scratch damage inflicted during manufacturing or assembly.

Functional Failure - One part failed the functional test at 256 hours in Cell 1. The part passed all parametric tests but would not function in accordance with the truth table. The part was left on test through 4000 hours and its failure symptoms remained constant. Curve tracer tests did not disclose any discrepancy and microscopic examinations of the die after delidding disclosed no anomaly. Because this was a single, isolated failure and due to the complexity of the circuit, no further investigation was performed. Consequently, the cause of failure was not established.

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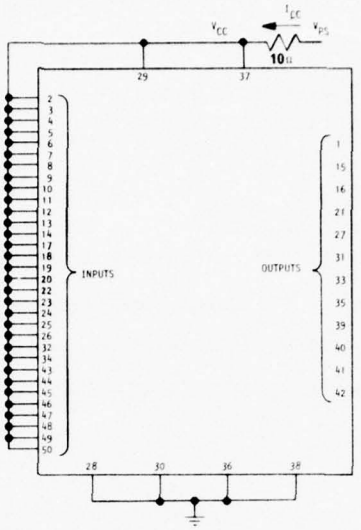
STEP STRESS AND LIFE TEST CIRCUIT



STEP STRESS TEST - FAILURE SUMMARY (10 DEVICES)

AMBIENT TEMP (°C)	V_{CC} (V)	CUMULATIVE FAILURES
175	5.0	0
200	5.0	0
225	5.0	0

LIFE TEST CONDITIONS

TEST CELL NUMBER	T_A AMBIENT TEMPERATURE (°C)	V_{CC} DEVICE VOLTAGE (VOLTS)	I_{CC} DEVICE CURRENT (MILLIAMPS)	P_d POWER DISSIPATION (MILLIWATTS)	T_J JUNCTION TEMPERATURE (°C)
1	225	5.0	210	1050	268
2	225	3.5	100	350	239
3	225	0	0	0	225
4	200	5.0	128	640	225
5	175	5.0	116	580	196

FIGURE E6. STEP STRESS RESULTS AND LIFE TEST CONDITIONS - P/N 785072 - 60 GATE RAYPACK CHIP

TABLE E4. LIFE TEST SUMMARY - P/N 785072 - 60 GATE RAYPACK CHIP

TEST CELL DESCRIPTION				CUMULATIVE FAILURES AT HOURS OF TEST										
CELL NO	APPLIED BIAS	AMBIENT TEMP	QUANTITY	4	8	16	32	64	152	256	512	1000	2500	4000
1	5.0 VDC	225°C	30	0	0	0	0	1	2	3	3	3	3	3*
2	3.5 VDC	225°C	30	0	0	0	0	0	0	0	0	0	0	0*
3	0 VDC	225°C	30	1	1	1	1	1	1	1	1	1	1	1*
4	5.0 VDC	200°C	30	0	0	0	0	0	0	0	0	0	0	0*
5	5.0 VDC	175°C	30	0	0	0	0	0	1	1	1	1	1	1*

* TEST TERMINATED

TABLE E5. FAILURE ANALYSIS SUMMARY - P/N 785072 - 60 GATE RAYPACK CHIP

	A. FAILED PARAMETERS OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TIME OF FAILURE (HOURS)				
		225°C			200°C	175°C
		5.0V	3.5V	0V	5.0V	5.0V
		CELL 1	CELL 2	CELL 3	CELL 4	CELL 5
MECHANICAL FAILURES	A. OPEN PIN B. OPEN Au-Au WIRE BOND C. DEFECTIVE BONDS D. BONDING ERRORS	1@64				1@152
MECHANICAL FAILURES	A. SHORTED PINS B. GOLD METAL BRIDGING TWO CONDUCTORS C. SMEARED METAL D. WORKMANSHIP DAMAGE			1@4		
UNDE-FINED	A. FUNCTIONAL TEST B. C. & D. NOT DETERMINED	1@256				
TEST ERROR	A. OPEN PIN B. CRACKED TEST CARD SOLDER JOINT C. MECHANICAL OVERSTRESS D. MISHANDLING	1@152				
	TOTAL NUMBER OF FAILED PARTS	3	0	1	0	1

200X

FIGURE E7. SMEAR OF GOLD THAT SHORT-CIRCUITED THE PINS 27 AND 28 CONDUCTORS - P/N 785072 - 60 GATE RAYPACK CHIP

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Test Error - One part failed due to an open pin that was not confirmed during bench testing. Subsequent investigation established that the open was caused by a cracked solder joint on the test card.

E8.0 DATA CORRELATION

The Table E5 Failure Analysis Summary identifies only one failure, the functional test failure in Cell 1 at 256 hours, considered applicable for a SAM-D configuration part in a storage environment. The other four failures are mechanical in origin and attributable to the interface necessary to test the part. Since the one failure is inadequate for failure distribution analysis, the parameters, I_{IL}, I_{IH}, B_{IH}, I_{OL}, I_{OH}, I_{OS}, and I_{CC}, were investigated for obvious trends. Four of these parameters are plotted in Figure E8 and show no obvious trends, a response typical of all the parameters. The parameter $\overline{I_{IH}}$ shows an increase for the last four measurement points but the percent change is very small and the absolute values are very far from the failure limits (average value at 4000 hours was 17.5 μA, failure limit is 100 μA). The increase was considered not well defined enough for extrapolation purposes.

The lack of failures and the absence of obvious parametric degradation trends indicates the test device has a high storage reliability ($\lambda(t)_{MAX} << 10^{-10}$ failures per hour).

E9.0 CONCLUSIONS AND RECOMMENDATIONS

- The test device experienced only one failure during the accelerated life test and demonstrated good parameter stability.
- The lack of test failures or extrapolated failure times precludes the calculation of a storage failure rate; however, these results would indicate that the test device has a high storage reliability ($\lambda(t)_{MAX} << 10^{-10}$ failures per hour).

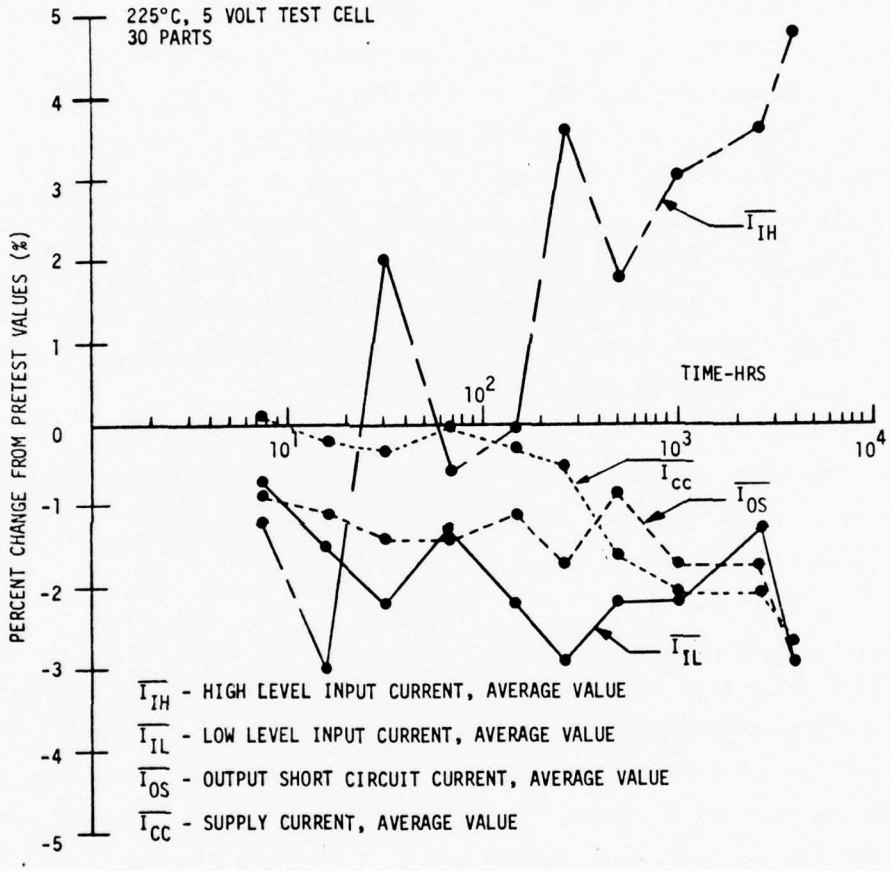

FIGURE E8. BEHAVIOR OF SELECTED PARAMETERS DURING LIFE TEST - P/N 785072 - 60 GATE RAYPACK CHIP

APPENDIX F

P/N 772926

OPERATIONAL AMPLIFIER

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F10.0	REFERENCE	F24

F1.0 PART DESCRIPTION

The Operational Amplifier, P/N 772926, an LM101A generic type device, is a beam lead monolithic integrated circuit intended for hybrid circuit application. The beam lead dice, manufactured by the Raytheon Company, Semiconductor Division, were procured by Raytheon Missile Systems Division and specially packaged in a hermetic 16 pin dual-in-line package (DIP) for the storage reliability test program.

This device and P/N 772921 (Appendix A) are identically packaged. The microcracks observed in the P/N 772921 DIP packages were also observed in the operational amplifier DIP packages. Appendix A, paragraph A1.0 discusses the microcracks and the hermeticity evaluation (Table A1) to which this part was subjected. Figure A1 (Appendix A) is a photograph of a package with microcracks.

The results of the hermeticity evaluation indicated that loss of hermeticity could be expected to occur during the test program. However, the lack of suitable replacement parts resulted in the decision to use this lot of parts in the accelerated life test. It should be pointed out that none of the failures which were generated during the accelerated life test could be associated with a package hermeticity problem.

F2.0 CONSTRUCTION ANALYSIS

Table F1 summarizes the physical details of the test configuration device, while Figure F1 provides schematic and functional diagrams. Figures F2 and F3 are photographs of the external and internal construction. This device contains no materials which would restrict testing below 300°C.

The typical SAM-D configuration, Figure F4, has the die beam lead bonded to gold-plated metallization deposited on a ceramic substrate in the same manner that the life test die is mounted in the DIP.

TABLE F1. PART CONSTRUCTION DETAILS - P/N 772926 - OPERATIONAL AMPLIFIER

A. IDENTIFICATION

1. Part Name: Operational Amplifier (LM101A)
2. Part Manufacturer: Raytheon Co., Semiconductor Div.
3. Part Number: 772926
4. Date Code: None

B. PACKAGE

1. Type: 16-Pin Ceramic Dual In-Line Package (Drawing No. 757438)
2. Weight: 1.24 grams
3. Materials:
   a) Lid: Kovar, gold plated
   b) Leads: Gold-plated Kovar which is braze welded to a refractory metal feedthru. The refractory metal is gold-plated in the internal area of the package.
   c) Seals: The lid is brazed to the lid frame and the seal around the leads is fired ceramic.

C. INTERNAL GEOMETRY

1. Interconnections: Beam leads bonded to gold-plated refractory metal conductors.

2. Die:

   a) Type: Silicon, planar (Beam Lead)
   b) Scribe Method: Etch
   c) Die Dimensions: 0.057 inch x 0.055 inch
   d) Passivation: Silicon Nitride over Silicon Dioxide

3. Metallization:

   a) Type: Gold/Titanium/Platinum
   b) Metallization Layers: One

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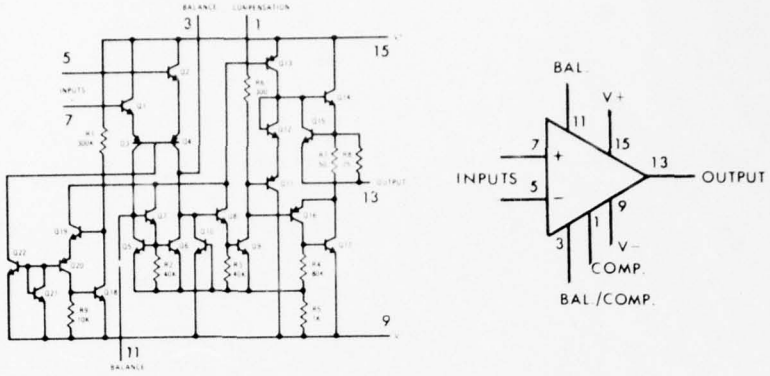

FIGURE F1. SCHEMATIC DIAGRAM AND FUNCTIONAL DIAGRAM - P/N 772926 - OPERATIONAL AMPLIFIER

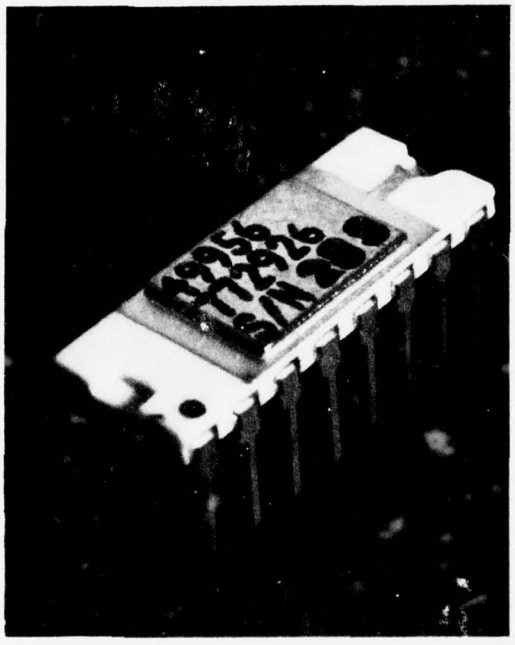

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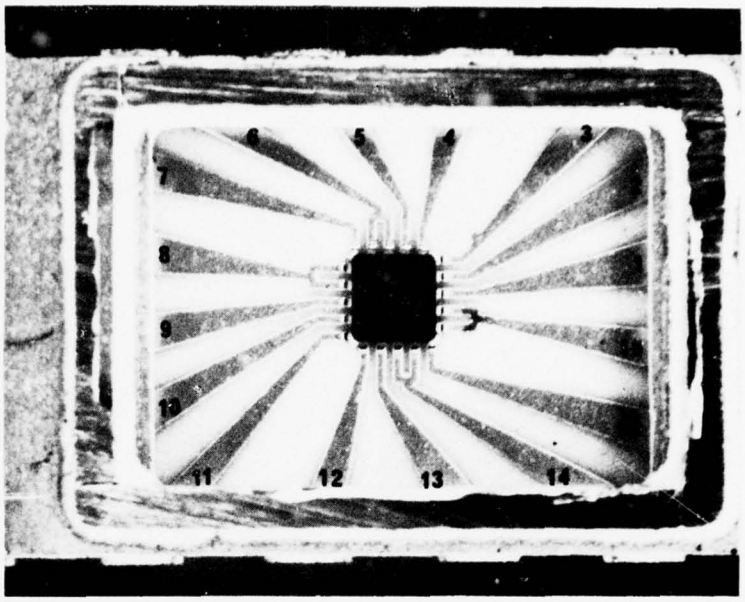
FIGURE F2. EXTERNAL CONSTRUCTION - P/N 772926 - OPERATIONAL AMPLIFIER



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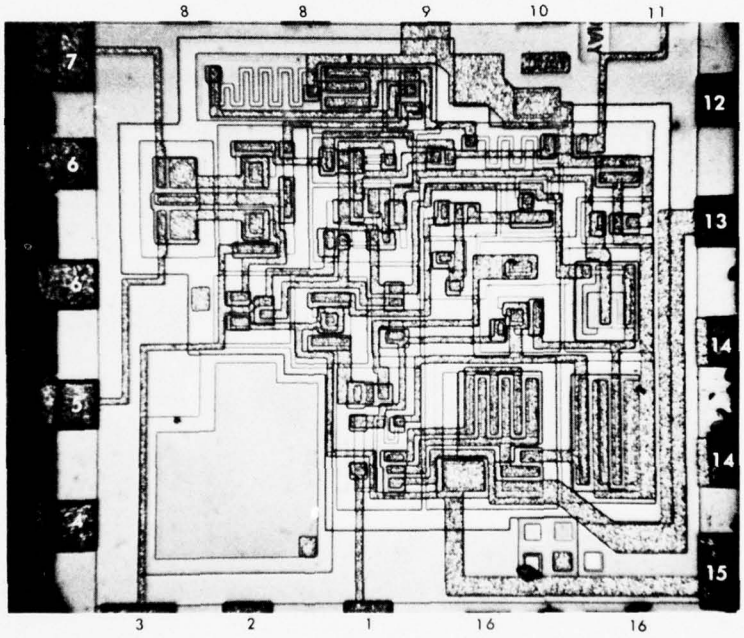

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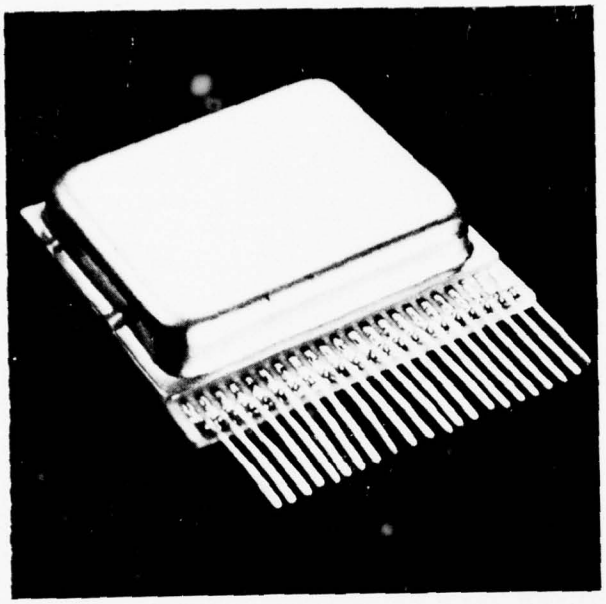
DIE TOPOGRAPHY

FIGURE F3. INTERNAL CONSTRUCTION DETAILS - P/N 772926 - OPERATIONAL AMPLIFIER



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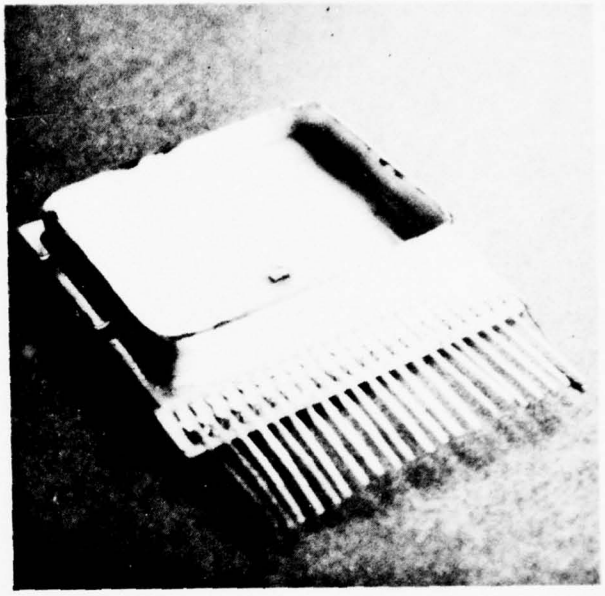
EXTERNAL



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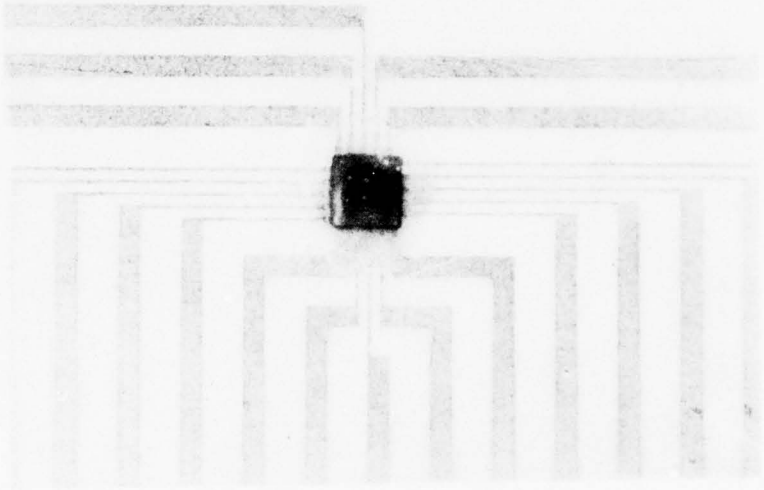
INTERNAL



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DIE MOUNTED IN SAM-D CONFIGURATION

FIGURE F4. TYPICAL SAM-D CONFIGURATION - P/N 773352 - OPERATIONAL AMPLIFIER

F3.0 ELECTRICAL TEST CRITERIA

Tables F2 and F3 provide the electrical test limits and electrical test conditions and calculations. In addition, the electrical test fixture is illustrated in Figure F5. The selected relays of Table F3 are closed in the electrical test fixture, Figure F5, to perform the desired test.

F4.0 BIAS CIRCUIT ANALYSIS

Bias circuit evaluation was facilitated by previous MDAC-E experience with 741 type operational amplifiers. The two Figure F6 bias circuits, both providing output voltage stability at elevated ambient temperatures, were investigated. Bias circuit 1 utilized two supply voltages and input biasing which drives the output voltage to positive saturation. Bias circuit 2 is biased to drive the output to positive saturation but only one supply voltage is required, with ground serving as a negative supply. The voltages applied to bias circuit 1 were $\pm$20 volts and V_{IN} equal 5.0 volts. V_{IN} was 5.0 volts for bias circuit 2, also, with 40 volts across the device.

Bias circuit 2 was selected to be the candidate life test circuit because it offered the highest temperature (225°C) with an acceptable current drain. An ambient temperature of 225°C and a maximum voltage of 40 volts were the limiting conditions established. To avoid catastrophic damage in the event of device failure, a 500 ohm resistor was used to limit short circuit current.

F5.0 STEP STRESS TEST RESULTS

Twenty devices configured in bias circuit 2 were subjected to a step stress test consisting of three 16 hour steps starting at an ambient temperature of 175°C and concluding at 225°C. Testing was terminated at 225°C due to the expected onset of thermal runaway at 250°C. The Figure F7 summary of the step stress test reveals only four failures, and these were due to input offset current being slightly out of specification. Therefore, bias circuit 2 and a maximum temperature of 225°C were considered acceptable for life testing.

TABLE F2. ELECTRICAL TEST LIMITS - P/N 772926 - OPERATIONAL AMPLIFIER

TEST NO	SYMBOL	$+V_S$ (VOLTS)	$-V_S$ (VOLTS)	V_{CM} (VOLTS)	R_L (OHMS)	T_A = 25°C MIN	T_A = 25°C MAX	T_A = 125°C AND -55°C MIN	T_A = 125°C AND -55°C MAX	UNITS
1	V_{IO} (12)	+15	-15	+12		-2	+2	-3	+3	mVdc
2	V_{IO} (0)	+20	20	0		-2	+2	-3	+3	mVdc
3	V_{IO} (-12)	+15	-15	-12		-2	+2	-3	+3	mVdc
4	V_{IO} (0,5)	+5	-5	0		-2	+2	-3	+3	mVdc
5	I_{IO} (12)	+15	-15	+12		-10	+10	-20	+20	nAdc
6	I_{IO} (0)	+20	-20	0		-10	+10	-20	+20	nAdc
7	I_{IO} (-12)	+15	-15	-12		-10	+10	-20	+20	nAdc
8	I_{IO} (0,5)	+5	-5	0		-10	+10	-20	+20	nAdc
9	I_{IB} (12)	+15	-15	+12		0	75	0	100	nAdc
10	I_{IB} (0)	+20	-20	0		0	75	0	100	nAdc
11	I_{IB} (-12)	+15	-15	-12		0	75	0	100	nAdc
12	I_{IB}(0,5)	+5	-5	0		0	75	0	100	nAdc
13	V_{OUT+} 10K	+20	-20	0	10K	+16	-	+16	-	Vdc
14	V_{OUT-} 10K	+20	-20	0	10K	-16	-	-16	-	Vdc
15	V_{OUT+} 2K	+20	-20	0	2K	+14	-	+14	-	Vdc
16	V_{OUT-} 2K	+20	-20	0	2K	-14	-	-14	-	Vdc
17	VSSR+	+20;+15	-20	0		80	-	80	-	dB
18	VSSR-	+20	-20:-15	0		80	-	80	-	dB
19	CMRR	+15	-15	$\pm$12		80	-	80	-	dB
20	I_S	+20	-20	0		0	3	0	2.5	mAdc
21	G_{LS}	+15	-15	0		50		25		V/mV

Initial and final test conducted at +25°C, +125°C and -55°C. Interim test conducted at +25°C.

TABLE F3. ELECTRICAL TEST CONDITIONS AND CALCULATIONS - P/N 772926 - OPERATIONAL AMPLIFIER

SYMBOL	TEST NO	APPLY (IN VOLTS)			RELAYS SELECTED	MEASURE		EQUATION	UNITS
		$+V_S$	$-V_S$	V_{REF}		VALUE	UNITS		
V_{IO} (12)	1	+15	-15	+12	K1, K10, K11	E_1	mV	V_{IO} (12) = E_1	mVdc
V_{IO} (0)	2	+20	-20	0	K2, K10, K11	E_2	mV	V_{IO} (0) = E_2	mVdc
V_{IO} (-12)	3	+15	-15	-12	K1, K10, K11	E_3	mV	V_{IO}(-12) = E_3	mVdc
V_{IO} (0,5)	4	+5	-5	0	K1, K10, K11	E_4	mV	V_{IO}(0,5) = E_4	mVdc
I_{IO} (12)	5	+15	015	+12	K1, K4, K10, K11	E_5			
		+15	-15	+12	K1, K3, K10, K11	E_6	mV	I_{IO} (12) = $2E_1-E_6-E_5$ 20	nAdc
I_{IO} (0)	6	+20	-20	9	K2, K4, K10, K11	E_7	mV		
		+20	-20	0	K2, K3, K10, K11	E_8	mV	I_{IO} (0) = $2E_2-E_8-E_7$ 20	nAdc
I_{IO} (-12)	7	+15	-15	-12	K1, K4, K10, K11	E_9	mV		
		+15	-15	-12	K1, K3, K10, K11	E_{10}	mV	I_{IO} (-12) = $2E_3-E_{10}-E_9$ 20	nAdc
I_{IO} (0,5)	8	+5	-5	0	K2, K4, K10, K11	E_{11}	mV		
		+5	-5	0	K2, K3, K10, K11	E_{12}	mV	I_{IO} (0,5) = $2E_4-E_{12}-E_{11}$ 20	nAdc
I_{IB} (12)	9							I_{IB} (12) = E_5-E_6 10	nAdc
I_{IB} (0)	10							I_{IB} (0) = E_7-E_8 10	nAdc
I_{IB} (-12)	11							I_{IB} (-12) = E_9-E_{10} 10	nAdc
I_{IB} (0,5)	12							I_{IB} (0,5) = $E_{11}-E_{12}$ 10	nAdc
V_{OUT+} 10K	13	+20	-20	-20	K2, K7, K8, K9, K11	E_{01}	V	V_{OUT+} 10K = E_{01}	V
V_{OUT-} 10K	14	+20	-20	+20	K2, K7, K8, K9, K11	E_{02}	V	V_{OUT-} 10K = E_{02}	V
V_{OUT+} 2K	15	+20	-20	-20	K2, K6, K8, K9, K11	E_{03}	V	V_{OUT+} 2K = E_{03}	V
V_{OUT-} 2K	16	+20	-20	=20	K2, K6, K8, K9, K11	E_{04}	V	V_{OUT-} 2K = E_{04}	V
VSRR+	17	+15	-20	0	K2, K10, K11	E_{13}	mV	VSSR+ = 20 Log_{10} $\frac{E_2-E_{13}}{5,000}$	dB
VSRR-	18	+20	-15	0	K2, K10, K11	E_{14}	mV	VSRR- + 20 Log_{10} $\frac{E_2-E_{14}}{5,000}$	dB
CMRR	19							CMRR = 20 Log_{10} $\frac{E_1-E_3}{24,000}$	dB
I_S	20	+20	-20	0	K2, K5, K12	$V_{10\Omega}$	V	I_S = $V_{10\Omega}$ 100	mA
G_{LS}	21	+15	-15	+10	K2, K8, K10, K11	E_{15}	mV		
		+15	-15	-10	K2, K8, K10, K11	E_{16}	mV	G_{LS} = $\frac{20}{E_{15}-E_{16}}$	V/mV

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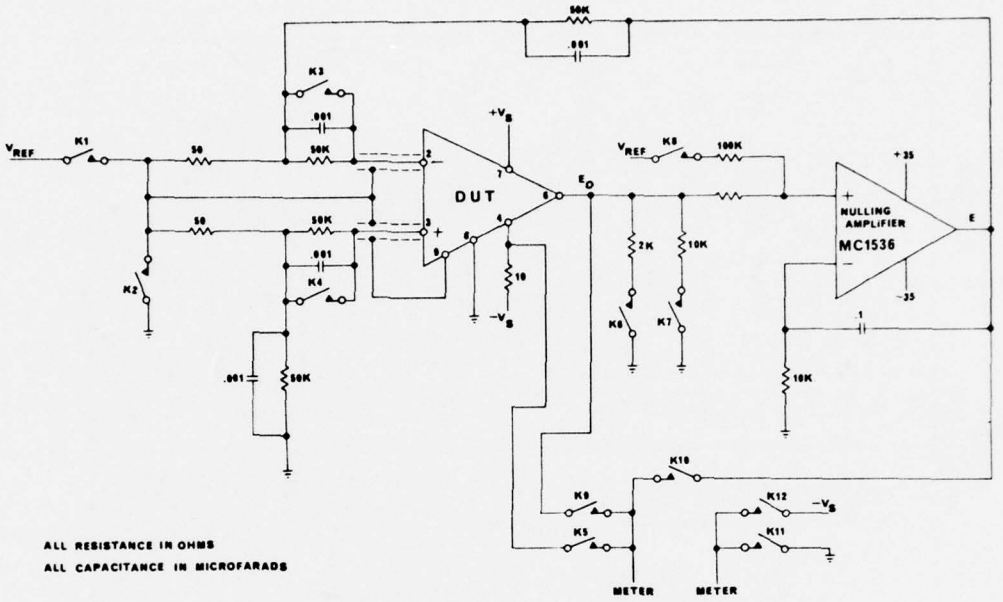
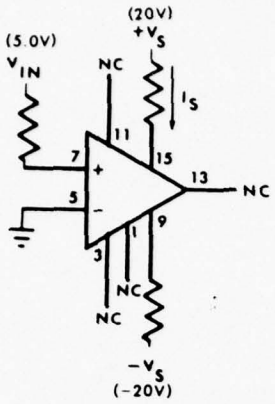
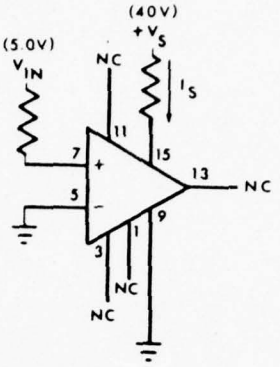


FIGURE F5. ELECTRICAL TEST FIXTURE - P/N 772926 - OPERATIONAL AMPLIFIER



BIAS CIRCUIT 1



BIAS CIRCUIT 2

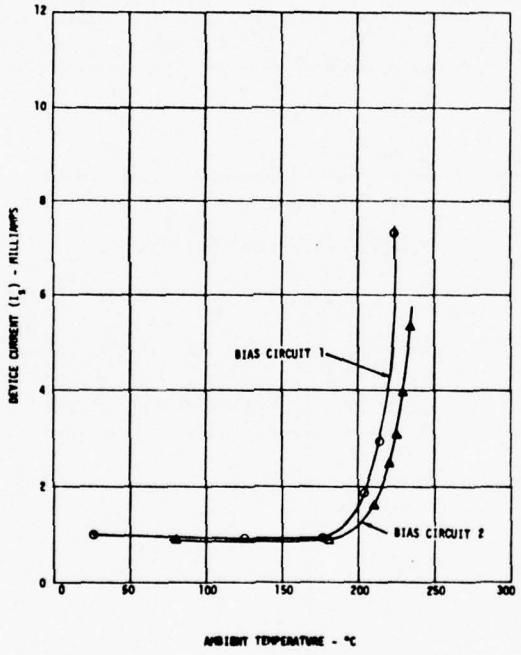


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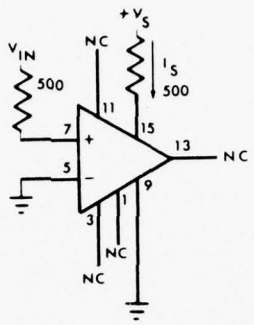
FIGURE F6. BIAS CIRCUIT EVALUATION - P/N 772926 - OPERATIONAL AMPLIFIER

STEP STRESS AND LIFE TEST CIRCUIT



STEP STRESS TEST - FAILURE SUMMARY (20 DEVICES)

AMBIENT TEMP (°C).	V_S (V)	CUMULATIVE FAILURES
175	40	2
200	40	2
225	40	4

LIFE TEST CONDITIONS

TEST CELL NUMBER	T_A AMBIENT TEMPERATURE (°C)	V_S DEVICE VOLTAGE (VOLTS)	I_S DEVICE CURRENT (MILLIAMPS)	P_d POWER DISSIPATION (MILLIWATTS)	T_J JUNCTION TEMPERATURE (°C)
1	225	40	2.9	116	235
2	225	25	2.2	55	230
3	225	10	1.3	13	226
4	225	0	0	0	225
5	200	40	1.3	52	205

FIGURE F7. STEP STRESS RESULTS AND LIFE TEST CONDITIONS - P/N 772926 - OPERATIONAL AMPLIFIER

F6.0 LIFE TEST CONDITIONS AND RESULTS

The life test conditions are included in Figure F7. The Table F4 summary shows the life tests continued to the 4000 hour readout with 54 cumulative failures.

F7.0 FAILURE ANALYSIS

Table F5 summarizes the failure analysis results.

Q1/Q2 h_{FE} Degradation - 53 life test parts exhibited excessive input bias current (I_{IB}) and/or excessive input offset current (I_{IO}). Many of these parts also exhibited excessive input offset voltage (V_{IO}), but this was due to the IR drop developed across a series input resistor (R_S = 50K ohms) of the test circuit as a result of the excessive I_{IO}. All failures occurred at a common mode voltage of +12V. In a few worst case instances I_{IB} or I_{IO} was also excessive at V_{CM} = 0V or -12V. The magnitude and sign of I_{IO} indicated that the failures were predominately due to degradation of the non-inverting input.

The excessive input currents were traced to low h_{FE} in Q1 and/or Q2. Q1 is the pin 7 (non-inverting) input transistor and Q2 is the pin 5 (inverting) input transistor. Two examples of curve tracer h_{FE} measurements via die level probing are presented in Table F6. Since constant collector currents are maintained through Q1 and Q2, a decrease in h_{FE} causes a proportional increase in their base currents, which are the amplifier input bias currents. The measured values of h_{FE} were found to be higher at higher collector voltages (due to increased leakage and base width modulation) which is why I_{IO} and I_{IB} were generally in tolerance at common mode voltages of 0V ($V_{CE} \simeq 20V$) and -12V ($V_{CE} \simeq 27V$). Further electrical probing established that the low gain was caused by degradation of the base-emitter junction as illustrated in Figure F8. I_{IO} and I_{IB} would recover if the parts were baked or in some instances if the parts were left on test, indicative of a surface instability mechanism. The mechanism probably involved depletion or inversion of the input transistor base region due to the accumulation of a net positive charge in the passivation over the base. The accumulation generally results from the drift of ions under the influence of an applied bias. The two failures that occurred in the 0V cell suggest that the mechanism may not be dependent on an applied external bias. These two devices exhibited marginal I_{IB} or V_{IO} at the time of failure and were left on test. I_{IB} or V_{IO} peaked, then returned to within specification and remained stable thereafter.

TABLE F4. LIFE TEST SUMMARY - P/N 772926 - OPERATIONAL AMPLIFIER

TEST CELL DESCRIPTION				CUMULATIVE FAILURES AT HOURS OF TEST										
CELL NO	APPLIED BIAS	AMBIENT TEMP.	QUANTITY	4	8	16	32	64	128	256	512	1000	2500	4000
1	40 VDC	225°C	30	2	2	2	2	2	2	3	4	4	8	22*
2	25 VDC	225°C	30	1	1	1	2	2	3	3	3	3	3	13*
3	10 VDC	225°C	30	1	1	1	1	3	3	4	5	5	7	11*
4	0 VDC	225°C	30	0	0	0	1	2	2	2	2	2	2	2*
5	40 VDC	200°C	30	2	3	4	6	6	6	6	6	6	6	6*

* TEST TERMINATED

TABLE F5. FAILURE ANALYSIS SUMMARY - P/N 772926 - OPERATIONAL AMPLIFIER

A. FAILED PARAMETER OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TIME OF FAILURE (HOURS)				
	225°C				200°C
	40 V	25 V	10 V	0 V	40 V
	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5
A. $I_{IO}/I_{IB}/V_{IO}$	1@4	1@4	1@4	1@32	2@4
B. LOW h_{FE} IN Q1 AND Q2 DUE TO B-E DEGRADATION	1@256 1@512	1@32 1@128	2@64 1@256	1@64	1@8 1@16
C. DRIFT OF MOBILE IONS	4@2500 14@4000	10@4000	1@512 2@2500 4@4000		2@32
D. CONTAMINATION IN THE PASSIVATION					
A. $I_{IO}/I_{IB}/V_{IO}$	1@4				
B. DEGRADED Q1 C-B JUNCTION					
C. NOT DETERMINED (BULK RELATED)					
D. NOT DETERMINED					
TOTAL NUMBER OF FAILED PARTS	22	13	11	2	6

TABLE F6. h_{FE1} OF Q1 AND Q2 FROM DIE LEVEL PROBING - P/N 772926 - OPERATIONAL AMPLIFIER

S/N	PARAMETER VALUES AT TIME OF FAILURE		CALCULATED BIAS CURRENTS	h_{FE1} @ V_{CE} = 3V* AND I_B = 500 nA
	$I_{IO}(V_{CM}=+12V)$	$I_{IB}(V_{CM}=+12V)$		
231(CELL 1@256 HRS)	+525 nA	+317 nA	$+I_B(+12V)$ 55 nA $-I_B(+12V)$ 580 nA	Q1 = 440 (LOW) Q2 = 34 (EXTREMELY LOW)
52 (CELL 5@32 HRS)	-35 nA	+61 nA(OK)	$+I_B(+12V)$ = 78 nA $-I_B(+12V)$ = 43 nA	Q1 = 480 (LOW) Q2 = 620 (NORMAL)

* $V_{CE} \cong 3V$ AT $V_{CM} = +12V$

Q1 I_{CBO} Failure - One part exhibited excessive I_{IO}, I_{IB}, and V_{IO} due to negative bias current at pin 7; i.e., excessive current flow out of the pin 7, non-inverting input. The negative bias current was traced to degradation of the collector-base junction of Q1 as shown in Figure F9. The degradation was not bake reversible indicating that the degradation was caused by a bulk related mechanism. Because this was a single, isolated failure no analysis other than microscopic exminations of Q1 after delidding was performed. The examinations disclosed no explanation for the degradation, consequently the exact failure mechanism was not established.

F8.0 DATA CORRELATION

Excluding one failure, the Table F5 Failure Analysis Summary attributes all test failures to drift of mobile ions in the passivation. Three parameters, I_{IO}, I_{IB}, and V_{IO}, failed for this reason. Data analysis revealed that the early test failures (<512 hours) typically involved initially marginal parts which drifted only slightly to exceed the specified parameter limit. I_{IO} was the predominant failed parameter and was analyzed in depth. The early I_{IO} failures exceeded the positive I_{IO} limit, whereas all failures after 512 hours exceeded the negative I_{IO} limit. Except for the zero volt cell, I_{IO} of all parts on test typically increased in the positive direction at the beginning of the life test, peaked, and then progressed toward the negative limit. The zero volt cell, which had only two marginal failures early in the test program, showed no discernable parameter trends.

Using the three point interpolation technique, failure times were established for the negative I_{IO} failures and the Figures F10 and F11 cumulative failure distributions were plotted. The three Cell 5 failure times were obtained by extrapolation techniques for those parts exhibiting an obvious degradation trend. The data reflects a single lognormal distribution and is summarized in Table F7 as the "main" population.

The Table F7 "freak" population summary data reflects all failures up to 512 hours. This "freak" population is not considered "well behaved" for the following reasons:

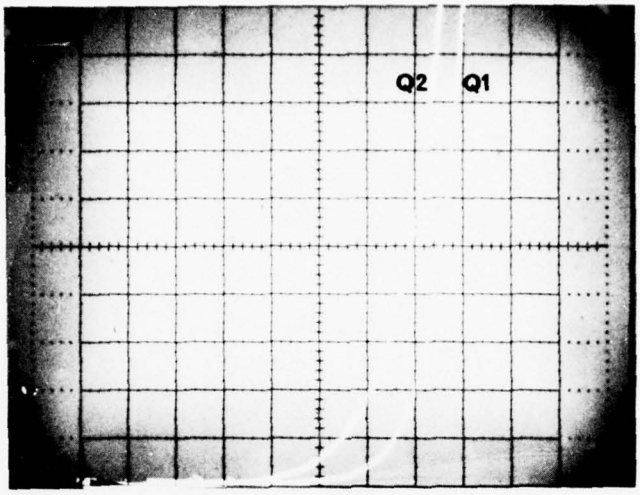


FIGURE F8. FOWARD BASE-EMITTER I-V CHARACTERISTIC OF Q2 (h_{FE} = 34) AND, FOR COMPARISON, Q1 (h_{FE} = 440) OF S/N 231 - P/N 772926 - OPERATIONAL AMPLIFIER

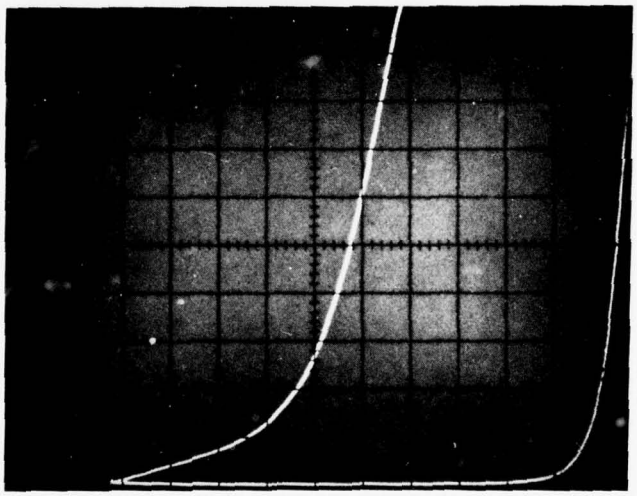


FIGURE F9. LEAKAGE CURRENT FROM V+ TO PIN 7 (L/H TRACE) COMPARED TO V+ TO PIN 5 (R/H TRACE). THE EXCESSIVE LEAKAGE FROM V+ TO PIN 7 INDICATES THAT THE C-B JUNCTION OF Q1 IS DEGRADED - P/N 772926 - OPERATIONAL AMPLIFIER

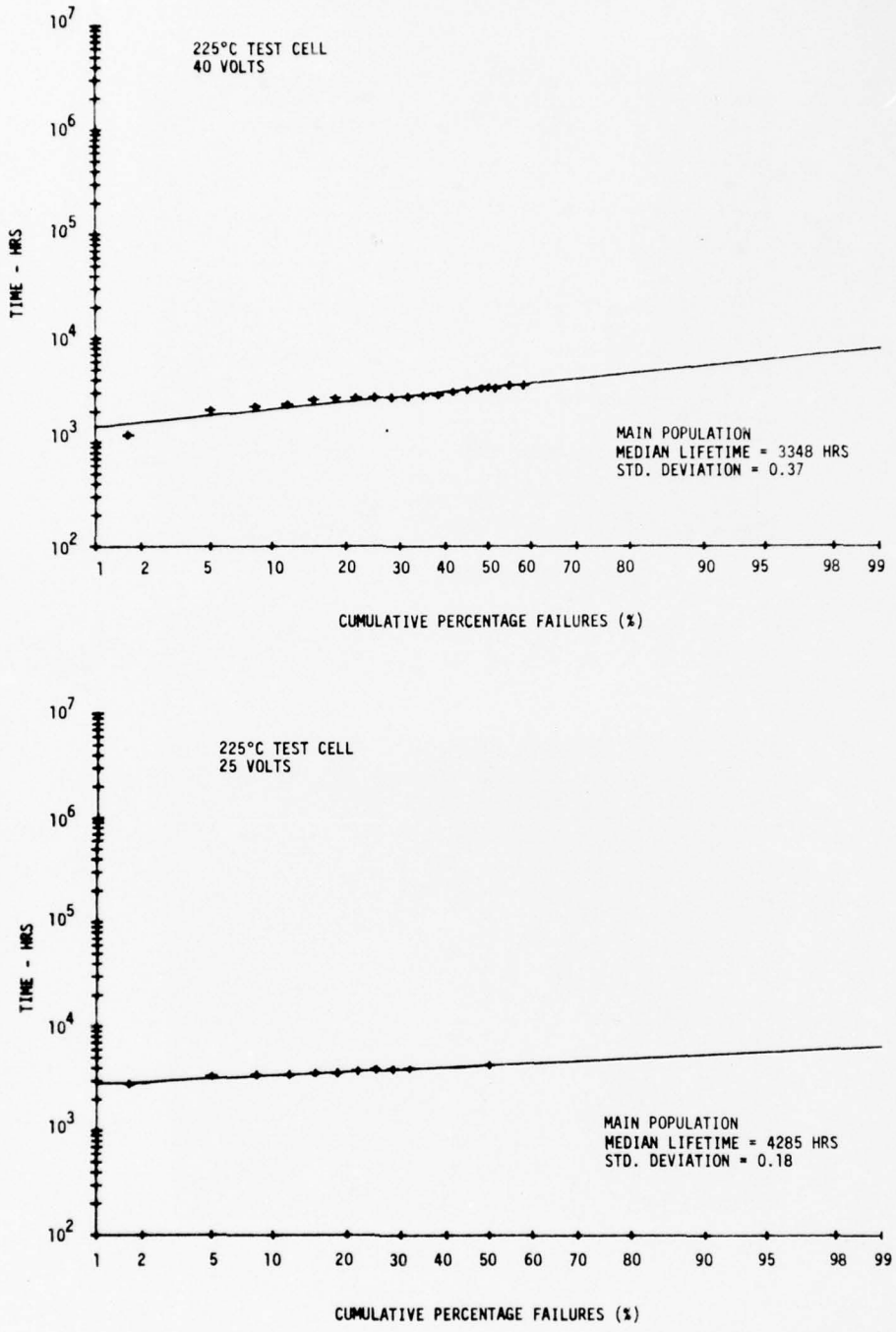


FIGURE F10. CUMULATIVE FAILURE DISTRIBUTIONS FOR CELL 1 (TOP) AND CELL 2 (BOTTOM) - P/N 772926 - OPERATIONAL AMPLIFIER

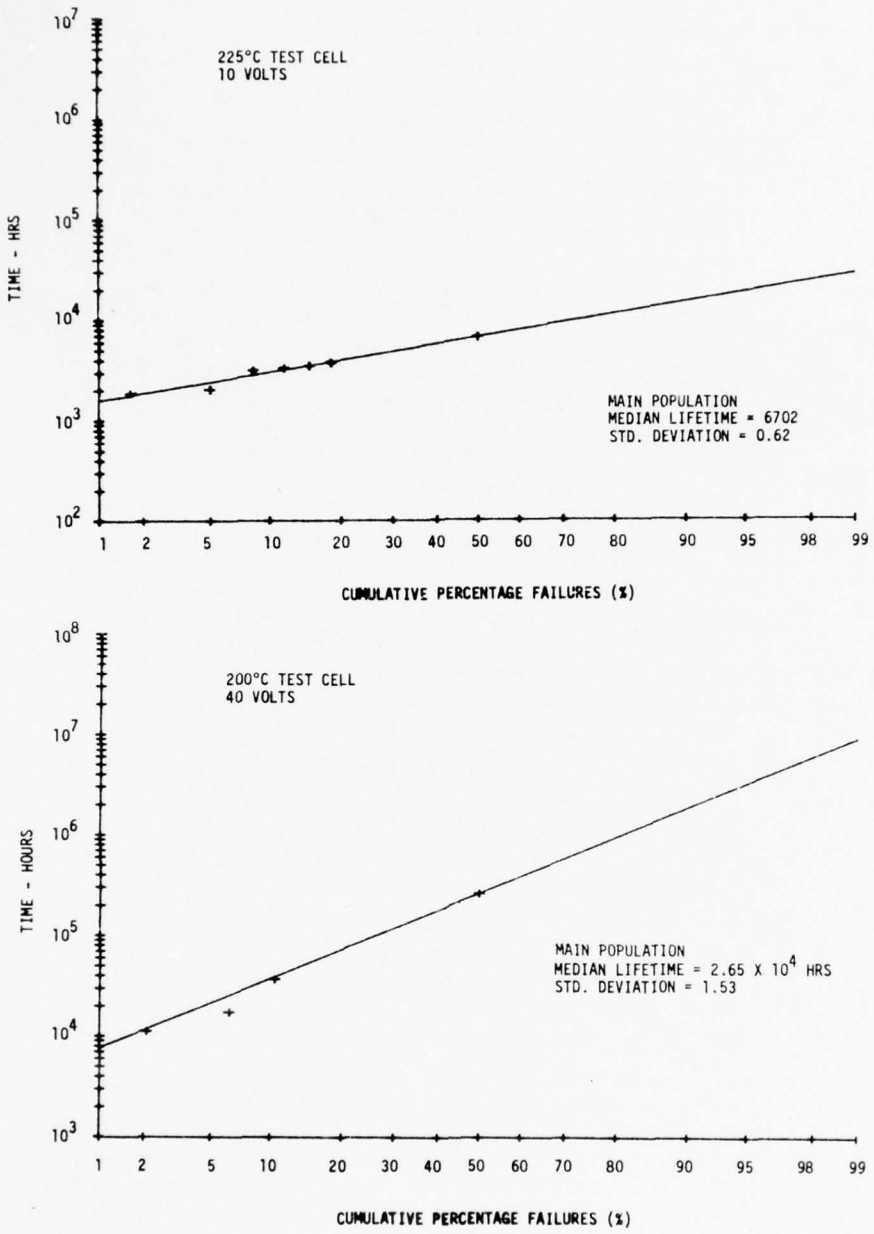


FIGURE F11. CUMULATIVE FAILURE DISTRIBUTION FOR CELL 3 (TOP) AND CELL 5 (BOTTOM) - P/N 772926 - OPERATIONAL AMPLIFIER

STORAGE RELIABILITY
OF MISSILE MATERIEL

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TABLE F7. SUMMARY DATA - P/N 772926 - OPERATIONAL AMPLIFIER

CELL NO.	TEST VOLTAGE (VOLTS)	NUMBER OF FAILURES	T_A (°C)	T_J (°C)	FREAK POPULATION			MAIN POPULATION		
					MEDIAN LIFE (HOURS)	STANDARD DEVIATION (HOURS)	% FREAK	MEDIAN LIFE (HOURS)	STANDARD DEVIATION (HOURS)	% MAIN
1	40	21	225	235	54	2.39	10.3	3143	0.34	89.7
2	25	13	225	230	19	1.53	10.0	4206	0.17	90.0
3	10	11	225	226	51	1.89	16.7	6066	0.60	83.3
4	0	2	225	225	30	0.75	6.7	----	----	93.3
5	40	9 ⚠	200	205	7	1.15	20	265,352	1.53	80

⚠ INCLUDES THREE EXTRAPOLATED TIMES TO FAILURE

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1) Although the failure mechanism is considered identical for both "freak" and "main" populations, the "freak" population failed I_{IO} (positive limit) and I_{IB}, whereas the "main" population failed only I_{IO} (negative limit). Additionally, many of the "freaks" were initially marginal, drifted only slightly to exceed the failure limit, and recovered when left on test.
2) Cell 5, 200°C and 40 volts, produced twice as many freak failures as Cell 1, 225°C and 40 volts, and had a much lower median lifetime (6.9 hours as opposed to 54 hours). This is contrary to what would be expected if an Arrhenius temperature relationship existed.
3) The two failures in the zero volt cell indicate the "freak" population could be expected to occur in a storage environment.

Because of these reasons no Arrhenius evaluation was accomplished for the "freak" population. However, a lot screening test using the Cell 5 test conditions for 500 hours should detect almost all of the "freak" population.

The Figure F12 Arrhenius plot reflects Cells 1 and 5 "main" population data and can be represented by the following equation:

$$\ln t_{50\%} = -62.64783 + \frac{3.09}{kT}$$

The high activation energy (3.09 eV), is attributed to the use of extrapolation for the three Cell 5 failure times. Previous operational amplifier testing [F1] yielded $1.6 \leq E_A \leq 2.3$ eV for main population surface instability failure mechanisms at rated voltage, confirming that the Cell 5 failure extrapolation is suspect. However the use of Cell 1 data and an $E_A = 1.6$ eV still produces a $\lambda(t)_{MAX} << 10^{-10}$ failures per hour, indicating a high storage reliability potential.

Cells 1 through 4 provide additional insight regarding operational reliability as a function of voltage. Figure F13 is a plot of the median lifetimes as a function of test voltage. For a constant temperature the Eyring Model reduces to:

$$\ln t_{50\%} = a - bf(V)$$

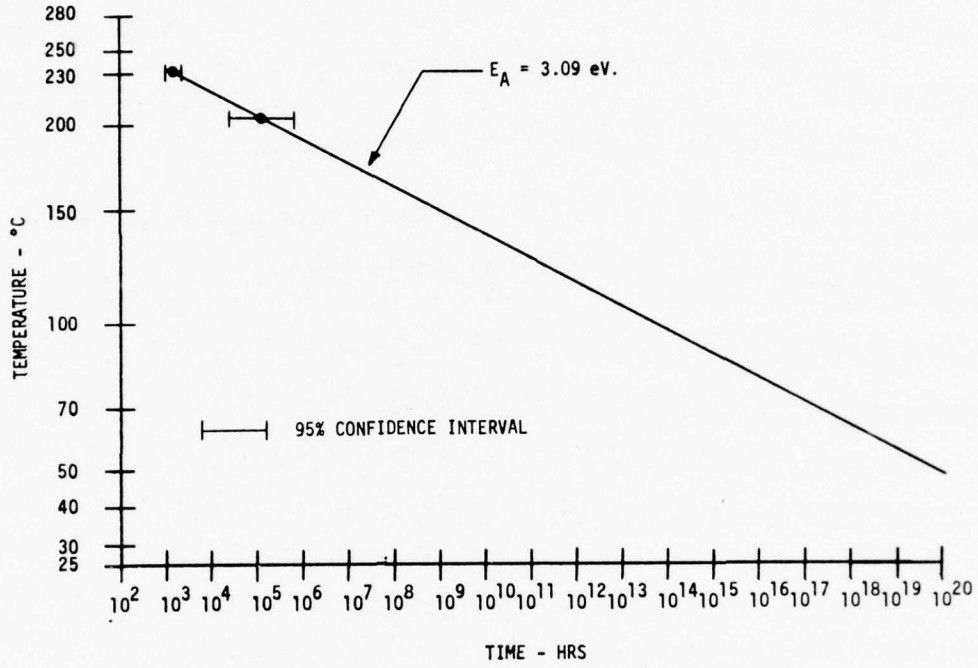

FIGURE F12. ARRHENIUS PLOT - P/N 772926 - OPERATIONAL AMPLIFIER

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TABLE F3. LIFE TEST SUMMARY - P/N 772951 - VOLTAGE REGULATOR

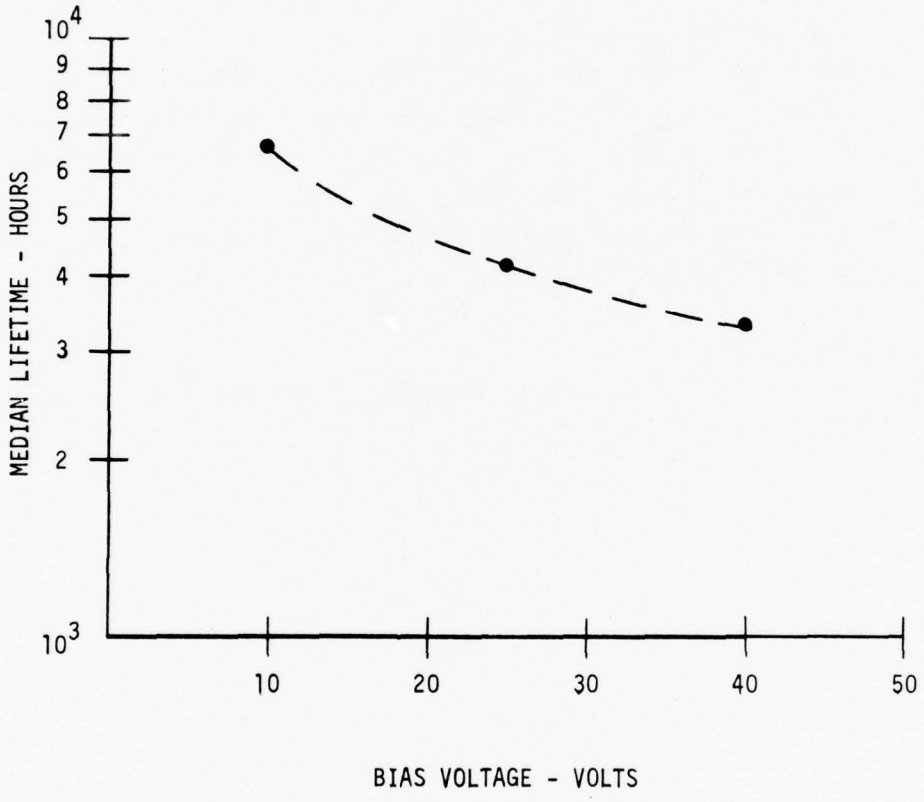

FIGURE F13. MEDIAN LIFETIME VERSUS TEST VOLTAGE AT 225°C AMBIENT TEMPERATURE - P/N 772926 - OPERATIONAL AMPLIFIER

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The Figure F13 data indicates the f(V) term is best satisfied by ln V; however, $f(V) = \frac{1}{V}$ also adequately represents the data. An f(V) = V is rejected on the basis of no failures and the lack of a parameter trend in the zero volt cell. Additional voltage testing at lower temperatures is required to provide the data necessary for identifying the constants ("a" and "b") in the above equation.

F9.0 CONCLUSIONS AND RECOMMENDATIONS

- The zero volt cell produced only two marginal failures, indicating a high storage reliability potential.
- Calculated failure rates, based on voltage induced failures, indicates a high operational reliability after removal of the freak population.
- The "freak" population, consisting of marginal failures, did not exhibit an Arrhenius temperature relationship.
- A lot screening test (200°C, 40 volts) for 500 hours should detect most of the "freak" population.

F10.0 REFERENCES

[F1] G. M. Johnson, "Evaluation of Microcircuit Accelerated Test Techniques", RADC-TR-76-218, July 1976.

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APPENDIX G

P/N 773051

VOLTAGE REGULATOR

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G1.0 PART DESCRIPTION

The negative voltage regulator, P/N 773051, is a LM104 type device manufactured by National Semiconductor Corporation. The die is mounted in a 10-pin, TO-5 can utilizing conventional chip and wire construction. This test configuration is different from the SAM-D use configuration.

G2.0 CONSTRUCTION ANALYSIS

The pertinent construction details of the test configuration part are listed in Table G1. Figures G1, G2 and G3 provide a photograph of the external construction, schematic and functional diagrams, and photographs of the internal construction. This device contains no material which limited life testing below 300°C.

The typical SAM-D configuration, Figure G4, utilizes a 10-lead flatpack version of the voltage regulator soldered to a ceramic circuit board.

G3.0 ELECTRICAL TEST CRITERIA

Table G2 is a list of the electrical tests performed on this device, including the test conditions and limits. The "relays selected" column refers to the test fixture relays, Figure G5, which, when selected, are closed.

G4.0 BIAS CIRCUIT ANALYSIS

Two bias circuits were evaluated and are pictured in Figure G6 along with device current vs ambient temperature plots. Bias circuit 1 is identical to the burn-in circuit of 773051. Bias circuit 2 differs from bias circuit 1 in that the regulated output pin and booster pin are left open. Bias circuit 1, with the unregulated supply voltage equal to -40 volts, experienced thermal runaway at an ambient temperature between 225°C and 250°C. Bias circuit 2 remained thermally stable at ambient temperatures beyond 250°C. In addition, bias circuit 2 remained stable at 250°C with -50 volts as the unregulated supply voltage.

Bias circuit 2 was selected as the candidate accelerated life test circuit. The maximum ambient temperature was 250°C and the selection of a maximum voltage for the life test was delayed pending the results of the step stress test. A 1K ohm current limiting resistor was used to avoid catastrophic damage in the event of device failure.

TABLE G1. PART CONSTRUCTION DETAILS - P/N 773051 - VOLTAGE REGULATOR

A. IDENTIFICATION

1. Part Name: Voltage Regulator (LM104)
2. Part Manufacturer: National Semiconductor Corporation
3. Part Number: 773051
4. Date Code: 434

B. PACKAGE

1. Type: 10-Pin, TO-5
2. Weight: 0.975 gram
3. Materials:

   a) Cap: Steel
   b) Header: Kovar, gold-plated
   c) Leads: Kovar, gold-plated
   d) Cap Seal: Weld
   e) Lead Seal: Glass

C. INTERNAL GEOMETRY

1. Interconnections

   a) Type: Aluminum
   b) Diameter: 0.0011 inch
   c) Bonds:
      1) Aluminum-aluminum ultrasonic at the die
      2) Aluminum-gold ultrasonic at the lead

2. Die:

   a) Type: Silicon, planar
   b) Scribe Method: Mechanical
   c) Dimensions: 0.055 inch x 0.055 inch
   d) Attach Method: Gold Eutectic
   e) Glassivation: Silicon Dioxide

3. Metallization:

   a) Type: Aluminum
   b) Number of Layers: One

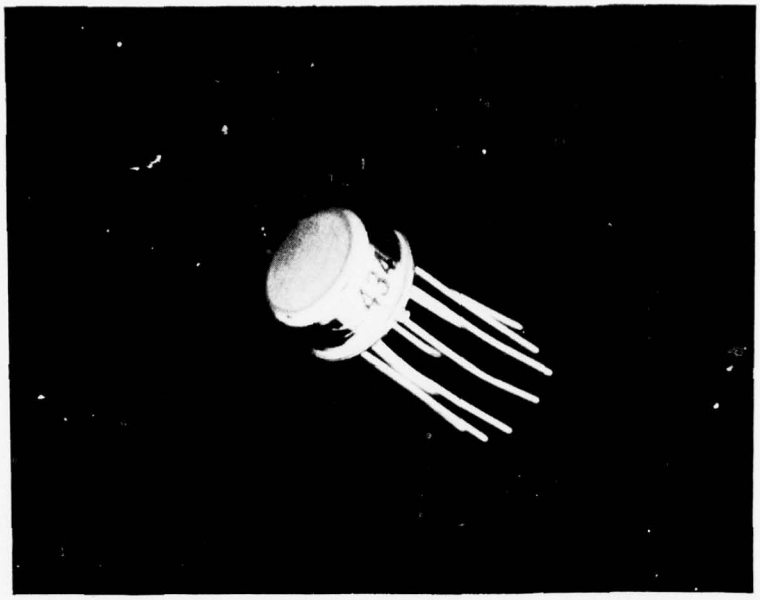

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FIGURE G1. EXTERNAL CONSTRUCTION - P/N 773051 - VOLTAGE REGULATOR

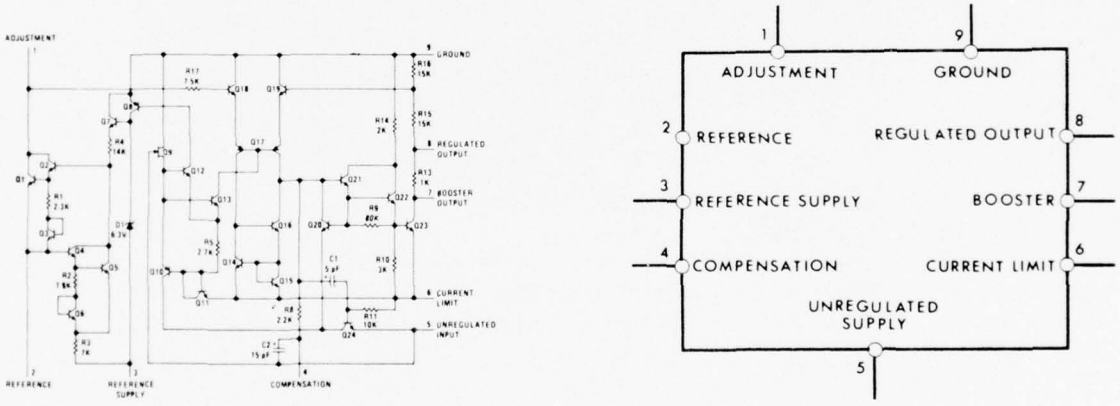
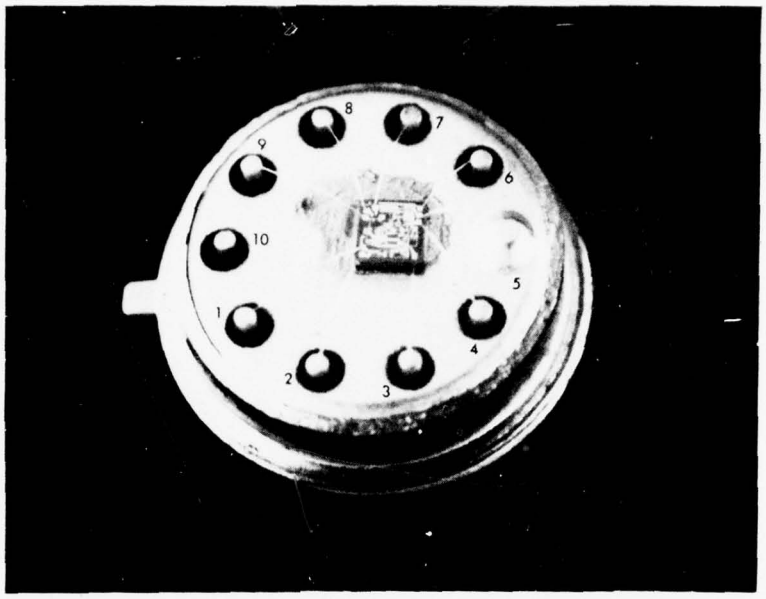


FIGURE G2. SCHEMATIC DIAGRAM AND FUNCTIONAL DIAGRAM - P/N 773051 - VOLTAGE REGULATOR



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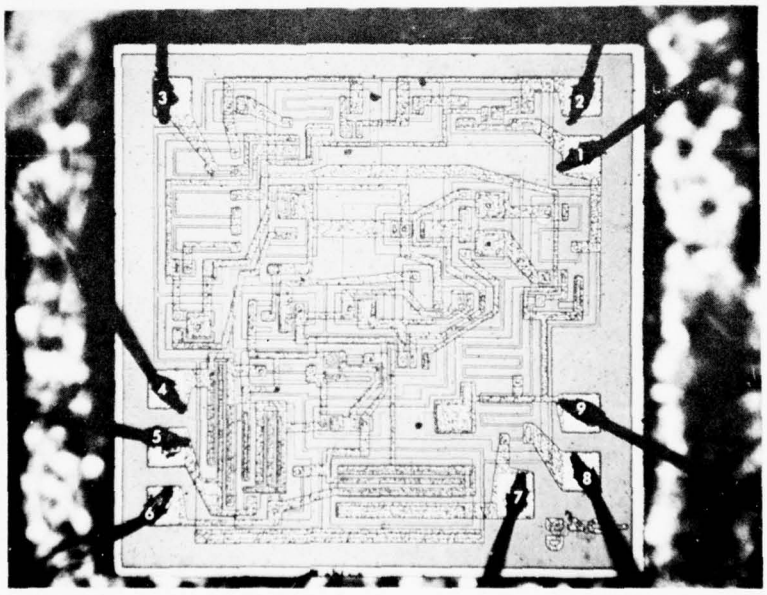
VIEW WITH LID REMOVED



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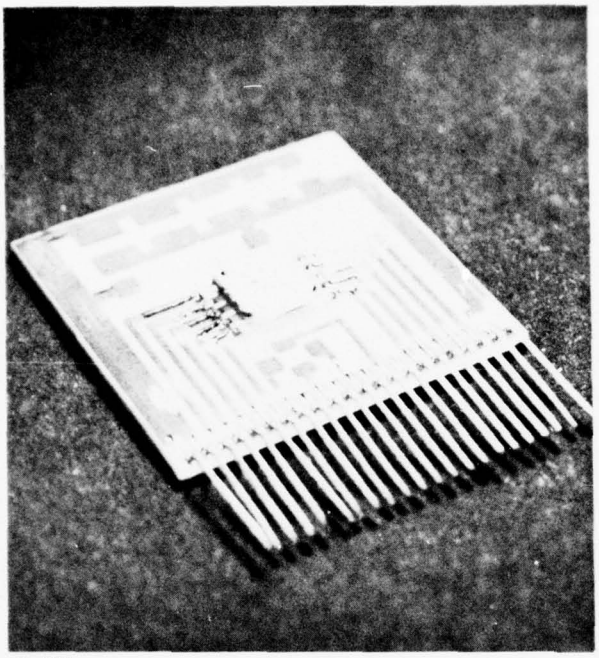
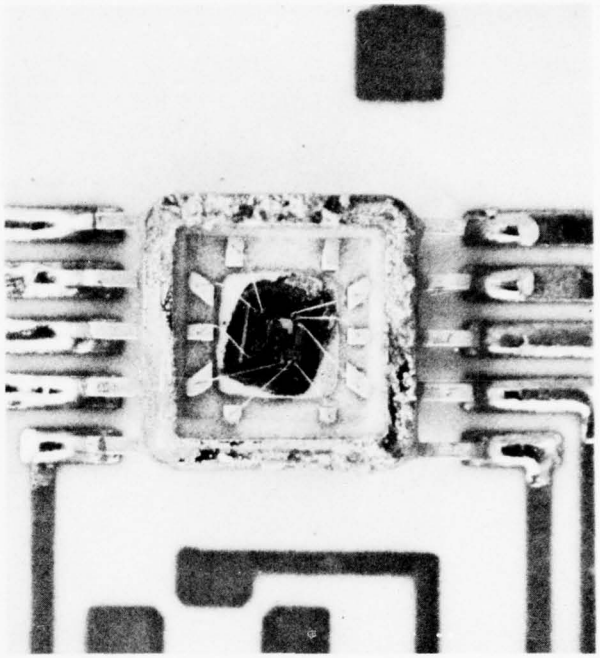
DIE TOPOGRAPHY

FIGURE G3. INTERNAL CONSTRUCTION DETAILS - P/N 773051 - VOLTAGE REGULATOR



1.9X

EXTERNAL



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INTERNAL

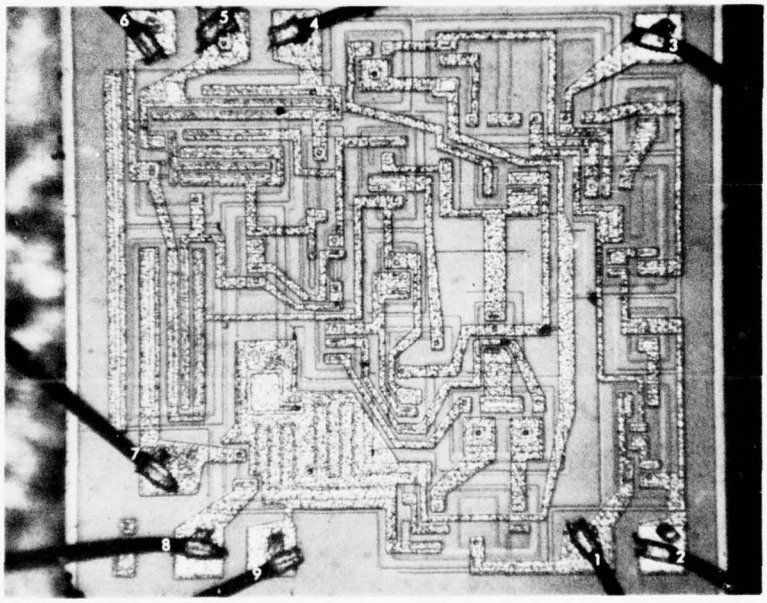

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FIGURE G4. TYPICAL SAM-D CONFIGURATION - P/N 773337 - VOLTAGE REGULATOR

TABLE G2. ELECTRICAL TEST CONDITIONS - P/N 773051 - VOLTAGE REGULATOR

TEST NO.	SYMBOL	V+ (VOLTS)	V- (VOLTS)	R_{REF} (OHMS)	R_{ADJ} (OHMS)	RELAYS SELECTED ⚠	+125°C>T_A>-55°C MIN	+125°C>T_A>-55°C MAX	UNITS
1	V_{OUT}	0	-15	2.4K	5K	K1,K3,K4,K5	-11.0	-9.0	V_{dc}
2	I_{QSC}	0	-50	2.4K	5K	K2,K5	----	3.5	mA
3	$V_{REG}(-12)$	0	-12	2.4K	5K	K1,K3,K4,K5	----	----	V_{dc}
4	$V_{REG}(-50)$	0	-50	2.4K	5K	K1,K3,K4,K5	----	----	V_{dc}
5	V_{REG}	$V_{REG} = V_{REG}(-12) - V_{REG}(-50)$					-150	+150	mV
6	V_{SF}	$V_{SF} = V_{OUT}/5{,}000$					1.8	2.2	V/KΩ

⚠ REFERENCE FIGURE G5.

INITIAL AND FINAL TEST CONDUCTED AT +25°C, +125°C AND -55°C.
INTERIM TEST CONDUCTED AT +25°C.

ELECTRICAL TEST FIXTURE

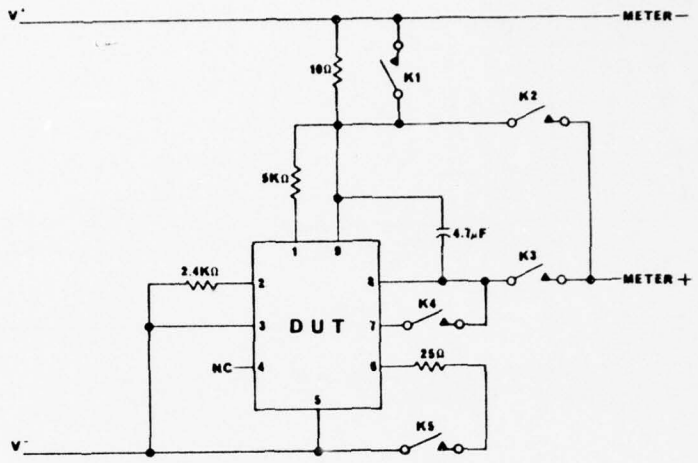
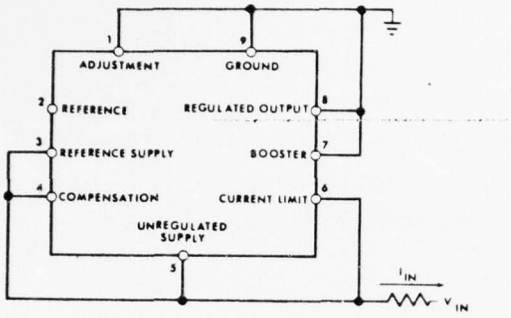
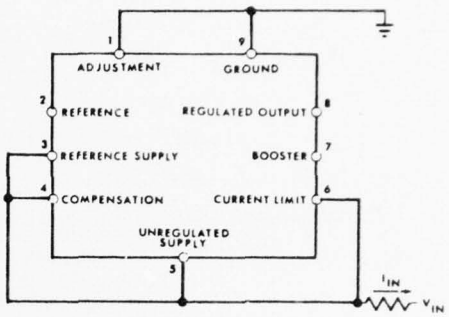


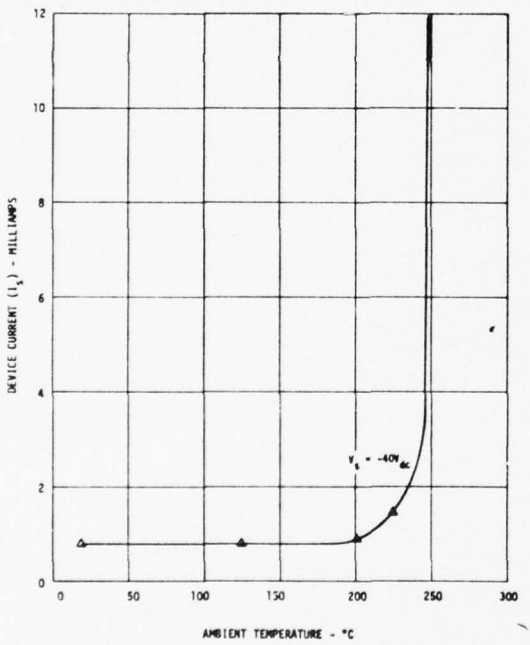
FIGURE G5. ELECTRICAL TEST FIXTURE - P/N 773051 - VOLTAGE REGULATOR



BIAS CIRCUIT 1



BIAS CIRCUIT 2



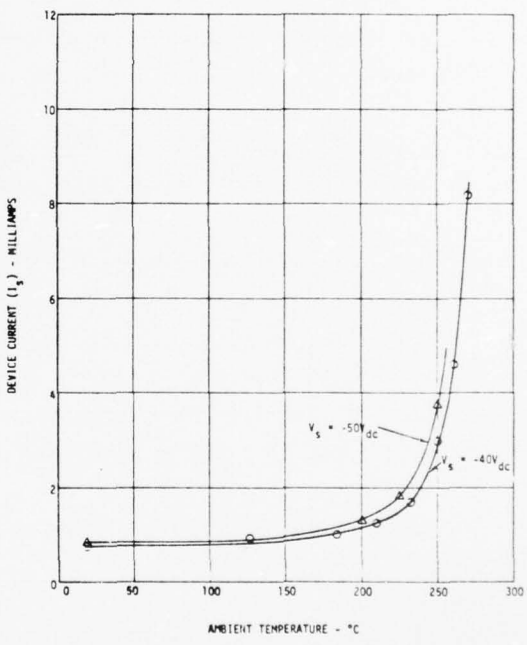


FIGURE G6. BIAS CIRCUIT EVALUATION - P/N 773051 - VOLTAGE REGULATOR

G5.0 STEP STRESS TEST RESULTS

A step stress test on 20 devices in bias circuit 2 was performed. The voltage on the parts was -40 volts. Four 16 hour steps, the first at 175°C and the last at 250°C, generated five failures. All of the failures were marginal and four of them recovered with an 8 hour, 225°C bake. It was decided to subject these devices to three additional steps of 16 hours with the unregulated supply voltage at -50 volts. Six marginal failures, including the five previous failures and one new failure, were observed. Figure G7 contains a step stress test summary. It was concluded that the life test could be run with -50 volts as the maximum voltage and 250°C the maximum ambient temperature.

G6.0 LIFE TEST CONDITIONS AND RESULTS

A summary of the life test conditions appears in Figure G7. The Table G3 life test summary shows Cell 1 was terminated after 512 hours with 22 failures, and the remaining cells continued to the 4000 hour readout. Failures were experienced in all the cells having an applied bias. The zero volt cell experienced no failures.

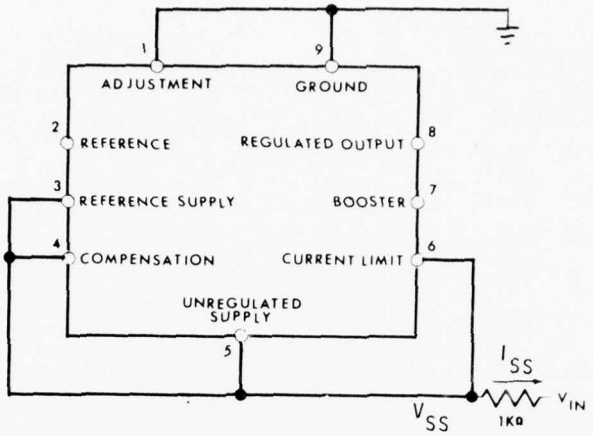
G7.0 FAILURE ANALYSIS

The failure analysis results are summarized in Table G4.

Surface Instability Failures - Forty-one (41) parts failed line regulation (V_{REG}) during the life tests. Twenty-two (22) parts exhibited negative failed values ranging from -165 mV to -562 mV. Nineteen (19) parts exhibited positive failed values ranging from +154 mV to +8032 mV. Failed parts would recover completely if baked or if stored at room temperature which is indicative of a surface instability mechanism involving mobile ionic contamination in or on the passivation.

The degradation could not be isolated to a specific junction or component via curve tracer pin-pin testing of failed parts. For this reason and because no failures of this type occurred in the storage cell, no further troubleshooting of the circuit was performed. Microscopic examinations of failed parts after delidding disclosed that the die surface of most of the parts contained one or more spots of contamination which appeared to be either a residue or debris. A worst case example is shown in Figures G8 and G9. SEM examination of the

STEP STRESS AND LIFE TEST CIRCUIT



STEP STRESS TEST - FAILURE SUMMARY (20 DEVICES)

AMBIENT TEMP (°C)	V_{SS} (V)	CUMULATIVE FAILURES
175	-40	0
200	-40	0
225	-40	3
250	-40	5
BAKE-OUT	0	1
200	-50	4
225	-50	6
250	-50	6

LIFE TEST CONDITIONS

TEST CELL NUMBER	T_A AMBIENT TEMPERATURE (°C)	V_{SS} DEVICE VOLTAGE (VOLTS)	I_{SS} DEVICE CURRENT (MILLIAMPS)	P_d POWER DISSIPATION (MILLIWATTS)	T_J JUNCTION TEMPERATURE (°C)
1	250	50	3.7	185	264
2	250	25	2.3	58	254
3	250	0	0	0	250
4	225	50	1.8	90	233
5	200	50	1.3	65	206

FIGURE G7. STEP STRESS RESULTS AND LIFE TEST CONDITIONS - P/N 773051 - VOLTAGE REGULATOR

TABLE G3. LIFE TEST SUMMARY - P/N 773051 - VOLTAGE REGULATOR

TEST CELL DESCRIPTION				CUMULATIVE FAILURES AT HOURS OF TEST										
CELL NO	APPLIED BIAS	AMBIENT TEMP.	QUANTITY	4	8	16	32	64	128	256	512	1000	2504	4000
1	50 VDC	250 C	30	3	4	4	8	11	15	16	22*			
2	25 VDC	250 C	30	0	0	0	0	0	0	0	1	1	3	3*
3	0 VDC	250 C	30	0	0	0	0	0	0	0	0	0	0	0*
4	50 VDC	225 C	30	2	2	4	5	6	6	7	7	7	11	11*
5	50 VDC	200 C	30	0	0	0	1	3	5	5	5	5	6	6*

* TEST TERMINATED

TABLE G4. FAILURE ANALYSIS SUMMARY - P/N 773051 - VOLTAGE REGULATOR

	A. FAILED PARAMETER OR SYMPTOMS	QUANTITY OF FAILURES AND TIME (HOURS) OF FAILURE				
	B. FAILURE MODE	250°C			225°C	200°C
	C. FAILURE MECHANISM	50 V	25 V	0 V	50 V	50 V
	D. CAUSE OF FAILURE	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5
SURFACE INSTABILITY FAILURES	A. V_{REG}	3@3	1@512		2@4	1@32
	B. NOT DETERMINED	1@8	2@2504		2@16	2@64
	C. PROBABLY MOBILE ION DRIFT	4@32			1@32	2@128
	D. PROBABLY CONTAMINATION IN THE PASSIVATION	3@64			1@64	
		4@128			1@256	
		1@256			4@2504	
		6@512				
TEST ERROR	A. CATASTROPHIC					1@2504
	B. NONE (RETEST OK)					
	C. NONE					
	D. TEST SET FAULT					
	TOTAL NUMBER OF FAILED PARTS	22	3	0	11	6

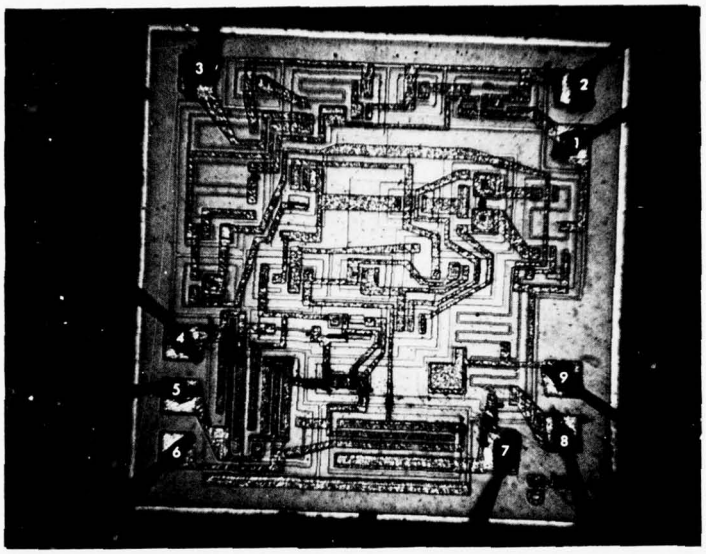


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FIGURE G8. EXAMPLE OF CONTAMINATED DIE - P/N 773051 - VOLTAGE REGULATOR

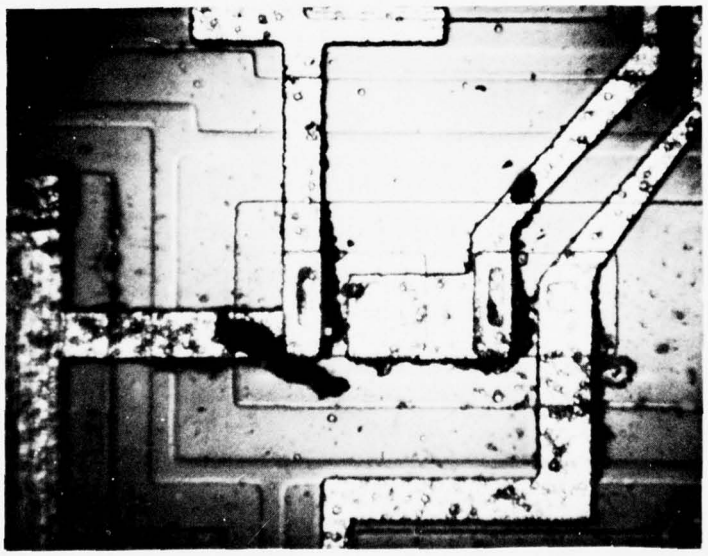

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FIGURE G9. CLOSEUP OF THE CONTAMINATION - P/N 773051 - VOLTAGE REGULATOR

contamination, Figures G10 and G11, showed that it was located on top of the glassivation and that the glassivation was intact. Thus, it is unlikely that the contamination was responsible for the instability of these parts. More probably, the instability resulted from ions or charges in the passivation that were introduced during device processing.

Test Error - One part failed catastrophically (no output voltage or supply current) during the life test. The failed parameters could not be verified during a bench test (all parameters were normal) and internal examinations and wire pull tests disclosed no deficiency which could have caused intermittent operation. Therefore, this failure was probably caused by a test set fault such as an intermittent connection.

G8.0 DATA CORRELATION

Excepting the one test induced failure, the Table G4 Failure Analysis Summary sttributes mobile ion drift as the probable failure mechanism for the 41 test failures. This failure mechanism appears to be voltage/temperature/time dependent, as evidenced by the total number of failures attributed to each test cell. Cell 3 (0 volt, 250°C) had no failures in 4000 hours, indicating that the mobile ion drift is not applicable to a storage environment or that the test was not long enough.

The failed parameter, line regulation (V_{REG}), has a specified range of $\pm$150 mV. The early failures tended to exceed the upper limit (+150 mV) while the later failures exceeded the lower limit (-150 mV). As shown in Table G2, V_{REG} is calculated using the following equation:

$$V_{REG} = V_{REG}(-12) - V_{REG}(-50)$$

Both $V_{REG}(-12)$ and $V_{REG}(-50)$ are negative voltages. At the start of the life tests both parameters experienced a slight voltage shift in the positive direction. This shift was sufficient in some cases to produce failures exceeding the +150 mV limit. As the test progressed the value of $V_{REG}(-50)$ tended to degrade (increase in the positive direction) at a greater rate than $V_{REG}(-12)$, resulting in failures exceeding the -150 mV limit. Where failed parts were allowed to continue in test,

400X (SEM)

FIGURE G10. SEM PHOTO OF THE CONTAMINATION ON THE SURFACE OF THE GLASSIVATION LAYER - P/N 773051 - VOLTAGE REGULATOR

600X (SEM)

FIGURE G11. SEM CLOSEUP OF THE CONTAMINATION - P/N 773051 - VOLTAGE REGULATOR

the $V_{REG}(-50)$ parameter continued to degrade and sometimes exceeded the V_{OUT} maximum limit of -9 Vdc. The $V_{REG}(-50)$ parameter in Cell 3, the zero volt cell, displayed good stability throughout the 4000 hour test and showed no degradation trends. While this precluded use of extrapolation techniques to predict Cell 3 failure times, sufficient trends were indicated in Cells 2 and 5 to provide extrapolated failure times to supplement the actual Cells 2 and 5 failures.

Figures G12 and G13 show the cumulative failure distributions for Cells 1, 2, 4 and 5. Each exhibits a bimodal failure distribution, indicative of a "freak" and "main" population. The significant distribution data are summarized in Table G5. The Cell 2 data indicates that both the "freak" and "main" failure distributions are sensitive to the magnitude of applied bias, a conclusion further corroborated by the absence of failures in the zero volt test cell.

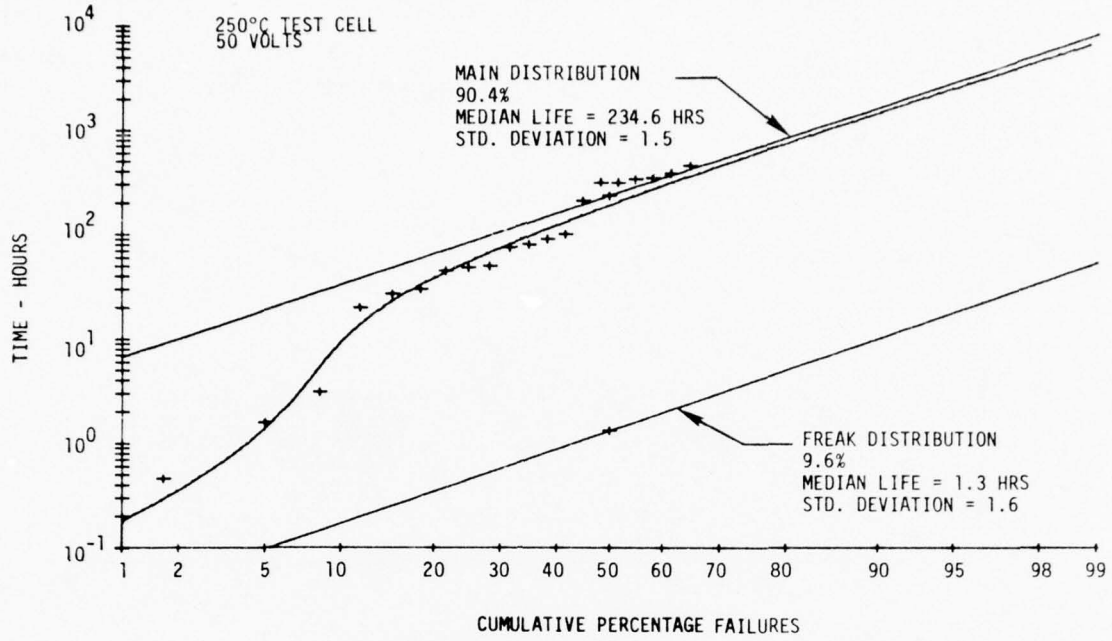
An Arrhenius evaluation of the three 50 volt test cells' data allows a conservative estimate of storage median lifetimes. The Arrhenius plots of Figure G14 of the "freak" and "main" distributions can be represented by the following equations:

$$\ln (t_{50\%})_{freak} = -22.7364 + \frac{1.358}{kT}$$

$$\ln (t_{50\%})_{main} = -33.0669 + \frac{2.0115}{kT}$$

Included in Figure G14 is 25 volt data from Cell 2. Assuming the same "freak" and "main" population activation energies established for the 50 volt data allows projection of median lifetimes for the reduced voltage condition. Under these conditions approximately a two order of magnitude improvement in median lifetime is realized by reducing voltage from 50 to 25 volts.

The 25 volt data was used to develop a conservative estimate for a storage failure rate. Using the "pooled" technique for determining the standard deviation, the following expression was derived for the instantaneous failure rate:



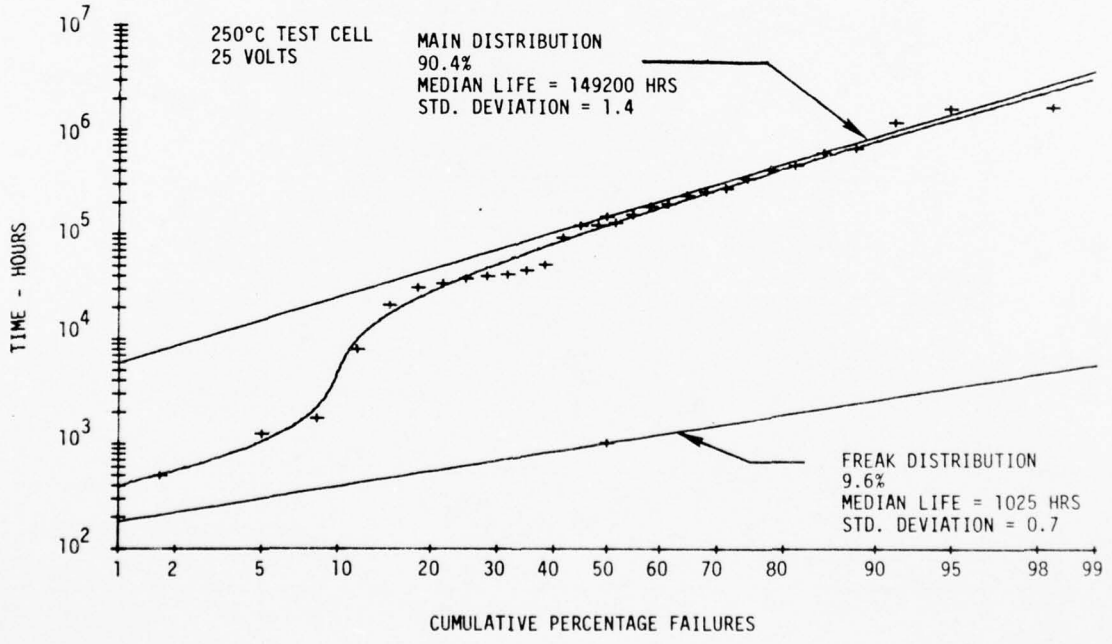


FIGURE G12. CELL 1 (TOP) AND CELL 2 (BOTTOM) CUMULATIVE FAILURE DISTRIBUTIONS - P/N 773051 - VOLTAGE REGULATOR

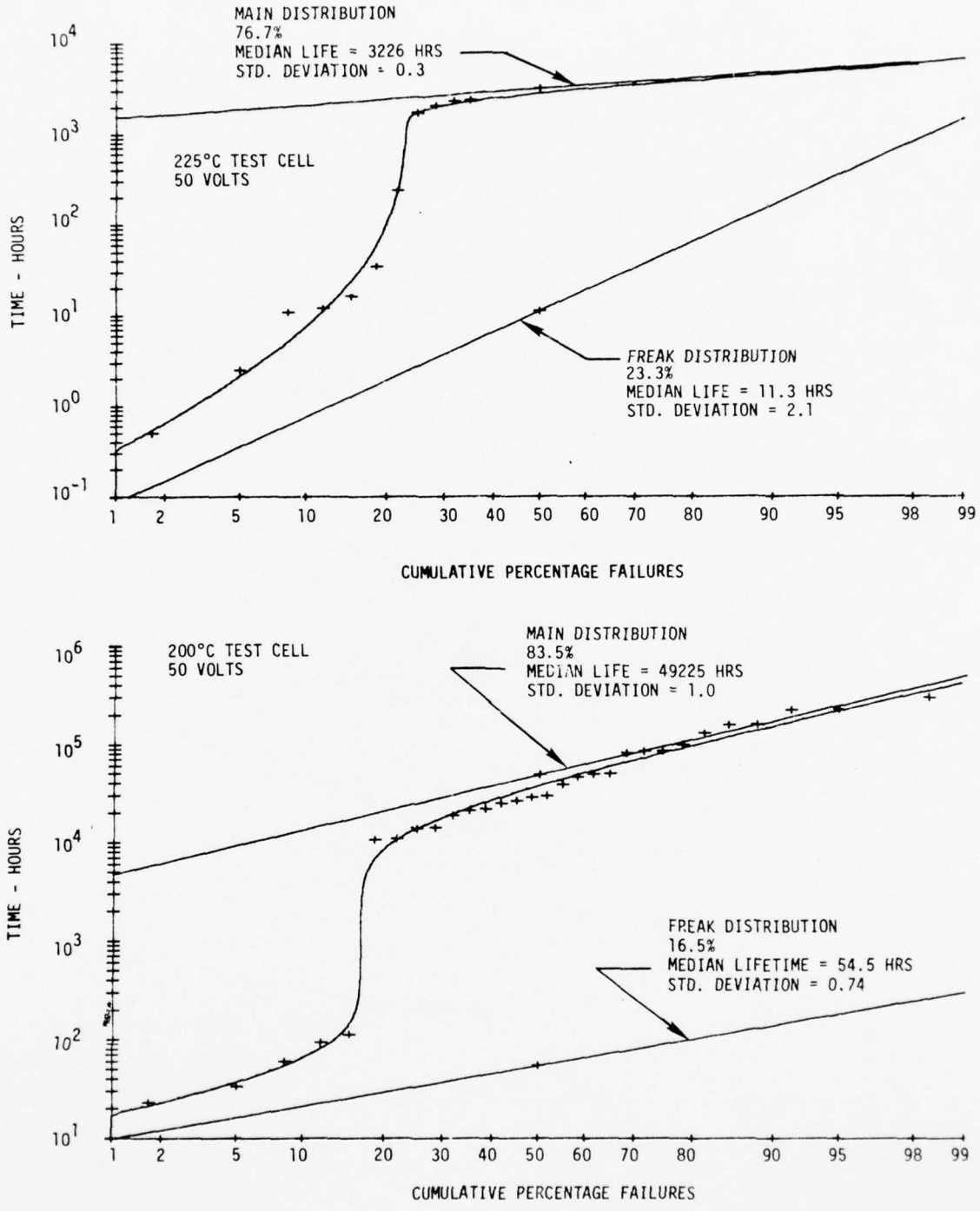


FIGURE G13. CELL 4 (TOP) AND CELL 5 (BOTTOM) CUMULATIVE FAILURE DISTRIBUTIONS - P/N 773051 - VOLTAGE REGULATOR

TABLE G5. DISTRIBUTION DATA SUMMARY - P/N 773051 - VOLTAGE REGULATOR

CELL NO.	TEST VOLTAGE	T_A (°C)	T_J (°C)	FREAK DISTRIBUTION			MAIN DISTRIBUTION		
				MEDIAN LIFE (HOURS)	STANDARD DEVIATION (HOURS)	%	MEDIAN LIFE (HOURS)	STANDARD DEVIATION (HOURS)	%
1	50V	250	278	1.3	1.6	9.6	234.6	1.5	90.4
2	25V	250	258	1,025.0	0.7	9.6	149,200.0	1.4	90.4
3	0V	250	250	-	-	-	72,740.0	.9	100.0
4	50V	225	243	11.3	2.1	23.0	3,226.0	0.3	76.7
5	50V	215	200	54.5	0.74	16.5	49,225.0	1.0	83.5

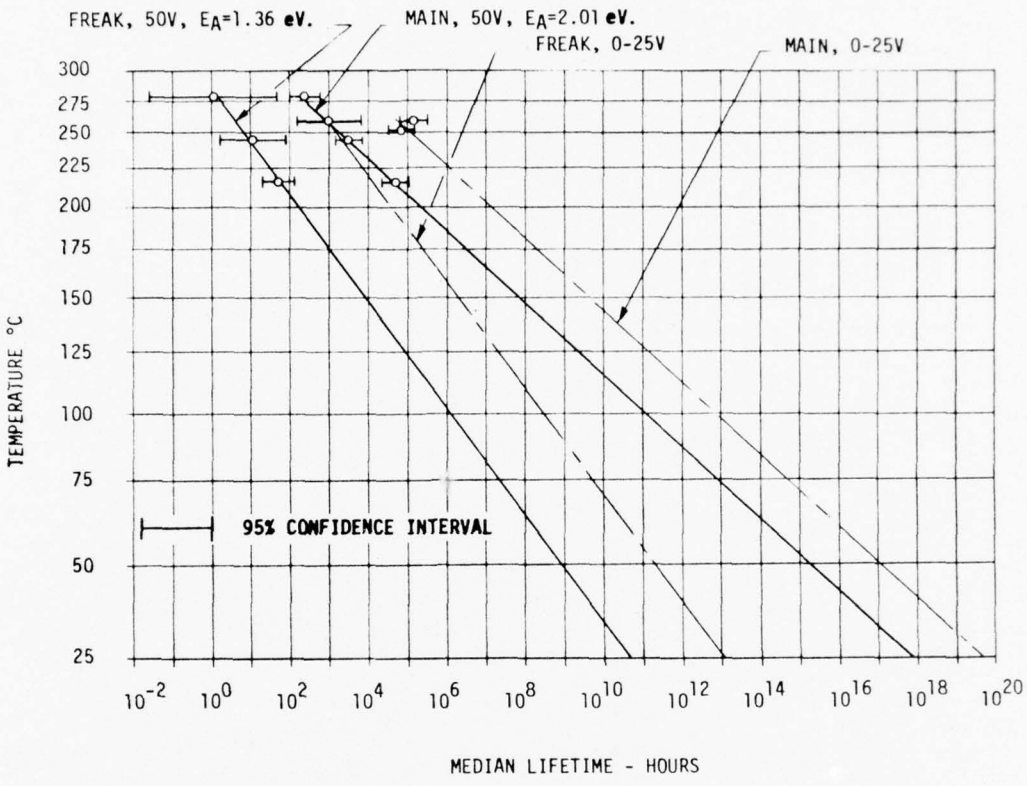


FIGURE G14. ARRHENIUS PLOTS - P/N 773051 - VOLTAGE REGULATOR

$$\lambda(t)_{\text{ZERO VOLT}} = \left[\frac{\frac{1}{t} \exp - \frac{\left[\ln t + 22.7364 - 1.3580\left(\frac{1}{kT}\right)\right]^2}{2(1.61)^2}}{\int_t^\infty \frac{1}{t'} \left[\exp - \frac{\left[\ln t' + 22.7364 - 1.3580\left(\frac{1}{kT}\right)\right]^2}{2(1.61)^2} \right] dt'} \right] \times 0.10$$

$$+ \left[\frac{\frac{1}{t} \exp - \frac{\left[\ln t + 33.0669 - 2.0115\left(\frac{1}{kT}\right)\right]^2}{2(1.66)^2}}{\int_t^\infty \frac{1}{t'} \left[\exp - \frac{\left[\ln t' + 33.0669 - 2.0115\left(\frac{1}{kT}\right)\right]^2}{2(1.66)^2} \right] dt'} \right] \times 0.90$$

The calculated maximum instantaneous failure rate, $\lambda(t)_{MAX}$, for the storage time (20 years) and temperature range (25°C-100°C) of interest is 3.25×10^{-10} failures per hour. An appropriate screening test (250°C, 50 volts, 24 hours) would remove over 90% of the freak population and improve the failure rate.

Since the calculated failure rate is based on derivations involving the 25 volt data, the storage failure rate is expected to be much better. The use of the screening test to eliminate the majority of the "freaks" would result in an improved operational failure rate.

G9.0 CONCLUSIONS AND RECOMMENDATIONS

- No failures were encountered during the 4000 hour, zero volt test at 250°C, indicating this voltage regulator has a high storage reliability potential.
- Data analysis revealed that both voltage and temperature are life accelerators. Use of voltage generated data allows prediction of a conservative failure rate (3.25×10^{-10} failures per hour) for a storage condition.

- Voltage generated failure distributions reveal presence of "freak" and "main" populations. A 24 hour screening test conducted at 250°C with 50 volts bias would eliminate over 90% of the "freak" population.

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STORAGE RELIABILITY OF MISSILE MATERIEL (ACCELERATED TESTING OF--ETC(U)
APR 77 J MCGARRY, V WEISSFLUG, E SISUL DAAH01-74-C-0928
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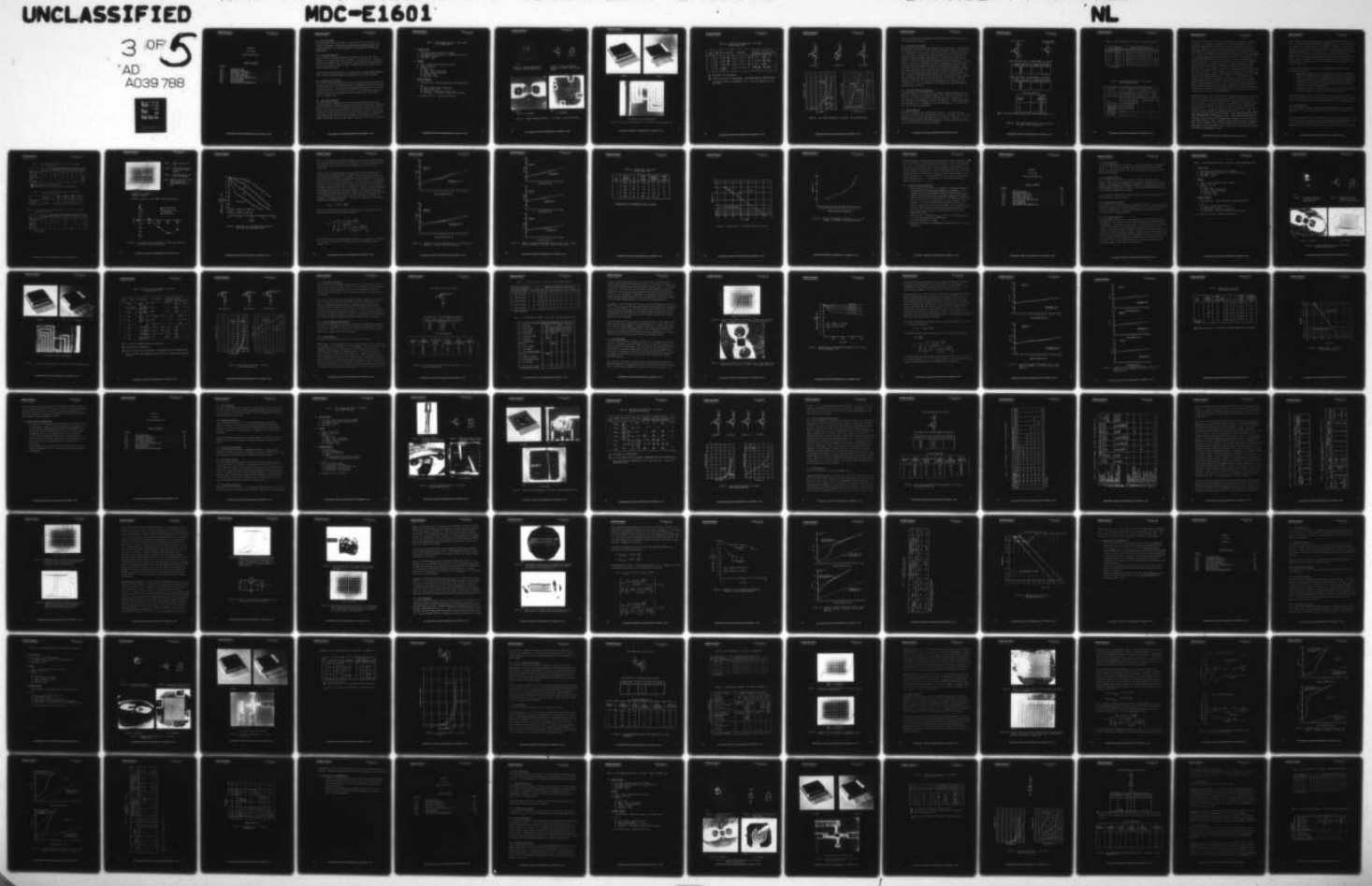

APPENDIX H

P/N 772928

NPN LOW POWER SWITCH

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H1.0 PART DESCRIPTION

The NPN Low Power Switch, P/N 772928, is a beam lead transistor mounted in a 3-lead, TO-18 package. The device was manufactured by Raytheon Company, Semiconductor Division. This test configuration is different from the SAM-D use configuration.

H2.0 CONSTRUCTION ANALYSIS

Table H1 summarizes the pertinent physical details of the test part, while Figures H1, H2 and H3 present pictorial details. The beam lead die is bonded to the gold plated header of the TO-18 package. Hermetic sealing is accomplished by a glass lead seal and a welded cap seal. This part contains no materials which limited testing below 300°C.

Figure H4 shows the beam lead die as it would be used in a typical SAM-D application. The die is beam lead bonded to metallization on a ceramic substrate.

H3.0 ELECTRICAL TEST CRITERIA

Initial tests were conducted; however, due to a problem which was discovered after the first step stress, a second initial test was conducted on this device and used as the baseline data. The electrical test measurements performed for this second initial test as well as the interim and final tests are identified in Table H2. The problem which was discovered after the first step stress is discussed in detail in paragraph H7.0.

H4.0 BIAS CIRCUIT ANALYSIS

The three Figure H5 candidate bias circuits were evaluated to determine their current/temperature relationship and device stability as a function of temperature. Bias circuit 1 had 1.0 volt reverse bias across the emitter-base junction and a variable voltage source on the collector. Bias circuit 2 and bias circuit 3 had 0 volt and 3.5 volts reverse bias across the emitter-base junction, respectively, and variable voltage sources on their collectors. The results of testing at ambient temperatures up to 250°C are shown in Figure H5. Bias circuit 1 with 16.0

TABLE H1. PART CONSTRUCTION DETAILS - P/N 772928 - NPN LOW POWER SWITCH

A. IDENTIFICATION

1. Part Name: NPN Low Power Switch (2N3960)
2. Part Manufacturer: Raytheon Co., Semiconductor Division
3. Part Number: 772928
4. Date Code: 7537

B. PACKAGE

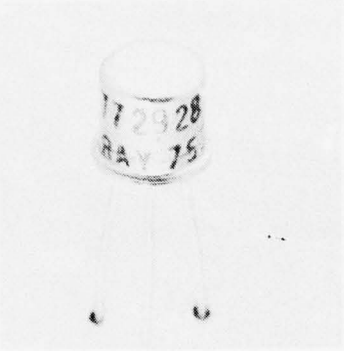
1. Type: 3-Lead, TO-18 (Drawing No. 757431)
2. Weight: 0.318 gram
3. Materials:
   a) Cap: Steel
   b) Header: Kovar, gold-plated
   c) Leads: Kovar, gold-plated
   d) Cap Seal: Weld
   e) Lead Seal: Glass

C. INTERNAL GEOMETRY

1. Interconnections: Beam leads bonded to gold-plated header.

2. Die:
   a) Type: Silicon, planar (Beam Lead)
   b) Scribe Method: Etch
   c) Dimension: 0.0145 inch x 0.0145 inch
   d) Passivation: Silicon Nitride over Silicon Dioxide

3. Metallization Type: Gold/Titanium/Platinum



3.4X

FIGURE H1. EXTERNAL CONSTRUCTION - P/N 772928 - NPN LOW POWER SWITCH

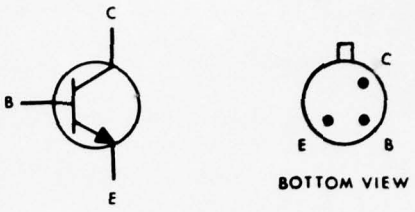
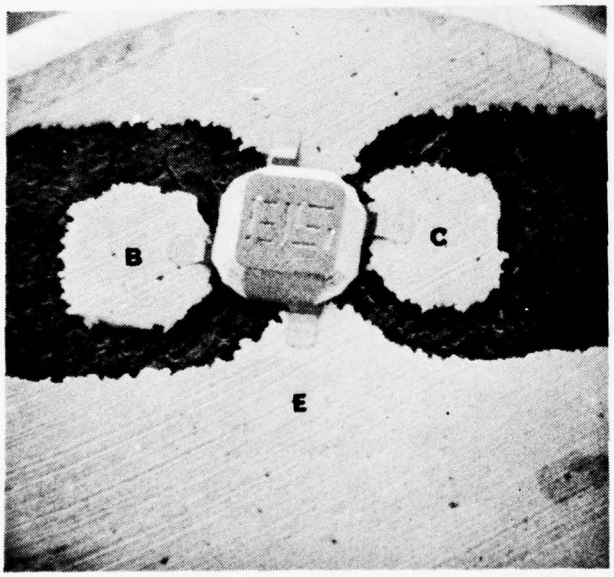


FIGURE H2. SYMBOL AND TERMINAL DIAGRAM - P/N 772928 - NPN LOW POWER SWITCH



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VIEW WITH LID REMOVED

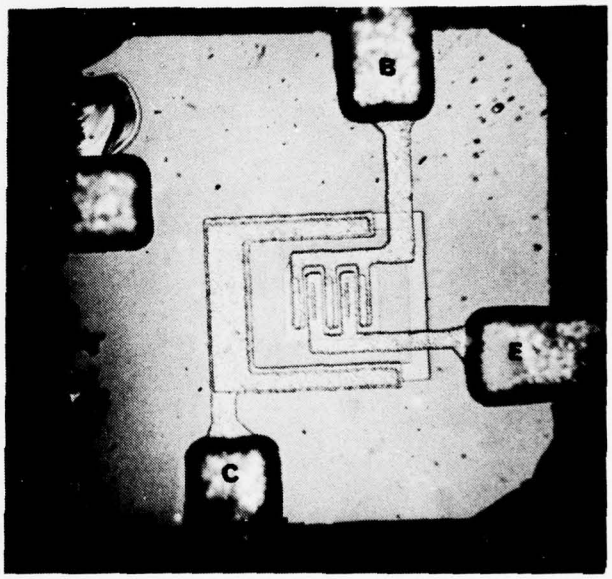

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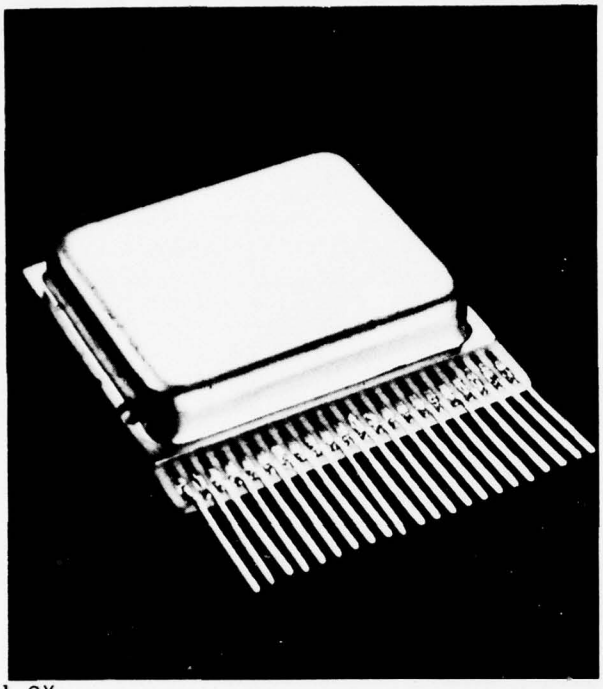
FIGURE H3. INTERNAL CONSTRUCTION DETAILS - P/N 772928 - NPN LOW POWER SWITCH



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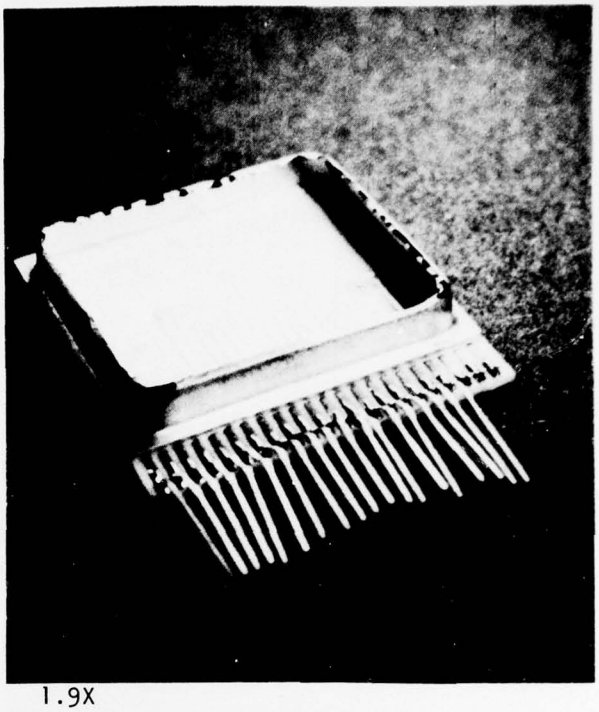
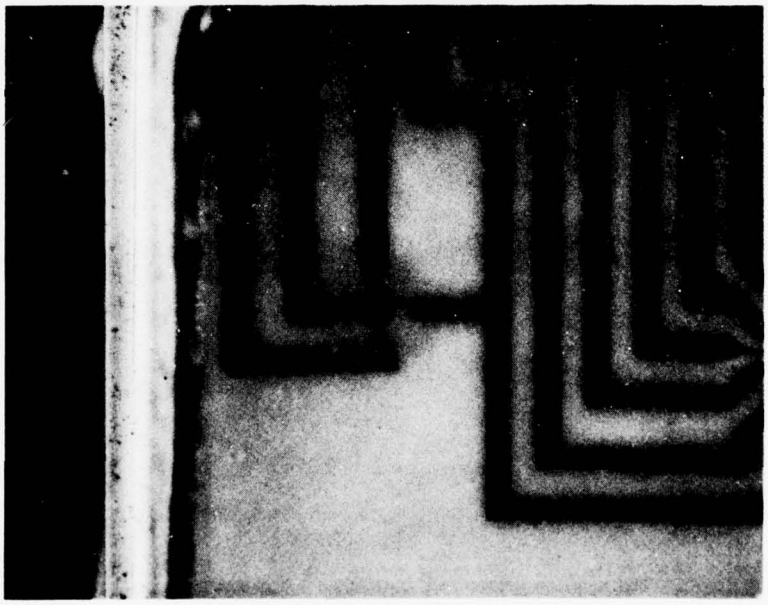
EXTERNAL



1.9X

INTERNAL



7X

DIE MOUNTED IN SAM-D CONFIGURATION

FIGURE H4. TYPICAL SAM-D CONFIGURATION - P/N 773379 - NPN LOW POWER SWITCH

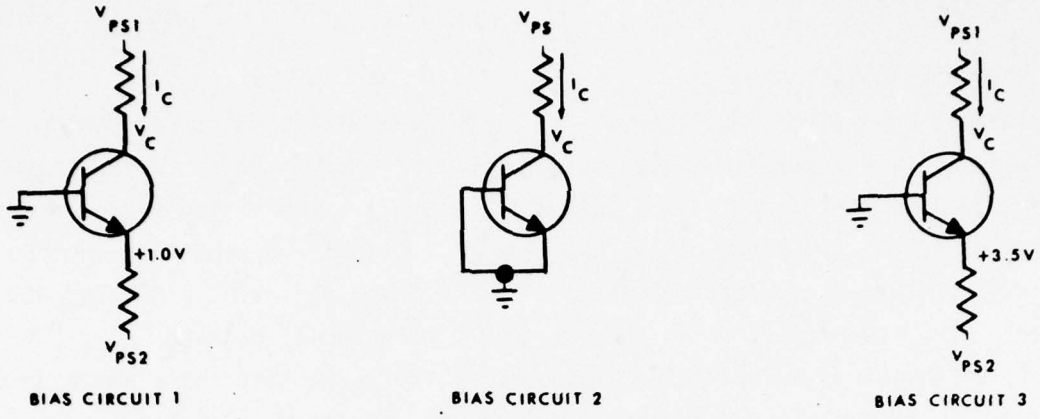
TABLE H2. ELECTRICAL TEST CONDITIONS - P/N 772928 - NPN LOW POWER SWITCH

TEST NO.	SYMBOL	MIL-STD-750	CONDITIONS	T_A=+25°C		T_A=+150°C		UNITS
				MIN	MAX	MIN	MAX	
1	H_{FE1}	3076 (1)	V_{CE} = 1.0V; I_C = 1.0mA	25	-	(2)	-	-
2	H_{FE2}	3076 (1)	V_{CE} = 1.0V; I_C = 10mA	40	200	(2)	(2)	-
3	H_{FE3}	3076 (1)	V_{CE} = 1.0V; I_C = 30mA	25	-	(2)	-	-
4	I_{CES}	3041.1 COND. C	V_{CE} = 10V; V_{EB} = 0V	(2)	(2)	(2)	(2)	µA

(1) EQUIVALENT TEST CONFIGURATION

(2) LIMITS NOT SPECIFIED BY PART DRAWING - MEASUREMENT MADE FOR INFORMATION ONLY.

INITIAL AND INTERIM TEST CONDUCTED AT +25°C. FINAL TEST CONDUCTED AT +25°C AND +150°C.



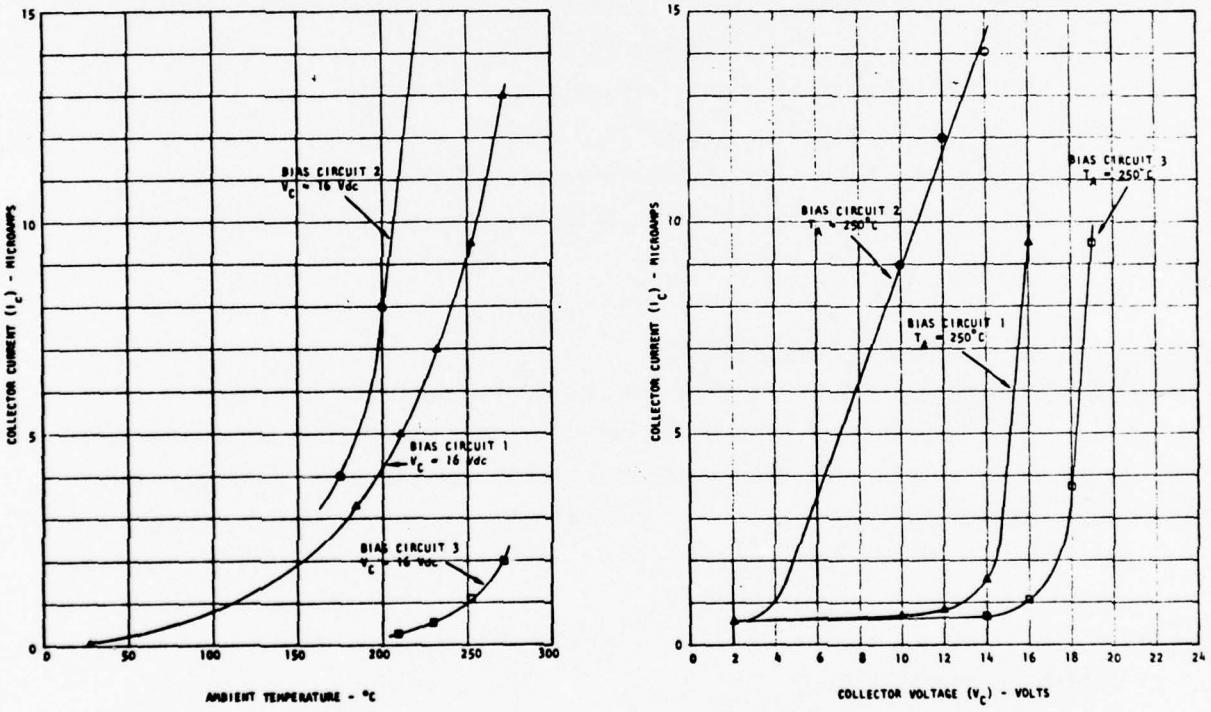


FIGURE H5. BIAS CIRCUIT EVALUATION - P/N 772928 - NPN LOW POWER SWITCH

volts on the collector was acceptable for the accelerated life test and was used in the first step stress test.

H5.0 STEP STRESS TEST RESULTS

An additional step stress test was conducted on this device due to a problem which was discovered after the first step stress was concluded. (Refer to paragraph H7.0 for a discussion of this problem.) The first step stress utilized bias circuit 1. Figure H6 contains a summary of the ambient temperatures for each step and the cumulative failures throughout the step stress. The duration of each step was 16 hours. The seven failures which were generated were all degraded h_{FE1}. Failure analysis of these parts determined that some of the parametric tests which were originally performed altered the condition of the emitter-base junction. Those tests were eliminated and all of the parts were subjected to a laboratory ambient test consisting of the Table H2 tests to serve as the initial baseline data. In addition it was decided that no bias should be applied to the parts during life test in order to avoid reversing the failure mode. Therefore, ten devices with no bias applied were subjected to a second step stress, the results of which are included in Figure H6. The three failures generated in this step stress test indicated that a life test consisting of five storage cells (unbiased) would be acceptable for this device.

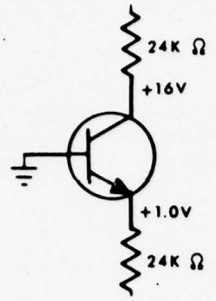
H6.0 LIFE TEST CONDITIONS AND RESULTS

Figure H6 contains a list of the life test condition (ambient temperatures) for each cell. As shown in the Table H3 summary, Cells 1 and 2 were terminated after 1000 hours of life test with twenty-six and thirty failures, respectively. The three remaining cells remained in life test for 4000 hours. Twenty-eight failures were generated in Cell 3, nineteen in Cell 4 and one in Cell 5. All of the life test failures were h_{FE1} degradation.

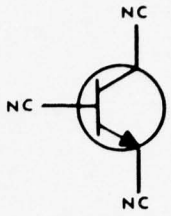
H7.0 FAILURE ANALYSIS

Table H4 is a summary of the failure analysis results. Ten parts failed h_{FE1} during the step stress tests and 104 parts failed h_{FE1} during the life tests. The parameter h_{FE1} has a specified minimum limit of 25 at V_{CE} = 1 Vdc and I_C = 1 mA. The 114 parts displayed no other failed parameter. All h_{FE1} failures were attributed to the same surface instability mechanism.

FIRST STEP STRESS CIRCUIT



SECOND STEP STRESS AND LIFE TEST CIRCUIT



FIRST STEP STRESS TEST - FAILURE SUMMARY (20 DEVICES)

AMBIENT TEMP (°C)	CUMULATIVE FAILURES
200	0
225	0
250	6
275	7

SECOND STEP STRESS - FAILURE SUMMARY (10 DEVICES)

AMBIENT TEMP (°C)	CUMULATIVE FAILURES
200	0
225	0
250	1
275	3

LIFE TEST CONDITIONS

TEST CELL NUMBER	T_A ⚠1 AMBIENT TEMPERATURE (°C)
1	250
2	225
3	200
4	175
5	150

⚠1 ALL CELLS ARE STORAGE (WITHOUT BIAS) CELLS AND THEREFORE, $T_A = T_J$.

FIGURE H6. STEP STRESS RESULTS AND LIFE TEST CONDITIONS - P/N 772928 - NPN LOW POWER SWITCH

TABLE H3. LIFE TEST SUMMARY - P/N 772928 - NPN LOW POWER SWITCH

TEST CELL DESCRIPTION				CUMULATIVE FAILURES AT HOURS OF TEST										
CELL NO.	APPLIED BIAS	AMBIENT TEMP.	QUANTITY	4	8	16	32	64	128	256	512	1000	2500	4000
1	0	250°C	30	0	0	0	2	5	17	20	25	26*		
2	0	225°C	30	0	0	0	0	2	20	25	27	30*		
3	0	200°C	30	0	0	0	0	0	0	6	11	19	27	28*
4	0	175°C	30	0	0	0	0	0	0	0	0	2	9	19*
5	0	150°C	30	0	0	0	0	0	0	0	0	0	0	1*

* TEST TERMINATED

TABLE H4. FAILURE ANALYSIS SUMMARY - P/N 772928 - NPN LOW POWER SWITCH

A. FAILED PARAMETER B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TIME OF FAILURE (HOURS)						
	0 VDC					V_{CE}=15 VDC	0 VDC
	250°C	225°C	200°C	175°C	150°C	INITIAL STEP STRESS	SECOND STEP STRESS
	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5		
	2@32	2@64	6@256	2@1000	1@4000	6@250°C Step	1@250°C Step
A. h_{FE1}	3@64	18@128	5@512	7@2500		1@275°C Step	2@225°C Step
B. B-E DEGRADATION	12@128	5@256	8@1000	10@4000			
C. MOBILE ION DRIFT OR SURFACE STATES	3@256	2@512	8@2500				
D. PASSIVATION DESIGN/ PROCESSING OR CONTAMINATION	5@512 1@1000	3@1000	1@4000				
TOTAL NUMBER OF FAILED PARTS	26	30	28	19	1	7	3

During initial step stress testing, h_{FE1} displayed two inflections as evidenced in Table H5. It apparently increased as a result of the 200°C step, then decreased through the 225°C and 250°C steps, then increased as a result of the 275°C step. Analysis of the three failed parts removed after the 250°C step established that the low h_{FE1} was caused by degradation of the emitter-base junction. Further investigations disclosed that the emitter junction (and consequently the low-current h_{FE1}) of the device was unstable, even at room temperature. If the transistor was heated with no applied bias, the junction degraded (h_{FE1} will decrease) with time. If the emitter junction was reverse biased or avalanched, the b-e improved as illustrated in Figure H7. In this example, h_{FE1} of the transistor was 121 upon receipt. After baking the transistor for 64 hours at 250°C (no bias), h_{FE1} dropped to 24 and the b-e forward characteristic degraded to that shown by trace (1). After applying 5 volts reverse bias to the emitter junction for 5 minutes, h_{FE1} improved to 40 and V_{BE} to that shown by trace (2). After avalanching the emitter junction (V_{EB} = 7 volts, I_B = 1 microampere) for 30 seconds, h_{FE1} improved to 88 and V_{BE} to that shown by trace (3). By applying reverse emitter bias and heating the transistor for a few minutes, h_{FE1} could be made to increase beyond its original value. The cycle could then be repeated. These findings indicated that the mechanism responsible for the emitter junction instability was surface related and probably involved charging and discharging of surface states or ion drift in the passivation.

Examination of h_{FE1} of the 5 control sample transistors used during the first step stress test revealed that a shift in h_{FE1} occurred during parametric testing. These five devices saw no environmental stress and were tested along with the 20 step stress parts . As shown in Table H6, h_{FE1} increased two-fold between the first test (as-received) and the second test (post 200°C step), then remained stable thereafter. The h_{FE1} increase was traced to measurement of BV_{CBO}. Upon receipt, h_{FE1} was measured first followed in order by BV_{CBO}, I_{CEX}, V_{CESAT}, V_{BEON}, I_{CBO}, I_{EBO}, and BV_{CEO} (BV_{EBO} was not measured). Then, during incoming testing only, the measurements were repeated at 150°C. Experiments established that the increase in h_{FE1} was due in part to measurement of BV_{CBO} at 25°C and in part to measurement of BV_{CBO} at 150°C. Apparently these transistors contain a conductive path, such as a diffusion spike or pipe, between the collector and the emitter that causes a floating voltage to appear on the emitter and avalanche the emitter junction during measurement of BV_{CBO}.

These findings account for the variation of h_{FE1} during the initial step stress test. As shown in Figure H8, the apparent increase in h_{FE1} due to the 200°C step was caused by the incoming parametric measurements. Actually, h_{FE1} decreased from the start of the 200°C step through completion of the 250°C step due to time-temperature degradation of the emitter junction. The h_{FE1} increase that occurred after the 250°C step was suspected to be due to eventual improvement of the emitter junction caused by the one volt reverse bias on the junction during step stress. This was confirmed by performing a second step stress test on ten unbiased parts. As shown in Table H7, with no applied bias h_{FE1} did not improve during the 275°C step.

In view of these findings, the following changes were incorporated for the accelerated life testing:

- Measurement of BV_{CBO}, I_{CBO}, and I_{EBO} and other parameters at each test point was eliminated to avoid avalanching or reverse biasing the emitter-junction or affecting the h_{FE1} parameter during parametric measurements.
- Each device was remeasured to determine the values of h_{FE1} at the start of the life test (since all devices had been subjected to the complete incoming 25°C and 150°C measurements).
- No bias was applied to the parts during life test to avoid reversing the failure mode relevant to storage conditions (h_{FE1} decrease).

One hundred and four (104) parts failed due to low h_{FE1} during the life tests. Analysis of representative failures confirmed that the low h_{FE1} was due to degradation of the emitter base junction caused by mobile ion drift or surface states.

H8.0 DATA CORRELATION

The life tests were conducted using only elevated temperature as an accelerator. Therefore, all failures are considered directly applicable to a storage environment.

The Table H4 Failure Analysis Summary reveals that all test failures were attributed to a surface instability mechanism caused by passivation design/processing. In all cases this mechanism caused h_{FE1} degradation, as shown in Figure H9 plot of normalized h_{FE1} versus time. Note that one curve depicts both the 225°C and 250°C

TABLE H5. h_{FE1} DURING FIRST STEP STRESS TEST - P/N 772928 - NPN LOW POWER SWITCH

	AS RECEIVED	POST 16 HOUR 200°C STEP	POST 16 HOUR 225°C STEP	POST 16 HOUR 250°C STEP	POST 16 HOUR 275°C STEP
MEAN h_{FE1} @ 25°C	69	73	52	37	46
h_{FE1} RANGE	37-133	43-130	31-121	21-107	22-92
NO. OF PARTS ON TEST	20	20	20	20	17 (1)
NO. FAILED	0	0	0	6	1 (2)

(1) THREE OF THE SIX 250°C FAILURES WERE REMOVED.
(2) THE THREE PREVIOUS FAILURES RECOVERED; ONE PREVIOUSLY GOOD PART FAILED

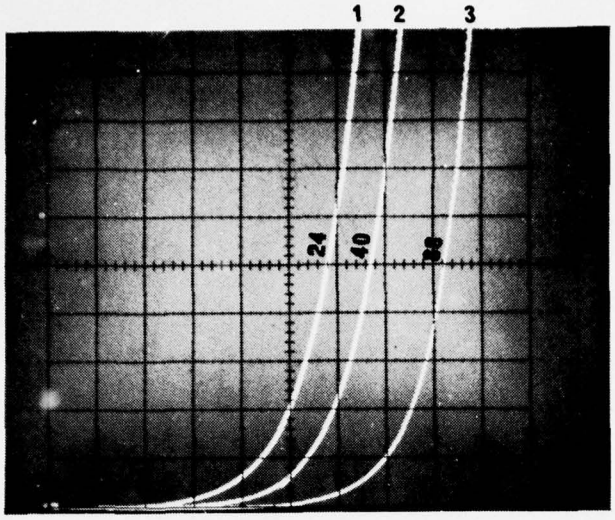
TABLE H6. h_{FE1} OF THE FIVE CONTROL SAMPLES - P/N 772928 - NPN LOW POWER SWITCH

	AS RECEIVED	200°C STEP	225°C STEP	250°C STEP	275°C STEP
MEAN h_{FE1} @ 25°C	42	90	92	92	92
h_{FE1} RANGE	35-48	83-98	84-100	81-100	81-100

TABLE H7. h_{FE1} DURING THE SECOND (UNBIASED) STEP STRESS - P/N 772928 - NPN LOW POWER SWITCH

	AS RECEIVED	PRE-STEP STRESS	POST 16 HR, 200°C STEP	POST 16 HR, 225°C STEP	POST 16 HR, 250°C STEP	POST 16 HR 275°C STEP
MEAN h_{FE1} @ 25 C°	53	93	53	40	32	27
h_{FE1} RANGE	35-81	69-107	34-65	26-48	22-41	19-34
NO. OF PARTS ON TEST	10	10	10	10	10	10
NO. FAILED	0	0	0	0	1	3 *

* TWO NEW FAILURES



TRACE 1 - AFTER 64 HOURS, 250°C BAKE

TRACE 2 - AFTER REVERSE BIASING (5 VDC) THE E-B FOR 5 MINUTES

TRACE 3 - AFTER AVALANCHING THE E-B FOR 30 SECONDS

NOTE - NUMBERS ALONG SIDE OF EACH TRACE INDICATE THE CORRESPONDING VALUES OF h_{FE1}

HORIZONTAL = 50 mV/DIV.
VERTICAL = 2nA/DIV.

FIGURE H7. V_{BE} VS. I_B - P/N 772928 - NPN LOW POWER SWITCH

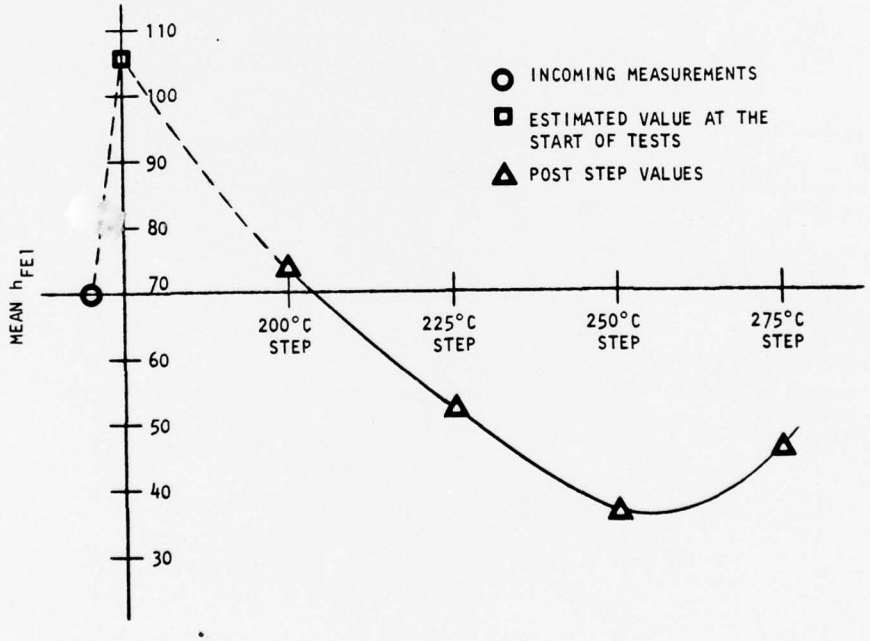


FIGURE H8. PLOT OF MEAN h_{FE1} AT 25°C DURING THE FIRST STEP STRESS TEST - P/N 772928 - NPN LOW POWER SWITCH

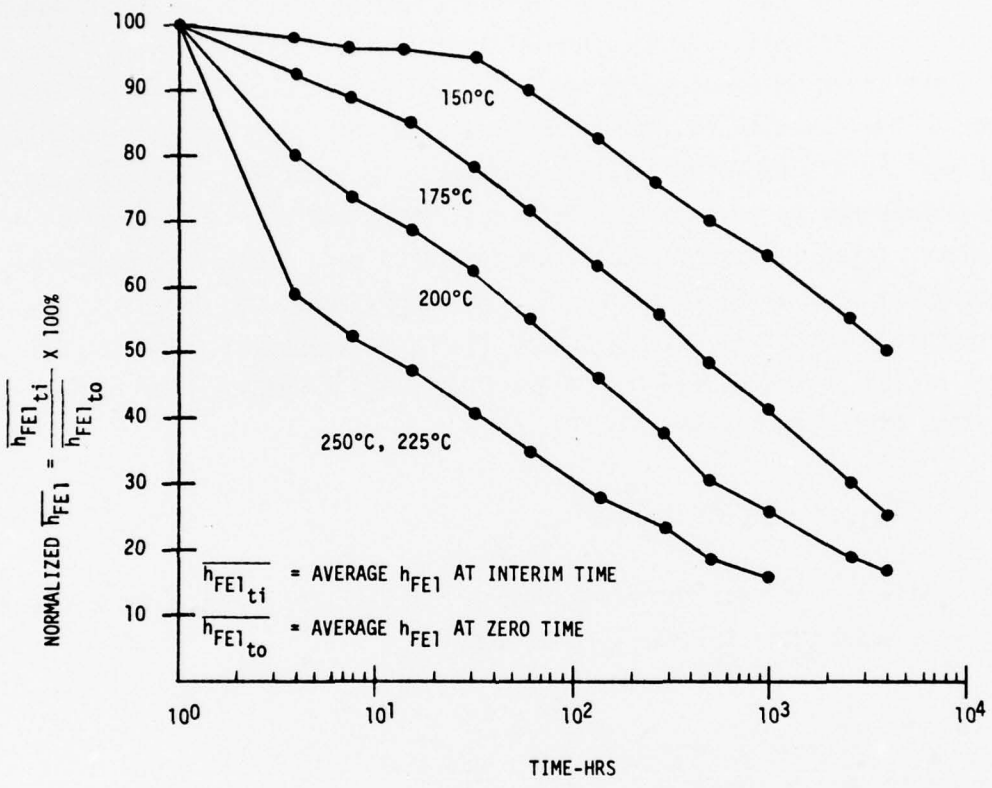


FIGURE H9. NORMALIZED h_{FE1} TIME/TEMPERATURE DEGRADATION - P/N 772928 - NPN LOW POWER SWITCH

test cells, indicating no discernible difference in their h_{FE1} degradation rates. The data shows that the initial rate of degradation is related to ambient temperature; however, after a period time the rates appear constant for all test temperatures.

The 150°C test cell experienced only one h_{FE1} failure during the 4000 hour life test but obvious degradation trends allowed the use of regression techniques to extrapolate times to failure. The cumulative failure distributions for the five test cells are shown in Figures H10 and H11. All show a good fit to the lognormal failure distribution, with no indication of a distinct freak and main population. Pertinent failure distribution data is summarized in Table H8. The fact that the two highest temperature test cells, 250°C and 225°C, had no discernible differences in degradation rates indicates that the degradation rate does not change above some temperature between 200°C and 225°C. Therefore, only the data from the three lower temperature cells, 200°C, 175°C, and 150°C, were used to establish the parameters of the Arrhenius equation. The Figure H12 Arrhenius plot can be represented by the following equation:

$$\ln t_{50\%} = -13.17986 + \frac{0.814}{kT}$$

Using the "pooled" technique to obtain standard deviation, storage failure rates were calculated using the following relationship:

$$\lambda(t) = \frac{\frac{1}{t} \exp - \frac{\left[\ln t + 13.17986 - \frac{0.814}{kT}\right]^2}{2(0.761)^2}}{\int_t^\infty \frac{1}{t'}\left[\exp - \frac{\left[\ln t' + 13.17986 - \frac{0.814}{kT}\right]^2}{2(0.761)^2}\right] dt'}$$

The Figure H13 plot of a 20-year storage failure rate as a function of temperature has a $\lambda(t)_{MAX}$ of 5.662×10^{-6} failures per hour in the temperature range of interest.

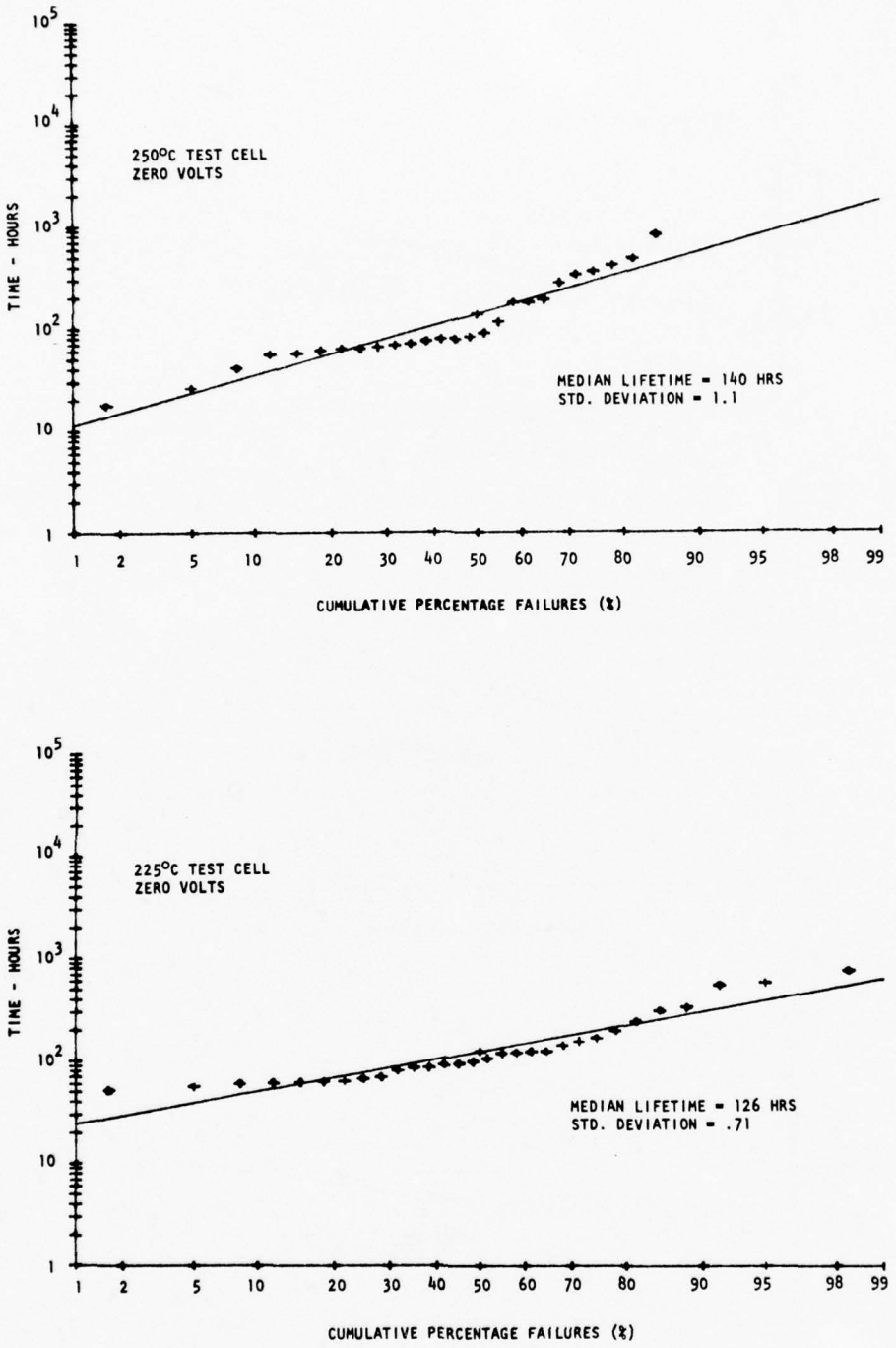


FIGURE H10. CUMULATIVE FAILURE DISTRIBUTIONS FOR CELL 1 (TOP) AND CELL 2 (BOTTOM) - P/N 772928 - NPN LOW POWER SWITCH

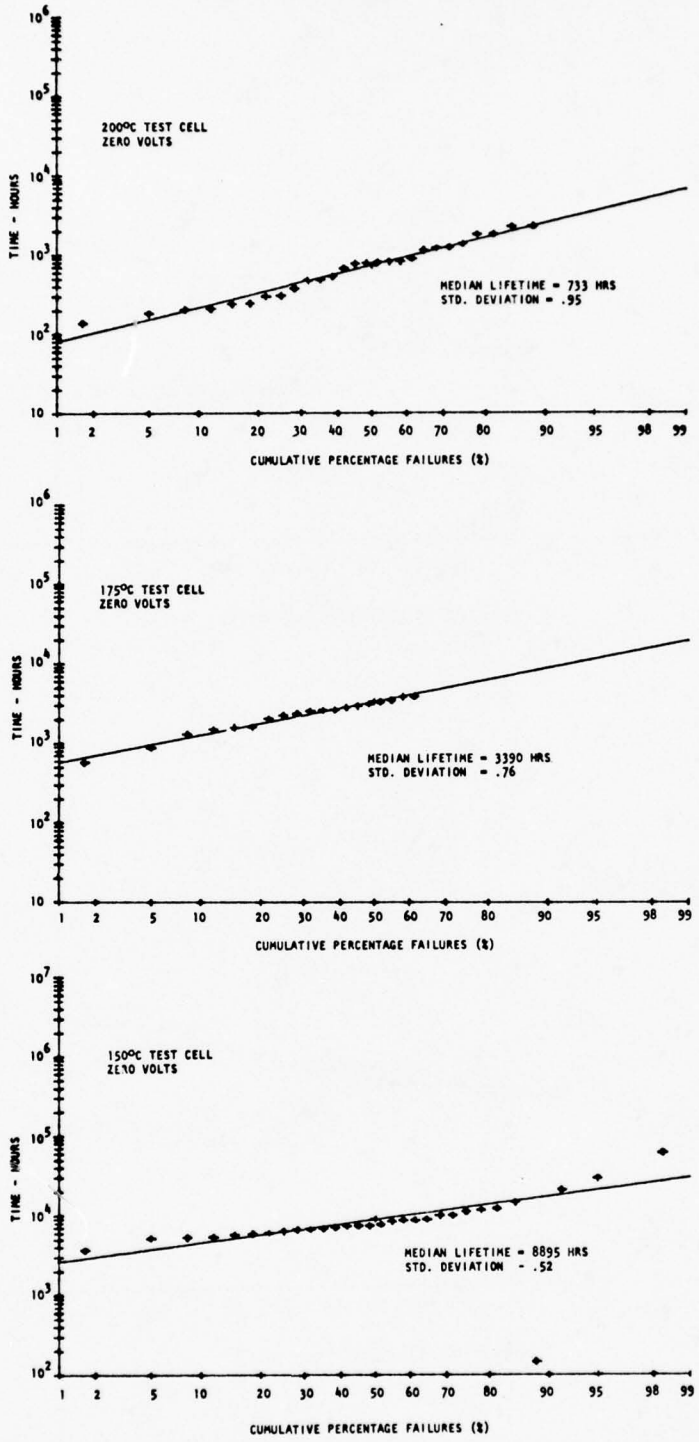


FIGURE H11. CUMULATIVE FAILURE DISTRIBUTIONS FOR CELL 3 (TOP), CELL 4 (MIDDLE) AND CELL 5 (BOTTOM) - P/N 772928 - NPN LOW POWER SWITCH

TABLE H8. SUMMARY DATA - P/N 772928 - NPN LOW POWER SWITCH

CELL NO.	TEST VOLTAGE (VOLTS)	T_A (°C)	MEDIAN LIFE (HOURS)	STANDARD DEVIATION (HOURS)	NUMBER OF FAILURES
1	ZERO	250	140	1.1	26
2	ZERO	225	126	0.71	30
3	ZERO	200	733	0.951	28
4	ZERO	175	3390	0.764	19
5	ZERO	150	8895	0.523	1*

*SUPPLEMENTED BY 29 EXTRAPOLATED TIMES TO FAILURES.

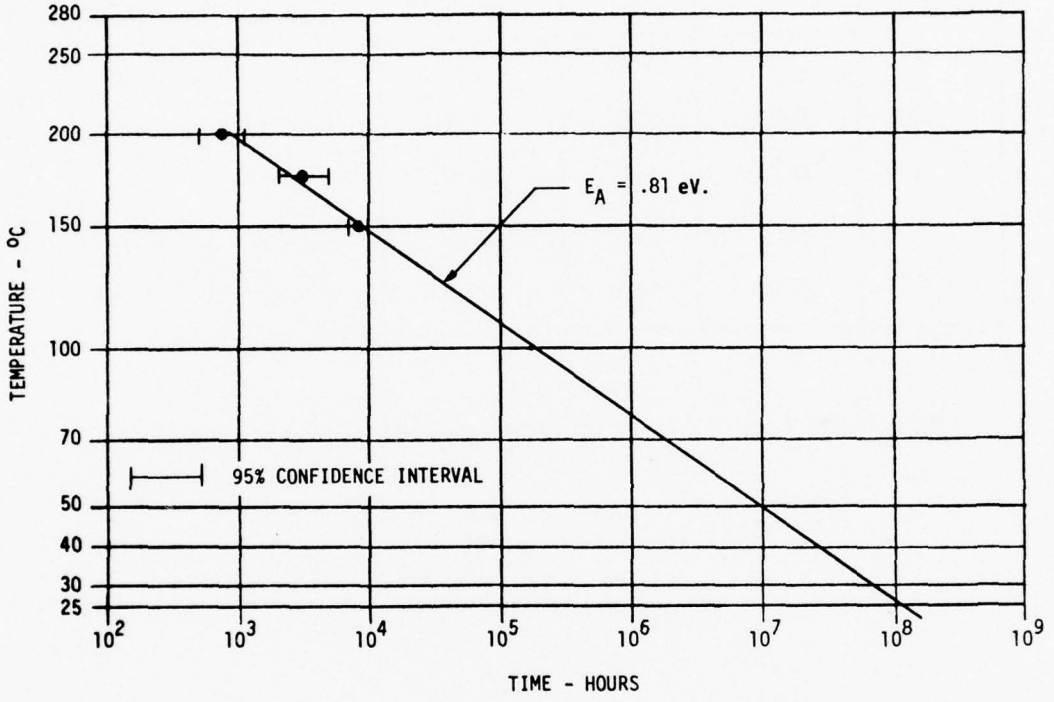


FIGURE H12. ARRHENIUS PLOT - P/N 772928 - NPN LOW POWER SWITCH

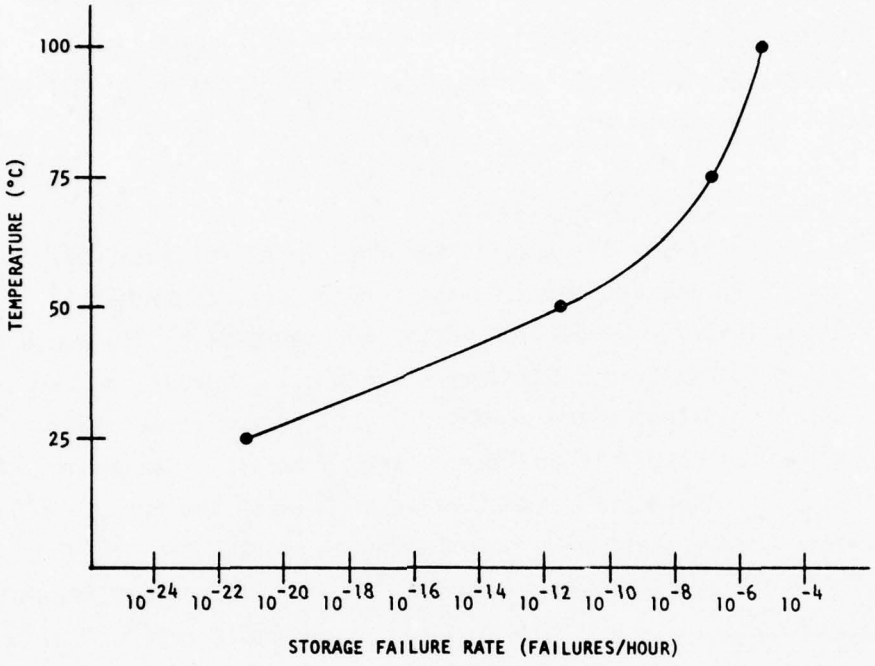


FIGURE H13. MAXIMUM INSTANTANEOUS FAILURE RATE, $\lambda(t)$, 20 YEAR INTERVAL - P/N 772928 - NPN LOW POWER SWITCH

The preliminary part drawing for P/N 772928 specified a storage temperature range of -65°C to +200°C and a maximum junction temperature of 200°C. This particular lot of parts is not capable of meeting these criteria. A high temperature lot sampling test would quickly reveal if the h_{FE1} degradation mechanism is included in parts processed for production. Figure H9 shows that after 100 hours of life testing at 200°C the average value of h_{FE1} for 30 parts had decreased to less than 50% of the initial value. Since the life tests did not reveal any discernible "freak" population, a 100% lot screening test for this particular failure mechanism would not be appropriate.

H9.0 CONCLUSIONS AND RECOMMENDATIONS

- This particular lot of parts is not capable of reliable performance at the specified storage and junction temperature requirements. A lot screening test for production parts (100 hours at 200°C) would quickly reveal if the failure mechanisms causing h_{FE1} degradation is present.
- Any electrical test which reverses biases or avalanches the emitter base junction will result in an improvement in the h_{FE1} parameter. Additionally, if there are conductive paths between the collector and emitter, a BV_{CBO} test will give the same result. Any lot sampling test evaluating h_{FE1} degradation mechanism should exclude measurement of BV_{EBO}, BV_{CBO}, I_{CBO}, and I_{EBO} to preclude possible reversal of the degradation mechanism.
- This device has a calculated $\lambda(t)_{MAX}$ of 5.662×10^{-6} failures per hour in the storage temperature range of interest.
- No "freak" population is evident.
- Additional lot testing is recommended to determine extent of lot to lot variability.

APPENDIX I

P/N 772929

PNP LOW POWER AMPLIFIER

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I1.0 PART DESCRIPTION

The PNP Low Power Amplifier, P/N 772929, is a beam lead transistor, type 2N2907, mounted in a three lead TO-18 package. The die was manufactured by Raytheon Company, Semiconductor Division. This test configuration is different from the SAM-D use configuration.

I2.0 CONSTRUCTION ANALYSIS

Table I1 summarizes the pertinent construction details of this device and Figures I1 and I2 provide a photograph of the external construction and a terminal diagram. Two photographs, one of the die mounted in the package and one of the die topography, are provided in Figure I3. Testing was not restricted below 300°C by the materials contained in this device.

The typical SAM-D configuration, Figure I4, has the beam lead die bonded to the metallization on a ceramic substrate.

I3.0 ELECTRICAL TEST CRITERIA

The electrical tests for this device are summarized in Table I2. The emitter-base breakdown voltage test was deleted following the initial test to avoid avalanching the emitter-base junction. Special testing indicated that avalanching this junction resulted in h_{FE1} degradation.

I4.0 BIAS CIRCUIT ANALYSIS

The three Figure I5 bias circuits were examined for current/voltage/temperature relationships. All of the bias circuits had a voltage on the collector and the base grounded. The emitters of bias circuits 1, 2, and 3 were open, grounded and -1.0 volt, respectively. With the collectors maintained at -60 volts, bias circuit 3, as shown in Figure I5, required less supply current than the other bias circuits at elevated temperatures and was, therefore, selected the candidate life test circuit. The maximum collector voltage would be -60 volts but the determination of a maximum ambient temperature was delayed until the completion of the step stress test. Current limiting resistors of 15K ohms were used to avoid catastrophic damage in the event of device failure.

TABLE I1. PART CONSTRUCTION DETAILS - P/N 772929 - PNP LOW POWER AMPLIFIER

A. IDENTIFICATION

1. Part Name: PNP Low Power Amplifier (2N2907)
2. Part Manufacturer: Raytheon Co., Semiconductor Division
3. Part Number: 772929
4. Date Code: 7527

B. PACKAGE

1. Type: 3-Lead, TO-18 (Drawing No. 757433)
2. Weight: 0.3i6 gram
3. Materials:
   a) Cap: Steel
   b) Header: Kovar, gold-plated
   c) Leads: Kovar, gold-plated
   d) Cap Seal: Weld
   e) Lead Seal: Glass

C. INTERNAL GEOMETRY

1. Interconnections: Beam leads bonded to gold-plated header

2. Die:
   a) Type: Silicon, planar (Beam Lead)
   b) Scribe Method: Etch
   c) Dimension: 0.0032 inch x 0.0032 inch
   d) Passivation: Silicon Nitride over Silicon Dioxide

3. Metallization Type: Gold/Titanium/Platinum

3.8X

FIGURE I1. EXTERNAL CONSTRUCTION - P/N 772929 - PNP LOW POWER AMPLIFIER

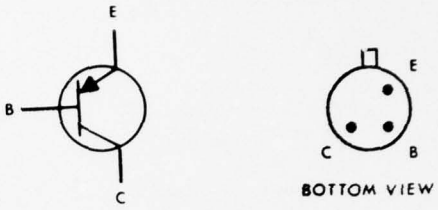
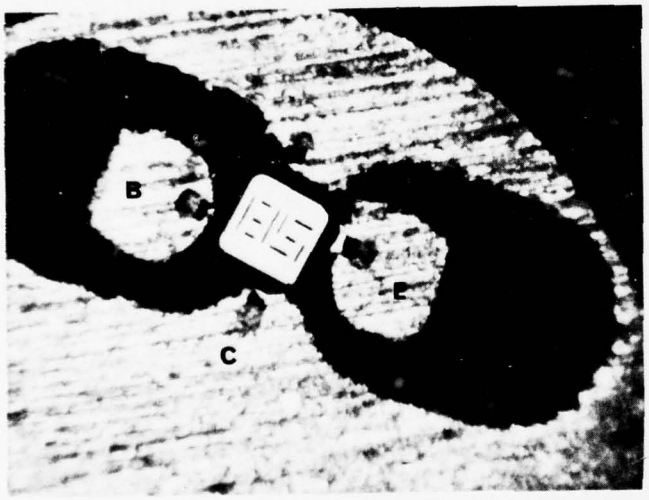
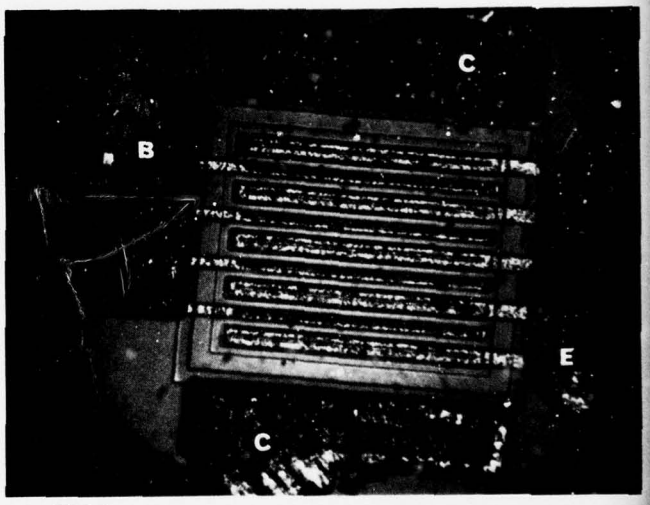


FIGURE I2. SYMBOL AND TERMINAL DIAGRAM - P/N 772929 - PNP LOW POWER AMPLIFIER



37X

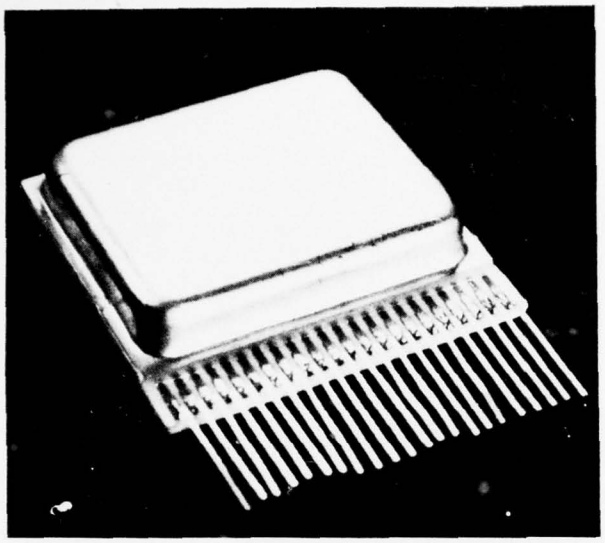
VIEW WITH LID REMOVED



132X

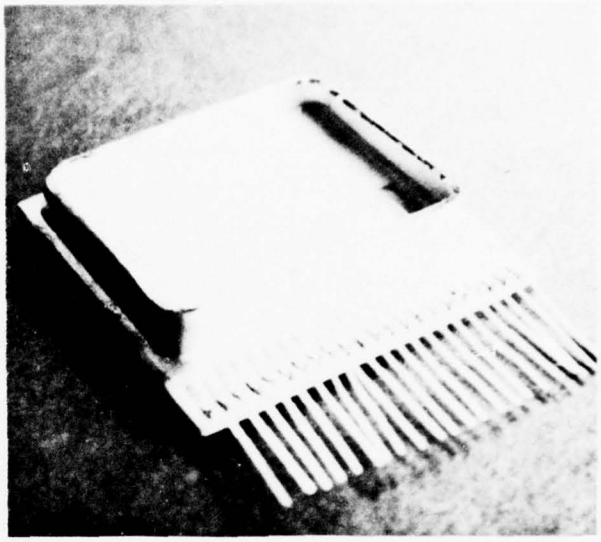
DIE TOPOGRAPHY

FIGURE I3. INTERNAL CONSTRUCTION DETAILS - P/N 772929 - PNP LOW POWER AMPLIFIER



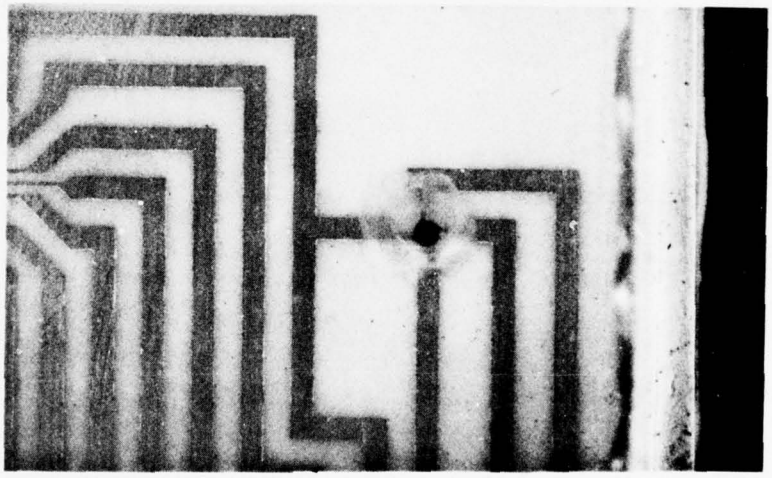
1.9X

EXTERNAL



1.9X

INTERNAL



7X

DIE MOUNTED IN SAM-D CONFIGURATION

FIGURE I4. TYPICAL SAM-D CONFIGURATION - P/N 773380 - PNP LOW POWER AMPLIFIER

TABLE I2. ELECTRICAL TEST CONDITIONS - P/N 772929 - PNP LOW POWER AMPLIFIER

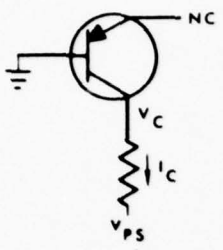
TEST NO.	SYMBOL	MIL-STD-750	CONDITIONS	T_A=+25°C		T_A=+150°C		UNITS
				MIN	MAX	MIN	MAX	
1	BV_{CBO}	3001 COND. D	I_C = 10μA	75	-	(3)	-	Vdc
2	BV_{EBO} (1)	3026 (2) COND. D	I_E = 10μA	5	-	(3)	-	Vdc
3	BV_{CEO}	3011 (2) COND. D	I_C = 10mA	75	-	(3)	-	Vdc
4	I_{CEX}	3041 COND. A	V_{CE} = 30V; V_{BE} = 0.5V	-	50	-	(3)	nA
5	I_{CBO}	3036 COND. D	V_{CB} = 50V	-	20	-	20	nA
6	$I_{B(OFF)}$	--	V_{CE} = 30V; V_{BE} = 0.5	-	50	-	(3)	nA
7	H_{FE1}	3076 (2)	V_{CE} = 10V; I_C = 1.0mA	75	-	(3)	-	-
8	H_{FE2}	3076 (2)	V_{CE} = 10V; I_C = 1.0mA	100	-	(3)	-	-
9	H_{FE3}	3076 (2)	V_{CE} = 10V; I_C = 10mA	100	-	(3)	-	-
10	I_{EBO}	3061 (2) COND. D	V_{EB} = 3.0V	(3)	-	(3)	-	nA

(1) THIS TEST WAS ELIMINATED AFTER THE INITIAL TEST.

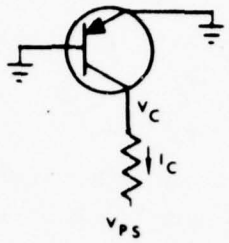
(2) EQUIVALENT TEST CONFIGURATION

(3) LIMITS NOT SPECIFIED BY PART DRAWING - MEASUREMENT MADE FOR INFORMATION ONLY.

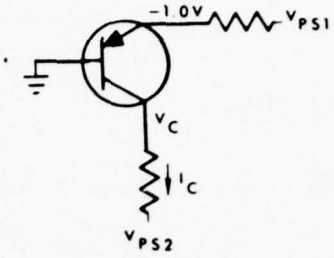
INITIAL AND FINAL TEST CONDUCTED AT +25°C AND +150°C. INTERIM TEST CONDUCTED AT +25°C.



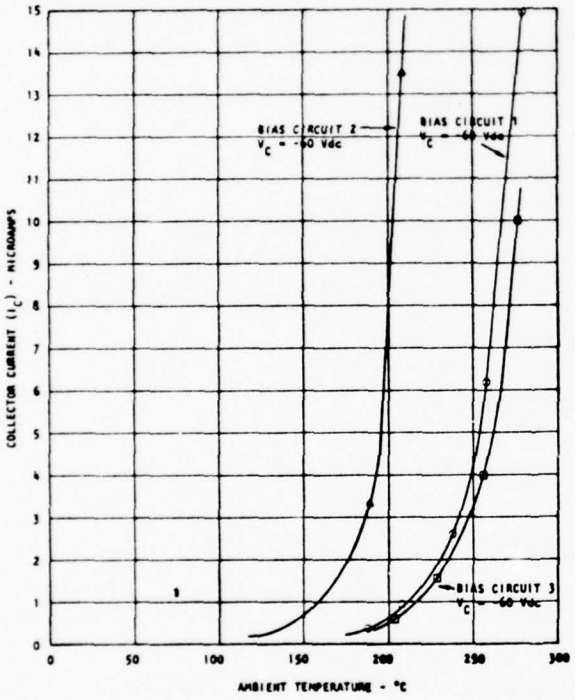
BIAS CIRCUIT 1



BIAS CIRCUIT 2



BIAS CIRCUIT 3



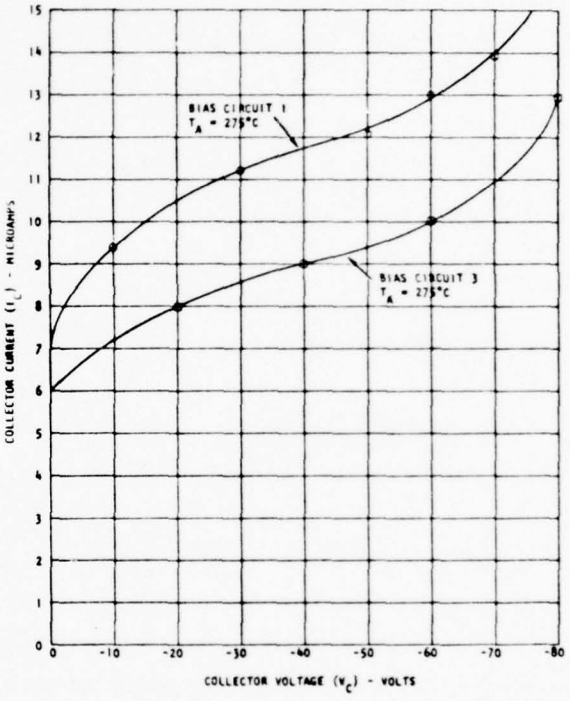


FIGURE I5. BIAS CIRCUIT EVALUATION - P/N 772929 - PNP LOW POWER AMPLIFIER

I5.0 STEP STRESS TEST RESULTS

A step stress test was performed on twenty devices configured in bias circuit 3 with -60 volts on the collectors. Four steps of sixteen hours at 25°C intervals, starting at 200°C and concluding at 275°C, were accomplished with only one failure, after the last step. Figure I6 contains a summary of the step stress test results.

Bias circuit 3 and -60 volts were considered acceptable conditions for the life test. The step stress results indicated that an ambient temperature of 275°C would be acceptable, but the bias circuit evaluation demonstrated that the collector current was relatively high and, more importantly, would increase greatly with small excursions of oven temperature. Therefore, it was decided that one cell at maximum voltage would be operated at 275°C and three cells operated at 250°C with collector voltages of -60 volts, -30 volts and 0 volt (storage cell). The fifth cell would be a maximum voltage cell at 225°C ambient temperature.

I6.0 LIFE TEST CONDITIONS AND RESULTS

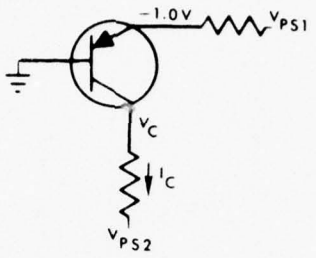
The life test conditions, as discussed in the previous paragraph, are tabulated in Figure I6. The 4000 hour life test was completed, producing eleven failures; five in Cell 1, two in Cell 2, zero in Cell 3, three in Cell 4 and 1 in Cell 5. Table I3 is a summary of the life test results.

I7.0 FAILURE ANALYSIS

A summary of the failure analysis results is provided in Table I4.

ICBO Failures - Nine parts exhibited excessive I_{CBO} during life test. The values of I_{CBO} ranged from 21 nanoamperes to 26 microamperes. Three of these parts also exhibited excessive I_{CBO}. Curve tracer tests of failed parts disclosed a channeled reverse collector-base characteristic, as illustrated in Figure I7, which is usually indicative of surface instability. However, the parts did not recover when baked and several parts exhibited erratic or intermittent leakage during the life test or during curve tracer testing, all of which indicated that the leakage was mechanical in nature rather than surface related. After delidding, the collector-base junction would exhibit a completely normal characteristic when the beam-lead die was removed from the header or if the die simply was nudged with

STEP STRESS AND LIFE TEST CIRCUIT



STEP STRESS TEST - FAILURE SUMMARY (20 DEVICES)

AMBIENT TEMP (°C)	V_C (V)	CUMULATIVE FAILURES
200	-60	0
225	-60	0
250	-60	0
275	-60	1

LIFE TEST CONDITIONS

TEST CELL NUMBER	T_A AMBIENT TEMPERATURE (°C)	V_C COLLECTOR-BASE VOLTAGE (VOLTS)	I_C COLLECTOR CURRENT (MICROAMPS)	P_d POWER DISSIPATION (MICROWATTS)	T_J JUNCTION TEMPERATURE (°C)
1	275	-60	9.2	550	275
2	250	-60	3.6	220	250
3	250	-30	3.0	90	250
4	250	0	0	0	250
5	225	-60	1.5	90	225

FIGURE I6. STEP STRESS RESULTS AND LIFE TEST CONDITIONS - P/N 772929 - PNP LOW POWER AMPLIFIER

TABLE I3. LIFE TEST SUMMARY - P/N 772929 - PNP LOW POWER AMPLIFIER

TEST CELL DESCRIPTION				CUMULATIVE FAILURES AT HOURS OF TEST										
CELL NO	APPLIED BIAS	AMBIENT TEMP	QUANTITY	4	8	16	32	64	128	256	512	1000	2500	4000
1	60 VDC	275°C	30	1	1	1	1	1	1	1	3	3	4	5*
2	60 VDC	250°C	30	0	0	0	0	1	1	1	1	1	1	2*
3	30 VDC	250°C	30	0	0	0	0	0	0	0	0	0	0	0*
4	0 VDC	250°C	30	0	1	1	1	1	1	1	1	3	3	3*
5	60 VDC	225°C	30	1	1	1	1	1	1	1	1	1	1	1*

* TEST TERMINATED

TABLE I4. FAILURE ANALYSIS SUMMARY - P/N 772929 - PNP LOW POWER AMPLIFIER

A. FAILED PARAMETERS OR SYMPTOM B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TIME OF FAILURE (HOURS)				
	275°C	250°C			225°C
	60V	60V	30V	0V	60V
	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5
A. ICBO AND ICEX B. DIE-TO-HEADER LEAKAGE C. HEADER BURRS D. PROCESSING ERROR	1@4 2@512 1@4000	1@64		1@8 2@1000	1@4
A. h_{FE2} B. INITIALLY MARGINAL C. NOT DETERMINED D. PROCESS INDUCED DEFICIENCY		1@4000			
A. h_{FE1} B. DEGRADED B-E JUNCTION C. BULK AND SURFACE RELATED D. NOT DETERMINED	1@2500				
TOTAL NUMBER OF FAILED PARTS	5	2	0	3	1

a probe. Detailed examinations of the die and the header disclosed only one probable explanation for the intermittent leakage. All nine parts contained metal burrs around the header cutout and the emitter and the base posts, as illustrated in Figure I8. Loose burrs or burrs protruding from the header (the collector terminal) or the base post probably bridged the collector-base metallizations on the die, causing the leakage. Scratch marks on the headers indicated that the headers had been lapped to grind the emitter and base posts flush with the header. The burrs probably were generated as a result of this lapping operation.

h_{FE} Failures - One part failed due to low h_{FE2} (97) at the 4000 hour test point in Cell 2. The low h_{FE2} was not bake reversible and the part exhibited an abnormally low and marginal value of h_{FE2} (117) upon receipt, which indicated that the part probably contained a bulk deficiency introduced during manufacturing. Routine examinations of the die did not disclose the deficiency, thus the exact failure mechanism was not established.

One part failed due to low h_{FE1} (56) at 2500 hours in Cell 1. Curve tracer tests established that the low h_{FE1} was caused by degradation of the base-emitter junction. After an unpowered bake h_{FE1} improved to 85, which is within specification but only 47% of the as-received value (182). This indicated that the failure mechanism was probably both surface and bulk related. Because this was a single, isolated failure of this type, the part was not investigated further.

I8.0 DATA CORRELATION

The Table I4 Failure Analysis Summary attributes nine of the eleven test failures to burrs on the header, a condition which is peculiar to the test configuration and not applicable to SAM-D usage. These nine failures were discounted for evaluation purposes. Of the two remaining test failures, the h_{FE1} degradation was attributed to a combination of bulk and surface mechanisms, and the h_{FE2} failure was probably the result of an initially marginal part combined with a process induced deficiency.

Since the two h_{FE} failures are insufficient for failure distribution analysis, parameter trends were investigated for possible extrapolation of times to failure. Figure I9 shows the h_{FE1} degradation pattern for three of the test cells. The

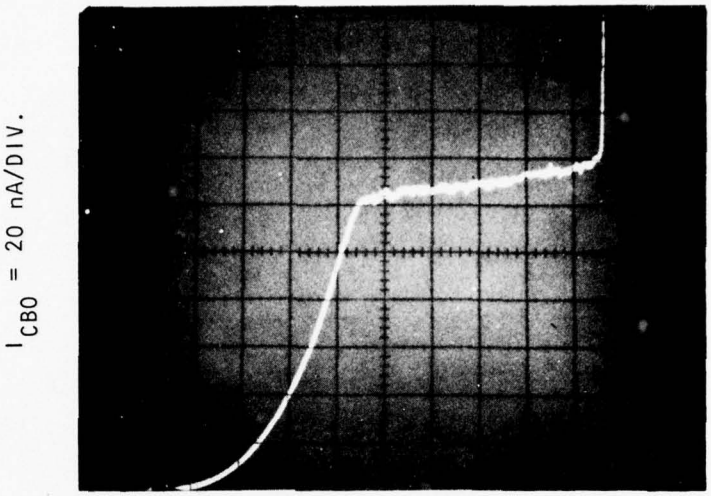
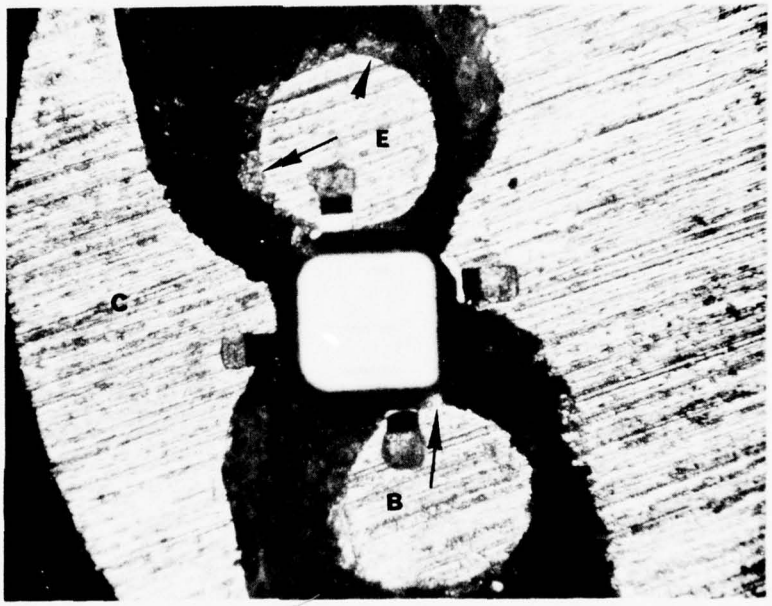


FIGURE I7. EXAMPLE OF THE REVERSE COLLECTOR-BASE DEGRADATION DISPLAYED BY THE I_{CBO} FAILURES - P/N 772929 - PNP LOW POWER AMPLIFIER



60X

FIGURE I8. I_{CBO} FAILURE AFTER DELIDDING SHOWING THE METAL BURRS (ARROWS) ON THE HEADER AND THE POSTS - P/N 772929 - PNP LOW POWER AMPLIFIER

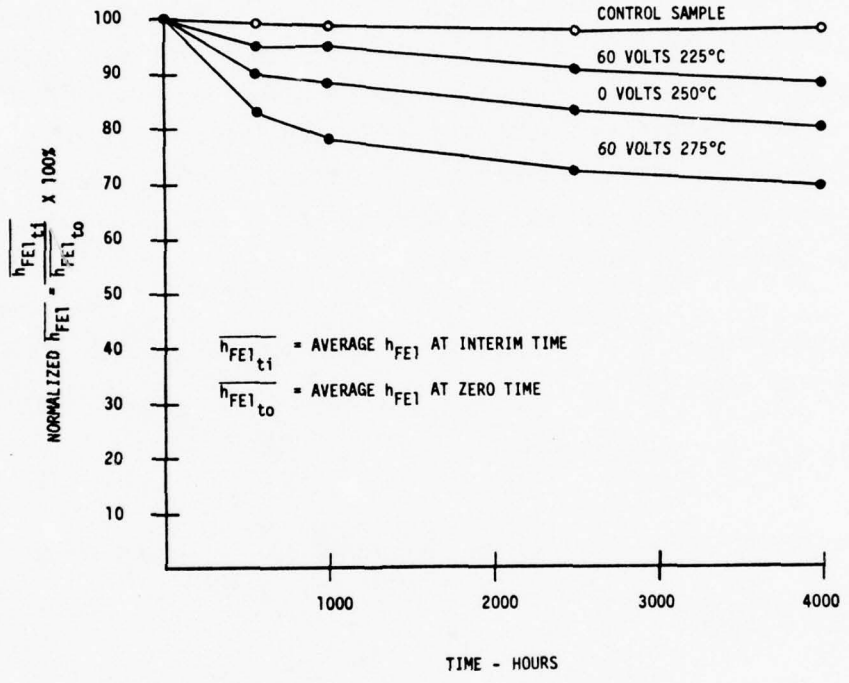


FIGURE I9. NORMALIZED h_{FE1} TIME/TEMPERATURE DEGRADATION - P/N 772929 - PNP LOW POWER AMPLIFIER

zero volt 250°C data would indicate the h_{FE1} degradation mechanism is primarily influenced by test temperature and not test voltage. This conclusion is corroborated by two biased test cells (60 volts and 30 volts) at 250°C. Each experienced h_{FE1} degradation rates very similar to the zero volt cell.

Two degradation models, linear time and log time, were investigated and both were found to adequately describe the data with a high degree of correlation. The linear degradation model was selected because it provided both the best data correlation and the most conservative estimate of failure times. The cumulative failure distribution for each test cell, using extrapolated times to failure, is shown in Figures I10 and I11. All show a good fit for the lognormal failure distribution. No "freak," or infant mortality, population is evident. The pertinent distribution data is summarized in Table I5. Since the data of the three 250°C test cells suggest that temperature may be the predominant accelerator, their data was pooled for analysis purposes.

The Figure I12 Arrhenius plot reflects Cells 1, 5 and the "pooled" Cells 2, 3 and 4. The Arrhenius equation is:

$$\ln t_{50\%} = 0.28054 + \frac{0.43}{kT}$$

Instantaneous failure rates were calculated using the following relationship:

$$\lambda(t) = \frac{f(t)}{R(t)}$$

$$\lambda(t) = \frac{\frac{1}{t} \exp - \frac{\left[\ln t - 0.28054 - \frac{0.43}{kT}\right]^2}{2(0.34)^2}}{\int_t^\infty \frac{1}{t'} \left[\exp - \frac{\left[\ln t' - 0.28054 - \frac{0.43}{kT}\right]^2}{2(0.34)^2}\right] dt'}$$

The maximum calculated $\lambda(t)$ over the storage temperature range (25°C to 100°C) for a 20-year period is 2.9×10^{-10} failures per hour. This conservative estimate reflects a good storage reliability potential for this transistor.

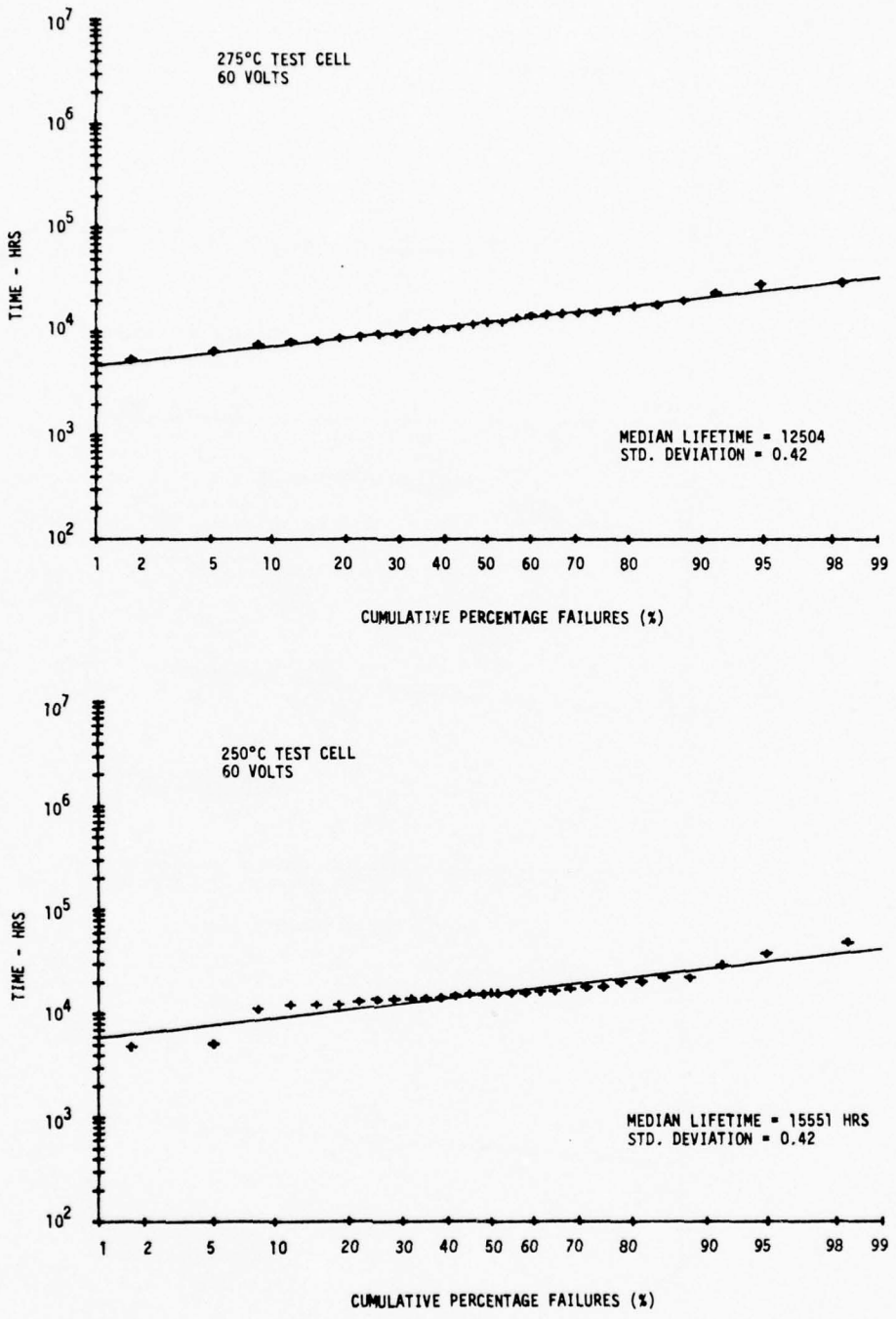


FIGURE I10. CUMULATIVE FAILURE DISTRIBUTIONS FOR CELL 1 (TOP) AND CELL 2 (BOTTOM) - P/N 772929 - PNP LOW POWER AMPLIFIER

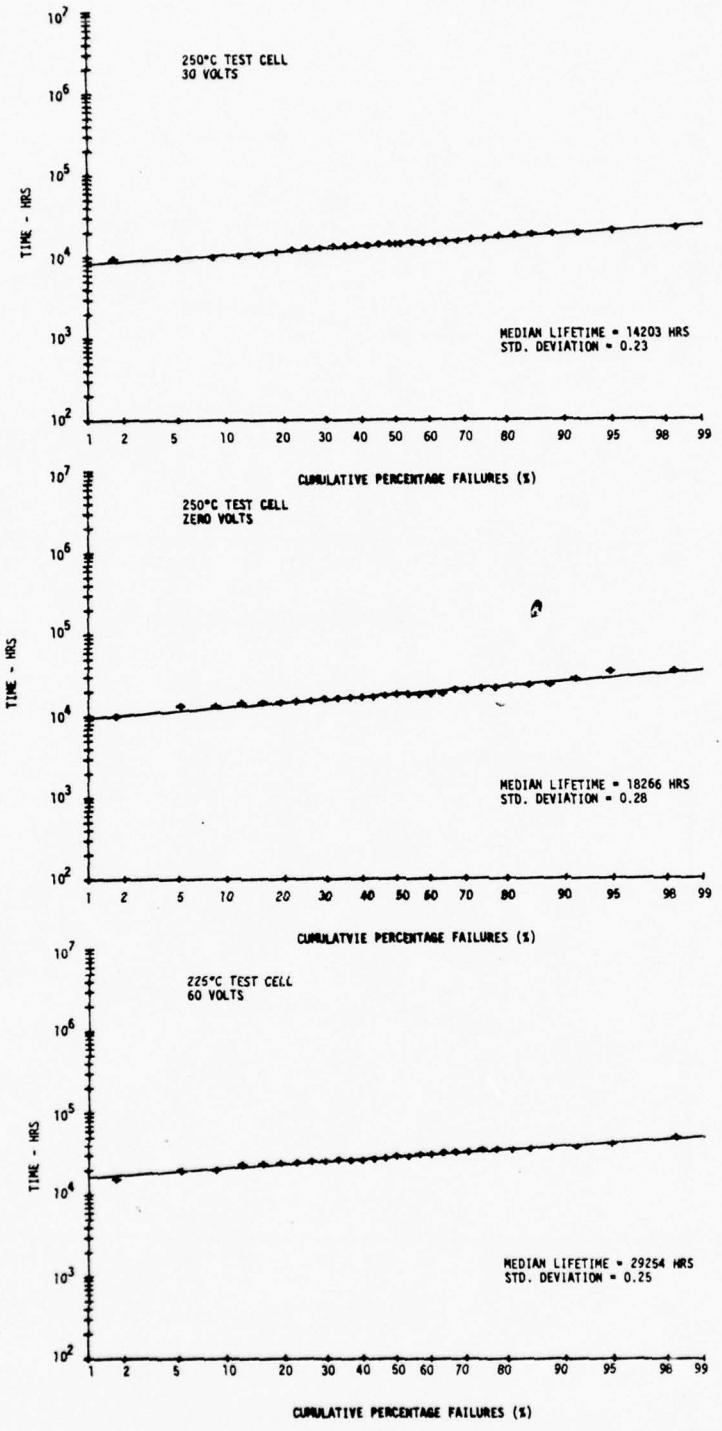


FIGURE III. CUMULATIVE FAILURE DISTRIBUTIONS FOR CELL 3 (TOP), CELL 4 (MIDDLE) AND CELL 5 (BOTTOM) - P/N 772929 - PNP LOW POWER AMPLIFIER

TABLE I5. SUMMARY DATA - P/N 772929 - PNP LOW POWER AMPLIFIER

CELL NO.	TEST VOLTAGE (VOLTS)	NUMBER OF FAILURES [1]	T_A (°C)	T_J (°C)	MEDIAN LIFE (HOURS)	STANDARD DEVIATION (HOURS)
1	-60	29	275	275	12,504	0.42
2	-60	30	250	250	15,551	0.42
3	-30	30	250	250	14,203	0.23
4	ZERO	29	250	250	18,266	0.28
5	-60	29	225	225	29,254	0.25
(2, 3, 4, Pooled)	--	89	250	250	16,007	0.32

[1] Except for one Cell 1 test failure, all other failures are extrapolated.

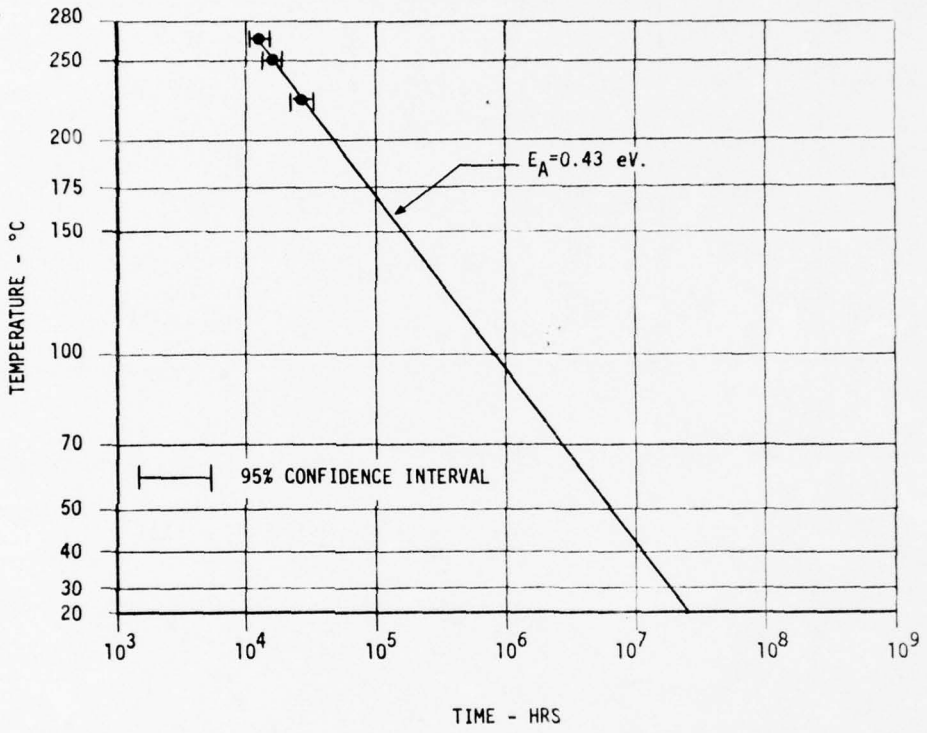


FIGURE I12. ARRHENIUS PLOT - P/N 772929 - NPN LOW POWER AMPLIFIER

The preliminary part specification, P/N 772929, specifies a maximum storage or junction temperature of 200°C. The Figure I12 Arrhenius plot shows the projected median median life to be less than a 20-year storage time (175,320 hours) at temperatures above 150°C, suggesting a reduction in the specified maximum allowable storage and junction temperature to 125°C.

I9.0 CONCLUSIONS AND RECOMMENDATIONS

- This transistor will experience h_{FE} degradation as a function of time and temperature. However, the rate displayed by this particular lot of parts results in degradation which would not be significant in a 20-year time period at temperatures up to 100°C. If this is typical performance, this part has a good storage reliability potential.
- A short term high temperature sampling test (225°C, 100 hours) of production lots would provide a good monitor for the integrity of the part. More than 10% h_{FE1} degradation would indicate atypical performance.
- The preliminary part specification identifies the maximum storage and junction temperature as 200°C. This may be too high and should be investigated.

STORAGE RELIABILITY
OF MISSILE MATERIEL

REPORT MDC E1601
29 APRIL 1977

APPENDIX J

P/N 773052

NPN LOW POWER AMPLIFIER

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J1.0 PART DESCRIPTION

This NPN Low Power Amplifier, P/N 773052, is a conventional chip and wire transistor, type 2N5652, manufactured by KMC Semiconductor Corporation, and packaged in a four lead TO-72 can for the test program. The test configuration is different from the SAM-D use configuration.

J2.0 CONSTRUCTION ANALYSIS

The pertinent physical details of the test configuration are summarized in Table J1. Figures J1 and J2 provide an external photograph and a functional schematic of the device. A view with the lid removed and the die topography are provided in Figure J3. The device contains no materials that limited testing below 300°C.

The typical SAM-D configuration is pictured in Figure J4. It consists of the die mounted in a "pill box" package that is mounted to a ceramic printed circuit board.

J3.0 ELECTRICAL TEST CRITERIA

The electrical test conditions are summarized in Table J2. A BV_{EBO} test was included for information purposes. Performance of this test did not result in any part degradation as evidenced by the stability of the control sample.

J4.0 BIAS CIRCUIT ANALYSIS

Four bias circuits are illustrated in Figure J5 with collector current versus ambient temperature plots for each. The collector currents of bias circuits 1 and 2 are substantially lower than those of bias circuits 3 and 4 at elevated ambient temperatures. Bias circuit 2 was selected the candidate life test bias circuit because it required fewer external parts and power supplies. The maximum ambient temperature and collector-base voltage tentatively selected for the accelerated life test were 270°C and 20 VDC. A 12K ohm current limiting resistor was used to preclude catastrophic damage in the event of device failure.

J5.0 STEP STRESS TEST RESULTS

Twenty devices in bias circuit 2, V_C = 20 VDC, were subjected to a step stress test consisting of five 16 hour steps at 25°C intervals starting at 175°C and concluding

TABLE J1. PART CONSTRUCTION DETAILS - P/N 773052 - NPN LOW POWER AMPLIFIER

A. IDENTIFICATION

1. Part Name: NPN Low Power Amplifier (2N5652)
2. Part Manufacturer: KMC Semiconductor Corp.
3. Part Number: 773052
4. Date Code: 264

B. PACKAGE

1. Type: 4-Lead, TO-72
2. Weight: 0.341 gram
3. Material:
   a) Cap: Steel
   b) Header: Kovar, gold-plated
   c) Leads: Kovar, gold-plated
   d) Cap Seal: Weld
   e) Lead Seal: Glass

C. INTERNAL GEOMETRY

1. Interconnections:
   a) Type: Aluminum Wire
   b) Diameter: 0.007 inch
   c) Bonds:
      1) Aluminum-aluminum ultrasonic at the die
      2) Aluminum-gold ultrasonic at the post

2. Die:
   a) Type: Silicon, Planar
   b) Scribe Method: Mechanical
   c) Dimensions: 0.015 inch x 0.015 inch
   d) Attach Method: Gold Eutectic
   e) Passivation: Silicon Dioxide

3. Metallization Type: Aluminum

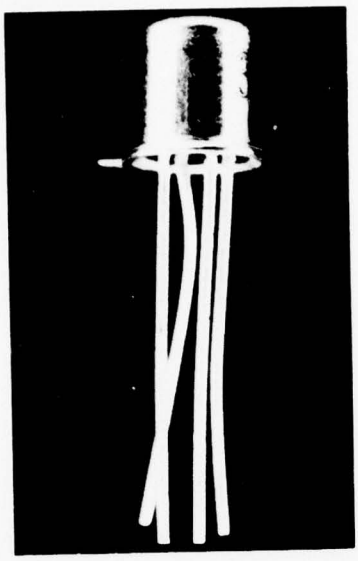

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FIGURE J1. EXTERNAL CONSTRUCTION - P/N 773052 - NPN LOW POWER AMPLIFIER

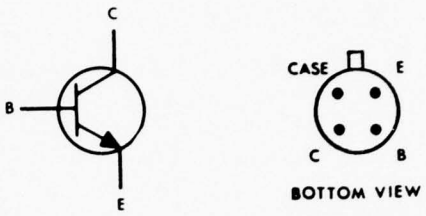
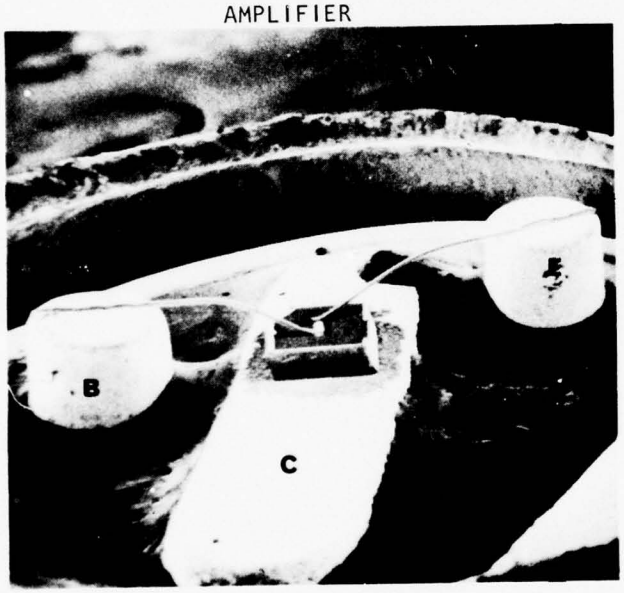


FIGURE J2. SYMBOL AND TERMINAL DIAGRAM - P/N 773052 - NPN LOW POWER AMPLIFIER



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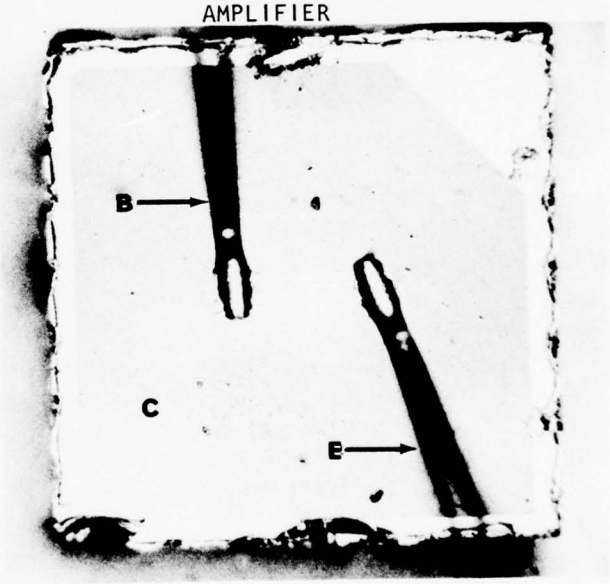
VIEW WITH LID REMOVED



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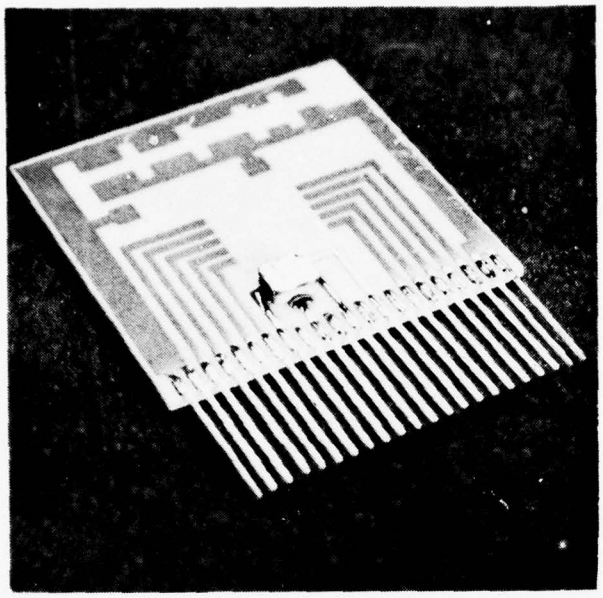
DIE TOPOGRAPHY

FIGURE J3. INTERNAL CONSTRUCTION DETAILS - P/N 773052 - NPN LOW POWER AMPLIFIER



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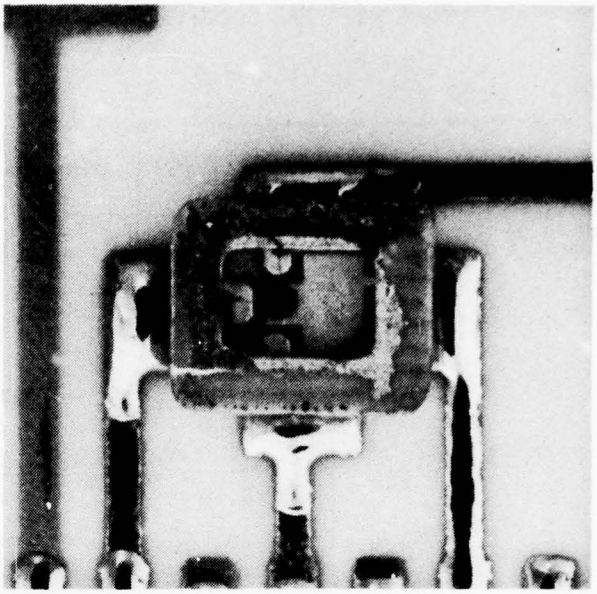
EXTERNAL



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INTERNAL

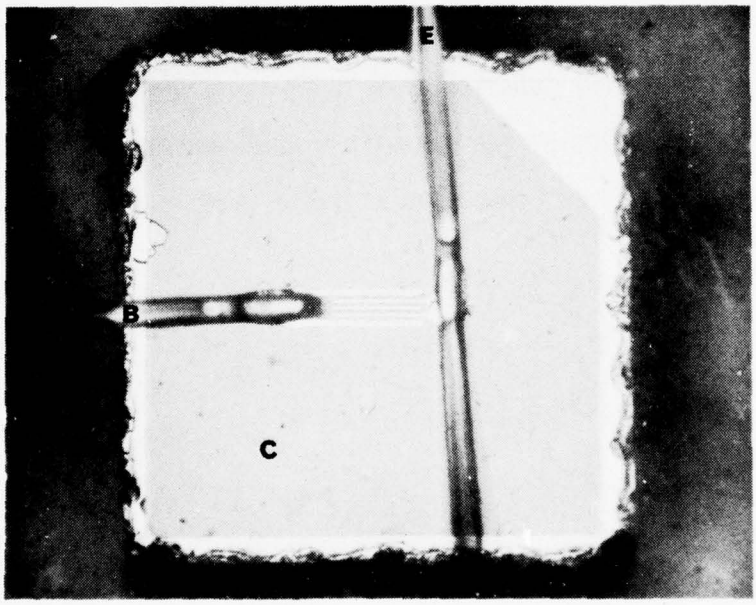

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FIGURE J4. TYPICAL SAM-D CONFIGURATION - P/N 773340 - PNP LOW POWER AMPLIFIER

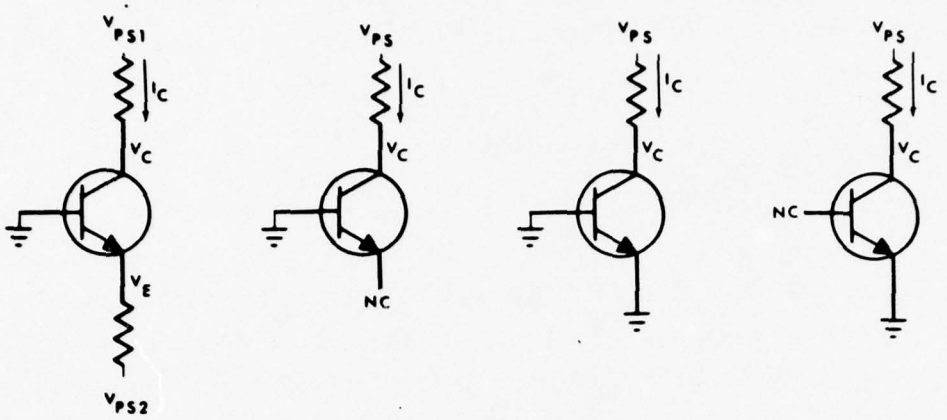
TABLE J2. ELECTRICAL TEST CONDITIONS - P/N 773052 - NPN LOW POWER AMPLIFIER

TEST NO.	SYMBOL	MIL-STD-750	CONDITIONS	T_A=+25°C		T_A=+100°C		T_A=-55°C		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
1	BV_{CBO}	3001 COND. D	I_C = 20μA	20	-	20	-	(2)	-	Vdc
2	I_{CBO}	3036 COND. D	V_{CB} = 6.0V	-	10	-	10	-	2	nA
3	BV_{EBO}	3026 COND. D (1)	I_E = 20μA	3	-	(2)	-	(2)	-	Vdc
4	I_{EBO}	3061 COND. D (1)	V_{EB} = 3.0V	(2)	-	(2)	-	(2)	-	μA
5	H_{FE1}	3076 (1)	V_{CE} = 6.0V; I_C = 5.0mA	40	200	(2)	(2)	25	-	-
6	H_{FE2}	3076 (1)	V_{CE} = 6.0V; I_C = 20mA	40	200	(2)	(2)	(2)	(2)	-
7	I_{CEO}	3041	V_{CE} = 15.0V	(2)	-	(2)	-	(2)	-	nA

(1) EQUIVALENT TEST CONFIGURATION

(2) LIMITS NOT SPECIFIED BY PART DRAWING - MEASUREMENT MADE FOR INFORMATION ONLY.

INITIAL AND FINAL TEST CONDUCTED AT +25°C, +100°C AND -55°C. INTERIM TEST CONDUCTED AT +25°C.



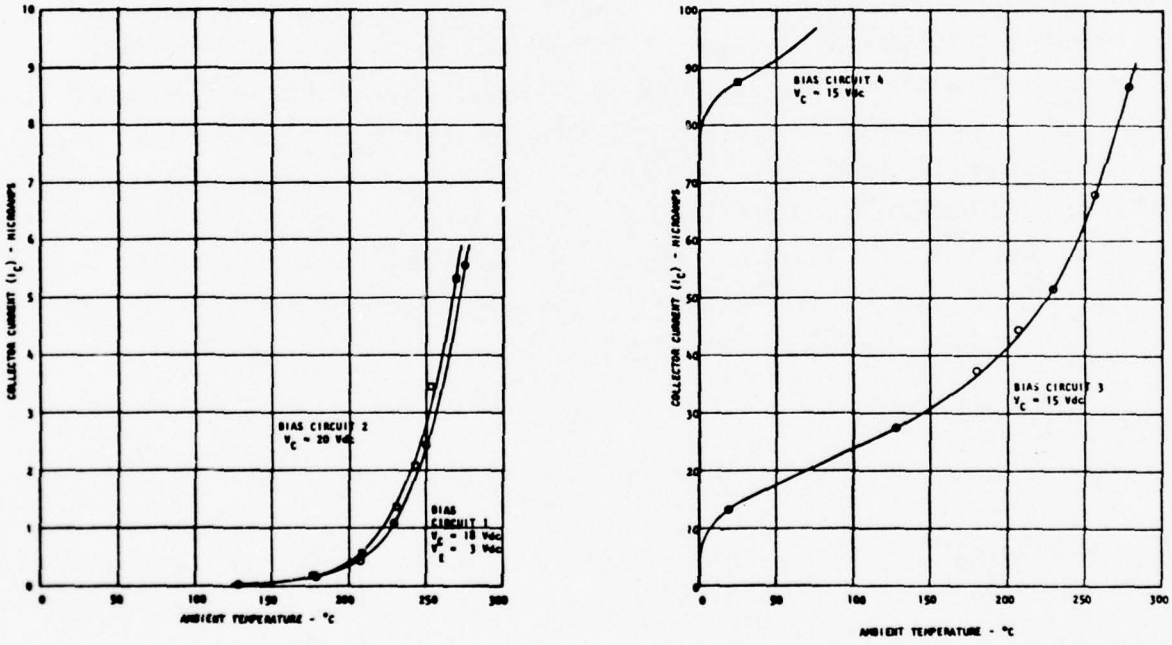


FIGURE J5. BIAS CIRCUIT EVALUATION - P/N 773052 - NPN LOW POWER AMPLIFIER

at 275°C. Ten h_{FE1} degradation failures were generated. The step stress test is summarized in Figure J6 and the failures are discussed in Paragraph J7.0. The bias circuit and life test condition limits were considered acceptable for the accelerated life test program.

J6.0 LIFE TEST CONDITIONS AND RESULTS

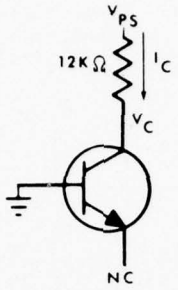
The life test conditions for each cell are summarized in Figure J6. The maximum temperature was initially selected as 270°C. However, the oven was erroneously set to 263°C as the test started; this temperature was acceptable and no change was made. Since this was a part selected for a voltage sensitivity analysis, Cells 1 through 4 were at the same maximum temperature with various applied bias levels, including zero. As shown in the Table J3 summary, all 5 test cells experienced 50% failures within 128 hours. However, the life tests were continued beyond the 50% failure point to provide additional data. Cells 1 and 2 were terminated after 32 hours with over 80% failures. Cells 3, 4 and 5 were halted after 256 hours (80% failures), 1000 hours (83% failures), and 4000 hours (87% failures), respectively. Early in the life tests, the occurrence of failures appeared to be demonstrating a voltage sensitivity. When Cells 1 and 2 were terminated, the opportunity arose to initiate two more cells (cells 6 and 7) to obtain additional information. Cells 6 and 7 were added to the life test program and proceeded to 2500 hours (67% failures) and 8000 hours (43% failures), respectively. Because of the rapid h_{FE} degradation, additional electrical tests were accomplished at 0.5, 1.0 and 2.0 hours. Cell 7 was extended to 8000 hours and provided additional useful failure data.

J7.0 FAILURE ANALYSIS

Table J4 is a summary of the failure analysis results.

Surface Instability Failures - One hundred and fifty-four (154) life test parts and 10 step stress parts failed because h_{FE1} had decreased to less than the specified minimum limit of 40. Failure of h_{FE1} was often accompanied by failure of h_{FE2}, but no other parameter was out of tolerance or showed any significant shift. Unpowered bakes of failed parts established that two mechanisms, one reversible and one nonreversible, were responsible for the gain decrease. In general, the early failures in the powered cells were due to the reversible mechanism and all

STEP STRESS AND LIFE TEST CIRCUIT



STEP STRESS TEST - FAILURE SUMMARY (20 DEVICES)

AMBIENT TEMP (°C)	V_C (V)	CUMULATIVE FAILURES
175	20	4
200	20	4
225	20	5
250	20	7
275	20	10

LIFE TEST CONDITIONS

TEST CELL NUMBER	T_A AMBIENT TEMPERATURE (°C)	V_C COLLECTOR-BASE VOLTAGE (VOLTS)	I_C COLLECTOR CURRENT (MICROAMPS)	P_d POWER DISSIPATION (MICROWATTS)	T_J JUNCTION TEMPERATURE (°C)
1	263	20	4.6	92	263
2	263	13	3.4	44	263
3	253	6	1.6	10	263
4	263	0	0	0	263
5	225	20	1.1	22	225
6	225	6	0.2	1	225
7	225	0	0	0	225

FIGURE J6. STEP STRESS RESULTS AND LIFE TEST CONDITIONS - P/N 773052 - NPN LOW POWER AMPLIFIER

TABLE J3. LIFE TEST SUMMARY - P/N 773052 - NPN LOW POWER AMPLIFIER

TEST CELL DESCRIPTION				CUMULATIVE FAILURES AT HOURS OF TEST															
CELL NO.	APPLIED BIAS	AMBIENT TEMP.	QTY	.5	1	2	4	8	16	32	64	128	256	512	1000	2500	4000	6000	8000
1	20VDC	263°C	30	--	15	16	17	22	24	24*									
2	13VDC	263°C	30	--	8	8	10	26	27	27*									
3	6VDC	263°C	30	--	8	9	11	16	17	17	17	20	24*						
4	0VDC	263°C	30	--	3	5	5	7	8	9	9	12	18	21	25*				
5	20VDC	225°C	30	--	8	8	8	8	9	9	10	15	15	17	18	23	26*		
6	6VDC	225°C	30	5	5	5	5	5	5	5	7	10	11	11	11	20*			
7	0VDC	225°C	30	1	1	1	1	1	1	1	1	2	2	3	4	7	8	10	13*

*Test Terminated

TABLE J4. FAILURE ANALYSIS SUMMARY - P/N 773052 - NPN LOW POWER AMPLIFIER

	A. FAILURE SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. FAILURE CAUSE	QUANTITY OF FAILURES AND TIME OF FAILURE (HOURS) BY TEST CELL							
		263°C				225°C			
		20V	13V	6V	0V	20V	6V	0V	STEP STRESS
		CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7	
SURFACE INSTABILITY FAILURES	A. LOW h_{FE} B. DEGRADED E-B JUNCTION C. MOBILE ION DRIFT D. CONTAMINATION IN THE PASSIVATION AND C-E PIPE	1@1	2@1 1@4 1@8	6@1		7@1	3@0.5		3@175°C STEP 2@275°C STEP
	A. LOW h_{FE} B. DEGRADED E-B JUNCTION C. INCREASE IN SURFACE STATE DENSITY D. PASSIVATION DESIGN/PROCESSING	5@1 1@2 1@4 5@8 2@6	6@1 1@4 1508 1@16	2@1 1@2 1@4 5@8 1@16 3@128 4@256	3@1 1@2 2@8 1@32 3@128 6@256 3@512 4@1000	1@1 1@16 1@64 5@128 1@512 1@1000 5@2500 3@4000	2@0.5 2@64 3@128 9@2500	1@0.5 1@128 1@512 1@1000 3@2500 1@4000 2@6000 3@8000	1@175°C STEP 1@225°C STEP 2@250°C STEP 1@275°C STEP
BULK AND MECHANICAL FAILURES	A. h_{FE} CATASTROPHIC B. OPEN COLLECTOR C. LOOSE DIE D. INSUFFICIENT DIE BOND EUTECTIC					1@512			
	A. LOW h_{FE} AND BREAKDOWN VOLTAGES B. DEGRADED JUNCTIONS C. POORLY DEFINED DIFFUSIONS D. PHOTOLITH DEFECTS				1@2		1@256		
	A. LOW BV_{CBO} B. DEGRADED C-B JUNCTION C. INITIALLY MARGINAL D. PROCESS-INDUCED DEFECTS			1@4					
TEST ERROR	A. LOW h_{FE} AND BV_{EBO} B. SHORTED E-B JUNCTION C. ELECTRICAL OVERSTRESS D. TESTER TRANSIENT				1@16				
	TOTAL NUMBER OF FAILED PARTS	24	27	24	25	26	20	13	10

other failures were due to the nonreversible mechanism or a combination of both mechanisms. Examples of typical bake results are presented in Tables J5 and J6. If h_{FE1} recovered to the prestress value, the part was classified as reversible. If h_{FE1} did not improve or did not recover sufficiently, the part was classified as nonreversible.

Analysis of nonreversible failures established that the low h_{FE1} was caused by degradation of the emitter-base junction. Figure J7 illustrates the degradation displayed by the emitters of two failed transistors. Trace 1 is the forward base-emitter I-V characteristics of an unstressed transistor. All normal, unstressed transistors exhibit this V_{BE} characteristic, regardless of their value of h_{FE1}. Trace 2 is the V_{BE} characteristic of a transistor whose h_{FE1} had decreased from 45 (prestress) to 20 during life test. Trace 3 is the V_{BE} characteristic of a transistor whose h_{FE1} had decreased from 63 to 14 during life test. Because this transistor contains "washed" emitters, it was suspected that the degradation involved "softening" of the emitter junction due to aluminum migration and penetration of the junction. However, optical and SEM examinations of unetched and etched emitters and cross sections of emitters disclosed no evidence of lateral or vertical aluminum penetration. Furthermore, many failed parts were left on test and h_{FE1} of these parts eventually saturated at low, but non-catastrophic, values. If aluminum penetration was occurring, the emitter junction should have eventually shorted. Therefore, the degradation was attributed to a surface related mechanism rather than any bulk phenomenon. Because the instability was not bake reversible, the degradation probably was due to an increase in the surface state density at the Si/SiO_2 interface. Surface states in the vicinity of the emitter junction generate carrier recombination that reduces the gain of the transistor. Certain thermal oxidation techniques (such as steam growth) and processing steps can result in an initially low surface state density that can increase if the oxide is subsequently heated in a dry atmosphere.

Analysis of the bake reversible failures established that the low h_{FE1} of these parts was also due to degradation of the emitter-base junction. The transistors displayed a degraded forward base-emitter characteristic prior to bake, as illustrated in Figure J8, and the degradation was usually more severe than that displayed by the nonreversible failures. In many instances, the emitter-base

TABLE J5. EXAMPLES OF TYPICAL BAKE RECOVERY OF h_{FE1} - P/N 773052 - NPN LOW POWER AMPLIFIER

TEST CELL	PART S/N	TIME OF FAILURE	TIME OF REMOVAL	VALUE OF hFE1		
				PRE-STRESS	AT 1 HOUR	AFTER BAKING FOR 16 HOURS AT 225°C
5(V_{MAX}, 225°C)	101	1 HR	1 HR	64	22	63
	115			62	29	58
	121			53	17	51
	145			58	11	58
↓	154	↓	↓	46	23	43

TABLE J6. EXAMPLES OF TYPICAL NONRECOVERY OR INCOMPLETE RECOVERY OF h_{FE1} - P/N 773052 - NPN LOW POWER AMPLIFIER

TEST CELL	PART S/N	TIME OF FAILURE	TIME OF REMOVAL	VALUE OF hFE1				BAKE TIME/TEMP.
				PRE-STRESS	AT THE TIME OF FAILURE	AT THE TIME OF REMOVAL	POST BAKE	
4(V_O, 263°C)	195	1 HR	4 HR	50	38	37	35	16 HRS @ 270°C
	163	1 HR	1000 HR	48	26	18	19	↓
	193	1000 HR	↓	61	37	37	38	
↓	213	1000 HR	↓	62	25	25	27	↓
3(V_{LO}, 263°C)	234	256 HR	256 HR	69	29	29	34	6 HRS @ 225°C
2(V_{MID}, 263°C)	351	8 HR	32 HR	91	27	36	56	↓
	352	8 HR	32 HR	71	26	30	30	

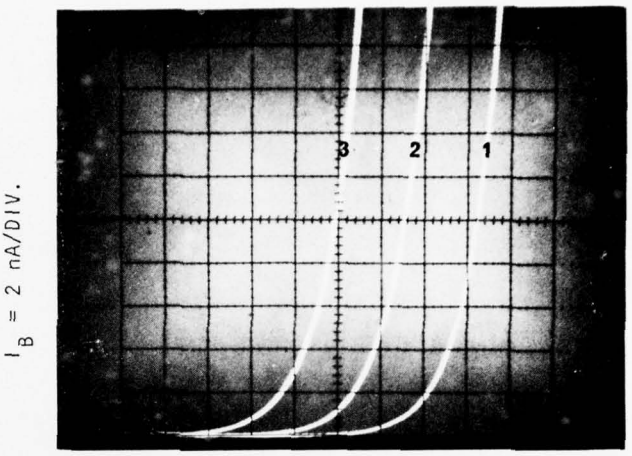


FIGURE J7. FORWARD BASE-EMITTER CHARACTERISTICS OF TWO FAILED TRANSISTORS (TRACES 2 AND 3) AND, FOR COMPARISON, A NORMAL UNSTRESSED TRANSISTOR (TRACE 1) - P/N 773052 - NPN LOW POWER AMPLIFIER

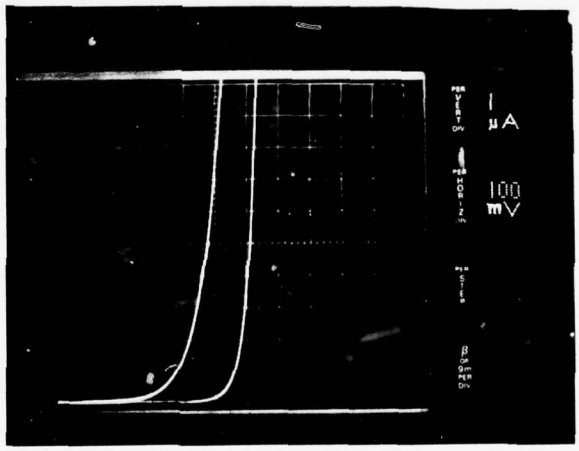


FIGURE J8. FORWARD BASE-EMITTER CHARACTERISTICS OF A FAILED TRANSISTOR (L/H TRACE) AND, FOR COMPARISON, A NORMAL UNSTRESSED TRANSISTOR (R/H TRACE) - P/N 773052 - NPN LOW POWER AMPLIFIER

junction displayed a channeled reverse characteristic as illustrated in Figure J9. The gain of the failed transistor depicted in Figures J8 and J9 had dropped from 58 to 11 after one hour in Cell 5. Reversible degradation of the emitter junction is caused by depletion or inversion of the p-type base region due to the accumulation of a net positive charge in or on the passivation over the base. The accumulation results from drift of mobile cation contamination, usually sodium ions, under the influence of applied bias and elevated temperature. During the life test, however, no external voltage was applied across the emitter-base junction; the c-b junction was reverse biased and the emitter terminal was open. Thus, any bias across the e-b junction would have had to come from an unforeseen floating potential on the emitter. The emitter floating potential of each failed transistor (nonreversible as well as reversible) from the powered cells was measured using the circuit shown in Figure J10. All of the nonreversible failures exhibited emitter floating voltages of 0.7 volt or less (generally 0V). All of the reversible failures exhibited floating voltages ranging from 0.5 volt to BV_{EBO}. These parts apparently contained a conductive path between the collector and the emitter such as diffusion spike or pipe. The resistance of the paths was high enough that it could not be detected parametrically (there was no correlation between I_{CEO} and the presence of a path), yet low enough to cause some of the voltage applied to the collector terminal during accelerated testing to develop on the emitter.

Bulk and Mechanical Failures - One part exhibited catastrophic values of h_{FE1} and h_{FE2} due to an open collector. The open collector was traced to separation of the silicon die from the header. Examination of the underside of the die disclosed that it contained an insufficient amount of die attach eutectic as shown in Figure J11. The gold eutectic did not alloy properly to the silicon either because the backside of the die was not cleaned properly or because the bonding temperature was too low. The problem was more extensive than indicated by this single failure. Sample testing of life test failures (that failed for other reasons) disclosed 16 other parts with defective die bonds. These parts exhibited excessive forward drop from base to collector, as illustrated in Figure J12, and in some instances the die would detach from the header if nudged with a probe. All of these 16 parts had been exposed to temperatures of 225°C or 263°C for 512 hours or more, suggesting that relatively long exposure to elevated temperature was required to

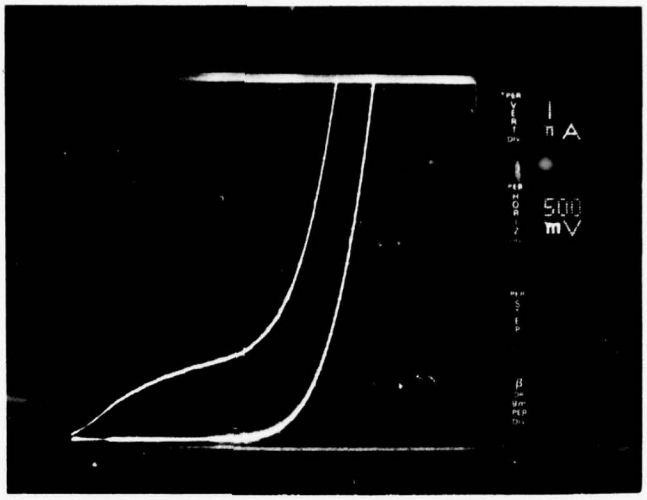


FIGURE J9. EXAMPLE OF A CHANNELED REVERSE EMITTER-BASE CHARACTERISTIC (L/H TRACE) DISPLAYED BY A FAILED TRANSISTOR AND, FOR COMPARISON, THE REVERSE E-B CHARACTERISTIC (R/H TRACE) OF A NORMAL TRANSISTOR - P/N 773052 - NPN LOW POWER AMPLIFIER

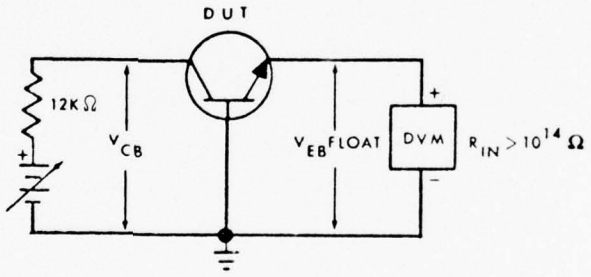
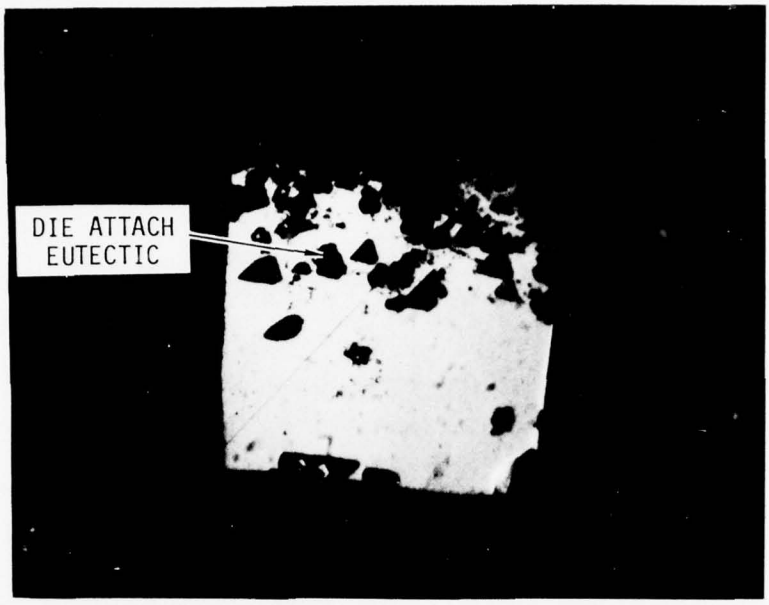


FIGURE J10. EMITTER FLOATING POTENTIAL MEASUREMENT CIRCUIT - P/N 773052 - NPN LOW POWER AMPLIFIER



132X

FIGURE J11. BACKSIDE OF THE LOOSE DIE SHOWING MINIMAL AMOUNT OF DIE ATTACH EUTECTIC - P/N 773052 - NPN LOW POWER AMPLIFIER

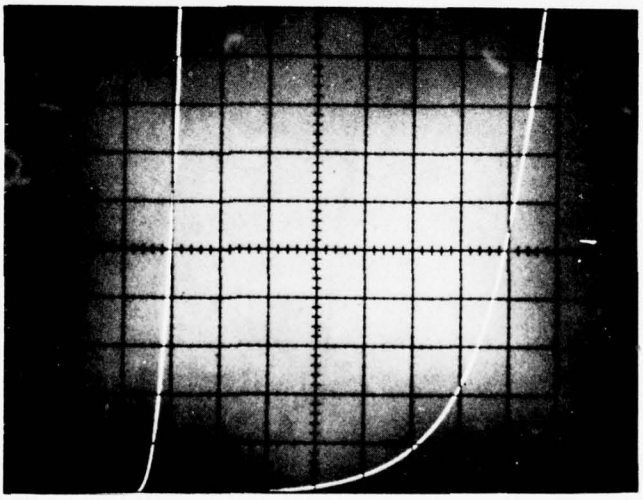


FIGURE J12. BASE-COLLECTOR FORWARD CHARACTERISTICS OF A TRANSISTOR WITH A DEFECTIVE DIE BOND (R/H TRACE) AND, FOR COMPARISON, A TRANSISTOR WITH A GOOD DIE BOND (L/H TRACE) - P/N 773052 - NPN LOW POWER AMPLIFIER

degrade the defective bonds to the extent that the forward b-c drop was affected. However, under actual usage conditions these parts probably would have exhibited much shorter lifetimes. Operation at high power dissipation levels or power cycling conditions would decrease the lifetimes because of impaired heatsinking ability due to the poor die bonds. Therefore, it is recommended that a $V_{CE}(SAT)$ type test be specified for this part to monitor the electrical quality of the die bond and that appropriate screening procedures be incorporated to monitor the mechanical integrity of the bond.

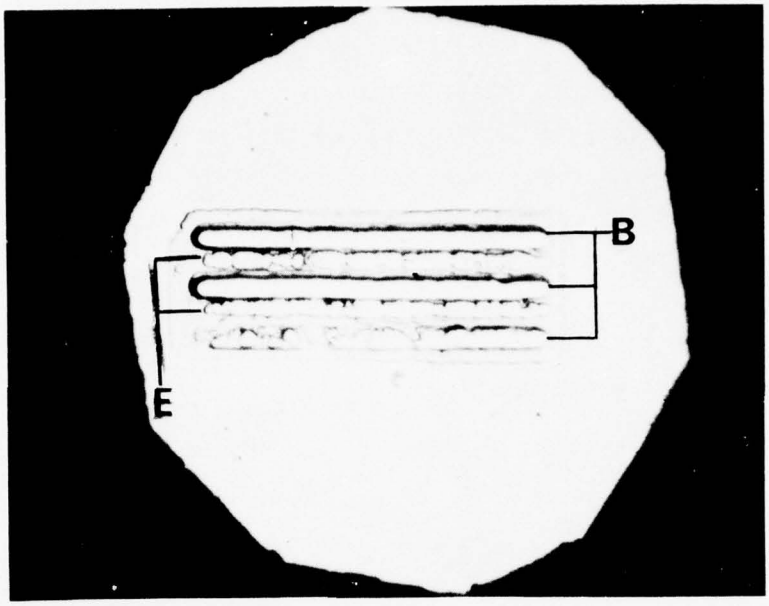
Two transistors exhibited low gain and low breakdown voltages due to degraded collector-base and emitter-base junctions. The degradation was traced to poor diffusion and contact definition, as illustrated in Figure J13, caused by photolithographic or etch errors.

One part exhibited low BV_{CBO} due to a degraded collector-base junction. The degradation was not bake reversible and this part exhibited marginal BV_{CBO} (23V) and abnormally high I_{CEO} (36 μA) upon receipt, which indicated that the degradation was caused by a bulk defect introduced during manufacturing. Chemical dissection of the junction did not reveal the flaw; consequently, the exact failure mechanism was not established.

Test Error - One part exhibited low h_{FE} and BV_{EBO} due to a shorted emitter-base junction. The short was caused by a flashover spike composed of aluminum, extending from an emitter finger to an adjacent base finger, as shown in Figure J14. The damage was attributed to electrical transients generated by the test set because 1) electrical transients characteristically produce this type of damage, and 2) two control samples failed in this same manner, which indicates that the damage was incurred during parametric testing rather than during accelerated life.

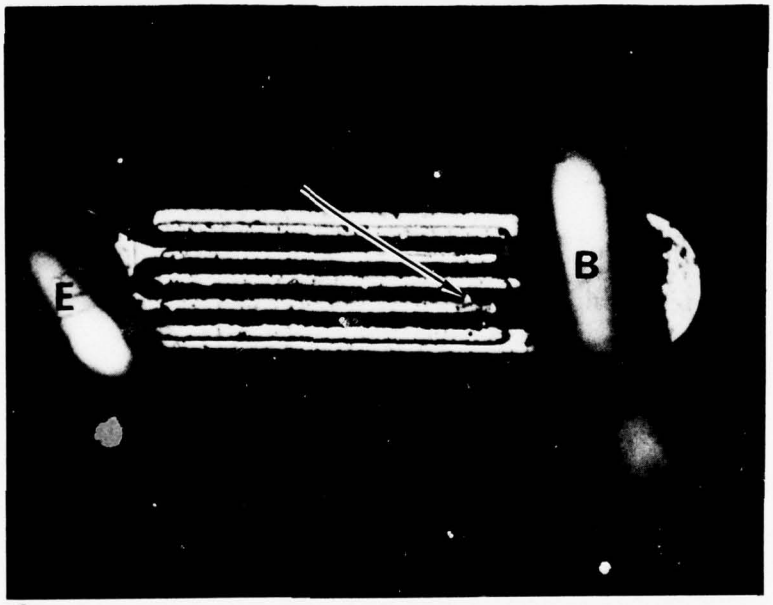
J8.0 DATA CORRELATION

The Table J4 summary attributes 154 h_{FE} surface instability life test failures to either an increase in surface state density of the oxide or to mobile ionic contamination within the oxide. Subsequent experiments indicated the entire lot was probably contaminated with mobile ions. However, this condition caused a failure only when the emitter-base junction was reverse biased during the life test, and this only occurred when there was a leakage path present from collector to emitter.



750X

FIGURE J13. TRANSISTOR DIE AFTER SILICON ETCH SHOWING THE RAGGED AND DISCONTINUOUS EMITTER AND BASE DIFFUSIONS AND CONTACTS - P/N 773052 - NPN LOW POWER AMPLIFIER



780X

FIGURE J14. LATERAL SPIKE OF ALUMINUM (ARROW) BRIDGING AN EMITTER AND A BASE FINGER - P/N 773052 - NPN LOW POWER AMPLIFIER

The h_{FE} degradation experienced by the two zero volt test cells, Figure J15, was attributed to a temperature induced increase in surface state density. This failure mechanism provided sufficient failures for statistical distribution analysis. The Figure J16 cumulative failure distribution plots show bimodal failure distributions, i.e., both early ("freak" population) and late ("main" population) failures. The data shows a good fit for the lognormal failure distribution. Pertinent distribution data is summarized in Table J7.

The Figure J17 Arrhenius plots of the "freak" and "main" populations can be represented by the following equations:

$$\ln (t_{50\%})_{freak} = -44.563 + \frac{2.07}{kT}$$

$$\ln (t_{50\%})_{main} = -42.649 + \frac{2.24}{kT}$$

The percentage of "freaks" in the two unbiased cells is 10.3%. Therefore, the total instantaneous failure rate, $\lambda(t)$, can be expressed as follows:

$$\lambda(t) = \lambda(t)_{freak} \times (0.103) + \lambda(t)_{main} \times (0.897)$$

$$= \left[\frac{\frac{1}{t} \exp - \frac{\left[\ln t + 44.563 - \frac{2.07}{kT}\right]^2}{2(1.36)^2}}{\int_t^\infty \frac{1}{t'} \left[\exp - \frac{\left[\ln t' + 44.563 - \frac{2.07}{kT}\right]^2}{2(1.36)^2} \right] dt'} \right] \times (0.103)$$

$$+ \left[\frac{\frac{1}{t} \exp - \frac{\left[\ln t + 42.649 - \frac{2.24}{kT}\right]^2}{2(1.52)^2}}{\int_t^\infty \frac{1}{t'} \left[\exp - \frac{\left[\ln t' + 42.649 - \frac{2.24}{kT}\right]}{2(1.52)^2} \right] dt'} \right] \times (0.897)$$

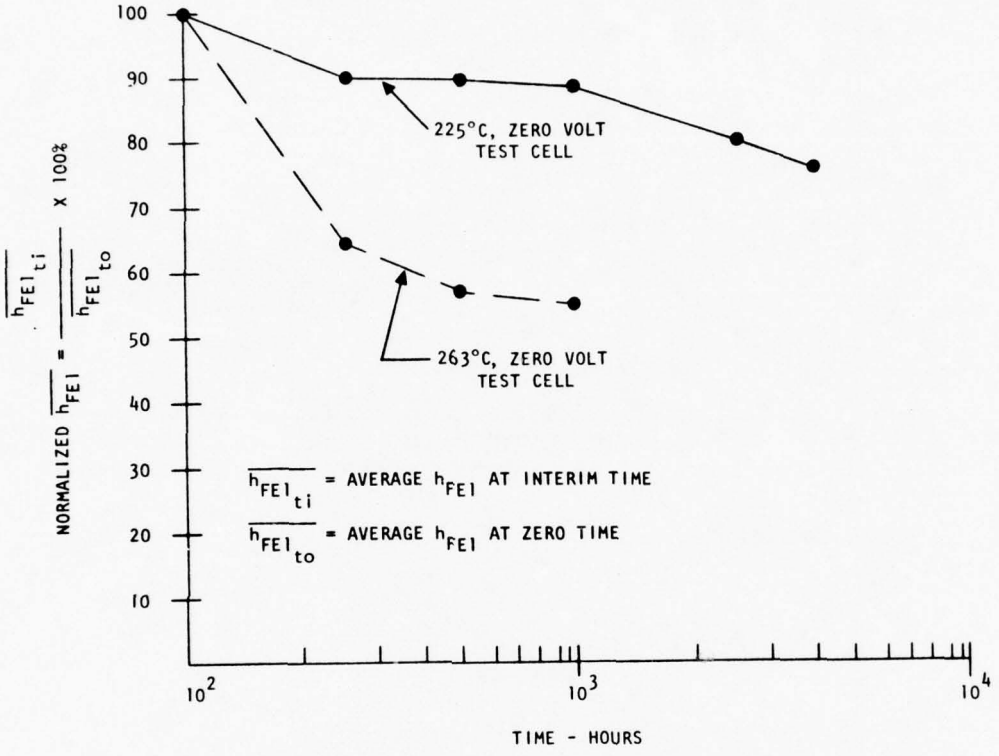


FIGURE J15. NORMALIZED h_{FEI} TIME/TEMPERATURE DEGRADATION - P/N 773052 - NPN LOW POWER AMPLIFIER

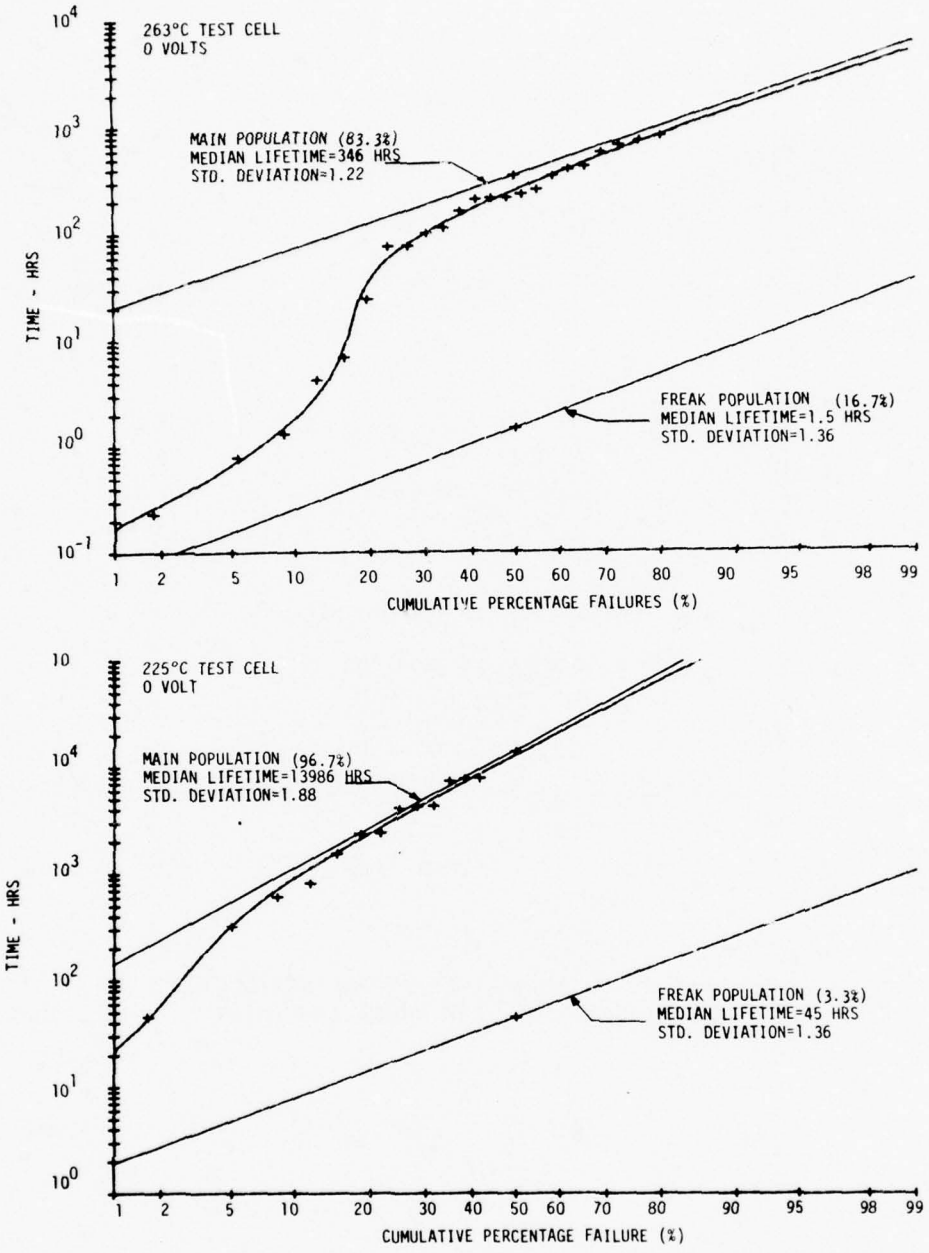


FIGURE J16. CUMULATIVE FAILURE DISTRIBUTIONS FOR CELL 4 (TOP) AND CELL 7 (BOTTOM) - P/N 773052 - NPN LOW POWER AMPLIFIER

TABLE J7. SUMMARY DATA - P/N 773052 -
NPN LOW POWER AMPLIFIER

Cell No	Test Voltage (volts)	Number of Failures	T_A (°C)	T_J (°C)	FREAK POPULATION			MAIN POPULATION		
					Median Life (hours)	Standard Deviation (hours)	% Freak	Median Life (hours)	Standard Deviation (hours)	% Main
4	Zero	23	263	263	1.5	1.36	16.7	346	1.22	83.3
7	Zero	13	225	225	45	1.36 ⚠1	3.3	13,986	1.88	96.7

⚠1 Insufficient data for calculation.
Cell 4 value assumed for Cell 7.

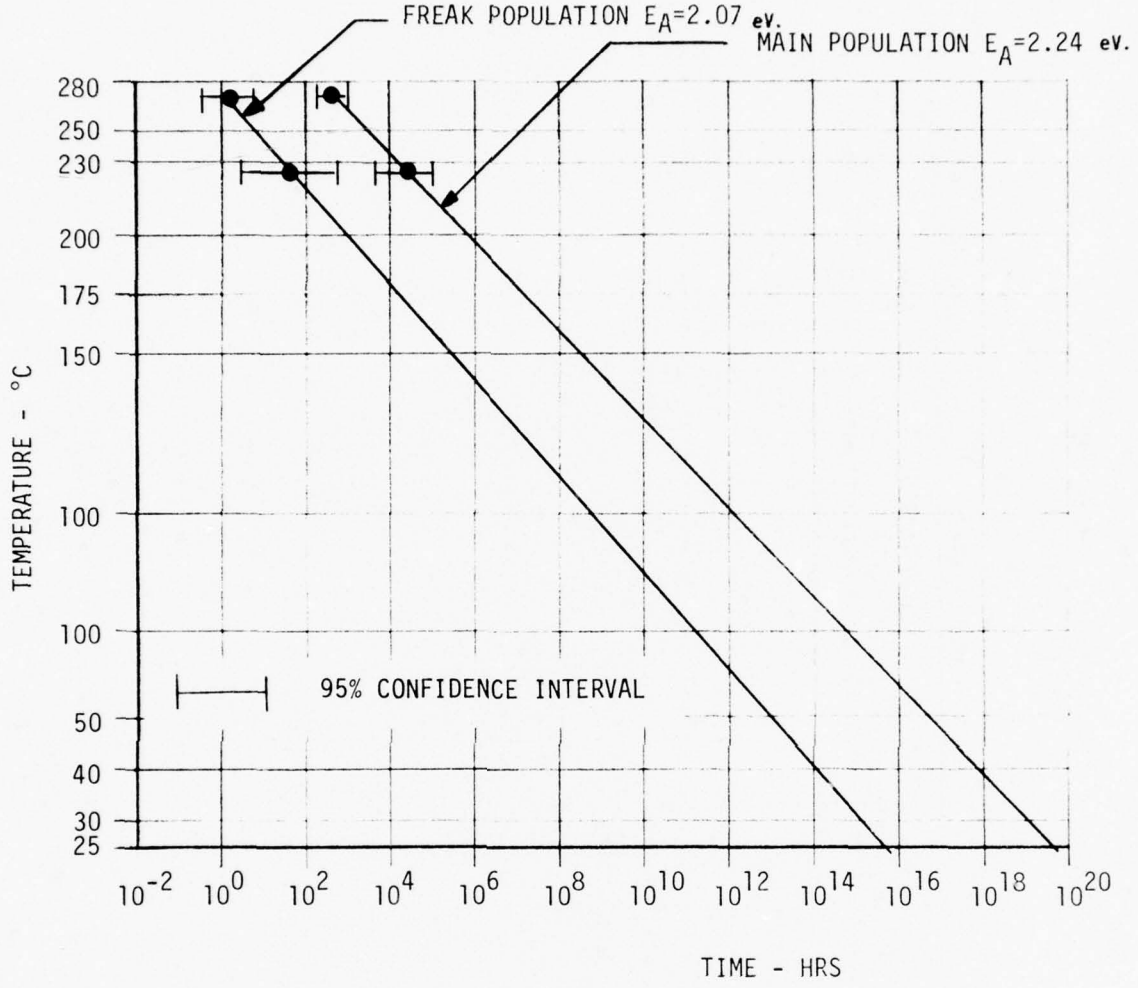


FIGURE J17. ARRHENIUS PLOTS - P/N 773052 - NPN LOW POWER AMPLIFIER

The part specification for this device has 200°C as the upper storage temperature limit. The data analysis reveals that the "freak" population will have a "short" median lifetime (≈100,000 hours) when stored at temperatures above 150°C. The suitability of the 200°C storage temperature limit should be investigated.

J9.0 CONCLUSIONS AND RECOMMENDATIONS

- This part will experience h_{FE} degradation as a function of storage time and temperature. The calculated 20 year maximum instantaneous failure rate, $\lambda(t)_{MAX}$, (6.973×10^{-15} failures per hour) appears acceptable.
- The die bond on this part exhibited marginal strength after the accelerated life test. One die came loose during the test and 16 others were observed to have defective bonds. A $V_{CE}(SAT)$ type test could be used to monitor the electrical quality of the die bond; an investigation should also be accomplished to establish if the die bond degradation is applicable to the SAM-D configuration.
- The entire lot was contaminated with mobile ions in the oxide. A short term test (4 hours with the emitter-base reversed biased) at 225°C will detect this condition.
- The part specification has +200°C as the upper storage temperature limit. This limit should be re-assessed due to the expected degradation at temperatures above 150°C.

APPENDIX K

P/N 772931

N CHANNEL FET

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K1.0 PART DESCRIPTION

The N Channel FET, P/N 772931, is a 2N4957 type beam lead junction field effect transistor mounted in a three lead TO-18 package and manufactured by Raytheon Company, Semiconductor Division. This test configuration is different from the SAM-D use configuration.

K2.0 CONSTRUCTION ANALYSIS

The pertinent construction details for the test configuration are tabulated in Table K1. Figures K1 and K2 provide an external view and a terminal diagram of the device. A photograph of the die mounted in the package and the die topography are provided in Figure K3. No materials contained in this part limited testing below 300°C.

The typical SAM-D configuration is pictured in Figure K4. The beam lead die is bonded to the metallization of a ceramic substrate.

K3.0 ELECTRICAL TEST CRITERIA

The electrical tests for this device include all the DC tests of 772931 and are listed in Table K2.

K4.0 BIAS CIRCUIT ANALYSIS

One bias circuit was evaluated and found suitable for the life test. The source and drain were grounded and a negative voltage was applied to the gate. Figure K5 illustrates this bias circuit and provides plots of gate current versus ambient temperature for gate voltages of -45 volts and -17 volts. Because the lower gate voltage did not allow operation at an appreciably higher ambient temperature, -40 volts, a voltage near the absolute maximum, was chosen to be the maximum life test voltage. An ambient temperature of 200°C was selected as the maximum for the life test. A 24K ohm current limiting resistor was used to preclude catastrophic damage in the event of device failure.

K5.0 STEP STRESS TEST RESULTS

A step stress test, consisting of three 16 hour steps at ambient temperatures of 175°C, 200°C and 225°C, was performed on 20 devices, using the biasing configuration described in Paragraph K4.0 with -40 volts on the gates. The twelve step

TABLE K1. PART CONSTRUCTION DETAILS - P/N 772931 - N CHANNEL FET

A. IDENTIFICATION

1. Part Name: N Channel FET (2N4957)
2. Part Manufacturer: Raytheon Co., Semiconductor Div.
3. Part Number: 772931
4. Date Code: 7528

B. PACKAGE

1. Type: 3-Lead, TO-18 (Drawing No. 757430)
2. Weight: 0.321 gram
3. Materials:

   a) Cap: Steel
   b) Header: Kovar, gold-plated
   c) Leads: Kovar, gold-plated
   d) Cap Seal: Weld
   e) Lead Seal: Glass

C. INTERNAL GEOMETRY

1. Interconnections: Beam leads bonded to gold-plated header

2. Die:

   a) Type: Silicon, planar (Beam Lead)
   b) Scribe Method: Etch
   c) Dimensions: 0.018 inch X 0.018 inch
   d) Passivation: Silicon Nitride over Silicon Dioxide
   e) Glassivation: Silicon Dioxide over interdigitated fingers

3. Metallization Type: Gold/Titanium/Platinum

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3.4X

FIGURE K1. EXTERNAL CONSTRUCTION - P/N 772931 - N CHANNEL FET

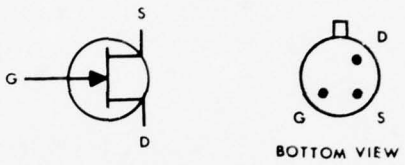
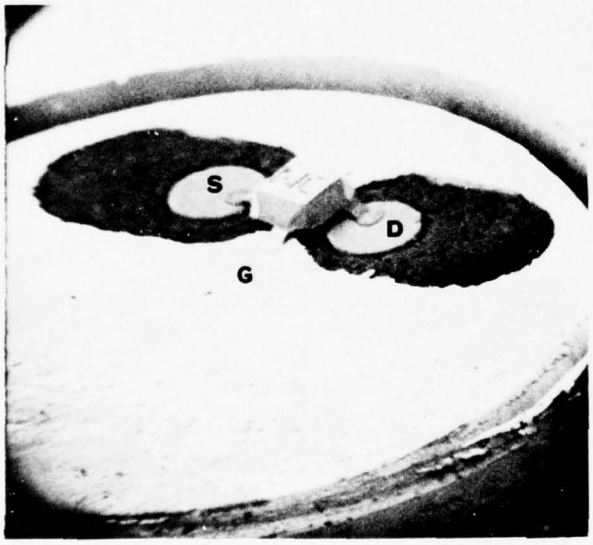
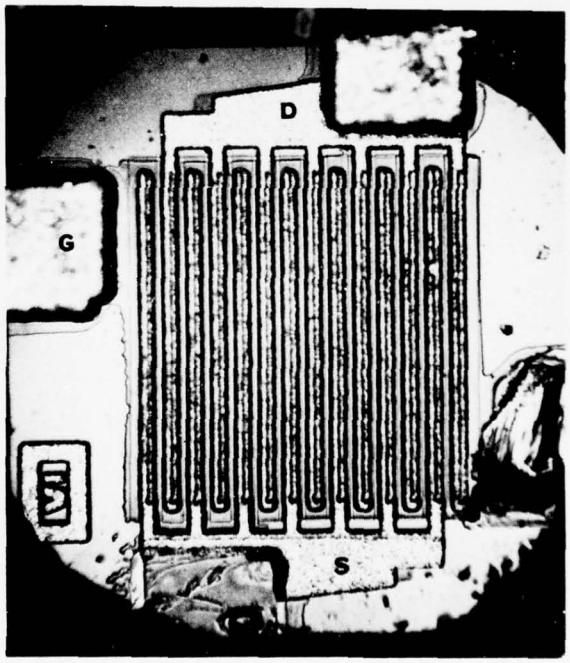


FIGURE K2. SYMBOL AND TERMINAL DIAGRAM - P/N 772931 - N CHANNEL FET



40X (SEM)

VIEW WITH LID REMOVED



199X

DIE TOPOGRAPHY

FIGURE K3. INTERNAL CONSTRUCTION DETAILS - P/N 772931 - N CHANNEL FET

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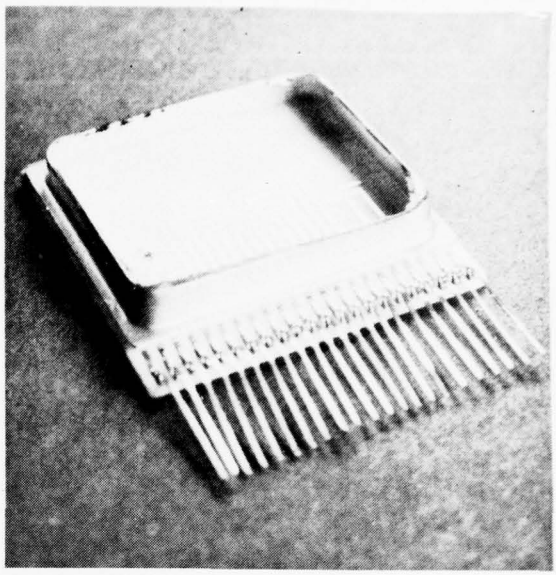
EXTERNAL



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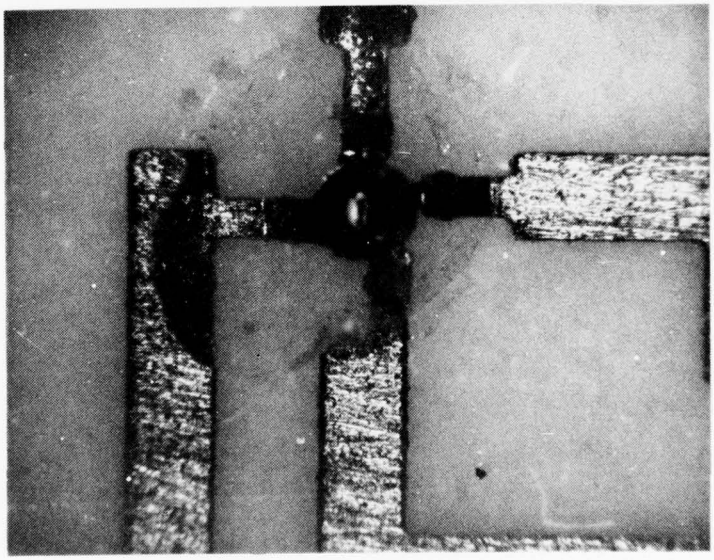
INTERNAL



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DIE MOUNTED IN SAM-D CONFIGURATION

FIGURE K4. TYPICAL SAM-D CONFIGURATION - P/N 773381 - N CHANNEL FET

TABLE K2. ELECTRICAL TEST CONDITIONS - P/N 772931 - N CHANNEL FET

TEST NO.	SYMBOL	MIL-STD-750	CONDITIONS	T_A=+25°C		T_A=+150°C		UNITS
				MIN	MAX	MIN	MAX	
1	$\|V_{(BR)GSS}\|$	3401 COND. C (1)	I_G = 1.0 µA	40	-	(2)	-	Vdc
2	$\|I_{D(OFF)}\|$	3413 COND. A (1)	V_{DS} = 15V; V_{GS} = 10V	-	0.25	-	500	nA
3	$\|I_{GSS}\|$	3411 COND. C (1)	V_{GS} = 20V	-	500	-	1000	pA
4	$\|V_{GS(OFF)}\|$	3403 (1)	V_{DS} = 15V; I_D = 1.0nA		-8	-	(2)	Vdc
5	$V_{DS(ON)}$	3405 (1)	I_D = 10 mA	-	0.5	-	(2)	Vdc

(1) Equivalent test configuration
(2) Limits not specified by part drawing - Measurement made for information only.

Initial and final test conducted at +25°C and +150°C. Interim test conducted at +25°C.

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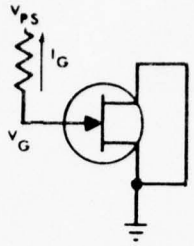

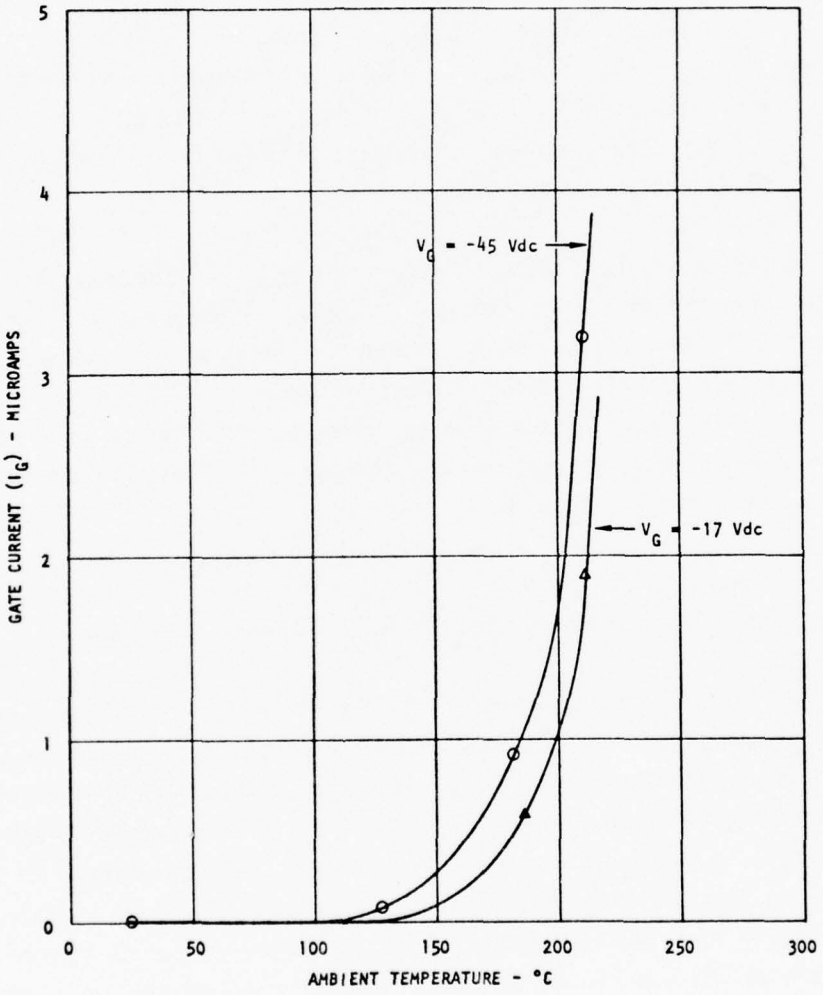

FIGURE K5. BIAS CIRCUIT EVALUATION - P/N 772931 - N CHANNEL FET

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stress failures, summarized in Figure K6, are included in the failure analysis discussion in Paragraph K7.0. The step stress test conditions with a maximum ambient temperature of 200°C were considered acceptable for the accelerated life test program.

K6.0 LIFE TEST CONDITIONS AND RESULTS

The life test conditions are included in Figure K6. Additional electrical measurements at 1.0 and 2.0 hours were incorporated to provide more data on early test failures. As summarized in Table K3, all test cells completed 4000 hours of life testing; however, at 128 hours the life test was delayed due to a group of electrical overstress failures. Replacement parts were subjected to the Cell 1 and Cell 5 life test conditions and advanced to the 128 hour point, at which time the accelerated life test was resumed.

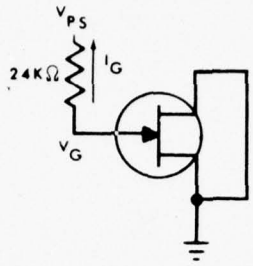
During the delay of the life test, an effort was made to determine the exact cause of the overstress failures. The test methods were reviewed and handling techniques were examined. It was not determined whether the failures were caused by static electricity or by a transient during electrical testing. However, handling techniques used with CMOS devices were initiated for this device and the occurrence of subsequent overstress failures was greatly reduced. These overstress failures posed no problem for the test program.

K7.0 FAILURE ANALYSIS

A summary of the failure analysis results is provided in Table K4.

Surface Instability - Nine step-stress and forty-three life test parts exhibited excessive I_{GSS} and/or $I_{D(off)}$ due to degradation of the drain and/or the source junction. The degraded junctions exhibited either a channeled characteristic, as illustrated in Figure K7, or nonlinear leakage, as illustrated in Figure K8. All parts recovered, if baked, if stored at room temperature, or if left on test, which indicated that the degradation was due to a surface instability mechanism such as ion drift through the passivation or separation of mobile charges in the fringing field of the reverse biased junction. Thus, these failures were attributed to the design or the processing of the SiO_2/Si_3N_4 passivation.

STEP STRESS AND LIFE TEST CIRCUIT



STEP STRESS TEST - FAILURE SUMMARY (20 DEVICES)

AMBIENT TEMP. (°C)	V_G (V)	CUMULATIVE FAILURES
175	-40	3
200	-40	9
225	-40	12

LIFE TEST CONDITIONS

TEST CELL NUMBER	T_A AMBIENT TEMPERATURE (°C)	V_G GATE VOLTAGE (VOLTS)	I_G GATE CURRENT (MICROAMPS)	P_d POWER DISSIPATION (MICROWATTS)	T_J JUNCTION TEMPERATURE (°C)
1	200	-40	2.2	88	200
2	200	-20	1.5	30	200
3	200	0	0	0	200
4	175	-40	0.6	24	175
5	150	-40	0.2	8	150

FIGURE K6. STEP STRESS RESULTS AND LIFE TEST CONDITIONS - P/N 772931 N CHANNEL FET

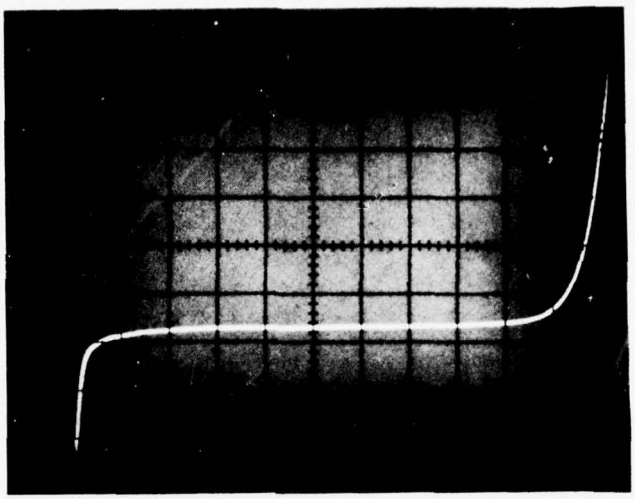
TABLE K3. LIFE TEST SUMMARY - P/N 772931 - N CHANNEL FET

TEST CELL DESCRIPTION				CUMULATIVE FAILURES AT HOURS OF TEST												
CELL NO	APPLIED BIAS	AMBIENT TEMP.	QUANTITY	1	2	4	8	16	32	64	128	256	512	1000	2504	4000
1	40 VDC	200 C	44	4	7	10	10	12	14	14	19	21	24	25	28	29*
2	20 VDC	200 C	30	1	1	1	1	1	1	2	2	2	2	2	3	4*
3	0 VDC	200 C	30	0	0	2	2	2	3	3	4	4	4	4	4	4*
4	40 VDC	175 C	30	1	2	2	2	2	4	4	4	5	6	6	9	12*
5	40 VDC	150 C	36	1	3	6	6	6	7	7	8	9	11	12	13	13*

* TEST TERMINATED

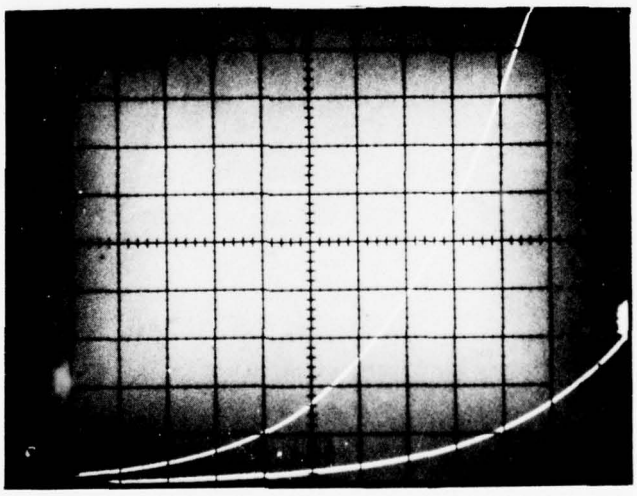
TABLE K4. FAILURE ANALYSIS SUMMARY - P/N 772931 - N CHANNEL FET

	A. FAILED PARAMETER OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TIME OF FAILURE (HOURS)					
		STEP STRESS	200°C			175°C	150°C
			40V	20V	0V	40V	20V
			CELL 1	CELL 2	CELL 3	CELL 4	CELL 5
SURFACE INSTABILITY FAILURES	A. I_{GSS} AND/OR $I_{D(OFF)}$ B. DEGRADED DRAIN OR SOURCE JUNCTION C. MOBILE ION DRIFT D. CONTAMINATION IN THE PASSIVATION	2@175°C STEP 4@200°C STEP 3@225°C STEP	4@1 2@4 1@16 1@32 4@128 2@256 1@512 2@2504 1@4000	1@1 1@2504 1@4000	1@4	1@1 1@2 2@32 1@256 1@512 3@2504 2@4000	1@1 2@2 1@4 1@128 1@256 2@512 1@1000 1@2504
TEST ERROR	A. BV_{GSS} & I_{GSS} & $I_{D(OFF)}$ B. SHORTED OR DEGRADED DRAIN OR SOURCE JUNCTION C. FLASH-OVER SHORTS D. ELECTRICAL OVERSTRESS	1@175°C STEP 2@200°C STEP	3@2 1@4 1@16 1@32 1@128 2@512 1@1000 1@2504	1@64	1@32 1@128	1@4000	2@4 1@32
	A. $I_{D(OFF)}$ AND I_{GSS} B. DEGRADED SOURCE JUNCTION C. NOT DETERMINED D. NOT DETERMINED				1@4		
	TOTAL NUMBER OF FAILED PARTS	12	29	4	4	12	13



HORIZ. ≈ 2 VOLTS/DIV
VERT. ≈ 50 nA/DIV

FIGURE K7. EXAMPLE OF CHANNELED CHARACTERISTICS (I_{GSS} VS. V_{GSS}) - P/N 772931 - N CHANNEL FET



HORIZ. = 2 VOLTS/DIV
VERT. = 50 nA/DIV

FIGURE K8. EXAMPLE OF NON-LINEAR LEAKAGE. TOP TRACE = $I_{D(OFF)}$; BOTTOM = I_{GSS} - P/N 772931 - N CHANNEL FET

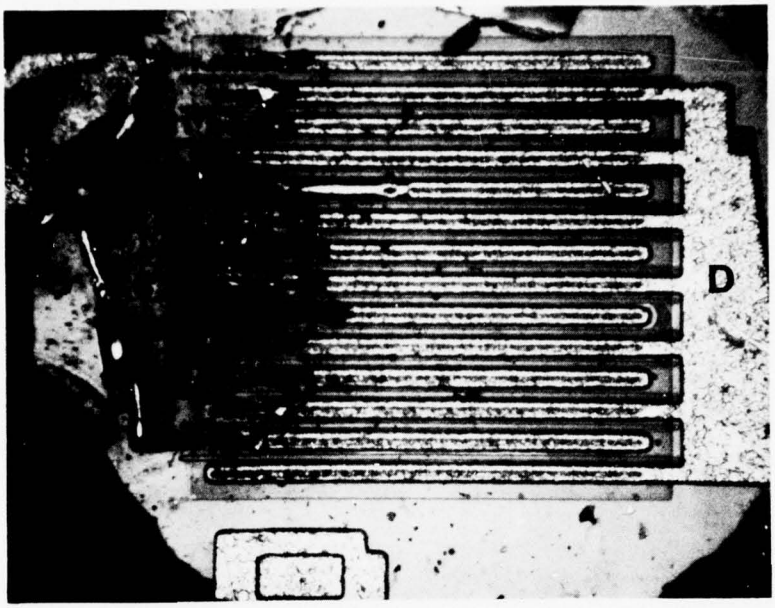
Shorted Junctions - Three step-stress and eighteen life test parts exhibited low BV_{GSS} and excessive I_{GSS} and $I_{D(off)}$ due to a degraded (low breakdown) or shorted drain or source junction. In a few instances the die contained obvious damage, as illustrated in Figure K9. In most instances, however, the metallization and passivation had to be removed and the silicon etched in order to delineate the bulk damage. As illustrated in Figure K10, these parts contained trails of melted silicon (flashover shorts) extending from a drain or source ohmic contact to the adjacent gate diffusion. The type of damage was characteristic of electrical overstress caused by a voltage transient or possibly even static electricity.

Mechanical Failures - One part in the zero volt cell exhibited excessive $I_{D(off)}$ and I_{GSS} due to a degraded source junction. The degradation worsened when the part was subjected to 225°C and 250°C bakes. $I_{D(off)}$ and I_{GSS} recovered completely when the beams were cut and the die was removed from the header, indicating that the degradation was mechanical in nature. However, microscopic examinations of the die and the package did not disclose any anomaly; therefore, the exact cause of failure was not determined.

K8.0 DATA CORRELATION

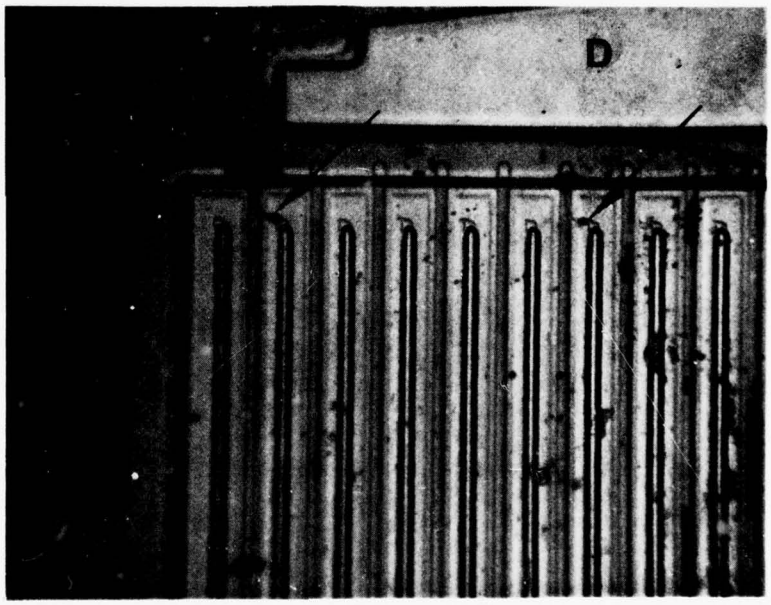
The Table K4 Failure Analysis Summary attributes all but one of the life test failures to one of two causes, contamination in the passivation and electrical overstress. The one exception was mechanical in nature. The source of the electrical overstress could not be positively established. Voltage transients or static electricity are both possibilities. In any event the electrical overstress failures are not applicable for data analysis. Replacement parts were added to the test program to maintain an adequate sample size for data evaluation.

All test cells exhibited surface instability failures attributed to an ion drift or charge separation failure mechanism caused by contamination in the passivation. The mechanism appears voltage/temperature dependent. The three 40 volt test cells, each at a different temperature, produced the most failures and displayed a temperature sensitivity. The 20 volt and zero volt test cells, Cells 2 and 3, respectively, produced significantly fewer failures, suggesting the existence of a voltage sensitivity.



250X

FIGURE K9. EXAMPLE OF CATASTROPHIC DAMAGE (VAPORIZED SOURCE METALLIZATION) - P/N 772931 - N CHANNEL FET



491X

FIGURE K10. CLOSE-UP OF THE DIE AFTER SILICON ETCH SHOWING FLASH-OVER SHORTS (ARROWS) EXTENDING FROM A DRAIN CONTACT AND A SOURCE CONTACT TO THE GATE - P/N 772931 - N CHANNEL FET

Cells 2 and 3 were investigated for obvious degradation trends which would allow extrapolation of times to failure. Figure K11 shows the behavior of $I_{D(off)}$ and I_{GSS}, the two parameters which failed in the high voltage cells. No degradation trend is obvious in Cell 3, the zero volt cell. I_{DSS} in Cell 2, the 20 volt cell, did show signs of degradation, indicating a voltage sensitivity. However, the average value at 4000 hours was only 0.04 nA, much less than the limit of 0.25 nA. Therefore, extrapolation of times to failure was not pursued.

The cumulative failure distribution for Cells 1, 2, 4 and 5 for the surface instability failures are shown in Figures K12 and K13. The three 40 volt cells display "freak" and "main" populations with the "freaks" accounting for 14.7% of the 3 cell population. The three Cell 2 failures also give an indication of comprising a "freak" and "main" population. The pertinent distribution data is summarized in Table K5. The data indicates the "freak" population is primarily voltage dependent and the "main" population is voltage/temperature dependent, as shown by the Figure K14 Arrhenius plots. The 40 volt Arrhenius relationships can be expressed as follows:

$$\ln\,(t_{50\%})_{freak_{40V}} = -14.29033 + \frac{0.11}{kT}$$

$$\ln\,(t_{50\%})_{main_{40V}} = -8.20604 + \frac{0.674}{kT}$$

Since the freak population appears to be primarily voltage dependent, a conservative storage failure rate can be estimated from the 40 volt main population data. Using the "pooled" technique to calculate the standard deviation, the maximum instantaneous failure rate, $\lambda(t)$, can be expressed as follows:

$$\lambda(t) = \frac{\frac{1}{t}\exp -\frac{\left[\ln t + 8.206 - 0.674\left(\frac{1}{kT}\right)\right]^2}{2(2.82)^2}}{\int_t^\infty \frac{1}{t'}\left[\exp -\frac{\left[\ln t' + 8.206 - 0.674\left(\frac{1}{kT}\right)\right]^2}{2(2.82)^2}\right] dt'}$$

The calculated maximum instantaneous failure rate, $\lambda(t)_{MAX}$, is 1.3×10^{-6} failures per hour. Since this value reflects a 40 volt condition and the zero cell exhibits

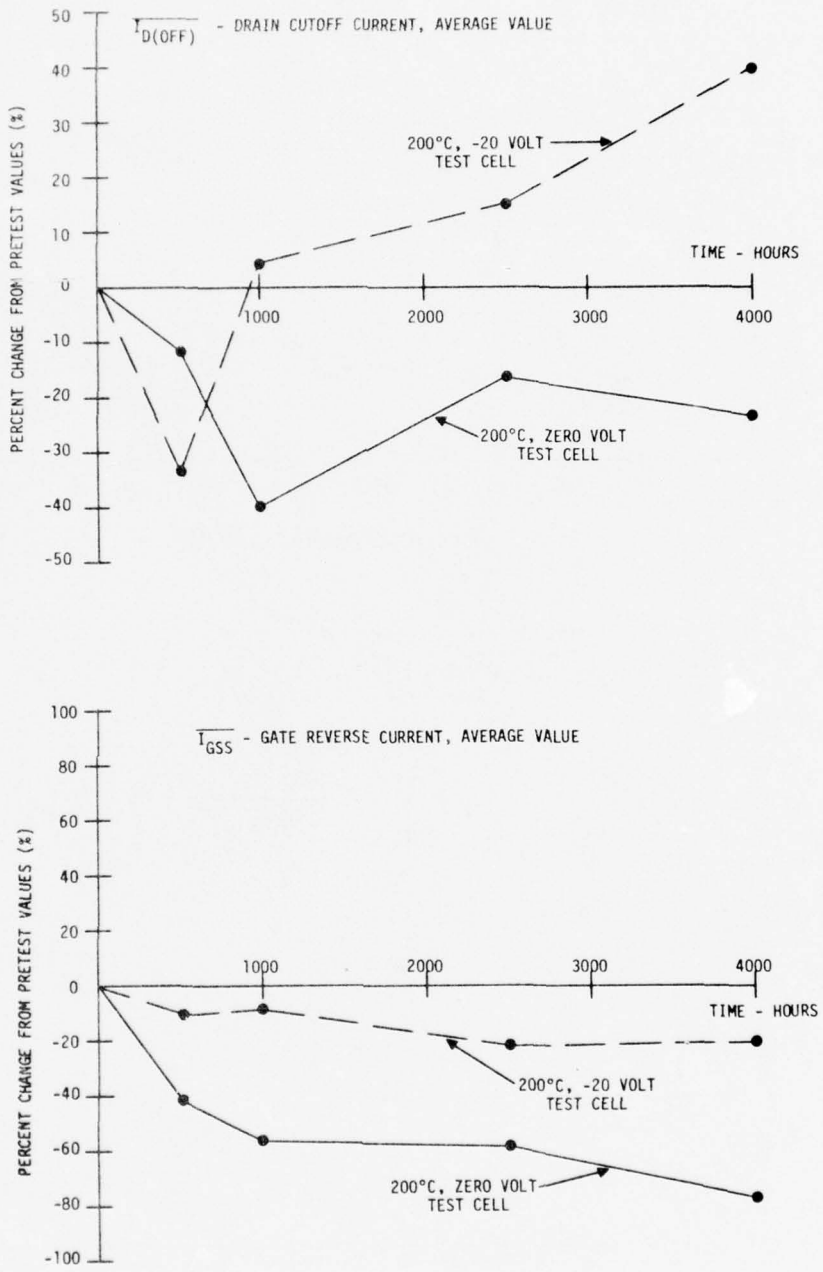


FIGURE K11. BEHAVIOR OF SELECTED PARAMETERS DURING LIFE TEST - P/N 772931 - N CHANNEL FET

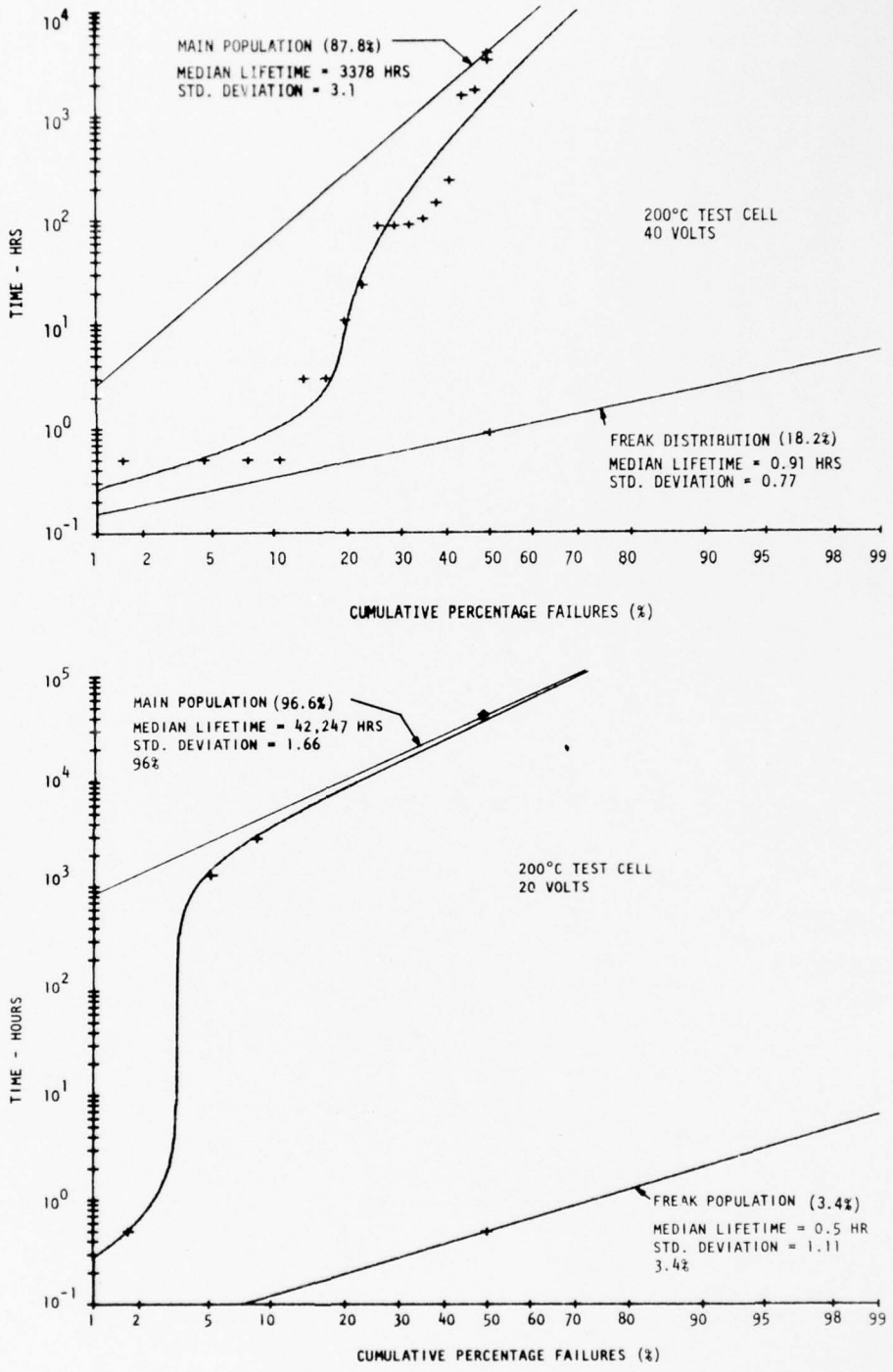


FIGURE K12. CUMULATIVE FAILURE DISTRIBUTIONS FOR CELL 1 (TOP) AND CELL 2 (BOTTOM) - P/N 772931 - N CHANNEL FET

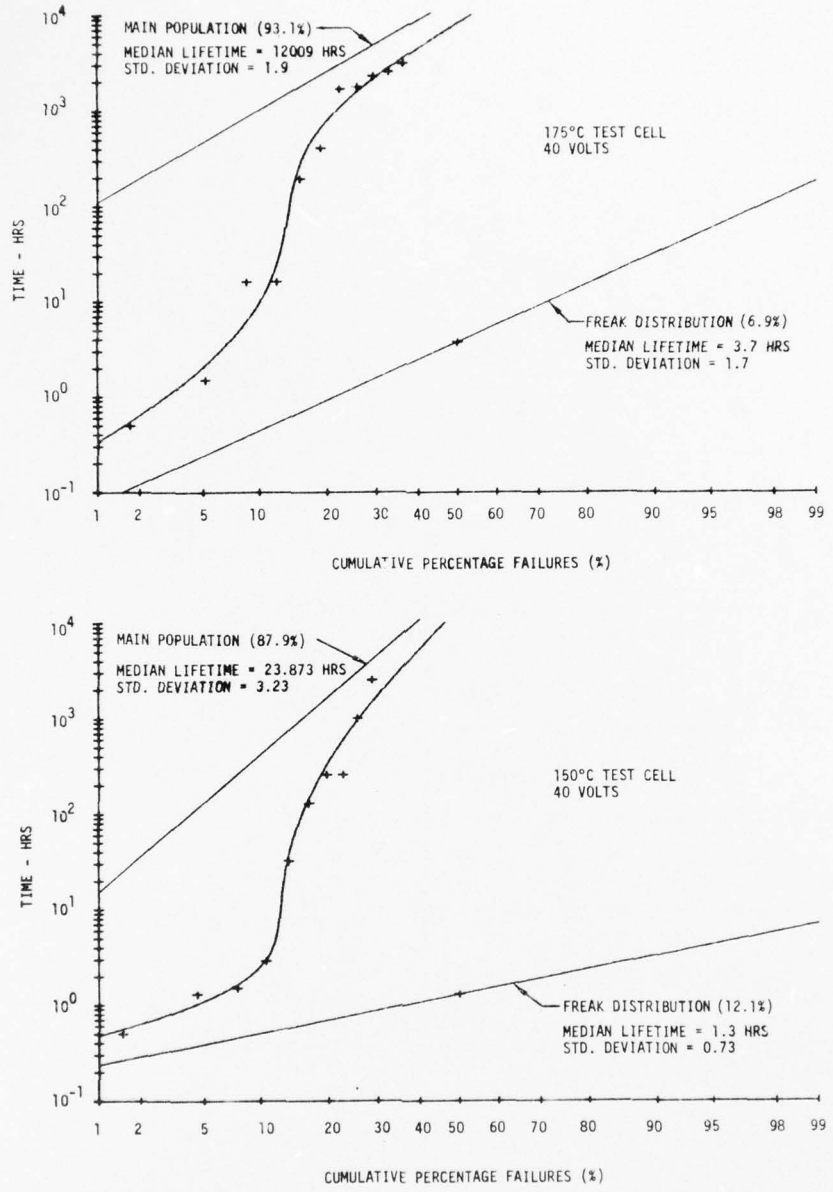


FIGURE K13. CUMULATIVE FAILURE DISTRIBUTIONS FOR CELL 4 (TOP) AND CELL 5 (BOTTOM) - P/N 772931 - N CHANNEL FET

TABLE K5. SUMMARY DATA - P/N 772931 - N CHANNEL FET

CELL NO.	TEST VOLTAGE (VOLTS)	NUMBER OF FAILURES	T_A (°C)	T_J (°C)	FREAK POPULATION			MAIN POPULATION		
					MEDIAN LIFE (HOURS)	STANDARD DEVIATION (HOURS)	% FREAK	MEDIAN LIFE (HOURS)	STANDARD DEVIATION (HOURS)	% MAIN
1	40	18	200	200	0.91	0.77	18.2	3,378	3.1	87.8
2	20	3	200	200	0.5	1.11 △1	3.4	42,247	1.66	96.6
3	0	1	200	200						
4	40	11	175	175	3.7	1.7	6.9	12,009	1.9	93.1
5	40	10	150	150	1.3	0.73	12.1	23,873	3.23	87.9

△1 "Pooled" value of the three 40V cells.

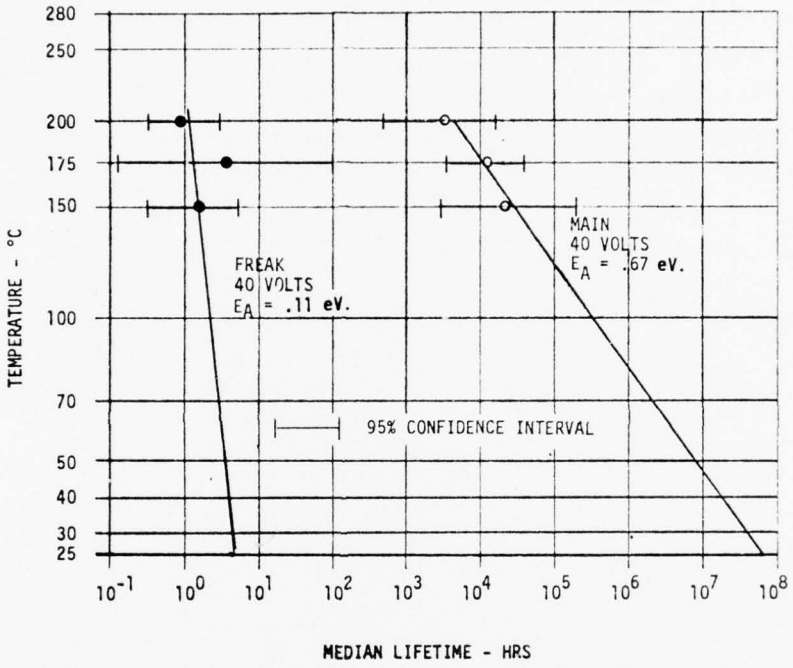


FIGURE K14. ARRHENIUS PLOTS - P/N 772931 - N CHANNEL FET

no degradation trends, the calculated failure rate is conservative by orders of magnitude. Therefore, this device should have a good storage reliability potential.

K9.0 CONCLUSIONS AND RECOMMENDATIONS

- This device experienced only two failures and exhibited good parameter stability when stored for 4000 hours at 200°C. The calculated failure rate using data from the 40 volt test cell indicates a high storage reliability potential.
- A short term high temperature screening test (200°C, 10 hours) will improve operational reliability by eliminating the "freak" population (14.7% of total population).

APPENDIX L

P/N 772932

GENERAL PURPOSE SWITCH

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L3.0	ELECTRICAL TEST CRITERIA	L2
L4.0	BIAS CIRCUIT ANALYSIS	L2
L5.0	STEP STRESS TEST RESULTS	L2
L6.0	LIFE TEST CONDITIONS AND RESULTS	L9
L7.0	FAILURE ANALYSIS	L9
L8.0	DATA CORRELATION	L9
L9.0	CONCLUSIONS AND RECOMMENDATIONS	L13

L1.0 PART DESCRIPTION

The General Purpose Switch, P/N 772932, is a 1N914 type beam lead diode packaged in a three lead TO-18 package and manufactured by Raytheon Company, Semiconductor Division. This test configuration is different from the SAM-D use configuration.

L2.0 CONSTRUCTION ANALYSIS

The pertinent construction details of the test configuration are listed in Table L1. Figures L1 and L2 provide a photograph of the package and a terminal diagram of the device. Photographs of the die mounted in the package and the die topography are provided in Figure L3. This device contains no materials which would restrict testing below 300°C.

The typical SAM-D configuration, Figure L4, has the die beam lead bonded to the metallization deposited on a ceramic substrate.

L3.0 ELECTRICAL TEST CRITERIA

The electrical tests used for this device are listed in Table L2. Test number 5 of Table L2, $I_{R(4)}$, was a manual test performed at selected interim readout times.

L4.0 BIAS CIRCUIT ANALYSIS

This device was evaluated at various reverse bias voltages and ambient temperatures, as summarized in Figure L5. At 75 volts reverse bias, the device went into thermal runaway before 250°C, while at 35 volts reverse bias the device went into thermal runaway prior to 275°C. It was decided that the step stress test would have the devices reverse biased with 75 volts at ambient temperatures up to and including 225°C. Determination of maximum life test temperature and voltage was withheld pending the step stress test results. A 12K ohm current limiting resistor was selected preclude catastrophic damage in the event of device failure

L5.0 STEP STRESS TEST RESULTS

Twenty devices with 75 volts reverse bias were subjected to three 16 hour steps at ambient temperatures of 175°C, 200°C and 225°C and produced no failures, as summarized in Figure L6. An additional step at 250°C with a reverse bias of 35 volts was performed and also failed to produce a failure. It was decided that, for the life test, the maximum voltage would be 35 volts, permitting the maximum temperature to be 250°C.

TABLE L1. PART CONSTRUCTION DETAILS - P/N 772932 - GENERAL PURPOSE SWITCH

A. IDENTIFICATION

1. Part Name: General Purpose Switch (1N914)
2. Part Manufacturer: Raytheon Co., Semiconductor Div.
3. Part Number: 772932
4. Date Code: 7526

B. PACKAGE

1. Type: 3-Lead, TO-18 (Drawing No. 757432)
2. Weight: 0.312 gram
3. Materials:

   a) Cap: Steel
   b) Header: Kovar, gold-plated
   c) Leads: Kovar, gold-plated
   d) Cap Seal: Weld
   e) Lead Seal: Glass

C. INTERNAL GOEMETRY

1. Interconnections: Beam leads bonded to gold-plated header

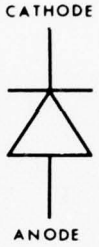
2. Die:

   a) Type: Silicon, planar (Beam Lead)
   b) Scribe Method: Etch
   c) Dimensions: 0.0023 inch X 0.0023 inch
   d) Passivation: Silicon Nitride over Silicon Dioxide

3. Metallization Type: Gold/Titanium/Platinum

3.8X

FIGURE L1. EXTERNAL CONSTRUCTION - P/N 772932 - GENERAL PURPOSE SWITCH



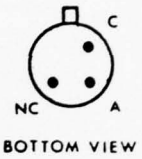
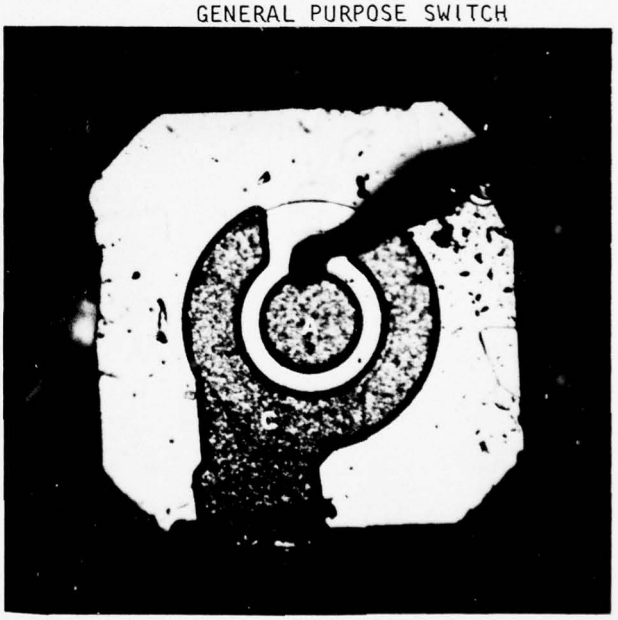


FIGURE L2. SYMBOL AND TERMINAL DIAGRAM - P/N 772932 - GENERAL PURPOSE SWITCH

37X

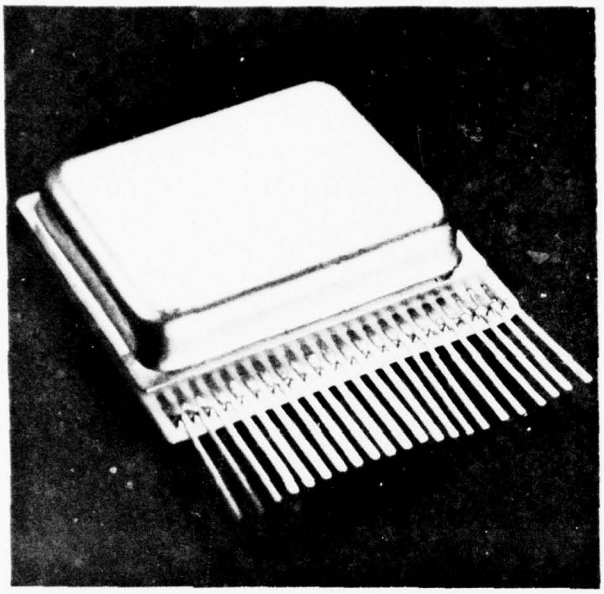
VIEW WITH LID REMOVED



132X

DIE TOPOGRAPHY

FIGURE L3. INTERNAL CONSTRUCTION DETAILS - P/N 772932 - GENERAL PURPOSE SWITCH

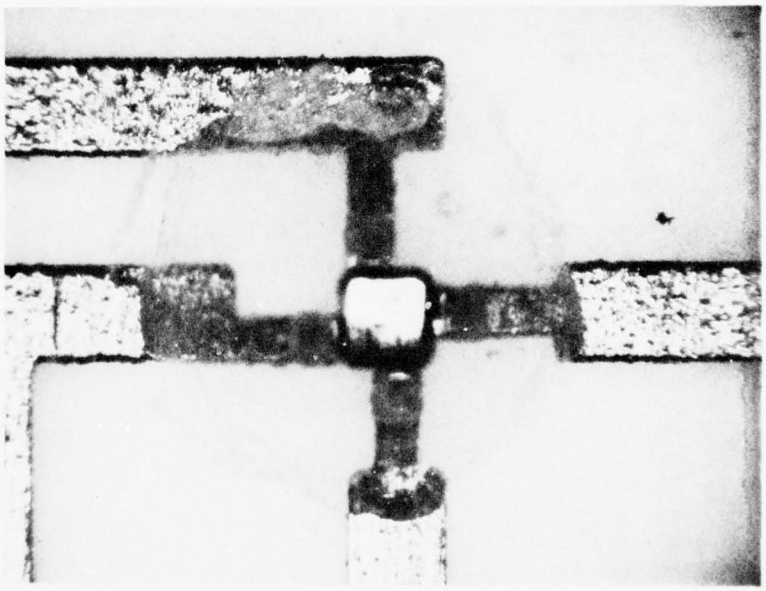


1.9X

EXTERNAL

1.9X

INTERNAL



30X

DIE MOUNTED IN SAM-D CONFIGURATION

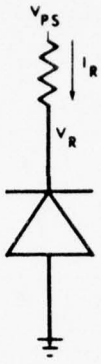
FIGURE L4. TYPICAL SAM-D CONFIGURATION - P/N 773382 - GENERAL PURPOSE SWITCH

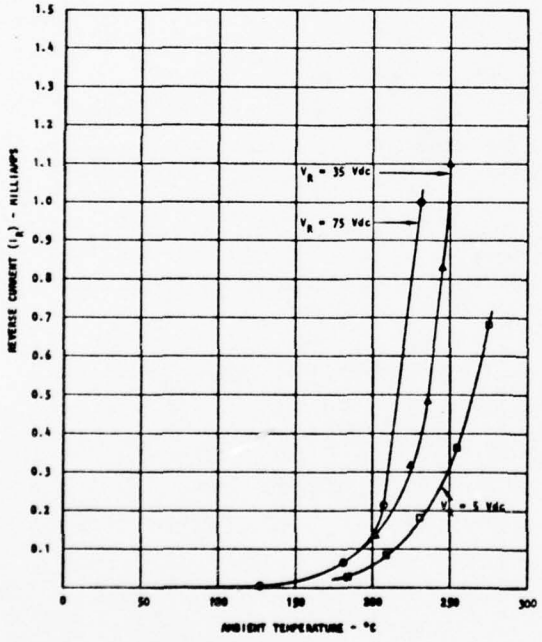
TABLE L2. ELECTRICAL TEST CONDITIONS - P/N 772932 - GENERAL PURPOSE SWITCH

TEST NO.	SYMBOL	MIL-STD-750	CONDITIONS	T_A=+25°C		T_A=+150°C		UNITS
				MIN	MAX	MIN	MAX	
1	V_F	4011	I_F = 10 mA	-	1.0	-	(2)	Vdc
2	$I_{R(1)}$	4016	V_R = 4.0 V	-	200	-	(2)	nA
3	$I_{R(2)}$	4016	V_R = 30 V (1)	-	(2)	-	50	µA
4	$I_{R(3)}$	4016	V_R = 60 V	-	(2)	-	(2)	
5	$I_{R(4)}$	4016	V_R = 100 V	-	100	-	(3)	µA

(1) V_R is 30V for T_A = +25°C test and 20V for T_A = +150°C test.
(2) Limits not specified by part drawing - Measurement made for information only.
(3) Test not performed at T_A = +150°C.

Initial and final test conducted at +25°C and +150°C. Interim test conducted at +25°C.





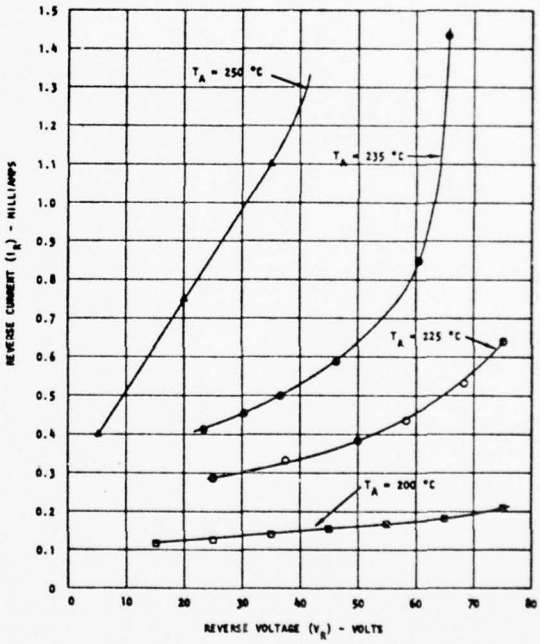
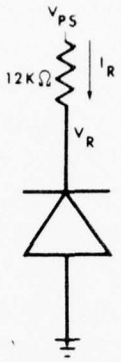


FIGURE L5. BIAS CIRCUIT EVALUATION - P/N 772932 - GENERAL PURPOSE SWITCH

STEP STRESS AND LIFE TEST CIRCUIT



STEP STRESS TEST - FAILURE SUMMARY (20 DEVICES)

AMBIENT TEMP. (°C)	V_R(V)	CUMULATIVE FAILURES
175	+75	0
200	+75	0
225	+75	0
250 ⚠1	+35	0

⚠1 V_R was 75 Vdc for 175°C, 200°C and 225°C steps. For the 250°C step, V_R was reduced to 35 Vdc because the device would have gone into thermal runaway at 75 Vdc.

LIFE TEST CONDITIONS

TEST CELL NUMBER	T_A AMBIENT TEMPERATURE (°C)	V_R REVERSE VOLTAGE (VOLTS)	I_R REVERSE CURRENT (MILLIAMPS)	P_d POWER DISSIPATION (MILLIWATTS)	T_J JUNCTION TEMPERATURE (°C)
1	250	35	1.1	39	262
2	250	20	0.7	14	254
3	250	5	0.4	2	251
4	250	0	0	0	250
5	225	35	0.3	11	228

FIGURE L6. STEP STRESS RESULTS AND LIFE TEST CONDITIONS - P/N 772932 - GENERAL PURPOSE SWITCH

L6.0 LIFE TEST CONDITIONS AND RESULTS

The accelerated life test conditions are included in Figure L6. As summarized in Table L3, the life test proceeded for 4000 hours during which only five failures were observed.

L7.0 FAILURE ANALYSIS

Table L4 is a summary of the failure analysis results.

Surface Instability Failures - Two diodes exhibited excessive $I_{R(4)}$ due to low breakdown voltage. $I_{R(4)}$ is measured at V_R = 100V and, as shown in Figure L7, the reverse breakdown voltage of both diodes (68V and 80V) was less than 100 volts. Both devices completely recovered after baking. $I_{R(4)}$ of each part improved to one microampere and their breakdown voltages increased to 120 volts. Thus, these failures were attributed to a surface instability mechanism, most likely mobile ion drift in the field of the reverse biased junction, caused by contamination in or on the SiO_2/Si_3N_4 insulators.

Test Error - Three diodes failed V_F due to an open internal beam lead. In each instance, the lead had melted open and the die was severely damaged, as illustrated in Figure L8, indicative of electrical overstress. Since all three failures occurred at the same test point, 16 hours, the overstress was probably caused by an accidental overvoltage or overload during the parametric measurements.

L8.0 DATA CORRELATION

The Table L4 Failure Analysis Summary identifies electrical overstress as the cause of three of the five total test failures, and are therefore not applicable for data analysis. The two remaining failures, excessive I_R (Reverse Leakage) attributable to mobile ion drift, are insufficient for failure distribution analysis.

Parameter trends were evaluated and found to be inconclusive. The I_R, reverse leakage, parameters in the powered cells were increasing, but at test completion the maximum average value for any test cell was only 1 μA, as opposed to a limit of 100 μA (Table L2). Cell 4, the unpowered cell at 250°C, displayed no obvious trend. Two Cell 4 parameters, V_F, the forward voltage drop, and $I_{R(3)}$ are plotted in Figure L9. The relatively large mean value changes in $I_{R(3)}$ are attributed to

TABLE L3. LIFE TEST SUMMARY - P/N 772932 - GENERAL PURPOSE SWITCH

TEST CELL DESCRIPTION				CUMULATIVE FAILURES AT HOURS OF TEST										
CELL NO	APPLIED BIAS	AMBIENT TEMP.	QUANTITY	4	8	16	32	64	128	256	512	1000	2500	4000
1	35 VDC	250°C	30	0	0	1	1	1	1	1	1	1	1	1*
2	20 VDC	250°C	30	0	0	1	1	1	1	1	1	1	1	2*
3	5 VDC	250°C	30	0	0	0	0	0	0	0	0	0	0	0*
4	0 VDC	250°C	30	0	0	0	0	0	0	0	0	0	0	0*
5	35 VDC	225°C	30	0	0	1	1	1	1	1	1	1	1	2*

* TEST TERMINATED

TABLE L4. FAILURE ANALYSIS SUMMARY - P/N 772932 - GENERAL PURPOSE SWITCH

	A. FAILED PARAMETERS OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TIME (HOURS) OF FAILURE				
		250°C				225°C
		35 V	20 V	5 V	0 V	35 V
		CELL 1	CELL 2	CELL 3	CELL 4	CELL 5
SURFACE INSTABILITY	A. $I_{R(4)}$ B. LOW BREAKDOWN VOLTAGE C. MOBILE ION DRIFT D. PASSIVATION CONTAMINATION		1@4000			1@4000
TEST ERROR	A. V_F B. MELTED OPEN BEAM C. ELECTRICAL OVERSTRESS D. OVER VOLTAGE OR OVERLOAD	1@16	1@16			1@16
	TOTAL NUMBER OF FAILED PARTS	1	2	0	0	2

AD-A039 788 MCDONNELL DOUGLAS ASTRONAUTICS CO-EAST ST LOUIS MO F/G 9/1
STORAGE RELIABILITY OF MISSILE MATERIEL (ACCELERATED TESTING OF--ETC(U)
APR 77 J MCGARRY, V WEISSFLUG, E SISUL DAAH01-74-C-0928
UNCLASSIFIED MDC-E1601 NL

4 OF 5
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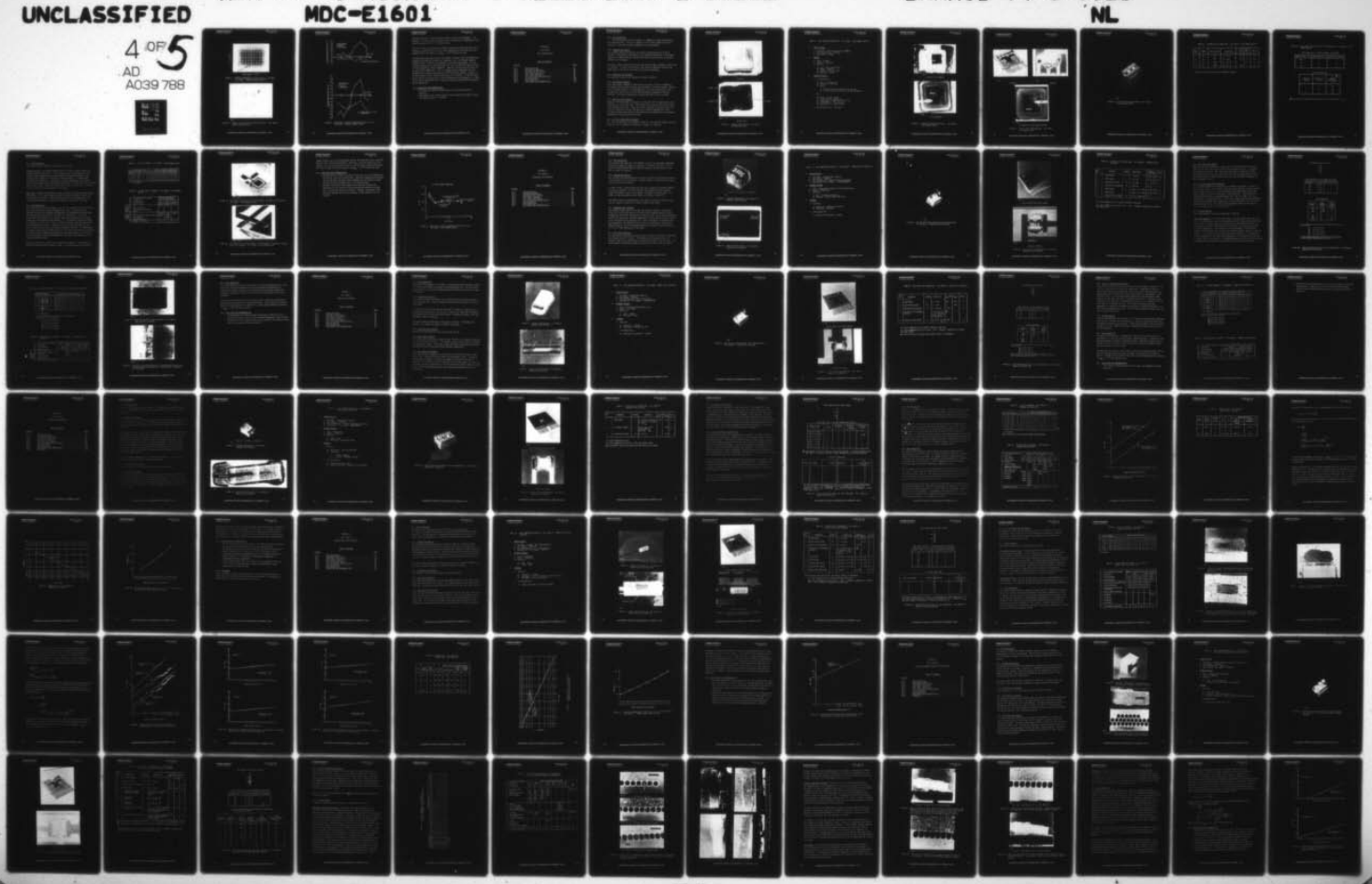
A039 788



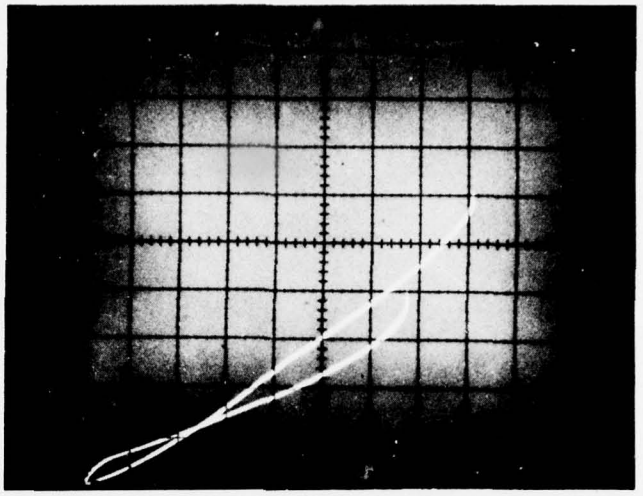


FIGURE L7. REVERSE CHARACTERISTIC OF THE TWO $I_{R(4)}$ FAILURES - P/N 772932 - GENERAL PURPOSE SWITCH

105X

FIGURE L8. EXAMPLE OF THE DAMAGE SUSTAINED BY THE DIE - P/N 772932 - GENERAL PURPOSE SWITCH

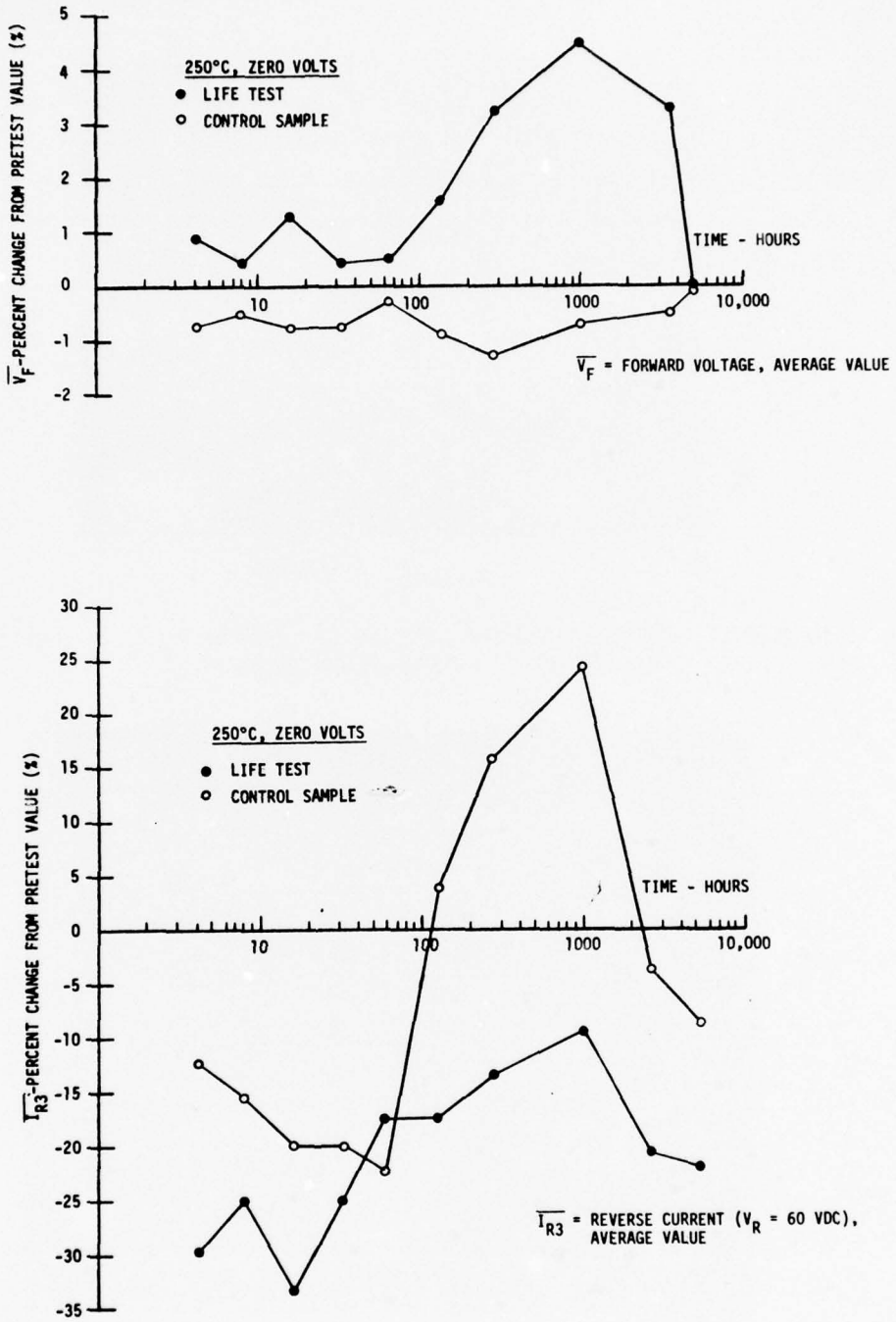


FIGURE L9. BEHAVIOR OF SELECTED PARAMETERS DURING LIFE TEST - P/N 772932 - GENERAL PURPOSE SWITCH

inherent variations in measuring test currents as low as 10 nanoamperes. The decrease in V_F at the end of the test is not an indication of a degradation trend since the parameter limit is a positive value.

The lack of both test failures and parameter degradation trends precludes calculation of a storage failure rate, but does indicate that this diode has a high storage reliability potential ($\lambda(t)_{MAX} << 10^{-10}$ failures per hour).

The preliminary part specification, P/N 772932, includes a 100% High Temperature Reverse Bias (HTRB) test at 300°C for 168 hours, with a 10% Percent Defective Allowable (PDA). Failures are determined by end point measurements. The two failures detected during the accelerated life test show that this device can have a surface instability failure mechanism. These two failures both occurred late in test (2500 to 4000 hours). The lot acceptance data accompanying the part shipment do not reflect performance of a 300°C HTRB test; however, a sample of 45 parts passed a 150°C, 168 hour HTRB test with no failures. If the test parts were a typical lot, there was no "freak" population to be screened out. In light of the high allowable PDA (10%), a review of the specification HTRB requirements may be appropriate.

L9.0 CONCLUSIONS AND RECOMMENDATIONS

- This beam lead diode has demonstrated a high storage reliability potential.
- The production part HTRB screening criteria should be reviewed to ensure the appropriateness of a 10% PDA.

APPENDIX M

P/N 773053

HIGH CURRENT SWITCH

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M1.0 PART DESCRIPTION

The High Current Switch, P/N 773053, is a 1N4942 type diode manufactured by Unitrode Corporation. The die is mounted in a "Pill-Box" package as shown in Figure M1. Leads were attached by MDAC-East for test purposes.

M2.0 CONSTRUCTION ANALYSIS

The pertinent construction details for the test configuration are listed in Table M1. Figure M2 provides details of the internal construction. The cathode connection is made by the gold eutectic bond used to attach the die to the gold conductor of the package.

The typical SAM-D configuration utilizes the same "Pill-Box" package as illustrated in Figure M3. In order to electrically test the parts MDAC-East installed the leads shown in the Figure M4 picture of the test configuration.

M3.0 ELECTRICAL TEST CRITERIA

The electrical tests for this device are listed in Table M2.

M4.0 BIAS CIRCUIT ANALYSIS

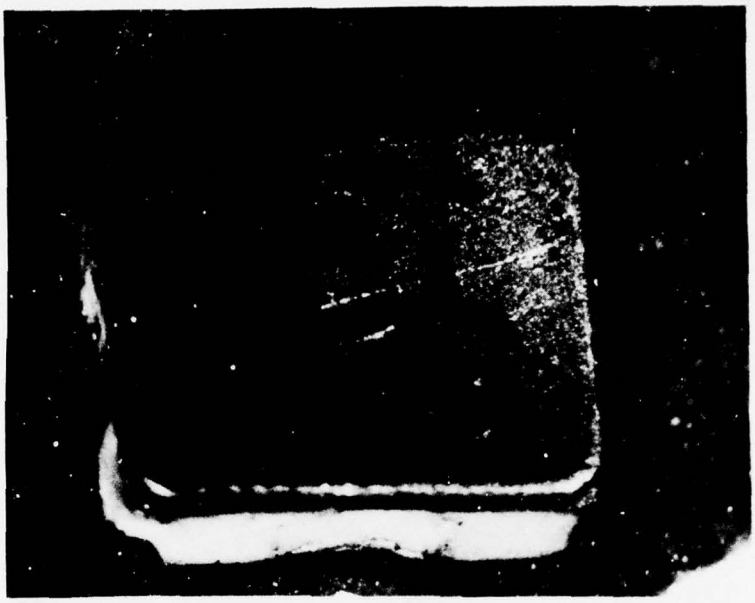
Since the original shipment of these devices was lost in transit to MDAC-East, only eighty-three devices ultimately were available for the test program. Because of this reduced quantity, it was decided that a life test consisting of three storage cells (zero volts) at three different ambient temperatures would be performed. The ambient temperatures selected were 225°C, 250°C, and 275°C.

M5.0 STEP STRESS TEST RESULTS

Because of the small number of devices, only 6 parts, with no applied bias, were subjected to a step stress test. Three sixteen hour steps at 225°C, 250°C and at 275°C produced no failures. Table M3 contains a summary of the step stress test. Sixty-four additional failure free hours at an ambient temperature of 275°C provided confidence that the test configuration was non-destructive and therefore acceptable for the accelerated life test.

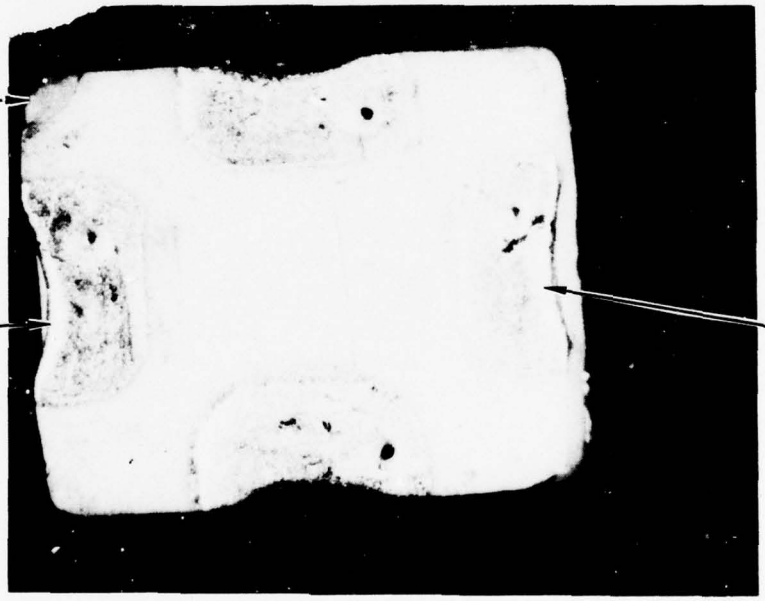
M6.0 LIFE TEST CONDITIONS AND RESULTS

The life test conditions are included in Table M3. The Table M4 summary shows the three test cells proceeded for 4000 hours, producing 31 failures.



20X

TOP VIEW



20X

BOTTOM VIEW

FIGURE M1. EXTERNAL CONSTRUCTION - P/N 773053 - HIGH CURRENT SWITCH

TABLE M1. PART CONSTRUCTION DETAILS - P/N 773053 - HIGH CURRENT SWITCH

A. IDENTIFICATION

1. Part Name: High Current Switch (1N4942)
2. Part Manufacturer: Unitrode
3. Part Number: 773053

B. PACKAGE

1. Type: Pill-Box
2. Weight: 0.066 gram
3. Material:

   a) Lid: Kovar, gold-plated
   b) Header: Ceramic
   c) Leads: Thick Film Gold
   d) Cap Seal: Solder

C. INTERNAL GEOMETRY

1. Interconnections:

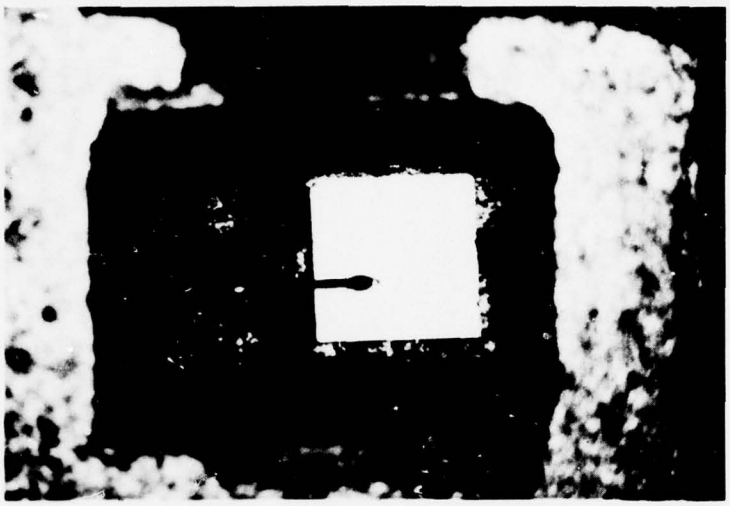
   a) Type: Aluminum Wire
   b) Diameter: 0.002 inch
   c) Bonds:

      1) Aluminum-aluminum ultrasonic at the die
      2) Aluminum-gold ultrasonic at the gold conductors

2. Die:

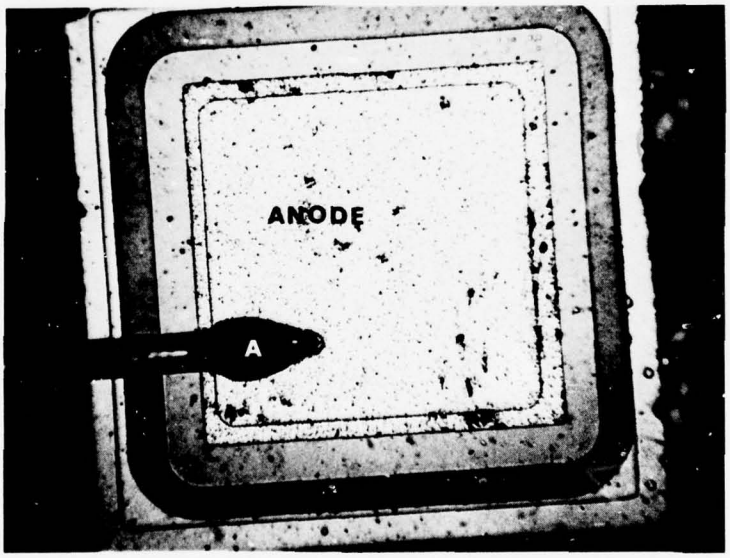
   a) Type: Silicon, planar
   b) Scribe Method: Mechanical
   c) Dimensions: 0.032 inch X 0.032 inch
   d) Attach Method: Gold Eutectic
   e) Passivation: Silicon Dioxide

3. Metallization Type: Aluminum



57X

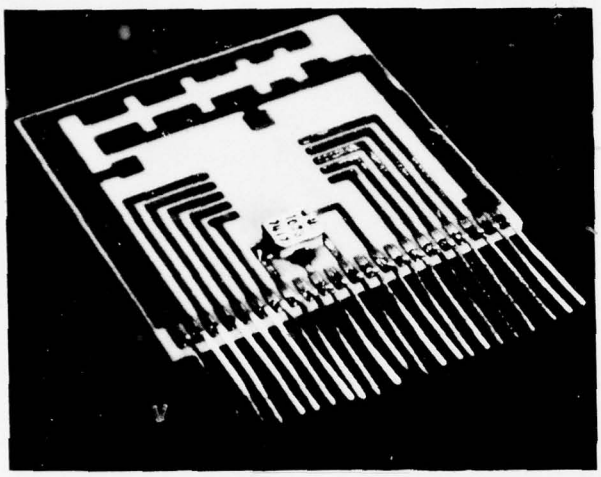
VIEW WITH LID REMOVED



105X

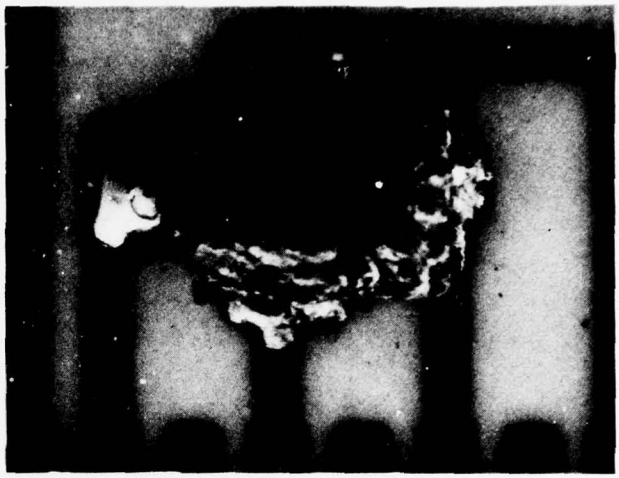
DIE TOPOGRAPHY

FIGURE M2. INTERNAL CONSTRUCTION DETAILS - P/N 773053 - HIGH CURRENT SWITCH



1.9X

EXTERNAL



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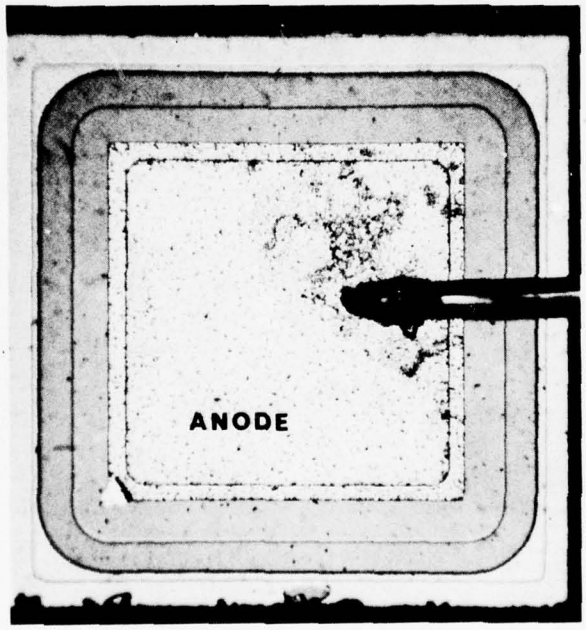
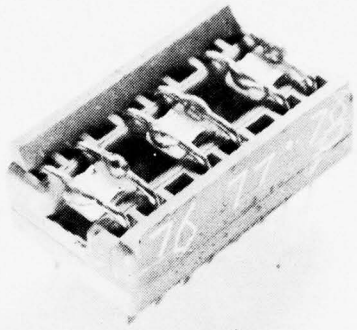
INTERNAL



105X

DIE MOUNTED IN SAM-D CONFIGURATION

FIGURE M3. TYPICAL SAM-D CONFIGURATION - P/N 773344 - HIGH CURRENT SWITCH



2.3X

FIGURE M4. DEVICES WITH LEADS ATTACHED - P/N 773053 - HIGH CURRENT SWITCH

TABLE M2. ELECTRICAL TEST CONDITIONS - P/N 773053 - HIGH CURRENT SWITCH

TEST NO.	SYMBOL	MIL-STD-750	CONDITIONS	T_A = +25°C		UNITS
				MIN	MAX	
1	V_{F1}	4011	I_F = 1.0A	0.6	1.3	Vdc
2	V_{F2}	4011	I_F = 0.5A	0.6	1.3	Vdc
3	I_R	4016	V_R = 75 Vdc	-	1.0	µA
4	BV	4021	I_R = 50 µA	100	-	Vdc

Initial, final and interim test conducted at +25°C.

TABLE M3. STEP STRESS RESULTS AND LIFE TEST CONDITIONS - P/N 773053 - HIGH CURRENT SWITCH

STEP STRESS TEST - FAILURE SUMMARY (6 DEVICES)

AMBIENT TEMP. (°C)	APPLIED BIAS (V)	CUMULATIVE FAILURES
225	0	0
250	0	0
275	0	0

LIFE TEST CONDITIONS

TEST CELL NUMBER	APPLIED BIAS (VOLTS)	T_A ⚠1 AMBIENT TEMPERATURE (°C)
1	0	275
2	0	250
3	0	225

⚠1 All cells are storage (without bias) cells and therefore, $T_A = T_J$.

M7.0 FAILURE ANALYSIS

The failure analysis results are summarized in Table M5.

Wire-to-Die Short - Two diodes exhibited excessive reverse leakage current (I_R) traced to a wire-to-die short. In each instance, due to poor lead dress, the internal anode aluminum lead wire had contacted the unpassivated edge of the substrate (the cathode) as illustrated in Figure M5 and M6. Lifting the wire eliminated the excessive I_R. Insufficient clearance between the wire and the edge of the die appears to be an inherent design flaw. Examination of the unstressed construction analysis sample, the three control samples, and ten Cell 3 survivors disclosed that all 14 parts contained no wire loop.

Open Leads - Twenty-nine (29) diodes failed V_F traced to resistive or open external solder joints. A tin-based solder was used to attach the external leads to the gold package mounting pads. After prolonged exposure to high temperature, the joints deteriorated due to scavenging or leaching of the gold by the solder.

M8.0 DATA CORRELATION

The Table M5 failure analysis summary shows only two applicable life test failures, both involving excessive reverse leakage current (I_R). The balance of the reported failures were attributed to degradation of the MDAC-East attached leads and, therefore, not applicable to the SAM-D use configuration. The two I_R failures were both caused by the internal anode lead wire contacting the unpassivated edge of the substrate (the cathode). As illustrated in Figures M5 and M6, the lead dress for this wire is flat, providing a marginal clearance between the wire and the edge of the die. Examination of 16 parts revealed that this wire dress is typical and not just an isolated workmanship variation. The combination of the two failures and the identification of the marginal lead dress are sufficient to warrant further temperature/temperature cycling investigation of this design. This investigation could yield recommendations for design modifications or a lot temperature screening test.

The two I_R failures are insufficient for statistical analysis. Investigation of electrical parameter data revealed no trends. The average value of the reverse

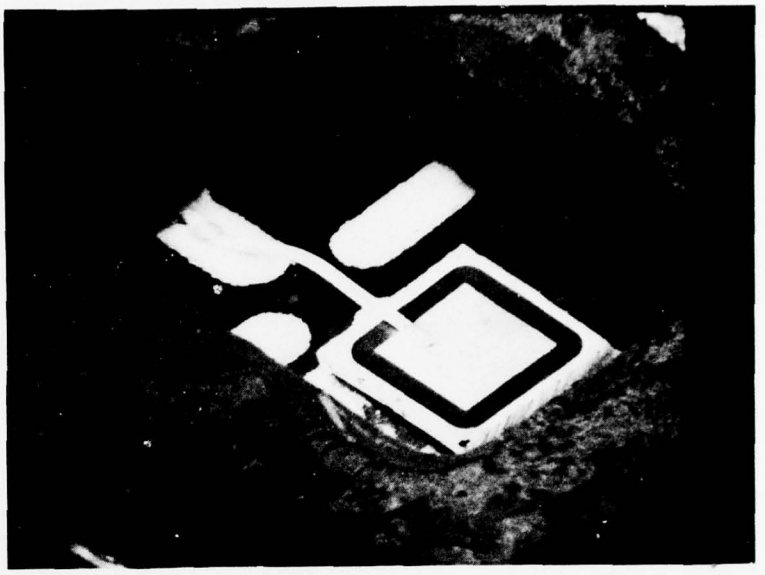
TABLE M4. LIFE TEST SUMMARY - P/N 773053 - HIGH CURRENT SWITCH

TEST CELL DESCRIPTION				CUMULATIVE FAILURES AT HOURS OF TEST										
CELL NO	APPLIED BIAS	AMBIENT TEMP	QUANTITY	4	8	16	32	64	128	256	512	1000	2504	4000
1	0 VDC	275°C	30	0	0	0	0	0	0	0	1	1	14	22*
2	0 VDC	250°C	27	0	0	0	0	0	0	1	1	1	7	8*
3	0 VDC	225°C	15	0	0	0	0	0	0	0	0	0	0	1*

* TEST TERMINATED

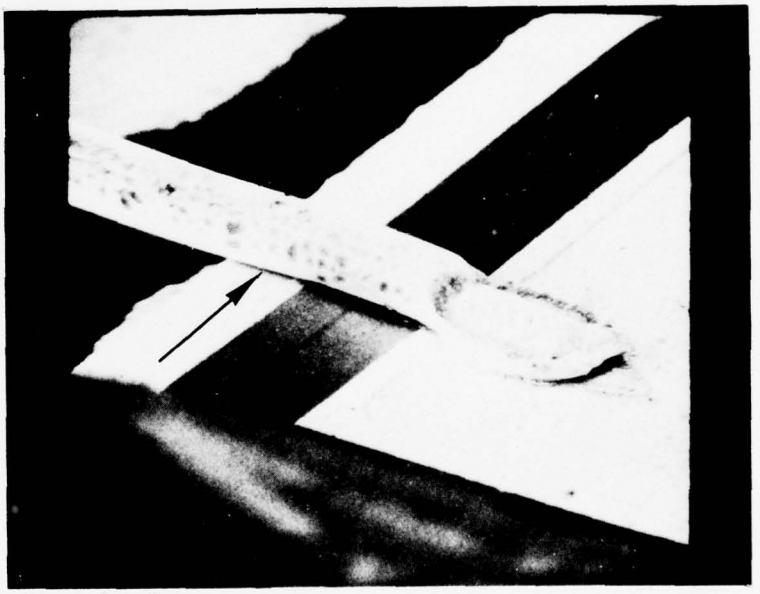
TABLE M5. FAILURE ANALYSIS SUMMARY - P/N 773053 - HIGH CURRENT SWITCH

	A. FAILED PARAMETERS OF SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TIME (HOURS OF FAILURE) 0V 275°C CELL 1	250°C CELL 2	225°C CELL 3
MECHANICAL FAILURES	A. I_R B. WIRE TO DIE SHORT C. POOR LEAD DRESS AND WIRE SAG D. DESIGN	1@512	1@256	
TEST CONFIG. FAILURE	A. V_F B. OPEN OR RESISTIVE EXTERNAL SOLDER JOINT C. GOLD SCAVENGING D. SOLDER COMPOSITION	13@2504 8@4000	1@1000 5@2504 1@4000	1@4000
	TOTAL NUMBER OF FAILED PARTS	22	8	1



30X (SEM)

FIGURE M5. SEM PHOTO OF INTERIOR OF THE DIODE SHOWING THE ANODE WIRE LEAD DRESS - P/N 773053 - HIGH CURRENT SWITCH



200X (SEM)

FIGURE M6. SEM CLOSE-UP OF THE WIRE SHOWING THE POINT WHERE IT CONTACTED THE EDGE OF THE DIE (ARROW) - P/N -773053 - HIGH CURRENT SWITCH

leakage current (I_R) at each measurement time for the three test cells, Figure M7, shows no signs of obvious degradation. Therefore, no failure times were extrapolated. The lack of sufficient failures for analysis would indicate this device has a high storage reliability potential ($\lambda(t)_{MAX} << 10^{-10}$ failures per hour).

M9.0 CONCLUSIONS AND RECOMMENDATIONS

- The possibility of lead to die shorts can be a lot to lot variable due to the marginal lead dress configuration. Additional temperature evaluations (using temperature and power) are recommended for this design to assess the need for design changes and/or a lot screening test.
- Although insufficient failure data was available for failure rate quantification, the few test failures encountered indicate this diode has a high storage reliability potential. However, the marginal lead dress configuration must be fully assessed if this potential is to be realized.

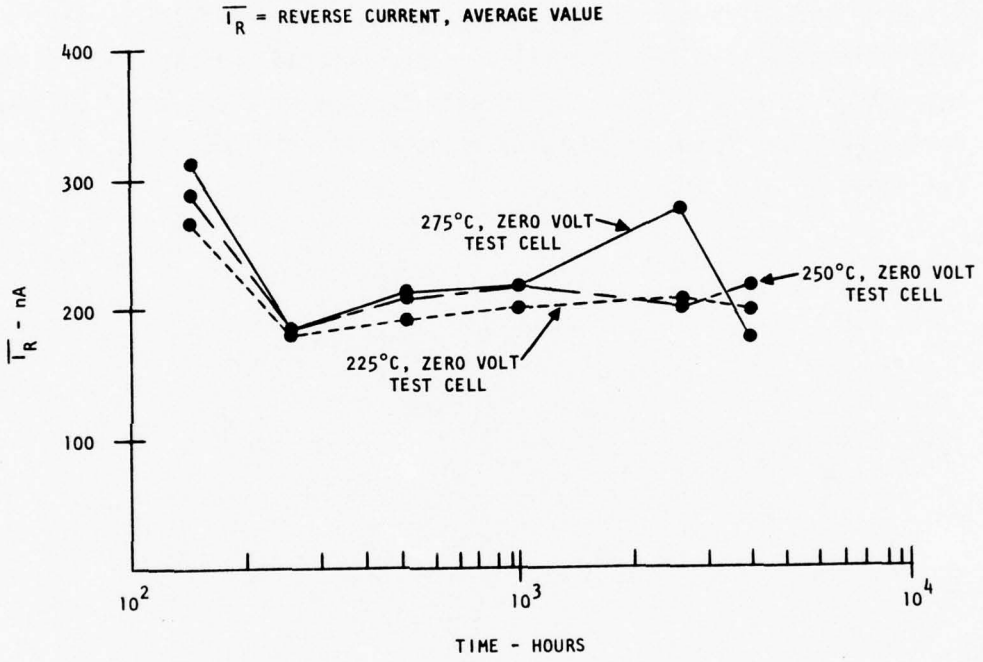


FIGURE M7. BEHAVIOR OF SELECTED PARAMETERS DURING LIFE TEST - P/N 773053 - HIGH CURRENT SWITCH

APPENDIX N

P/N 773054-21

PORCELAIN CHIP CAPACITOR

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N1.0 PART DESCRIPTION

The Porcelain Chip Capacitor, P/N 773054-21, consists of noble metal electrodes molecularly bonded and sealed in a monolith of nonporous porcelain. The test devices, manufactured by American Technical Ceramics, were delivered in chip form, as shown in Figure N1.

N2.0 CONSTRUCTION ANALYSIS

The pertinent construction details are listed in Table N1, and Figure N2 shows a cross sectional view of the device. The part contains no materials which would limit the testing below 300°C.

In order to apply voltages during the life test, a method for attaching leads to the chip was required. Of several methods investigated, the best utilized 0.060 inch diameter nickel wire soldered to the chips with 309°C solder. An example of devices mounted in this manner is provided in Figure N3.

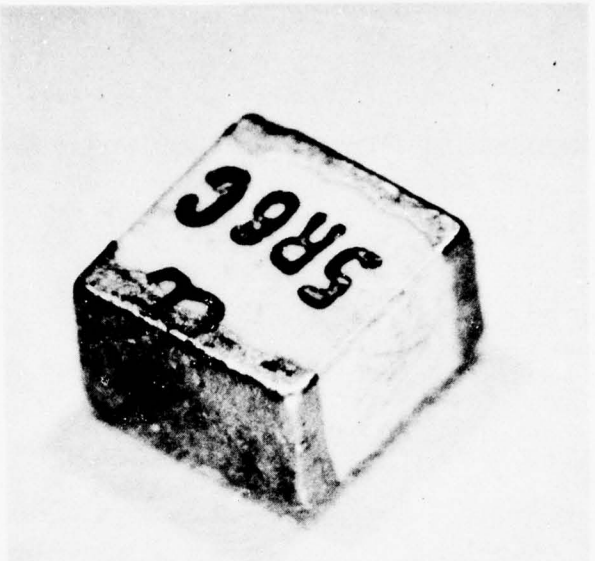
The typical SAM-D use configuration of this device, pictured in Figure N4, has the chip capacitor soldered to a ceramic printed circuit board.

N3.0 ELECTRICAL TEST CRITERIA

The electrical tests used for this part are listed in Table N2. Dissipation factor (DF) could not be used as a failure criterion because almost all parts exceeded the limit after installation of the test leads. DF was measured throughout the test program and although a degradation was experienced, the cause could not be attributed to the capacitor chip. Once a chip began to experience test lead degradation, the repeatibility of the DF test became poor. However the measured values of DF did not become excessive and almost all parts ranged from 10^{-3} to 10^{-4} after 6000 hours of life tests.

N4.0 BIAS CIRCUIT ANALYSIS

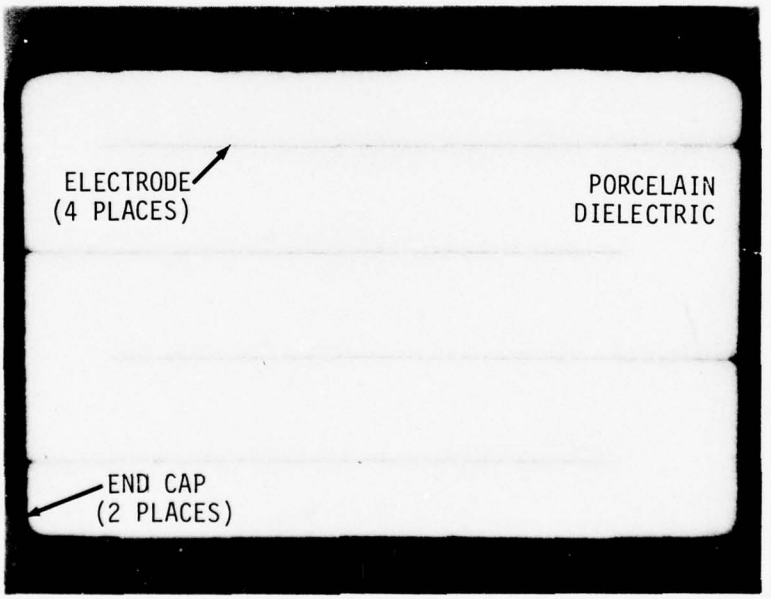
The test device was operated at rated voltage, 500 VDC, as the ambient temperature was elevated from 25°C to 250°C. The leakage current remained below .5 μA. Therefore, 500 VDC was established as the maximum voltage in the life test. The maximum ambient temperature tentatively selected for the life test was 250°C.



0.117 in. x 0.117 in. x 0.075 in.

10X

FIGURE N1. EXTERNAL CONSTRUCTION - P/N 773054-21 - PORCELAIN CHIP CAPACITOR



37X

FIGURE N2. CROSS SECTION OF DEVICE - P/N 773054-21 - PORCELAIN CHIP CAPACITOR

TABLE N1. PART CONSTRUCTION DETAILS - P/N 773054-21 - PORCELAIN CHIP CAPACITOR

A. IDENTIFICATION

1. Part Name: Porcelain Chip Capacitor
2. Part Number: 773054-21
3. Part Manufacturer: Americal Technical Ceramics
4. Manufacturer's Part Number: ATC-100B5R6CP500

B. EXTERNAL PACKAGE

1. Type: Hermetically sealed, self-encapsulated chip
2. Weight: 0.583 grams
3. Materials:

   a) Body: Non-Porous Porcelain
   b) End Caps: 20% Palladium, 80% Silver

C. INTERNAL

1. Materials:

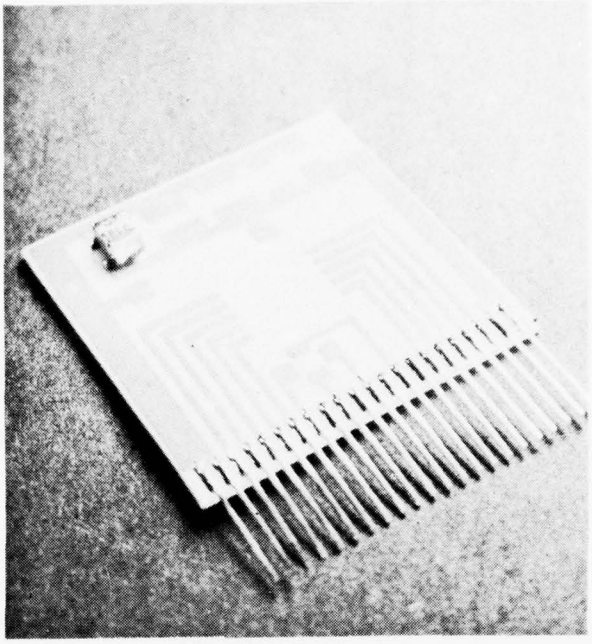
   a) Dielectric: Non-Porous Porcelain
   b) Electrode: Palladium

2. Interconnections:

   a) End Cap to Electrode: Sintered

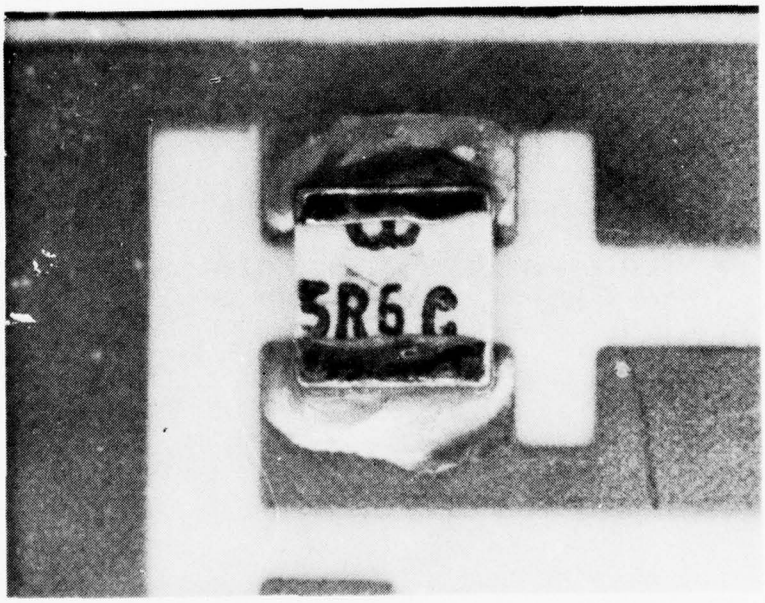
1.6X

FIGURE N3. DEVICES WITH LEADS ATTACHED (TEST CONFIGURATION) - P/N 773054-21 - PORCELAIN CHIP CAPACITOR



1.9X

DEVICE MOUNTED ON CIRCUIT BOARD



10X

CLOSE-UP OF DEVICE

FIGURE N4. TYPICAL SAM-D CONFIGURATION - P/N 772935 - PORCELAIN CHIP CAPACITOR

TABLE N2. ELECTRICAL TEST CONDITIONS - P/N 773054-21 - PORCELAIN CHIP CAPACITOR

TEST NO.	PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
				MIN	MAX	
1	CAPACITANCE	C	f = 1.0 MHz	5.35	5.85	pf.
2	CAPACITANCE	C	f = 0.5 MHz	5.35	5.85	pf.
3	DISSIPATION FACTOR	DF	f = 0.5 MHz	-	10^{-4}	-
4	INSULATION RESISTANCE	IR	V = 500 Vdc	10^6	-	Ω
5	CAPACITANCE	C	T_A=-55°C, f=1.0 MHz	5.35	5.85	pf.
6	CAPACITANCE	C	T_A=125°C, f=1.0 MHz	5.35	5.85	pf.
7	INSULATION RESISTANCE	IR	T_A=125°C, V=500 Vdc	10^6	-	Ω

ALL TESTS CONDUCTED AT 25°C UNLESS OTHERWISE SPECIFIED.

ALL TESTS CONDUCTED FOR INITIAL TEST. TESTS 1 THROUGH 4 CONDUCTED FOR INTERIM AND FINAL TESTS.

N5.0 STEP STRESS TEST RESULTS

Twenty devices were subjected to a step stress test consisting of four 16 hour steps at 25°C intervals starting at 200°C and concluding at 275°C. The devices were biased with 500 VDC. The Figure N5 summary shows five marginal failures were generated during the step stress test, all occurring after the 275°C step. These test conditions (250°C maximum at 500 VDC) were considered acceptable for the accelerated life test.

N6.0 LIFE TEST CONDITIONS AND RESULTS

The life test conditions for each cell are included in Figure N5. As shown in the Table N3 summary, the life tests continued to the 6000 hour readout; however, after 256 hours, Cells 1, 2, and 3 experienced severe degradation of the lead attach solder, resulting in some cases in lead separation. These three cells continued the life test as unbiased storage cells, Cell 1 at 285°C, Cell 2 at 225°C and Cell 3 remained at 250°C. Cells 4 and 5 experienced the same degradation at 1000 hours and 2500 hours respectively, and were continued in the life test as unbiased storage cells. Five failures were generated during the life test of which four were from Cell 2 and one from Cell 3.

N7.0 FAILURE ANALYSIS

The failure analysis results are summarized in Table N4.

Capacitance Decrease - Five parts failed due to low capacitance during the life test. The capacitance of each part had decreased only slightly during accelerated life and was only about one or two picofarads below the specified minimum limit at the time of failure. Metallurgical cross-sections of failed parts disclosed no sign of degradation in the dielectric or the electrodes of the capacitors. However, the palladium-silver end caps were severely voided as shown in Figures N6 and N7. It is believed that the voids caused discontinuities in the connection to the electrodes and this reduced the capacitance. A tin-based solder was used to attach leads to the end caps. At elevated temperature, the silver was scavenged or leached from the end caps by the solder resulting in the observed voids.

STEP STRESS AND LIFE TEST CIRCUIT

STEP STRESS RESULTS - FAILURE SUMMARY (20 DEVICES)

AMBIENT TEMP. (°C)	V_{PS} (V)	CUMULATIVE FAILURES
200°C	500	0
225°C	500	0
250°C	500	0
275°C	500	5

LIFE TEST CONDITIONS

TEST CELL NUMBER	T_A AMBIENT TEMPERATURE (°C)	V_{PS} DEVICE VOLTAGE (VOLTS)
1 ⚠1	250 ⚠1	500
2 ⚠2	250 ⚠2	375
3	250	0
4 ⚠3	225	500
5 ⚠4	200	500

DUE TO LEAD DEGRADATION, THE FOLLOWING TEST CELLS BECAME ZERO VOLTAGE CELLS AT THE TIMES INDICATED.

⚠1 0 Vdc, 285°C, 256 HRS.

⚠2 0 Vdc, 225°C, 256 HRS.

⚠3 0 Vdc, 225°C, 1000 HRS.

⚠4 0 Vdc, 200°C, 2500 HRS.

THE DEVICE CURRENT DOES NOT EXCEED .5 μA REPRESENTING A DISSIPATION OF .25 mW. THIS POWER DISSIPATION CAUSES A NEGLIGIBLE TEMPERATURE RISE. T_{IMAX} (MAXIMUM INTERNAL TEMPERATURE) IS THEREFORE TAKEN TO BE EQUAL TO T_A.

FIGURE N5. STEP STRESS RESULTS AND LIFE TEST CONDITIONS - P/N 773054-21 - PORCELAIN CHIP CAPACITOR

TABLE N3. LIFE TEST SUMMARY - P/N 773054-21 - PORCELAIN CHIP CAPACITOR

TEST CELL DESCRIPTION				CUMULATIVE FAILURES AT HOURS OF TEST												
CELL NO	APPLIED BIAS	AMBIENT TEMP.	QUANTITY	4	8	16	32	64	128	256	384	512	1000	2500	4000	6000
1	500 VDC	250°C ⚠1	30	0	0	0	0	0	0	0	0	0	0	0	0	0*
2	375 VDC ⚠2	250°C ⚠2	30	0	0	0	1	1	1	1	2	2	2	2	2	4*
3	0 VDC	250°C	30	0	0	0	0	0	0	0	0	0	1	1	1	1*
4	500 VDC ⚠3	225°C	30	0	0	0	0	0	0	0	-	0	0	0	0	0*
5	500 VDC ⚠4	200°C	30	0	0	0	0	0	0	0	-	0	0	0	0	0*

* TEST TERMINATED

DUE TO LEAD DEGRADATION, THE FOLLOWING TEST CELLS BECAME ZERO VOLTAGE CELLS AT THE TIMES INDICATED:

⚠1 0 VDC, 285°C, 256 HOURS

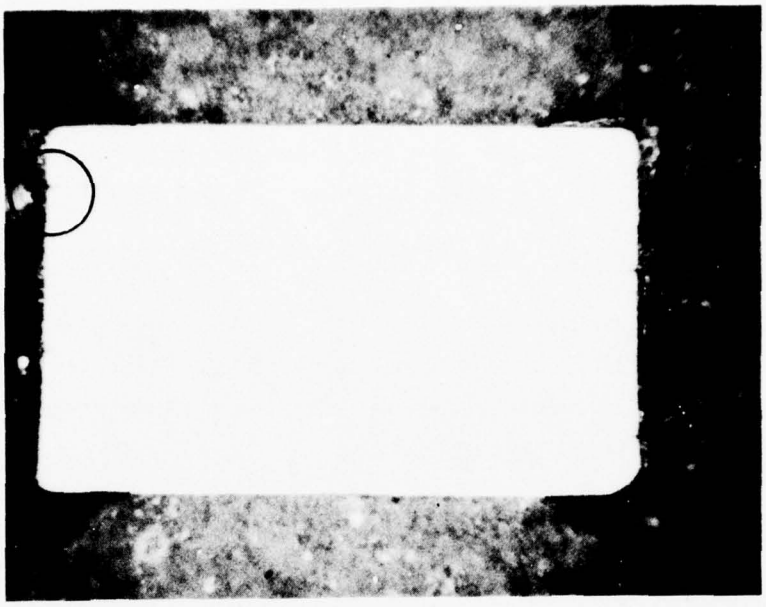
⚠2 0 VDC, 225°C, 256 HOURS

⚠3 0 VDC, 225°C, 1000 HOURS

⚠4 0 VDC, 200°C, 2500 HOURS

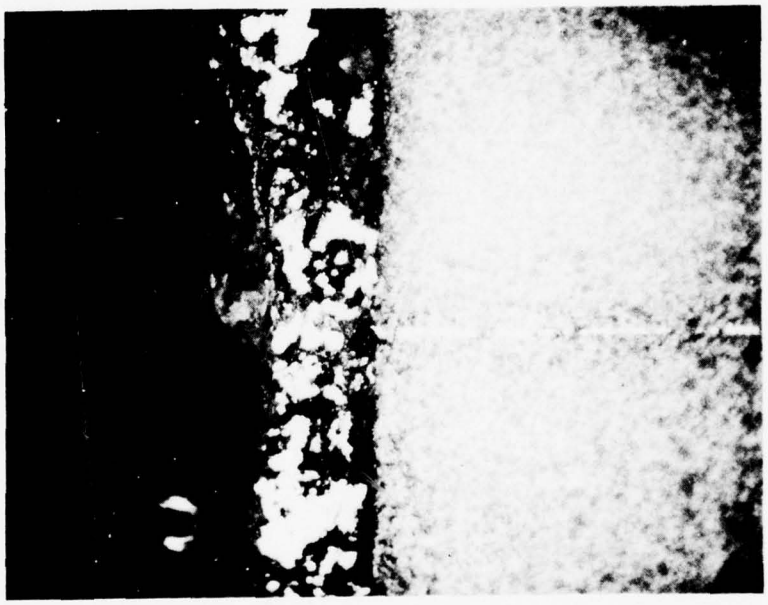
TABLE N4. FAILURE ANALYSIS SUMMARY - P/N 773054-21 - PORCELAIN CHIP CAPACITOR

	A. FAILED PARAMETER OR SYMPTOMS	QUANTITY OF FAILURES AND TIME (HOURS) OF FAILURE				
	B. FAILURE MODE	250°C			225°C	200°C
	C. FAILURE MECHANISM	500 V	375 V	0 V	500 V	500 V
	D. CAUSE OF FAILURE	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5
TEST CONFIGURATION FAILURES	A. CAPACITANCE (TOO LOW)		1@32	1@1000		
	B. DISCONTINUITIES (OPENS) IN THE END CAPS.		1@384 2@6000			
	C. SILVER SCAVENGING					
	D. SOLDER COMPOSITION					
	TOTAL NUMBER OF FAILED PARTS	0	4	1	0	0



30X

FIGURE N6. CROSS SECTION OF A FAILED CAPACITOR - P/N 773054-21 - PORCELAIN CHIP CAPACITOR



200X

FIGURE N7. CLOSE-UP OF THE AREA ENCIRCLED IN FIGURE N6 SHOWING THE VOIDS IN THE PALLADIUM-SILVER END CAPS - P/N 773054-21 - PORCELAIN CHIP CAPACITOR

N8.0 DATA CORRELATION

The 5 capacitance failures are insufficient for failure distribution analysis and no obvious capacitance degradation trend existed among the unfailed parts. Although the average capacitance value decreased during the test program, the change was less than 2% and the results from the five test cells were indistinguishable.

Since most of the test program was conducted without voltage as an accelerator, the results are applicable to a storage environment. Even lacking sufficient DF data the results indicate this capacitor has a high storage reliability potential ($\lambda(t)_{MAX} << 10^{-10}$ failures per hour).

N9.0 CONCLUSIONS AND RECOMMENDATIONS

- o The accelerated life tests provided insufficient failures for failure distribution analysis and no obvious parameter degradation trends existed.
- o Although failure rate quantification is not possible, this capacitor should have a high storage reliability potential.

APPENDIX O

P/N 773055-6

CERAMIC CHIP CAPACITOR

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01.0 PART DESCRIPTION

The Ceramic Chip Capacitor, P/N 773055-6, contains noble metal electrodes sealed in a monolith of ceramic, providing a self-encapsulated chip. The test devices, manufactured by Union Carbide Corporation, were delivered in chip form, as shown in Figure 01.

02.0 CONSTRUCTION ANALYSIS

The pertinent construction details are listed in Table 01 and Figure 02 shows a cross sectional view. The part contains no materials which would limit testing below 300°C.

As with the porcelain chip capacitor discussed in Appendix N, leads had to be attached to this device for the life test. Nickel wire, 0.025 inch in diameter, was soldered to the device using 309°C solder. An example of devices with leads attached is shown in Figure 03.

The typical SAM-D configuration is pictured in Figure 04. The ceramic chip capacitor is soldered to a ceramic printed circuit board.

03.0 ELECTRICAL TEST CRITERIA

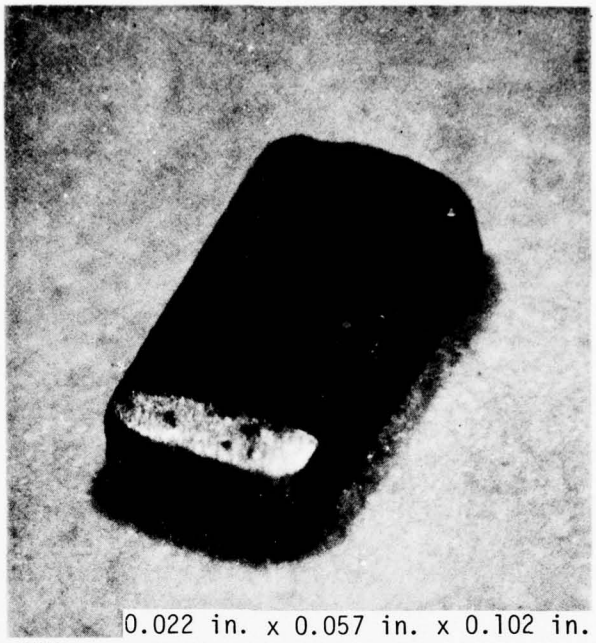
Table 02 lists the electrical tests used for this device.

04.0 BIAS CIRCUIT ANALYSIS

The test device was operated at rated voltage, 100 VDC, as the ambient temperature was elevated from 25°C to 250°C. The leakage current did not exceed 5 μA through this temperature range. The maximum voltage and ambient temperature tentatively selected for the life test were 100 VDC and 250°C respectively.

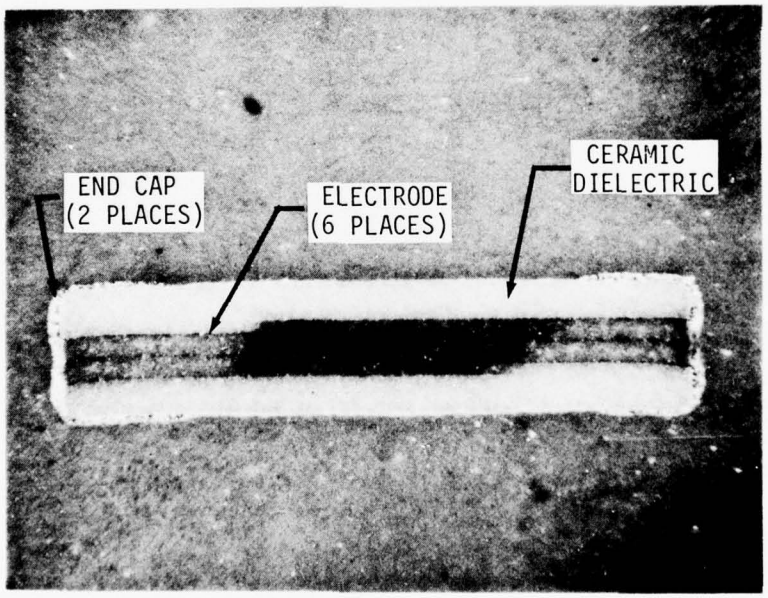
05.0 STEP STRESS TEST RESULTS

Twenty devices were subjected to a step stress test consisting of four 16 hour steps at 25°C intervals starting at 200°C and concluding at 275°C. The devices were biased with 100 VDC. The Figure 05 summary shows three failures were generated, all following the 275°C step and all due to open leads. The life test conditions, maximum voltage equal to 100 VDC and maximum ambient temperature equal to 250°C, were considered acceptable, even though lead degradation could be anticipated.



0.022 in. x 0.057 in. x 0.102 in.
20X

FIGURE 01. EXTERNAL CONSTRUCTION - P/N 773055-6 - CERAMIC CHIP CAPACITOR



37X

FIGURE 02. CROSS SECTION OF DEVICE - P/N 773055-6 - CERAMIC CHIP CAPACITOR

TABLE 01. PART CONSTRUCTION DETAILS - P/N 773056 - CERAMIC CHIP CAPACITOR

A. IDENTIFICATION

1. Part Name: Ceramic Chip Capacitor
2. Part Number: 773055-6
3. Part Manufacturer: Union Carbide Corp.
4. Manufacturer's Part Number: C1006102lK1X2H

B. EXTERNAL PACKAGE

1. Type: Self-encapsulated ceramic chip
2. Weight: 0.011 gram
3. Materials:

   a) Body: Ceramic
   b) End Caps: Silver

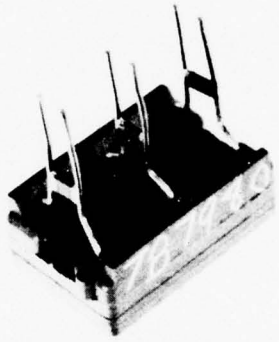
C. INTERNAL

1. Materials:

   a) Dielectric: Ceramic
   b) Electrode: Platinum and Gold

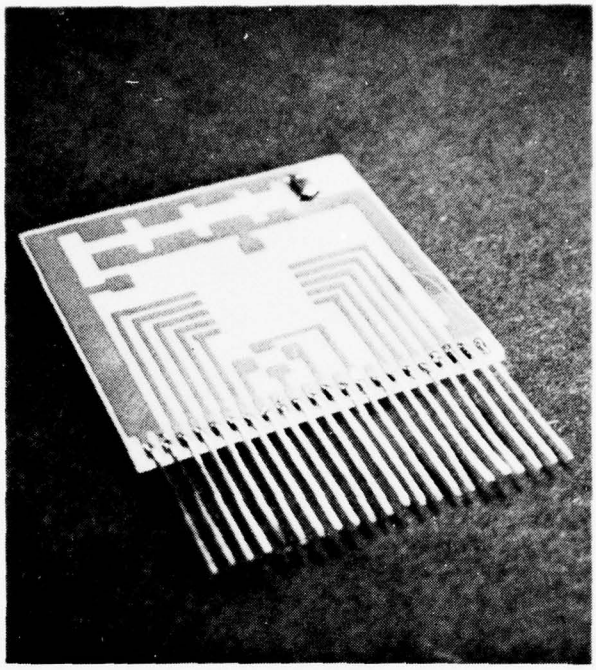
2. Interconnections:

   a) End Caps to Electrodes: Sintered



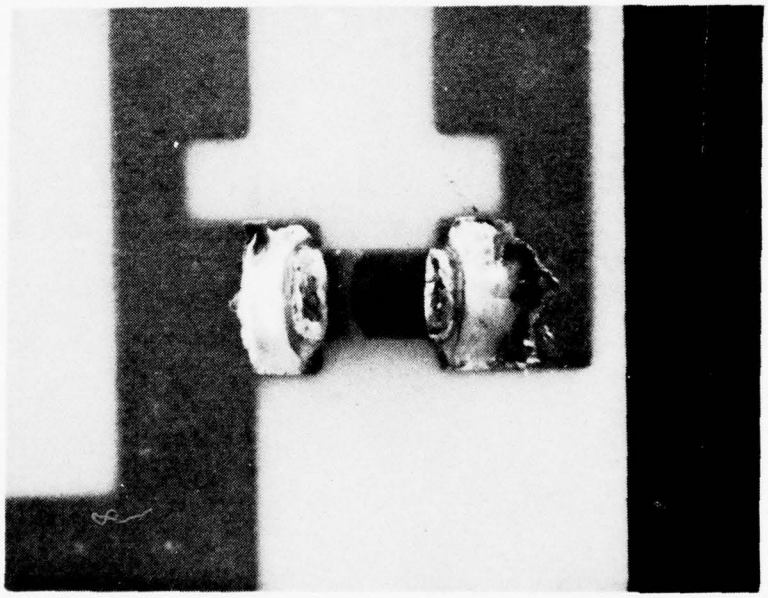
1.6X

FIGURE 03. DEVICES WITH LEADS ATTACHED (TEST CONFIGURATION) - P/N 773055-6 - CERAMIC CHIP CAPACITOR



1.9X

DEVICE MOUNTED ON CIRCUIT BOARD



9.7X

CLOSE-UP OF DEVICE

FIGURE 04. TYPICAL SAM-D CONFIGURATION - P/N 772936 - CERAMIC CHIP CAPACITOR

TABLE 02. ELECTRICAL TEST CONDITIONS - P/N 773055-6 - CERAMIC CHIP CAPACITOR

TEST NO	PARAMETER	SYMBOL	CONDITION	LIMIT		UNITS
				MIN	MAX	
1	CAPACITANCE	C	f = 1 KHz	900	1100	pf
2	DISSIPATION FACTOR	DF	f = 1 KHz	-	.025	-
3	INSULATION RESISTANCE	IR	V = 100 Vdc	1×10^5	-	MΩ
4	DIELECTRIC WITHSTANDING VOLTAGE	-	V = 25 Vdc for 1 to 5 Seconds, surge current is to be $\leq$50 mA	⚠	-	-
5	INSULATION RESISTANCE	IR	T_A=125°C, V=100 Vdc	1×10^4	-	MΩ

ALL TESTS CONDUCTED AT 25°C UNLESS OTHERWISE SPECIFIED.

ALL TESTS CONDUCTED FOR INITIAL TEST. TEST 1 THROUGH 4 CONDUCTED FOR INTERIM AND FINAL TESTS.

⚠ CAPACITOR SHALL NOT EXHIBIT ANY DAMAGE, ARCING, OR BREAKDOWN.

STEP STRESS AND LIFE TEST CIRCUIT

STEP STRESS TEST - FAILURE SUMMARY (20 DEVICES)

AMBIENT TEMP. (°C)	V_{PS} (V)	CUMULATIVE FAILURES
200	100	0
225	100	0
250	100	0
275	100	3

LIFE TEST CONDITIONS

TEST CELL NUMBER	T_A AMBIENT TEMPERATURE (°C)	V_{PS} DEVICE VOLTAGE (VOLTS)
1 ⚠1	250 ⚠1	100
2 ⚠2	250 ⚠2	75
3	250	0
4 ⚠3	225	100
5 ⚠4	200	100

DUE TO LEAD DEGRADATION, THE FOLLOWING TEST CELLS BECAME ZERO VOLTAGE CELLS AT THE TIMES INDICATED.

⚠1 0 Vdc, 285 °C, 256 HRS.
⚠2 0 Vdc, 225°C, 256 HRS
⚠3 0 Vdc, 225°C, 1000 HRS
⚠4 0 Vdc, 200°C, 2500 HRS

THE DEVICE CURRENT DOES NOT EXCEED 5 μA REPRESENTING A DISSIPATION OF 0.5 mW. THIS POWER DISSIPATION CAUSES A NEGLIGIBLE TEMPERATURE RISE. THEREFORE, $T_{I\,MAX}$ (MAXIMUM INTERNAL TEMPERATURE) IS TAKEN TO BE EQUAL TO T_A.

FIGURE 05. STEP STRESS RESULTS AND LIFE TEST CONDITIONS - P/N 773055-6 - CERAMIC CHIP CAPACITOR

06.0 LIFE TEST CONDITIONS AND RESULTS

The life test conditions for the five test cells are included in Figure 05. The life test continued to the 6000 hour readout and is summarized in Table 03. Cell 2 contained 22 parts because the initial Cell 2 parts were destroyed by an overvoltage condition and only 22 spares were available as replacements. After 256 hours Cells 1, 2, and 3 experienced degradation of the lead attach solder causing, in some cases, the leads to separate from the chip. These cells were continued in the life test as unbiased storage cells, Cell 1 at 285°C, Cell 2 at 225°C and Cell 3 remained at 250°C. Cells 4 and 5 experienced the same degradation at 1000 hours and 2500 hours respectively, and were continued in the life test as unbiased storage cells. The life test produced 3 failures, two from Cell 3 and one from Cell 4.

07.0 FAILURE ANALYSIS

Table 04 summarizes the failure analysis. All three failures exhibited capacitance which was only slightly out of specification. Upon cross sectioning these parts, no anomalous conditions were observed. Further failure analysis was not performed because of the small number of failures, consequently the exact cause of failure was not determined.

08.0 DATA CORRELATION

The Table 04 failure analysis summary shows only three life test failures, all attributed to a slight out of specification capacitance value. Evaluation of the measured parameters yielded no degradation trends. Capacitance values typically varied less than 1% and the Dissipation Factor (DF) actually improved slightly during the course of the life tests.

The three test failures are insufficient for failure distribution analysis and the lack of parameter degradation trends precludes the extrapolation of times to failure. Therefore this capacitor should have a high storage reliability potential ($\lambda(t)_{MAX} << 10^{-10}$ failures per hour).

09.0 CONCLUSIONS AND RECOMMENDATIONS

- This capacitor exhibited good stability under high temperature storage conditions.

TABLE 03. LIFE TEST SUMMARY - P/N 773055-6 - CERAMIC CHIP CAPACITOR

TEST CELL DESCRIPTION				CUMULATIVE FAILURES AT HOURS OF TEST												
CELL NO	APPLIED BIAS	AMBIENT TEMP.	QUANTITY	4	8	16	32	64	128	256	384	512	1000	2500	4000	6000
1	100 VDC ①1	250°C	30	0	0	0	0	0	0	0	0	0	0	0	0	0*
2	75 VDC ②2	250°C	22	0	0	0	0	0	0	0	0	0	0	0	0	0*
3	0 VDC	250°C	30	0	0	0	0	1	1	2	2	2	2	2	2	2*
4	100 VDC ③3	225°C	30	0	0	0	1	1	1	1	1	1	1	1	1	1*
5	100 VDC ④4	200°C	30	0	0	0	0	0	0	0	0	0	0	0	0	0*

* TEST TERMINATED

DUE TO LEAD DEGRADATION, THE FOLLOWING TEST CELLS BECAME ZERO VOLTAGE CELLS AT THE TIMES INDICATED:

①1 0 VDC, 285°C, 256 HOURS
②2 0 VDC, 225°C, 256 HOURS
③3 0 VDC, 225°C, 1000 HOURS
④4 0 VDC, 200°C, 2500 HOURS

TABLE 04. FAILURE ANALYSIS SUMMARY - P/N 773055-6 - CERAMIC CHIP CAPACITOR

A. FAILED PARAMETER OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TIME (HOURS) OF FAILURE				
	250°C			225°C	200°C
	100 VDC	75 VDC	0 VDC	100 VDC	100 VDC
	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5
A CAPACITANCE B, C, D NOT DETERMINED			1@64 1@256	1@32	
TOTAL NUMBER OF FAILED PARTS	0	0	2	1	0

- The three life test failures are insufficient for storage failure rate quantification. However, the few test failures and the parameter stability both indicate this capacitor has a high storage reliability potential.

APPENDIX P

P/N 773056-20

TANTALUM CHIP CAPACITOR

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STORAGE RELIABILITY
OF MISSILE MATERIEL

REPORT MDC E1601
29 APRIL 1977

P1.0 PART DESCRIPTION

The Tantalum Chip Capacitor, P/N 773056-20, is manufactured by National Components Industries Incorporated. The test devices were delivered in chip form as shown in Figure P1.

P2.0 CONSTRUCTION ANALYSIS

Table P1 is a summary of the pertinent physical details and Figure P2 shows a cross sectional view of the capacitor. The conductive silver epoxy used to attach the cathode to the end cap prohibited long term testing at ambient temperatures higher than 175°C.

The attachment of leads to the devices was required in order to life test the parts under electrical bias. Several types of solders were evaluated. When the highest temperature solder (309°C) was used to attach leads, the dissipation factor increased and in some cases exceeded the specification due to the thermal shock. The lowest temperature solder (221°C) subjected the parts to less thermal shock but was more susceptible to time/temperature degradation. Devices with leads attached are pictured in Figure P3 in the test configuration. A medium temperature solder (268°C) offered the best compromise and was evaluated in the test described in Paragraph P6.0.

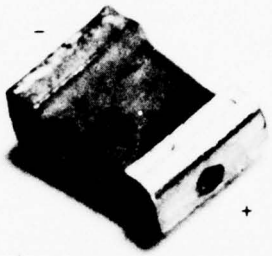
The typical SAM-D configuration is illustrated in Figure P4. It consists of the capacitor mounted on a ceramic printed circuit board.

P3.0 ELECTRICAL TEST CRITERIA

Table P2 contains a list of the electrical tests for this device.

P4.0 BIAS CIRCUIT ANALYSIS

The devices were operated at 13VDC, rated voltage, as the ambient temperature was elevated from 25°C to 175°C. The leakage current did not exceed 10μA. The test voltage, 13VDC, and the 175°C limit imposed by the conductive silver epoxy were tentatively selected as maximum accelerated life test conditions. A 1K ohm current limiting resistor was selected to preclude catastrophic damage in the event of device failure.



0.143 in. x 0.100 in. x 0.088 in.

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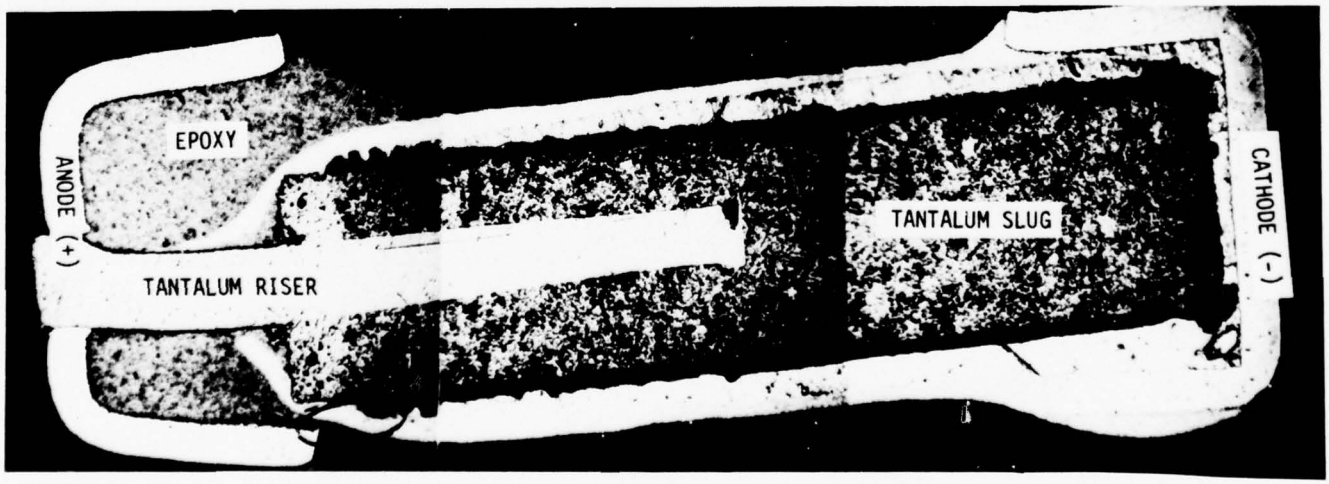
FIGURE P1. EXTERNAL CONSTRUCTION - P/N 773056 - TANTALUM CHIP CAPACITOR



50X

FIGURE P2. CROSS SECTION OF DEVICE - P/N 773056-20 - TANTALUM CHIP CAPACITOR

TABLE P1. PART CONSTRUCTION DETAILS - P/N 773056-20 - TANTALUM CHIP CAPACITOR

A. IDENTIFICATION

1. Part Name: Tantalum Chip Capacitor
2. Part Number: 773056-20
3. Part Manufacturer: National Components Industries
4. Manufacturer's Part Number: BN6225E020K5

B. EXTERNAL PACKAGE

1. Type: Molded Epoxy
2. Weight: 0.069 gram
3. Materials:

    a) Body: Epoxy
    b) End Caps: Gold-plated nickel

C. INTERNAL

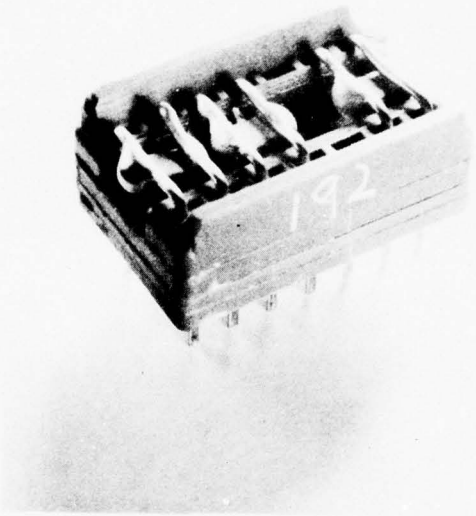
1. Material:

    a) Dielectric: Tantalum Pentoxide
    b) Electrode:

        1) Anode: Tantalum
        2) Cathode: Manganese dioxide

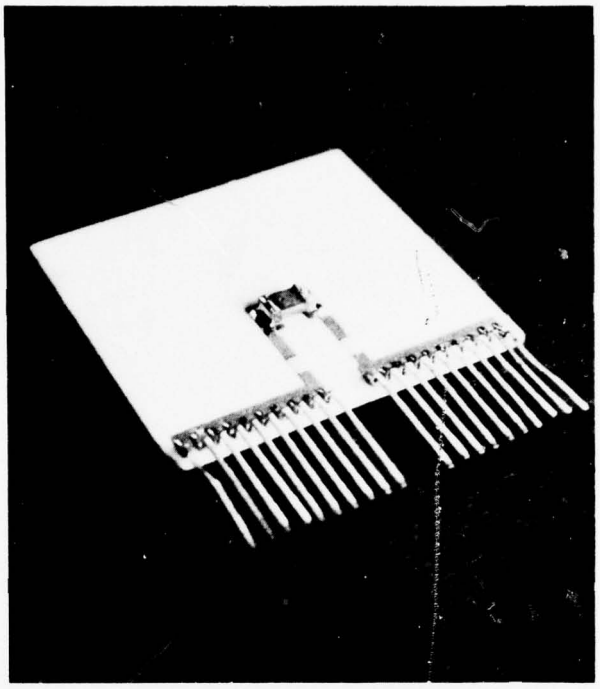
2. Interconnections:

    a) Anode to End Cap: Weld
    b) Cathode to End Cap: Conductive Silver Epoxy



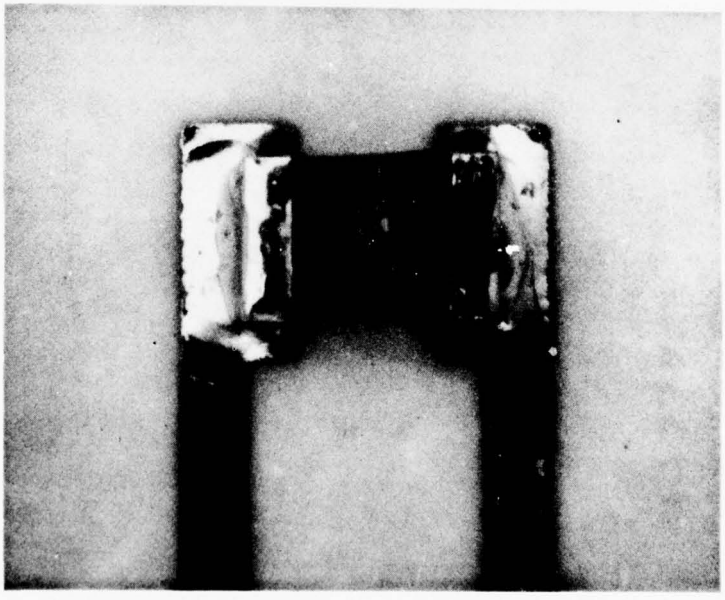
2.1X

FIGURE P3. DEVICES WITH LEADS ATTACHED (TEST CONFIGURATION) - P/N 773056-20 - TANTALUM CHIP CAPACITOR



1.9X

DEVICE MOUNTED ON CIRCUIT BOARD



10X

CLOSE-UP OF DEVICE

FIGURE P4. TYPICAL SAM-D CONFIGURATION - P/N 772937 - TANTALUM CHIP CAPACITOR

TABLE P2. ELECTRICAL TEST CONDITIONS - P/N 773056-20 - TANTALUM CHIP CAPACITOR

TEST NO.	PARAMETER	SYMBOL	CONDITION	LIMITS		UNITS
				MIN	MAX	
1	CAPACITANCE	C	f = 120 Hz, DC BIAS = 2.2 VOLTS, AC VOLTAGE = 1.0 V_{rms}	1.98	2.42	µA
2	DC LEAKAGE CURRENT	-	V = 20 Vdc, WITH A 1000Ω SERIES RESISTOR ⚠1	-	0.88	µA
3	DISSIPATION FACTOR	DF	f = 120 Hz	-	0.06	-

ALL TESTS CONDUCTED AT 25°C.

ALL TESTS CONDUCTED FOR INITIAL, FINAL AND INTERIM TESTS.

⚠1 MEASUREMENT TAKEN AFTER ELECTRIFICATION PERIOD OF 5 MINUTES.

P5.0 STEP STRESS TEST RESULTS

Twenty devices were subjected to a step stress test. High temperature solder (309°C) was used to attach leads to these parts in order to observe the effects of the thermal shock when attaching the leads and to allow the step stress test to exceed the 175°C limit which was to be imposed on the life test. As shown in the Figure P5 summary, ten devices were out of specification (DF) following the lead attach process, but all improved after the 150°C step with only three devices remaining out of specification. No new failures were encountered until the 225°C and 250°C steps. The voltage and temperature conditions previously selected as life test limits (13VDC and 175°C) were considered acceptable.

P6.0 LIFE TEST CONDITIONS AND RESULTS

The conditions for each cell are summarized in Figure P5. In order to establish confidence in the lead attach integrity, Cell 3 was initiated prior to starting the remaining cells. Three types of solder were used to attach leads in the Cell 3 parts; 309°C solder was used for 3 devices, 221°C solder for 3 devices and 268°C solder for the remaining 24 parts. Two of the three devices with 309°C solder were out of specification (DF) following lead attachment. The remaining 27 parts did not exhibit this change in parameters. After 512 hours with no evidence of solder degradation in Cell 3, the remaining four cells (1, 2, 4 and 5) were started into life test utilizing 268°C solder for lead attach.

During the life test it was determined that the presence of bias voltage in the 4 powered cells was healing some of the dc leakage failures. Consequently, the data obtained from those cells was considered questionable and therefore, not analyzed; two additional cells, 6 and 7, were initiated without bias voltages to provide storage related data.

As shown in the Table P3 summary, Cells 1, 2, 4 and 5 completed 6000 hours of life test, Cell 3 was terminated at 2500 hours with more than 50% failures, and Cells 6 and 7 were halted after 5460 hours.

STEP STRESS AND LIFE TEST CIRCUIT

STEP STRESS TEST - FAILURE SUMMARY (20 DEVICES)

PHASE OF STEP STRESS TEST	V_{PS} (VOLTS)	CUMULATIVE FAILURES C	CUMULATIVE FAILURES I_{DC} LEAKAGE	CUMULATIVE FAILURES DF
PRE LEAD ATTACH	--	0	0	0
POST LEAD ATTACH	--	0	0	10 ⚠
150°C - 19 HRS.	13	0	0	3
175°C - 19 HRS.	13	0	0	3
200°C - 21 HRS.	13	0	0	3
225°C - 21 HRS.	13	0	1	3
250°C - 70 HRS.	13	1	10	5

⚠ TEN DEVICES FAILED DF AFTER THE LEAD ATTACH PROCESS. ALL PARTS IMPROVED AFTER THE 150°C - 19 HR STEP, HOWEVER 3 PARTS REMAINED OUT OF THE SPECIFICATION.

LIFE TEST CONDITIONS

TEST CELL NUMBER	T_A AMBIENT TEMPERATURE (°C)	V_{PS} DEVICE VOLTAGE (VOLTS)
1	175	13
2	175	6.5
3	175	0
4	150	13
5	125	13
6	150	0
7	125	0

THE DEVICE CURRENTS ARE BETWEEN 0.01 AND 10 μA REPRESENTING DISSIPATIONS BETWEEN 0.13 μW AND 130 μW. THE TEMPERATURE RISE DUE TO POWER DISSIPATION OF THIS MAGNITUDE IS NEGLIGIBLE. THEREFORE, T_{IMAX} (MAXIMUM INTERNAL TEMPERATURE) IS TAKEN TO BE EQUAL TO T_A.

FIGURE P5. STEP STRESS RESULTS AND LIFE TEST CONDITIONS - P/N 773056-20 - CERAMIC CHIP CAPACITOR

P7.0 FAILURE ANALYSIS

Table P4 is a summary of the failure analysis results. There were 33 devices which failed dissipation factor only. All but one of these failures occurred in cells with bias voltages. Because the data from these cells were not considered applicable to storage life (Paragraph P6.0) the dissipation factor only failures were not analyzed.

There were 41 life test parts that failed due to excessive dc leakage current, 36 of which were in test cells without an applied bias. Curve tracer tests of failed capacitors disclosed that the leakage current was always erratic, varying between normal values of leakage and values in excess of the measured value (flickering). This indicated that the dielectric had ruptured and was self healing during the test. Metallurgical cross-sections of failed devices disclosed no sign of deterioration and no significant damage or defects. Consequently, the excessive leakage was attributed to dielectric breakdown caused by minute imperfections or impurities in the Ta_2O_5 dielectric or at the Ta_2O_5/MnO_2 interface.

P8.0 DATA CORRELATION

The Table P4 failure analysis summary reveals two failure mechanisms were encountered during the life tests. For reasons previously given the Dissipation Factor failures were not analyzed. DC leakage failures, encountered primarily in the zero volt test cells, were attributed to either degradation of impurities or imperfections in the dielectric. The DC leakage failures are considered applicable because they were accelerated by temperature alone.

The DC leakage failures usually occurred abruptly with no indication of a degradation trend. Failures were therefore assumed to have occurred at the midpoint of the time measurement interval. Data analysis was accomplished using the Weibull failure distribution, an approach used previously in evaluating tantalum chip capacitor leakage current characteristics [P1].

The Figure P6 Weibull plots show a good fit for the Weibull failure distribution. The pertinent parameters for these two distributions are summarized in Table P5. The calculated shape parameters (β), 1.74 and 1.86, are close enough to substantiate that the shape parameter is independent of the applied stress. Since voltage is not a variable, the Arrhenius model was used with the scale parameter (θ), the 63rd percentile, as the dependent variable.

TABLE P3. LIFE TEST SUMMARY - P/N 773056-20 - TANTALUM CHIP CAPACITOR

CELL NO.	APPLIED BIAS	AMBIENT TEMP.	QUANTITY	CUMULATIVE FAILURES AT HOURS OF TEST														
				4	8	16	32	64	128	256	512	1000	1504	2000	2500	3000	3504	4000	6000
1	13 VDC	175°C	30	0	0	0	0	0	0	0	0	0	4	7	10	-	-	14	17*
2	6.5 VDC	175°C	30	1	1	1	1	1	2	2	2	3	7	9	10	-	-	12	12*
3	0 VDC	175°C	30	1	1	1	1	1	1	3	6	17	-	-	28*				
4	13 VDC	150°C	30	0	0	0	0	0	0	0	0	1	2	2	2	-	-	3	6*
5	13 VDC	125°C	30	0	1	1	1	1	1	1	1	1	2	2	2	3	-	3	3*
6	0 VDC	150°C	30	0	0	-	-	0	0	0	0	0	-	3	3	-	8	13	18*
7	0 VDC	125°C	30	0	0	-	-	0	0	0	0	0	-	0	0	-	0	0	0*

* TEST TERMINATED

⚠1 CELL 6 AND CELL 7 LAST TWO READOUTS ACTUALLY OCCURRED AT 4504 AND 5460 HOURS.

TABLE P4. FAILURE ANALYSIS SUMMARY - P/N 773056-20 - TANTALUM CHIP CAPACITOR

A. FAILED PARAMETERS OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURES	QUANTITY OF FAILURES AND TIME (HOURS) OF FAILURE						
	175°C			150°C		125°C	
	13V	6.5V	0V	13V	0V	13V	0V
	CELL 1	CELL 2	CELL 3	CELL 4	CELL 6	CELL 5	CELL 7
A. DC LEAKAGE		1@1504	1@4	1@1000	3@2000	1@8	
B. DIELECTRIC BREAKDOWN			2@256	1@1504	5@3504	1@1504	
C. DEGRADATION OF IMPURITIES OR IMPERFECTIONS IN THE DIELECTRIC			3@512		5@4504	1@3000	
D. PROCESS INDUCED DEFECTS			11@1000 11@2500		4@5460		
A. DISSIPATION FACTOR	4@1504	1@4		1@4000	1@5460		
B. NOT ANALYZED	3@2000	1@128		3@6000			
C. NOT ANALYZED	3@2500	1@1000					
D. NOT ANALYZED	4@4000	3@1504					
	3@6000	2@2000					
		1@2500					
		2@4000					
TOTAL NUMBER OF FAILED PARTS	17	12	28	6	18	3	0

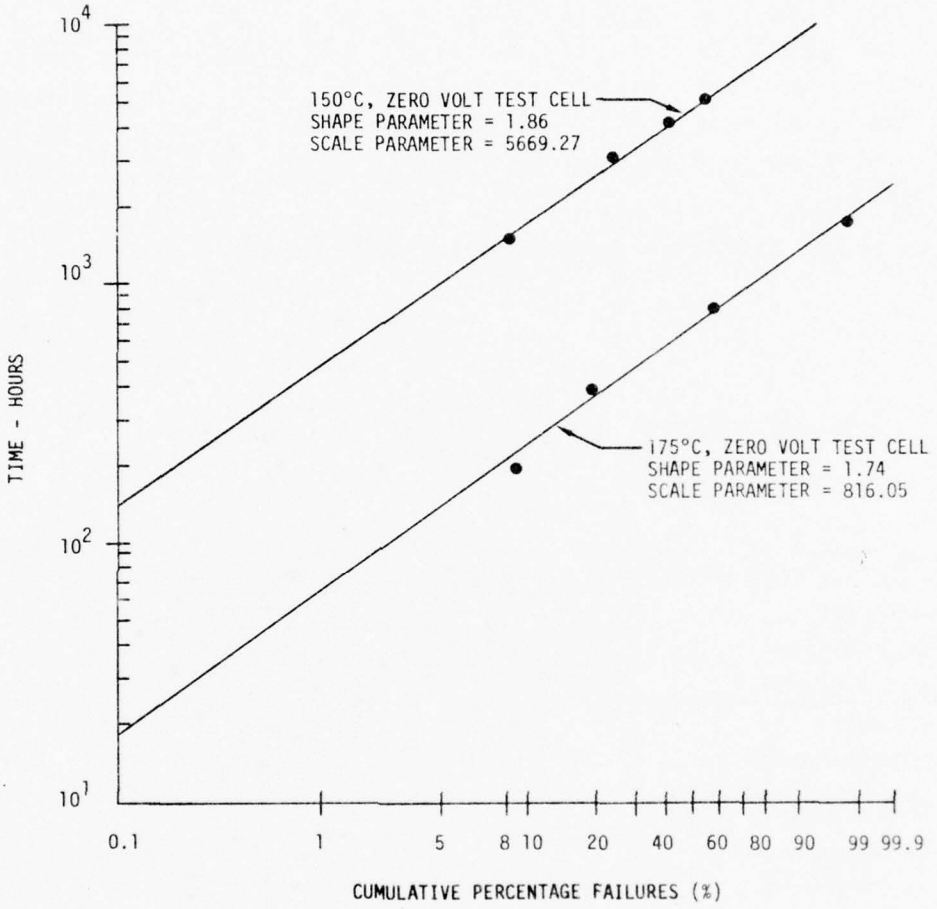


FIGURE P6. WEIBULL CUMULATIVE FAILURE DISTRIBUTION - P/N 773056-20 - TANTALUM CHIP CAPACITOR

TABLE P5. SUMMARY DATA - P/N 773056-20 - TANTALUM CHIP CAPACITOR

CELL NO.	TEST VOLTAGE (VOLTS)	NUMBER OF FAILURES	T_A (°C)	T_J (°C)	MAIN POPULATION	
					SCALE PARAMETER (θ) (HOURS)	SHAPE PARAMETER (β)
3	ZERO	27	175	175	816.05	1.74
6	ZERO	17	150	150	5669.27	1.86

The Figure P7 Arrhenius plot can be represented by the following equation:

$$\theta = 4.605 \times 10^{-12} \exp \frac{1.267}{kT}$$

Using an average shape parameter of 1.8, failure rates $\lambda(t)$ were calculated using the following relationship:

$$\lambda(t) = \frac{f(t)}{R(t)}$$

$$= \left[\frac{\beta}{t}\right]\left[\frac{t}{\theta}\right]^{\beta}$$

$$= \left[\frac{1.8}{t}\right]\left[\frac{t}{4.605 \times 10^{-12} \exp \frac{1.267}{kT}}\right]^{1.8}$$

$$= \left[\frac{1.8}{t}\right]\left[t(2.1715 \times 10^{11}) \exp - \frac{1.267}{kT}\right]^{1.8}$$

The maximum instantaneous failure rate, $\lambda(t)_{MAX}$, is 1.13×10^{-6} failures per hour. Figure P8 shows the failure rate behavior for a twenty-year period as a function of temperature.

The part specification for this capacitor establishes +125°C as the upper storage temperature limit. The results of this program indicate that extended storage at temperatures above 100°C will result in failure rates larger than 10^{-6} failures per hour. If this is a typical lot of parts, consideration should be given to lowering the maximum storage temperature to 100°C. If this is not a typical lot, a lot sampling test could be investigated as a possible lot acceptance test. Additional testing (or data) is necessary to develop appropriate accept/reject criteria.

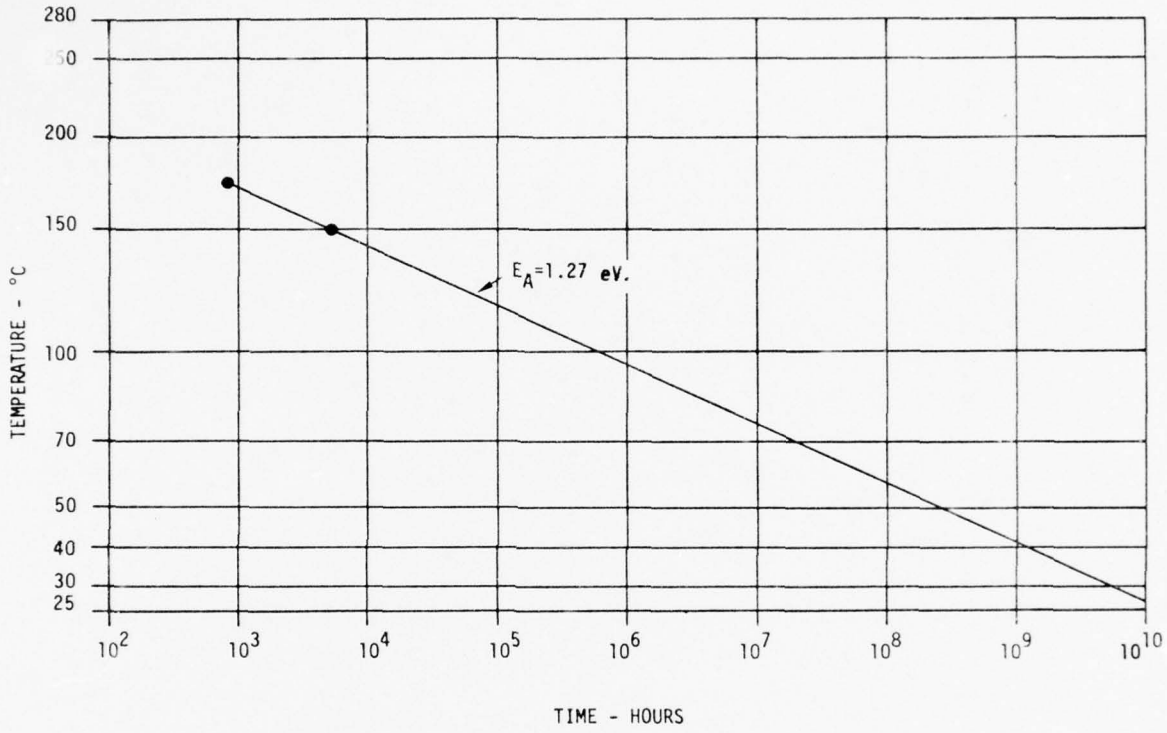


FIGURE P7. ARRHENIUS PLOT - P/N 773056-20 - TANTALUM CHIP CAPACITOR

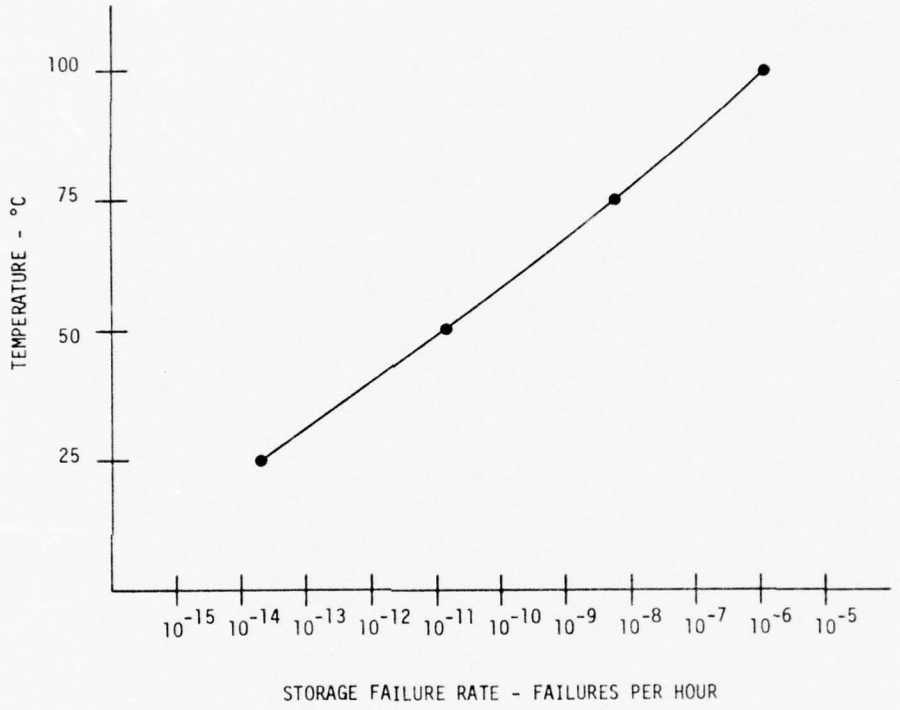


FIGURE P8. MAXIMUM INSTANTANEOUS FAILURE RATE, $\lambda(t)$, 20 YEAR INTERVAL - P/N 773056-20 - TANTALUM CHIP CAPACITOR

The one early failure in Cell 3 was not included in the analysis and is considered the "freak" or infant mortality population. This small (1.7%) "freak" population percentage can be screened with a short-term high temperature test (24 hours at 175°C); however, this screen is applicable only to the zero volt or storage freak population and has an unknown effect on the undefined operational freak population.

P9.0 CONCLUSIONS AND RECOMMENDATIONS

- The failure data showed a very good fit to the Weibull failure distribution and each test cell had approximately the same shape parameter.
- The maximum failure rate over the storage time (20 years) and temperature range of interest (25°C to 100°C) is 1.13×10^{-6} failures per hour.
- This capacitor should be considered marginal for storage at temperatures greater than 100°C. The additional investigation recommended in paragraph P8.0 appears appropriate.
- A 100% screening test (175°C for 24 hours) can be utilized for the small (1.7%) "freak" storage population; however, the operational "freak" population has not been defined.

P10.0 REFERENCES

[P1] J. Burnham, "Leakage Current Stability of Solid Tantalum Chip Capacitors Under Highly Accelerated Voltage and Temperature Conditions", 1973 Proceedings, 23rd Electronics Components Conference, pp. 111-124.

APPENDIX Q

P/N 773057-18

CERAMIC AXIAL LEAD CAPACITOR

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Q1.0	PART DESCRIPTION	Q2
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Q1.0 PART DESCRIPTION

The Ceramic Axial Lead Capacitor, P/N 773057-18, was manufactured by U.S. Capacitor Corporation and consists of noble metal electrodes and a ceramic dielectric. The body material is molded epoxy and the device has nickel axial leads. The test configuration is identical to the SAM-D use configuration.

Q2.0 CONSTRUCTION ANALYSIS

The pertinent construction details are listed in Table Q1. Figures Q1 and Q2 provide an external view and a cross sectional view of the part respectively. The molded epoxy used to encapsulate the device was expected to be the predominant time/temperature limiting feature. Previous testing indicated satisfactory operation at 200°C for 200 hours. Since the internal solder has a liquidus temperature of 222°C, the maximum ambient temperature was limited to 200°C for the life test.

The typical SAM-D configuration, Figure Q3, consists of a capacitor identical to the life test device soldered to a ceramic printed circuit board.

Q3.0 ELECTRICAL TEST CRITERIA

The electrical tests for this device are listed in Table Q2.

Q4.0 BIAS CIRCUIT ANALYSIS

This device was operated with rated voltage, 50VDC, applied as the ambient temperature was elevated from 25°C to 200°C. The leakage current did not exceed 10nA. Therefore, the tentative maximum conditions for the life test were 50VDC and 200°C.

Q5.0 STEP STRESS TEST RESULTS

Twenty devices biased with 50VDC were subjected to a step stress test consisting of six 16 hour steps at 25°C intervals starting at 125°C and concluding at 250°C. Eleven parts failed, all after the 250°C step. Figure Q4 summarizes the step stress test. All failures were marginal capacitance and/or dissipation factor. Therefore, the selected maximum life test conditions were considered acceptable.

TABLE Q1. PART CONSTRUCTION DETAILS - P/N 773057-18 - CERAMIC AXIAL LEAD CAPACITOR

A. IDENTIFICATION

1. Part Name: Ceramic Axial Lead Capacitor
2. Part Number: 773057-18
3. Part Manufacturer: U. S. Capacitor Corp.
4. Manufacturer's Part Number: C33C180J

B. EXTERNAL PACKAGE

1. Type: Molded-epoxy
2. Weight: 0.295 gram
3. Materials:

   a) Body: Epoxy
   b) Leads: Nickel

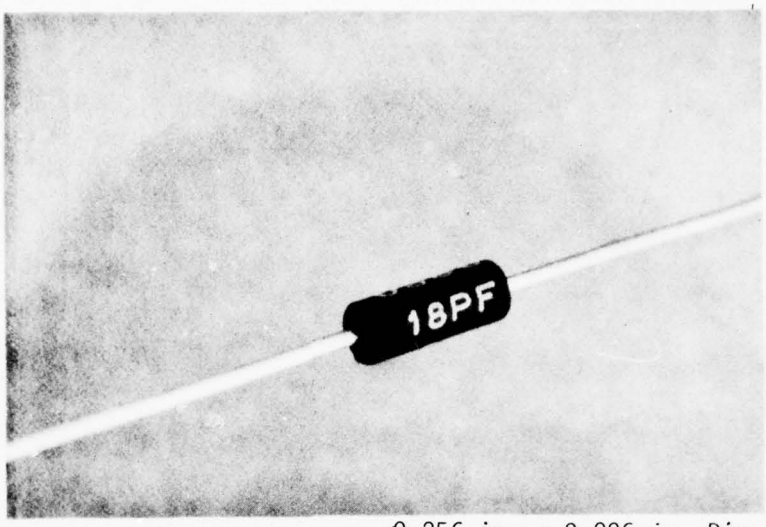
C. INTERNAL

1. Materials:

   a) *Dielectric: Ceramic*
   b) Electrodes: Silver, Palladium, Gold or Platinum
   c) End Caps: Silver or Palladium

2. Interconnections:

   a) Leads to End Caps: 95.5 Silver solder



3.2X 0.256 in. x 0.096 in. Dia.

FIGURE Q1. EXTERNAL CONSTRUCTION - P/N 773057-18 - CERAMIC AXIAL LEAD CAPACITOR

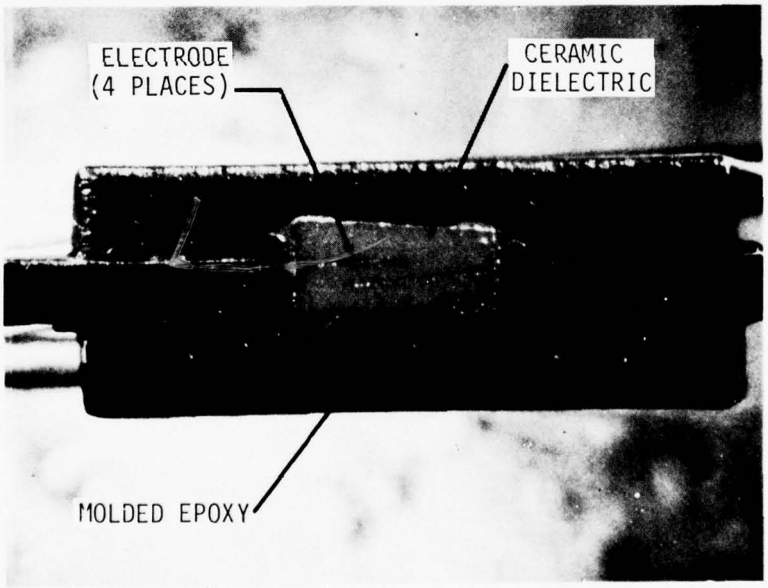


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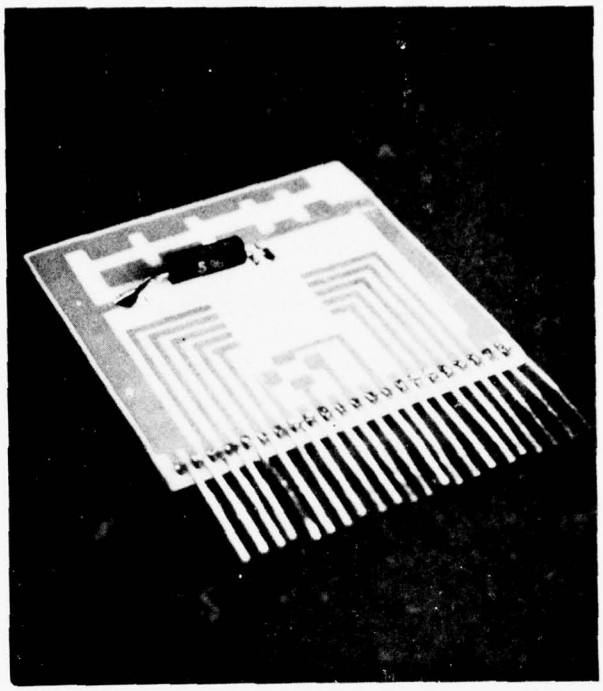
FIGURE Q2. CROSS SECTION OF DEVICE - P/N 773057-18 - CERAMIC AXIAL LEAD CAPACITOR



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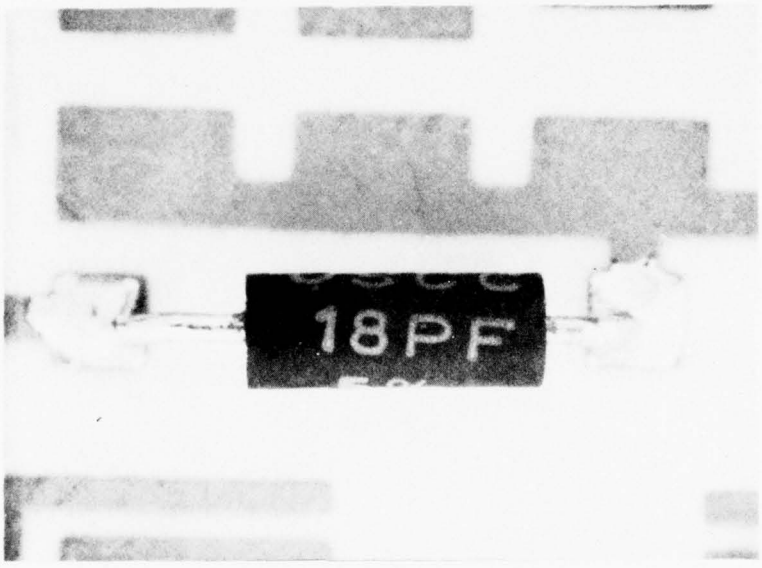
DEVICE MOUNTED ON CIRCUIT BOARD



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CLOSE-UP OF DEVICE

FIGURE Q3. TYPICAL SAM-D CONFIGURATION - P/N 772938 - CERAMIC AXIAL LEAD CAPACITOR

TABLE Q2. ELECTRICAL TEST CONDITIONS - P/N 773057-18 - CERAMIC AXIAL LEAD CAPACITOR

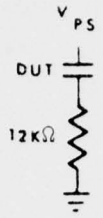
TEST NO	PARAMETER	SYMBOL	CONDITION	LIMITS MIN	LIMITS MAX	UNITS
1	CAPACITANCE	C	f = 1.0 KHz	17.10	18.90	pf
2	DISSIPATION FACTOR	DF	f = 1.0 KHz	-	0.15	%
3	INSULATION RESISTANCE	IR	V = 50 Vdc	$1x10^5$	-	MΩ
4	DIELECTRIC WITHSTANDING VOLTAGE	-	V = 125 Vdc for 1 to 5 seconds, surge current is to be ≤50 mA	⚠1	-	-
5	CAPACITANCE	C	T_A-125°C, f=1.0 KHz	17.10	18.90	pf
6	CAPACITANCE	C	T_A=-55°C, f=1.0 KHz	17.10	18.90	pf
7	DISSIPATION FACTOR	DF	T_A=125°C, f=1.0 KHz	-	0.15	%
8	DISSIPATION FACTOR	DF	T_A=-55°C, f=1.0 KHz	-	$1x10^5$	%
9	INSULATION RESISTANCE	IR	T_A=125°C	$1x10^5$	-	MΩ

⚠1 CAPACITOR SHALL NOT EXHIBIT ANY DAMAGE, ARCING, OR BREAKDOWN.

ALL TESTS CONDUCTED AT 25°C UNLESS OTHERWISE SPECIFIED.

ALL TESTS CONDUCTED FOR INITIAL TEST. TESTS 1 THROUGH 3 CONDUCTED FOR INTERIM TEST. TEST 1 THROUGH 4 CONDUCTED FOR FINAL TEST.

STEP STRESS AND LIFE TEST CIRCUIT



STEP STRESS RESULTS - FAILURE SUMMARY (20 DEVICES)

AMBIENT TEMP. (°C)	V_{PS} (V)	CUMULATIVE FAILURES
125	50	0
150	50	0
175	50	0
200	50	0
225	50	0
250	50	11

LIFE TEST CONDITIONS

TEST CELL NUMBER	T_A AMBIENT TEMPERATURE (°C)	V_{PS} DEVICE VOLTAGE (VOLTS)
1	200	50
2	200	37.5
3	200	0
4	175	50
5	150	50

THE DEVICE CURRENT DOES NOT EXCEED 10 nA REPRESENTING A DISSIPATION OF 0.5 μW. THIS POWER DISSIPATION CAUSES A NEGLIGIBLE TEMPERATURE RISE. THEREFORE, T_{IMAX} (MAXIMUM INTERNAL TEMPERATURE) IS TAKEN TO BE EQUAL TO T_A.

FIGURE Q4. STEP STRESS RESULTS AND LIFE TEST CONDITIONS - P/N 773057-18 - CERAMIC AXIAL LEAD CAPACITOR

Q6.0 LIFE TEST CONDITIONS AND RESULTS

A summary of the life test conditions for each cell is included in Figure Q4. The Table Q3 summary shows the life test proceeded for 6000 hours, producing 101 failures. Some of the test cells were allowed to continue beyond 50% failures to provide additional data.

Q7.0 FAILURE ANALYSIS

Table Q4 is a summary of the failure analysis results.

Dissipation Factor Failures - Ninety-nine (99) life test parts failed due to excessive dissipation factor. A few of these parts also failed due to slightly low capacitance. Metallurgical cross sections of failed devices disclosed a general deterioration of the capacitor materials which accounted for the increased dissipation factor and low capacitance. The molded epoxy package material of all of the parts examined was severely cracked and the ceramic dielectric material of most of the parts had cracked as illustrated in Figures Q5 and Q6. A few parts contained broken internal solder joints to the end caps as illustrated in Figure Q7. The damage was probably caused by a combination of thermal deterioration and thermal expansions and contractions of the device material.

Capacitance Failures - Two (2) life test parts in Cell 5 failed capacitance (only) at 6000 hours. Cross sections of these two parts did not disclose the cause of low capacitance. In addition, neither part showed any sign of material degradation.

Q8.0 DATA CORRELATION

The Table Q4 failure analysis summary attributed the Cell 1 through 4 Dissipation Factor (DF) failures to material degradation, occurring at temperatures of 175°C or greater. The two 150°C test cell failures (capacitance) did not exhibit signs of this material degradation. Although material degradation is a storage failure mechanism, the validity of using the observed degradation rate for projection purposes has not been established in this instance. Atypical response due to excessive temperature or temperature cycling is a possibility and must be considered when assessing the data analysis results.

TABLE Q3. LIFE TEST SUMMARY - P/N 773057-18 - CERAMIC AXIAL LEAD CAPACITOR

TEST CELL DESCRIPTION				CUMULATIVE FAILURES AT HOURS OF TEST											
CELL NO.	APPLIED BIAS	AMBIENT TEMP.	QTY	4	8	16	32	64	128	256	512	1000	2500	4000	6000
1	50VDC	200°C	30	0	0	0	0	0	0	0	0	9	29	30	30*
2	37.5VDC	200°C	30	0	0	0	0	0	0	0	0	8	29	30	30*
3	0VDC	200°C	30	0	0	0	0	0	0	0	2	2	18	28	28*
4	50VDC	175°C	30	0	0	0	0	0	0	0	0	0	1	3	11*
5	50VDC	150°C	30	0	0	0	0	0	0	0	0	0	0	0	2*

*Test Terminated

TABLE Q4. FAILURE ANALYSIS SUMMARY - P/N 773057-18 CERAMIC AXIAL LEAD CAPACITOR

A. FAILED PARAMETERS OR SYMPTOMS	QUANTITY OF FAILURES AND TIME (HRS) OF FAILURE				
B. FAILURE MODE	200°C			175°C	150°C
C. FAILURE MECHANISM	50V	37.5V	0V	50V	50V
D. CAUSE OF FAILURE	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5
A. DISSIPATION FACTOR AND CAPACITANCE	9@1000	8@1000	2@512	1@2500	
B. EXCESSIVE RESISTANCE	20A2500	21@2500	16@2500	2@4000	
C. DETERIORATION AND CRACKING OF THE MATERIALS	1@4000	1@4000	10@4000	8@6000	
D. MATERIAL THERMAL LIMITATIONS					
A. CAPACITANCE					2@6000
B. NOT ANALYZED					
C. NOT ANALYZED					
D. NOT ANALYZED					
TOTAL NUMBER OF FAILED PARTS	30	30	28	11	2

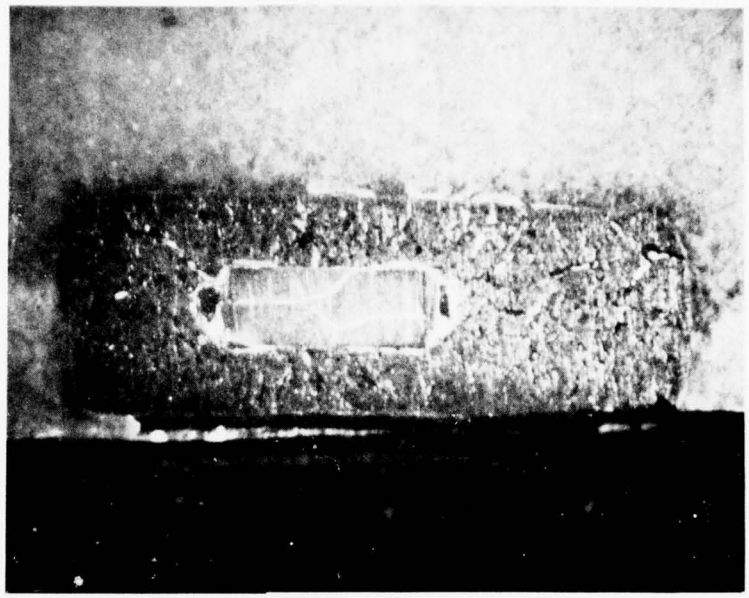


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FIGURE Q5. EXAMPLE OF FAILED PART SHOWING CRACKED EPOXY PACKAGE AND CERAMIC DIELECTRIC - P/N 773057-18 - CERAMIC AXIAL LEAD CAPACITOR

30X

FIGURE Q6. CLOSE-UP OF THE PART SHOWN IN FIGURE Q5 AFTER SECTIONING INTO THE PLATES SHOWING THAT THE CRACKS IN THE CERAMIC SEVERED SOME OF THE PLATES - P/N 773057-18 - CERAMIC AXIAL LEAD CAPACITOR

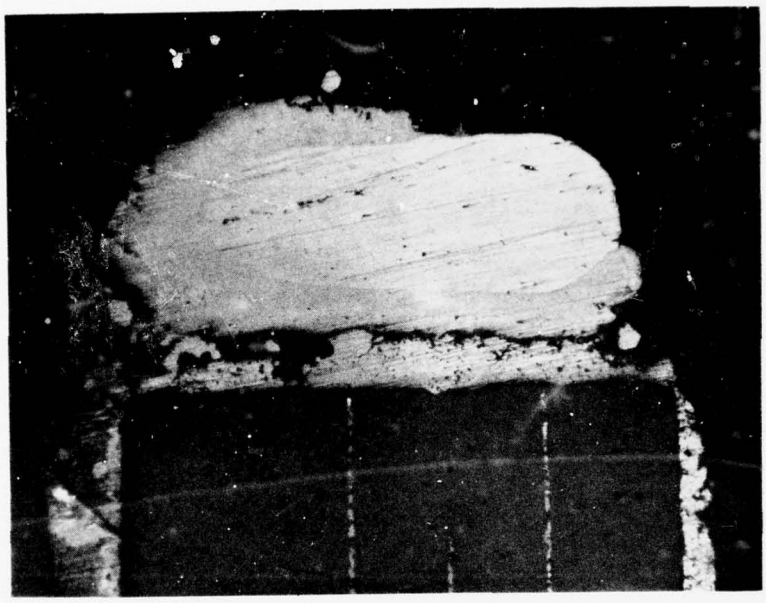

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FIGURE Q7. EXAMPLE OF A CRACKED INTERNAL SOLDER JOINT - P/N 773057-18 - CERAMIC AXIAL LEAD CAPACITOR

Cells 1 through 4 failure times were established using interpolation techniques and the cumulative failure distributions were investigated. Both the Weibull, Figure Q8, and the lognormal, Figures Q9 and Q10, failure distributions were found to adequately describe the data. K-S goodness of fit tests did not establish a definite preference for either distribution. Pertinent distribution data is summarized in Table Q5. The Figure Q11 Arrhenius plots, using the 50 volt data from both distributions, can be represented by the following equations:

$$\underline{\text{lognormal}}$$

$$\ln t_{50\%} = -23.92412 + \frac{1.27}{kT}$$

$$\underline{\text{Weibull}}$$

$$\theta = 4.260352 \times 10^{-10} \exp \frac{1.182}{kT}$$

The Weibull failure rate was higher than the lognormal failure rate by many orders of magnitude and was therefore chosen for more extensive failure rate analysis. The Figure Q12 plot of maximum Weibull instantaneous failure rate, $\lambda(t)$, as a function of temperature for a twenty-year storage period was calculated using the following equation:

$$\lambda(t)_{50 \text{ volt}} = \frac{f(t)}{R(t)}$$

$$= \left[\frac{\beta}{t}\right]\left[\frac{t}{\theta}\right]^{\beta}$$

$$= \frac{2.94}{t}\left[\frac{t}{4.260352 \times 10^{-10} \exp \frac{1.182}{kT}}\right]^{2.94}$$

Although this $\lambda(t)$ was obtained using 50 volt data, the results are considered applicable to a storage environment because the failure mechanism displayed a lack of voltage sensitivity in Cells 1, 2 and 3. The calculated $\lambda(t)_{MAX}$ is 9.4×10^{-10} failures per hour.

STORAGE RELIABILITY
OF MISSILE MATERIEL

REPORT MDC E1601
29 APRIL 1977

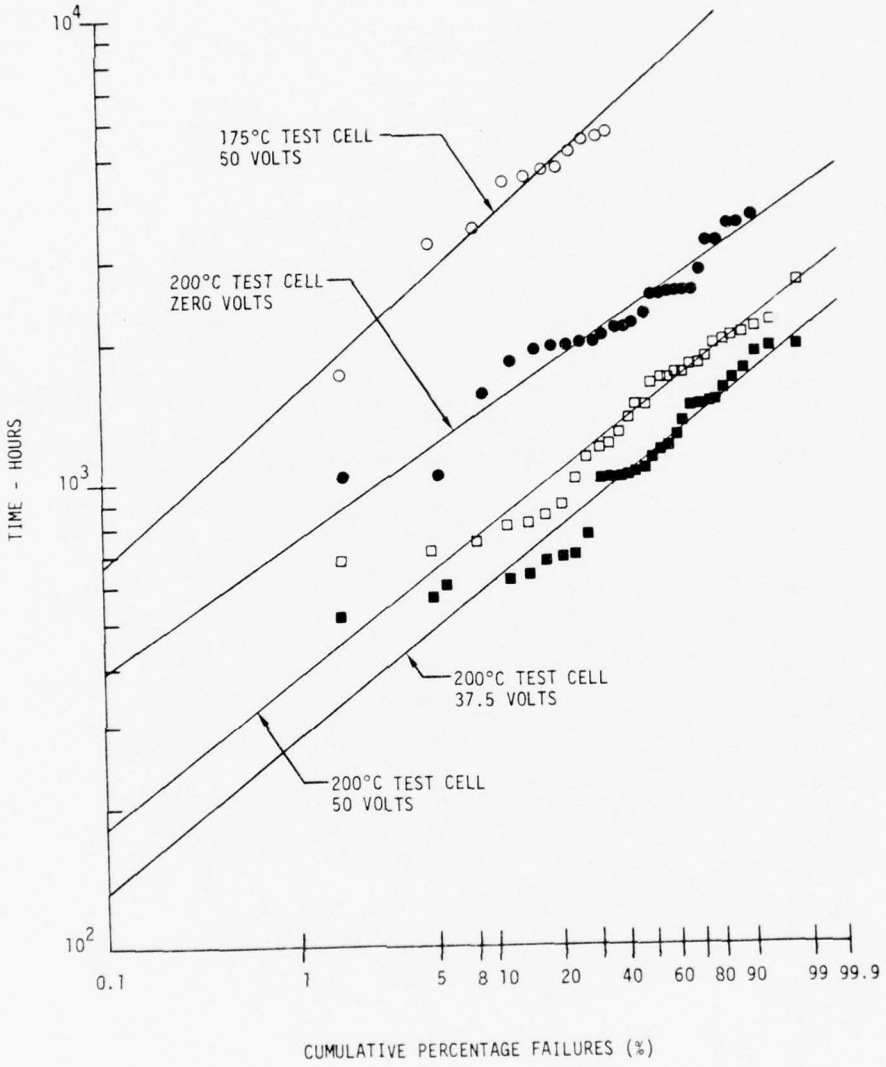

FIGURE Q8. WEIBULL CUMULATIVE FAILURE DISTRIBUTION - P/N 773057-18 - CERAMIC AXIAL LEAD CAPACITOR

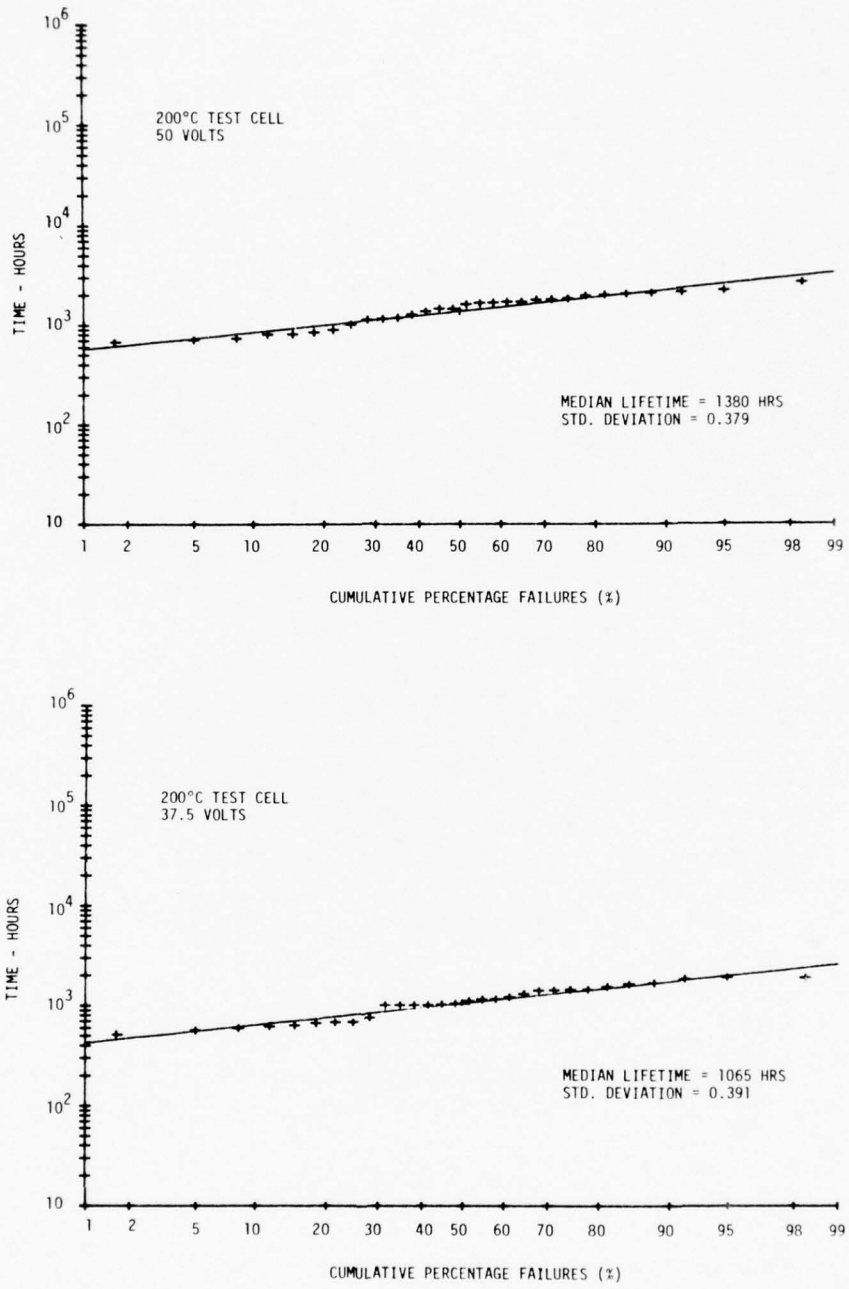

FIGURE Q9. CUMULATIVE FAILURE DISTRIBUTION FOR CELL 1 (TOP) AND CELL 2 (BOTTOM) - P/N 773057-18 - CERAMIC AXIAL LEAD CAPACITOR

STORAGE RELIABILITY
OF MISSILE MATERIEL

REPORT MDC E1601
29 APRIL 1977

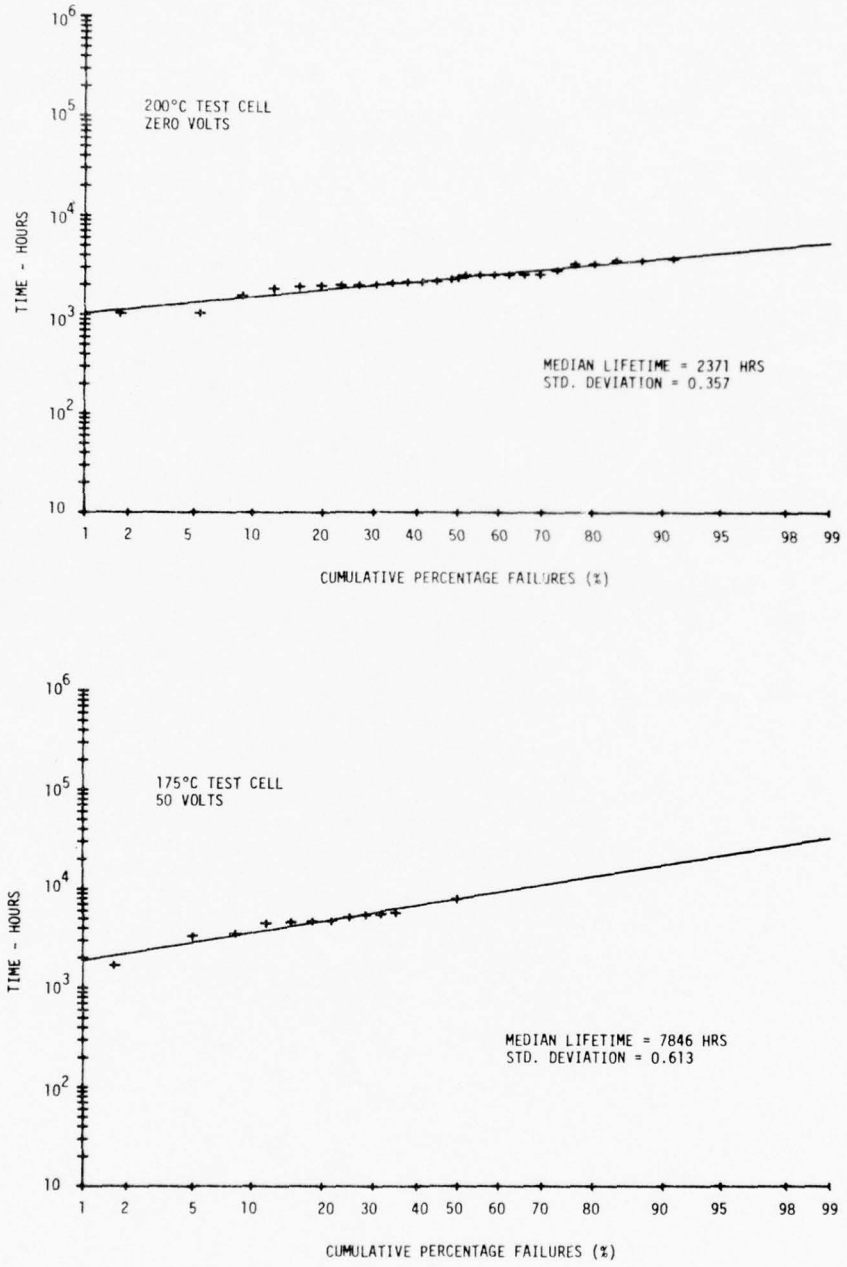

FIGURE Q10. CUMULATIVE FAILURE DISTRIBUTION FOR CELL 3 (TOP) AND CELL 4 (BOTTOM) - P/N 773057-18 - CERAMIC AXIAL LEAD CAPACITOR

TABLE Q5. SUMMARY DATA - P/N 773057-18 - CERAMIC AXIAL LEAD CAPACITOR

CELL NO.	TEST VOLTAGE (VOLTS)	NUMBER OF FAILURES	T_A (°C)	T_{INT} (°C)	WEIBULL ANALYSIS		LOGNORMAL ANALYSIS	
					θ (HOURS)	β (HOURS)	MEDIAN LIFE (HOURS)	STANDARD DEVIATION (HOURS)
1	50	30	200	200	1655	3.13	1380	.379
2	37.5	30	200	200	1286	3.02	1065	.391
3	0	28	200	200	2748	3.55	2371	.357
4	50	11	175	175	8336	2.74	7846	.613

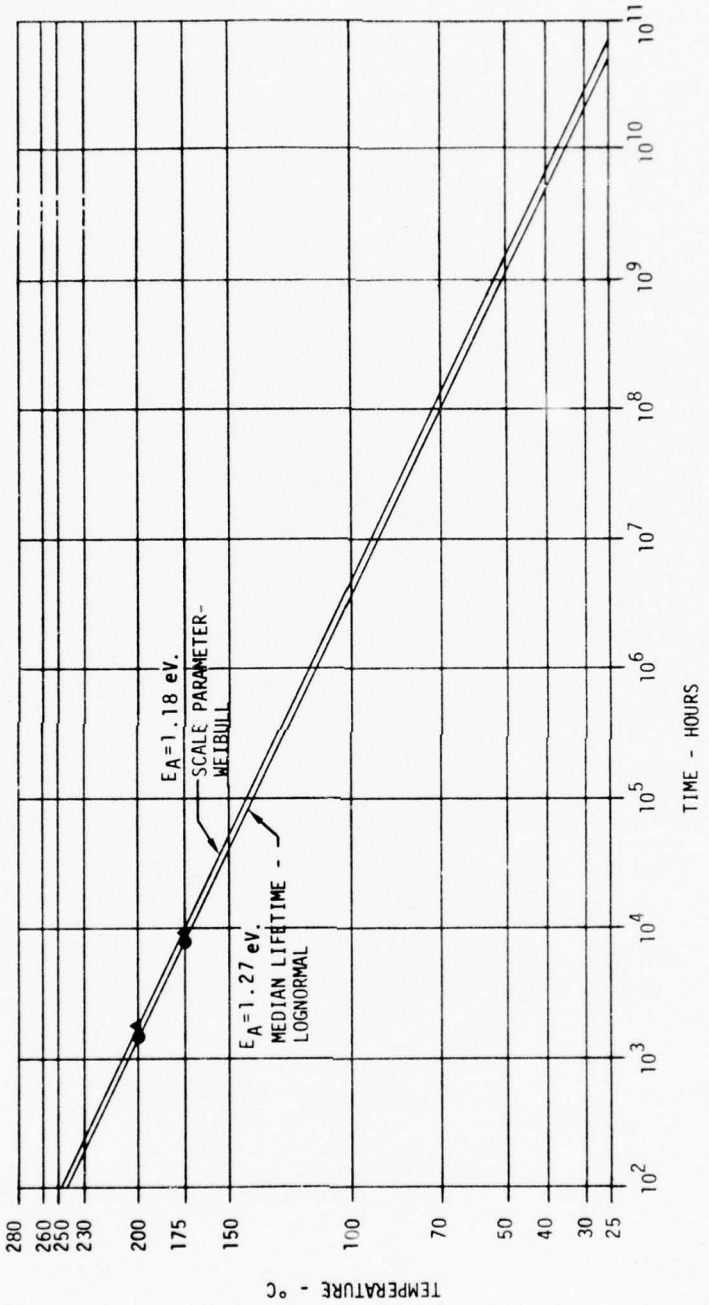

FIGURE Q11. ARRHENIUS PLOTS - P/N 773057-18 -
CERAMIC AXIAL LEAD CAPACITOR

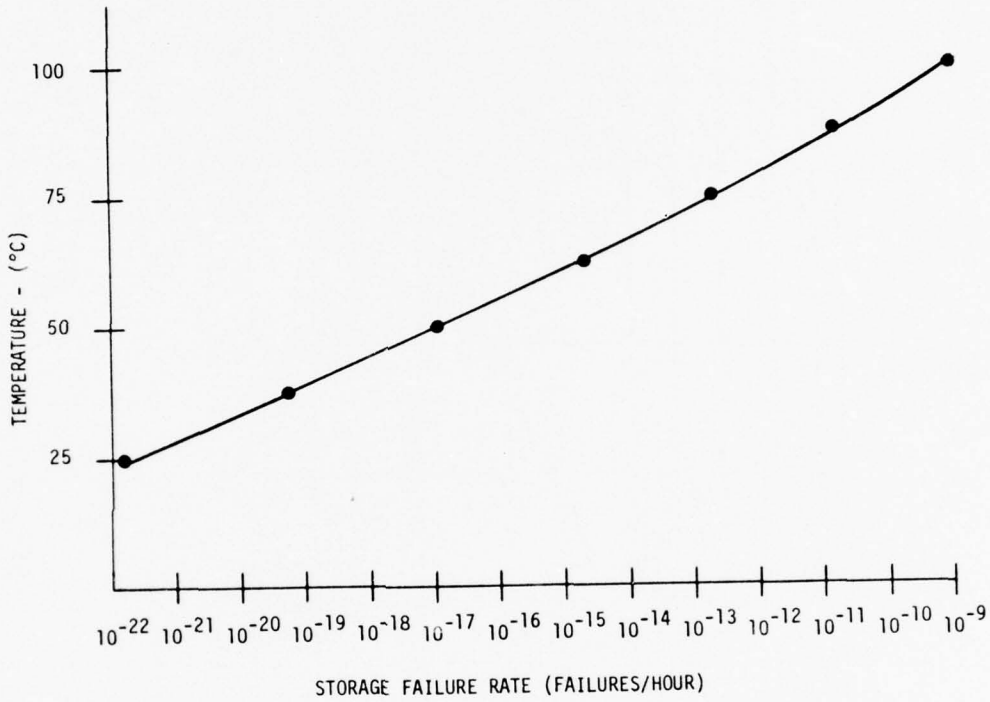

FIGURE Q12. MAXIMUM INSTANTANEOUS FAILURE RATE, $\lambda(t)$, 20 YEAR INTERVAL - P/N 773057-18 ~ CERAMIC AXIAL LEAD CAPACITOR

The Weibull Arrhenius model provides a means of investigating the lack of epoxy degradation failures in Cell 5 (150°C). From Figure Q11 the projected value of the scale parameter, θ, is 5.1×10^4 hours at 150°C. Using an average value of 2.94 for the shape parameter, β, the Figure Q13 plot shows the expected cumulative failure distribution at 150°C. For a sample size of 30 parts the first failure would be expected to occur after 16,000 hours and the probability of a failure occurring within a 6000 hour life test is small. This in no way substantiates the hypothesis that the epoxy degradation mechanism would occur at 150°C or less; however, it does show that the 150°C data does not refute that hypothesis.

Q9.0 CONCLUSIONS AND RECOMMENDATIONS

- The epoxy degradation failure mechanism in the 175°C and 200°C test cells was not evidenced in the 150°C test cell. Although data analysis suggests that the 150°C results are not unexpected, the possibility that the DF failures were induced by a material overstress condition cannot be discounted.
- Assuming the applicability of the failure mechanism to a storage environment, data analysis indicates the acceptability of either a Weibull or a lognormal failure distribution. No freak population is evident. The Weibull yields the most conservative failure rates and these appear acceptable for the storage time and temperature range of interest.

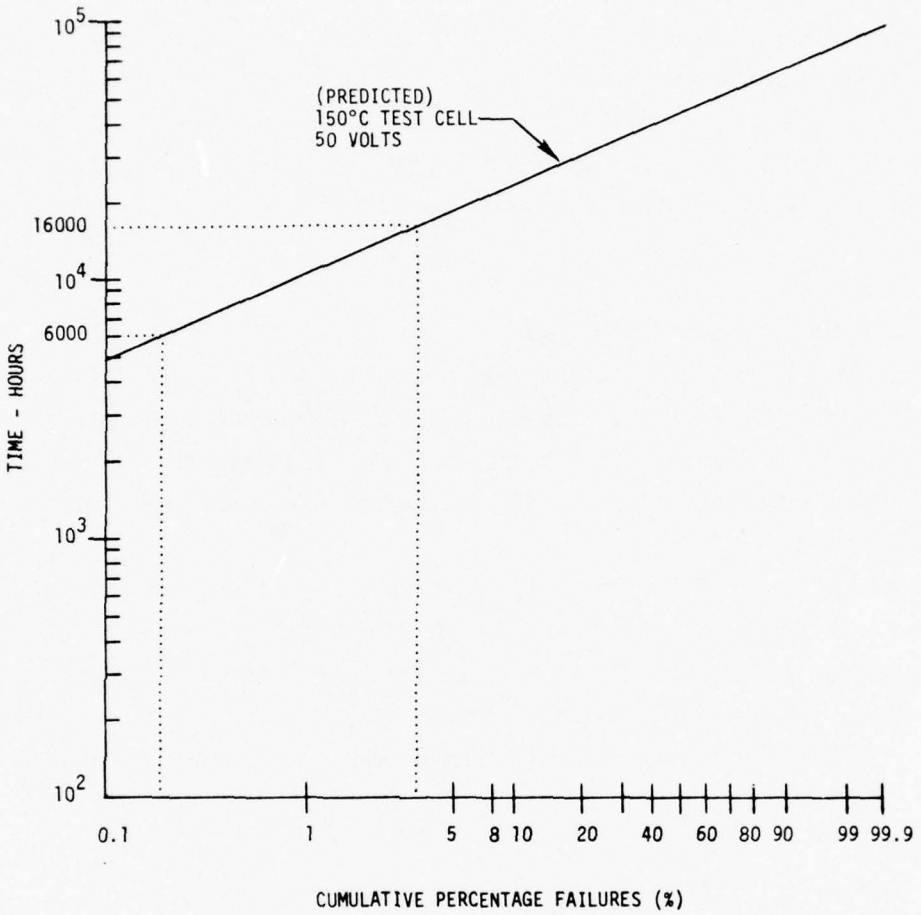

FIGURE Q13. PREDICTED CUMULATIVE FAILURE DISTRIBUTION AT 150°C - P/N 773057-18 - CERAMIC AXIAL LEAD CAPACITOR

APPENDIX R

P/N 773058-39

HIGH SELF-RESONANT FREQUENCY INDUCTOR CHIP

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R10.0	REFERENCES	R23

R1.0 PART DESCRIPTION

This device is a High Self-Resonant Frequency Inductor Chip, P/N 773058-39, manufactured by Piconics Incorporated. The test devices were delivered in chip form as depicted in Figure R1, and leads were attached by MDAC-EAST for the test program.

R2.0 CONSTRUCTION ANALYSIS

The pertinent physical details are summarized in Table R1, and a cross sectional view of the part is provided in Figure R2. The molded diallyl phthalate used to encapsulate the inductor limited the maximum life test temperature to 175°C. In order to apply bias nickel leads were attached to the parts using 221°C solder. Figure R3 shows the test configuration.

The typical SAM-D configuration is pictured in Figure R4. It consists of a chip identical to the life test part soldered to a ceramic printed circuit board.

R3.0 ELECTRICAL TEST CRITERIA

Table R2 contains a list of the electrical tests used for this part.

R4.0 BIAS CIRCUIT EVALUATION

The device was operated with a constant current of 160 mA as the ambient temperature was elevated from 25°C to 175°C. The power dissipation at 150°C was 73 mW and caused a 17°C temperature rise in the inductor. The maximum temperature tentatively selected for the life test was 150°C such that, with the 17°C rise due to power dissipation, the 175°C limit imposed by the diallyl phthalate would not be exceeded. The maximum electrical limit selected was 160 mA.

R5.0 STEP STRESS TEST RESULTS

The Figure R5 summary shows twenty-five devices were subjected to a step stress test consisting of four 16 hour steps at 25°C intervals, starting at 125°C and concluding at 200°C. The devices were drawing 160 mA. No failures were experienced following the 150°C step. The test was continued to establish device limits and substantial failures occurred at the next two steps (175°C and 200°C). The maximum conditions which had been tentatively selected for the life test (150°C, 160 ma) were considered acceptable.

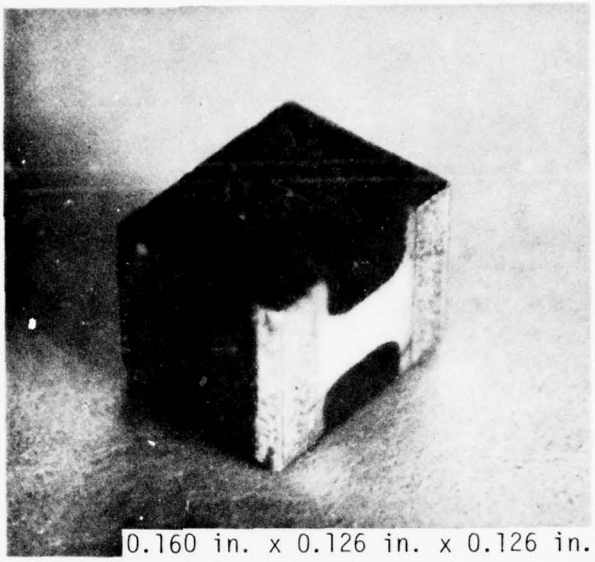

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FIGURE R1. EXTERNAL CONSTRUCTION - P/N 773058-39 - CHIP-HIGH SELF-RESONANT FREQUENCY INDUCTOR

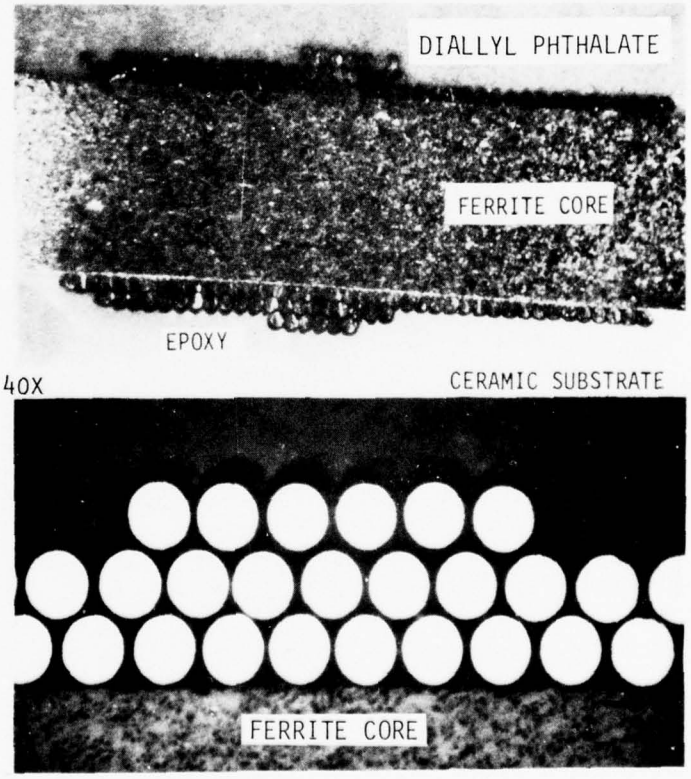

FIGURE R2. CROSS SECTIONS OF DEVICE - P/N 773058-39 - CHIP-HIGH SELF-RESONANT FREQUENCY INDUCTOR

TABLE R1. PART CONSTRUCTION DETAILS - P/N 773058-39 - HIGH SELF-RESONANT FREQUENCY INDUCTOR CHIP

A. IDENTIFICATION

1. Part Name: High Self-Resonant Frequency Inductor Chip
2. Part Number: 773058-39
3. Part Manufacturer: Piconics Inc.
4. Manufacturer's Part Number: PG153K3F

B. EXTERNAL PACKAGE

1. Type: Molded Diallyl Phthalate
2. Weight: 0.088 gram
3. Materials:

   a) Body: Diallyl Phthalate
   b) End Cap: Gold over-nickel over tungsten

C. INTERNAL

1. Materials:

   a) Core: Ferrite
   b) Windings: 0.004 inch copper wire
   c) Winding Insulation: Polynylon (Nylon covered polyurethene)

2. Interconnections:

   a) Copper wire to End Caps: Weld

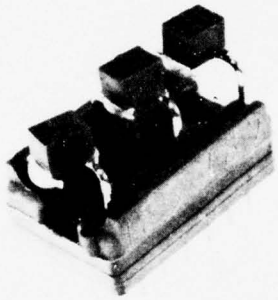

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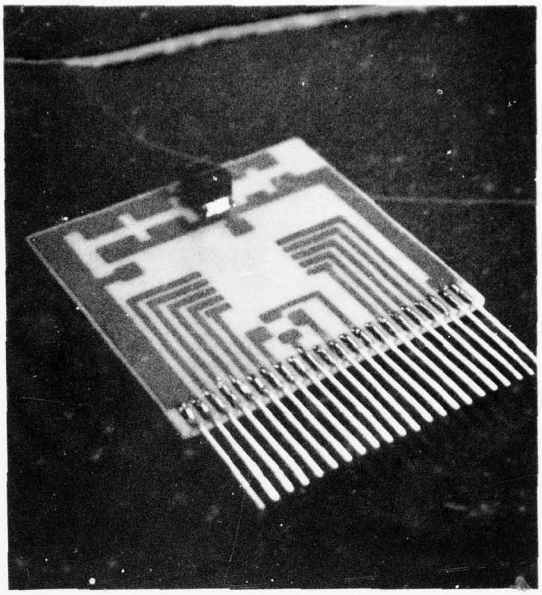
FIGURE R3. DEVICES WITH LEADS ATTACHED (TEST CONFIGURATION) - P/N 773058-39 - CHIP-HIGH SELF-RESONANT FREQUENCY INDUCTOR



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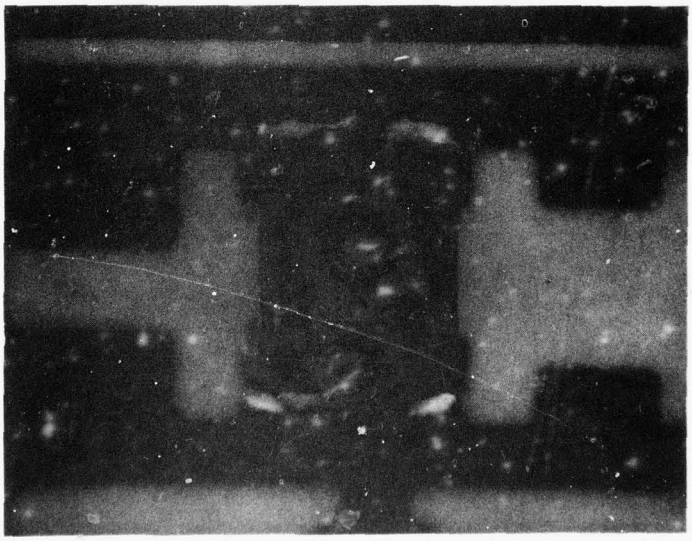
DEVICE MOUNTED ON CIRCUIT BOARD



10X

CLOSE-UP OF DEVICE

FIGURE R4. TYPICAL SAM-D CONFIGURATION - P/N 772939 - CHIP-HIGH SELF-RESONANT FREQUENCY INDUCTOR

TABLE R2. ELECTRICAL TEST CONDITIONS - P/N 773058-39 - CHIP-HIGH SELF-RESONANT FREQUENCY INDUCTOR

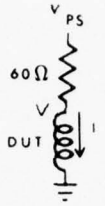
TEST NO	PARAMETER	SYMBOL	CONDITIONS	LIMITS MAX	LIMITS MIN	UNITS
1	D.C. RESISTANCE	R	-	-	2.30	Ω
2	QUALITY FACTOR	Q	f = 1.0 MHz	30	-	-
3	SELF RESONANT FREQUENCY	-	$\angle\theta = 0°$	13.0	-	MHz
4	INDUCTANCE	H	f = 1.0 MHz	13.5	16.5	μh
5	INCREMENTAL CURRENT INDUCTANCE CHANGE	-	f=1.0 MHz; D.C. BIAS CURRENT = 0 mA AND 87 mA	-	5	%
6	INDUCTANCE STABILITY	-	T = -31.7°C (1) f = 1.0 MHz	-	5	%
7	INDUCTANCE STABILITY	-	T = 85°C (2) f = 1.0 MHz	-	5	%
8	DIELECTRIC WITHSTANDING VOLTAGE	-	500 V_{rms} APPLIED BETWEEN CASE AND TERMINATIONS TIED TOGETHER	-	100	μA
9	INSULATION RESISTANCE	IR	500 Vdc APPLIED BETWEEN CASE AND TERMINATIONS TIED TOGETHER	10^4	-	MΩ

(1) THE CHANGE IN INDUCTANCE FROM 25°C TO -31.7°C DIVIDED BY THE INDUCTANCE AT 25°C.

(2) THE CHANGE IN INDUCTANCE FROM 25°C TO 85°C DIVIDED BY THE INDUCTANCE AT 25°C.

ALL TEST CONDUCTED FOR INITIAL AND FINAL TEST. TESTS 1 THROUGH 5 CONDUCTED FOR INTERIM TEST. T_A = 25°C UNLESS OTHERWISE SPECIFIED.

STEP STRESS AND LIFE TEST CIRCUIT



STEP STRESS TEST - FAILURE SUMMARY (25 DEVICES)

AMBIENT TEMP. (°C)	I (mA)	CUMULATIVE FAILURES
125	160	0
150	160	0
175	160	7
200	160	21 ⚠1

⚠1 THE FOUR REMAINING DEVICES EXHIBITED OPEN LEADS AFTER THE 200°C STEP.

TEST CELL NUMBER	T_A AMBIENT TEMPERATURE (°C)	V DEVICE VOLTAGE (VOLTS)	I DEVICE CURRENT (MILLIAMPS)	P_d POWER DISSIPATION (MILLIWATTS)	T_{IMAX} MAXIMUM INTERNAL TEMPERATURE (°C)
1	150	0.46	159	73	167
2	150	0.36	127	46	161
3	150	0	0	0	150
4	125	0.44	159	70	141
5	100	0.41	160	66	115
6	125	0	0	0	125
7	100	0	0	0	100

FIGURE R5. STEP STRESS RESULTS AND LIFE TEST CONDITIONS - P/N 773058-39 - CHIP-HIGH SELF-RESONANT FREQUENCY INDUCTOR

R6.0 LIFE TEST CONDITIONS AND RESULTS

The life test conditions for each cell are included in Figure R5 and Table R3 summarizes the life test results. The large number of catastrophic failures in Cells 1 and 2 resulted in the addition of interim measurement points to provide more resolution in failure time determination. Cells 6 and 7 (zero volts) were also added at 125°C and 100°C, respectively, to provide lower temperature data in the event that failure analysis attributed Cell 1 and 2 failures to temperature overstress. The life test duration was extended to 9000 hours for Cells 6 and 7 to provide a maximum amount of data.

Cells 1 and 2 were continued beyond the 50% failure point to provide additional failures for analysis.

R7.0 FAILURE ANALYSIS

A summary of the failure analysis results is presented in Table R4.

Inductance and Q-Factor Failures - Twenty-one (21) step stress and 71 life test parts failed due to low inductance and low Q-factor. The decrease was generally abrupt and about one order of magnitude. The decrease in Q was generally directly proportional to the decrease in inductance. Metallurgical cross sections of failed parts established that the low inductance/Q-factor was caused by deterioration of the poly-nylon insulation on the windings and short-circuits between turns and the core. Figure R6 shows a close-up of the insulation and copper wire in two failed inductors and, for comparison, a normal, unstressed inductor. The wire of S/N 187 contains no trace of insulation and S/N 70 contains only a vague cloud of insulation around the windings. The turns of wire adjacent to the core in the failed inductors were distorted and flattened against the core probably due to thermal expansions of the materials. Because the wires contained no insulation, the flattened turns shorted to the core causing an abrupt decrease in inductance and Q. The insulation of the failed inductors had diffused into the diallyl phthalate and the epoxy cement surrounding the wire. The diffusion was more severe, or at least more apparent, where the wire was embedded in the epoxy. Figure R7 shows this phenomenon. The insulation (the dark material) of S/N 35 has diffused into the epoxy and has accumulated at the epoxy/ceramic interface. The insulation of S/N 167 has diffused throughout the epoxy and all of the

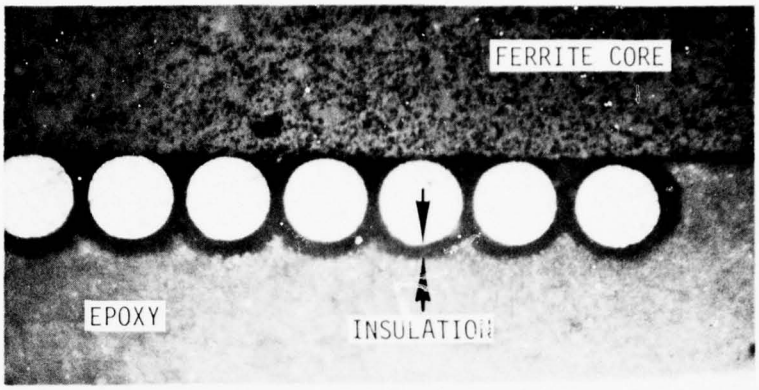
TABLE R3. LIFE TEST SUMMARY - P/N 773058-39 -
HIGH SELF-RESONANT FREQUENCY INDUCTOR CHIP

TEST CELL DESCRIPTION				CUMULATIVE FAILURES AT HOURS OF TEST																							
CELL NO.	APPLIED BIAS	AMBIENT TEMP.	QTY	4	8	16	32	64	128	144	160	176	240	256	304	512	752	1000	1500	2000	2500	3170	4000	6000	7000	8000	9000
1	MAX. VOLT.	150°C	30	0	0	3	7	12	19	21	22	23	24	--	24	26	26*										
2	MID. VOLT.	150°C	30	0	0	0	1	5	13	13	18	18	19	--	21	24	27*										
3	ZERO VOLT.	150°C	30	0	0	0	0	0	1	--	--	--	--	1	--	1	--	2	4	6	8	10	10	13*			
4	MAX. VOLT.	125°C	30	0	0	1	2	2	2	--	--	--	--	4	--	4	--	6	9	10	10	10	10	11*			
5	MAX. VOLT.	100°C	30	0	0	0	0	0	0	--	--	--	--	0	--	0	--	0	0	0	--	0	0	0	0	0	0*
6	ZERO VOLT.	125°C	30	-	-	-	-	1	2	--	--	--	--	2	--	2	--	3	3	--	4	--	4	4	4	5	5*
7	ZERO VOLT.	100°C	30	-	-	-	-	0	0	--	--	--	--	0	--	0	--	0	0	--	0	--	0	0	0	0	0*

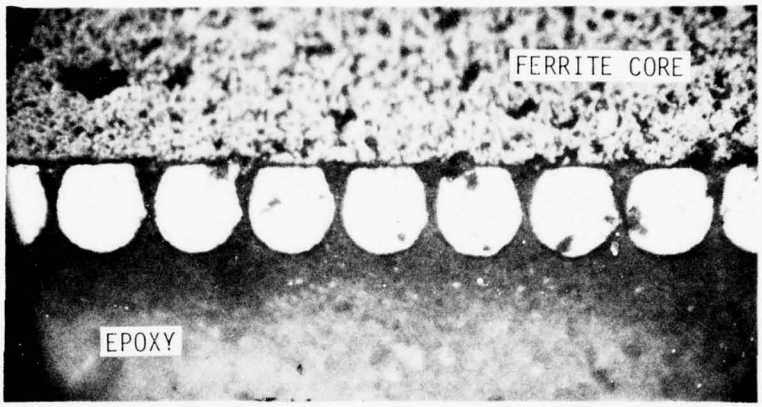
* TEST TERMINATED

TABLE R4. FAILURE ANALYSIS SUMMARY - P/N 773058-39 - HIGH SELF-RESONANT FREQUENCY INDUCTOR CHIP

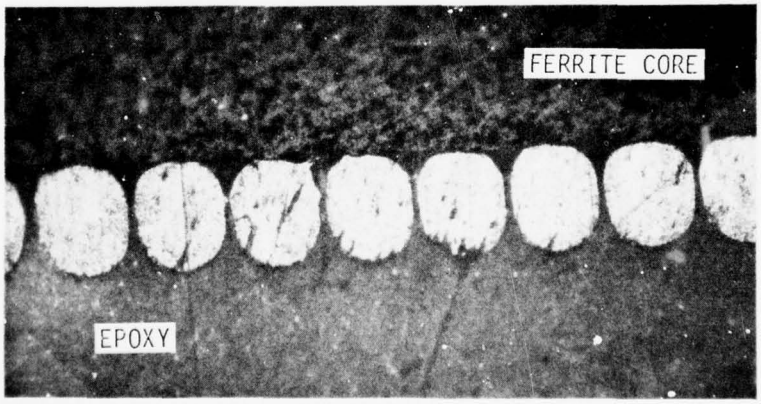
A. FAILED PARAMETERS OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TEST TIME (HOURS)							
	150°C			125°C	100°C	125°C	100°C	
	V_{MAX} CELL 1	V_{MID} CELL 2	V_O CELL 3	V_{MAX} CELL 4	V_{MAX} CELL 5	V_O CELL 6	V_O CELL 7	STEP STRESS
A. INDUCTANCE AND Q-FACTOR B. SHORTED TURNS C. DIFFUSION OF INSULATION AND THERMAL EXPANSIONS D. MATERIAL LIMITATIONS	3@16 4@32 5@64 7@128 1@144 1@160 1@176 1@240 2@512	1@32 4@64 8@128 5@160 1@240 1@304 3@512 2@752	1@128 1@1000 2@1500 2@2000 2@2500 2@3170 3@6000	1@256 2@1000 3@1500 1@2000 1@6000				7@175°C STEP 14@200°C STEP
A. INDUCTANCE B. DIELECTRIC DETIORATION C. DIFFUSION OF INSULATION D. MATERIAL LIMITATIONS PLUS INITIALLY MARGINAL INDUCTANCE						1@64 1@128 1@1000 1@2500 1@8000		
A. CATASTROPHIC B. OPEN EXTERNAL SOLDER JOINT C. GOLD SCAVENGING D. SOLDER COMPOSITION/HANDLING	1@144	1@304 1@752		1@16 1@32				4@200°C STEP
A. Q-FACTOR B. NONE (RETEST OK) C. NONE (RETEST OK) D. INTERMITTENT TEST SET INTERFACE				1@256				
TOTAL NUMBER OF FAILED PARTS	26	27	13	11	0	5	0	25



250X UNSTRESSED INDUCTOR

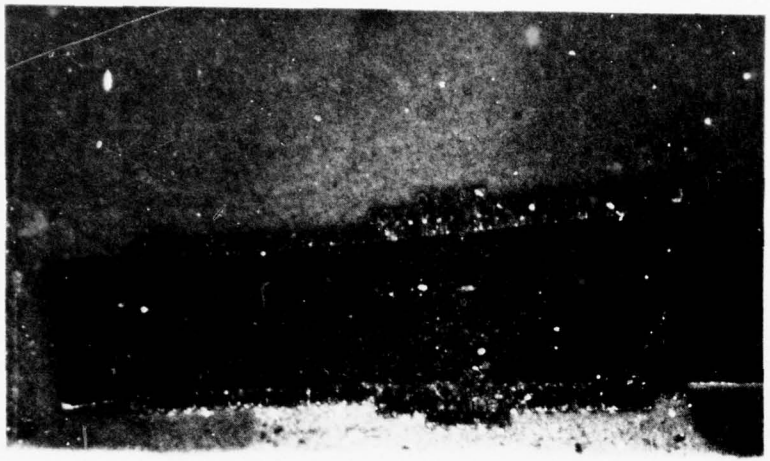


250X S/N 70: 128 HOUR, 150°C, V_{MAX} FAILURE

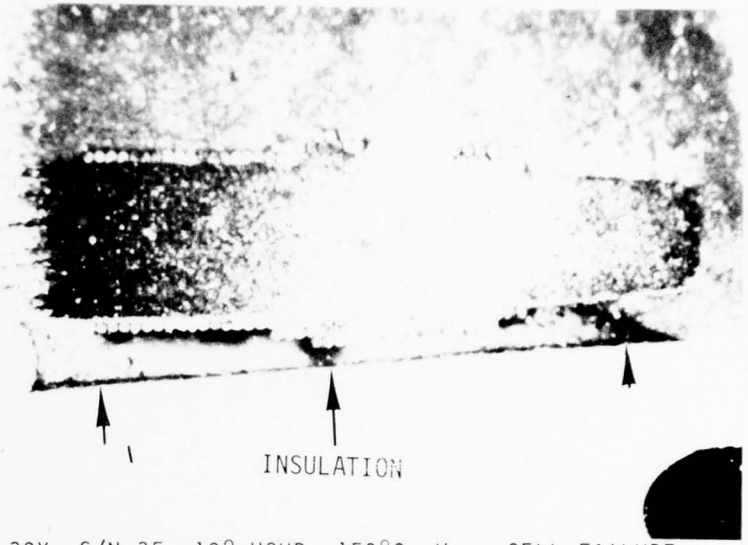


250X S/N 187: 256 HOUR, 125°C, V_{MAX} FAILURE

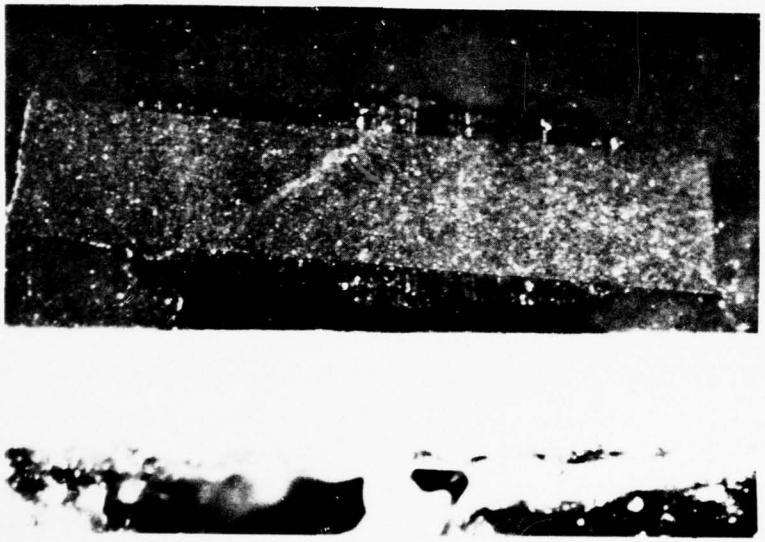
FIGURE R6. CLOSE-UP OF THE WINDINGS OF 2 FAILED INDUCTORS AND, FOR COMPARISON, AN UNSTRESSED INDUCTOR - P/N 773058-39 - CHIP-HIGH SELF-RESONANT FREQUENCY INDUCTOR



30X UNSTRESSED INDUCTOR



30X S/N 35: 128 HOUR, 150°C, V_{MAX} CELL FAILURE



30X S/N 167: 128 HOUR, 150°C, V_0 CELL FAILURE

30X S/N 187: 256 HOUR, 125°C, V_{MAX} CELL FAILURE

FIGURE R7. CROSS SECTIONS OF 3 FAILED INDUCTORS AND, FOR COMPARISON, AN UNSTRESSED INDUCTOR - P/N 773058-39 - CHIP-HIGH SELF-RESONANT FREQUENCY INDUCTOR

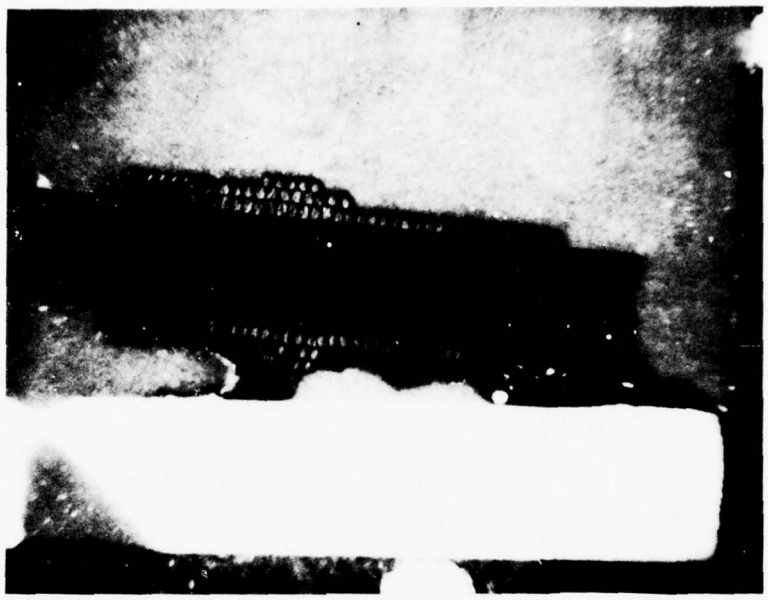
insulation of S/N 187 has diffused over to the interface. Although all of these failures occurred only in Cells 1 through 4, the mechanisms responsible for the failures (diffusion of insulation and flattening of the wires) were also occurring in Cells 5 through 7 as will be shown in the next section.

Marginal Inductance Failures - Five parts in Cell 6 failed due to marginally low inductance only. The inductance of all four parts was marginal upon receipt and during life test the inductance decreased only slightly (about 5%) and gradually. In general, all of the inductors on test showed a slight gradual decrease in inductance during life. Only these four parts which were very borderline upon receipt failed as a result of this shift. To determine the cause of the decrease and to determine if the mechanisms responsible for the failures in Cells 1 through 4 were progressing in Cells 5 through 7, these four parts and representative survivors from Cell 7 were metallurgically cross-sectioned.

The cross sections of the failed parts disclosed that the winding insulation had diffused into the epoxy cement as illustrated in Figure R8. The turns of wire adjacent to the core were flattened as shown in Figure R9, but enough insulation remained to prevent any turn from shorting to the core.

In the Cell 7 survivors the turns were flattened as shown in Figure R10 and the epoxy cement was slightly darkened as shown in Figure R11, indicating that some of the insulation probably diffused into the epoxy. These findings indicate that the slight decrease in inductance was probably caused by dielectric deterioration due to the diffusion of the insulation. This mechanism is only important if a slight decrease in inductance would affect circuit performance. More importantly the findings show that eventually, due to the diffusion and due to thermal expansion of the materials, an abrupt, possible catastrophic, drop in inductance and Q-factor will occur.

Open Leads - Four step stress parts and five life test parts failed catastrophically because one or both of the external leads broke off of the package. A tin-based solder was used to attach the external leads to the gold-plated inductor mounting tabs. After exposure to elevated temperature, the joints deteriorated due to scavenging or leaching of the gold by the solder and, as a result, the joints broke during handling of the part.



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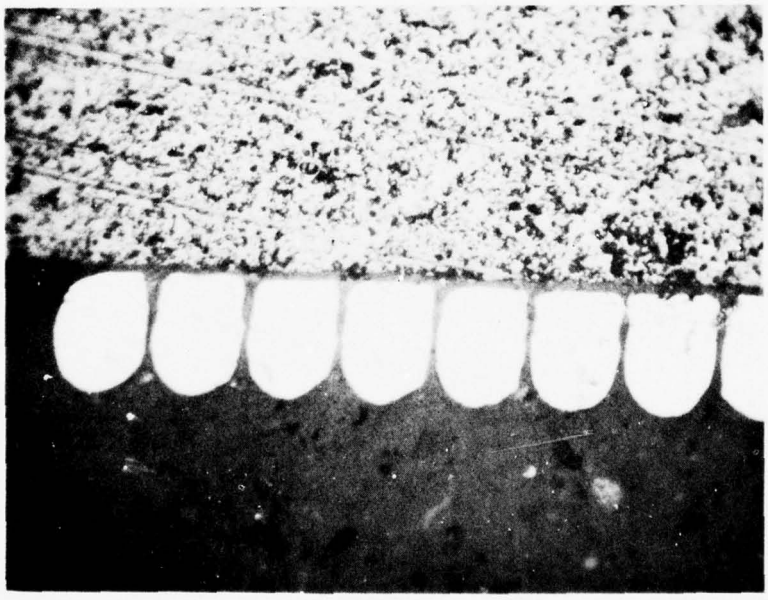
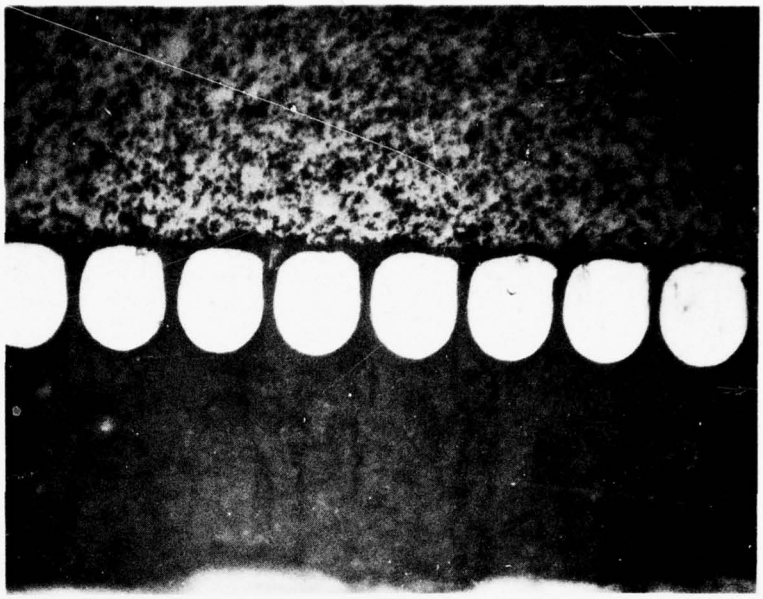
S/N 324: 64 HOUR, 125°C, V_O CELL FAILURE

FIGURE R8. CROSS SECTION OF A CELL 6 PART THAT EXHIBITED LOW INDUCTANCE ONLY SHOWING THE INSULATION DIFFUSION (THIS PART HAD BEEN LEFT ON TEST AFTER FAILING AT 64 HOURS AND THEN REMOVED AT 9000 HOURS) - P/N 773058-39 - CHIP-HIGH SELF-RESONANT FREQUENCY INDUCTOR



250X

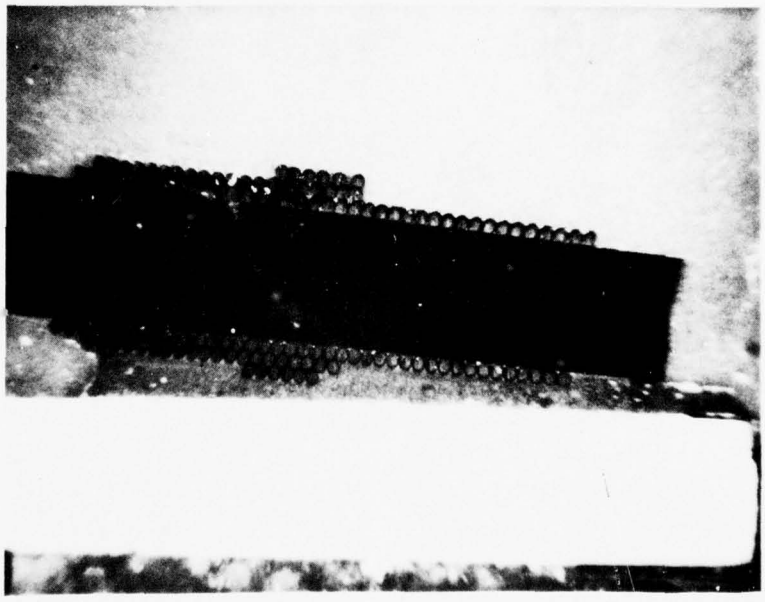
FIGURE R9. CLOSE-UP OF THE WINDINGS OF THE INDUCTOR SHOWN IN FIGURE R8 - P/N 773058-39 - CHIP-HIGH SELF-RESONANT FREQUENCY INDUCTOR



250X

S/N 343: 8000 HOUR, 100°C, V_0 CELL SURVIVOR

FIGURE R10. CROSS SECTION OF THE WINDINGS OF A CELL 7, 8000 HOUR SURVIVOR - P/N 773058-39 - CHIP-HIGH SELF-RESONANT FREQUENCY INDUCTOR



30X

S/N 344: 8000 HOURS, 100°C, V_0 CELL SURVIVOR

FIGURE R11. CROSS SECTION SHOWING THE SLIGHTLY DARKENED EPOXY CEMENT OF A CELL 7, 8000 HOUR SURVIVOR - P/N 773058-39 - CHIP-HIGH SELF-RESONANT FREQUENCY INDUCTOR

Test Error - One part in Cell 4 failed due to low Q-factor and was removed for analysis. Bench testing did not verify the failure. Subsequent investigation established that the low reading had been caused by an intermittent high impedance in the test set interface. From this point on in the test program, parts exhibiting low Q-factor only were bench tested immediately and any part found to have failed due to interface intermittencies was put back on test.

R8.0 DATA CORRELATION

The Table R4 failure analysis summary shows insulation diffusion and thermal expansion as the primary failure mechanism. Since this mechanism occurred primarily in Cells 1 through 4, the highest temperature test cells, there was concern that the parts were failing due to a test induced overstress condition. Therefore, two unpowered test cells, Cells 6 and 7, were added to the test program to provide lower temperature (125°C and 100°C) data. Cells 6 and 7 accumulated 9000 hours with none of the catastrophic failures typical of Cells 1 through 4. However, Cell 6 (125°C) experienced five inductance failures attributed to the same insulation diffusion mechanism experienced in Cells 1 through 4. Internal examination of some Cell 7 (100°C) survivors revealed the onset of the same insulation diffusion mechanism. Since the preliminary part drawing, 773058, identifies a maximum operating temperature limit of 125°C, the Cell 6 and 7 results show the insulation degradation mechanism occurs within the part temperature limits and is therefore, a valid mechanism for analysis.

Five other life test failures were caused by degradation of the MDAC-East installed test leads. Since these leads were installed for test purposes only, and are not typical of SAM-D usage, these five failures were discounted for data analysis purposes.

Data analysis was focused on the Cells 1 through 4 catastrophic failures. Since failure time interpolation was not possible, failures were assumed to have occurred at the midpoint of the measurement interval. [Note: When catastrophic failures were encountered, the measurement intervals were shortened to allow more precise failure time estimates.] The lognormal failure distribution and the Arrhenius model have been used previously to describe insulation life characteristics [R1].

This approach was investigated and found to adequately represent the data. Figures R12 and R13 shows Cells 1 through 4 cumulative failure distributions on lognormal probability paper. No "freak", or early failure, population is discernable. The pertinent data is summarized in Table R5. Note that Cells 1, 2 and 3, although at the same ambient temperature, had different internal temperatures; therefore, four temperature data points were available for the Arrhenius evaluation. The Figure R14 Arrhenius plot includes the four data points; however, the Arrhenius relationship was defined using the Cell 1, 2 and 4 data because they provided the lowest activation energy and, consequently, the most conservative estimate of median life. The Arrhenius equation can be represented as follows:

$$\ln t_{50\%} = -73.129 + \frac{2.93}{kT}$$

Storage failure rates can be calculated using the following equation and the "pooled" value for standard deviation:

$$\lambda(t) = \frac{f(t)}{R(t)}$$

$$= \frac{\frac{1}{t} \exp - \frac{\left[\ln t + 73.129 - \frac{2.93}{kT}\right]^2}{2(1.46)^2}}{\int_t^\infty \frac{1}{t'} \exp \left[\frac{\left[\ln t' + 73.139 - \frac{2.93}{kT}\right]^2}{2(1.46)^2} \right] dt'}$$

The calculated $\lambda(t)_{MAX}$ is 4.4×10^{-10} failures per hour.

R9.0 CONCLUSIONS AND RECOMMENDATIONS

- Although the calculated failure rate (4.4×10^{-10} failures per hour) appears to be an acceptable number, the detected onset of the insulation diffusion failure mechanism in the 100°C test cell requires further investigation of lot-to-lot variability. This part should be considered marginal for extended usage or storage at part temperatures of 100°C or greater.
- The nature of the insulation degradation failure mechanism and the lack of a discernable freak population would indicate that a high temperature (100%) screening test is not appropriate. However, a high temperature sampling inspection test would serve to identify marginal lots.

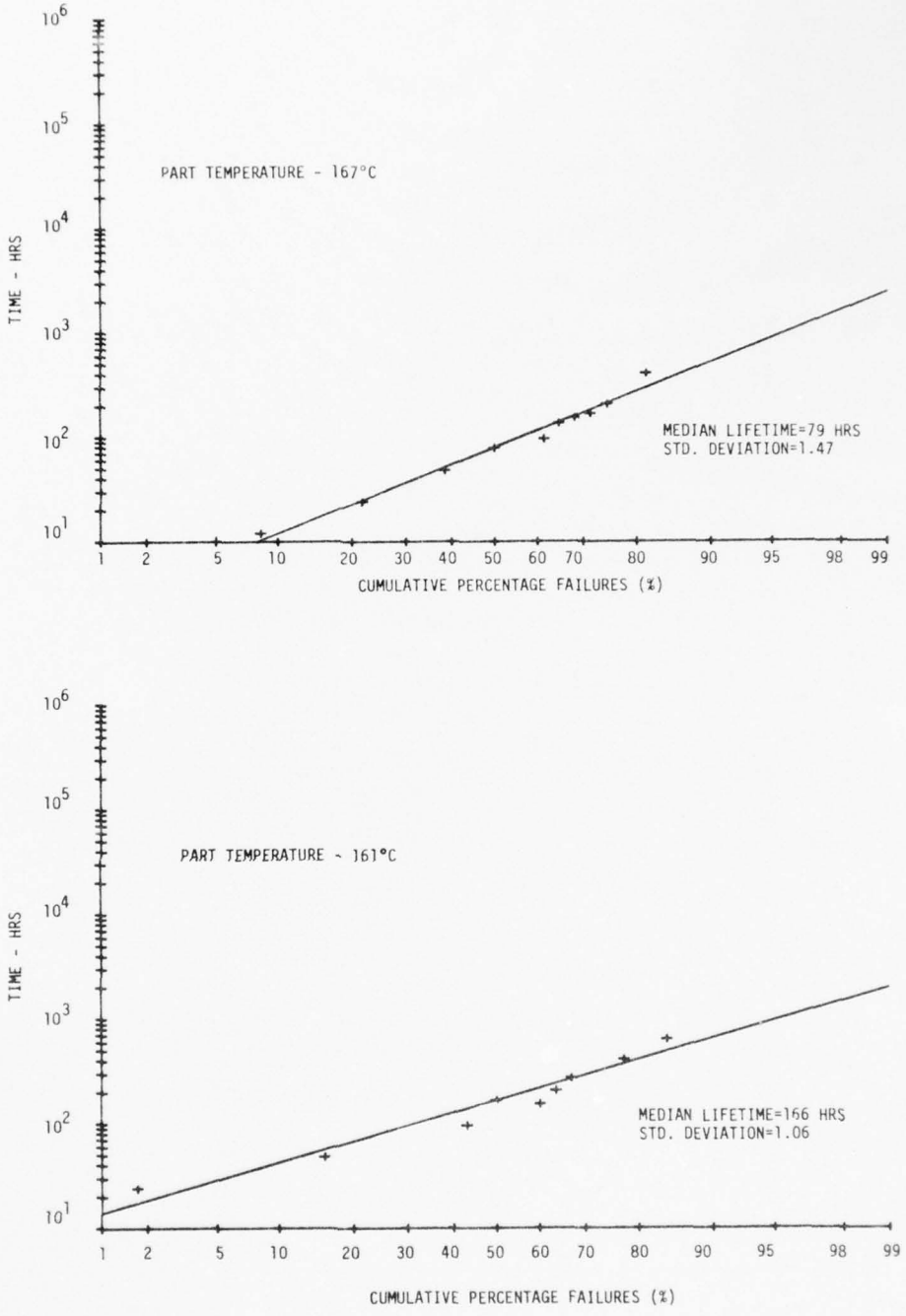


FIGURE R12. CUMULATIVE FAILURE DISTRIBUTION FOR CELL 1 (TOP) AND CELL 2 (BOTTOM) - P/N 773058-39 - HIGH SELF-RESONANT FREQUENCY INDUCTOR CHIP

AD-A039 788 MCDONNELL DOUGLAS ASTRONAUTICS CO-EAST ST LOUIS MO F/G 9/1
STORAGE RELIABILITY OF MISSILE MATERIEL (ACCELERATED TESTING OF--ETC(U)
APR 77 J MCGARRY, V WEISSFLUG, E SISUL DAAH01-74-C-0928
UNCLASSIFIED MDC-E1601 NL

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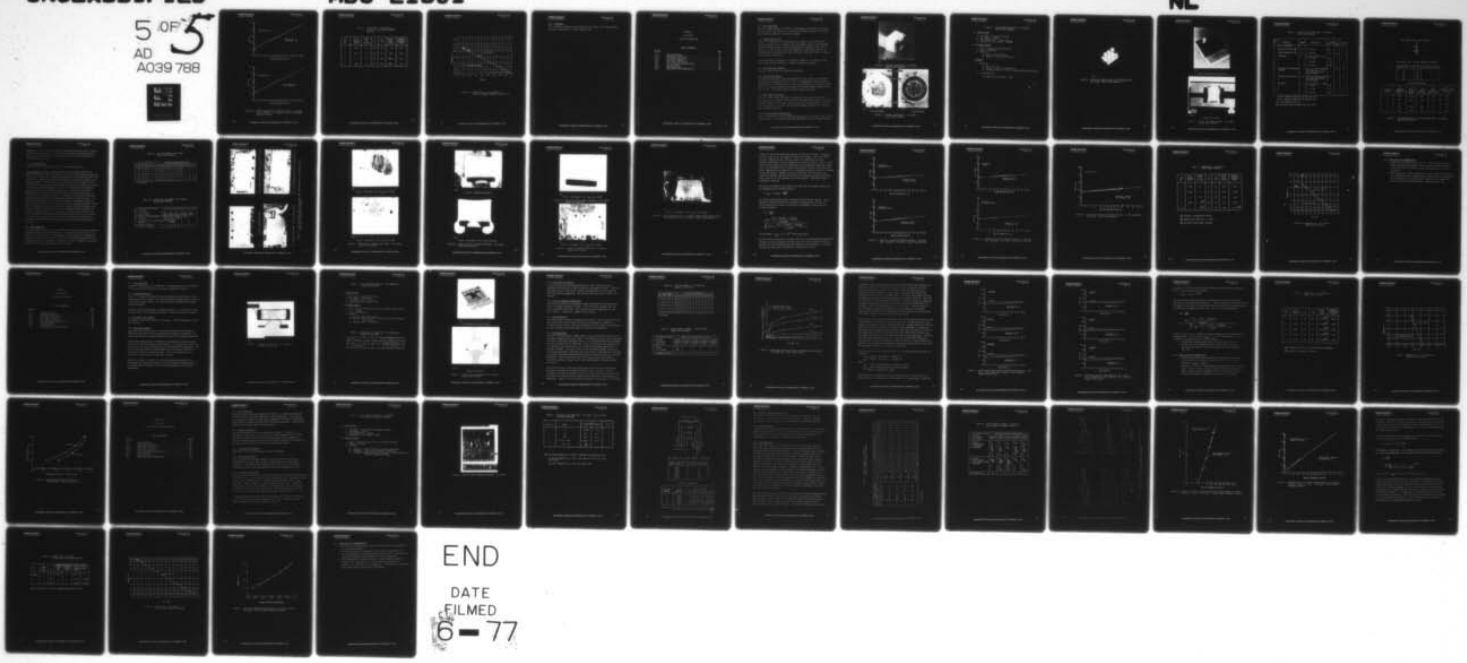
A039 788



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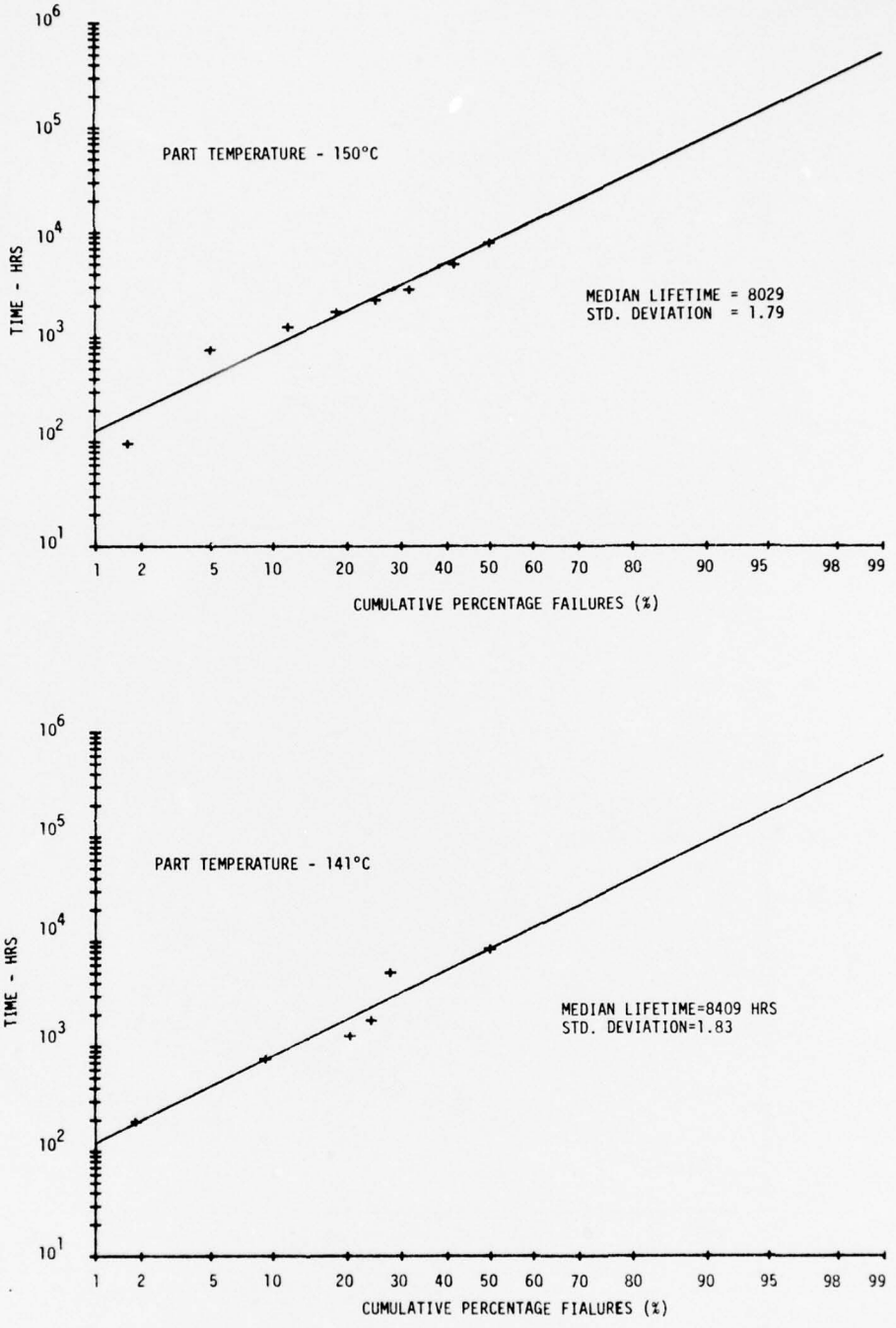

FIGURE R13. CUMULATIVE FAILURE DISTRIBUTION FOR CELL 3 (TOP) AND CELL 4 (BOTTOM) - P/N 773058-39 - HIGH SELF-RESONANT FREQUENCY INDUCTOR

TABLE R5. SUMMARY DATA - P/N 773058-39 - CHIP-HIGH SELF-RESONANT FREQUENCY INDUCTOR

CELL NO.	TEST VOLTAGE (VOLTS)	NUMBER OF FAILURES	T_A (°C)	$T_{INT.}$ (°C)	MEDIAN LIFE (HOURS)	STANDARD DEVIATION (HOURS)
1	0.46	25	150	167	79	1.47
2	0.36	25	150	161	166	1.06
3	0	13	150	150	8029	1.79
4	0.44	8	125	141	8409	1.83

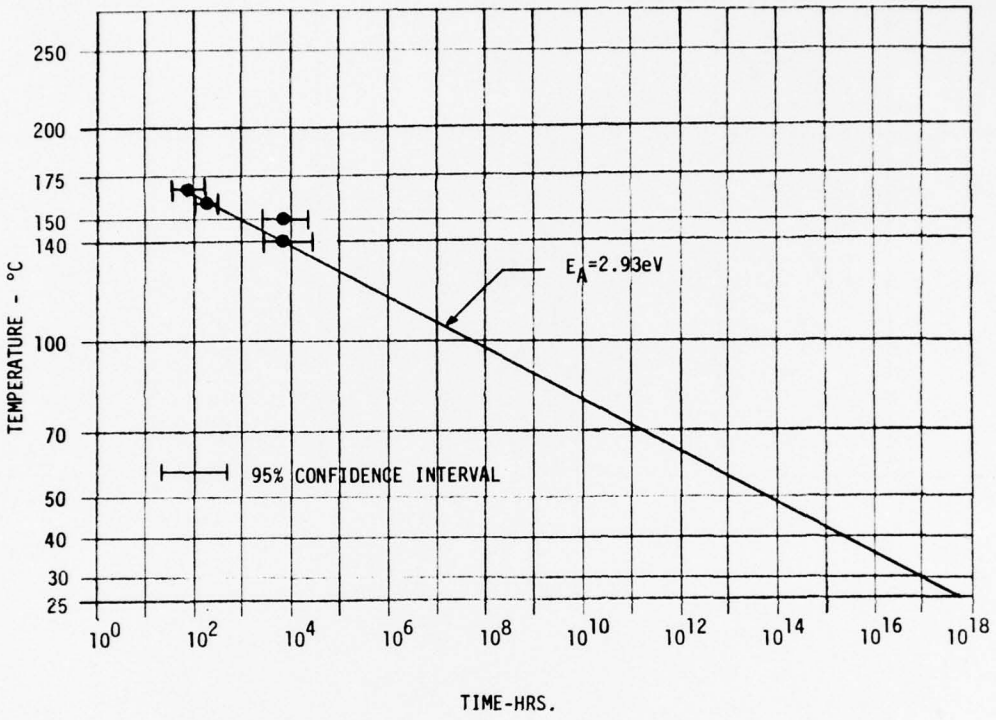

FIGURE R14. ARRHENIUS PLOT - P/N 773058-39 -
HIGH SELF-RESONANT FREQUENCY INDUCTOR CHIP

R10.0 REFERENCES

[R1] W. Nelson, "Analysis of Accelerated Life Test Data", IEEE Transactions on Electrical Insulation, pp. 165-181, December 1971.

APPENDIX S

P/N 773059

FERRITE BEAD INDUCTOR

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S1.0 PART DESCRIPTION

The Ferrite Bead Inductor, P/N 773059, is manufactured by Piconics Incorporated. The test devices were delivered in chip form as depicted in Figure S1, and leads were attached by MDAC-EAST for the test program.

S2.0 CONSTRUCTION ANALYSIS

Table S1 is a summary of the pertinent physical details of this device while Figure S2 provides a cross sectional view of the device and an x-ray enlargement. The encapsulating material is diallyl phthalate which imposed a 175°C limit on testing. In order to apply bias it was necessary to attach leads and this was accomplished by soldering nickel leads to the parts using 221°C solder. Figure S3 shows the test configuration.

The typical SAM-D configuration is pictured in Figure S4. It consists of the ferrite bead inductor soldered to a ceramic printed circuit board.

S3.0 ELECTRICAL TEST CRITERIA

Table S2 lists the electrical tests for this device.

S4.0 BIAS CIRCUIT ANALYSIS

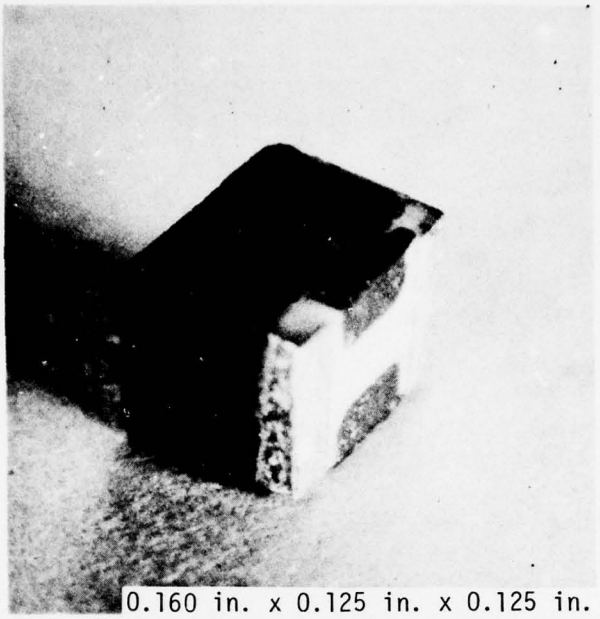
The device was operated at the maximum rated DC current, 200 mA, as the ambient temperature was elevated from 25°C to 175°C. The temperature rise due to power dissipation at 175°C ambient was 1°C. This was not enough rise to restrict testing below 175°C, which was tentatively selected as the maximum ambient temperature for the life test. The maximum electrical limit selected was 200 mA.

S5.0 STEP STRESS TEST RESULTS

Twenty-five devices were subjected to a step stress test consisting of four 16 hour steps at 25°C intervals starting at 125°C and concluding at 200°C. No failures occurred through the 175°C step. The step stress test is summarized in Figure S5. The maximum conditions for the life test which had been selected (175°C, 200 mA) were considered acceptable.

S6.0 LIFE TEST CONDITIONS AND RESULTS

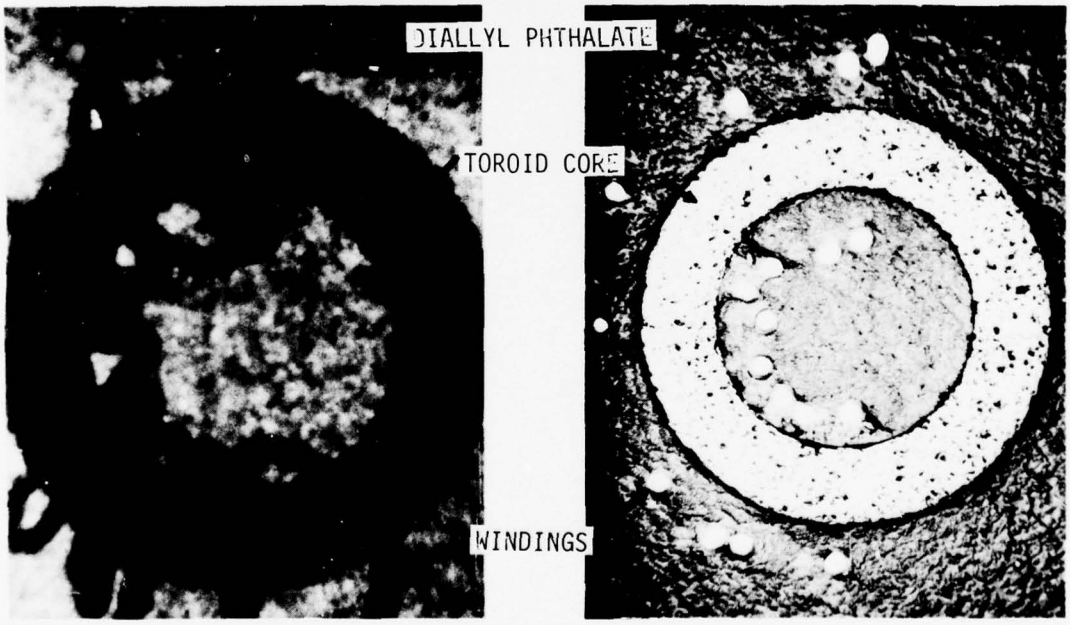
Figure S5 includes the life test conditions for each cell. As shown in the Table S3 Summary, Cells 1, 2 and 3 were halted after 2000 hours with 25, 23 and 26 failures



0.160 in. x 0.125 in. x 0.125 in.

8X

FIGURE S1. EXTERNAL CONSTRUCTION - P/N 773059 - FERRITE BEAD INDUCTOR



37X

X-RAY ENLARGEMENT

30X

CROSS SECTION

FIGURE S2. INTERNAL CONSTRUCTION - P/N 773059 - FERRITE BEAD INDUCTOR

TABLE S1. PART CONSTRUCTION DETAILS - P/N 773059 - FERRITE BEAD INDUCTOR

A. IDENTIFICATION

1. Part Name: Ferrite Bead Inductor
2. Part Number: 773059
3. Part Manufacturer: Piconics Inc.
4. Manufacturer's Part Number: PG272K0F

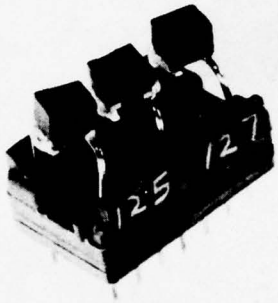
B. EXTERNAL PACKAGE

1. Type: Molded Diallyl Phthalate Chip
2. Weight: 0.088 gram
3. Materials:
   a) Body: Diallyl Phthalate
   b) End Caps: Nickel over tungsten

C. INTERNAL

1. Materials:
   a) Core: Ferrite
   b) Windings: 0.004 inch copper wire
   c) Winding Insulation: Polynylon (Nylon covered polyurethene)

2. Interconnections:
   a) Copper Wire to End Caps: Weld

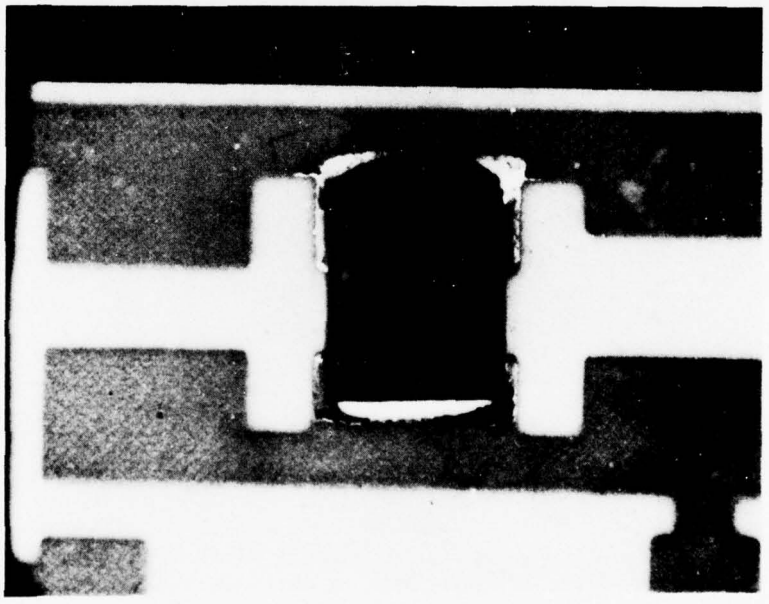


1.6X

FIGURE S3. DEVICE WITH LEADS ATTACHED (TEST CONFIGURATION) - P/N 773059 - FERRITE BEAD INDUCTOR

1.9X

DEVICE MOUNTED ON CIRCUIT BOARD



8.5X

CLOSE-UP OF DEVICE

FIGURE S4. TYPICAL SAM-D CONFIGURATION - P/N 772940 - FERRITE BEAD INDUCTOR

TABLE S2. ELECTRICAL TEST CONDITIONS - P/N 773059 - FERRITE BEAD INDUCTOR

TEST NO	PARAMETER	SYMBOL	CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
1	D. C. RESISTANCE	R	-	-	0.15	Ω
2	SERIES RESISTANCE ⚠1	R_S	f = 60 MHz	200	-	Ω
3	SERIES REACTANCE ⚠1	X_S	f = 60 MHz	55	195	Ω
4	IMPEDANCE	Z	DC BIAS CURRENT = 0 mA f = 10 MHz	50	-	Ω
5			f = 40 MHz	150	-	Ω
6			f = 60 MHz	200	-	Ω
7	DIELECTRIC WITHSTANDING VOLTAGE	-	500 V_{rms} APPLIED BETWEEN CASE AND TERMINATIONS TIED TOGETHER	-	100	μA
8	INSULATION RESISTANCE	IR	500 Vdc APPLIED BETWEEN CASE AND TERMINATIONS TIED TOGETHER	10^4	-	MΩ
9	IMPEDANCE	Z	DC BIAS CURRENT = 100mA f = 10 MHz	35	-	Ω
10			f = 40 MHz	110	-	Ω
11			f = 60 MHz	150	-	Ω

ALL TESTS CONDUCTED FOR INITIAL AND FINAL TEST.

TESTS 1 THROUGH 6 CONDUCTED FOR INTERIM TESTS.

ALL TESTS CONDUCTED AT 25°C.

⚠1 CALCULATED USING IMPEDANCE AND PHASE ANGLE.

STEP STRESS AND LIFE TEST CIRCUIT

STEP STRESS TEST - FAILURE SUMMARY (25 DEVICES)

AMBIENT TEMP (°C)	I (mA)	CUMULATIVE FAILURES
125	200	0
150	200	0
175	200	0
200	200	1

LIFE TEST CONDITIONS

TEST CELL NUMBER	T_A AMBIENT TEMPERATURE (°C)	V DEVICE VOLTAGE (VOLTS)	I DEVICE CURRENT (MILLIAMPS)	P_d POWER DISSIPATION (MILLIWATTS)	T_{IMAX} MAXIMUM INTERNAL TEMPERATURE (°C)
1	175	0.032	200	6.4	176
2	175	0.024	150	3.6	176
3	175	0	0	0	175
4	150	0.030	200	6.0	151
5	125	0.029	200	5.8	126

FIGURE S5. STEP STRESS RESULTS AND LIFE TEST CONDITIONS - P/N 773059 - FERRITE BEAD INDUCTOR

respectively. These cells were allowed to continue beyond 50% failure to provide additional data for analysis. As the failure degradation trend became apparent, additional measurement times were incorporated to provide more resolution for failure time determination.

S7.0 FAILURE ANALYSIS

A summary of the failure analysis results is presented in Table S4.

Series Reactance Failures - Seventy-eight (78) life test parts failed due to low series reactance. Metallurgical cross sections of failed inductors established that the low reactances were caused by deterioration of the winding insulation and short-circuits between turns and the core identical to that which occurred in the 773058-39 inductor. Figure S6 shows that the insulation on the copper wire had diffused into the epoxy cement (used to attach the toroid to the ceramic substrate) as indicated by the dark appearance of the epoxy in the three failed inductors compared to that of the unstressed inductor. As a result of the insulation deterioration and thermal expansion of the materials, turns had shorted to the toroid core as illustrated in Figure S7. In addition to the failure mechanisms, other types of deterioration was observed, particularly in the 175°C parts. The diallyl phthalate of most of the parts had shrunk, as illustrated in Figure S8, and its color had changed from blue to grey. One part examined contained a cracked ceramic substrate as shown in Figure S9 and two parts contained a cracked toroid core as illustrated in Figure S10. All of the reactance failures occurred only in Cells 1 through 4 (at 175°C or 150°C), but cross sections of survivors from Cell 5 showed that the same mechanisms were progressing at 125°C. As illustrated in Figure S11, the epoxy was slightly discolored indicating that some of the insulation probably diffused into the epoxy cement and one turn had shorted to the core.

S8.0 DATA CORRELATION

The Table S4 failure analysis summary attributes all failures to the same mechanisms, insulation diffusion and thermal expansions. These results are similar to those discussed in paragraph R9.0 for P/N 773058-39, and the same analysis methods were generally followed. One distinction is that this ferrite bead inductor exhibited a degradation pattern as opposed to catastrophic failure. Therefore, interpolation techniques were used to estimate device failure times.

TABLE S3. LIFE TEST SUMMARY - P/N 773059 - FERRITE BEAD INDUCTOR

TEST CELL DESCRIPTION				CUMULATIVE FAILURES AT HOURS OF TEST													
CELL NO	APPLIED BIAS	AMB. TEMP.	QUANTITY	4	8	16	32	64	128	256	512	1000	1500	2000	2500	3000	4000	6000
1	MAX VOLT	175°C	30	0	0	0	0	0	0	0	0	5	23	25*				
2	MID VOLT	175°C	30	0	0	0	0	0	1	1	1	8	20	23*				
3	ZERO VOLT	175°C	30	0	0	0	0	0	0	0	0	8	26	26*				
4	MAX VOLT	150°C	30	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4*
5	MAX VOLT	125°C	30	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0*

* TEST TERMINATED

TABLE S4. FAILURE ANALYSIS SUMMARY - P/N 773059 - FERRITE BEAD INDUCTOR

A. FAILED PARAMETERS OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TIME (HOURS) OF FAILURES				
	V_{MAX} CELL 1	V_{MID} CELL 2	V_0 CELL 3	V_{MAX} CELL 4	V_{MAX} CELL 5
A. LOW EQUIVALENT SERIES REACTANCE	5@1000	1@128	8@1000	4@6000	
B. SHORTED TURNS	18@1500	7@1000	18@1500		
C. DIFFUSION OF INSULATION AND THERMAL EXPANSIONS	2@2000	12@1500 3@2000			
D. MATERIAL LIMITATIONS					
TOTAL NUMBER OF FAILED PARTS	25	23	26	4	0

57X S/N 28: 1500 HOURS, 175°C, V_{MAX} CELL FAILURE

57X S/N 175: 6000 HOURS, 150°C, V_{MAX} CELL FAILURE

57X S/N 193: UNSTRESSED CHOKE

57X S/N 94: 1000 HOURS, 175°C, V_O CELL FAILURE

FIGURE S6. CROSS SECTIONS OF THREE FAILED CHOKES AND, FOR COMPARISON, AN UNSTRESSED CHOKE - P/N 773059 - FERRITE BEAD INDUCTOR

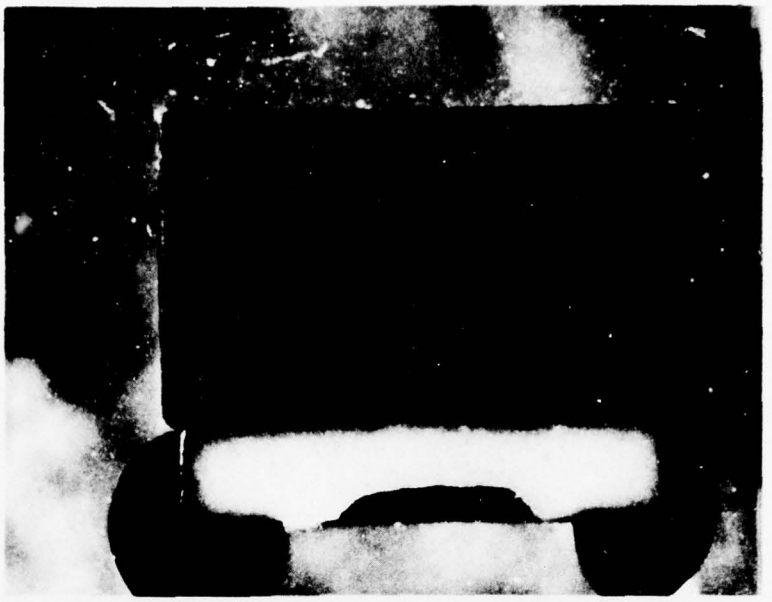
400X

S/N 38: 1000 HOUR, 175°C, V_{MAX} CELL FAILURE

400X

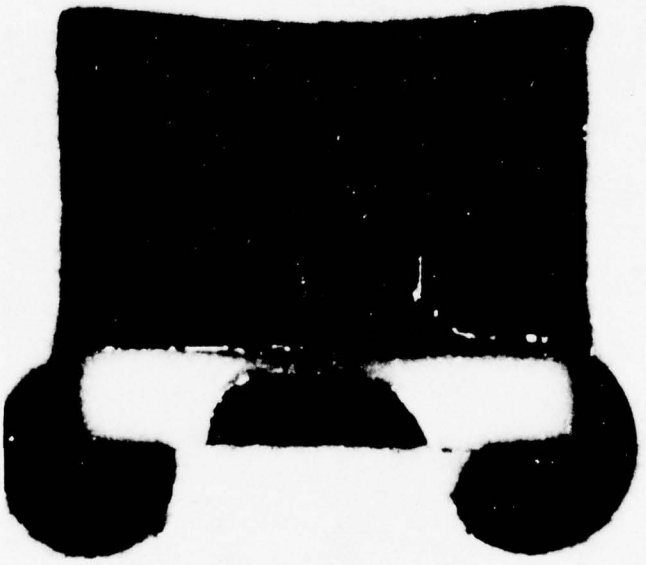
S/N 94: 1000 HOURS, 175°C, V_0 CELL FAILURE

FIGURE S7. TWO EXAMPLES OF TURN-TO-CORE SHORTS - P/N 773059 - FERRITE BEAD INDUCTOR



20X

S/N 193: UNSTRESSED INDUCTOR



20X

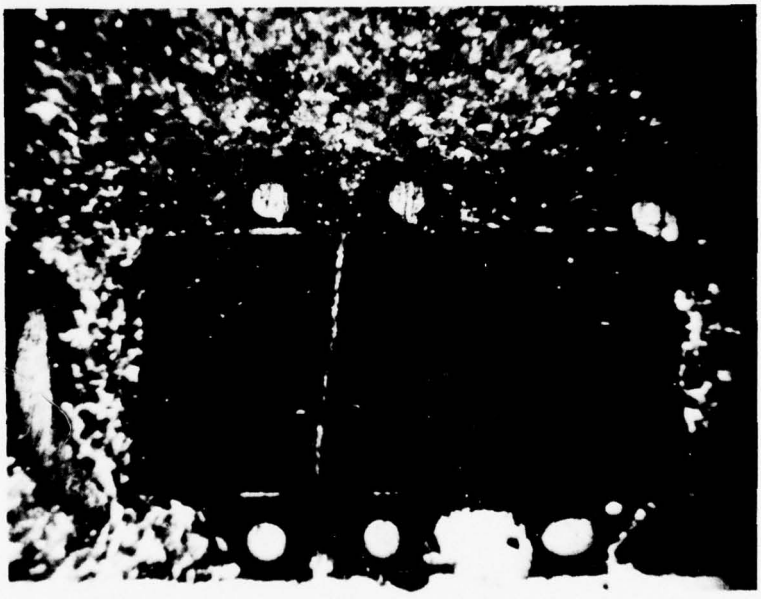
S/N 94: 1000 HOURS, 175°C, V_0 CELL FAILURE

FIGURE S8. EXAMPLE OF DIALLYL PHTHALATE SHRINKAGE - P/N 773059 - FERRITE BEAD INDUCTOR

20X

S/N 38: 1000 HOURS, 175°C, V_{MAX} CELL FAILURE

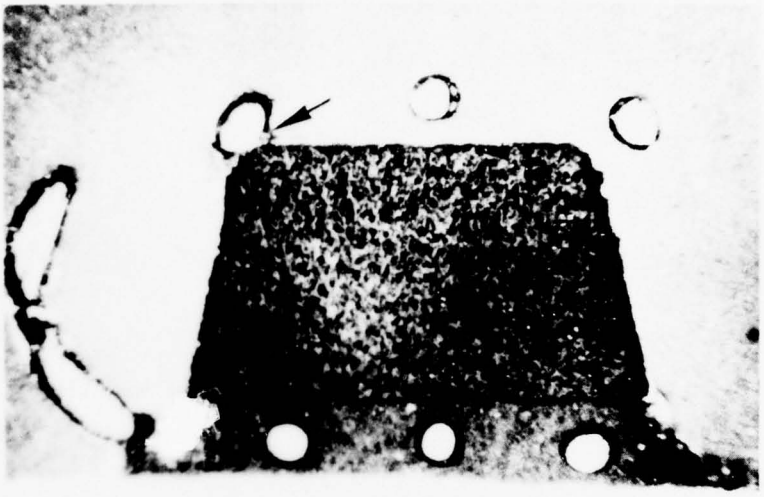
FIGURE S9. PART WITH CRACKED CERAMIC SUBSTRATES - P/N 773059 - FERRITE BEAD INDUCTOR



57X

S/N 38: 1000 HOURS, 175°C, V_{MAX} CELL FAILURE

FIGURE S10. EXAMPLE OF CRACKED TOROID CORE - P/N 773059 - FERRITE BEAD INDUCTOR



57X

S/N 191: 6000 HOURS, 125°C, V_{MAX} CELL SURVIVOR

FIGURE S11. CROSS SECTION OF A CELL 5 SURVIVOR SHOWING SHORTED TURN (ARROWS) AND DISCOLORED EPOXY - P/N 773059 - FERRITE BEAD INDUCTOR

Figures S12 and S13 are cumulative lognormal failure plots for Cells 1 through 4. All show a good fit for the lognormal failure distribution. Cell 4, the 150°C test cell, experienced four failures; however, five additional parts were degrading sufficiently to allow extrapolation of times to failure. Cells 1, 2 and 3 were at approximately the same temperature and provided almost identical results. Cell 3, the unbiased test cell, had the lowest median lifetime of the three 175°C cells, suggesting that voltage was not an accelerator and had little or no influence on the test outcome. Therefore, the data of the three 175°C test cells were combined for analysis purposes and the Figure S14 cumulative failure distribution shows a good fit for the lognormal failure distribution. Distribution data is summarized in Table S5.

The Figure S15 Arrhenius plot, based on the 150°C and 175°C median lifetimes can be represented by the following equation:

$$\ln t_{50\%} = -26.5936 + \frac{1.3064}{kT}$$

The "pooled" technique was used to calculate the distribution variance. Having defined the failure distribution, the median lifetime and the variance, the following equation was used to calculate the instantaneous failure rate for a storage environment:

$$\lambda(t) = \frac{f(t)}{R(t)}$$

$$= \frac{\frac{1}{t} \exp - \frac{[\ln t + 26.5936 - 1.3064(\frac{1}{kT})}{2(0.32)^2}}{\int_t^\infty \frac{1}{t'} [\exp - \frac{[\ln t' + 26.5936 - 1.3064(\frac{1}{kT})}{2(0.32)^2}] \, dt'}$$

The calculated $\lambda(t)_{MAX}$ is 5.1×10^{-14} failures per hour.

The preliminary specification stipulates 125°C as the maximum operating temperature. Although no failures occured in the 125°C test cell, cross sections of survivors from that test cell showed that the same mechanisms were progressing. This would indicate that additional investigation is required for this part.

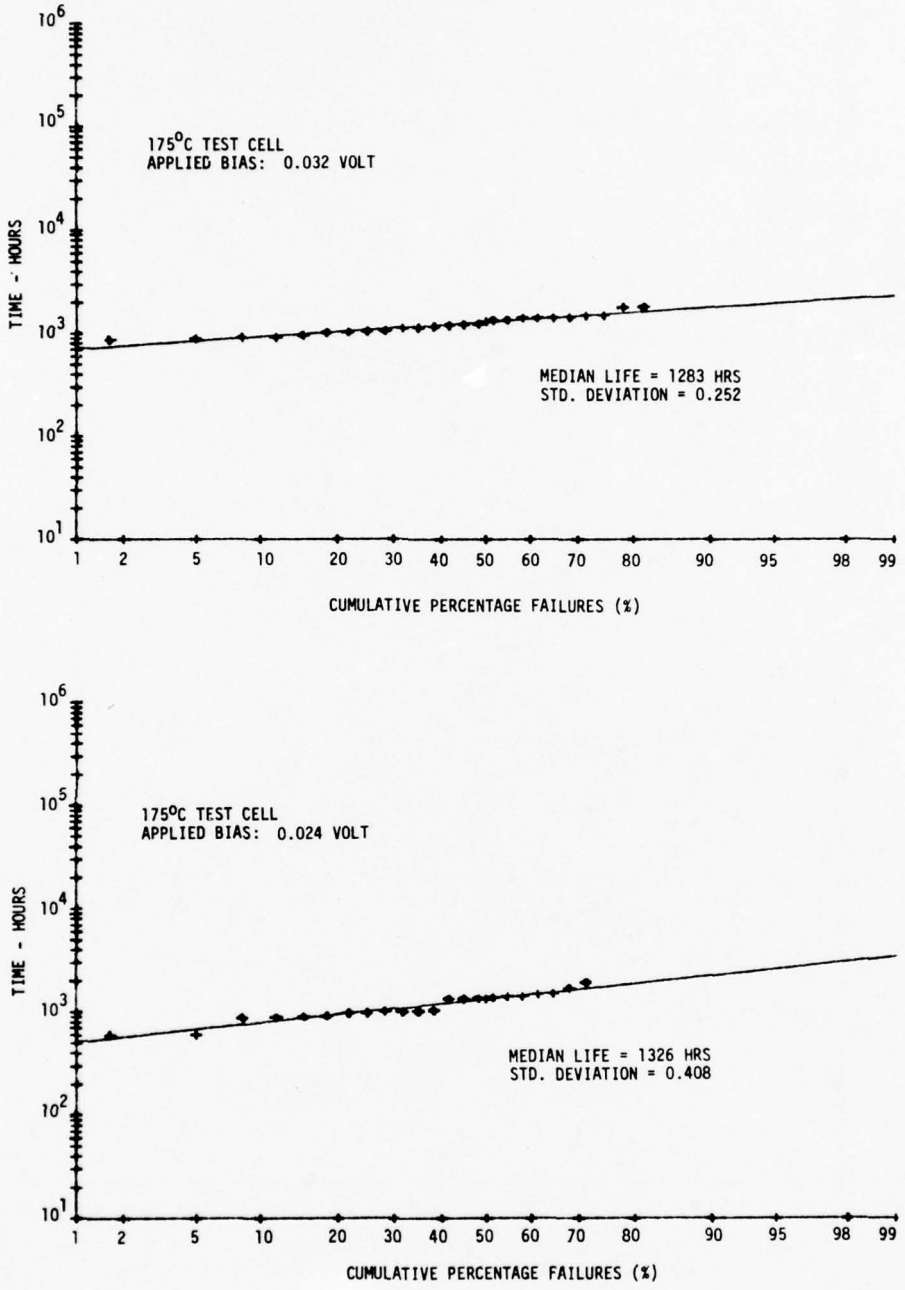


FIGURE S12. CUMULATIVE FAILURE DISTRIBUTION FOR CELL 1 (TOP) AND CELL 2 (BOTTOM) - P/N 773059 - FERRITE BEAD INDUCTOR

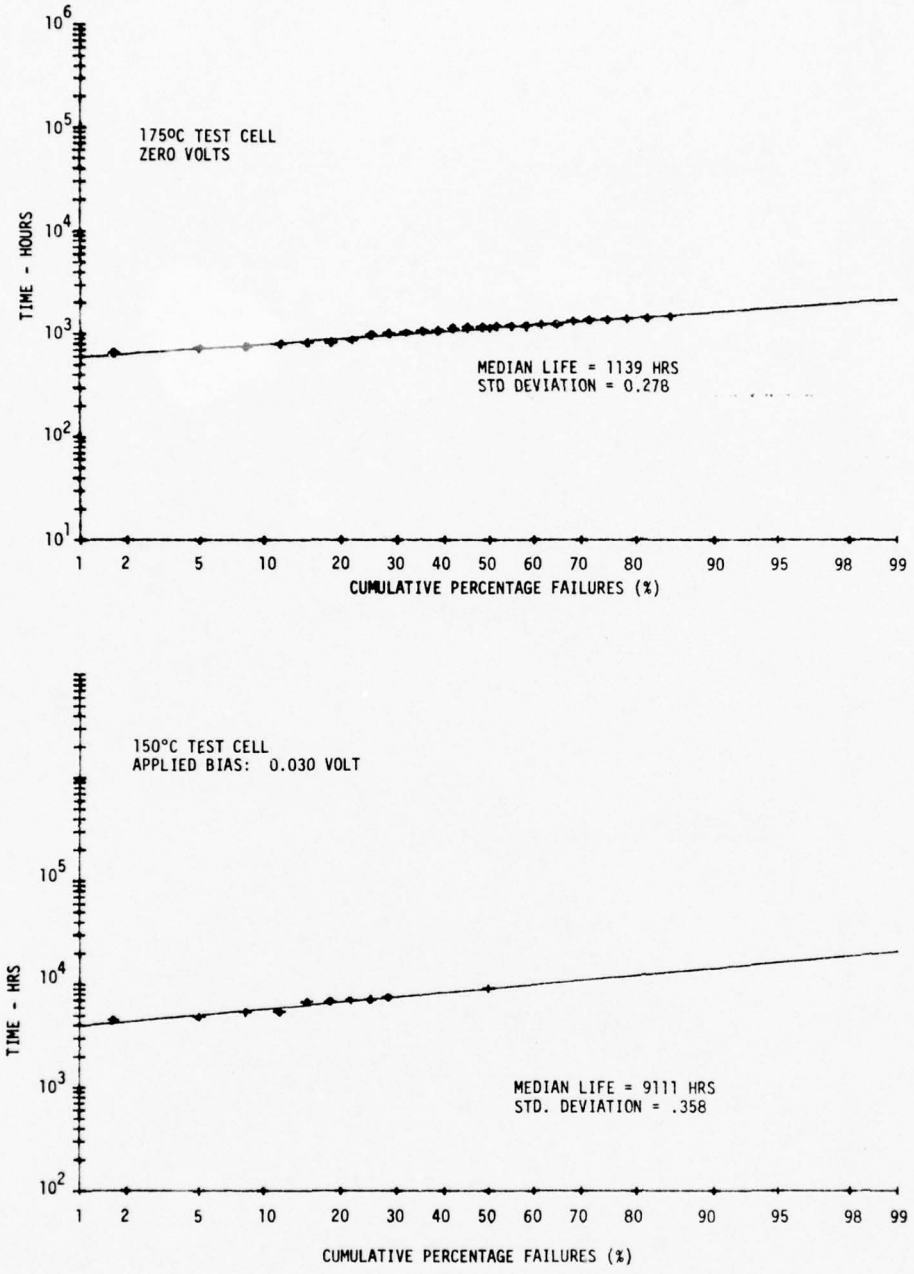


FIGURE S13. CUMULATIVE FAILURE DISTRIBUTION FOR CELL 3 (TOP) AND CELL 4 (BOTTOM) - P/N 773059 - FERRITE BEAD INDUCTOR

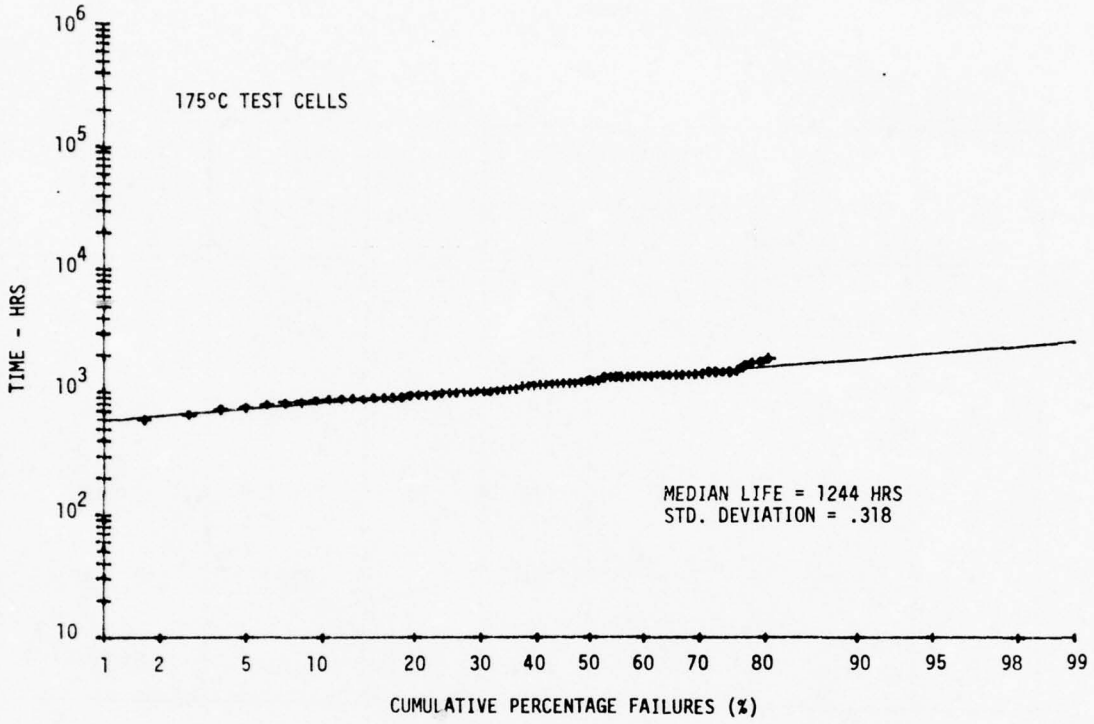


FIGURE S14. CUMULATIVE FAILURE DISTRIBUTION FOR CELLS 1, 2 AND 3 COMBINED - P/N 773059 - FERRITE BEAD INDUCTOR

TABLE S5. SUMMARY DATA - P/N 773059 - FERRITE BEAD INDUCTOR

CELL NO.	TEST VOLTAGE (VOLTS)	NUMBER OF FAILURES	T_A (°C)	T_{INT} (°C)	MEDIAN LIFE (HOURS)	STANDARD DEVIATION (HOURS)
1	0.032	25	175	176	1283	0.252
2	0.024	23	175	176	1326	0.408
3	0	26	175	175	1139	0.278
4	0.030	9 (1)	150	151	9111	0.358
1,2,3	---	74 (2)	175	176	1244	0.317 (3)

(1) INCLUDES 5 EXTRAPOLATED FAILURES

(2) COMBINED DATA FROM CELLS 1, 2 AND 3

(3) CALCULATED USING POOLED TECHNIQUE

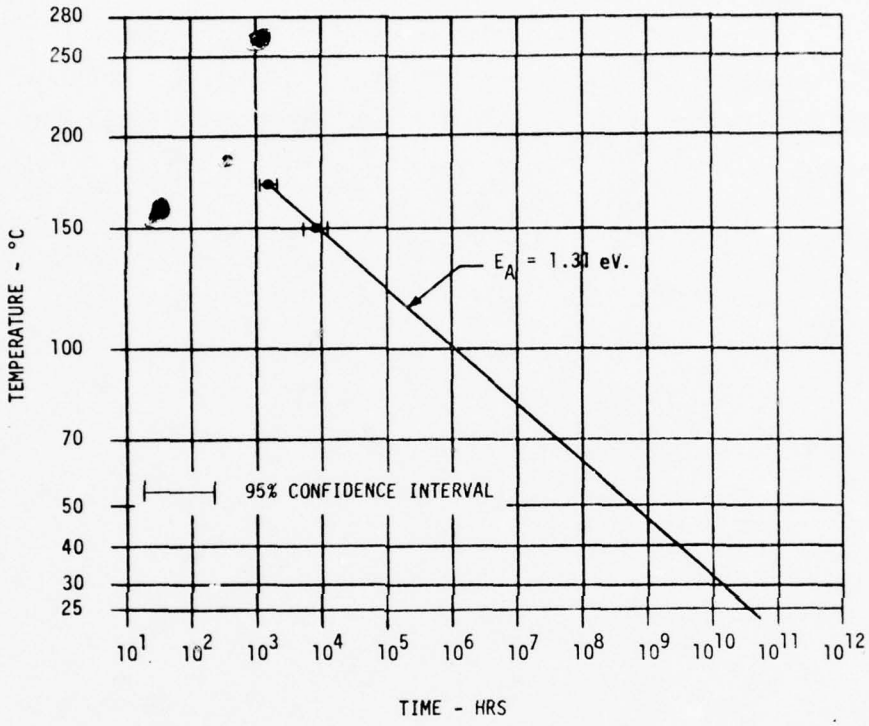


FIGURE S15. ARRHENIUS PLOT - P/N 773059 - FERRITE BEAD INDUCTOR

S9.0 CONCLUSIONS AND RECOMMENDATIONS

- Although the calculated failure rate (5.1×10^{-14} failures per hour) appears acceptable, the presence of the insulation diffusion mechanism in the 125°C test cell requires further investigation for lot-to-lot variability.
- The nature of the insulation degradation failure mechanism and the lack of a discernable "freak" population would indicate that a high temperature 100% screening test is not appropriate. However, a high temperature sampling inspection test would serve to identify marginal lots.

APPENDIX T

P/N 773060-300

CERAMIC CHIP RESISTOR

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T1.0 PART DESCRIPTION

The Ceramic Chip Resistor, P/N 773060-300, is manufactured by Cal-R-Incorporated. The test devices were delivered in chip form as depicted in Figure T1.

T2.0 CONSTRUCTION ANALYSIS

Table T1 is a summary of the pertinent physical details of the resistor. The ruthenium base resistor material and the platinum/gold conductor pads are fired on a 96% alumina ceramic carrier. This device contains no materials that limited testing below 300°C.

The typical SAM-D configuration is pictured in Figure T2. It consists of a part identical to the life test device soldered to a ceramic printed circuit board.

T3.0 ELECTRICAL TEST CRITERIA

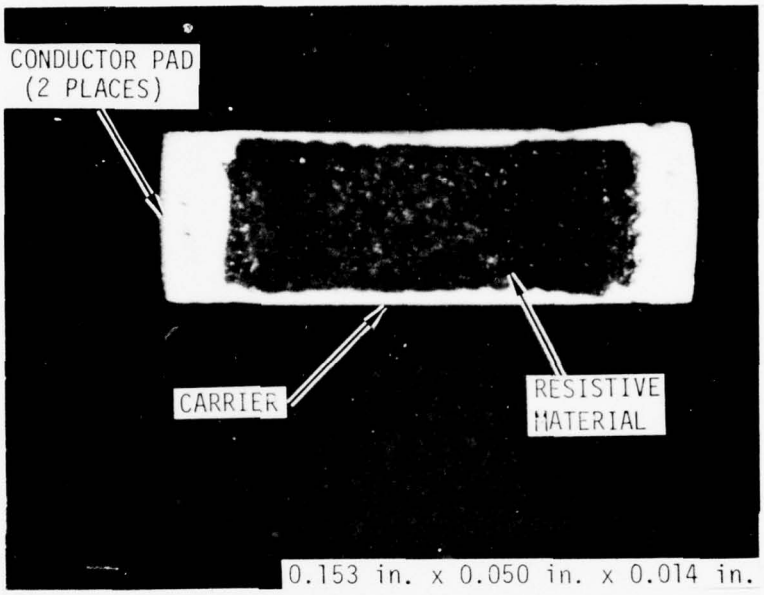
The electrical test for this device is resistance. Table T2 provides the limits for this test.

T4.0 BIAS CIRCUIT ANALYSIS

Upon receiving the parts a "mini" life test was initiated which consisted of several devices stored at 250°C and periodically removed for measurement. The resistance continued to increase through the course of this 1000 hour experiment.

A lead attach evaluation was initiated which included several types of solder. Devices were both hand soldered and dip soldered. In all cases, the lead attach joints were fragile and failed when raised to elevated ambient temperatures. This was not surprising because of the extremely small surface area (0.034 inch x 0.063 inch) available for attaching leads. It was in anticipation of this eventuality that the "mini" life test was initiated.

Based on the results of the "mini" life test (resistance degradation but no catastrophic failures) and the inability to attach permanent soldered leads, it was decided that an unbiased life test would be performed at five different temperatures.



20X

FIGURE T1. EXTERNAL CONSTRUCTION - P/N 773060-300 - CERAMIC CHIP RESISTOR

TABLE T1. PART CONSTRUCTION DETAILS - P/N 773060-300 - CERAMIC CHIP RESISTOR

A. IDENTIFICATION

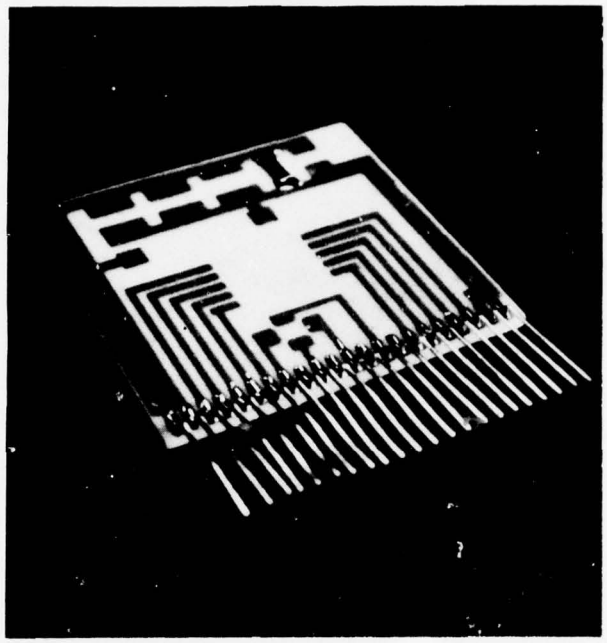
1. Part Name: Ceramic Chip Resistor
2. Part Number: 773060-300
3. Part Manufacturer: Cal-R-Inc.
4. Manufacturer's Part Number: N/A

B. EXTERNAL PACKAGE

1. Type: Resistor and conductor pads fired on 96% alumina ceramic carrier.
2. Weight: 0.0066 gram
3. Materials:
   a) Carrier: 96% alumina ceramic
   b) Resistor: Ruthenium base fire-on material (Electro Material Corp. of Am.)
   c) Conductor Pads: Platinum/Gold

TABLE T2. ELECTRICAL TEST CONDITIONS - P/N 773060-300 - CERAMIC CHIP RESISTOR

TEST NO.	PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
				MIN	MAX	
1	RESISTANCE	R	—	12.35	13.65	KΩ



1.9X

DEVICE MOUNTED ON CIRCUIT BOARD

9.7X

CLOSE-UP OF DEVICE

FIGURE T2. TYPICAL SAM-D CONFIGURATION - P/N 773050 - CERAMIC CHIP RESISTOR

T5.0 STEP STRESS TEST RESULTS

A step stress test was not required because the "mini" life test which was performed (Paragraph T4.0) at 250°C produced no catastrophic failures. Since five temperatures were to be utilized, two were selected (100°C and 125°C) near the specified operating temperature. The remaining three cells were at 150°C, 175°C and 200°C.

T6.0 LIFE TEST CONDITIONS AND RESULTS

The life test conditions, as previously stated, consisted of five unbiased cells at 25°C increments from 100°C to 200°C. The life test was continued until all cells had reached 10,000 hours. Only three failures were generated, all from Cell 1 (200°C). Table T3 is a summary of the life test.

T7.0 FAILURE ANALYSIS

The failure analysis results are summarized in Table T4. Visual examination of the three failed parts did not establish the cause of degradation. Because the failures were only slightly below the specification limit, further failure analysis was not performed and the exact cause of failure was not determined.

T8.0 DATA CORRELATION

The Table T4 failure analysis summary shows a total of three test failures, all in the highest temperature test cell, 200°C. No catastrophic failures were encountered. The three failures were tolerance failures, i.e., the measured resistance exceeded the upper tolerance limit of 13650 ohms. Since the life tests were conducted using only temperature as an accelerator, all failures are considered applicable to a storage environment. The Figure T3 plot of the normalized average resistance at the discrete measurement times shows that the resistors in each test cell displayed an increasing resistance characteristic which was a function of both test time and temperature. The average value of the control samples, which were stored at laboratory conditions, nominally 25°C, had a maximum change of 0.02% during the test period.

Insufficient failures in the test program resulted in the use of extrapolation techniques to estimate the average (or median) times to failures. This was considered a satisfactory approach since all test parts were exhibiting increasing resistance with time, the rate of increase being proportional to the ambient test temperature. Analysis of the resistance distribution in each cell, all at discrete

TABLE T3. LIFE TEST SUMMARY - P/N 773060-300
CERAMIC CHIP RESISTOR

TEST CELL DESCRIPTION				CUMULATIVE FAILURES AT HOURS OF TEST													
CELL NO.	APPLIED BIAS	AMBIENT TEMP.	QTY	4	8	16	32	64	128	256	512	1000	2500	4000	6000	8000	10,000
1	ZERO VOLT.	200°C	30	0	0	0	0	0	0	0	1	1	1	3	3	3	3*
2	ZERO VOLT.	175°C	30	0	0	0	0	0	0	0	0	0	0	0	0	0	0*
3	ZERO VOLT.	150°C	30	0	0	0	0	0	0	0	0	0	0	0	0	0	0*
4	ZERO VOLT.	125°C	30	0	0	0	0	0	0	0	0	0	0	0	0	0	0*
5	ZERO VOLT.	100°C	30	0	0	0	0	0	0	0	0	0	0	0	0	0	0*

*TEST TERMINATED

TABLE T4. FAILURE ANALYSIS SUMMARY - P/N 773060-300 -
CERAMIC CHIP RESISTOR

A. FAILED PARAMETER OR SYMPTOMS	QUANTITY OF FAILURES AND TIME (HOURS) OF FAILURE				
B. FAILURE MODE	200°C	175°C	150°C	125°C	100°C
C. FAILURE MECHANISM	ZERO VOLTS	ZERO VOLTS	ZERO VOLTS	ZERO VOLTS	ZERO VOLTS
D. CAUSE OF FAILURE	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5
A. RESISTANCE B, C, D NOT DETERMINED	1@512 2@4000				
TOTAL NUMBER OF FAILED PARTS	3	0	0	0	0

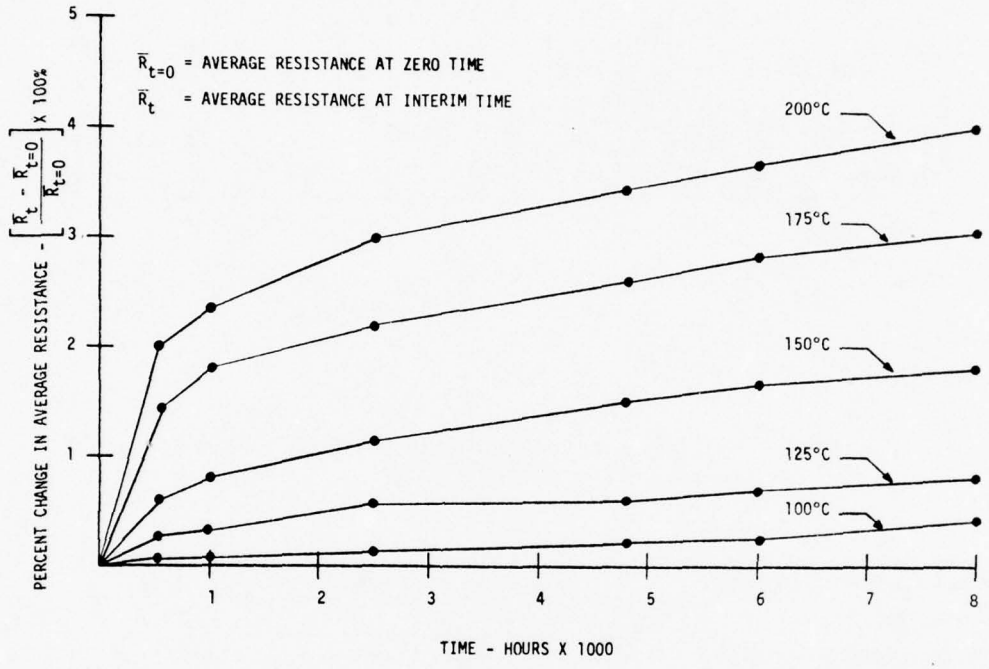


FIGURE T3. NORMALIZED AVERAGE RESISTANCE TIME/TEMPERATURE DEGRADATION - P/N 773060-300 - CERAMIC CHIP RESISTOR

measurement times, revealed skewed normal distributions which could adequately be depicted by lognormal distributions. Figure T4 shows the pre-test resistance cumulative distribution function for the 200°C, 175°C, and 100°C test cells, plotted on lognormal probability paper. While the shape of the distributions remained relatively stable during 8000 hours of life tests, the average resistance increased as a function of time and temperature, as shown in Figure T5. (Note that the 100°C data is for the 4696 hour test point). Note that the test data continues to describe a lognormal distribution and that the variances remained relatively unchanged. These results were typical for all test cells. From this analysis it was concluded for extrapolation purposes that the assumption of a lognormal resistance distribution was reasonable and that the variances of this distribution would remain constant over the extrapolation time period.

Data analysis of the three lower temperature cells (100°C, 125°C and 150°C) indicates that resistance is increasing linearly with time, thus allowing the use of linear regression techniques to predict resistance behavior. However, analysis of the 175°C and 200°C test data indicates the resistance is best described by a second order polynomial, due to a departure from linearity during the latter portion of the test. This suggests that the lower temperature test cells (100°C, 125°C and 150°C) may also depart from linearity if sufficient test time could be accumulated. Therefore, use of the lower temperature test cells as the basis for failure extrapolation could provide an optimistic estimate of storage reliability. Since extrapolation is required, the more conservative approach of utilizing the 200°C and 175°C test data was selected as the basis for failure rate evaluation.

The second order polynomials describing the 175°C and 200°C median resistances are as follows:

$$t_{175} = 130{,}532 - 270.962(R') + .140935(R')^2$$
$$t_{200} = 138{,}468 - 263.114(R') + .125555(R')^2$$

where

t_{175} = time to specified median resistance at 175°C
t_{200} = time to specified median resistance at 200°C
R' = median resistance minus 12000Ω

These equations were evaluated for median lifetimes, that is, the time for the median resistance to exceed the specified 13650Ω limit, and the data is summarized

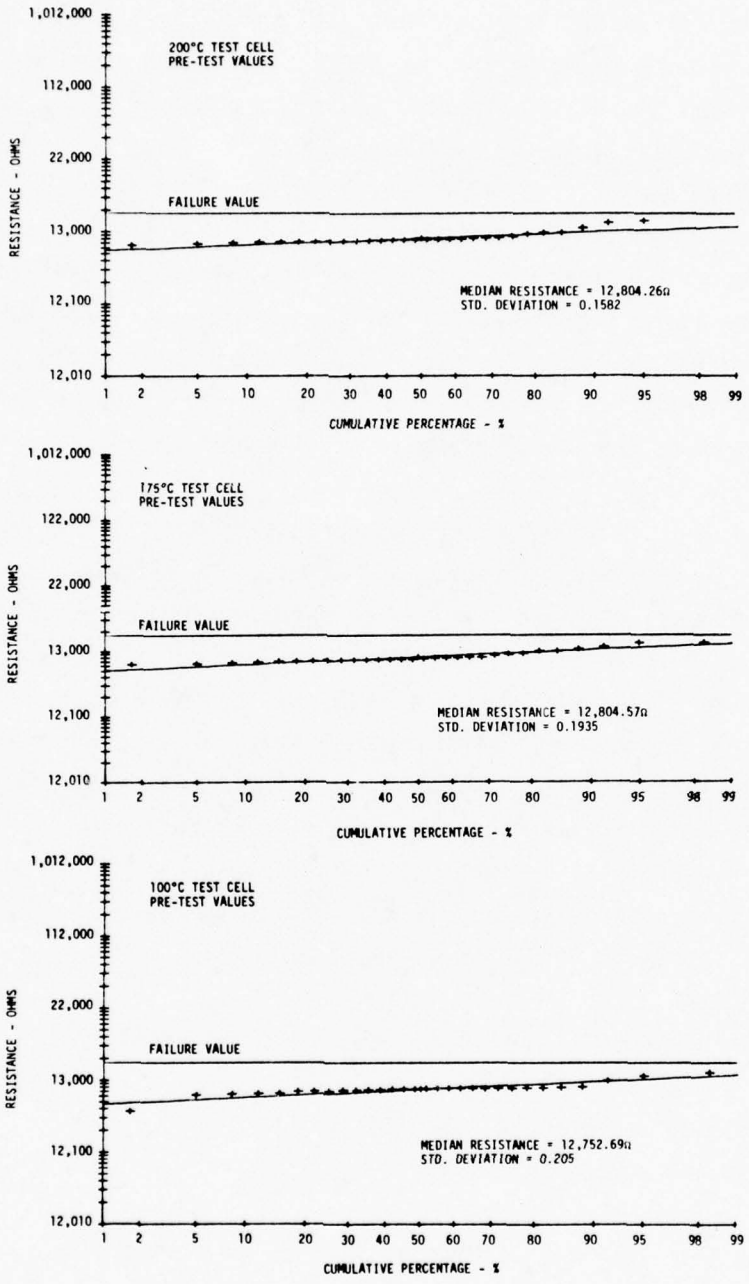


FIGURE T4. PRE-TEST RESISTANCE CUMULATIVE DISTRIBUTION FOR CELL 1 (TOP), CELL 2 (MIDDLE) AND CELL 5 (BOTTOM) - P/N 773060-300 - CERAMIC CHIP RESISTOR

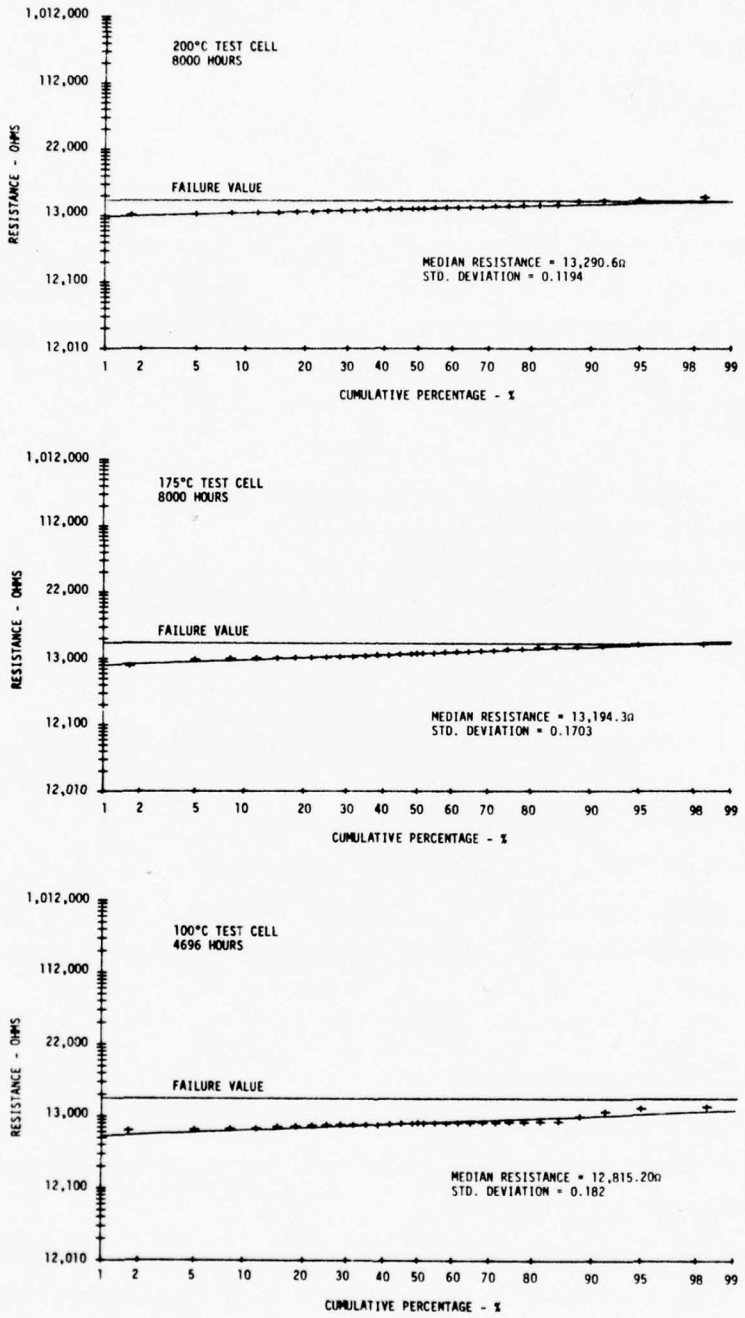


FIGURE T5. RESISTANCE CUMULATIVE PERCENTAGE FOR CELL 1 (TOP), CELL 2 (MIDDLE) AND CELL 5 (BOTTOM) - P/N 773060-300 - CERAMIC CHIP RESISTOR

in Table T5. The 175°C and 200°C data yielded the following Arrhenius equation, which is shown graphically in Figure T6.

$$\ln t_{50\%} = 4.0218 + \frac{0.2739}{kT}$$

The distribution standard deviation was established by "pooling" the standard deviations of the individual distributions. Having defined the failure distribution, the median lifetime and the standard distribution, the following formula was used to calculate the instantaneous failure rate, $\lambda(t)$, for a storage environment.

$$\lambda(t) = \frac{f(t)}{R(t)}$$

$$\lambda(t) = \frac{\frac{1}{t} \exp - \frac{[\ln t - 4.0218 - 0.2739(\frac{1}{kT})]^2}{2(0.82)^2}}{\int_t^\infty \frac{1}{t'}[\exp - \frac{[\ln t - 4.0218 - 0.2379(\frac{1}{kT})]2}{2(0.82)^2}] \, dt'}$$

Figure T7 shows $\lambda(t)$ as a function of storage temperature for ten and twenty year storage periods. The calculated $\lambda(t)_{MAX}$ is 3.3×10^{-6} failures per hour. This estimate is conservative for the following reasons:

- Extrapolation techniques were used to estimate time to failure.
- Failure times were estimated using the 175°C and 200°C test data which departed from the linearity displayed by the lower temperature test cells.

T9.0 CONCLUSIONS AND RECOMMENDATIONS

- Considering the conservative data analysis approach, the calculated storage failure rates appear acceptable over the storage time and temperature range of interest.
- There was no "freak" or infant mortality, population present in the parts tested. The test results indicate that high temperature testing up to 200°C, although causing a permanent increase in resistance, can be effectively utilized as a sampling test to ensure lot integrity.

TABLE T5. SUMMARY DATA - P/N 773060-300 - CERAMIC CHIP RESISTOR

CELL NO.	TEST VOLTAGE (VOLTS)	T_A (°C)	T_{INT} (°C)	MEDIAN LIFE (HOURS)	STANDARD DEVIATION (HOURS)
1	ZERO	200	200	46,153 (1)	0.668
2	ZERO	175	175	67,140 (1)	0.654
3	ZERO	150	150	102,076 (2)	0.869
4	ZERO	125	125	163,592 (2)	1.152
5	ZERO	100	100	279,286 (2)	0.603

(1) EXTRAPOLATED VALUES, USING SECOND ORDER POLYNOMIALS

(2) ESTIMATE FROM ARRHENIUS EQUATION

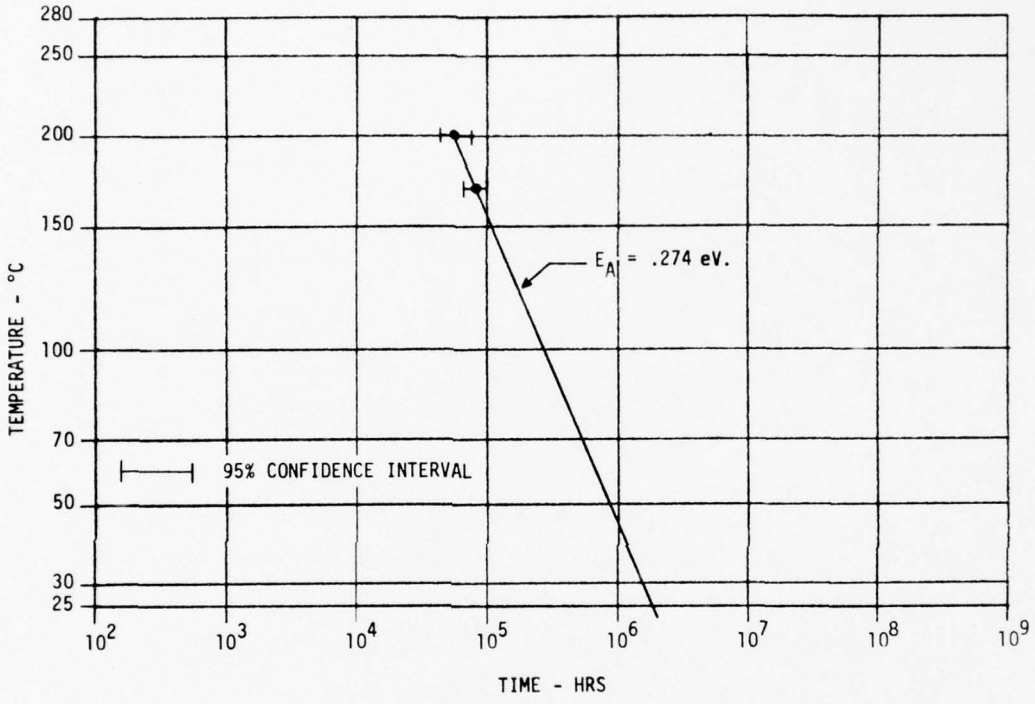


FIGURE T6. ARRHENIUS PLOT - P/N 773060-300 - CERAMIC CHIP RESISTOR

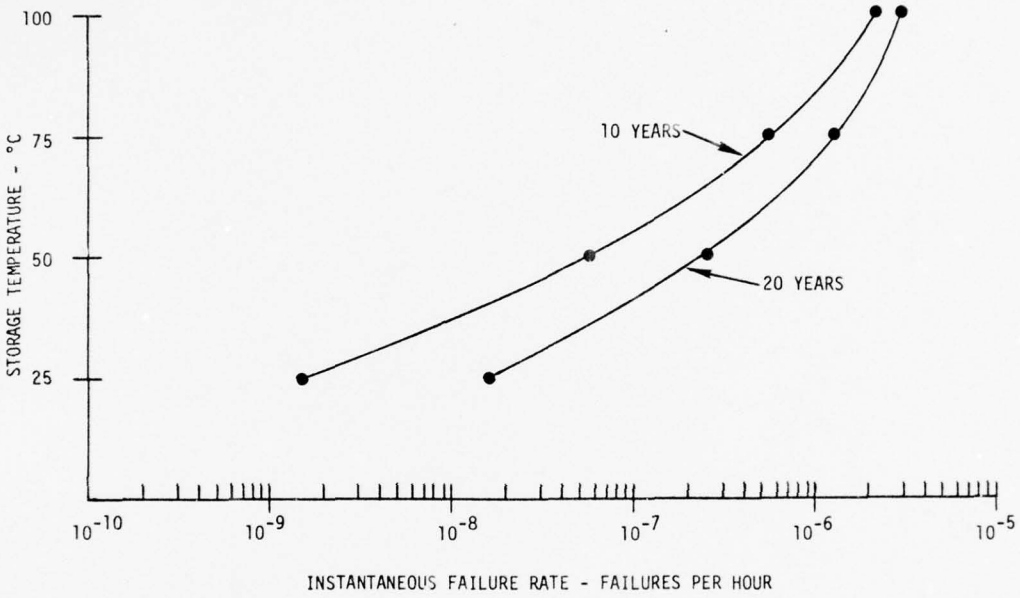


FIGURE T7. MAXIMUM INSTANTANEOUS FAILURE RATE, $\lambda(t)$ - P/N 773060-300 - CERAMIC CHIP RESISTOR

STORAGE RELIABILITY
OF MISSILE MATERIEL

REPORT MDC E1601
29 APRIL 1977

APPENDIX U

P/N 773207

SPECIAL HYBRID TECHNOLOGY SUBSTRATE

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U1.0 PART DESCRIPTION

The Special Hybrid Technology Substrate, P/N 773207, is a ceramic substrate with 14 fired resistors of Du Pont 1400-series resistor composition. The conductors are platinum/gold composition insulated at crossovers with Du Pont crystallizable glass dielectric composition #8299 fired on the ceramic substrate. The parts were manufactured by Raytheon Missile Systems Division.

U2.0 CONSTRUCTION ANALYSIS

The pertinent physical details are summarized in Table U1. Figure U1 is a photograph of the device. Six of the resistors were trimmed to specific values for the test program. R11 utilizes 300 ohms per square resistor composition and the remaining trimmed resistors are of 30 ohms per square resistor composition. The part contains no materials which limited testing below 300°C.

U3.0 ELECTRICAL TEST CRITERIA

Table U2 is a list of the electrical tests for this device.

U4.0 BIAS CIRCUIT ANALYSIS

A bias circuit using four power supplies, one for each resistor branch, was initially used to operate four of the six trimmed resistors at rated power dissipation. The remaining two trimmed resistors were at 25% of rated power. The devices remained stable when operated in an ambient temperature of 275°C.

U5.0 STEP STRESS TEST RESULTS

Twenty six devices configured as discussed in the previous paragraph were subjected to a step stress test consisting of seven 16 hour steps at 25°C increments starting at 125°C and concluding at 275°C. Eighteen marginal resistance failures were generated. Figure U2 contains a summary of the step stress test. In addition, 4 catastrophic failures occurred during the step stress test that were traced to deficiencies in the step stress test fixture. These failures were not included in the Figure U2 summary unless they had previously failed resistance.

To preclude this type of catastrophic failure during the life test, an alternate circuit utilizing only one power supply was used. This slightly altered the power dissipation to the values provided in Figure U2.

TABLE U1. PART CONSTRUCTION DETAILS - P/N 773207 - SPECIAL HYBRID TECHNOLOGY SUBSTRATE

A. IDENTIFICATION

1. Part Name: Special Hybrid Technology Substrate
2. Part Number: 773207
3. Part Manufacturer: Raytheon
4. Manufacturer's Part Number: 773207

B. EXTERNAL PACKAGE

1. Type: Fourteen resistors fired on a ceramic substrate.
2. Weight: 3.5 grams
3. Materials:

   a) Resistors: DuPont 1400-Series resistor compositions
   b) Conductors: Platinum-gold conductor composition
   c) Dielectric between conductor crossovers: Crystallizable glass dielectric composition #8399.

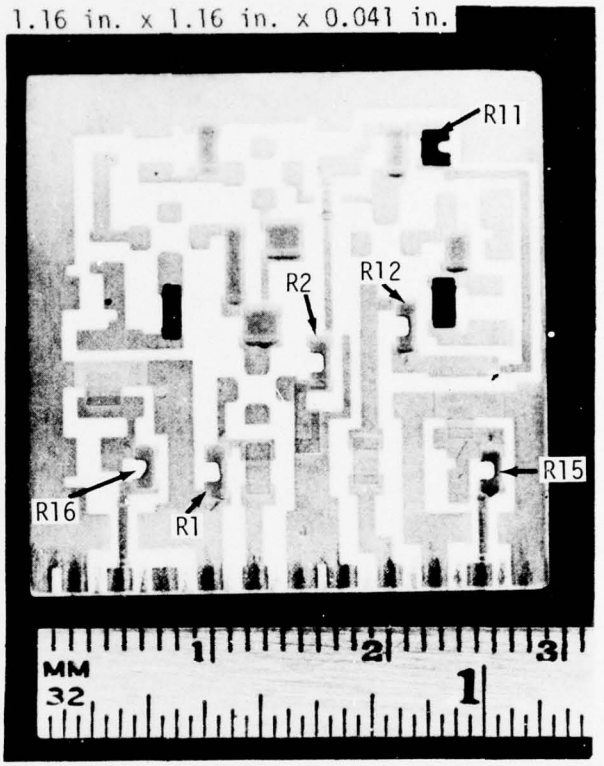


FIGURE U1. SPECIAL HYBRID TECHNOLOGY SUBSTRATE - P/N 773207

TABLE U2. ELECTRICAL TEST CONDITIONS - P/N 773207 - SPECIAL HYBRID TECHNOLOGY SUBSTRATE

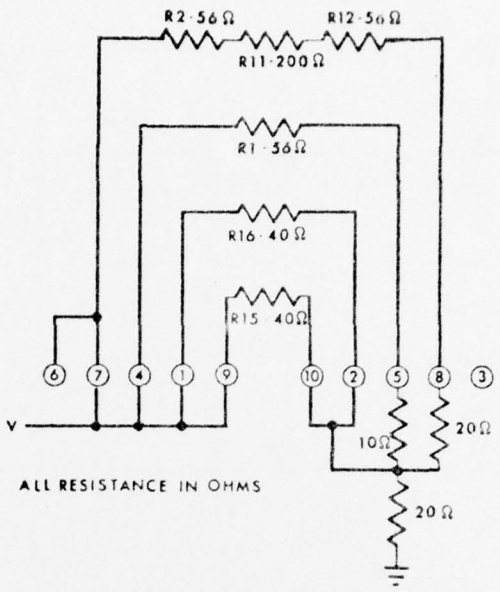
TEST NO	SYMBOL	LIMITS		UNITS
		MAX	MIN	
1	R1	54.88	57.12	Ω
2	R15	38.0	42.0	Ω
3	R16	38.0	42.0	Ω
4	R2 + R11 + R12	299.76	324.24	Ω
5	R(1 - 9)	⚠		

⚠ RESISTANCE BETWEEN PIN 1 AND PIN 9 RECORDED FOR INFORMATION ONLY.

ALL TESTS CONDUCTED AT T_A = 25°C, -55°C AND 125°C FOR INITIAL AND FINAL TESTS.

ALL TESTS CONDUCTED AT T_A = 25°C FOR INTERIM TEST.

LIFE TEST CIRCUIT



STEP STRESS TEST - FAILURE SUMMARY (26 DEVICES)

AMBIENT TEMP (°C)	CUMULATIVE FAILURES
125°C	3
150°C	7
175°C	9
200°C	10
225°C	13
250°C	18
275°C	18

LIFE TEST CONDITIONS

TEST CELL NUMBER	T_A AMBIENT TEMP. (°C)	% OF RATED POWER					
		R1	R2	R11	R12	R15	R16
1	263°C	103	24	87	24	100	100
2	263°C	77	18	65	18	75	75
3	263°C	0	0	0	0	0	0
4	250°C	103	24	87	24	100	100
5	225°C	103	24	87	24	100	100

FIGURE U2. STEP STRESS RESULTS AND LIFE TEST CONDITIONS P/N 773207 - SPECIAL HYBRID TECHNOLOGY SUBSTRATE

U6.0 LIFE TEST CONDITIONS AND RESULTS

The life test conditions for each cell are included in Figure U2. The life test continued until all five cells reached 6000 hours, and Table U3 provides the cumulative failure summary at each measurement time during the life test.

U7.0 FAILURE ANALYSIS

A summary of the failure analysis results is presented in Table U4. All failures were marginal resistance. Microscopic examination disclosed no anomalous conditions. Because the failures were marginal, further failure analysis was not performed and the exact cause of failure was not determined.

U8.0 DATA CORRELATION

Three individual resistors, R1, R15 and R16, and a series of three resistors, R2+R11+R12, were available for measurement during the accelerated life tests. No catastrophic failures were encountered. The Table U4 failure analysis summary establishes that failures were the result of resistors exceeding their lower or upper specified limits, and then only slightly. Almost all early failures were due to exceeding the lower resistance limit, and most of these failures eventually recovered. The general tendency was for the resistors to initially decrease in resistance and then begin to increase. Figure U3 shows the Cell 1 (263°C, 50 volts) resistance changes as a function of measurement time. All the measured resistors showed an initial decrease in resistance, followed by a gradual increase as the test progressed. These results are typical of the 263°C test cells, and the presence of an electrical stress in two cells appeared to have no accelerating influence. The lower temperature test cells followed the same general pattern but with smaller percentage changes. The initial resistance decrease is attributed to an annealling effect which would probably not be a factor at temperatures below 100°C. Therefore, all the failures due to a decrease in resistance were not used in data analysis.

Resistor R1 provided the most failures. The early failures were discounted because they had marginal initial values. Since the three 263°C test cells displayed almost identical results, their failure data were combined for anlaysis purposes. Both the Weibull and the lognormal failure distributions, Figure U4 and U5, provided adequate fits for the test data. The Weibull distribution was selected

TABLE U3. LIFE TEST SUMMARY - P/N 773207 -
SPECIAL HYBRID TECHNOLOGY SUBSTRATE

TEST CELL DESCRIPTION					CUMULATIVE FAILURES AT HOURS OF TEST												
CELL NO.	APPLIED BIAS	AMB. TEMP.	QTY	RESISTOR	4	6	8	16	32	64	128	256	512	1000	2500	4000	6000
1	MAX. VOLT.	263°C	30	R1	4	4	5	5	5	5	6	6	6	7	7	7	9*
				R15	3	10	10	11	11	11	11	12	12	12	12	12	12*
				R16	1	1	1	1	1	1	1	1	1	1	1	1	1*
				(R2+R11+R12)	0	0	0	0	0	0	0	0	0	0	0	0	0*
2	MID. VOLT.	263°C	30	R1	6	6	6	6	6	6	6	6	6	7	8	10	12*
				R15	1	1	2	2	2	4	4	5	5	5	5	5	5*
				R16	4	4	4	4	4	4	4	4	4	4	4	4	5*
				(R2+R11+R12)	0	0	0	0	0	0	0	0	0	0	0	0	0*
3	ZERO VOLT.	263°C	30	R1	4	5	5	5	5	5	5	5	7	8	9	10	10*
				R15	3	3	4	4	4	4	4	4	4	4	5	5	5*
				R16	2	2	2	2	2	2	2	2	2	2	2	2	4*
				(R2+R11+R12)	0	0	0	0	0	0	0	0	0	0	0	0	0*
4	MAX. VOLT.	250°C	30	R1	0	0	0	0	2	2	2	2	3	4	4	4	4*
				R15	1	1	3	6	6	6	6	6	7	7	8	8	8*
				R16	1	1	1	1	1	1	1	1	1	1	1	1	1*
				(R2+R11+R12)	0	0	0	0	0	0	0	0	0	0	0	0	0*
5	MAX. VOLT.	225°C	30	R1	1	1	2	2	2	2	2	2	3	3	3	3	4*
				R15	1	1	2	2	3	3	3	4	5	5	5	5	5*
				R16	0	0	0	0	0	0	0	0	0	0	0	0	1*
				(R2+R11+R12)	0	0	0	0	0	0	0	0	0	0	0	0	0*

* TEST TERMINATED

TABLE U4. FAILURE ANALYSIS SUMMARY - P/N 773207 - SPECIAL HYBRID TECHNOLOGY SUBSTRATE

A. FAILED PARAMETER OR SYMPTOM B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TIME (HOURS) OF FAILURE				
	263°C			250°C	225°C
	MAX. VOLT.	MID. VOLT.	ZERO VOLT.	MAX. VOLT.	MAX. VOLT.
	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5
A. RESISTANCE B. RESISTANCE DECREASE C. PROBABLY ANNEALING D. NOT DETERMINED	R1 4@4 1@8 R15 3@4 7@6 1@16 1@256 R16 1@4	R1 6@4 R15 1@4 1@8 1@64 1@256 R16 4@4	R1 4@4 R15 3@4 1@8 R16 2@4	R1 1@512 R15 1@4 2@8 3@16 1@512 1@2500 R16 1@4	R1 1@4 1@512 R15 1@4 1@8 1@32 1@256 1@512 R16
A. RESISTANCE B. RESISTANCE INCREASE C. PROBABLY MATERIAL DEGRADATION D. NOT DETERMINED	R1 1@128 1@1000 2@6000 R15 R16	R1 1@1000 1@2500 2@4000 2@6000 R15 1@64 R16 1@6000	R1 1@6 2@512 1@1000 1@2500 1@4000 R15 1@2500 R16 2@6000	R1 2@32 1@1000 R15 R16	R1 1@8 1@6000 R15 R16 1@6000
TOTAL NUMBER OF FAILURES	22	22	19	13	10

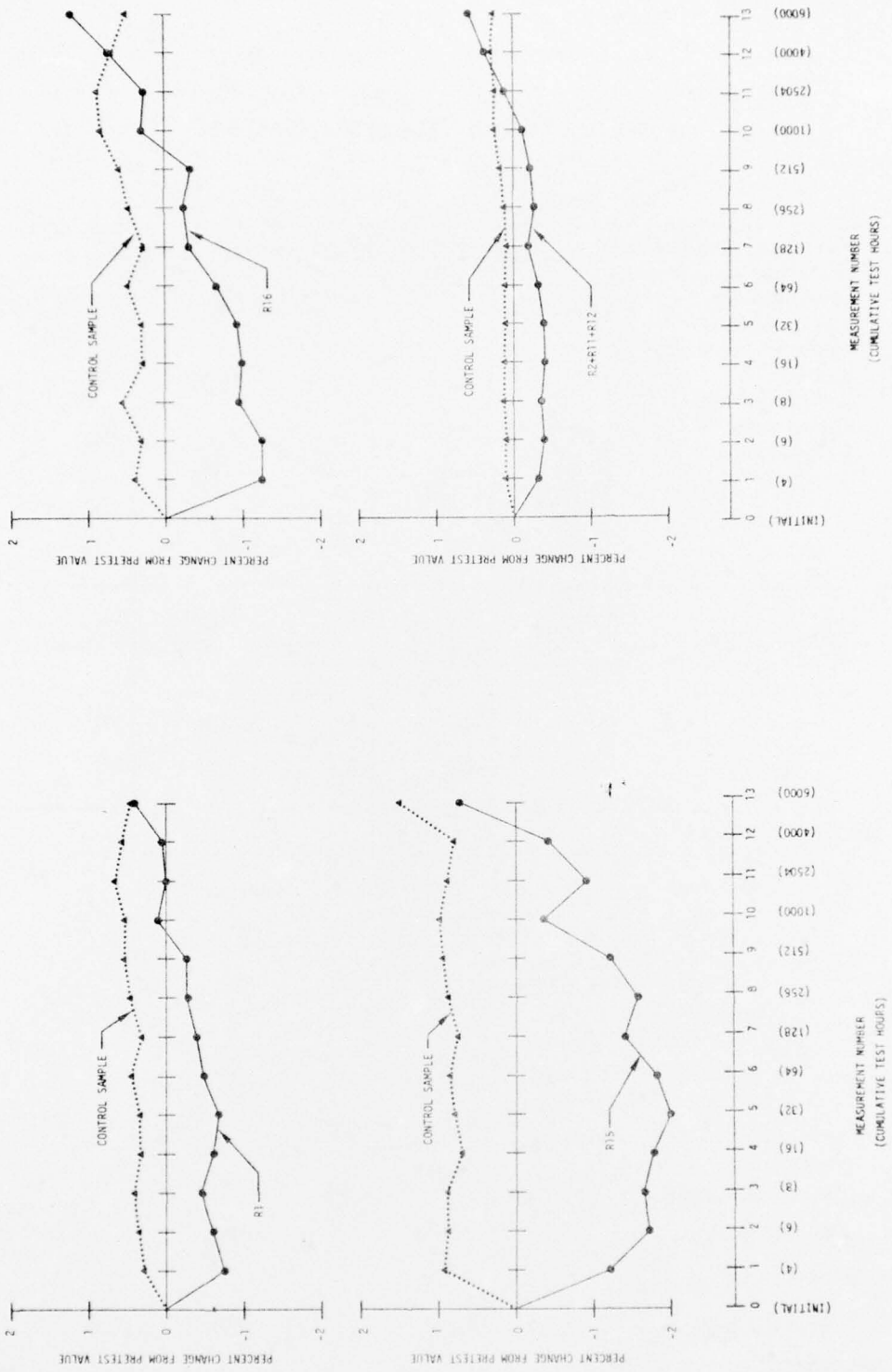


FIGURE U3. RESISTANCE (AVERAGE VALUES) CHANGES VERSUS MEASUREMENT TIME FOR CELL 1 - P/N 773207 - SPECIAL HYBRID TECHNOLOGY SUBSTRATE

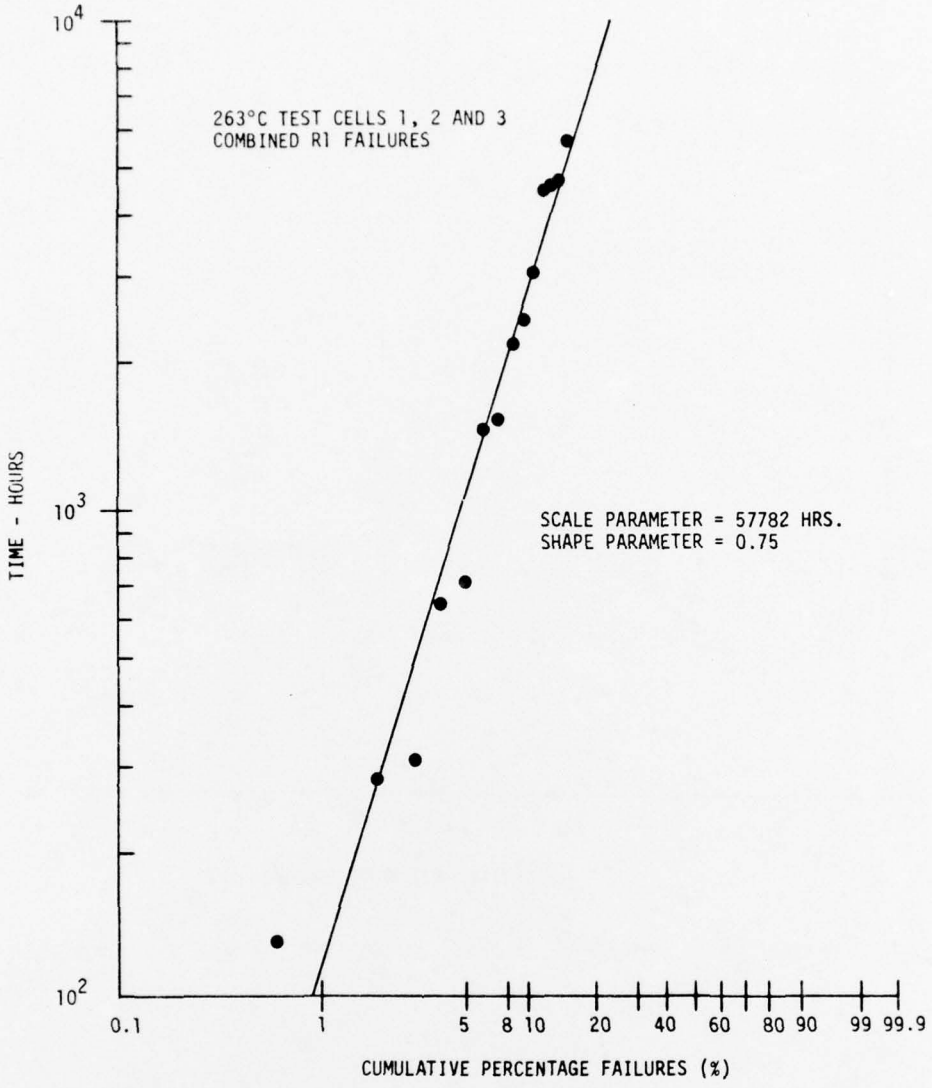


FIGURE U4. WEIBULL CUMULATIVE FAILURE DISTRIBUTION FOR THE COMBINED R1 FAILURES OF CELLS 1, 2 AND 3 - P/N 773207 - SPECIAL HYBRID TECHNOLOGY SUBSTRATE

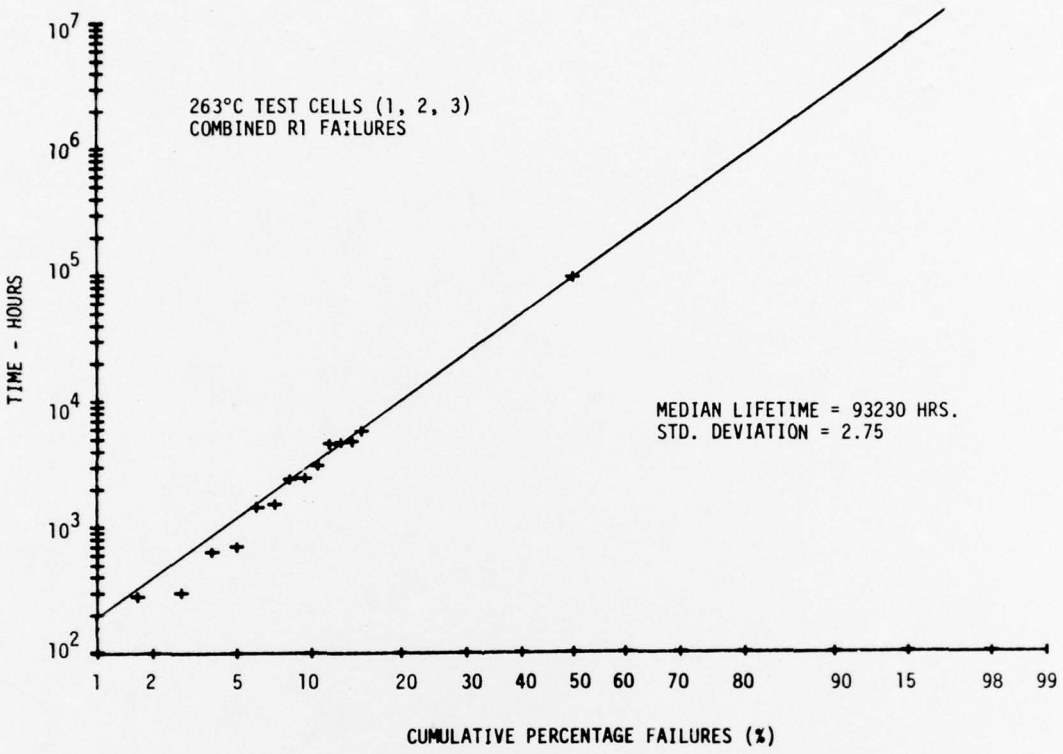


FIGURE U5. LOGNORMAL CUMULATIVE FAILURE DISTRIBUTION FOR THE COMBINED R1 FAILURES OF CELLS 1, 2 AND 3 - P/N 773207 - SPECIAL HYBRID TECHNOLOGY SUBSTRATE

for failure rate analysis because it yielded the most conservative failure rate estimates. Since Cells 4 (250°C) and 5 (225°C) contributed only one applicable failure each, their failure distributions assume a shape parameter (β) of 0.75, allowing the calculation of a scale parameter (θ). Pertinent distribution data are summarized in Table U5.

The Figure U6 Arrhenius plot was prepared using the Table U5 scale parameters and can be represented by the following equation:

$$\theta = 6.317611 \times 10^{-14} \exp \frac{1.91}{kT}$$

Instantaneous failure rates, $\lambda(t)$, plotted in Figure U7 (20 year storage period) as a function of temperature, were calculated using the following expression:

$$\lambda(t) = \frac{f(t)}{R(t)}$$

$$= \left[\frac{0.75}{t}\right]\left[\frac{t}{6.317611 \times 10^{-14} \exp \frac{1.91}{kT}}\right]^{0.75}$$

The calculated $\lambda(t)_{MAX}$ is 2.96×10^{-10} failures per hour.

In addition to the deposited resistors, the substrates contained crossovers (conductive paths on top of each other separated by insulation) which could have degraded during the life tests. Crossover integrity was observed indirectly through the resistance measurements. R1 had no crossovers in the resistance measurement circuit, whereas R15 and R16 each had a crossover in parallel with the measured resistance. A leakage path in parallel with the resistor would lower the measured resistance. Since the trends of R15 and R16 closely followed that of R1, which had no crossovers, it was concluded that the crossovers had no degradation which lowered the measured resistance.

TABLE U5. SUMMARY DATA - P/N 773207 - SPECIAL HYBRID TECHNOLOGY SUBSTRATE

CELL NO.	NUMBER OF FAILURES	T (°C)	LOGNORMAL DISTRIBUTION		WEIBULL DISTRIBUTION	
			MEDIAN LIFE (HOURS)	STANDARD DEVIATION (HOURS)	SCALE PARAMETER (HOURS)	SHAPE PARAMETER
1,2,3 (COMBINED)	14	263	9.323×10^4	2.75	5.778×10^4	0.75
4	1	250	----	----	1.228×10^5	0.75 (1)
5	1	225	----	----	1.268×10^6	0.75 (1)

(1) 0.75 WAS ASSUMED FOR CELLS 4 AND 5, ALLOWING SCALE PARAMETER CALCULATION.

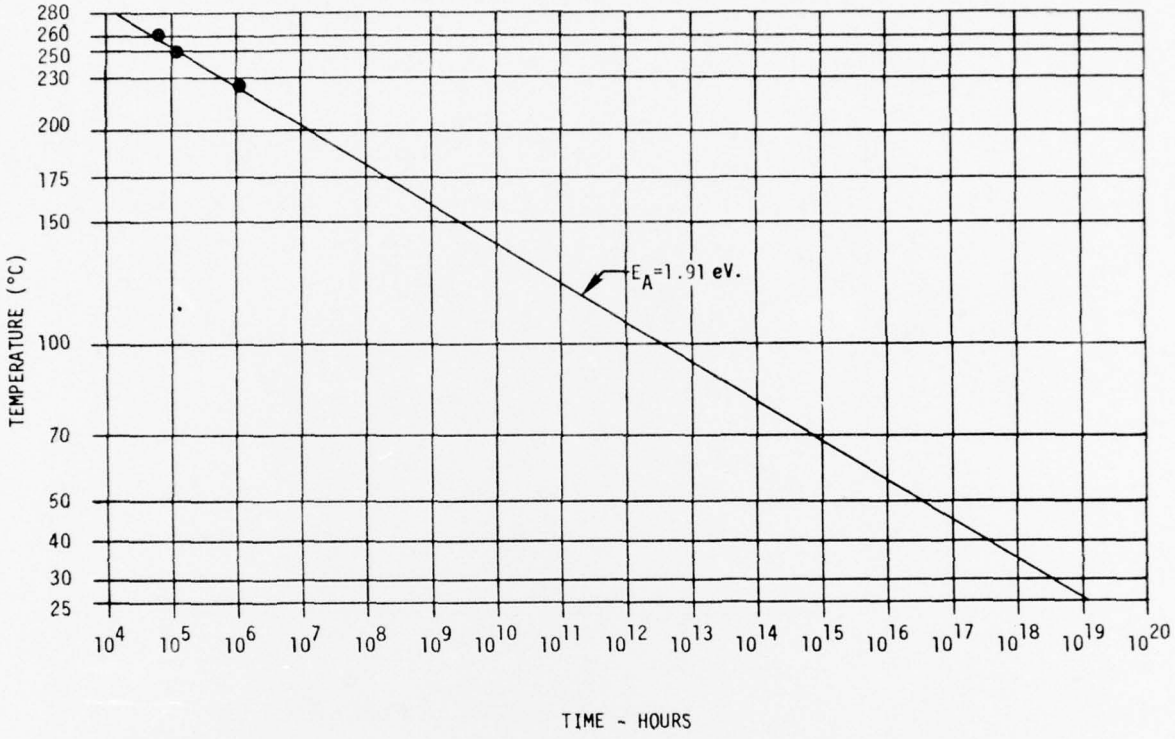


FIGURE U6. ARRHENIUS PLOT - P/N 773207 -
SPECIAL HYBRID TECHNOLOGY SUBSTRATE

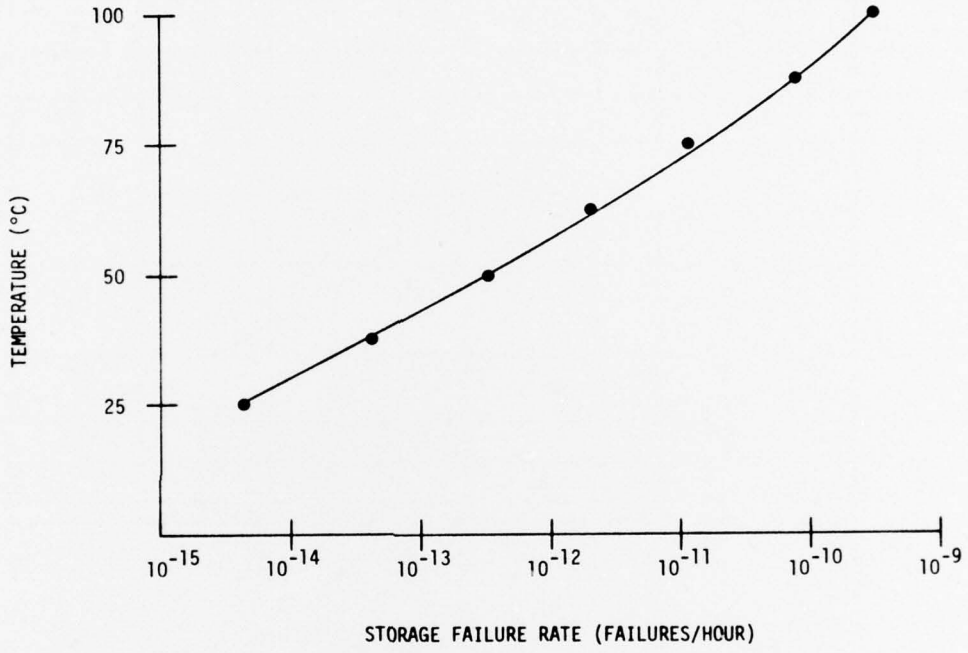


FIGURE U7. MAXIMUM INSTANTANEOUS FAILURE RATE, $\lambda(t)$, 20 YEAR INTERVAL - P/N 773207 - SPECIAL HYBRID TECHNOLOGY SUBSTRATE

U9.0 CONCLUSIONS AND RECOMMENDATIONS

- The use of an electrical stress during the life tests was not established as an accelerating factor.
- The deposited resistors displayed excellent stability during the life tests and should have a good storage reliability potential. The crossovers displayed no degradation which affected resistance measurements.
- A high temperature screening test (250°C, 16 hours) might be useful to initially "set" the resistors to a lower value in anticipation of a gradual rise in resistance at use temperature. An alternative lot sampling test could be used to verify typical performance.