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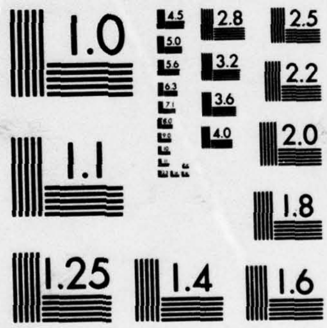
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NEW PASSIVATION METHODS OF GaAs

FINAL TECHNICAL REPORT

by

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TABLE OF CONTENTS

		Page
ABSTRACT		1
CHAPTER 1	Introduction	2
CHAPTER 2	Anodically grown double oxide structures on GaAs	4
	Anodisation method and electrochemical studies	4
	Charge storage devices	6
CHAPTER 3	MOS-Devices	12
	Investigation of growth and annealing parameters	13
	Measurements on "Standard Oxides"	14
	Inversion layer FETs	18
	Enhancement-Depletion Mode MOSFETs	19
CHAPTER 4	Anodisation of InP	23
	I/V Characteristics of MOS Structures	23
	Optimisation of electrolyte composition	23
	Anodisation in the dark	24
	Analysis of Multicomponent Thin Films on GaAs by Anodic Processes	25
	Anodic Oxidation of Silicon	26
	Analysis of Thin-Film Epitaxy - GaAs Junctions	28
	Study of Dissolution Rates with Anodic Oxidation of GaAs for various Electrolytes	28
	Oxide Structural Studies	29
	Naturally occurring Oxide Layers on GaAs	
	Anodic Oxides	30
	As-grown anodic oxide layers	30
	Annealed anodic oxide layers	30
	LIST OF RECENT PUBLICATIONS	35

Abstract

The investigation of the anodic growth processes of semiconductor oxides has resulted in improved oxides, superior interface conditions between semiconductor and oxide, and long-term charge storage devices. MOSFETs in the three modes of inversion, depletion and accumulation were fabricated and useful electronic characteristics were obtained. The study of an optimisation of the electrolyte and other aspects were continued. Further results on the oxidation of InP are presented.

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CHAPTER 1

INTRODUCTION

The writing of this report has again been a stimulating occasion for all concerned with oxidation work here because several useful contributions can be presented.

Using evaporated Aℓ, the possibilities of composite oxides on GaAs arise. The first advantage to be gained is reduced leakage currents. Then, however, the possibility of further considerable reduction in anodic growth currents becomes available which enables one to grow in an entirely different manner from that practised previously. At low current densities the relatively high threshold value for cation drift means that only OH^- ions, which have a low threshold value, contribute to oxide growth. This facility of operating above or below the cation drift threshold is a useful facility to grow native oxides either above or below the oxidised aluminium film on our samples. Long-term storage MAOS devices were thus produced which have given storage facilities longer than those obtained in corresponding Si devices because the energy gap of our native oxide enables one to use thermally assisted tunnelling for charging and discharging. These devices will be useful for fast read-out information-storage MAOSFETs. If anion growth only is used, improved interface conditions are also possible. These details are presented in Chapter 2. The possibilities of various MOSFETs were systematically explored and transistors in each of the three possible space charge modes were fabricated, namely enhancement, depletion and inversion. These results are described in Chapter 3. Of course there are many open problems still, such as the relatively low transconductance of the inversion mode transistor. But possibly with the results now available, as described in Chapter 2, we might be able to make good progress there to. In Chapter 4 some further results on InP and several other technological aspects investigated or in the process of investigation are presented.

The work was again jointly funded (apart from inhouse contributions and some postgraduate research Scholarships from

other sources) by the European Research Office and the United Kingdom Science Research Council. The following postdoctoral fellows worked on this project: Drs. A. Colquhoun, E. Kohn and B.L. Weiss. A newcomer who has just been appointed under the grant by the European Research Office, will be Dr. P.A. Breeze, who will be our first chemist with a Ph.D from Cambridge University. Postgraduate research students were: B. Bayraktaroglu, S.J. Hannah, A.F.A.B. El-Safti, E.T. Mills, and B. Livingston, the latter being jointly supervised by Dr. M. Faktor of the G.P.O. Laboratories at Martlesham, where related developments to that of our work is also undertaken, and myself.

CHAPTER 2

2. ANODICALLY GROWN DOUBLE OXIDE STRUCTURES ON GaAs

(B. Bayraktaroglu and S.J. Hannah)

2.1 Introduction

Although anodically grown native oxides on GaAs have been used to produce GaAs MOSFETs[(1),(2)] they are not yet exploited in connection with several other device applications known with Si due to the instability it has so far exhibited against many chemicals, including some photoresist developers and most of the commonly used acids and also against high temperature annealing, i.e. > 400°C. With a new anodisation method, utilising an $A\ell_2O_3$ layer together with the native oxide, it is now possible to extend the device applications of GaAs.

2.2 Anodisation method and electrochemical studies

The growth kinetics of anodically grown native oxide on GaAs has been investigated in detail in order to be able to control the properties and reproducibility of these oxides. Results of these investigations has led to a new understanding of mobile ionic species involved during anodic oxidation of GaAs.

It is well established in the literature that during anodic oxide growth, the current passing through the oxide is ionic, and, depending on the dominant ionic species, the growth takes place predominantly either at the oxide-electrolyte or at the semi-conductor-oxide interface. This can be explained in terms of the difference in threshold fields for the activation of anions and cations and also the difference in their mobilities in the oxide. For GaAs it has been established that the field required for the activation of anions (i.e. OH^-) is lower than the field required for the activation of cations (i.e. Ga and As ions). However, the mobility of cations, once activated, is much higher than that of anions and therefore above a critical field film growth occurs almost entirely at the oxide-electrolyte interface. At very low fields (correspondingly at very low current densities e.g. < $20\mu A/cm^2$) cation activation becomes negligible and growth takes place at the semiconductor-oxide interface.

Double oxide layers on GaAs are produced by first evaporating a known thickness of Aℓ on a cleaned and etched GaAs surface and then anodising the whole structure in AGW electrolyte (the

composition of the electrolyte has been explained in detail by Hasegawa in a previous report). In such a scheme the first oxide to grow is Al_2O_3 and subsequently, depending on the current density and also Al_2O_3 thickness, GaAs native oxide can be made to grow either at the electrolyte or at the semiconductor interface. At high current densities (i.e. > $2 mA/cm^2$), after all the Al is converted into Al_2O_3, the field at the GaAs-Al_2O_3 interface is high enough for the ionisation and also the activation of Ga and As cations into the Al_2O_3. These interstitial cations can then drift under the influence of the applied field through the Al_2O_3 to the oxide-electrolyte interface hence forming GaAs-native oxide at this interface. If the Al_2O_3 thickness is larger than ∿ 500Å then at such high fields the movement of Ga and As cations through Al_2O_3 becomes limited and due to high space charge build up inside this oxide electrical breakdown occurs resulting in locally damaged areas in Al_2O_3. Figure 1(a) shows the composite oxide structure and characteristic overpotential versus time curves plotted during growth, formed in this way. A chemical test, using tartaric acid which is a slow etchant of GaAs-native oxide but does not attack Al_2O_3, in conjunction with a Dektak profile plotter, has indicated that after the GaAs-native oxide is etched there remains an oxide whose thickness is very close to what is expected from the Al_2O_3 layer alone. MIS diodes, utilising this double oxide structure with the Al_2O_3 thickness being ∿ 150Å, have shown several improvements over the "standard oxide" (as defined in section 2.3 below). MOS diodes, in particular, gave a very narrow hysteresis, stabilisation of frequency dispersion and higher electrical breakdown strength. This indicates that the Al_2O_3-layer acts as a buffer layer separating the bulk of the oxide from the interface. Also, for the first time, the high-frequency CV-curve exhibits a steeper slope than the low frequency one (Figure 2). However, having a thin layer of Al_2O_3 underneath the native oxide did not show charge storage properties within the applicable gate bias range before dielectric breakdown.

On the other hand, by using low current densities (i.e. < $20 \mu A/cm^2$), GaAs native oxide grows entirely underneath Al_2O_3, Figure 1(b). An etch test similar to that described above showed no etching of the surface oxide of the composite oxide

formed this way. However, the thickness of the composite oxide is much thicker than expected from the Al_2O_3 thickness alone. Overpotential-time curves plotted during growth is a useful means of calculating the thickness of both oxides. As it can easily be seen in Figure 1 overpotential-versus/time curves have different characteristic transition regions just before GaAs native oxide starts to grow. Overpotential at which this transition occurs is in agreement with the expected value of overpotential after all Al layer has been anodised. Further increase in overpotential is attributed to the growth of GaAs and its thickness therefore can be calculated with the known thickness-overpotential ratio for GaAs.

Since the Al_2O_3 dissolution into the electrolyte is negligible it acts as a buffer layer between the native oxide and the electrolyte, enabling native oxide growth at very low current densities, which would otherwise be impossible as the dissolution rate of the native oxide is comparable to its growth rate at such current densities. Al_2O_3 acts as a diffusion barrier against anodic impurities in the electrolyte thus yielding a superior native oxide. A thick layer of Al_2O_3 (> 500Å) on top of native oxide offers high temperature stability of the native oxide as it acts as an overlayer preventing As or As_2O_3 loss from the native oxide, in a similar manner as used with Thin Film Epitaxy.[1] Since Al_2O_3 is inert to most chemicals including the positive photoresist developer, composite oxides produced in this way are now extremely stable against normal GaAs native oxide etchants. MIS diodes prepared, utilising this type of double oxide structures, have shown further improved electrical characteristics especially in connection with the dielectric-semiconductor interface. The time taken to rise from a deep depletion into an inversion mode is shorter than that of normal native oxide MOS diodes. The Cmin/Cmax ratio of capacitance-voltage plot is now very close to theoretically expected values.

2.3 Charge Storage Devices

One of the most interesting applications of the second type of double oxide structures is in connection with charge storage devices. MAOS (Metal, Al_2O_3, Oxide, Semiconductor) diodes produced with native oxide thicknesses of 50-200Å underneath ~ 600Å of Al_2O_3 have shown reproducible, strong charge storage properties. If very low current densities are used (i.e. < $20\mu A/cm^2$) the thickness

of the native oxide becomes extremely uniform resulting in identical electrical characteristics of every diode produced over a large slice of GaAs. The structure was annealed in N_2 at 350°C for 15 min prior to the evaporation of Aℓ contact pads.

The C-V curves of MAOS diodes are used for the investigation of the charge storage properties. Since the shift of the C-V curves is parallel, the shift in C-V curves can be taken as the shift in flat-band voltage. No distortion of the original shape of the C-V curves suggests that the charging of the oxide and surface traps is negligibly small.

The shift of the C-V curves is opposite to that expected from ion migration or polarisation. Charge instability could, therefore, be attributed to charging of the traps at the native oxide-$A\ell_2O_3$ interface by tunnelling of electrons and also possibly of holes through the native oxide. Since the charge instability has been observed over a wide range of thickness of native oxide and since the native oxide of GaAs has a relatively narrow bandgap (~ 5 eV), tunnelling is likely to be in the form of indirect tunnelling such as Fowler-Nordheim tunnelling.

Although it is most likely that any double insulator films on semiconductors will result in some form of a charge storage device, it is usually extremely difficult to obtain a non-volatile device with strong charge storage properties. Basically, the charge stored at the double insulator interface is due to the difference in the currents through the insulators at a given gate bias. If the insulators have good dielectric properties this charge will remain at the interface until a gate bias of opposite polarity is applied. Charging and discharging and consequently the charge retention time characteristics of the memory device are a strong function of the insulator thicknesses and also of the semiconductor insulator interface.

In the MAOS systems on GaAs produced as described above, a thick layer of $A\ell_2O_3$ (~ 600Å) ensured good insulating properties for the leakage of stored charge to the gate metal. Therefore, throughout these investigations the thickness of $A\ell_2O_3$ has been fixed at this value. However, the effect of the thickness of GaAs-native oxide and native oxide-GaAs interface properties were investigated.

Although it is possible to grow GaAs-native oxide underneath $A\ell_2O_3$ with a current density of $20\mu A/cm^2$, it was found that the native oxide-GaAs interface can be markedly improved if even lower current densities are used. At $20\mu A/cm^2$ the field at GaAs surface is still high enough for the activation of Ga and As cations into the native oxide, but not into $A\ell_2O_3$. Therefore native oxide will grow predominantly at native oxide-$A\ell_2O_3$ interface. However, at a current density of $10\mu A/cm^2$ or lower cation activation into native oxide becomes negligible and therefore growth takes place almost entirely at GaAs-native oxide interface. Since the activation energies for Ga and As are different, the last system is likely to retain a stoichiometric GaAs surface. The effect of this relatively higher field growth mechanism (i.e. $20\mu A/cm^2$) on the charge storage properties of MAOS diodes is in the form of the distortion of original C-V curve after the application of gate pulses. Recovery of original curve cannot be achieved by the application of a gate bias of opposite polarity.

On the application of a positive gate bias (Figure 4(b)) electrons in the conduction band of GaAs have a certain probability to tunnel part of the oxide into the native oxide conduction band and under the influence of the field drift to the double oxide interface and be captured by traps at this interface. Hence an effective negative charge accumulation at this interface occurs. When the gate bias is lifted the energy band of GaAs will be bent as shown in Figure 4(c) under the influence of negative stored charge. If the amount of charge stored is Q/cm^2 then a gate voltage of ΔV must be applied in order to obtain flat-band condition. ΔV is given by:-

$$\Delta V = -\frac{d_2}{\varepsilon_2} Q \qquad (1)$$

where

d_2 is the thickness of $A\ell_2O_3$

ε_2 is the permittivity of $A\ell_2O_3$.

At the initiation of a gate pulse (V_G) the voltage drop across first insulator (native oxide) $V_1(0)$ is given by:-

$$V_1(0) = \left(1 + \frac{\varepsilon_1}{\varepsilon_2}\frac{d_2}{d_1}\right)^{-1} V_G \qquad (2)$$

and V_1 then decays with time throughout the charging period. Since the charging current is exponentially dependent on the voltage across this insulator (Fowler-Nordheim currents) this decay will be exponential with time. If the current through the second insulator ($A\ell_2O_3$) is considered negligible the current through first insulator is given by:-

$$J_1 = -\left(\frac{\varepsilon_1}{d_1} + \frac{\varepsilon_2}{d_2}\right)\frac{dV_1}{dt} = \frac{V_1}{R_1} \qquad (3)$$

where R_1 is the resistance of native oxide and defined in the form

$$R_1 = \rho_1 d_1 = \rho_{10} d_1 e^{-\alpha_1 (V_1/d_1)} \qquad (4)$$

where ρ_{10}, α_1 are constants.

A solution of Equation (3) yields

$$\Delta V = V_G + \frac{1}{\beta_1} \ell n\ \beta_1 \beta_2 V_G \tau \qquad \text{for } \Delta V > 1 \text{ Volt} \qquad (5a)$$

and

$$\ell n\ \Delta V = \beta_1 V_G + \ell n\ \beta_2 V_G \tau \qquad \text{for } \Delta V < 1 \text{ Volt} \qquad (5b)$$

where β_2 is a constant of $A\ell_2O_3$
τ is the pulse duration.

Figure 3 is a plot of C-V shift (ΔV) as a function of τ for an MAOS system with native oxide thickness $\sim 60\text{Å}$. Experimental results therefore agree quite closely with the theoretically proposed model above. A value for β_1 can be found from the slope of straight lines in Figure 3 (a). It is interesting to note the change in the slopes of the straight lines for $V_G \geq 16V$. The ratio of the slopes is almost exactly 2 : 1. This may suggest that at a critical field, hole injection as well as electron injection into the native oxide takes place.

Since our GaAs MAOS system has an insulator with a narrower band gap nearer to the semiconductor, the mechanism which governs the charging of the double oxide interface is different from the discharging with no applied gate bias (storage mode). Figure 5(a) shows the charging mode of a MAOS device with positive gate bias. Using Equation (2) with $\varepsilon_1 = 4$, $\varepsilon_2 = 8$, $d_2 = 600\text{Å}$, $d_1 = 60\text{Å}$, one

obtains a band edge lowering of ~ 1.5 V for a gate bias of +10V. Since the band gap of native oxide is ~ 5eV this lowering is quite substantial for indirect tunnelling. It is curious to note that the change in the slopes of the charging curves (Figure 3) occurs when native oxide conduction band is lowered almost exactly to the Fermi level (i.e. a lowering of 2.5V). After the gate bias is removed the double oxide interface will be slightly raised due to the stored negative charges. However, this rise will not be enough for indirect back tunnelling up to a ΔV value of ~ 6V for d_1 = 60Å. (For larger values of d_1, the critical value for ΔV will also become larger). For ΔV values less than the critical, the charge loss mechanism is likely to be direct tunnelling. A comparison of GaAs MAOS system with Si MNOS system (Figure 5) shows the clear advantage of long term charge storage properties of GaAs MAOS, since d_1 can be made quite large without causing much difficulty in charging or discharging mode.

Charge retention tests were carried out at room temperature by first applying a pulse of +20V for 1.5s to the gate and then measuring ΔV at regular time intervals (d_1 = 60Å). The first measurement of ΔV was made 30 secs. after the application of the pulse. The diode was stored with no gate bias between measurements. The backshift of the C-V curves (i.e. ΔV) is then directly proportional to log τ, 0.25V/decade of time or better.

Figure 6 shows the charging and discharging of a GaAs MAOS device as a function of gate bias with pulse width (τ) as a parameter. Effective threshold voltages for charge storage can be found by extrapolating the straight line portion of each curve and clearly as the pulse width increases the threshold voltage decreases. The slopes of the charging and discharging portion of the memory cycle (i.e. τ = 1.5 sec curve) are the same which indicates that indirect tunnelling again takes place in the erase mode. Figure 7 shows the ΔV dependence on V_G for MAOS diodes with different native oxide thicknesses (d_1). Pulse width was kept constant at 120ms. Again, as expected, the threshold voltage increases with increase in native oxide thickness. The slopes of the curves however decreases with the increase in d_1.

Investigations of the properties of the GaAs MAOS devices will be continued utilising MAOS FETs. For this purpose FETs

similar to that described in reference (1) (scheme a) will be used. This time instead of anodically grown $A\ell_2O_3$, an evaporated SiO layer is being used which satisfy the necessary requirements for the thin film epitaxy process.

REFERENCES (Chapter 2)

(1) B.Bayraktaroglu, E. Kohn, H.L. Hartnagel, "First Anodic-Oxide GaAs MOSFETs based on Easy Technological Processes", Electronics Letters, 12, No. 2, pp53-54. 1976.

(2) D.L. Lile, A.R. Clawson, D.A. Collins, "Depletion-mode GaAs MOSFET", Applied Physics Letters, 29, p207, 1976.

FIGURE CAPTIONS

Figure 1 Overpotential versus time curves of anodically grown double oxide structures on GaAs.

Figure 2 C-V plots of double oxide structures on GaAs with 150Å of $A\ell$ at the GaAs interface.

Figure 3 C-V shift (ΔV) versus charging time (τ) with pulse height (V_G) as a parameter.

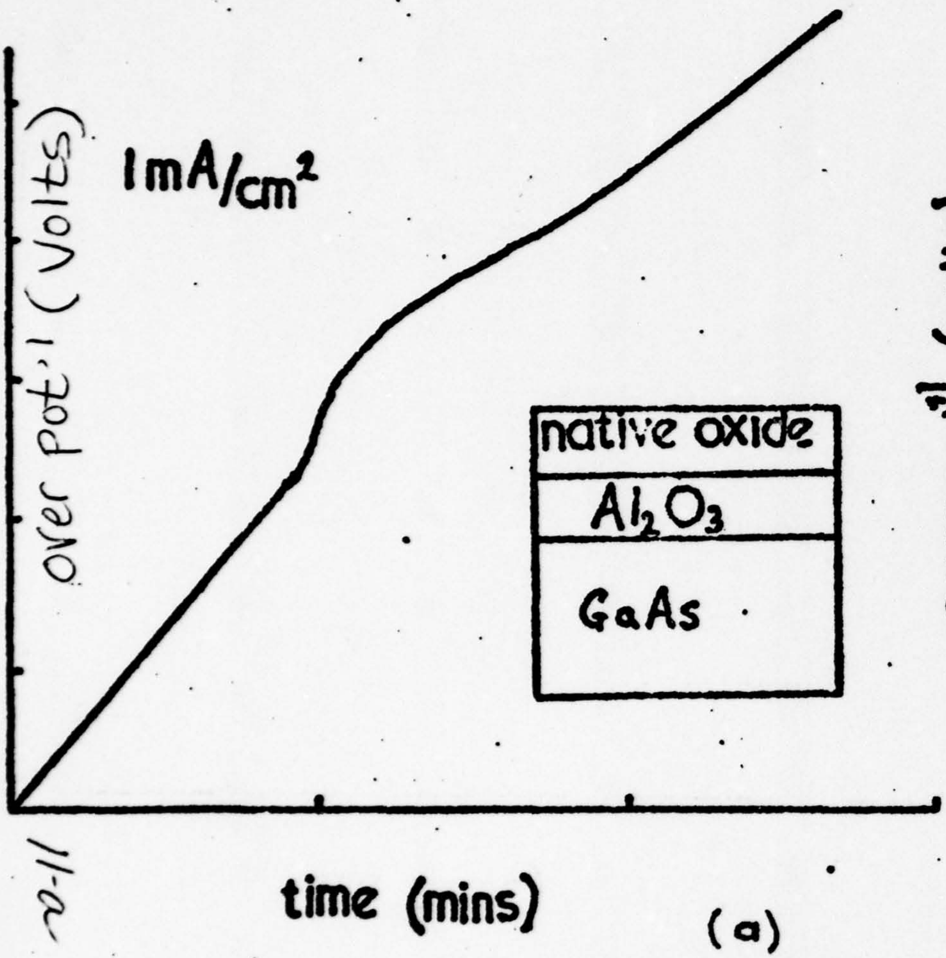
Figure 4 Energy-band diagrams of GaAs MAOS system in charging and storage mode.

Figure 5 Comparison of GaAs MAOS and Si MNOS systems in charging and storage mode.

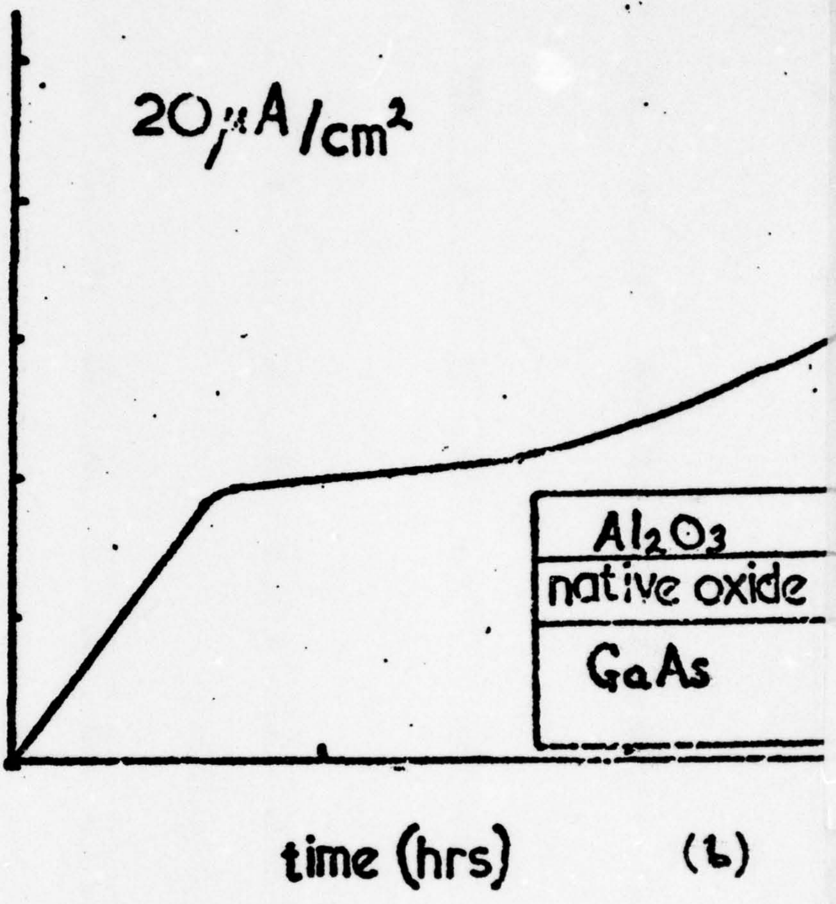
Figure 6 ΔV versus pulse height (V_G) with pulse width (τ) as a parameter and memory cycle for $\tau = 1.5$ sec.

Figure 7 ΔV versus pulse height (V_G) with native oxide thickness (d_1) as a parameter.

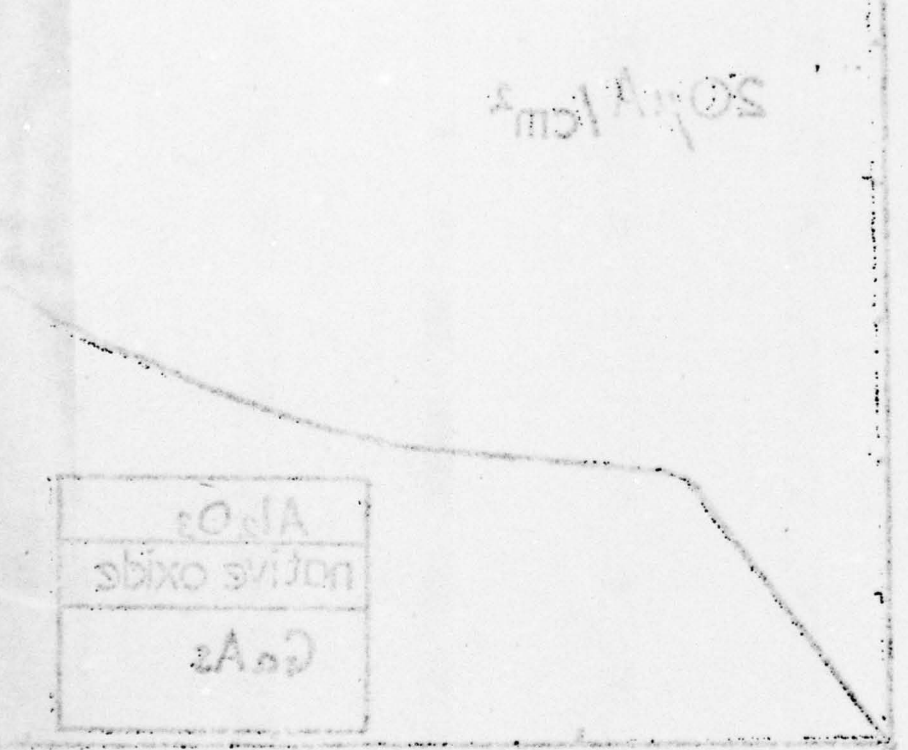
Fig 1



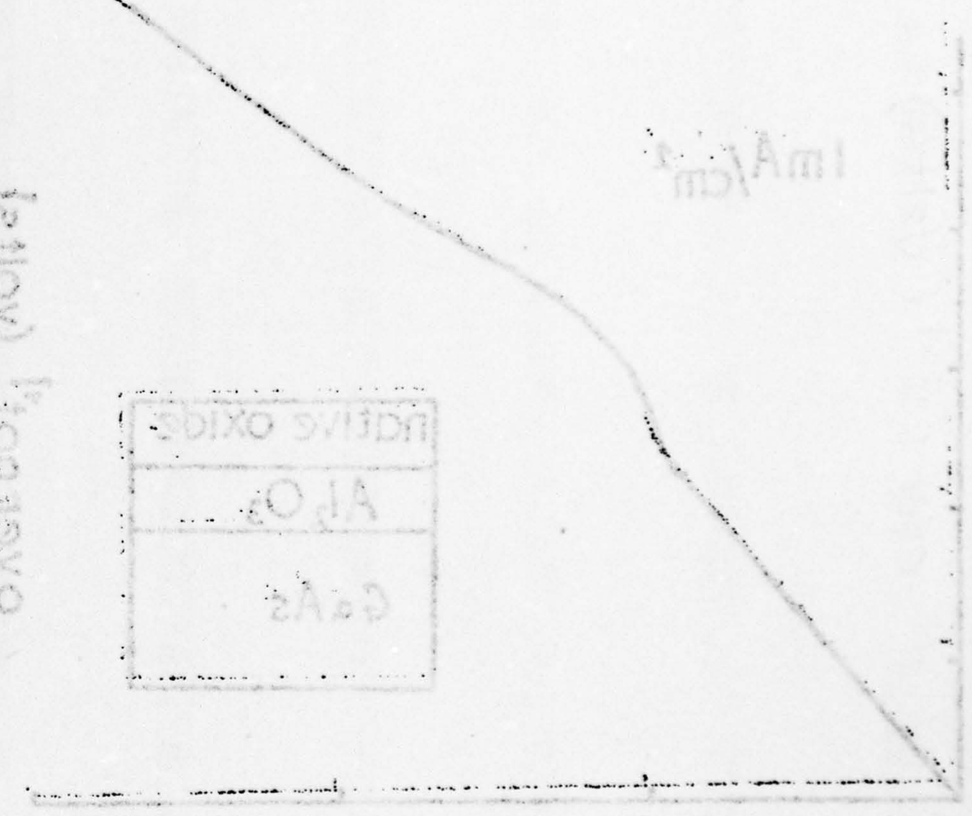
(a)



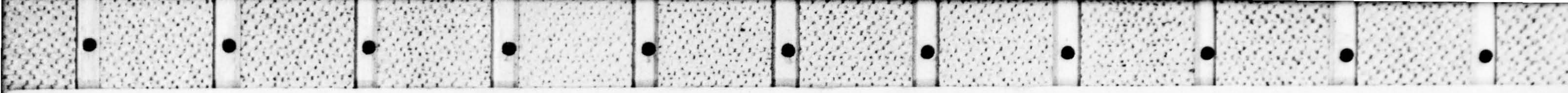
(b)



20μA/cm²
Al2O3
native oxide
GaAs
time (hrs)
(b)



overpot. (volts)
1mA/cm²
native oxide
Al2O3
GaAs
time (mins)
(a)



C/pF

140

100

Sample: M2/B2
Frequency: 1 KHz
Ramp speed: 0.5 V/Sec

-20 -15 -10 -5 5 10 15 20 25
Vc/V

(a)

C/pF

140

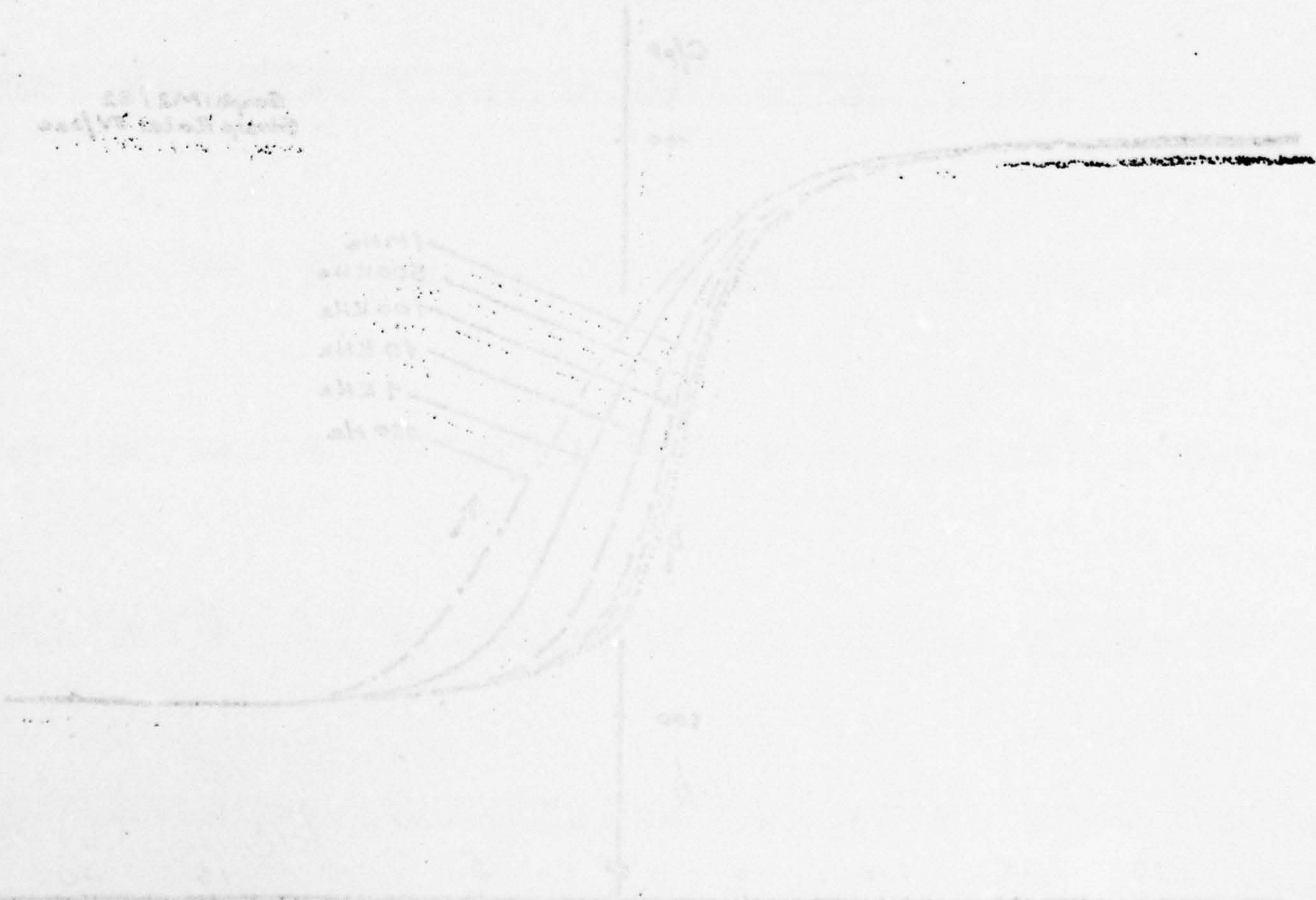
100

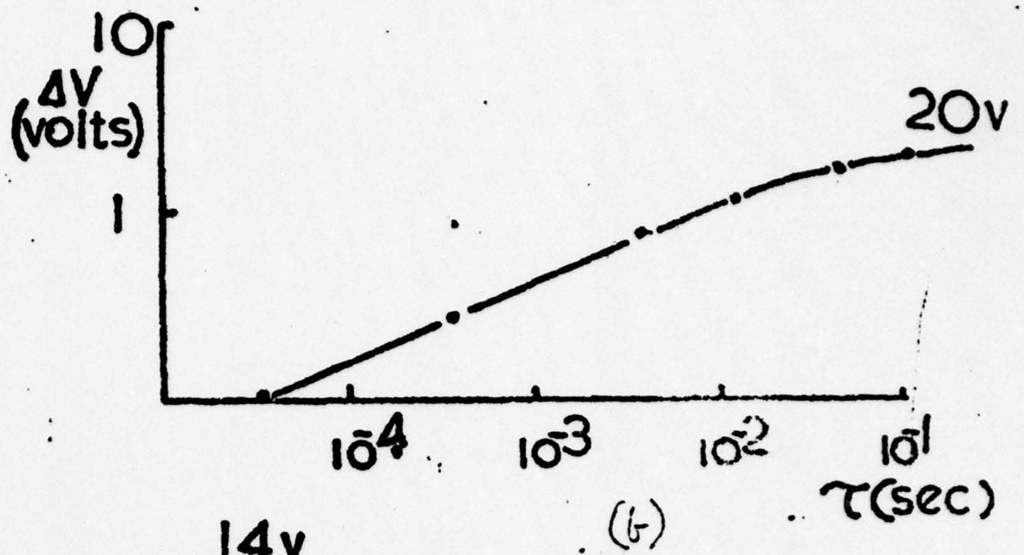
Sample: M2/B2
Sweep Rate: 5V/sec

1 MHz
500 KHz
100 KHz
10 KHz
1 KHz
250 Hz

-20 -15 -10 -5 5 10 15 20 25
Vg/V

FIG 2 (b)





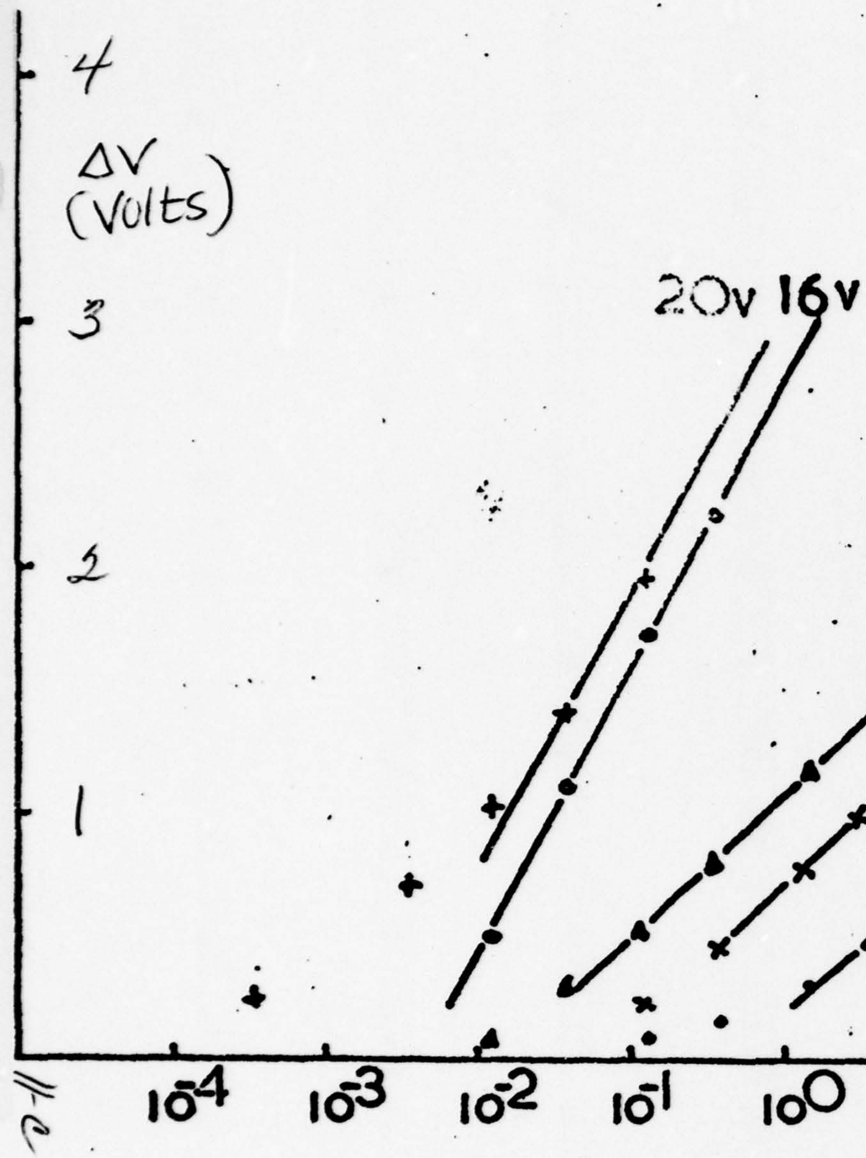
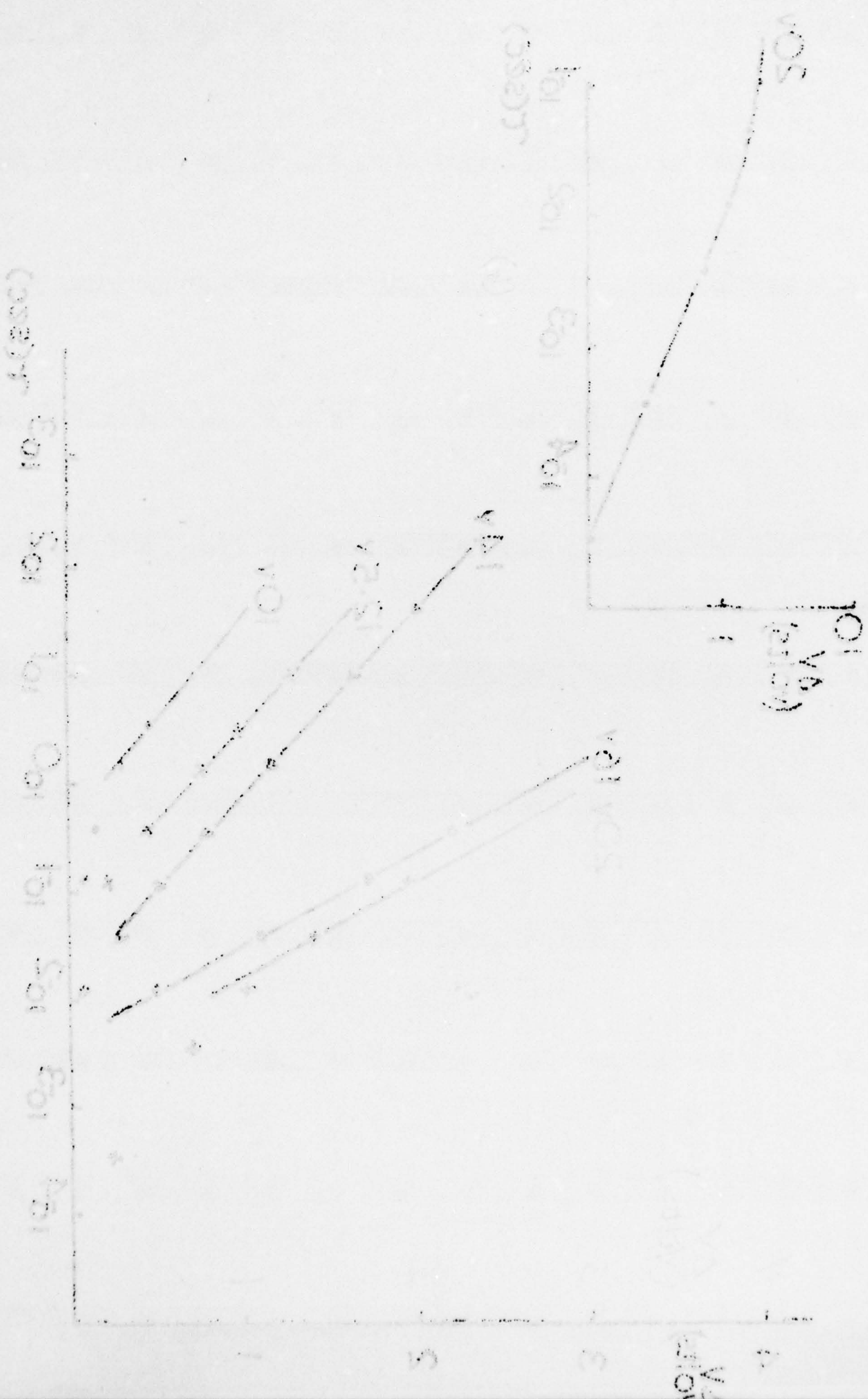
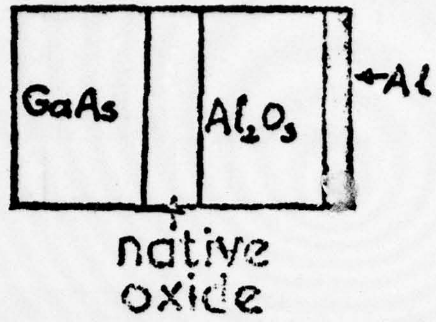
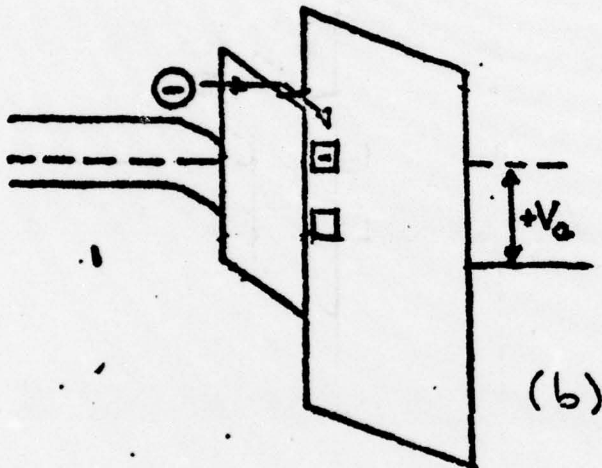
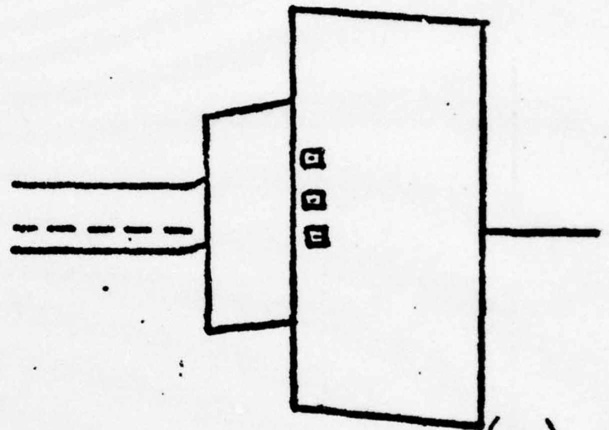


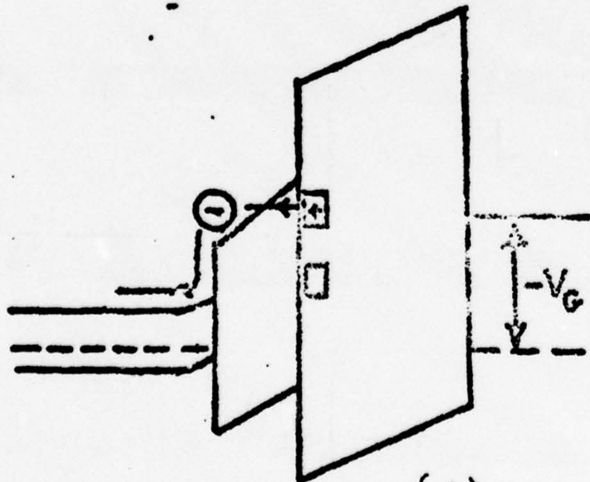
FIG 3











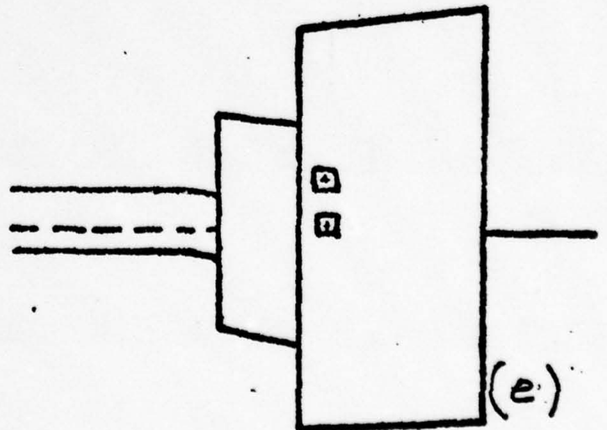
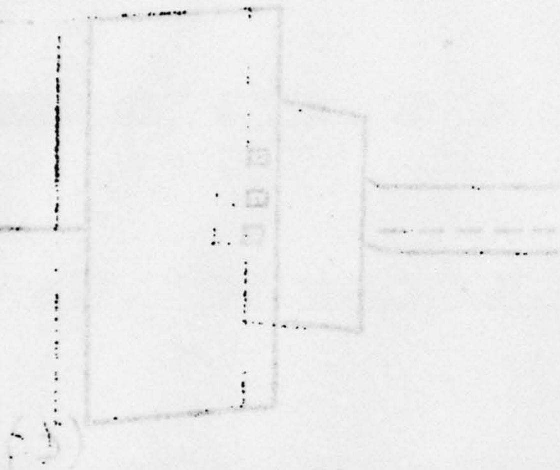
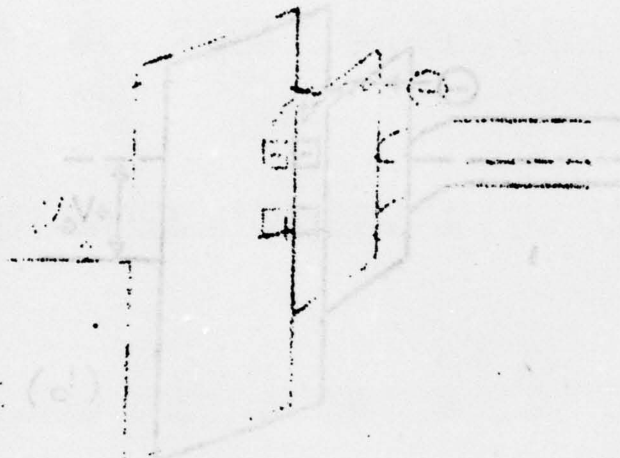
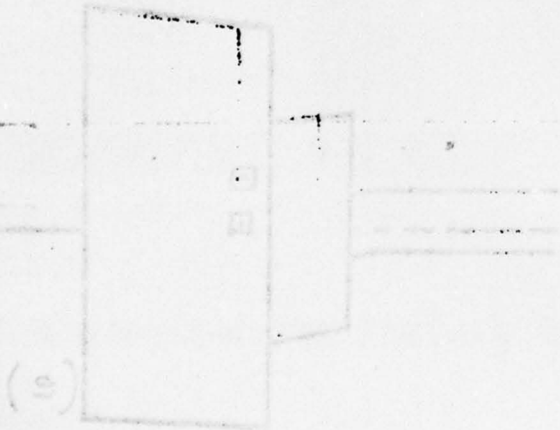
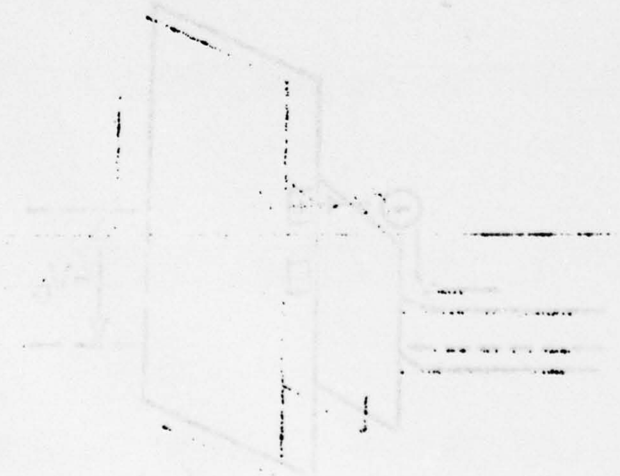


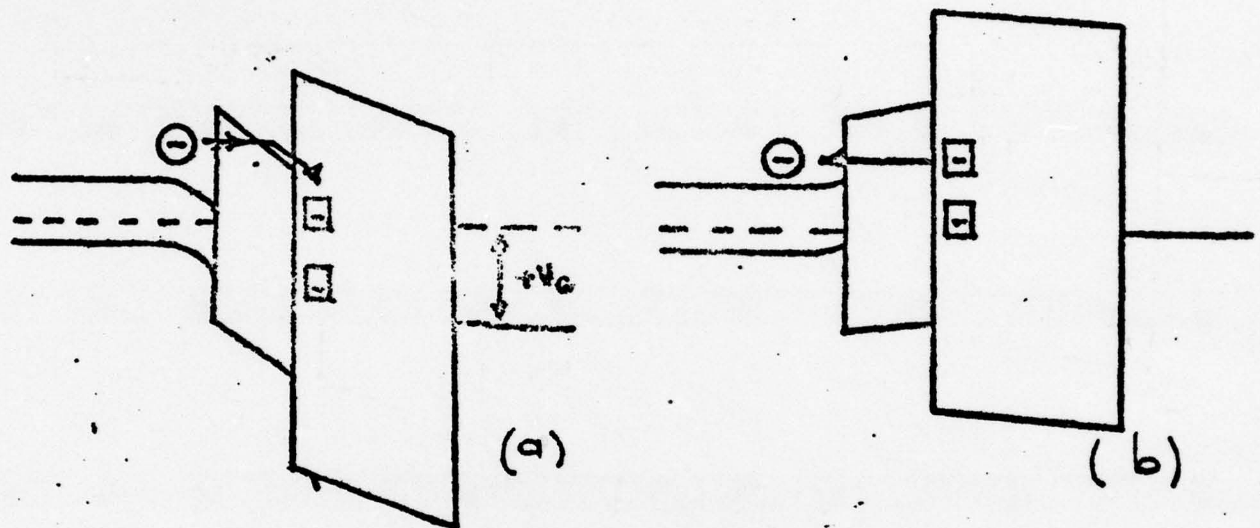
FIG 4



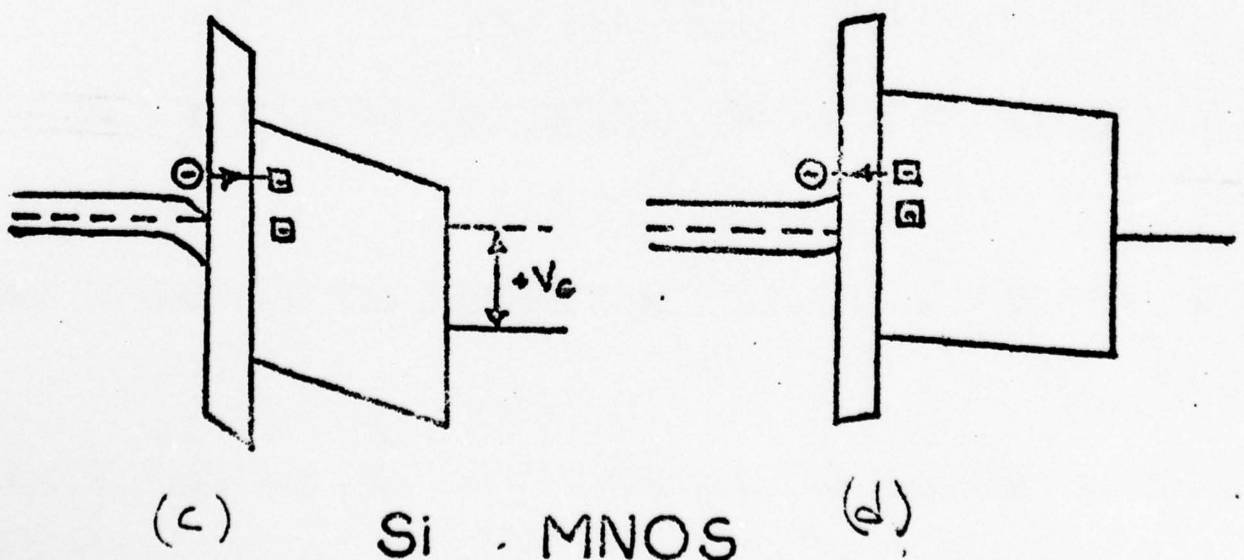








GaAs MAOS



(c) Si MNOS (d)

FIG 5

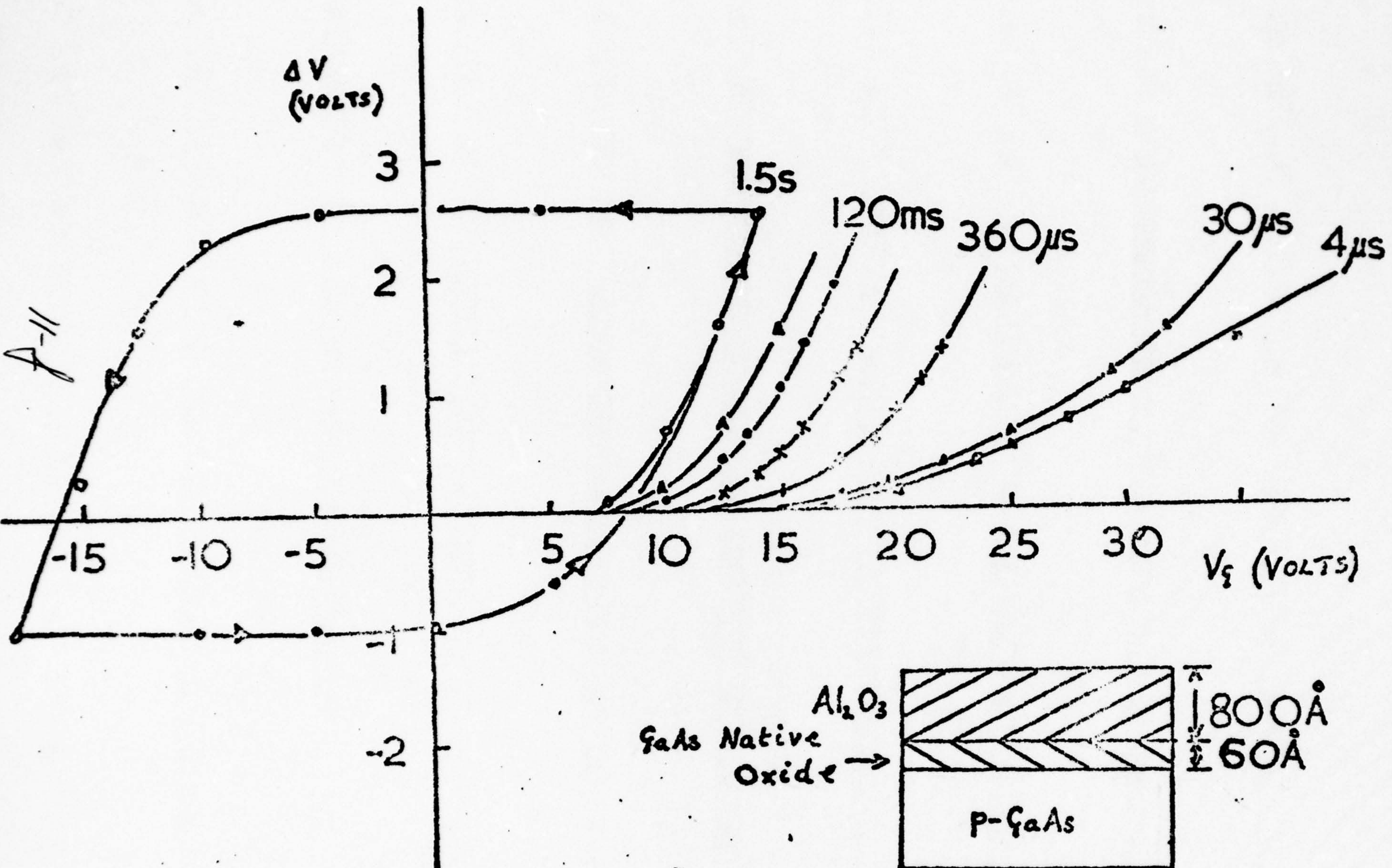


FIG 6

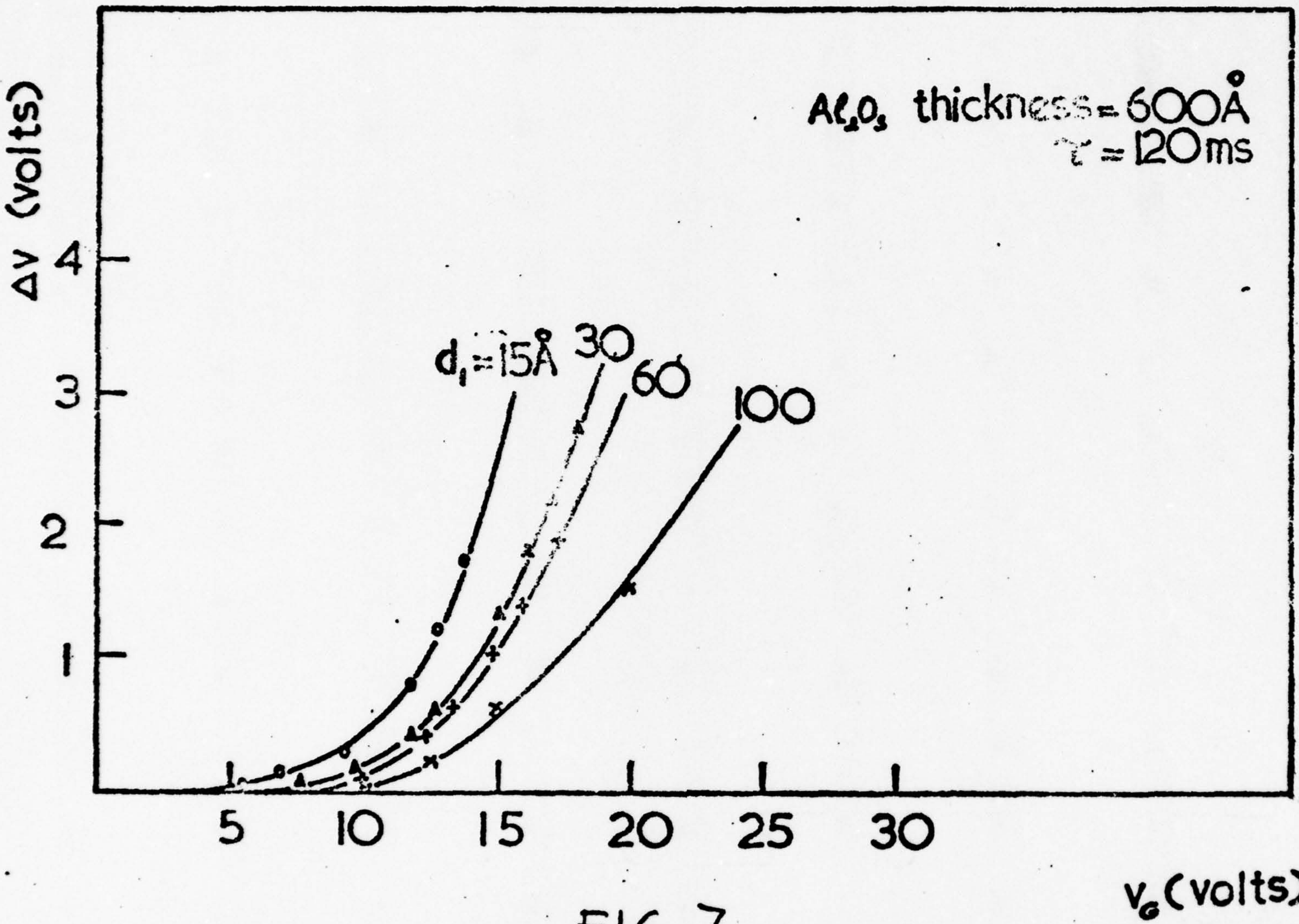


FIG 7

CHAPTER 3

3. MOS-Devices

(B. Bayraktaroglu, A. Colquhoun, S.J. Hannah, E. Kohn)

3.1 Introduction

Last year preliminary results with GaAs-inversion layer MOSFETS were achieved.[1] However at that time it was not possible to explain in detail why the dc-characteristics were essentially different from those predicted by the material data.

Therefore the electrical behaviour of MOS-diodes has been studied extensively by means of CV-, GV- and IV- measurements at various temperatures in various frequency ranges and under various transient conditions.

A number of disadvantages of the anodic MOS-system were identified, mainly due to a charge injection phenomenon into the oxide and, as a result, the development turned towards the incorporation of an Aℓ-oxide layer into the system (see chapter by B. Bayraktaroglu) and by this towards a new technique of oxide growth.

The annealing of MOS-diodes has continuously been optimised in several respects. It was seen that high temperature annealing, even in N_2, leads to partially crystalline and decomposed oxides (see chapter by B.L. Weiss). H_2 annealing even below 350^oC was found to lead to a highly unstable hysteresis.

From these results a "Standard Oxide" was produced, grown at a low current density and annealed in N_2 at 350^oC for 10 min incorporating a rapid cooling, which was then incorporated into the FET structures.

A newly designed Inversion-Layer MOSFET (IL-MOSFET) with a reduced gate length of 5μm was fabricated. The dc-characteristics could be directly related to the results of the MOS-diode measurements. Despite the difficulty to achieve proper inversion, a field effect mobility of $\mu \approx 2250 \frac{cm^2}{Vs}$ was estimated.

Secondly, a new Enhancement-Depletion Mode MOSFET (EDM MOSFET) on insulating substrate was developed. The device has been fabricated in both self-aligned and non-self-aligned gate techniques

and is suitable for monolithic integration. Especially the enhancement mode capability of the device is essentially larger than that of MESFETs, JFETs or SIGFETs.

3.2 Investigation of Growth and Annealing Parameters

(B. Bayraktaroglu, S.J. Hannah, E. Kohn)

Problems in the IL-MOSFET fabrication process already lead to an optimisation in the oxide growth technique and annealing parameters last year.[1]

This was now followed by a systematic investigation over a wide range of annealing temperatures for various annealing gases and oxides grown under various conditions. CV- and IV- measurements as well as structural investigations (see chapter by B.L. Weiss) were carried out.

Minimising the effects of crystallinity, leakage current and hysteresis lead to a "Standard Oxide" fabricated at a low current density of $I \lesssim 0.1\ mA/cm^2$ only limited by the desolution current of the diode in the electrolyte of $I_o \approx 35 \mu A/cm^2$, an annealing temperature around 350^oC with an annealing time of 10 min in N_2, rapidly cooled down. Annealing in O_2 for 2 hours was found to stabilise breakdown characteristics, but may effect an ohmic contact metalisation.

Figure 1 shows the hysteresis amplitudes at a capacitance corresponding to the mid-point of the CV-curve shift between accumulation and inversion for MOS-diodes produced under various conditions. The lowest values (open circles) correspond to diodes fabricated under otherwise optimised conditions. The leakage current behaviour of them is demonstrated in Figure 2. The IV-curves obtained had principally a transient characteristic even for the high currents in the high temperature annealed samples and the data demonstrated were taken after 30 min of applied stress bias. The dc-conductivity increases exponentially above 350^oC, reaching the $\mu A/cm^2$ - range at 700^oC for a gate bias of +15V (d_{ox} = 1000Å). In this case the capacitance behaviour can be explained by the dc-current flowing. Slowly cooled samples appeared less stable and showed a higher leakage current density.

The slope in the CV-curve could not be influenced essentially by the various annealing atmospheres (H_2, O_2, H_2O, N_2, Ar_2). It means that the annealing process changes the bulk oxide properties

even at low temperatures, but only to a lesser extent the interface properties. The interface then is degraded at higher temperature, probably due to some crystallisation effects.

3.3 Measurements on "Standard Oxides"

E. Kohn

A wide range of measurements were undertaken in a temperature range of 77k to 350k in the CV-, GV- and IV- domain, applying various transient conditions as in particular: RF-capacitance voltage and partially parallel conductance voltage measurements from nearly dc up to 10MHz, operating the gate bias in the switching mode and applying a ramp speed from (nearly) zero to 1000V/sec. (The instrumentation used consisted of a 2-phase lock-in amplifier (Ortholoc), a Boonton Bridge (75C), a capacitance measuring assembly (GE 1620-A), an automatic CV-plotter[2], and a system where the rf-current into the MOS-diode is measured by means of a series resistance and the amplified signal then displayed on an Oscilloscope;) Quasi static CV-measurements by means of the DC-slow linear voltage ramp method (using a Keithley 602 Electrometer), and DC-current voltage measurements (with a Keithley 602 Electrometer) in a quasi static condition and the switching mode of the gate bias.

As in most MIS-systems we see a charge injection instability in the anodic oxide GaAs-MOS system. This is demonstrated in Figure 3 by a stress bias experiment showing an asymetric and anti-clockwise hysteresis for p-type material (and correspondingly a clockwise hysteresis for n-type substrate). The writing speed of the curve is fast enough (15V/sec) to show nearly parallel shifted curves, so that the shift may be directly related to a flat band voltage shift (V_{FB}-shift), although there is a difficulty to verify the flat band voltage condition.

The V_{FB}-shift can widely be approximated by a logarithmic time dependence (Figure 4), with an initial delay time for charge storage and a saturation for average applied fields of less than approximately 2 x 10^6 V/cm. For higher fields charging occurs up to breakdown of the interface barrier.

Further information on charging was gained from transient IV-measurements. The initial delay in the V_{FB}-shift offers the possibility to determine the bulk oxide conductivity from the initial current response in a switching experiment, whereas after V_{FB}-shift

saturation the barrier limited steady state current is determined.[3] Figure 5 shows the IV-characteristics for the initial current response (measured approximately 1 sec after switching) and the steady state current (taken after 30 min), where the gate bias now has to be corrected by the flat band voltage shift. The plot of I vs. $\sqrt{V_G}$ shows a widely linear range for both the initial current response and the corrected steady state current pointing towards initially bulk oxide limited IV-behaviour by Poole-Frenkel conductivity and barrier limited behaviour by Schottky-emission in the steady state case. An $\varepsilon_{dyn} \approx 4.5$ to 5.5 is derived, implying the basic Poole-Frenkel effect, whereas optical measurements show $\varepsilon_{opt} = 3.3$ and CV- measurements $\varepsilon_{stat} \approx 8$.

The time delay of the currents under constant applied gate bias obeys a $I \sim t^{-a}$ low with $a = 0.4$ to 0.9 except in the initial phase, which is a well known behaviour for space charge effects in oxide films.[3] The amount of trapped charge is found by integrating the (charging) current in time until the V_{FB}-shift saturates. The charge centroid[4] was found to reach values up to $d_{ox}/2$, indicating that the span of the charge distribution extends across almost the entire thickness of the insulator. Steady state currents between 10^{-9} A/cm² and less than 5×10^{-11} A/cm² (which was the resolution of the measuring equipment) at average external fields of 2×10^6 V/cm have been measured, indicating the spread of the experimental data.

As indicated above, the V_{FB}-shift does not saturate for high applied fields, but approaches the stress bias. After some time under stress bias a high ohmic conductivity appears and the capacitance collapses. However the breakdown is not destructive. Nearly unchanged CV-curves, but with slightly reduced charging characteristics and reduced area of safe operation, appear after recovery (which can take some days). Obviously breakdown appears across the interface barrier, which had taken most of the oxide field, with partial degradation of the barrier region. The IV-characteristics obtained after formation and recovery are very similar to those obtained from the initial current response but without hysteresis effects or dependence on the writing speed and do not show a saturation at high fields (as in the initial current response curves probably due to a fast V_{FB}-shift). Measurements in the temperature range of the bulk limited current case after formation yields a thermal activation energy of 0.65 eV for the

Poole-Frenkel defects.

The above results show that the charge injection across the interface is best described by a combination of tunnelling and trapping processes as : for low fields direct tunnelling into oxide traps with a high back tunnelling probability, for medium fields additionally trap assisted tunnelling into the oxide conduction band with successive trapping of charge deep in the bulk oxide and for high fields direct tunnelling into the oxide conduction band or avalanche breakdown across the interface barrier.

For further characterisation by CV- and GV- measurements, two facts from the above results have especially to be considered : 1. in steady state measurements the gate bias has to be corrected by the V_{FB}-shift, and 2. assuming a direct tunnel process involved in the charge injection phenomena, a single time constant at a certain given interface potential is not to be expected for the dynamic interface loss.

But even taking this into account, an "anomalous" frequency and temperature dispersion is found[5] as demonstrated in Figures 6 and 7. At high frequencies and low temperatures a decay in the slope of the CV-curve is observed, which cannot be explained by classical freezing-out of interface states considering reasonable values for capture cross sections at the particular surface potential (which may be estimated from MOSFET measurements).

Applying the technique after Nicollian and Goetzberger[6] and plotting the data of capacitance and parallel conductance in a Cole-Cole diagram[7] (between 5KHz and 500KHz) fail to obtain information on surface potentials and interface-state densities. Especially the Cole-Cole diagram shows that no semiconductor depletion layer capacitance can be extrapolated.

Thus the commonly applied interface model and equivalent circuit is very much in doubt. Fitting the data into the diffusion model[3] or including a metamorphologic layer[9] also does not give satisfactory results. It means that at present no model is available to explain all phenomena of the interface in question. The behaviour can probably be explained much better by oxide-dispersions. New stimulations are expected in connection with the characteristics of EDM-MOSFETs. The capacitance shift $\frac{C_{max} - C_{min}}{C_{max}}$ was always less than that predicted for $\frac{C_{ox} - C_{inv}}{C_{ox}}$

(see Figures 6 and 7), thus doubting if accumulation or inversion are possible at all. Plots of C_{max} vs. $\frac{1}{d_{ox}}$ for various doping concentrations ($2 \times 10^{16} cm^{-3}$ to $2 \times 10^{17} cm^{-2}$) and both p-type and n-type material (at 5KHz) however indicate a band bending towards accumulation to $E_{acc} - E_{c,v} < 0.08eV$ (even taking into account charge injection and related V_{FB}-shift). Thus band bending is mainly limited at weak inversion. This is confirmed with MOSFET measurements.

The characteristics appear with corresponding tendency for p-type and n-type substrate, and it seems improbable to assume a simple interface trap causing pinning in weak inversion but more likely we see minority carrier response with oxide traps (also causing the ledge in the deep depletion CV-curve) or oxide dispersion.

If no inversion layer charge is built up at the interface the deep depletion CV-curve is measured. The effect is seen in transient measurements as the non steady state case or stably if high leakage currents are passing through the film. The latter case can be excluded for the system in question.

The transient between the deep depletion branch and the inversion branch of the CV-curve is mainly determined by the balance between minority carrier generation in the GaAs depletion layer and interface generation-recombination. These processes have been studied (in the dark) by means of Zerbst-plots[10] and the linear sweep MOS-C technique.[11] Both methods show good agreement and result in (bulk) minority carrier life times of:

$$\tau_n = 3.1 \times 10^{-11} \text{ sec} \quad (\rho \approx 1.8 \times 10^{17} \text{ cm}^{-3})$$

$$\tau_\rho = 3.6 \div 4,5 \times 10^{-10} \text{ sec} \quad (n \approx 2 \times 10^{16} \text{ cm}^{-3})$$

The Zerbst-plots also give information on the surface generation velocity, which is obtained to :

$$S_n = 5.7 \times 10^5 \frac{cm}{sec}$$

$$S_p = 1.5 \times 10^4 \frac{cm}{sec}$$

(The data obtained from substrates, as used in the other CV-measurements). From this data the inversion layer cut-off frequency

can be obtained. Due to uncertainties in the inversion level only a rough estimation is possible with f_c in the lower Hz range. In fact the transition between the LF-CV curve and the HF-CV curve was found to appear around 10Hz.

From the above results the disadvantages at least due to an unstable interface barrier behaviour becomes obvious. New developments lead therefore to the incorporation of $A\ell_2O_3$ into the system (see chapter by B.Bayraktaroglu).

3.4 Inversion layer FETs *
(E. Kohn)

New inversion layer FETs (IL-FETs) with a reduced gate length of 5μm have been fabricated on p-type GaAs ($p \approx 5 \times 10^{16}$ cm^{-3}) incorporating the "standard oxide" and using the technology previously reported as Scheme B. Gate oxide thickness was 1000Å, gate width 200μm.

The output characteristic is shown in Figure 8. The highly conducting "mode" of the oxide is present due to the nonhomogeneous field distribution under the gate as seen from the splitting of the curves at the origin. The transconductance is still too low, indicating that only part of the gate bias is effective. The characteristics at the onset of saturation, namely the drain current at saturation I_{DS} and the source to drain voltage at saturation V_{DS} with the gate bias as parameter, were compared with a simple theory involving:

1. the gradual channel approximation,
2. a drift velocity field approximation of $\mu_o E$ for $E < E_C$ and $\mu_o E_C$ for $E \geq E_C$ with μ_o=low field mobility,
3. an amount of the inversion layer Fermi level equal to the corresponding bulk Fermi level (which determines basically the threshold voltage).

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*We wish to thank Professor H. Beneking from the Institute for Semiconductor Electronics at the RWTH Aachen (West Germany) for some special technological facilities made available for this work and M. Heyer from the abovementioned Institute for supplying the epitaxial material.

4. approximately zero source and drain contact resistances, and
5. a grounded substrate connected to source.

The expressions for I_{DS} and V_{DS} give then curves of these quantities vs. the gate voltage V_G at the onset of saturation. The resulting V_{DS} vs. V_G is given by Figure 9. Agreement between theory and experiment can only be considered to be acceptable if only a small portion of the applied gate bias V_G* is considered to be effective due to band pinning in (weak) inversion. With this value of V_G* the drain current at saturation $\frac{I_{DS}}{\beta}$ normalised on the geometrical factor $\beta = \frac{W.G\ \mu_o}{L_G}$ is obtained (Figure 10) and finally curve fitting with the device current leads to an inversion layer mobility of $\mu_o \sim 2300\ \frac{cm^2}{Vs}$ as given in the inset of Figure 10.

The result reflects the limitations given by the MOS-system used. The main question which remains is the achieving of proper inversion. Latest developments (see chapter by B. Bayraktaroglu) however have not yet been incorporated. The inversion layer mobility does not restrict possible microwave applications.

3.5 Enhancement-Depletion Mode MOSFETs
(A. Colquhoun, E. Kohn)

The result of the "standard oxide" measurements encouraged us to develope EDM-MOSFETs with the aim to operate them mainly in the enhancement mode.

Devices were realised in a self-aligned and non self-aligned gate notched channel structure on semi-insulating substrate. A cross section (Figure 11(a), (b)) shows that the structures are basically a variation of the notched channel concept as frequently used for MESFETs, JFETs and SIGFETs.

The technology used for the non self-aligned gate structure is basically that previously reported as scheme B[1] however with some modifications due to the SI-substrate. Therefore only the technology used in the self-aligned gate structure is described briefly.

The device area was first defined by mesa etch, followed by Au Ge metallisation for source drain and rear side contacts. Next the gate and contact pad areas were opened with a negative (or equally well positive) photoresist mask. Subsequently the oxide

layer was formed in the gate area only. For that purpose an ohmic contact at the rear side is needed to achieve good electrical contact through the semi-insulating substrate and the growth has to be supported by illumination (see chapter by A. Colquhoun).

The "notch" of the structure was formed by the etching of the GaAs surface during the same anodic oxidation step which was used to grow the gate oxide. The amount of this etching was basically determined by the voltage supported across the gate oxide, also taking into account the dissolution rate of the oxide in the electrolyte and the etching during the passivation time. The oxide was then thinned in a 0.5% HCℓ solution to a thickness of 900Å (interference colour) immediately followed by Aℓ gate metal evaporation. Subsequently float-off of the photoresist produced the final structure. The oxide was then annealed as in the case of the "standard oxide".

The output characteristics of a device fabricated on a VPE-layer ($n \sim 5 \times 10^{16} cm^{-3}$, without buffer layer) are shown in Figure 12. The output current capability in depletion mode is limited by the maximum stable depletion layer width given by the inversion level. As a transient behaviour however a deep depletion mode is possible resulting in a depletion characteristic similar to that of MESFETs. (For the particular device presented the notch was adjusted to make pinch-off possible in the dc-mode).

In enhancement the transconductance vs. gate bias does not follow the square law behaviour but saturates. This is to be expected in the particular device presented because of an increasing dynamic series resistance in the unetched area on either side of the gate and charge injection into the oxide and related V_{FB}-shift of the MOS-system. In comparison Figure 12 also shows the MESFET characteristics of the identical channel, where the oxide layer was removed and replaced by a metal Schottky contact. The output current saturates when the active channel area near the source contact is completely opened and the gate diode becomes conducting, whereas the MOSFET characteristic is basically limited by oxide breakdown (approximately 15 V). However the transconductance of the MOSFET device is reduced by approximately 22% but can certainly be improved by using thinner oxides. Hysteresis effects are not essentially different and are thus mainly caused by deep traps in the material.

The realisation of the EDM MOSFET is possible on the same material as used for MESFETs or TEDs and thus the new device represents also an additional element in these circuits. However the incorporation of an n^o-buffer layer with a high electron mobility is needed to achieve a high transconductance.

First dynamic measurements show a small signal rise-time of better than 1 ns for non self-aligned gate devices with 10μm gate length.

Further investigations into the enhancement mode as well as transient depletion mode behaviour, the dynamic behaviour and stability behaviour, are to be carried out next.

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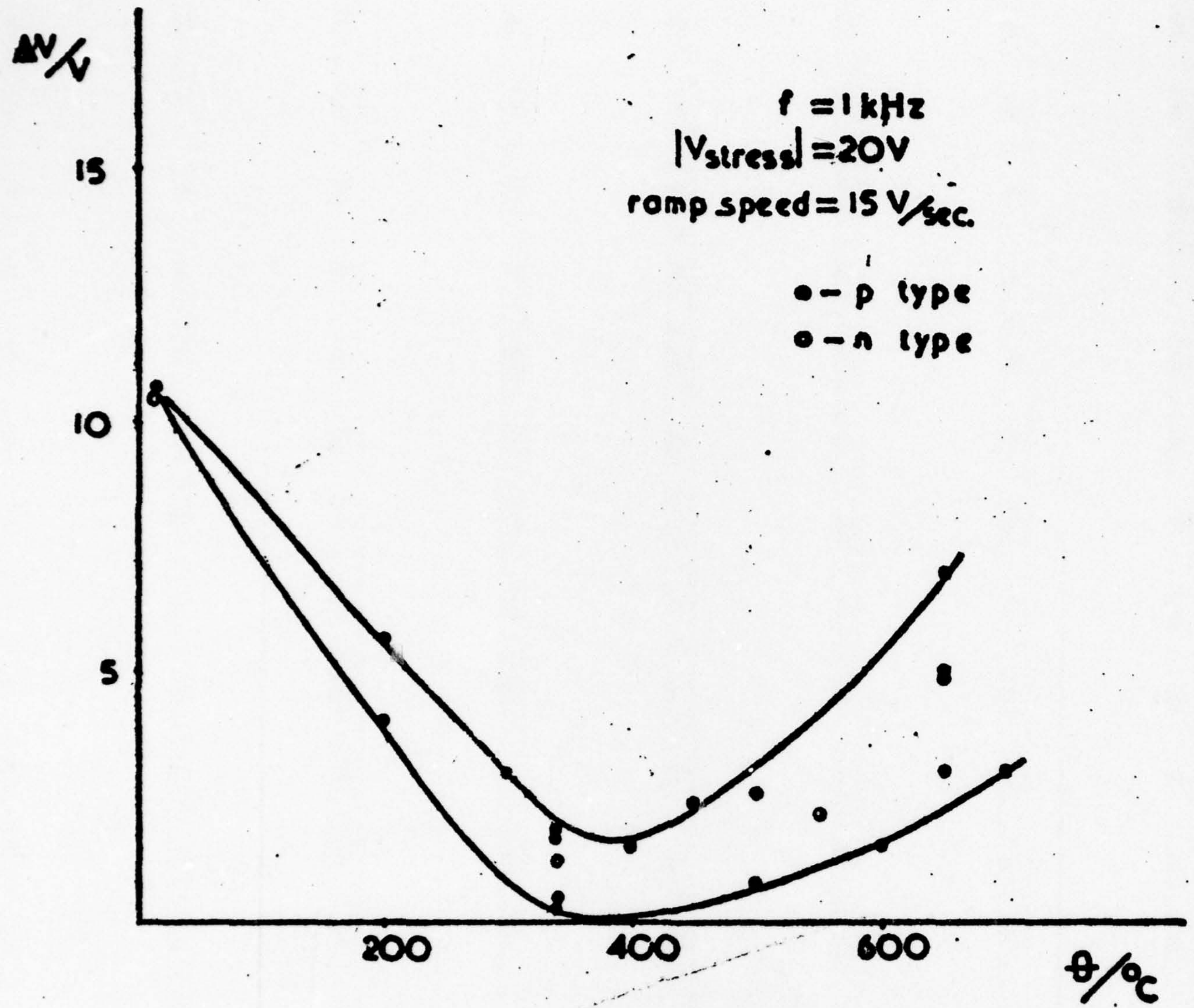
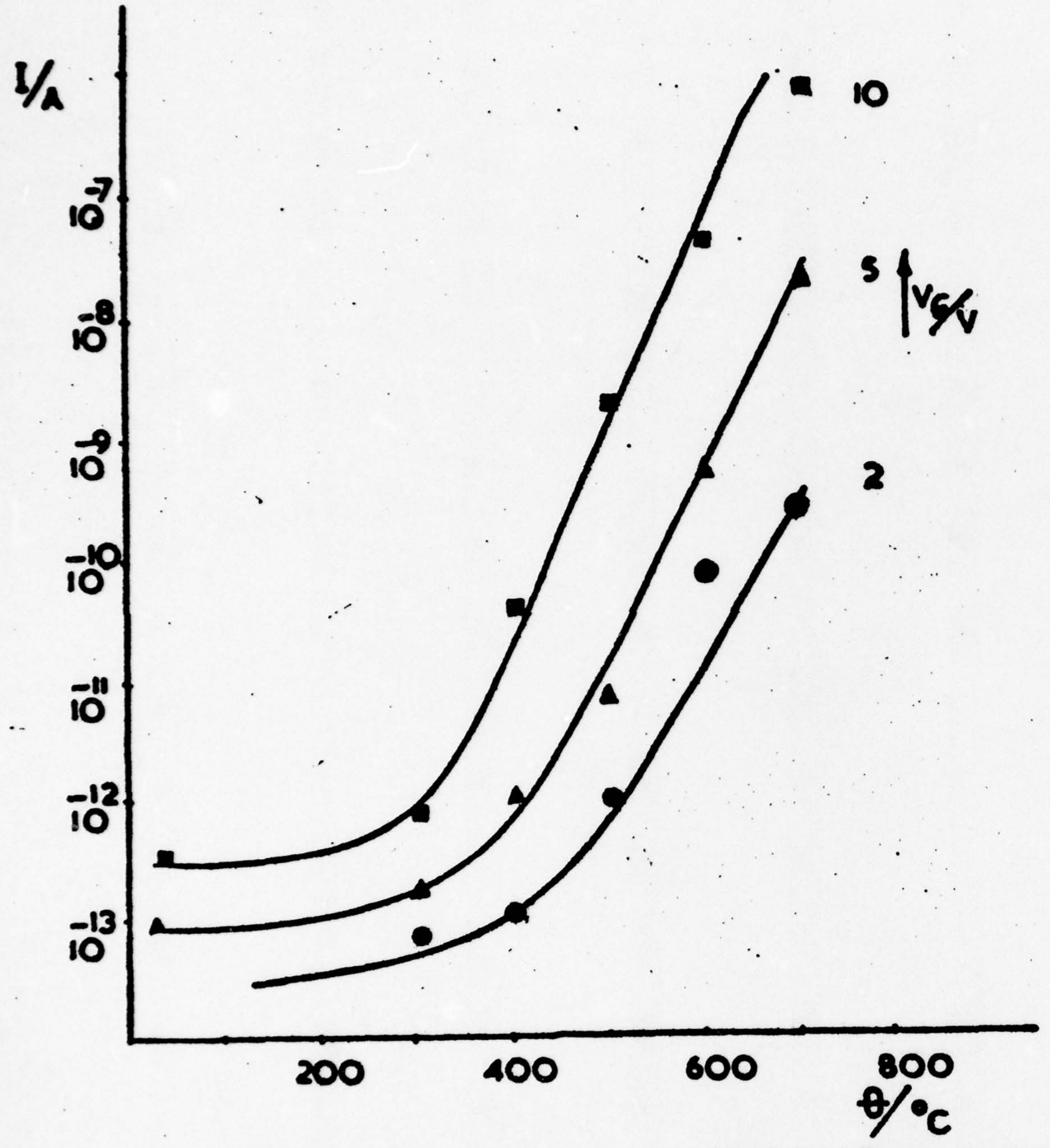


Hysteresis vs. Annealing Temperature

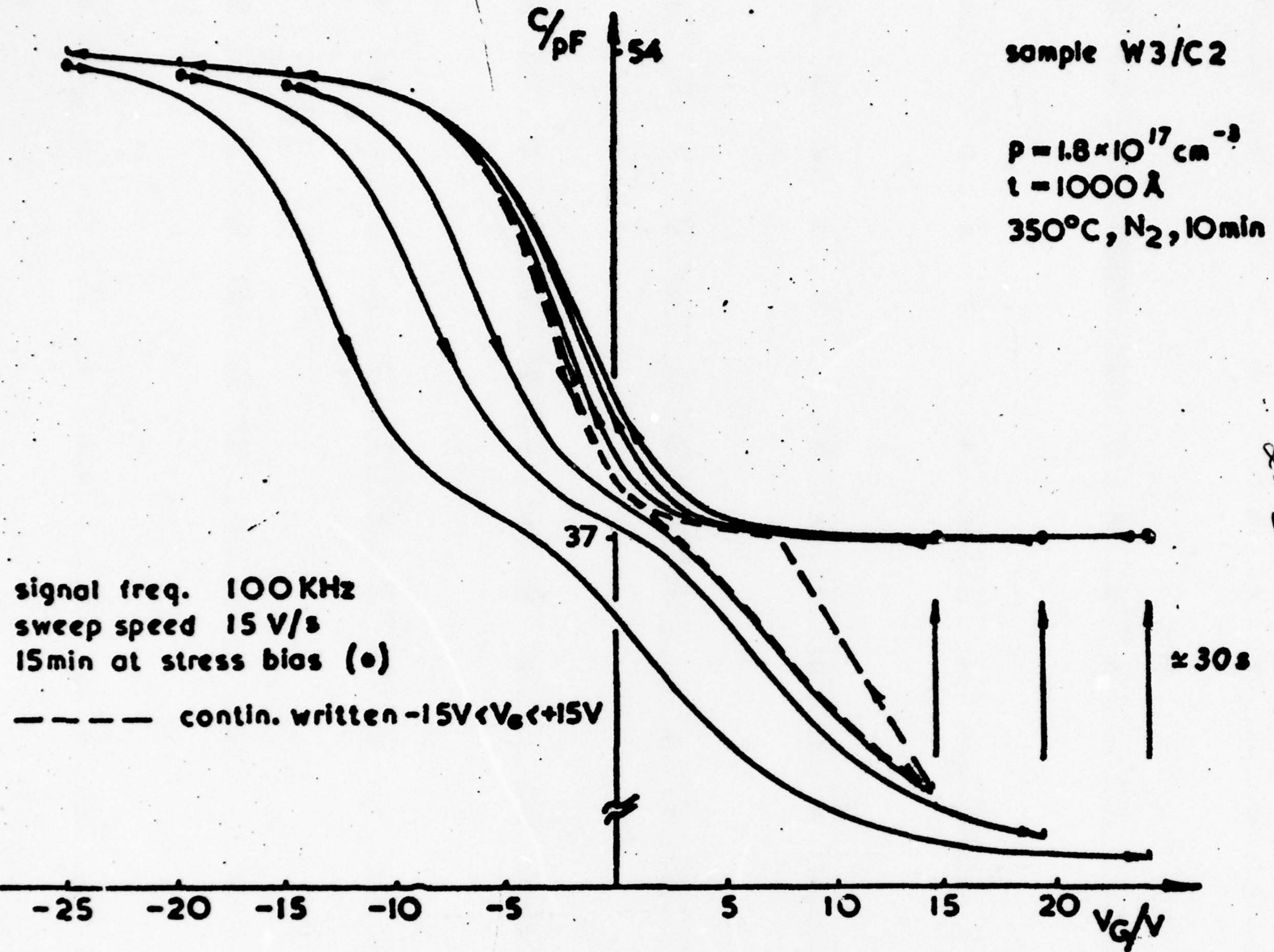
Fig. 1 - Fig. 1



Leakage Current vs. Annealing Temperature

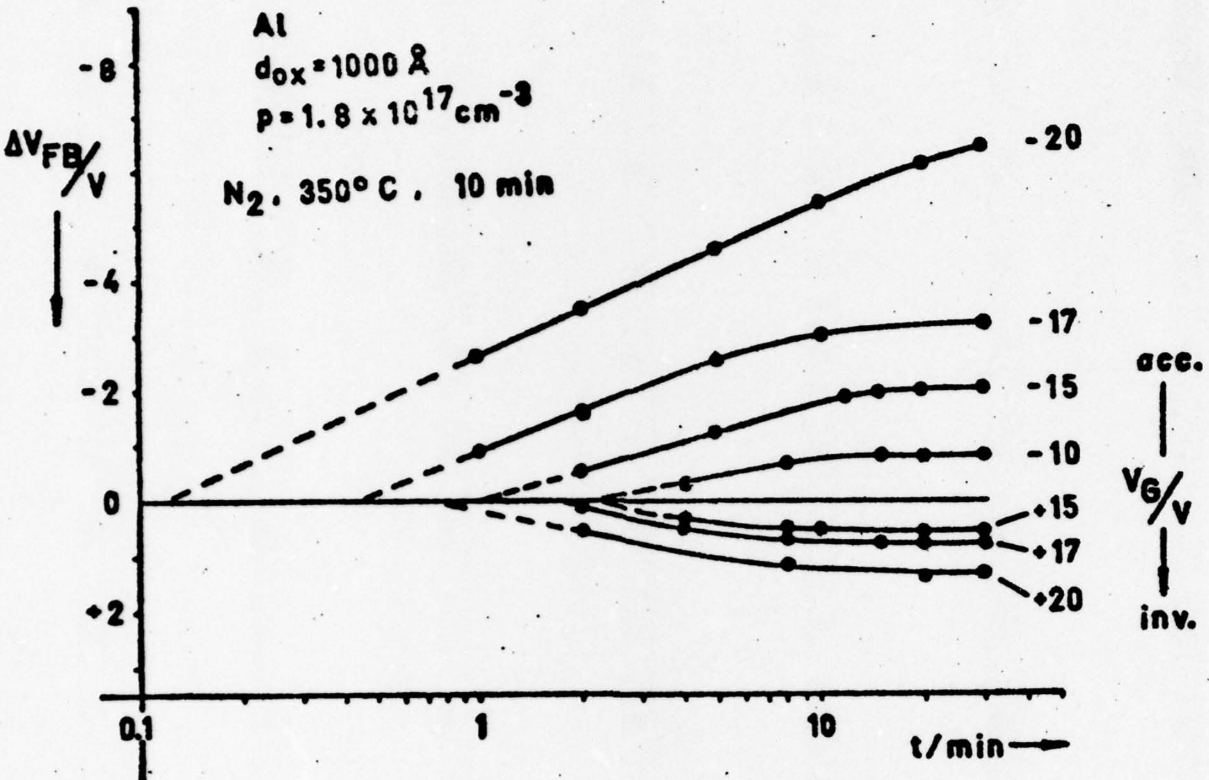
Fig. 2

22-6



CV-curve — stress bias dispersion

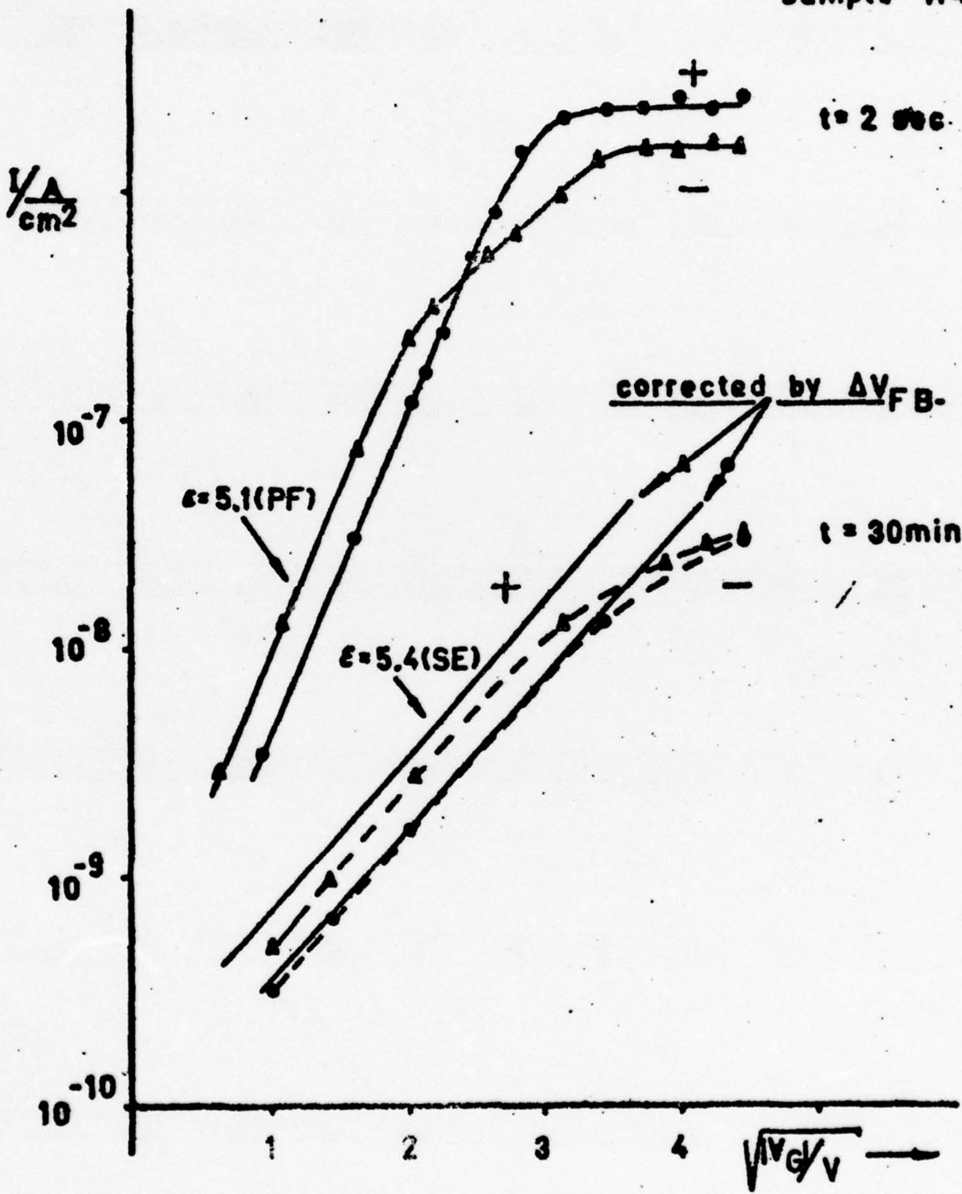
Fig 3



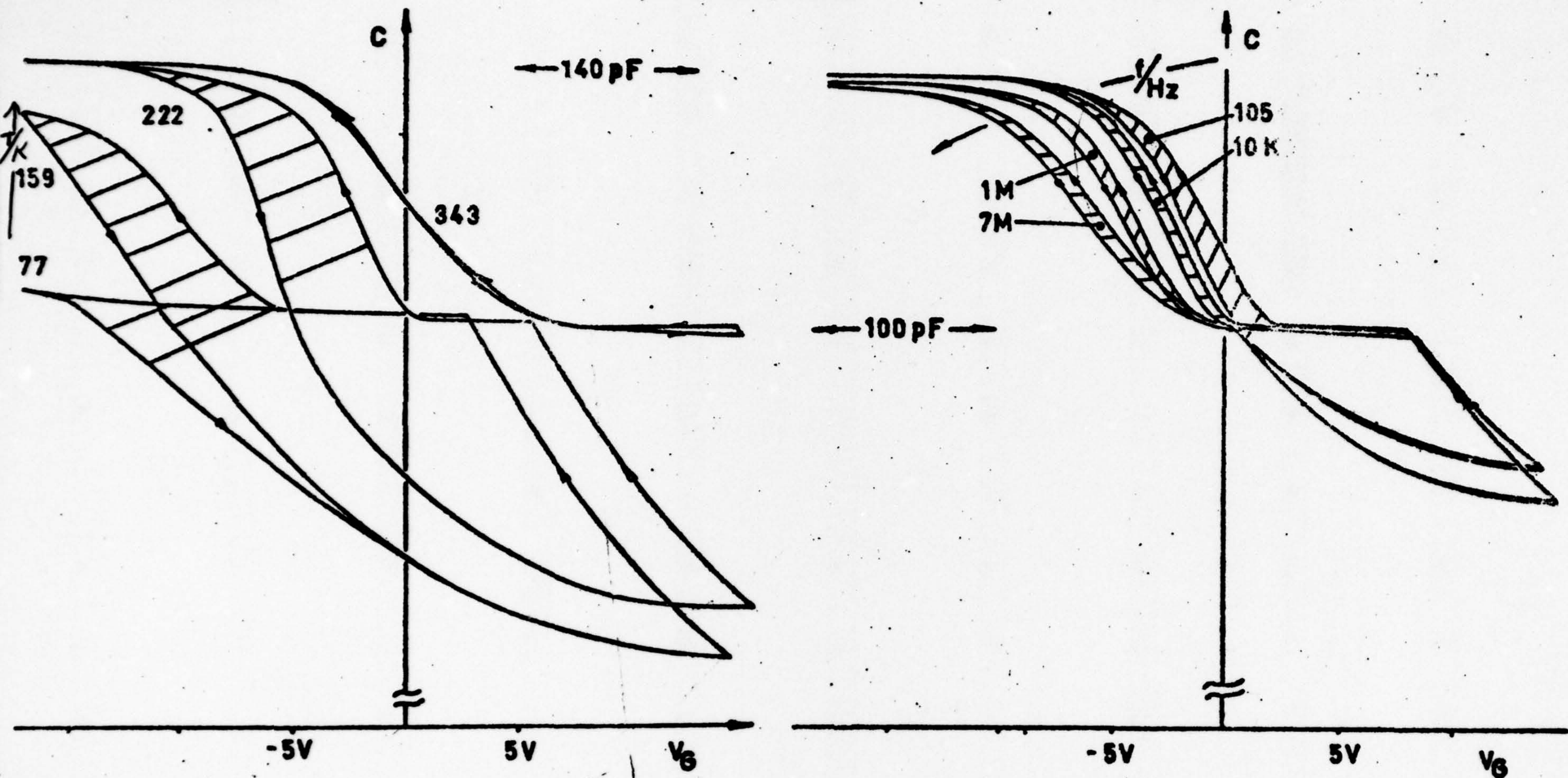
Oxide Charging Characteristics

Fig. 4

22-e



IV - Characteristics



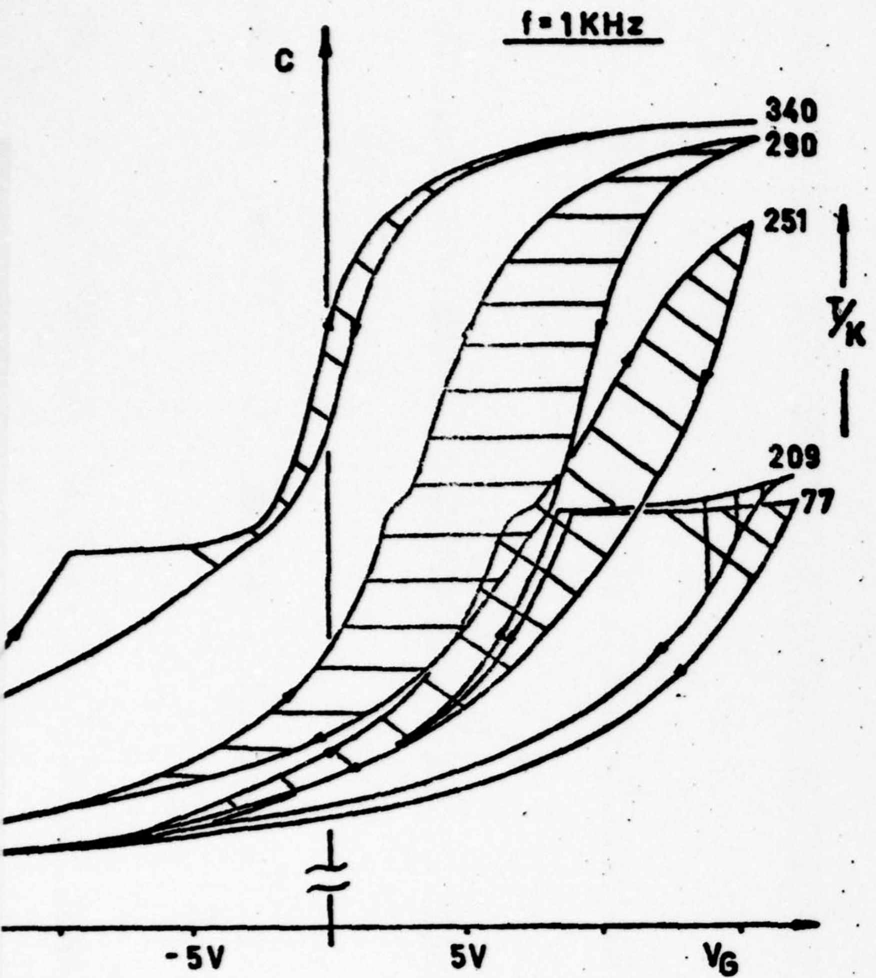
Temperature and Frequency Dispersion (p-GaAs)

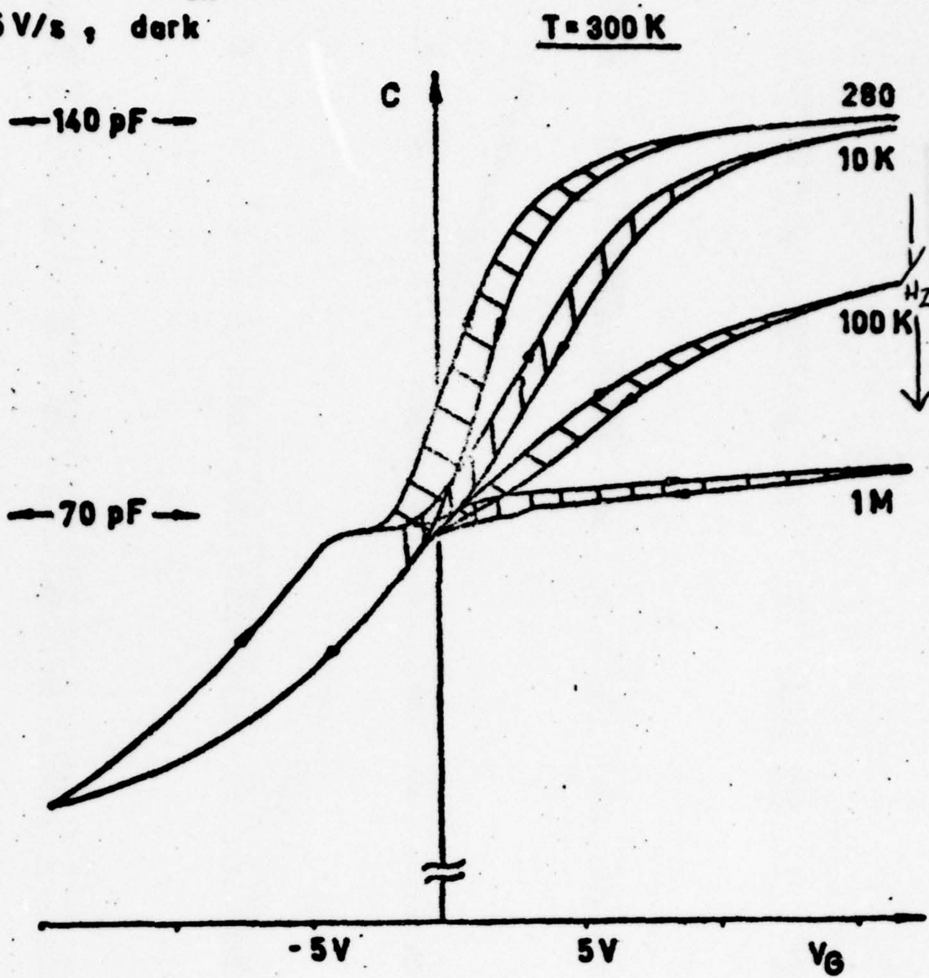
Fig. 6

sample B2

$n = 2 \times 10^{16}\ cm^{-3}$, $d_{ox} = 1000 Å$

15 V/s , dark

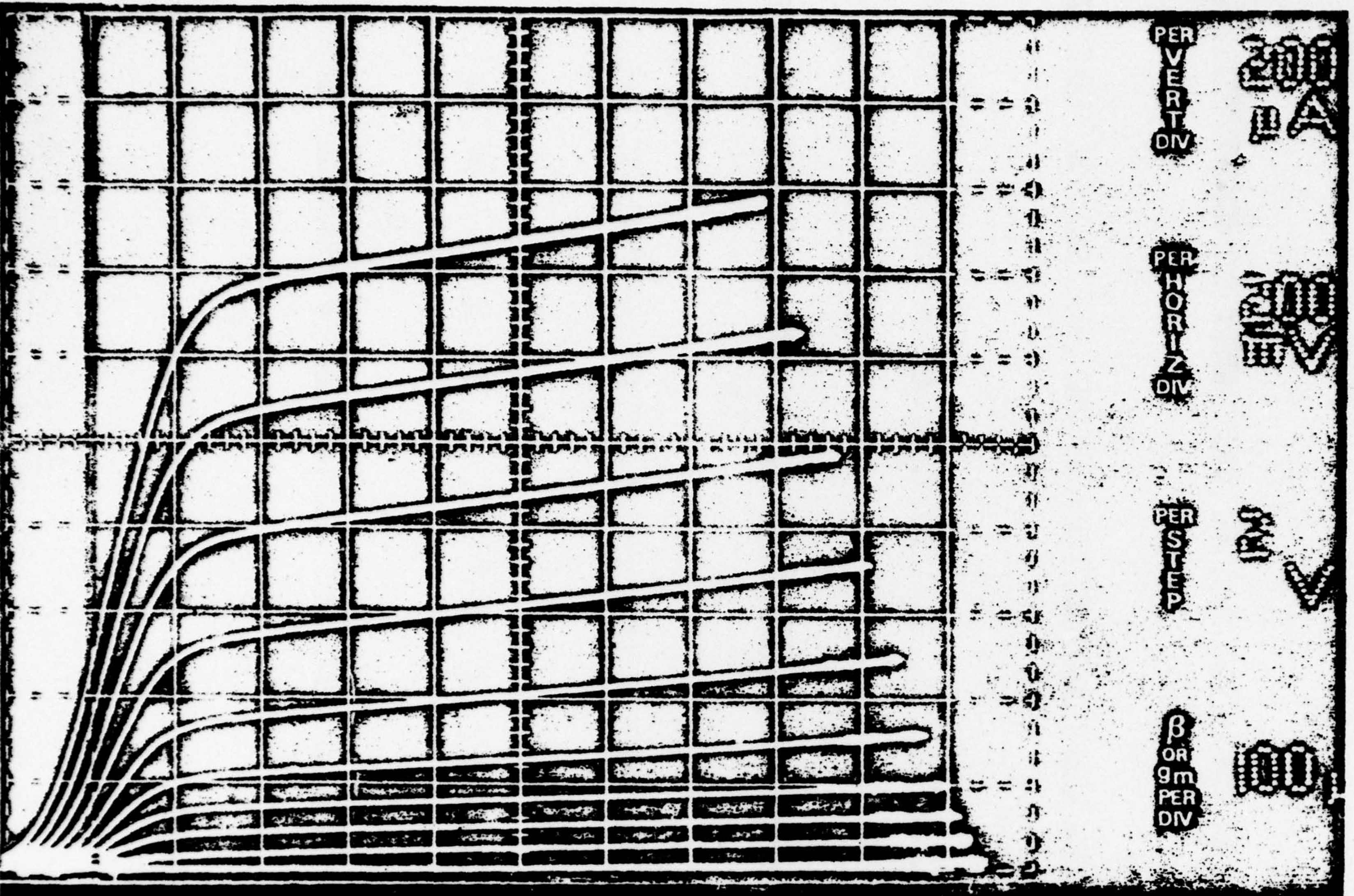




Temperature and Frequency Dispersion (n-GaAs)

22-g

Fig. 7

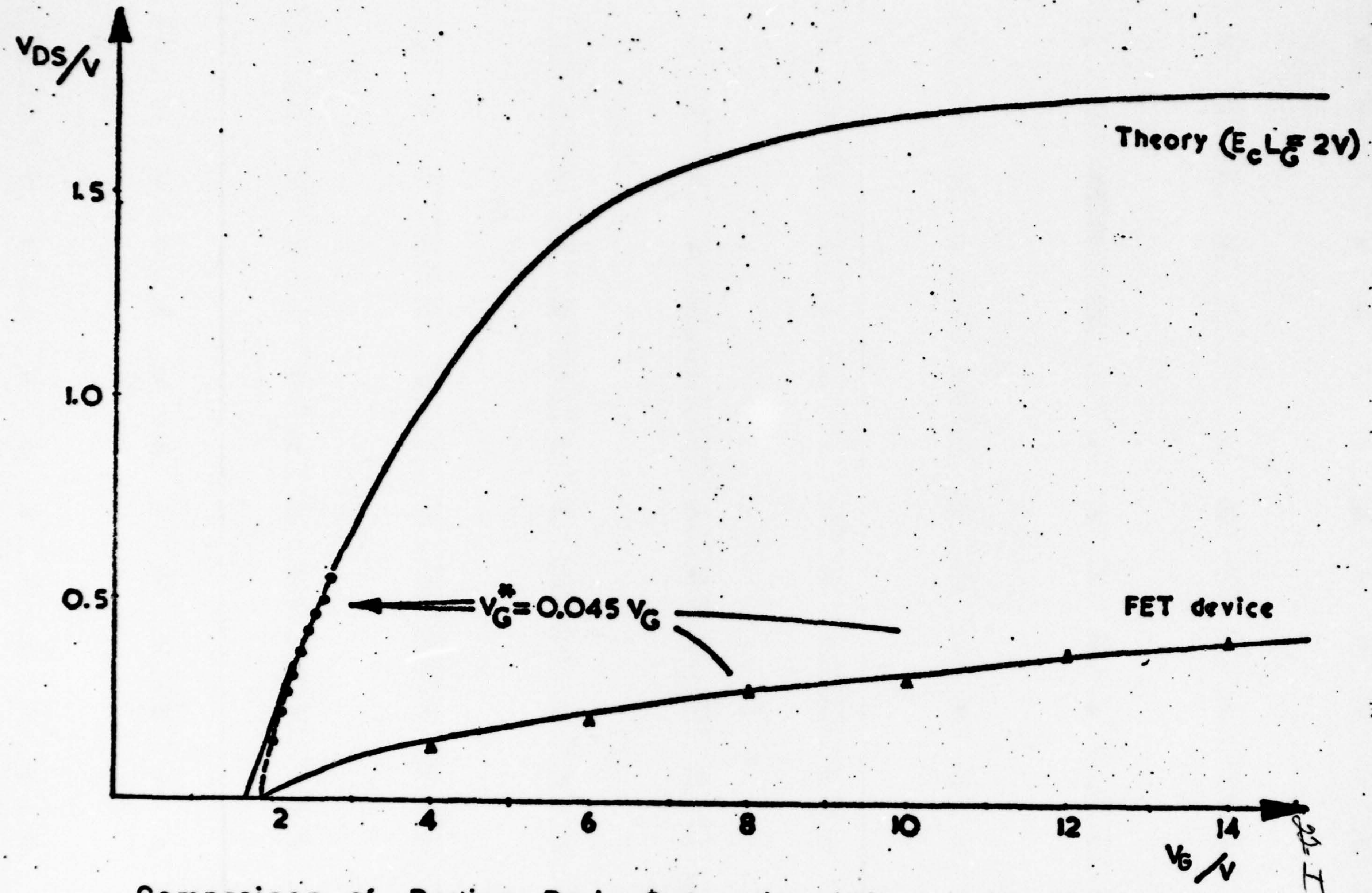


L_G = 5 um W = 200 um d_{ox} = 1000 Å p = 5×10^{16} cm^{-3}

22-h

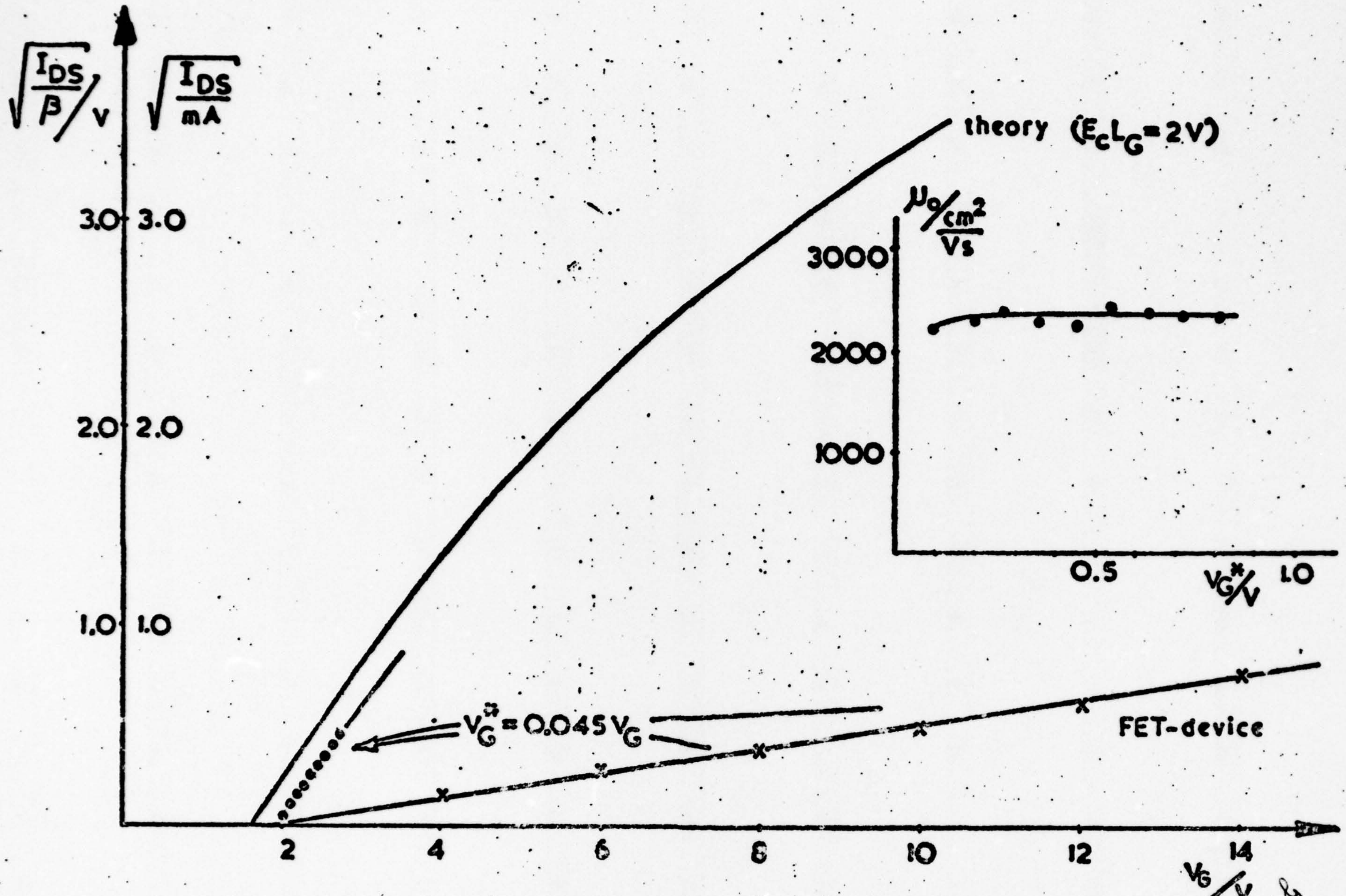
Inversion Layer MOSFET

Fig. 8



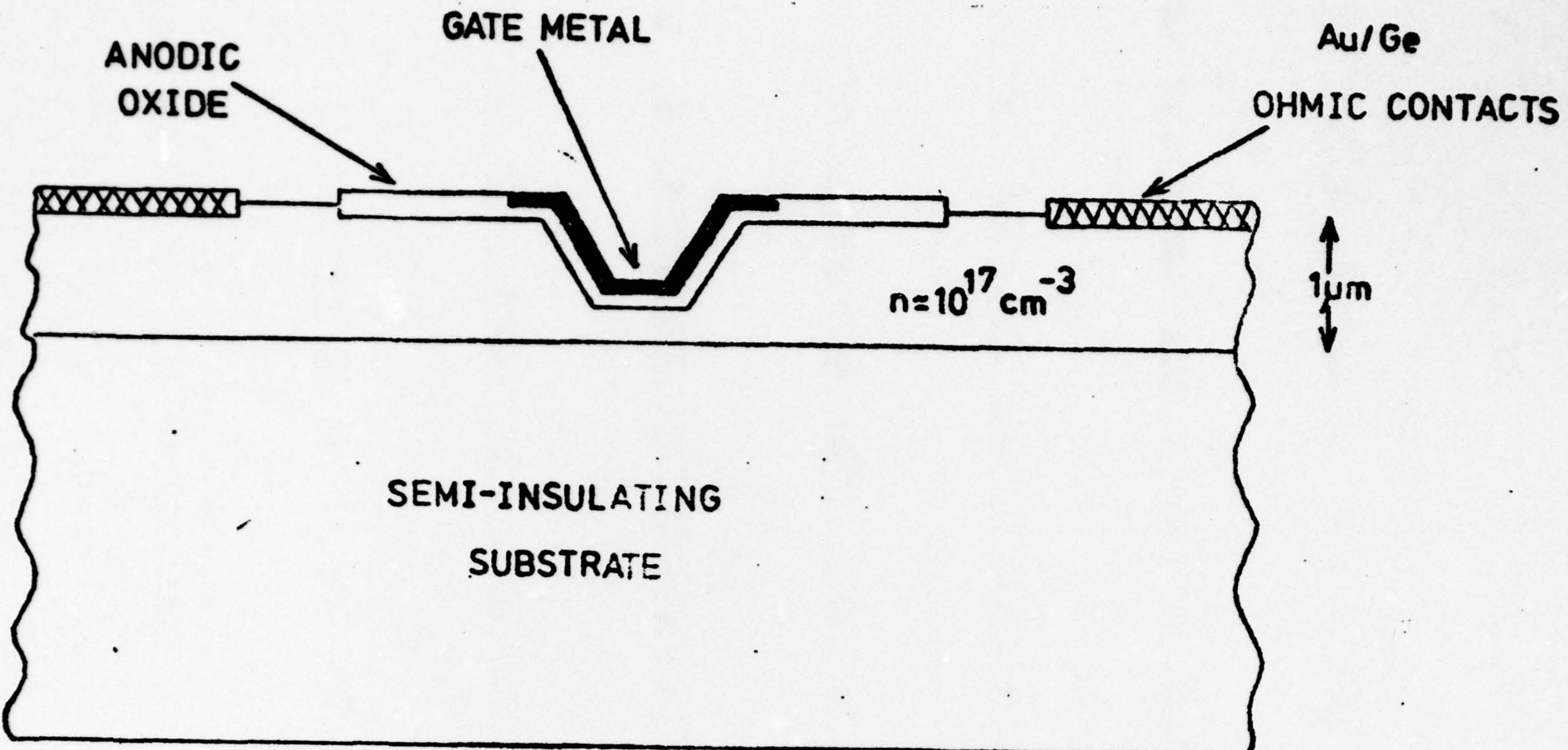
Comparison of Device Drain Saturation Voltage with Theory

Fig. 9



Comparison of Device Drain Current with Theory

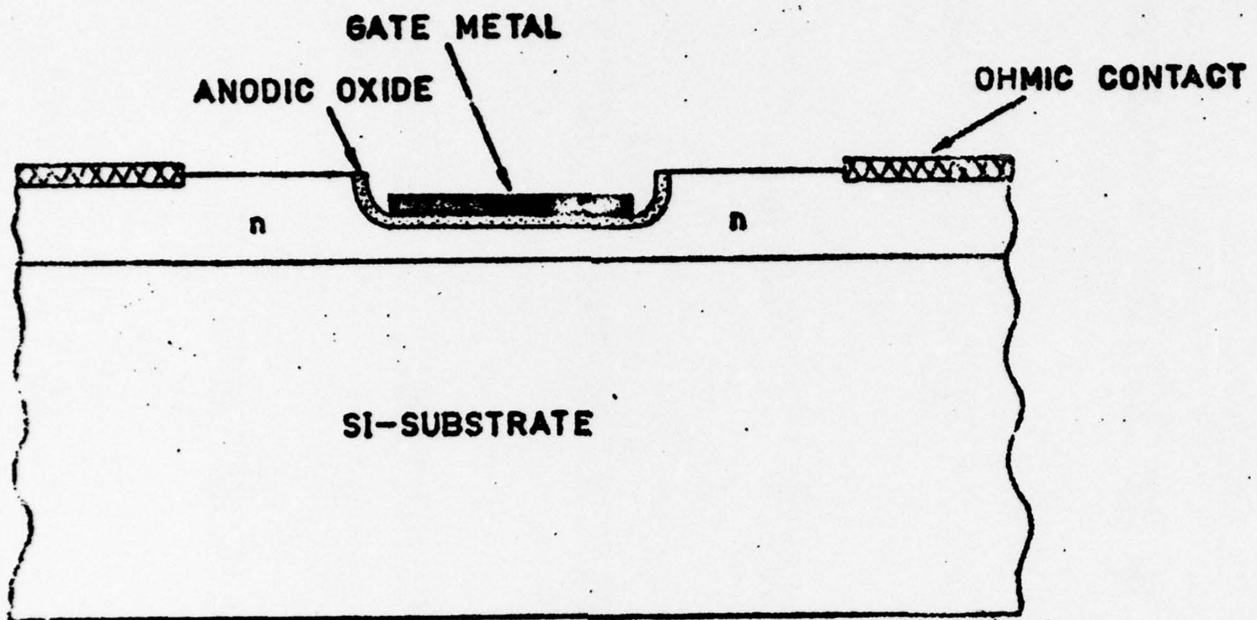
Fig 10



Cross Section of Enh./Depl. MOSFET

22-k

Fig. 11a

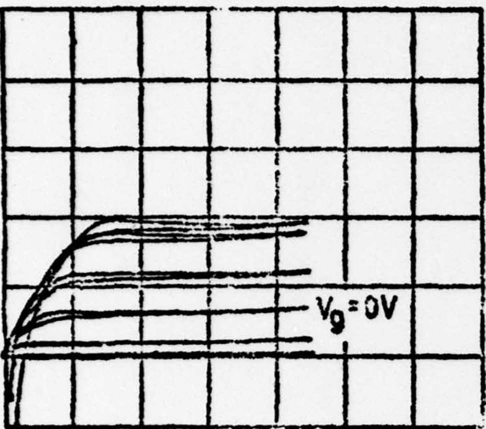


Cross Section of Selfaligned Gate Enh./Depl. MOSFET

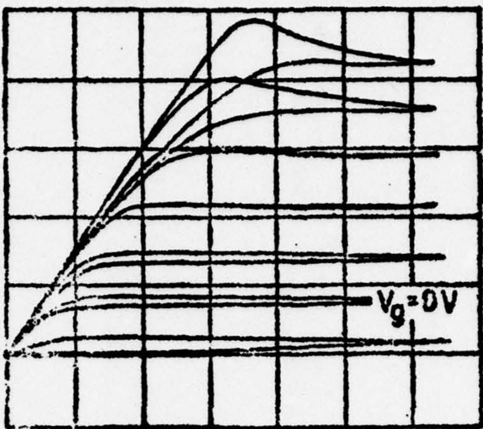
22-L

Fig. II 6

MeSFET



MOSFET



MeSFET		MOSFET
0.5 mA/div	Drain current	0.5 mA/div
2 V/div	S-D voltage	2 V/div
0.5 V/step	Gate bias	1 V/step

$L_G = 20\ \mu m$
$W = 200\ \mu m$

Comparison of MeSFET and Enh./Depl. MOSFET Caracteristics

Fig. 12

CHAPTER 4

4. ANODISATION OF InP
(A. Colquhoun)

4.1 I/V Characteristics of MOS Structures

The I/V characteristics of similar MOS structures to those used previously for C/V measurements have been measured.[1] The same electrolyte composition was used when growing the oxides.

A typical characteristic for these structures is shown in Figure 1, where the bias voltage shows the polarity which was applied to the top (aluminium dot) contact to the oxide. The current was measured with a Keithley electrometer and the voltage source was a slow ramp generator. This was used so that the capacitor charging current was minimised and did not mask the conductive element of the current.

For the example shown in Figure 1 the ramp rate was set at 4mV/sec with a sweep scan of -3V to + 3V. The curve 1 in the positive direction is the I/V for the 'virgin' oxide, and successive sweeps of bias voltage are shown in curves 2 and 3. The oxide appears to reach an equilibrium situation corresponding to curve 3.

Such a characteristic has been reported before for SiO_2[2] and for Si_3N_4[3] and was attributed to ionic polarisation. For the present case this would require an ion density $\sim 10^{20}$ charges/cm^3 in the grown oxide and it seems that ionic polarisation cannot be totally responsible for the I/V of Figure 1. A more likely explanation is that electronic conduction current through the oxide is being controlled by band bending at the oxide/InP interface. Where this band bending is caused by either the generation of positive ions or the filling of oxide traps located at some distance from the interface. This mechanism is illustrated in Figure 2 which shows the energy band diagrams at various times during one cycle of an I/V measurement. (N.B. For this diagram the effect of applied bias on the surface potential of the InP has been neglected, as this should have only a small effect on the oxide/semiconductor barrier).

4.1.2 Optimisation of electrolyte composition

From the behaviour of the anodic current during oxide growth, there appears to be a critical voltage at which the oxide breaks down at the edges. This breakdown voltage has been measured as a function of the pH of the electrolyte by first using an unbuffered

solution and subsequently adding NH_2OH. The results are shown in Figure 3 and clearly indicate that, for InP, the oxide is less susceptible to breakdown at lower pH values. The concentration of the tartaric acid solution and the ratio of glycol to aqueous solution were also optimised to produce best results with

5 parts propylene glycol
1 part 25% tartaric acid solution.

An anodisation system using a second anode of Indium metal has now been adopted, this was done for two reasons. First, to ensure that any metallic impurities in the electrolyte are drifted towards the cathode. Second, to saturate the electrolyte with In^{3+} ions by continued dissolution of the Indium anode. During anodic oxide growth the Indium anode is maintained at a small positive voltage and does not affect the oxide growth. The saturation of the solution with Indium has been found to produce more uniform oxide growth.

Substitution of phosphoric acid for tartaric acid was also found to stabilise the oxide growth although the oxide growth rate is critically dependent on the electrolyte composition. Figure 4 illustrates this. Here the oxides were grown under virtually constant current conditions with the composition of the original solution (A) being 5 parts glycol to 1 part 50% H_3PO_4 as indicated on the figure. Addition of 10 mls H_3PO_4 gave curve (B), then 10 mls H_2O gives (C), then 100 mls glycol gives (D), then 250 mls glycol gives (E), further addition of glycol gives (F).

The composition was finally optimised at

10 parts ethylene glycol)	Solution saturated
1 part 50% H_3PO_4)	with Indium.

MOS capacitor structures produced using this oxide show superior C/V characteristics but a similar low breakdown voltage.

4.1.3 Anodisation in the Dark
(A. Colquhoun)

As outlined in the previous report, the anodic current behaviour during anodisation of n-type material can be used to measure the carrier concentration of the material.[4] Some additional observations on this behaviour have now been made.

Because of the higher electric field at the edges of the exposed GaAs surface, field ionisation initially takes place at the edges and hence anodic oxide growth begins at the edges. This means

oxide growth is reduced, and this leads to a non-exponentially decaying anodic current during this initial oxide growth. Figure 5 shows the variation of anodic current with time, where the current is plotted on a logarithmic scale. For this sample $n = 2 \times 10^{16} cm^{-3}$, $V_S = 36$ V, Is = $2 mA/cm^2$. The linear portions of the graph have been extrapolated back to show up the effect of premature breakdown at the edges.

The anodic current behaviour of a p-type sample with part of the surface covered in n-type material, has now been measured in both light and dark conditions and is shown in Figure 6. For this sample $p = 2 \times 10^{16} cm^{-3}$, $n = 1 \times 10^{17} cm^{-3}$, $V_B = 30$ V, and Is = $0.5 mA/cm^2$. The dashed lines are idealised curves calculated from the areas and carrier concentrations of the two types of material, and the solid lines are the experimental results. There is good agreement between the two sets of curves.

4.2 Analysis of Multicomponent Thin Films on GaAs by Anodic Processes
(A.F. El-Safti)

As reported previously,[5] thin film epitaxy uses a suitable metallisation, including a sufficiently thick layer ofGa on GaAs together with In, Ge and Ag ohmic contact, with subsequent heating and a slow cooling cycle in an atmosphere of As_4 and H_2. The As gas diffuses into the metal film and is used, together with the Ga, which has to have a supersaturation level, to grow single-crystal GaAs onto the original GaAs. Here we describe a much simplified method to establish the GaAs regrown layer by using the recently improved anodic process[6] which has given good MOS properties on GaAs,[7] has been used for the analysis of n-type GaAs[8] and enabled the fabrication of the first native-oxide GaAs MOSFET.[9] The basic concept of this new analytical method is that many materials show a characteristic current behaviour when employed anodically under carefully controlled conditions.[6]

Initially single component films of In, Ga, Ge and Ag were deposited on n-type (100) GaAs substrates ($n = 2 \times 10^{18} cm^{-3}$) which had previously been ultrasonically cleaned in acetone, trichloroethylene and methanol, and etched in an aqueous solution of NH_4OH and H_2O_2. The metal films were evaporated onto GaAs in a conventional vacuum system with a residual pressure of 2×10^{-6} torr, the film thickness being determined from the change in frequency of oscillation of a quartz crystal mounted inside the vacuum

chamber. The thin films were anodised using an electrolyte consisting of an aqueous solution of tartaric acid and propylene glycol buffered to PH 6.3 with NH_4OH,[6] a constant cell voltage of 150 V, and initial current density of $1mA/cm^2$, in order to establish the anodisation current behaviour of each metal. It was found that the Ga exhibits a different current-decay behaviour to GaAs, while the In and Ge dissolved and the Ag anodised in an unusual manner where the initial oxide growth was not dissolved with the subsequent oxide growth being dissolved in the electrolyte.

The metallisation was then deposited onto a sample of GaAs, in order of deposition were: 200Å In, 200Å Ga, 1000Å Ge and 2000Å Ag, and the sample was cleaved into two pieces. One piece was anodised to determine the anodic current behaviour and the metallurgical structure of the unalloyed sample (Figure 7(a). The other sample was processed through the thin film epitaxy process and subsequently anodised (Figure 7(b), where the anodisation-current behaviour is different. This is first caused by a diffusion intermixing of the metals. However the onset of GaAs oxidation is given by the final steep exponential decay which occurs earlier for the post-alloyed sample, indicating the transformation of Ga into GaAs.

In conclusion, it is shown that the new electrolytic process can be useful for a relatively simple study of thin film structures.

4.3 Anodic Oxidation of Silicon
(A.F. El-Safti)

At the beginning of our work nearly all the electrolytes which are known for the production of dense oxide films on silicon were investigated to select the optimum anodising bath criteria. The following systems have received special attention:

(a) N-Methylacetamide (NMA) - KNO_3 - H_2O, used by Schmidt[10] and Duffek,[11]

(b) Ethylene glycol - KNO_3 - H_2O, used by Duffeck[12] and Barber,[13]

(c) H_3PO_4 in Amylalcohol, used by Anand.[14]

(d) Propylene glycol - Tartaric Acid - H_2O, used by Hasegawa.[15]

After a large number of experiments, it was found that the non-aqueous solutions are much better for the anodisation of silicon than the acid solutions because they allow higher forming voltages,

cause less contamination and give denser oxides. Furthermore, it was found that the use of the glycol as a solvent has the following advantages over the other nonaqueous solutions: low cost, high purity, electrolyte solubility, good stability towards heat and electrolysis and bright interference colours which allow a more accurate calibration for a thin oxide thickness. It was found that a solution consisting of (glycol - 0.04 KNO_3 - 3% H_2O) gives the best results by using a constant current density of (2 - 10 mA/cm^2), but the ionic current efficiency was only 2.65%.

In order to establish a better method of increased efficiency to produce dense oxide films on silicon by anodisation with high efficiency, the following work has been undertaken. Other experimental results, as recently reported for the anodisation of GaAs-Aℓ structures (see chapter 1 above and (16)) were adapted for Si. It is known[17] that the silicon oxide growth takes place either at the oxide-electrolyte interface when the silicon ions diffuse to the surface or at the silicon-oxide interface when the OH^- ions diffuse into the oxide. This depends on the activation energy for both silicon and OH^- ions, and also on their mobilities in the oxide. The idea was to use a thin layer of metal oxide on silicon during anodisation, to act as a buffer layer between the silicon oxide and the electrolyte, enabling silicon oxide growth underneath the metal oxide at very low current densities.

Thin layers of Aℓ (300, 500 and 1000Å) were deposited on p-type silicon substrates (1.5 - 3 Ω cm) which were previously degreased in hot trichloroethylene and rinsed in the order, acetone, de-ionised water. They were then etched in 10% HF for 3-4 min, rinsed in running de-ionised water and blown dry. The Aℓ films were evaporated onto silicon in a conventional vacuum system with a residual pressure of 2×10^{-6} torr. 99.999% grade Aℓ was thermally evaporated from tungsten coil filaments onto the unheated silicon substrates.

The whole structure was anodised by a constant current density of $20\mu A/cm^2$ in a solution consisting of tartaric acid and glycol[15] which enabled the oxidation of Aℓ with a negligible $A\ell_2O_3$ dissolution.[16] This $A\ell_2O_3$ was then to act as a buffer layer between SiO_2 and the electrolyte. During the anodisation of the three samples a break-down was observed after the forming voltage reaches (15, 25 and 50 V). When the anodised samples were examined under the

microscope small hillocks were clearly visible on the surface and showed that the surfaces could exhibit an occasional break or hole in the aluminium-oxide layer. This would mean that the silicon underneath this crack is directly exposed to the electrolyte. The hillocks are not necessarily related to any structure in the as-deposited Aℓ film because the unanodised samples, examined under the microscope, showed similar very fine structures. It would appear that during anodisation migration of Aℓ in the metal film occurs and accumulation at the surface develops. Similar hillocks were observed[18] during the plasma anodisation of Aℓ-Si structures.

This means that Aℓ cannot be used to form a buffer layer of Al_2O_3 between SiO_2 and the electrolyte. Now it is planned to undertake similar experiments by using thin layers of Ta onto Si.

4.4 Analysis of Thin-Film Epitaxy - GaAs Junctions
(H.T. Mills)

High quality ohmic contacts onto GaAs and InP have been produced by Thin Film Epitaxy.[19] [20] It is proposed to investigate the nature of the resulting grown layer by using Rutherford Scattering. The problem is that the relatively thick overlayer of Ag will 'mask' any information obtained from the regrown layer. Work is in progress on selectively removing the Ag by anodisation without destroying this underlying layer.

p-n junctions have been produced on GaAs with good I-V characteristics by using Thin Film Epitaxy. It is now proposed that the metallisation and the resulting junction be investigated using anodisation.

4.5 Study of Dissolution Rates with Anodic Oxidation of GaAs for various Electrolytes
(B. Livingstone)

It has been well established in recent years from experimentation reported in our previous European Research Office reports that the use of a mixed solution of glycol and water (AGW) as an electrolyte for the anodic oxidation of GaAs produces a very uniform amorphous oxide. An optimisation of the electrolyte used in anodic oxidation is of prime importance and experiments have been performed, using various aqueous solutions, to measure their dissolution current densities. When a constant voltage source is

connected through a limiting resistor to the anodic bath, the current density flowing through the sample decreases as the oxide is grown until a steady state situation arises in which the rate at which the oxide is produced at the semiconductor-oxide interface is equal to the rate at which the oxide is dissolved by the electrolyte at the oxide-electrolyte interface. This steady state current density is thus a direct measure of the dissolution rate of the oxide into the electrolyte and by using a Farodaic analysis a value of this rate can be obtained.

The experiments were all performed on n-type (100) 10^{18} Si doped GaAs samples using a platinum cathode and a 50 V constant voltage supply with a 100kΩ limiting resistor. The results obtained are shown in Figure 8 and as can be seen the dissolution rates of a 0.2M and 0.02M solutions of $(NH_4)H_2PO_4$ are comparable and even less than that of the AGW electrolyte.[21]

Further work is to be carried out in conjuction with the quality of the oxide produced by the aqueous electrolyte and the growth under constant current operation.

4.6 Oxide-Structural Studies
(B. Weiss)

4.6.1 Naturally occurring oxide layers on GaAs

Surface oxide layers of about 20Å thickness are present on all GaAs surfaces and are formed by a reaction with the surrounding atmosphere. They are very important since they may affect the surface properties of the material including work function, barrier height an- surface recombination velocity. Surfaces of the above type are known "real" surfaces.

A study was made of the surface structure of "real" GaAs surfaces after polishing, cleaning in the common organic solvents (acetone, trichloroethylene and methanol) and etching in a 10% solution of hydrochloric acid.. Using reflection high energy electron diffraction (RHEED) the results show that the relative thickness of this surface film varies for each solvent with methanol producing the thickest film followed by acetone and trichloroethylene, where both of the latter films have the same thickness.[22] Etching in HCℓ however did not completely remove any of the oxide films. Also demonstrated was the catastrophic effect of unpurified water on GaAs; it produced a good polycrystalline gallium oxide on the sample

surface.

4.6.2 Anodic Oxides

The initial part of this investigation was concerned with the properties of the as-grown oxide samples which was followed by a study of the effects of annealing on the structure and properties of the anodic oxides.

The techniques which were used here to analyse the samples were reflection high energy electron diffraction (RHEED) and X-ray diffraction to study the surface and the bulk of the oxide respectively, the SEM and microprobe analyser to study the surface topography and chemical composition of the sample respectively and etching in HCℓ to determine the resistance to acids.

As-grown anodic oxide layers

A comparison of the results of the X-ray and electron diffraction experiments for the unannealed samples show that the most pronounced crystallisation occurred at the oxide/GaAs interface and that the anodic oxide crystallised out, under certain circumstances, as (100) orientated $\beta\text{-}Ga_2O_3$.

A series of samples were grown using current densities of 2.0, 1.0 and 0.1 $mAcm^{-2}$. Those grown with a current density of 2.0 $mAcm^{-2}$ were found to contain some crystalline $\beta\text{-}Ga_2O_3$ at the interface while the remaining samples were seen to be amorphous.[23] The chemical analysis of these samples showed that the As content of the oxide was an inverse function of the growth current density (i.e. those grown with a low current density contain more As than those grown with a high current density). Chemical solubility tests showed that all of those oxides were soluble in HCℓ and the surface of the oxide and the surfaces left after the etching were found to be flat, as seen with at a magnification of 10,000 x.

Annealed anodic oxide layers

Some of the samples were grown as above and annealed in a high purity nitrogen atmosphere for 10 mins in a quartz furnace tube whose temperature was controlled electronically, since hydrogen reduced the oxide at 600°C to metallic Ga. Additionally, the samples grown with a current density of 0.1 $mAcm^{-2}$ were cooled quickly (100°C per min) as well as at the normal slow rate of 300°C per hour.

After annealing to sufficiently high temperatures (above

about 400°C) all the samples, with the exception of those cooled quickly, were found to have polycrystalline β-Ga_2O_3 present at the oxide/GaAs interface and its volume and crystallite size increased with annealing temperature.[23] The threshold annealing temperature for the onset of interfacial crystallisation was found to be an inverse function of the growth current density used. The samples cooled quickly were found to be completely amorphous. Some surface crystallisation was found in the samples annealed at higher temperatures but the crystallite size here was small so that it was of minor importance when compared with the interfacial crystallisation. The chemical analysis proved to be somewhat complex especially in view of the limitations imposed by the methods, so that higher resolution techniques are required to obtain the relevant information. A preliminary study, using Auger depth profiling, has shown to be extremely useful in determining the chemical structure of the oxide. However, there seems to be some correlation between the As loss during annealing and the decrease in the oxide resistivity and general degradation of the electrical characteristics above 350°C. This also suggests that the interfacial layer of β-Ga_2O_3 has a marked effect. Resistance to chemical attack was also found in the higher temperature annealed samples, again suggesting the presence of β-Ga_2O_3. The surfaces of these samples were also found to be flat, certainly up to a magnification of 10,000.

The above results show that the growth current density and the cooling rate after annealing are the two most important factors determining the occurrence of crystallisation. The chemical composition of the layers is of a complex form and can only be suitably determined using more sophisticated methods such as Auger depth profiling. However, the production of β-Ga_2O_3 at the oxide/GaAs interface and the loss of the As component of the oxide are seen to be important factors which influence the electrical characteristics. A more detailed knowledge of the growth mechanism and a more detailed chemical analysis would enable a better attempt to optimise the processing steps and the characteristics of the oxide layers to produce suitable MOS structures, especially for MOSFETs, although the present structures have been used for the fabrication of successful GaAs MOSFETs

Since anodisation allows a controlled amount of GaAs to be removed this was found to be of use in the preparation of thin GaAs samples for TEM studies. An advantage of this method is that it does not damage the material which is to be studied in the TEM. Experimental details have been published.[24]

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Fig. I/V Characteristics of InP Native Oxide

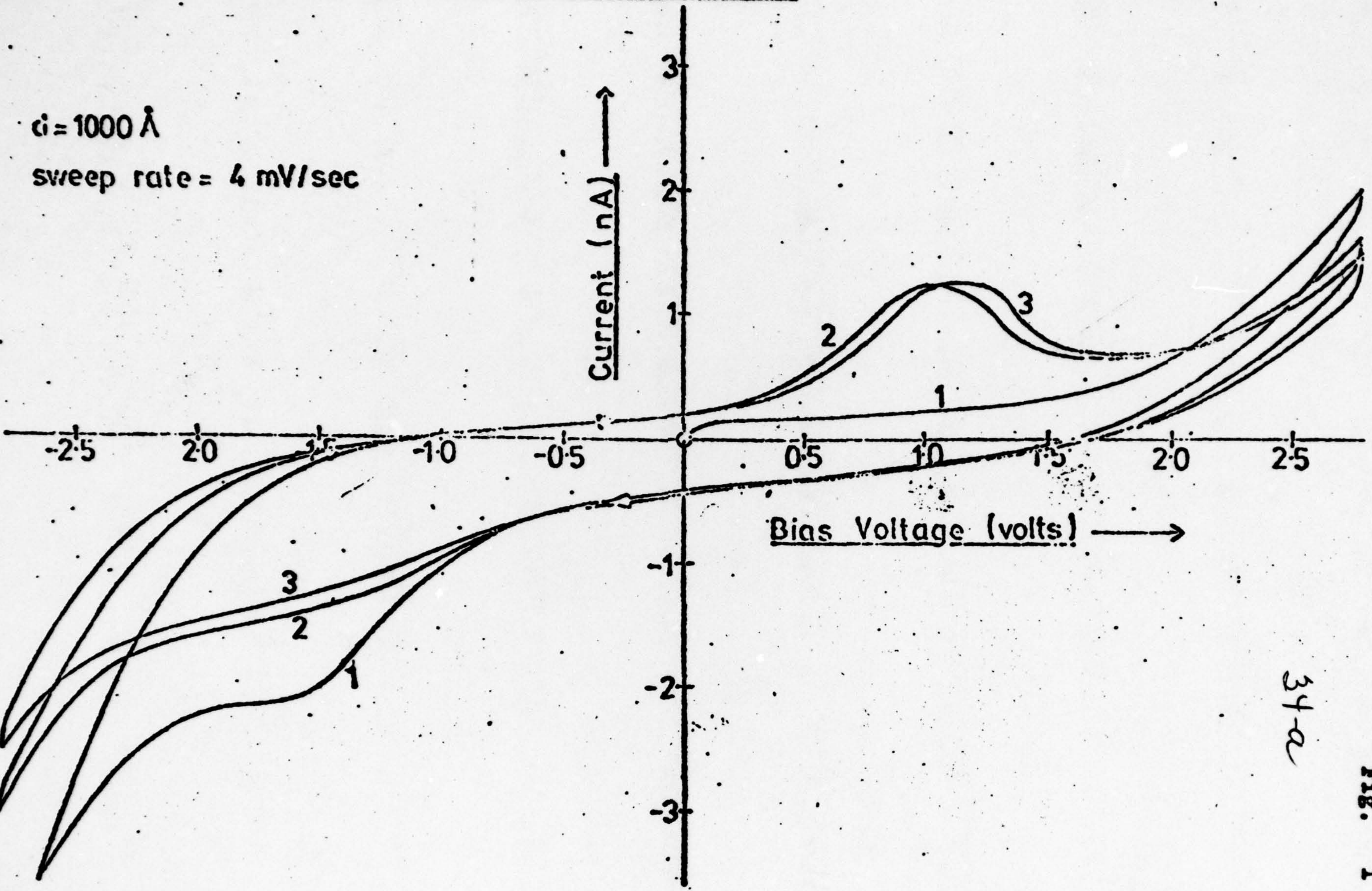


Fig. 1

Fig 2

Fig 2 Band Diagrams for InP MOS Structure

34-b

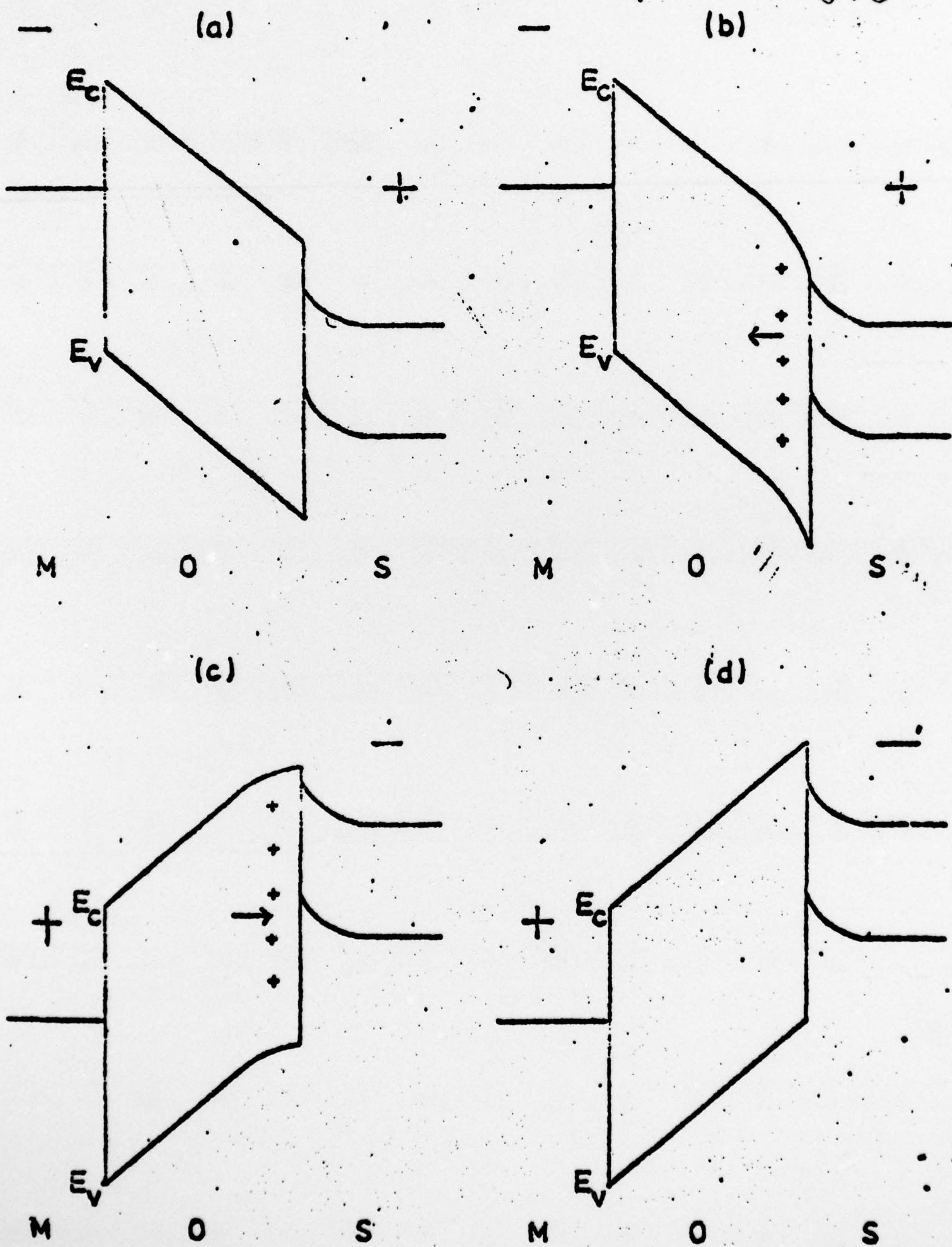
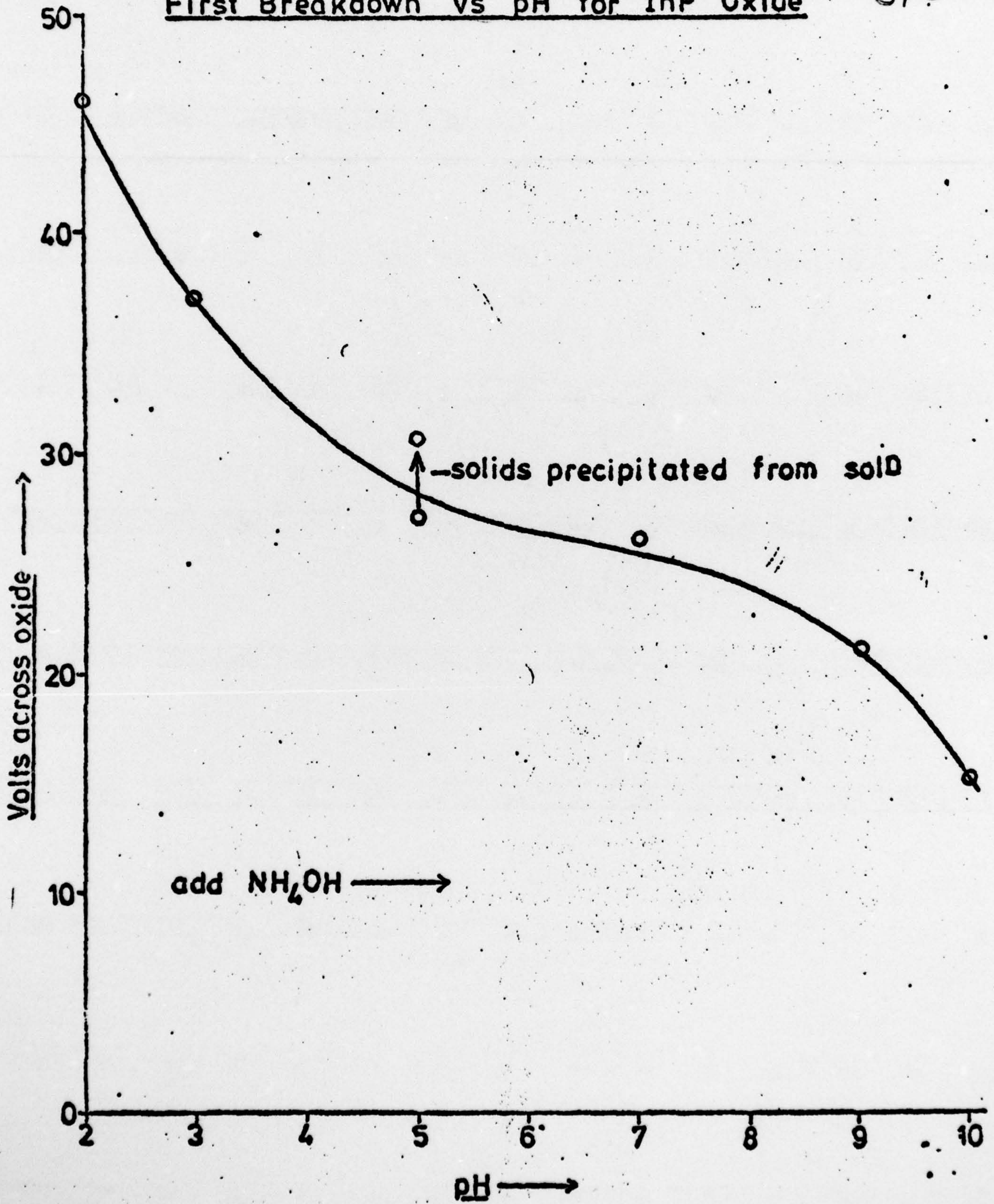


Fig 3



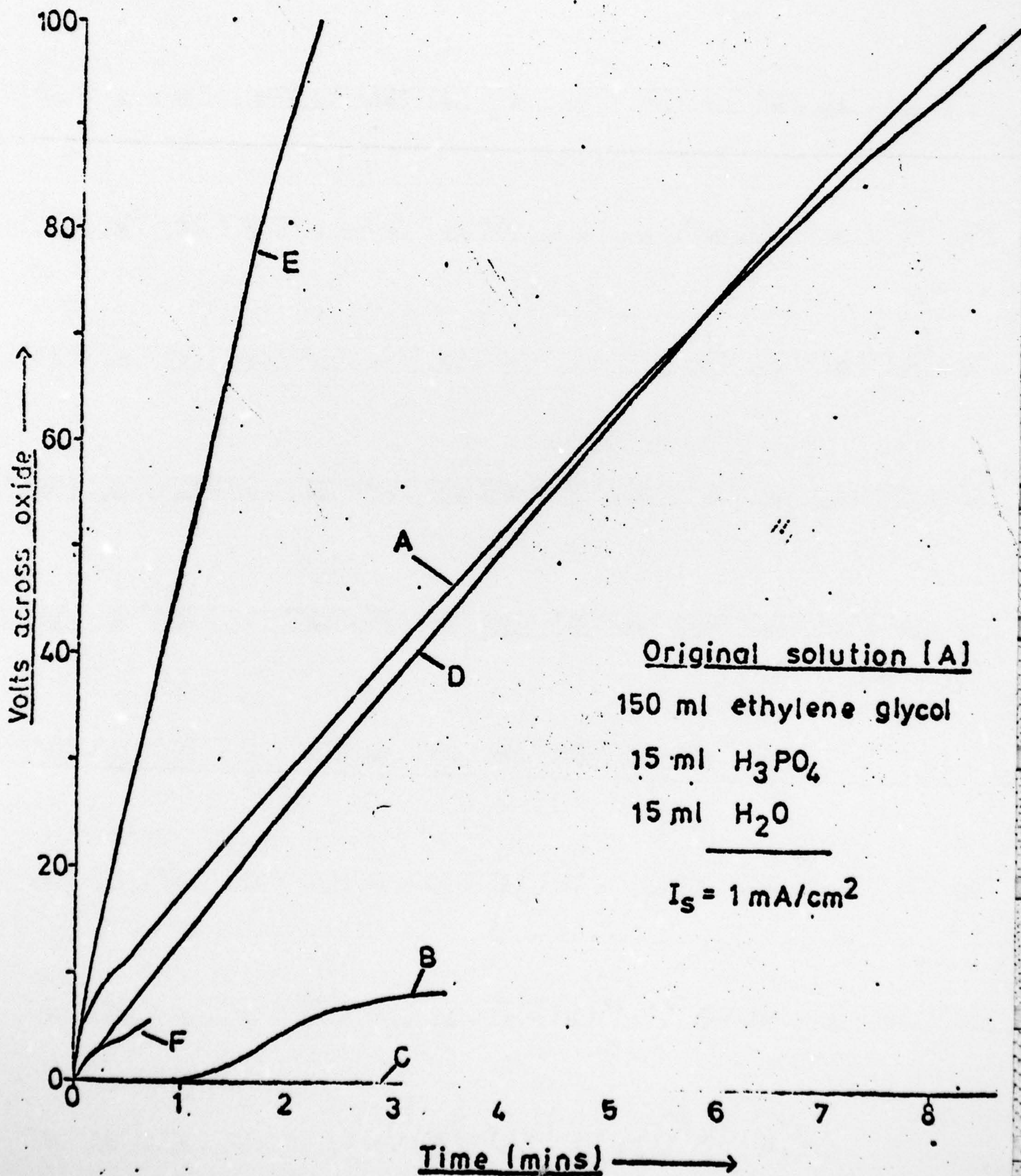
[100 ml propylene glycol

Fig 4

Oxide build-up for various electrolyte compositions

Fig 4

34-d



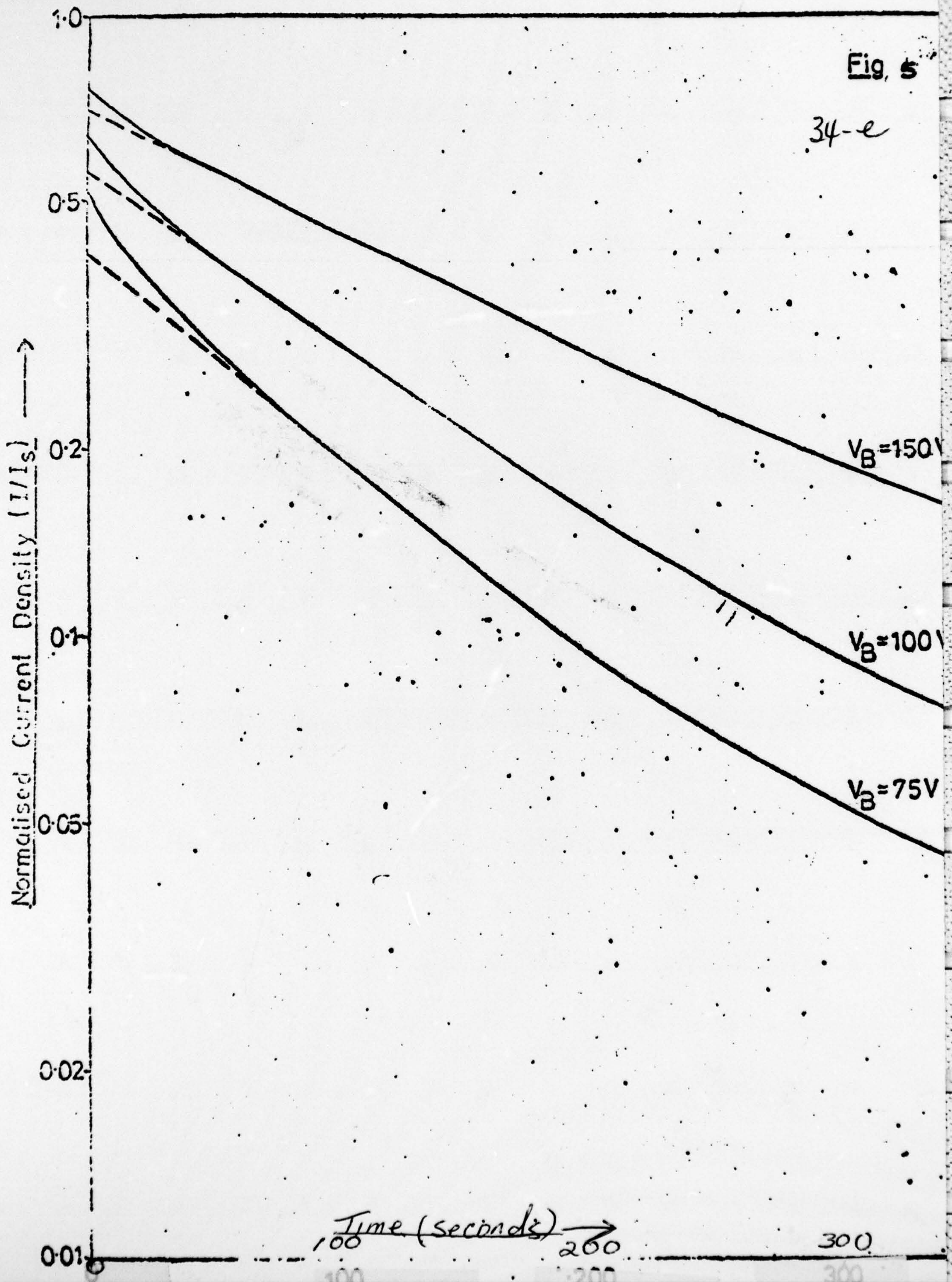


Fig. 5
34-e
1.0
0.5
0.2
0.1
0.05
0.02
0.01
Normalised Current Density (I/Is) →
V_B=150V
V_B=100V
V_B=75V
0
100
200
300
Time (seconds) →

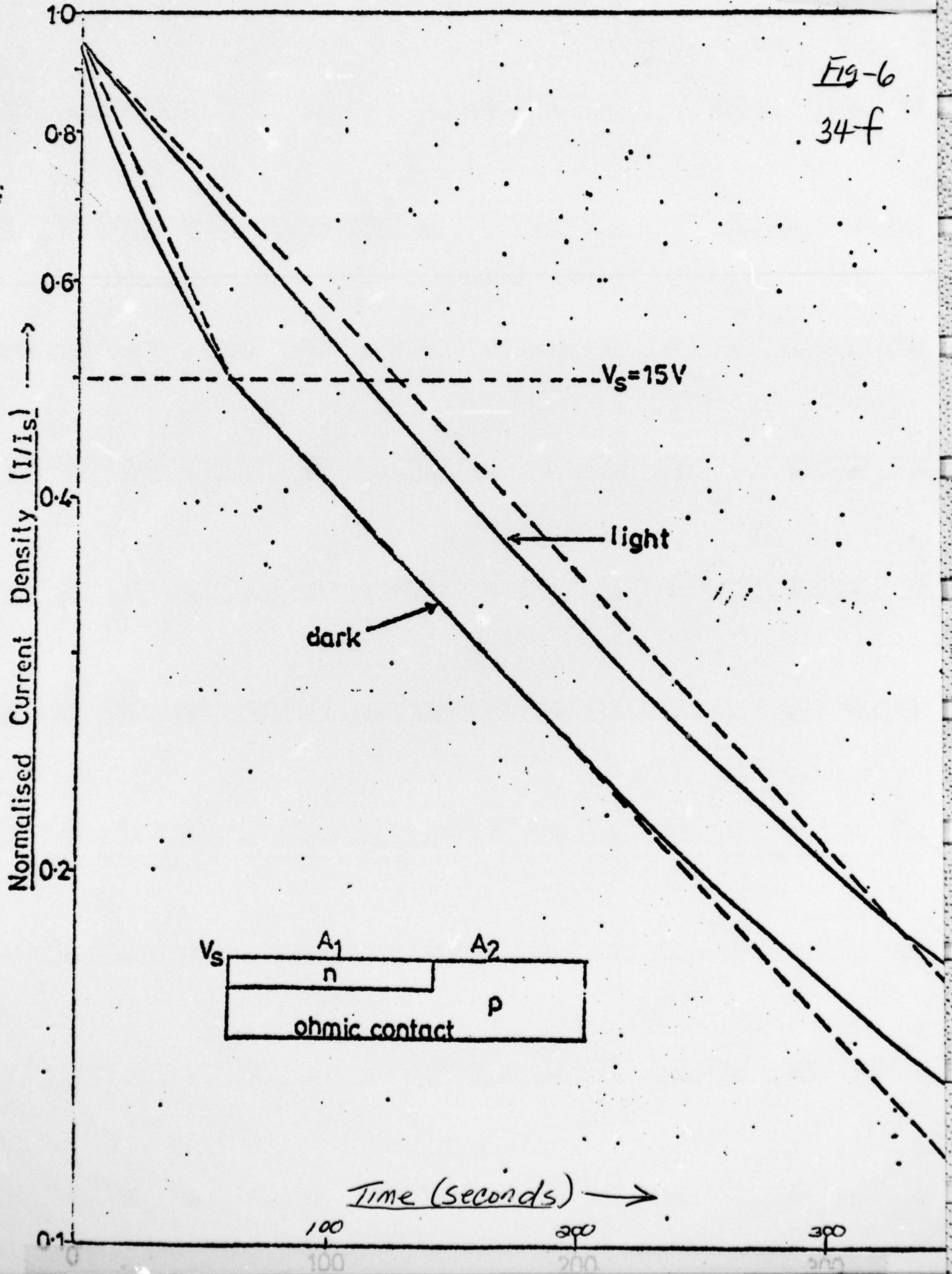
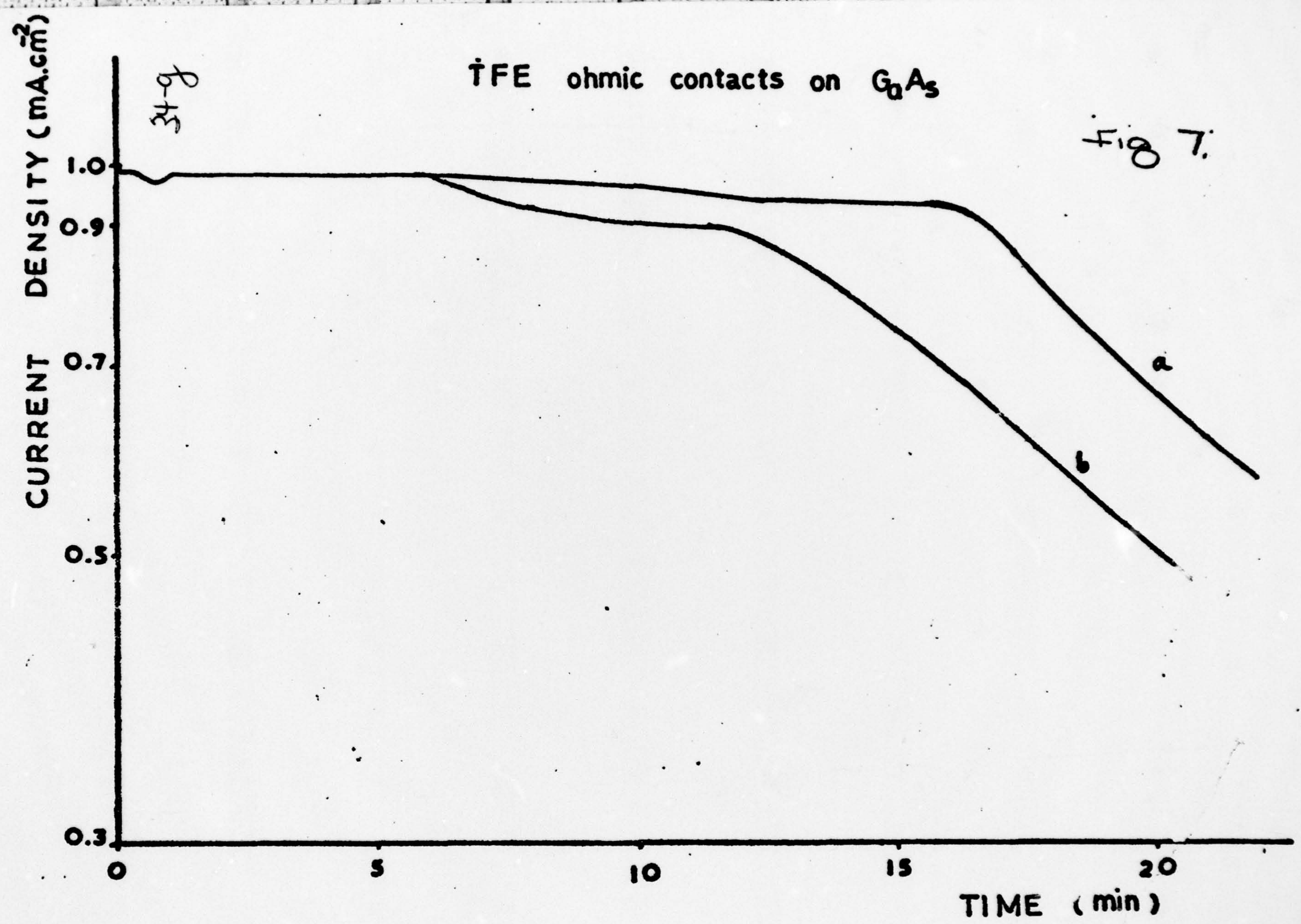


Fig 6
Fig-6
34-f
1·0
0·8
0·6
0·4
0·2
0·1
Normalised Current Density (I/Is) ⟶
Vs=15V
light
dark
Vs
A1
A2
n
p
ohmic contact
Time (seconds) ⟶
100
200
300



TFE ohmic contacts on GaAs
Fig 7.
34-g
CURRENT DENSITY (mA.cm-2)
1.0
0.9
0.7
0.5
0.3
0
5
10
15
20
TIME (min)
a
b

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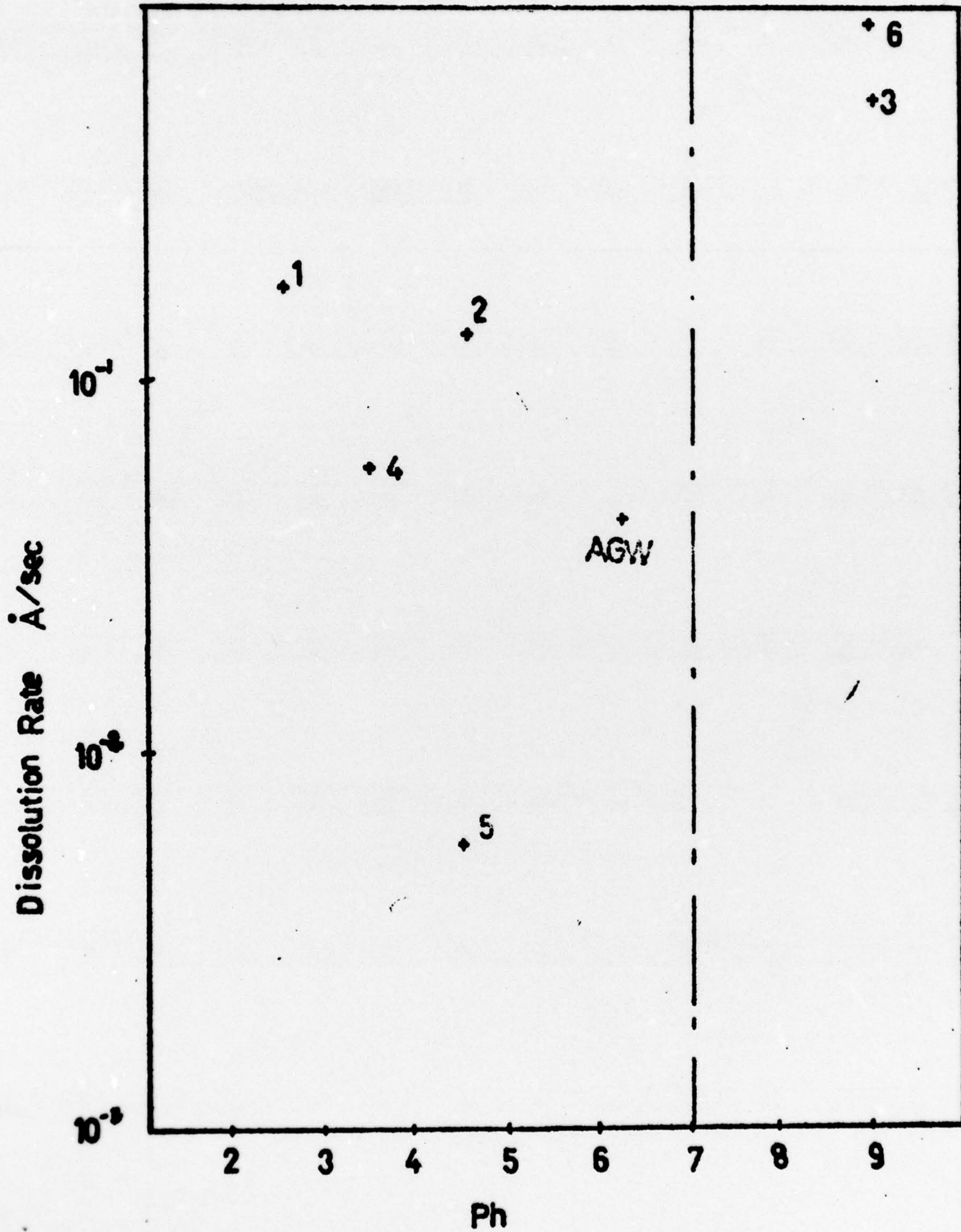
Fig 8

34-h



1- 0·003M H_3PO_4
2- 0·3M NaH_2PO_4
3- 0·1M Na_2HPO_4
4- 0·2M $(NH_4)H_2PO_4$
5- 0·02M $(NH_4)H_2PO_4$
6- 0·1M $(NH_4)_2HPO_4$

samples grown with a current density of 0.1 mAcm^{-2} were cooled quickly (100°C per min) as well as at the normal slow rate of 300°C per hour.

After annealing to sufficiently high temperatures (above

END

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DTIC