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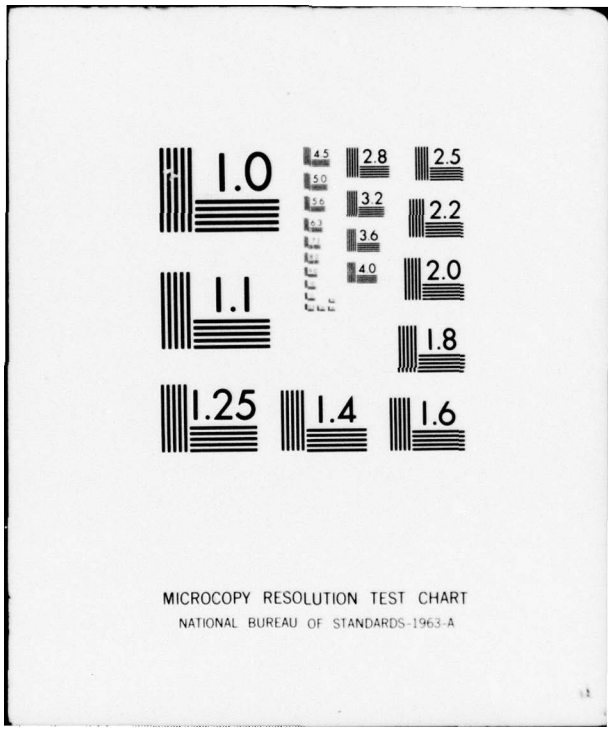
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Research and Development Technical Report

ECOM-77-2641-1

HIGH VOLTAGE NANOSECOND PULSE GENERATORS

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June 1977

First Triannual Report for Period 30 Dec 76 to 30 Apr 77

Prepared for:

ECOM

US ARMY ELECTRONICS COMMAND FORT MONMOUTH, NEW JERSEY 07703

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This First Triannual Report describes work performed during the period 1 Jan 77 to 30 Apr 77 to develop three high voltage nanosecond pulse generators. The objective of the development is a set of pulse generators of small volume, low weight, and high efficiency. The design for Task A Pulse Generator, operating either single pulse or 15 Hz, at a pulsewidth of 125 ns, pulse voltage of 30 kV, and pulse current of 1200 amps, has been completed. Switches to meet the lower voltage, higher speed requirements of pulse generators for Tasks B and C will be evaluated in test circuits.

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I. INTRODUCTION

This report covers work done during the period 1 January 1977 to 30 April 1977 on Contract DAAB07-77-C-2641 to develop a set of high voltage nanosecond pulse generators. The work is being performed by Cober Electronics in Stamford, Connecticut for the U.S. Army Electronics Command, Ft. Monmouth, New Jersey. The work is directed toward fulfilling the requirements of Technical Guidelines entitled "High Voltage Nanosecond Pulse Generators" dated 27 July 1976. Listed below are the requirements for Task A, Task B, and Task C.

Task A

a.	Output Voltage	30KV
b.	Peak Current	1200A
c.	Prr	15Hz and single pulse
d.	Pulse Width (50%)	125ns
e.	Rise Time (10% to 90%)	20ns max.
f.	Fall Time (90% to 10%)	40ns max.
g.	Pulse Energy Output	4.5 joules
h.	Pulser Efficiency	90% min. (resistive load)
i.	Life	10^6 pulses min.
j.	Weight	2.0kg max.

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k.	Volume	360cm^3 max.
l.	Form Factor	Cylindrical
m.	Maximum Outer Diameter	6.5cm

Task B

a.	Output Voltage	5KV
b.	Peak Current	4A
c.	Prr	10,000Hz
d.	Pulse Width (90%)	100ns
e.	Rise Time (10% to 90%)	10ns max.
f.	Fall Time (90% to 10%)	20ns max.
g.	Pulser Efficiency	90% min. (resistive load)
h.	Pulse Energy Output	0.0023 joules
i.	Life	1000 hrs. min.
j.	Weight	2.0kg
k.	Volume	360cm^3 max.

Task C

a.	Output Voltage	1KV
b.	Peak Current	1) 15A to charge up C_L = 30pF in 2 nsec 2) 20mA during flat top portion of pulse
c.	Prr	15,000Hz
d.	Pulse Width (50%)	20ns
e.	Rise Time (10% to 90%)	2ns max.
f.	Fall Time (90% to 10%)	4ns max.
g.	Pulser Efficiency	90% min.

h.	Life	1000 hrs. min.
i.	Weight	2.0kg max.
j.	Volume	360cm^3 max.

II. TASK A APPROACH

The initial design of the pulse generator for Task A has been completed and all parts have been ordered. Presented in Figure 1 and 2 are schematic diagrams for the power supply and modulator for the pulse generator of Task A. In the initial design, emphasis was placed on the size of the unit. In order to approach the volume requirements for Task A, the 30KV, 1200A pulse will be formed by discharging a Blumlein circuit. A ringing-choke dc-to-dc converter charges the Blumlein circuit capacitors to 30KV by transforming the 28 volt input. To minimize breakdown between closely spaced high voltage points, the pulse generator will be encapsulated in a clear RTV silicone rubber having a dielectric strength of 500 volts/mil.

A conventional pulse forming network (PFN) requires the network capacitors to be charged to 60KV in order to form a 30KV pulse. The 30KV voltage required to charge the Blumlein network capacitors results in less volume in the following areas:

1) converter high voltage transformer
2) network capacitors
3) triggered spark gap with associated circuitry.

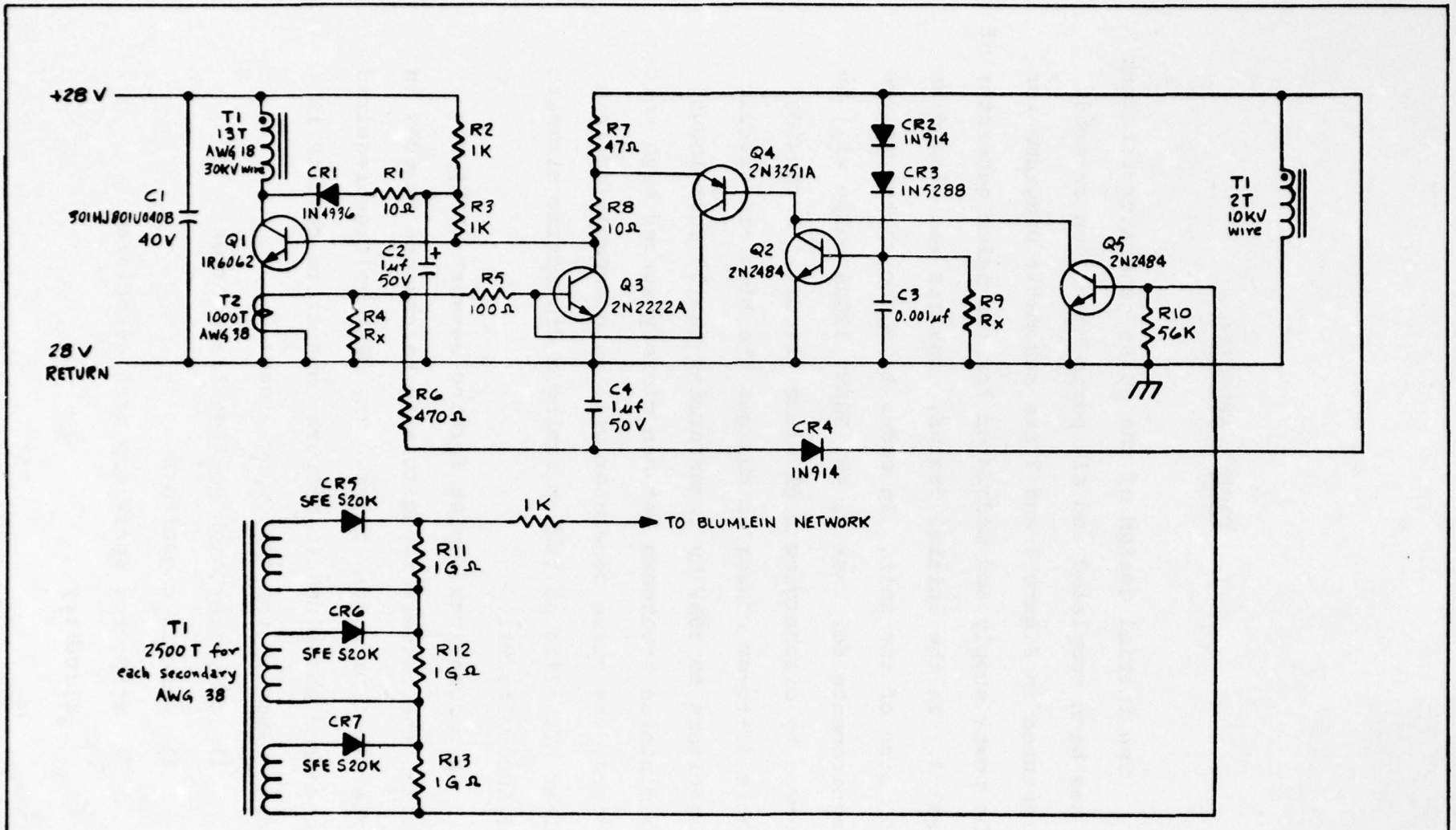

FIGURE 1
TASK A POWER SUPPLY

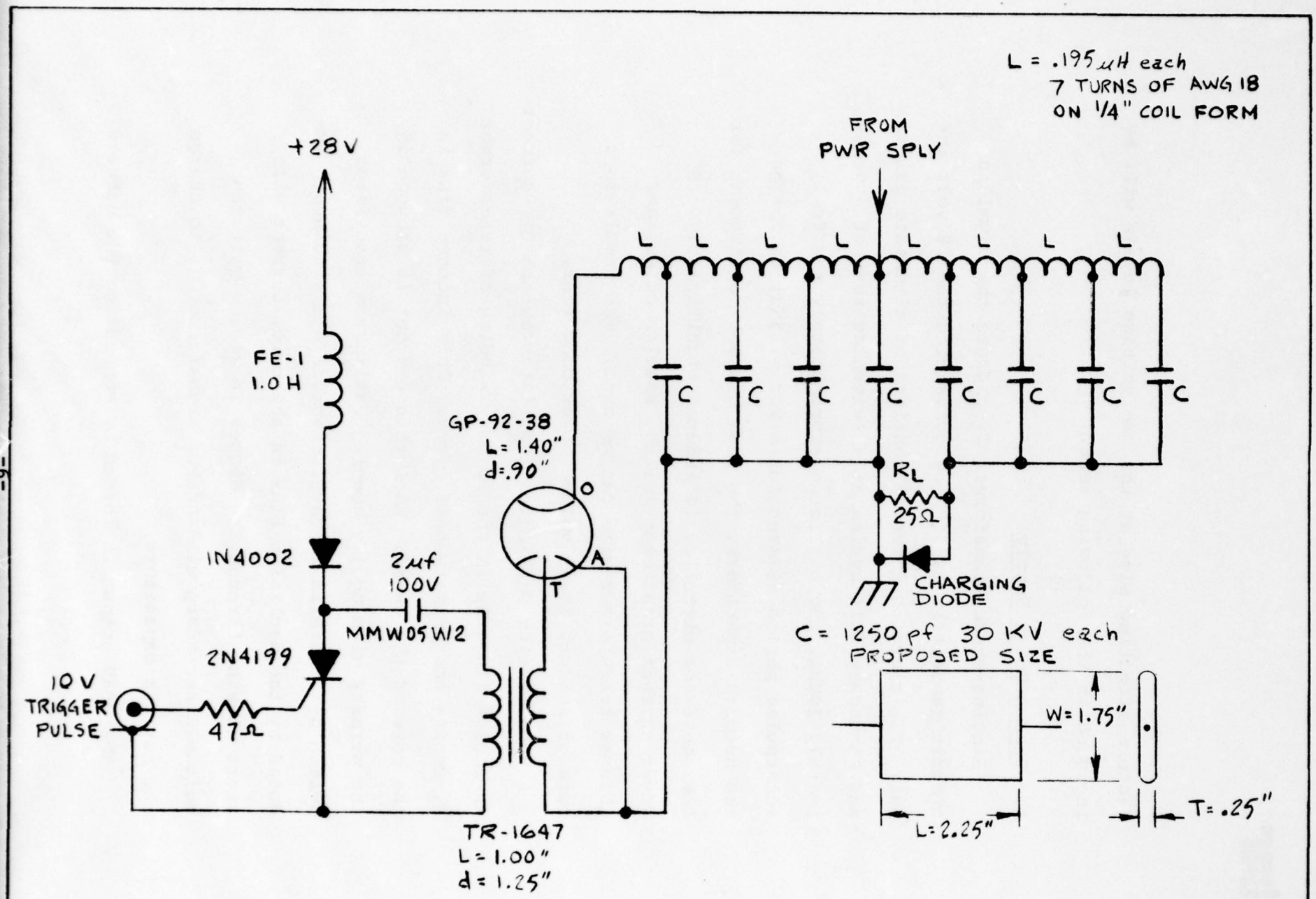

FIGURE 2
TASK A MODULATOR

Factors affecting size at the two voltage levels will be included in the following text.

A. Task A Power Supply

Ringing-choke transformer T_1 charges the Blumlein circuit capacitors to 30KV by converting the 28 volt input. The charging interval consists of alternate primary and secondary half cycles at a switching rate of approximately 20KHz. By utilizing approximately the full interpulse period (67msec for a Prr = 15Hz) to charge the network capacitors, the peak current requirement for the converter circuitry is reduced significantly. A lower current transistor switch, smaller cores, and thinner transformer wire can be used. The result is a more efficient, lower volume power converter.

Upon closing Darlington transistor switch Q_1, current increases linearly in the primary winding of transformer T_1 during the primary half cycle. This induces flux in the core of the choke. When this current is stopped in the primary winding (by opening Darlington transistor switch Q_1), polarities reverse across all windings. Induced by the declining flux in the core, current will start flowing through the diodes in series with the multiple secondary windings of transformer T_1 to charge the network capacitors.

The 30KV output is formed by connecting the outputs

of the three secondary windings of transformer T_1 in series. Each secondary consists of 2500 turns of AWG38 wire wound around a separate molypermalloy powder toroid core. Each core has an outer diameter of 1.33 inches, an inner diameter of 0.76 inches, and a height of 0.46 inches. The primary winding passes through the center window of all three cores and is insulated to withstand the 30KV potential difference between primary and secondary.

To charge a conventional pulse forming network to 60KV would require six secondary windings for transformer T_1. The primary winding would have to be insulated to withstand a 60KV potential difference. A toroid core with a larger center window would be required. A 60KV transformer for the converter would require a volume at least twice the volume for a 30KV transformer.

The function of the control circuitry is, 1) determine the correct time for turning off the transistor switch Q_1, 2) limit the input and output currents, 3) assure starting of the conversion action, and 4) establish the correct charging voltage at the output. Each function is described in more detail below.

Constant current diode CR_3 generates a ramp waveshape at the base of timing transistor Q_2. The ramp is derived from an isolated winding of transformer T_1 (the drive winding) and starts anew with every primary half cycle.

Transistor Q_2 drives current bypass transistor Q_3 through PNP transistor Q_4. When transistor Q_3 turns on, it shunts all drive current away from the base of Darlington transistor switch Q_1. As a result, the primary half cycle of the converter is terminated. The drive current originates from the drive winding through drive resistors R_7 and R_8 and is adequate to saturate transistor switch Q_1 under all operating conditions.

Drive current bypass transistor Q_3 also serves as a current limiter. Transistor Q_3 shunts all drive current away from the base of transistor switch Q_1 when the peak input current reaches a predetermined value. Current transformer T_2 monitors the current in the emitter lead of transistor switch Q_1 and provides a control signal to the base of transistor Q_3. A resistor, connected to the rectified negative reflected output voltage assures that the base of transistor Q_3 is also influenced by the value of the output voltage. As the input current is proportional to the output power (not to the output current) this circuit corrects the turn-on point of transistor Q_3 with a negative bias proportional to the output voltage. Uniform output current is achieved over the whole charging interval.

Starting is achieved by applying drive current to the base of transistor switch Q_1 from the 28 volt input.

Resistors R_2 and R_3 are used. Capacitor C_2 delays the voltage build-up such that during short circuit conditions when the secondary half cycles are very long, no positive bias appears on the base of transistor switch Q_1. During every primary half cycle the start delay capacitor is discharged through a diode so that a new delay cycle could start. Negative bias is assured on the base of transistor switch Q_1 during the secondary half cycle by applying the negative voltage of the drive winding through drive resistors R_7 and R_8.

Transistor Q_5, in parallel with timing transistor Q_2, terminates the switching converter process when the charging voltage reaches 30KV. A resistive divider provides a sample of the charging voltage to drive the base of transistor Q_5. Upon discharge of the Blumlein network, the switching converter is ready to resume the charging cycle.

B. Task A Modulator

The 30KV, 1200A pulse, having a pulse width (50%) of 125 nsec, will be formed by discharging a Blumlein circuit with a triggered spark gap. Each network of the Blumlein circuit has a 12.5 ohm impedance. To meet the 20 nsec rise time and 40 nsec fall time requirement, each network has four sections.

The capacitors in the Blumlein circuit have a signi-

ficant effect on the size of the pulse generator for Task A. To achieve minimum volume in a high voltage capacitor requires the dielectric material of the capacitor to have both a high dielectric constant and a high dielectric strength. Based on discussions with various capacitor vendors, dielectric materials presently used in the fabrication of high voltage capacitors have either a high dielectric constant or a high dielectric strength, but not both properties. In addition, some high voltage capacitors utilize a margin where the dielectric material extends beyond closely spaced capacitor electrodes. The margin is used to minimize capacitor failure at the electrode edges. As the voltage rating of the capacitor is increased, the margin increases. Since the margin does not contribute to the volume efficiency of a capacitor, it must be minimal.

Numerous capacitor vendors were contacted on the availability of a 1250pF, 30KV capacitor occupying minimum volume. A capacitor using mica dielectric was chosen. The proposed size for each of the eight capacitors is 2.25" x 1.75" x 0.25". The dielectric will be stressed at approximately 1600 volts/mil. Volume efficiency for these capacitors is increased by using a proprietary winding technique to minimize margin by series stacking

three 10KV capacitors.

The eight capacitors for the Blumlein circuit will be stacked side-by-side so that leads for adjacent capacitors are approximately 0.25" apart. The eight 0.195uH inductors will be wound in a continuous solenoid such that each inductor has a length of approximately 0.25".

The trigger pulse will be formed by discharging a capacitor with an SCR. The capacitor is resonant charged to 56 volts from the 28 volt input. A trigger transformer, having a 1:250 turns ratio, applies the high voltage trigger pulse to the trigger electrode of the spark gap. Operating the spark gap with the adjacent electrode at ground potential eliminates the requirement to insulate the trigger transformer for 30KV. Discharging a 30KV Blumlein circuit, as opposed to discharging a PFN charged to 60KV, allows use of a smaller spark gap and requires less voltage to the trigger electrode.

III. TASK B APPROACH

An ITT 7621 thyratron, modified so that the reservoir can be heated separately from the filament, has been ordered. Normally, this thyratron is provided with a common, internal connection of a reservoir heater lead and filament heater lead. Filament heater power is approximately 18 watts while reservoir heater power is approximately 2 watts.

The peak and average current requirements for Task B are much less than the absolute maximum ratings for the 7621 thyratron. The 7621 is rated for a peak anode current ib of 100A and a DC average current Ib of 0.1A. Although rated for a peak forward anode voltage of 8KV, the 7621 thyratron is expected to perform satisfactorily at 10KV for this low average power application. A test circuit will be fabricated to evaluate the performance of this thyratron to meet the requirements of Task B with filament heater power gradually reduced.

If the approach described above does not prove to be successful, one possible fallback position is to implement a series arrangement of one of the solid-state devices which will undergo evaluation to meet the requirements of Task C. In addition, the use of a magnetic switch to meet the requirements of Task B will be investigated.

IV. TASK C APPROACH

A survey of commercially available devices to meet the ultra high speed requirements of Task C was conducted. A major consideration in choosing possible candidates was that the device require minimal drive to turn on. Three devices were selected. A MOSPOWER FET, an avalanche transistor, and a nanosecond SCR. Test circuits using these devices in a series arrangement have been constructed and will undergo evaluation.

Figure 3 shows the test circuit for the VMP22 MOSPOWER FET. The VMP22 MOSPOWER FET has a minimum drain-source breakdown voltage of 90 volts. Voltage sharing between the two VMP22 devices is provided by the divider consisting of resistors R_1 and R_2. To achieve nanosecond response time, a short duration, high current drive pulse is required to charge the input capacitance of 50pF typical and output capacitance of 40pF typical of the VMP22. The MH0026, an MOS clock driver capable of high peak output currents, provides drive to Q_1. Capacitors C_1 and C_2 form a capacitive divider to couple charge to the gate of Q_2.

Figure 4 shows the test circuit for the 2N5271 avalanche transistors. Capacitors C_1 and C_2 are charged in parallel and discharged in series through transistors Q_1 and Q_2

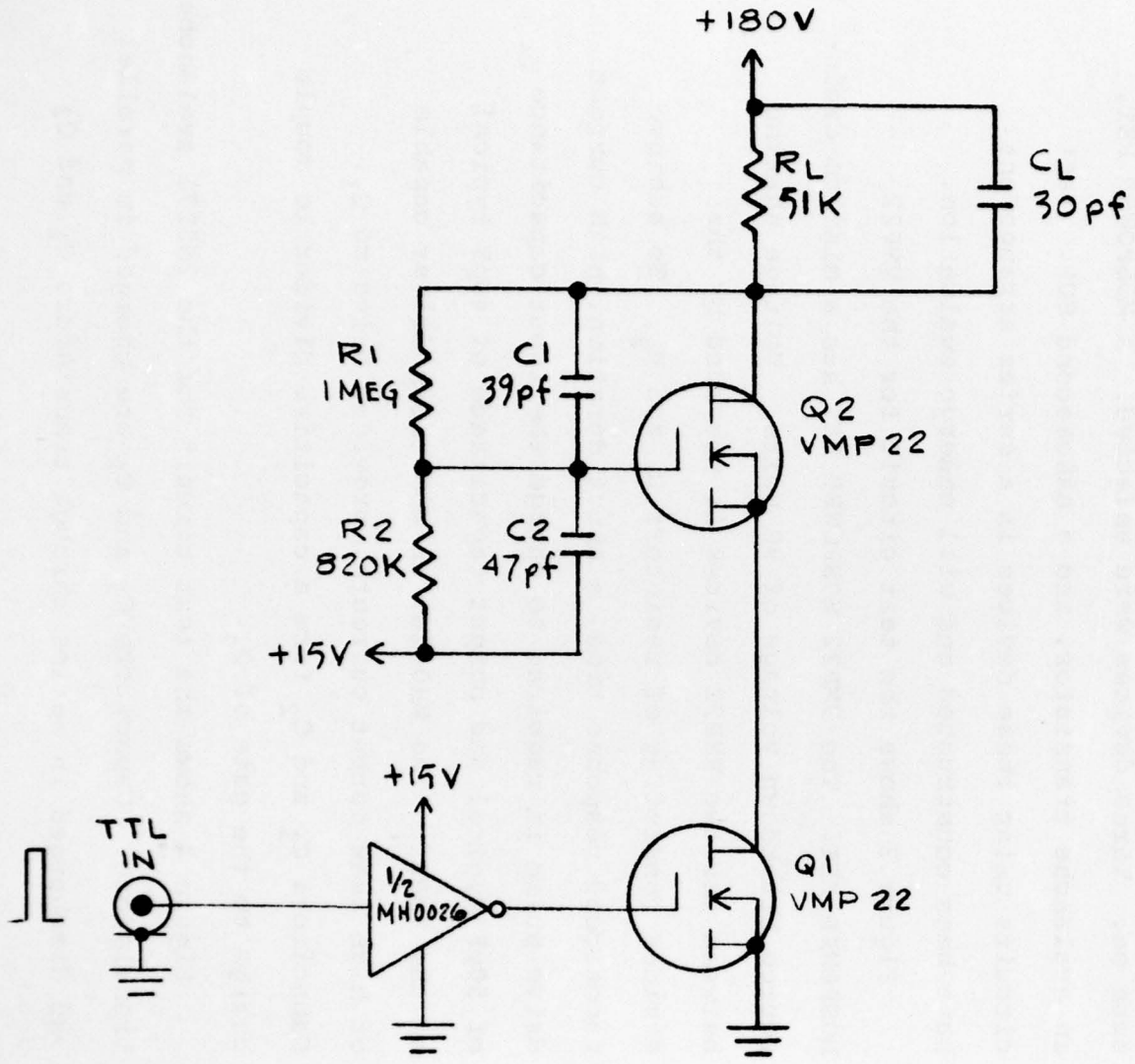

FIGURE 3

MOS POWER FET TEST CIRCUIT

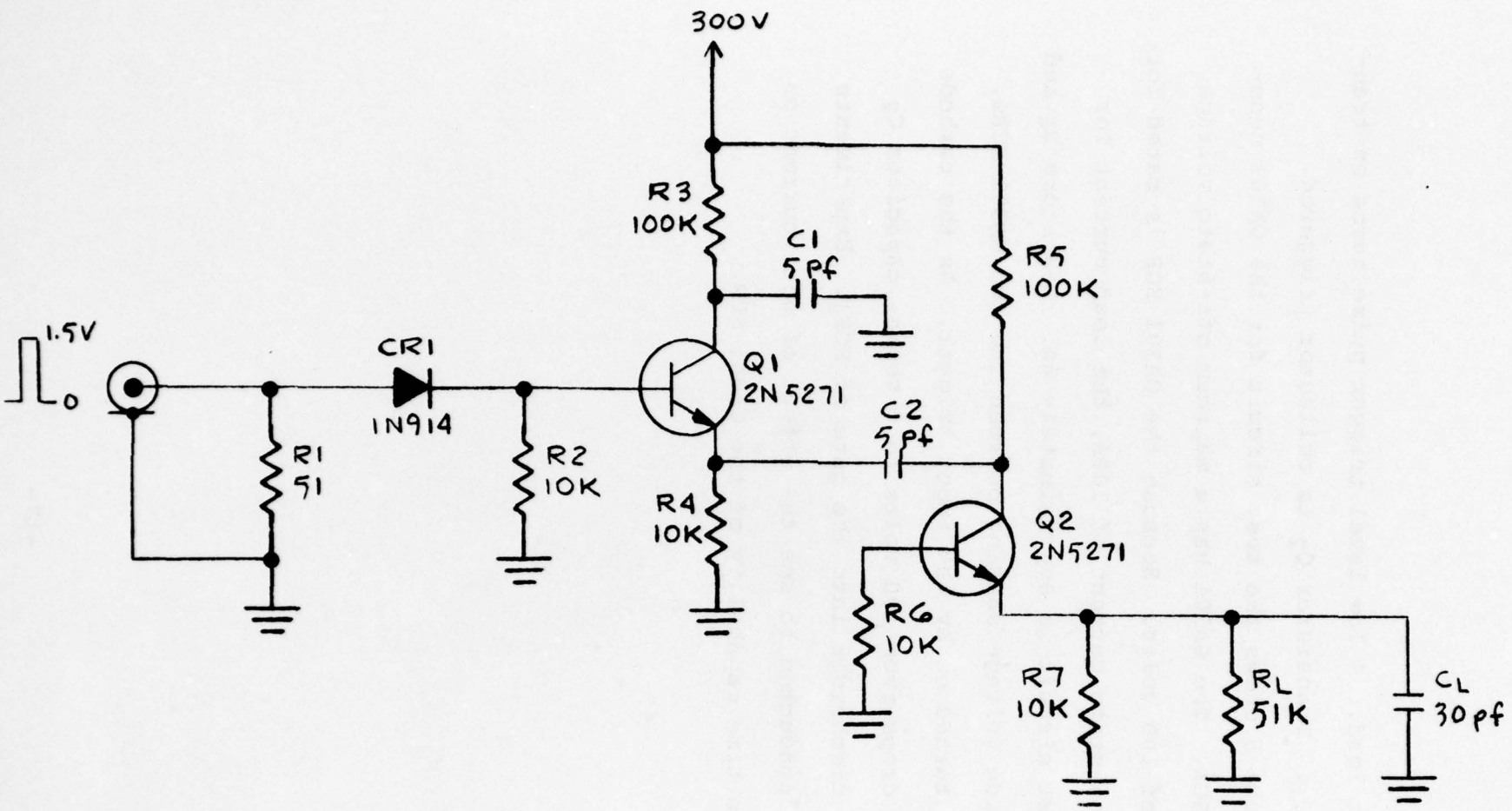

FIGURE 4

AVALANCHE TRANSISTOR TEST CIRCUIT

into the load. A low level trigger pulse turns on transistor Q_1. Transistor Q_2 is collector triggered.

Figure 5 shows the test circuit for the GA301 nanosecond SCR. The GA301 has a maximum off-state voltage rating of 100 volts. Because the GA301 SCR is rated for a peak on-state current of 100A, the load current for this test circuit is approximately 4A. Resistors R_6 and R_7 provide voltage sharing between the two GA301 SCRs. SCR_1 is turned on by the input trigger. As the cathode of SCR_2 drops from 100 volts to 0 volts, capacitor C_2 rapidly discharges into the gate of SCR_2. Experiments will be conducted to see the effect of gate current on the rise time capability of the GA301 SCR.

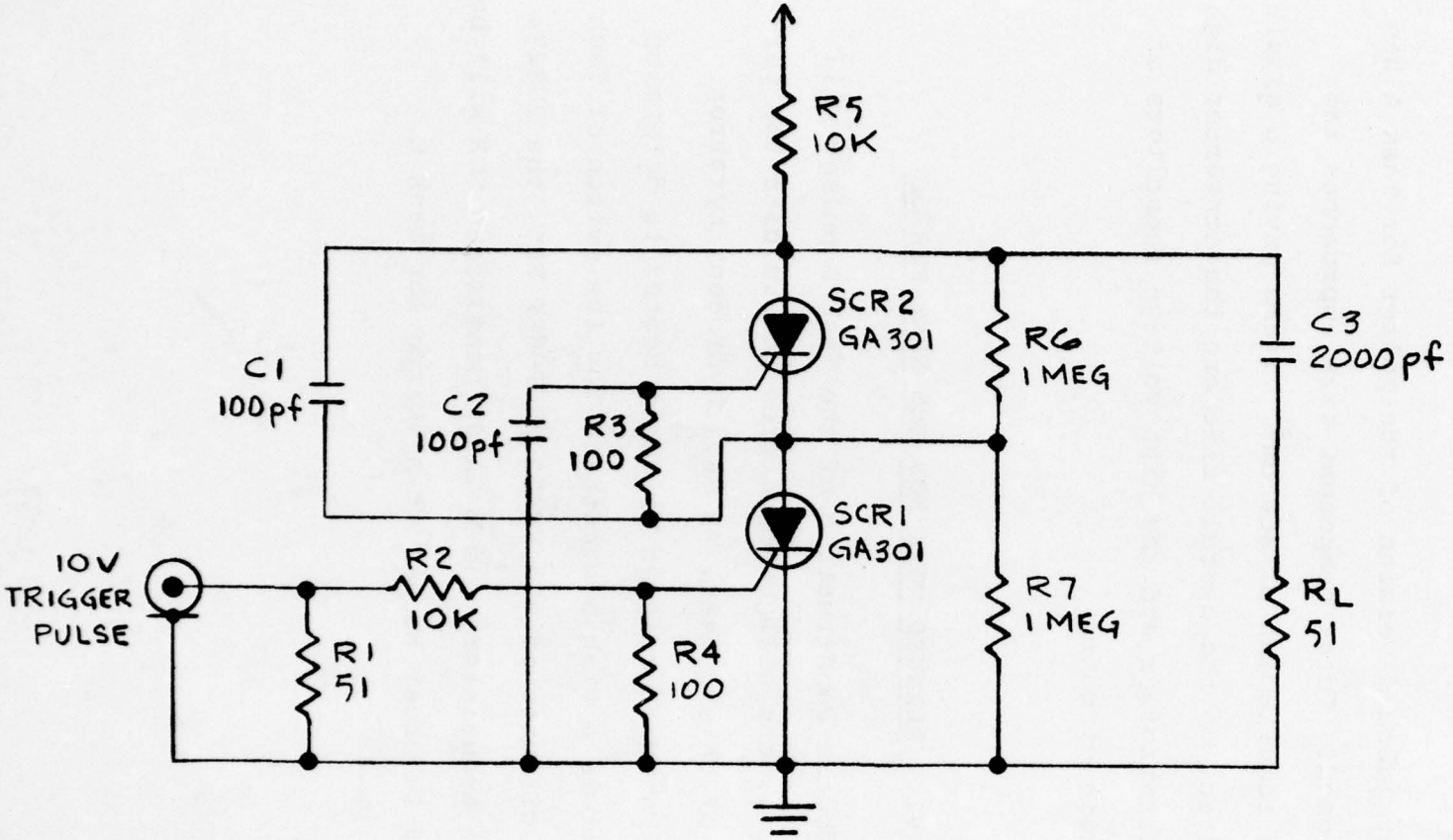

FIGURE 5

NANOSECOND SCR TEST CIRCUIT

V. CONCLUSIONS

The breadboard version of the pulser for Task A has been designed. Total component size approaches the specified requirement of 360 cm^3. Items having a significant effect on the overall size are the converter high voltage transformer and the high voltage capacitors of the Blumlein circuit.

VI. PLANNED WORK FOR THE NEXT PERIOD

Breadboard construction of the Task A pulser will commence. Tests will be conducted to evaluate the performance of this pulser. A 7621 hydrogen thyratron will be tested at reduced filament heater to determine whether it is a viable candidate for the switch of Task B. Test circuits of the VMP22 MOSPOWER FET, the 2N5271 avalanche transistor, and a GA301 nanosecond SCR will be evaluated in order to select a switch for Task C.

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