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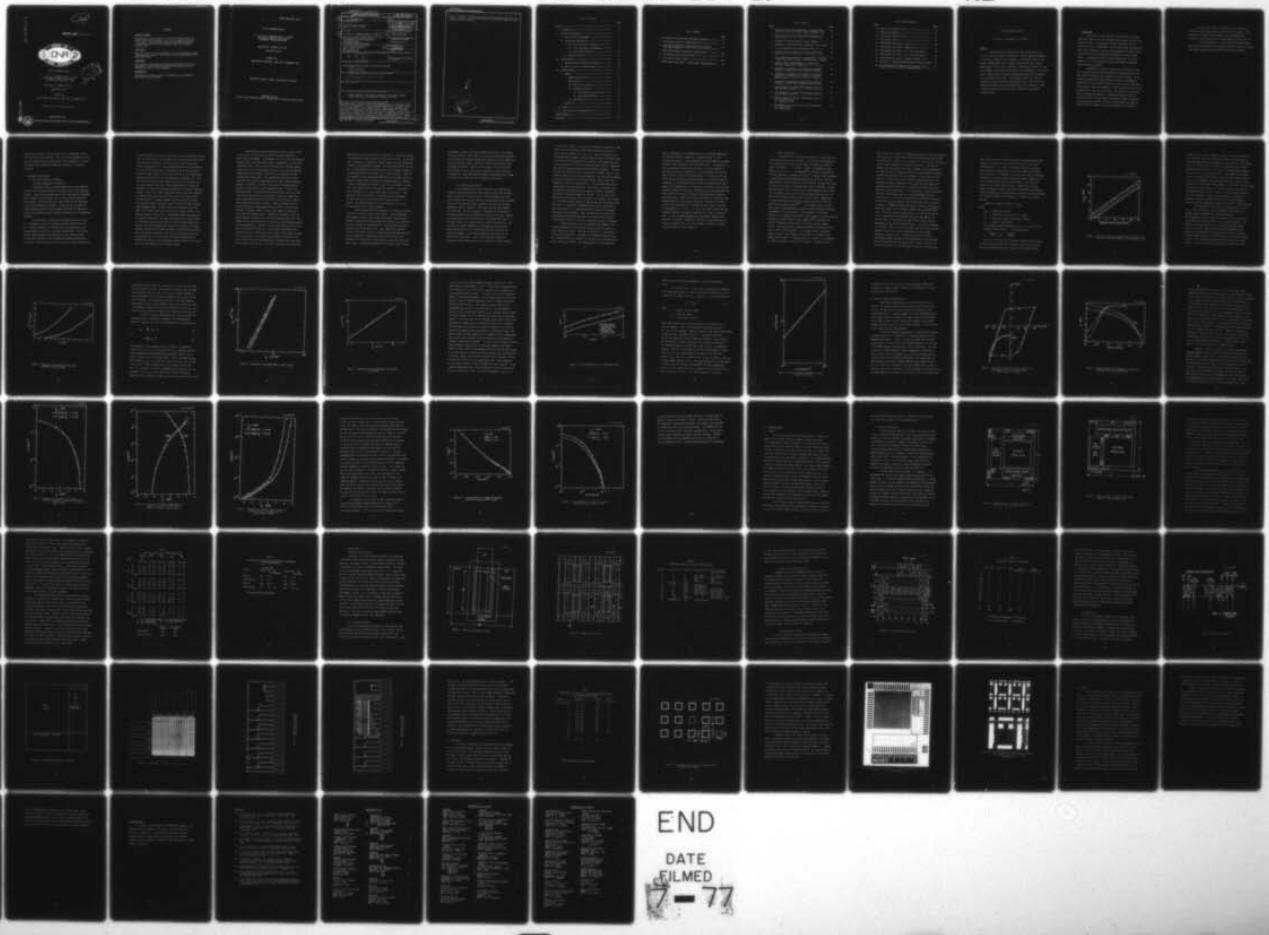

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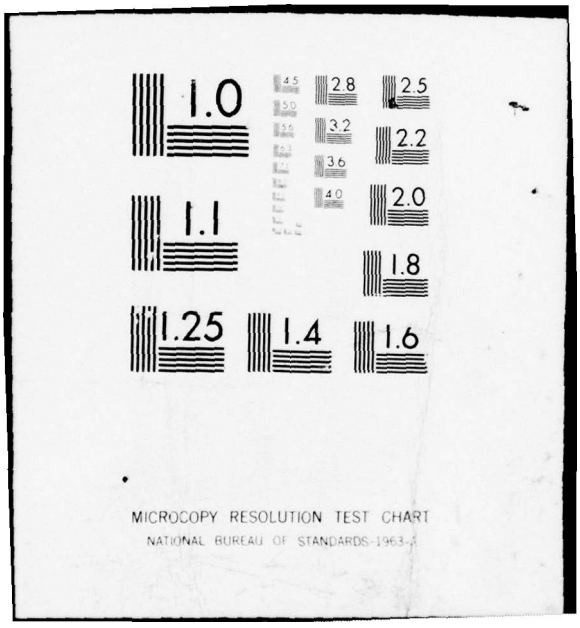
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THIN FILM MEMORY DEVICES

K. K. Yu, P. R. Malmberg and T. P. Brody
Westinghouse Research Laboratories
Pittsburgh, Pennsylvania, 15235

ONR Contract - N00014-75-C-1138

ONR TASK 213-134

15 APRIL 1977

FINAL REPORT FOR PERIOD 1 JUNE 1975-13 DECEMBER 1976

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Individual memory transistors have been developed which are ten times faster than previous transistors. Various charging mechanisms of the memory transistor were considered. It now appears that the high channel impedance model most accurately represents the slow negative WRITE behavior of the memory transistors. Addressing and control circuits were designed to permit practical operation of the memory in a block access mode. A WRITE mode was developed which greatly reduced the disturbance of non-addressed memory cells. A high density memory test array was designed and fabricated with operating memory

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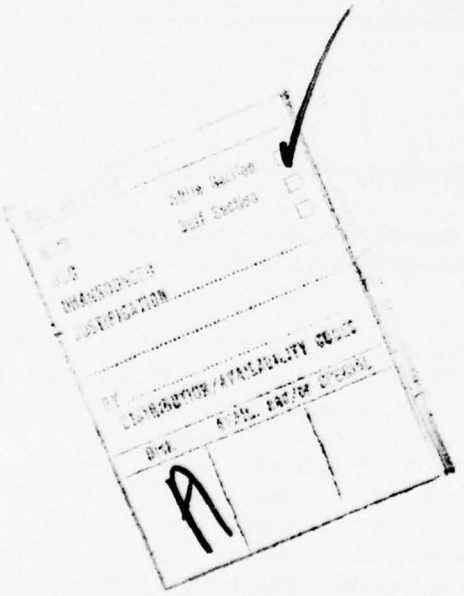
cells. Sufficient knowledge and experience were gained through this work to permit us to make a practical nonvolatile thin film memory compatible with existing computer systems.



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THIN FILM MEMORY DEVICES

K. K. Yu, P. R. Malmberg, T. P. Brody

Abstract

Individual memory transistors have been developed which are ten times faster than previous transistors. Various charging mechanisms of the memory transistor were considered. It now appears that the high channel impedance model most accurately represents the slow negative WRITE behavior of the memory transistors. Addressing and control circuits were designed to permit practical operation of the memory in a block access mode. A WRITE mode was developed which greatly reduces the disturbance of non-addressed memory cells. A high density memory test array was designed and fabricated with operating memory cells. Sufficient knowledge and experience were gained through this work to permit us to make a practical nonvolatile thin film memory compatible with existing computer systems.

I. Introduction

This project is the outgrowth of several years' work (also sponsored by ONR) on the basic component device, namely, the thin film memory transistor. The originally envisaged application of this transistor was in X-Y addressible "active matrix" arrays, in conjunction with a display material, such as an electroluminescent phosphor layer, the whole to form an electronically addressible flat panel storage display. A small scale version of such a display (40 x 40 picture elements on a 1 inch square) was developed and demonstrated during previous contract periods[1].

Subsequently, it became evident that the same basic device and technology (thin film vacuum deposition) could be utilized in the fabrication of extremely large nonvolatile digital memories. It was therefore proposed that a small effort be devoted to a feasibility demonstraton of such a memory, fabricable entirely by thin film deposition techniques, and thus potentially of very low cost by virtue of the automatability of the thin film process. Thin film LSI circuits have been successfully fabricated by a completely automated sequence of operations inside a single, highly sophisticated, computer-controlled vacuum deposition system[2], and hence, the probability was high that eventually memory arrays could also be fabricated in this fashion.

In the present contract, the objective was to design and fabricate a 4kbit block-oriented thin film nonvolatile memory, as well as continue to improve the performance of the individual memory transistors. These objectives were largely,though not fully, achieved.

In this Final Report, we cover work on process improvements, memory device development, device modeling, analysis of speed of response, 4kbit memory design, test-array design, fabrication and results.

II. Process Investigation

The thin film deposition system was carefully reviewed in terms of the processing requirements for the 4-kbit memory to be fabricated. Because of the high density and large area features of the memory array, uniformity and yield factors play particularly important roles in the overall process consideration. Repeatability and optimization of the devices should also be considered at the same time due to the implicit relationship between these two factors and uniformity. A highly optimized device would not be practical if its parameters are so sensitive to small process variations as to drastically affect the uniformity of the devices in the whole array. During the course of this program, the work on process investigation can be grouped into two categories. One dealt with the vacuum deposition system and its associated toolings. The other dealt with the fabrication process itself.

A. Vacuum System and Equipment

One of the major factors for low yield in thin film integrated circuits is electrical shorts. Such shorts can result either from misalignment of masks or from actual physical imperfection of the deposited layers. The problem of physical imperfection will be discussed later in the fabrication process section. Mask misalignment can sometimes be due to poor mask/substrate registration of the mask changing assembly. However, this was not usually the case in our system. We

found that the misalignment was more often caused by heating effect on the mask itself. In extreme cases, the mask even buckled as a result of thermal expansion. This was particularly true when a material was deposited at high power and for a long time, such as that used for thick Al_2O_3 or for gold depositions. To minimize the thermal expansion problem, special Kovar heat shield masks were used under the regular masks (i.e., on the side exposed to the radiation source). The design of the shield masks were such that distortion of the mask do not affect the pattern on the regular mask. Results of this scheme had been very satisfactory.

A variable speed rotating shutter with a specially designed slit opening was installed in the vacuum system. The purpose of this shutter was to control the deposition of extremely thin layers such as the Al used for the floating gate of the memory device, or the In used for doping of the CdSe semiconductor. The opening of the slit was so designed that every position on the substrate is exposed for exactly the same amount of time after one complete sweep of the slit across the substrate. The amount of exposure time of the substrate is determined by the speed of the shutter rotation and the number of passes of the slit across the substrate. The angular speed of the shutter can be varied continuously from 3 to 40 degrees per second, corresponding to substrate exposure times of 0.65 to 0.053 seconds per pass respectively. The rotating shutter essentially extended the low end of the operating range of the existing deposition monitor by more than one order of magnitude. Using this shutter, In doping of the CdSe semiconductor had been

accurately controlled to less than 0.1Å thick, an equivalent of about 10^{13} atoms/cm^2 in atomic density. Also, as will be discussed in a later section on memory device processing, this shutter enabled us to control and optimize the floating gate deposition condition not previously attainable.

B. Fabrication Investigation

1. Thin Film Transistors in General

(a) Yield Improvement Investigation

As mentioned earlier, physical imperfection of the deposited layers is one of the major factors of low yield in thin film integrated circuits. Causes of this problem varied over a wide range of categories. Many of them are system dependent due to the particular design of the vacuum system. Some are general thin film problems and are applicable to all thin film deposition systems. In this section, we report all problems associated with our own deposition system and our approach in solving these problems relating to physical imperfection of the deposited materials.

To avoid shorts or opens in the finished thin film circuits, it is necessary to clean the substrates and masks carefully for every run. The glass substrates, as obtained from the manufacturer, have various degrees of surface dirt and edge irregularities. After trying various cleaning materials and studying the wafer cleaning methods for the silicon industry, a new procedure for substrate cleaning was introduced. The new procedure involved a series of careful cleaning and

inspection steps to be carried out for each substrate just before insertion into the vacuum system. The sequence of the solutions used is such that each solution is compatible with the previous solution and removes residues remaining from it. Edge irregularities are carefully smoothed out to avoid tiny glass chips on the substrate before the cleaning is initiated. Masks should be cleaned after each use to avoid accumulated material from getting onto the new substrates in subsequent use. This is particularly true for thick deposition masks such as that used for the Al_2O_3 insulator deposition. Thick accumulation also reduced the openings on the mask; thus reducing the geometry of the actual deposited pattern. Worst of all, thick accumulation tended to peel when subjected to thermal stress, resulting in shorts or opens in the final circuit. Previous method of cleaning the masks required the removal of masks from the mask holders, resulting in days of tedious and time consuming mask realignment tasks. A new procedure was developed to allow the masks to be cleaned without being removed from the mask holders, a tremendous saving in time and labor. As mentioned a while ago, peeling of the deposited materials on the masks and fixtures in the vacuum system is a potential low yield factor when it occurs during the fabrication process. Several experiments were conducted to eliminate the peeling problem, especially on the masks, the edge of the electron gun crucible, and on the shield and shutter. We found that selectively coating the problem areas with a very thin layer of indium or aluminum greatly enhanced the adhesion of the subsequently deposited material onto these areas and thus eliminated the troublesome problem.

Metallization is also an important process in terms of final circuit yield. Even the silicon industry placesheavy emphasis on metallization development. At the moment, gold is our main metallization material, and is used many times during the fabrication of a thin film integrated circuit. Gold is used for the contacts to the TFT devices as well as for all the interconnection lines. Due to its high melting temperature and high thermal conductivity, the evaporation of gold requires high thermal power. Our investigation indicated that gold evaporation was partially responsible for the masks' thermal expansion problem. In addition , the whole vacuum system was being heated up and must be cooled before the next deposition step. Precious time was being wasted. Furthermore, many electrical shorts had been traced to particles splattered onto the substrate. Upon close examination, these splattered particles had been found to be gold spitted from the source during the evaporation process. Several alternative ways of evaporating gold were experimented with in an effort to improve the situation. Different shapes of Al_2O_3 coated tungsten heating coils were tried with moderate success. Although both problems of heat and splattering were reduced by the use of these coated heating coils, the coating cracked easily after each run and the gold was contaminated with the cracked material. It would be too costly and wasteful to use a new heater and new gold for every run. Other methods experimented with involved the use of crucible liners for the water cooled copper crucible of the electron gun. The crucible liner thermally isolated the cold copper crucible from the e-beam heated gold, allowing lower input power for the same evaporation rate. As a result, the whole vacuum system was

much cooler during and after the gold evaporation. In the early series of experiments, a single graphite crucible liner was used. It was found that, in addition to reducing the thermal problem, the gold splattering problem was also drastically reduced. The exact reason was not too clear, but it was postulated that it might be due to less thermal "turmoil" in the molten gold source as a result of the thermal isolation. Based on this assumption, gold evaporation experiments were performed using two graphite crucible liners to increase the thermal isolation. However, no drastic improvement was observed. Even so, we continued to use the double liner method because there was less cracking of the graphite liner, presumably due to less thermal stress in each liner. Gold deposition rate was optimized by considering the various thermal and time effects as well as the final TFTs and test circuit results. The optimum condition for fabricating thin film circuits was obtained at a rate of about 0.5Å/sec.

Copper metallization was considered as a possible alternative to gold for economic as well as yield reasons. Initial experiments using graphite crucible liners yield unsatisfactory results mainly because of similar splattering problems as occurred in gold deposition. It was also found that the average size of the splattered particles increased with the deposition rate. Other commercially available crucible liners made of vitreous carbon,hot pressed graphite and intermetallic compound of titanium diboride/boron nitride were tried. Although none of these liners yield completely nodule-free deposited copper layers, a double-liner combination of vitreous carbon (inside)

and graphite (outside) did yield reasonably good layers. On the large area test capacitors using 1500Å of Al_2O_3 and the double-liner-deposited Cu electrodes, the average breakdown field obtained was about 4×10^6 V/cm. This was reasonably close to the value of 6×10^6 V/cm obtained for the $Al/Al_2O_3/Al$ structures. However, the occurrence of shorts was still more frequent for the Cu electrodes as compared to the Al electrodes. It seemed that a multi-metallization approach using both Al and Cu might be the best for a high yield, low cost memory array process.

(b) Miscellaneous Studies

We have observed from time to time that well controlled and repeatable device characteristics would suddenly depart from the usual expected values for no obvious reasons. When experiments were consequently planned and conducted, the device characteristics would gradually come back to the expected values, sometimes even before the intended experiments could be completed. This effect was both time consuming and frustrating. But more important, it may even lead to erroneous conclusions drawn from the experiments carried on at the time. Drawing on the experience here through the years, we have identified one of the major causes of the sudden changes in device characteristics. The cause was the varying composition of the evaporant source material. This was particularly true for materials that could react with the ambient environment or could change composition as a result of the evaporation process itself. CdSe is a material that changed its composition during evaporation due to the difference in vapor pressure

of Cd and Se. However, we found that by properly conditioning the CdSe source, we could repeatedly control the resultant drain current to within a few microamperes from run to run. CdSe was evaporated from a resistively heated tungsten crucible coated with Al_2O_3. We started with a fresh batch of CdSe material in the crucible, in an amount much more than that required for one run, and used this same source for subsequent runs until the deposited films resistivity began to increase. To condition the CdSe source material, we evaporated off 2000Å of CdSe at a rate of 2Å per second with the substrated shielded. Then the rate was lowered to the device deposition rate of about 0.5Å per second (actual rate dependent on the device specifications). This pre-evaporation was performed before every CdSe deposition. After about 10 deposition runs, the deposited CdSe films resistivity began to increase, resulting in high positive threshold voltages for the TFTs. The used CdSe source material was then replaced with a new batch. In a series of six consecutive runs where the only deposition variation was the conditioning of the CdSe source, we established unambiguously that proper conditioning of CdSe source material is a good and practical procedure for obtaining predictable device parameters. When the CdSe source was used without the deliberate conditioning procedure, the resultant device current varied greatly from run to run with no particular pattern of variation.

Annealing effects on device parameters were examined. The initial experiments were concentrated on the prolonged annealing at a fixed temperature of 360°C. This was the temperature at which most of the devices were annealed. In general, with increased annealing time, the transconductance g_m of the TFT increased while the zero-gate-biased drain current I_{d0} decreased. The annealing effect on both parameters

could be explained on the assumption that at the annealing temperature, the CdSe film gradually changed from an amorphous phase to a more crystalline structure. As this happened, the electron mobility increased because of less scattering in the crystalline region. Consequently, g_m also increased with annealing (See section III on Device Physics for the relation between g_m and mobility). Before annealing, the CdSe TFT showed very poor field effect characteristics. In particular the drain current showed very little saturation tendency as the drain voltage was increased. As the film became more crystalline and behaved more like a single crystal semiconductor, the drain current saturation characteristic improved, resulting in lower I_{d0}. Both g_m and I_{d0} slowly approached some final values as the structural change of the semiconductor reached an equilibrium state. However, the rate and the amount of change with time depended greatly on the particular fabrication processes of the TFTs. At 360°C, the time required for attaining the final values could vary from 40 minutes up to 15 hours. For most of the memory devices near the optimized condition, the required annealing time is about 45 minutes at 360°C. At lower annealing temperatures, the required annealing time increases, as expected. Stability of the TFTs was also monitored as a function of annealed time. From the experiments conducted, no effects on device stability had been observed.

2. Memory Transistors

The memory TFT we have been investigating is a dual dielectric insulated gate field effect transistor. The concept of controlling the trap characteristics between the two dielectric layers was originally derived from two particular sources. Firstly, we attempted to adopt Kahng and Sze's concept of floating gate[3] to improve our memory TFT. Secondly, the work of Laibowitz and Stiles[4] on charge storage phenomenon of small metal particles seemed particularly suited for our thin film memory devices. When the metallic layer between the two dielectric layers is thick and continuous, the floating gate model is applicable. However, when the metallic layer is so thin as to be discontinuous in such a way that the metallic particles are actually isolated from each other, the metal particle charge storage concept is more suitable. Combination of these two concepts have resulted in useful and practical thin film memory devices reported earlier[5-7]. At the present time, we have no direct means of distinguishing one model from another based on electrical measurements of the final devices. For convenience, we have been referring to our memory device as FGTFT (floating gate thin film transistor). Meanwhile, concurrent with our work, Kahng et al[8] introduced the concept of interfacial dopant (IFD) for the dual dielectric memory devices. They reported useful tungsten IFD doping concentration in the range of 10^{14} to 10^{15} atoms/cm^2. In our memory devices, the general range of metallic layer thickness is about 10Å. For aluminum, with a gram-molecular weight of 27 grams per mole and a density of 2.7 grams/cm^3, the 10Å is equivalent to about 6×10^{15} atoms/cm^2. In view of this fact,

we are now also referring to our floating gate layer by the more appropriate name of interfacial dopant layer. We also change the name FGTFT to MTFT (for memory TFT). However, we will continue to characterize our IFD layer in terms of layer thickness for convenience in practice. Both gold and aluminum were investigated for the IFD. However, from our experiments we found that gold IFD generally caused more frequent shorts of the gate structure than aluminum. This was attributed to large pieces of gold nodules on the film coming from the actual evaporation process. Consequently, all results presented in this report are with aluminum IFD. Aluminum thickness varying from 5 to 30 Å had been investigated with deposition rates ranging from 2 to 22 Å per second. Using the saturated threshold voltage window ΔV_{HL} (for a given WRITE/ERASE voltage of $\pm$ 30 volts for 1 sec each) as a quick measure of the memory TFT quality, we found that ΔV_{HL} increased with the IFD deposition rate as indicated in Figure 1. Threshold voltage window ΔV_{HL} is defined as the algebraic difference between the two threshold voltages after each WRITE/ERASE cycle. The data presented in this figure are for an IFD thickness of 11 Å. Although there is considerable scatter in the results, the general trend, as indicated by the shaded region, shows a definite improvement of ΔV_{HL} with IFD deposition rate. To the best knowledge of the authors, this is the first time that such results had even been reported. There are no previous publications on this subject. Although the results in Fig. 1 indicated an interesting linear relationship between ΔV_{HL} and the IFD deposition rate, this phenomenon has not been subjected to theoretical study. However, there are two possible explanations for the improvement of ΔV_{HL} with IFD deposition

rate. One is that the sticking coefficient of aluminum onto the gate insulator is improved at higher deposition rate due to the higher impinging energy. As a result, more dopants remained on the device even though the thickness monitor recorded the same total thickness. This possibility is in agreement with the increase of ΔV_{HL} on IFD layer thickness to be discussed later. The second possible explanation is that the dopant nuclei particle sizes condensed on the device are smaller at the higher deposition rates. Assuming that the total deposited volume of aluminum is the same at the different deposition rates, and treating the charges stored at the dopant particles according to the capacitor model as in reference (4), we found the following results:

charges per condensed nucleus $Q_i = C_i V_{app}$

where

V_{app} = applied gate voltage

C_i = capacitance of each nucleus = $\frac{\varepsilon}{t} 4\pi r_i^2$

ε, t = dielectric constant and thickness of Al_2O_3

r_i = radius of each nucleus.

total charges stored in the entire device is $Q = N\ Q_i$ for the N deposited aluminum nuclei. Q can be expressed as

$$Q = \frac{4\pi\varepsilon V_{app}}{t} (N\ r_i^2) = \frac{\text{constant}}{r_i}$$

since $N\ r_i^3$ is constant for a fixed total volume of all the nuclei. The above calculation shows that for smaller nuclei sizes, the total charge, and consequently ΔV_{HL}, is larger for a given WRITE voltage.

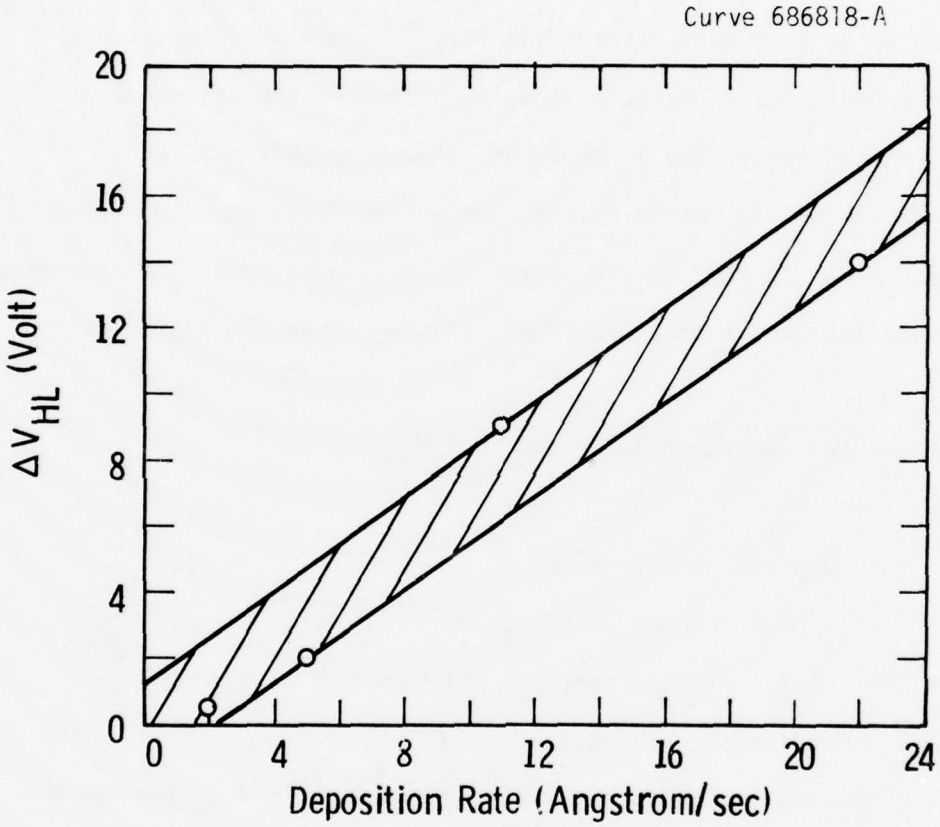

Figure 1. Threshold voltage window dependence on the deposition rate of Al interfacial dopant. Dopant thickness - 11Å

To obtain a more explicit dependent of ΔV_{HL} on the aluminum deposition rate, much more refined and controlled experiments will be needed to study the aluminum nucleation phenomena on glass substrates. The scattering in the results of Fig. 1 could be the accumulated effect of non-uniformity and uncertainty in the accuracy of the monitoring equipment at the low end of the indicating scales. As an example, a 1 Å variation in the IFD thickness would amount to about 10% error! Exact dependence of ΔV_{HL} on IFD thickness is more ambiguous than on the IFD rate, mainly because of the reason sighted above. However, we found that, in general ΔV_{HL} increased with IFD thickness up to about 10 Å, and was insensitive to IFD thickness from 10 to 30 Å. From 20 to 30 Å, gate shorts tended to occur more frequently. Based on these observations, an optimal IFD thickness range was established to be about 10 to 20 Å, yielding a practical Al doping concentration ranging from 6×10^{15} to 1×10^{16} atoms/cm^2.

Investigation was also conducted in optimizing the thin SiO layer. This thin layer has a major influence on the transport of charges between the semiconductor and the memory traps at the Al_2O_3/SiO interface. Like any other thin films, the properties of the SiO layer are very sensitive to the deposition condition. SiO deposition rate was varied from 2 to 10 Å/s with thickness varying between 90 to 200 Å. Again using the saturated threshold voltage window as a quick measure of the memory device quality, we found the optimum SiO deposition rate to be about 2 Å/s with an optimum thickness of 100 to 130 Å. Higher deposition rate generally yield less stable devices. As to the thickness, gate shorts occurred when the SiO was

less than 100 Å thick. As the SiO thickness increased, larger WRITE voltages were required for the same switching. In order to have WRITE voltages between 30 and 40 volts, the SiO layer should not be more than 130 Å thick.

III. Device Physics

A. General Thin Film Transistor Parameters

In an attempt to optimize the memory TFTs, we investigated the gain of the TFTs in more detail. Improving the gain of the memory TFT is equivalent to an indirect improvement in the memory switching capability. In particular, we examined the transconductance g_m and the electron mobility μ of the TFTs at various current levels. In the theory of the conventional field effect transistors (FET), the saturated drain current I_{ds} can be approximately described by the equation:

$$I_{ds} = K(V_g - V_T)^2 = \frac{\mu Cg}{2\ell^2}(V_G - V_T)^2 \qquad (1)$$

where

K = proportionality constant

V_g = applied gate voltage

V_T = threshold voltage

Cg = gate capacitance

ℓ = channel length

μ = carrier mobility

The square root of I_{ds} is then proportional to the applied gate voltage. In the TFTs studied, we found that $(I_{ds})^{1/2}$ and V_g do not have the same relationship for both depletion mode and enhancement mode TFTs (as shown in Figure 2). If equation (1), describing the I-V behavior of

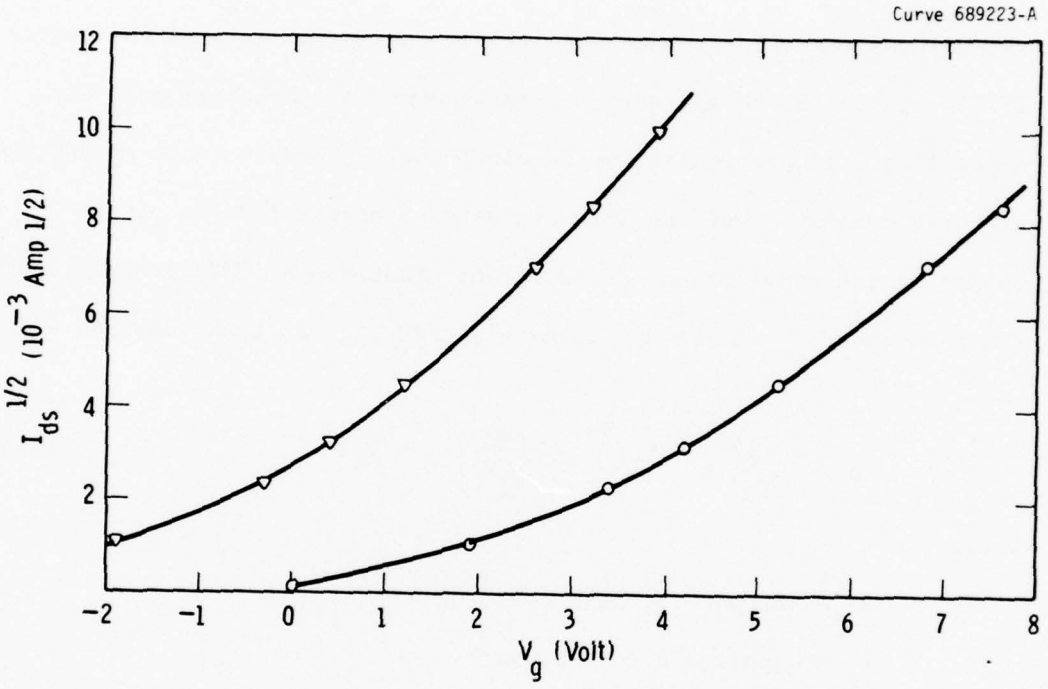

Figure 2. Square root of saturated drain current dependence on gate voltage

the general insulated-gate FETs, is applied to the TFTs, then the TFTs can be considered as having a proportionality constant K that is slowly increasing with either the drain current I_{ds} or the gate voltage V_g. Since the parameter K involves mostly geometric factors except for the carrier mobility μ and the dielectric constant of the gate insulator (incorporated in Cg), the most probable cause for the varying K is that μ is dependent on either the carrier concentration or the electric field instead of being constant as assumed in the derivation of equation (1).

In order to evaluate the mobility effect in more detail, the transconductance of the TFTs were examined. The transconductance, defined as $\Delta I_{ds}/\Delta V_g$, can be derived from equation (1) and expressed as:

$$g_m = \frac{\mu C_g}{\ell^2} (V_g - V_T) \tag{2}$$

or

$$= \left(\frac{2C_g}{\ell^2} \mu I_{ds}\right)^{1/2} \tag{3}$$

The expression for g_m indicated that, for constant μ, it should be a linear function of V_g or of the square-root of I_{ds}. Typical results of several geometrically identical TFTs with different values of V_T are shown in Figures 3 and 4 on log-log scales. Figure 3 indicates that g_m varies almost as $(V_g - V_T)^2$ rather than linearly with V_g. The fact that Figure 3 does not show a single line for the different devices may be due to the uncertainty involved in estimating the true value of V_T. The dependence of g_m on I_{ds} for the same devices is shown in Figure 4. Regardless of the different V_T values and the type of devices, all the data

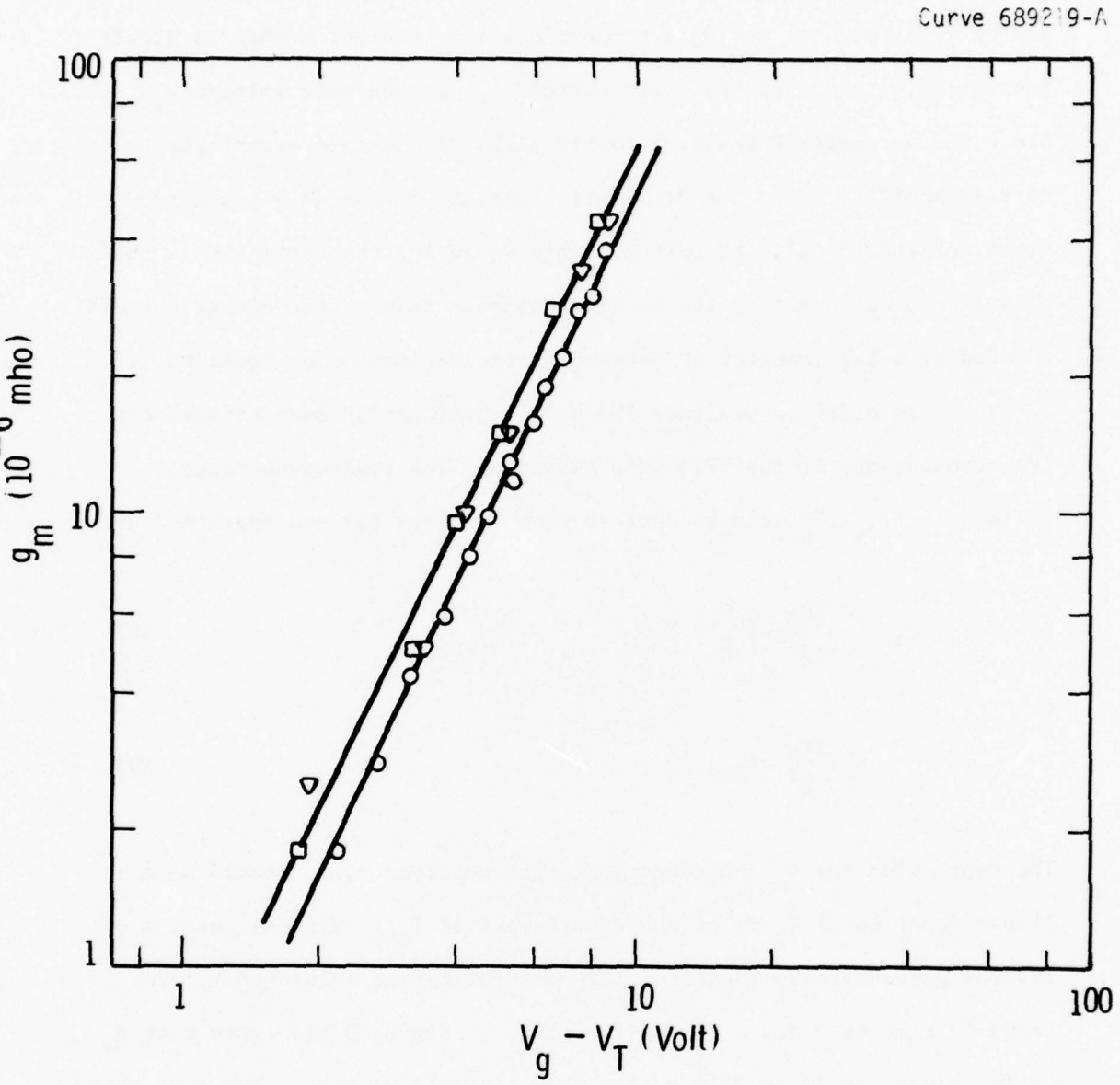

Figure 3. Dependence of transconductance on gate voltage

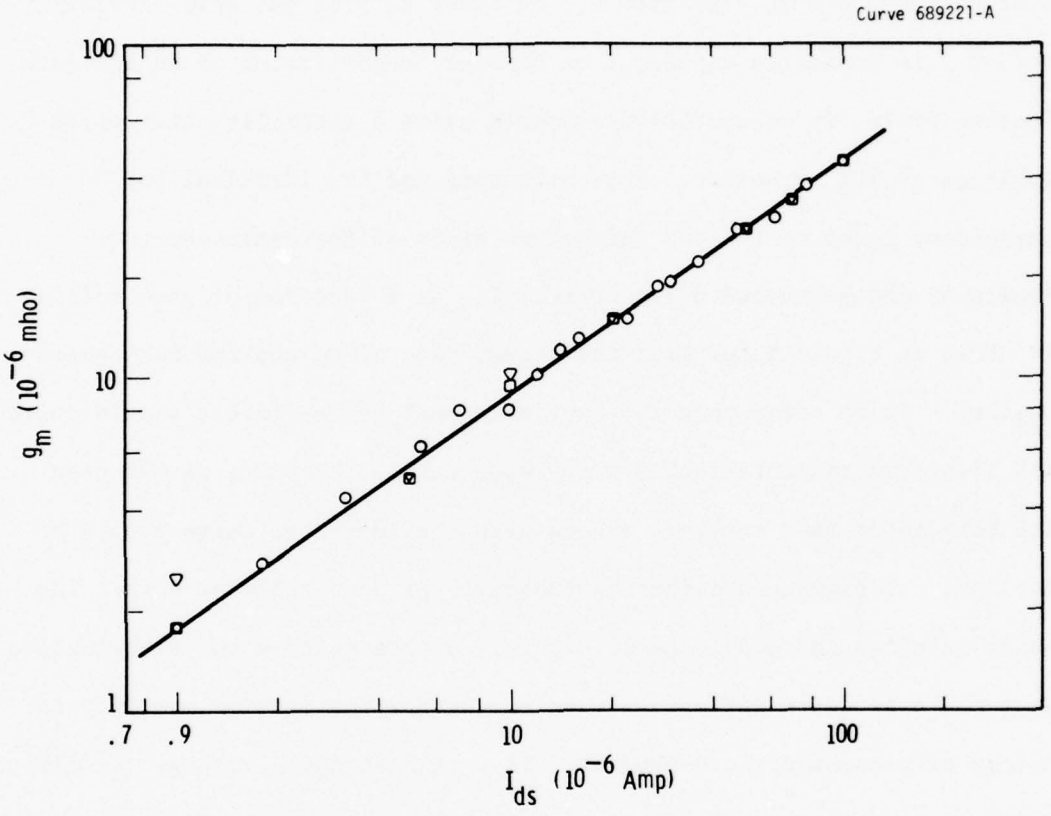

Figure 4. Dependence of transconductance on saturated drain current

fitted nicely into a single straight line with a slope of 0.7. This means that g_m is proportional to $I_{ds}^{0.7}$. Taking away the expected square root dependence on I_{ds} as indicated in equation (3), the remaining 0.2 power dependence must come from μ. In order to find out more explicitly whether μ is basically dependent on carrier concentration or on the gate electric field, we conducted experiments using a specially constructed double-gated TFT structure. This structure has two identical but independent gates on the top and bottom sides of the semiconductor. Results of the saturated drain current I_{ds} as a function of gate voltage are shown in Figure 5 for each individual gate alone and for both gates together. It is noted that the two individual gates yield a single curve with identical characteristics with respect to each other, as expected. With both gates tied together as one gate, an identical curve should be obtained, but displaced either horizontally or vertically or both. The manner in which the double-gated curve is displaced from the single-gated curve would be quite different based on whether the carrier mobility is voltage or concentration dependent. If μ were strictly voltage (or electric field) dependent, the net effect of both gates together would simply double the drain current of the single-gated case at the same gate voltage. On the other hand, if μ were concentration dependent only, then only half of the gate voltage (for both gates together) would be required to obtain the same drain current as in the single-gated case. Close examination of the results in Figure 5 clearly indicated the latter behavior. We can conclude unambiguously that μ is only dependent on carrier concentration and not on the electric field. The observed dependence of g_m on V_g is

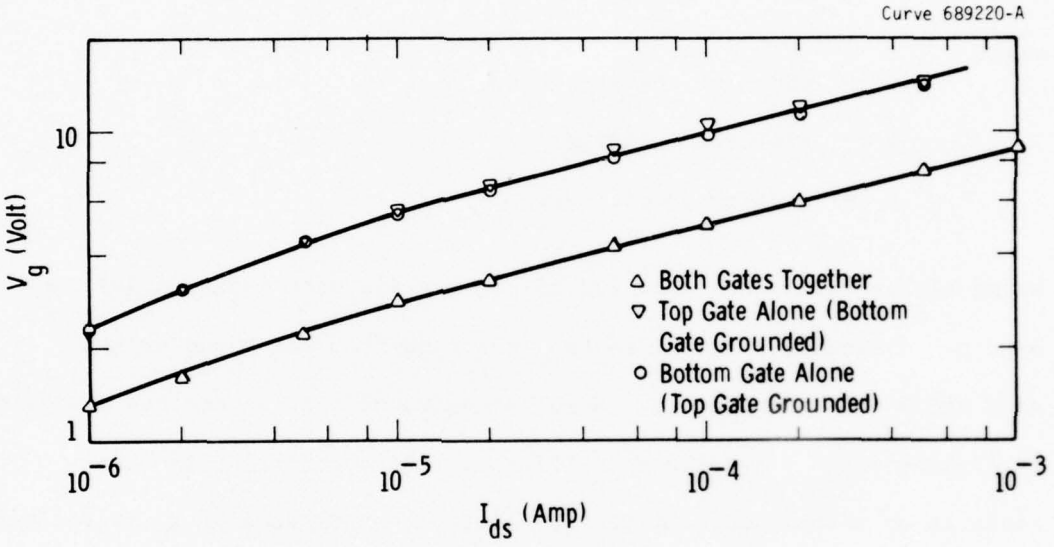

Figure 5. I-V characteristics for a double-gated TFT

then only due to the implicit dependence of carrier concentration on V_g.

In order to relate μ to the carrier concentration, we measured, for a given gate voltage, the values of g_m and the conductance G_o of the device near the origin of the $I_{ds} - V_{ds}$ curves. G_o can be expressed as:

$$G_o = \frac{w}{\ell} q\mu n \qquad (4)$$

where

w = width of the TFT channel

q = electronic charge

n = carrier density ($\#/cm^2$)

Using either equation (2) or (3) in conjunction with equation (4), we have two unknowns, μ and n, in two equations from which the values of μ and n can be evaluated. Results evaluated for the devices characterized in Figures 3 and 4 are shown in Figure 6. It should be noted that there is an assumption involved in using the expression of g_m as derived from the constant μ theory to evaluate μ that is known to vary with n. The assumption is that at a given value of V_g (or I_{ds}), μ is essentially constant. Therefore the equations (2) and (3) are applicable at a given value of V_g (or I_{ds}), and the mobility so deduced is the effective mobility, μ_{eff}, under these conditions only. We see from Figure 6 that μ_{eff} increases almost linearly with n. The values obtained here are comparable to values reported by Koelmans and DeGraaff[9] from Hall Measurements. However, we do not expect the same μ,n dependence because of our thin film and of the device structure. If n could be assumed to be uniform

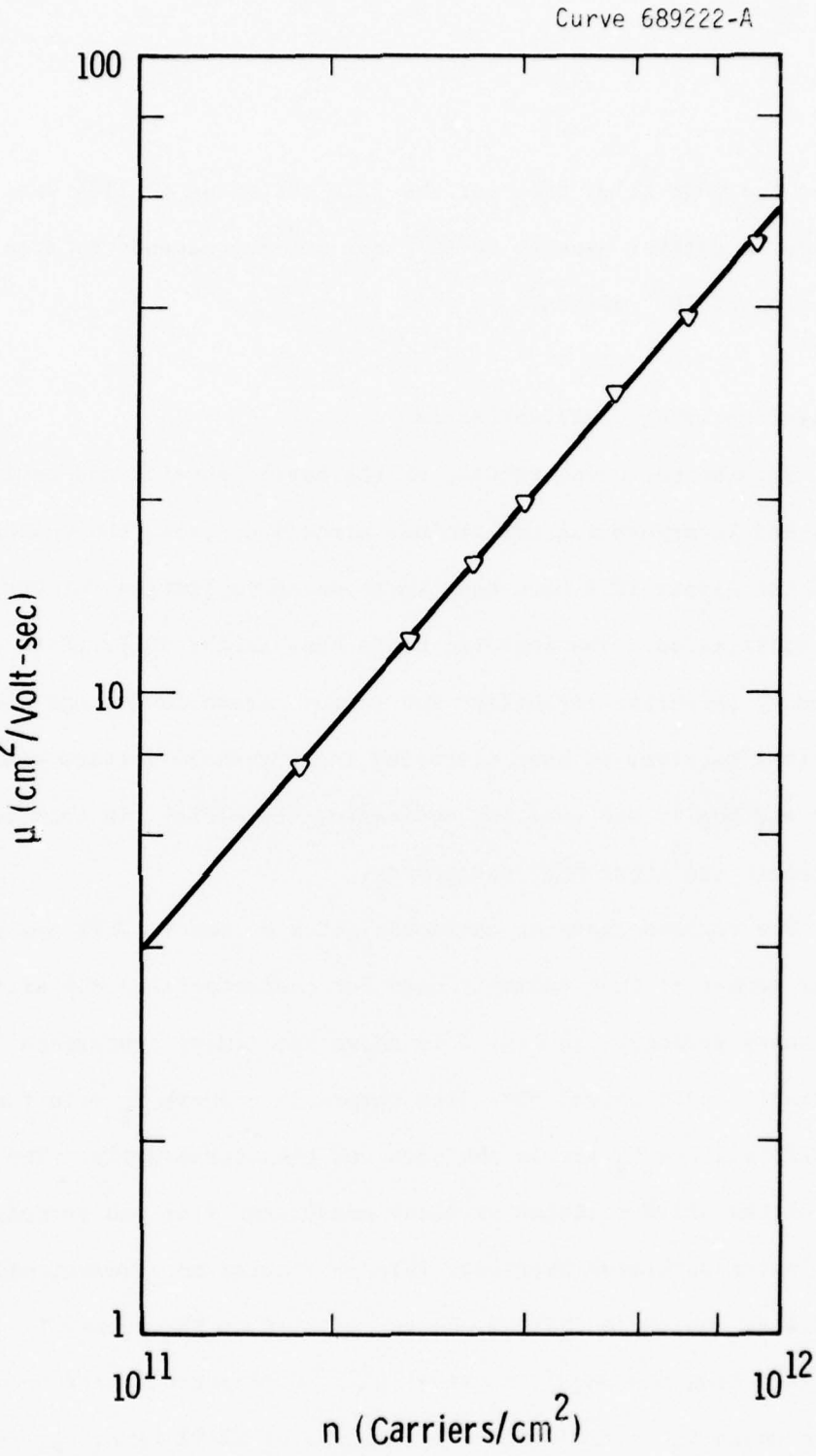

Figure 6. Electron mobility dependence on carrier density for CdSe TFT

throughout the CdSe film, then for the film thickness of 100Å used in our devices, a carrier density of 10^{11} per cm^2 corresponds to a carrier concentration of 10^{17} per cm^3.

B. Memory Transistor Characteristics

With better understanding of the device physics and device material, and incorporating the refined process control, the characteristics of the memory TFTs have been improved and optimized for the intended application. The improved MTFTs have faster WRITE/ERASE speed, better memory retention capability and larger threshold voltage window. In an earlier section, we have discussed the threshold voltage window parameter and how it was used for optimizing the MTFTs. In this section, we will report the other MTFT parameters.

The various charging characteristics of memory TFTs are measured in similar manner as that commonly used for characterizing the silicon MNOSFET memory devices. In Fig. 7 is shown the memory hysteresis loop characteristics of atypical MTFT with threshold voltage V_T as a function of the WRITE voltage V_W across the gate and the source/drain. The time duration of the WRITE voltages in these measurements is one second, in order to insure saturated charging. This particular measurement will be referred to as the state WRITING characteristics of the memory TFT, as distinguished from the usual transient WRITING characteristics shown in Fig. 8, in which V_T is recorded as a function of WRITE time, t_w, for a given V_W. The static characteristics show good threshold voltage window and an almost symmetric loop behavior, very similar to the silicon MNOS devices.

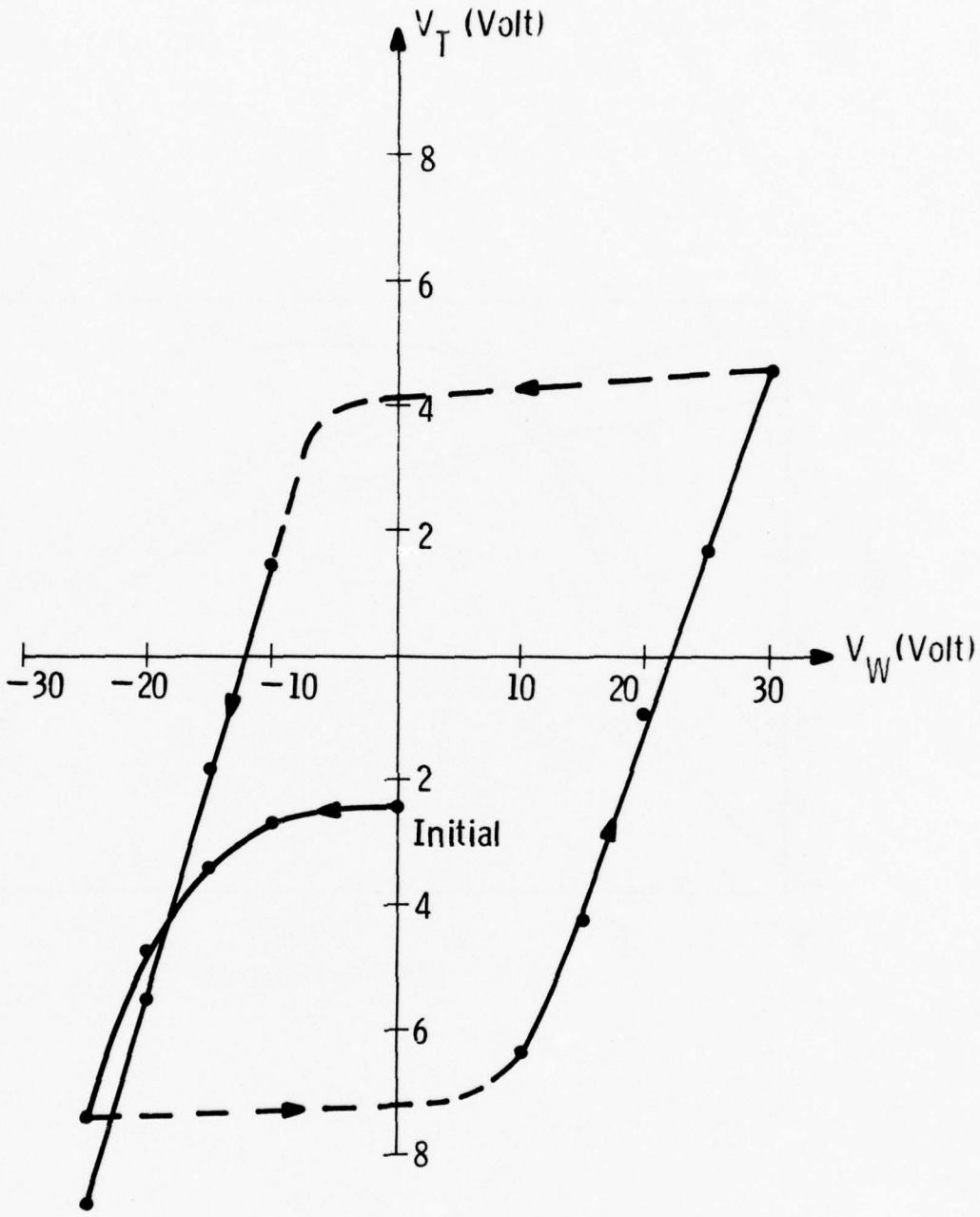

Figure 7. Static WRITE characteristics of a memory TFT. Threshold voltage versus WRITE voltage. WRITE duration = 1 second

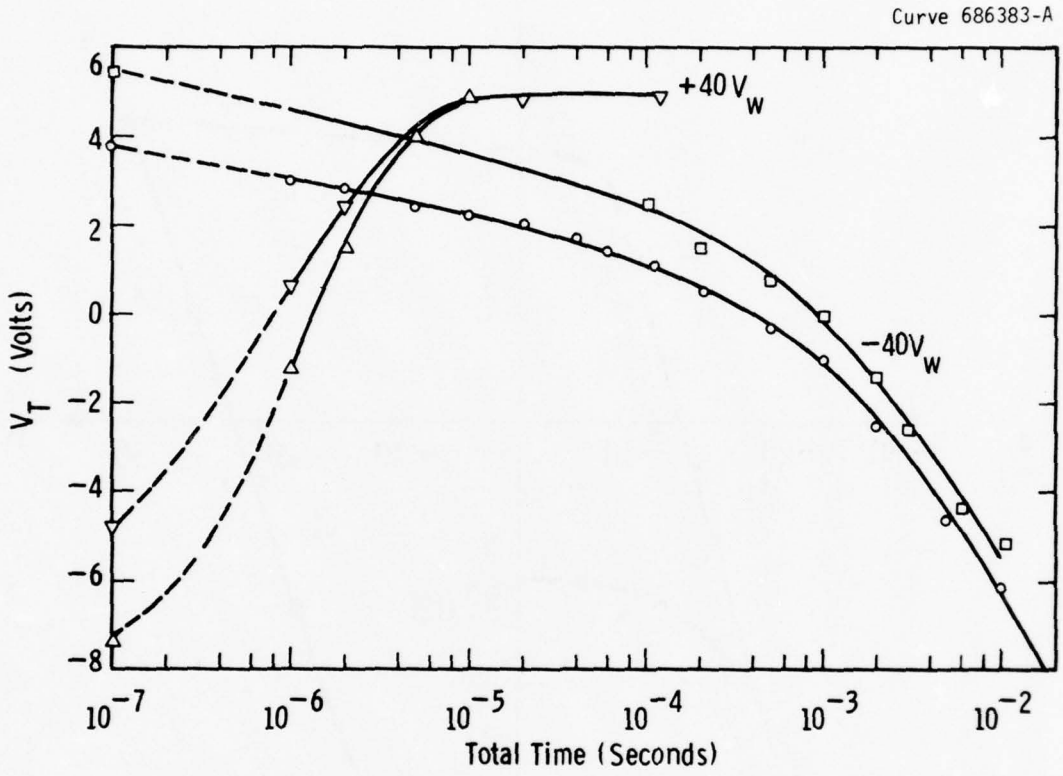

Figure 8. Transient WRITE characteristics of a memory TFT. Threshold voltage versus WRITE time

The transient WRITING characteristics, on the other hand, show assymetrical behavior not usually observed in the silicon MNOS devices. Figure 8 shows two WRITING curves for each polarity of V_W, each starting from a different initial threshold voltage V_{TO}. The two positive V_W curves gradually merge together and the threshold voltages saturate nicely with the WRITING time, just as the silicon MNOS devices. The saturation time of about 10 μs is also comparable to the fast type MNOS devices. The negative V_W curves, however, are quite different. They show no sign of saturation even up to 10 ms. Furthermore, the two curves do not seem to merge together as in the case of positive V_W. Comparing with the earlier results[6,7], the writing speeds have been improved by an order of magnitude in both directions. However, the negative V_W direction is still much slower relative to the positive V_W direction. At the moment, we do not have a satisfactory explanation for all the peculiar negative WRITE characteristics. Several possible causes exist and will be discussed in the following sections.

Generally, there are two schools of thought concerning the charging mechanism. One is that only electrons are involved in the charge transport, and the other is that both electrons and holes are involved. If the single specie model is adopted for MTFT charging, then the slow negative WRITE phenomena could be interpreted as due to the difficulty of removing electrons from the interfacial traps. On the other hand, using the double species model, the same slow negative WRITE phenomena would have to be interpreted as due to the difficulty of transposing holes from the semiconductor to the traps. Aside from these two basic possible causes for the slow negative speed, there

existed other possibilities not directly related to the nature of the traps and the charge carriers. One is that the entire applied voltage is not completely across the gate insulator. The CdSe TFT, being an n-type device, would be turned off completely by the large negative voltage on the gate, resulting in a very large channel resistance ($\sim 10^9$ ohms or more). Therefore, when charge started flowing, a large portion of the applied gate voltage is taken up by the channel resistance. Viewing it differently from the RC time constant consideration, the negative WRITE direction would be much slower than the positive WRITE direction, during which the channel resistance would be smaller by at least 3 orders of magnitude. Another possible cause for the slow negative WRITE could be due to the leakage of electrons from metal gate electrode. These electrons would partially compensate for the electrons leaving the traps, resulting in only a small net loss of electrons.

To gain more insight into the charging mechanisms, we examined the charging current density J of the memory TFTs under various conditions. The charging current density was obtained from the incremental slope of the transient WRITING curve such as that shown in Figure 8, using the following relation:

$$J = C \frac{\Delta V_T}{\Delta t}$$

where C is the capacitance per unit area of the thick gate insulator. For the particular device used in Figure 8, the unit area capacitance is 3.6×10^{-8} farad/cm^2 with a gate area of 1.9×10^{-3} cm^2. The resultant charging current densities as a function of V_T for the two + 40 V_W

WRITING curves of Figure 8 are shown in Figure 9. The interesting point to note is that the data for the two V_{TO} cases all fit very nicely into one single curve. This is in agreement with all the existing charging theories of MNOS devices, regardless of the detailed transport mechanisms. All the existing theories[10] implicitly assume an unlimited supply of carriers for transport across the gate insulator. Consequently the transport mechanism between the semiconductor and the interface traps dominetes the flow of charges. Under such conditions, it follows that for a given WRITE voltage V_W across a given device, the charging current is determined uniquely by the threshold voltage V_T, and is independent of the time of V_W application. This is so because the charging currents is determined by the electric field which is, in turn, determined by the trapped charges or the equivalent V_T. This fact is clearly illustrated in Figure 9. The exact shape of the charging current curve is difficult to anticipate because of its dependence on the detailed transport mechanism of the charges across the various media of the gate structure. However, the general trend of this curve is in agreement with MNOS theories, in that the current is high initially and drops rapidly near the final V_T value. For comparison purposes, corresponding curves for a thick oxide (50 Å) Si MNOS-FET is shown in Figure 10. It is seen that, except for the actual current magnitude, the shape of the MNOS curves for both directions of charging is about the same as that for the $+ V_W$ case of the memory TFT. Results for the $-V_W$ case of the memory TFT are shown in Figure 11. Two major peculiarities should be noted. First is that the data for the

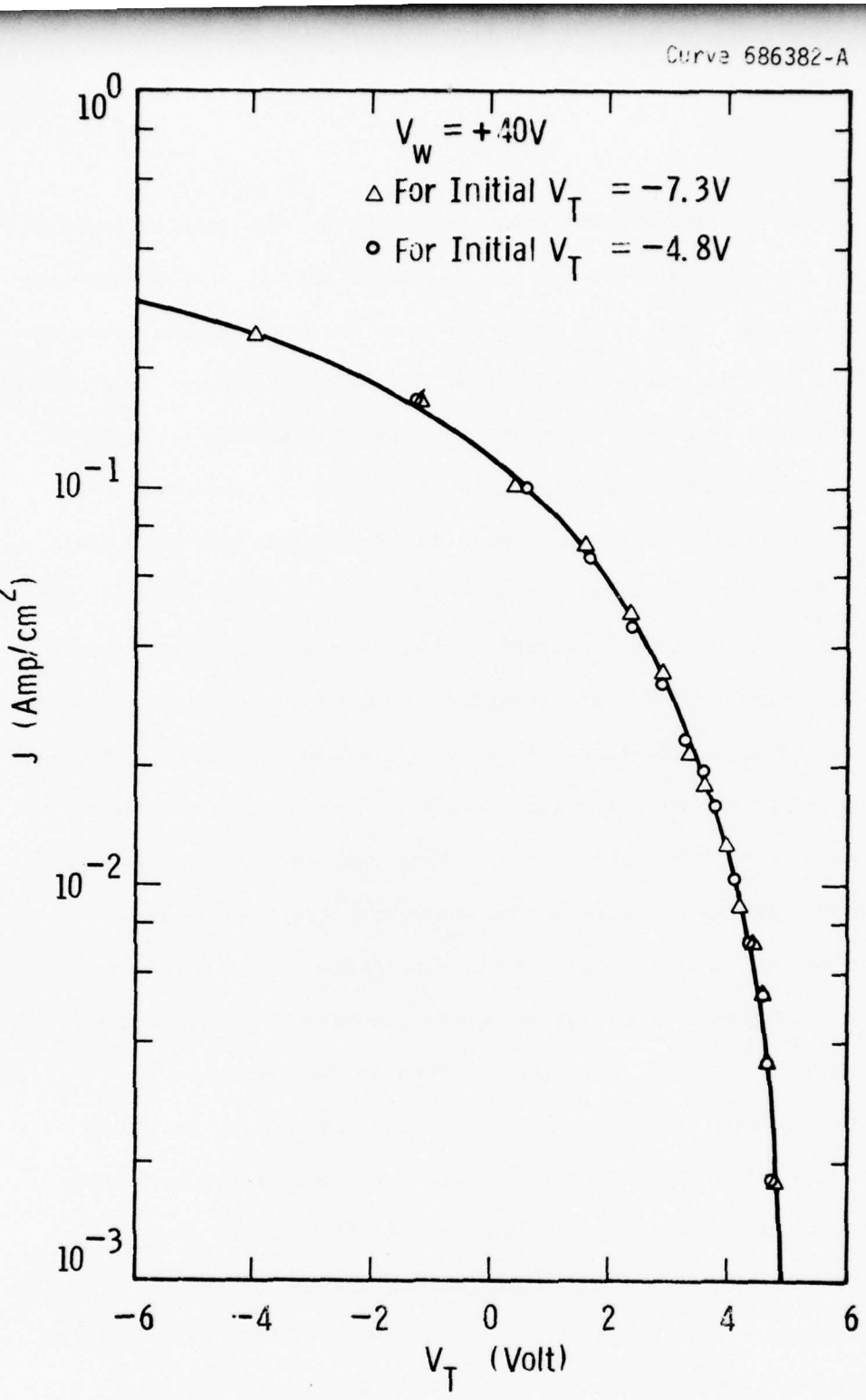

Figure 9. Dependence of charging current density on threshold voltage of a memory TFT for positive WRITE voltage

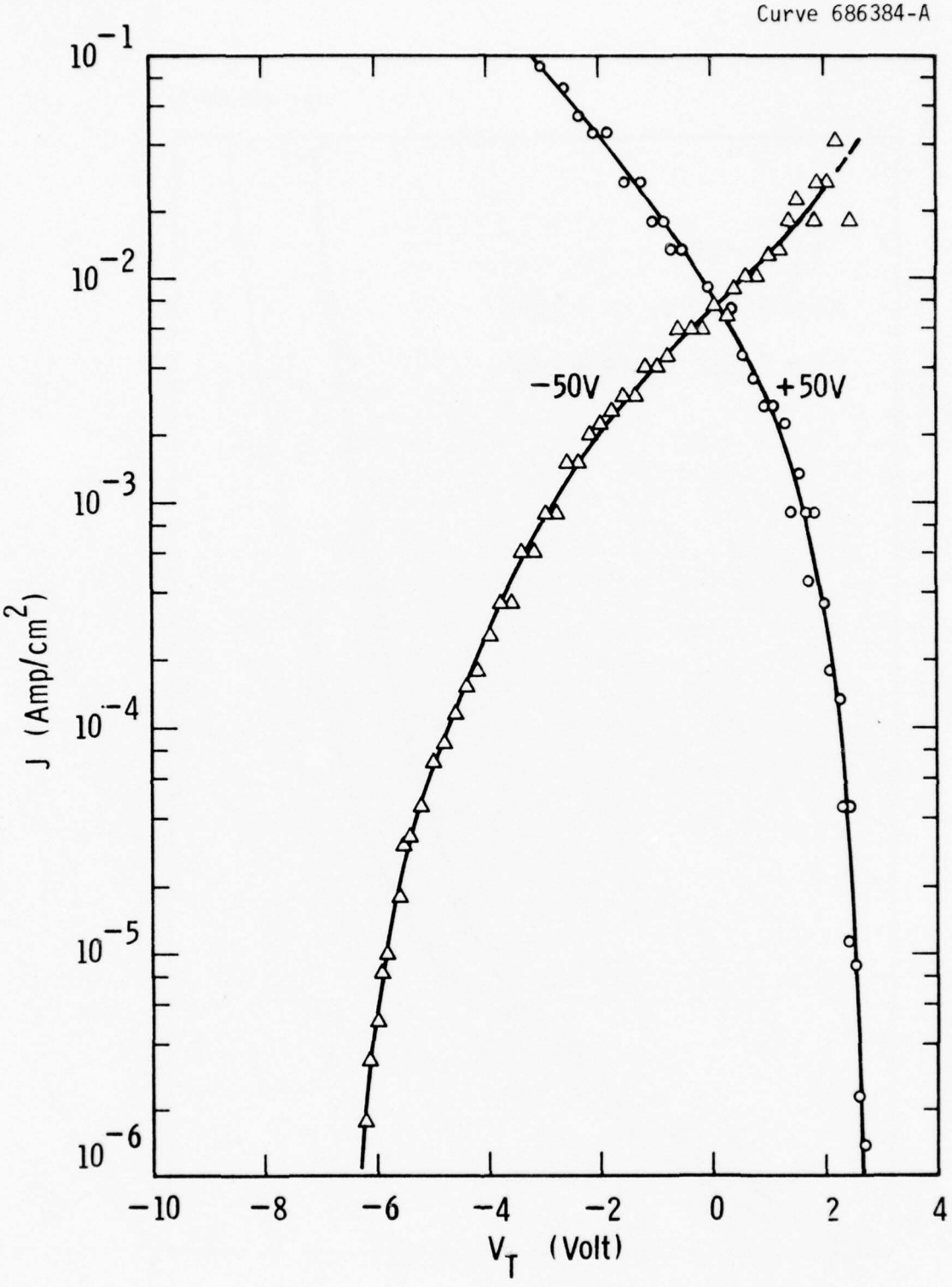

Figure 10. Dependence of charging current density on threshold voltage of a Si MNOS-FET for positive and negative WRITE voltages

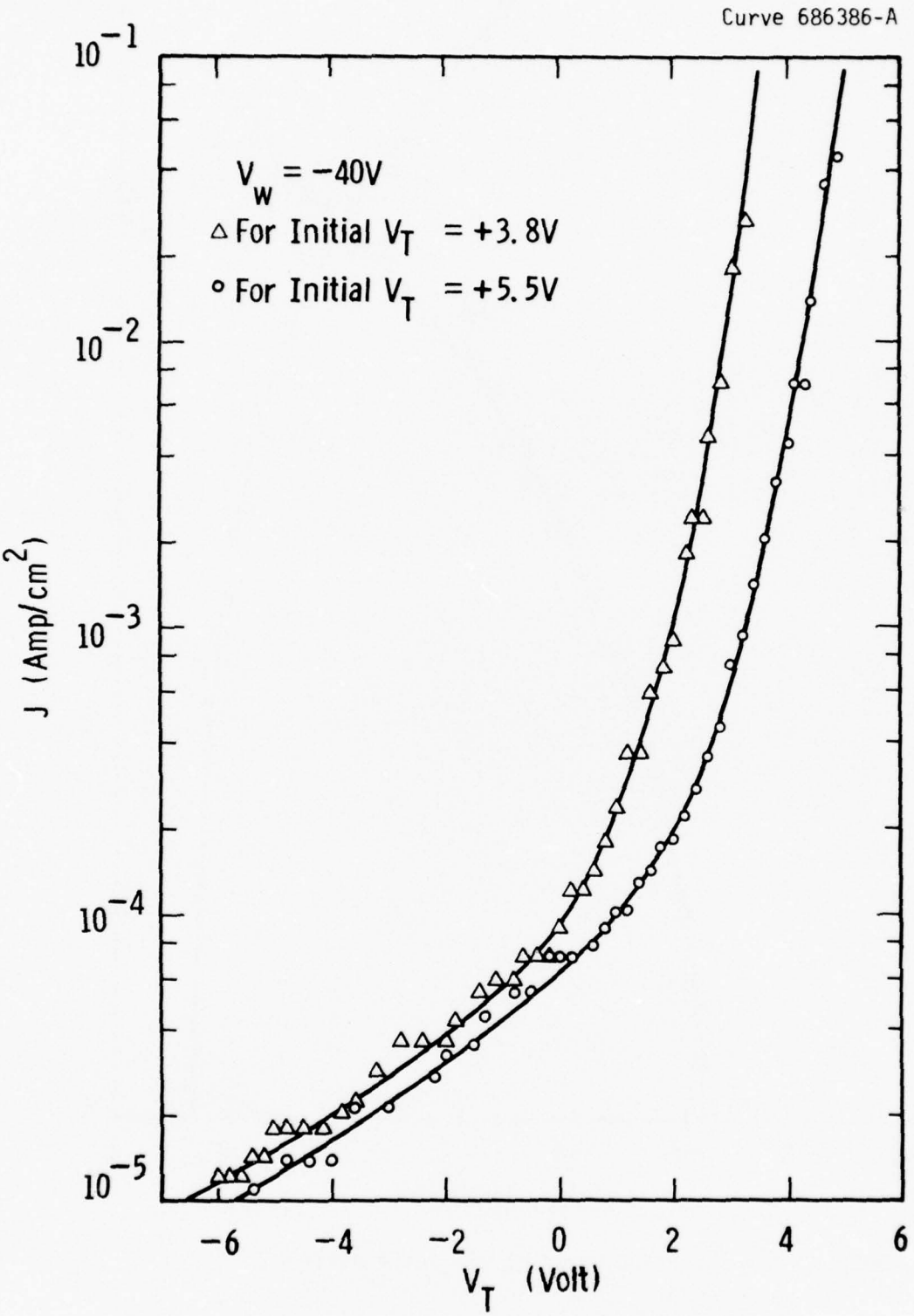

Figure 11. Dependence of charging current density on threshold voltage of a memory-TFT for negative WRITE voltage

two V_{TO} cases do not fit into the same curve as in the $+V_W$ data. Second, the shape of these curves is also different from both the $+V_W$ cases of the memory TFT and the positive and negative WRITE cases of the MNOS device. The rapid initial drop of the charging current accounts for the slow negative WRITE phenomenon exhibited in Figure 8. The fact that the two curves do not coincide indicates that other factor(s) outside of the gate structure is limiting the charge flow, in contrast to the $+V_W$ case where V_T uniquely determines the charging current. Pursuing further, we examined the time behavior of the memory TFT charging current for the $-V_W$ case as shown in Figure 12. The most surprising result is seeing the two sets of data on the same time curve. This fact implies very strongly that an external mechanism (i.e. external to the gate structure, but still within the entire device) constitutes the major impedance to charge flow in the $-V_W$ case. At the moment, we place no special attention to the shape of the curve in Figure 12 other than the near-unity slope of the curve. The time behavior of the memory TFT charging current for $+V_W$ cases is shown in Figure 13 for comparison purpose. As expected, the two V_{TO} cases do not coincide. Again, no special attention was attached to the shape of the curves at the moment,as they depend on the detail charge transport mechanism. The major point to be noted here is that the shape of the $+V_W$ curves is definitely different from the $-V_W$ cases.

At the moment, we do not have a single satisfactory model for all the peculiar negative WRITE characteristics. However, the existing information does allow us to qualitatively weigh the various mechanisms. The fact that we could obtain equal charging

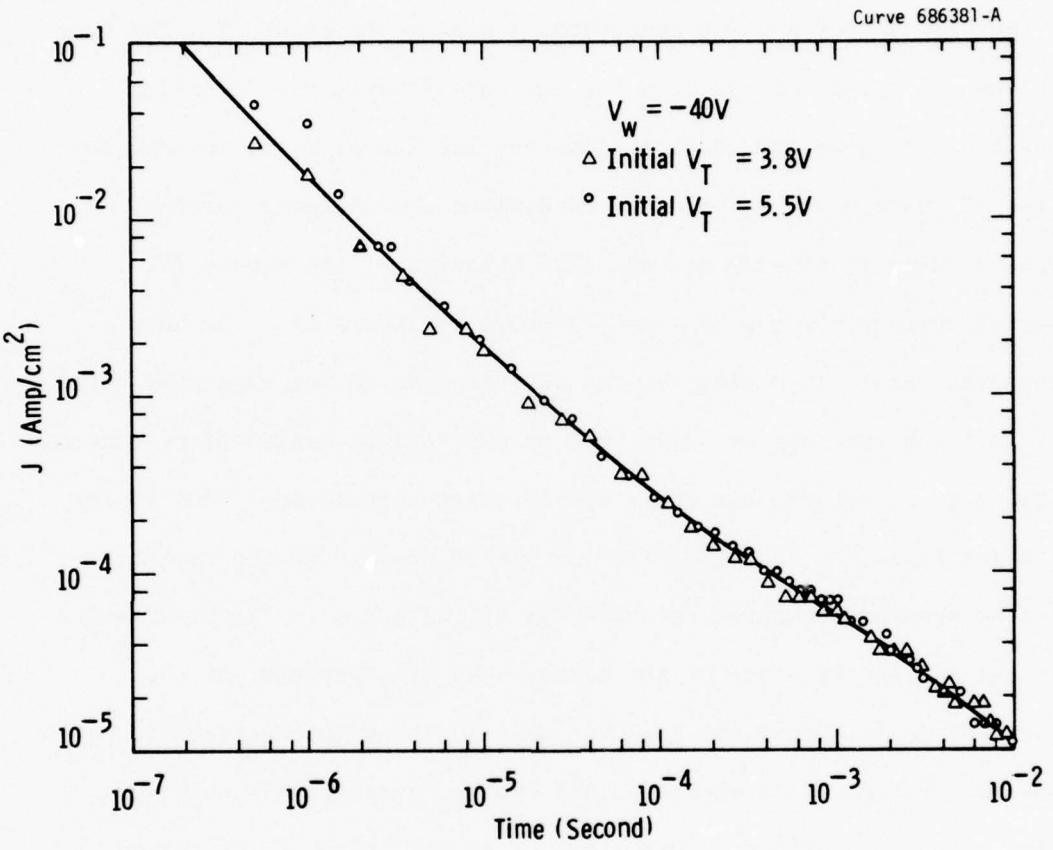

Figure 12. Time dependence of a memory TFT charging current for negative WRITE voltage

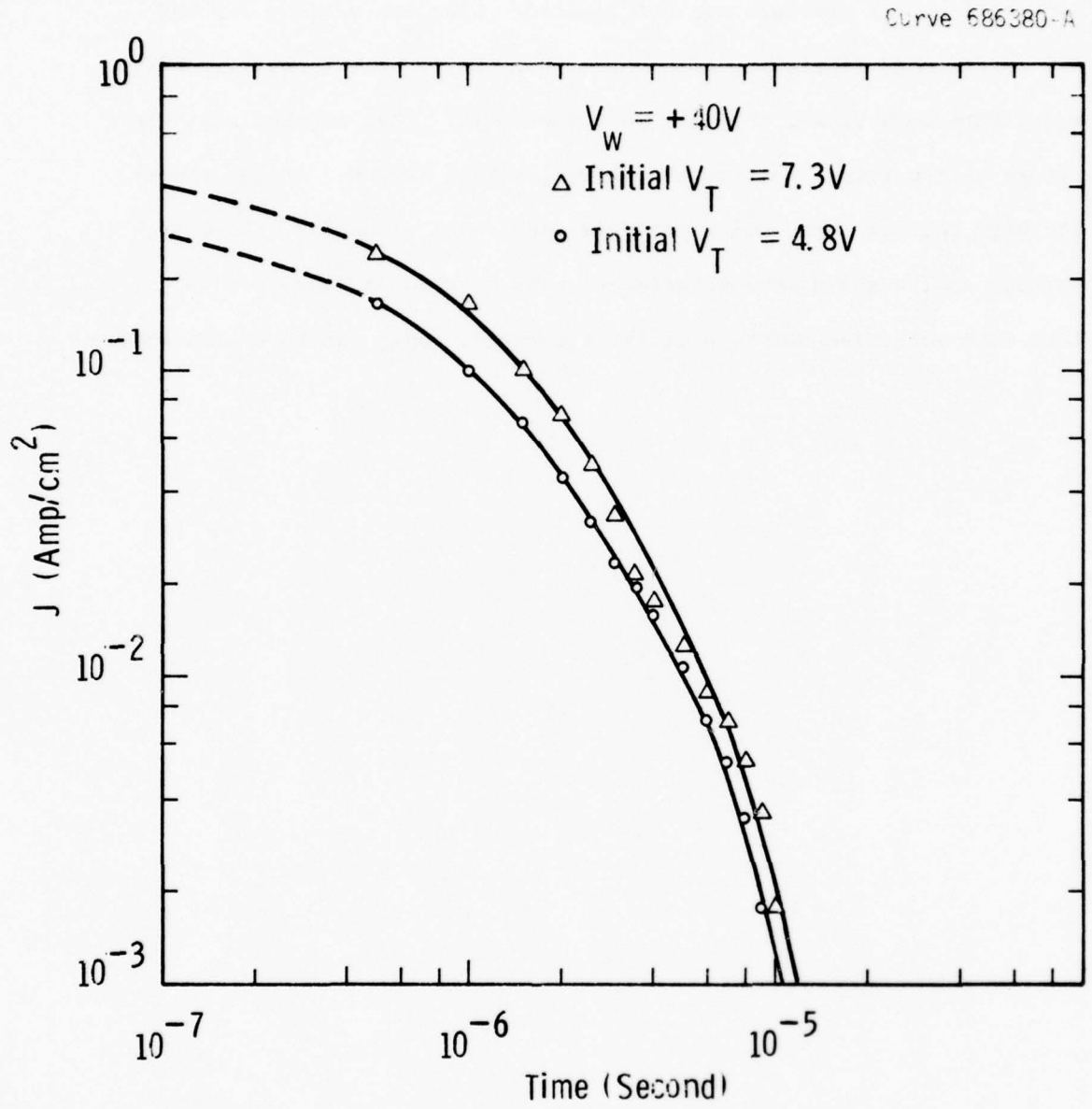

Figure 13. Time dependence of a memory TFT charging current for positive WRITE voltage

in both directions in the static WRITE case (Fig. 7) indicated that the amount of charge carriers was not limited. From the various IFD and SiO experiments (including some gold IFD), the transient negative WRITE was always much slower than the positive WRITE. This implies that the nature of the traps was not the major limiting factor. At the moment, the high channel impedance hypothesis seems most plausible. However, further analyses and more experiments will have to be conducted to test each mechanism before a definite charging model can be established.

IV. 4096-bit Memory

A. Design

The 4-kbit memory design has several aspects: design of the memory cell and memory cell array, design of address and control (i.e., peripheral) circuits, and design of an appropriate test device. During this study, the essential design was carried through the detailed schematic stage for all of these, but only the memory cell, memory cell test array, and test device reached the layout, mask fabrication, and device fabrication and test stages. Recognition of the important bearing which block-oriented operation of the memory would have on its practical utilization has had a continuing influence on our memory design thinking. For example, the relatively simple serial access required in this mode allows the use of serial addressing via shift register circuits - as opposed to address decoding circuits - an especially attractive form of which is the so-called bucket-brigade shift register. The test device which was designed included a 10-stage bucket-brigade as one of the test units, with a view toward determining its potential utility for this and similar thin film transistor circuitry applications. There are numerous other advantages of the block-access mode for the FGTFT memory and they are discussed in the following section.

In the following sections, design considerations for the 4-kbit FGTFT memory as a practical device are presented, followed by a discussion of the control circuit design, and then a description of the test device

and corresponding layout and mask set. Fabrication and tests of the test device are described in the succeeding section.

1. Design Considerations

The selection of a 4096 (64 x 64) memory cell array to demonstrate the FGTFT technology was made so that the resulting device would represent as closely as possible a practical, useful memory. Originally, it was planned to configure the memory as 256 words by 16 bits, but later it was decided to change to 512 words of 8 bits because 1) the 8-bit word length or byte is commonly used in computers and computer peripherals, and is matched to current 8-bit microprocessors which could be used in testing the memory, 2) the package pin count is reduced by 16, and 3) both input and output circuits could be combined on one edge of the device, thereby simplifying the overall circuitry and improving fabrication yield (see Figure 14).

A further major concern was either 1) to improve or 2) to accommodate the relatively slow negative WRITE characteristic of the memory cells, so as to give the memory maximum accessibility. It became apparent that one of the best methods of accommodating the slow negative write is to use the memory in block-oriented applications, wherein the entire 4096 bits can be read or written during each access. Since the contents are changed only during block access, this permits all bits to be negatively written together in a Block Clear action previous to the next WRITE operation, and allows subsequent block writing by word sequence to be confined to the positive or fast writing direction.

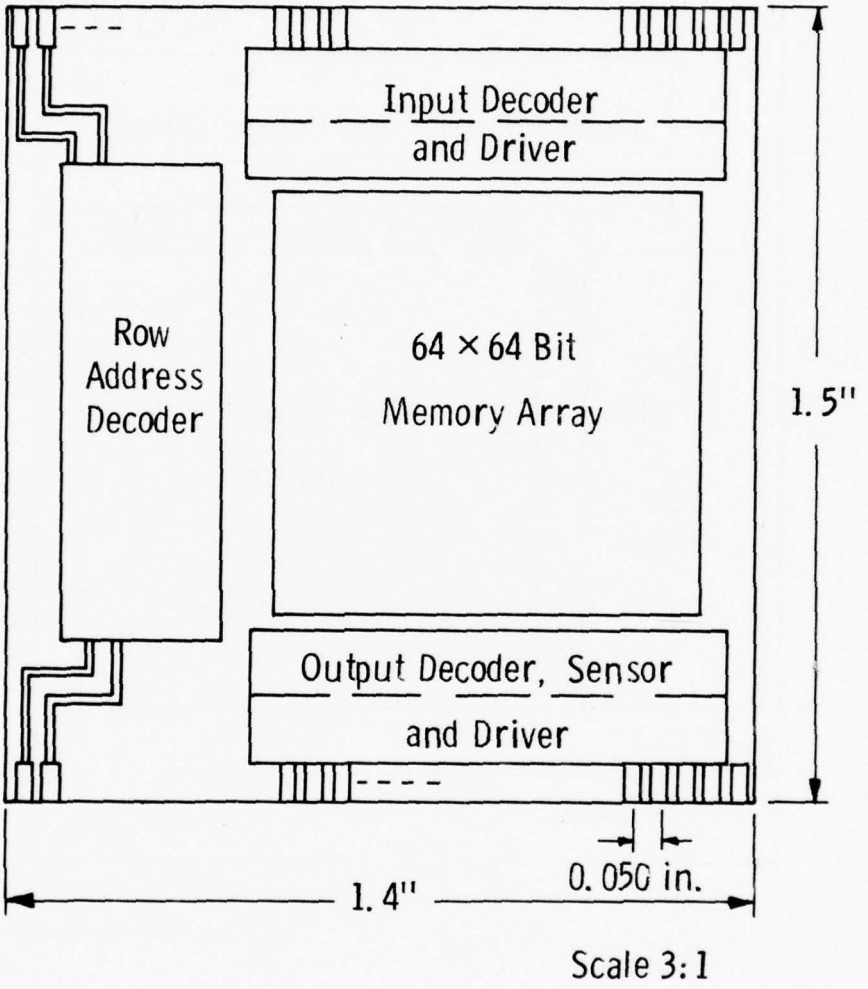

Figure 14. Module placement in 4096-bit FGTFT memory devices -- (a) 256 word x 16 bit

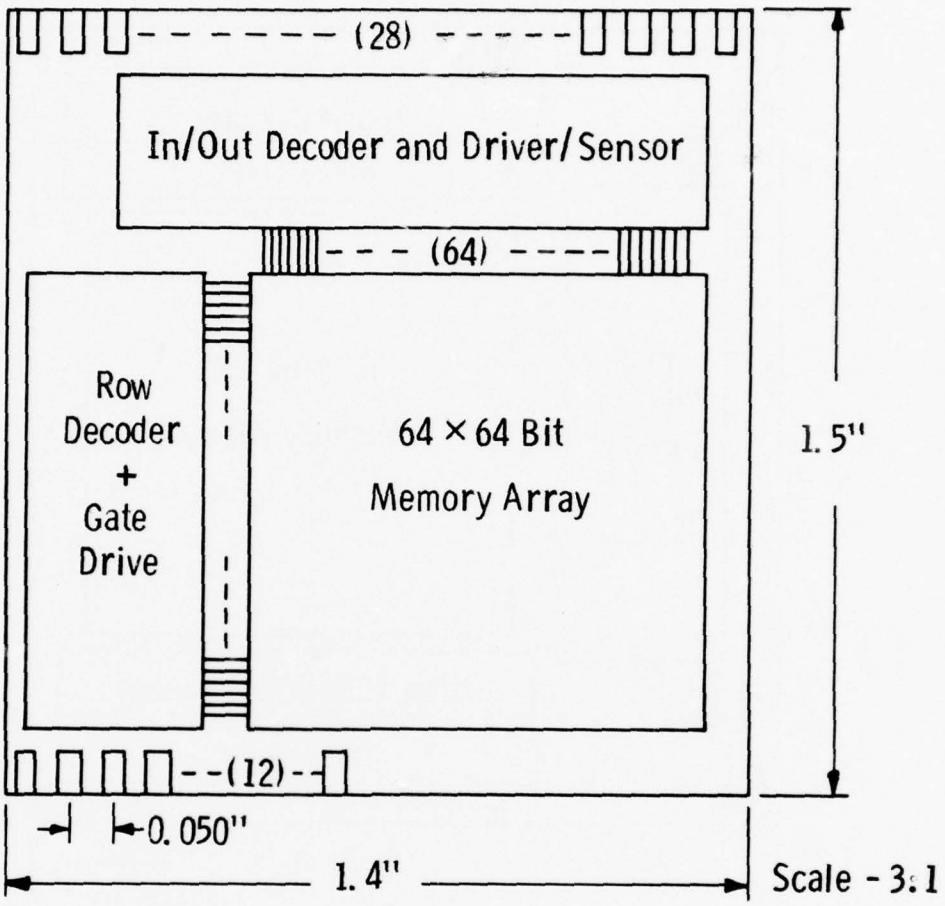

Figure 14. Module placement in 4096-bit FGTFT memory devices -- (b) 512 word x 8 bit

The resulting savings in overall operating time is about proportional to the number of words in the memory block, and with a 512-word block, the 512:1 savings essentially offsets the disadvantage of the slow negative WRITE. To implement Block Clear, the supporting circuitry is designed to permit all cells to be negatively written simultaneously. Figure 15 shows typical WRITE voltages and times required during a) conventional random access operation of the memory, and b) block access operation. The input and output logic levels in the block-access operation can be equal, and the memory array cells get equal READ or WRITE activity. Furthermore, the block non-select operation can be implemented to conserve power, and the serial word access permits the use of low-complexity shift register addressing. A summary of the important advantages of block-oriented usage of the FGTFT memory is given in Table 1.

A third design consideration was to minimize disturbance of non-addressed cells during WRITE and READ operations. In previous, conventional cell addressing methods, the voltage appearing between gate and source-drain, V_{G-SD}, on non-addressed memory cells is one-half the required WRITE voltage, since half of the WRITE voltage is impressed on the gate bus and half on the source-drain buses for the addressed cell. Because of the hysteretic relationship of WRITE voltage to "stored" or memory threshold voltage V_{TH}, illustrated in Figure 7, an appreciable deterioration of the memory threshold voltages of non-addressed cells may occur during these WRITE operations. A method of applying cell operating potentials was conceived in which V_{G-SD} of non-addressed cells is limited to 1/3 the WRITE potential, thereby reducing the effective

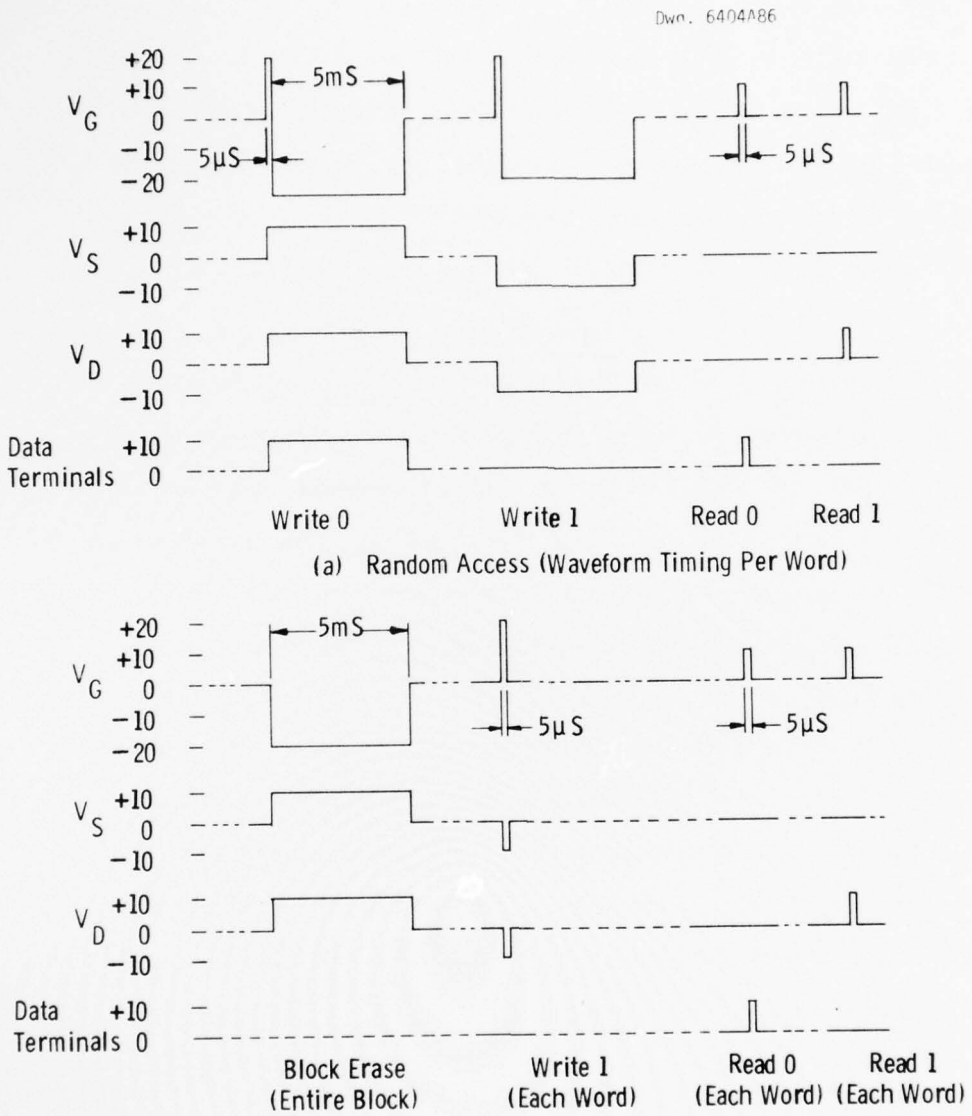

Figure 15. WRITE/READ timing for 512 word x 8 bit FGTFT memory --
(a) Random access
(b) Block access

Table 1

Advantages of Block-Access FGTFT Memory Operation

* Block Clear followed by writing "1"s only is time-economic

* Input and Output logic levels can be equal

* Block Non-select operation can be implemented to conserve power

* Serial word access permits use of low-complexity shift register addressing

* Memory array cells get equal READ or WRITE activity

disturbance to a more tolerable value. The new method is illustrated by the data of Table 2 in terms of the potentials appearing on the various cells of the memory array. A WRITE potential of 30V is assumed. The essential feature of the method is that the gate bus of the addressed row is held at +20V, i.e., 2/3 of the WRITE potential, during positive WRITE, while the source-drain buses of addressed and written cells are held at -10 volts for the remaining 1/3 of the WRITE potential, and all others at +10V. A corresponding procedure, with opposite polarities, is used for negative WRITE. The date of Table 3 show how effective this method is in reducing WRITE-disturb of non-addressed cells. This table, based on the cell memory characteristics for long-duration writing of Figure 7, shows that the conventional writing methods reduces the memory cells's "0" to "1" V_{TH} span from 15.9V to 2.4V which can be sensed only marginally, whereas the improved method reduces this span only to 8.3V, easily sensed reliably by the output amplifiers.

A final design objective which was considered was providing a capability to interface with customary logic levels and supply voltages, and also providing an "on-board" block select function which would effectively disconnect in/out data connections and remove power from the memory block when not being accessed. These objectives were partially met with the present design. As noted in Table 1, operating the memory in a block-accessed mode permits Data In/Out levels to be matched. One of the supply voltages (+25V) is somewhat unconventional, but control/address levels which assume -15V, 0, and +15V potentials are quite easily provided externally. Eventually, additional on-board circuitry could standardize these signal levels. The Data In/Out circuits are compatible with databus operation, and hence a standby, block non-select mode could be implemented fairly easily with modest additional design. However, this function was not provided in the current design.

Table 2

Operating Potentials of FGTFT Memory Cells

Cell[3]		WRITE[1] All 1's		WRITE 1		WRITE 0		READ 1		READ 0	
		NM[2]	LDM	NM	LDM	NM	LDM	NM	LDM	NM	LDM
C_{SS}	V_G	-15	-20	+15	+20	-15	-20	+15	+10	+15	+10
	V_S	+15	+10	-15	-10	+15	+10	0	0	0	0
	V_D	+15	+10	-15	-10	+15	+10	+10	+10	0	0
	V_{G-SD}	-30	-30	+30	+30	-30	-30	+15	+10	+15	+10
C_{SN}	V_G	-15	-20	+15	+20	-15	-20	+10	+10	+10	+10
	V_S	+15	+10	-15	-10	+15	+10	0	0	0	0
	V_D	+15	+10	-15	-10	+15	+10	0	0	0	0
	V_{G-SD}	-30	-30	+15	+10	-15	-10	+10	+10	+10	+10
C_{NS}	V_G	-15	-20	0	0	0	0	0	0	0	0
	V_S	+15	+10	-15	-10	+15	+10	0	0	0	0
	V_D	+15	+10	-15	-10	+15	+10	+10	+10	0	0
	V_{G-SD}	-30	-30	+15	+10	-15	-10	-10	-10	0	0
C_{NN}	V_G	-15	-20	0	0	0	0	0	0	0	0
	V_S	+15	+10	0	+10	0	-10	0	0	0	0
	V_D	+15	+10	0	+10	0	-10	0	0	0	0
	V_{G-SD}	-30	-30	0	-10	0	+10	0	0	0	0

1. 0 = Low impedance state, 1 = High impedance state
2. NM: Normal Mode, LDM: Low-disturbance Mode
3. Cell Designations

	Selected Column	Non-selected Column
Selected Row	C_{SS}	C_{SN}
Non-selected Row	C_{NS}	C_{NN}

Table 3

Write-Disturb Effects in Normal Mode and Low-Disturb Mode Memory Operation

Action	Normal Mode					
	V_{G-SD}	V_{TH}	Δ_{TH} (disturbed)	V_{G-SD}	V_{TH}	Δ_{TH} (disturbed)
Write-1	+30	+ 3.5		+30	+ 3.5	
Write-Disturb	-15	- 1.8		-10	+ 1.5	
Write-0	-30*	-12.4*		-30*	-12.4*	
Write-Disturb	+15	- 4.2	2.4	+10	- 6.8	8.3

*By extrapolation from Figure 7

2. Memory Design

(a) Memory Cell and Matrix

The memory cell design consisted essentially of determining a cell geometry that would give adequate alignment tolerances, element clearances, and memory transistor transconductance within the 320-micron x 320-micron cell confines determined by available space. The latter was set by the maximum overall device size of 1.4" x 1.5" compatible with the available laboratory fabrication system. The cell layout shown in Figure 16 was selected from a number of trial layouts (including ones with interdigitated source-drain electrodes) as having the highest transconductance for a cell with 320-micron center-to-center horizontal and vertical spacings, and accommodating a 15-micron mask-to-mask misalignment tolerance. A 2 x 2 sub-array of these cells is shown in Figure 17, where the numbers refer to different aperture mask levels for the various elements and correspond to mask designations as given in Table 4. An alternative gate mask was designed with gate-to-source/drain overlap reduced from 15 microns to 5 microns to reduce gate capacitance. This was to be used to increase memory operating speed, if sufficient alignment accuracy were achievable.

(b) Peripheral Circuits

In view of the repeated requirement for logic inverters and load transistors in the peripheral circuits, it was decided to include both enhancement and depletion mode N-channel transistors in this circuitry as a means for minimizing current, power, and transistor size

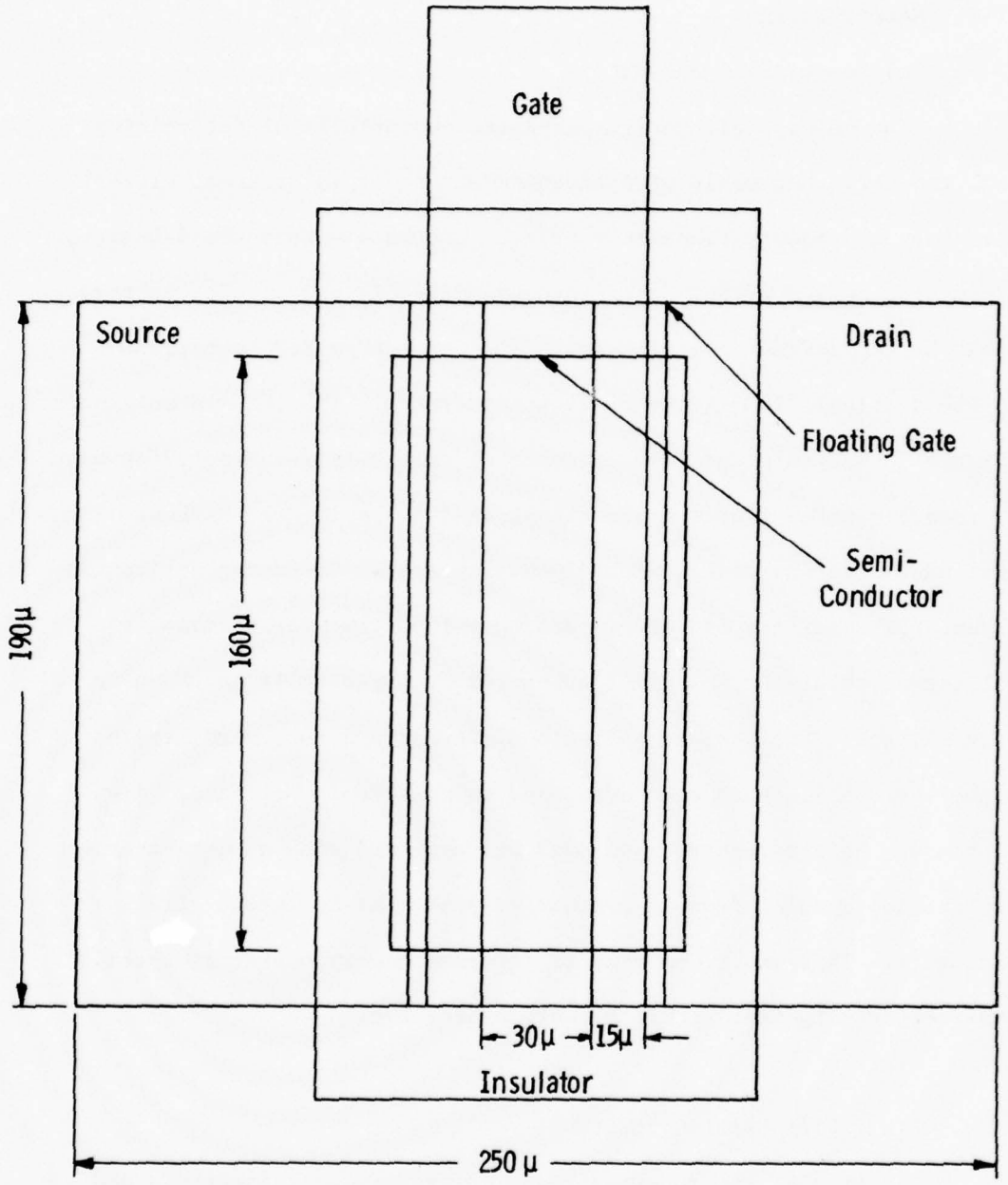

Figure 16. Memory cell transistor layout

Dwg. 6404A87

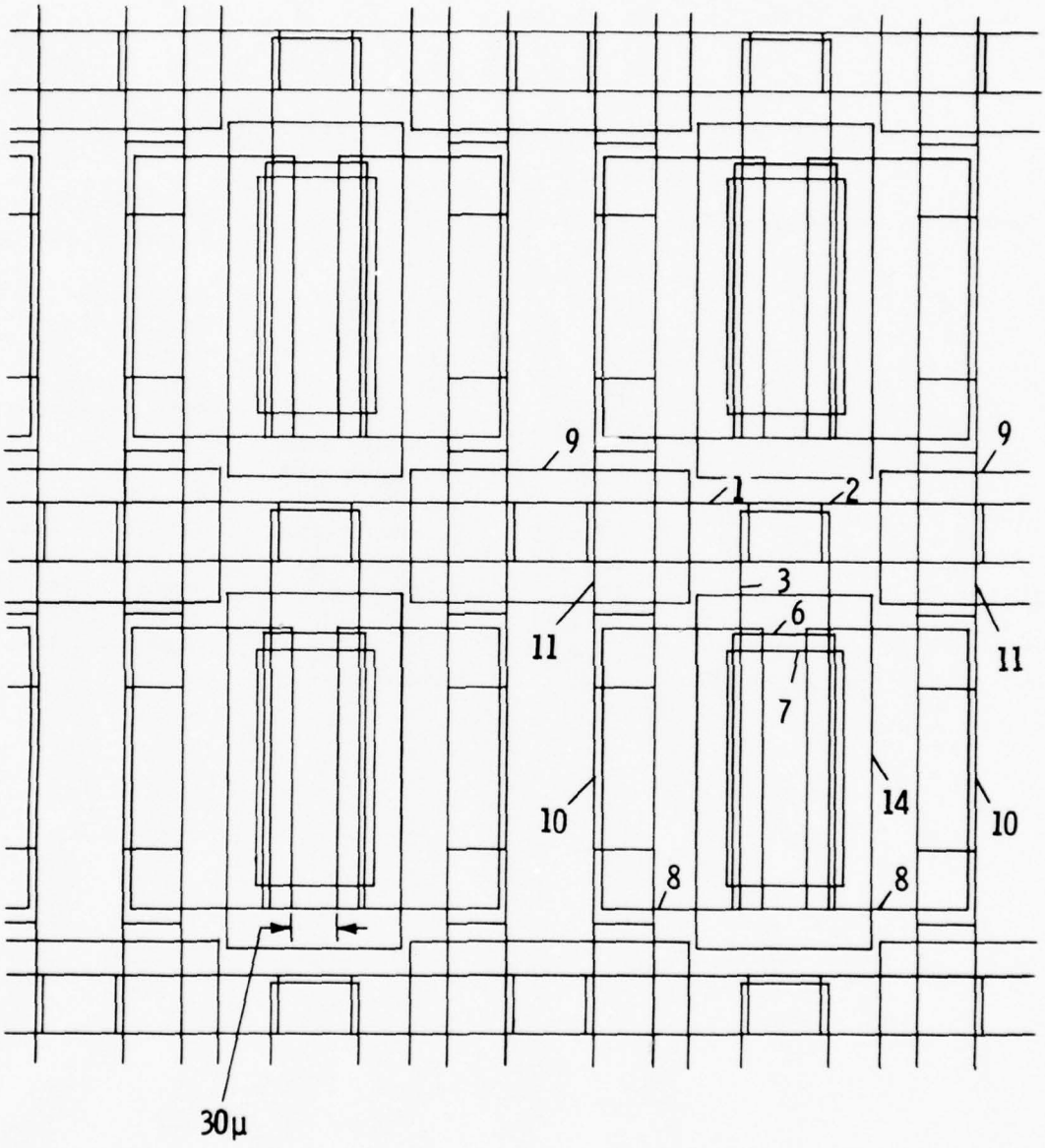

Figure 17. Memory cell sub-array

Table 4

FGTFT Memory Mask and Deposition Identification

Mask No.	Deposition No.	Material	Memory Elements	Circuit and Test Device Elements
1	1	Cu	Hor. Conds. A	Hor. Conds. A
2	2	Cu	Hor. Conds. B	Hor. Conds. B
3	3	Cu	Gate	Gate
4	3	Cu	Gate, Alt.	Gate, alt.
5	4,6,9,11	Al_2O_3		Gate insulator
6	5,10	Al	Floating gate	
7	7	CdSe	Semiconductor	
8	8	CuIn	Source-drain	Source-drain
9	12	Al_2O_3	Crossover ins.	Crossover ins.
10	13	Cu	Vert. Conds. A	Vert. Conds. A
11	14	Cu	Vert. Conds. B	Vert. Conds. B
12	7A	CdSe		Semiconductor, enh.
13	7B	CdSe, In		Semiconductor, depl.
14	4A,6A,9A,11A	SiO	Memory gate ins.	

for equivalent performance or speed. The following two subsections describe the principal control and addressing circuitry developed for operating the FGTFT memory in the new low-disturb WRITE/READ mode as a 512 word x 8 bit block-access non-volatile memory.

(1) Source-Drain Control Circuit

A combined input/output, READ/WRITE control circuit was designed in schematic form, a section of which is shown in Figure 18. The addressed 8-bit word group is selected as 1 of 8 from the 64 columns of memory cells by one of 8 control lines (B_1 to B_8) activated by a 3-bit decoder at one end of this circuit block (but not shown in the figure). This circuit controls the operating potentials occurring on the source and drain electrodes of the memory cells. The On-Off status of the switch transistors in the control circuit and the resulting potentials appearing on the source and drain buses during the WRITE, READ, and Block Clear modes are shown in Table 5. The Data Out line sinks the line to OV for a READ "1" and is pulled to +10V by load transistor T_7 for a READ "0". For databus operation, the +10V bus can be set at OV, resulting in open circuit ouput for a READ "1" (or for block non-select). Also, for databus operation, Data In and Data Out lines can be joined, since the levels are compatible.

(2) Gate Control Circuit

In the 512 word x 8 bit memory, 6 bits of the 9-bit address code are used to address one of the 64 rows in the memory, the remaining 3 bits being used to select one of 8 groups of 8-bit bytes, as described

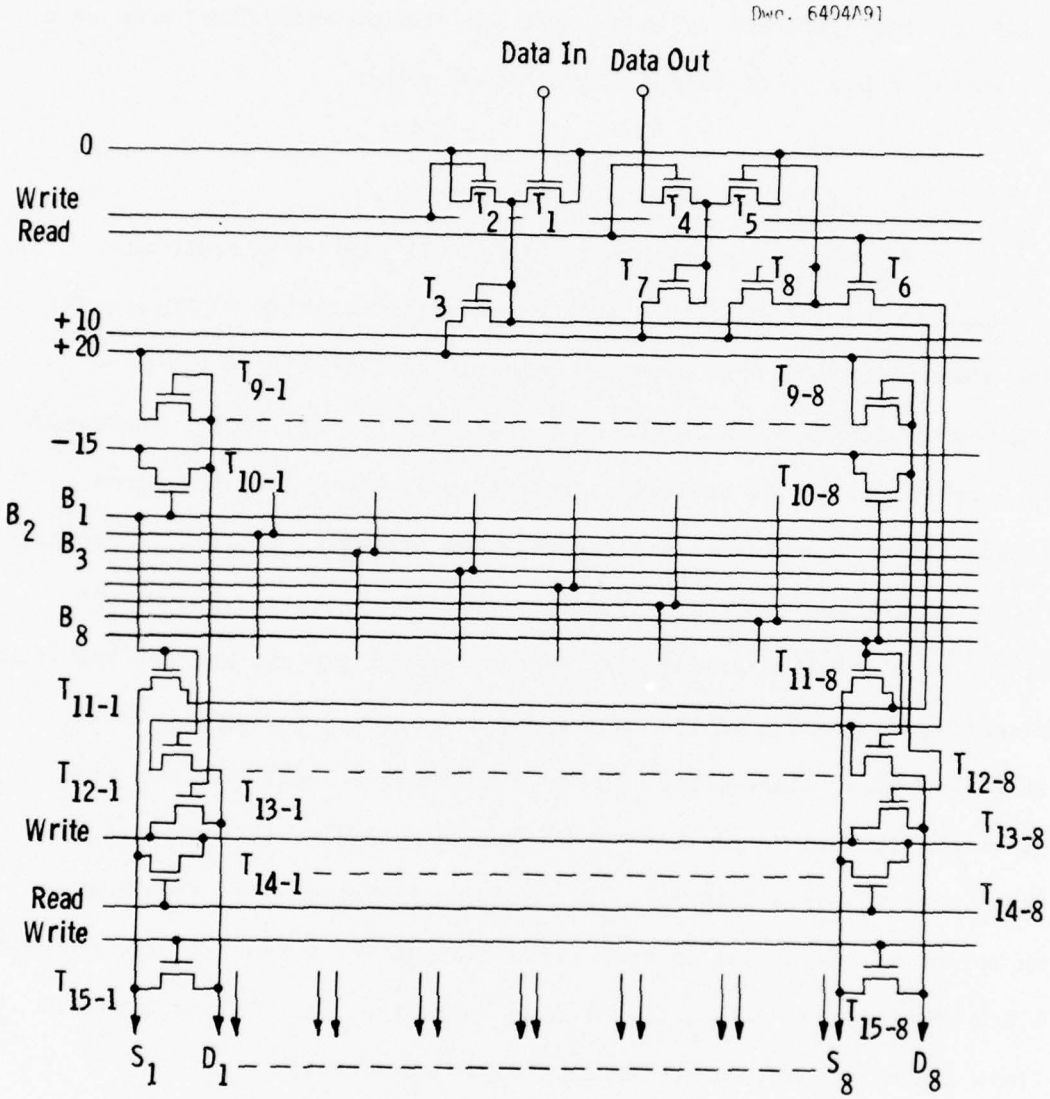

Figure 18. Source-drain control circuit

Table 5

Source-Drain Control Circuit States

	Bulk Clear	Write "1"	Read	Write (Non-select)	Read (Non-select)
T_2[1]	0[2]	0	1	0	1
$T_{4,6}$	0	0	1	0	1
T_{10}	0	1	1	0	0
T_{11}	0	1	1	0	0
T_{12}	0	1	1	0	0
T_{13}	1	0	0	1	1
T_{14}	0	0	1	0	1
T_{15}	1	1	0	1	0
V_S	+10	-10	0	-10	0
V_D	+10	-10	0,+10	-10	0

1. Transistor designations as in Figure 18

2. 0 = non-conducting, 1 = conducting

in the last section. The address decoder and gate control circuit design is unchanged from the beginning of the study, since it was not affected by the change from 256 x 16 to 512 x 8 organization, nor by adopting block-access operation of the memory. The schematic of a portion of this circuit is shown in Figure 19. Inverters to generate the complements of the six address bits A_0 to A_5 would be located at one end of this circuit, and are not shown. Transistors T_0 through T_6 form a shunt address decoder, the selected output line of which connects the addressed gate bus via T_{10} to the Gate Control bus, whereas non-addressed gate buses are connected to the Block Clear bus via T_9, driven by the inverter $T_{7,8}$. The On/Off status of the switch transistors of this gate control circuit and the gate bus voltages in the WRITE, READ, and Block Clear modes are shown in Table 6. During Block Clear, all gate buses are "non-selected", and thereby connected to the Block Clear bus which is driven to -20V during the relatively slow Block Clear negative WRITE operation.

(c) Test Device

In view of the relative complexity of the peripheral control circuits required for the FGTFT memory, it was felt that experience in obtaining satisfactory performance from memory cells in a large array would be advisable before attampting to fabricate the complete device. Accordingly, a test device was designed to permit testing cells embedded in a 64 x 64 memory matrix, as well as transistor and capacitors required for the peripheral circuitry. The layout of this device is shown in

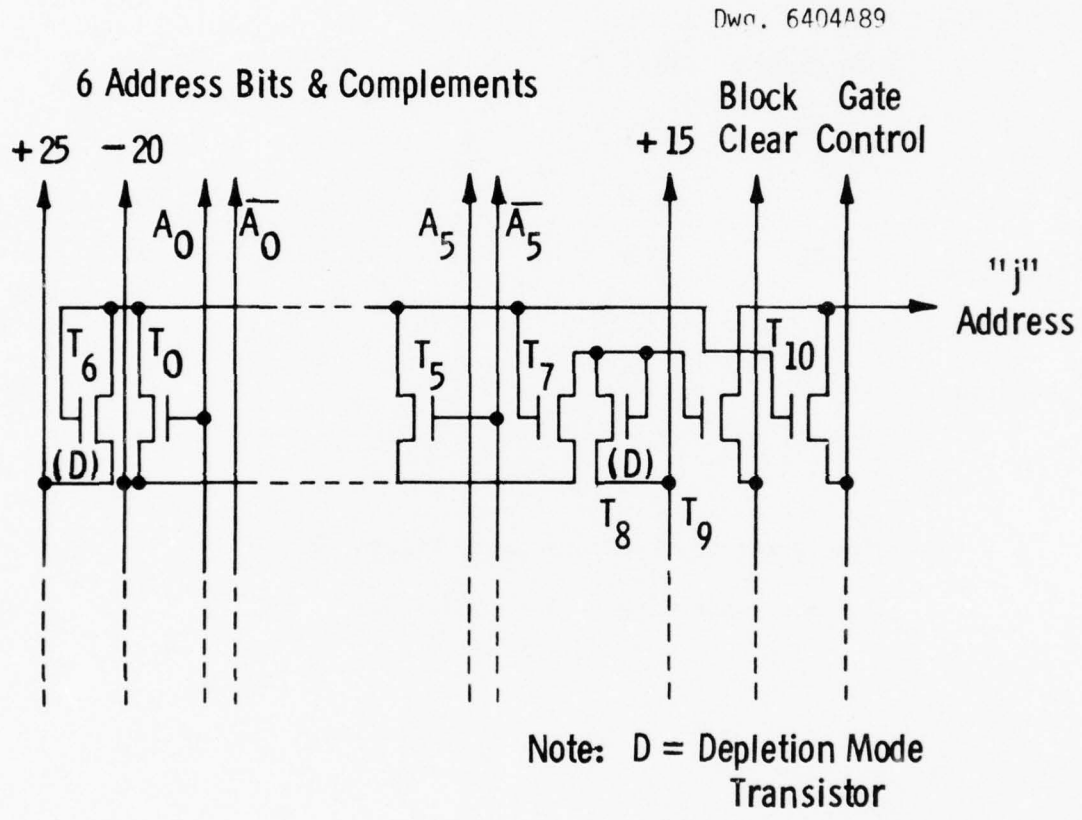

Figure 19. Gate control circuit

Table 6

Gate Control Circuit States

	Bulk Clear	Write "1"	Read	Write (Non-select)	Read (Non-select)
$T_{7,10}$ [1]	0 [2]	1	1	0	0
T_9	1	0	0	1	1
$V_{\text{Block Clear}}$	-20	0	0	0	0
$V_{\text{Gate Control}}$	0	+20	+10	+10	+20
$V_{\text{Gate Bus}}$	-20	+20	+10	0	0

1. Transistor designations as in Figure 19

2. 0 = non-conducting, 1 = conducting

Figure 20. The central square area is for the memory array, while the rectangles at the lower and right edges contain memory test cells, enhancement and depletion test transistors, and capacitors and crossovers for insulation evaluation. In addition, a 10-stage bucket brigade (BBD) test device is included to permit initial evaluation of thin-film BBD's as shift registers for serial addressing of memory, for use in block-accessed memories.

A portion of the test memory cell array is shown in Figure 21. The 64 x 64 cell array is connected to 32 output pads in such a way that an 8 x 4 array of cells is accessible for testing individually, the remaining cells being arranged for parallel testing, having 7-row common gate leads and 15-column common source leads and common drain leads. This permits evaluation of the memory cell behavior within the 64 x 64 matrix, and as well as measurement of bus capacitances, crossover integrity, and population of electrical defects in the 4096-cell matrix. The bottom test area contains two test memory cells, 5 depletion and enhancement mode transistors with various channel widths, and two test capacitors, as shown in Figure 22. Figure 23 shows the second test area, which contains 4 transistors, one capacitor, and the 10-stage bucket brigade shift register. The latter was designed as a tetrode type TFT bucket brigade, but triade BBG action can also be obtained by bypassing with conductive cement the extra transistor in each stage.

The detailed geometric design and layout of the test device, including the aperture mask geometries requried for the various deposition levels, was performed through use of the Applicon interactive graphics

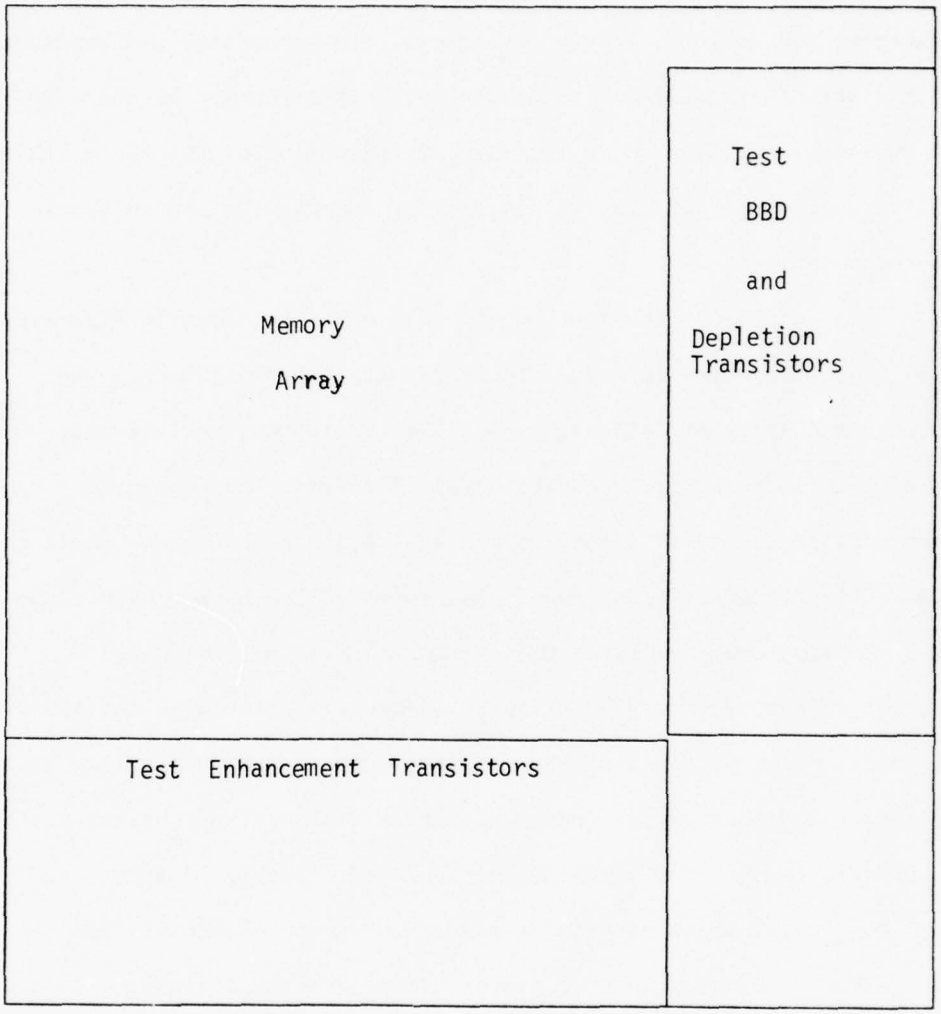

Figure 20. FGTFT memory test device - layout

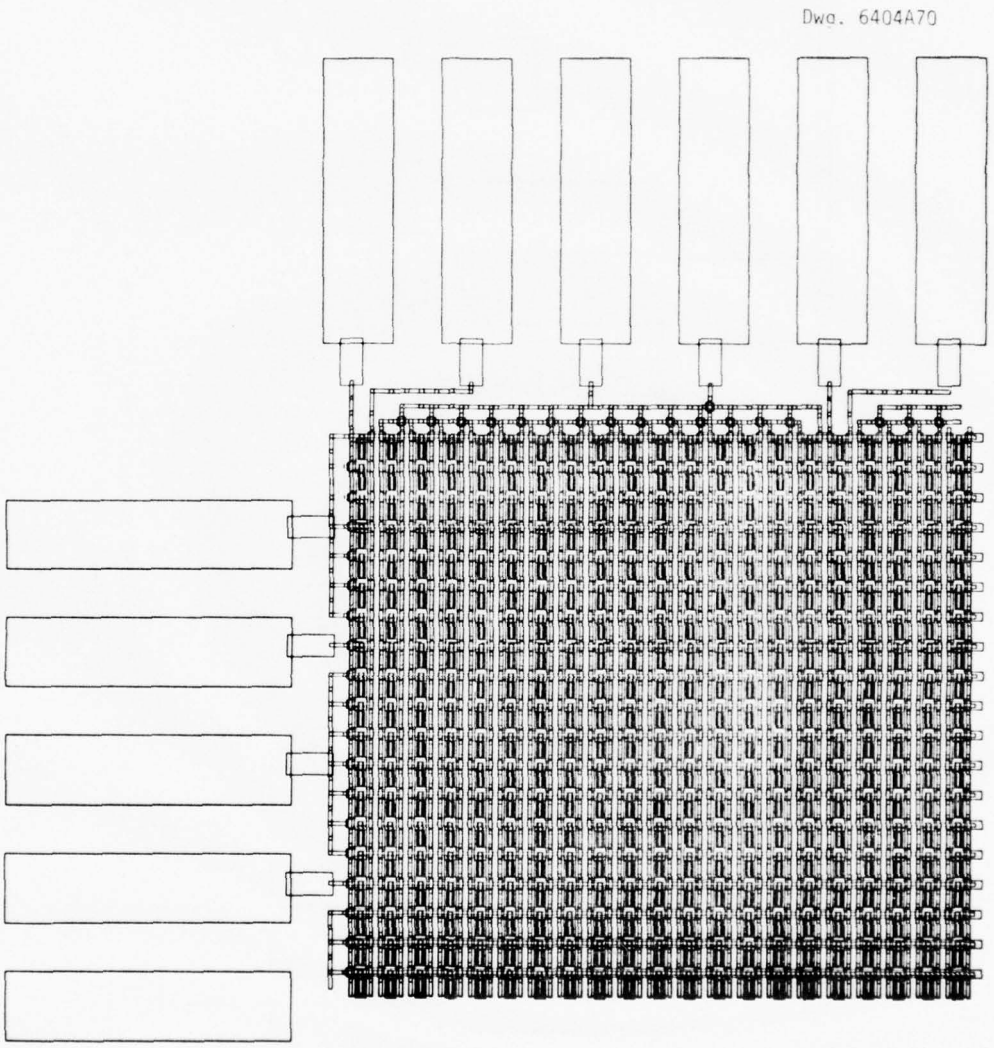

Figure 21. FGTFT memory test device - memory array

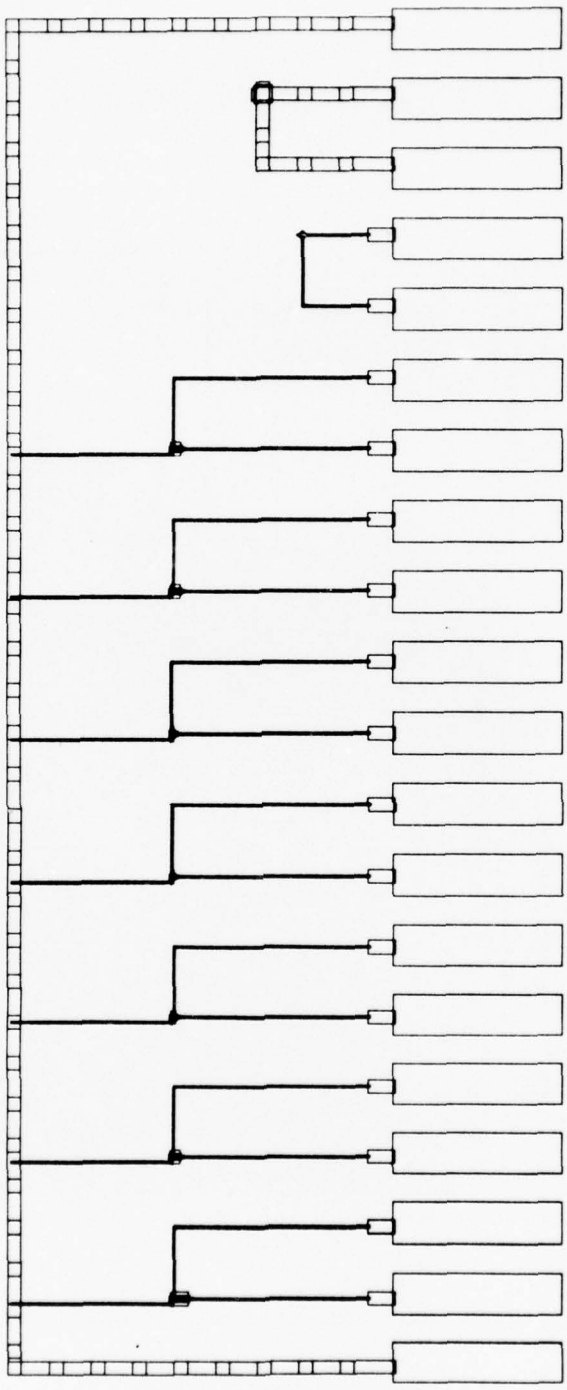

Figure 22. FGTFT memory test device
No. 1 test area layout

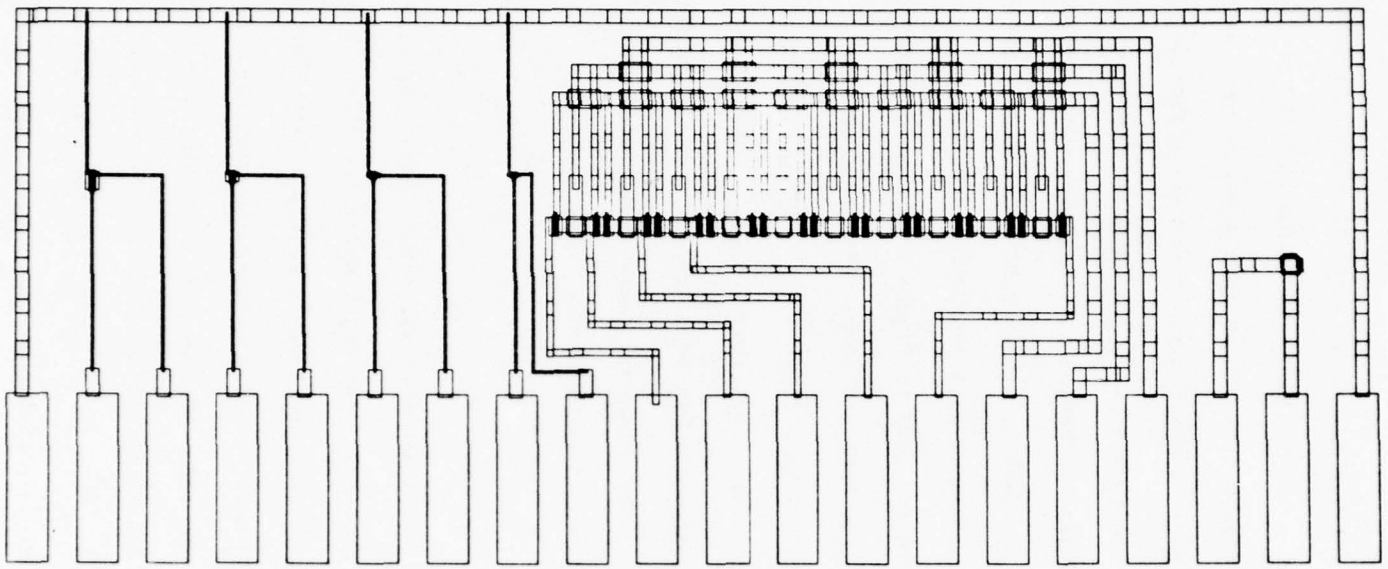

Figure 23. FGTFT memory test device
No. 2 test area layout

layout system. The various mask levels are as listed in Table 4. Care was taken to maintain a high level of mask integrity by providing straight-line webs in both axes across each mask, as well as maintaining a minimum land area gap. Typical circuit element apertures, minimum land area gaps, and work tolerances are given in Table 7. A 14-position alignment pattern, plus orientation key, was located along 2 opposite edges of each mask. On Mask 8, all 14 positions of this pattern were placed so that it could serve as a master alignment mask. A drawing of this alignment pattern is shown in Figure 24. Master photoplates for these patterns using the Applicon output were made on 3" x 3" x .060" high resolution plates at the Advanced Technology Laboratories of the Westinghouse DCES Division in Baltimore, using a David Mann pattern generator. The corresponding set of metal aperture masks, fabricated by Towne Laboratories, Inc., Somerville, NJ, were then used in the test device fabrication, discussed below in Section B.

B. Fabrication

The actual fabrication of the 4-kbit memory array was delayed due to various mask problems. The major delay for almost a month was due to the shut down of the mask maker's manufacturing plant during the summer. When the masks finally arrived, the source-drain mask was over-etched of core material and needed to be replaced. Alignment of the masks was quite a task due to the fine resolution required over a relatively large area. Despite all these problems, we managed to fabricate two good arrays out of only three actual runs. This fact

Table 7

FGTFT Memory Test Device - Aperture Mask Characteristics
(All Dimensions in Microns)

Mask No.	Circuit Element Apertures	Land Area Gap	Typical Tol. ±
*WE-P-760603-1	40 x 210	110	10
-2	40 x 210	110	10
-3	60 x 270	50	5
-4	40 x 270	50	2.5
-5	320 x 320	100	5
-6	70 x 190	30	5
-7	80 x 160	160	5
-8	110 x 170	130	5
-9	90 x 190	130	5
-10	40 x 210	110	10
-11	40 x 210	110	10
-12			
-13			
-14	120 x 240	80	5

*Town Laboratories mask designations

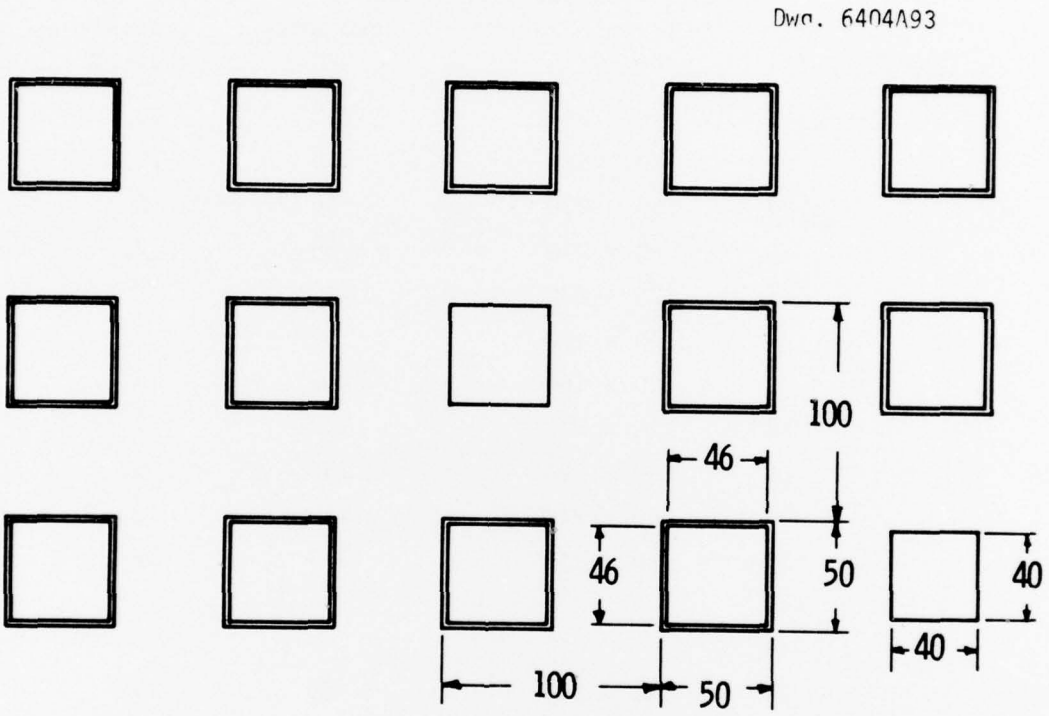

Figure 24. FGTFT memory test device - alignment pattern
(dimensions in microns)

was attributed to the time we had spent on optimizing the device and on improving the various phases of the entire processing procedure. In Figure 25 is shown a picture of the finished array. However, the bucket-brigade shift register test circuit was not complete. As discussed in the design section, the masks were designed in such a way as to obtain either a complete memory array substrate or a complete peripheral test circuit substrate. Due to the lack of time, only the memory array substrates were fabricated. The finished array shows good geometrical resolution and almost perfect alignment. Individual transistor tests show the expected typical characteristics. Figure 26 shows the detailed features of the actual finished array at two different magnifications. The width of the horizontal busbars is 40μ. The vertical busbars appeared wider than 40μ. This was due to the actual mask openings, which we did not have the time nor deemed necessary to replace.

Although we did not have time to fully evaluate the memory arrays the results obtained so far were very encouraging. The fabrication of high density memory arrays over a large area by the thin film technique is now a reality rather than a possible feasibility. Doubling the existing resolution is a certain feasibility. At higher densities, however, mask making problems will be the limiting factor. These will definitely be improved with experience.

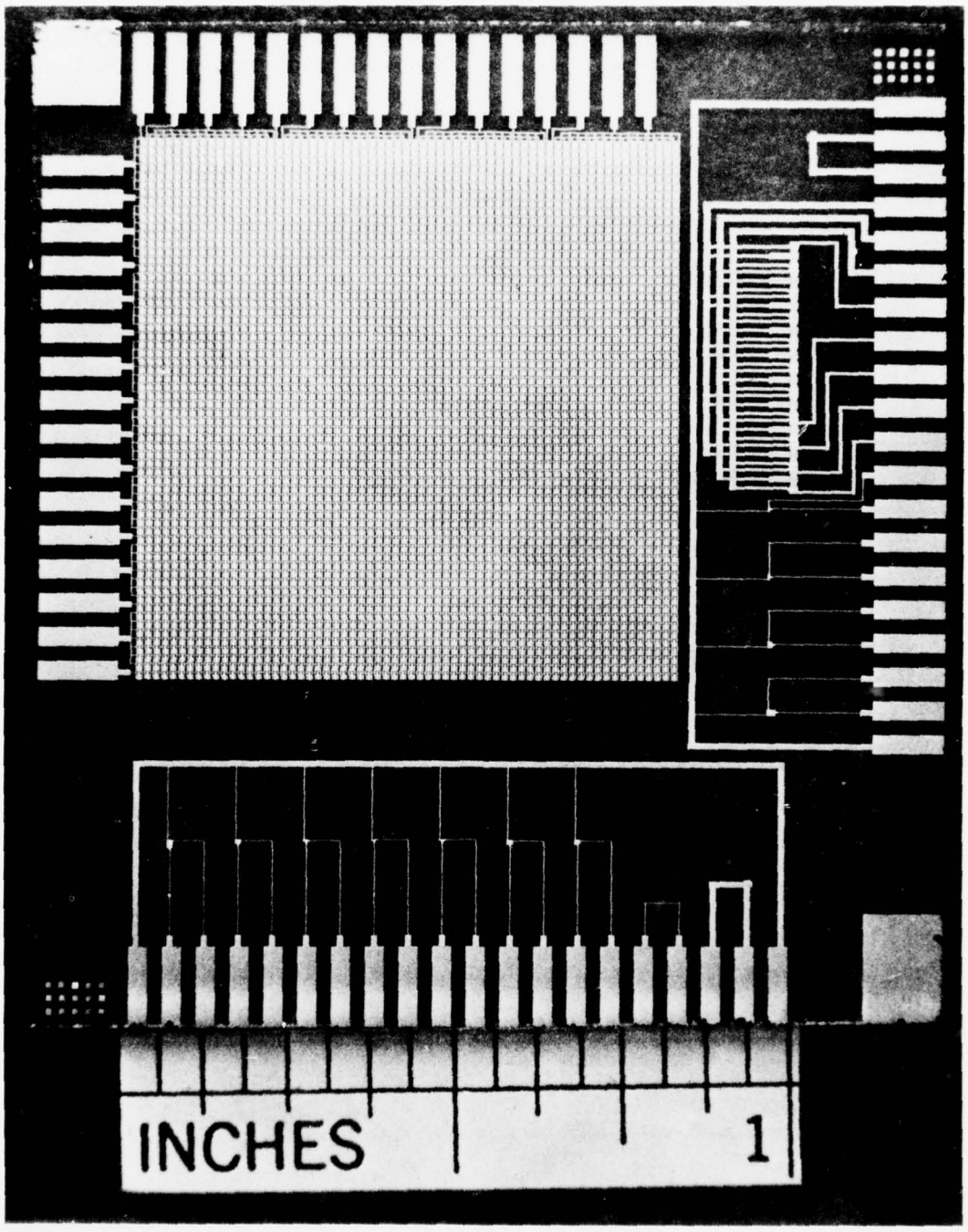

Figure 25. Picture of a completed 4096-bit memory array test device

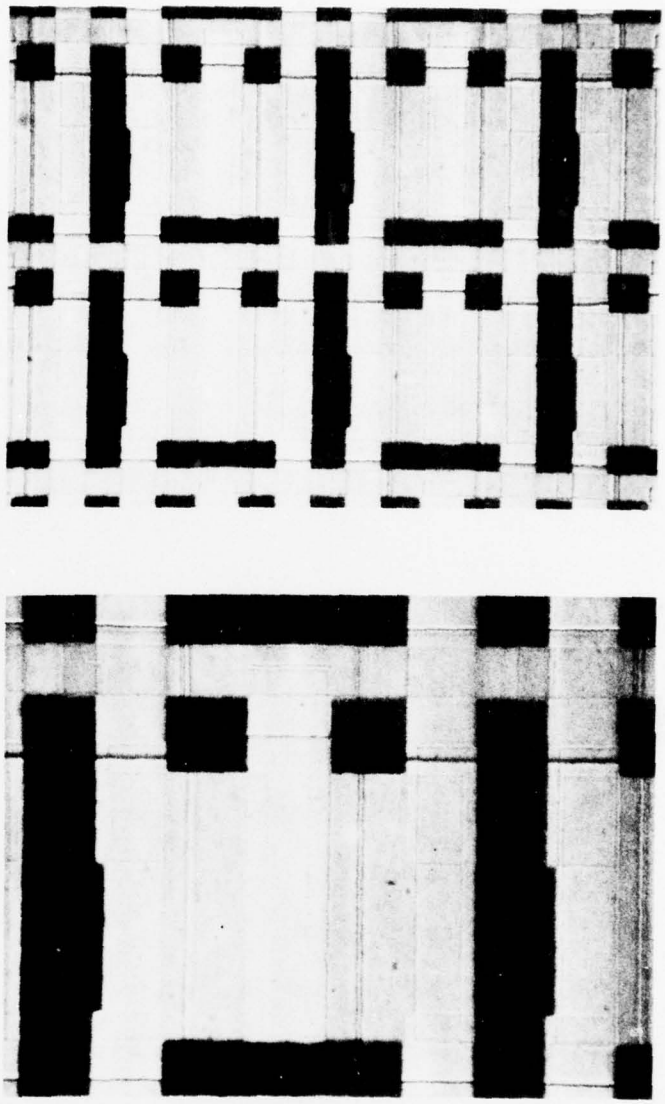

Figure 26. Photo-micrograph of completed cell structure in the memory array at two different magnifications

V. Summary

Major modifications were made on the vacuum deposition system aiming at improved yield, uniformity, control and device characteristics. Rigorous cleaning procedures for masks and substrates were introduced. Heat shields, special adhesive thin coatings, and crucible liners were used to minimize heating, peeling and splattering problems. Various deposition conditions were studied and optimized for best results. In particular, optimum thickness and rate of deposition were obtained for CdSe, SiO, and the aluminum interfacial dopant (IFD). The installation of the specially designed rotating slit was a major improvement. It enabled the controlled deposition of ultra thin layers that eventually led to the optimization of the IFD deposition. The resultant optimized memory TFTs (FGTFT) have more than an order of magnitude improvement in switching speed. The threshold voltage window of the FGTFTs was also improved from about 15 volts to 25 volts.

A large portion of the work was devoted to device physics study. Using a specially constructed double-gated TFT structure, the drift mobility variation of the electrons in CdSe TFTs was found to be dependent only on the carrier concentration. Its apparent dependence on gate voltage was due to the field effect of carrier concentration dependence on gate voltage. Various charging mechanisms were proposed to explain the slow transient negative WRITE characteristics of the FGTFTs. Although time did not permit us to examine each mechanism in

great detail, our results indicated that the nature of the traps was not a major cause. The most probable cause, at the moment, is the high channel impedance of the transistor during the negative WRITE period.

Detailed designs were carried out for the memory cell, memory array, peripheral circuitry, and test devices. The 4096-bit memory was organized as 512 words of 8 bits each, and was designed to operate in the Block-Oriented mode instead of the conventional random access mode. The Block-Oriented operation was considered particularly advantageous for the slow negative WRITE condition of the memory transistor. A special peripheral circuit design allowed only 1/3 of the applied voltage to appear across the non-addressed cells, thus minimizing their disturbance during WRITE/READ operations. The actual memory array itself was arranged as 64 x 64 cells with each cell area measuring 320μ x 320μ . Two complete memory arrays were fabricated with workable memory cells.

VI. Conclusions and Recommendations

The applicability of thin film techniques to the fabrication of large nonvolatile semiconductor memories has been demonstrated. Thin film memory transistors have positive writing speeds and readout capabilities comparable to silicon MNOSFETs, but have much slower negative writing speeds. To a large extent, this slowness can be compensated for by the block organization of the memory, allowing a block clear operation to be carried out simultaneously on all bits within a block (4096 in our case).

More interesting still is the potential for substantial scaling-up of the memory size. Thin film arrays are not subject to the area limitations of silicon IC technology, while being capable (at least in principle) of resolutions comparable to that of silicon. Operating thin film matrix arrays extending over 30 in^2 have already been demonstrated,[11] hence a 512 x 512 or 1/4 million bit thin film memory array, extending over an area of four inches on the side could be visualized. With higher resolution techniques, now under active development, such an area would contain a 1 to 4 million bit, fully decoded, block-oriented memory.

With the very limited time (and funds) available for the present contract, a fully operational memory array was not achieved. However, in a very small number of fabrication runs, fully operable transistors within the array were obtained, and we estimate that with an additional

2-3 months of fabrication experience, a fully operational 4kbit memory could indeed be obtained.

It is often stated that for digital applications, silicon is the only possible technology, and all attempts to generate useful digital structures by other solid state techniques are doomed to failure and should therefore not even be attempted. Like the developers of magnetic bubble memories, we strongly disagree with such a shortsighted and ultimately dangerous philosophy. Such a philosophy may or may not* ensure US leadership in silicon technology, but leaves the country without resources of radical innovation, from which future generations of information-processing systems will necessarily have to come. To say that nothing lies beyond silicon is oddly reminiscent of those who said, a generation ago, that nothing lies beyond miniature, high speed vacuum tubes, except perhaps more vacuum tubes with finer tolerances!

We therefore recommend, with some emphasis, that the Office of Naval Research continues to support exploratory developments like the one described in this report. Any such funding is, at best, negligible compared with the funding (both by industry and by government agencies) going into further elaboration and refinement of silicon technology. We do not claim that the disparity is not justified, but would plead that some finite amount of effort, other than zero, be maintained in areas which are, through the exercise of some imagination, capable of

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*See e.g. "Japan builds semiconductor drive on US Market", Electronics, Feb. 17, 1977.

potential breakthroughs in performance or cost-effectiveness. That thin film transistor technology is indeed such an area has already been convincingly demonstrated by our team in the flat panel display field. Given more time and support, we feel confident that similar giant strides could be made in the field of very large capacity nonvolatile memories.

Acknowledgments

It gives us great pleasure to acknowledge the support of our ONR monitor Cmdr. D. Hanson on the project. We would also like to express out thanks to M. A. Schrock of the Interactive Graphics Department for the actual layout of mask design on the Applicon machine, and to D. Yanda and G. Machiko for their assistance in various phases of the project.

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Webster Research Center
800 Phillips Road W114
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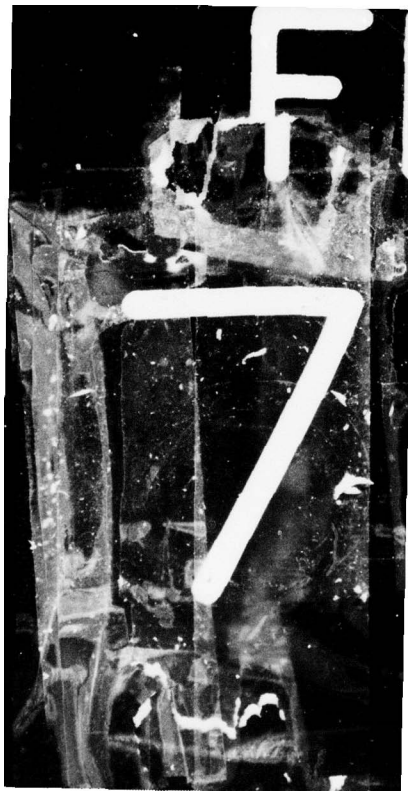
ATTN: J. B. Flannery 1

Tektronix, Inc
P.O. Box 500
Beaverton, OR 97005
ATTN: A. Silzars 1

Sperry Flight Systems
Phoenix, AZ
ATTN: J. R. Trimmier 1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